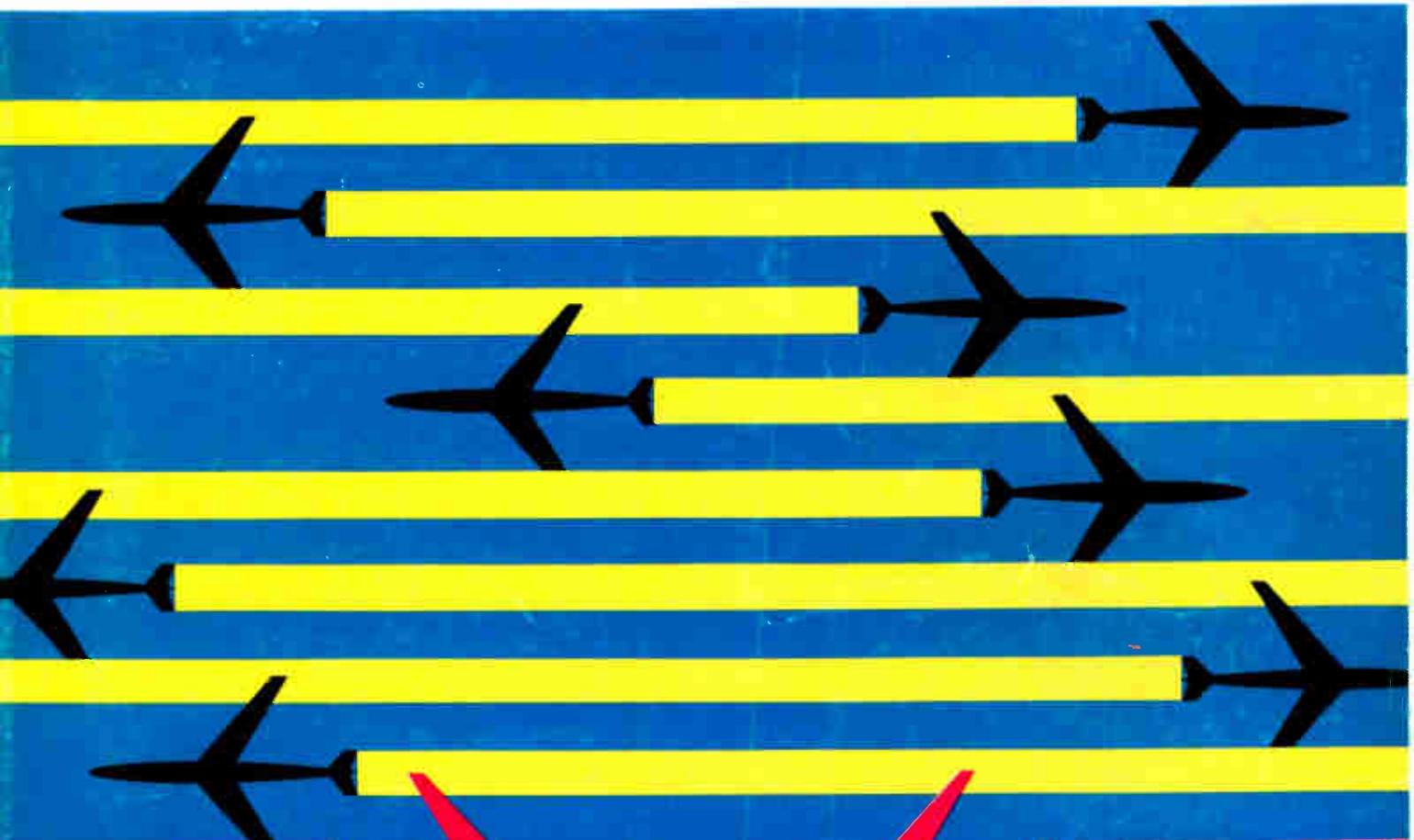


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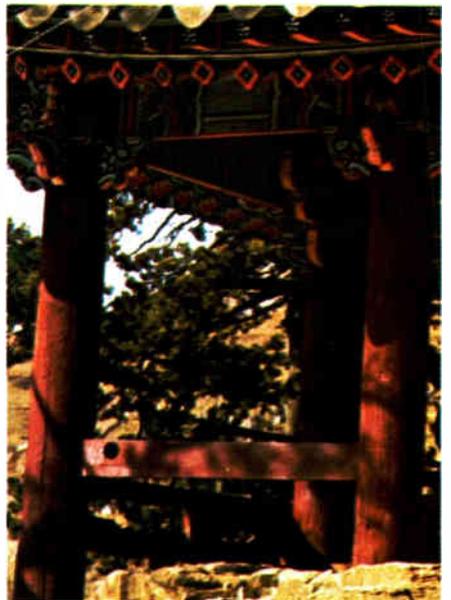
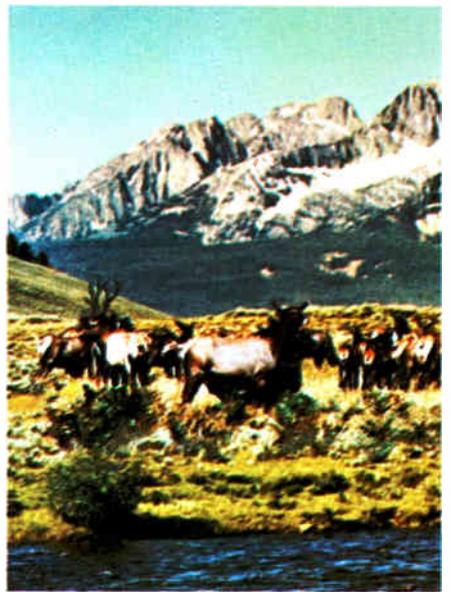
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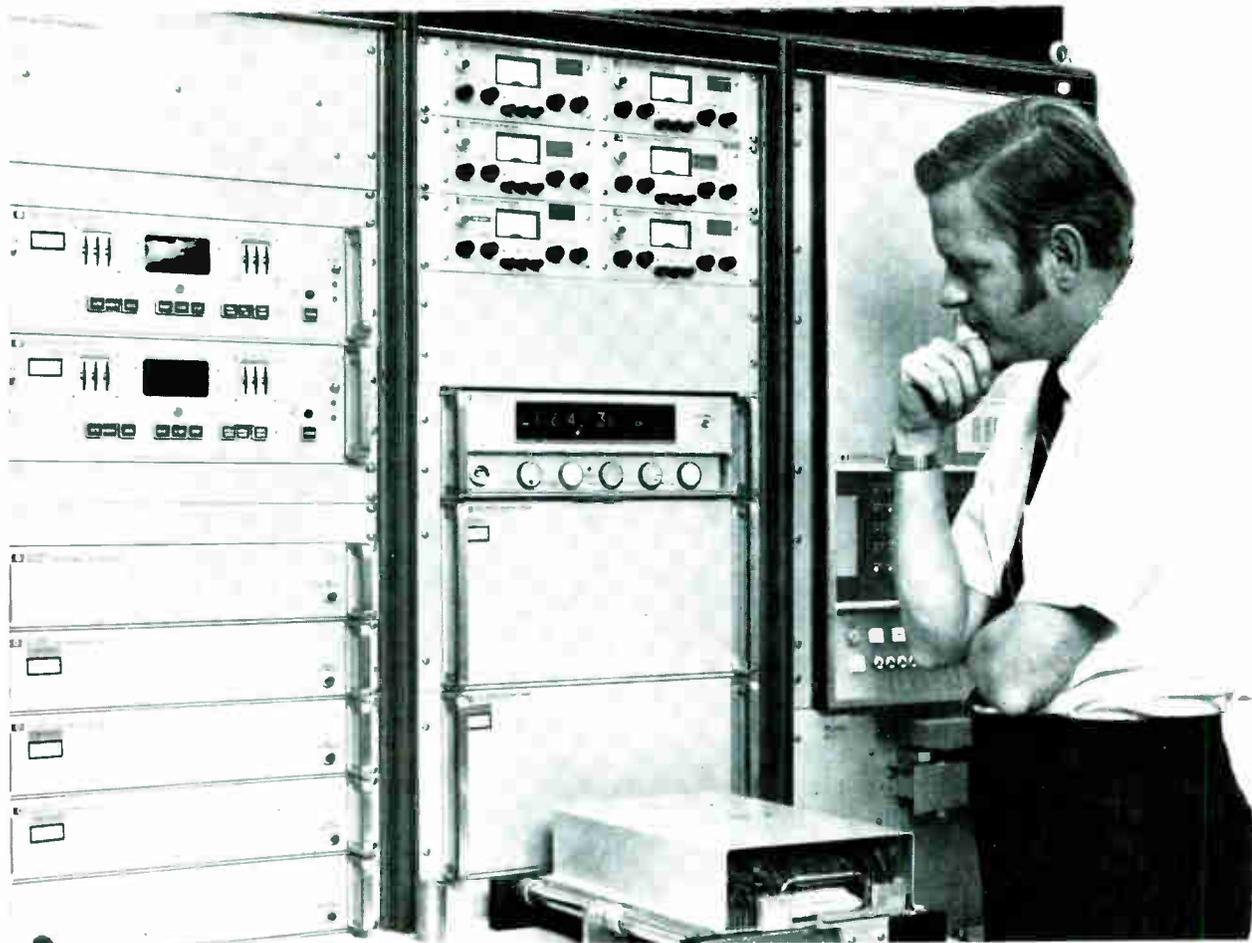
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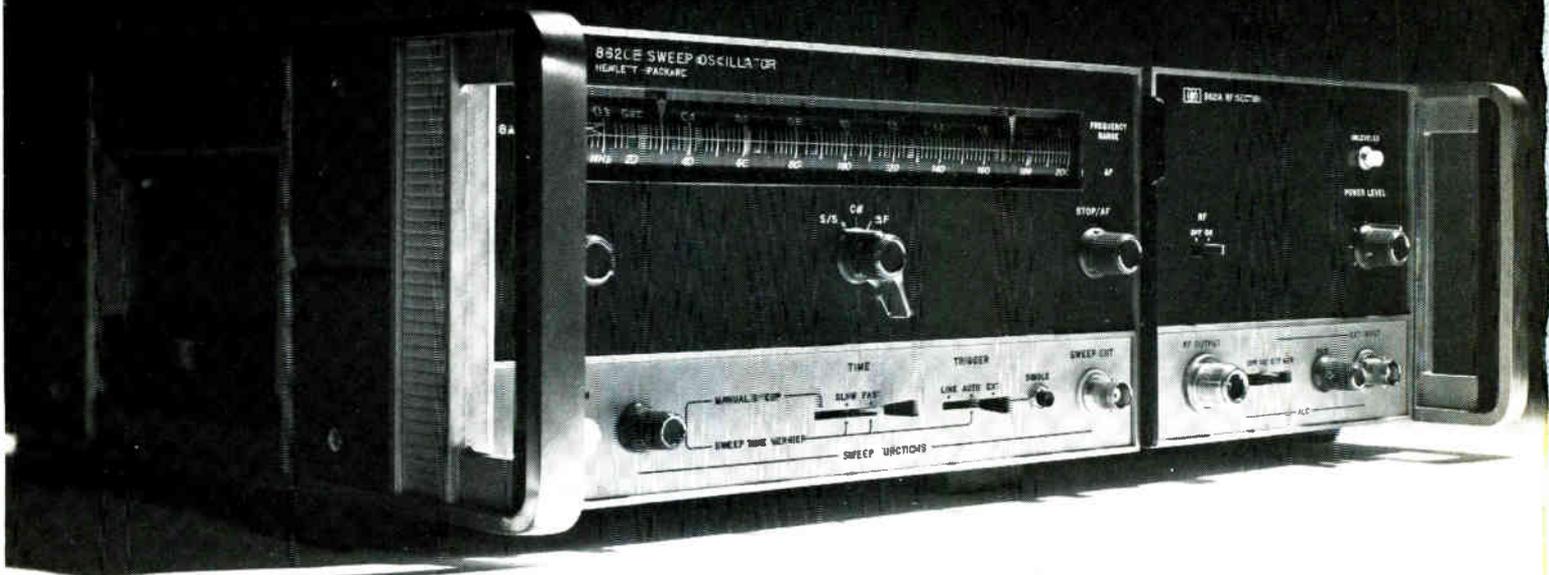
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The Federal budget is a major document and a major story for us because of its impact all across the electronics industries. The budget is printed on 593 pages and its appendix covers another 1,112 pages. Our three-man Washington bureau, beefed up by three senior staff editors from New York, read nearly every word that pertained to electronics. But that was just the beginning of the job needed to present the budget's real meaning to electronics firms (see p. 109).

With a document that massive and a subject so complex, the Government takes no chances on its message being misunderstood. About 48 hours before release time, copies of the budget books are distributed to the press. Then a day before release, the many Government departments hold press briefings. Our team split up to cover them, then spent the rest of the day buttonholing key Administration sources. The day the budget became public, they fanned out to make calls on Capitol Hill to see how the major items will fare when they get to Congress.

A not surprising fact, when you consider that *Electronics* prides itself on its in-depth news coverage, is the wealth of reporting experience on newspapers and wire services that our budget team brought to bear. In addition to their 40 man-years covering electronics technology, one or another of them has worked for the Wall Street Journal, NBC News, Hartford Courant, Bergen Record, Poughkeepsie Journal, Wilmington News-Journal, Sy-

racuse Herald-Journal, Rochester Democrat-Chronicle, and the Medill News Service. Just a bit of name-dropping to emphasize that we are a news magazine for the industry, covering electronics like a big newspaper covers its city.

Washington bureau chief Ray Connolly sums up the massive and hectic budget coverage this way: "The frustrations of orchestrating a successful Federal budget story are akin to those of a conductor getting Jefferson Airplane to sing Beethoven's Ninth Symphony with Fred Waring and his Pennsylvanians. Every year, reporters have to listen to economists and politicians at the same time. The score is fascinating, of course, but the interpretations sound very strange on first reading. The intriguing part is that the performances are always unique."

Controversial subjects have a way of breeding more controversy. In our last issue, we printed a controversial critique of MOS/LSI testing by an engineer who, in charge of installing a test set-up, had been in a position to evaluate what was being offered. We ran it under the heading "Opinion", well realizing that many readers would have different views, and we invited dissenters to write to the editor. Expect a spirited, comprehensive rebuttal in a future issue.



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Readers comment

IC patents

To the Editor: In your Electronics Newsletter reporting on Hughes Aircraft Co.'s patent for the silicon gate MOS process and a possible conflict involving Bell Labs and Philco-Ford patents [Jan. 4, p. 17], you state that "The conflict is reminiscent of the Texas Instruments-Fairchild scuffle over the basic IC patent finally resolved in favor of Fairchild."

This statement is misleading. Basic integrated circuit patents were not involved in the Noyce vs Kilby patents, and the ruling of the U.S. Court of Customs and Patent Appeals on Nov. 6, 1969 did not affect TI's basic patent position in the field of integrated circuits.

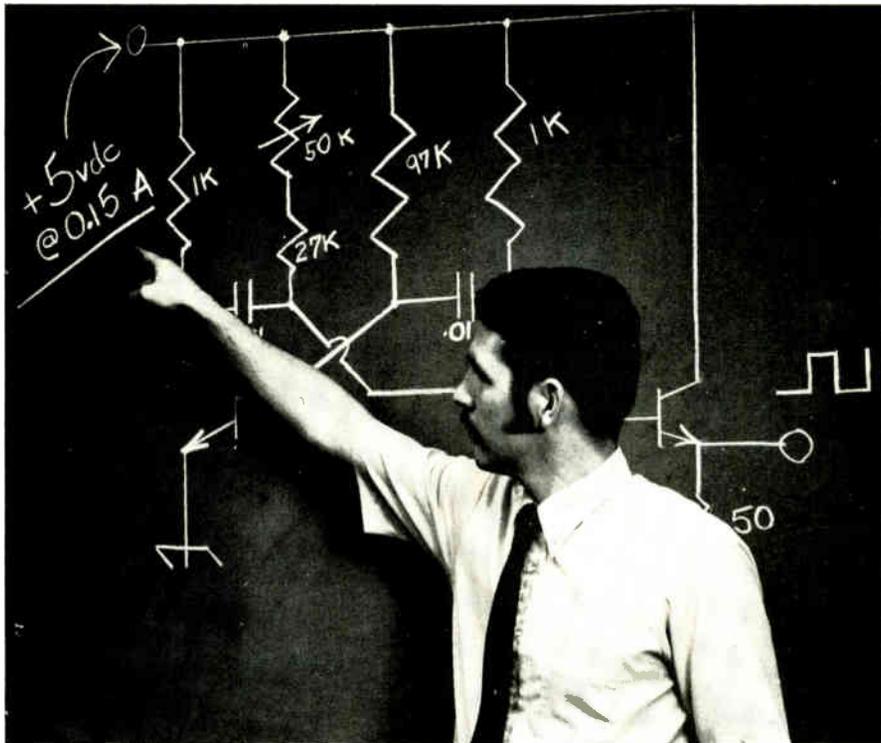
Jack S. Kilby, who invented integrated circuits in 1958, filed for basic IC patents in February 1959. These were issued in June 1964 and established the primacy of his invention of ICs. The subject matter in the interference was limited to an interconnection technique used in the manufacture of integrated circuits. Specifically, the technique is one in which adherent metal conductive patterns are placed over an oxide insulating layer on a semiconductor IC. These metal conductive patterns are used to make electrical interconnections.

TI challenged Noyce's claims to this improvement and the court ruled that Noyce could keep his claims from a 1961 patent relating to a manufacturing technique for making such interconnections in ICs. TI, however, holds the basic patents for ICs, and while the interconnection technique is an important improvement and contribution, this ruling in no way affected TI's basic patent position in ICs.

Bryan F. Smith
Senior vice president
Texas Instruments Inc.
Dallas, Texas

Taresheets?

To the Editor: Mark me not as a stodgy purist nor yet a plodder in the picayune, but in the story on the computerized deli scale [Dec.



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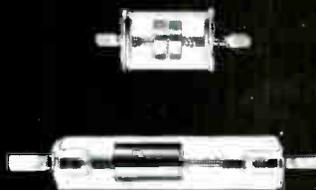
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Readers comment

21, 1970, p. 31], the reference to "tear (sic) weight" reveals vistas of language deterioration that makes the efforts of the mod Madison Avenue clique seem jejune.

I could be charitable and grant you a typo or the honest but misguided diligence of an untechnical proofreader, but I had the uncomfortable feeling that it was a tongue-in-cheek bit of humor at the expense of the "double-thickness" or "heavy" wrapping paper bunch behind the counter; the risk is that the (like myself) humorless among your readers would miss the intended chuckle and a whole new tradition would come into being, staunchly defended by the new faithful.

Is it at all possible that the world could be bloodily divided into two hostile camps over such a tiny differential as "tare" and "tear"? Inconceivable! Man is too mature!

Henry W. T. Dutton
Flygt Corp.
Norwalk, Conn.

▪ Sadly, reader Dutton is mistaken. "Tear" for "tare" wasn't an attempt to rip off a bad pun; rather, it was a typographical error.

Frequency flub

To the Editor: Your story on the electronic watch market [Dec. 21, 1970, p. 83] notes that Intersil Inc. provides CEH, a Swiss research consortium, with "a bipolar five-stage counter that divides down an 8-kilohertz signal to 50 hertz." This is wrong. The IC, consisting of an oscillator, a five-stage frequency divider, and a motor-driving circuit, operates a vibrating motor at 256 Hz and is controlled by a quartz crystal oscillating at 8,192 Hz. The circuits for the first series of 6,000 Beta 2.1 watches were diffused by Faselec in Switzerland. They are available off the shelf.

Heinz Rüegg
Faselec AG
Zurich, Switzerland

▪ Gremlins crept into the frequency output figure. Obviously, the five-stage counter divides the 8K or 8,192-Hz signal down to 256 Hz.

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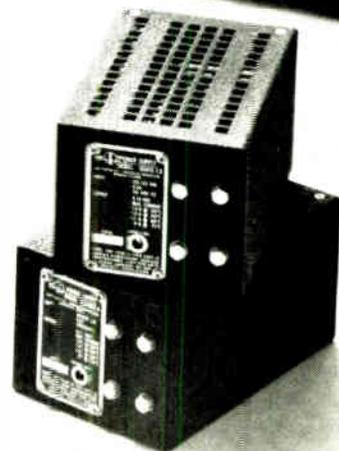
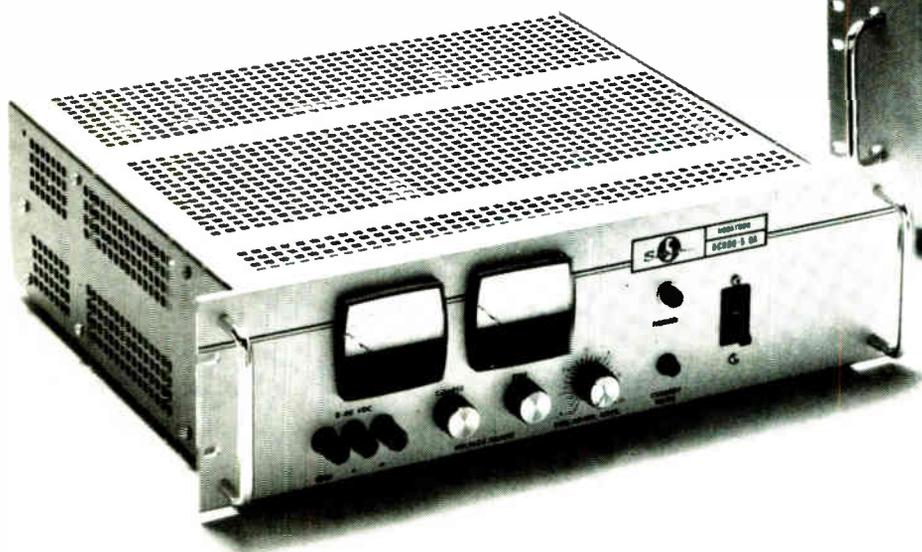
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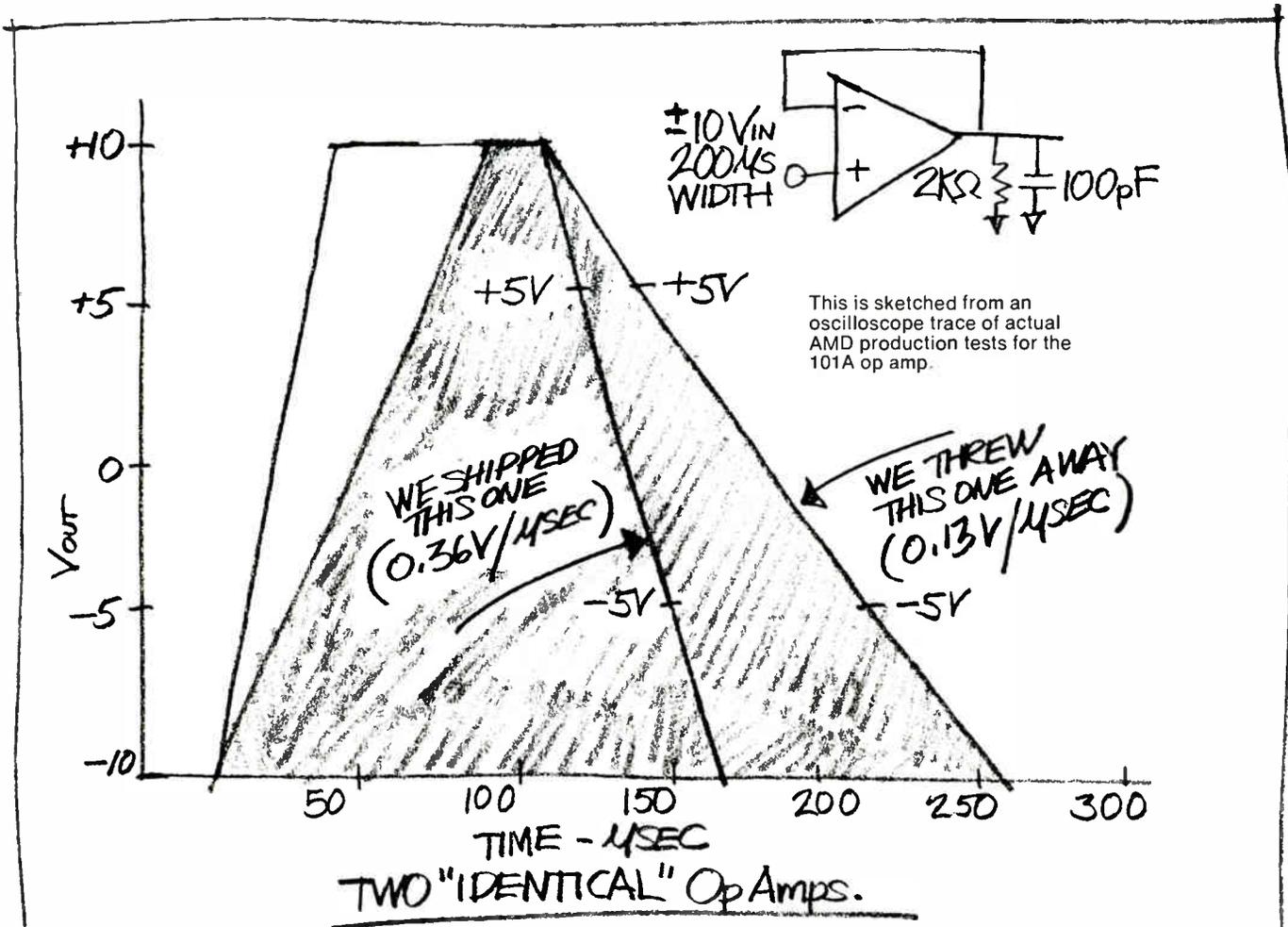
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108A/208A/308A	0.1	0.3	1.6	4.8
107/207/307	0.2	0.5	3.2	8.0
101/201/301	0.2	0.5	3.2	8.0
101A/201A/301A	0.2	0.5	3.2	8.0
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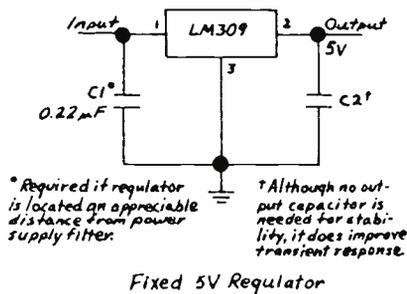


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Significantly, no external components or adjustments are required.

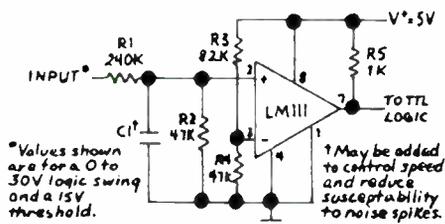
But the real beauty of the LM 309 is the fact that you just plug it in and relax—knowing full well that it's *guaranteed* to limit incoming voltage transients so that the TTL (or DTL) circuits it drives will *always* work. (What comfort to know you've got a regulator that will—in the worst case—actually destroy itself to avoid damaging any of your more expensive digital circuits!)

Both the LM 309 and its military counterpart, the LM 109, are available off-the-shelf in two package configurations: a TO-5 which delivers output currents in excess of 200mA if adequate sinking is provided; and a TO-3, in which the available output current is greater than 1A.

Prices (100-999) are as follows: LM 109H \$20.00, LM 209H \$7.50, LM 309H \$5.50, LM 109K \$25.00, LM 209K \$8.95, LM 309K \$6.50.

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LM 111.



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A plug-in replacement for both the LM 710 and LM 106, our new LM 111 voltage comparator has it all over its predecessors.

First of all, the LM 111 is very easy to use.

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Another big advantage is the 111's input impedance. It's so high, the resulting input current is a remarkable *one thousand times* lower than the 710's (250 nanoamps versus 25 microamps)!

Since we're dealing in superlatives, here's another: Gain with the LM 111 is 200,000, or *two hundred times better* than previously available.

Designed to drive RTL, DTL, TTL or MOS logic, the versatile LM 111 will also handle lamps or relays up to 50V at 50mA.

Finally, the entire LM 111 series (including the LM 211 and LM 311) is available off-the-shelf in TO-5, flat-pack or dual-in-line package configurations.

Prices (100-999) are very competitive.

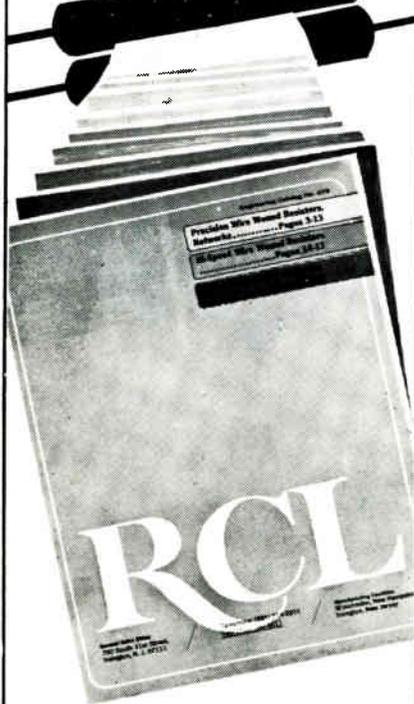
For example: LM 111H \$12.00, LM 211H \$7.50, LM 311H \$3.25.

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People



Adduci

Listen to Jim Adduci on his goals as president of the Electronic Industries Association: "Identify the issues affecting this industry. That's the first important job. Then decide what you want to do about them. That's the second important job." His *con brio* delivery of these ostensibly basic principles is not gratuitous. "In a trade association," he explains, "you can waste an awful lot of time and muscle accomplishing a lot of routine actions. You get into a situation where you are responding to so many things that sometimes you feel like the job is being done. Once in a while you've got to sit back and ask yourself what you really should be doing for this industry; what are the one, two, three, or four important things that must be done?"

Identifying the issues and assigning priorities have occupied much of Vincent James Adduci's time since he moved from a vice presidency at the Aerospace Industries Association last fall to become EIA's top salaried staffer. These are the areas in which he is moving with obvious care following the departure of George Butler from the top association slot after a year marked by staff disputes and some budget overruns.

Thus far, Adduci, who says he is impressed by EIA's staff and industry committee talent, has made two internal changes, and has slated another. First he created a new second-in-command post, assistant general manager, and named William Moore, Government Products division vice president, to the job. At the same time, he moved

Jean Caffiaux, Engineering Department manager, into Moore's old slot. Both men were naturals for their new assignments, says Adduci. Moore "knows the members—he has an accounting degree, and knows the public affairs side of dealing with Capitol Hill." And Caffiaux, he adds, is "an engineer, and with the change in the government procurement picture, where we must be more concerned with research and development, this also was a good move."

With EIA's new emphasis on international activities, Adduci says another long-time staffer, David Hull, will take over internal responsibility for the International Council, which will comprise two members from each of EIA's seven divisions.

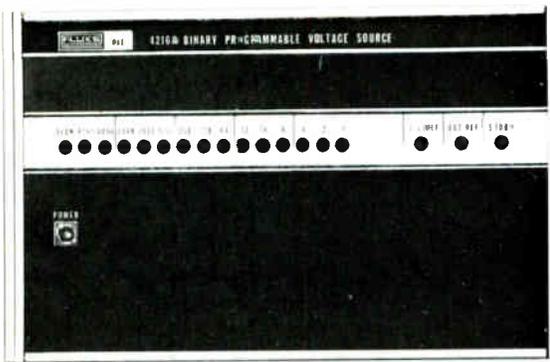
Adduci himself knows Washington from both the government and industry sides. After a 21-year Air Force career—part of it spent as a Colonel in the Pentagon, doing legislative liaison work—Adduci joined the Aerospace Industries Association in 1960. Legislative liaison is the military euphemism for lobbying, and Adduci's experience with the military, coupled with a decade at AIA, has given him the kind of insight that EIA needs and should be able to put to good use.

A year ago there was no Enviro Control. Five years from now the Washington, D.C., firm expects to be doing \$100 million worth of business.

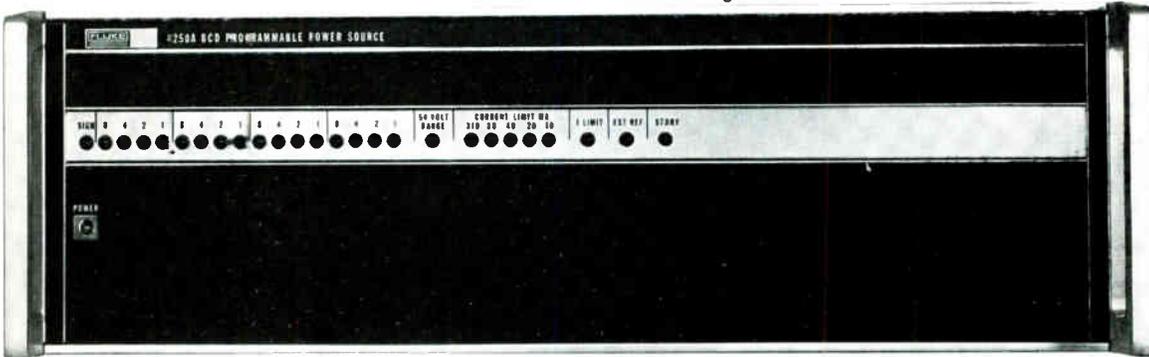
Such ambition isn't rare in the pollution-control field. Nevertheless, many companies are finding business hard to come by, leading to complaints about a mythological or imaginary market.

Enviro Control's founder and president, Charles MacArthur, thinks the market is very real. "There is money to be made if you select the market very carefully, if you go into an area where competition isn't very tough, and if you have something industry needs," he says.

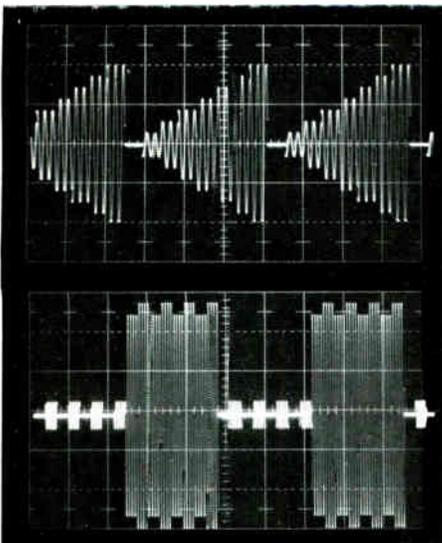
MacArthur, a 40-year-old physical chemist, started Enviro last



Instrument photos show Model 4216A Binary Programmable Voltage Source in half-rack version at top and Model 4250A BCD Programmable Power Source in full rack configuration.



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Settling Time		30 μ s	100 μ s	
Basic Unit*		\$995	\$1295	

*Options extra

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summer after spending four years at the Pentagon as deputy director of research and development—a far cry from his current enterprise. This experience, he says, will be invaluable because many pollution problems can be solved with military and aerospace techniques and equipment. "I've always maintained," he says "that for pollution control and abatement, 80% of the necessary technology already is available."

New entries into the pollution field, notes MacArthur, have ignored some cardinal rules. "The biggest reasons companies have been falling down are that they don't have a product; they say they're in every part of the environment (and don't concentrate on one market); and they don't have adequate financing. They start with \$60,000 or \$80,000. You just can't live on that."

For financing, MacArthur went to Publishers Company Inc. of Washington. Enviro Control has become a subsidiary of this \$55 million firm.

As for a specialty, Enviro Control will stick to the water pollution field. It will consult in this area, and develop products—the first one is due in early summer. MacArthur calls it a process analyzer/process controller for monitoring specific pollutants in an industrial plant's effluent.

He has no doubt the product will sell. "The service I'm going to give them [industry] is now costing them \$500 to \$1,000 a month," he says. "I can give them the same service 24 hours a day, completely automatically with a black box, for about half of that. You can't beat the economics. Any place you come in with economics on your side, you have it made."

MacArthur refuses to give any design details about his black box. However, he notes that it will have an aerospace heritage. "All the advanced features that we have incorporated are electronic in nature," says MacArthur. "What we have done is taken essential space electronics and applied them to commercial products."

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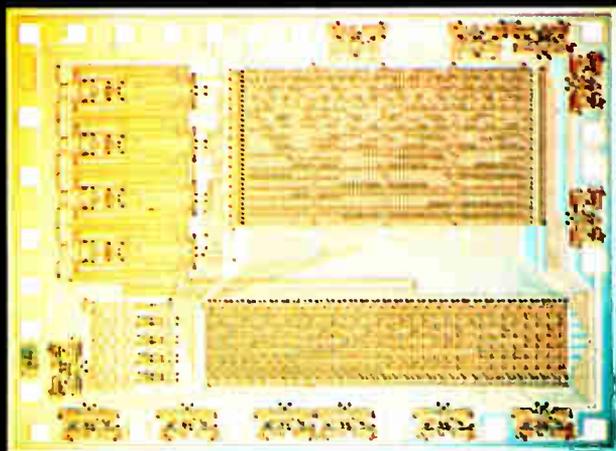
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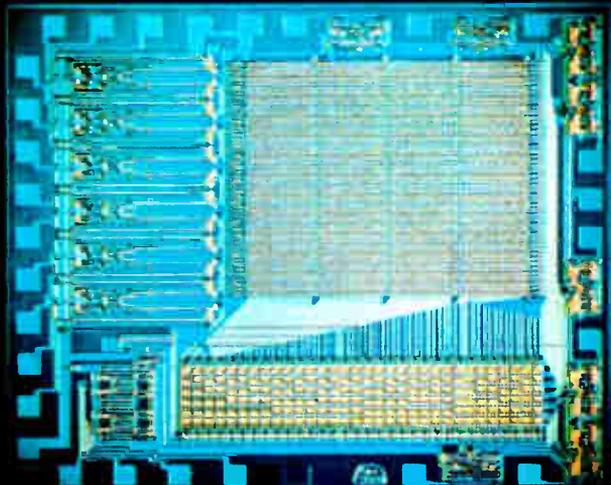
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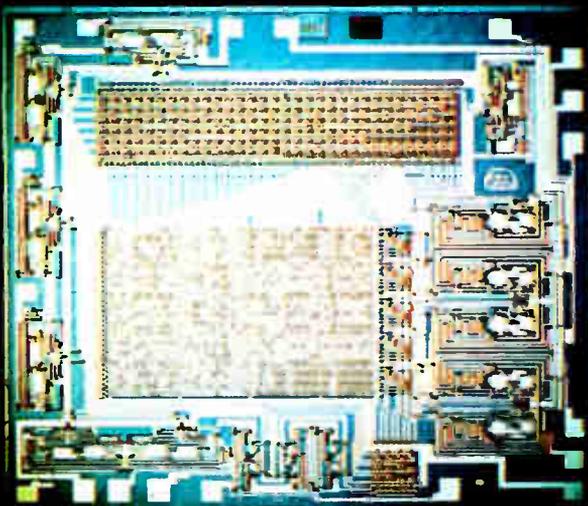


UA2548/3548 2048-bit ROM

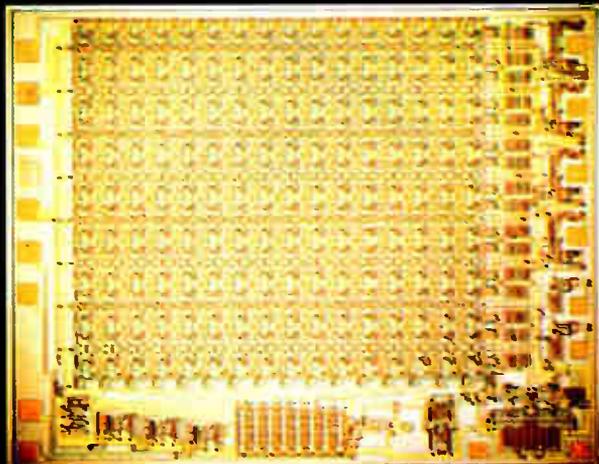


JA2572/3572 3072-bit ROM

UA2540/3540 2240-bit character generator



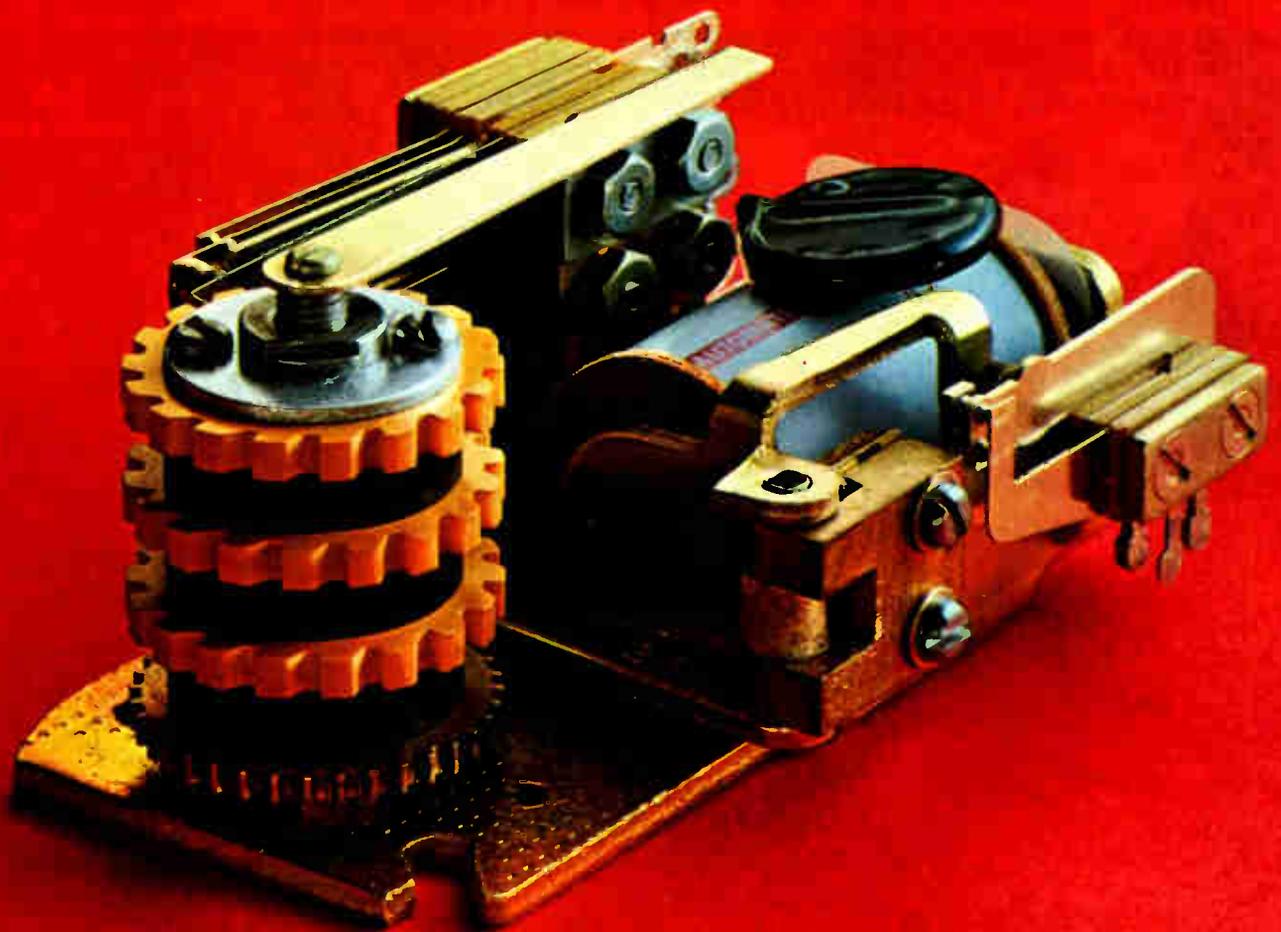
UA2556/3556 256 x 1 RAM



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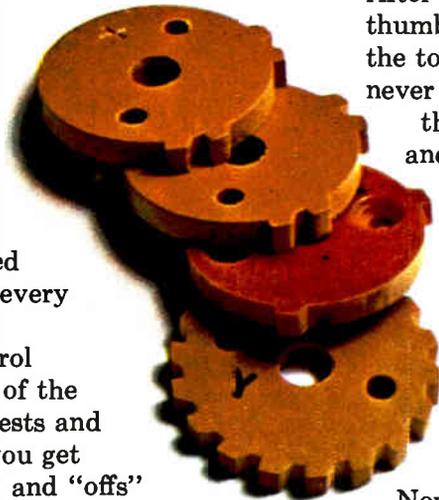
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and a double-jointed thumb**



We combine the simplicity of a cam-operated relay with a tough, time-proven stepping switch to give you an uncomplicated and sturdy relay. The brains of our OCS relay are precisely notched cams that give it an unforgettable memory. Power blackouts won't change it.

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Meetings

Calendar

International Convention & Exhibition, IEEE; Coliseum and New York Hilton Hotel, New York, March 22-25.

European Semiconductor Device Research Conference, IEEE, DPG (German physical society), NTG (German communications society); Munich, March 30-April 2.

Reliability Physics Symposium, IEEE; Stardust Hotel, Las Vegas, March 31-April 2.

USNC/URSI IEEE Spring Meeting, Statler Hilton Hotel, Washington, April 8-10.

National Telemetry Conference, IEEE; Washington Hilton Hotel, April 12-15.

International Magnetics Conference (Intermag), IEEE; Denver Hilton, Denver, Colo., April 13-16.

Conference & Exposition on Electronics in Medicine, Electronics/Management Center, Medical World News, Modern Hospital, Postgraduate Medicine; Sheraton-Boston Hotel and the John B. Hynes Civic Auditorium, April 13-15.

Offshore Technology Conference, IEEE, Houston, April 18-21.

International Geoscience Electronics Symposium, IEEE; Marriott Twin Bridges Motor Hotel, Washington, April 18-23.

Frequency Control Symposium, U.S. Army Electronics Command; Shelburne Hotel, Atlantic City, N.J., April 26-28.

Relay Conference, College of Engineering, Oklahoma State University Extension, National Association of Relay Manufacturers; Stillwater, Okla., April 27-28.

Southwestern IEEE Conference and Exhibition, Houston, Texas, April 25-May 2.

Symposium on Theory of Computing, Association for Computing Machinery; Shaker Heights, Ohio, May 3-5.

Call for papers

Conference on Engineering in the Ocean Environment, IEEE; Town and Country Hotel, San Diego, Sept. 21-23. Mar. 30 is deadline for submission of abstracts to Dr. Maurice Nelles, Technical Chairman, Bissett-Berman Corp., 3939 Ruffin Road, San Diego, Calif. 92112.



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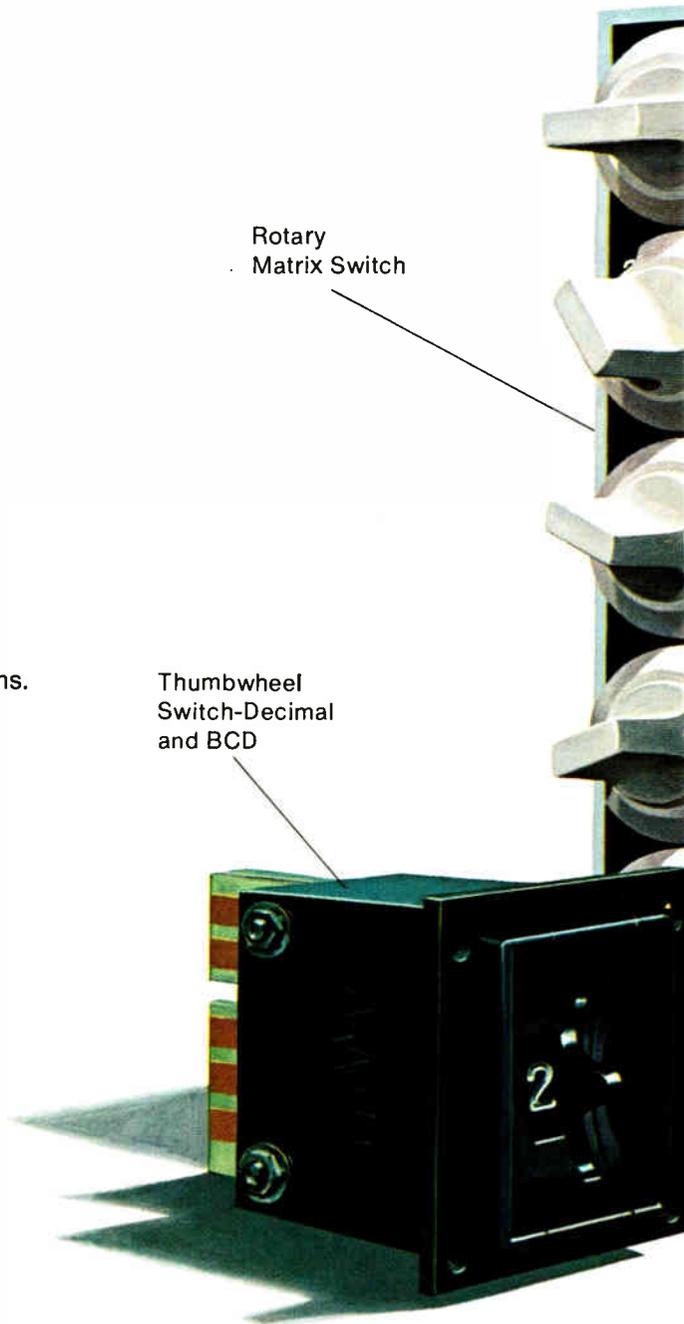
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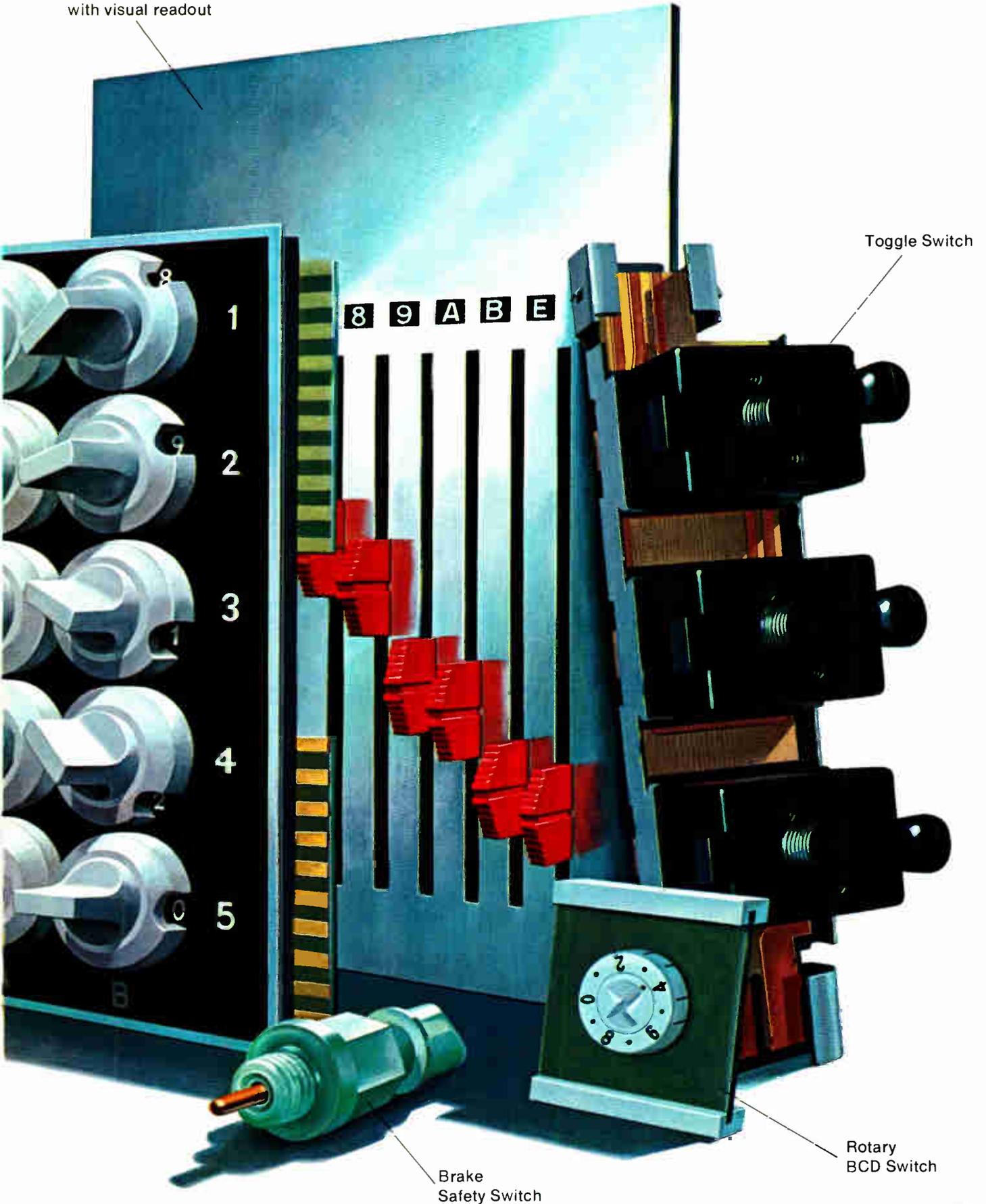
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Electronics Newsletter

February 15, 1971

Hardware invades software domain

A computer that has a high-level programming language implemented directly in hardware has been built at the Digital Systems Research department of Fairchild Camera & Instrument Co. Conventional computers need compilers (large software packages) to translate programs into machine language, so Fairchild's design is an important advance by hardware into a previously all-software realm. It could mean hardware replacements for software in other language compilers, input/output control systems, and possibly even monitors and operating systems.

The machine, called Symbol IIR, has a clock rate of 320 nanoseconds, a memory cycle time of 4 microseconds, and can compile 70,000 statements per minute (Fortran-like statements, although the language is called Symbol). Iowa State University bought the machine last month with a grant from the National Science Foundation.

The cpu consists of about 100 pc cards, each with about 200 ICs. Fairchild's CT μ L current-mode logic family was used. The machine can handle 32 terminals; all control and the time-sharing supervisor are hard-wired. No cabling or wirewrap is employed (except to get from the cpu to the main core memory or the terminals). All interconnections are done with two-sided pc cards.

With equivalent memory and peripherals, Symbol IIR "would give an IBM 360/67 a run for its money," says Rex Rice, manager of the project.

Motorola readies ECL to fight Schottky TTL

Watch for Motorola's Semiconductor Products division to unveil a new set of emitter-coupled logic devices with speed and power dissipation that should make them directly competitive with Schottky-clamped TTL devices. Motorola officials aren't talking, but it's known that potential customers have received samples.

The first batch of devices in this MECL 10,000 series are expected to include about 12 functions, and fit into what Motorola calls its MECL 2.5 family. Those devices have propagation delays per gate of about 2 nanoseconds and power dissipation of about 60 milliwatts per gate; the 10,000 series will dissipate only about 25 mW per gate, giving a speed-power product of 50 picojoules vs. 120 to 150 picojoules for some other MECL 2.5 family members.

One potential user regards the circuits as a means to allay the wariness of some designers about the high power dissipation associated with high-speed ECL devices, and as a direct competitor to Schottky-clamped TTL, even though Motorola also is getting into that business [*Electronics*, Feb. 1, p. 18].

TI automation cuts light-emitter prices

Texas Instruments, going after the high-volume consumer light-emitting diode market, has cut the price of LEDs to 35 cents in 25,000 quantities—or 10 to 20 cents less than competition prices. In lots of 100 to 4,000 they're 49 cents. Ian McCrae, marketing manager of TI's Optoelectronics department, says that high price is what has been keeping LEDs from pushing incandescent lamps out of small-bulb indicators such as exposure indicators on cameras.

TI says it got its price down by completely automating the produc-

Electronics Newsletter

tion cycle. The company won't detail its techniques, but they could have far greater potential than just for LED fabrication. The obvious conclusion is that the automation can be used in semiconductor fabrication as well.

LED display may go on telephones

Bell Laboratories has developed a light-emitting diode display that eventually could find its way to pushbutton phones. A 72-by-7 matrix of gallium-phosphide (GaP) diodes, the display has a one-bit TTL shift register for each diode. This memory capability allows generation of variable-width characters, or a rolling display for pushbutton phones. When a number is pushed, it's displayed on the right side of the display while previously displayed numbers shift one character to the left.

MOS digital filters to make appearance

What are believed to be the first MOS/LSI digital filter components should be available in small quantities by month's end from North American Rockwell Microelectronics Co., Anaheim, Calif. The arrays are a serial/parallel multiplier, a shift register/adder, and a unit that can be used as an analog-to-digital or digital-to-analog converter, depending on how it's used in a circuit. The devices will be available as beam-lead chips or as packaged parts. A typical circuit using the multiplier and shift register/adder arrays will dissipate about 300 milliwatts at a 1-megahertz bit rate.

They're expected to be used as radar anticlutter filters, filters in receivers with combined navigation and communications functions, or in laboratory spectrum analyses. The Navy is known to be considering having its Omega navigation receivers function as communications receivers as well; the NRMEC devices should provide the precise filtering needed to cleanly separate the two signals.

Digital tester capable of speeds up to 340 Mb/s

The first of what may become a commercial line of ultra-high-speed digital-communications test sets was delivered last week to Bell Laboratories by Tau-Tron Inc. of Lowell, Mass. The set could check a range of gear from modems to millimeter wave carrier links, and it uses so-called maximum-length shift registers to create pseudo-random binary-pulse trains at speeds of 240 to 340 megabits per second—a technique borrowed from Tau-Tron's development of high-speed LSI testers [*Electronics*, Dec. 7, 1970, p. 107]. By contrast, most commercial test gear is concentrated in the speed range well below 9,600 bits per second.

Presumably, Bell will use the system in development of its 300-mega-bit T-5 digital carrier system due for field trials around 1975. Meanwhile, Tau-Tron is considering going commercial with the technology, and applying it not only to digital testing, but to communications security—properly used, the maximum-length shift register technique is said to provide an almost unbreakable enciphering system.

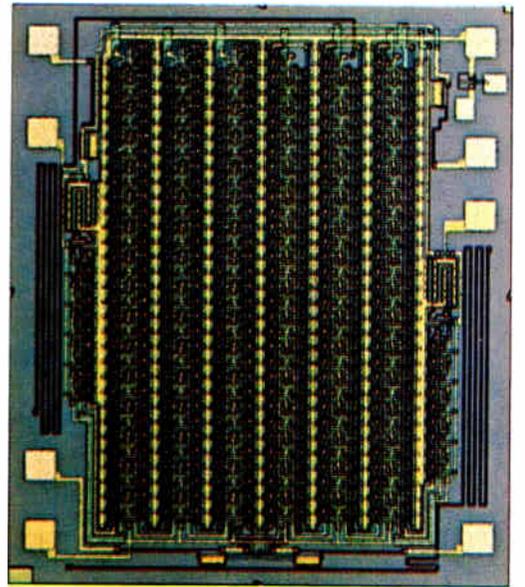
Jameson to head space agency

The managers will have triumphed over the technicians if Frank G. Jameson, president of Teledyne Ryan Aeronautical Co., is named administrator for NASA as expected. Jameson, 46, would be the second NASA administrator—James G. Webb was the other—to come to the job on the basis of his managerial experience.



MOS

BY



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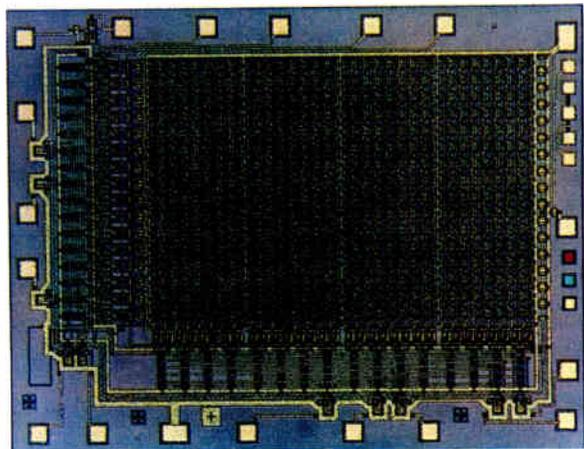
- Low address-line capacitance of 2.5 pF (typ) improves system speeds
- Eliminates need for separate chip select clock signal to refresh stored information
- Low capacitance and high "on"-to-"off" current ratio of the output circuit for simplified bipolar interfacing
- Wired-OR capability for memory expansion
- Only 400 ns access time
- Low drive power required compared to other high-threshold MOS
- Monolithic fabrication with the proven P-MOS process
- Low Power Dissipation — 50 μ W/bit

Motorola MOS memories available now

2240-bit read only memory — MCM1130

64-bit read/write memory — MC1170

1024-bit read/write memory — MCM1173L



1024 word by 1-bit dynamic RAM — MCM1173L

Available soon

Diversification and capability are the bywords for these scheduled MOS memory products:

2240-bit read only memory — MCM1120

1024-bit (Si Gate) read/write memory — MCM2372L

2048-bit read only memory (256 x 8) or (512 x 4) — MCM1110

4096-bit (Si Gate) read only memory (512 x 8) — MCM2340

2560-bit read only memory (256 x 10) or (512 x 5)—MCM1150

For details, circle 280



Move Ahead with Motorola

MOS REGISTERS

Reach for performance — get lowest prices, too

Shift registers have been the most used device types in the early years of designing with MOS. For example, when the industry needed an elastic memory (low data rate in/high data rate out) for printer buffers, MOS shift registers were called on . . . move-ahead types . . . like Motorola's dual 100-bit static MC1160G shift register.

- DC to 2 MHz operation for a wide range of applications
- Specified for single or cascade operation for use as a 100-bit or a 200-bit shift register
- Non-inverting buffered outputs for greater drive capability
- Typical delay time is only 150 ns
- Common supply and clock lines
- Independent input/output lines

Motorola MOS shift registers available now

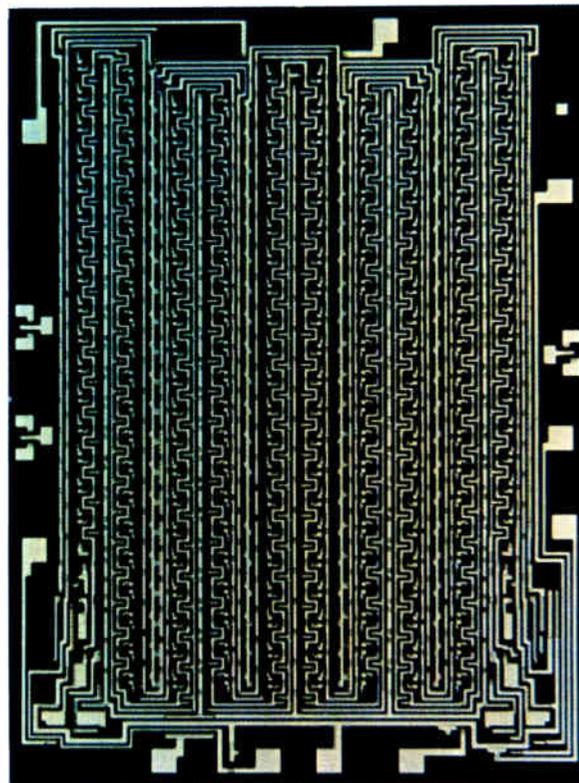
Triple 66-bit dynamic shift register — MC1141G
200-bit dynamic shift register — MC1142G
Dual 100-bit static shift register — MC1160G
Dual 50-bit static shift register — MC1161G

Available soon

The desirability of the Silicon Gate technology for many designs is evident in this great line-up of MOS shift registers scheduled for introduction soon.

Dual 100-bit dynamic shift register (Si Gate) — MC2380G (cover photo)
Dual 100-bit dynamic shift register (Si Gate) — MC2381G
Quad 64-bit dynamic shift register — MC2246G
Quad 256-bit dynamic shift register (Si Gate) — MC2384L

Dual 512-bit dynamic shift register (Si Gate) — MC2385G
1024-bit dynamic shift register (Si Gate) — MC2386G
Dual 256-bit static shift register (Si Gate) — MC2363G
Dual 100-bit static shift register (Si Gate) — MC2360G
Dual 250-bit static shift register (Si Gate) — MC2362G
500/512-bit dynamic shift register — MC2244G



Dual 100-bit static shift register — MC1160G

NOTE: MC1100 series denotes high threshold, MC2200 series denotes low threshold, MC2300 series denotes Si Gate

For details, circle 280

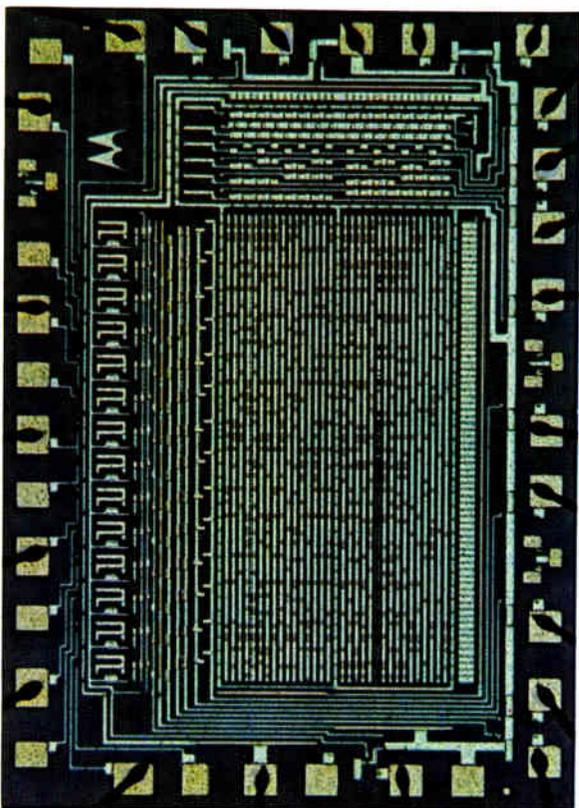


Move Ahead with Motorola

MOS LOGIC

Greater component density encourages LSI now

MOS has set an altogether new pattern in standard development. In previous logic forms, single and



2240-bit column
select character generator — MCM1131L

relatively simple logic functions were packaged in

many independent product types for years before complexity began developing. MOS benefits from greater chip component densities to make MSI and LSI feasible from the beginning. So when CRT people needed 5 x 7 character generation, an MOS2240-bit column select character generator like Motorola's MCM1131L was the logical solution. It features:

- Matrix options — 64 x 5 x 7 or 32 x 5 x 14
- Only 500 ns maximum access time
- Open drain output buffers sink 1.6 mA (min) for bipolar compatibility
- Wired-OR capability for memory expansion
- Programmed to standard USASCII Code
- Proven monolithic P-MOS process

Motorola general purpose MOS available now

8-channel multiplex switch — MC1150L

2-of-8 channel multiplex switch — MC1151L

Versatile general purpose logic element — MC1155L

Versatile general purpose logic element — MC2255L

2240-bit column select character generator — MCM1131L

2240-bit column select character generator — MCM1132L

Available soon

Representative of the complexity of coming Motorola logic introductions are these two additional character generators.

2240-bit character generator — MCM1121L

2240-bit character generator — MCM1122L

NOTE: MC1100 series denotes high threshold, MC2200 series denotes low threshold.

For details, circle 280



Move Ahead with Motorola

MCMOS

Works on next to no power — and ignores noise

Complementary MOS has its roots in the reliability conscious military and aerospace fields, and now spreads its branches and foliage over a widening range of commercial and industrial applications. Its low power requirements make it the mainstay for tiny, delicate, portable electronic watch systems, yet its high noise immunity makes it ideal for use in rugged applications like industrial controls. Complementary MOS offers operation with a wide range of supply voltages, and as the only logic to work directly from a car battery is a natural for automotive applications. MCMOS, Motorola complementary MOS, features:

- P and N-Channel devices in a single monolithic structure
- Real economy of operation with low quiescent power dissipation of only 50 nW/package (typ)
- Thrives in noisy environments — Noise immunity = 45% of V_{DD} (typ)
- Matches power supplies with any of them — 4.5 V to 18 V

MCMOS available now

Quad 2-input NOR gate — MC14001L (MC2501L)
Dual 4-input NOR gate — MC14002L (MC2502L)
Dual type D flip-flop — MC14013L

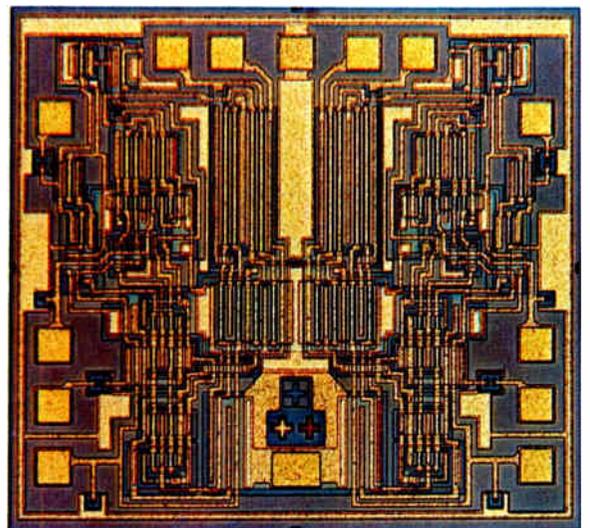
Available soon

This short term new product activity plus eighteen new MSI circuits planned from the ground up for system compatibility make MCMOS the premium low power logic family.

64-bit read/write memory — MCM14005L

Quad exclusive OR gate — MC14501L

Quad 2-input NAND gate — MC14011L



Dual type D flip-flop — MC14013L

Dual 4-input NAND gate — MC14012L

Dual 4-bit shift register — serial in/parallel out — MC14015L

MCMOS — Trademark of Motorola

For details, circle 280



Move Ahead with Motorola

CUSTOM MOS

Your designs or ours — Original from the ground up, or use our Polycell concept

Let's start by assessing MOS circuitry.

- MOS processing is inexpensive permitting low-cost device manufacture.
- MOS component geometries are small permitting component densities and highly complex circuits on relatively small chips.
- MOS circuits are easy to design encouraging widespread design efforts.

Combined, these three MOS characteristics — inexpensive processing, high component densities, and simple circuit design — clearly point MOS technology in one specific direction; that is, *custom circuitry*.

New ground rules for user and manufacturer

Users will be designing their own proprietary circuits and will implement systems with fewer building blocks. Each of these will be more complex and represent a larger portion of the complete system than is generally prevalent today.



figure 1

For the IC manufacturer, this demands quick-reaction time capabilities and versatile design techniques allowing the customer to interface at

any point in the design cycle. We emphasize this. We can and will enter the custom design process at any point in the cycle the customer desires.

This means we will work at either extreme or pick up the job anywhere in between. Give us your masks and we'll give you the product. Give us your system requirements, and we'll develop the design and deliver your product. We'll do it on the drawing board and with the computer.

Polycells and CAD

Combining a library of standard MOS computer building blocks called polycells, an educated computer, and a variety of computer design and drafting aids, Motorola has developed a custom and customer oriented design capability. We're proud of our CAD capability but we recognize that



figure 2

it is only an aid to humans interfacing with humans. Here's how it works.

1. From the polycell library of logic building blocks, the designer selects the polycells to be used in his system.

2. He partitions the system to delineate a number of chips on which the system is finally implemented.

3. Armed with the appropriate preliminary logic diagrams, he transforms these into detailed topological chip layouts, either on a CRT console



(Figure 1), or in the form of a conventional drawing with a computer controlled digitizer (Figure 2).

4. With the exact geometries so displayed, the designer juggles the polycells for the most advantageous layout, and plots the required cell interconnection pattern (on the CRT console or on a coordinate digitizer). A conventional ink plot can be employed for layout verification.

5. Finally, a computer generated program that details the final design is used to control an auto-

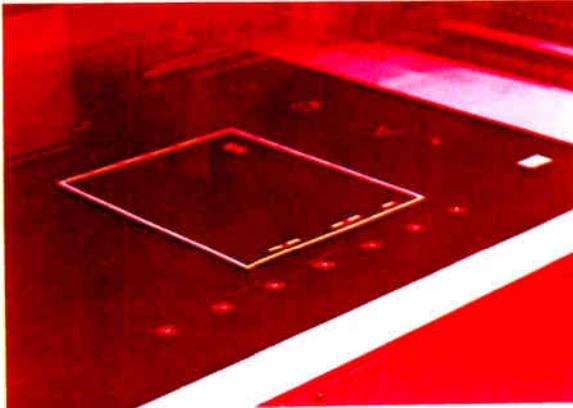


figure 3

matic drafting machine (Figure 3) to prepare a complete set of masks for the MOS array.

Generic to the Motorola polycell program is a line of completely characterized circuits whose specifications, both electrical and physical, are stored in a computer memory. When a detailed layout is required, it is drawn automatically by the ink plotter in response to information stored in the memory. The amount of time saved through computer-aided design is one of the pivots around which a custom capability revolves. And so are the number and types of basic cells that define an engineer's design freedom. Motorola's initial line consisted of P-channel, high-threshold, static cells (51) with propagation delays of approximately 74 ns per logic level and a power dissipation of 1.7

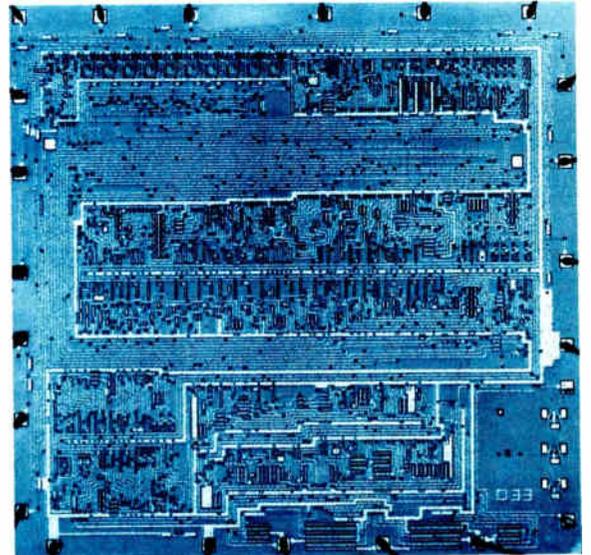
mW or less per gate. A second series of 28 cells has a power dissipation of less than 0.45 mW per gate and a propagation delay of about 300 ns.

In addition, a series of 12 shift registers and a family of 172 dynamic (2-phase) logic cells have been put into the library. Corresponding sets of low threshold, silicon gate and CMOS cells are being rapidly expanded.

Emphatically, MOS technology is expected to be a dynamic growth area in the years ahead, and custom design capability represents a major challenge to all involved.

Motorola is very much involved.

If you have a custom MOS project, call Motorola Custom MOS, 602-273-3832. A 172-page Polycell MOS/LSI design brochure available for



Custom MOS/LSI in Boeing 747 electronics.

the asking on your company letterhead, covers most of the cells in the library. The balance will be sent automatically as brochure supplements are published. Write to Custom MOS, Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Arizona 85036.



Move Ahead with Motorola

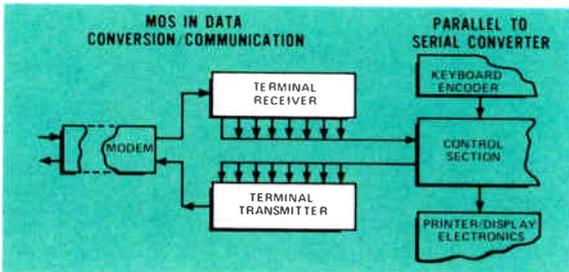
SYSTEMS MOS

The thrust of Motorola's new MOS product activity, in 1971 and beyond, is orientation to the systems needs of the markets we serve. The final criterion for all future standard MOS product is service within the total needs of our customers.

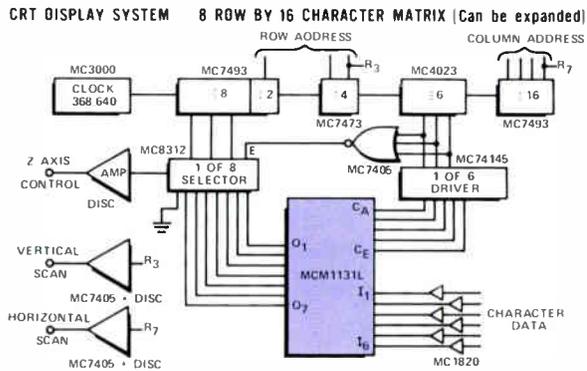
This MOS product philosophy of serving systems is presently hard at work in such diverse fields as electronic timing and time keeping, desk-top calculators, memory systems for processors, CRT display systems and other data handling system requirements.

Complementary MOS, MCMOS, is ideally suited to reducing the costs of personal electronics timepieces capable of operating reliably with the extremely small power supplies necessary for this purpose. As a result of Motorola's systems development work, new products with extensive applications will evolve.

MOS subsystems for terminal equipment



A good example of Motorola's systems approach



to terminal equipment requirements are new developments in products for terminal receivers and transmitters and for CRT display systems.

Systems orientation vital

Another case of orienting new products to the systems needs is the Motorola memory system designed with multiple MCM1173L RAMs for use with a processor. And so it will go, into the future, whether the requirements are for standard or custom designed product, Motorola MOS will be oriented to fulfilling the system needs — all MOS where MOS delivers the best results or interfacing with other logic forms when that is the best solution.



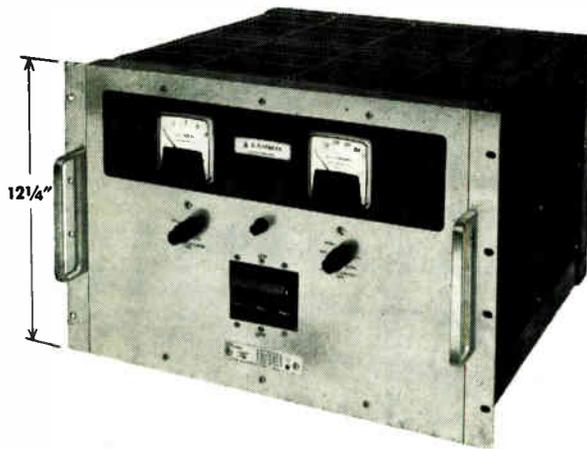
MOTOROLA MOS

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Series/parallel operation

LB SERIES, METERED, FULL-RACK SIZE: 7" x 19" x 20 1/16"

Model	Voltage Range	Max. Current (Amps) at Ambient of: ⁽¹⁾				Price ⁽²⁾
		40°C	50°C	60°C	71°C	
LB-701-FM-OV	0-7.5	300	270	235	200	\$1,500
LB-702-FM-OV	0-15	180	170	160	150	1,500
LB-703-FM-OV	0-36	80	75	70	65	1,400
LB-704-FM-OV	0-60	50	47	44	40	1,400
LB-705-FM	0-125	25	22	19	16	1,400
LB-706-FM	0-300	10	9.5	9.0	8.0	1,400

LB SERIES, METERED, FULL-RACK SIZE: 12 1/4" x 19" x 22 1/16"

Model	Voltage Range	Max. Current (Amps) at Ambient of: ⁽¹⁾				Price ⁽²⁾
		40°C	50°C	60°C	71°C	
LB-721-FM-OV	0-7.5	500	450	400	350	\$2,700
LB-722-FM-OV	0-15	300	265	225	180	2,700
LB-723-FM-OV	0-36	135	130	125	120	2,500
LB-724-FM-OV	0-60	80	75	70	65	2,500
LB-725-FM	0-125	40	36	32	28	2,500
LB-726-FM	0-300	16	15	14	13	2,500

NOTES:

1. Current rating applies over entire voltage range.

2. Prices include meters. LB Series models are not available without meters. Prices for all models up to and including 60 Vdc include built-in overvoltage protection. Prices are FOB Melville, New York. Prices and specifications are subject to change without notice.

LAMBDA
ELECTRONICS CORP.
A  Company

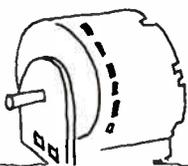
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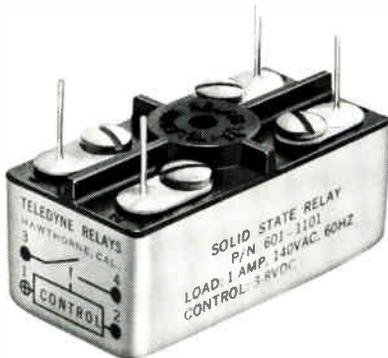
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ETC.

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- All solid state (NO REEDS)
- Zero voltage switching available to minimize RFI
- Transient protected on input and output
- PC board or screw terminal mounted



PART NUMBERING (Economy Line)

INPUT (CONTROL) VOLTAGE RANGE	OUTPUT VOLTAGE RATING	OUTPUT (LOAD) CURRENT RATING & PART NUMBERS				
		1 AMP	3 AMP	5 AMP	7 AMP	10 AMP
3-10 VDC	140 VAC	601-1001	601-1002	601-1003	601-1004	601-1005
	280 VAC	601-1006	601-1007	601-1008	601-1009	601-1010
6-32 VDC	140 VAC	601-1011	601-1012	601-1013	601-1014	601-1015
	280 VAC	601-1016	601-1017	601-1018	601-1019	601-1020
15-45 VDC	140 VAC	601-1021	601-1022	601-1023	601-1024	601-1025
	280 VAC	601-1026	601-1027	601-1028	601-1029	601-1030
20-75 VDC	140 VAC	601-1031	601-1032	601-1033	601-1034	601-1035
	280 VAC	601-1036	601-1037	601-1038	601-1039	601-1040

NOTE: Add "P" to P/N for printed circuit (pin) mounting only.

ECONOMY LINE PRICE/QUANTITY (Typical)

LOAD Amps @ 140 VAC	QUANTITY		
	10 - 24	100 - 249	1000 - 2499
1	\$12.20	\$ 8.75	\$ 6.65
3	13.50	9.70	7.35
5	15.30	10.60	8.10
7	16.60	11.55	8.80
10	18.45	12.80	9.75

PART NUMBERING (Zero Voltage Turn-On)

INPUT (CONTROL) VOLTAGE RANGE	OUTPUT VOLTAGE RATING	OUTPUT (LOAD) CURRENT RATING & PART NUMBERS				
		1 AMP	3 AMP	5 AMP	7 AMP	10 AMP
3-8 VDC	140 VAC	601-1101	601-1102	601-1103	601-1104	601-1105
	280 VAC	601-1106	601-1107	601-1108	601-1109	601-1110
7-85 VDC	140 VAC	601-1111	601-1112	601-1113	601-1114	601-1115
	280 VAC	601-1116	601-1117	601-1118	601-1119	601-1120
90-280 VAC	140 VAC	601-1121	601-1122	601-1123	601-1124	601-1125
	280 VAC	601-1126	601-1127	601-1128	601-1129	601-1130

ZERO VOLTAGE TURN-ON LINE PRICE/QUANTITY (Typical)

LOAD Amps @ 140 VAC	QUANTITY		
	10 - 24	100 - 249	1000 - 2499
1	\$21.60	\$15.00	\$11.40
3	22.95	15.94	12.11
5	24.30	16.88	12.83
7	25.65	17.81	13.55
10	27.45	19.06	14.50

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U. S. fires first shot at Japanese calculator lead

Electronic Arrays subsidiary says it will make 30,000 units a month, but will supply machines to OEMs only

Electronic calculators are probably generating more excitement among U.S. MOS array suppliers than any other product. About 50% of the MOS parts shipped last year in this country went into calculators [*Electronics*, Nov. 23, 1970, p. 83]—though some estimates go as high as 65%—and most of those machines were made in Japan. Now the predicted American counter-attack has begun with a new company, International Calculating Machines Inc., hoping to challenge the Japanese.

What puts ICM in a good position to mount that challenge is the fact that it's a wholly owned subsidiary of an MOS/LSI array maker, Electronic Arrays Inc. of Mountain View, Calif. [*Electronics*, Feb. 1, p. 17].

ICM's production line is in fact housed in a 50,000-square-foot facility at Electronic Arrays' Systems division in Woodland Hills, Calif. By the end of this month, that line will be producing calculators at the rate of about 3,000 a month, and eventually, ICM officials say, it will be able to handle 30,000 units a month.

James Johnson is ICM's vice president and general manager, and Al Kovalsky is director of marketing.

ICM's sole business is manufacturing calculators—it won't even

market them, but will supply them to original equipment manufacturers and business machine distributors. The first ICM product has been dubbed the Senator Mini-Calc by Caltype Corp., a Los Angeles wholesaler of office machines and ICM's first customer. James Hill, Caltype executive vice president, says his company has made a "sizeable commitment" for the first machine, which has an eight-digit cold-cathode tube display but can provide 16-digit answers by displaying the eight least significant bits of an answer when the user actuates the machine's alternate display key.

The machine is built with the basic chip calculator set marketed by Electronic Arrays last year [*Electronics*, July 20, 1970, p. 122]. But it's regarded by Kovalsky as only the first in a broad line that will take advantage of Electronic Arrays' MOS/LSI capability, the systems capability in Woodland Hills, and a 40,000-square-foot offshore assembly facility in Singapore.

ICM takes advantage of other people's marketing organizations, giving them the benefit of its manufacturing capability. ICM gets the chips from Mountain View, has the case made to its specifications, and assembles the whole unit—electronics, keyboard, display, and case—in Woodland Hills. The Caltype machine sells for \$395.

Kovalsky says ICM has developed a family of machines that can be implemented by reprogramming one of the standard six chips (soon to be reduced to five) to give a different function—such as an accumu-

lator, which an accountant should find attractive. Or ICM can incorporate custom chips. One likely custom job is a multiple-column printing calculator, which would require reprogramming one read-only memory of the six-chip set and designing an output chip for the printer. ICM would probably quote six to eight months for this kind of custom chip development, with Electronic Arrays doing the new design and the ROM reprogramming in Mountain View.

"But we can go to any calculator maker right now and convert him to an LSI machine to his specs by July," claims Kovalsky, who believes this capability is unmatched. "We think the leaders in the calculator business are going to be determined in the next 12 months," Kovalsky adds. "Any of the majors in this country starting from scratch now couldn't turn out a machine

Challenger. Machine, with which ICM hopes to win chunk of the calculator market, has eight-digit display but can give 16-digit answers.



this year. Our goal is to supply calculators for everyone in the industry."

ICM has a prototype of a "multiplier" calculator using six chips and a light-emitting-diode display.

Companies

Philco's closing

to spur sales scramble

The semiconductor industry is preparing to scramble for customers left without a supplier following the decision of the Philco-Ford Corp. to close its Microelectronics division. At the same time, many are wondering if any of their competitors will join Philco in folding their operations. The Philco shutdown came about four months after GTE Sylvania closed its Semiconductor division [*Electronics*, Oct. 12, 1970, p. 46].

While Philco says it will deliver on all present orders and sell the "three to four million circuits now in production," most of its contracts will have to be "renegotiated"—which, in many cases, means terminated. Philco's biggest order, \$2.3 million worth of diode-transistor logic circuits for the Lockheed Missile and Space Co.'s Poseidon missile flight-control system, will be filled. But large contracts are outstanding with Burroughs (for DTL), Japan's Yamaha (for electric-organ MOS), and "other Japanese companies."

At least one competitor, the Intel Corp. of Mountain View, Calif., stands to gain; it was engaged in a small price war with Philco over shift registers. Other potential gainers are Fairchild Semiconductor of Mountain View and ITT Semiconductor of West Palm Beach, Fla.; both Philco and ITT were making Fairchild's 930 DTL series.

Philco-Ford officials, in explaining why they closed the division that had its genesis back in the preplanar transistor days, said, in so many words, that business was bad and didn't seem likely to im-

prove. What they didn't say was that the division contributed only 2% to 3% of Philco's total business.

In the view of a rival semiconductor executive, operations such as Philco's are trivial in the corporate structure "and really a pain in the backside to management." Also, in his view, there wasn't the "full, dedicated commitment to semiconductors."

Lines in the Philco catalog include 7400, 9620, 740 MSI, and 9300 MSI transistor-transistor logic; 9908 milliwatt resistor-transistor logic; dielectric-isolated and radiation-hardened DTL; and a line of linear—op amps, hf amps, and voltage comparators. In MOS/LSI, Philco was turning out custom circuits, shift registers, counters, logic, read-write memories, seven read-only memories, and two read-write static random access memories.

A Philco spokesman says the R&D operation under Clarence Thornton will be retained. However, it will develop circuitry and systems rather than devices. The facility will examine requirements, then work with outside manufacturers. Such work will continue in the automotive area.

An effort to find a single buyer for the 415,000 square feet of manufacturing facilities was unsuccessful, so Philco will attempt to sell piecemeal—171,000 square feet in Blue Bell, Pa., 122,000 at Spring City, Pa., 84,000 at Lansdale, Pa., and 35,000 on Taiwan. There are 1,000 employees at the three Pennsylvania locations and another 1,000 on Taiwan.

Memories

New charge storage programs MOS ROM

Q. What's behind Intel's 2,048-bit MOS read-only memory [*Electronics*, Jan. 4, p. 17] that the company says it can program electrically 24 hours after receiving a customer's program tape?

A. A novel charge storage element.

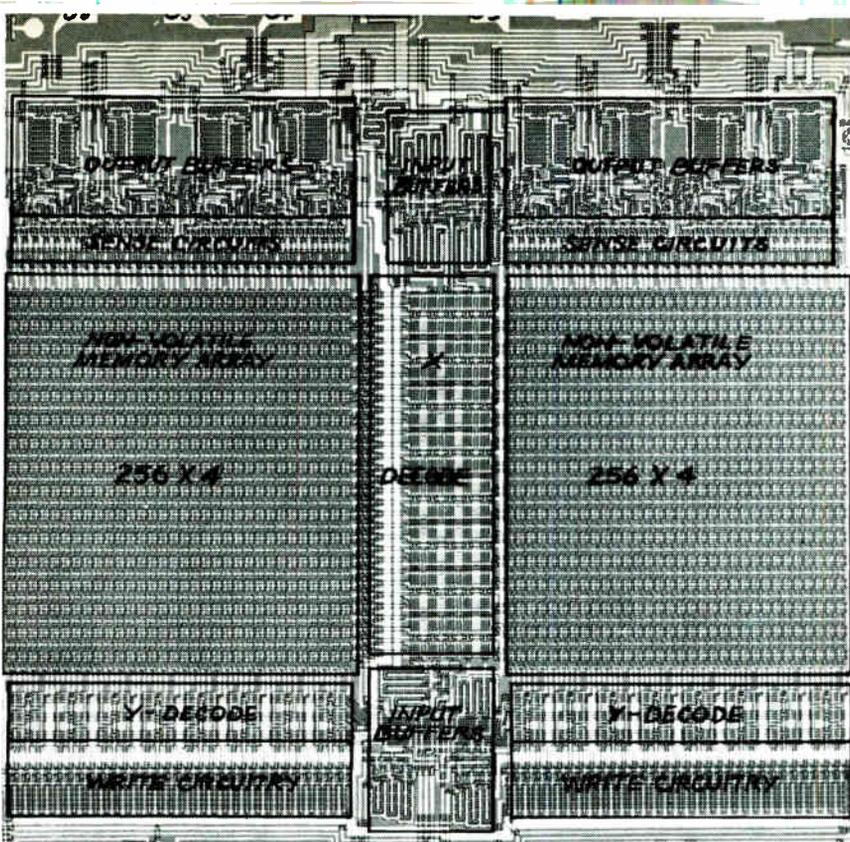
Dubbed FAMOS by Intel because of its Floating-gate Avalanche-injection MOS construction, the element, essentially a MOSFET with silicon gates, gives the ROM its advantage—its fully decoded, electronically programable features—and makes it the first programable ROM of this complexity to reach the market.

Most other approaches to electrically alterable ROMs—including metal-nitride-oxide silicon memories and metal-aluminum-oxide silicon memories—rely on charge storage in the dielectric that forms part of the gate of an isolated-gate field effect transistor. But these devices are plagued by the difficulty of controlling the electrical characteristics of the dielectric. This, coupled with the need for additional circuitry to achieve on-chip decoding, limits the approach to arrays that aren't very complex.

Intel gets around the problem by keeping the gates of its charge storage element floating (making no electrical contact), and then by trapping charge on them. Charges are transported to the floating gate by avalanche injection from source or drain junctions. (For avalanche a pulse above -30 is required.) Because the gate is floating, the electrons flowing through the oxide cause negative charge to accumulate on the gate.

For p channels, this negative charge inverts the silicon under the gate, that is, it induces conduction in a layer connecting source and drain. Thus, the presence or absence of gate charge can be sensed by measuring the conductance in the layer. And since the gate is surrounded by silicon dioxide, a very low conducting dielectric, no discharge path is available for the charges accumulated on the gate. Most of the charge will remain, it's estimated, more than 109 years at normal temperatures—a long memory indeed.

If reprogramming is required, the element can be erased and returned to initial condition by being illuminated with ultraviolet light, which causes a photocurrent from



Changeable chip. In addition to fully decoded and electrically programmable features, Intel memory, organized as 256 words of 8 bits, is TTL compatible and can operate in both static and dynamic modes.

gate to substrate. The charge cannot be removed electrically because the gate electrode is not electrically accessible. This light-zap erase technique gives Intel a simple method of correcting the entire memory array before it gets the final package seal. Further, even after the package is sealed, selective elements can be erased by exposing them to X radiation, of above 5×10^4 rads.

4,096-bit bipolar ROM boon to microprograms

Microprogramming was developed to replace control logic in digital systems. But because available semiconductor read only memories weren't fast or dense enough—speed was possible with bipolar, density with MOS—microprogramming with semiconductor ROMs has been used largely to store look-up tables and in character generators for cathode-ray-tube displays.

But that limitation may be on its way out now that Signetics Memory Systems has developed a bipolar process that enables it to produce a 4,096-bit bipolar ROM—the largest such device available to

date. And while the device will be available as an ASCII character generator, William H. Davidow, marketing vice president, says that its main use will be in the control portion of computers. "One 4,096-bit ROM in the control section can save the manufacturer over \$100 in the cost of using small scale integration." It replaces 114 dual in-line packages, says Davidow.

The savings are not in the device costs but in the cost of using the circuits. "In one study that we've done it cost the manufacturer about \$130 to implement the control function of his system. But by using microprogramming with our 4,096-bit ROM, the cost could come down to \$11.70," he says. In a calculator, for example, a floating-point option could be added with only one ROM and 1 watt of power. Davidow emphasizes the cost factor: "Even if the price of the components went to zero, the system cost will be reduced by only 30%—you have to get rid of connections and one way to do this is with microprogramming ROMs."

The 4,096-bit ROM is the first device to come out of the recently formed subsidiary of Corning Glass Works. Signetics Memory Systems

will be concentrating initially on bipolar memory products. And the key to the 4,096-bit ROM is the company's bipolar process. Davidow describes it as a thin epi (3-micron) process with Schottky clamping. "The Schottky barrier diodes allow us to produce circuits with almost no storage time," he says; the memory has a 60-nanosecond access time and a power dissipation of only 0.125 milliwatt per bit. Decoding is provided on the chip, the memory is organized as 1,024 words by 4 bits, and it's packaged in a 16-pin DIP.

Governments

Mails must go through still more machinery

While the U.S. Postal Service, which took over for the old Post Office Department late last year [*Electronics*, Sept. 14, 1970, p. 125] in an attempt to adopt a more businesslike approach to mail delivery, is not technically an arm of the Government, it still relies on Federal money. That will be the case for at least until 1985, with the payout decreasing annually.

The result is that the Postal Service's management team has been mulling a fundamental management problem: how to get more work out of the same number of men. Judging from the figures that appear in the President's fiscal 1972 budget, the solution seems to be more automation. And since development efforts lagged under the largely political former management, the only way automated systems can be obtained is through an extensive research and development effort.

As a result, the Postal Service plans to increase its R&D efforts by 72% in fiscal 1972—from the \$64.2 million approved by Congress in fiscal 1971 to the new request for \$110.5 million. The bulk of the research money, \$70.9 million, will go toward applied research and development efforts, such as continuation of the pilot postal plant at Cincinnati, Ohio, where the Postal

Electronics review

Service will be looking for improved bar code readers and small-scale computers to route the mail. The Postal Service also is expected to continue its efforts in optical character recognition which have already led to award of development contracts to IBM, Recognition Equipment Inc. in Dallas, and the Philco-Ford Corp.

The general research budget also is up, from \$7.4 million to \$11.2 million. Parts of this request are expected to go toward developing computer-aided postal vending machines and advanced research on mail-by-wire services.

Lasers

Yttrium aluminate performs at Raytheon

Studies made in the early 1960s showed that yttrium aluminate ($YAlO_3$) was potentially a good laser material but also nearly impossible to grow, and most laser experimenters forgot about it.

Now Raytheon's Roch R. Monchamp has proven the studies wrong by growing $YAlO_3$ and growing it five times faster and so less expensively than yttrium aluminum garnet, the current king of the laser rods in terms of output and efficiency. And not only is Raytheon growing it, but researchers there say they've tested it against the best YAG available and won, both in long-pulse and Q-switched operation. So far the Raytheon group's efforts have been encouraging enough to gain funding from the Air Force and Army. Work was led by Marvin J. Weber, a principal research scientist.

$YAlO_3$ outperforms YAG at nearly every turn. YAG is popular because it's hard and takes a good optical finish, but $YAlO_3$ is harder; YAG is popular because it takes rare earth dopants easily, but $YAlO_3$ not only takes a broader range of dopants, its lattice structure distributes them more uniformly. Other YAG characteristics from thermal conductivity to optical transmission bandwidth are matched or exceeded says Mon-

champ, material sciences group manager.

$YAlO_3$ is also said to outdo YAG as a laser for simple physical reasons. While YAG crystals are built up out of cubical cells; $YAlO_3$ cells are orthorhombic. This means that instead of going together in a single relative arrangement as in YAG crystals, $YAlO_3$ cells can form crystals with any of four different lattice arrangements relative to the axis of the rod.

By growing $YAlO_3$ with particular cell orientations, it's possible to get low-gain, high-energy-storage rods for long-pulse and Q-switched operation, or high-gain rods for efficient continuous-wave emission. And by picking one lattice configuration or another, it's possible to select either linearly polarized emission or emission polarized at right angles to the optical axis of the cells.

Experiments bear out the claims made for the new material. In a runoff between a neodymium-doped YAG rod, a neodymium-lutetium doped YAG rod and a neodymium-chromium $YAlO_3$ rod, the $YAlO_3$ appeared superior. In long pulse operation, the Nd-doped YAG rod saturated at an output of about 750 millijoules, the Nd-Lu YAG reached about 850, but the $YAlO_3$ hit about 1,150 millijoules.

Z-switched, $YAlO_3$ not only yielded more output, but absorbed more energy before being pumped into saturation. Nd-doped YAG reached about 75 millijoules and then saturated at about 20-joules pump energy. The $YAlO_3$ never really saturated and was delivering about 200 millijoules at 60-joules pump input when the power supply hit its own output limit.

Medical Electronics

Stanford presses work on sensors . . .

Millions of dollars are spent each month on research and development in the semiconductor industry. Since most goes for processes or techniques that could lead to

new markets or make existing markets more profitable, the commercial world overlooks some areas. At Stanford University, Stanford, Calif., however, the R&D efforts in the integrated circuit laboratory are concentrated on some of these neglected areas, one of which is biomedical instrumentation.

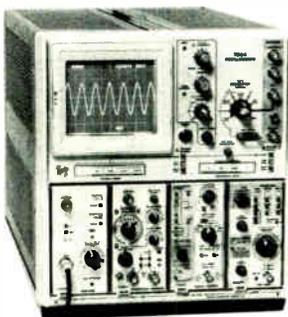
According to one lab spokesman, "our projects are oriented toward biomedical and human applications. This is partly because we have a large medical center to work with and partly because the big semiconductor companies don't like the risks involved with biomedical instrumentation." Several of these projects are described in papers given at a session on integrated electronics in biomedicine at the International Solid State Circuits Conference in Philadelphia.

According to Kensall D. Wise, one of the authors of a paper describing an IC pressure transducer, IC techniques can be applied to making implantable sensors. For instance, he says, ability to control geometries precisely on very small dimensions "promises to allow the fabrication of sensors which combine both small size and reliability. And the ability to batch-fabricate these transducers should make them relatively inexpensive."

The thin-diaphragm diffused piezoresistive pressure transducer for biomedical instrumentation that his paper describes has been developed using IC techniques. According to the developers, these devices have advantages over other types of pressure transducers in that they operate at low stress levels, have a resistance change that is a linear function of pressure over a wide range, and have a high sensitivity to pressure changes. Because of this high sensitivity, stylus arrangements for achieving pressure multiplication are not needed, and this simplifies transducer packaging.

Using IC photoengraving operations, the diaphragm as well as the sensing element—a diffused resistor—can be batch fabricated from a single starting material. The

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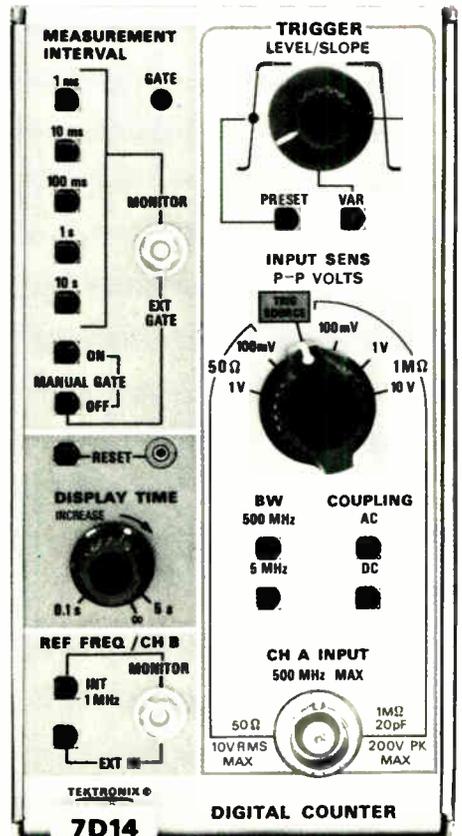
By placing the oscilloscope's vertical in the CHOP mode, the shaped signal from the counter's Schmitt trigger circuit (lower trace in both photos) is displayed directly on the CRT. The top photo shows that the highest amplitude signal is triggering the counter. In the bottom photo the level control is set to a point where it also triggers on a lower level signal so there are two outputs from the Schmitt trigger and, therefore, twice the frequency is indicated. Ambiguous readings are no longer a problem when you can see what you are counting.

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Electronics review

completed sensor consists of a circular silicon chip with an outer diameter of 1.6 mm and an active diaphragm 1.2 mm in diameter and 5 micrometers thick. Four resistors are diffused into the diaphragm area and interconnected to form a bridge network. The supporting rim is 50 micrometers thick, which is the thickness of the original silicon substrate.

The chip is mounted in the tip of a small catheter, which provides the reference pressure to the back of the diaphragm, as well as a means of electrical connection to the chip. A typical catheter has an inside diameter of about 0.8 mm (32 mils) so the researchers are now working on reducing the size of the transducers from the present 1.6 mm to 0.8 mm.

... and reading aid for the blind

Another Stanford University researcher, R. A. Nordstrom, will discuss a new compound transistor structure, the field-effect modified (FEM) bipolar transistor, which will possibly be used in the imaging array of a reading aid for the blind. It operates in the charge storage mode and, according to Nordstrom, offers an order-of-magnitude improvement in responsivity over a comparable conventional phototransistor. Other possible applications include an illumination-to-frequency converter and an inverter with high noise-immunity for digital circuits.

The device contains an annular gate region, which is formed during the emitter processing step and is connected to the collector. Fabrication is such that the channel between internal and external base becomes depleted or pinched off when the collector-base junction is sufficiently reverse biased. The FEM transistor base region is therefore similar to a p-channel junction FET. In effect, the FET gate and the bipolar collector are the same.

The difference between the FEM device and a regular transistor is that in the conventional transistor,

the entire base-collector junction contributes to the total internal capacitance while only the area inside the annular gate contributes in the FEM transistor. Because of this lower capacitance, the FEM device is more responsive—it has a higher output voltage than a regular device for the same input illumination. Nordstrom says that because the FEM transistor employs standard fabrication technology, he expects to see it used in ICs.

Receiver extends implant battery life

The use of battery-operated, implanted telemetry systems for biomedical instrumentation is growing rapidly. In most cases flexibility and operating lifetime are severely limited by the capacity of the power source.

However, P. H. Hudson, now with the Electronic Components Laboratory at the Army Electronics Command, Ft. Monmouth, N. J., has developed a novel monolithic micropower command receiver that can extend operating lifetime of an implanted telemetry package almost to the shelf life of its battery. The approach is simple: the receiver disconnects the power source when the system is not in use.

The command receiver consists of an rf amplifier, a-m detector, and audio amplifier. Sensitivity is better than 100 microvolts and total power dissipation is less than 15 microwatts. It is designed to operate from a single 1.35-volt mercury cell and is fabricated entirely on a single silicon chip. The only necessary off-the-chip components are the antenna and the battery.

Hudson, who did the work while at Stanford University, says that the tuned rf a-m receiver offers the lowest power drain and requires the smallest die size among several possible monolithic command receiver designs. Receiver power drain depends primarily on gain and frequency response of the rf amplifier. He says that for low power drain, both operating fre-

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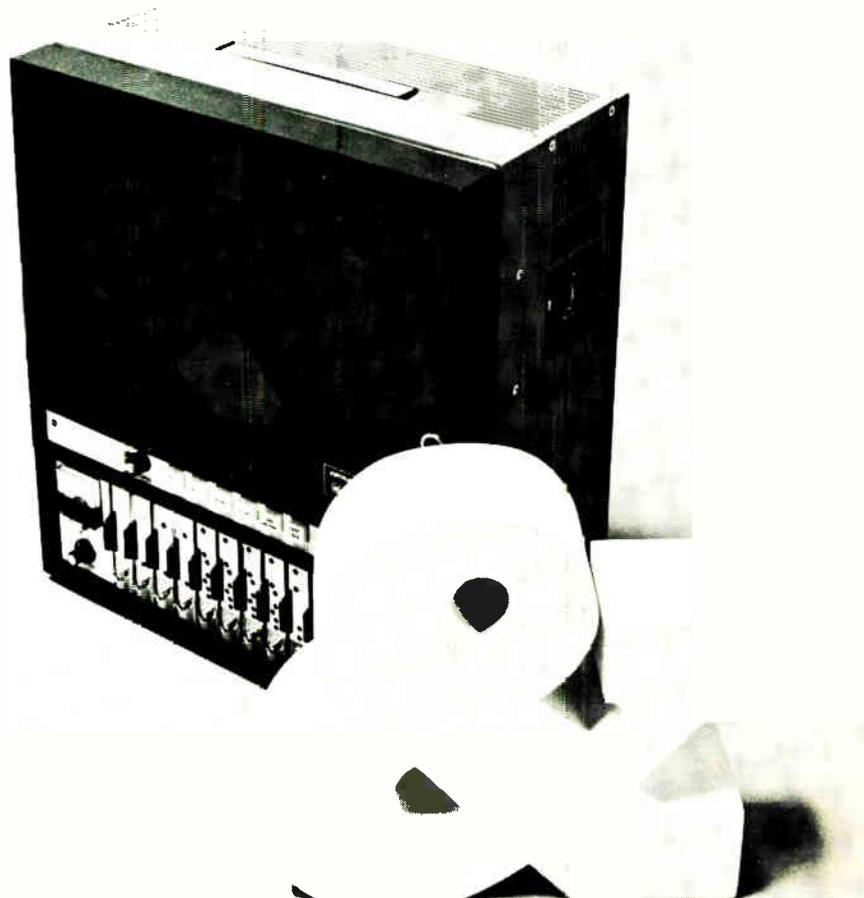
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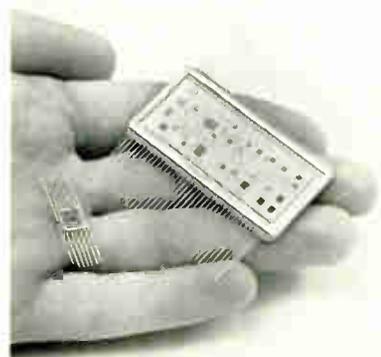
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Electronics review

quency and voltage gain of the rf amplifier should be as low as possible. A carrier frequency of 500 kilohertz (in the distress calling band) was chosen as a reasonable compromise between conflicting requirements for low power dissipation and a small, efficient receiving antenna. An rf voltage gain of 10 is required to achieve receiver sensitivity of $100 \mu\text{V}$ and a signal-to-noise ratio of 12 decibels.

The two-stage amplifier, or "gain cell" as Hudson calls it, is used as the basic building block of the command receiver. Its function as a 500-kHz amplifier, an a-m detector, or an audio amplifier is largely determined by selecting appropriate load resistor and coupling capacitor.

The gain cell employs a diode-biasing technique that avoids the need for prohibitively high-value resistors. Due to the high circuit impedance level, it uses small-value monolithic coupling capacitors. What's more, the cell has a mid-band voltage gain that is relatively insensitive to resistor tolerance; essentially no power is wasted in biasing networks, and it provides two stages of amplification using only three isolation wells.

Solid state

GaAs device doubles as microwave switch

Engineers at the RCA Corp. have developed a gallium arsenide field effect transistor that can serve as a microwave switch—and it can be controlled by the infrared emissions of 1.5 microns, normally found in an ordinary flashlight beam. When the device is fabricated as a thin wafer and inserted in a waveguide, its surface resistivity can be changed from absorption to reflection simply by shining a light on it. The work, done at RCA's David Sarnoff Research Center in Princeton, N.J., wasn't aimed at a particular application.

Unlike ordinary FET phototransistors, the RCA development contains a semi-insulated, chromium-

doped substrate under the n layer. And if the n layer is depleted, the device becomes an insulator with no conduction in either the channel or the substrate. In other FET phototransistors, a metal gate contact, rather than a block of insulation, remains after depletion. Since microwave energy can be absorbed when the n layer isn't depleted and reflected when it is, the new device can act as a microwave switch. "It's the first FET phototransistor in this category," says G. A. Swartz, one of the three authors of a paper on the new device presented at the International Solid State Circuits Conference in Philadelphia.

When a voltage is applied to a metalized contact on the substrate, current flows between the source and drain on the n layer. The n layer becomes positively biased and the substrate negatively biased, causing an electric field to appear between the n layer and the substrate contact. The result is a voltage drop across the substrate and a different drop across the p⁺n junction between the n layer and the substrate. The bias across the p⁺n junction depletes the n layer but not the substrate—because there are more chromium atoms in the substrate than donor atoms in the n layer.

As a light is shined on the substrate, it excites the electrons from the chromium sites, depleting the n layer and reducing the substrate resistance to a preset value, say 377 ohms. In this case microwave energy is absorbed.

While it can handle microwaves, the new FET phototransistor can't switch as fast as ordinary microwave switches because light has to pass through the high-resistance substrate to the chromium sites. Its switching speed ranges from about 1 millisecond to less than 0.1 millisecond; sensitivity is 1 microwatt per square centimeter. The small signal gain is 30 decibels, and input and output impedances are on the order of a few megohms and 1 kilohm, respectively. Both can be varied by the amount of applied bias. Operation is restricted to 140°C, 60°C lower than for ordi-

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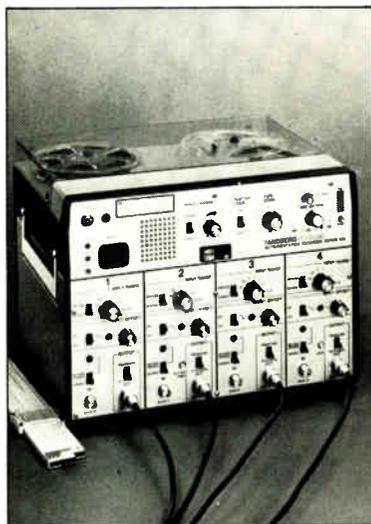
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Electronics review

nary GaAs devices.

"Construction is almost trivial," says Swartz. Starting with a substrate and vapor-phase-grown GaAs, an n layer is grown on the chromium-doped GaAs. Metalized contacts then are attached to the device's surface to accept the bias. Care must be taken in fabrication of the n layer, since impurity layers between the p⁺n junction will affect performance. Present lab yield is close to 100%, says RCA.

Integrated electronics

Beam-leaded transistors offered in quantity

Beam-lead transistors and ICs, recognized as a vast improvement over conventional wire-bonded chips in hybrid circuits, haven't been available in quantity for most users. Now, Texas Instruments is bringing out its first standard beam-lead products, and they will be available in production quantities. And marketing manager Richard L. Cunningham expects them to be competing with plastic transistors in as little as two years.

Up to now, beam leads have been used mainly in high-reliability military applications. Here, their silicon nitride passivation eliminates the need for hermetic packages, and the titanium-platinum-gold metallic compounds of aluminum and gold (purple plague, white plague, and so on), that can make devices unreliable. At the same time, they weigh less and occupy less space than the smallest packaged transistors and ICs.

TI has been supplying hybrid circuits using beam-lead transistors and other devices for some time, chiefly to Western Electric for the Safeguard program. But Cunningham points out that different features of beam lead devices make them attractive in different markets. For consumer use, low price is vital, and mill prices are now relatively high, high volume would change that dramatically. Even in volume, the chips would still cost

more to manufacture than the conventional chips used in plastic transistors. But they don't require a lead frame, encapsulant, or, most significant, the labor of assembly and bonding. Because of this, Cunningham says, beam-lead devices can be competitive in price with plastic transistors when the volume gets high enough. He says that's at least two years away because of the difficulty of persuading manufacturers to convert from one assembly method to another.

The first products will be an op amp, npn transistors, pnp transistors, a single diode, and nine diode arrays. In development are a core driver, n-channel FETs, and a 1.5-gigahertz transistor. As for prices, TI won't discuss them for over-1,000 orders, but would say that they are below those for regular transistors.

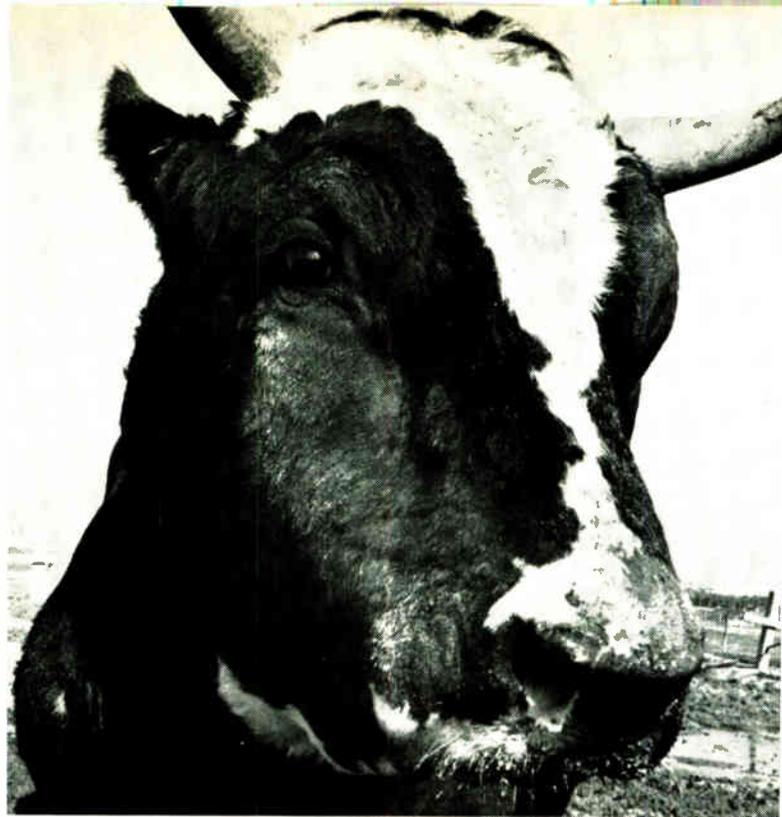
Another market for beam-lead transistors is high-speed computers. Here they can replace miniature plastic transistors in "discrete" emitter-coupled logic circuits. This construction permits the use of optimized transistors and produces lower capacitances than with monolithic circuitry. The result is higher speeds than possible with monolithic ECL.

The obvious cloud over Cunningham's plans is the monolithic circuit. However, he feels that it will be a long time—if ever—before ICs eliminate hybrid circuits. Techniques such as beam-lead bonding reduce formerly high hybrid costs, and many circuits such as high-frequency and high-performance amplifiers may well continue to resist complete integration.

Communications

Modem has built-in error detection

In most data communications systems the error-checking function is performed by the computer in a stop-and-wait manner—data transmission is stopped while the check is going on. Now there's a modem that can check for errors while



Theirs.



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If 1970 was the year of the RAM, then 1971 begins to look like the year of the Bull. Not that proclamations announcing the death of core memories are any news to us. We've been listening to them ever since we started to build core memory systems back in the fifties. But the cacophony has built to a shrill new high. And some of those who shout the loudest have lost track of where enthusiasm leaves off—and irresponsibility begins. It is our old-fashioned feeling that the main reason for advertising is to tell you about new products. Not new hopes, but new products. Not new possibilities, but new products. Products that we have developed and tested. Products that we can and do deliver. We don't want to sound too holy. A perfect track record isn't one of our claims. But leadership in core technology is.

Incidentally, that's the main ingredient of all our new products for 1971. Core. We've built more different types than anybody. For almost two decades. And, frankly, we know more about core memory systems than anybody. So, once again, we have a series of new memory products—that use core.

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transmitting data at 4,800 bauds. Acknowledgement data is sent at 150 bauds on a reverse channel. And since the modem does the error checking, the computer is free to perform other tasks.

The new modem has two hard-wired special-purpose computers. One computer, an error-detection algorithm, employs an error-detection Bose-Chaudhuri code to yield an undetected error probability of 1 in 10^{12} . "This is the function that all other modems leave to the computer," says Carl Nordling, director of product management at Paradyne Corp., Clearwater, Fla., developers of the modem.

The other special-purpose computer actually is a digital filter that performs automatic equalization. Its function is to increase the system's signaling rate by equalizing of the dial-up telephone line's delay distortion. According to Nordling, this circuit will equalize 95% of all dial-up lines.

The new modem was designed by Paradyne to interface with the IBM 2780 terminal, something that the 4,800-baud Bell 203 modem can't do without costly hardware and software changes. If the new modem is put into the 2780 system as a replacement for a 2,000-baud Bell 201A modem, the throughput speed of line printers and card readers can be increased by as much as 300%. For instance, printing speed can be hiked from 100 to 240 lines per minute when an IBM printer is used, and can be as high as 400 lines per minute with a high-speed printer.

The modem is available in three versions: a unit for original equipment manufacturers, a direct replacement for the Bell 201A in an IBM binary synchronous channel system, and a parallel interface version that looks like a peripheral device, such as a magnetic tape unit.

All three are priced at about \$6,000. All can operate in either full or half duplex.

Transistor-transistor logic is used in the modem, while the buffers are MOS registers. All the filters are operational amplifiers. The entire

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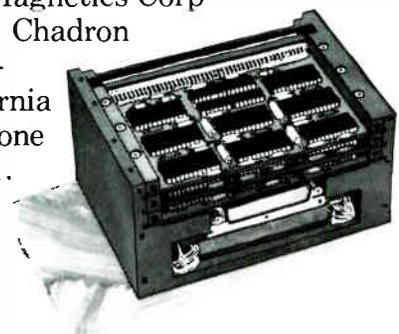
In construction, we've gone from wired-in cordwood modules to plug-in printed circuit modules. And we've

used monolithic IC's and hybrid data loop circuits in ceramic dual-in-line packages. The unit is therefore field repairable and easy to maintain.

Lest all that jazzy semiconductor talk should lead you astray, the SEMS-8 memory is built out of (dare we say it?) core. 20 mil lithium core. But don't worry. It's so small and light, your friends need never know.

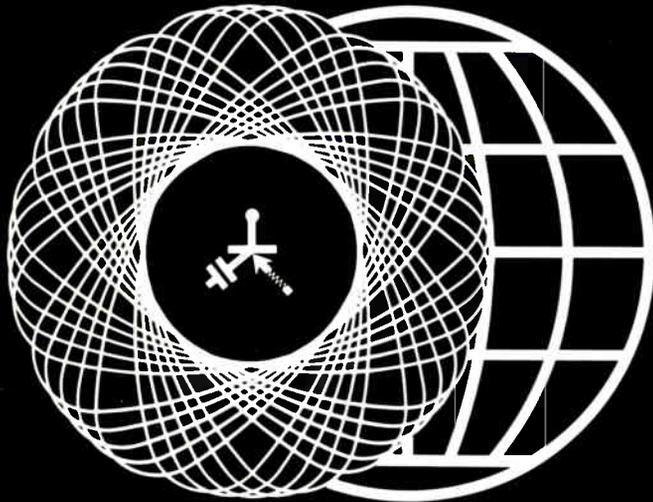
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EM Electronic Memories is a division of Electronic Memories & Magnetics Corporation, 12621 Chadron Avenue, Hawthorne, California 90250. Telephone (213) 644-9881.



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Marketing

New alliance to aid smaller firms

A cooperative move by a manufacturer's representative and a group of 12 distributors in the New York metropolitan area could offer an opportunity for smaller manufacturers to keep pace with the state of the electronic art.

The representative is Comtronic Associates of Garden City, N.Y. The 12 distributors are in northern New Jersey. Notes Murray J. Gallagher, Comtronic vice president, "Up to now, a rep just hasn't had the time to call on smaller companies. And the distributor finds himself dealing mostly with purchasing agents. The result has been that those companies find themselves using outdated components for the systems they make, components that actually cost them more money."

Gallagher says that his company has pinpointed 700 manufacturers in New Jersey as potential customers of the representatives and distributors.

"Those smaller companies," he adds, "will now have access to the engineering service, consultation, and design help that formerly was available only to the high-volume customers. And we, of course, hope to steer more users to the lines we represent."

Gallagher hopes to add seven or eight sales engineers to his staff.

For the record

Rush wire. The race for quick-turnaround wiring schemes that replace printed circuit interconnections has gained another contestant—Infobond, a method for putting wires on printed circuit boards with a numerically controlled head. It's offered by Infobond Corp. of Burlington, Mass., a spinoff of Inforex Inc., the manufacturer of key-to-

Electronic Memories gently draws your attention to an off-the-shelf planar stack so small that it will fit most commonly used printed circuit boards.

We built this one to solve our problems with the mini-computer people—and their problems as well. Yes, it's low cost: competitive with any other low cost planar stack on the market. Yes, it's off-the-shelf: we can deliver in volume in sixty days or less.

But the main point is this: the size is so small that you can fit this baby on just about any type of PC board. It's 1/2" high x 6" wide x 6 1/2" deep. And in that little package you get 4K x 18 bits of core storage. At a price no semiconductor can match. To the mini-computer designer, this means an immediate core memory source regardless of the system's physical room for storage area.

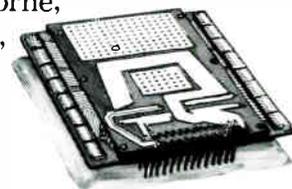
The stack will operate at either 700 or 800 nanoseconds, depending on whether you order 18 or 20-mil diameter core. Extended temp cores are standard for operation from 0 to 70° C.

The rather unusual "folded" design gives you almost fifty percent decrease in drive line inductance. Winding impedance and uniformity compares favorably to the compact frame designs. Much better than other planars.

Incidentally, we held a contest to find a good name for this stack. It is now called the EM 2220. Just goes to prove that we know more about core than about fancy names.

Here and Now: EM 2220 is in limited production for off-the-shelf delivery. Come in and we'll show them to you. Figure about sixty days for volume orders.

EM Electronic Memories is a division of Electronic Memories & Magnetics Corporation, 12621 Chadron Avenue, Hawthorne, California 90250, (213) 644-9881.



("I still think a couple of 'incredibles' would help.")

In the United States there are two more possibilities how to make the coming decades your most successful ones.

1st possibility

**To record
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Kienzle*
Digital Printers
offer considerable
advantages.
Parallel input,
incorporated
read-out unit
for BCD outputs
or 1-out-of-10
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Kienzle*
Digital Printers
are available as
tape printers or
with motor-returned
carriage and,
upon request,
also with card and
tape punching units.

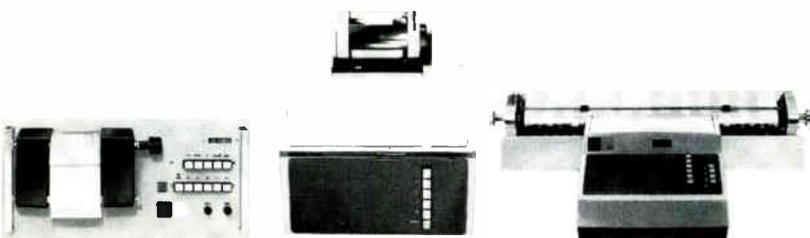
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are a novelty
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For the distribution
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Electronics review

disk computer input systems. Info-forex systems have used the Info-bond process for a year and a half.

The key step in the process is in sublimating the insulation on the wire to make the solder bond. Four-mil wires are laid down between guide pins and soldered to pads on the board, which is etched to carry only power and ground to the ICs. The insulation is a proprietary compound of the polyurethane type.

In operation, the board moves under the bonding head until the pad is directly beneath it. The head, which has the insulated wire running down through it, descends, its tip is heated with a short pulse of current, the insulation melts, and the wire is pressed against the solder-plated pad. As the heat from the wire melts the solder, a blast of nitrogen surrounds the pad for an inert atmosphere. A cooling air blast is applied, and a probe checks continuity to see if the bond has actually been made. The board then moves to the next position to be connected. At the end of a wiring net, a cutter clips the wire, and the probe then checks for an open circuit.

Home. Illiac 4, the super-size computer, will be moved to the Ames (NASA) Research Center in Mountain View, Calif., when it's completed. The computer, being built by the Burroughs Corp. in Paoli, Pa., for the Defense Department's Advanced Research Projects Agency, under a subcontract from the University of Illinois, will be tested in Paoli and then shipped to Ames early in 1972 for final assembly and evaluation. The computer will be owned by the Defense Department and operated by Ames. The university will be responsible for construction and development of system software. It also will be able to do research using the machine through the ARP network as will the Defense Department and other universities.

In the chips. Now that Mostek has announced its one-chip calculator [*Electronics*, Feb. 1, p. 19],

Electronic Memories unobtrusively mentions the development of its 7.3 million bits-per-module Megamemory 1000; very compact, but a little too large to be unobtrusive.

Speaking gently about this little monster is a little like talking baby talk to a five hundred pound gorilla. (Actually, maximum weight is only 350 lbs.). But its speed belies its bulk: full cycle time of 1.5 microseconds and access time of 850 nanoseconds. You get a wide range of storage capacities—from 32K by 160 to 54K by 14. It's definitely a compact monster. A patented drive/sense scheme eliminates several switches normally associated with 2 wire 2 1/2D design. This straight-forward, practical design approach enhances reliability and breaks through price barriers that have always restricted core memory use in large-scale storage applications. As an add-on memory, Megamemory 1000 has been designed for interface with virtually any

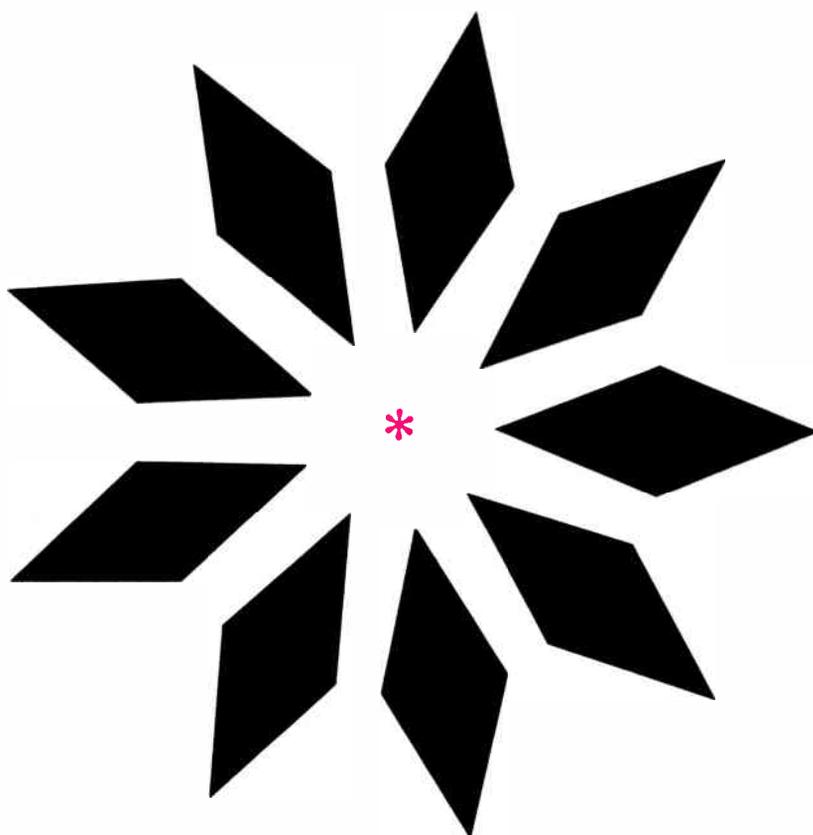
customer specification. If you need fast large storage either as an extension of your main frame memory or for peripheral memories, it would be difficult to conceive of a more compact, faster or more economical solution. But... you never know.

Here and Now: Megamemory 1000 is a little too large to lug to your place for a demo. But it's working at our place. We don't claim off-the-shelf deliveries, but we are geared up to produce. Fast.

EM Electronic Memories is a division of Electronic Memories & Magnetics Corporation, 12621 Chadron Avenue, Hawthorne, California 90250. Telephone (213) 644-9881.



("Did we tell them to call it Supercore or Epicore?")



Complete HF Receive Antenna capability in a 50 meter circle

How Hermes did away with vast rhombic or log-periodic antenna farms shoed away by a shrewd array ...

Take 1 meter diameter loops 4 meters apart and get an omni directional broad-band receiving array. covers 2 - 32 MHz

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Electronics review

Texas Instruments says its entry in the one-chip market should be in production by June [*Electronics*, Nov. 23, 1970, p. 83], and will sell as a standard product for less than \$15 in 25,000 quantities. The chip is a four-function, eight-digit calculator. Three registers provide constant multiplication or division, and there is a full-floating decimal point.

At the same time, Japan's Canon Corp. has increased its order for TI thermal print heads to go into Canon's Pocketronic calculator [*Electronics*, Jan. 4, p. 17]. Canon says it soon will start exporting the machines, and that sales in the U.S. will begin next month. The company is also considering production of another calculator with a light-emitting-diode readout.

Turnabout. Tektronix Inc. has substituted 10 "unpaid nonwork-days" for layoffs announced in December [*Electronics*, Jan. 4, p. 28]. Howard Vollum, president, hinted that things may be looking up when he said that "orders have ceased to decline."

Slash. IBM has made several moves that seem calculated to discourage peripheral-making competitors. First, it discontinued extra-time charges for its major disk storage units [*Electronics*, Dec. 21, 1970, p. 26]. Almost simultaneously, it brought out new versions of its 2319 disk unit that were usable with several different models of the 360 and 370 computers. The hooker in this 2319 announcement: the machine is mechanically almost identical to the older standard 2314 disk storage unit, but sells for substantially less—and therefore, in the opinion of most observers, amounts to no more than a bargain-priced 2314.

Now, IBM has struck again. It has introduced big discounts for purchasers—not lessors—of two System 360 models, the 2361 large core storage, and the original eight-spindle 2314 disk unit, which gave way some time ago to newer one-, two-, and four-spindle drives prior to the introduction of the 2319.

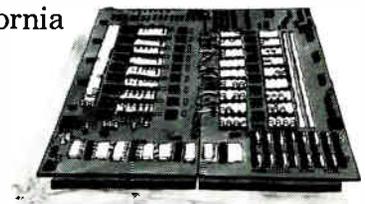
Electronic Memories discreetly suggests a very low cost system for expansion modules or smaller main frame memories and that may even replace some disc memories: Micromemory 4000.

We recommend you read carefully. Because there's been a lot of wishful talk about a product like this one. The big difference is that we actually have it. We're talking about a 32K x 18 bits card type memory with control logic that allows it to be operated as 65K by up to 9 bits. Cycle time is 1.5 usec and access time is 800 nsec. And, starting April, we can deliver this memory off-the-shelf. By that we mean within days from receipt of order. Not weeks or months. And we don't want to talk price in this message; but we will say that the cost will cause many computer manufacturers to review their "make-or-buy" decisions. If you've been searching for a truly low-cost main frame memory or reliable expansion modules, we can assure you that this new family of "Micromemories" will open up

a whole new area of system thinking. With regard to disc memories. With regard to claims you have seen or heard about semiconductor memories. With regard to other claims about low-cost core memory systems. If you have system responsibility, you really owe it to yourself to get the full details on our "Micromemory" family.

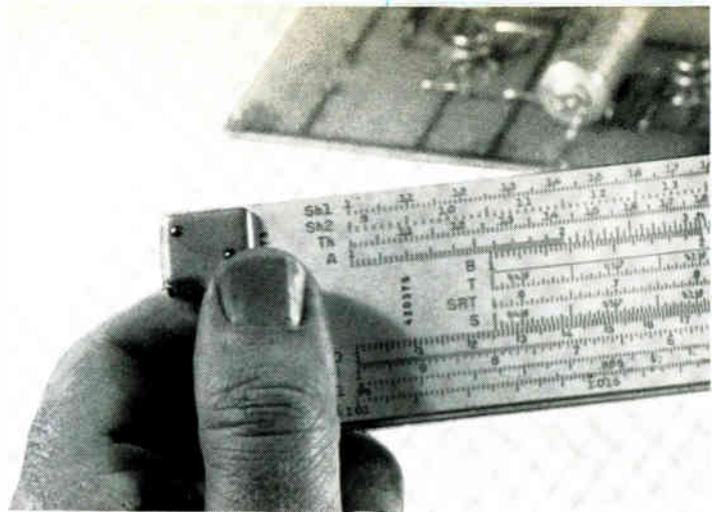
Here and Now. This ad is just a few weeks premature. The design is fully proved and tested. The prototypes are in existence. But our claim to production quantities will have to wait until April.

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("Just one little 'new-and-sensational' wouldn't hurt.")

RCA Solid State Data for Designers



3N200—the last word in RF amplifiers up to 500 MHz

Looking for excellence in UHF performance? RCA's 3N200 dual-insulated gate MOSFET boasts a "pedigree" at 400 MHz that reads like a performance checklist for military and industrial communications, aircraft and marine mobile equipment, CATV, MATV, telemetry and multiplex equipment. 3N200 features: high unneutralized RF power gain

- 12.5 dB (typ.) at 400 MHz

dual-insulated gates

- wide dynamic range
- low cross modulation
- simplified AGC circuitry
- operation at maximum gain **WITHOUT NEUTRALIZATION**

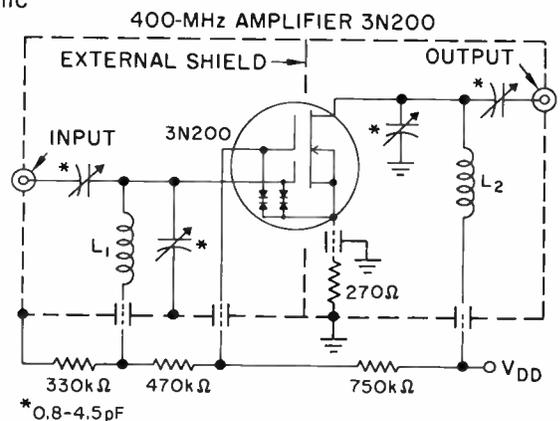
integral back-to-back diodes

- bypass transients exceeding approximately ± 10 volts
- symmetrical diode characteristics preserve wide dynamic input range

low noise figure

- 4.5 dB (typ.) at 400 MHz
- For technical data, circle Reader Service No. 314.

400 MHz high-gain, low-noise amplifier using the RCA-3N200.



Op amps rated for higher current output at no increase in price

Where output power up to $\frac{1}{4}$ watt is a major consideration, look into RCA's

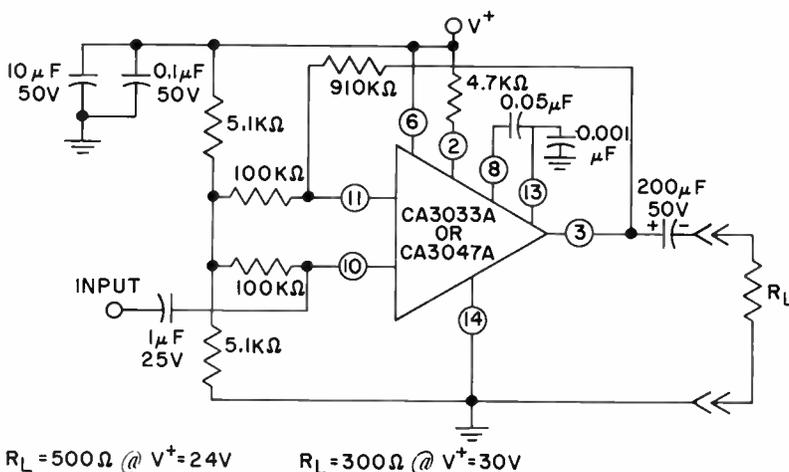
premium op amp types CA3033A and CA3047A. Now characterized for operation at ± 15 V, these high-gain op amps can handle up to 76 mA mini-

um peak-to-peak output current and 255 mW typical sine-wave output power. And they still offer you outstanding economy! The RCA-CA3033A in 14-lead dual-in-line ceramic package still costs only \$4.90 at the 1,000-unit level; the CA3047A in 14-lead dual-in-line plastic package, only \$2.90 at the 1,000-unit level.

In response to many requests for information on how to use an op amp with a single power supply, the schematic at left shows a practical hookup for such an application.

Use either the CA3033A or CA3047A with a single 30-V supply. With $R_L = 300$ ohms, this circuit provides 255 mW output and a swing of 25 V, with less than 5% distortion.

Want to know more? Circle Reader Service No. 315.

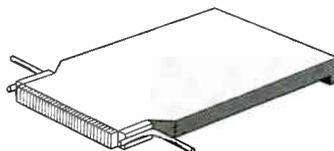


RCA offers new modular approach to GaAs laser arrays

The RCA TA7789 and TA7790 arrays of gallium-arsenide laser diodes, connected in series, are designed for gated viewing, security illumination, target designation, and other high average power applications.

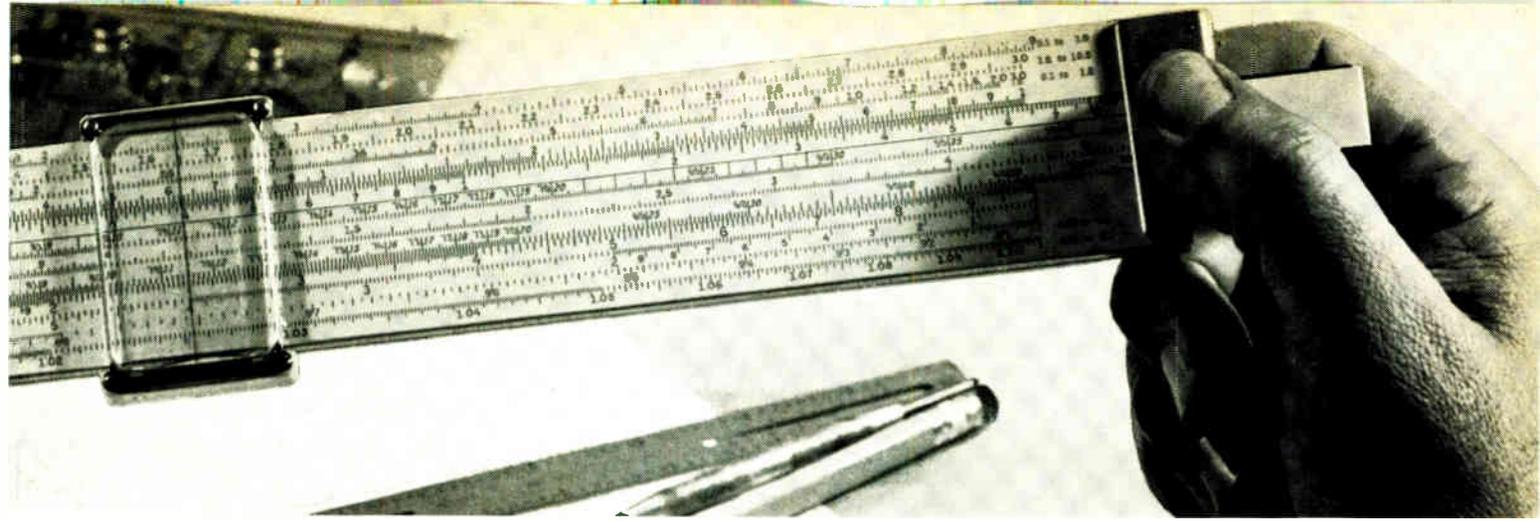
Smog? Fog? You can cut through

them with these laser modules that operate at cryogenic temperatures. The TA7789 and TA7790 can be used to make high average-power arrays



and custom arrays, because each module contains a keying tab to locate it in proper relationship to others, allowing them to be stacked side by side or on top of each other to meet increased power-output requirements.

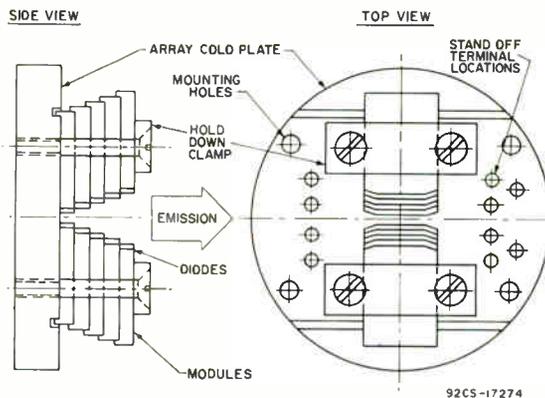
For military, industrial, or commercial optoelectronic systems, the TA-7789 and TA7790 feature power outputs of 50 to 100 watts peak, or 1 to 4



watts average, respectively; power efficiency of 20% minimum; a duty factor of 4%, and a peak emission wavelength of 8525 Å at 77°K.

Circle Reader Service No. 316. for further information.

Typical stack of 10 RCA TA7789/TA7790 modules

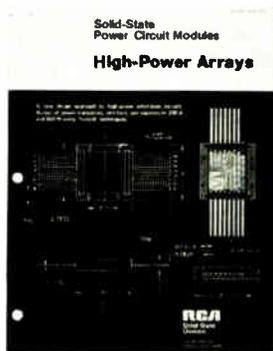


Available now! New RCA booklet features circuit module high-power arrays

Should your next generation of power circuits use hybrids? You should certainly consider this approach if your power circuits:

- cost more than a few dollars
- utilize power semiconductors
- are reasonably complex
- employ over 10 components

RCA's new brochure, "Solid-State Power Circuit Modules" (HPA-100), illustrates an array and building block approach to power hybrids which is unique in the electronics industry. With standard products outlined in this new RCA brochure, you can obtain current capabilities to



300 A and power handling to 800 W.

Following are listed some of the typical circuit categories which can be constructed using power hybrid technology to advantage:

- 40 A printer paper advance circuits
- 200 A servo motor controls
- battery operated vehicle controls
- 50 A variable speed induction motor controls
- 5 kW inverters

Thus, if you are considering next generation equipment and the best approach to it, ask your

RCA Representative how RCA power hybrids can provide you with the key to both price and performance!

To order your copy of the RCA Solid State Division's detailed brochure HPA-100, circle Reader Service No. 317.

applications, this series of SCR's from RCA is made for you. They permit operation at frequencies as high as 25 kHz... with reduced-size magnetic components!

Let us know if your circuit demands *greater* limits of stress than listed in the preceding table:

For technical data on RCA's fast-switching SCR's, circle Reader Service No. 318.

These 400 V power transistors can become your standards for off-line conversion

Cut the size and weight of the power transformer, eliminate the heat sinks, get added savings on the chassis—and thereby reduce the size and cost of your power supply. The RCA 2N3585, 2N5240, 2N5840, 2N5805, 2N6078 (TA7673), and TA7007 families of power transistors are cost-saving leaders that can do a big job. They're all 400-volt devices, and they give you a current choice from 2 amperes to 20 A.

Family	Package	Power Output (W)	Ic Max. (A)	Ic (for beta of 10) (A)
2N3585	TO-66	125	3	2
2N6078 (TA7673)	TO-66	250	5	3
2N5240	TO-3	250	5	3
2N5840	TO-3	250	5	3
2N5805	TO-3	500	10	5
TA7007	TO-3	1000	20	10

The right combinations of these units for your particular applications can become your standards for off-line power conversion. And there's an added benefit: with RCA silicon power, you isolate from your power line for a new dimension in safety. Circle Reader Service No. 319.

For price and availability information on all solid-state devices, see your local RCA Representative or your RCA Distributor. For specific technical data, write RCA, Commercial Engineering, Section 70B-15/UM7, Harrison, N. J. 07029. International: RCA, 2-4 rue du Lievre, 1227 Geneva, Switzerland, or P.O. Box 112, Hong Kong.

RCA Solid State Division

Fast-switching SCR's from RCA can revamp your power supply designs

RCA's 40555, 2N3650 and TA7395 fast-switching SCR's give you a performance range from 5 A to 40 A,

family	rms current	di/dt	dv/dt (min.)	turn-off time (max.)
40555	5 A	200 A/μs	100 V/μs	6 μs
2N3650	35 A	400 A/μs	200 V/μs	15 μs
TA7395	40 A	400 A/μs	200 V/μs	15 μs

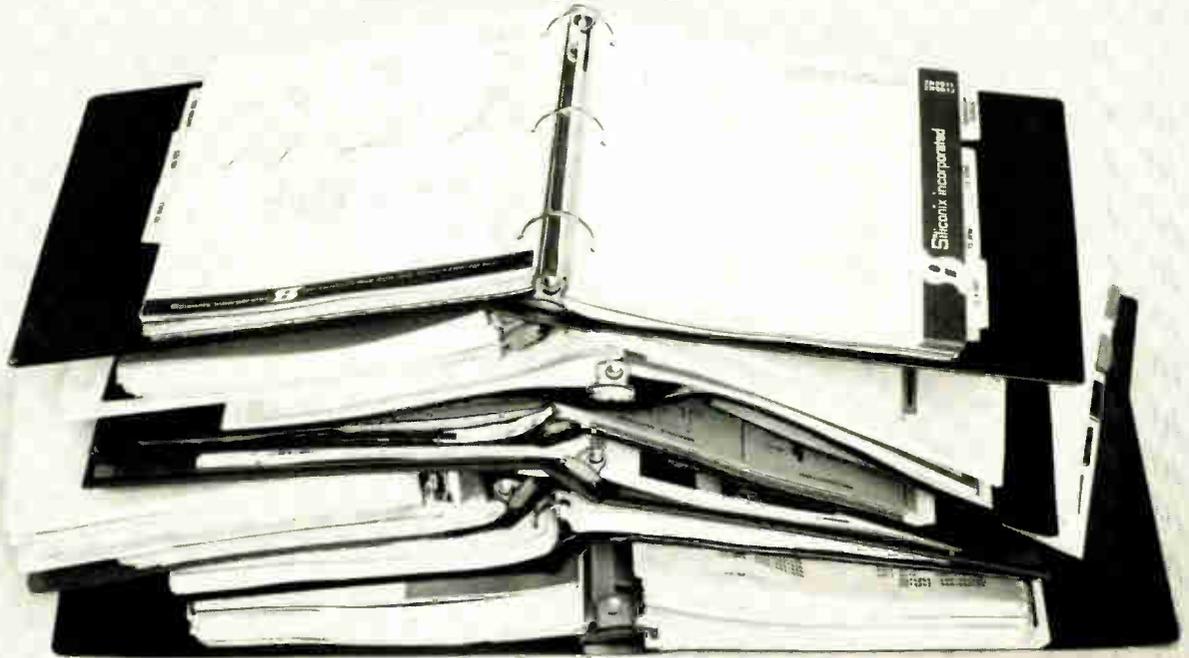
from 100 V to 600 V. The selection of one of these devices for your fast switching circuits can help you enter the "miniaturization race" by reducing size, weight, and system cost.



TA7395/2N3653 — actual size.

If you are designing high-speed switching circuits for power inverters, radar pulse modulators, switching regulators, or other high current pulse ap-

Why search any further?



Since we have the industry's most complete line of monolithic and matched dual FETs, it's almost certain you'll only have to "one-stop" shop... at Siliconix.

Reliability? Every unit is manufactured to meet MIL-S-19500. In fact, our entire line exhibits performance that actually goes beyond the standard industry ratings.

Our data sheets spell out the details, but here are some excerpts. Our U280 series monolithic duals and 2N5196 series matched pairs for general purpose use. For high frequency applications our matched pair 2N5911 series has a



Monolithic Dual FETs

typ. g_m of 6,000 μmho . The 2N5906 series has a 1 μA max. input current.

Low noise? The 2N5515 series exhibits input noise less than $10 \text{ nV}/\sqrt{\text{Hz}}$ and $\text{CMRR} > 100 \text{ dB}$.

Look at it this way. When you order from Siliconix, you no longer have to pour through hundreds of data sheets. Or circle bingo card after bingo card. Or even pray that a delivered unit's performance matches its printed specs.

All you have to do is call your Siliconix representative. When you do you'll be ordering from the source with you in mind.

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Washington Newsletter

February 15, 1971

USAF's B-1 likely to be attacked by 92nd Congress

Watch for the 92nd Congress, led by Senate critics of defense spending, to add the Air Force B-1 advanced strategic bomber and its \$370 million budget request to the list of programs to be cut back or killed (see p. 109). This is the word from Capitol staffers readying for hearings on the Nixon budget, which asks \$295 million in new money for the North American Rockwell aircraft program.

The new plane is considered more than usually vulnerable in view of reports that it has divided the Nixon administration. "It's Packard's baby," says one source, referring to Deputy Defense Secretary David Packard and the report that he threatened to resign late last year when the B-1 funding request was challenged by George Shultz, director of the Office of Management and Budget, acting for the White House.

Tri-Tac switch to get \$18 million in fiscal 1972

Specifications for the wideband digital switch planned for use in Tri-Tac, the tri-service tactical communications system that has been substituted for the defunct Project Mallard, should be written by the end of February. So says Tri-Tac's overseer, Louis DeRosa, assistant to the Secretary of Defense for telecommunications. He adds that the Tri-Tac switch is programmed for \$18 million in fiscal 1972 outlays, of which \$8 million will be drawn from reprogrammed fiscal 1971 funds. Up to 150 switches costing between \$500,000 and \$1 million each will be needed in the 1975-76 period to shunt secure voice and data traffic over highly survivable satellite and microwave circuits.

NSF supports growth of EDP in education ...

Companies anxious to discover money for increasing the applications of computers to education will find \$8.4 million in the National Science Foundation's fiscal 1972 budget request. That figure, \$2.4 million above the present level, represents nearly all of the \$2.5-million increase in the NSF's \$17.5-million account for education and research computing.

A breakout of the NSF account shows, in fact, that research applications money is down \$400,000 to \$4.1 million, while engineering funds jump \$500,000 to \$5 million. Industry sources attribute the reorientation of funds to the desire of White House science adviser Edward David to expand uses of existing technology in society.

... but support lessens for engineering schools

White House efforts to reorient national priorities—and the economy—to peacetime goals will be reflected in declining fiscal 1972 support of university research and development by the Pentagon, NASA, and the Atomic Energy Commission. Combined school funds for the three are down \$26 million to \$401 million, in contrast with the sharp increases reflected in the overall \$880 million and \$381 million sought by the Department of Health, Education, and Welfare and the National Science Foundation, respectively, for their school funds.

The NSF's \$128-million increase, however, could offset some declining defense support. But in view of White House Science adviser David's recent criticism that engineering schools are still turning out too many graduates with an aerospace and defense orientation and need to be redirected, corporate planners don't expect the NSF's new funds to benefit electronics much.

Washington Newsletter

Arinc holds out for vhf aerosat

Despite the blow dealt by the White House Office of Telecommunications Policy, the communications arm of the airline industry is not giving up its hopes for a vhf aeronautical services satellite. In a letter to Federal Communications Commission chairman Dean Burch, J. S. Anderson, chairman of Aeronautical Radio Inc., urges the FCC to argue for vhf frequencies for aerosat use at the CCIR joint meeting in Geneva.

Anderson points out that the high-frequency radio channels now employed would be hopelessly congested if it were not for the extended-range vhf facilities in use along the U.S. coastline, and even these are stretched to their limits. "Satellite relay is the only solution, and the only compatible and timely solution is to extend the existing universally used vhf system through vhf satellites," he says. OTP's plan to loft uhf satellites [*Electronics*, Feb. 1, p. 69], will not relieve frequency congestion for at least 10 years, Anderson asserts.

New bill would protect employees' patent rights

Electronics companies that require their engineers to sign away patent rights for a dollar per year will be in a vulnerable position when Congress starts taking cracks at that widespread practice later this year. Rep. John E. Moss (D., Calif.) early in the session introduced a bill requiring employers to compensate employees for their inventions, and has also expressed his general intent to push for legislation in this area.

The bill, which provides for an inventions adviser in the Labor Department and an arbitration board in the Commerce Department's Patent Office, but which sets no concrete guidelines for compensation, has been severely criticized as cumbersome and expensive. Patent Office sources, however, say that hearings by the House subcommittee on patents, trademarks, and copyrights could lead to a rewrite of the bill and its eventual passage into law.

"Whistle blowing" picks up steam

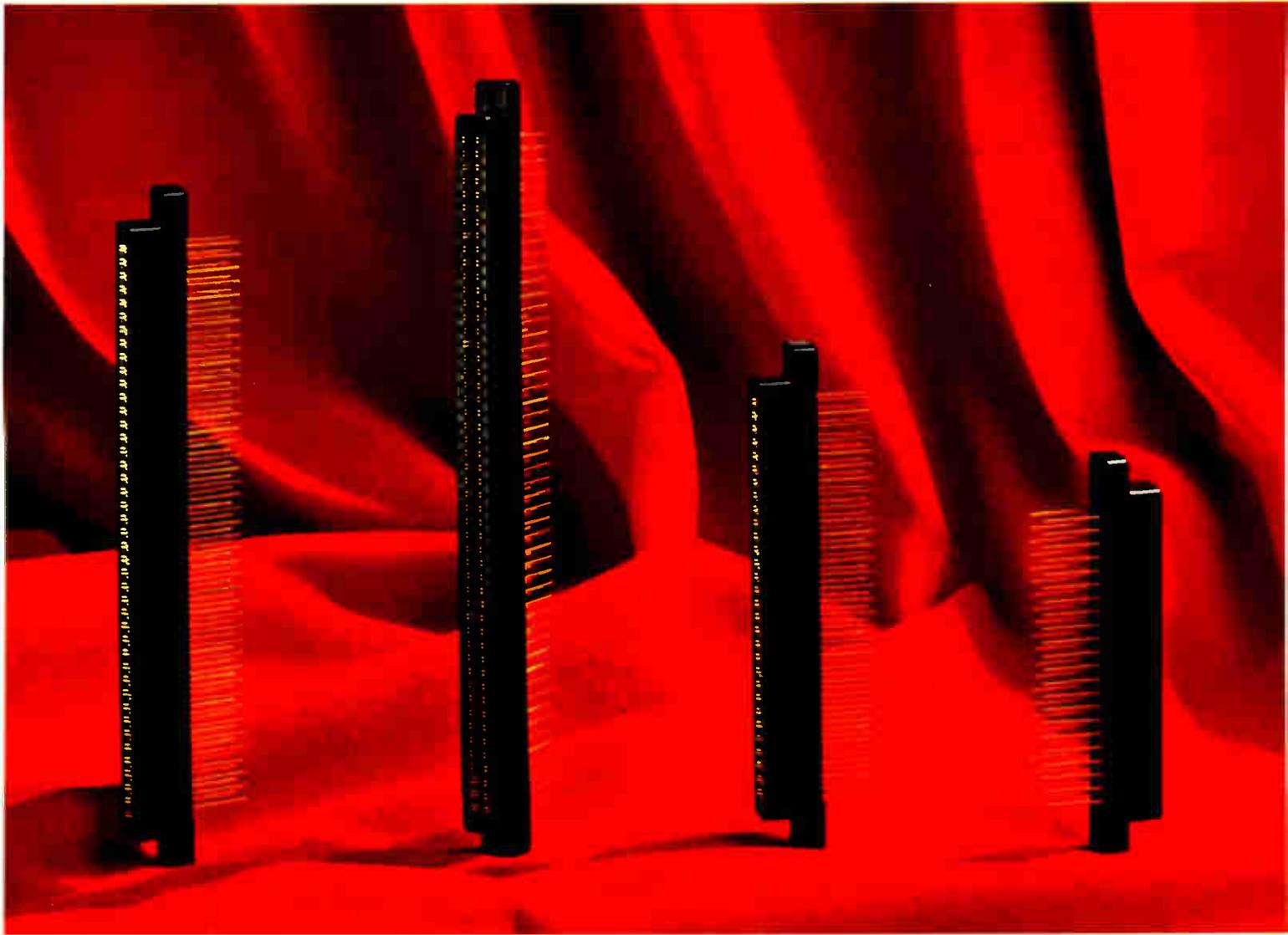
Electronics companies, with so many engineers now unemployed and unhappy, could be a prime target of Ralph Nader's new Clearinghouse for Professional Responsibility. Now just one man, Peter Petkas, and a post office box number (Box 486, Washington, D.C.), it aims at enlisting the aid of scientists and engineers in "blowing the whistle" on corporate and government activity that may not be in the public interest.

Should this be taken seriously? Capitol sources think so. The anonymity and consumer clout of Ralph Nader are a powerful combination. And Petkas can use the 15-lawyer staff that services all the Nader movements to investigate adequately documented allegations and report to the public through lawsuits, Congressional testimony, and other public-interest activity.

Addenda

A three-agency committee is completing a plan that will ready a scanning-beam microwave landing system for use by 1976 [*Electronics*, Feb. 1, p. 26]. As a first step, officials from the Department of Transportation, the Pentagon and NASA have tentatively agreed that contracts should be awarded this summer for studies defining the signal format of the next-generation landing system. . . . Transportation Secretary John A. Volpe will highlight the Electronics Industries Association spring conference, March 8-11, by speaking at EIA's annual Government-industry dinner at the Staler Hilton, Washington, D.C.

A new cost-saver...



to wrap your wires around.

Here's a new family of miniature pc connectors from Amphenol for wire wrapping applications. They cost you less because we've engineered new industrial grade materials into these connectors, yet retained all the same features found in military connectors.

Contact spacing is on a .100 X .200, or .125 X .250 grid and the connectors are available in 22-, 30-, 43- and 50-position models with either grid spacing.

These new 225 Series connectors have bifurcated bellows contacts for smooth, positive, 2-point mating action no matter how irregular the board

surface. The bellows exert firm pressure on the pads even under extreme vibration and shock conditions. You get thousands of insertions and withdrawals without a failure.

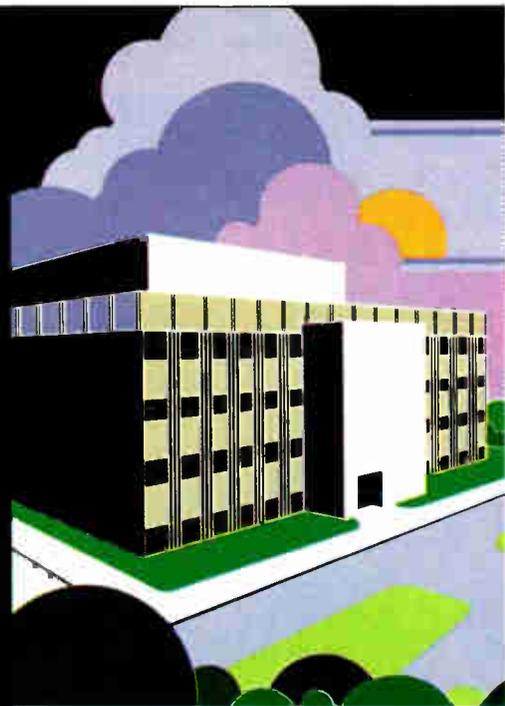
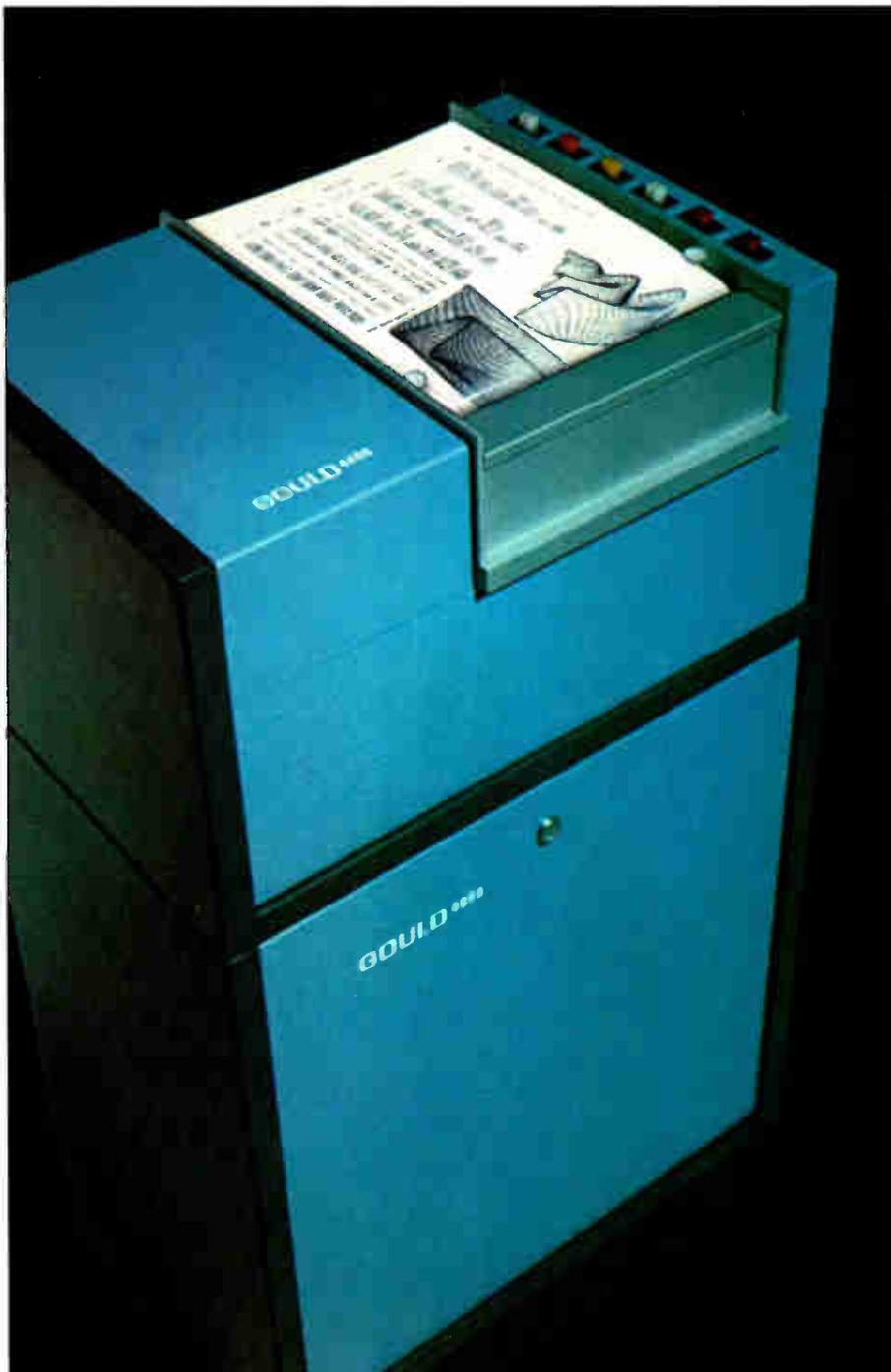
We can also give you this new low-cost connector with solder terminations on .156 centers. And there's a QPL version to MIL-C-21097B, too.

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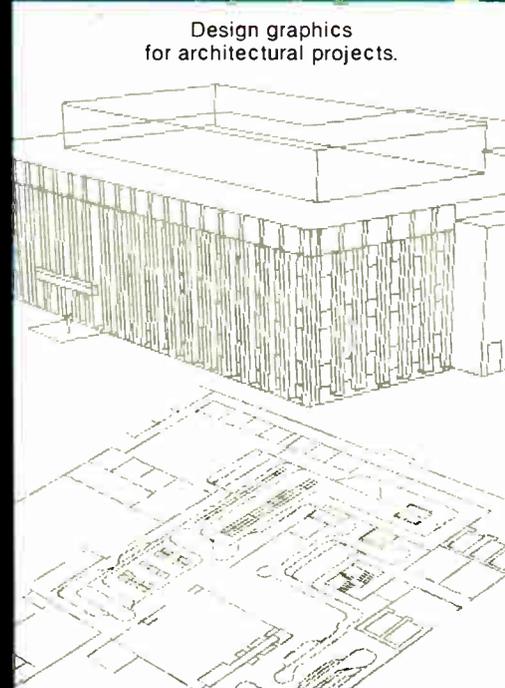


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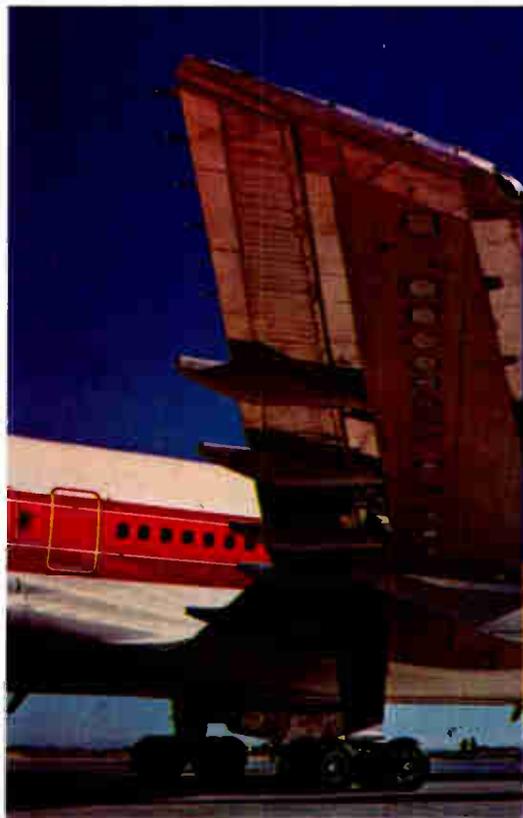
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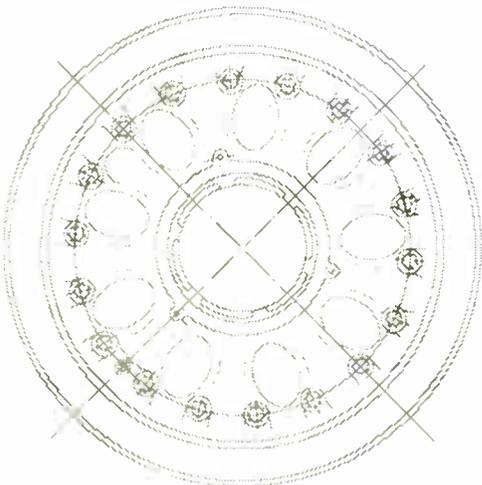
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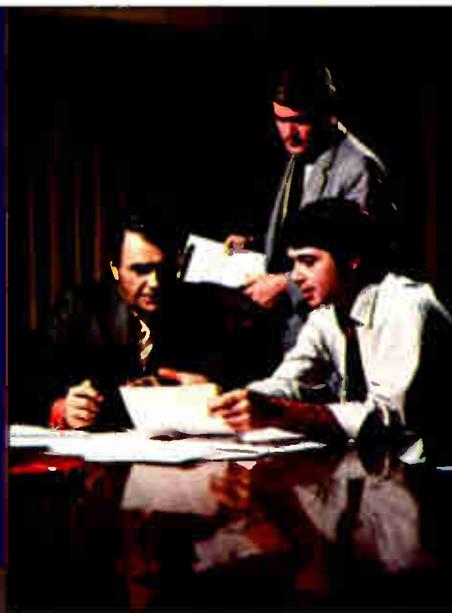
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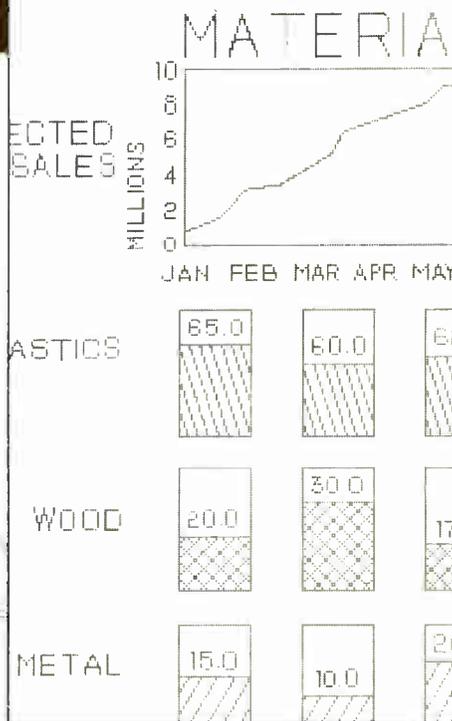
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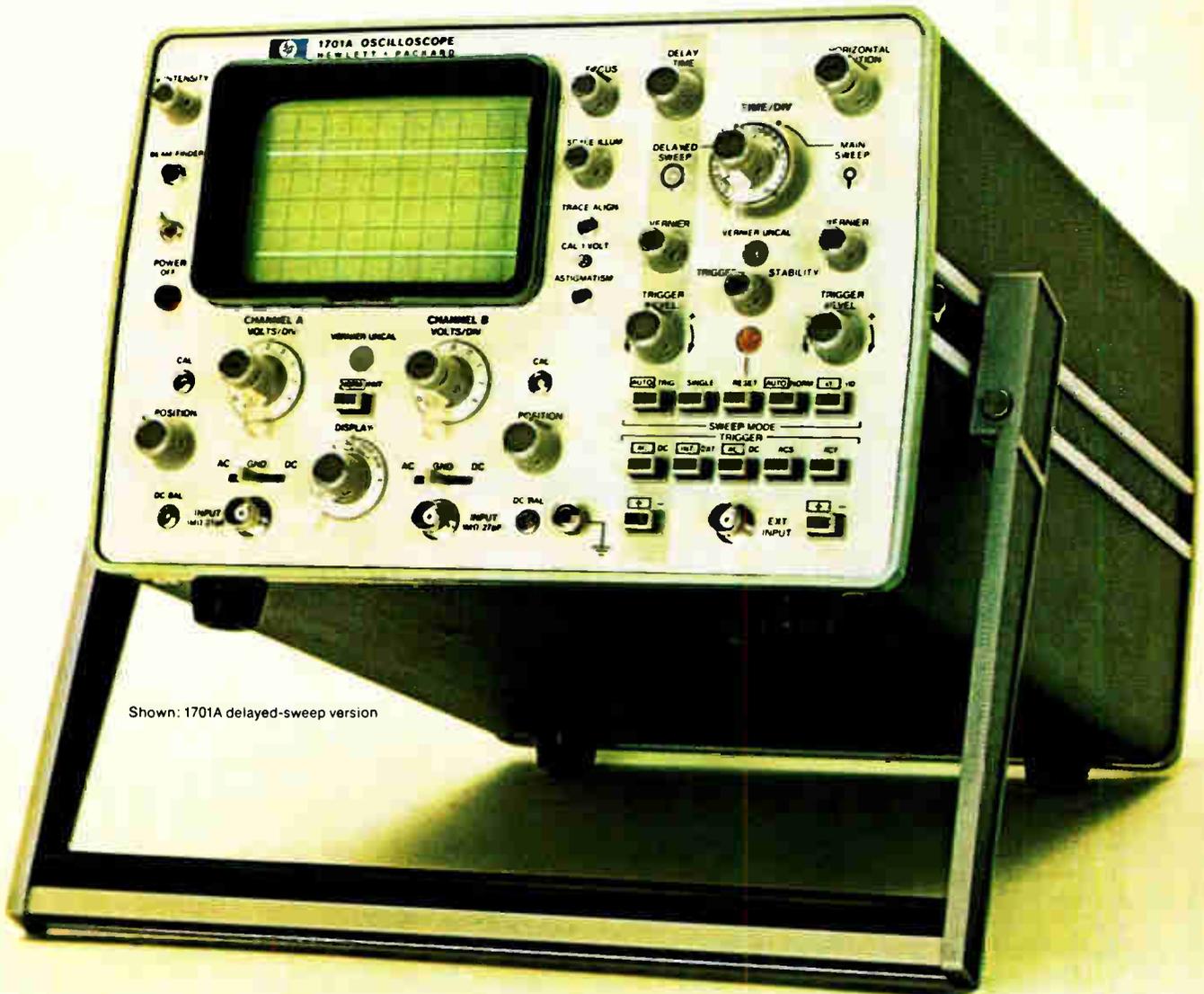
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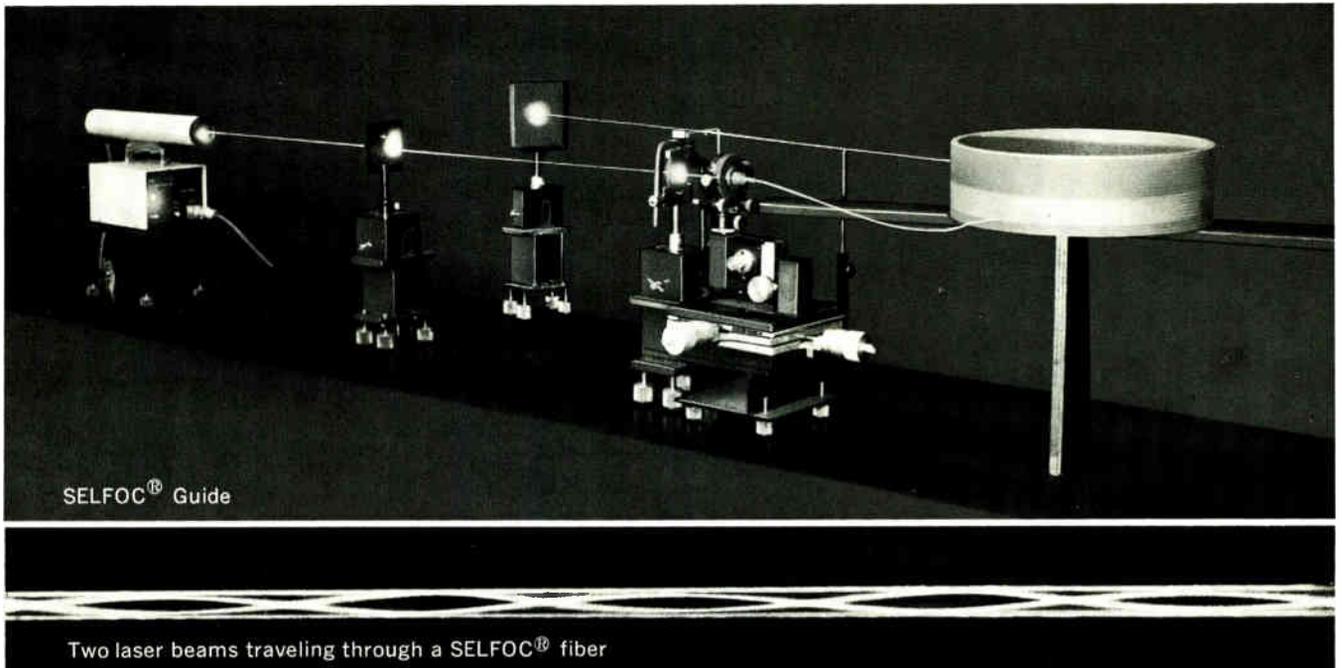
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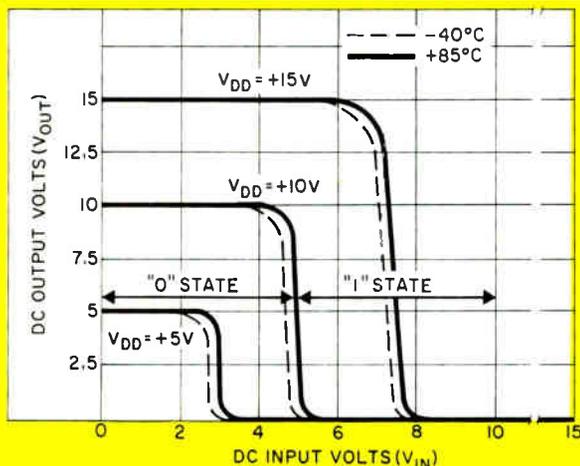
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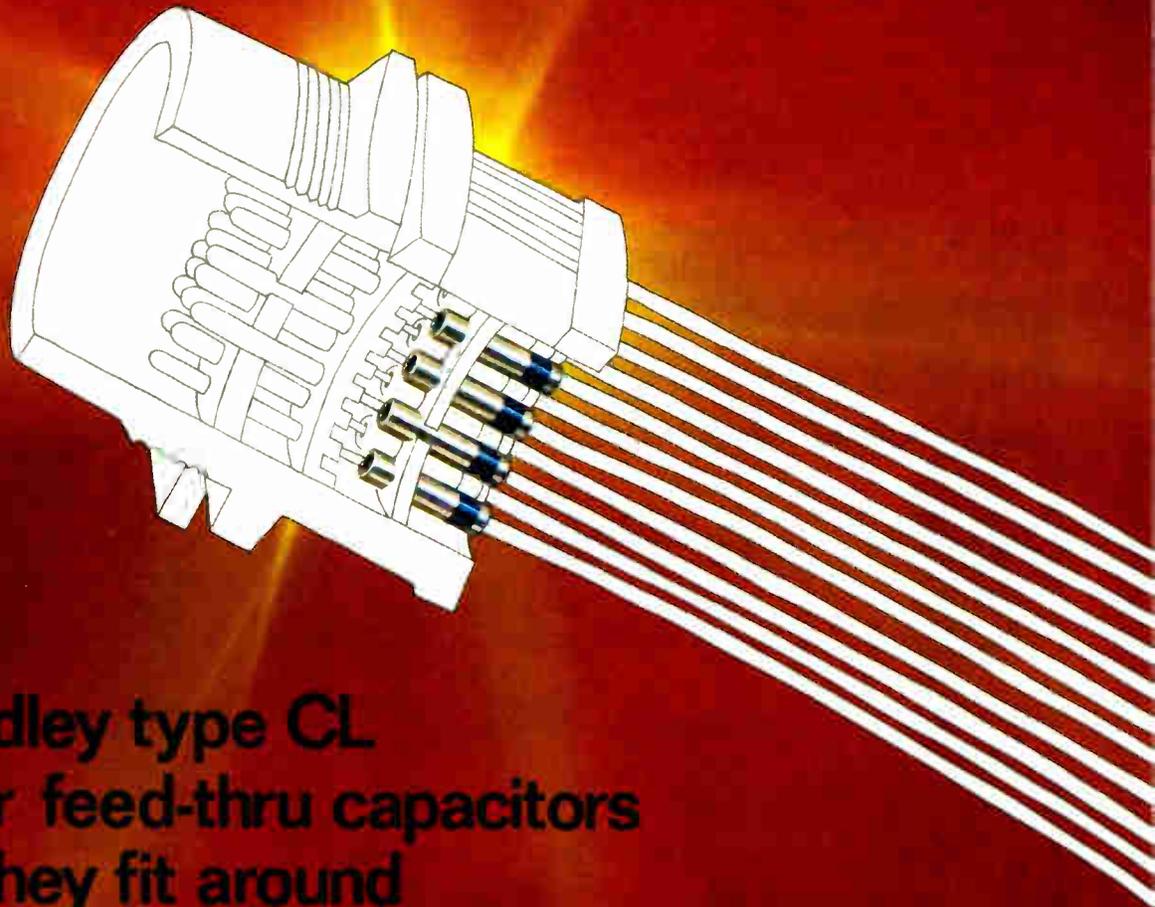
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Technical articles

Digital designers have their own matchmaker, page 70

Performance of high-speed digital systems can suffer from circuit-to-connector mismatches, which can cause serious energy losses. The problem can't always be solved by adapting existing rf and microwave connectors. But pin-and-socket units designed for the job are small enough to accommodate IC packages and can handle 10 gigahertz.

Glass-mat laminates: wet blanket for color TV fires, page 76

The heated controversy over color television fires could be cooled off considerably by a well-established insulating material—glass-mat-reinforced laminates. Long used to meet the stringent safety requirements of industrial applications, the material offers color TV makers a number of attractions, including flame and arc resistance combined with high strength.

With ion implantation, many things are possible, page 80

One of the things that already has happened is a 1,024-bit by one-word MOS random access memory with a read cycle time below 400 nanoseconds. Built by Mostek, the RAM owes its speed to depletion-mode transistors, while low-threshold enhancement-mode devices give the memory compatibility with transistor-transistor logic. Ion implantation puts both on the same chip.

It's a bird? It's a plane? Associative processors can tell, page 91

The complexities of air traffic control—including tracking of hundreds of aircraft, isolation of potentially hazardous courses, and display—may be too much for the conventional computer. But then there's the associative processor, which is supposed to excel at searching through rapidly changing lists of random digital data and performing arithmetic operations on many pairs of numbers. That's why the FAA will give an associative processor its first real test this spring.

Double diffusion quintuples the speed of MOS, page 99

The portal to microwave MOS transistors is one window in a standard mask. It's used by Signetics in two diffusion steps to simply and inexpensively form MOS devices with a 1-micron channel length. That size channel can give microwave transistors that rival bipolar devices in performance. Typical results: 10-gigahertz maximum frequency, 7-decibel gain at 2 GHz, and a 4.5-dB noise figure at 1 GHz.

And in the next issue . . .

Ruggedizing a minicomputer . . . microwave building blocks with Gunn oscillators . . . Josephson devices emerge from the laboratory.

Successful matchmakers: miniconnectors for digital ICs

With digital circuits operating at higher frequencies, mismatch can give designers energy-reflection problems; available pin-and-socket units are small enough to accommodate IC packages and can work at up to 10 GHz

by Robert Harwood, AMP Inc., Harrisburg, Pa.

□ Circuit-to-connector impedance mismatch used to be a problem mainly in the high-frequency world of rf and microwave circuit applications. But switching speeds of digital ICs are moving into that realm—indeed, transistor-transistor logic circuits already switch at speeds exceeding 0.5 nanosecond—and so connections for these circuits also have to contend with mismatch problems.

Now there's a family of connectors that overcomes many of the shortcomings of existing approaches. These new chevron-shaped, pin-and-socket connectors provide a good match for both 75- and 50-ohm characteristic impedance systems for frequencies into the gigahertz range.

Being specially designed for digital circuits, the new connectors don't encounter the tradeoffs usually incurred with other approaches. For example, although special connectors for rf and microwave systems can handle frequencies in the range of digital system requirements, they are much too large for interconnecting tiny medium- and large-scale integrated circuits. Moreover, conventional pin-and-socket and card-edge connectors, while permitting greater signal line density, yield too high a mismatch.

The new connectors, on the other hand, are at least smaller than the package to which they are joined, and they can intermix dc and rf lines to reduce line lengths and crossovers on a system's printed circuit boards. Furthermore, crosstalk can be as low as -80 decibels. Finally, they require a low push-together force while retaining a strong mating force.

Engineers familiar with pulse circuitry know only too well about the effects of too much capacitance in an interconnection system. With high-frequency components of the signal shunted aside and prevented from reaching the load, pulses are delayed and their shapes are distorted.

These problems are similar to those that crop up when improperly matched conventional connectors—unmatched printed circuit, matched pc, and coaxial—are used in pulse systems with fast rise times, which operate with high frequencies. When high-frequency components pass through the connectors, they are reflected by the connector-circuit mismatch and are removed from the pulse train. The pulses are distorted and delayed; power, which may be at a premium in some systems, is unnecessarily dissipated.

(To find how much energy is reflected, see "Mechanics of mismatch," p. 73).

A circuit's high-frequency response depends on the rise time of the pulses:

$$f_h = \frac{0.350}{t_r}$$

where frequency f_h is in hertz and rise time t_r is in seconds.

The frequency response necessary to accommodate the fast rise times of today's electronic circuitry can be quite high: magnetic memories with 10-ns rise times produce frequency components of 35 megahertz; metal oxide semiconductor circuits (1-ns rise time) show 350-MHz signals; and in fast-switching transistor-transistor logic (0.5-ns rise time) signals go up to 0.7 gigahertz.

An impedance mismatch at the electrical connectors joining two lines slows rise times because it reflects high-frequency signal components back toward the pulse source. The amount of reflected energy depends on the degree of mismatch which, in turn, depends on several factors.

One of the most important factors affecting a connector is the physical length of the unmatched section compared to the wavelength of the signal. The longer the unmatched section, the more power it will reflect. Thus, for proper high-frequency performance the connectors should be as short as possible.

Another factor usually neglected in designing digital circuit connectors is crosstalk, in which one signal line is degraded by another's output.

Crosstalk in multicontact connectors is largely due to capacitive coupling between the closely spaced contacts within the connector. Some crosstalk also is caused by inductive coupling. Moreover, there's a tradeoff with respect to reflected energy: crosstalk usually increases as the connector size shrinks.

It's relatively simple to obtain impedance matching or impedance control when all the circuitry is in a single planar device made up of active and passive components on a flat dielectric substrate. Normally, interconnections between active and passive elements on such a substrate are flat conductor paths deposited on one side of the insulating substrate and a solid conductive sheet on the other side. This setup is similar to microstrip. Impedances along the intercon-

nections are matched to a standard 75 or 50 ohms by adjusting dielectric and conductor dimensions in accordance with the substrate's dielectric constant.

When such ICs are soldered directly to a printed circuit board, the matching problem is minimal—the physical distance from the device to the board is extremely small. Any impedance mismatch at this transition would cause very little rf energy reflection except at extremely high frequencies.

However, when devices on one pc board must be connected to devices on another, trouble can begin. Since these boards often are plugged into an intermediate fixture, or mother board, any interconnection between one board and another usually is lengthy enough to produce significant energy reflection if a mismatch exists. And with the usual point-to-point backpanel wiring, mismatches are the rule. In fact, no commercially available technique for point-to-point wiring matches impedances throughout the wire run.

However, impedance can be matched to some degree by using twisted pairs of wire for the more critical signal paths. Here the insulating material, and insulation and conductor diameters must be carefully selected. Similar effects can be obtained from shielded wire or coaxial cable. Nevertheless, impedance will still be mismatched where conductors are terminated at the point-to-point wiring posts—the match cannot be maintained as wires fan out to reach the posts.

Where impedance matching throughout a system is required, it's achieved by the fixed geometry of pc mother boards, either flexible or rigid flat cable, or coax.

To join one part of such a system to another, unmatched connectors are by far the most commonly used devices. They may be of the conventional pin-and-socket type or the less expensive and more popular card-edge units.

In matching these connectors to signal lines, it is

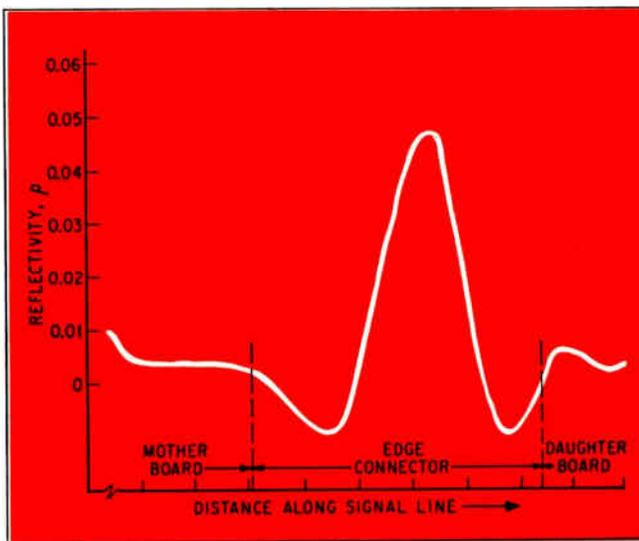
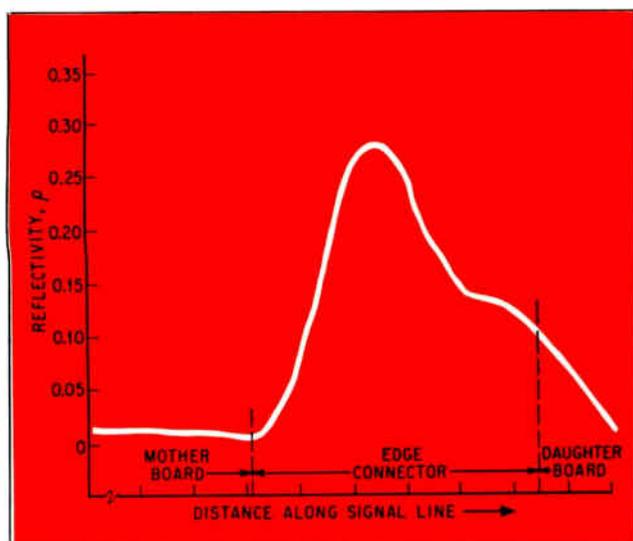
recognized that unmatched connectors are normally inductive and have a high characteristic impedance. Both parameters are functions of signal conductor-to-ground conductor spacing and geometry. Hence, the extremely narrow-diameter contact pins act more inductive than capacitive. Because of their relatively far-apart spacing, their characteristic impedance is high. And since normally only one or two ground lines are carried through a connector, spacing between signal and ground conductors is even larger, boosting impedance further.

Therefore, compensating such a connector involves compensating for the high inductive impedances. One approach is to place lumped capacitances on the pc board at the connector termination, and using at least one ground contact pin for each critical signal pin. If the capacitances are near (less than a half wavelength from) the connector's inductive sections, the effects of the inductive and capacitive sections tend to average, and the connector appears matched.

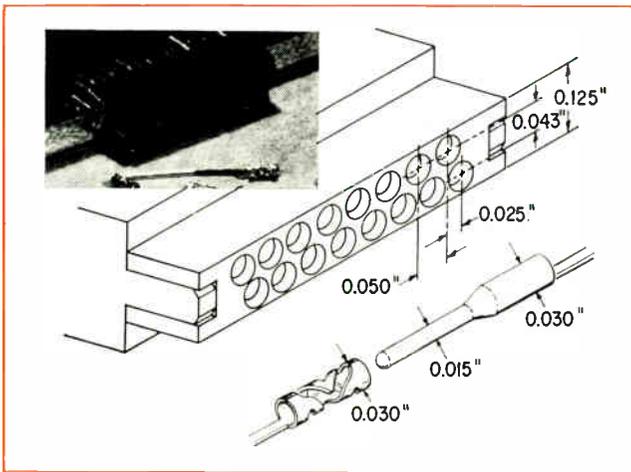
A user-compensated pc connector will reflect significantly less energy than its uncompensated brother. This is illustrated in Fig. 1 which plots reflection coefficient (ρ) as a function of position within the connector and associated circuit using time-domain reflectometry (TDR). The curves were made on a TDR plotter for two card-edge connectors, one compensated the other uncompensated. Standard pulse rise time of TDR equipment is 0.15 ns.

In the test configuration, each connector joined a microstrip daughter board to a microstrip mother. One of the connector's two rows of contacts carries the ground plane; the other carries the signal lines.

The TDR trace shows that the uncompensated pc connector reflects approximately 30% of the energy from the microstrip circuitry. Although an attempt could be made to compensate this connector by adding a capacitive section on the boards, the connector



1. Mismatch. Nearly 30% of the high-frequency energy is reflected by a standard card-edge connector as indicated (a) in this time-domain reflectometry trace. The connector does considerably better when compensation is added (b)—reflected energy is down to 5%. Compensation is achieved by grounding a pin on each side of the signal pin, and terminating them to special pads on the printed circuit board that's plugged in.



2. **Strong socket.** Spiral or chevron-shaped socket of new connectors exerts strong pressure on an inserted mating pin. Even at 10 GHz, connectors are less than a half-wavelength long.

also can be compensated within itself by including a ground pin on each side of the inductive signal pin to provide the required capacitance. These ground pins then are connected to grounding pads, which also add some capacitance to the system. Now the connector reflects only 5% of the incident energy.

In the TDR trace of Fig. 1, the magnitude of the reflection coefficient is presented at each point along the signal path. However, the distance scale along the X axis—determined from the time it takes the pulse to propagate down the interconnection system and return—varies because the propagation velocity of the pulse depends on the material's dielectric constant. This material changes, of course, as the signal passes from one part of the interconnection system to the next. Only relative distances are meant to be shown in this and in the other TDR plots.

Inductive impedance elements in the TDR trace are represented by portions of the trace above the $\rho = 0$ line; capacitive impedance elements present in the trace are represented by portions of the trace below the $\rho = 0$ line. For a compensated connector, the two impedances average out because the areas above and below the $\rho = 0$ lines are about equal.

However, even in a compensated connector, if the pulse rise times are short enough, the inductive and

capacitive sections are not averaged together but remain individually resolved. Each will reflect signal energy, and the connector will not be adequately compensated.

Several manufacturers offer compensated connectors with several relatively larger contact pins already built in. These pins, with their greater capacitance, are used in place of the added capacitances.

Precision coaxial connectors are the best for use in high-frequency matching. On a low-loss coaxial cable, such connectors will handle frequencies to 18 GHz and pulses with rise times as low as 10 picoseconds.

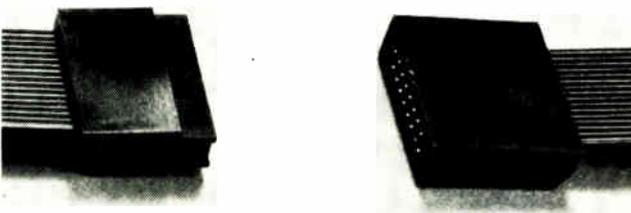
State-of-the-art performance for coupling pc boards to cable can be obtained with the standard 7-millimeter precision connector manufactured by companies such as General Radio and Precision Electronics. This \$50 connector, an inch in diameter, reflects only 0.6% of the energy when joined to microstrip.

The subminiature SM series of coaxial connectors, SMA, SMB and SMC might be more suitable; sizes are half as large as in the standard.

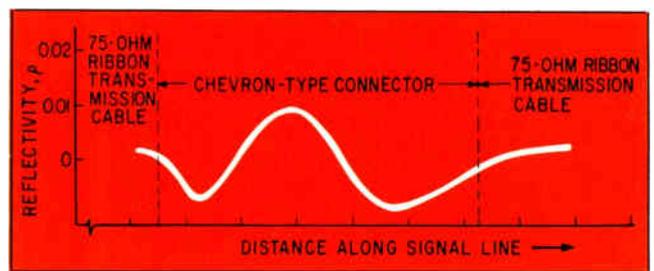
An SMA connector mounted perpendicularly to microstrip pc board and a rigid 50-ohm coaxial cable reflects less than 1% of the energy in the leading edge of the 0.15-ns TDR pulse. In a right-angle configuration interconnecting 50-ohm microstrip on mother and daughter boards, the SMA connector reflects 2% of the incident energy.

However, regardless of their improved high frequency performance, coax connectors aren't suited for flat pc boards. Spacing between signal center lines must be in inches, rather than in the mils needed for high-density packaging. In addition, being designed for thick metal chassis, they are difficult to mount on pc boards. Few can be terminated via mass reflow soldering techniques, as are conventional connectors. Finally, most contain only a single contact pin, a distinct disadvantage since most pc board modules have multiple rf signal and dc power lines.

The new connector family is shown in its basic pc board configuration in Fig. 2. They are pin-and-socket devices with contacts less than one-quarter the length of the contacts in the smallest conventional card-edge connectors. Centerline spacing between pins in a single row also is smaller—50 mils, against 100 mils. And the new connectors, whose characteristics are shown in the table on page 74, have impedances of 75 ohms and 50 ohms, allowing them to match to both 75- and 50-ohm systems at frequencies



3. **Flat cable.** Chevron connectors can be used on woven- and ribbon-type transmission line. TDR trace for connector on 75-ohm ribbon-type line indicates only 1.5% energy reflection.



Mechanics of mismatch

Whenever a mismatch occurs, some part of the total energy will be reflected at the discontinuity. For infinitely long lines (those that are longer than a wavelength at the highest frequency considered), the amount of mismatch is independent of frequency—it depends on impedance alone. For example, if a signal traveling down a long line with a characteristic impedance of A ohms encounters a long line of characteristic impedance B ohms, the amount of voltage reflected by the mismatch is expressed by the reflection coefficient, where:

$$\rho = \frac{B-A}{B+A}$$

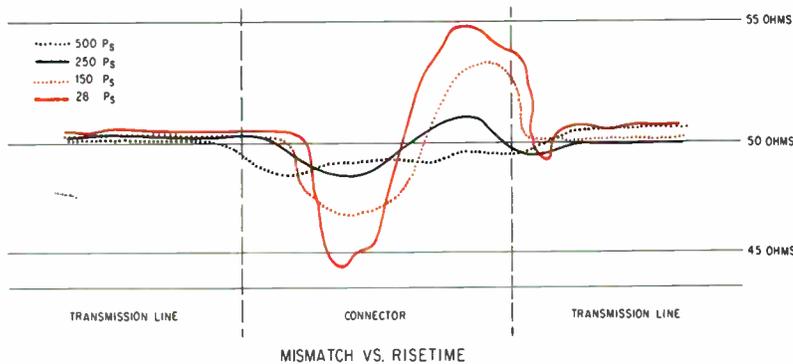
(For a 10% voltage reflection, for example, $\rho = 0.1$) But if the B-ohms section were about a half-wavelength or shorter at the signal frequency, this relation no longer is exactly true.

A kind of impedance-averaging effect occurs; the impedance looking toward the B-ohm line is modified to a value somewhere between A and B ohms. This new apparent impedance depends on the length of the B-ohm line compared to a half wavelength, and the difference between impedance A and B. Consequently, the value of the reflection coefficient

decreases to somewhat less than the maximum value expressed in the ratio $(B-A)/B+A$. One of the best ways to determine the value is to use time-domain reflectometry techniques.

A connector joining two transmission lines of identical characteristic impedance behaves like the B-ohms section. If the connector's length is appreciably less than the signal wavelength, the impedance appears invisible to the signal energy. This example is found when connectors are used in relatively low-frequency digital circuits.

But as the signal frequencies increase (wavelength decreases) the size of the connector approaches one wavelength, and it starts reflecting the high-frequency energy. How the apparent mismatch varies as rise times shorten is shown in the figure. For example, at 1 gigahertz, the highest frequency present in a pulse with a 300-picosecond rise time, the wavelength is only about two inches in a connector that uses diallyl phthalate dielectric. This high-temperature-resistant and sturdy thermosetting plastic material is used in many high-quality connectors. And even at frequencies as low as 100 megahertz (3.1 nanosecond rise time), the length of conventional connectors is an appreciable part of a wavelength; an impedance mismatch may seriously degrade the signal.



as high as 5 GHz. With this capability, they can pass pulses with rise times as low as 0.07 ns with little distortion. And in some applications, the connectors are suitable at up to 10 GHz.

Contacts within the connector are kept short because of the new chevron-shaped socket design (Fig. 2). This chevron shape exerts more pressure for its length on a pin that's inserted into it than an ordinary spring-loaded card-edge socket.

Pressure is built up by the inserted pin which, in effect, tries to "unwrap" the chevron. However, the chevron's pointed apex exerts a high pressure which holds the pin tightly in the socket.

Mated length of a beryllium copper contact is 160 mils; diameter is 30 mils. With staggered rows of contacts, as shown in the figure, spacing between contact lines can be halved to 25 mils, allowing greater signal-line density. For example, a two-row, 16-pin connector measures only $\frac{7}{16}$ inch across.

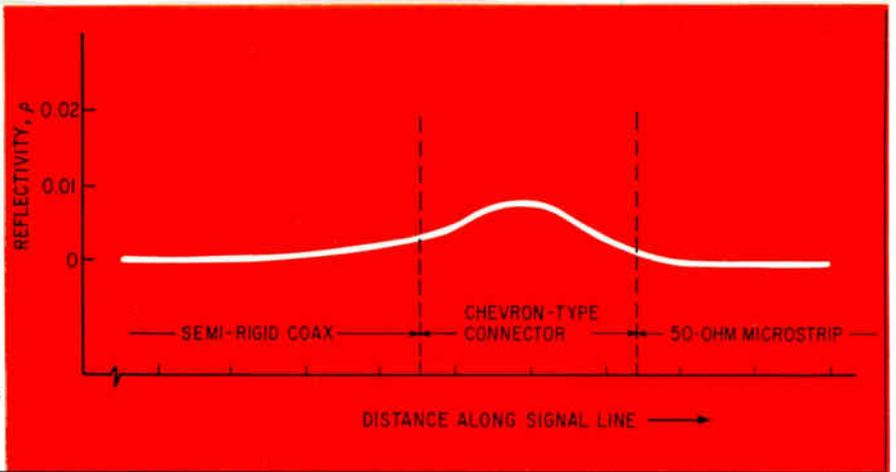
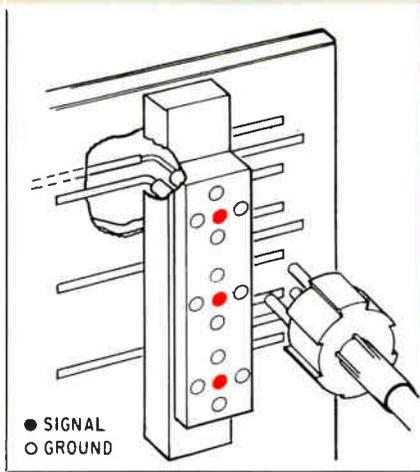
Because the contacts are so short—less than a half

wavelength at 10 GHz—energy reflection at the low gigahertz frequencies is negligible. By carefully selecting the connector dielectric material and controlling the contact spacing and dimensions, mismatches can be reduced still further.

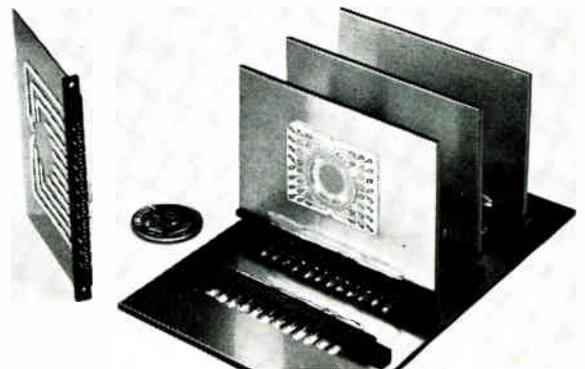
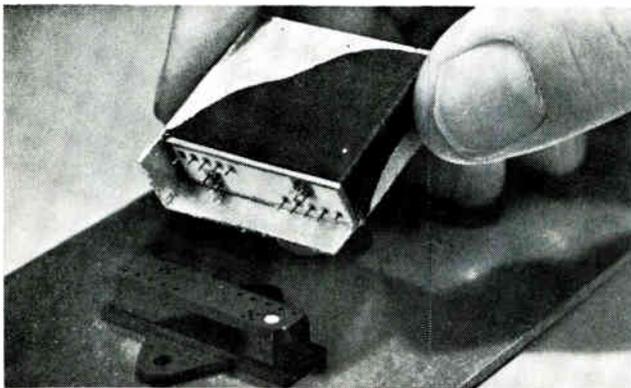
Crosstalk varies with the connector's impedance and the pattern of the signal wires, as shown in the table. At about 1 GHz, crosstalk can be as low as -80 dB in the 50-ohm connector family; in the 75-ohm family it's -60 dB. At best, crosstalk in a conventional edge connector is only -20 dB.

Set in place in an actual application, the chevron connector's reflected energy is low indeed. Connected to 75-ohm microstrip, in a mother-daughter board configuration a 75-ohm connector reflects less than 1% of the incident energy, as measured in a TDR test. This performance is about as good as that of an expensive precision coaxial connector. And a 16-line card-edge chevron connector pair costs less than \$4.

The chevron unit can also be used with 75-ohm,



4. **Contact clusters.** Chevron-shaped contacts are small enough to be used in a connector for subminiature, 45-mil, semi-rigid coax. Joining the coax to 50-ohm microstrip, the connector reflects about 0.8% of the incident energy, as shown by this TDR trace.



5. **Variety.** Two applications for 50-ohm chevron-type connectors include the combination of two rf lines with 10 pulse and dc lines for two IC substrates mounted inside a hermetic package (left), and signal and dc lines for mother-daughter board packaging of MSI devices (right).

Meet the families							
75-ohm family							
Connector type & pattern	ρ @.35-ns rise-time	Cross-talk @ 1 GHz	Mates with				Use with
			90°	card edge	cable	coax	
90° or edge ← .050	.005	-39dB	✓	✓	✓	no	1/16" microstrip
90° or edge ← .100	.005	-60	✓	✓	✓	no	1/16" microstrip
Cable ← .050	.015	-22	✓	✓	✓	no	Round-conductor ribbon, woven or extruded, .025" centers
Cable ← .100	.015	-60	✓	✓	✓	no	Round conductor ribbon, woven or extruded, .025" centers
50-ohm family							
Connector type & pattern	ρ @0.07-ns rise-time	Cross-talk @ 1 GHz	Mates with				Use with
			90°	card edge	cable	coax	
90° or edge ← .124	.039	80dB	✓	✓	no	✓	1/32" microstrip or 1/16" stripline
90° or edge ← .084	.039	-56	✓	✓	no	no	1/32" microstrip or 1/16" stripline
90° or edge ← .060	.039	-34	✓	✓	no	no	1/32" microstrip or 1/16" stripline
90° or edge ← .050	.039	-31	✓	✓	✓	no	1/32" microstrip or 1/16" stripline
Cable ← .050	.039	-31	✓	✓	✓	no	3-wire, .050" signal centers, round-conductor ribbon
90° or edge ← .120	.039	-80	✓	✓	no	✓	1/32" microstrip or 1/16" stripline
Coax	.039	-80	✓	✓	no	✓	.045" o.d. semi-rigid

round-conductor, ribbon-type transmission cable, which has 25-mil conductor spacing. When used with two such cables, the connector reflects about 1.5% of the energy, as shown in the TDR plot of Fig. 3. Crosstalk in the connector when one ground is shared between two signal lines is relatively high: -22 dB at 1 GHz. But the ribbon cable itself offers just as much crosstalk as an equal length of connector so the performance is relatively adequate. An unshared ground pattern will reduce crosstalk levels to below -60 dB.

To make a 50-ohm connector from the 75-ohm unit the spacing between the pins is decreased from 50 to 42 mils and the pin pattern is altered to form three rows of contacts instead of two, as shown in Fig. 4. These changes yield greater isolation because a cluster of four ground pins surround each signal pin. This technique cannot be used with the 75-ohm connector because, to maintain characteristic impedance, the rows of contacts would have to be too far apart—100 mils instead of 42 mils. Shielding then would be less effective than with only two rows of contacts.

Matching with the 50-ohm connectors is extremely good, about equal to that obtained with a coaxial adapter. Used to join semi-rigid coax to 50-ohm microstrip, the connector reflects only about 0.8% of the incident energy, as indicated in Fig. 4. □

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FULLY DECODED P-CHANNEL STATIC MOS ROMS			
IM7601	1024-bit (256x4)	421/521	12.00
IM7602	1024-bit (128x8)	422/522	17.20
IM7603	2048-bit (256x8/512x4)	4230/5230	26.00
IM7604	2560-bit (512x5)	4240/5240	29.10
IM7605	2560-bit (256x10)	---	29.10
P-CHANNEL MOS SHIFT REGISTERS			
IM7703/4	Dual-512-bit/1024-bit	1403/4	12.00
IM7706/7	Dual-100-bit	406/7	4.00
IM7713/14	Dual-512-bit/1024-bit (shift rate equals clock rate)	---	12.00

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Glass-mat laminates can put a damper on color TV fires

Long familiar as a high-power electrical insulation, glass-mat laminates are also an economical way of satisfying the new, more stringent flame safety requirements for color TV receivers

by George R. Mitchell, *Glastic Corp., Cleveland, Ohio*

□ The evidence that insulation failures cause fires in color television receivers has put pressure on set manufacturers to find materials with greater flame resistance. Prodded by the National Commission on Product Safety's disclosures, both Underwriters' Laboratories Inc. and the American Society for Testing Materials have stiffened their flame and insulation resistance test requirements. And at the same time, the likelihood of routine Government surveillance of consumer product safety through Federal agencies has accelerated the search for new flame-safety materials.

But an already established insulation that satisfies the new tests ought not to be overlooked. This material—glass-mat-reinforced laminates—has the advantage of being relatively inexpensive and available from half a dozen or so large suppliers, besides having been in use for 10 to 15 years in industrial applications where flame safety and structural strength are essential.

In color receivers these laminates, designated GPO-2 and GPO-3 by the National Electrical Manufacturers Association, are being used for high-voltage parts such as switches, yokes, and flyback transformers, as well as for circuit and terminal boards. In such applications they may be anywhere from 0.025- to 0.125-inch thick; a square foot of the 0.0625-in. thickness costs 40 cents to 60 cents, depending on variations in the formulation. They have high flexural strength and dielectric or electric strength of 400 to 550 volts per mil. In addition, their impact strength is 3 to 8 foot-pounds per inch, so that circuit boards of glass-mat laminate don't crack upon insertion of metal terminals and in some applications can be made quite thin.

But this same physical strength does have a drawback—it's more difficult to punch holes through glass-mat laminates than through the commonly used paper-reinforced laminates. Punches and dies of hardened steel, as well as high stripper pressures, are required. However, changes in resin formulation have improved the sheering ability of the materials, and, though steel punches must still be employed, surface cracks no longer occur, nor does the insulation surface pull away around the punch hole when the punching tool retracts. This pulling away of the surface was a real problem, because it admitted moisture and

caused undesirable changes in insulation resistance.

As a result, glass-mat laminates have become as machineable as other insulations and at the same time provide effective flame resistance in thicknesses through 0.031 in. Equally important, the materials resist arcing and tracking, which are dangerous because they can create high-resistance conductive paths that build up intense heat and may start fires.

The reason glass-mat-reinforced polyester laminates exhibit good flame and arc resistance has to do with the structure of the mat. The openness of its surface permits fillers to be used in the resin mix, which is not the case with closely knit materials like glass, cloth, or paper. Moreover, there is a variety of possible fillers that impart different flame- and arc-resistant characteristics. Alumina trihydrate, for instance, exhibits better resistance to flame and arcing than less expensive fillers such as calcium carbonate, yet is still low cost and also cures fast.

The UL flame resistance tests that the laminates have to pass are referred to as SE-0 and SE-1, so that materials meeting their requirements are said to be approved for SE-0 or SE-1 flame resistance. UL SE-0 requires a 0.5-in.-wide sample, 5 in. long,



1. Safer socket. This picture tube socket has a high-voltage backing made of arc- and track-resistant laminate qualified to pass UL's flame resistance test.

to be suspended vertically in a flame from a Bunsen burner. After 10 seconds, the burner is removed, leaving the insulation alight. If the flames from the burning insulation go out within another 10 s, the burner flame is immediately reapplied and the test repeated. The material passes the test if the average of the first and second burning times does not exceed 5 s, and if there is no flammable dripping. The UL SE-1 test is similar to the SE-0, except the average burning time cannot exceed 25 s.

UL's slow-burning test calls for the same size of sample as its two flame resistance tests. But the sample is suspended horizontally and the Bunsen burner flame applied to one end for 30 s. If the rate at which the sample burns between a 1-in. mark from its ignited end and a 4-in. mark toward the other end does not exceed 1.5 inches per minute, the material is classified as slow burning.

An arcing test assesses how long a material holds out against the tendency of a high-voltage, low-current arc to form a high-resistance conductive path through its surface, while a tracking test assesses how long it holds out when its surface is contaminated with moisture or other conductive particles. The ASTM D 495 test, for instance, is usually conducted on a 0.125-in.-thick sample under clean, dry laboratory conditions rarely encountered in real-life applications. On the other hand, the ASTM D 2303-64T liquid contamination, inclined-plane tracking test differentiates among solid electrical insulating materials on the basis of their resistance to voltage stresses along a surface wetted with an ionizable, electrically conductive, liquid contaminant.

Together these ASTM tests show that glass-mat laminates of the GPO-2 and GPO-3 grade have arc and track characteristics suitable for preventing fires under the conditions that exist in color TV receivers. In addition, UL presently has the following requirements for specific radio and TV applications of these materials:

- Power line switches. Flame resistance must be SE-0 in the thickness to be used for the finished part. Arc resistance must last a minimum of 180 s for 0.125-in. thickness; that is, with electric leads connected flush to the surface of the insulation and an arc created above the surface, the material must resist conducting the arc on the surface for 180 s. For internal parts of switches, such as the rotor or drive arm which pivots from one contact to another, arc resistance is not required, but the material must be slow burning, and the entire switch must comply with overload and endurance requirements which specify a high-voltage inrush from a tungsten lamp load.

- Flyback transformer terminal boards and picture tube yokes. Flame resistance in end-use thickness must be SE-1. If the board is not in an enclosure or placed a minimum distance from high-voltage parts, it must also pass the 180-s high-voltage arcing test required for power line switches. (Because color TV flyback transformers have been suspected of causing fires, users tend to specify SE-0 flame-resistant, 180-s arc-resistant laminates.)

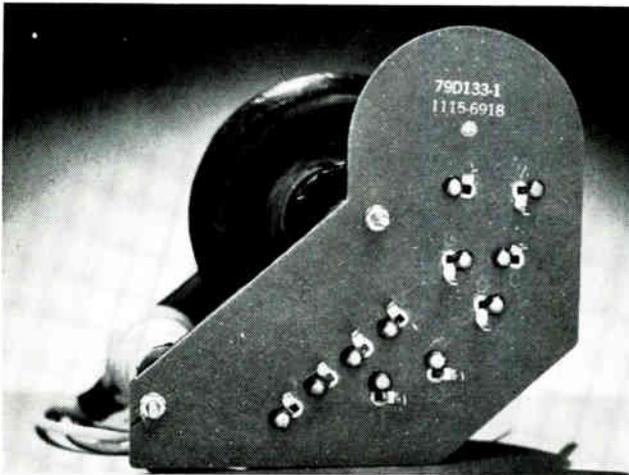
- Circuit boards for parts dissipating power of 50 watts or more. Flame resistance requirements will be the SE-1 test as of Jan. 1, 1972. But in the meantime, UL might insist on a flame test for boards made of new materials or materials unfamiliar to UL engineers.

The glass-mat laminates in Table 1 meet UL materials requirements for SE-0 and SE-1 flame resistance in thicknesses as low as 0.025 in. and attain 180-s arc resistance. By comparison, fabric melamine laminate has good flame and arc resistance and is easy to cut and punch for part fabrication, but it's generally higher priced than glass-mat types. Paper phenolic laminates are lower priced than glass-mat grades, pass SE-1 in flame resistance, can be cut and punched easily, but are not as arc resistant as the glass-mat laminates. The glass/paper

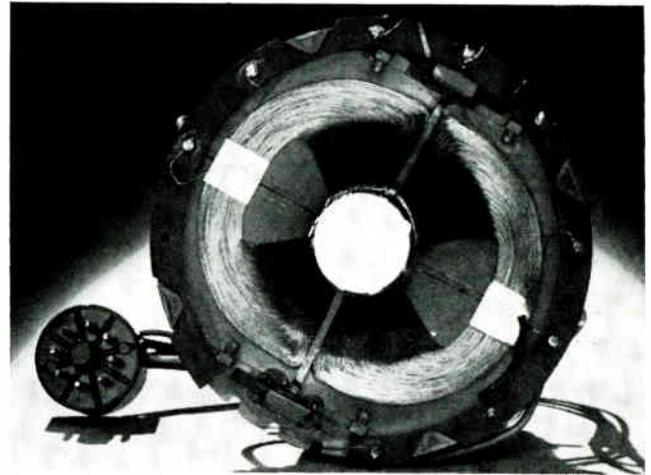
Table 1.

Characteristics of flame resistant laminates

NEMA Grade	GPO-3	GPO-3	GPO-3	GPO-2	Special high-pressure laminates developed for TV and radio applications		
	GPO-2	GPO-2	GPO-2		Glass/paper phenolic	Paper phenolic	Fabric melamine
Reinforcement resin	Glass-mat polyester	Glass-mat polyester	Glass-mat polyester	Glass-mat polyester	SE-1 0.062	SE-1 0.062	SE-0 0.062
UL flame resistance for minimum thickness in inches	SE-0 0.025	SE-0 0.025	SE-1 0.062	SE-0 0.032	100	35	180
Arc resistance of 0.125-in.-thick sample in seconds (tungsten electrodes used)	186	182	187	130	—	—	—
Inclined-plane track resistance of 0.25-in.-thick sample in minutes	300	>600	>600	15	—	—	—
UL recognition temperature in °C (electrical/mechanical)	105/105	105/105	130/160	130/160	140/140	140/140	115/120
Perpendicular dielectric strength in volts/mil	400	400	400	400	625	600	450
Impact strength of notched sample in foot-pounds per inch	8	8	8	8	4	0.7	0.9
Approx. price per square foot of 0.0625-in. thickness	\$.59	\$.56	\$.52	\$.47	\$.46	\$.32	\$ 1.05



2. Flyback board. Because of its flexural strength, glass-mat-reinforced laminates can also be used to make terminal boards like the one on this flyback transformer.



3. Laminate yoke. To decrease the risk of fire during high-voltage operation, the terminal board in this picture tube yoke is glass-mat-reinforced laminate.

Table 2.
Glass-mat laminate test results

	High-arc-resistant composition	High-physical-strength composition
UL high-current arcing test—arcs required to ignite material on surface with electrodes placed 0.0625 in. above surface	No ignition in 200 arcs	No ignition in 200 arcs
UL hot-wire ignition test—seconds taken to cause material to ignite	No ignition when energized 5 min.	32 ¹
UL high-voltage arc resistance test—seconds taken to track and ignite sample	No track when energized 2 min.	No track when energized 2 min.
UL high-voltage arc tracking test	Did not track	Did not track
UL vertical SE-0 flame test—duration in seconds of first ignition		
flaming	0	0
glowing	0.7	0.7
dripping	None	None
—duration in seconds of second ignition:		
flaming	0	0.3
glowing	3	1.7
dripping	None	None
ASTM D 495 arc resistance test—seconds taken by a 0.125-in.-thick sample to break down	187	183

¹More than 15 seconds is required.

phenolic laminates pass SE-1 in flame resistance, are intermediate in arc resistance, and are comparatively low priced.

In addition, out of the battery of arcing, tracking, and ignition tests summarized in Table 2, only one was failed by 0.0312-in. thicknesses of glass-mat-reinforced laminates—the hot-wire ignition test for one of the formulations. Both of the glass-mat laminate compositions illustrated—one featuring good

arc resistance and the other good flexural strength for fabrication—exceeded the 5-s maximum for SE-0 average first and second ignition flaming times. These characteristics make them very suitable insulation materials for line power switches specified for color television receivers.

A final, important requirement in television and radio insulation is that the materials withstand extended periods of use at elevated temperatures. Actually, the temperature specified by UL tests are intended to be those at which the insulation will continue to be effective throughout its life without significant changes in either its dielectric or its flexural strength.

For example, commonly used paper-reinforced phenolic laminates of punching grade, designed XXXPC, are recognized for 125°C service because in field tests at this temperature (called the recognition temperature) they exhibit no dielectric or flexural strength failures. However, when aged in a laboratory oven at 125°C with samples placed at all four corners and in the middle of the oven, XXXPC takes about 11,000 hours to lose 50% of its initial dielectric strength. This value is a benchmark against which other laminates have to be measured in order to be recognized by UL.

For instance, a UL recognition temperature of a GPO-2 laminate is 130°C, which means that when oven aged it will operate continuously for the same number of hours as XXXPC did at 125°C—11,000 hours—before its dielectric strength decreases to 50% of its initial value. Based on previous experience, a 105°C rating should be adequate for most radio and television applications.

A particular advantage of industrial laminates like the glass-mat-reinforced types is that their flame resistance does not degrade as a result of elevated temperature aging, despite their loss of dielectric and flexural strength. This characteristic is vital in color television receivers, which become very hot after long periods in operation. □

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Depletion-mode devices hike speed of MOS random access memory

Ion implantation process yields 1,024-bit by one-word array that has submicrosecond read cycle time and TTL compatibility, but requires no clock and isn't troubled by carrier injection problems

by Vernon McKenny, Mostek Corp., Carrollton, Texas

□ Combining depletion-mode and low-threshold enhancement-mode devices, produced on a single chip by ion implantation, yields a high-speed, random access memory that requires no clock and overcomes the carrier injection problem that plagues dynamic MOS units. It also interfaces directly with transistor-transistor logic and fits into a 16-pin package instead of the usual 18-pin unit.

Depletion-mode transistors are used in the decoding, driving, and sense amplifier circuits for better speed-power products than enhancement-mode devices alone can provide. They also help speed up circuit operation by allowing wide voltage swings that decrease series resistances for fast capacitor charging. That's how the new 1,024-word by one-bit memory, designated the MK4006P, achieves read access and read cycle times of less than 400 nanoseconds, and a write cycle time below 650 ns.

The depletion-mode transistors also account for the elimination of precharging, along with the clock usually required to control the precharging that's commonly used to increase speed. With depletion-mode transistors as loads, necessary speed is attained without any need for precharging, resulting in one less pin on the package. Another is saved by eliminating a bias supply that's normally needed to prevent MOS transistors from injecting currents that discharge storage capacitors (see "Injection rejection" p. 84).

A depletion device's behavior when used as a load for an enhancement device in an inverter circuit is shown in Fig. 1. The depletion-mode device's gate (Fig. 1a) is tied to its source so that $V_{GS} = 0$, and the device is always on (since V_{GS} is less than the pinch-off voltage, 5 volts).

Thus, because of its characteristic curve, it acts as a constant current device; current, I_1 , is approximately equal to $(W/L)_1 (V_p)^2$ where V_p is pinch-off voltage, a constant. Also shown are an inverter with an enhancement-mode device as a load (Fig. 1b) and an inverter with a resistive load (Fig. 1c).

The drain-source characteristics shown in Fig. 1d illustrate the V-I curve for the inverter transistor, Q_2 , as one curve, since all inverter devices are the same. However, load lines for the three cases are different. As the load voltage decreases (V_{out} approaches V_{DD}), the resistive and enhancement loads provide decreasing charging current for the output load capacitance.

For the resistor load, I_1 is $(V_{DD} - V_{out})/R_L$; for the enhancement mode load, I_1 is approximately $(W/L)_1 (V_{DD} - V_T - V_{out})^2$.

However, the charging current from the depletion load remains essentially constant until V_{out} is quite close to V_{DD} . This extra charging current will charge the load capacitance faster than the resistive and enhancement loads. Thus, since all three loads have been adjusted to have the same quiescent point, the depletion load offers the highest speed (Fig. 1e) for the same power dissipation. The resistive load is next fastest, while the enhancement load is slowest. Approximate transfer curves for the circuits (Fig. 1f) show the depletion load's sharpest transition.

The depletion load inverter can be represented as a pair of constant current sources (Fig. 2). If I_1 is made greater than I_2 either by giving depletion-mode transistor Q_1 a greater channel width-to-length ratio W/L , or by decreasing the drive, V_{in} , to Q_2 , then V_{out} will approximate V_{DD} when the load capacitance charges. This is apparent from the current-source analogy: since I_1 is the larger, it controls charging and brings the output up to V_{DD} . This situation approximates that of a high-gain amplifier—a small change in V_{in} produces a large swing at the output. But if I_2 is greater than I_1 , then V_{out} will charge toward V_{SS} .

For large-signal inputs, V_{in} is made positive enough so that Q_2 , the inverter transistor, is strongly cut off; thus, $I_2 = 0$. In this case, the switching time of the negative-going edge of V_{out} is completely determined by I_1 —it alone acts to charge the capacitor. The positive-going switching time is determined by $I_2 - I_1$. These times are expressed as the product of the voltage change, $V_{DD} - V_{SS}$, and the capacitance, divided by the charging current:

$$\Delta t (+) = \frac{(V_{DD} - V_{SS}) C_L}{I_2 - I_1}$$

$$\Delta t (-) = \frac{(V_{DD} - V_{SS}) C_L}{I_1 - I_2}; (I_2 \cong 0)$$

Thus, to make the switching times equal, the device geometry ratio, $(W/L)_2/(W/L)_1$, must be adjusted so that $I_2 = 2I_1$.

Depletion-mode device advantages are even more apparent when three types of high-speed, high-ampli-

tude drivers are compared. These are a saturated inverter, a bootstrap inverter, and the depletion inverter.

The saturated inverter (Fig. 3a) has a poor speed-power product; most negative level is $V_{DD} - V_T$.

The bootstrap (Fig. 3b), finding greater popularity in MOS circuits, has a better speed-power figure of merit. An added advantage: it can attain V_{DD} at its output for a short time. However, normal diode leakage eventually will cause the bootstrapped node to drop to $V_{DD} - 2V_T$. But there's a way around this: a low-power MOS device can be placed in parallel with the bootstrapped load; V_{out} falls only to $V_{DD} - V_T$.

Depletion inverters offer an even better speed-power product than bootstrap inverters. They also attain V_{DD} as the most negative level and remain at that level indefinitely. This is particularly useful on an address line or in a TTL-compatible output buffer on a memory, where maximum negative amplitude must be maintained.

In the new RAM, depletion-mode devices provide faster switching inverters and gates in the row and column decoders, drivers, and buffers. Another useful feature is higher gain in the sense amplifiers. However, depletion-mode devices are not used in individual memory cells—those circuits primarily perform charge-steering junctions.

The storage matrix of the new RAM is organized (see block diagram, Fig. 4) into 32 rows and columns, or 1,024 cells. Basically, the row address decoder and driver signals combine with the read and write signals to enable the selected row for the read and write condition; the column decoder then uses these signals to control the flow of data into and out of the memory.

Because of charge leakage, data must be refreshed every 2 milliseconds.

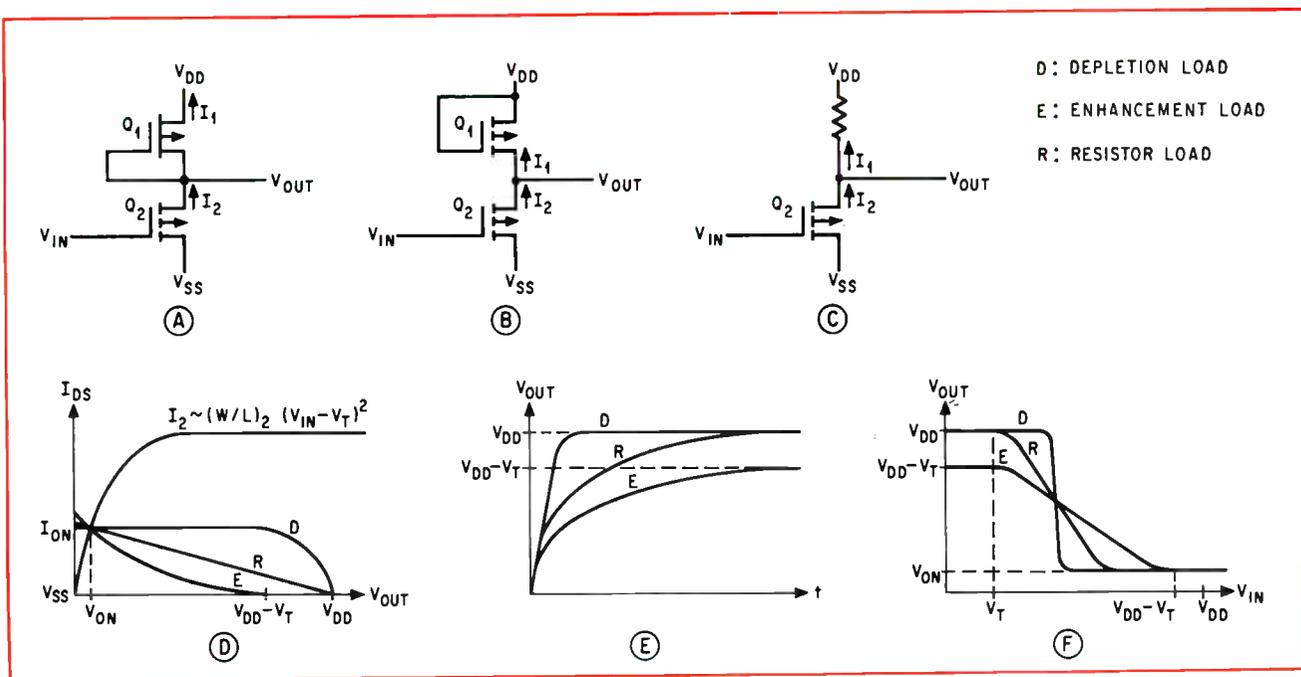
In a typical read-modify-write cycle, the row and column addresses are applied first. With a READ signal on the READ-WRITE line, the row decoder output, R_n , and the READ signal are combined to activate R_n READ for a selected row. All 32 cells in the selected row transfer their data to the sense amplifier inputs at each column's edge. The column decoder output connects the selected column's sense amplifier to the output through D_{out} SELECT. The reading operation is completed; time involved is the read access time.

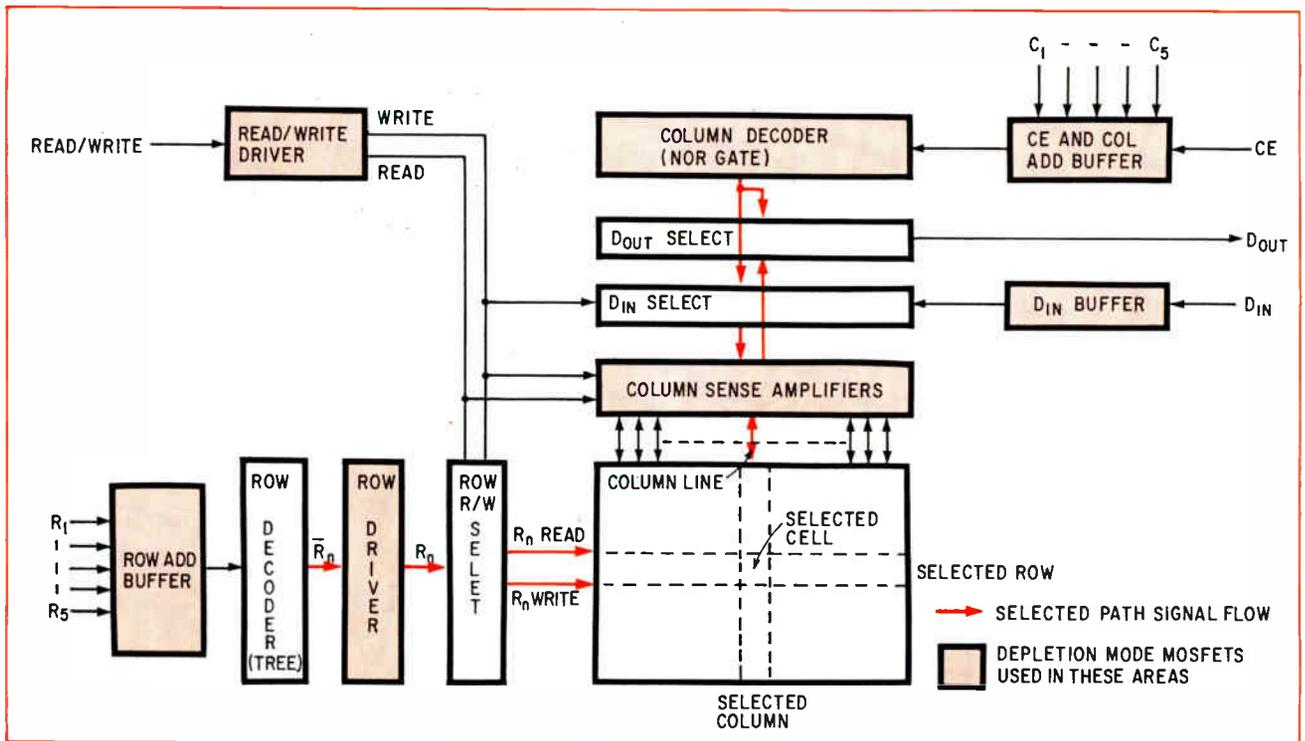
New data is fed in through D_{in} . The WRITE signal now is applied at the READ-WRITE input. Data from the previous read condition of the read-write-modify cycle unselected by the column decoder is returned to each cell's storage nodes; the new input data is combined with the column decoder output and applied to a sense amplifier to be written into a cell.

Operation of an individual cell is shown in Fig. 5. The memory chip requires only +5-v and -15-v supplies. The +5 v is for compatibility with TTL and DTL logic levels; the +5-v supply line serves as the return signal path, since there is no system ground connection to the chip. The +5 v substrate voltage is considered chip ground; -15 v thus becomes -20 v with respect to substrate ground.

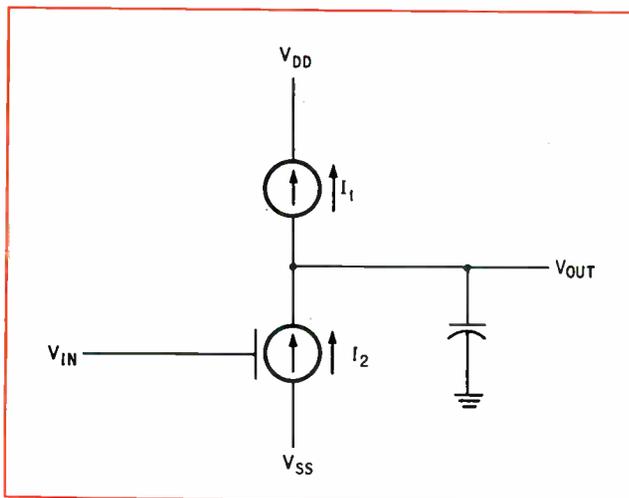
Note that the difference in voltage supplies for the DTL or TTL and the MOS chip also results in a difference in logic levels. A TTL or DTL logic 0 (0 v) results in an MOS 0 of +5 v; a TTL or DTL 1 (+5 v) results in an MOS 1 of -15 v. Thus, DTL and TTL use positive logic (logic 1 higher in level than logic 0) while

1. Depletion-mode load. Of three typical inverter circuits—depletion load, A, enhancement-mode MOS load, B, and resistor load, C—depletion type is fastest because it operates at constant current for greater range of voltages, as in D. Load current helps change output load capacitance faster, E, and transfer characteristic, F, shows sharper transition for depletion-mode circuit.





4. Full memory. Shaded blocks indicate sections of RAM that use depletion-mode devices. Paths shown in color indicate signal flow for selected row and column.



2. Equivalent. Operation of depletion-mode inverter circuit is equivalent to two constant current sources, where larger of the two currents determines rate at which an output capacitor charges up.

the MOS chip uses negative logic (logic 1 lower in level than logic 0). All logic diagrams shown are in terms of negative logic: for example, a NOR gate is equivalent to a positive-logic NAND gate.

At the storage node, A in Fig. 5, the capacitance, shown dashed in color, is the total capacitance to substrate at that point, not an actual physical capacitor. The same is true for the capacitor shown at node B

at the input of the sense amplifier, which temporarily stores information during the write cycle.

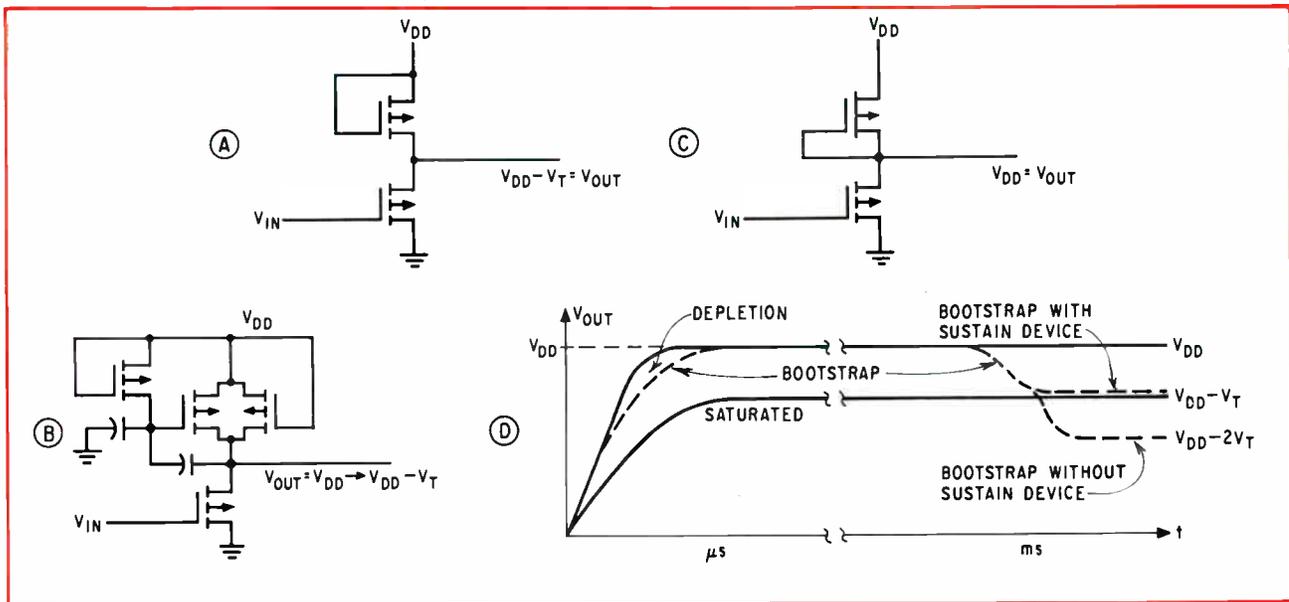
The storage capacitor holds a negative charge for a positive logic 1 entered at the data input, D_{in} . With a positive logic 0, there is no charge on the capacitor. To understand how the charge gets to the capacitor, consider a read cycle and then a write cycle.

In a read cycle, suppose R_n , R_n READ, R_n WRITE, C_n , and WRITE are at V_{SS} (0 V) and READ is at V_{DD} , $-20V$. When the row address is applied, R_n and R_n READ go negative to about -14 V, which is $V_{DD} - V_T'$ where V_T' includes threshold voltage of the enhancement-mode device (-1.5 V), body effect, and the effect of limited charging time.

Body effect, inherent in all MOS structures, takes into account the increase in threshold voltage caused by the bias voltage, V_{BS} , applied between source and bulk material. If $V_{BS} = 0$ V, then the threshold voltage is the normally specified value, -1.5 V in the MK4006P. But if V_{BS} has a finite value, the gate voltage must be increased beyond this nominal threshold if conduction is to occur. The increase in threshold voltage is approximately proportional to the square root of V_{BS} . In this case, the bias between bulk and source creates a 2-V increase in threshold voltage. Thus, $V_{DD} - V_T'$ is reduced from -18.5 V to about -16.5 V. Because the time for charging the capacitance is limited, this voltage is further reduced to -14 V.

R_n READ turns on Q_1 , connecting storage-node transistor Q_3 to the column line so that the charge on the storage capacitor is read out.

If there is no charge on the capacitor, Q_3 does not turn on and the column line simply charges through transistor Q_6 to -14 V. Since the READ pulse also turns on Q_9 , the sense amplifier input node B thus is connected to the column line so that the voltage



3. **Widest swing.** Depletion-mode inverter circuit, C, attains V_{DD} as most negative output level, while bootstrap circuit, B, and enhancement-mode inverter, A, do not offer as wide a range on a dc basis. Depletion-mode circuit also has best speed-power product.

change on the column line can be read out.

If the storage capacitor were charged to a negative voltage, Q_3 would be turned on; the column line then would discharge toward ground, to about -10 V ($V_{D1} - V_T' - 4$ V, where 4 V is dropped across Q_6).

Depletion mode transistors provide high gain to the sense amplifier and decrease drive requirements on the storage cell. The sense amplifier is designed with a built-in offset voltage of about -12 V—a value exactly between -10 V and -14 V, the two possible final values of the column line. The sense amplifier's gain is adjusted so that its input need change by only 0.5 V to drive the output to -14 V or 0 V.

This property allows the small devices in the storage cell to drive the high-capacitance column line over a maximum swing of only ± 2.5 V instead of the 10- to 15-V swing common in other memories. To achieve a further increase in speed, column line capacitance is reduced by the -12 V bias (the usual 0-V bias produces p-n junction capacitances about three times higher). The two effects—reduced capacitance and reduced voltage swing—improve column line response time by a factor of 10 or more compared with conventional circuits.

The memory can be operated in a continuous READ mode by holding the READ-WRITE line at logical 1 (0 V), while providing the CHIP ENABLE signal. Within typically 300 ns after the address change, all switching has occurred, and thus output data becomes valid.

Data readout is nondestructive, and can continue until the storage capacitor's charge starts to degrade through p-n junction leakage. Under worst-case voltage conditions and at elevated temperatures, the data will remain on the storage capacitor for at least 2 ms. Therefore, data must be refreshed every 2 ms. Since the refreshing is accomplished for an entire row at a

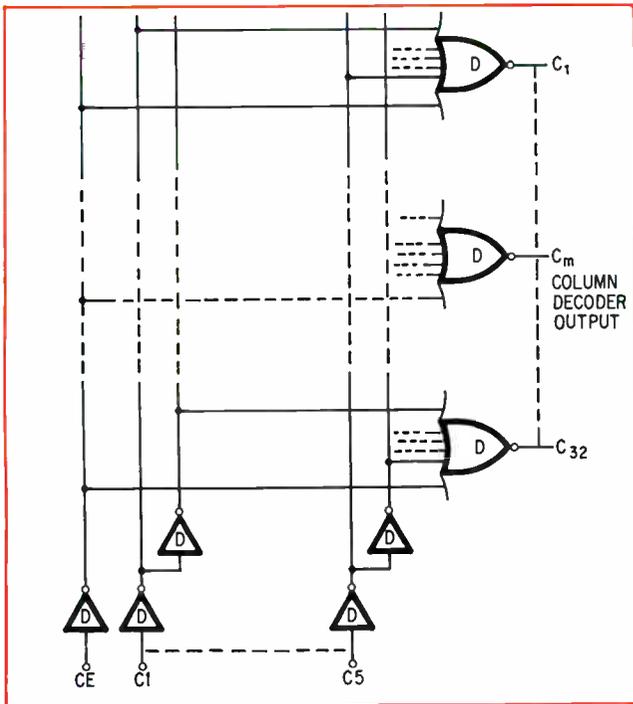
Depletion modes and ion implants

MOS circuits generally use enhancement-mode transistors, in which no conduction between drain and source takes place with zero gate-to-source voltage. Such devices are commonly fabricated on an n-type substrate and operate with a negative gate voltage to form a p-type channel between the diffused p-type drain and source regions. To form a conductive channel, the applied negative voltage must exceed a certain threshold, ranging from about -1.5 volts for low-threshold devices up to -4 or -5 v.

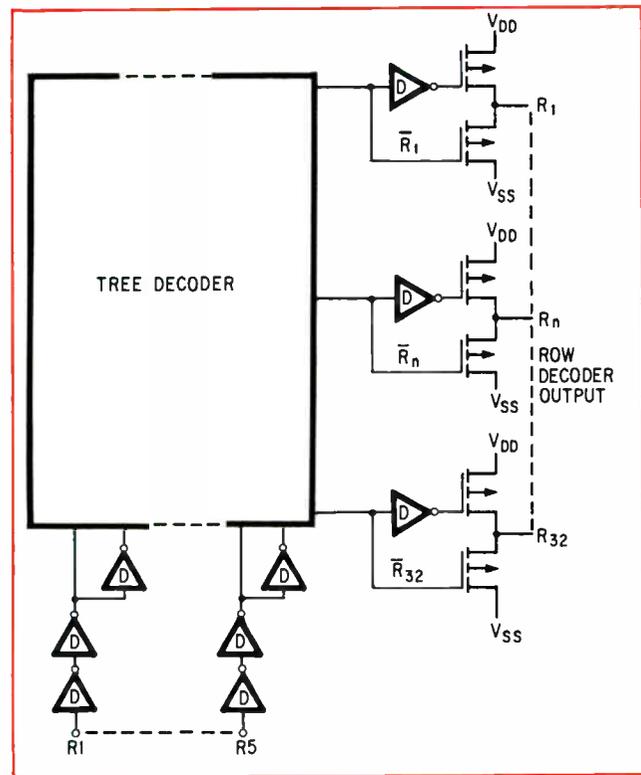
In the depletion mode device, however, a conductive channel is formed when $V_{GS} = 0$. To turn off a p-channel device, the gate-source voltage must be increased to about $+5$ v, the pinch-off voltage, which corresponds to the threshold voltage. To form a p-channel depletion-mode transistor, light p-type doping of the channel is required. Proper doping has been difficult to achieve chemically because the oxide grown after the doping process tended to absorb impurities at the high temperatures required for oxide growth. However, with ion implantation, the oxide already is in place when the dopant ions are implanted.

In the MK4006P 1,024 x 1 RAM, two ion implant steps are used with the p-type dopant, boron. The first one lowers the enhancement-mode thresholds from -4 v to a nominal -1.5 v, and the second implant produces the depletion-mode transistors.

In the future, ion implantation also could be used to manufacture precisely controlled complementary MOS circuits as well as n-channel devices free of unwanted, parasitic, depletion-mode devices, while at the same time producing depletion-mode devices in the desired locations. Such combinations could produce RAMs as large as 2,000 to 8,000 bits on a single chip with access times less than 100 nanoseconds.



6. Column decoder. Depletion-load inverters drive depletion-mode NOR gates. Decoder uses 32 six-input NOR gates. Selected column is driven by one gate (the only one that provides an output at $V_{1,1}$). D indicates circuits with depletion-mode devices.



7. Row decoder. Tree decoder drives 32 depletion-load inverters and push-pull buffers. Selected row is driven to $V_{1,1}$, $-V_T'$. D indicates circuits with depletion-mode devices.

time, a total of 32 REFRESH cycles are required to completely refresh all the bits on the chip. Column address is ignored during the REFRESH cycle.

To refresh the cell of Fig. 5, information at the storage node first is transferred to the sense amplifier output as in the read cycle. The READ-WRITE input then is changed to a WRITE condition. This causes the READ line to discharge to 0 V and the WRITE line to charge to -20 V. The column load resistor, Q_6 , then is turned off and node B at the sense amplifier input is isolated from the column line. Q_{10} connects the column line to the sense amplifier output. The data that had been on the column line is stored on the capacitance at node B. R_n READ goes to 0 V and R_n WRITE goes to -14 V, turning Q_1 off and Q_2 on. The storage capacitor therefore is connected back to the column line and receives the information stored at the output of the sense amplifier. If the storage node was previously at 0 V, it stays at 0 V. If it had been at a negative voltage, it will be restored to -11 V ($V_{DD} - 2V_T'$). At this point, the READ-WRITE input is changed back to the READ condition; the row address is changed, and REFRESH for the new row proceeds.

Although all the nodes in a row are refreshed simultaneously, the WRITE mode operates on only one node at a time. During the WRITE cycle, all the cells in the selected row are automatically refreshed except the one selected for a new data input.

For this cell, the C_m line, instead of being at 0 V as in all the other columns, is put at -20 V by the col-

umn address decoder. Hence, the input data buffer, through transistors Q_7 and Q_8 , can overpower the information stored on node B. The sense amplifier receives this new input and delivers it back to the storage cell through a process similar to REFRESH.

Depletion-load gates are used in the column decoder (Fig. 6). Each of the 32 six-input gates drives a column line and carries input from various combinations of true and complement data for the five-column address inputs. The sixth gate's input is the complement of the CHIP ENABLE external input.

In the circuit (Fig. 6), if CE is at a positive logic 1 (0 V), the NOR gate produces 0 V at its output regardless of the address information. All column decoder outputs are clamped at 0 V and the chip is disabled. To enable the chip, the CE input is changed to -5 V, positive logic 0, and one of the 32 six-input NOR gates will have an input of all six lines at 0 V. This gate will turn on its column line, C_m , to -20 V.

Depletion-load gates also speed up row decoding, where signals have a longer delay path to their output than the column decoding signals. The individual row-decoder stages must have less delay and switching times than the corresponding column decoder units. The TTL level input signals first are amplified and then used to generate five pairs of address signals which feed the tree decoder. This device has 32 output lines feeding buffers, which in turn feed the 32 row address lines (R_n). Each buffer consists of a depletion mode inverter driving an enhancement push-pull. □

Designer's casebook

Counter shifts signal phase only one way

by Peter J. Kindlmann
Yale University, New Haven, Conn.

Twisted-ring counters do a better job of generating phase-shifted waveforms than flip-flops connected in a more straightforward way. The phase shifts on the counter outputs aren't ambiguous, and the counter takes fewer logic devices.

An assembly of three flip-flops, like the first circuit below, has been used in the past to generate waveform pairs with a 90° phase difference. But the sign of the phase difference is not well defined because the flip-flops operate in the toggle mode. Their phase ambiguity is $\pm 180^\circ$.

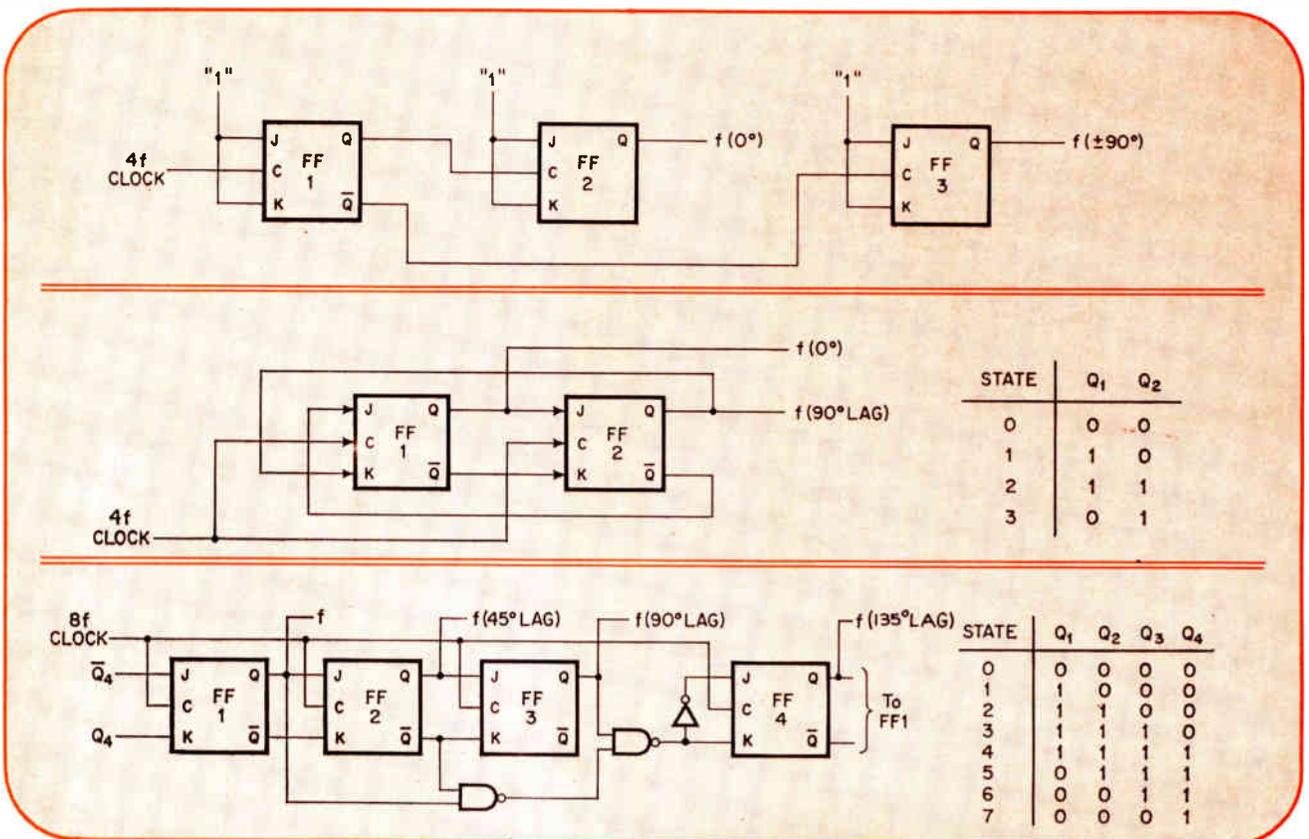
Connecting just two J-K flip-flops as a twisted

ring counter produces the state sequence shown in the truth table. The Q output of flip-flop 2 always lags the output of flip-flop 1 by 90° no matter which state initiates the sequence when the clock pulse is applied.

A variety of other phase shifts can be obtained by adding stages to the twisted-ring counter, as the four-stage version illustrates. The flip-flop states may be arbitrary when power is first applied. The fourth stage and its input gating insures initiation of the correct state sequence. The state steering of flip-flops, as illustrated by the truth tables, provides outputs with successive phase shifts. Each is shifted the same amount.

The two-stage counter is sufficient for most applications such as motor drive, phase-sensitive detectors and single-sideband modulators. Some applications require filtering of the digital outputs. Filtering is quite easy since the outputs are symmetrical square waves and there is a 3:1 frequency ratio between the fundamental and lowest harmonics.

Lag or lead? A system using the old-style phase shifter made with toggled flip-flops cannot tell which output leads and which lags. But the sequence through the twisted-ring counters guarantees that each of the outputs lags the first by a fixed amount even when the starting states are arbitrary.



Series limiter tracks signal, finds symmetry

By Roland J. Turner,
RCA Corp. Missile Surface Radar division, Morristown, N.J.

Multichannel limiting with a single series limiter is a lot less expensive than having a shunt limiter in each channel. But symmetry suffers when the reference dc level is fixed and the signal level isn't. However, a series cutoff limiter preserves symmetry via a unique feed-forward design that makes V_{ref} track V_{in} during class A operation. Interference inputs block themselves by driving one output diode to cutoff.

The series high-voltage tracking, symmetrical cutoff limiter shown limits 10 video channels simultaneously. It costs about one-tenth as much as the shunt limiter it replaces and is much more efficient. When activated by a high-level interference signal, the limiter acts as a current switch. Since no current is drawn from the source driver, that circuit can be an inexpensive, low-current device, too.

During quiescent operation, input and output diodes D_1 and D_2 are biased in their class A region. They draw current equally from their current source because

the dc voltage levels at their cathodes are matched. The currents are 11 milliamperes.

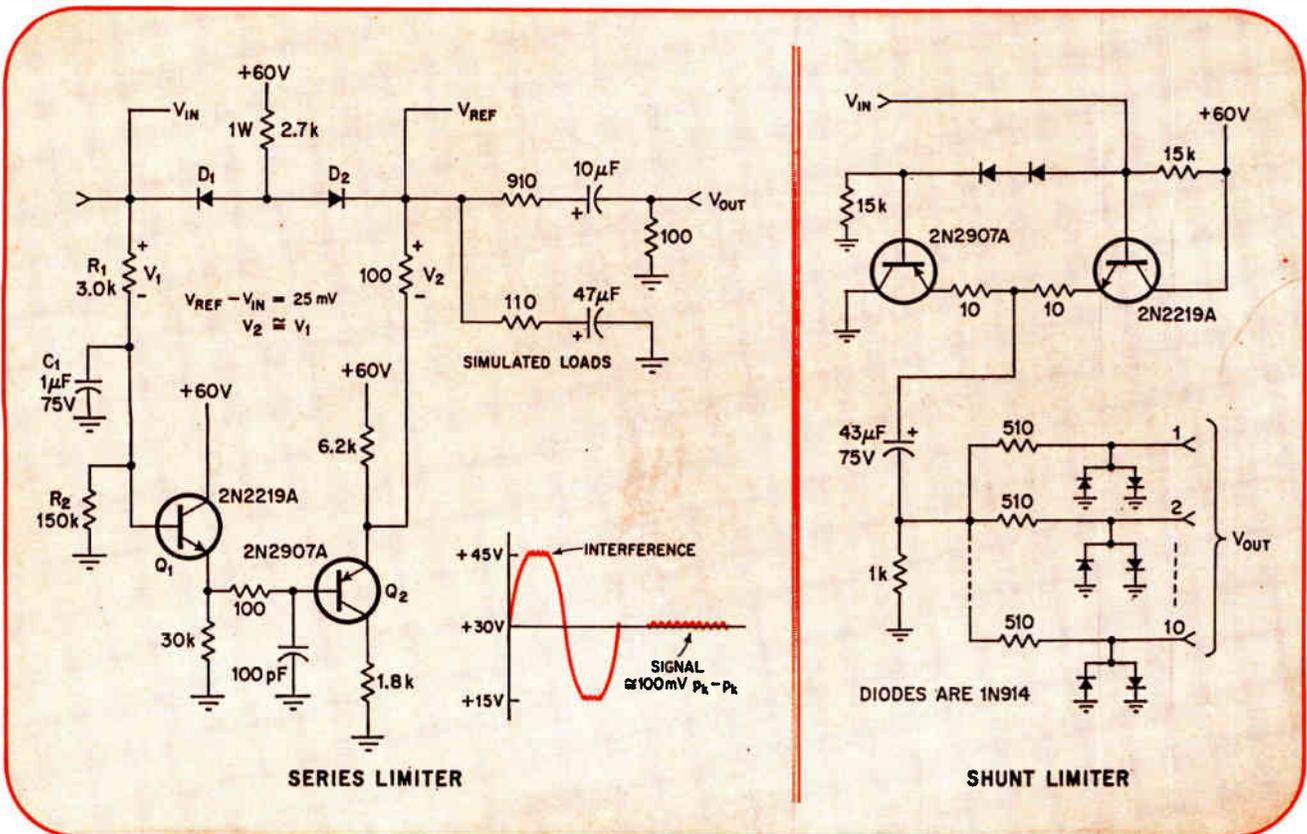
The match is made by extracting the input dc level with low-pass filter R_1C_1 and passing this level through transistors Q_1 and Q_2 . The voltage drop, V_2 , caused by the quiescent current drop, is compensated with R_2 . This resistor establishes an opposing voltage drop, V_1 . The quiescent voltage differential across the two diodes $(V_{ref} - V_{in}) = 25$ millivolts. Since Q_1 and Q_2 are complementary, their emitter-base voltage drops cancel and the output tracks the input over a wide temperature range.

Any interference signal above 400 mV drives the series limiting diode to cutoff and no interference can appear across the output.

In class A performance tests, composite signals up to 140 mV peak-to-peak passed through the limiter with low harmonic and intermodulation distortion. A 140 mV, 10-kilohertz signal produced harmonic distortion products less than -44 decibels. Two 70 mV input signals, one at 12 kHz, the other at 15 kHz, produced intermodulation distortion products less than -46 dB.

The main benefit of tying V_{ref} to the average signal level is that a large coupling capacitor is no longer required. This capacitor alone costs \$28.50 in the shunt limiter, while the total parts cost of the series limiter is \$3.

Tracking unlimited. Reference voltage of series limiter tracks the average input level. This allows low-level signals to pass with little distortion, but diodes cut off the higher interference levels. A shunt limiter, however, must block high voltage with a large, expensive high-quality capacitor to maintain a ground reference.



OP amps delay and shape data signals

by Barry M. Kaufman
Vega Electronics, Santa Clara, Calif.

Symmetrical operation, continuously adjustable delay times, and low cost are features of a delay equalizer for digital communications systems. It has been used in a high-speed modem to achieve coincidence among data signals transmitted over circuits that have different propagation delays. Signals arriving early are delayed as needed by changing the potentiometer setting.

Amplifier A_1 is a buffer that shapes the input pulses. Voltage divider R_1 and R_2 prevents the input from exceeding the amplifier's common-mode range. If the input pulses have fast rise and fall times and if they swing between the positive and negative potentials of the power supplies, A_1 isn't needed— A_2 alone will delay such pulses and keep them square.

A_2 's output follows the negative-going and positive-going transitions of A_1 's output after a delay of about $0.3 R_4 C_1$. If the output of A_1 is at the positive bus level, the noninverting input of A_2 rests at 5.7 volts and C_1 is charged. Or, when A_2 's input is negative, the rest level is -5.7 volts, and C_1 is discharged. The two rest levels are set by the drops across the diode com-

binations of D_1 and D_2 and D_3 and D_4 , respectively.

A_1 's output swings from negative to positive, current through R_3 , R_4 , and R_5 begins charging C_1 toward the positive level. After the RC time, the voltage on A_2 's input rises through zero and the output goes positive abruptly. Positive feedback coupled through C_1 and R_5 drives the input hard to the positive rest state. A swing from positive to negative reverses the action and output polarity with the same delay.

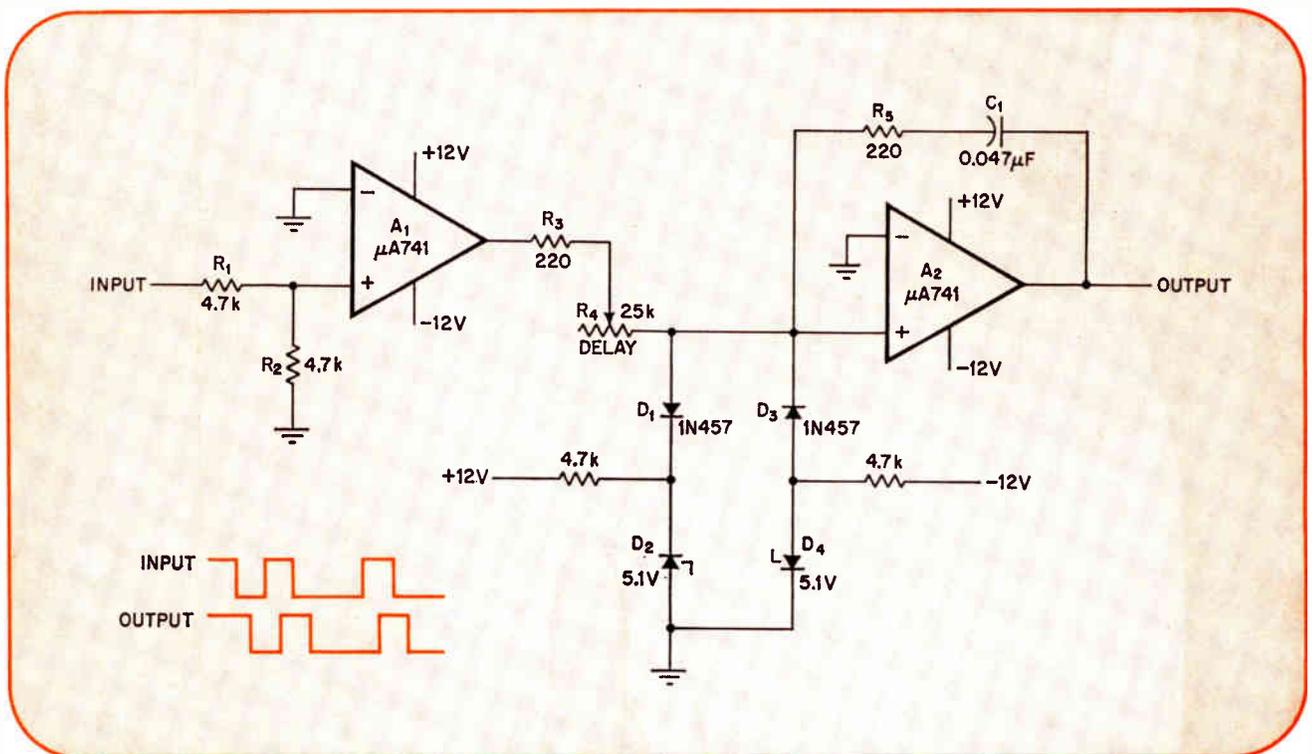
Because the delay times are equal, there is no bias distortion of the signal. The equality of the delays is assured by matching the zener voltages of D_2 and D_4 (the drop across D_1 or D_3 when they are conducting is a semiconductor constant, 0.6 volt).

Reset time is very short compared with a data bit length. Time delay is not a function of signal pulse width or pulse duty cycle, since C_1 is rapidly charged or discharged through a relatively low impedance. Delays up to 80% of the shortest bit time are obtained. With the RC values shown, they last from 50 to 400 microseconds; if C_1 is larger they can range up to tens of milliseconds. R_3 and R_5 mainly limit surge currents and have little effect on timing.

The circuit operates at a data rate of 2,000 bits per second in the modem application. An amplifier such as the $\mu A 748$ may be substituted for the internally compensated $\mu A 741$ if the 741's slew rate is too slow for higher-frequency applications.

Designer's casebook is a regular feature in Electronics. Readers are invited to submit novel circuit ideas and solutions to design problems. Descriptions should be brief. We'll pay \$50 for each item published.

Delay equalizer. Potentiometer R_4 adjusts signal delays in communications circuit. It changes the time required for C_1 to charge or discharge by varying the current flow around A_2 . The RC time constant determines when feedback into A_2 will drive the output to follow the input. Diode drops stabilize voltages and delay times.



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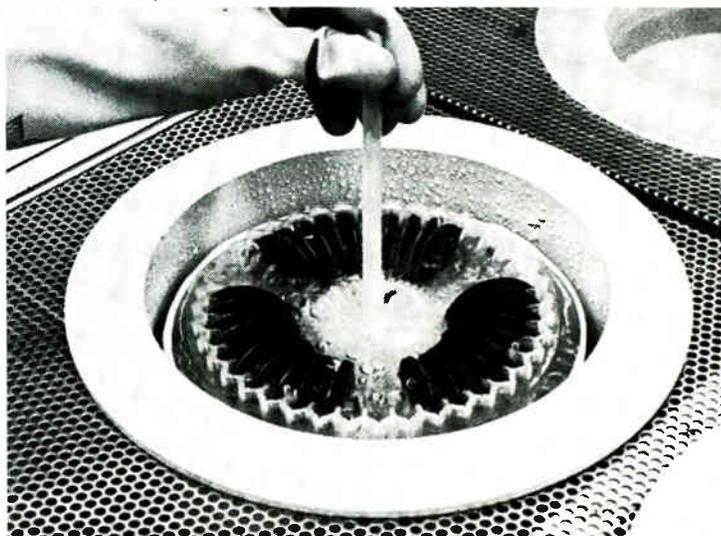
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The coming of age of the associative processor

The FAA will shortly begin tests of an air traffic control system built around the first operational model of a computer that handles unsorted data 300 times as fast as conventional machines

by J. A. Rudolph, Louis C. Fulmer, and Willard C. Meilander, *Goodyear Aerospace Corp., Akron, Ohio*

□ This spring, for the first time, an associative processor will go to work in a real-life situation. At the Knoxville, Tenn., airport, the Federal Aviation Administration will start using one as part of an air traffic control system test. At busier airports than Knoxville's, the computer can keep track of hundreds of aircraft, isolate those that are on collision courses or in other potentially hazardous situations, and provide information for display, all at 200 or more times the speed of conventional machines.

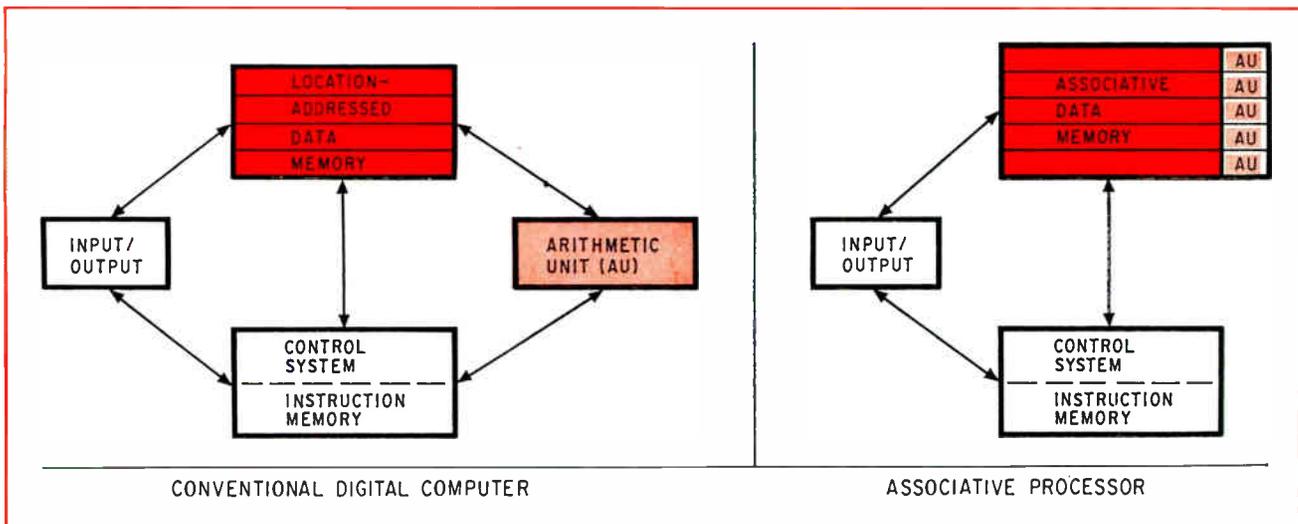
In general, an associative processor excels at searching through rapidly changing lists of random digital data for a desired item, at perhaps 1,000 times the speed of the conventional computer. It also excels at performing arithmetic operations on many pairs of numbers, with a speed advantage of perhaps 300.

This latter capability derives from the fact that associative processors are a particular kind of array processor, the class of machines that contain from dozens to thousands of simultaneously operating arithmetic units, instead of the single or few units in today's newest supercomputers of sequential design. The machine to be tested at Knoxville was built by

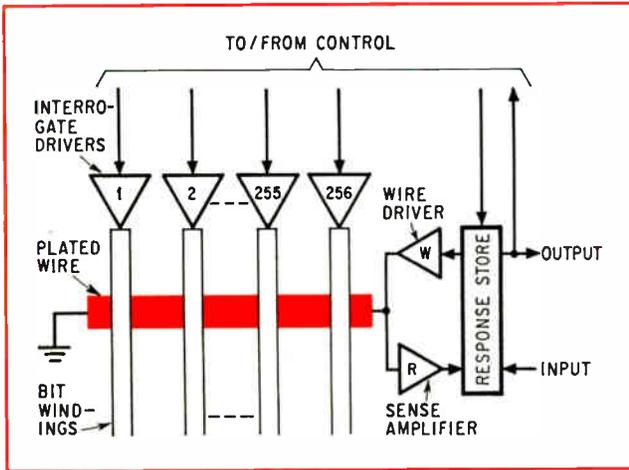
Goodyear Aerospace Corp. Other array processors, such as the Burroughs Corp.'s Illiac 4 and a Bell Laboratories machine for real-time radar tracking, may be ready for user tests within the next year or two. But of these, the associative processor is by far the least expensive.

A computer of the associative kind has of course many applications besides air traffic control—which is not to say that it can be applied efficiently to every type of problem. In fact, for highly complex information handling problems, a hybrid system that contains both associative and conventional machines is generally most effective. Still, the processor's success in the tracking and conflict-detection test at Knoxville will prove one of the important milestones in the FAA's plan to provide automatic aids to air traffic controllers. Other critical parts of the FAA Terminal Automation Program—such as display improvements and automated communication channels—may also move closer to reality, once array processing has been proven.

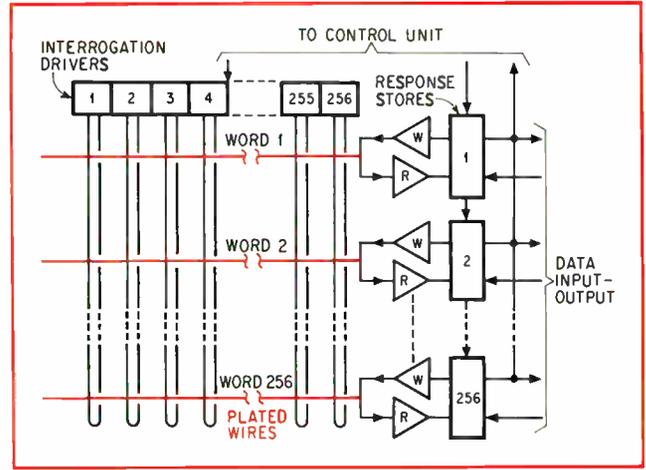
What stimulated the development of the associative processor were very real limitations of the conventional computer—its unsuitability for applications in-



1. Comparison. The associative processor's principal features, which distinguish it from the conventional digital computer, are its use of an associative memory and the replacement of the single large arithmetic unit with small serial arithmetic units, labeled A_{ij} , connected to each word in the memory.



2. Processing element. The Goodyear associative processor comprises many basic elements, each consisting of one plated wire and one response store. The wire stores 256 bits.



3. Processor module. The associative processor's basic building block is this module, itself containing 256 processing elements. Because each element stores 256 bits, the module is logically "square."

volving high-speed searches of large, rapidly changing data bases, and its inability to perform more than one or a few arithmetic operations at a time. This first became obvious in real-time automated command and control systems and later in the extremely complex equations encountered in nuclear reactor design and worldwide weather forecasting.

The problem derived from two of the sequential computer's basic characteristics: its memory must be addressed by specific location, one word at a time, and it can perform only one operation, such as "add," at one time. And if the entire content of a memory has to be checked through and processed serially, a lot of time is necessary.

The obvious answer—ever-increasing computer speed—soon could be pushed no further. Hardware designers found that even when they increased circuit speeds they couldn't get around the transmission line delays between circuit elements. Moreover, new software improvements, though they simplify computer operation, have tended to cancel speed increases in hardware because they devote growing amounts of memory space and active computing time to non-productive overhead and bookkeeping chores.

A new computer architecture that circumvented the sequential machine's limitations was necessary, and the associative processor provides it. First, the associative processor does not need addresses, but uses the characteristics of stored data directly. To locate a particular item, or group of items with a common characteristic, the processor simply calls for the desired characteristic; words with that characteristic are immediately identified in the memory, whatever their location. In this way, the data's location in the memory need not be known in advance, nor does the processor have to check every word one at a time or sort the incoming data as it arrives. And sorting not only slows down the loading process considerably, but is valueless for satisfying a request that doesn't fit the pattern according to which the data was sorted

when it was loaded.

Second, the associative processor can perform many operations simultaneously. Suppose it's necessary to obtain the sums of many pairs of numbers stored in the memory. In the sequential processor each pair passes one at a time through a single adder, and even with a fast adder, if many pairs must be added the total computation time is long. But in the associative processor each word in the memory has its own simple adder, and all the adders can form sums simultaneously. Although each one is relatively slow and takes longer to obtain an individual sum than would a high-speed central adder, the total elapsed time for obtaining all the sums is orders of magnitude less than with the central adder.

These two major differences between the conventional digital computer and the associative processor are shown in their block diagrams (Fig. 1). In the associative processor, the single arithmetic unit of the conventional machine has been eliminated, and the location-addressed, sequentially accessed memory of the conventional machine has been replaced with an associative array, which is a modified associative memory, search memory, or parallel search memory. The main memory in the conventional computer usually contains both data and instructions, but for the sake of this illustration a separate memory, part of the control system, contains the instructions. The associative processor uses the usual input/output equipment, controls, and instruction memory.

Because the associative array can simultaneously compare all the items it contains against some input item, it takes only one memory cycle to locate any data item or portion of an item—a matter of microseconds. (The item located may exactly match the external word, or may bear some other specific relation to it—greater than, less than, and so on.) The conventional computer, however, would require two cycles per item—one to fetch the instruction and one

Parallel association

Although Goodyear Aerospace Corp. has a good leg up on the possibilities of solving air traffic control problems with an associative processor, not all observers are sure that the company's approach is necessarily the best.

One source familiar with the FAA activities in air traffic control underlines the tremendous number of variables that must be taken into account in aircraft conflict prediction and avoidance—not only the aircraft's position, speed, and direction, but also the type of aircraft, its size, weight, potential rates of ascent and descent, and so on—and he questions if Goodyear's system is really capable of absorbing all this data quickly enough.

Another associative processor approach is being taken by the Aerospace and Defense group of Honeywell, Inc. Though not under a contract to the FAA at present, it has been working on the air traffic control problem as an extension of another contract it has, to build an associative memory for the National Aeronautics and Space Administration.

Honeywell's approach is to combine an associative memory made of metal oxide semiconductor circuits with a random-access memory made of bipolar circuits. In its present design both memories have capacities of 256 words, like Goodyear's plated-wire module, but the associative word length is 104 bits and the random-access word length is 128 bits. These are interrelated in such a way that in effect the system consists of a single memory of 256 words by 232 bits, of which 104 bits are associatively addressed (Goodyear's is 256 by 256, with

all bits associatively addressed). This memory, a serial adder and appropriate controls form the basic module of the associative processor.

Dale Gunderson, a research section chief at Honeywell, claims that this approach has some important advantages over Goodyear's plated-wire design. First, fully parallel reading and writing and fully parallel searching are possible with the solid-state design. Second, this fully parallel transfer of data permits much easier interfacing of the associative processor with a general-purpose processor—and any reasonable installation requires both kinds of programs, as the authors point out in the accompanying article.

In Goodyear's design, all searching and all data transfers out of the array are carried out serially by bit in any given word, although in parallel through all words involved in the operation—a "bit slice." Data can also be put into Goodyear's array in parallel.

Most associative processor operations are basically serial, so Goodyear's approach works. It's just that searches and data transfers, when they occur, are handled in parallel, according to Gunderson.

Honeywell's work is probably the next closest to practical application, after Goodyear's. Meanwhile, Goodyear has built its own solid state associative processor and can demonstrate it for prospective customers; and the Air Force continues to support work on the plated-wire module, particularly a militarized version.

—Wallace B. Riley

to fetch the item. Execution time in most computers would be a negligible part of the second cycle.

For example, to search an unordered list of 3,000 items a high-speed conventional computer with a typical cycle time of 0.5 microsecond would need approximately 3,000 μs . But the associative processor can search that list in less than 3 μs , a 1,000-to-1 improvement. Furthermore, only one instruction need be written for the associative processor to perform the entire search.

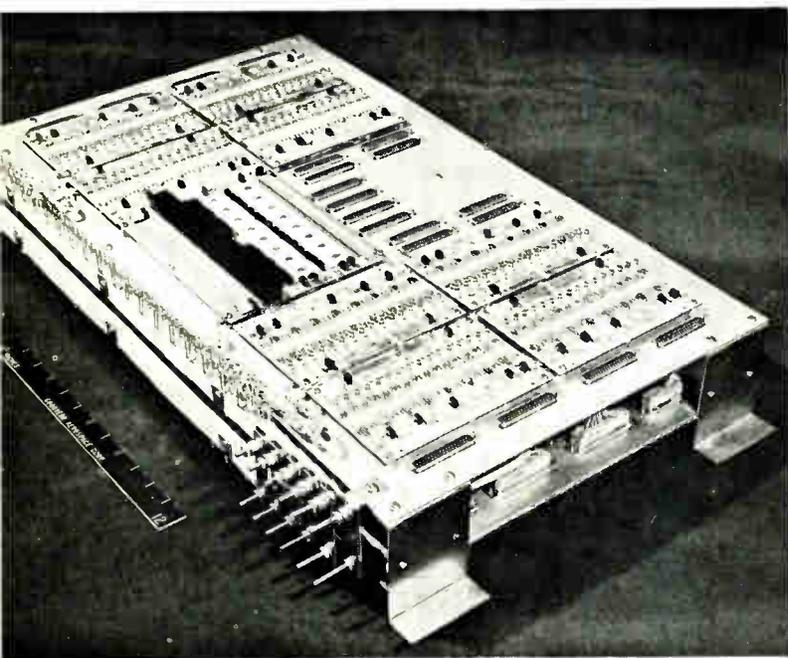
Similarly, the logic and arithmetic cells, which are attached on a one-to-one basis to each word in the associative array and replace the conventional processor's arithmetic unit, also speed up operations when the number of items to be handled is large. These cells operate serially by bit on the data in the memory word to which each is connected. All the individual cells simultaneously execute the same instruction as directed by the control unit. Thus, in one instruction execution time, data from every word in the array is simultaneously processed through the arithmetic unit at each word.

A high-speed, 0.5- μs -cycle-time conventional machine, processing all bits in parallel, can retrieve and add two 24-bit items and store the sum in approximately 3 μs . An associative processor working serially at the rates listed on page 95 might take 28 μs to do the same thing. But if 3,000 such data pairs must be added together, the associative processor would

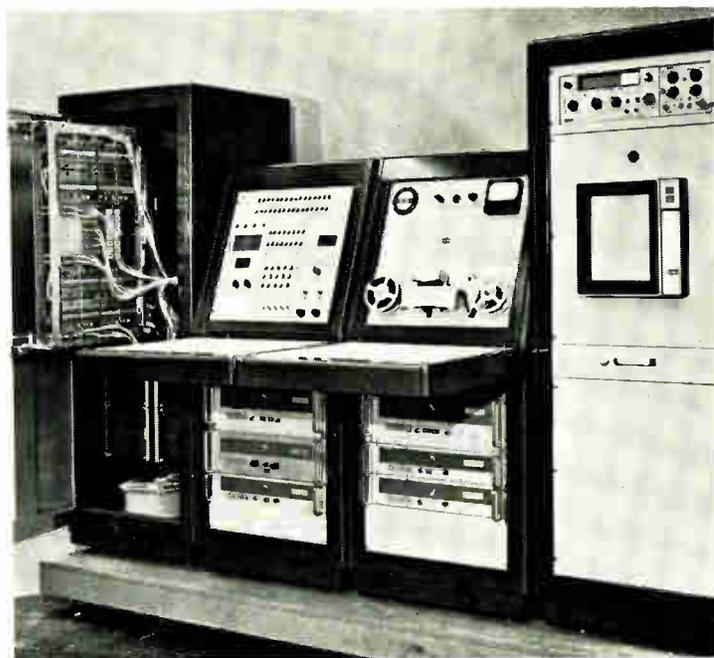
still take 28 μs , while the conventional computer would take 9,000 μs .

Only when the items are few does the conventional processor take less time than the associative processor, because the conventional processor does its processing bit-parallel, not bit-serial. With a greater number of items, the processing time for the conventional processor increases rapidly, but that for the associative processor increases very slowly, if at all.

After all, the associative processor is in effect the equivalent of many very simple digital processors containing a one-word memory and an arithmetic unit, all operating simultaneously from a single central control unit and an instruction memory. However, while words in the conventional memory are only 12 to 48 bits long, words in the associative array are likely to be hundreds of bits long. For one thing, the more bits attached to the arithmetic unit the less the cost per bit for hardware. For another, each memory word must be long enough to hold data words being operated upon and a place to store results. These lengthy words can be divided into shorter subwords under program control, and the associative processor can operate on the subwords in much the same way as its conventional counterpart operates on different words. For example, field A can be added to field B and the result stored in field C; or field C might be multiplied by field D and the result stored in field A. In addition, any of these fields can be compared



4. Array module. From assemblies like this, full-scale associative processors can be built. This unit contains 256 processing elements, each with a single plated wire storing 256 bits.



5. Model and exerciser. This demonstration unit, although not a fully fledged associative processor, is capable of showing the concept's feasibility. It is to be installed at Knoxville.

with an external word during associative searches, to identify those subject to further processing.

Programing costs are usually roughly proportional to the number of instructions required to execute a given task. For conventional computer applications these costs usually equal or exceed the hardware costs and for supercomputers are likely to be even higher. But the associative processor requires significantly fewer instructions to execute a given task and therefore is much less costly to operate.

In a typical large real-time system that manages a continuously changing data base, for example, the associative processor system would require fewer than 10% of the instructions needed by a conventional multiprocessor system. It's therefore an attractive approach to problems divisible into parts that can be simultaneously processed.

In addition, for these applications the associative processor is easier to program than any conventional multiprocessor or array computer; so fewer false starts occur, and execution time and memory space are more easily kept within reasonable bounds.

The two features that simplify the associative processor's programing are, once again, its parallel content addressing and simultaneous instruction execution on the entire data base. Parallel content addressing avoids all the bookkeeping problems that go with serial location addressing; data can be stored and retrieved in the associative processor without regard for its physical location in memory. And the ability of the associative processor to execute a single instruction simultaneously on many data words eliminates the need for most program loops used in the conventional processor; that is, it need not make more than one pass

through any sequence of instructions, whereas the conventional processor would require certain sequences of instructions to be repeated separately for each set of data.

The fact that both programing and execution time are independent of the number of data sets permits the capacity of the associative processor to be expanded modularly without any need for reprograming. This is extremely important in applications where the processing load is expected to increase.

Representative sets of search and arithmetic instructions for an associative processor are shown in the table. The timing formulas, although for a particular associative processor and a particular set of microprograms, are typical for most associative processors. They show that the execution time is proportional to the number of bits in the fields but is independent of the number of words in a field.

To build an associative processor, no unusual components are necessary. On the contrary, one associative-memory word can be stored in ferrite cores, semiconductor arrays, or plated wire, while the arithmetic and logical cell to process that word can be made from discrete transistors or from individual, medium-scale or large-scale integrated circuits. The choice depends on the tradeoffs the designer makes among speed, cost, power, and production readiness.

In the case of the associative processor to be installed at Knoxville this year (see Fig. 2), Goodyear Aerospace selected plated wire for the memory element because of its high-speed and low-power characteristics, and medium-scale ICs for the arithmetic unit because they match the packaging density of the plated-wire memory at the lowest obtainable cost.

A major part of the arithmetic unit is the response store, which in a simple associative memory provides logic and buffering for the storage element. Actually, in this associative processor only the response store logic is repeated for each word; the remainder of the machine's arithmetic capability is in the controls, which are common to many words. The response store plus the control unit together function as a serial arithmetic unit, a one-bit store for responses to a search, a buffer for parallel input or output, and a writing control for storing data in the plated wire. Depending on the operations required of the associative processor, the response store might take on different logic forms.

In Goodyear's associative processor the plated-wire design, with hybrid drive and sense electronics for the memory element and an MSI chip for the response store, gives read and write speeds of 100 and 300 nanoseconds, respectively. This in turn yields an exact match search time of 0.1 μ s per bit and an add time of approximately 1 μ s per bit.

The associative processor's basic building block is a 256-word module. It contains 256 processing elements, each consisting of one response store and its length of plated wire, and 256 interrogation drivers, each driving a printed-circuit conductor, or "strap". The strap encompasses all the plated wires in the module and can interrogate any one bit of all 256 words in the module in parallel. The module, diagrammed in Fig. 3, is therefore "square," or 256 words of 256 bits each.

The module has several capabilities that are not obvious when only the basic response store is considered. For example, it's capable of problem partitioning, and it contains interconnections that link adjacent processing elements to one another. With problem partitioning, different classes or types of data, perhaps to be processed by the computer in wholly unrelated tasks, can be stored in the same module. A few of the 256 bits in each word serve as identifiers or tags to separate the classes. The linking of elements permits the apparent word length in the computer to be extended; it also permits arithmetic operations to be performed on fields from different words just as on fields within the same word.

But basically the response store's function is to signal success once a search has located an item in the word to which it is attached. All such signals from a single module are fed into an equivalent OR function, whose output signals the control unit that at least one word has responded to the current search. Such a response triggers a subroutine in the processor that proceeds to identify the responder, or process it, set a bit to shield it from subsequent searches, and then search for any additional responders to the original inquiry. Processing of the individual words may range from simply counting them to performing extended arithmetic operations on each of them.

The control unit in Goodyear's model, which can supervise several modules, is conventionally designed and can be functionally divided into a sequential-instruction part and an associative-control part.

The sequential-instruction part is similar to the

control system of a conventional processor. It includes conventional input-output equipment and a conventional location-addressed memory, whose chief function is to store and process the stream of instructions that the associative processor modules are to execute.

The associative-control part is a set of registers, counters, control line drivers and receivers that control all associative processor modules. Since at any time only a single instruction is being executed in all modules, the counters and registers are common to all modules. Only the number of control line drivers and receivers depends on the number of associative processor modules.

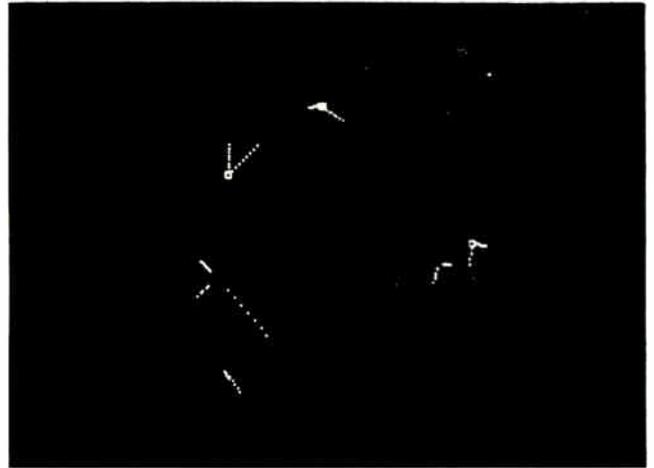
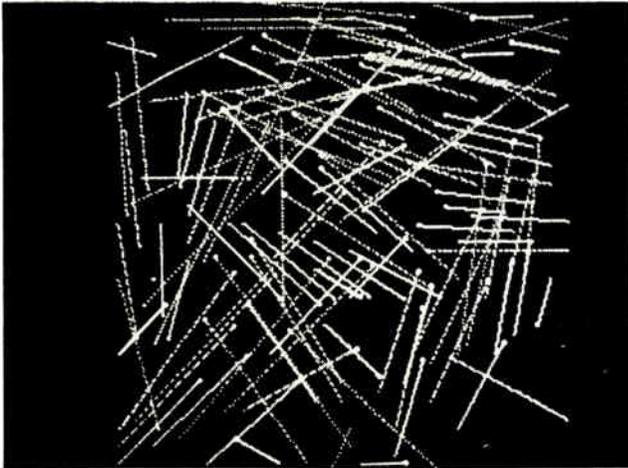
The practical limit on the number of modules depends on the hardware size and the processor's speed requirements. Since a single plated-wire module occupies only about 0.5 cubic foot, even 128 modules would not be very large. But so far we have found no application that required more than 24 modules; even a 16-module associative processor can process up to 250 million instructions per second. Since the parallel input/output channel is available for each word of the memory, a 16-module processor also has a tremendous capacity to accept or transmit data.

Because of its simple construction the associative processor is relatively inexpensive. Other superscale machines, such as Control Data Corp.'s STAR, 7600 or 6600, IBM's System 360 models 91 and 195, or the Burroughs/University of Illinois Illiac 4, can process from 2 million to 200 million instructions per second at a cost to the user of \$3 million to \$10 million. But the user cost of an associative processor capable of 325 million instructions per second is projected to be only \$1.5 million.

The associative processor to be installed at Knox-

Typical execution times	
Instruction	Execution time (microseconds)
Search	
Exact match	$0.1(n + 4)$
Less than	$0.1(n + 4)$
Greater than	$0.1(n + 4)$
Maximum value	$0.2(n + 2)$
Minimum value	$0.2(n + 2)$
Next lower	$0.3(n + 3)$
Next higher	$0.3(n + 3)$
Arithmetic	
Add common	$0.8(n + 1)$
Add fields	$1.1(n + 1) + 0.1$
Multiply common	$0.8n_1(n_2 + 3.2)$
Multiply fields	$1.1n_1(n_2 + 2.7)$

n=number of bits in pertinent data field.



6. With and without. At the left is the demonstration model's display of the tracks of 128 aircraft in a 64-mile-square airspace over a few minutes of time. In the same simulation displaying only conflicting tracks, several collisions or near misses are evident (right). With radar scanning the air space every 4 seconds, these computations occupy the associative processor less than 0.1% of the time.

ville will contain only one module, however, like the one in Fig. 4, and will make use of only a quarter of the full array design. Out of its total of 256 words of 256 bits each, only 128 128-bit words will be required to handle the traffic density around Knoxville and to satisfy the FAA's requirement for initial tests.

The processor itself is the same piece of equipment, shown in Fig. 5, that was first demonstrated at Goodyear Aerospace Corp. in July 1969 and has been put through many other demonstrations since. Built under contract F33-615-C-1555 for the Air Force Materials Laboratory, Wright-Patterson Air Force Base, Dayton, Ohio, it's being lent by the Air Force to the FAA and will be interfaced to Knoxville airport's existing installation with equipment supplied by Goodyear.

The demonstration of this processor's operation involved exercising the associative array through a variety of programable, content-addressed searches and simultaneous arithmetic operations followed by realistic combinations of these functions in simulated real-time command and control systems. It established that even a small associative processor of 128 words is extremely capable, and only small changes would be needed to add considerably to its capabilities. For example, it could achieve a processing rate of 4 million 32-bit add instructions per second—and this rate could be doubled if the response store design were altered slightly by, for example, adding a flip-flop to store the carry bit from a one-bit addition.

In one of the simulated command and control systems, the model was programed to simulate the motion of 128 aircraft in real time over an area 64 miles square—the density within each of several 1,000-foot altitude slices predicted for the Los Angeles area in 1990—and to identify aircraft flying collision or near-collision courses. Two versions of the program were displayed, one showing all 128 tracks, and one showing only the tracks of aircraft in danger of colliding as shown in the photographs above.

To solve and update the collision detection problem for 128 aircraft, the associative processor required only 3 milliseconds of each simulated 4-second radar scan, in contrast to the over 700 milliseconds per 4-second scan required by a large-scale, conventional computer executing the same task. In an actual installation the computer would have much more to do; in addition to conflict detection, it would have to track all the aircraft while maintaining identification of each, define evasive maneuvers when conflicts arose, translate the data into a form suitable for display, and perform many other tasks. For 128 aircraft these other tasks in the conventional computer would use almost all the remaining 3,300 ms of radar scan time. Furthermore, the larger the number of planes, the worse the comparative performance of the conventional computer becomes. For the time it takes to deal with them is roughly proportional to the square of their number, whereas the time an associative processor takes is only linearly proportional. □

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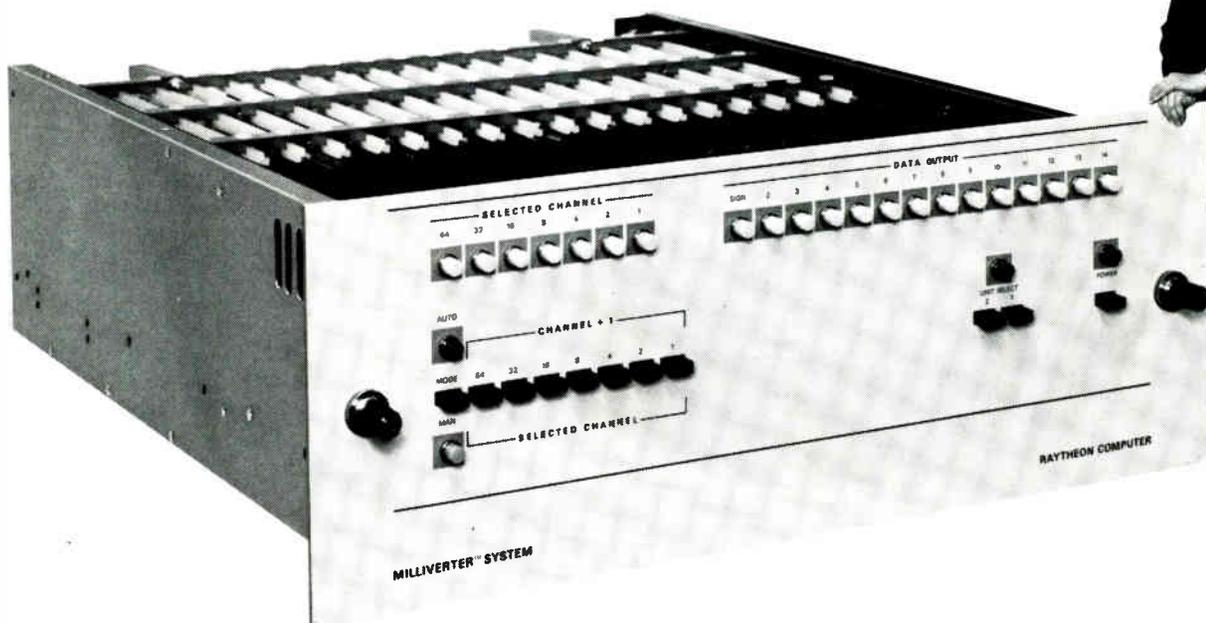
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Double-diffused MOS transistor achieves microwave gain

MOS devices with 1-micron channels made by two-stage diffusion rival discrete, bipolar microwave transistors in performance and also promise a fivefold increase in digital logic speeds

by T. P. Cauge, J. Kocsis, H. J. Sigg, and G. D. Vendelin, *Signetics Corp., Sunnyvale, Calif.*

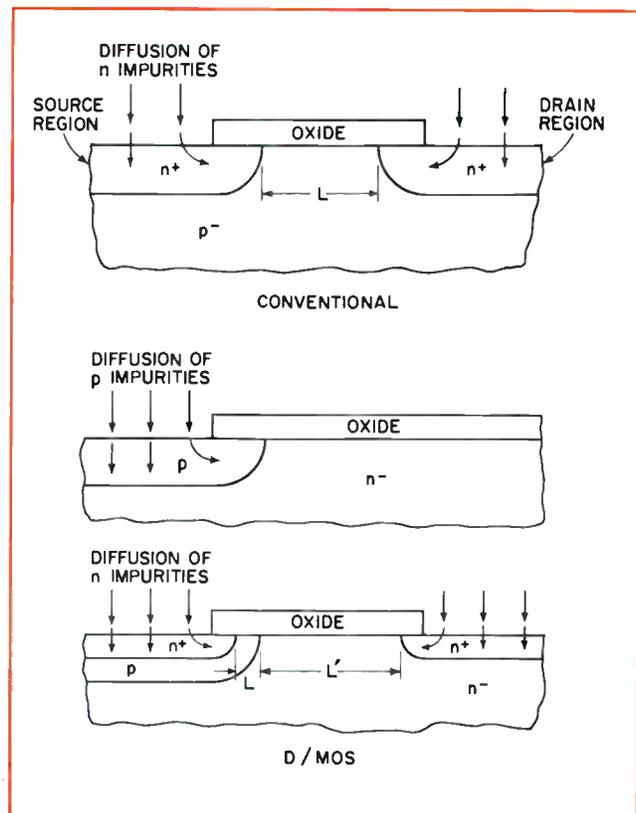
□ A new way of making metal oxide semiconductors not only multiplies their speed by a factor of five but opens up the entire realm of microwave applications to MOS technology. Called D/MOS, it involves a two-stage diffusion through a single mask opening, permitting channels of 1-micron lengths to be formed simply and inexpensively.

The result: discrete microwave transistors that exhibit a 10-gigahertz maximum frequency of oscillation, a 7-decibel gain at 2 GHz, and a noise figure of 4.5 dB at 1 GHz—performance usually associated only with bipolar devices. On the digital side, the D/MOS devices can be switched with subnanosecond speeds, and have the added advantage of high breakdown voltage if needed.

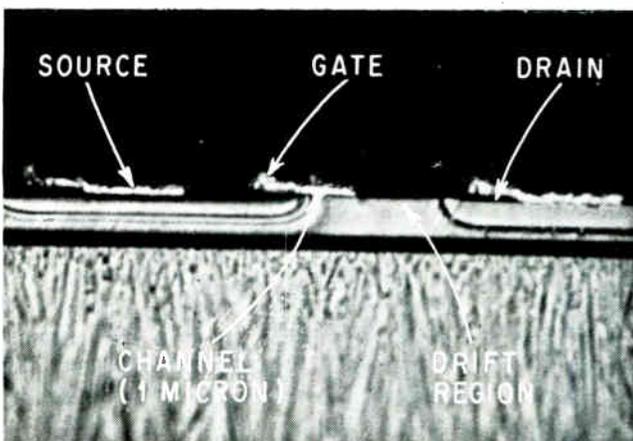
Discrete microwave FETs could only be obtained with a channel length of about 1 micron, which requires metal gate widths also of approximately 1 micron. But to manufacture devices with such narrow gates it has been necessary to use sophisticated, highly accurate photomasking techniques. Moreover, for digital ICs, high speed is also dependent on highly controlled doping and diffusion steps. The D/MOS process, on the other hand, achieves its micron-long

channels with metal widths and oxide openings no smaller than 8 microns, demanding photomasking and diffusion tolerances no stricter than those presently used in conventional bipolar IC technology.

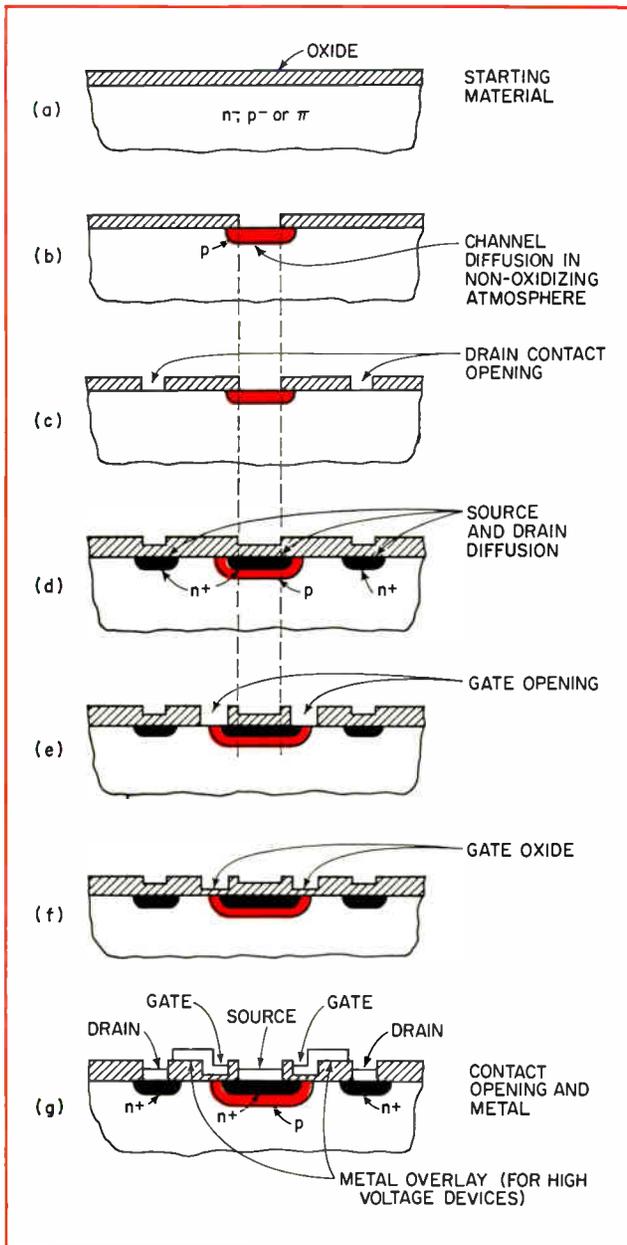
The high performance of D/MOS devices results directly from the method of forming the channel—the region between the source and drain. Figure 1 shows the cross-sections of a conventional, n-channel MOS device and a D/MOS device. In general, the



1. Process with a difference. Region between source and drain in conventional MOS structure (top) forms practically the entire channel length L , but in D/MOS structure it consists of a short channel L and a long drift region L' . Also, conventional channels require accurate control of oxide widths, whereas D/MOS channels are independent of oxide widths.



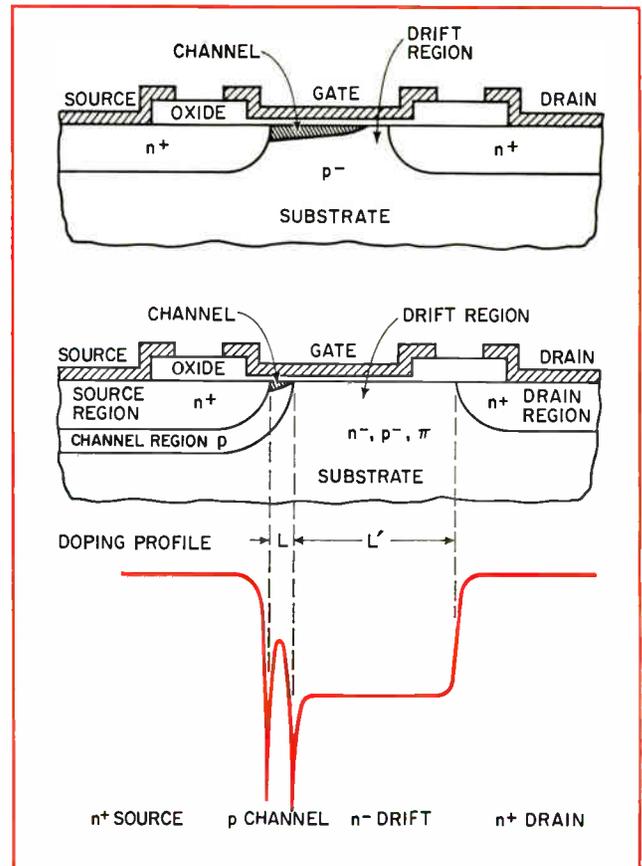
New channels. Photomicrograph shows cross-section of a typical D/MOS transistor; 1-micron channel lengths for microwave performance are produced by diffusing opposite-type-dopant impurities under a single mask edge, eliminating need for costly micron-dimensioned masks.



2. One method. Channel diffusions begin with step (b), when the oxide is opened and the first (p-type) diffusion is made. The second (n⁺) diffusion is made as shown in (d), for the source and drain regions.

frequency response, or speed, of any MOS transistor is determined primarily by channel length L and parasitic capacitance C , and improves as they become smaller. Reducing L cuts the transit time for carriers traveling between source and drain, while reducing C will decrease the charging time. (In an MOS device, parasitic capacitance exists between gate and drain, C_{GD} , sometimes called the feedback capacitance, as well as between gate and source, C_{GS} .)

In the usual MOS devices, unfortunately, a short L usually entails large parasitic capacitance, because the separation between source and drain determines the amount of sideways diffusion under the gate for a



3. Doping it out. Doping profile across D/MOS transistor (bottom) differs from conventional MOS device: profile is nonuniform in the narrow channel region. Most of the conductance-modulation takes place in the channel, which has characteristics that control the device's speed and gain.

given L , and the sideways-diffused region, which is also highly doped, represents large C_{GS} or C_{GD} . True, these parasitics can be minimized by the ion implantation and polysilicon gate processes, which are self-aligning and reduce the overlap between the gate region and the source and drain region. But they are expensive techniques. Moreover, MOS transistors that are conventionally processed with short L exhibit breakdown at low voltages.

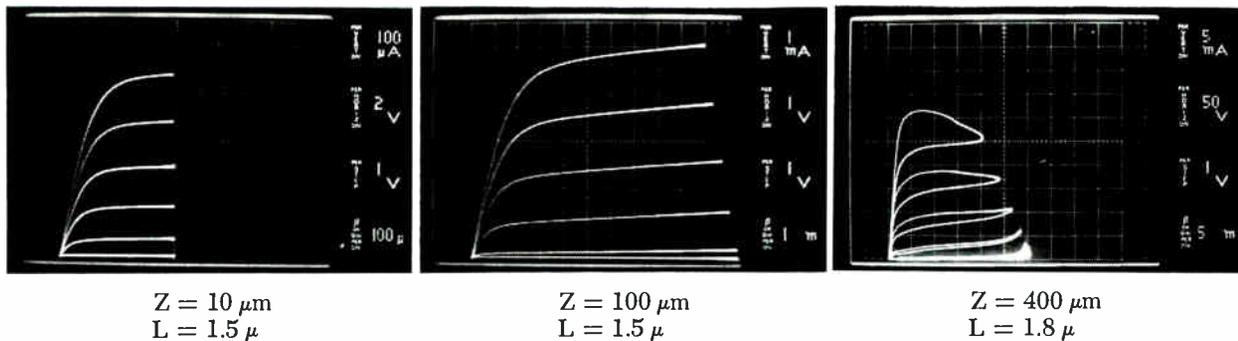
The D/MOS process eliminates all these problems, and results in a device which has a precisely controlled L of less than 1 micron, minimal C_{GS} , very small feedback capacitance C_{GD} , and no restriction on maximum drain breakdown voltage. As Fig. 1 illustrates, the D/MOS channel is a narrow region, sandwiched between two opposite-type regions and created by the sequential diffusion of two opposite-type dopant impurities under a single mask edge in the source region. Once this edge is formed, the critical distance L is a function only of the diffusion schedule—masking, exposure and etching errors are eliminated—and since one diffusion edge follows the other, L can be controlled in much the same way as is the base width of a bipolar transistor.

D/MOS shows its stuff

The high performance available from the D/MOS process is confirmed by the dc characteristics of typical devices. Curve traces show drain current, I_D , as a function of drain voltage, V_D , for different values of the channel width, Z . Each trace was recorded at a different value of gate voltage, ranging in 1-volt increments from 0 to 5 volts.

The transconductance, g_m , a measure of device gain, is the change in drain current with gate voltage. Since the gate voltage steps in the traces shown are 1 volt,

g_m corresponds to the difference in the curves for sequential steps of gate voltage after saturation. For any channel width, g_m quickly saturates, typically at small gate voltages of 4 to 6 v. This indicates that a D/MOS device achieves its optimum performance at these voltages, in sharp contrast to conventional MOS devices, which have to be driven hard to achieve maximum speed and gain. In fact, conventional p-channel devices typically require comparatively high supply voltages, in the range of 15 to 30 v.



Admittedly, sideways diffusion also controls channel length in the conventional process. But there it leads to large overlap parasitic capacitance when narrow channels are required. For the D/MOS process, the sideways diffusion lengths are much smaller, even for very narrow channels, and because overlap capacitance only exists on the source side for D/MOS, it can be kept to a minimum.

Channel lengths in the range of 0.4 to 2 microns are easily achieved in D/MOS processing, even when the relatively noncritical bipolar diffusion schedules are used. In contrast, because the variations in mask quality, exposure and etching can affect channel length by 1 micron or more, typical MOS transistors in production today are fabricated with 5-micron lengths, and for this reason are unable to compete in speed with bipolar devices.

The details of fabrication are illustrated in Fig. 2. First, the oxide is grown on the substrate starting material, which can be an n^- or p or π substrate type. Next, the oxide is opened and the first, p-region, channel is diffused, to a depth of 0.5 to 3.0 microns. Since the oxide edge determines the self-alignment of the channel (the second, n^+ , diffusion in the double diffusion process is also made through this opening), it must be as sharp a vertical cut as possible.

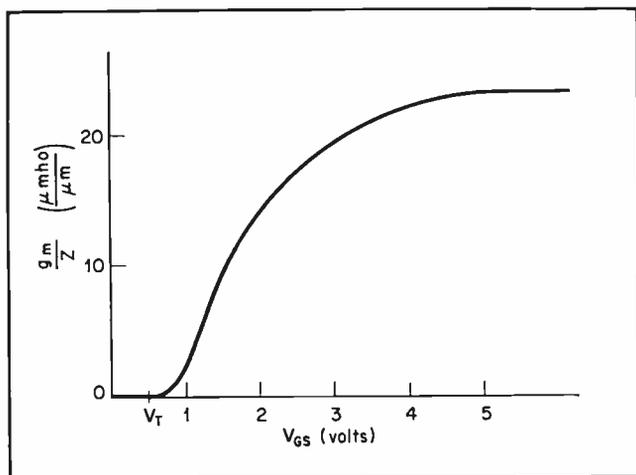
The major portion of the p diffusion can be carried out in an inert, nonoxidizing atmosphere like nitrogen. For one thing, the diffusion edge ought not to be contaminated with too much oxide material, since removal of the excess prior to n^+ source diffusion would damage the edge's definition. For another, the p-region at the surface during this step is critical, since, as in all MOS processes, the channel doping profile determines the threshold voltage.

Once the first diffusion is complete, the drain contact is opened while at the same time the original channel edge is protected. Then the n^+ source and drain regions are diffused in an oxidizing atmosphere as in conventional MOS, the diffusion through the original channel opening forming the required source diffusion. During this step the source and channel doping profiles are superimposed to give the required narrow p-type channel region between the n^+ source and the starting substrate material.

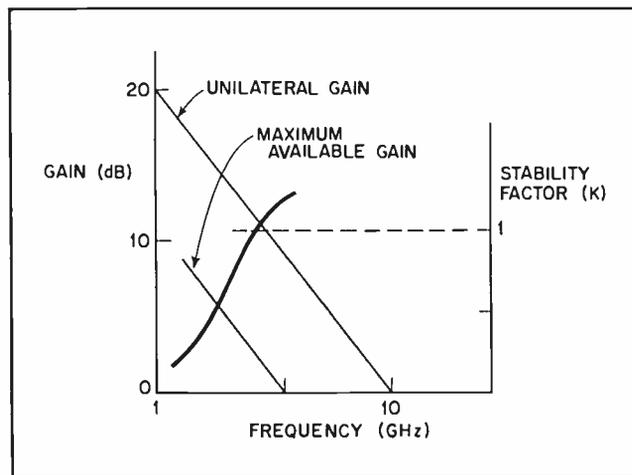
The remaining steps are identical to conventional MOS processing, except that in D/MOS the size and location of the gate electrodes lead to special benefits. The gate metal doesn't just serve to modulate the channel conductance, as in conventional MOS, but the electrode, by overlapping the substrate material, also acts as a field plate and gives D/MOS its high-voltage capability. In addition, the gate metal is also offset from the drain's n^+ region to minimize gate-to-drain capacitance.

Details of the construction and operation of a D/MOS device, and how they differ from those of conventional MOS devices, are shown in Fig. 3 (the widths of the metal electrodes are assumed to be the same for both cross-sections). What makes the D/MOS device different is the additional layer of impurities—the p-channel region—that exists between the source and the substrate. Whereas conventional MOS has one active channel region between source and drain, the active part of D/MOS consists of two well defined regions: a short modulated inversion region, and a longer drift region. The short region forms the channel and gives the D/MOS device its speed.

In spite of differences in construction, operation of a D/MOS transistor is similar to that of an ordinary



4. Making big gains. Since maximum gain occurs at only 4 volts above threshold, low-voltage D/MOS circuits are possible. Conventional MOS, on the other hand, requires large driving voltages for same gain.



5. Microwave bound. Microwave gains are achieved with D/MOS construction. Prototype devices exhibit f_{max} of 10 GHz and maximum available gains up to 5 GHz. Values of K above 1 indicate unconditional stability.

MOS transistor. The number of carriers in the channel is controlled by voltage applied between gate and channel, their velocity by voltage applied between drain and source. The product of the number of carriers and their velocity is proportional to the drain current. In the n-channel case, the carriers are electrons delivered by the source; they travel with increasing velocity through the channel, which injects them into the drift region, from which they are finally collected by the drain. In the D/MOS device the channel is so short that even a low voltage across it is enough to accelerate the carriers to their highest possible velocity, v_s , or the scattering-limited drift velocity. At this carrier velocity, the device's operating speed is at its maximum.

The important device equations for the D/MOS structure can now be given. Since the number of carriers in the channel is determined by the gate voltage, a small change in that voltage, ΔV_G , produces a maximum change in drain current:

$$\Delta I_{D,max} = v_s C Z \Delta V_G \quad (1)$$

where C is the gate-to-channel capacitance per unit area and Z is the gate width. It follows that the ratio of transconductance to gate width, g_m/Z , is equal to $v_s C$, (or $24 \mu\text{mhos}/\mu$ for this device, since v_s is 6.5×10^6 cm/s and oxide thickness is $1,000 \text{ \AA}$).

At a large enough drain voltage, called the saturation voltage, $V_{D,sat}$, the drain end of the channel ceases to be inverted. A further increase in drain voltage does not affect the current, because the channel is pinched off at the end. According to basic MOS theory,

$$V_{D,sat} \cong V_G - V_T \quad (2)$$

where V_G is of course the gate voltage and V_T the threshold voltage at which the device starts to conduct.

For the carrier velocity in the channel to approach the limit, v_s , the voltage across the channel divided by its length must exceed a certain critical field strength, E_{crit} . The value E_{crit} is also important in determining the maximum transconductance, or gain.

For the highest transconductance, the average field in the channel, $V_{D,sat}/L$, should be larger than the critical field for velocity saturation or, in terms of the second equation,

$$\frac{V_G - V_T}{L} \cong E_{crit} \quad (3)$$

When the channel ejects the carriers into the drift region, their number is no longer controlled by the gate voltage (as it was in the channel) but by the current from the channel. Their velocity, as they are swept through the drift region, is established by the local electric field strength. If the drain voltage is sufficient to maintain an electric field strength higher than E_{crit} in the drift region, the carriers move with velocity v_s , to the drain, where they are collected. Transit time through the drift region, τ_{td} , is

$$\tau_{td} = \frac{L_d}{v_s} \quad (4)$$

where L_d is the length of the drift region. For $L_d = 5 \mu$ and $v_s = 6.5 \times 10^6$ cm/s, τ_{td} is only 80 picoseconds. If, on the other hand, the field in the drift region is weak, the number of carriers has to be high, and the region acts as a resistor.

It should be noted that if the gate voltage changes suddenly, the drain current does not change immediately. To increase or decrease the number of carriers in the channel, the gate-to-channel capacitance has to be charged through the channel resistance. In addition, the transit time through the drift region causes a small delay.

Several design advantages result directly from the D/MOS short channel lengths. From theory, current driving capability, g_m , and the gain-bandwidth product, f_t , bear a reciprocal relationship to the channel length and to the square of the channel length, respectively, the D/MOS device, with about a fifth the channel length of conventional n-channel MOS, offers a g_m greater by a factor of 5 and f_t greater by a factor of

Versatility's a virtue

Flexibility is one of the strongest attractions of the D/MOS process—it allows the designer a choice of several different materials and fabricating techniques to fit his application. Basically, the same double diffusion schedule can be used with bulk, epitaxial, or silicon-on-insulator (SOI) substrates. The high-resistivity portion of the device can be n^- , p^- or π , and variations of the process include use of ion implantation, silicon gate technology, or the MNOS technology to achieve better processing control and/or self-alignment features.

For bulk substrate devices, either n^- , p^- , or π material can be used. If n^- substrate is selected, the device will exhibit very low feedback capacitance, C_{GD} , because the drift region normally will be depleted. This makes it very attractive for linear amplifier applications, where low C_{GD} results in high gain and independent matching of input and output. Furthermore, depletion into the drift region results in high-voltage devices with very narrow channels—and fast speeds. Thus the bulk n^- type D/MOS will be useful as components for high-speed drive circuits for high-voltage display systems.

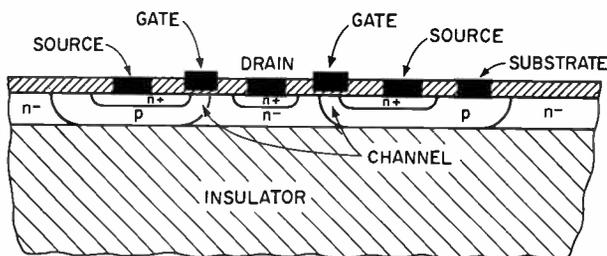
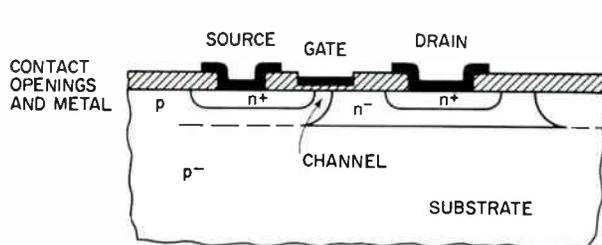
Since the threshold voltage in the D/MOS process can be controlled by the doping profile in the short channel, it is also possible to make depletion and enhancement mode devices, independent of the substrate used. Furthermore, because of the flexibility available in the starting substrate and diffusion materials, npn bipolar

transistors can be integrated on the same D/MOS wafer, thus combining the best of MOS and bipolar techniques. This goal is attractive for such high-power readout applications as LED displays, which now use discrete bipolars to drive the display.

A p^- substrate device provides device isolation, and therefore would be the best choice for digital ICs. In addition to the D/MOS enhancement mode device, conventional depletion devices are readily available for loads in this configuration, leading to even faster logic circuits than enhancement-mode devices yield. In addition, if the p^- substrate is depleted, low feedback and high voltage capabilities are readily available.

A D/MOS-on-SOI configuration is shown in the figure (right). In addition to the high-voltage and fast-switching capabilities that are available with basic n^- configuration, SOI/D/MOS devices keep parasitic substrate capacitance to a minimum, leading to still faster circuits. The insulating substrate also provides bulk resistors for logic applications; high-frequency isolation between components can be achieved readily.

Many different types of epitaxial substrate devices (left figure) are available with D/MOS processing. For example, if n^- epitaxial on p^- substrate is used, the device automatically has isolated drains. Moreover, epitaxial devices provide a means of grounding the channel region via the p^- substrate.



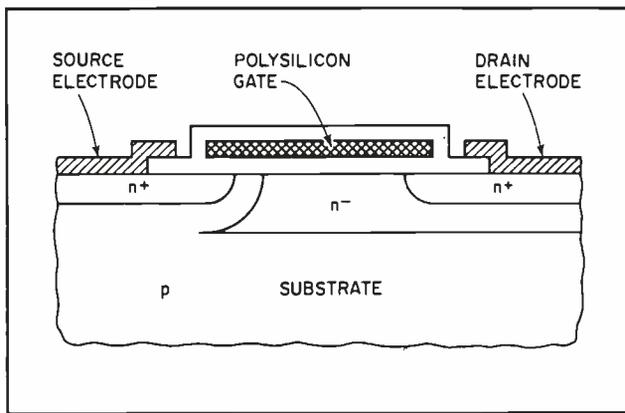
25 than conventional n-channel MOS. The parasitic capacitances (Miller capacitances), which are caused by the gate's overlapping of the source and drain diffusion regions, are also kept small since the overlapping could occur on only one end of a channel by the D/MOS process.

A second consideration is the modulation of the channel by drain voltage when $V_D > V_{Dsat}$. In conventional MOS devices, this leads to undesired feedback, lowering of the output impedance, and hence reduced power gain. In the D/MOS the drain voltage lies mostly across the low doped drain region, and a change in V_D will have little effect on the channel.

Breakdown voltage with D/MOS also can be made higher. In an ordinary, $5\text{-}\mu$ channel length device, punch-through from drain to source occurs at relatively low drain voltages, which limits drain-to-source breakdown voltage. But in the D/MOS device, the breakdown voltage can be designed independently of a short channel, not being limited by channel di-

mensions or doping level. To refer back to Fig. 3(b), the D/MOS drift region is made of a low doped portion, which can accommodate the depletion region associated with the drain-to-channel voltage. The doping concentration in this part of the device is at least an order of magnitude less than that in the channel, and therefore absorbs most of the voltage drop across the device. Thus, by extending the gate electrode towards the n^+ drain contact region over the gate oxide, it can be made to act as a field plate for high-voltage operation. This technique results in devices whose channel length, L , is $1.8\ \mu$ and whose maximum drain breakdown voltage is 600 V. Under normal operating conditions, with $V_D > V_{Dsat}$, the low doped region is fully depleted and consequently the gate-to-drain capacitance, C_{GD} , is very small.

A fourth advantage of the process is that, depending on the peak channel concentration and the fixed charges between channel and gate metal, the threshold voltage of the device can be negative (depletion type)



6. Self-alignment. Silicon gates are useful for D/MOS fabrication to provide self-alignment of gate as well as threshold adjustment. Note that the self-alignment feature is needed only on the source side.

or positive (enhancement type). Low peak channel doping in a short channel results in fast depletion type devices, suitable for linear high-frequency amplifier applications; a gate bias of a few volts yields stable operation, and the short channel (1μ or less) produces a high gain-bandwidth product. Higher peak channel dopings and channel lengths of 1 to 2μ produce enhancement type devices for switching applications, where zero gate voltage turns the channel off. Moreover, a few volts above threshold applied to the gate give this enhancement type device the full current driving capability predicted by theory. This is shown in Fig. 4, where for typical devices the ratio g_m/Z is plotted as a function of gate voltage, V_{GS} ; with V_{GS} above about 4 volts, g_m is a maximum. In addition, the drift region separates the channel from the drain and gives high output impedance and low feedback.

One problem common to all MOS devices, D/MOS types included, is the "source-bias effect," which occurs in single polarity (in contrast to complementary) logic ICs. When the source of an MOS device is at a potential different from the channel region—for example, in a load or a transmission gate—the subsequent change in threshold voltage can result in circuit malfunction. For a discrete microwave device, however, this restriction is lifted entirely, since source-to-substrate voltage is zero or fixed and source-bias effects are eliminated.

Microwave applications hold the most immediate promise for the D/MOS process. In fact, the s-parameters of D/MOS transistors closely match those of microwave bipolar transistors. The figures for power gain and stability factor (k) at microwave frequency that are shown in Fig. 5 represent a significant breakthrough in microwave device technology. The present status of the D/MOS device can be seen from the table, which compares the best microwave devices that have been reported in the literature and shows that only the D/MOS device has achieved microwave performance with relatively wide stripe widths, easily fabricated with conventional masks.

A small-signal equivalent circuit, derived from the

State-of-the-art microwave transistors

Device	f_{max}	Minimum stripe width
GaAs MESFET	30 GHz	1μ
Ge bipolar	17 GHz	1μ
Si bipolar	15 GHz	1μ
Si ion-implanted MOS	14 GHz	1μ
Si MESFET	12 GHz	1μ
Si D/MOS	10 GHz	8μ
Si JFET	1.5 GHz	$\approx 5\mu$
Si conventional MOS	1.3 GHz	$\approx 5\mu$

measured s-parameters, shows that the operation of the device is similar to that of a microwave Schottky-barrier field effect transistor (MESFET), except that a time delay term has been added to take into account the extra phase delay caused by the channel drift region. But this delay might not reduce the gain, since the carriers are not modulated in the drift region. However, the input parasitic gate-to-source capacitance does lower the frequency response by requiring an additional charging time, which delays the modulation of carriers in the active channel region. Further reduction of this parasitic capacitance will improve the gain at microwave frequencies. The best noise figure measurements give 45 dB at 1 GHz, although the devices that were tested had not been optimized for low noise.

It should be pointed out that for discrete microwave applications, the D/MOS device has at least two advantages over bipolars. Since its transconductance remains high and constant at large drain currents, it has a wide dynamic range of linear amplification, and will give linear gain with large output power. Then, too, it has a low cross-modulation distortion, which is not achievable with bipolar transistors, and can be used in both mixer and automatic gain control applications. Laboratory D/MOS amplifiers have been built with single-stage, narrowband gain of 15 dB at 1 GHz and broadband gain of 7 dB over the frequency band 0.5 to 1 GHz.

Besides discrete microwave applications, the D/MOS process is attractive for switching applications. For example, in a simple inverter stage with resistive loads, a typical device has exhibited a rise time as short as 210 ps and a delay time as low as 430 ps with 10-V supply voltages; at half those voltages rise time and delay time increased only 25%. Comparable switching performance has been achieved with both enhancement and depletion type D/MOS devices. Significantly, conventional n-channel depletion type MOS devices, operating in the same inverter stage, showed rise times approximately 10 times as long and delay times twice as long. □

Expand your Measurement Horizon

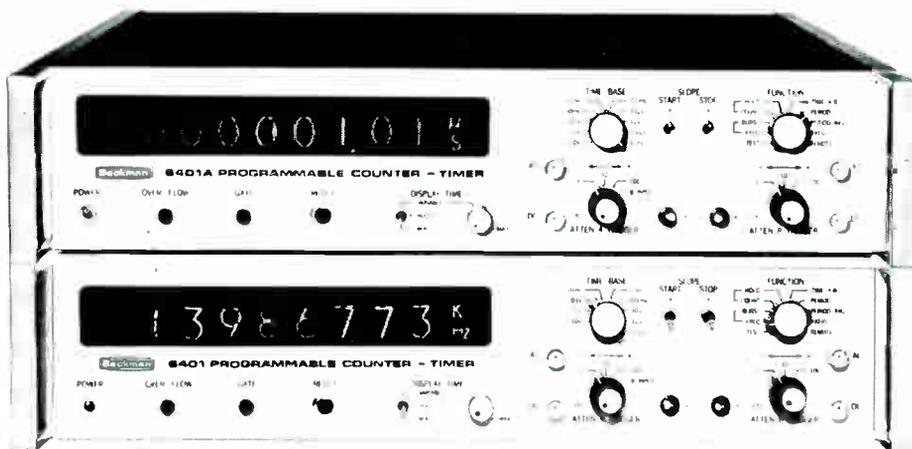
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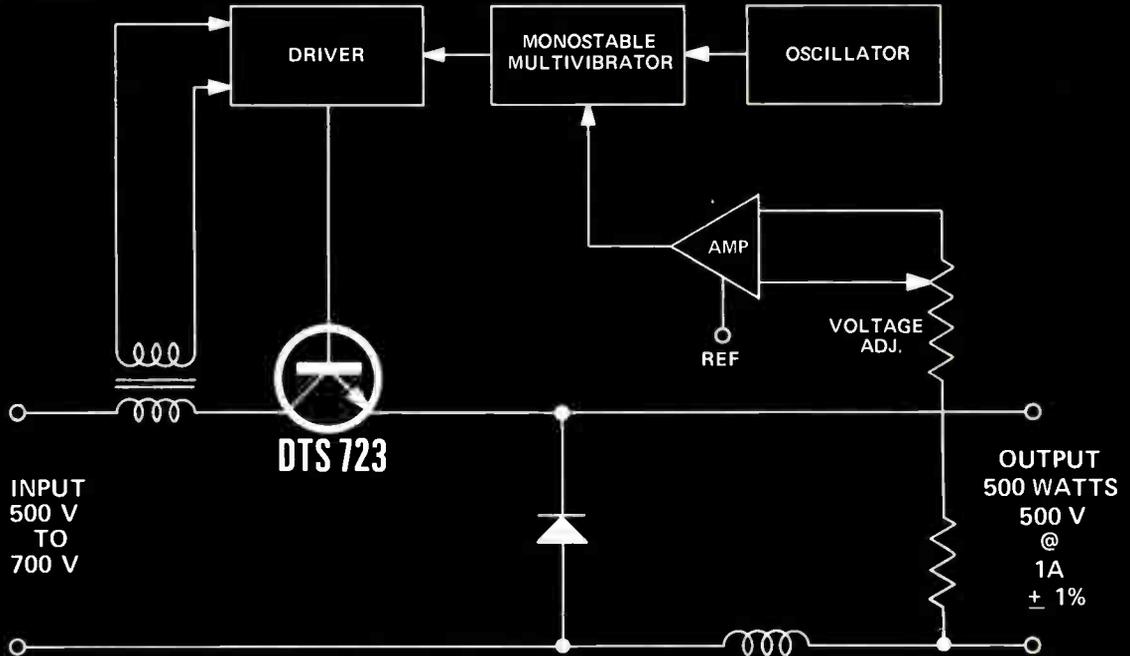
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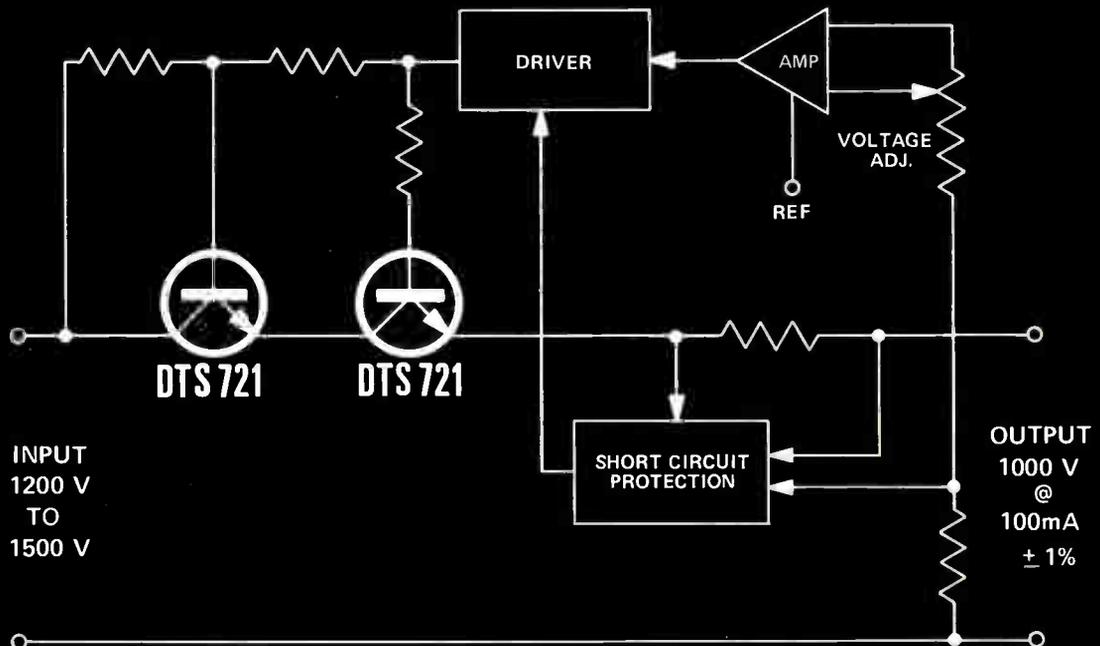
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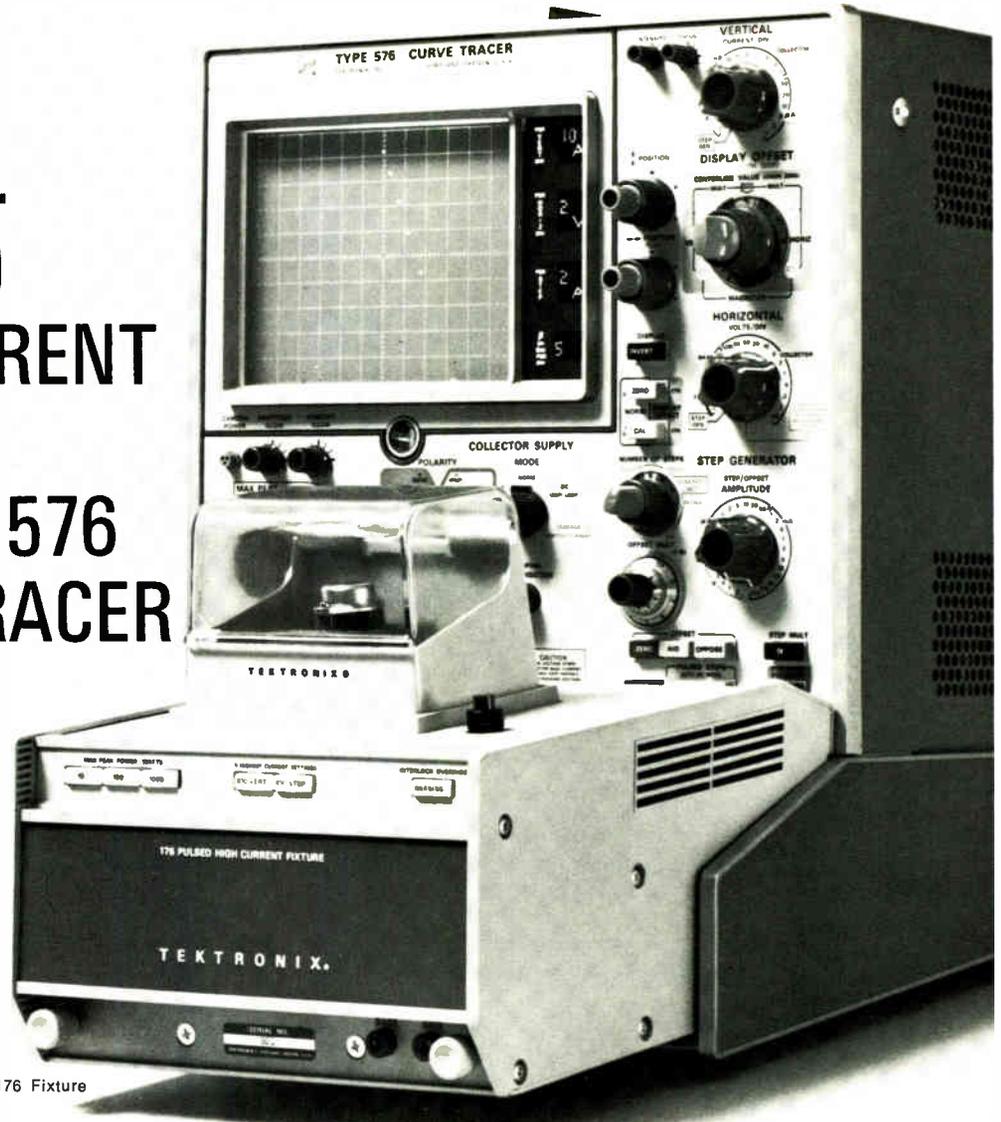
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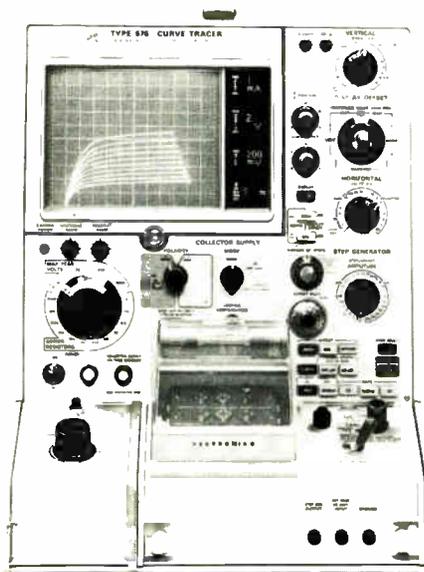
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□ President Richard Nixon's fiscal 1972 budget demonstrates to most Capital politicians and economists that Republican Richard Nixon already is running for reelection—and running scared. And the Democratic 92nd Congress already is making sounds that suggest it will respond in kind to the President's proposed \$229.3 billion budget that will generate an \$11.6 billion deficit.

For a lean and hungry electronics industry, the prospect of making Federal spending a do-or-die political battleground is disconcerting. Federal budgets are essentially political documents, of course, but the infighting between the White House and Congress is expected to be especially sharp this year. Though increased outlays for defense electronics research and development deferred by Vietnam war costs probably will suffer least in Congress, escalated new program procurements will be sharply challenged.

Many managers in electronics companies, politics aside, also are suspicious of the Nixon budget premise that the Federal deficit can be held to \$11.6 billion. Virtually no one buys the Nixon projection that revenues will expand by 9% to \$217.6 billion to meet that goal.

But the budget *per se* does provide industry with a base from which to forecast Federal programs. "It's the first move in a political chess game," says one industry vice president who tracks the moves of Government, the industry's best customer. "Defense dollars will go up—maybe not as

much as Nixon wants, but enough to put more people back to work on research in the Northeast and crank up enough procurement to save California's primes from bankruptcy. And we figure that enough of the programs are sufficiently new and big to gin up some pretty good competition again."

That analysis matches those of other industry sources in the Capital, who also agree that Nixon's \$16.1 billion revenue sharing with cities and states is unlikely to meet much success in Congress but nonetheless should be hedged against. Hedging will require increased corporate efforts to track local efforts on what the Administration describes as "social programs"—law enforcement, health care, education, and the environment. "More of the money for law enforcement and health will be spent locally anyway, regardless of what Congress does," says one specialist.

Space spending doesn't exactly rebound in the Nixon budget. Yet the severe annual cutbacks that began in the Johnson era appear to have stopped with the fiscal 1972 funding request. And that request—significantly increasing unmanned programs with their comparatively heavy electronics content—is expected to encounter only slight difficulty, if any, in Congress. Thus the recession appears to have achieved what the manned lunar landing could not—maintenance of NASA as a viable customer for new technology.

The Department of Transportation's potential for funding electronics firms in its air and ground

systems programs is overshadowed by the controversy surrounding the Nixon Administration's continued espousal of the supersonic transport. But whether SST lives or dies in the 92nd Congress, estimates are that air traffic control and urban mass transit systems present a combined potential that could make DOT second only to the Defense Department as the largest Federal customer for electronics. The Urban Mass Transit Administration, the Coast Guard, and even the Federal Railroad Administration are other DOT units that will provide new funds for electronics.

But ultimately, as the President proposes, so the Congress disposes, and it will surely be summer, perhaps autumn, before the House and Senate concur on significant appropriations.

And while Pentagon outlays surely will be cut below what the President has requested, a cantankerous Congress looking to November 1972 could well pre-empt the President's program to give the power back to the people by outspending him on domestic programs. Then, with everyone running scared, all economic bets would be off. □

Probing the budget

Defense	110
Space	114
Communications	117
Social programs	120
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Inflation offsets gains in procurement, R&D

The Department of Defense, the Federal Government's biggest spender, will be Richard Nixon's biggest economic gun in the battle to curb the recession in the fiscal year beginning July 1. In asking Congress to approve a \$76 billion defense budget—a \$1.5 billion increase over this fiscal year—the President expects to stem the cuts in electronics and aerospace jobs, get on with research and development programs deferred by Vietnam war costs, and modernize the armed forces, whose manpower is scheduled to be reduced.

Electronics companies are sure to get new business from the \$19.7 billion procurement request, some \$1.7 billion above this year's spending level, as well as from the \$7.8 billion research development, test, and engineering account, up \$779 million.

However, they won't necessarily be receiving more business. While Defense Secretary Melvin Laird's spending plan calls for significant starts on major new systems to provide a different mix of business, inflation means the Defense Department's new dollars will not buy much more in the new fiscal year. Nevertheless, when Laird marches on Capitol Hill to fire the opening gun in defense of this request, he

will be prepared for some sharp questions from congressmen and senators whose complaints range from a growing discontent with what they see as Administration dissembling on U.S. involvement in Indochina to more conventional criticisms of duplication and cost overruns on major weapons systems.

To counter his critics, Laird will contend that much of the new money sought already is spoken for by inflation, military and civilian pay increases already voted, plus a \$1.1 billion start on building a volunteer Army.

As for the industry side of the much-criticized military-industrial complex, Laird will note that another 120,000 jobs will disappear between the end of last year and June 30. And in the following 12 months, another 80,000 jobs will be lost before employment stabilizes at about 2,160,000 by June 30, 1972. So much for the bad news.

The good news for electronics companies is that there is fresh money for electronic communications systems, including computers, in addition to the heavy electronics funding components of aircraft, missiles, and ships [see table, below]. For example, the Worldwide Military Command and Control

System, through which the Defense Communications Agency would provide an integrated computer-communications system for major military commands, is budgeted for \$6.1 million in fiscal 1972, a nearly threefold increase from the present level. More significant, however, is that \$3.7 million of the increase comes in procurement accounts, which got only \$800,000 this fiscal year. R&D, on the other hand, is down for only a \$100,000 increase to \$1.6 million.

The overall procurement request for defense agencies—including the Defense Communications Agency, the Defense Supply Agency, and others—calls for spending \$66.5 million in the new fiscal year, a sharp increase on its \$40 million appropriation this year. And much of this goes for computers and communications hardware.

The Naval Electronic Systems Command's secret underwater surveillance system for submarines (known as Caesar) is slated for \$46.5 million for hardware in fiscal 1972, up from \$43.9 million, plus a classified amount for increased RDT&E. Expansion is believed to include a Pacific Coast acoustic detection system (called Sea Spider), equipped with hydrophones spaced along the ocean floor and linked by coaxial cable to shore-based computers. Components of the Caesar system in the Atlantic include computers from Control Data Corp., Minneapolis; sonars and hydrophones from Hazeltine Corp., Little Neck, N.Y., cable from Simplex Wire & Cable Co., Newington, N.H., and logic microcircuitry from Westinghouse Electric Corp.'s Baltimore division. The steady growth of Caesar and simi-

Department of Defense: where procurement dollars go

(millions of dollars)

	Dept. of Defense total			Army	Navy	Air Force
	FY 1970	FY 1971	FY 1972	FY 1972	FY 1972	FY 1972
Aircraft	6,364	6,180	6,401	124	3,354	2,922
Missiles	3,159	3,382	3,772	1,101	727	1,944
Ships	2,464	2,590	3,329	—	3,329	—
Combat vehicles, weapons and torpedoes	546	493	476	205	272	—
Ordnance, vehicles, and related equipment	4,146	2,856	3,226	1,821	577	825
Electronics and communications	1,140	838	795	172	354	256
Other procurement	2,041	1,634	1,721	396	729	545
Total procurement	19,860	17,974	19,720	3,819	9,342	6,493

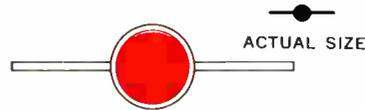
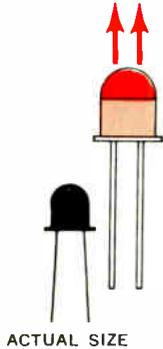
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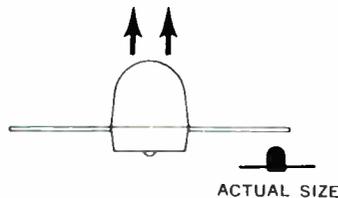


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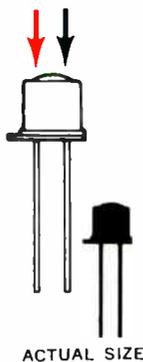
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lar antisubmarine warfare electronics sensor systems reflects the fact that the Navy—whose requirements lately have been subordinated to immediate Army and Air Force needs for Southeast Asia—will lead a new program for “modernizing our whole force structure,” says one Pentagon leader.

In addition to antisubmarine warfare, the push on other intelligence and early warning systems throughout the defense spending program is evident. For example, the Naval Air Systems Command is budgeted for its first major procurement of Grumman’s E-2C Hawkeye, the early warning and interceptor control turboprop for fleet air defense. The E-2C, an uprated

E-2A with advanced avionics and G.E./Utica’s APS-111 radar, is programmed for nearly \$274 million in procurement and \$40 million for RDT&E. The figures for this year are \$43 million and \$58.4 million, respectively, using reprogrammed funds after Congress struck a \$92.3 million request from the fiscal 1971 budget.

And while Navair is proposing these gains, the Naval Electronics Systems Command is requesting \$1 million more to raise its research effort on the controversial extra-low frequency communications program (Project Sanguine) to \$5.6 million.

On and under the ocean is where the Navy will pick up much of its \$1.8 billion increase for fiscal 1972. The Navy is seeking seven more DD-963 destroyers, five more SSN-

688 high-speed attack submarines, conversion of six Poseidon missile boats, and a doubling of R&D money for the big new craft envisioned for the Undersea Long-Range Missile System. It’s also said to have a significant increase in classified money for the SSN Conform, an antisubmarine warfare concept combining the SSN 688’s high-speed and deep-diving abilities with the SSN 685’s quiet, nuclear-powered turbine electric drive system. General Dynamics’ Electric Boat division, Groton, Conn., is the prime beneficiary of all these submarine programs. Significant fallout in money is expected for advanced electronics needed in sonars, radars, and electronic countermeasures. Some electronics also will be required for weapons such as the Westinghouse Mark 48 torpedo and the Naval Ordnance System Command’s UUM-44A-2 submarine rocket, which includes BQQ-2 integrated sonar by Raytheon’s Submarine Signal division, Portsmouth, R.I.

The Navy’s increase for communications and electronics procurement, including ship- and shore-based transmitters and related instruments, is pegged at \$24 million for a total of \$301 million. Aircraft support gear is scheduled to rise by \$3.5 million to \$183.8 million. This increase includes funds for the Versatile Avionics Shop Test system for aircraft carriers; PRD Electronics Inc., Westbury, N.Y., is development and production prime.

Marine Corps procurement requests are down sharply to \$157 million from this year’s \$272 million. Though the corps will be get-

Defense: major procurements

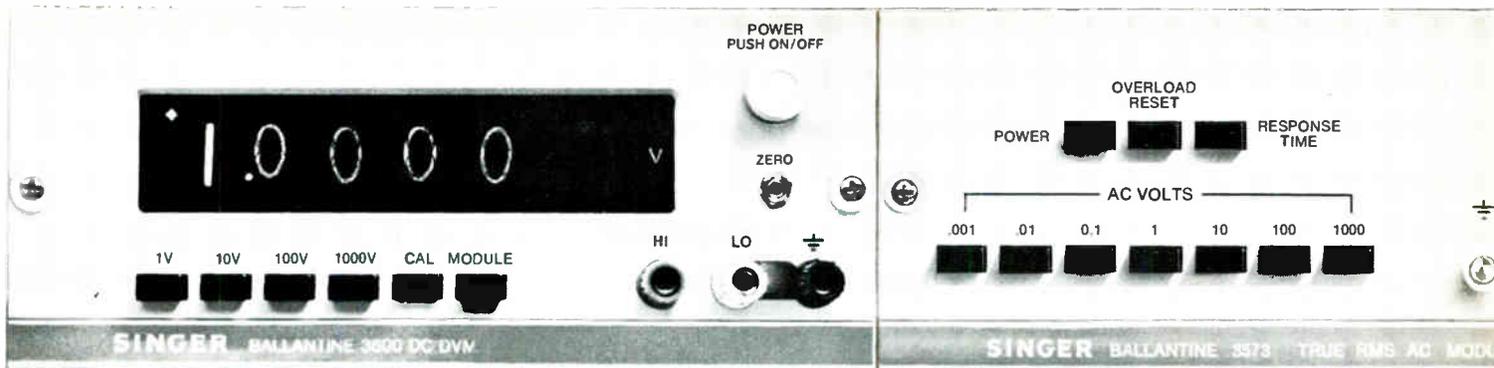
(quantity)

	FY 1970 program	FY 1971 program	FY 1972 program
Aircraft			
Army	1,005	802	400
Navy and Marine Corps	339	268	290
Air Force	552	558	188
Total aircraft	1,896	1,628	878
Helicopters	(1,247)	(1,129)	(442)
Fixed-wing aircraft	(649)	(499)	(436)
Missiles			
Army	33,079	19,076	16,033
Navy and Marine Corps	3,051	3,141	2,458
Air Force	1,600	542	3,035
Total missiles	37,730	22,759	21,526
Ships—Navy			
New construction	10	15	19
Conversions	5	10	9
Total ships	15	25	28
Tracked combat vehicles			
Army	3,754	1,800	360
Marine Corps	117	298	509
Total tracked combat vehicles	3,871	2,098	869
Torpedoes—Navy	152	211	422
Other weapons			
Army	466,622	274,039	2,480
Navy and Marine Corps	11,148	1,316	220
Air Force	1,392	—	—
Total other weapons	479,162	275,355	2,700

Where defense research dollars go

(millions of dollars)

	Dept. of Defense total			Army	Navy	Air Force
	FY 1970	FY 1971	FY 1972	FY 1972	FY 1972	FY 1972
Military sciences	509	510	541	180	143	140
Aircraft	1,641	1,643	1,988	198	638	1,152
Missiles	2,280	2,043	2,011	961	560	412
Military astronautics	638	467	499	13	49	434
Ships and small craft	305	338	490	—	490	—
Ordnance, vehicles and related equipment	332	340	351	158	98	95
Other equipment	1,188	1,176	1,390	358	269	438
Programwide management and support	558	543	567	64	161	330
Emergency fund	—	50	50	—	—	—
Total research, development, testing, and evaluation	7,451	7,109	7,888	1,932	2,407	3,002



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ting more AV-8A Harrier V/STOL aircraft, its communications and electronics and missiles budgets are off sharply to \$40 million and \$1.6 million, respectively, compared with this year's \$74.5 million and \$5 million.

Proposed procurement outlays for both the Army and Air Force are down in fiscal 1972, largely reflecting the Vietnam wind-down. Where the Navy's total buys, exclusive of ships, will rise \$720 million to \$5.5 billion, the Army and Air Force purchases will drop \$370 million and \$414 million, respectively, to \$4.7 billion and \$6.6 billion.

Indeed, the only Army procurement category to show an increase is the missile account, up some \$40 million to \$1.3 billion. This covers Safeguard ABM hardware plus continued buys of Raytheon's improved Hawk and Philco-Ford's Chaparral for air defense, the Hughes Aircraft TOW, LTV's Lance antitank systems, plus modifications to Martin Marietta's Pershing missile, managed from Orlando, Fla. Communications and electronics procurement, however, are off \$72 million to \$195 million for the new fiscal year.

Though buys for Army aircraft, largely helicopters, have been cut very sharply by the budget knife—from \$320 million currently to \$87 million—the service has tucked away \$20.5 million for its first purchase of the Utility Tactical

Transport Aircraft System, a light transport helicopter. However, this program is being funded from RDT&E accounts. Money is expected to be used for competitive prototypes, with Textron's Bell Helicopter Co., Hughes Aircraft Co., United Aircraft's Sikorsky division leading the competition. The program received only \$1 million in fiscal 1971 for studies after nearly being scrubbed by the joint-service Heavy Life Helicopter.

Every Air Force aircraft procurement account is down, even though significant R&D funds are available for support of the McDonnell Douglas Corp.'s F-15 and Northrop Corp.'s F-5E international fighter to be provided to U.S. allies [see table]. However, the F-15 surely will come under congressional scrutiny as the Armed Services Committee questions whether or not the Navy's F-14 might not do just as well for the Air Force. The service and DOD already have their own in-house analysis in progress and expect to make a strong case for the F-15. But despite strong DOD support, the F-15 still is not certain of full approval. Moreover, the new Air Force procurements still do not begin to match the phasedown of General Dynamics Corp.'s F-111 production, off \$476 million in the budget request.

On the missile side, the USAF request rises by \$320 million to \$1.77 billion, largely due to increased buys of Boeing's Minuteman 3 ICBM and its air-launched Short-Range Attack Missile. Support for

telecommunications equipment to support major USAF systems such as ground-based radars is down \$40 million to \$260 million, marking the third consecutive drop in that budget.

The boost in the RDT&E request is well distributed throughout the Directorate of Defense Research and Engineering, Army, Navy, and Air Force, even though DDR&E staffers suggest it is not as much as their director, Dr. John S. Foster Jr., wanted.

The biggest incremental increase is for aircraft and related hardware, reflecting the variety of new systems entering major development—the Heavy Lift Helicopter, the USAF A-X close-support aircraft, the Navy's Lamps helicopter for destroyer antisubmarine warfare, and the Army's UTTAS. These systems add on to programs already in full-scale development, including the Navy's F-14A fighter/interceptor, its F-14B growth version, the S-3A antisubmarine warfare carrier plane, the USAF F-15, plus the B-1 advanced strategic bomber. An unspecified classified sum also is included for further exploration of remotely piloted interceptor aircraft.

Missile R&D money rises \$45 million in the DOD budget to \$2.06 billion, with the Navy's Ulms follow-on for Poseidon submarines, and its Harpoon antiship and Agile air-to-air missile leading the way. Army missile R&D money goes largely for the Safeguard ABM, of course, as well as the SAM-D re-

Holding the line on the NASA budget is particularly significant to the space electronics industry, since the Apollo program will continue to wind down; it will cost \$302 million less next year. Making up for this decline is a 35% increase requested for unmanned programs—a \$750 million total that will enable NASA to get going on several major missions, including some new starts. The White House has given NASA the go-ahead for its Grand Tour of the outer planets, its stalled Viking Mars missions, and the High Energy Astronomical Observatory series.

This relatively favorable outlook didn't come cheap, though. NASA

Space

Unmanned starts will counter shuttle cuts

Battered by declining interest in space exploration and demands for reordering of national priorities, NASA nevertheless has won one of its toughest battles in the fiscal 1972 budget. After five consecutive years of sharp budgetary cutbacks,

NASA has finally held its ground at \$3.27 billion for the upcoming fiscal year—a decrease of only \$27 million from fiscal 1971—despite early attempts by White House aides to cut the space agency's budget by as much as \$500 million.

Key defense program budgets

(millions of dollars)

Maker, model, and mission	FY 1972	Change from FY 1971
Aircraft		
Lockheed/Navy S-3A carrier-based ASW	582	+294
Lockheed/Navy P-3C land-based ASW	318	+152
North American/USAF B-1 advanced strategic bomber	370	+295
Grumman/Navy F-14 carrier-based fighter	935	0
McDonnell Douglas/USAF F-15 fighter	414	+ 67
Hawker Siddeley USMC AV-8A strike fighter, V/STOL	95	+ 31
McDonnell Douglas/Navy, USAF F-4 fighter/interceptor	934	- 2
Procurement (includes \$78 for USAF, up \$54)	806	+148
RDT&E	128	-146
LTV/Navy A-7 light attack	78	- 30
LTV/USAF A-7 close air support	205	- 38
Northrop/USAF F-5E light air defense	70	+ 61
USAF/AX close air support*	47	+ 19
General Dynamics/USAF F-111 interceptor	190	-476
Lockheed/Army AH-56 attack helicopter (R&D)	13	- 4
Navy/Lamps helicopter, destroyer-borne ASW	39	+35.4
USAF/AWACS (airborne warning & control)	145	+ 58
Grumman/Navy E-2C	305	+203
Army UTTAS helicopter (utility tactical transport)	21	+ 20
Missiles		
Boeing-TRW/USAF Minuteman 3 intercontinental nuclear	926	+206
Boeing/USAF SRAM air-launched, short-range nuclear	237	+ 69
LTV/Army Lance battlefield support	112	+ 28
Army Missile Command/Dragon, anti-tank	39	+ 22
Hughes/USAF Maverick, air-to-ground	87	+ 56
AT&T/Army Safeguard, continental missile defense	1,278	- 53
Raytheon-Martin Marietta/Army SAM-D, surface-to-air	116	+ 33
RCA/Navy Aegis, fleet air defense	100	+ 28
General Dynamics/Navy Standard, fleet air defense	63	+ 14
General Dynamics/Navy Standard ARM, air-ground anti-radar	0.1	+ 2.3
Raytheon/Navy-USAF Sparrow 3, air-to-air, ship-to-air	72	+ 47
Ships		
ULMS (undersea long-range missile system)	110	+ 65
Poseidon (six submarine conversions from Polaris)	409	+ 27
General Dynamics/SSN 688, high-speed attack (5 starts)	881	+219
General Dynamics/SSN Conform, high-speed, quiet sub	**	**
Litton/DD-963, high-speed destroyers (7 new starts)	599	+118

*Northrop, Fairchild Hiller building competing prototypes
**Classified

placement for the Hawk in Air Defense. Being phased down and likely to be cancelled is the General Dynamics' Pomona Calif., division's Standard ARM missile. Planned for air-to-surface destruction of missile-site radars. Standard ARM got \$2.4 million in R&D money in fiscal 1971 and was touted in

some circles as ready to move into production at an estimated budget of \$400 million to \$500 million. Defense Department sources say there's no standard ARM R&D money in the new budget and only \$100,000 for procurement—just about enough to cover termination costs. □

NASA research and development

(thousands of dollars)

	FY 1970	FY 1971	FY 1972
Manned space flight			
Apollo	1,684,367	914,400	612,200
Space flight operations	343,100	515,200	672,775
Advanced missions	2,500	1,500	1,500
Space science and applications			
Physics and astronomy	112,851	116,000	110,300
Lunar and planetary exploration	150,900	144,900	311,500
Space applications	128,304	167,000	182,500
Launch vehicle procurement	107,819	124,900	146,100
Advanced research and technology			
Aeronautical research and technology	95,685	102,000	110,000
Space research and technology	119,977	107,000	75,105
Nuclear power and propulsion	55,269	55,200	27,720
Tracking and data acquisition			
	278,000	290,000	264,000
Technology utilization			
	5,000	4,000	4,000
Total	*3,110,427	*2,555,000	2,517,300

*Includes programs not listed for which there is no funding in fiscal 1972.



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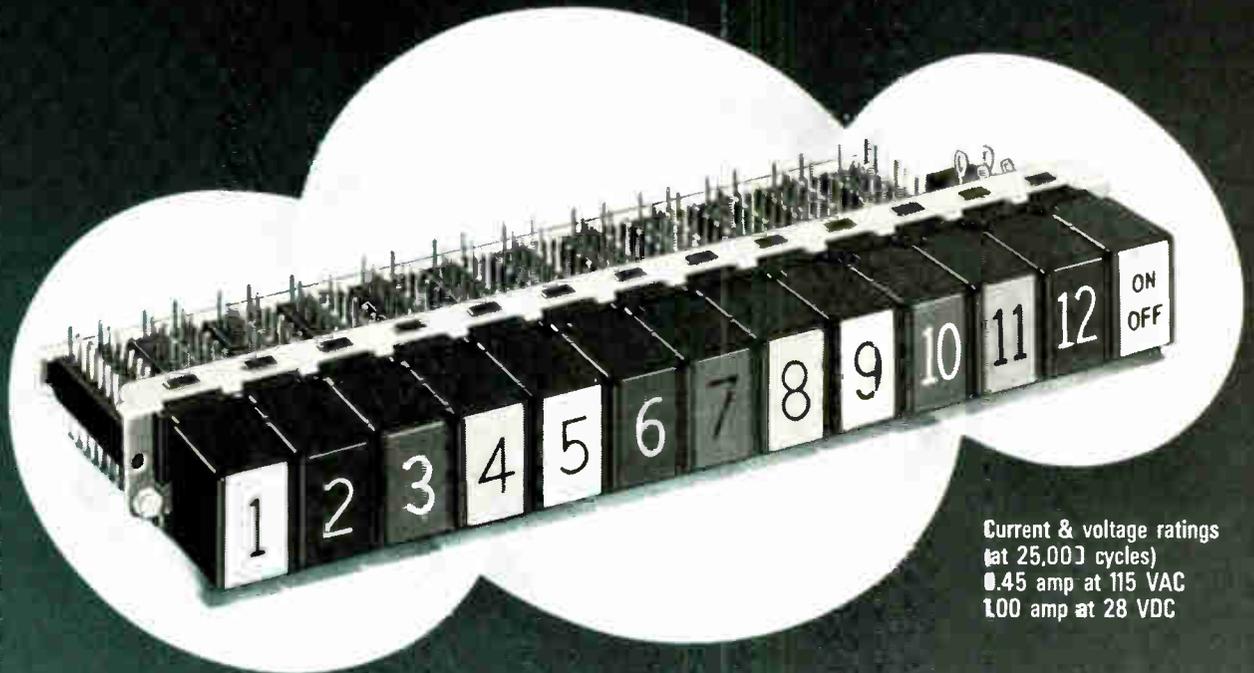
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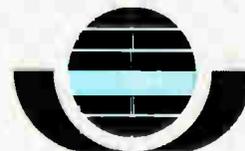
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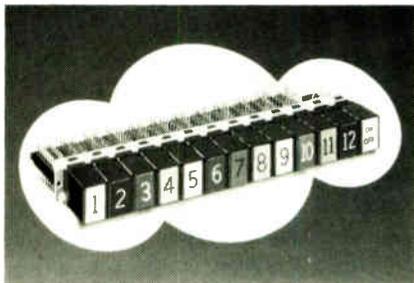
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was obliged to compromise its manned space flight program beyond the already programed cuts in Apollo lunar missions. The reusable space shuttle, successor to Apollo as the big-ticket item, got only a half start—NASA is requesting only half the money it wanted next year, which further delays the \$6-billion-plus program.

First soundings on Capitol Hill indicate the civilian space program's relatively modest funding level will move neatly through the legislative maze. Congressional observers feel the space program won't be a hot political issue this year vis-a-vis the more visible and controversial Nixon proposals on reorganization of the Executive Branch, revenue sharing with the states and welfare reforms.

The biggest increase in the unmanned program is the \$145 million more NASA will spend on the Viking Mars orbiter/lander program. Budgeted for \$180 million in fiscal 1972, Viking is divided into two parts: the lander, to be developed by Martin Marietta Corp., Denver, Colo., under a \$359 million contract, and the orbiter, slated to be built under the supervision of the Jet Propulsion Laboratory, Pasadena, Calif.

Several major contracts already have been awarded. RCA's Communications Systems division, Moorestown, N.J., will build the S-band receiver. Teledyne Inc., Los Angeles, will build the terminal descent radar for the lander, while Philco-Ford Corp., Philadelphia, will build the S-band transmitter and Texas Instruments Inc., Dallas, the telemetry set for the orbiter. To be awarded is the contract for

More in store for communications

More money for communications research and analysis is included in the fiscal 1972 budget for the Federal Communications Commission and the White House Office of Telecommunications Policy, while even larger gains are sought for what is fast becoming OTP's technical arm, the Department of Commerce's Office of Telecommunications.

The Federal Communications Commission is requesting a total of \$29.99 million, a \$3.8 million increase in its budget authority. Of the total, \$4.18 million would go towards research and planning in communications technology, a \$1.26 million gain over fiscal 1971. A good share of the sum is expected to be spent on a joint FCC-OTP study of frequency spectrum utilization [*Electronics*, Feb. 1, p. 31].

The Office of Telecommunications Policy's budget shows only a \$100,000 increase, but the figure is deceptively small when recent organizational changes are considered. By shuffling the National Electromagnetic Compatibility Analysis Center, which absorbed virtually all of the office's \$972,000 R&D budget outlays in fiscal 1971 to the Commerce Department, OTP seeks to free its \$1 million research and analysis budget for contract studies. Possible study topics include a review of interconnection standards if the FCC approves specialized common carriers, and the work on frequency utilization. The office's total request for the new fiscal year is \$2.62 million.

Doing the technical work on the frequency study for the White House group is the Department of Commerce's Office of Telecommunications, which has absorbed OTP's old role as secretariat of the Interdepartment Radio Advisory Committee, the interagency group that coordinates government frequency use. Because it is absorbing this and other functions, formerly held by the White House agency, the Commerce office is asking for \$5 million in the new year, or nearly twice the \$2.6 million approved this year.

The Commerce office is budgeted for \$1.45 million this year for its work in frequency management and usage, \$1 million more than last year. In addition, it is targeted for \$483,000 for research and analysis applied to policy formulation, \$2 million for utilization of telecommunications technology, and \$976,000 for improvement of government telecommunications systems. For fiscal 1971, the sums were \$304,000, \$1.3 million and \$533,000, respectively.

Probing the news

the lander's duplexed computers.

Peak funding for the two Vikings, scheduled to blast off in August 1975, will be reached in fiscal years 1973 and 1974. Between \$250 and \$300 million a year will be spent for the two spacecraft.

Fiscal 1972 is the make-or-break year for beginning work on a spacecraft to make the Grand Tour of the outer planets. If it didn't make it past the White House this year, the billion-dollar Grand Tour probably would have been dropped. But it's in the budget to the tune of \$30 million, enough to get rolling toward a 1976-1977 mission—either a flyby of Jupiter, Saturn, and Pluto, or a Jupiter orbiter. Two more shots are planned in 1979 to fly by Jupiter, Uranus, and Neptune.

"If we don't start now," says one top NASA official, "we'd have to scratch the 1976-77 missions." The 1979 shots still would be possible, but the shortened program would be less attractive, he adds. The agency is committed to the two 1979 missions, but has not yet decided on the 1976-77 missions; they will be two three-planet flybys, a "number of Jupiter orbiters," or a mix of the two, the official says.

No big contractor money will be let out in fiscal 1972, but "there would be an increase in the number of small contracts awarded to electronics companies," he adds.

JPL is running the Grand Tour for NASA, but one systems contractor will be selected to assume overall responsibility for the program. JPL has been working on spacecraft design for the past two years in its Thermoelectric Outer Planet Spacecraft project [*Electronics*, March 30, 1970, p. 108]; this approach, along with the self-test and repairing computer, "looks good at this point," says the NASA official.

Another big new start is the High Energy Astronomy Observatory program, whose goal is to launch two 21,000-pound spacecraft into near-earth orbit in 1975 and 1976. About \$13.5 million is budgeted for the start of the program in 1972. The spacecraft, now in

preliminary design by Grumman Aerospace Corp. and TRW Systems Group, Redondo Beach, Calif., would be used to gather data on high-energy X-rays, gamma rays, and cosmic rays. Runout cost of the program will be \$200 to \$250 million, NASA sources say.

NASA also plans to award contracts in the late spring for the \$95 million to \$120 million Mariner Venus-Mercury missions, scheduled for 1973 launches. Their scientific package will include two TV cameras, a 20-watt S-band transmitter, a 200-milliwatt X-band radio, a scanning electronic analyzer, magnetometer, ultraviolet spectrometer, infrared radiometer, and charged-particle analyzer.

The future of NASA's manned flight program hinges on the space shuttle, of course. But money for

that has slipped again. The result: no manned space flights for about five years after completion in 1974 of the Skylab program, using Apollo vehicles. And while the White House decisions to cut shuttle funding from \$190 million to \$100 million won't affect awards of engine development contracts this summer, according to Dale Myers, associate administrator for manned space flight, they will slip development of the avionics and airframe by three to four months.

The shuttle's current timetable calls for teams led by McDonnell Douglas Corp., St. Louis, and North American Rockwell Corp., Downey, Calif., to submit their preliminary designs in May. After extensive review, NASA is scheduled to award detailed design contracts in March 1972, leading to

NASA space science and applications

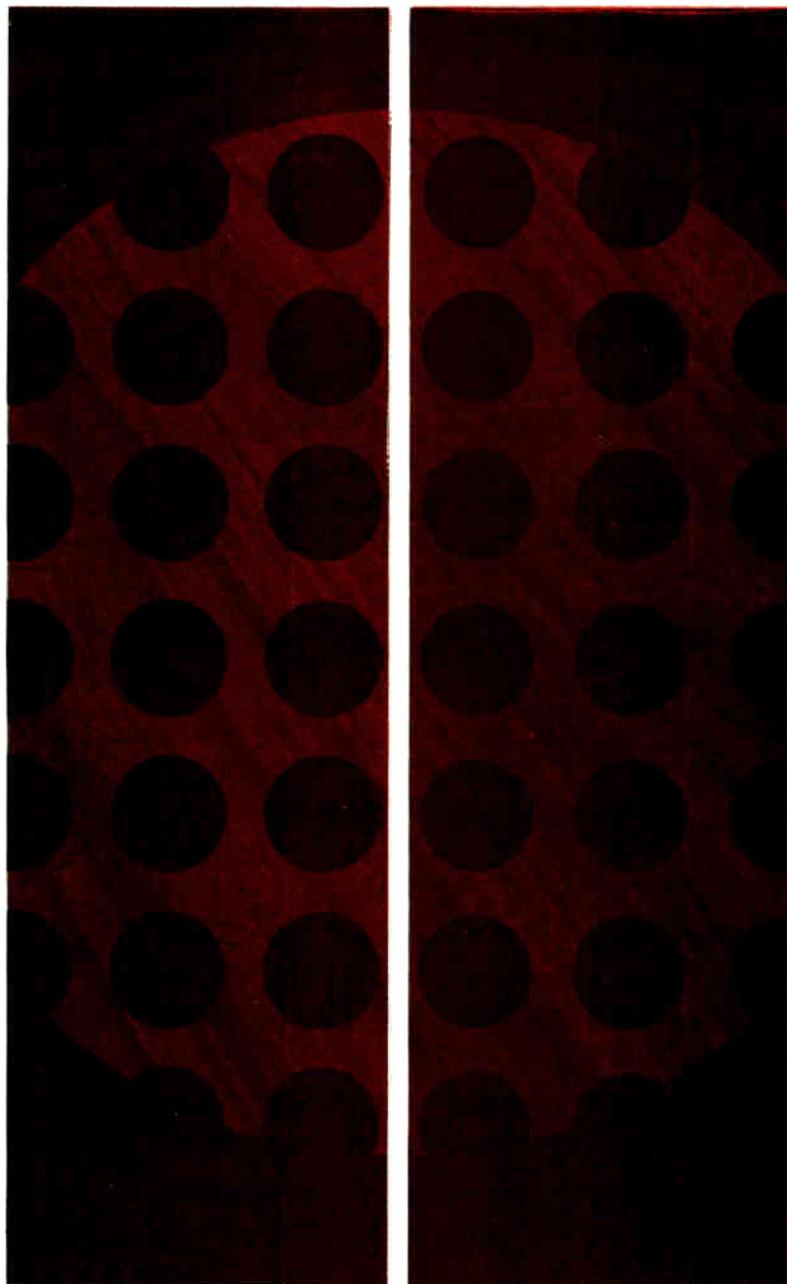
(thousands of dollars)

	FY 1970	FY 1971	FY 1972
Physics and astronomy	112,851	116,000	110,300
Solar observatory	14,515	16,431	19,000
Astronomical observatory	33,283	26,400	11,000
High energy astronomical observatory	—	—	13,400
Orbiting explorers	18,295	26,200	24,500
Sounding rockets	18,500	19,000	18,000
Airborne research	1,600	3,000	2,500
Balloon support	1,000	1,000	1,000
Supporting research and technology	16,718	16,569	15,400
Data analysis	8,940	7,400	5,000
Large space telescope study	—	—	500
Lunar and planetary exploration	150,900	144,900	311,500
Mariner-Mars 1969	3,715	500	100
Mariner-Mars 1971	59,256	31,200	14,400
Mariner-Venus/Mercury 1973	900	14,700	38,300
Viking	40,000	35,000	180,400
Outer planet missions	—	—	30,000
Pioneer	22,270	35,500	17,600
Helios	300	1,900	2,500
Supporting research and technology	—	—	—
advanced studies	18,080	17,800	18,800
Planetary astronomy	3,800	4,800	4,800
Data analysis	2,579	3,500	2,400
Planetary quarantine	—	—	2,200
Space applications	128,304	167,000	182,500
Earth resources survey	26,000	59,950	48,500
Earth Research Technology Satellite (A and B)	(15,000)	(48,950)	(37,500)
Aircraft program	(11,000)	(11,000)	(11,000)
Earth observatory satellite studies	—	—	1,000
Nimbus	27,239	25,300	23,100
Synchronous meteorological satellite	2,700	10,850	13,000
Cooperative applications satellite	83	100	2,600
Global atmospheric research program	—	1,000	2,500
Meteorological soundings	3,000	3,100	2,500
Tiros/TOS improvements	3,700	3,200	1,600
Applications technology satellite	38,965	30,300	60,300
Radio interference and propagation program	438	1,000	1,000
Geodetic satellites	1,700	1,700	1,300
Air traffic control satellite studies	—	3,000	—
Supporting research and technology	—	—	—
advanced studies	24,479	27,500	25,100
Launch vehicle procurement	107,819	124,900	146,100
Scout	13,700	14,200	16,500
Delta	32,400	34,000	37,200
Centaur	46,019	68,000	75,900
Titan	6,700	4,700	12,500
Agna	5,000	—	—
Supporting research and technology	—	—	—
advanced studies	4,000	4,000	4,000
Total	*519,529	*565,700	750,400

*Includes bioscience programs, for which there is no funding in fiscal 1972.

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initial flight tests in 1975 or 1976.

As the shuttle's development slips further into the late 1970's NASA is adding on more and more requirements. Myers says that NASA and Air Force representatives recently decided that the shuttle should include a skin-tracking radar capability and an 1,100-mile crossrange.

The shuttle's major electronic elements include an integrated data system, a microwave or laser communications link, an inertial guidance platform, and various fly-by-wire controls. Its electronic component is expected to account

for 15% to 20% of the craft's \$6-plus billion cost.

As the shuttle goes, so goes another major manned space program—the \$3 billion space station, which will be erected module by module with components carried into earth orbit by the shuttle. Myers says the 1972 budget includes \$15 million for studies on the program's data processing and research modules, which “can be assembled in erector set fashion to form large space stations.” He notes that NASA has taken a hard look at the enormous data processing and data transmission requirement once specified for the station. “We're getting a lot more realistic about the data require-

ments,” he says. This fiscal year system specs will be decided and design bids may go out.

Included in the aeronautics section of NASA's budget is \$15 million for a new program start—the development of a short take-off and landing aircraft. Flight tests should begin around 1975 to 1977.

To make sure that avionics are ready for the craft when it takes its maiden flight, NASA's Office of Applied Research and Technology “is congealing its talent and avionics hardware” in its newly formed Aeronautical Operating Systems division, a NASA source says. An additional \$2.5 million will be requested for STOL avionics to be performed by the unit. □

Social programs

Pickings are slim in 'human resources'

The President's fiscal 1972 budget envisions spending more money on “human resources” than on defense, but new opportunities for electronics firms are hard to find in the Administration's plans for social programs. Nonetheless, Federal outlays for law enforcement, health care, and pollution control in fiscal 1972 will provide a small but respectable market for electronics companies.

Perhaps the greatest potential for new electronics systems and hardware is the budget request for the Justice Department's fledgling Law Enforcement Assistance Administration: its 1972 budget request of \$698.4 million is up one-third over fiscal 1971. More than two-thirds of the total is slated for direct transfer to states and localities through grants to improve and strengthen law enforcement agencies. And a portion of these grants will be spent on high-electronics-content items like police communications systems and computerized information networks.

Also of significance to electron-

ics firms is an almost threefold increase in the 1972 research budget. It calls for the National Institute of Law Enforcement and Criminal Justice to be funded at \$21 million so that research can continue on such projects as remote detection of bombs and weapons; remote research surveillance sensors; automation of crime laboratories; night vision gear; voiceprint equipment; and evaluation of helicopters and short-takeoff-and-landing aircraft for police operations.

The largest single source for Federal medical electronics money is the Health Services and Mental Health Administration of the Department of Health, Education and Welfare. This year's \$139 million request for medical facilities construction is expected to generate from \$60 to \$75 million in new electronics purchases.

The National Heart and Lung Institute, with perhaps the heaviest budget for electronic equipment in HEW's National Institutes of Health, expects to continue spending about \$12.3 million on

electronics, despite an estimated \$7 million increase in overall outlays to \$184 million.

In the HEW Office of Education budget request, outlays for education for the handicapped, which have some electronics content, are expected to increase \$13 million to a proposed 1972 level of \$103 million in a total education budget of \$4.7 billion. Money for educational broadcast facilities in the new budget was cut to the pre-1970 level of \$4 million, after last year's dramatic increase to accommodate the backlog of applications.

The Food and Drug Administration's fiscal 1972 budget requests are up \$15.6 million to \$98.1 million. Of possible interest to electronics firms is the \$4 million slated to establish a National Center for Toxicological Research at the Pine Bluffs Arsenal, Arkansas. There is also new money in the President's budget to “develop an initial testing and monitoring program to determine the safety and efficiency of medical devices.”

In other departments, Interior's Bureau of Mines is budgeted for an increase in coal mine health and safety obligations of \$6.5 million, raising the program request to \$80.3 million. Research will be stepped up this year, and more money will be spent on equipment for measuring noxious gases in coal mines.

Interior's Geological Survey more than doubled its requests for

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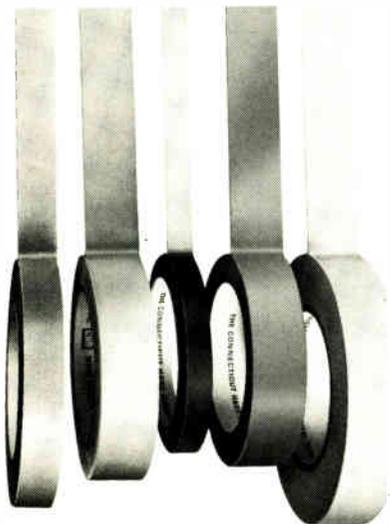
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the Earth Resources Observation Systems program. The \$5.2 million effort would continue research into remote sensing of mineral resources and the application of data derived from satellite and aircraft observation. Budget emphasis this year is on use of data from NASA's first Earth Resources Technology Satellite (ERTS-A), built by General Electric Co., New York, and scheduled for an early 1972 launch, as well as continued development of the EROS data center in Sioux Falls, S.D.

The Commerce Department's newly formed National Oceanic and Atmospheric Administration shows a budget boost for environmental prediction and satellite

operations. The agency can be expected to spend some of its \$6 million environmental prediction increase on remote sensing meteorological equipment. Outlays for satellite operations under the new budget also would increase by \$6 million to a \$29 million total.

And in its budget request for the data buoy system, the agency is asking for \$1 million more than the \$13 million the Coast Guard received for the project last year. Although the prototype network for collecting oceanographic and marine meteorological data is still in the concept formulation stage, officials say that the two prime contracts for state-of-the-art hardware will be awarded sometime in March. At current funding rates, the prototype will reach the hardware stage by fiscal 1976. □

Transportation

FAA, urban agency will be big spenders

In a word association game, an engineer likely would respond to "Department of Transportation" with "supersonic transport," for the controversial SST indeed is DOT's most visible technological effort. But the SST overshadows the growing national concern with congested highways and airways that is pushing the transportation agency's growth curve higher and higher. In fact, DOT one day could be right behind the Defense Department as the largest Government customer for electronic gear.

Though the SST is slated for \$235 million in President Nixon's fiscal 1972 budget request, the outlook for the Boeing Co. program is not bright. Since the Senate failed to enact the fiscal 1971 request for \$290 million, the program has been operating with interim funds.

Prospects are brighter for DOT's Federal Aviation Administration, with its air traffic control programs and their associated hardware. The

new budget asks \$322.8 million for air traffic control system improvements and related research and development, an increase of \$15.8 million from the current budget.

The bulk of the fiscal 1972 money is expected to go into radar and automation equipment for en-route air traffic control centers, which are budgeted for \$162.1 million, up sharply from the current \$115.8 million. Similar equipment for terminal centers is programmed for \$75 million—\$1 million below this year's outlay. Another \$29.5 million is set aside for instrument landing systems and radio ranging equipment, an increase of \$3 million.

However, the R&D outlook at FAA isn't as bright. Questions by White House budget aides about the agency's ability to spend large sums of R&D money efficiently have held the budget allotment down to \$72.4 million—barely \$3 million more than fiscal 1971 and far less than FAA's \$150 million request.

Under the FAA's research budget, \$68.6 million would go toward refining terminal and en-route traffic control systems; \$2.5 million would be used to improve radio ranging aids and to develop a microwave instrument landing system.

The situation at the Urban Mass Transportation Administration is exactly opposite that of the FAA. The urban transportation agency spends the bulk of its grant money on such conventional systems as trains and buses, both with a small electronics component. It plans to spend \$600 million here, \$200 million more than in fiscal 1971.

On the other hand, the budget request for the agency's R&D office is \$75 million, nearly twice last year's \$40 million. The bulk of it will go for development of transportation systems to serve downtown cores of cities.

Although the Coast Guard has lost its National Data Buoy program to the National Oceanic and Atmospheric Administration [see social programs, p. 120], the Coast Guard R&D budget nevertheless shows an increase. But the \$8 million increase in budget authority to \$17.5 million is for growing costs of ongoing programs.

These programs include development of an air-dropped ice penetrometer that will gauge ice density and transmit data to an aircraft, and of a side-looking airborne radar for detecting ice masses.

The most significant new start in the Coast Guard's R&D program is development of a second-generation harbor advisory radar.

Another Department of Transportation agency with a bulge in fiscal 1972 R&D spending is the Federal Railroad Administration. Under the category of high-speed ground transportation research and development, this agency is requesting \$11 million more for a total of \$29 million in new budget authority. Most of this will be used to develop a high-speed ground effect system using linear induction motors, and for new propulsion and command and control subsystems for high-speed rail networks.

This special report was written by *Electronics'* Washington bureau: Ray Connolly, manager, Larry Armstrong, and Jim Hardcastle. Additional reporting came from Howard Wolff and William Buccì.



Since Washington State is a known source for much of the advanced systems design, engineering and fabrication required by business and government, you can see that the electronics industry is already very much at home here. One important reason for that is the skilled labor pool (25% more productive than the national average) produced by Washington's superior and complete educational system . . . people whose abilities you can put to work now if you locate your new plant or expand facilities in the Evergreen State. Here are a few more good reasons:

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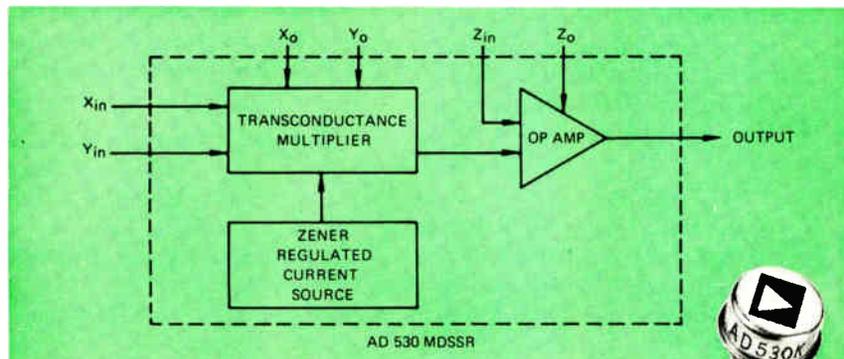
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SCALE FACTOR VS. SUPPLY VOLTAGE	2%/V
OFFSET VOLTAGE VS. TEMPERATURE	0.2 mV/ $^{\circ}C$
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Tektronix adds 50-MHz scope to 7000 series

by Owen Doyle, Instrumentation editor

Rack-mountable mainframe with vertical, horizontal plug-ins sells for \$2,200; unit has large display area

In the evolution of its 7000 series oscilloscopes, Tektronix Inc. reversed the usual procedure of starting with a simple and inexpensive unit and then adding capabilities. In fact, the initial scope was a 150-megahertz unit, priced at \$4,000 and up, and boasting a multitude of capabilities. Periodically since then, the company has been introducing simpler, less-expensive additions [see panel, p. 127].

The newest of these probably will be the most popular because it's aimed at the biggest cross-section of the laboratory-scope market—50-MHz measurements. Designated the 7403N, it's a 50-MHz mainframe that can take up to three plug-ins. Tek expects the new model will gradually replace the 540 series. With the 7403N, Tek is emphasizing cost—only \$2,200. The 7403N "lets someone who doesn't have the higher frequency requirement go with an instrument that has full compatibility with the rest of the line, but make an investment that is still quite modest," says Robert LeBrun, marketing product manager for the 7000 series.

LeBrun points out that the 50-MHz region is the "breadbasket" of the scope market, and notes that applications at that frequency are myriad. He feels that the new unit will be particularly well received

in test systems because of its large display area.

The package comprises the mainframe (\$950), a dual-trace vertical amplifier (the 7A18, \$500), and a dual time base (the 7B53N, \$750). The cathode ray tube is large for a 50-MHz scope: the diagonal dimension is 6½ inches, allowing a display area of eight divisions by 10 divisions (1.22 centimeters per division).

The mainframe weighs only 30 pounds and is available for rack mounting. Like other 7000 scopes, the 7403N has pushbutton control, and offers front-panel switching between vertical plug-ins.

Tek engineers designed the 7A18 and the 7B53N plug-ins specifically for the new mainframe. With the 7A18 vertical amplifier, the scope has a sensitivity range of 5 millivolts to 5 volts/division.

The 7B53N dual time base has

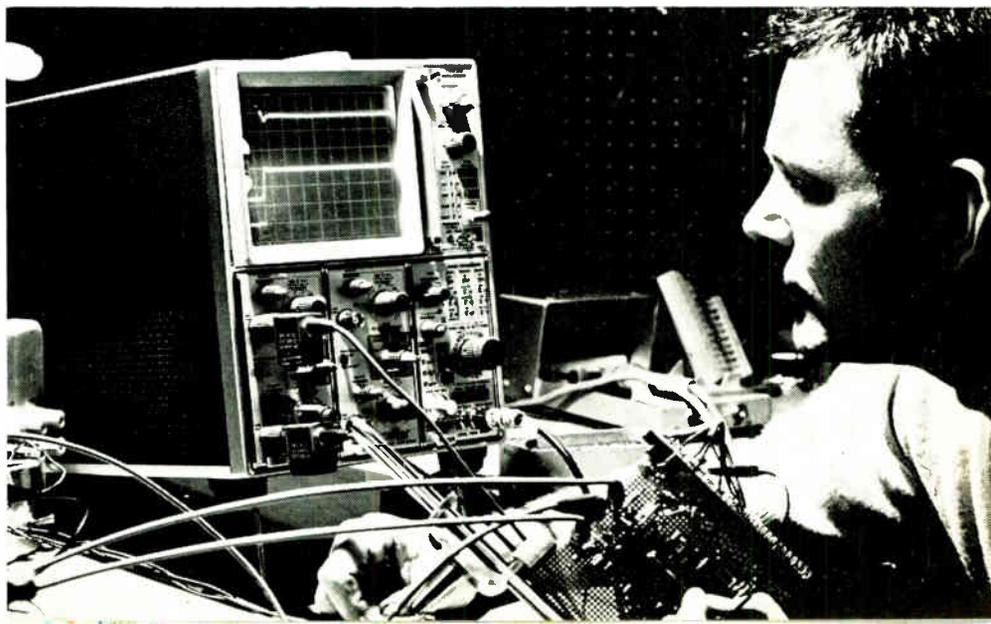
sweep speeds from 5 seconds/division to 50 nanoseconds/division, along with 10-power magnification for 5 ns/division. Triggering can be achieved to 100 MHz.

Applications will hinge on the user's choice of plug-ins. With a few exceptions, all the 7000 series plug-ins work in the 7403N. These include a differential comparator (7A13), a vertical amplifier with 10-microvolt sensitivity (7A22), and a current probe (7A14).

The new mainframe won't take the 7D13 multimeter and 7D14 counter [*Electronics*, Aug. 3, 1970, p. 101]. They're excluded because the mainframe's CRT can't be fitted to generate alphanumeric characters, as do other 7000 tubes.

This feature was left off to keep the price down, explains LeBrun. "While the character readout is an option [on the other 7000 scopes], electronics were put into the main-

Big picture. The 7403N has 8-by-10-division display (1.22 cm/div.). With new plug-ins sensitivity is 5 mV/div.; sweep goes to 50ns/div.



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Tom Hilb, President of Aspen Skiwear, Inc. and his two children.



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frame so that it would accept the board that has the actual circuitry," he says. "Now most of the price of the readout is on the board, but there are some dollars in the mainframe. For this package, we chose to leave character generation out, so those dollars aren't needed."

LeBrun notes that a user can even trim the price below the \$2,200 mark with the right choice of plug-ins. If he can get by with a single trace and no sweep delay, the user can pick the 7A15 vertical amplifier, which costs half as much as the \$500 7A18, and the 7A50, which is \$300 less than the \$750 7B53N. "You're still into a 50-MHz instrument that has full plug-in compatibility, and you're into it for well under \$2,000 (i.e. \$1,650)," says LeBrun.

He also notes that the mainframe offers an inexpensive way to obtain a sampling oscilloscope. All the 1100 sampling plug-ins fit the new mainframe, so it's possible to display repetitive signals that have frequencies as high as 14 gigahertz.

The new scope will debut at the IEEE Show. Delivery time for the first units off the production line will be approximately two months.

Tektronix Inc., P.O. Box 500, Beaverton, Ore. 97005 [338]

The 7000 family in profile

Introduced at Wescon in 1969 [*Electronics*, Aug. 4, 1969, p. 163], Tektronix Inc.'s 7000 series is the company's high-performance oscilloscope line.

The first 7000 was the 7704—a 150-megahertz machine that bristles with unusual features such as push-button controls, fiber-optic display, and alphanumeric character generation on the cathode ray tube.

The 7000 family now has three basic members: the 7704, which typically sells for \$4,600 (for a mainframe, dual-trace vertical plug-in, and delayed-sweep horizontal plug-in); the 90-MHz 7503 and 7504, which typically go for \$3,300 and \$3,500 respectively; and the new 50-MHz 7403N for \$2,200.

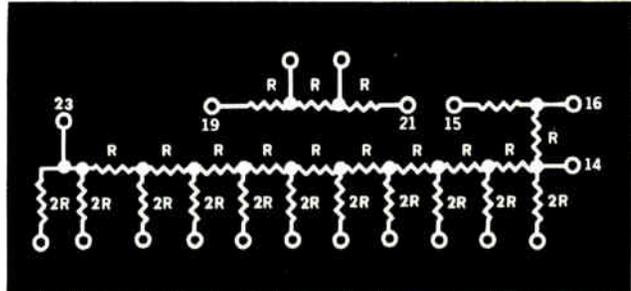
The 7704 and the 7504 can take four plug-ins, while the 7503 and 7403N can take three. All 7000 scopes have the same maximum sensitivity—10 microvolts per division. The 7704 has faster sweep speed—2 nanoseconds per division, against 5 ns/division for the others.

More additions to the 7000 family are being planned. In the design stage is a high-frequency unit. Although the market for 150-MHz-and-up scopes is small, it's a growing one, populated by engineers testing computers and high-speed logic. The fastest scopes available now go to 300 MHz. Tek has not yet made a move in the race for this market [*Electronics*, Aug. 17, 1970, p. 121].

While evolving the 7000 series, Tek also has been active in the low-frequency area. In fact, it has just introduced the 5100 series, which shows a family resemblance to the 7000 scopes, but can't use their plug-ins. The 5100 scopes take three plug-ins, go to 2 MHz, and typically cost under \$1,000. An unusual feature is that the display unit, including CRT, is purchased separately from the mainframe, called the 5103N. It costs \$220; display modules begin at \$320. The scope is intended for electrical service shops and scientific labs.

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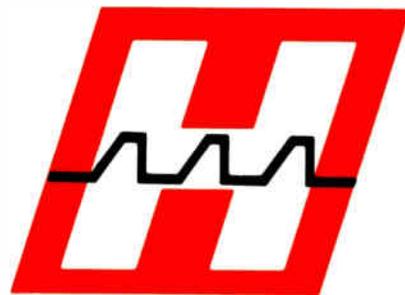
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HI-1010 — \$15.60*ea. — accuracy 0.05% — temp. range 0°C to +75°C
 \$19.20*ea. — accuracy 0.05% — temp. range —55°C to +125°C

HI-0910 — \$10.80*ea. — accuracy 0.1% — temp. range 0°C to +75°C
 \$14.40*ea. — accuracy 0.1% — temp. range —55°C to +125°C

*100 to 999 unit price.



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Components

Resistor nets move into DIPs

Standard products are aimed at high-speed logic circuits, other industrial applications

In line with the swing to dual in-line packages for passive components [*Electronics*, Dec. 21, 1970, p. 97], thick film cermet resistor net-

works are being put in ceramic TO-116 packages. And in line with its own shift from military to industrial product development, the microcircuit operation of Beckman Instruments' Helipot division has introduced three low-priced items of this kind for off-the-shelf sales.

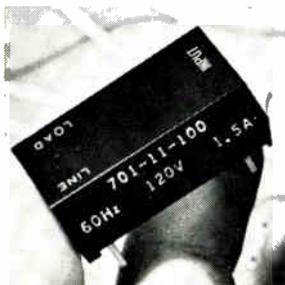
Pricetags on two of the units—a digital pull-up network and a digital line-terminator array—are higher than for the individual axial-lead composition film resistors with which they'll compete, but Beckman's George Smith stresses that the price "on the board" will give the new devices an edge. Smith, manager of research and development in microcircuit operations, and

sales engineer Lyle Pittroff add that for the third product, an analog scaling network, Beckman's prices are lower on a unit basis than those for the wirewound resistors they'll supplant.

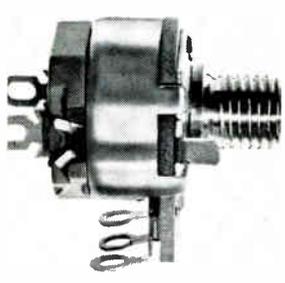
"The dual in-line package is becoming an industry standard," Smith observes. "We feel the old ways of packaging resistor networks are outmoded because industrial equipment manufacturers want DIPs to go with their automatic insertion equipment." The swing to DIPs represents a major move at Beckman. It embodies considerable investment in capital equipment—tooling for the substrates and lead frames, automatic parts handlers,



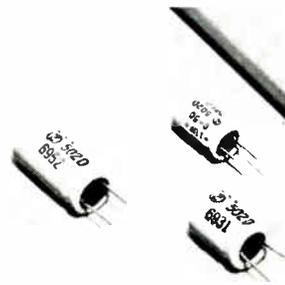
Solid state lamps series MV5020 are for use as panel indicator lights. They virtually eliminate replacement costs. These lights have an operational lifetime of about one million hours contrasting with an operating life of approximately 2,000 hours for incandescent bulbs. Price (1-9) is \$1.65 each. Monsanto Electronic Special Products, Bubbs Rd., Cupertino, Calif. 95014 [341]



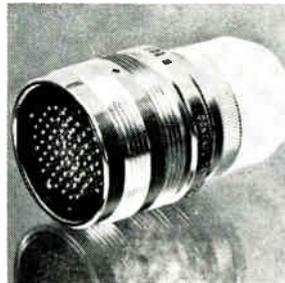
Solid state relay controller comes in two standard pin grid patterns for application to pc boards. The 701 and 702 are available in load voltage ratings of 120/240, 50/60 Hz, at 1.5 amperes. Control voltages are 5 or 24 V dc. Operate time is 1 ms. Prices are \$4.55 to \$8.15; delivery, four to six weeks. Hamlin Electronics Inc., 3066 W. Clarendon Ave., Phoenix. [345]



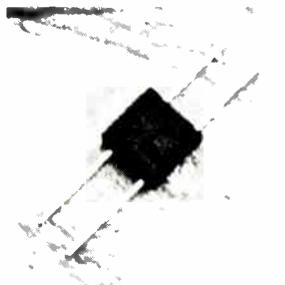
Thin-profile spst switch series 055 was designed for use with 5/8-in.-diameter controls. Features include compactness, completely noncombustible housing material, and self-cleaning contacts for longer switch life. Applications include instrumentation, communications equipment, and aircraft navigation controls. CTS Corp., W. Beardsley Ave., Elkhart, Ind. [342]



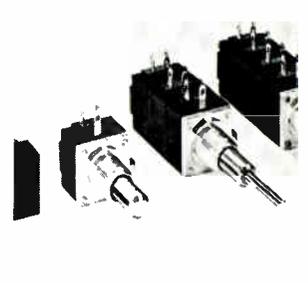
Miniature aluminum electrolytic capacitors can be installed vertically on high-density wiring boards. Type 502D Vertilytic devices are suited for applications in high quality industrial instrumentation, desk top calculators, and computers. They come in voltage ratings of 3, 6, 16, 25, and 50 V dc; capacitances from 1 μ F to 330 μ F. Sprague Products Co., North Adams, Mass. [346]



Lightweight connector is designed to interface CDC computers with peripheral equipment manufactured by other companies. It is a quick-disconnect, push-pull connector with 61 contacts on 0.117-in. centers. Operating temperature range is -67° to $+257^{\circ}$ F. Contact current rating is 7.5 amperes per contact. Control Data Corp., 31829 LaTienda Rd., Westlake, Calif. 91361 [343]



Microminiature inductor series 155 is for use in commercial and military communications as well as in the computer and related fields, where performance and reliability are critical and costs are important. It is constructed with all internal connections thermocompression bonded for high-temperature processing. Delevan Div. of American Precision Industries, E. Aurora, N.Y. [347]



Modular potentiometers series 70 are highly versatile. They are supplied as single or multisection units and are available in cermet, carbon composition, or in combination. Resistance ranges are from 100 ohms to 5 megohms for cermet, 50 ohms to 10 megohms for composition with very broad taper capability. Allen-Bradley Co., 1201 S. Second St., Milwaukee, Wis. 53204 [344]



Variable trimmer capacitors models JMC-5200 and JMC-5201 are Mil approved devices. They have a capacitance range of 0.8-10 pF with a Q factor greater than 5,000 at 100 MHz. Working voltage is 250 V dc with a test voltage of 500 V dc and a temperature coefficient of 0 ± 15 ppm/ $^{\circ}$ C. Size is $3/8 \times 3/8$ in. Johanson Mfg. Corp., Rockaway Valley Rd., Boonton, N.J. [348]

and computer-controlled laser resistor trimming and testing. These three products are the first in a broad line of digital and analog resistor networks that will be coming from Beckman this year.

The digital pull-up network is designated the model 899-1. It consists of 13 resistors with a common terminal, and comes in resistance values of 2,000 or 6,000 ohms for use in high-speed, high-current logic applications. These include unused TTL gate pull-up, wired-OR pull-up, and parallel high-speed pull-up. Resistance tolerance is $\pm 2\%$ maximum at 25°C. Smith says this compares with a resistance tolerance of about 10% for composition film resistors. Pittroff points out that the 899-1, with its 13 resistors, occupies the same circuit board space as about seven axial-lead resistors.

Temperature coefficient of the 899-1 is 400 parts per million per °C maximum, and resistance stability is 1% maximum shift after 1,000 hours at full rated power at 70°C. Smith feels the 899-1 will be widely used in instrumentation applications, including commercial aircraft instrumentation. The units will sell for 81 cents each in quantities from 1,000 to 4,999.

The other digital unit is the 899-3, for use as a terminator array for 110-ohm twisted pair or coaxial lines. This item also will compete with axial-lead composition film resistors, and Smith terms it "a good, low-cost alternative. But the user is also concerned about power," Smith notes. "He may need to dissipate 1/4 watt. The older resistors can do it, but they're usually larger and not as stable if you push them close to their rated power. Ours can be run without derating."

Resistance stability, temperature coefficient, and tolerance for the 899-3 are the same as for the 899-1. Price for 1,000 to 4,999 is 72 cents each; again, because there are seven isolated resistors in the package, its price, assembled on the board, will be below that for the less-expensive composition film resistors.

The model 899-2 analog scaling network can be used anywhere that operational amplifiers are used, Smith says, and also with phase-locked loops and multipliers as gain-scaling networks. Pittroff says, "You can hook op amps to this part in all kinds of gain configurations—from 1/15 to 15 in the operational and differential mode, to 2 to 16 in the potentiometric mode."

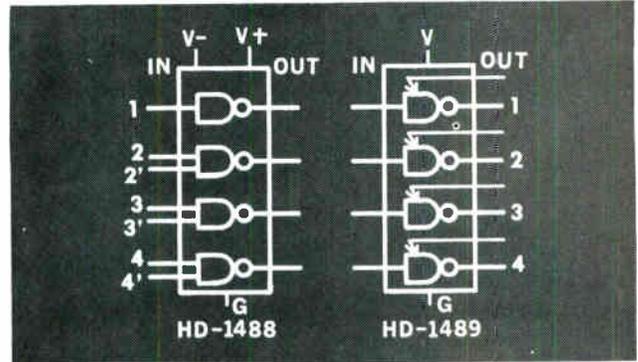
Smith says the big advantage with the 899-2 is that it takes advantage of the tracking of resistors on a common substrate, a capability that can't be duplicated with discrete resistors. Voltage ratio tolerance is $\pm 0.1\%$ maximum; voltage ratio temperature coefficient is ± 20 ppm/°C; and voltage ratio stability with load life shows a maximum shift of just 0.02% after 1,000 hours at full rated power at 70°C.

The 899-2 is priced at \$1.55 each in quantities from 1,000 to 4,999. Smith says there's no inexpensive alternative to the unit, which is a grouping designed to provide a variety of precision resistor ratios. Precision wirewound discrete resistors cost about \$1 each.

Helipot Division, Beckman Instruments Inc., 2500 Harbor Blvd., Fullerton, Calif. 92634 [349]

new

RS-232C DRIVER/RECEIVER



OFF-THE-SHELF DELIVERY

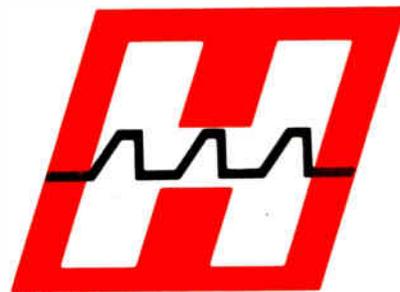
Meets EIA RS-232C interface specifications. Input threshold levels are compatible with TTL and DTL logic. Four circuits facilitate transmission of single-ended binary data.

	HD-1488 Driver	HD-1489 Receiver
Impedance	300 Ω Min. (OUTPUT)	3000 to 7000 Ω (INPUT)
Voltage Swing	$\pm 6V$ Min. (OUTPUT)	$\pm 30V$ (INPUT)
Power Supply	$\pm 9V$	+5V
Propagation Delay	(tpd-) 30ns (tpd+) 250ns	(tpd+) 60ns (tpd-) 25ns
Temperature range	-0°C to +75°C.	

Types available in 14-lead dual in-line package at:

HD-1488 \$6.80*ea. HD-1489 \$4.43*ea.

*100 to 999 unit price.



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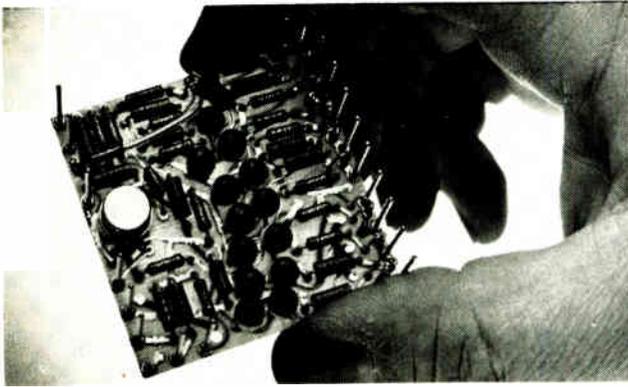
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New products



Discrete digital-analog converter is aimed at low-price markets

When buying a digital-to-analog converter, an engineer looks for tradeoffs among price, settling time, temperature coefficient, output swing, and linearity, plus other factors. And if he finds one with good tradeoffs, he figures he has made a good deal.

That's the reasoning behind Hybrid Systems Corp.'s model 330-12. Built with discrete components assembled on a printed circuit board, it has specifications that allow it to compete with converters costing more than its single-unit price of \$125.

About the only concession made to advanced technology is the use of temperature-coefficient-matched thin film resistors. Otherwise, says Carl M. Kramer, sales manager, the real push has gone into a careful binning and rebinning of discrete components to get the best possible matches. "Working on a hybrid format would increase cost more than the benefits of a common substrate could offset," says Kramer. "It doesn't make sense to go to a sophisticated production method if the only result is higher cost."

The 330-12 is a 12-bit digital-to-analog converter with dimensions of 2 by 2 by 0.4 inches. It's a voltage output device that is linear to one-half the least significant bit with selectable swings of ± 5 V, ± 10 V or 0 to -10 V. And the company says it's fully monotonic, with no dips in its characteristics curves.

Settling time is 10 microseconds, which is not the fastest available but is still faster than some devices selling for \$185. One \$185 unit offers 2 microseconds, but the 330-12 has a better temperature coefficient. Drift is guaranteed at ± 20 parts per million.

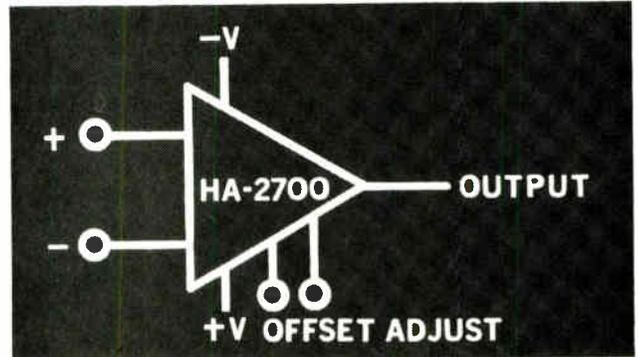
The 330-12 uses a dual zener diode voltage reference with servo loops around it to boost accuracy. In addition, its immunity to variation in the 15 V required of the mainframe is 0.05% per percent of variation.

Kramer says the 330-12 is aimed at cathode ray tube displays, analog-to-digital converters, digitally controlled supplies, and other applications where the specifying engineer is sensitive to tradeoffs. Delivery time is two weeks.

Hybrid Systems Corp., 95 Terrace Hall Ave., Burlington, Mass. 01803 [389]

new

4th GENERATION OP AMP.



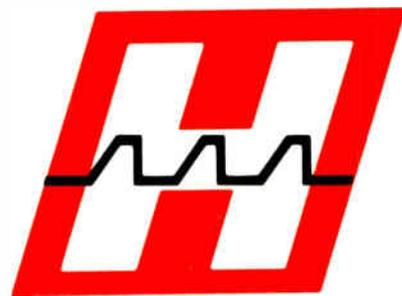
OFF-THE-SHELF DELIVERY

Operates at very low power levels without compromising large signal response or output drive capability.

- Slew Rate — $20\text{V}/\mu\text{s}$
- Input Offset Voltage — 0.5mV
- Power Dissipation — 2.5mW at $\pm 15\text{V}$
- Open Loop Gain — 2.0×10^6 at $R_L = 2\text{K}$
- Input Bias Current — 5.0nA
- Power Supply Range — $\pm 5.5\text{V}$ to $\pm 22\text{V}$
- Built-in Short Circuit Protection
- Offset Null Capability
- Internally Compensated

The HA-2700 is available in the TO-99 package at \$10.20* (0°C to $+75^\circ\text{C}$), \$16.20* (-25°C to $+85^\circ\text{C}$) and \$24.00* (-55°C to $+125^\circ\text{C}$)

*100 to 999 unit price.



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New products

Instruments

MOS/LSI tester is flexible

System can be used in laboratory, pilot line, or production environment

"Some companies stress speed in their test systems, and some push computer capability, but we emphasize flexibility," says Andrew

Kay, president of Non-Linear Systems Inc. The company is marketing an MOS/LSI test system that can be used in the laboratory, in engineering tests, in pilot production, or on a manufacturing line.

The NLS tester, designated the Series A-2, has 42 pins and reaches a top speed of 2 megahertz. "For most applications a computer isn't needed," says Kay, "because the program can be changed in five or 10 minutes at the most." Programming is done by a card reader. This loads a semiconductor memory organized into 48 channels, six of which are control channels and the other 42 are for the test pins. Each channel has a total of 512 serial

bits. Word length is variable from 2 to 512 bits.

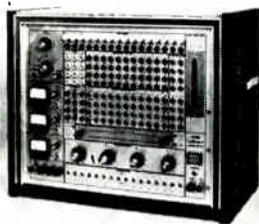
The memory also can be loaded manually. With this alternative, a program already loaded from a card can be altered, providing increased programing flexibility.

The test head assembly, which receives inputs from wafers, is a circular device holding 42 hybrid sense amplifiers—the pins. The wafer is held in a prober beneath the center of this assembly and is indexed so that each device may be checked in turn.

With this approach, says Wilber Bailey, project engineer, only about 2 inches separate the device output and the sense amplifier. This makes



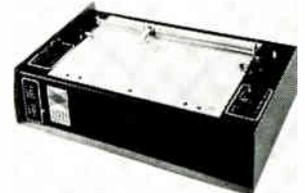
Multipurpose, multirange electrometers permit precise, stable measurements of low amplitude dc voltages, currents and charges without significant source loading. The line consists of the model 134 ac line powered electrometer, the model 135 battery powered unit, and the model 136 digital display type. Princeton Applied Research Corp., P.O. Box 565, Princeton, N.J. 08540 [361]



Dc and dynamic tester model LAN-44A is capable of complete testing and fault diagnosis of most circuit boards of 44 pins or less. It also easily tests any type of integrated circuit by means of a simple adapter at the test connector. Digital or analog testing can be accomplished. Price is \$3,900. Automated Control Technology Inc., 745 Distel Dr., Los Altos, Calif. [362]



Dual-channel oscilloscope 5002 is for use in R&D laboratories, quality control, production testing and precision electronic servicing. Vertical bandwidth is from dc to 25 MHz (-3 db point). Gaussian response makes the instrument usable beyond 50 MHz. Input impedance is 1 megohm, 30 pF. Price is \$995. The Hickok Electrical Instrument Co., 10514 Dupont Ave., Cleveland, Ohio [363]



X-Y recorders series 380 are for laboratory and production testing, and any other application where X-Y graphics may be utilized. They are ruggedly built and easy to operate. Standard $8\frac{1}{2} \times 11$ in. chart paper is used. The paper is driven by rollers that have knurled surfaces, and which grip the paper positively. Laboratory Data Control Inc., Box 10235, Riviera Beach, Fla. [364]



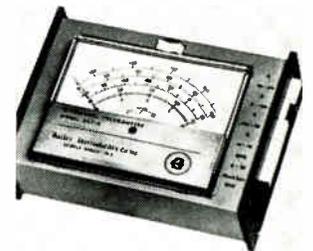
Five-inch oscilloscope model 556A is for use on production lines and educational and general applications. Vertical amplifier is ac/dc coupled and fully compensated for optimum response with a sensitivity of 20 mV/cm over dc to a 1.5 MHz bandwidth. Sweep frequency range is from 10 Hz to 100 kHz in 4 ranges. Kikusui Electronics Corp., 200 Park Ave., New York 10017 [365]



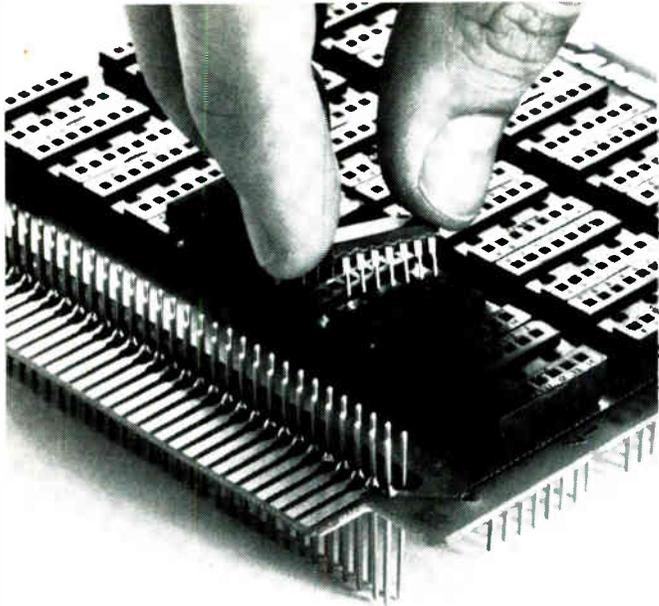
Digital voltmeter model HVM-30-1, useful up to 30 kV dc (50 kV dc with a range extender), can be used as a direct-reading, nonblinking, four-digit DVM or as a precision (0.1% accuracy) voltage divider. As a DVM, the instrument has an accuracy of $\pm 0.05\%$ full scale (± 2 digits). Unit measures $13 \times 9 \times 5$ in. Capatron division of AMP Inc., Elizabethtown, Pa. 17022 [366]



Selective level meter SPM-9 permits level, attenuation and duty cycle measurements on data and remote control transmission systems. Frequency range for selective measurements is from 300 Hz to 8 kHz. Meter frequency-setting accuracy is ± 10 Hz. Unit features solid state circuitry (except tuning indicator). W. & G. Instruments Inc., 6 Great Meadow Lane, Hanover, N.J. [367]



Thermocouple thermometer model BAT-4 gives temperature measurements within seconds on transistors, resistors and other components. Sensor is a thermocouple microprobe 0.008 in. in diameter. Accuracy is 1°C in the range -100°C to $+175^\circ\text{C}$ and differential measurements can be made to 0.2°C . Price with microprobe is \$295. Bailey Instruments Inc., Saddle Brook, N.J. [368]



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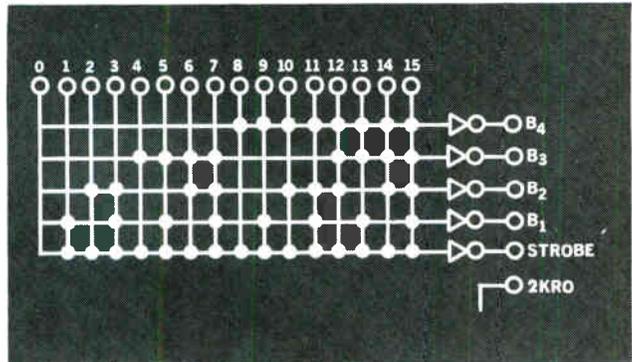
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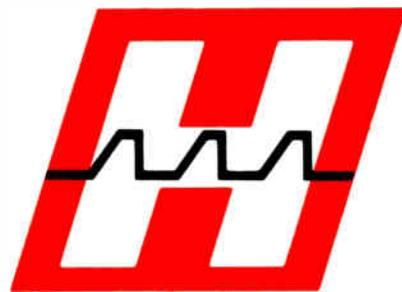
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- Temperature Range — 0°C to +75°C

The HD-0165 is available in a 24-lead dual in-line package at: \$4.60*ea.

*100 to 999 unit price.



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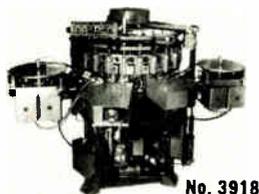
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New products

for minimal loading of the test device as well as a high-quality output signal. The amplifier's input impedance is greater than 1,000 megohms, while capacitance is less than 10 microfarads.

Amplifier output is matched to a 50-ohm coaxial cable. Bailey notes that since the test head is remote from the system, several heads can be multiplexed to one console.

Only two dc (parametric) tests are provided in the first NLS system — a probe contact verification and one to check device power consumption. Functional tests are made in real time to determine input and output levels, and timing. The system includes a clock/strobe generator with four clock and four strobe comparator phases. Each clock phase is independently programable through digit switches.

Strobe phases are independently programable for width and delay. Phase delay is variable from 0-8 milliseconds or 80% of the duty cycle, while each phase pulse width is programable from 50 nanoseconds to 8 ms, again 80% of the cycle. Clock amplitude is variable from 0 to -30 volts. Accuracy is $\pm 2\%$ of frequency and 3% of width and delay.

Clock and input data, and comparator levels are accurate to $\pm 1\%$ of setting, or 100 millivolts. The comparator responds to failure within 35 ns. Failures are signaled by a red light and then may be displayed on a bit-by-bit basis by interrogating the channel (pin input) in which the failure occurred.

Besides systems, NLS will sell modules, such as clock generators and test head assemblies.

The first test system is scheduled to be delivered this month to North American Rockwell Microelectronics Co. This system, to be used for engineering tests, is priced at \$210,000. Other Series A-2 systems can sell for as low as \$125,000 to \$150,000, Kay says. A simpler tester, the Series A-1, requires more manual operations and will sell for \$40,000 to \$70,000.

Non-Linear Systems Inc., P.O. Box N,
Del Mar, Calif. 02014 [369]

Transients recorder analyzes high-speed analog signals

Recording a high-speed analog signal usually is difficult, while processing it for further analysis can be complicated, time consuming, and inefficient. But the whole procedure can be automatic with a transients recorder from Biomation Inc.

With its high-speed, eight-bit analog-to-digital converter and its 1,024-word MOS shift register memory, the model 802 can capture and hold the digital equivalent of an analog signal as a function of time. Sweep time can be varied from 500 microseconds to 20 seconds. Bandwidth is 500 kilohertz and input sensitivity is variable from 10 millivolts to 50 volts full scale.

Biomation provides address information, and the unit can sense front-panel settings and even change them from a connector on back, says B.J. Moore, vice president. The digital format allows the recorder to interface relatively easily with computer systems.

Triggering can be either external or derived from the input signal itself. The trigger can be received before, during, or after the signal occurs. With pretrigger recording, leading edges can be viewed without a delay line or a tape loop. A mixed sweep combining two independent time bases can be used to obtain high-resolution viewing of either the beginning or ending of a signal. Time base changes are continuously adjustable through the full range of the sweep.

Recorded information can be output from memory in analog or digital form. The analog output is smoothed and can be displayed on any oscilloscope using either the fast analog output, or a strip chart recorder or other device connected to the 802's slow analog output.

The 802 also can be used as a high-speed peripheral data-gathering instrument and input buffer memory for a digital computer.

Price for the 802 is \$2,950, and delivery time is 60 days.

Biomation Inc., 1070 East Meadow Circle, Palo Alto, Calif. 94303 [370]

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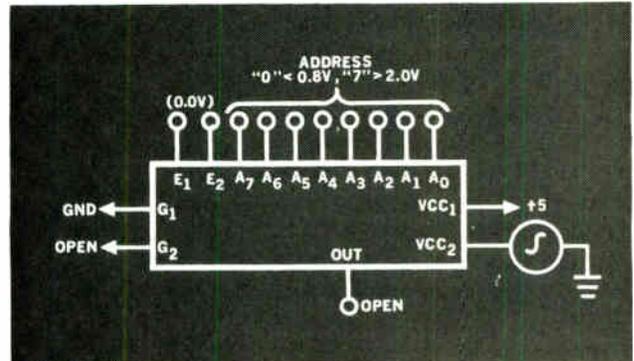
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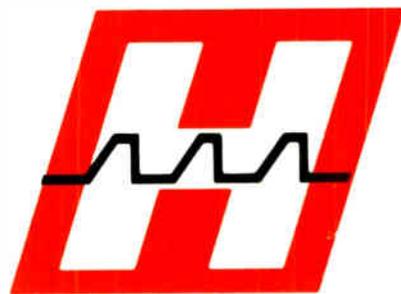
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New products

Semiconductors

Chip modem is low priced

1,200-baud MOS/LSI unit, built to replace Bell's 202, costs \$95 in OEM version

Since the Carterfone decision of 1968, independent manufacturers have been trying to replace Bell System modems with their own

units, most recently in monolithic form. One of these, developed by Modex Inc., employs MOS/LSI technology and offers either asynchronous operation at 1,200 baud or synchronous operation at 1,800 baud. The modem, called the model 202, is available either as a single printed circuit card for OEM applications or as a free-standing unit with its own power supply.

But the manufacturer says the big selling point is the chip itself. Consisting of more than 450 logic circuits using 2,200 transistors, the one-eighth-inch-square chip performs all the functions of Bell's 202, and adds some that the Bell unit doesn't have. OEM versions will sell

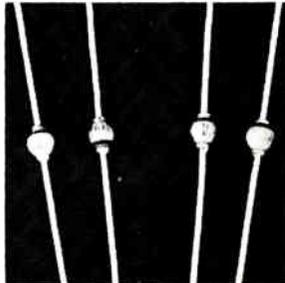
for about \$95 each in 1,000 lots. The free-standing model costs \$75 more.

Among features of the Modex 202 are compatibility with both diode-transistor logic and transistor-transistor logic, a fast-carrier detector, reverse-channel operation at either 5 or 150 baud, transmit and receive synchronization, remote line test, and manual self-test. With the fast-carrier feature, the modem can recognize the data signal in 20 milliseconds, an improvement on standard carrier detectors.

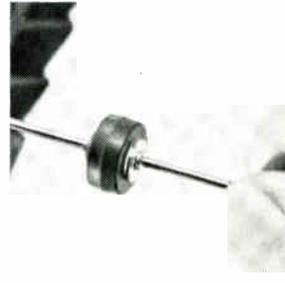
Three remotely controlled test options are offered. In the self-test mode, the transmitter output is connected to the receiver input through



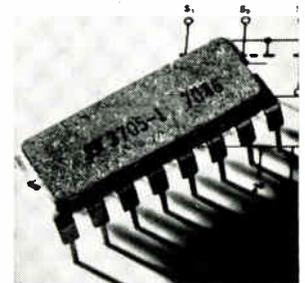
High-gain phototransistors series CLT2100 provide light currents of up to 12 mA, at 5 volts and 5 milliwatts per square centimeter. Dark currents are 25 nA at 10 V with collector-to-emitter breakdown voltages up to 50 V. A narrow, 3 to 1 light sensitivity is standard, and rise and fall times of 3 μ s are typical. Clairex Electronics, 560 S. 3rd Ave., Mt. Vernon, N.Y. [436]



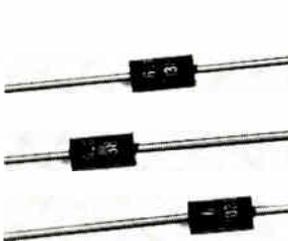
Glass-passivated rectifier, designated Glass-Amp II, features cavity-free construction and high temperature brazed joints. It is suited for such critical applications as telephone switching gear, computers, military equipment, and other similar applications where the cost of component failure is high. General Instrument Corp., 600 W. John St., Hicksville, N.Y. 11801 [437]



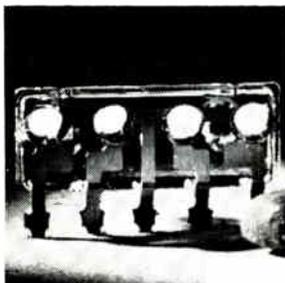
Six-ampere silicon rectifiers series MR751 come in a plastic, axial-lead case. They are provided in four working peak reverse voltage ratings: 100, 200, 400 and 600 V. They display a forward voltage drop of 0.9 V max and a reverse current of 0.25 mA max at rated dc voltage. Inrush surge current capacity is 400A. Motorola Semiconductor Products Inc., Box 20924, Phoenix 85036 [438]



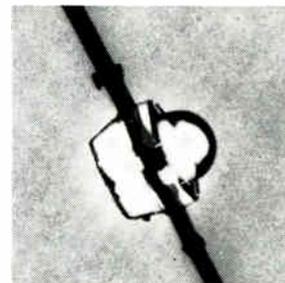
Monolithic 8-channel multiplex switch SI3705DK is a pin-for-pin replacement for the Fairchild 3705. Utilizing p-channel enhancement-mode technology, the multiplexer includes a one-out-of-eight decoder on the chip. Logic input lines are TTL compatible and may be used directly with no level-shifting interface. Siliconix Inc., 2201 Laurelwood Rd., Santa Clara, Calif. 95054 [439]



Pulse-rated 5-watt zener diodes in the TZC series are intended for multicircuit functions. They come in standard zener voltage ratings from 6.8 through 200 V. They feature 200 ampere forward surge current ratings and V_r maximums of 1 volt and 5 amperes dc. Prices start at 77 cents each in 100 lots. Semicon Inc., 10 North Ave., Burlington, Mass. 01803 [440]



Light-emitting diode array MV-5040 is intended for indicator panel and pc board applications. It consists of four gallium-arsenide-phosphide chips on a gold-plate Kovar lead frame. The diode chips have a center-to-center distance of 0.1 inch. Each diode has an output of 750 foot-lamberts with an input of 1.6 V dc at 20 mA. Monsanto Co., Bubb Road, Cupertino, Calif. [441]



Visible red light-emitting diode, called Red-Lit 50, is designed to provide a highly consistent radiation pattern that exhibits a luminance of 750 foot-lamberts at 20 mA. The light output is visible over a minimum of 45° angle. Package width is 80 mils, allowing mounting within 0.087 mil centers of a common card reader. Litronix Inc., N. Tantau Ave., Cupertino, Calif. [442]



Two asynchronous TTL counters are fully programmable. The SN54/74196 decade counter and SN54/74197 binary counter are pin-for-pin replacements for the 8280/81 and 8290/91. Each counter is dc coupled, eliminating restraints normally encountered with charge-stored elements. Units count input frequencies of 0 to 50 MHz. Texas Instruments Inc., Box 5012, M/S 308, Dallas [443]

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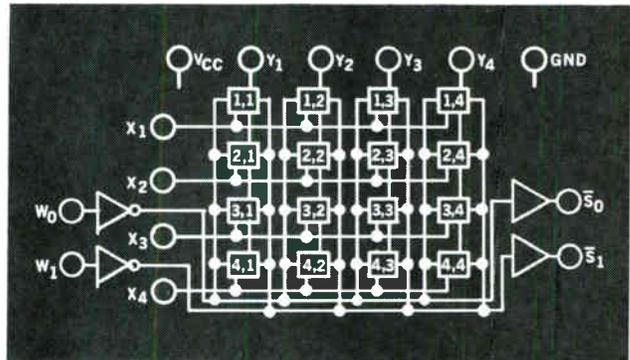
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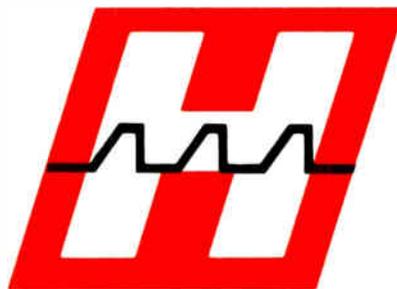
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"Reliability is a feature that's inherent with MOS/LSI," says Donald Lake, Modex vice president. "The units are dynamically burned in for 160 hours to insure reliability and mean time between failures of one million hours."

The OEM modem is mounted on a 9- by 5¼-inch card; the free-standing unit measures 6 by 9 by 2 inches and weighs 2½ pounds. A rack-mounted version that holds 12 cards in a standard 19-inch rack is available as an option. The OEM unit requires three voltages for operation: +5 volts at 75 milliamperes, +12 V at 125 mA, and -12 V at 125 mA. Operational temperature range is 0° to 70°C.

Evaluation units are available now; production quantities will be ready in March. An all-MOS, 2,400-baud replacement for the Bell 201, with automatic equalization, will be ready next year.

Modex Inc., 3150 Pullman Ave., Costa Mesa, Calif. 92627 [444]

Three complex hybrids perform analog functions

"Analog LSI" is the term National Semiconductor Corp. uses to describe its new series of complex hybrid integrated circuits. Jack Christian Jr., a marketing manager, points out that one of them, the LH0023 sample-and-hold circuit, "contains all types of semiconductors—linear, digital, MOS, and field effect transistors. We're using all our technology, and that's why we call it analog LSI."

The LH0023 is a complete sample-and-hold circuit in one package, needing only ± 15 volts and a capacitor. Christian says that with this type of circuit, "you need a

capacitor, and you can't get this in a can. Besides, by having the capacitor outside, the basic LH0023 becomes a more universal part." It's also small—according to Christian, the first TO-8 sample-and-hold on the market. The commercial version will sell for \$30 each in quantities of 100.

Christian points out that the hybrid facility at National does not exist just to produce devices until they can be made monolithically. "Monolithic circuits shouldn't replace hybrids, they should complement them," he says. The LH0023, he points out, contains five monolithic ICs.

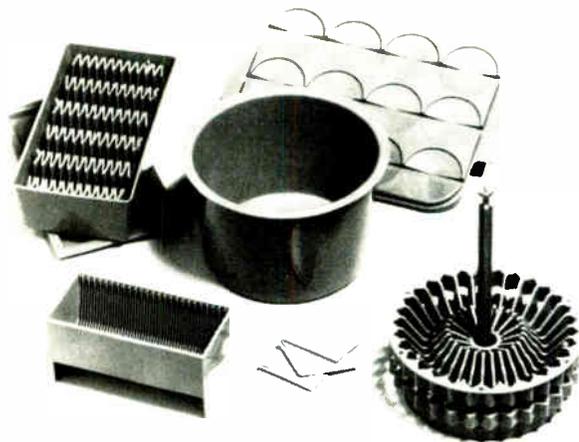
Another new hybrid product in the analog LSI series is the LH0033 FET input buffer amplifier, also known as a very high-speed voltage follower. It's designed as a buffer amplifier for high-speed line drivers, and as an interface circuit between fast a-d converters or high-speed comparators. It has a very high slew rate—typically 1,500 volts per microsecond and about 3,000 V per microsecond max—and a propagation delay of only 1.2 nanoseconds. Input impedance is 10^{11} ohms, and bandwidth is dc to 100 megahertz.

For the commercial-temperature-range LH0033 device in a TO-8 can, the price is \$20 in 100-lots.

The third circuit is a dual-level shifter. Called the DH0034, the circuit changes transistor-transistor-logic voltage levels (ground and 5 V), to IBM's solid-logic-technology voltage levels (ground and -3.6V). Christian says that the main use for this circuit is in computer peripherals since in effect it can make a piece of equipment "plug-compatible with IBM." It can also shift levels from +25 to -25 V and so has many applications in data transmission equipment. The DH0034 sells for \$11.20 in quantities of 100, and it's in a TO-5 can.

All three hybrid ICs will be available from stock by the end of February.

National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, Calif. 95051 [445]



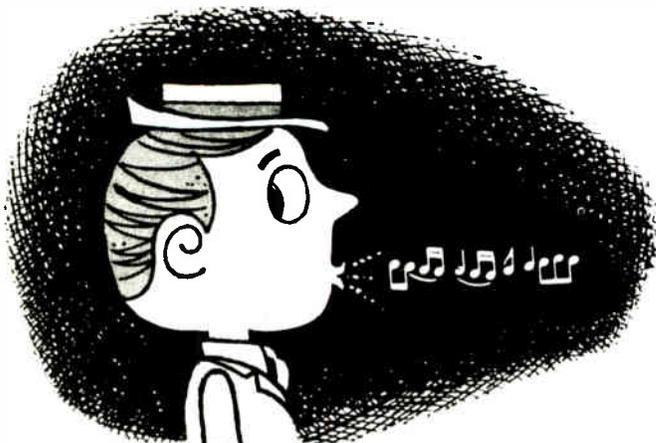
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New products

Open-loop ferrite rods make fast, easy-to-build memory

Read-only memories are finding increasing usage in process controllers, video displays, military guidance systems, and in micro-programming for computers. The ROM approaches include toroidal and U-shaped ferrite cores, plated wire, and semiconductors. Still another storage technique, built around an open-loop ferrite rod, is called Q core to indicate the company that developed it, the two-year-old Quadri Corp. in Phoenix.

In the model 401-18 Q-core system, the basic module has 100,000 bits on one printed circuit board. These can be organized to fit the customer's needs—2,000 words by 48 bits, 4,000 by 24, 8,000 by 12, and all the way up to configurations using 192-bit words. John Bruder, manager of advanced product development, says the Q-core storage element itself, the open-loop ferrite rod, gives true high-speed random access. Access time is 75 nanoseconds and total cycle time is 200 ns.

A sense coil is wound around the storage element circumferentially, and rows of rods (each a cylinder with a 1/8-inch diameter and 3/4-inch length) are arranged in a matrix. To encode a 1, the word wire is put on the 1 side of the Q core; a 0 is stored by running the word wire on the opposite side.

Because the flux paths are in air, inductance is very low. This means fast rise times and therefore high operating speed. It also means that the rod, sense winding, and word wire make up a transformer with a poor output signal.

But this signal is enhanced by adding inexpensive transistors. Bruder says he pays 11 cents each for transistors, from which he makes two-transistor sense amplifiers that bring the signal to a suitable level for driving transistor-transistor-logic circuits. The rods cost about a penny apiece. A conventional U-core transformer read-only memory can drive TTL logic directly without sense amplifiers; the U cores and their ferrite caps,

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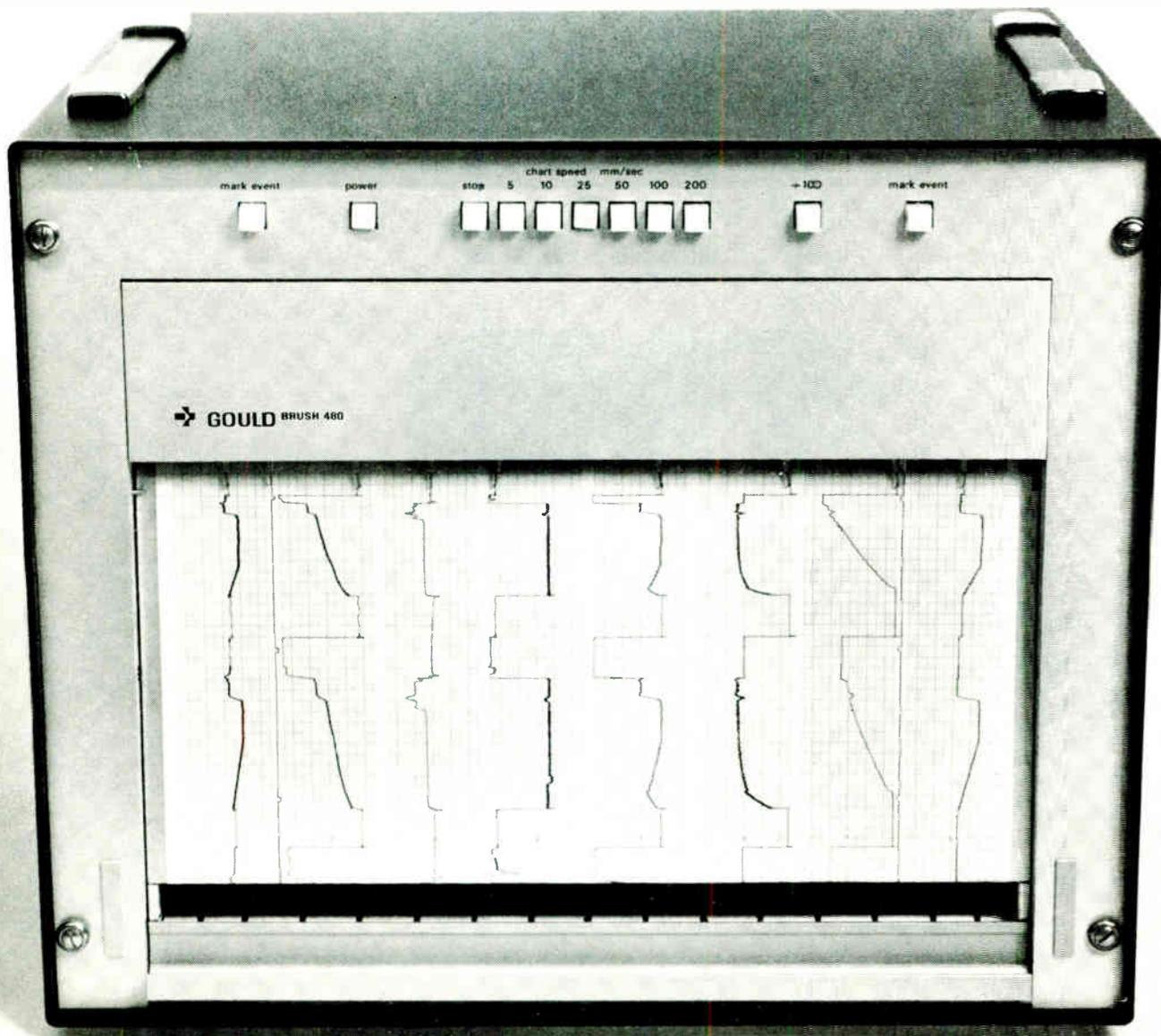
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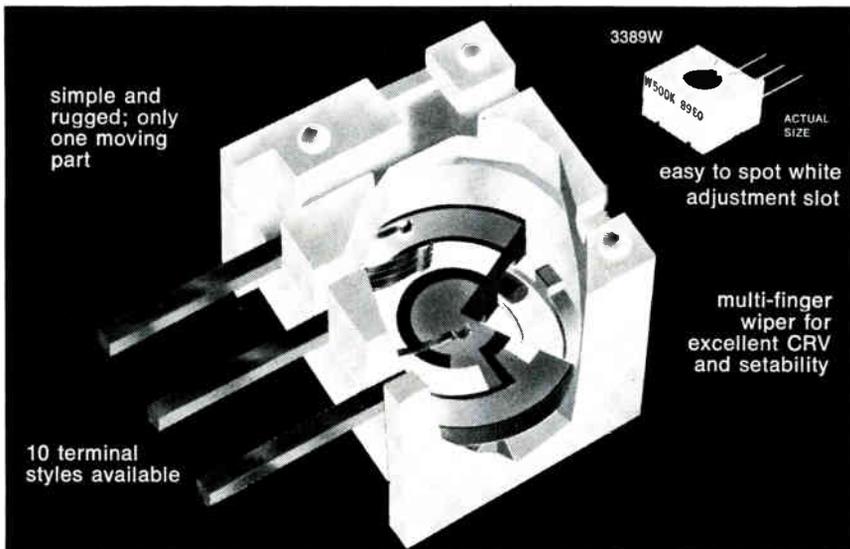
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New products

which complete the magnetic circuit around the windings, cost about 25 cents each, says Bruder.

The costs for components for the Q-core and the U-core approach are about the same. But the advantage comes in ease of manufacturing. The wires for the Q cores can be dropped into place easily over the ferrite rods, and no caps have to be machined to fit or to be mechanically secured against vibration.

Bruder says another technique that can be used with Q cores is to have a bias current on one side of the core opposite to the drive current. If the bias line and word wire are on the same side of the core, its output will be a 0; if they're on opposite sides of the core, a 1 is derived. This kind of arrangement also helps cancel out any noise or crosstalk generated by the intricately wound wires.

Bruder says noise is further minimized by assuring that the core rows are spaced far enough apart so that the magnetic field from one row doesn't radiate into an adjacent row.

The 401-18 uses a pluggable board. Bruder says the ROM can be altered in the field simply by snipping a wire and rerouting it around different sides of the cores in the matrix to change 1s to 0s, and vice versa. The entire 100,000-bit system consumes 6 to 10 watts running at 300 ns. The unit is less than 8 in. wide, less than 12 in. long, and 1½ in. thick. It's sold off the shelf; cost per bit for the 100,000-bit system is about 1½ cents in quantities of 100 or more.

Quadri Corp., 2959 West Fairmont, Phoenix, Ariz. 85017 [446]

MOS chip contains 16-bit shift register-multiplexer

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New products

tronics division has developed a 16-bit shift-register-controlled multiplexer on a chip. It will do the job previously done by several components—a shift register, a multiplexer, and 16 switches.

A feature of this metal oxide semiconductor device is that it can be reconfigured electrically. For instance, it may serve as a four-bit/four-channel multiplexer in one application or as an eight-bit/two channel unit in another. As a 16-bit/one channel unit, the MOS chip performs as a digital-to-analog converter.

Called the model MU-6-8572, it belongs to a family of DTL/TTL-compatible, single-chip circuits. It utilizes low-threshold field effect transistors; these are silicon nitride-passivated, p-channel, enhancement-mode devices. The shift register controls an MOS switch at each of the 16 outputs; each switch has break-before-make action.

Another major feature of the device is its maximum repetition rate of 300 kilohertz. The input pulses are 25 microseconds long and are spaced 0.5 microsecond apart. Pulse rise and fall times are 1 microsecond, consistent with pulse width and separation. The levels of the shift, data, and reset inputs are +0.8 volt for a logic 0 and 1.5 V for a logic 1. Noise immunity is 0.4 V, while input leakage is 1 microampere. Input capacitance is 20 picofarads.

Serial data output logic levels are +0.4 V for a logic 0 and +1.0 V for a logic 1. Data timing is 200 nanoseconds minimum, as is reset timing. The switches' output resistance is 400 ohms maximum with a maximum leakage of 1 μ A. Turn-on time can range from 0.5 to 1.5 microseconds.

Mounted on a standard 24-pin dual in-line package, the MU-6-8572 requires input voltages of +5 V and -12 V.

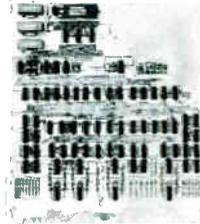
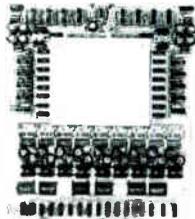
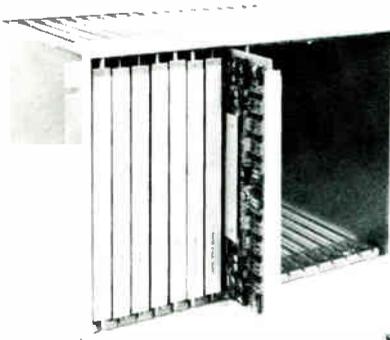
The shift-register-controlled multiplexer is available in quantities of 100 at \$32.40 each. Production quantities require four to six weeks.

General Instrument Microelectronics Division, 600 West John St., Hicksville, N.Y. 11802 [447]

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- What can computers do in medical record keeping and data analyses that they couldn't do before?
- How safe is medical electronics equipment — from the standpoints of both patient and operator?
- How stringent are major test equipment requirements of the clinical laboratory?
- What are the most effective techniques now in use in multiphasic screening?
- What are the key problems in hospital electronic equipment buying and maintenance?
- How will the Cooper Committee report affect new device control legislation?

These questions will be fully explored at a series of unique workshop sessions during the three-day 3rd National Conference on Electronics in Medicine to be held in Boston next April.

The 1971 meeting will include 50 per cent more topics and speakers than the previous conference. Morning sessions will feature speakers who have been selected for their expertise as well as for the articulate manner in which they convey their knowledge to a professional gathering such as this.

The enthusiasm of the '70 conferees for the afternoon panel/workshops has won a repeat performance — this time with topical discussions and specialists who will lead the workshops. They'll attack problems from all sides, then invite attendees to become active participants in the sessions. Conferees will have a chance to join at least two of the six workshop sessions.

An important adjunct to the technical program will be an exposition of new hardware (and software) in the medical electronics field.

SPEAKERS:

Dr. John Knowles, General Director
The Massachusetts General Hospital
Boston, Mass.: Feature address

Dr. Donald M. MacArthur, former
Deputy Director (Research & Technology)
Department of Defense
Topic: Hospital of the future

Dr. H. Fernandez-Moran
The University of Chicago
Topic: Information storage

Dr. Charles Edwards, Commissioner
Food and Drug Administration
Topic: FDA's role in medical device legislation

William Goodrich, General Counsel, FDA
Topic: Evaluating present and proposed regulatory practices

Professor Oliver Schroeder, Director
Law-Medicine Center
Case Western Reserve University
Topic: Medicolegal aspects of electronics in medicine

John T. Kimbell, Exec. Vice President
Baxter Laboratories
Topic: How industry views device legislation

Dr. Arthur C. Beall, Jr.
Baylor University, College of Medicine
Topic: Device legislation: Another look

Dr. Cesar A. Caceres
Professor and Chairman
Department of Clinical Engineering
The George Washington University Medical Center
Topic: Cardiac screening

Dr. Octo Barnett
Director, Laboratory of Computer Science
The Massachusetts General Hospital
Topic: Hospital automation

Dr. John B. Henry, Professor and Director,
Dept. of Pathology
State University of New York
Upstate Medical Center
Topic: Multiphasic screening

Dr. Julius Korein
Dept. of Neurology
New York University Medical Center
Topic: The computer and the medical record

Dr. Max Harry Weil
Associate Professor of Medicine
Presbyterian Hospital, Los Angeles
Topic: Patient monitoring

Dr. Joel Nobel, Director of Research
Emergency Care Research Institute
Philadelphia
Topic: Evaluating equipment

Dr. Dwight E. Harken
Chief, Thoracic Surgery
Peter Bent Brigham Hospital
Topic: Periontogenic diseases

Dr. William A. Spencer, Director
Texas Institute for Rehabilitation and Research
Topic: Electronic prosthetic devices

Dr. Allen Wolfe
Barnes Engineering Company
Stamford, Conn.
Topic: Thermography

Dr. Aida S. Khalafalla
Senior Principal Research Scientist
Honeywell
Topic: Plethysmography

Mr. Roger S. Powell
National Heart & Lung Institute, NIH
Topic: Electrical energy systems for
artificial hearts

EXHIBITS:

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WORK SESSIONS:

Patient monitoring: Leader, Dr. Howard Hochberg; Roche Medical Electronics. A discussion of routine and critical problems in patient monitoring, including available instrumentation and equipment needed to provide improved monitoring.

Computers in medicine: Leader, Dr. William E. Chapman, Palo Alto Medical Research Foundation. What the computer can and can't do in medical record-keeping, data analysis, and medical history taking.

Safety clinic: Leader, Allan F. Pacela, chief research scientist, Beckman Instruments. A forum at which doctors and engineers will be able to exchange views on what is available and what is needed to improve the safety of medical electronic equipment from the standpoint of both patients and operators.

Laboratory automation: Leader, Dr. Hugo C. Pribor, Director, Institute of Laboratory Medicine, Perth Amboy. A discussion of the major test equipment requirements of the clinical laboratory, with a critical evaluation of present and future needs.

Multiphasic screening: Leader, Dr. Allen Pryor, Latter Day Saints Hospital. What are the most efficient techniques now in use and how can they be improved? This session will probe the question.

Impact of electronics instrumentation in hospitals: Leader, John Foster, Associate Director, Tufts-New England Medical Center. Key problems center on selecting and organizing electronics equipment in the hospital to get maximum immediate benefit.

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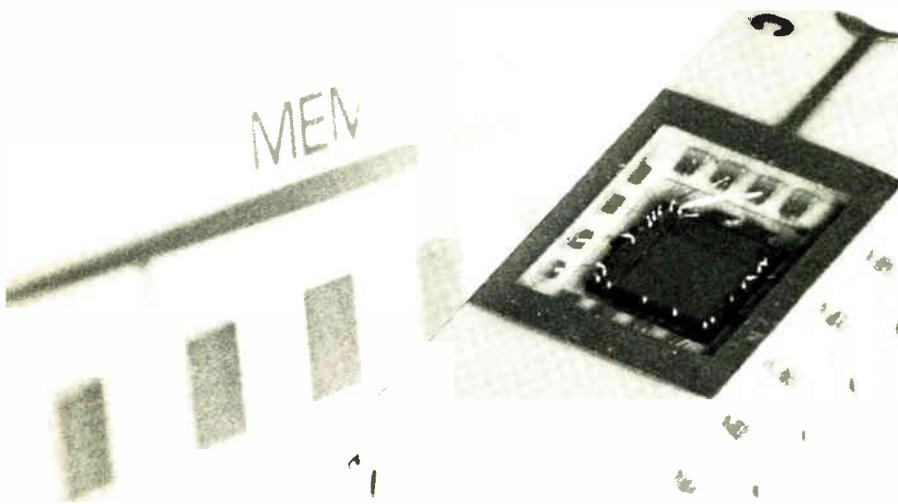
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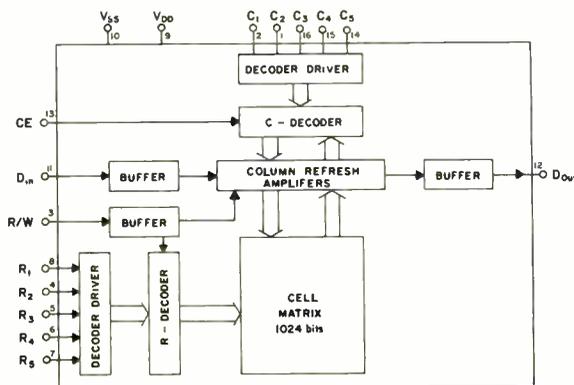


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International Newsletter

February 15, 1971

Sony to sell color TV sets in France and England

Japan's Sony Corp. is starting an effort to penetrate the potentially lucrative European color TV market. Sony began selling a Secam-type set in France last month, while sales of a PAL version for England—with newly developed circuits that Sony claims do not infringe on AEG-Telefunken's PAL patents—will begin in April. Both sets are similar to the 12-inch Trinitron color set sold in the U.S. Sony expects first-year sales in France and England to total 12,000 and 30,000, respectively.

The French receiver, which sells for \$567, is made under license to Cie. Francaise de Télévision, which holds the Secam patents. On the other hand, the English version, to be sold at about \$480, is perhaps more significant because Sony claims to have developed new circuits that do not violate Telefunken's PAL patents—though Telefunken is expected to strongly resist the incursion. This is probably Sony's sole road into PAL territory, because Telefunken generally does not license manufacturers located outside of PAL countries. In an exception to its usual policy, Telefunken did grant Hitachi Ltd. a PAL license because it wanted access to the single-tube color camera (and perhaps other patents) held by Hitachi. But the terms of that license exclude Hitachi sales in Germany and Italy. Sony isn't revealing its intentions toward other PAL countries.

Two British firms pull out of avionics

Unable to compete in an increasingly U.S.-dominated avionics equipment market, two British firms—Standard Telephones and Cables Ltd. and Pye of Cambridge Ltd.—are severely cutting back their activities. Standard Telephones and Cables, an ITT subsidiary, will abandon avionics completely, except for maintenance, after fulfilling existing orders. STC's main line is ground instrument landing systems gear. It also makes other ground aids, including precision approach radars and, until last year, radio altimeters. The company says that the resources required to make avionics gear, particularly in ground installations, have become completely out of proportion to the profit obtainable. The Swedish ITT subsidiary, Standard Radio and Telefon AB, transferred its ground avionics activity to a tripartite combine with Saab and the Swedish government some months ago, but Standard Elektrik Lorenz, the German ITT unit, says it has no intention of pulling out of avionics.

Likewise, the Philips group has shut down the Avionics division of Pye of Cambridge and has offered its business to MEL Equipment Co. Ltd., another Philips subsidiary specializing in military avionics. MEL will absorb only 75 of Pye Avionics' 625 employees.

Germans slate test of digital data switching system . . .

West Germany's postal administration soon will be operating what it calls the world's first computer-controlled electronic switching system for use with public teletypewriter and other digital data transmission lines. A prototype, developed by Siemens AG and installed at the company's Munich facilities, will be tried out on an experimental transmission link connected to terminal equipment at the Darmstadt post office research labs. It will be hooked into the public network by mid-1972 for further trials. Postal officials believe that by the end of the decade all of the nation's three dozen or so conventional electromechanical switching systems will be replaced by the new units.

International Newsletter

The system operates on time-multiplex principles and can handle up to 28,000 data channels, depending on transmission speeds. Speeds achieved are the standard 50 baud for teletype communications, and 200, 2,400, and 9,600 baud for data transmissions. The system has a storage capacity of around 1 million bytes.

... and start work on EDP railroad reservation system

Germany's federal railroads have started up an EDP project of their own—a computerized space reservation system that eventually will comprise hundreds of booking terminals installed throughout much of Western Europe. Participating are the railroads of Austria, Belgium, Luxembourg, and Denmark. The system not only will handle reservations, but also will determine fares, and perform cost and statistical analyses for the railroads and for the various booking offices.

Heart of the system is a Frankfurt-based data processing center consisting of four Siemens computers—two 4004S, 64-kilobyte machines for data transmission and two 4004/45, 131-kilobyte central processors for control purposes. This center will handle some 430 booking terminals—330 installed at train stations and travel agencies throughout West Germany and 100 in the other four countries. Input/output terminals are being supplied by Walther Bueromaschinen GmbH.

Swedish data network faces 2-year delay ...

Design changes will cause a two-year delay in installation of the nationwide data system intended to link some 520 offices of Svenska Handelsbanken, the Swedish banking organization, on line to central computers [*Electronics*, Aug. 17, 1970, p. 115]. Originally slated for full operation by late this year, the system's target now is 1973, according to Svenska Philips, which is under contract for delivery of \$10 million of terminal equipment. Philips took over the contract several years ago from Arenco Electronics, a subsidiary of the Swedish Match Co., when Arenco ran into problems.

The major terminal design change involves linking a number of cashier posts in each office to small "local" computers, rather than linking one terminal to one computer as originally planned. This change will put at least 1,100 terminals (averaging two to each office) on line. Other alterations involve what Philips says is an improved printout system, and use of cassette tapes for storing data in local offices. As a result of these changes, Philips is planning to close down a plant in Gothenburg and is concentrating development and production of the terminal equipment in a Stockholm plant.

... but vehicle taxes may go on line

In order to facilitate legislation for taxation of diesel-powered vehicles on a distance-driven basis, Sweden has appointed a board to study the various metering devices available or under development with an eye toward integrating the tax system and the mileage recording units' output into a computer system. This approach could be helped by a program under way to use a centrally computerized system for all auto and truck registrations. What's more, since this system involves a nationwide network, it could be convenient to use it to handle tax accounting as well, if the input from the recording devices can be easily transferred into the central computer system. Target date for the metering plan to become effective is Jan. 1, 1974.

One-tube color camera is aimed at consumers

Completing trio of consumer color goods, new Sony unit eliminates black index stripe to give improved resolution

A consumer-oriented, one-tube color camera that Sony expects to start selling at the end of this year will complete the company's trio of color consumer products—TV receiver, video tape recorder, and camera. The color recorder is still somewhat too expensive for the average consumer, and the color camera—with a target price in Japan of less than \$830—is even more expensive.

The recorders, however, are already making the transition from the consumer field—Sony says its annual production of VTRs is now about 40,000—and the cameras will follow the same route as increased production and experience brings lower prices. Sony's industrial two-tube color camera, the cheapest one available in Japan, cost more than six times the target price for the new one-tube camera.

Sony is trumpeting the color camera as an entirely new concept, but in some ways it represents another step along one branch in the evolution of the two-tube color camera developed by NHK for the 1964 Olympics—[*Electronics*, Feb. 6, 1966, p. 103]. In the NHK camera, one tube is used to generate a high-resolution black-and-white picture signal; the second tube generates a low-resolution color signal.

A mask with 80 groups of red,

green, blue, and black strips is located in front of the color-signal tube, the output of which corresponds sequentially to red, green, and blue picture information. At the black stripes, an interruption in the picture information serves as a timing pulse.

In 1969, Sony started marketing a simplified industrial camera based on a similar principle. In it, the three color signals are added to form a low-resolution luminance signal. That luminance signal is compared with the separate luminance signal to adjust the level of the chroma signals with respect to the separate luminance signal. Increasing the number of stripe groups should give a luminance signal of sufficient resolution that the separate luminance signal could be eliminated—the path Sony took to build its one-tube camera.

Sony made an important refinement in its new camera tube, though. It did away with the black stripe. The basic system wastes one-quarter of the incident illumination at the black stripe. The black stripe also increases the width of the repetitive group of stripes, decreasing the number of groups that can be arranged in front of the photosensitive target.

To keep costs down, Sony was limited to a 1-inch tube, whose effective target width is about 14 millimeters. Since at least 200 groups of stripes must be used, even with no black stripe the width of each stripe is in the order of about 20 microns, close to the limit of the technology used by Sony.

Elimination of the index stripe

eliminates discontinuity in the signal, greatly improving camera performance. Also its elimination gives between three and four times the resolution by avoiding the need for a filter to remove a subcarrier generated in black-stripe filters. What's more, the vidicon beam focus does not have to be as sharp; when the index stripe is present the pulse representing its position must be very sharp.

Getting rid of the index stripes is easy, but some other means must be used to generate the index signal to be able to detect the chroma signal. Sony developed a new camera tube, the Trinicon, that generates the index signal electronically at the same time the chroma signals are generated. In addition to the signal electrode, the Trinicon, which is based on the vidicon, has a transparent index electrode between the photosensitive surface and the glass faceplate. This index electrode must be aligned with the three color stripe groups for proper generation of the index pulses.

With this tube, the three primary colors are sampled 120° out of phase with each other. An analysis of the composite signal shows that it is very similar to the NTSC color signal; color information is present in the form of color difference signals that disappear when no color information is present.

The prototype camera is reasonably compact and light. Without the lens it is 13.9 inches long, 6.6 inches high, and 6.5 inches wide, and it weighs only 14.5 pounds. Sony emphasizes that these figures are for prototypes made in the lab-

oratory and that a production group would make a smaller and lighter camera.

Great Britain

**RAF Jaguars to be fitted
with small ILS receiver**

Current instrument landing equipment specifications date back some 25 years, and there has been little incentive for makers to incorporate advanced electronic techniques. For demodulation, airborne receivers still use ferromagnetic filters, which drift with temperature and time and have to be aged and matched before use. In England, a digital airborne receiver got to prototype stage but no further [*Electronics*, Aug. 4, 1969, p. 23].

However, Cossor Electronics Ltd., a Raytheon subsidiary, has fared better with a new receiver design that uses synchronous detection instead of iron-cored filters and is built around integrated circuits as much as possible. This equipment will be standard on British Aircraft Corp. Jaguar interceptor-trailers, due for first delivery to the RAF next year. The first receiver to meet full specification is nearly done, and flight proving models are due in May.

In ILS systems, the airborne receiver compares 90-hertz and 150-Hz tones that are amplitude modulated onto vhf (localizer) and uhf (glide path) carriers transmitted from the ground. In the localizer axis, the 90-Hz tone predominates to the left of the path center line, the 150-Hz tone to the right. In the glide path axis, the 90-Hz modulation predominates above the ideal descent path and the 150-Hz tone below. The receiver filters the two tones and compares their depth of modulation. When it is identical, the aircraft is on the center line. Any difference deflects a needle in the pilot's display to indicate the direction and degree of error.

Cossor's demodulation technique is the work of Mike Mansfield and Howard Prangnell. Like conventional demodulators, each tone

channel provides a dc output proportional to modulation depth and these are compared in a difference amplifier which outputs to the meter. In each channel, the dc output is obtained by using a variable frequency oscillator that is phase locked to the modulation frequency to open and close MOSFET switches so that they pass only a selected portion of the modulation waveform to the difference amplifier. R-C pulse oscillators are used and each is designed to select its particular modulation frequency.

The oscillators are phase locked by feeding back their outputs to open and close further MOSFET switches so that they pass to the oscillator, via an op amp network, a portion of the modulation waveform. The feedback timing is in quadrature to the modulation, so that the modulation half-wave passed is approximately negative peak to positive peak, with an average dc value near zero. This small current is fed through an op amp with very high dc gain to the oscillator. The gain is such that only a minute amount of phase difference is sufficient to phase lock the oscillator to the modulation wave. If the oscillator changes frequency, the phase lock shifts, the modulation half-wave passed is no longer virtually peak-to-peak so that its dc level changes, and this change acts as an error signal to bring the oscillator back into line.

In fact, the oscillators run at four times the modulation frequency and each is followed by two TTL digital chains. One chain feeds back the quadrature control signals to the oscillator control switches, and the other feeds in-phase control signals to the switches passing the rectified waveform to the difference amplifier.

Because the system depends essentially on comparison techniques, it is the ratios of the resistive networks used that primarily determine system accuracy, not their absolute values. Prangnell says that this characteristic makes the Cossor system easier to produce to high initial accuracy, using thick film construction. Tests on a proto-

type built to category two operational standards—which permit a maximum root-mean-square error in the difference of the depths of modulation at a course center line of ± 9 microamps—showed a worst-case error of $2.6 \mu\text{A}$. Mansfield says nearly all the error came from inherent offsets in the op amps used.

Japan

**Extra transistor raises
bipolar memory performance**

A bipolar buffer memory being developed by Hitachi combines high speed with a power consumption lower by at least an order of magnitude than other similar devices. The key to the memory is a third transistor that, during readout only, switches the collector impedance of the flip-flop transistors to a low value for fast response time. The rest of the time, high impedance keeps power consumption down.

A high ratio of operating current to standby current is important in keeping power consumption and, thus, heat dissipation low. What's more, low power consumption leads to the compact construction needed for high-speed operation. A 288-bit Hitachi prototype achieved access and write times of 4 microseconds, standby power consumption of 100 microwatts, and a chip size of 70 by 100 mils.

The archetypical word-organized bipolar memory has two dual-emitter transistors with collectors and bases cross coupled to make a flip flop. Two emitters, one from each transistor, are connected together at the word line. One second emitter is connected to the plus digit line, the other second emitter to the minus digit line.

Normally one of the transistors is on and one off. Readout is performed by raising the potential of the word line toward the collector voltage. Current flowing in the word line is interrupted, and current from the one transistor flows into the digit line to which the second emitter of that transistor is connected. Write is performed by

raising the voltage of the word line and one of the digit lines. Because the voltage is raised, current is reduced to about 80% of the standby current.

At last year's International Solid State Circuits Conference, a group from Bell Laboratories described a bipolar memory with an operating current five to eight times the standby current. Hitachi's new design, to be disclosed at this year's ISSCC, is even more efficient and provides an operating current-to-standby-current ratio of 40 to 200 times.

In Hitachi's approach, one emitter from each transistor is connected to the emitter voltage line through a high-value resistor rather than directly to the word line. The third transistor included in the basic cell is also a dual-emitter type. Its collector is connected to the power supply end of the collector-load resistors. Each emitter is connected through a small value resistor to one of the collectors of the flip flop and the base is connected to the word line. When the cell is accessed, the low-value resistors in the emitter circuit of the switching transistor are, in effect, connected in parallel with the high-value flip-flop load resistors.

In the actual circuit, the high values of collector and common emitter resistors would occupy a prohibitively large amount of real estate if standard diffused resistors were used. This problem was solved by using pinched resistors, which enables fabrication of high resistances in almost no space and which cancels out problems with resistor temperature variation.

Switzerland

MESFET memory stuffs in the bits

Anyone aiming to improve his memory should write the word "MESFET" near the top of his work list. For MESFETs may mean 4,096-bit memories packed onto a single 100-by-100-mil chip. What's more, access time will run less than 100

nanoseconds. And MESFET memories will be as stingy with power as they are with real estate—a 4,096-bit chip would need only 50 milliwatts.

Forerunners of these metal semiconductor field effect transistor memories have been built at IBM's Rueschlikon research center on the outskirts of Zurich by a multinational team of semiconductor scientists. Karsten E. Drangeid, who leads the group, will describe the Swiss work at the International Solid State Circuits Conference.

Drangeid's group calls its device a fixed-address MESFET memory cell with normally-off Schottky barrier FETs. Already proved out are single standard memory cells—four transistors and two resistors. Each cell takes up 2.4 square mils of real estate. Currently under test is a three-by-three array of cells. But there is no timetable yet for stepping up to a 4,096-bit array.

The group first began looking at MESFETs as a way to push the operating frequencies of FETs well up into the microwave region. A little over two years ago, the team had 12-gigahertz silicon transistors to their credit [*Electronics*, Dec. 9, 1968, p. 199]. Last year, they boosted the frequency to 15 GHz for silicon and logged 17 GHz—the limit of their measuring instruments—for a gallium arsenide Schottky barrier device. The curve measured for the GaAs transistor indicates a maximum frequency of 30 GHz.

To achieve these frequencies, Drangeid's team had to develop ways to grow very thin epitaxial layers—between 0.2 and 0.3 micron. The thin layers, of course, have to be paired with very tight spacing—1 micron between the source, drain, and gate contact.

For the epitaxy, the key is a lower than usual process temperature, 950°C. To fit everything in tight, the researchers used projection masking and self-alignment. Windows for the gate and the source and drain contacts are opened in one step. Then chrome-nickel is deposited on all three, making each a Schottky barrier contact. The source and drain con-

tacts, though, are converted to ohmic contacts by covering them with gold antimonide and heating them to 550°C.

Drangeid still sees a heady potential for MESFETs as high-frequency transistors. In fact, his team intends to see what the operating frequency limit of FETs can be. "Fifty or 60 GHz looks possible," he says. But IBM's principal business being what it is, the Rueschlikon researchers realized right off that the tight spacings needed to build microwave transistors also pointed to a very high packing density for the cells.

Trouble is, though, that an ordinary MESFET needs a negative bias on the gate, a real drawback in practice. The bias is needed to drive the depletion layer all the way through the epitaxial layer—0.2 micron thick for the high-frequency MESFET. However, a very shallow inherent depletion layer lies under the metal gate electrode; To get a normally-off device, Drangeid's group builds its cells with an epitaxial layer only 0.08 micron thick. The cells then have a threshold voltage of 0.1 volt and they operate off a 0.9-V supply.

Synergism between watches and electronics helps both

With \$1,500, quartz crystal, integrated circuit watches starting to grace the wrists of the well heeled, it's clearer than ever that what's

Limelight. One laser welder on display splits beam for three welds at once.



good for watchmakers is good for electronics.

The symbiosis extends from the marketplace all the way back to production lines, where electronic equipment speeds fabrication of mechanical watch movements and where watchmaking machinery speeds assembly of electronic equipment. Signs of the intertwining popped up constantly at the Zurich Microtecnic high-precision techniques show this month.

One of the most exemplary machines on view at Microtecnic was a programmed assembly table that is the mainstay of Equipments Industriels de Montage SA (ISM), a Lausanne specialist in watchbuilding machines.

ISM engineers took a hard look at timepiece assembly and found that a whopping saving in manual motions—and therefore in assembly time—could be realized when operators put one part at a time in several watch movements rather than several parts at a time in one movement. When five parts are involved, for example, the time saving works out to 64%. So ISM developed a machine that carries movements past an assembly station with a small bin for the part to go into the movement at that time. Each time the carrier makes a revolution, a new bin moves into place.

Inserting components into thumb-nail-sized printed circuit cards involves much the same kind of hand motions, so ISM has found customers for the machine among Swiss and British electronics hardware producers. After the pc boards have made their rounds for component insertion, a holding ring is slipped over the carrier, and it takes another turn—upside down—for soldering. The carrier holds either 20 or 25 boards or movements; the time for a revolution can be set from 10 minutes to 1 hour. In its latest application, the machine has gone full cycle—it's used to make pc boards for watches.

Electronic gear is doing its bit for mechanical movements, too. Omega Equipment Louis Brandt et Frère SA spot-welds copper-beryllium coupling wheels for its auto-

matic wristwatches with a ruby laser, which it developed with Alcyon Electronique & Physique SA. Alcyon's laser puts out 30-joule pulses at a maximum repetition rate of one pulse per second. Omega's hardware splits the beam—with mirrors—into three, so that three equally spaced welds are made.

The beam splitter also can be had in versions for two, four, or six welds at a time. Production rate is 1,400 pieces an hour. Omega is marketing the laser welder to outsiders at \$35,000 and up, depending on accessories.

Likewise, the mechanical movement people also are doing their bit for electronics. Les Fabriques de Balanciers Reunies SA of Bienne, which turns out balance wheels for watch movements, several years ago found it needed a long-life, clean-breaking, fast-operating microswitch. What it wanted wasn't on the market so FBR designed one.

The switch pairs a reed with a two-piece magnetic circuit. When the actuating button is pushed, one of the magnetic pieces moves within range of the reed relay, closing it. When the button is released, the two pieces snap back together, opening the contact. Speed of commutation can run higher than 50 operations per second. Because there are no springs to tire out, life is remarkable—up to 100 million operations, depending on the load on the contacts. FBR has been selling the switches to outsiders for the past three years.

France

Laser and piezoelectric crystals align masks

Engineers often need dimensions smaller than 1 micron for designing LSI circuits, high-frequency transistors, and other advanced components. But even the best optical mask alignment tables reach their limit at about 1 micron. Some researchers try to beat the movement problem by designing new types of alignment tables. Bell Laboratories, for example, is developing a

table that floats on an air cushion to avoid vibrations.

France's Thomson-CSF is taking a different approach. The company's Central Research Laboratory has built a prototype table whose movements, tracked by laser beams, can be corrected to within 0.3 micron. Adding a system of electronic digital interpolation can reduce the error to a minuscule 0.04 micron.

The French table actually is a sandwich of four interconnected platforms. Two of them, moving in the X and Y directions, are driven by motor-turned lead screws. Two corrective plates are hooked to these main plates by ceramic piezoelectric connections. On two sides of this layered assembly, mirrors reflect a split laser beam that is bounced to four standard interferometers. With the laser beam striking each end of the two sides, information on rotational as well as lateral movement is fed to the interferometers. A portion of the laser beam also is reflected from a stable mirror placed on the machine's projection column, giving a standard for comparison.

As the table's distance from the interferometers varies, so does the light intensity the interferometers receive from the mirror reflection. The interferometers thus send varying voltage to the table's piezoelectric layers, which expand and contract to correct the table's wiggles.

The table also gives a precise reading of a substrate's position, allowing adjustments. A digital-to-analog converter transforms the signal from a binary counter into an analog signal corresponding to the wafer's position. This signal can be observed on an oscilloscope or can be recorded for use with a computer.

The world market for such machines should total "several dozen" over the next few years, estimates Raymond Marcy, head of Thomson-CSF's coherent light applications laboratory. He figures the Thomson-CSF table would cost some 10% more than the \$200,000 pricetag of existing top-quality units.

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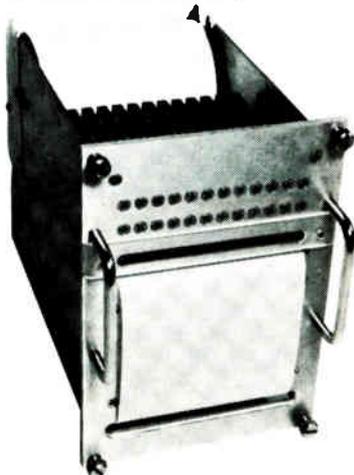
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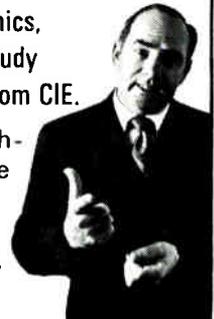
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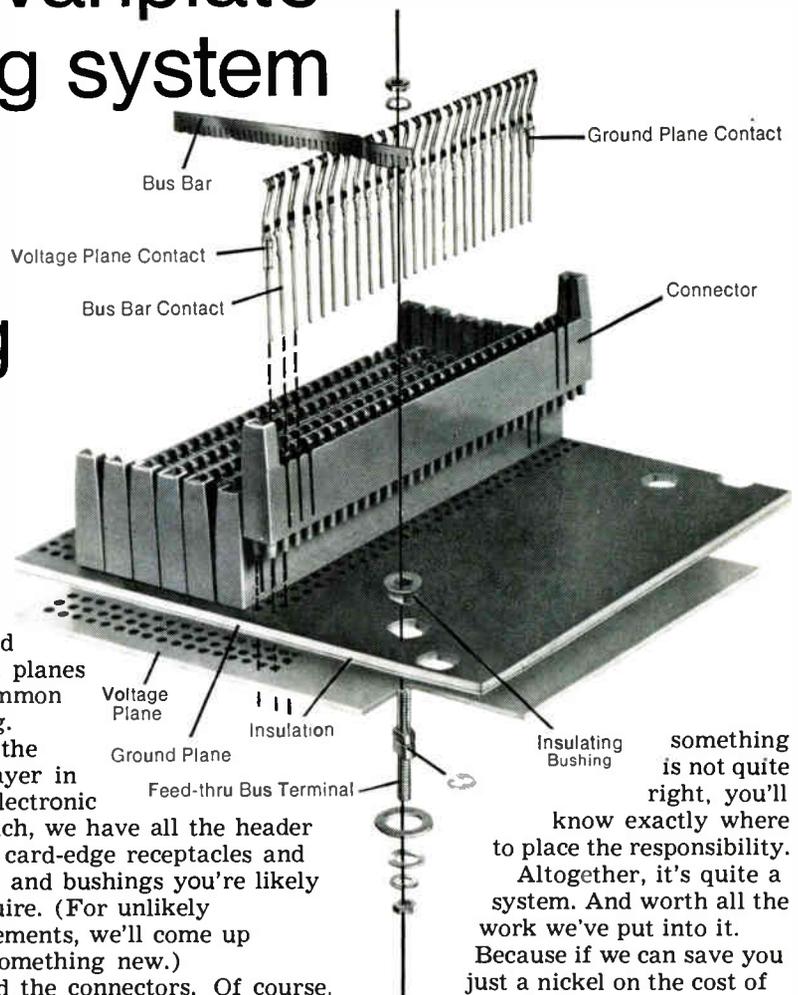
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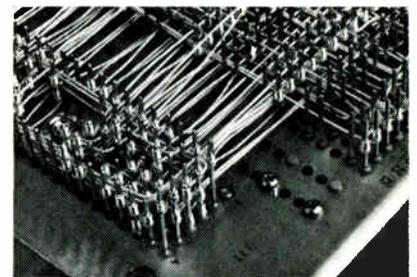
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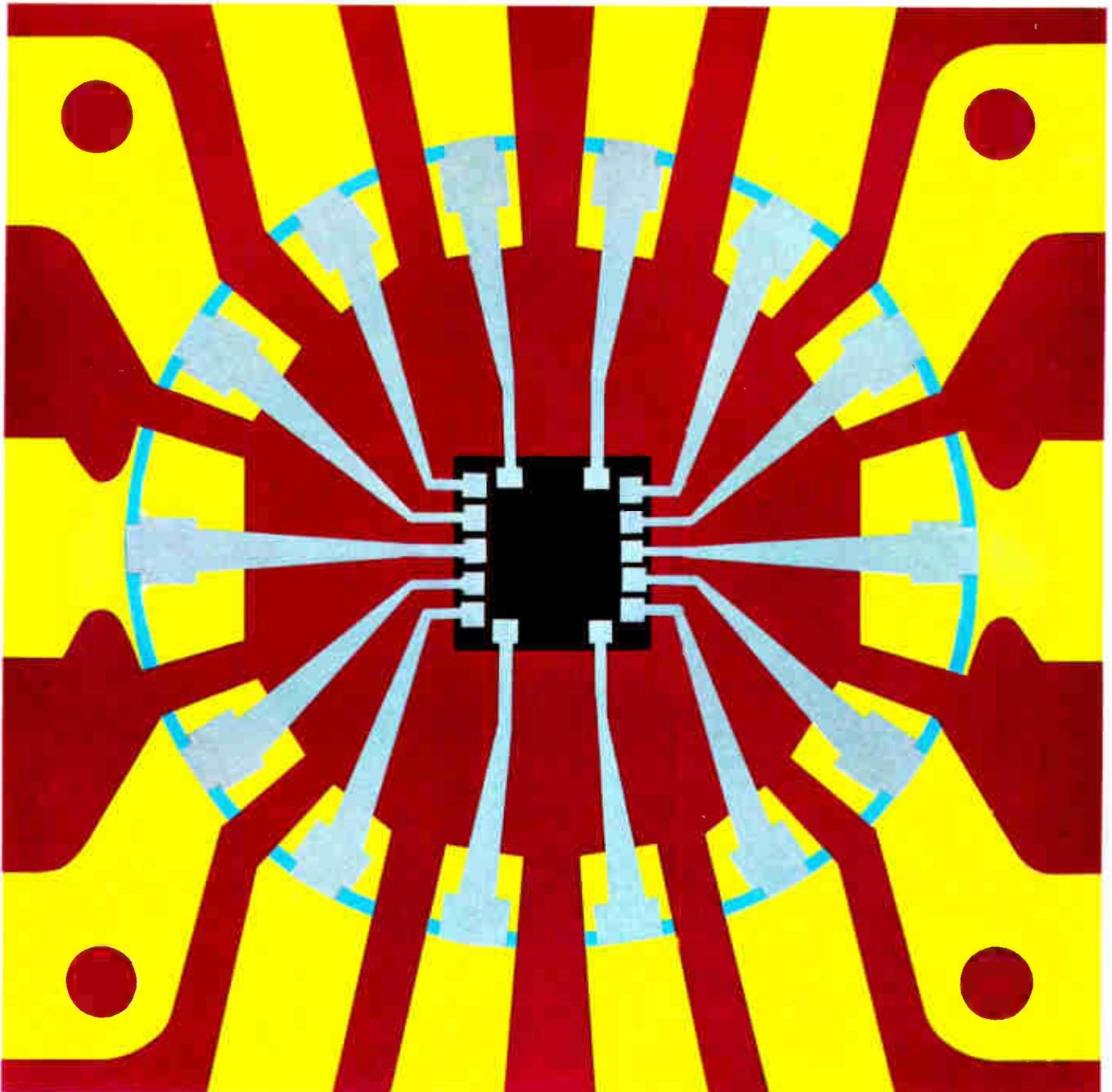
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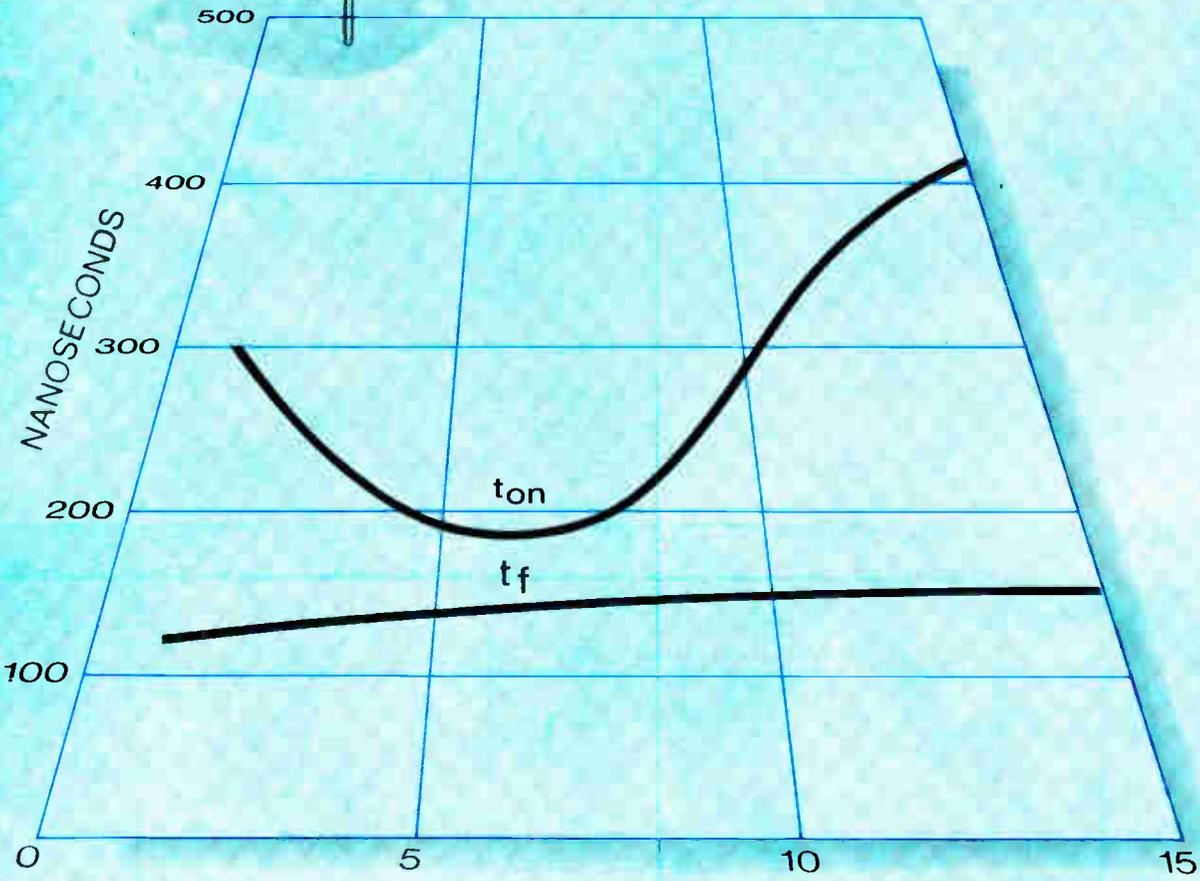
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