

APRIL 10, 1980

**COLOR MONITORS GLAMORIZE BUSINESS COMPUTERS/153**

Chips synthesize true-to-life speech/113

ECC embraces materials, processing/119



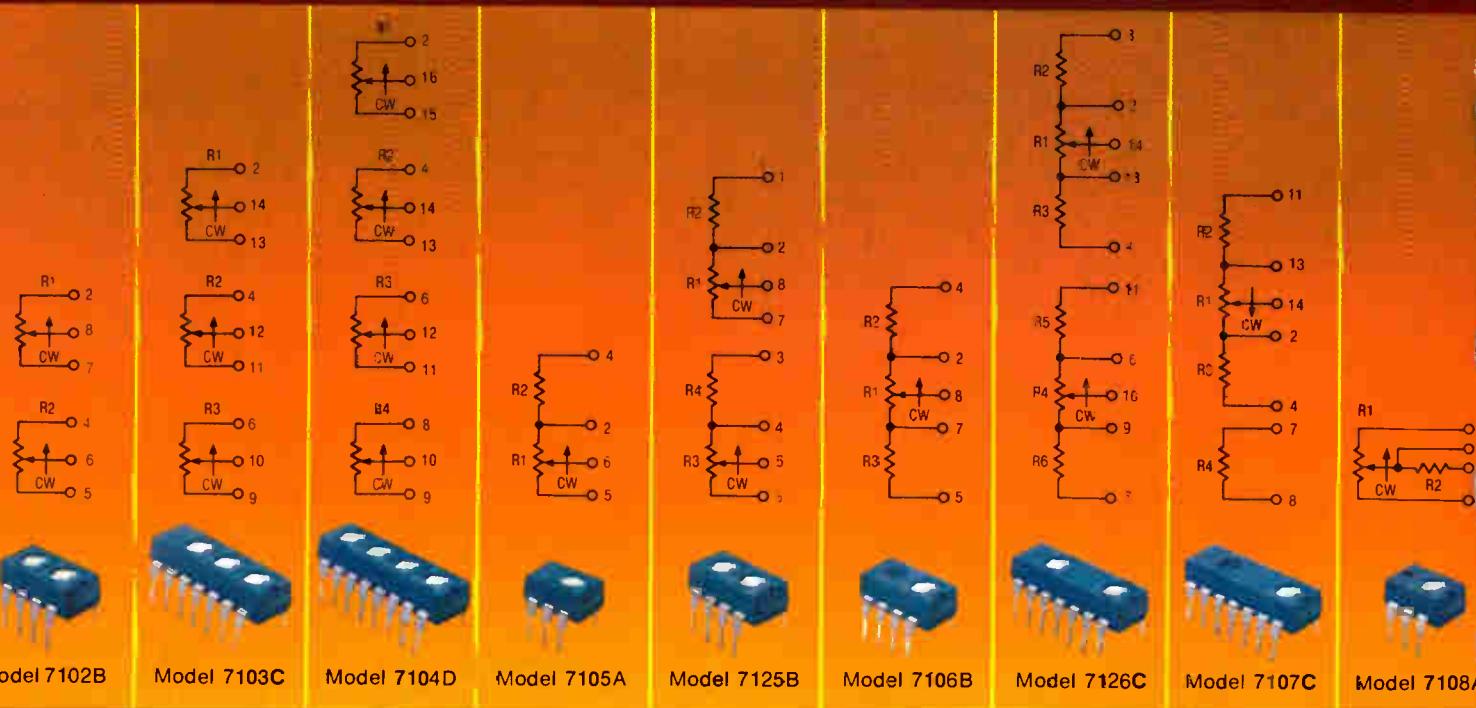
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## Cover: Calculatorlike keyboard programs precision multimeter, 105

Microcomputers controlling and simplifying multimeter operation have until now been inaccessible to the user: programmed to do specific jobs, they were not set up to learn new ones. But Fluke's new programmable 5½-digit multimeter enables the engineer to mold the processing power as needs dictate. Programs for a wide range of measurement tasks can be entered via an optional hand-held keyboard and stored in detachable modules.

Cover illustration is by Ron Chironna.

## Japanese IC industry leaders make overtures in Washington, 81

When Japanese electronics manufacturers had trouble with product quality in the 1950s, they hired American consultants to help them straighten out the problem. Now, in the name of easing tensions in international trade, the Japanese come to Washington offering to show U.S. integrated-circuit makers how to improve the quality of their parts.

## Speech-synthesis chip mimics individual human voices, 113

Not all speaking electronic gadgets made with National Semiconductor's speech synthesizer will sound the same—they can be given distinguishable, natural-sounding voices. To do this, waveforms of a given human voice are digitized; the data is then compressed and stored in semiconductor memory.

## Mapping scheme expands 16-bit processor's memory space, 130

Since the addressing capabilities of microprocessors are approaching those of some mainframe computers, it's not surprising that sophisticated memory organization akin to that of mainframes and minicomputers is turning up in microcomputer systems. A Z8000-based microcomputer board incorporates a mapping scheme that both adds to the logical memory space and eases its management.

## Small option cards are just right for board-level computers, 135

If a single-board computer's application demands extra math-processing power or more input/output ports, for instance, the extra circuitry may not justify another board of the same size. Intel Corp. has worked out a standard bus for attaching small expansion cards to a new family of single-board computers so that users can get what they need without waste.

## . . . and in the next issue

A family of 16- going on 32-bit microprocessors made with high-performance n-channel MOS . . . factors bearing on alpha-particle-induced soft errors in random-access memories . . . coverage of Electro/80 . . . estimating losses in a butt joint between an optical fiber and a light-emitting diode . . . a floating-point math-processing chip.

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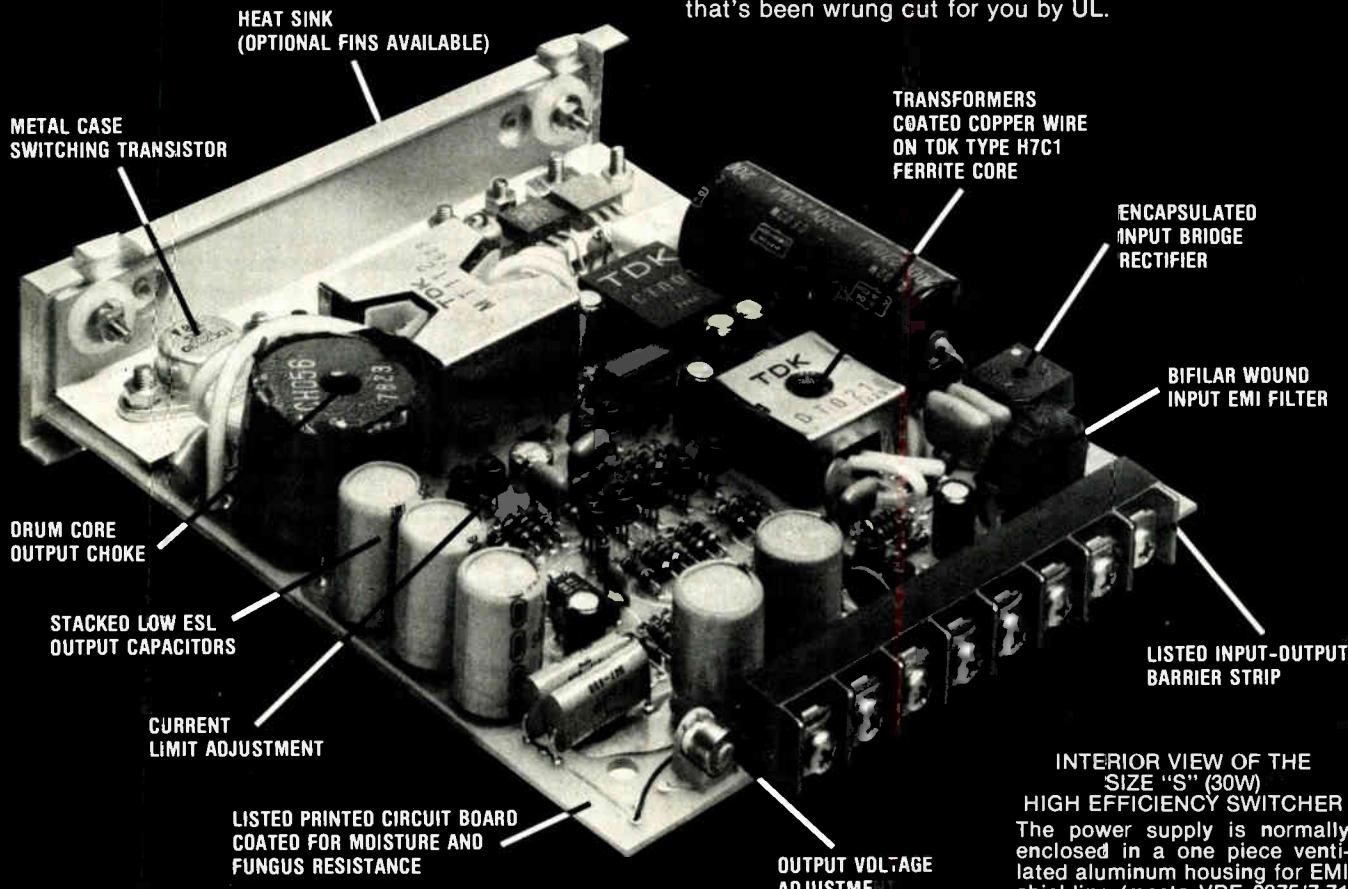
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## Publisher's letter

**R**emember those old movies in which the heroes are songwriters who sit down at the piano and dash off new tunes on the spot? Well, something like that kind of inspiration came over the engineers who developed the 8860A digital multimeter at John Fluke Manufacturing Co., Mountlake Terrace, Wash.

Only this product was not completed on the spot. In this case the first question was, "What would happen if we attached a calculator to a voltmeter?" As with many such brainstorms, the Fluke engineers first tried out the concept on other Fluke engineers. A voltmeter was seemingly linked to a display and to a calculator, and then various company personnel were asked what they would do with such a combination. It turned out that they liked the idea. But the test was not for real—the calculator was not actually hooked up to the voltmeter. Instead, an engineer sitting out of sight fed responses from the keyboard into the display. In any case, Fluke had the kernel of a new product.

Some two years later, after much research with customers, Fluke consummated the marriage of a calculatorlike keyboard with a microprocessor and a 5½-digit multimeter. The cover article on how it was done starts on page 105.

Author Lee Meyer, Fluke's product manager for the General Test and Service division, points out the danger in putting too much weight on inside opinion. "The original idea had so much appeal, it was easy to get carried away. That's why we made a special effort to check out this product with potential users throughout the project," he says.

The other trick in this kind of product development is to pick potential users who will provide frank opinions rather than feed back what they think the company wants to hear. "Sometimes we go overboard on talking to people who are on the negative side," Meyer adds. "The goal is to get objectivity."

tronics conference? Yes, say Roger Allan, components editor, and Jerry Lyman, packaging and production editor, who put together our report on the upcoming Electronic Components Conference (p. 119). They were struck with the wide diversity of technical papers at the ECC.

Roger at first found it difficult to understand how the ECC can attract engineers when, for example, details of a laser-trimming circuit for hybrid components are presented alongside a discussion on the effects of polymer on palladium connector contacts.

The answer came from program chairman George Donaldson, supervisor of the Interconnections division, Sandia National Laboratories, Albuquerque, N. M. "It is because components manufacture, assembly technology, and materials disciplines interact so much with each other that the ECC survives as a conference," he states.

**C**apturing a new product category just as it takes off is one of the objectives of our Product Roundup features. The roundup of color monitors (p. 153) is no exception. In fact, it appears that there are more such devices to come, probably about the time of the National Computer Conference next month.

"The announcements in the last five to six months are only a drop in the bucket compared with what these companies say they have in store," comments Los Angeles bureau manager Larry Waller, who prepared the story. "And, not to be overlooked is the impact of the Japanese competitors on this market," adds Ana Bishop, assistant new products editor, who organized the roundup from the New York office.

The upshot is that the color monitor market has changed under the impetus of small-business computers.

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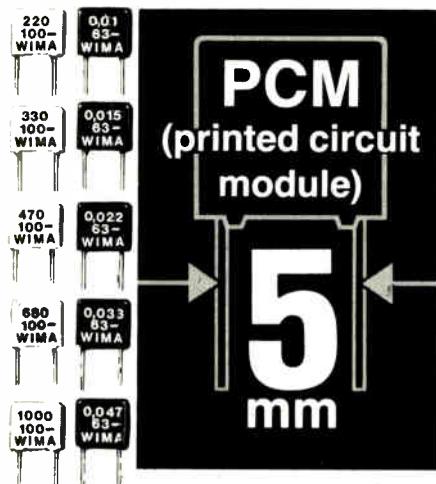
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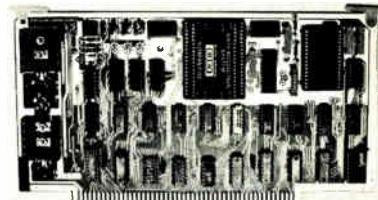
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## Readers' comments

### ABC was first

To the Editor: One of your readers has brought to our attention an item that appeared in your News Briefs column [Jan. 17, p. 48]. It refers to John W. Mauchly as co-inventor of the first electronic digital computer. The item cites page 308 of your April 1946 edition.

The claim of Mauchly and J. Presper Eckert Jr. was negated in a 1973 Federal district court decision. That decision recognized that John V. Atanasoff was the inventor of the first automatic electronic digital computer. He designed and built his computer, the ABC, while he was a member of the faculty at Iowa State University.

James L. Warner  
 Information Service  
 Iowa State University  
 Ames, Iowa

### Bell's baby

To the Editor: "Two-layer resist technique produces submicrometer lines with standard optics" by James B. Brinton [Feb. 14, p. 47] was well written and informative, but it contained a few misstatements that should be corrected.

The material in which the wafer is soaked to make the upper layer photosensitive is a potassium silver cyanide solution, not a potassium silver selenide solution.

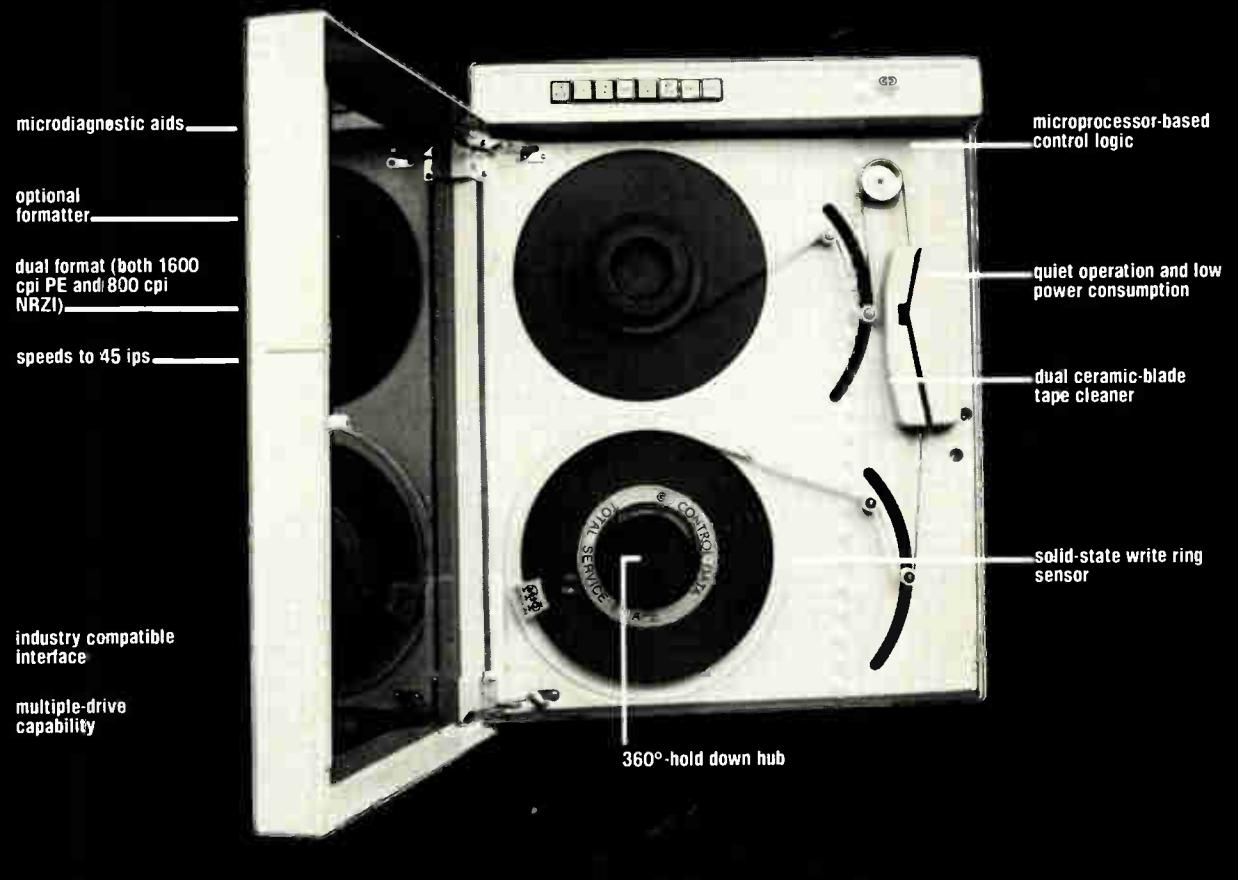
The work described was solely a Bell Labs development and not a joint effort with the Massachusetts Institute of Technology as stated. The student from MIT who coauthored the paper that was delivered by Dr. K. L. Tai at the Conference on Advanced Research in Integrated Circuits did his work at Bell Labs as a summer employee.

Adam Heller  
 Bell Laboratories  
 Murray Hill, N. J.

### Bubbles without TTL

To the Editor: "Bubble offerings start to balloon" [March 13, p. 41] was an excellent review of the growing number of magnetic-bubble memory products now available from various vendors. I would like to call your attention to an oversight,

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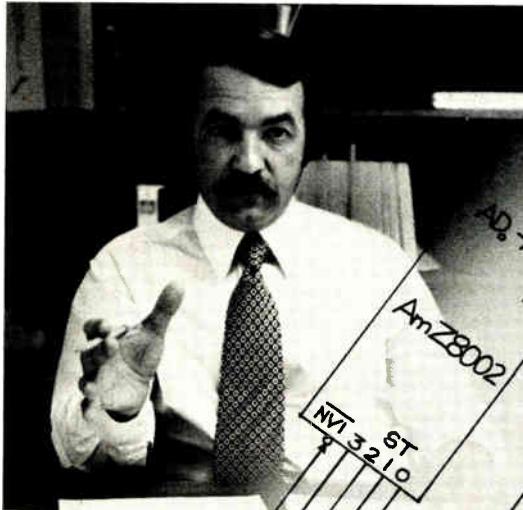
We chose the Z8000 because we believed you'd choose the Z8000. Because it's better. Here's why:

## "The AmZ8000 has a better architecture."

It has 16 registers. All general. All for you. Use them for data or addresses. Use them to write more efficient software with less code and faster execution.

The AmZ8000 has gobs of address space: 8M bytes of direct addressing in each of four possible address spaces. It has memory management with sophisticated relocation and protection features. It has a rich instruction set that operates on data types from quad length words right down to single bits. You can even map the I/O into memory or keep it separate.

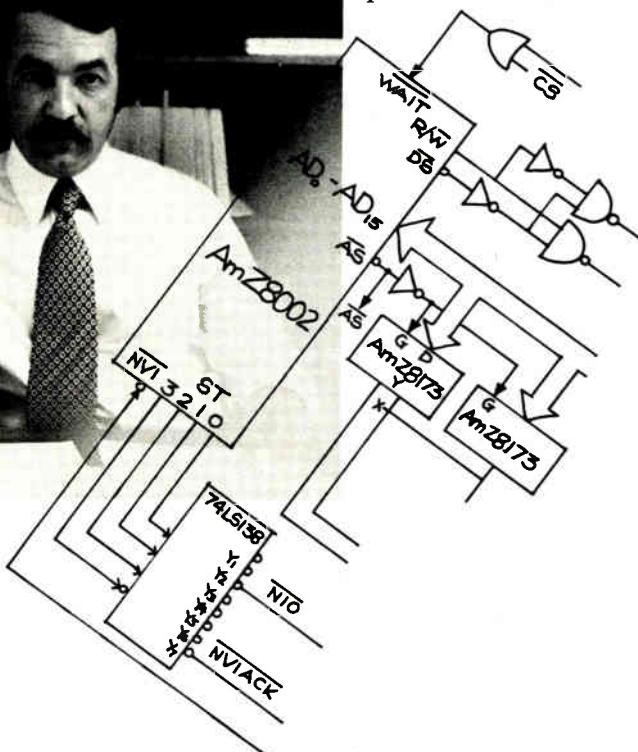
Sven Simonsen, Vice President  
and Technical Director,  
Advanced Micro Devices



As if all that weren't enough, the AmZ8000 has a whole series of string-oriented instructions to move, translate or compare up to 64K bytes of data in a single instruction.

## "The AmZ8000 has a better future."

The AmZ8000's architecture and instructions fit perfectly with today's computation, communications and instrumentation markets. So do the peripherals. And all the popular existing parts for the 8080A/8085A, including the Am9511A and Am9512 floating-point processors and the Am9517A



## "The AmZ8000 is better for your application"

DMA circuit, work great with the AmZ8000.

There's a CPU that's just right for you. For imbedded controllers, where 64K of memory is enough, there's a compact 40-pin CPU that uses less memory for programs. For addressing large memory spaces, there's a 48-pin CPU that's software compatible.

But best of all, we're getting ready to introduce a bunch of new bipolar and MOS peripherals. There's an I/O device with a built-in FIFO, a chained DMA controller, error correction circuits and an editing CRT controller, just to name a few.

As technology develops, newer and better software-compatible CPUs with higher throughput will be coming your way.

## "The AmZ8000 has better support."

We know you need supporting documentation. And we've got it. Ask us for our Data Book, our Processor Interface Manual and our Processor Instruction Manual.

We know you need software development tools. And we've got them, too. There's our macro assembler with powerful high-level constructs and a relocatable linking loader,

and a PASCAL compiler. Cross-software is available, too.

If you need a hardware development system, our AmSYS8/8 with in-circuit emulator was designed just for the AmZ8000. So was our Am96/4016 Evaluation Board. (To learn all about them, come to one of our field seminars or take one of the courses offered by our Education Department.)

And soon, you'll need parts. With the AmZ8000 you've got two major U.S. manufacturers with a mask-exchange agreement. We have international partners, also. When you need parts, we'll be there.

## "The AmZ8000 is better because we're better."

Advanced Micro Devices didn't become the nation's fastest growing IC company by accident. We did it by design. We only manufacture high-quality, high-volume parts. And from the day we opened for business, we've thrown in a freebie with every order: MIL-STD-883.

If you want your application to be better, get the MPU that's better. Get the AmZ8000. It's the best 16-bit family for you.

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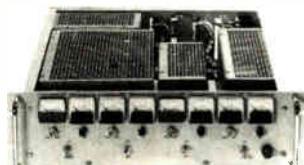
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### Readers' comments

however.

Texas Instruments is in production with custom bubble memory controllers that do not require the inconvenience of TTL implementation. The TIB0901 interfaces with the TIB0203 92-kilobit bubble and has been in high-volume production for two years. The TIB0903 controller is also currently in production and is intended for use with our new TIB1000 1-megabit and TIB0500 half-megabit magnetic-bubble memory.

James L. Allen Jr.  
Texas Instruments Inc.  
Dallas, Texas

### Wishful thinking

To the Editor: We at National appreciate the March 27 article on speech synthesis and our speech processor chip ["A pair of chips synthesizes lifelike speech," p. 39]. However, a major concept needs to be clarified.

Near the end it is stated that original-equipment manufacturers can digitize voices themselves, which is not the case. The code-compression algorithm must be implemented at National for custom vocabularies and then supplied to OEMs in programmable read-only memories or ROMs. This particular coding maximizes recognizability of the voice, making it possible for different products actually to sound like different people.

In addition, the 25,000-quantity price quoted was intended for custom chip set vocabularies and not for standard evaluation kits. Although it would be a tremendous windfall for us, we really don't expect people to buy standard kits in those quantities. The price of the evaluation kit will be in the area of \$150 for single quantities.

Dan Sowin  
National Semiconductor Corp.  
Santa Clara, Calif.

### 1979 Index ready

The index of articles published in Electronics during 1979 is available now. If you are interested in receiving a copy, circle 370 on the reader service card.

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## EXPANDED ZIP DIP® II Socket/Receptacle Series

New Textool models test up to 64 pin 900 mil devices

Textool's expanded ZIP DIP II socket/receptacle series (12 different sizes) now offers new models capable of testing 64 pin 900 mil, 48 pin 600 mil, 42 pin 600 mil, and 28 pin 400 mil devices.

Versatile ZIP DIP II sockets feature an enlarged entry for use with an even wider range of devices and a flat top plate for easier entry and extraction. Contacts are on even 100 mil spacing (300, 400, 600, and 900 mil) for more convenient mounting on standard hardware.

A built-in "stop" insures that the ZIP DIP II handle can't be easily overstressed. Top mounted assembly screws facilitate the replacement of damaged or worn internal parts. Textool has strengthened both hardware and plastic for increased reliability and screw

mounting of the socket to the ZIP DIP II receptacle makes possible a more positive locking system.

The ZIP DIP II receptacle (shown with socket mounted) has all the features of previous ZIP DIP receptacles, yet at a lower price. It virtually eliminates mechanical rejects, is a disposable plug-in unit requiring no soldering and has a typical life of 25,000-50,000 insertions. The receptacle is ideal for high volume hand testing and, since replacement time is eliminated, a test station can process literally millions of devices before it must be replaced.

Detailed information on these and other products from Textool . . . IC, MSI and LSI sockets and carriers, power semiconductor test sockets, and custom versions . . . is available from your nearest Textool sales representative or the factory direct.

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## People

### Defense cash should flow East, says Brownman

Harold L. Brownman is all for having more defense dollars spent in the Northeast. And as president of Lockheed Electronics Co., Plainfield, N.J., he may be in a good position to realize that goal.

Brownman, 56, has been with Lockheed Missiles & Space Co. since January 1977, when he joined after working for three years as the assistant secretary of the Army for installations and logistics. He came east to the electronics arm of the aircraft company last year, with ideas of bringing some of the Government's defense spending from the West Coast.

"Companies are blossoming in defense and nondefense areas on the West Coast. The center of gravity in this industry has gone to California because of the large aircraft companies," he notes. "We have got to fight to bring that center of gravity back here."

As a native New Yorker, Brownman is well aware of how important a role New York-area companies played in establishing the early electronics industries. "The New York metropolitan area was really the hub of the electronics business," he reminisces. "We have to be competitive in terms of personnel, policies, compensation, and fringe benefits to get the people back."

Brownman sees two positive aspects of the East Coast, by comparison with the West—lower housing costs, and the wide variety of engineering schools in the New York area. Brownman himself received an undergraduate degree in electrical engineering from the Polytechnic Institute of Brooklyn in 1944 and a masters in 1949.

Brownman is positioning Lockheed Electronics to take advantage of increased government spending. His New Jersey company has been noted mainly for its radar, fire control, and air-traffic control systems. And although Brownman is steering it toward new lines of business for future growth, he is still unsure of



**Defense pie.** Lockheed's Brownman intends to share in increased defense outlays.

exactly what these will be.

"LEC's strength is, in the main, in the military marketplace, and I plan to continue to focus on that marketplace." He adds, "I am not particularly enamored with the industrial and commercial marketplaces for LEC."

### Ravenal sees portability as key to future software

"With people switching microprocessors on the order of once a year, they are going to be forced to protect their software with portability," declares Bruce Ravenal, president of Language Resources Inc. of Sunnyvale, Calif. Ravenal, a co-designer of both Intel Corp.'s 8086 16-bit microprocessor and its 8087 math processor, carried this conviction with him both into and out of Intel.

For achieving that portability, the Pascal language is an excellent vehicle, he believes, and he has therefore become cochairman of the American National Standards Institute and Institute of Electrical and Electronic Engineers' joint ANSI/X3J9-IEEE Pascal standards committee. Its goal is an any-host, any-microprocessor compiler using standard Pascal—a seemingly impossible task, but as a weekend mountain climber, Ravenal is used to attaining lofty goals.

Ravenal owes his convictions on portability to his professor at the University of Colorado, William Waite, who is now also a vice president of Language Resources. When

# PDP11/23 ARRAY PROCESSOR SYSTEM



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AP-1

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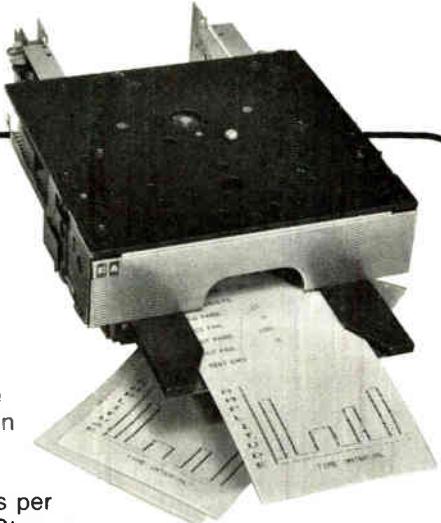
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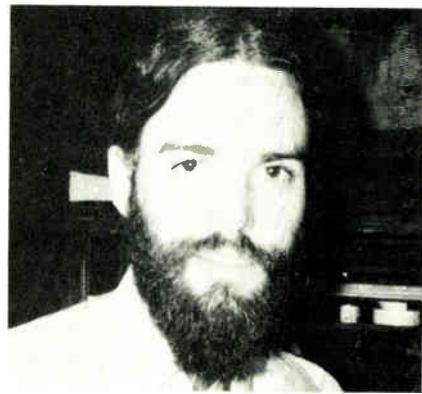
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16 Circle 103 on reader service card

## People



**Right word.** Language Resource's Ravelan thinks Pascal is ideal for portability.

Ravelan left Intel to design a Pascal language compiler [Electronics, March 27, p. 185], he assembled a combined Intel and University of Colorado team that included Steven Morse, the principal architect of the 8086; Dean Schulz, the project leader for the first compiler for ANSI's 1977 version of Fortran; and Waite.

What the group created was a compiler that could directly generate source code for 8080, 8085, 8086, and 8088 microprocessors, along with coprocessors such as the 8087 and 8089. Moreover, they designed the compiler so that it could be run on a number of host systems, including the Control Data Cyber, VAX, and Intel MDS/ISIS II. "We call this retargeting—for microprocessors—and rehosting—for the host computing systems," notes Ravelan. "The key: development of algorithms independent of the microprocessor."

Language Resources had an unusual origin in that its first customers provided the necessary seed money in mid-1978. They drew up contracts with the fledgling firm solely on the basis of its founders' reputations. Their faith proved well-founded, for the company booked \$500,000 in 1979 and expects to double that figure in 1980.

As his company grows, Ravelan is becoming more concerned with quality than sales volume. "As I see it, an emerging software company has two choices," he explains. "It can either aim to become a major software house, or it can be a tightly run small company. I would prefer our company to be the latter." □



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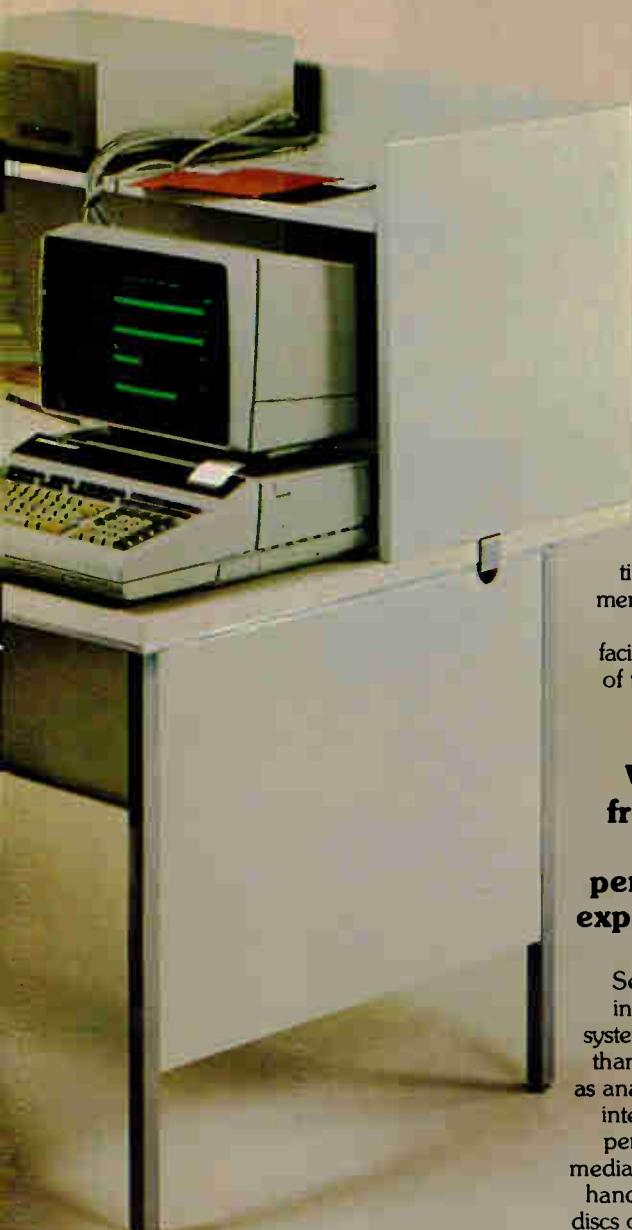
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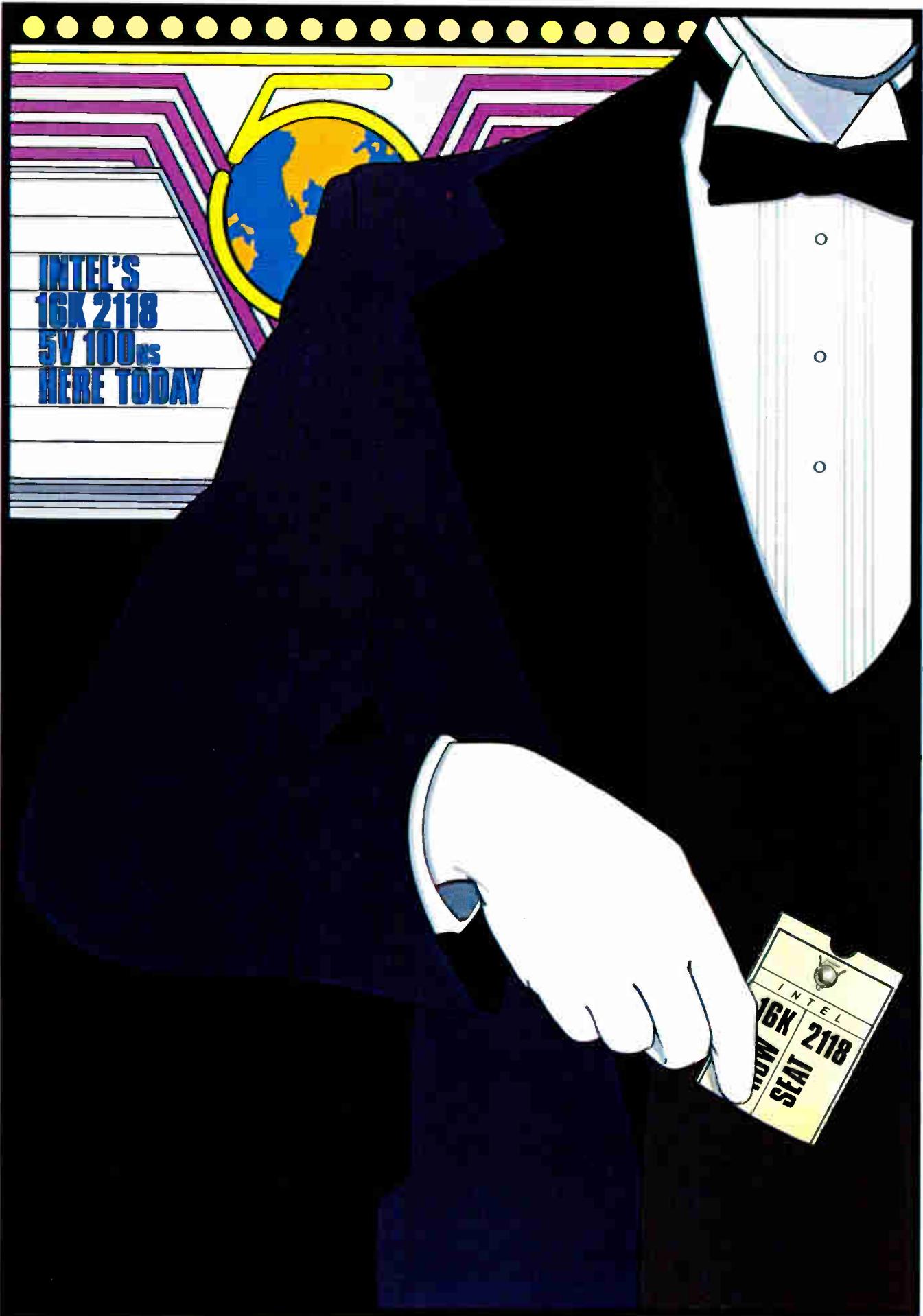
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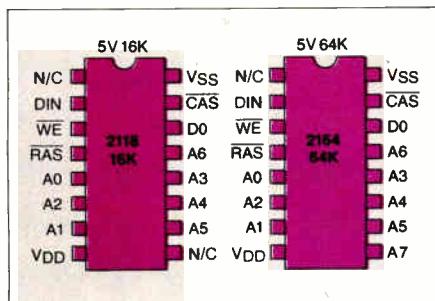
Intel's HMOS is the high performance technology that has revolutionized the semiconductor industry, combining improved scaling, speed, power and density with reliability and producibility. We've already delivered over 18 million leading edge HMOS

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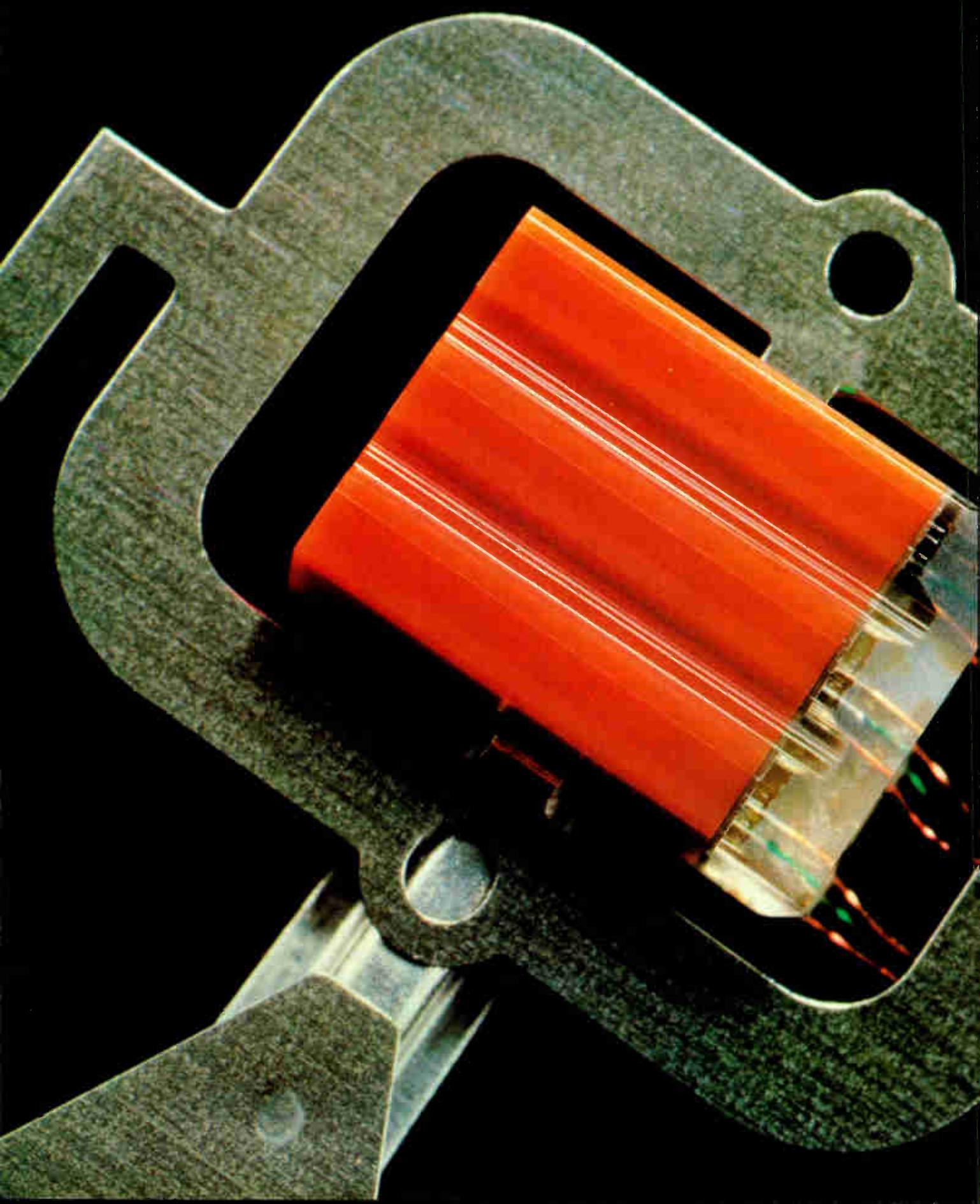


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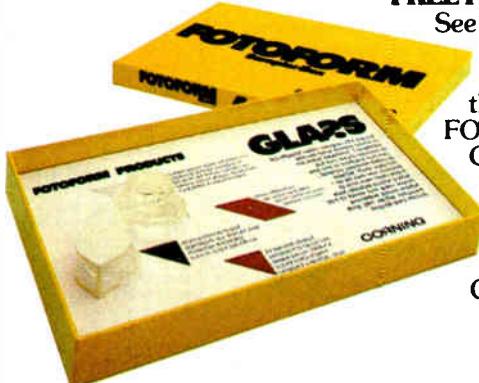
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# CORNING

*Actual size of the FOTOCERAM slider is less than a quarter inch in length. It is a critical part of a complete thin film head assembly made by Applied Magnetics, Goleta, Calif.*

## Outshining the teacher?

It was a strange happening indeed. The Japanese electronics companies had come to tell the Americans about quality control (p. 81). And on hand were Americans to confirm that the Japanese electronics companies practice what they preach, for the results are borne out in the high quality of their semiconductor components, consumer products, and computers.

What has happened? Are the Japanese, as one of their adages goes, "outshining the teacher"? The electronics industries in Japan started from scratch in the 1950s to establish quality control programs learned from the U. S. With typical Japanese zeal, they made quality control a way of life from top to bottom. It took time, but the decision to follow the long path has paid off. No longer does the world view the "Made in Japan" label with disdain.

The Japanese have drawn a distinction between what they see as the American view of quality control, which is to test, test, test, and throw out the failures. In their approach, the objective is to eliminate the failures by doing it right and then eliminate the tests. The ultimate objective is to use quality control to increase productivity.

But the most striking aspect of the quality control seminar put on by the Electronic Industries Association of Japan (EIA-J) is that the quality control movement on the island nation started at the top and trickled down to the individual workers. The message was that the same could be done in the United States. But because of the differences between the two cultures, many Americans might be sceptical.

Americans might well ask if the quality control function is the responsibility of a top manager, who sees to the company's total commitment. Quality control is one of those

motherhood topics that every company supports, but U. S. companies may not be able to match the Japanese in their all-out commitment.

In addition, the gulf between workers and management, between white collar and blue collar, is a factor in the United States. To some degree this adversary relationship is a hindrance to quality control, but not an insurmountable one. After all, the quality circle concept in which the Japanese take such pride started in America. This concept has workers, supervisors, and managers all working on solving quality problems in a cooperative effort. There are those who say that the American worker no longer has the drive or the incentive to participate in a quality circle. But some companies have successfully resurrected the idea. Others can do the same.

Along this line, J. M. Juran, the world-renowned expert in quality control, made an interesting observation following the Japanese QC seminar. He suggested that when American managers visit Japan to see at first hand how the Japanese run quality control programs, they should take along representatives of their work force with the goal of opening their eyes to what the American industry is up against.

Perhaps it does not require a trip to Japan for U. S. companies to make the effort to bring the work force in on the competitive pressures. It would not be too difficult to mount an information program not only to explain the need to meet the competitive challenge from overseas, but to challenge the worker to match the Japanese performance.

It is now high time to get back on the track of increasing productivity. Maybe then Americans will again be able to outshine their former students.



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The various OE units are divided into groups by frequency and by temperature stability. Models OE-20 and OE-30 are temperature compensated units. The listed "Overall Accuracy" includes room temperature or 25°C tolerance and may be considered a maximum value rather than nominal.



All OE units are designed for 9.5 to 15 volts dc operation. The OE-20 and OE-30 require a regulated source to maintain the listed tolerance with input supply less than 12 vdc.

Prices listed include oscillator and crystal. For the plug-in type add the suffix "P" after the OE number; eg OE-1P.

OE-1, 5 and 10 can be supplied to operate at 5 vdc with reduced rf output. Specify 5 vdc. when ordering.

Output — 10 dbm min. All oscillators over 66 MHz do not have frequency adjust trimmers.

Catalog	Oscillator Element Type	2000 KHz to 56 MHz	57 MHz to 139 MHz	140 MHz to 160 MHz	Overall Accuracy	25°C Tolerance
035213	OE-1	\$15.66				
035214	OE-1		\$17.99			
035215	OE-1			\$22.63	± .01% -30° to +60°C	± .005%
035216	OE-5	\$19.44				
035217	OE-5		\$22.91			
035218	OE-5			\$30.17	± .002% -10° to +60°C	± .0005% 2 - 66MHz ± .001% 67 to 139 MHz ± .0025% 140 to 160 MHz
Catalog Number	Oscillator Element Type	4000 KHz to 20000 KHz		Overall Accuracy	25°C Tolerance	
035219	OE-10	\$22.91		± .0005% -10° to +60°C	Zero trimmer	
035220	OE-20	\$33.65		± .0005% -30° to +60°C	Zero trimmer	
035221	OE-30	\$69.63		± .0002% -30° to +60°C	Zero trimmer	



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## Meetings

**Hanover International Fair, German Trade Fair and Exposition Corp. (D-3000 Hanover 82, Messegelände, West Germany), Hanover Fairgrounds, April 16-24.**

**18th International Magnetics Conference (Intermag), Magnetics Society of the IEEE, Sheraton-Boston Hotel, Boston, April 21-24.**

**29th Annual Conference and Exposition, National Micrographics Association (8719 Colesville Rd., Silver Spring, Md. 20910), New York Coliseum, New York, April 21-25.**

**International Conference on the Electronic Office, Institute of Electrical and Radio Engineers (99 Gower St., London WC1E 6AZ, England), Penta Hotel, London, April 22-25.**

**Electro-Optical Warfare III, Cabrillo Crow Coven and Naval Ocean Systems Center (Dr. P. C. Fletcher, NOSC, Code 015, San Diego, Calif. 92152), NOSC, April 23-25.**

**International Aerospace Exhibition, German Trade Fair and Exposition Corp. (D-3000 Hanover 82, Messegelände, West Germany), Hanover Airport, April 24-May 1.**

**Federal Data Processing Exposition, The Interface Group (160 Speen St., Framingham, Mass. 01701), Sheraton-Washington Hotel, Washington, D. C., April 28-30.**

**International Radar Conference, IEEE, Stouffer's National Center Hotel, Arlington, Va., April 28-30.**

**International Symposium on Circuits and Systems, IEEE, Shamrock Hilton Hotel, Houston, April 28-30.**

**28th Annual National Relay Conference, The National Association of Relay Manufacturers (D. D. Lingelbach, Oklahoma State University, 202 Engineering South, Stillwater, Okla. 74074), Oklahoma State University, Stillwater, April 28-30.**

**30th Annual Electronic Components**

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in individual character.*

—W.E. Channing



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## Meetings

**Conference, IEEE et al.**, Hyatt Regency Hotel, San Francisco, April 28-30.

**Second International Parametrics Conference**, International Society of Parametric Analysis (P. O. Box 3104, Dayton, Ohio 45431), Sheraton Poste Inn, Cherry Hill, N.J., April 29-May 1.

**Electronic Distribution Show and Conference**, Electronic Industry Show Corp. (222 S. Riverside Plaza, Chicago, Ill. 60606) Las Vegas Hilton Hotel, Las Vegas, May 1-3.

**Video '80—Congress and Exhibition on Video Systems**, AMK GmbH (D-1000, Berlin, Messedamm 22), Berlin Fairgrounds, May 5-7.

**World Electronics—Strategies for Success**, Financial Times Conferences (10 Cannon St., London, England) and Mackintosh International, Loews Monte Carlo Hotel, Monte Carlo, May 5-7.

**26th International Instrumentation Symposium**, Instrument Society of America (A. E. Bowman, Hy-Cal Engineering, 12105 Los Nietos Road, Santa Fe Springs, Calif. 90670), Red Lion Inn/Seatac Hotel, Seattle, Wash., May 5-8.

**International Symposium on Computer Architecture**, IEEE, La Boule, France, May 6-8.

**15th Annual Microwave Power Symposium**, International Microwave Power Institute (211 E. 43rd St., New York, N.Y. 10017), University of Iowa, Iowa City, May 6-9.

**Microwave Power Tube Conference**, Advisory Group on Electron Devices and Electron Devices Society of the IEEE, Naval Postgraduate School, Monterey, Calif., May 12-14.

**Electro/80**, IEEE, Hynes Memorial Auditorium, Boston, May 13-15.

**Custom Integrated Circuits Conference**, IEEE, Americana Hotel, Rochester, N.Y., May 19-21.

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*Ed Shortridge, Chief Engineer.*

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# ByteWyde options start with 8K static RAMs.

## Mostek calls it the 4118.

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The 4118 is also as fast as it is reliable. Access time is a scant 120ns (max.). Plus, it's available now, in quantity. At prices that are already cost-competitive with previous generation static RAMs.

Military versions of the 4118 are screened to MIL-STD 883B with access times of 150ns, 200ns and 250ns. And all three are guaranteed to operate over the full military temperature range of -55°C to +125°C.

## It's a BYTEWYDE™ memory.

The 1K x 8 4118 is a member of Mostek's BYTEWYDE family of compatible RAMs,

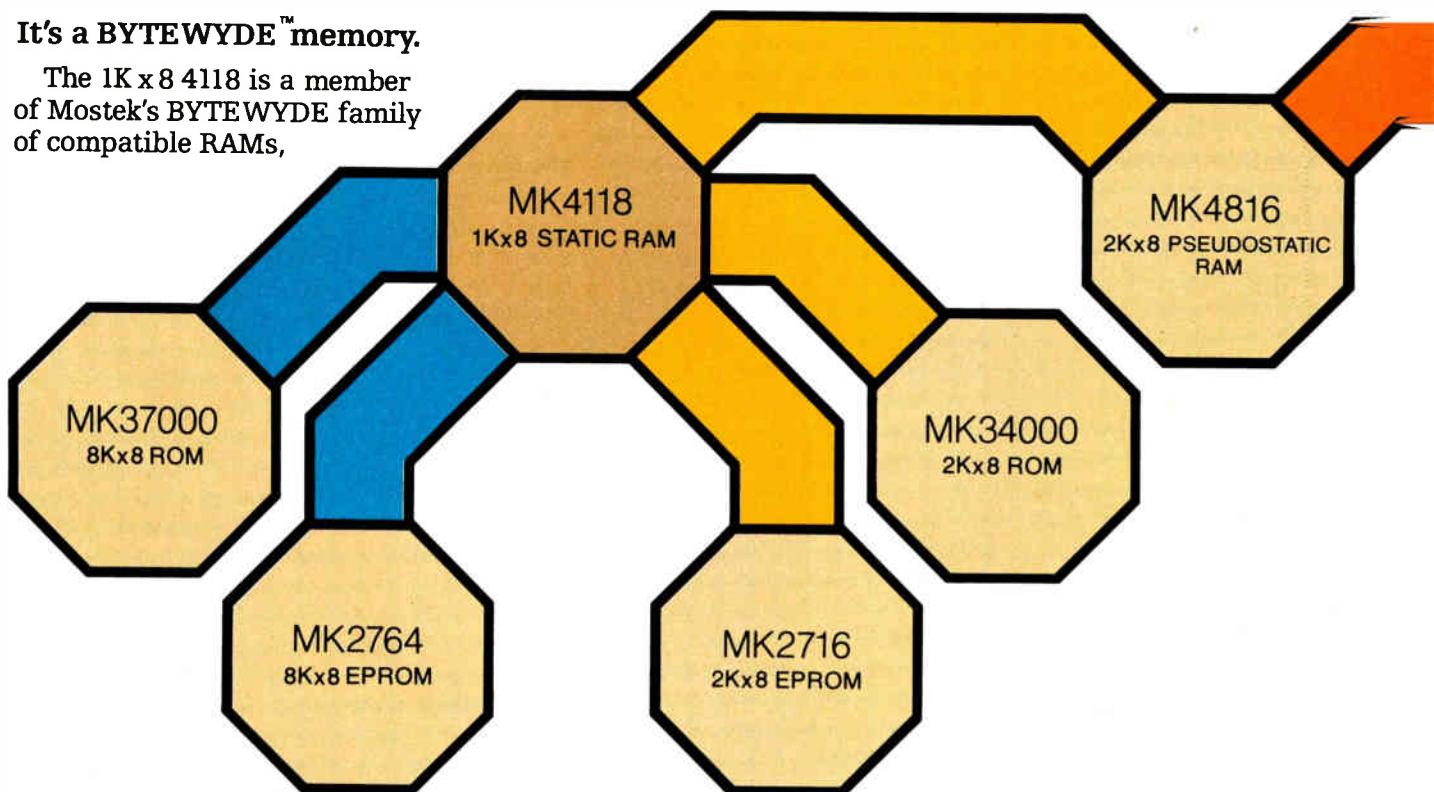
ROMs and EPROMs. These memories have a common pinout, so you can interchange all three types. And upgrade to next generation memories as well. Without redesign.

The coordinated design path concept of BYTWEYDE memories gives you flexibility, upgradeability and compatibility never before available. Consistent n-words x 8-bit organization makes these memories ideal for 8-bit and 16-bit microprocessor applications. By using them in building-block fashion, the design of a custom memory array is as easy as selecting and plugging in the circuits you need.

## Compatible with ROMs and EPROMs.

The 4118 is housed in a 24-pin package and designed to fit a 28-pin P.C. board socket so you can interchange it with present and next generation ROMs and EPROMs. Including the widely accepted 2716 EPROM. That, in itself, opens up dramatic new opportunities for compact microprocessor memory.

To explain: At design time, the exact ratio of ROM/EPROM vs. RAM is rarely known. Also, changes in that ratio frequently occur during the product life. Without common pinout, you need to layout 2 matrices of



sockets (1 for ROM/EPROM and 1 for RAM) to accommodate any change in the ratio. That wastes real estate. With a common pinout, however, you only need 1 matrix of 28-pin sockets. That reduces space and headaches.

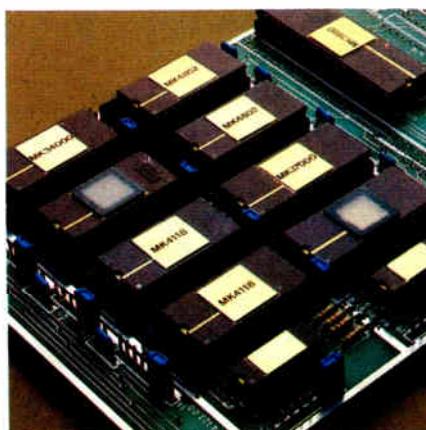
### Compatible with next generation RAMs.

The coordinated packaging philosophy of the 4118 applies to density upgrades as well. In fact, with the 28-pin socket layout, upgrades to 32K x 8 can be made without redesign. Consequently, you can take advantage of technology advancements to increase density. And reduce cost without redesign.

**MK4802**  
2Kx8 STATIC RAM

### Compatible with microprocessors.

Like other BYTEWYDE memories, the 4118 interfaces directly with all present and future generation microprocessors. An Output Enable control provides easy user control of the bus in all bus configurations. Two selection control functions (Chip Enable and Output Enable)



are consistently provided for all BYTEWYDE memories to avoid bus contention problems.

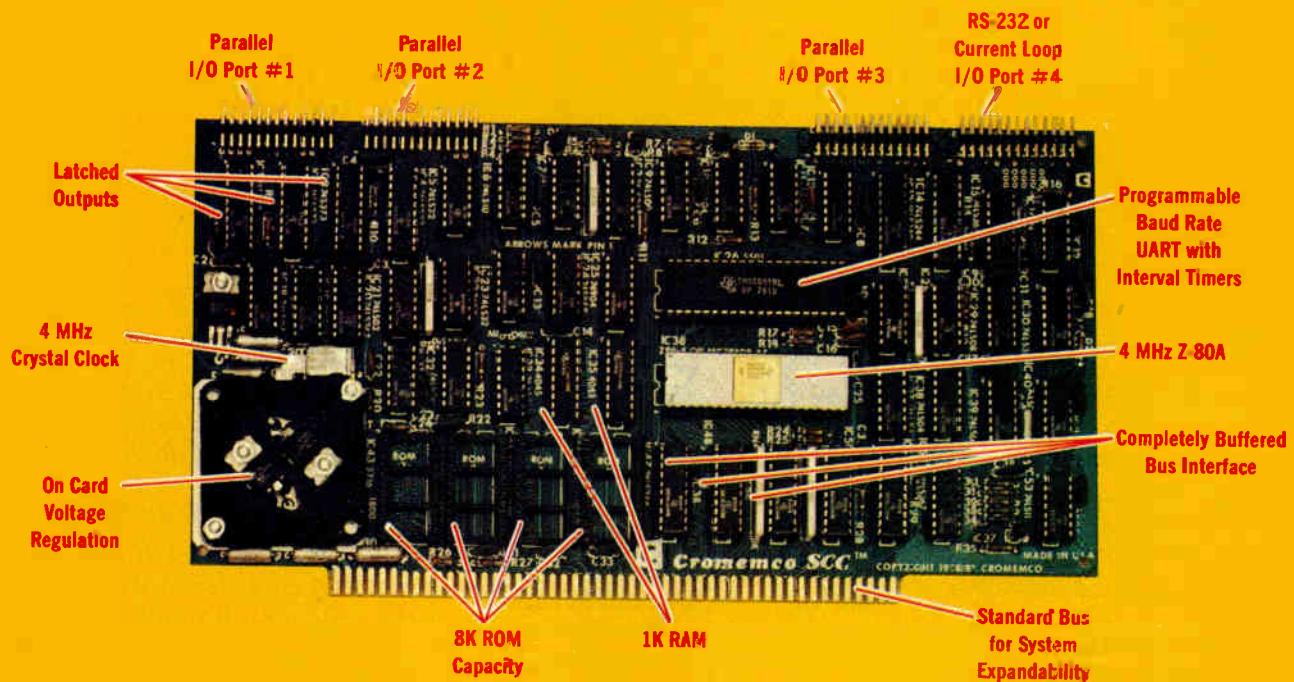
### Give yourself a choice.

Before you select your next memory components, consider the design path implications associated with them. Can they be interchanged with other types? Or upgraded through several generations without redesign? If not, you owe it to your design to evaluate Mostek's BYTEWYDE memories. To find out more, call or write: Mostek, 1215 W. Crosby Rd., Carrollton, Texas 75006, (214) 323-6000. In Europe, contact Mostek Brussels at 660.69.24.

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BYTEWYDE™ FAMILY PINOUTS

4118 4801	4802	34000	2716	4816	37000	2764	2764	37000	4816	2716	34000	4802	4118 4801						
				RFSH	NC	NC													
A7	A7	A7	A7	A7	A7	A7	1 2 3(1) 4(2) 5(3) 6(4) 7(5) 8(6) 9(7) 10(8) 11(9) 12(10) 13(11) 14(12)	(24)26 (23)25 (22)24 (21)23 (20)22 (19)21 (18)20 (17)19 (16)18 (15)17 (14)16 (13)15	28 27 (24)26 (23)25 (22)24 (21)23 (20)22 (19)21 (18)20 (17)19 (16)18 (15)17 (14)16 (13)15	VCC	VCC	VCC	NC	NC	CS	VCC	VCC	VCC	VCC
A6	A6	A6	A6	A6	A6	A6				A8	A8	A8	A8	A8					
A5	A5	A5	A5	A5	A5	A5				A9	A9	A9	A9	A9					
A4	A4	A4	A4	A4	A4	A4				A11	A11	NC	VPP	NC					
A3	A3	A3	A3	A3	A3	A3				OE/VPP	OE	OE	OE	OE					
A2	A2	A2	A2	A2	A2	A2				A10	A10	A10	A10	A10					
A1	A1	A1	A1	A1	A1	A1				CE	CE	CE	CE	CE					
A0	A0	A0	A0	A0	A0	A0				D7	D7	D7	D7	D7					
D0	D0	D0	D0	D0	D0	D0				D6	D6	D6	D6	D6					
D1	D1	D1	D1	D1	D1	D1				D5	D5	D5	D5	D5					
D2	D2	D2	D2	D2	D2	D2				D4	D4	D4	D4	D4					
VSS	VSS	VSS	VSS	VSS	VSS	VSS				D3	D3	D3	D3	D3					



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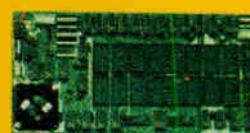
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# Electronics newsletter

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## TI to provide speech technology to its customers

Now that National Semiconductor Corp. has announced plans to begin selling speech-synthesis chip sets to original-equipment manufacturers [*Electronics*, March 27, p. 39], look for Texas Instruments Inc. to make the technology behind its speech synthesis available to outside customers as well. Expected soon from the Dallas firm is a package that may include a **second-generation, microprocessor-compatible speech-synthesis chip**. Like its predecessor, which was first employed as part of a three-chip set in TI's Speak & Spell learning aid [*Electronics*, June 22, 1978, p. 39], the new chip will be fabricated in p-MOS and will work with a linear predictive coding technique. TI is believed to be setting up its regional technology center in Chicago to provide customer support for vocabulary development and for writing linear predictive code to be housed in standard erasable programmable read-only memory. Pending availability of the new chip, customers may begin work with the already available TM990/306 speech-synthesis module [*Electronics*, Nov. 8, 1979, p. 44].

## Chip reduces number of devices for floppy control

Western Digital Corp. has come up with a chip that promises to reduce to four the number needed to control a floppy disk. A dozen or more discrete random logic devices must be used now. The Newport Beach, Calif., semiconductor specialty house says its WD 1691 performs **data-separation and write precompensation with its phase-locked-loop logic** and sells for \$16 when ordered by the hundred. To make up an entire floppy-disk control, the 1691 is linked to one of Western Digital's 1790 family of controllers and a model 2143 clock, along with an external voltage control. The company is also providing kits with three of the four parts for \$60.

## New Dataphone service proposed by AT&T for remote monitoring

A new national data-communications service for discrete polling of more than 16,000 remote unattended terminals from a master station using private lines is being proposed by American Telephone & Telegraph Co. In a Federal Communications Commission filing, AT&T says its Dataphone Select-a-Service employs **voice-grade channels for monitoring and managing systems for alarm and security, fire control, gas and oil pipelines, and power distribution**. DSAS has a "new-speed solid-state switch" at each site, AT&T says, to limit noise buildup and simplify fault isolation and correction without system shutdown—a problem in existing systems. The proposal to offer DSAS nationally on June 19 stems from the expanding market and resultant need to link the intrastate DSAS services covered by tariffs on file in 37 states.

## U. S. rules urged for TV broadcasting from satellite to home

The Federal Communications Commission got another spur this month to grapple with the issues of satellite-to-home TV transmission from two internal studies projecting a worldwide boom in that market over the next decade. Though the technology for using high-power direct-broadcast satellites (DBS) for beaming TV signals to small, low-cost home antennas is at hand, the reports' 275 pages note, the FCC must address **spectrum allocation, as well as potentially controversial economic and legal regulatory issues**. Among them: whether to leave DBS operations to the marketplace (with its potential for equipment incompatibility); whether to regulate DBS as a broadcasting or common carrier service—or as a hybrid of the two—or as a "private radio" service; and whether standards should be set up for signal-coding and -decoding devices.

# Electronics newsletter

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## **ADM-3A terminal to learn to recognize voice**

The ubiquitous ADM-3A dumb terminal from Lear Siegler Inc.'s Data Products division in Anaheim, Calif., is about to be given a breath of new life—and some intelligence. At next month's National Computer Conference in Anaheim, the ADM-3A will be shown with a new speech-recognition unit that permits an operator to give data or commands accurately to a computer or auxiliary peripherals without using hands or maintaining eye contact with the terminal's display.

Manufactured by Heuristics Inc. of Sunnyvale, Calif., the voice-recognition unit, which includes a Z80 8-bit microprocessor, 32 kilobytes of random-access memory, and up to 8 kilobytes of read-only memory, allows the user to talk into the terminal's noise-canceling microphone instead of typing certain functions on its keyboard. Meanwhile, Heuristics plans to make available a self-contained version of the voice recognizer, designated the 7000 voice controller, which will accept words and phrases up to 3 seconds in length—twice the acceptance rate of other such systems. Targeted at commercial and industrial markets, it will sell for \$3,000.

## **Intel to preview 64-K E-PROM for major customers**

Intel Corp. is about to distribute samples of its 2764 64-K ultraviolet-light-erasable programmable read-only memory to certain major accounts. However, the Santa Clara, Calif., firm still plans to begin general distribution of samples of the 64-K E-PROM in June and to ship production quantities in the fourth quarter of this year. Meanwhile, in the wake of slashing prices in February by as much as 60% on its 2732A and 2732A 32-L E-PROMS, Intel now plans a further reduction on the order of 25% to 30% for the 32-K devices.

## **Shugart doubles capacity of its fixed-disk drive**

Responding to the demands of systems designers for memory peripherals with more capacity and better performance, in low-cost, compact packages, Xerox Corp.'s Shugart Associates subsidiary will introduce a 58-megabyte 14-in. Winchester fixed-disk drive at next month's National Computer Conference in Anaheim, Calif. The new SA4100, with double the capacity of the Sunnyvale, Calif., firm's existing 29-megabyte SA4008 drive [*Electronics*, Sept. 12, p. 34] will list for about \$2,800 in large quantities. With an additional two disks and eight heads, the new drive retains the same compact size as the SA4000 series, mounting in a standard 19-in. rack And using 5.25 in. of panel space. Its recording density is 5,534 bits/in., with a track density of 172 tracks/in. It is expected to be available in the fourth quarter of this year.

## **Zilog proceeds with plans for terminal system**

Exxon Enterprises' establishment of Summit Systems in Cupertino, Calif., as a maker of office equipment [*Electronics*, March 13, p. 34] has not changed Zilog Inc.'s plans to intensify its microcomputer systems business. Summit was spun out of Zilog, which is another Exxon enterprise. The basis of this new systems effort, a multiterminal system dubbed the MCZ-2, is expected to be unveiled later this month. Besides more attractive packaging intended to make it easier for original-equipment manufacturers to integrate the device into business systems, the system reportedly has the hooks for enhancements, including a multitasking operating system and a networking scheme that will support multiprocessor configurations.

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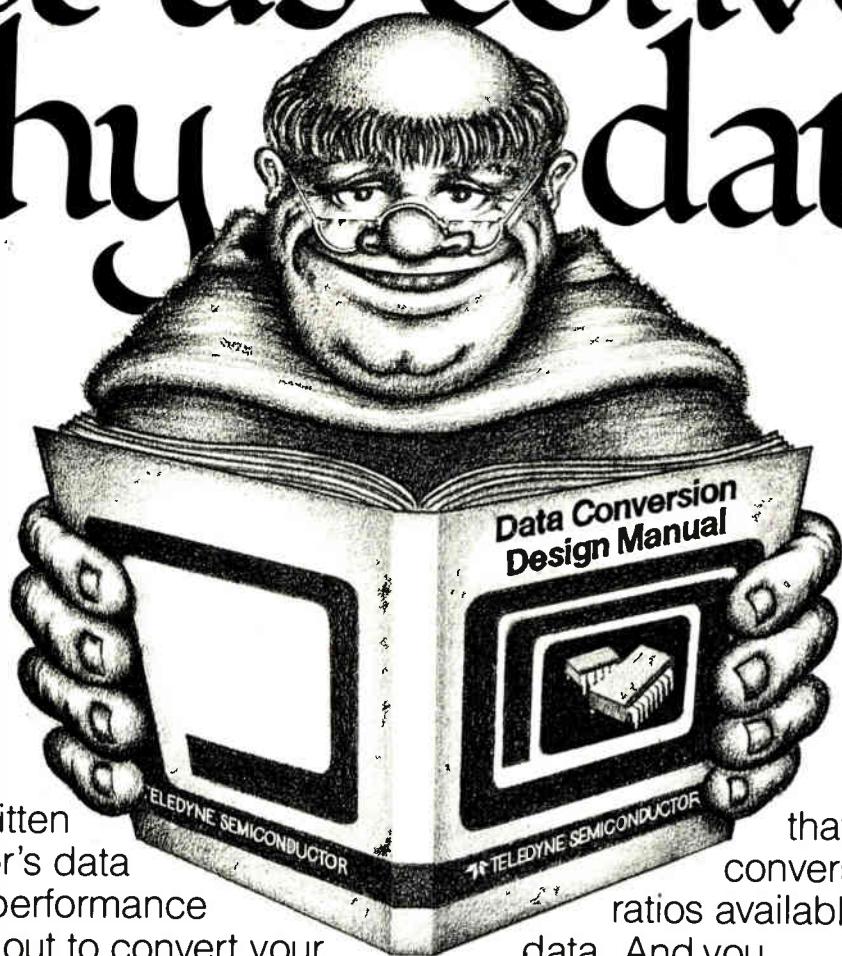
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# Fluorescent display alters drive method for high resolution

by Roger Allan, Components Editor

New technique avoids shadow effect that requires too wide a dot spacing for effective graphics

A Japanese display maker has devised an innovation in vacuum fluorescent technology that may open the door to high-resolution graphics and perhaps even video applications. Ise Electronics Corp. reports it has solved the problem of interference between adjacent elements that precluded resolution high enough for anything more complex than alphanumericics and simple graphics.

Engineers from the Ise, Japan, company will describe their development at this year's Society for Information Display meeting, in San Diego, April 28-May 1. They have constructed a matrix of 26 by 258 0.4-

millimeter-square zinc-oxide dots 0.25 mm apart, giving a viewing area of 16.55 by 167.35 mm. The dots are fluorescing anodes in what is the equivalent of a triode tube.

Vacuum fluorescent displays continue to attract researchers because they combine low cost with high brightness, low power distribution, and multiple colors. Unfortunately, they also fall prey to what is known as the shadow effect: a current strong enough to drive a dot brightly will illuminate adjacent dots by electron scattering, turning on these adjacent anodes partially or fully while leaving dim corners in the dot that is supposed to be illuminated.

**Separation.** The solution has been to separate the elements, which is fine for limited-character alphanumeric displays but little else. Thus, the typical pitch, or center-to-center-distance between dots, has been 1 mm; in the Ise prototype display,

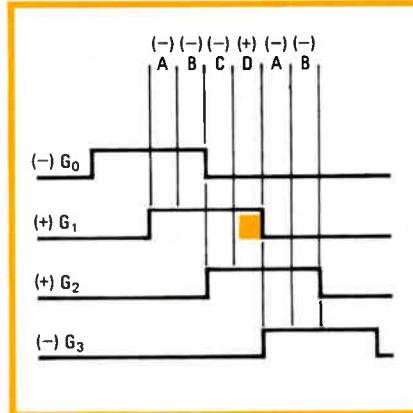
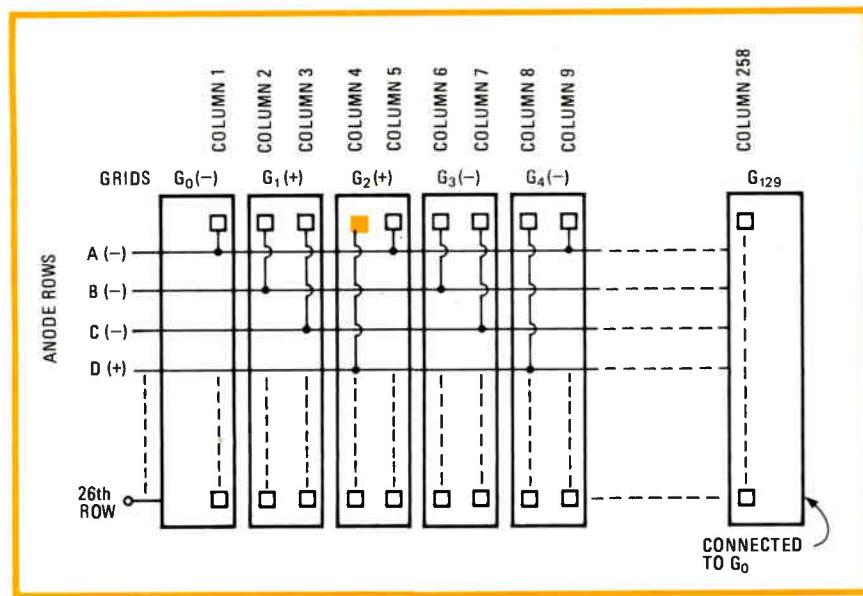
however, the pitch is 0.65 mm.

As described by Kazuhiko Kasano and his team members, the Ise innovation is the drive technique. Conventionally, alternate dots are tied and driven together, but the new drive ties together every fifth dot. Each grid covers and controls two columns of dots (see figure).

To turn on a dot, its grid and the adjacent one are driven with a positive voltage. In the conventional technique, the adjacent grid remains negative, repelling electrons from the positive grid and thus causing the shadow effect.

An essential element in the new technique is to use the anode voltage to control the fluorescing. Thus only the anode row line controlling the dot to be illuminated is given a positive potential. The combined potentials cause the dot to fluoresce.

Although driving the display this way increases the pin count, inter-



**Different matrix.** The troublesome shadow effect in high-density vacuum fluorescent displays is eliminated with this drive method. The display has 26 rows (anodes) by 258 columns (grids). Overlapping drive pulses (above) turn on only one anode (left).

connections, and drive voltages, it also maximizes the output brightness level—the researchers report a 210-foot-lambert brightness and a luminous efficiency of 5.2 lumens per watt. Moreover, they point out that the voltages of 70 V peak-to-peak for the anodes and 7.6 V for the filament

are much lower than those in plasma or electroluminescent displays.

The display uses conventional vacuum fluorescent techniques except for thin-film interconnections, rather than thick-film, on the back panel. An 8-bit microprocessor provides the driving intelligence.

### Computers

## Chips detect and correct errors in disk drives and main memories

In recent months, semiconductor makers have introduced a variety of special-purpose chips that extend their offerings to computer makers well beyond the traditional solid-state memories. One of the obvious functions for dedicated integrated circuits is error detection and correction, and American Micro Devices Inc. is jumping in with two new IC's, one for hard-disk drives and one for microprocessor-based systems.

The high recording densities of new disk drives increase the probability of errors during data recovery, so burst-error-detection and -correction schemes are growing more pop-

ular. But such schemes can take as many as 50 to 80 ICs to implement.

The new n-channel MOS AmZ8065 burst-error processor, unveiled at the recent International Electronic Components Exhibition in Paris, is a single-chip solution. It can detect and correct 12-bit burst errors in serial data streams at data rates up to 20 million bits/second [Electronics, March 27, p. 33].

**Four codes.** According to Krishna Rallapalli, manager of MOS microprocessor operations for the Sunnyvale, Calif., company, the 8065 can handle four common multiple-error-correcting codes called Fire codes

after their inventor, William Fire. These polynomials include the mainframe-standard 48- and 56-bit codes popularized by IBM, as well as the minicomputer 32- and 35-bit versions, and "cover over 80 percent of all applications for burst-error processing," Rallapalli claims.

The new chips join peripheral-control ICs for such functions as control of cathode-ray-tube displays and floppy-disk drives. But instead of serving as components in microprocessor-based subsystems, the new AMD parts are aimed at larger, more sophisticated systems—including main memories (see "Correcting another error type").

**Math.** The 8065 divides a section of the data stream by the selected polynomial and the resulting check code is then appended to the data stream. With the 32-bit code, there is an 11-bit error burst in a 42,987-bit sector of the disk; the 56-bit code can detect and correct an 11-bit error burst in a 585,442-bit sector.

When the data stream is read back, the IC again performs the data-stream division for data validation. Matching check codes indicate no errors, but if an error is detected the 8065 can extract the burst-error pattern, locate it in the data stream, and then correct the errors.

"There can be any number of bits in error as long as the distance between the first and the last error is 12 or fewer bits," Rallapalli says. This is the burst error common to disk drives, he explains.

**Correction.** If the 8065 detects an error, it has two methods of correction available. These are the full-period clock-around and Chinese remainder theorems.

The first is most often used in the industry because it requires less hardware to implement. It is a brute-force method, Rallapalli says, and takes almost as long as the transfer of data from the disk in the first place. For example, the 32-bit code requires nearly 43,000 clock periods.

With no sacrifice in accuracy, Rallapalli notes, the user can select the high-speed correction method based on the Chinese remainder theorem, which computes the error

### Correcting another error type

As microprocessor-based systems develop the power to address ever larger chunks of main memory, keeping them error-free becomes more important. Thus Advanced Micro Devices Inc. has developed a single chip that performs error-correction and -detection on 16-bit-long data fields.

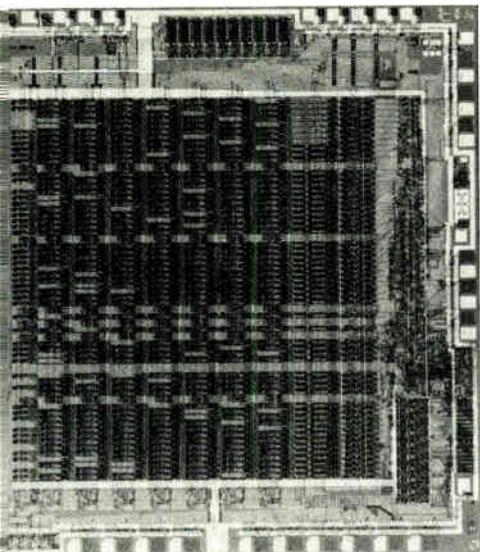
The new 2960 is the first in a series of memory management parts that the Sunnyvale, Calif., company plans as companions to its popular 2900 bit-slice-processor family. It also can be used with other microprocessors.

Using a modified Hamming code, the 2960 can generate 6 check bits for a 16-bit data field. By examining those check-bit errors, it can later correct single-bit errors and detect double-bit errors. Several of the parts can be cascaded to handle 32- or 64-bit data fields. To aid systems diagnostics, the bits associated with an error are accessible.

Warren K. Miller, one of the chip's designers, says one of its biggest advantages is that it does a function "that normally requires 20 to 30 chips." He is introducing the 2960 in a paper at next month's Electro/80 in Boston.

To speed operation, the IC is fabricated in emitter-coupled logic with TTL-compatible inputs and outputs. Although other details are not yet available, samples are scheduled to be available by the end of June with volume shipments late in the third quarter, a company spokesman says.

To ease design of main memory subsystems, AMD is introducing several other parts as well. Due in the next few months are the 2961 and 2962 bus buffers, the 2965 and 2966 memory drivers and the 2964 dynamic memory controller, which itself will replace another 10 to 15 chips. -Anthony Durniak



**Error corrector.** AMI's AmZ8065 serves as one-chip burst-error detector and corrector in hard-disk drives. It can handle four multiple-error-correcting binary codes.

location and the correction needed. In the case of the 56-bit Fire code, this technique "lowers the worst-case time for a correction from over 500,000 clock periods to a maximum of 111 clock periods," he says.

Available in June in sample quantities, and in the third quarter at \$69 each in 100-piece quantities, the AmZ8065 is characterized to work with the Z8000 16-bit microprocessor as a drive controller. It will also be available as a general-purpose device: the Am9520, characterized for operation with just about any microprocessor.

-Bruce LeBoss

### Solid state

## Platinum IR sensor has uniform response

A new solid-state infrared sensor may mean far cheaper, lighter cameras able to produce instantaneous images for a wider range of applications. The key is a focal-plane chip bearing platinum-silicide Schottky-barrier photodiodes sensitive well into the IR range.

The major benefit of the chip is the uniformity of its sensing-junction response. All junctions produce the

same current out for a given input, unlike other solid-state sensing arrays, and thus eliminate computer processing of output signals to recover accurate images.

**Discovery.** This characteristic uniformity first turned up in photo-response measurements on silicide diodes being developed for high-speed switching applications at the Rome Air Development Center, Hanscom Air Force Base, Bedford, Mass. Researchers noted that heating the metalized silicon substrate dissolved oxides and other impurities out of the silicon and into the metal, where they could not affect the uniformity of the junctions. These diodes were nickel, but platinum reaches further into the IR range.

In applying silicide diodes to infrared sending systems, RADC had RCA Corp.'s integrated-circuit technology research laboratory in Princeton, N.J., integrate charge-coupled-device circuitry into a design with signal processing and transfer on a single chip. The result [Electronics, March 27, p. 33] is a quarter-inch-square focal-plane chip bearing 1,250 junctions in a matrix.

Horizontal and vertical CCD registers separate the junctions. As the junctions activate, they discharge current to an adjacent CCD circuit for transfer by clock-controlled pulses to a video amplifier.

**Simple.** The process is little more complicated than that used in commercial CCD-based 35-millimeter cameras, says Freeman D. Shepherd, RADC's branch chief for electronics development technology. Like most infrared systems, however, devices using the chip will still require refrigeration to 95 Kelvin to eliminate extraneous, temperature-related current, he adds.

Shepherd foresees little fundamental difficulty in increasing the number of photodiodes on a chip to achieve image resolutions comparable to those of current IR cameras. "Right now we're getting mosaiklike images, but eventually we should have pictures as good as any you see on a television screen," he says. Both RADC and RCA's Automated Systems division in Burlington, Mass.,

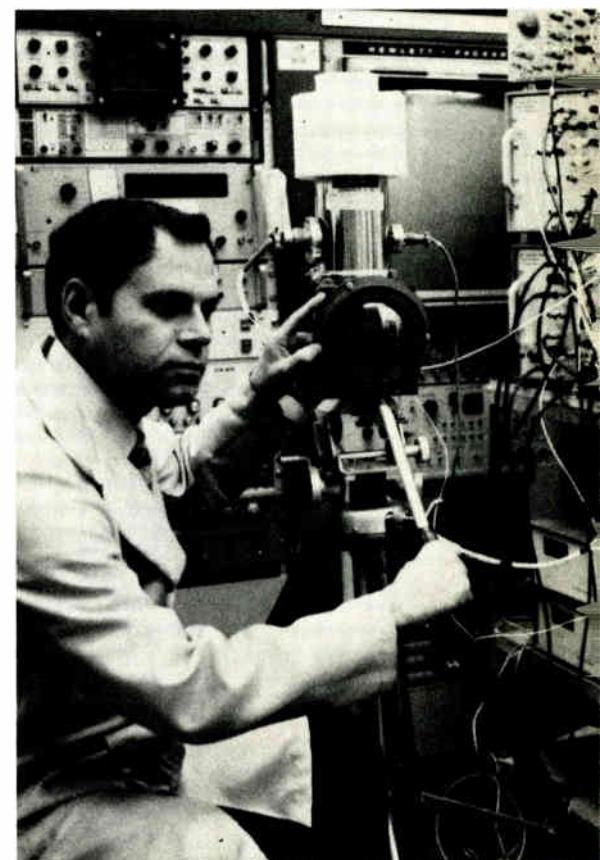
have put the chip in cameras (see photograph).

Eliminating the need for computer post-processing of sensor signals will be a major factor cutting IR systems' costs. A military-grade IR sensor system now costs as much as \$100,000; those using the chip could cost 90% less, weigh about 75% less, and consume only a quarter of the power. They should offer similar advantages over the alternative approach to IR cameras, which requires a bulky, expensive scanning mirror.

**Uses.** Commercial and medical systems also should see dramatic savings, Shepherd says. All this will mean wider applications for IR-sensing devices.

Military uses could include nighttime intrusion surveillance, and RADC and RCA are working on an advanced sensor for that. The chip also might be used to detect hot

**Smile.** USAF physicist Lyn Skolnik tests camera using a new IR sensor chip with uniform platinum-silicide Schottky barrier diodes needing no computer processing.



spots in integrated circuits, signifying faulty connections. Medical uses could include scanning for tumors and circulatory problems by detecting hotter tissue.

-Linda Lowe

### Design automation

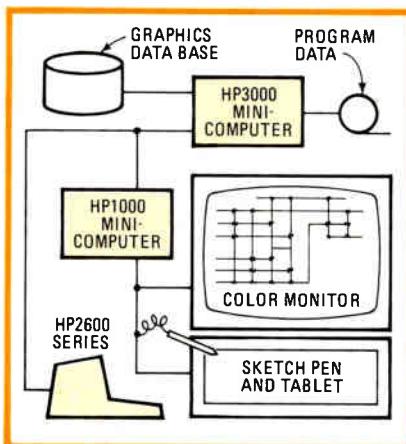
## CAD unit does more for chip designers

Taking computer-aided design a step further, Hewlett-Packard Co. has devised a CAD system for integrated circuits that lets designers do a simple sketch of the desired layout using a light pen and color graphics. The system interprets the sketch's symbols as circuit elements and the colors as masking levels and makes design-rule adjustments: the result is pattern data for a computerized mask maker.

HP calls its system Sticks because it takes over the design task at the stage of the topological (stick) diagram—and its speed and accuracy are deemed essential for the densely packed circuitry of the future. "It results in a cost reduction on the order of 2:1 to 10:1," depending on circuit characteristics and the skills of the designer being replaced, says Sam Boles, Sticks project manager at HP's General Systems division, Cupertino, Calif.

**Random logic.** The new CAD system is the first any company has been willing to discuss that automates this time-consuming portion of random-logic design. IBM Corp. has a system for gate-array master-slice chips that can be applied to both the basic chip design and the interconnections layout at an earlier stage in the design process [*Electronics*, May 24, 1979, p. 129], but it is not applicable to random logic.

Boles notes that the concept of synthesizing pattern-generation data from a simple topological diagram "has knocked around the industry for some time." Apparently no company except HP has been willing to invest the time and money it needs. As well as speeding the design process and making designers' lives



**Super CAD.** Hewlett-Packard has devised a computer-aided design system that lets EE's use a light pen and sophisticated symbology to sketch chip layouts.

easier, it can help alleviate the shortage of qualified designers, he notes.

The considerable difference between the HP development and commercially available CAD systems is in the level of symbology. The commercial systems have libraries of circuit elements, which the designer calls up via a keyboard, taking into account some 60 or 70 design rules in making a layout. Sticks automatically synthesizes the layout from line and point symbols in the topological sketch.

The system is in prototype, with first delivery to a division operation expected this fall. There are no plans to market it, since CAD advances tend to be as jealously guarded secrets as process improvements.

**Others.** However, IC houses and other original-equipment makers with solid-state capabilities are also active in the advanced CAD area. Among them are Rockwell International Corp., Motorola Inc.'s Austin, Texas, MOS division, and American Microsystems Inc.

System elements (see figure) are standard hardware, with the exception of the prototype color monitor. The key to Sticks is, of course, its software, and HP plans a massive development effort to extend the system's capability back to the circuit-schematic stage and ultimately to the logic-design stage. Also, Sticks now works only with HP's complementary-MOS on sapphire process.

Boles says software already developed includes a crude form of automatic spacing of circuit elements for the maximum density permitted by a process and a check for basic electrical errors. It will be compatible with what is called the silicon complier being developed at the California Institute of Technology [*Electronics*, Jan. 3, p. 40].

Rockwell International's Microelectronic Devices division in Anaheim, Calif., uses an advanced CAD system with color graphics and design-rule software that relies on the more traditional grid approach with a keyboard. Designers can more easily make circuit changes and optimize density than with Sticks, says Frank Micheletti, director of silicon devices technology.

At AMI in Santa Clara, Calif., designers use a keyboard-based system with color graphics that flashes when a design rule is violated. But it does not automatically lay out the chip according to the design rules.

However, it is likely that such companies on the forefront of IC technology will look at systems similar to Sticks. Warren H. Weimann, CAD manager for Motorola's MOS division, notes that the HP system is based on a graduate thesis in the public domain.

Motorola, for one, is looking at the concept, which Weimann says does offer big speed advantages. On the other hand, it can now perform a density squeeze in only one direction at a time, which does not give as dense a circuit as a designer can achieve, he notes.

-Bruce LeBoss

### Business

## Manufacturing gear is growth market . . .

Beyond the looming recession, a boom market awaits makers of semiconductor manufacturing equipment and their customers. That is the view of two industry experts—Michael Kraska, vice president of Merrill Lynch, Pierce, Fenner & Smith Inc., and Gunther Rudenberg, senior staff

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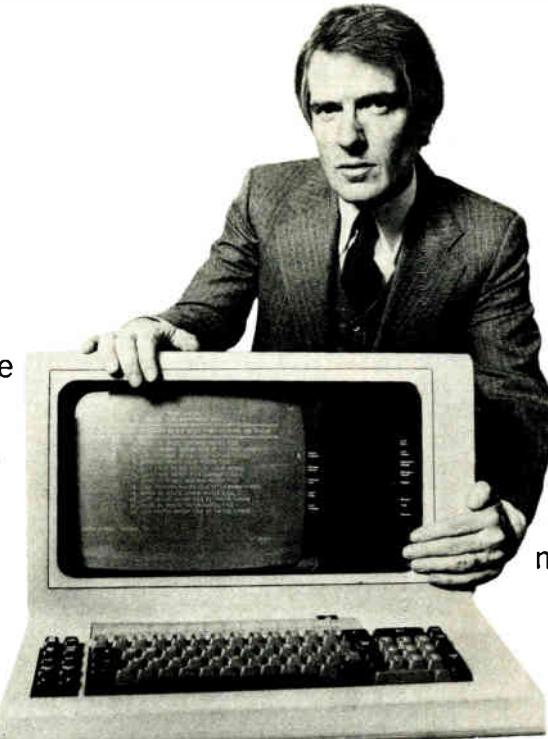
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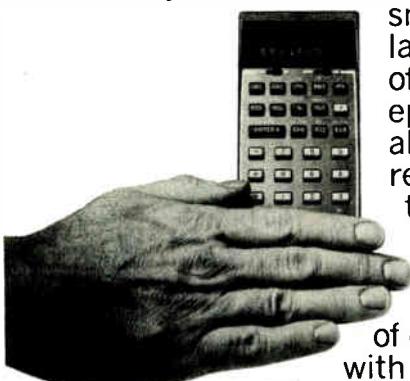
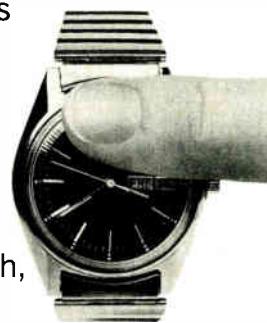


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### Second video disk player bows

Come June, U. S. consumers in a couple of cities will have a choice between two laser-based video disk players. Produced by Universal Pioneer Corp. (a Japanese amalgam of Pioneer Electronic Corp. of Japan, MCA Inc., and IBM Corp.), the VP-1000 will join the year-old video disk player marketed by the Magnavox unit of NV Philips. An MCA affiliate is already making disks that can play on either system. For \$749, consumers will be able to buy the VP-1000 in four cities, including Minneapolis-St. Paul and Dallas-Fort Worth. The \$775 Magnavision is now available in eight cities, including the Minneapolis and Dallas markets.

Pioneer's entry should buttress the laser-pickup approach in the forthcoming marketing clash with RCA Corp.'s capacitance-pickup, groove-guided systems scheduled to appear in early 1981 [*Electronics*, March 13, p. 48]. MCA has been marketing an industrial version of the Pioneer machine for about a year. Like Magnavision, the VP-1000 has forward, reverse, and variable fast- and slow-motion operations, and it alone permits random access by frame number. Both machines have freeze-frame and frame-at-a-time functions with disks that run for less than an hour.

Stereophonic sound is a feature of both machines, and Pioneer has a pulse-code-modulated output to accommodate a future electronics package for decoding digital sound signals once a standard for digital recording is established. A new subunit, Pioneer Artists, will supply disks, concentrating on stereo music performances. MCA is completing construction of a new disk manufacturing plant to supply the growing market, estimated at 100,000 units this year and 4 million in 1985 by Argus Research Corp.

At least one Japanese component supplier is betting on those estimates: Olympus Optical Co., Tokyo, is marketing a pickup for optical players. Pioneer says it is testing the Olympus pickup.

-Gil Bassak

member of Arthur D. Little Inc.

The New York-based Krasko predicts that the era of very large-scale integration will act as catalyst for a jump in the manufacturing equipment growth rate to between 15% and 20% a year—the average annual growth rate for the five years ending in 1978 was 12%. A billion dollar industry in 1979, it will double by 1985 in Krasko's view—if semiconductor producers weather the recession undamaged and can increase net profits enough to buy the expensive new equipment outright or pay off debts incurred in the purchase.

**Bullish.** Even on the recession, he is bullish, feeling that semiconductor businesses are well positioned to weather the next six months of uncertain business and foreseeing no repeat of the "Crash of '74." He also sees recent industry moves to increase profit margins as help in generating the capital needed for the capital expenditures that will in turn boost productivity—as does ADL's Rudenberg (see following story).

Krasko sees average profit margins increasing in the upswing cer-

tain to follow the recession. First the industry is exploiting its technology more effectively than in the past, and secondly, it is facing a growing demand for its products. Therefore he predicts an annual market of about four billion semiconductors of all types in five years, a threefold increase over his present estimate.

For Krasko's optimistic projections to materialize, U. S. makers of semiconductor manufacturing equipment will have to stress the price-performance ratio of their new products, he says. Failure to do so, he thinks, could divert customers to European and Japanese firms.

### . . . chip makers to shrug off recession

In Cambridge, Mass., H. Gunther Rudenberg backs Krasko's projections as he takes a detailed look at the worldwide semiconductor industry in a new ADL impact study. In fact, he expects only a temporary decline in the historic industry

growth rate of around 30% annually.

Despite the acknowledged need for higher industry profits, he says the constant-dollar price of semiconductors will continue to drop, though inflation may boost the actual price tags. He optimistically predicts a 1985 cost per function of 0.05¢ (see figure, p. 44).

Rudenberg says that industry capital expenditures have been on the upswing for at least three years and should continue up, even though the cost of capital equipment is itself rising. Fortunately, he notes, the expensive new equipment also is more productive, making it possible for semiconductor houses to continue to reduce constant-dollar prices.

The move to VLSI will not demand immediate replacement of optical lithographic systems, he feels. Instead he sees retrofit kits enabling many of today's masking systems to stay on line into the mid-1980s. He departs here from Krasko, who anticipates a quicker move into electron-beam and X-ray lithography.

Even with retrofits keeping a partial lid on, industry capital investment needs will be high. Ten years ago, he says, a firm had to invest about 50¢ in capital equipment to earn \$1 in sales. Today, he sees the figure as 75¢ and climbing.

**Recession.** But recessions hurt, and like Krasko, Rudenberg expects one, if only in the first half of 1980. He estimates that the delivery growth rate of semiconductor devices will be halved by this year's recession, but that it could rebound as soon as the third or fourth quarters of 1980.

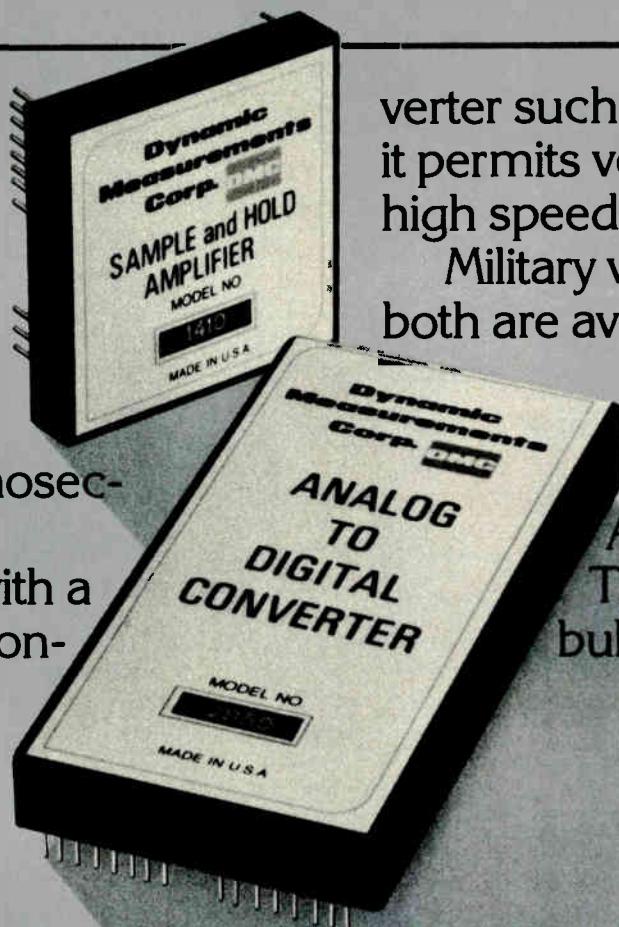
Such a development would mean a decline from a 30% growth rate to one of about 15%, followed by a return. Increased defense spending could drive growth well above 30% per year, he adds.

The markets are there and growing also. The electronic office (which he expects to account for half the semiconductor sales in the 1980s), telecommunications, and the consumer markets will be growing at from 12% to 30% yearly. The automotive market is simply growing too rapidly to call, he says. Finally,

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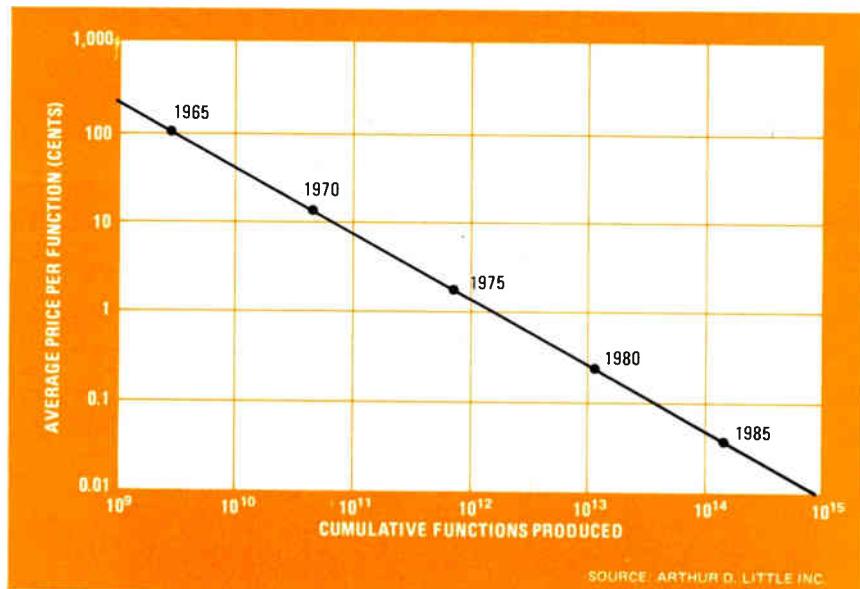
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**Dropping costs.** The history of the long-term growth of the world semiconductor industry suggests that the average price per function will continue to drop even if unit prices rise.

Rudenberg expects the electrical equipment industry to include increasingly large proportions of semiconductor equipment in their new designs. Semiconductors already account for about 8% of the average cost of electronic test and other

equipment, and he expects this to grow to 10% in the latter 1980s. The instrument field is itself a fast-growing market, a factor which will be bound to compound growth in this sector of the semiconductor business, he says.

-James B. Brinton

### Consumer

## Canada promoting video information system with advanced software capabilities

Another contender is surfacing in the burgeoning field of video information systems. Sponsored by the Canadian government and various system and hardware suppliers in that country, Telidon could offer flexible transmission capabilities, easy-to-use color graphics, and considerable interactivity.

**Competition.** The technique is beginning field trials in Canada, and its promoters are trying to drum up U.S. interest. It is in competition with two other basic types of video information systems, both also using TV sets as displays: viewdata, which uses telephone lines as a transmission medium, and teletext, which sends its data over the vertical blanking lines of standard television broadcasts.

A microprocessor and special software give the Telidon user's terminal its capabilities. Its sponsors make the point that it can use practically any transmission system, including satellites. "The terminal is almost entirely independent of the transmission mode and the data base," says a spokesman for the Canadian Department of Communications.

Data-base size is one of the major differences between the interactive viewdata systems, which permit users to become part of several networks, and the teletext systems, which essentially let users call up pages of prepared information. As well as being adaptable to either type of use, Telidon could let one user communicate with another directly if additional software and

memory capacity is provided.

Considerable effort went into the graphics capability—in fact, the entire system grew out of research by the Communication Department's Image Communications Laboratory into communication of graphic images. Image resolution of the system is 200 vertical and 256 horizontal picture elements, with double that possible with expanded video-picture memory. The color palette is eight grey shades and eight basic colors.

**Graphics.** Users can build pictures from basic geometric shapes, instead of working with the coordinates of a grid pattern. The program that permits this is one subset of the software; other subsets can be added to create images and speedily manipulate, recreate, rotate, scale, or transpose in almost any way virtually any portion of an image.

Its sponsors say Telidon could be used as a home computer, for electronic mail, and for similar applications. They say both the software and hardware are designed for adaptability to improvements in computer, transmission, data-base management, and display technologies. The terminal now costs over \$1,000, but very large-scale integrated circuits should slash its cost by more than half, they say.

Field tests across Canada will involve cable, telephone, dedicated-wire-pair, and optical-fiber transmission. Sponsored by phone companies, cable-TV companies and educational into mid-1981, according to government officials.

-Gil Bassak and Ben Mason

### Solid state

## ECL array shrinks to drop power loss

Coming later this year from Motorola Inc.'s Semiconductor group is a scaled-down version of its emitter-coupled-logic Macrocell array that, at 2 watts, dissipates only half the power. Thus the new Miniarray, with 24 major cells as against the larger version's 48, should appeal to

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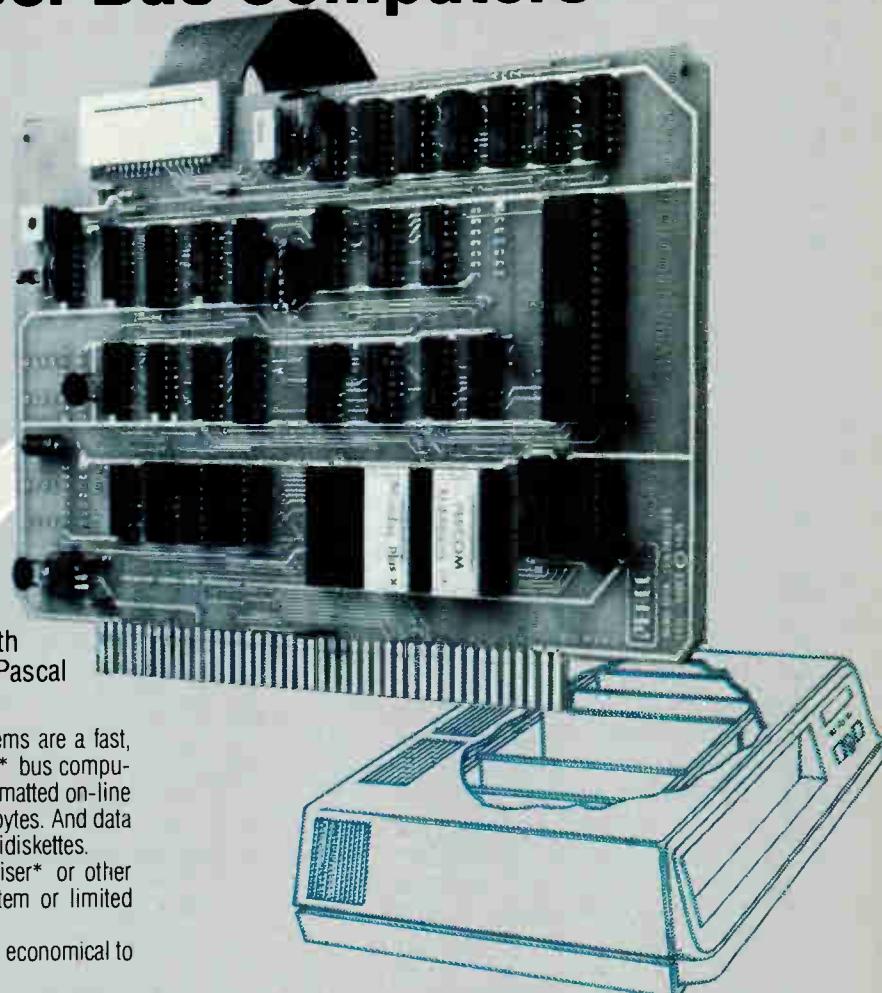
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the like of makers of computer peripherals and telecommunications and signal-processing gear.

The 4-w typical power dissipation for the Macrocell is no problem for mainframe computer builders who want ECL's speed and can cool their equipment relatively painlessly. "But there are a lot of guys out there that 4-w blows away," says James Miele, manager of business planning and tactical marketing for the Phoenix, Ariz., bipolar Integrated Circuits division. "Our studies show they need the speed, but not that density or that kind of power."

**Cooler.** Hence Miniarray, which can be kept in the ambient temperature range with a heat sink and airflow cooling of 500 linear feet per minute: the Macrocell needs 1,000 lin ft/min. Although the smaller array is still a paper product, potential users are showing some interest.

Macrocell differs from other ECL gate arrays in being split into functional blocks rather than individual gates [*Electronics*, Feb. 15, 1979, p. 113], allowing a simpler metalization layer for the interconnection that adapts the array to a specific logic function. However, the Miniarray is not just a Macrocell chopped in two, even though the bipolar process is identical, says Jerry Prioste, system engineer on the project.

Rather, the 24 major cells, plus interfacing and output circuitry, are in a new layout that lets the chip fit into a 40-pin package, in place of Macrocell's 68-pin package. Motorola thinks the smaller package size will fit better in Miniarray's potential applications.

**Real estate.** The miniarray is on a 33,000-square-mil die, against Macrocell's 55,000-mil<sup>2</sup> area. Its 24 cells equal 652 equivalent ECL gates if full adders and latches are implemented, or 904 with flip-flops and latches.

Potential speed is the same as the bigger version: 0.9- to 1.3-nanosecond propagation delay for cells connected as simple gates. Output cells can drive a 25- to 50-ohm transmission line.

Though it is possible to design almost anything with the highly flex-

## News briefs

### Amdahl acquires a firm, seeks a merger

IBM-compatible mainframe maker Amdahl Corp., Sunnyvale, Calif., is on the move to bolster its competitive position. The company and IBM-compatible peripheral maker Storage Technology Corp., Louisville, Colo., have signed a letter of intent to merge. At the same time Amdahl is acquiring Tran Telecommunications Corp., Marina Del Rey, Calif., a producer of digital-communications networks with 1979 revenues of about \$22 million. Tran is expected to operate as an Amdahl subsidiary, if stockholders of the privately owned company approve the acquisition.

### Better software wins cruise contract for Boeing

Boeing Aerospace Co.'s better software for the AGM-86B air-launched Cruise missile proved a key element in the Air Force selection late last month of the Seattle company as prime contractor in the competition against General Dynamics Corp. Boeing's software linking the missile's flight controls with McDonnell Douglas Corp.'s electronic navigation system known as Tercom—for terrain contour matching [*Electronics*, July 21, 1977, p. 69]—was superior to the software designed for General Dynamics by McDonnell, according to Air Force Secretary Hans Mark. Tercom permits cruise missiles to fly terrain-hugging patterns at altitudes of 200 to 600 feet and avoid detection by enemy ground radars. The five-year production program calls for 225 missiles and should be worth some \$4 billion to Boeing, McDonnell Douglas Astronautics Co., St. Louis, and subcontractors. General Dynamics is not out in the cold, however; the St. Louis company already has production contracts for the Navy and Army versions.

### IEEE 1, Feerst 0

It looks as if Irwin Feerst won't be getting \$1.13 back from the Institute of Electrical and Electronics Engineers after all. Feerst believes that sum is the amount from his annual dues going toward the IEEE's increased public relations effort [*Electronics*, Feb. 14, p. 49], but the Civil Court of the City of New York believes otherwise. Last month the court dismissed his complaint on a motion filed by the IEEE for lack of jurisdiction and for failure to state a cause of action. Feerst says that he is not planning to appeal.

### Sperry's Conigliaro dead at 55

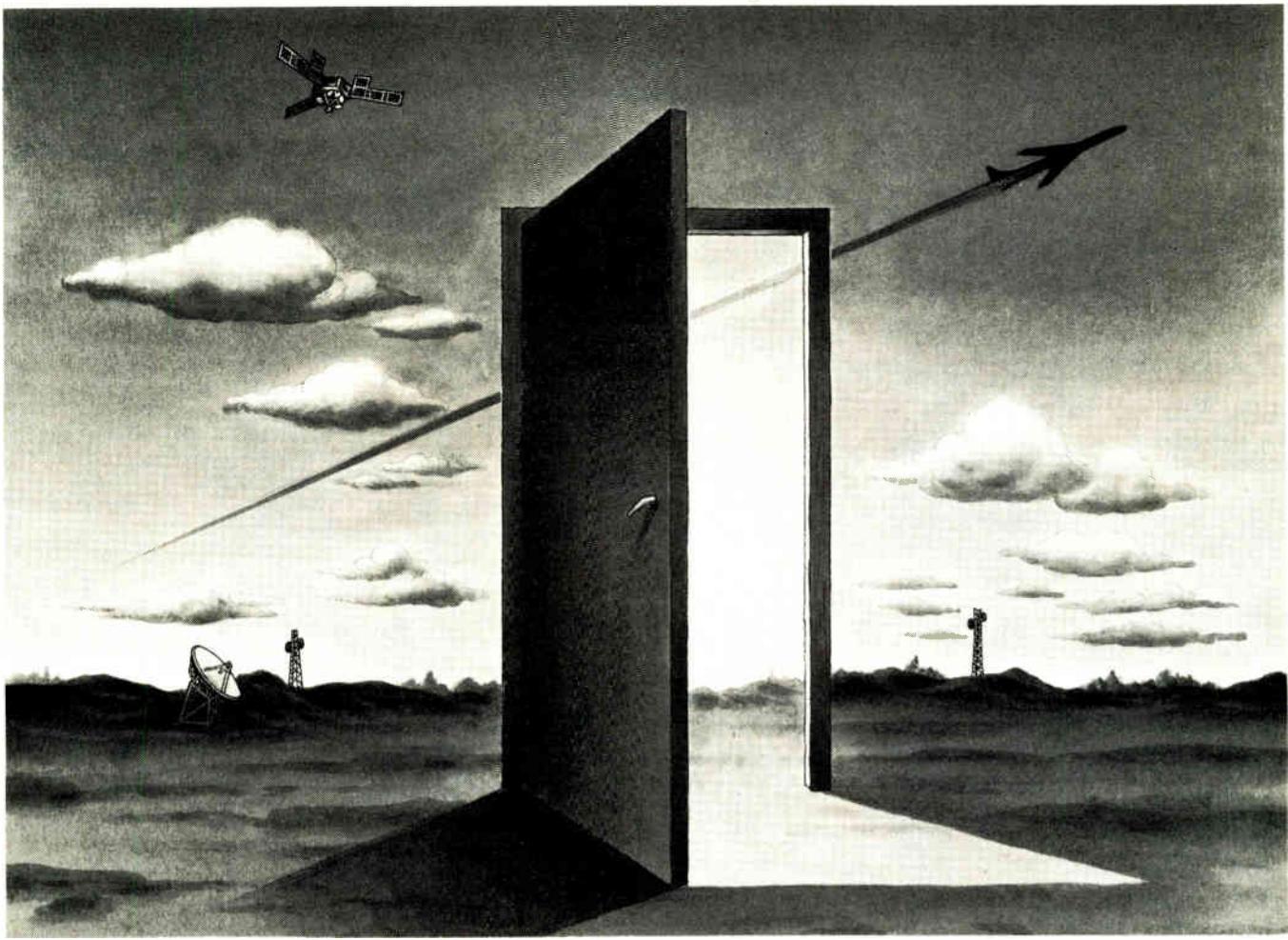
Salvatore A. Conigliaro, until recently president of the Sperry division of Sperry Corp. died late last month after a long illness. Conigliaro, 55, had been on a leave of absence from the company since January 7, and was to return as chairman of the Lake Success, N. Y., division in July. Robert L. Wendt had become president of the division following Conigliaro's departure.

### National to make TI low-power Schottky parts

In a move that should help quench the thirst for low-power Schottky TTL parts, National Semiconductor Corp., Santa Clara, Calif., plans to manufacture the 54AS/74AS and 54/ALS/74ALS Schottky series of Texas Instruments Inc. With a 4-nanosecond propagation delay at 1-milliwatt power dissipation, the 54ALS/74ALS series offers what is perhaps the best combination of power and speed available, whereas the 54AS/74AS (1.5 ns at 20 mw) is useful where very high speed is required. The TI circuits are somewhat faster than National's own LS<sup>2</sup> low-power Schottky parts [*Electronics*, Feb. 28, p. 149], but there is no functional duplication, so the company will make both families, it says.

### Reins to change hands at IBM

Late last month IBM's chairman, Frank T. Cary, announced that John R. Opel will become the chief executive officer as of Jan. 1, 1981. Opel was elected president in 1974; Cary became chairman and CEO in 1973 and will continue to serve as chairman of the board and of the board's executive committee, after Opel assumes his new responsibilities.



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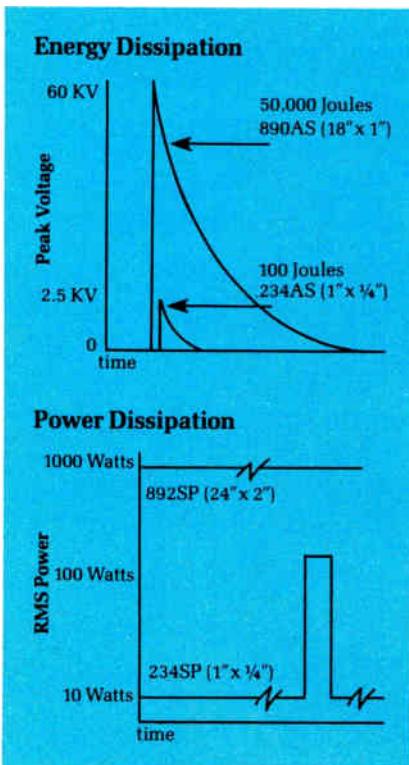
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## Electronics review

### Macrocell to go standard

All along, Motorola Inc.'s Semiconductor group has been planning to spin off standard emitter-coupled-logic parts from custom designs in its Macrocell line. The first is slated to bow later this spring.

Called the MC19000, it is an 8-bit-parity arithmetic-and-logic-unit slice for digital processors that will sell for \$100. Also, it will be produced by National Semiconductor Corp. in line with a Macrocell second-sourcing agreement signed late last year.

The second standard part is the MC19001 8-by-8-bit multiplier, which handles two 8-bit unsigned or signed 2's complement numbers and generates similar 16-bit products. The part can be used as a stand-alone 8-bit Multiplier or as a building block for larger arrays, Motorola says.

-L. W.

ible gate array, it looks as if Motorola's new small package will have clear sailing for a while with users who need its speed and low power. The other major ECL producer, Fairchild Camera and Instrument Corp., turns out gate arrays with dissipation similar to that of the Macrocell.

**Interest.** Confirming interest in lower-power ECL circuits is Robert Harrington, applications engineer at Kennedy Corp., a Monrovia, Calif., maker of computer-disk drives. "The heat is a problem in disk drives," he reports.

Thus Kennedy had to use low-power Schottky ICs in critical data-separation circuits in its new 8-inch hard-disk drives in place of the discrete ECL gate arrays used in its 14-in. Winchester disk drives, because ECL packages had to be separated by about 1.5 in. for cooling. However, the substitution caused speed to drop from 8 to 5.5 megahertz, and Harrington says he would consider the Miniarray when available—a point of agreement with other firms in the drive business.

For signal processing, there is interest in ECL for its speed—even with the high power dissipation—chiefly for military systems. However, a cooler package could spur wider application, says a source at TRW Inc.'s Defense and Space Systems division in Redondo Beach, Calif.

Motorola expects to turn its first Miniarray designs into silicon by late summer, so pricing is not set. However, it will be similar to Macrocell's in the cost of custom circuit options, which for the larger chip comes to

\$40,000 each in small quantities and \$15,000 each for more than 30. Macrocell's computer-aided-design process is directly adaptable, and Miele expects it will turn out Miniarrays easily.

-Larry Waller

### Commercial

### Meter reader may control remote alarm

Using standard complementary-MOS microprocessors and a Burroughs B-1835 central computer, Datavision Inc., a fledgling security equipment company in Detroit, believes it has come up with a cost-effective way to retrofit meters for remote reading of water, gas, and electricity consumption. Once installed, the system can also be connected to sensors to monitor up to eight additional functions such as burglar and fire alarms.

The system consists of a front-end processor installed in each home, an outdoor polling processor that collects information from eight front-end units, the central computer, and a central alarm-monitoring station. On command from the polling processor, the front-end processor takes a reading from a specially designed reading head that converts the meter's digits to encoded signals. This information is transmitted to the polling processor via telephone lines, where it is stored in a 16-K random-access memory until the central computer collects the data, again over leased telephone lines. The computer verifies the data, cal-

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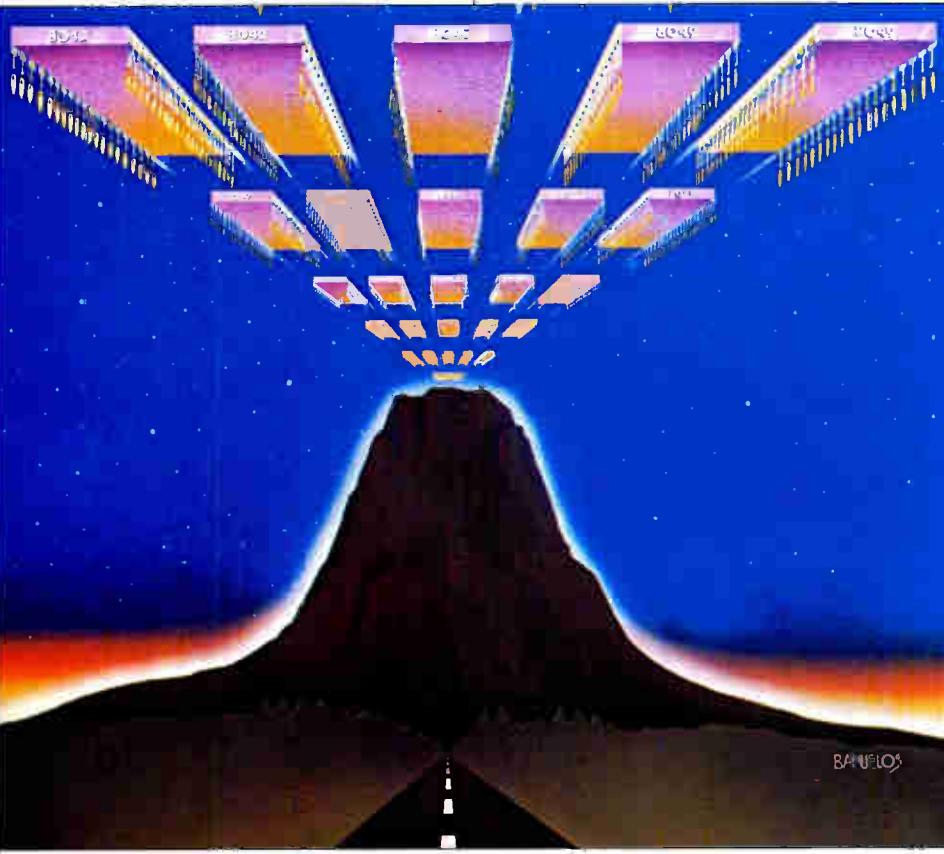
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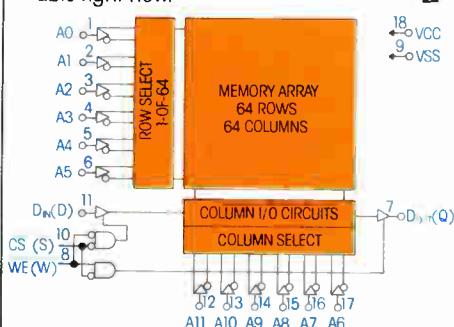
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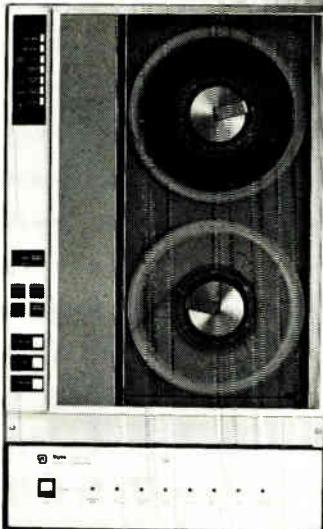
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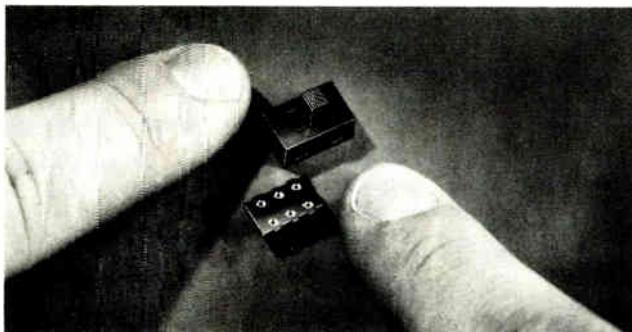
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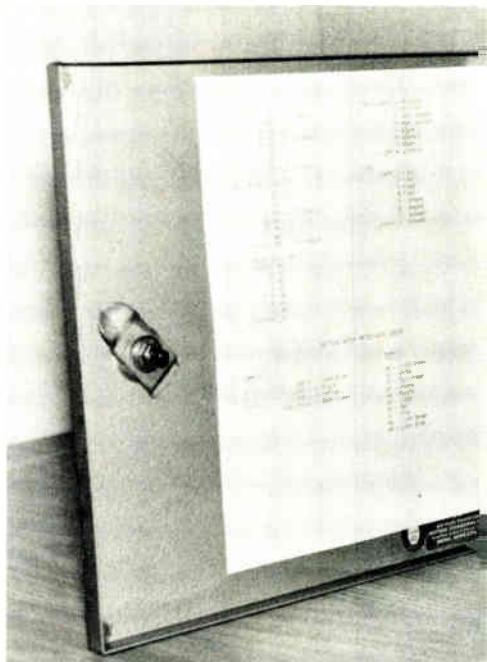


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## Electronics review

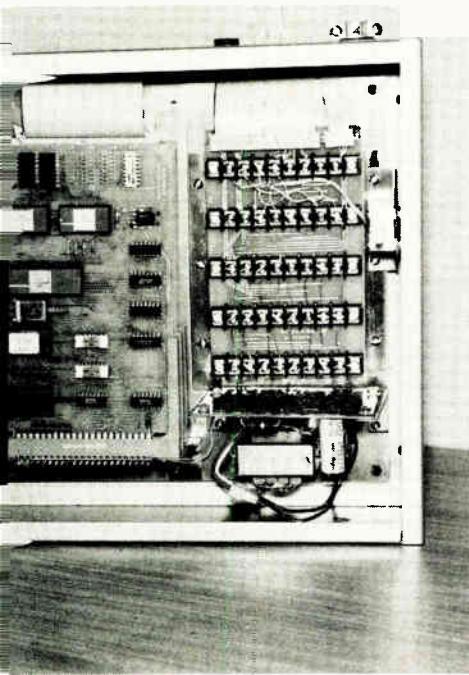


**Reader.** Front-end processor in Datavision's remote meter-reading system transmits encoded meter data to a polling processor linked to a computer.

culates the amount due, and produces a bill ready for mailing.

Both the front-end and the polling processor are built around RCA-1802 microprocessors, which Datavision chose for their low power operation and resistance to external noise. The company designed the system to be compatible with the upcoming RCA-1804 microprocessor and plans to switch when the higher-capacity 1804 is available. Ultimately, a custom chip will need to be designed, Datavision's president, Maurice B. Hogan, says, but the volume is not yet high enough.

**Suburban test.** The first test of the system, involving 25 homes in the suburban community of Grosse Pointe, Mich., is under way. The homes can be polled and billed in three minutes, compared with the several days it takes the community's water department to read the meters. If the initial trials succeed, the system could be expanded to cover some 2,100 homes and businesses. According to Datavision, the water department could cut its meter reading and billing costs by 50%. Larger electric and gas utilities could realize



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**PRESENTED BY:** Mark D. Walby, Product Manager, EG&G Reticon. Mr. Walby holds a BSEE from MIT and an MSEE from Stanford University. He is a recognized circuit and system designer, author and speaker.

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80% reductions, he says.

The meter-reading system is primarily a means of opening up a market for security systems, explains Carlo Ugval, Datavision's chairman. Once the front-end and polling processors are in place, there is enough capacity to add alarm monitoring. In this setup, the front-end processor is connected to smoke detectors and to door and window sensors. When triggered, it alerts the polling processor, which is usually located on a nearby telephone pole, and the alarm is immediately transferred to the central office. Eventually, the polling processor could be linked directly to terminals in the fire and police departments to provide direct emergency calls.

Although the system now uses leased telephone lines for information transmission, other means are available. The company is currently testing the telephone company's Dataphone Select-a-Station simulator system and is also looking into the possibility of using cable TV lines. It has preliminary designs for an ultra-high-frequency transmitting and receiving system as well.

Although Datavision is a small company competing with well-financed firms in the home security market, it is depending on getting a

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### Electronics review

foot in the door via the remote meter-reading approach it is promoting. The Grosse Pointe test will be key to its future. -David Whiteside

McGraw-Hill World News

### GTE to offer electronic mail

By summer, yet another company will be offering electronic mail service. GTE Telenet, a subsidiary of General Telephone & Electronics Corp., will start up its Telemail using its existing nationwide common-carrier network. A computer-based mail service enabling users to send, receive, and file messages electronically, Telemail will be used with a wide variety of data terminals and word processors supporting telecommunications interfaces.

With this move, GTE is joining the ranks of ITT with its Faxpak [Electronics, March 27, p. 50], Xerox and its Ethernet, Satellite Business Systems, and AT&T's troubled ACS. Telemail will allow the user to access an electronic "mail box" from any telephone using a desktop or portable terminal. Telenet [Electronics, Dec. 20, 1979, p. 33] solves the problem of interfacing equipment from different vendors by performing speed, code, and format conversions. The host machine that does this is a Tandem T-16 transaction processor. Eventually the Vienna, Va.-based subsidiary will offer the service of delivering voice messages, using store-and-forward technology.

**More.** AT&T's Antelope system, about which little more is known than a projected 1983 introduction, may also handle electronic mail-like functions of voice and data over existing twisted-wire pairs.

In another announcement late last month, Tymnet Inc., the Cupertino, Calif., common carrier, said that it will offer a second-generation mail service starting June 1. On-Tyme-II, based on the firm's existing electronic mail service, will provide direct communication between ASCII terminals and facsimile terminals, as will Faxpak.

-Pamela Hamilton

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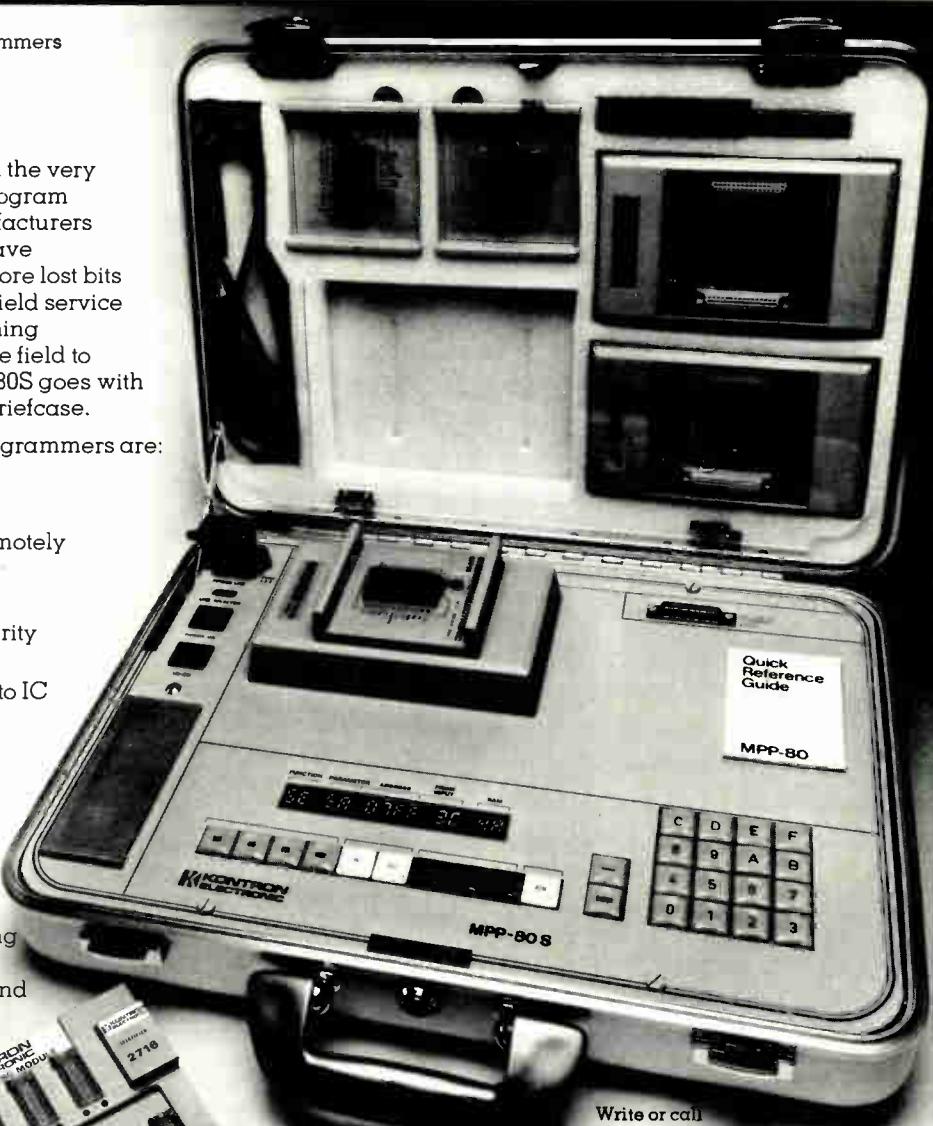
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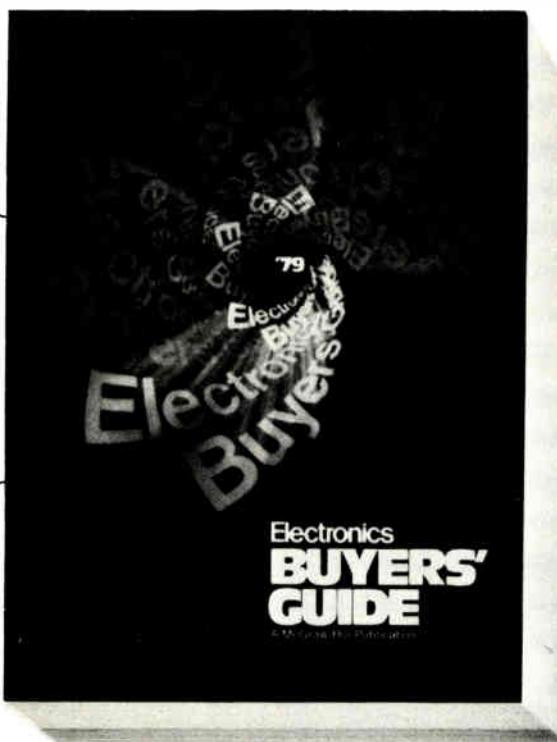
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# Washington newsletter

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## Budget cuts hit schools, R&D; defense spared . . .

Technology education and research and development come up short in President Carter's revised fiscal 1981 spending plans for space, energy, and the National Science Foundation. Military electronics R&D remains essentially unchanged, however, although a \$1 billion cut in defense procurement—mostly in aircraft and ship overhauls—is proposed. The NSF's education and research programs, heralded earlier as stimulating university science and engineering training [*Electronics*, Feb. 14, p. 95], will be cut \$100 million under Carter's budget-balancing plan. The National Aeronautics and Space Administration is scheduled to lose \$224 million, much of it in space science programs, including the joint U.S.-European solar polar spacecraft program. **Department of Energy solar R&D and demonstration efforts, including photovoltaics, will also be hard hit by spending cuts of \$247 million in fiscal 1981 in addition to a \$32 million cutback proposed for the existing fiscal year.**

## . . . as Carter's priorities raise questions In Congress, Industry

The budget debate to come in Congress—where Carter's priorities are already suspect—is sure to be fueled by concerned R&D communities in education and industry, not to mention social and urban program advocates outraged by even deeper cuts in their projects. One sore point: NASA's costly space shuttle program (\$1.87 billion) is untouched by fiscal 1981 cutbacks because of its importance for launch and retrieval of military as well as civilian satellites, but funds to develop scientific experiments and equipment for the shuttle-borne manned Spacelab are proposed to be cut 60% to \$29 million. Such R&D cuts "are nickel-and-dime economies that will do more harm in the long run than they achieve in savings," complains one senior House Budget Committee staff member. Suspicion of White House budget revisions overall is fanned in Congress and industry by what one electronics executive calls "Carter's fiscal sleight-of-hand." For example: in January, the President said his \$615.8 billion spending program in fiscal 1981 would generate a \$15.8 billion deficit. His revisions at the end of March cut outlays by only \$4.3 billion to \$661.5 billion, yet show a \$16.5 billion surplus. The reason: Federal receipts are now forecast to rise from \$600 billion to \$628 billion because of increased gasoline taxes and withholding taxes on interest and dividends.

## Solarsat studies to receive review for July decision

Advocates of solar-power satellite systems will get their best insights into what the July 15 program recommendation to the Secretary of Energy will be at the April 22-25 SPS Program Review and Symposium, which will be held on the University of Nebraska campus at Lincoln under the joint sponsorship of the Department of Energy and the National Aeronautics and Space Administration. The Energy Department's Fred Koomanoff, SPS program chief and meeting chairman, will draw on the symposium's 170 papers—including about 100 by study contractors—in drafting the department's recommendation. It will be forwarded to the White House later. SPS systems would employ photovoltaic cells to generate electrical energy, which would be beamed via microwaves to earth antennas for regional distribution. SPS proponents like the Sunsat Energy Council suspect that the open meeting is being held in out-of-the-way Nebraska to limit public attention, but Koomanoff insists that the site was chosen because "about half the contractors are from the West Coast or Texas."

# Washington commentary

## Sen. Stevenson blasts technology policies

As Japan enters the 1980s with a clear industrial strategy, the United States starts the decade "with no industrial strategy, no comprehensive energy policy, no food policy, no export strategy, and no strategy to repair the world's institutions for trade, development, and money."

This charge was leveled by Sen. Adlai Stevenson (D., Ill.) at a seminar on quality control and productivity presented for U. S. government officials and electronics industries executives by the Electronic Industries Association of Japan (see story, p. 81). Though such public critiques may be rare in Japan, American executives listened appreciatively as the chairman of both the Senate Banking subcommittee on international finance and the Commerce subcommittee on science, technology and space ripped into the economic, trade, and technology policies of the Carter Administration. Stevenson can afford to speak with brutal candor about Government failures, having announced several months ago that he will not be a candidate for reelection in November.

Stevenson says only that he intends to continue to speak out on public policy issues, but he has yet to disclose his future plans. In his role as chairman of two key Senate subcommittees, he has acquired extensive and detailed knowledge of economics and technology, particularly in the electronics industries. And he likes little of what he sees in the U. S.

### Why the U.S. lags

"Far more important" to Japan's industrial success than its quality control techniques, says Stevenson, is "the ability of Japanese industry and government to work cooperatively to target market opportunities, develop commercial products adapted to those opportunities, and funnel resources into projects with the greatest chance of increasing Japan's exports."

The U. S., on the other hand, "has fallen behind in the commercialization of technology," the Senator contends. "In general, American industry has been oriented to the domestic market. In electronics, it innovates, but it does not exploit innovations as aggressively as others." American government, he adds, "does little to encourage collaborative research and product development outside the military. Patent and antitrust policies have precluded the consortia which are a prominent factor in Japanese technological advances."

It seems ironic to him that Japan's computer industry "is organized by government for investment, basic research, and global competition,"

while "back in the U. S. the Justice Department is trying to break up IBM."

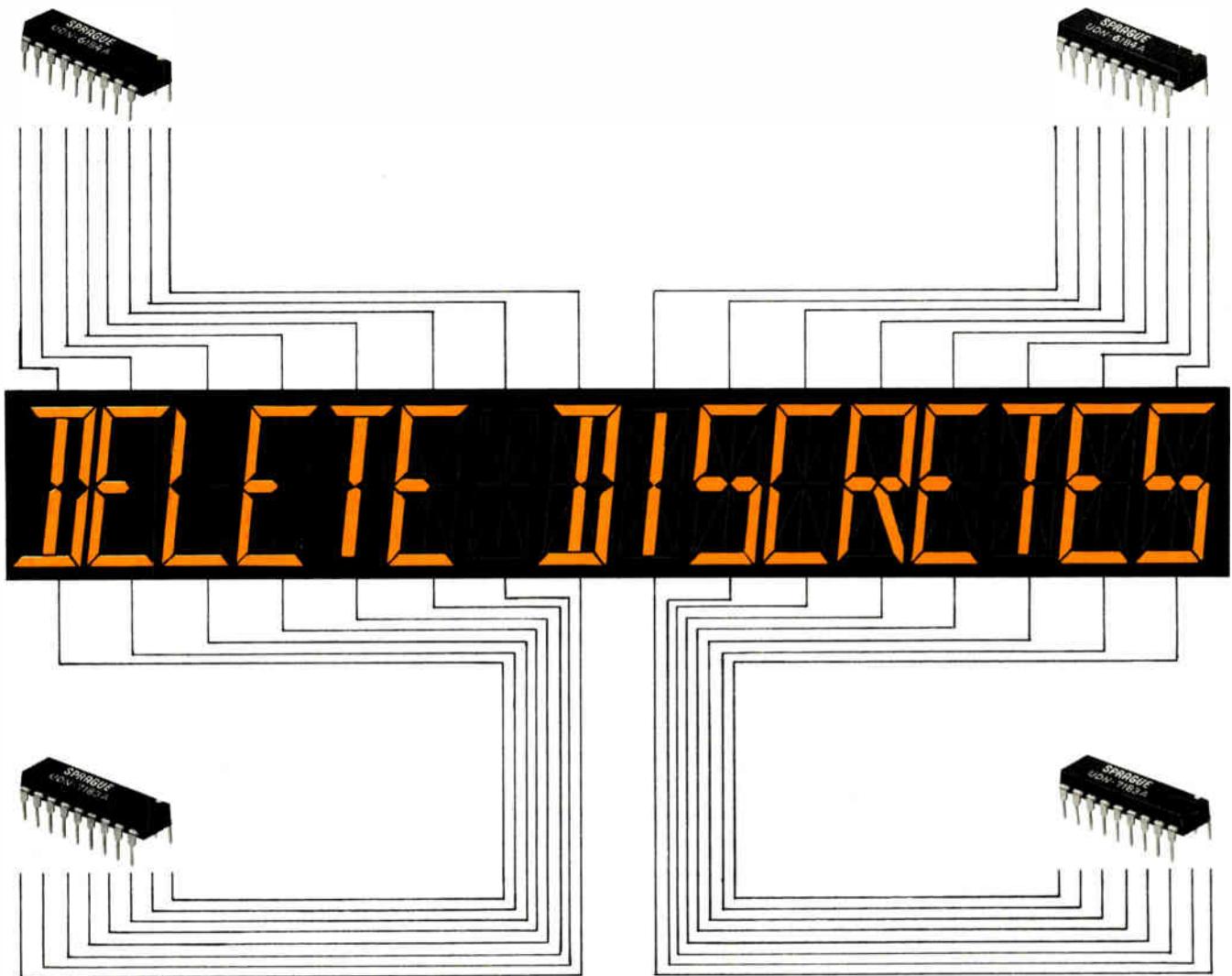
### Comparing subsidies

Stevenson warns that in the absence of a sound industrial policy, "political pressures will lock the U. S. into the kind of spiral of subsidies, inefficiencies, and declining productivity which destroyed the British economy." And he offers one more biting example of that trend. "In general, the Japanese draw labor and capital away from declining sectors and channel productive resources to target industries—computers, electronics, robotics, energy, and space. That may sound like government meddling, but the Ministry of International Trade and Industry's industrial investment is \$2 billion—less than one ninth, as a percentage of gross national product, of what the British spend subsidizing corporate geriatric cases and little more than the U. S. intends to invest this year in 'the new Chrysler Corporation.'"

America's most competitive and innovative industries—aerospace, agriculture, and computers—are those that have benefited most from Federal support of technology, the Senator argues, adding: "If by inadvertence, the U. S. stimulates an aerospace industry that dominates world markets, imagine what it might do by calculation."

Stevenson's solution for America's loosening grip on world technological leadership is not necessarily more government programs or planning. He proposes:

- More government-industry cooperation in the form of incentives for corporate retraining of workers displaced by structural economic change.
  - Jointly funded generic industrial technology centers in universities and nonprofit research institutions.
  - An information system to evaluate commercial potential of new technologies, to identify export and productivity enhancement opportunities, and to gather foreign intelligence. America should make use of foreign technology.
  - A national industrial strategy for competitiveness that includes accelerated depreciation, R&D investment incentives, and corporate and capital gains tax reduction, provided that the reductions promote "industries of the future." That last condition is critical, Stevenson observes, since "those nations which have been most successful at promoting noninflationary growth have demonstrated that how a nation's money is spent is as important as how much."
- Ray Connolly



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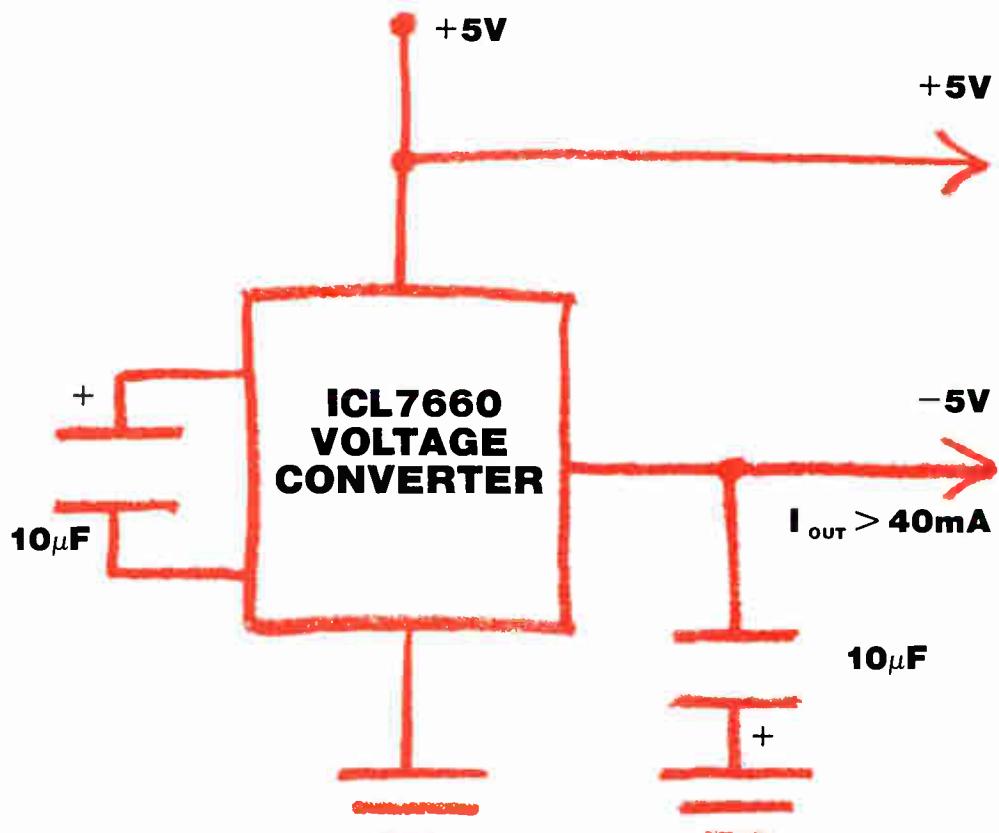


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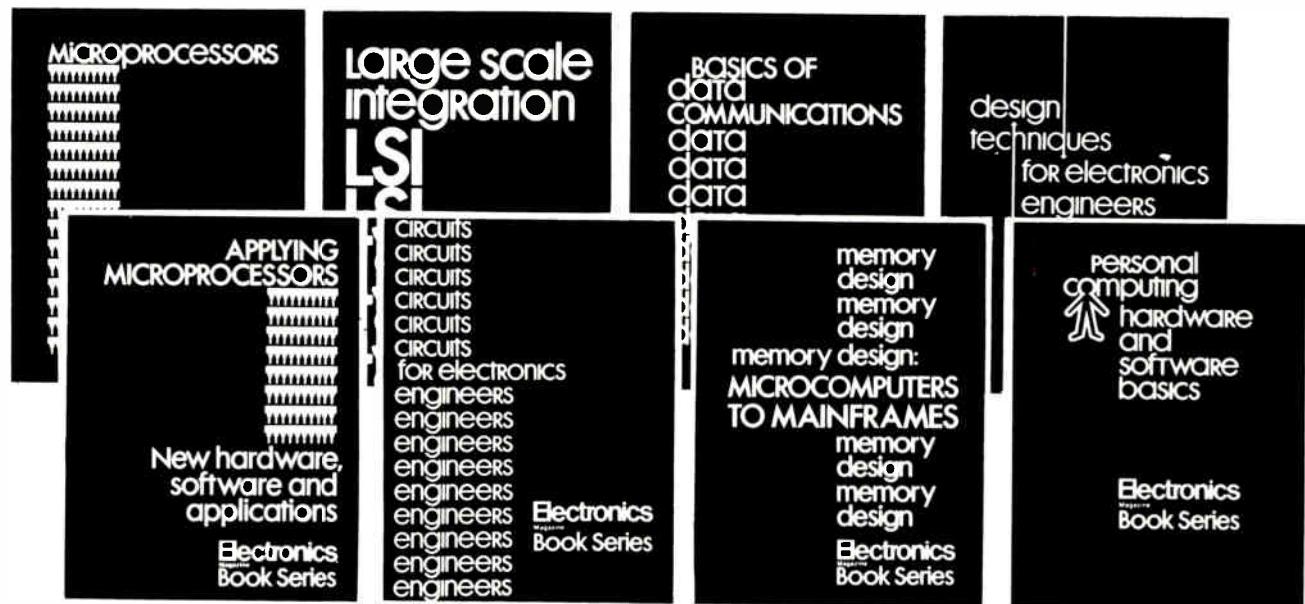
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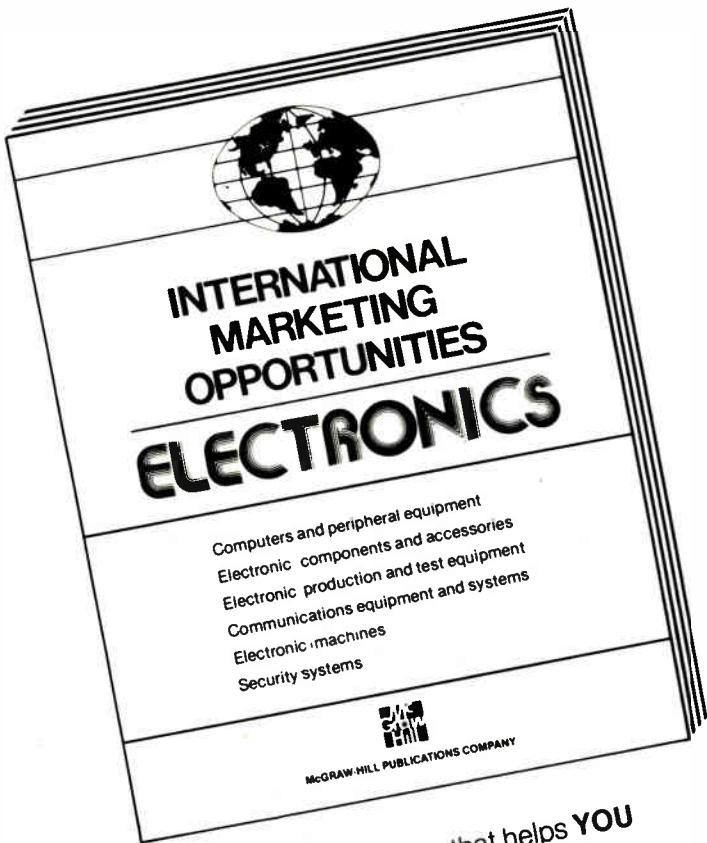
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Circle 62 on reader service card

many major network manufacturers who have installed it.

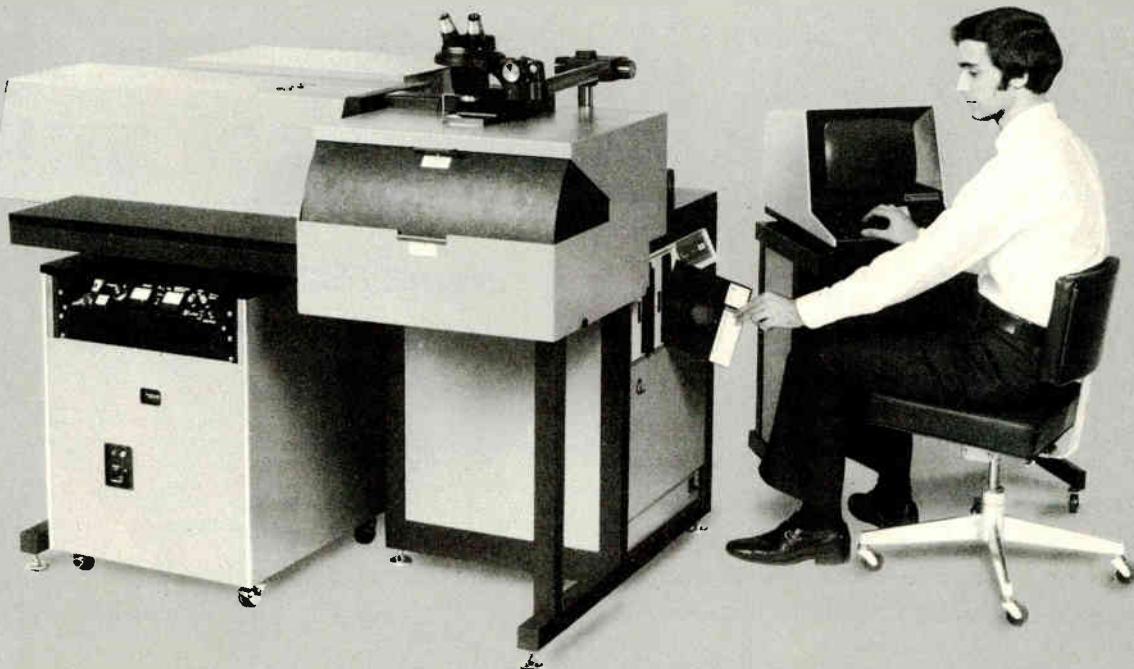
The system microcomputer is backed up by the laser trimming industry's most intelligent software operating system. It was developed specifically for high-speed laser trimming. The software directs the measurement/laser interaction, using a Chicago Laser exclusive high-level programming language. As a result, no comparable laser trim system is easier or faster to program than the CLS-33. On-line compiling and editing are featured for user convenience and easy program debugging in user language.

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# International newsletter

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## BPO demonstrates picture viewdata

In a move aimed at reestablishing a technical lead in the international viewdata stakes, the British Post Office has demonstrated a picture viewdata system at an international conference on the subject—Viewdata '80, held in London, March 26–28. **Full-color photographs, as well as alphanumeric text, can be stored in a computer and transmitted over telephone lines** to be held in a frame store in the TV terminal. In contrast, Canada's Telidon system is capable of advanced graphics but not photographs (see p. 44). The use of differential pulse-code modulation to compress the video data cuts the needed frame store size to 24 kilobytes and the transmission rate to 1,200 b/s. At that rate, a picture is transmitted in 1 minute; a practical system therefore requires a fast modem or direct connection to a digital exchange. Consequently, the post office sees picture viewdata, which is upwardly compatible with Prestel, its viewdata service, being introduced in the late 1980s and is concentrating on applications for the private business and overseas markets.

## Thomson-Brandt wants to be No. 2 In European color TV

Thomson-Brandt SA, best known for the high-technology hardware sold around the world by its subsidiary, Thomson-CSF, aims to become the second-ranking color TV producer in Western Europe, behind the Dutch-based Philips group. The Paris-based company, which took over the West German TV maker, Nordmende KG, in 1978, **wants to add to its stable Saba GmbH**, in Villingen/Schwarzwald, West Germany, a money-losing member of GTE's Consumer Electronics Group. Saba's output of some 500,000 color sets, added to the million-plus total for Thomson and Nordmende, would lift the French group to a level where it feels it could withstand the heavy competition in sight from Japanese suppliers. The latter are poised to move heavily into the big-screen market next year when the PAL patents that so far have kept them out start to expire.

## Big increase predicted for West German tabletop computer sales

By 1990, there will be some 1 million tabletop computers installed in West Germany—the type of systems known as home, hobby, or learning computers and selling for from \$250 to \$5,000. That forecast, from the Frankfurt-based computer consultants, Diebold Deutschland GmbH, works out to a **fiftyfold increase over the number currently installed**. The present West German home computer market is dominated by three firms, Commodore, Tandy's Radio Shack, and Apple, whose shares are pegged at 51%, 35%, and 4%, respectively. However, that ranking may change, Diebold says, as other firms, among them Hewlett-Packard, Texas Instruments, and West Germany's Triumph-Adler, move into the market.

## TI France devises two-chip set for ignition control

Working with engineers at the electronics subsidiary of French auto maker Régie Renault, Texas Instruments France SA has developed a two-chip electronic ignition system for 2-liter engines. To be installed starting next fall on Renault's new sport coupe, the Fuego, the system uses a single passive sensor consisting of a simple coil and magnet to monitor crankshaft speed and position. At its heart is an **integrated-injection-logic circuit that calculates the spark-timing advance**. The timing-advance curve is stored in 64 22-bit words in a mask-programmed read-only memory. Thus there is no chance of mistiming, say Claude Jacquemin, automotive circuit manager for TI France in Villeneuve-Loubet, near Nice. The system can withstand temperatures of  $-40^{\circ}$  to  $+125^{\circ}\text{C}$ .

# International newsletter

## Sharp develops C-MOS speech synthesizer, makes watch talk

Joining the parade of integrated speech synthesizers is a complementary-MOS circuit developed by Sharp Corp. that contains all the necessary components on its 5.3-by-5.2-mm chip (209 by 209 mils) except for a 6-bit digital-to-analog converter. Its 4-kilobyte read-only memory has sufficient capacity for 13 to 22 seconds of speech, including a male voice, a female voice, or a tone, and can be expanded by the addition of up to 1 megabyte of external ROM. Sharp engineers say that the 2-mA current drain at 4.5 v is at least an order of magnitude lower than that for a competitive n-MOS device recently announced by Matsushita Electric Industrial Co.

The chip will be used in consumer products. Its first application will be in what the company calls a quartz "secretary" watch. The size of a pocket radio, it uses speech synthesis in five ways. Besides announcing the present time at the touch of a button, it can be set to announce the hour and half hour or used as an alarm to announce a preset time by both voice and melody. It can also function as a timer to announce the passage of time or as a stopwatch to announce elapsed time. The watch is 114 by 60.7 by 23.0 mm (4.5 by 2.4 by 0.9 inches) and weighs 160 grams, including two AA batteries that will power it for a year. Sales will start April 25, with the price about \$70.

## Plessey launches two-chip universal frequency synthesizer

Though integrated-circuit frequency-synthesizer channel tuners have found slots in military mobile radios, they have generally proved too expensive for civil applications. Plessey Semiconductors Ltd., Swindon, aims to change that with a two-chip synthesizer set that it is launching at Communications '80, April 15-18, in Birmingham, England. The set, which comes in three frequency versions, comprises a fast modulo-2 or -4 divider fabricated using Plessey's process for high-speed bipolar circuits and an n-MOS controller capable of accepting inputs from read-only memory, programmable ROM, and microprocessors. It contains all decoding and control circuitry and requires only an external reference frequency of 4.8 MHz. There are four divider circuits: a 1-GHz and a 512-MHz modulo-4 divider and two 200-MHz modulo-2 dividers. Philips was the first to market with a chip set, developed at its Redhill, Surrey, research laboratories [*Electronics*, Aug. 31, 1978, p. 74], but Plessey claims a price breakthrough. Its chip set will sell for \$20 in volume quantities for some versions.

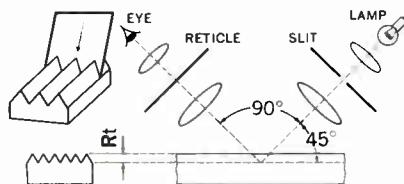
## Companies to unveil Teletex gear at Hanover fair

Using the April 16-24 Hanover fair as a forum, a number of communication equipment makers will introduce hardware for Teletex, the electronic mail service that West Germany's post office plans to start next year [*Electronics*, Nov. 9, 1978, p. 69]. For example, NV Philips Gloeilampenfabrieken's Data Systems division in Apeldoorn, the Netherlands, will stage what it terms the world's first public demonstration of international Teletex services, with its equipment tied to Philips terminals in New York, Montreal, and Stockholm. West Germany's Telefonbau und Normalzeit will show how a private automatic branch exchange can be used in Teletex communications; for that purpose, the Frankfurt-based firm has developed a microprocessor-controlled equipment that interfaces a PABX system with the digital data networks over which information is sent.

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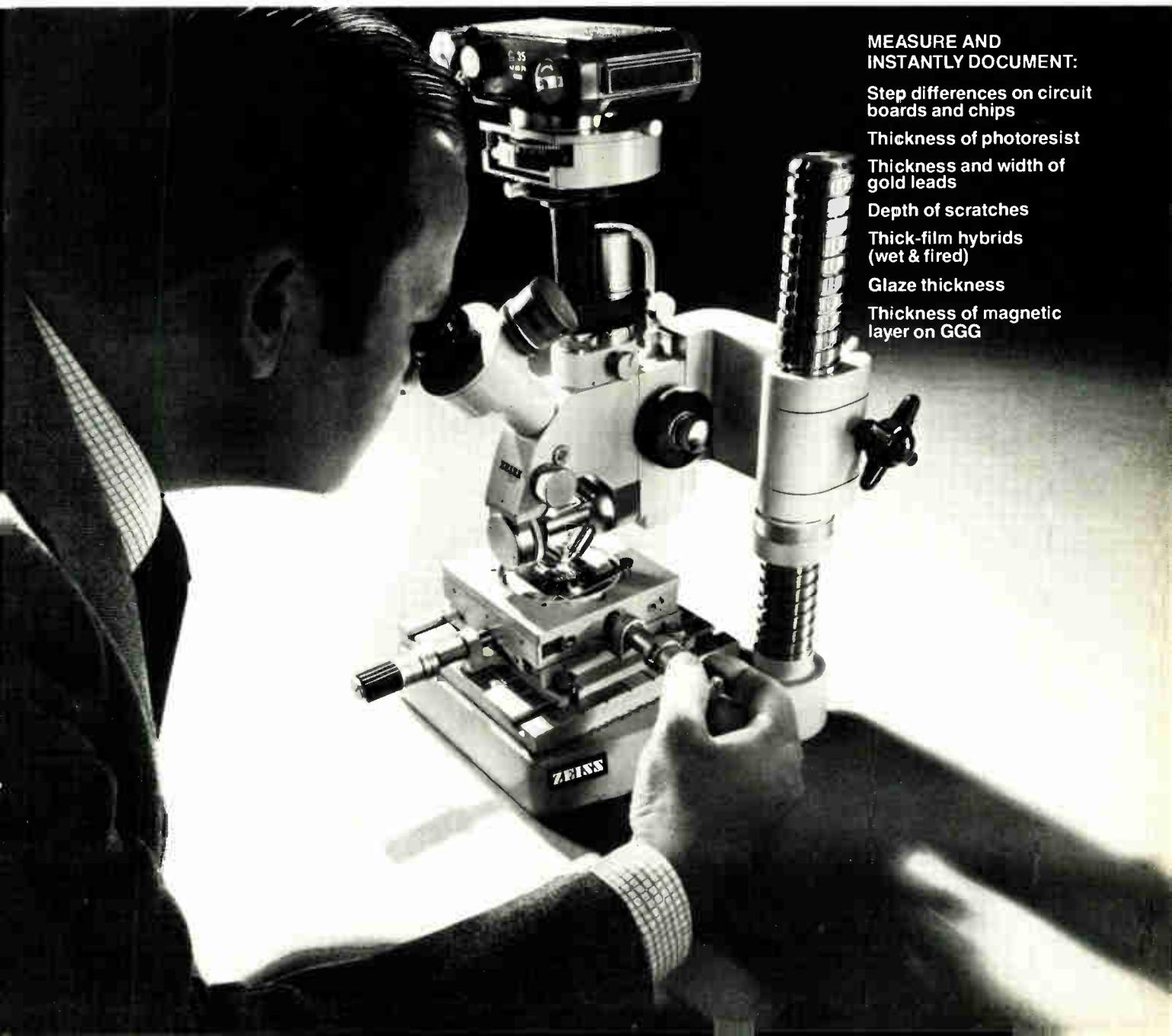
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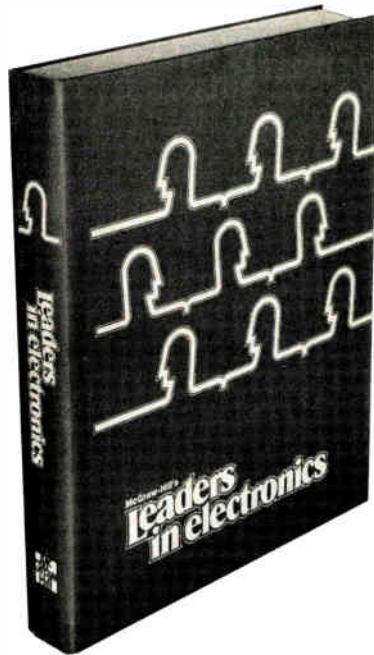
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### **Sample Listing**

Jones, John J

Chmn & CEO, Microprocessor Div of Computers Inc, 1023 W Warner Ave, Dayton, OH 45479, Tel (513) 555-2000. Born: Mar 26, 1926, Philadelphia, PA. Education: MBA, Harvard Business School, 1950; BSEE, Univ of Ill., 1946; PhD (Hon), Yale Univ, 1977. Professional Experience: Natl Bur of Standards, 1956-74, Adm Eng; Litton Ind, 1954-56, Sr Eng; NCR Corp, 1950-54, Eng. Directorships: Computers Inc since 1975. Organizations: IEEE since 1946, Sec Head 1972-73; AAAS since 1971; Midwest Ind Mgt Assn since 1974. Awards: Fellow, IEEE, 1977; Public Service Award, City of Dayton, 1976. Patents Held: 8 in computer circuits, incl Special Circuit for Microcomputer Chip Design 1975. Achievements: founded Microprocessor Inc 1974; project manager of first application of microprocessors for standard interfaces 1975. Books: 4 incl *Small Circuits and Their Applications* (editor), McGraw-Hill, New York, 1975. Personal: married 1950 to Mary (Smith), children John Jr, Jane Anne, Kevin. Residence: 344 W 34th St, Dayton, OH 45403, Tel (513) 555-4343.



## Switch contacts are normally closed in low-cost keyboard

by Kenneth Dreyfack, Paris bureau

**Novel design also replaces springs with magnet that keeps keys up, adding to simplicity and reliability**

A **unique keyboard**, which is also unusually simple, reliable, and low-cost, could revolutionize the keyboard business for terminals, push-button telephones, electric typewriters, and industrial equipment, believes its inventor, Edouard Serras-Paulet of Sigma Industries SA in Montaubon, north of Toulouse.

His approach has two novel aspects. First, a magnet rather than a spring holds each key up. Second, and more important, depressing a key does not generate a current.

**Dissatisfied.** Serras, who is also the company's founder and president, explains that he began looking at keyboard design during the early 1970s, when as a designer of airborne electronic equipment he saw the physical drawbacks in using springs to ensure key return. In 1972, he took out the first of a dozen patents protecting his new technique.

The new keyboard's baseplate is covered with a magnetized elastomer, a rubberlike material containing magnetized particles. A small metallic disk attached to the key plunger ensures that each key stays firmly in place. The company guarantees that each key can be depressed 10 million times before showing signs of mechanical fatigue.

Serras maintains that the magnetic system makes more sense mechanically. Spring-loaded keys require an increasing downward force as they

approach the contacts, reducing the probability of a firm contact when fully depressed. But in a magnetic system, the greatest downward force is required at the outset.

**Closed.** Serras did not stop there. To overcome one of the most common malfunctions in traditional keyboards, a poor electrical contact when a key is depressed, his firm designed a keyboard in which the switch contacts are normally closed.

Electrically, the keyboard circuit consists of an X-Y matrix printed on a Mylar circuit board with an insulating layer keeping the two sets of axes apart. A key is located at each intersection, and each key contains a diode. Five volts are applied sequentially to the vertical columns. If no key is depressed, the current flows through the diodes to 47-kilohm pull-up resistors located at the end of each horizontal row. The current drain is less than 2 milliamperes.

Depressing a key opens the matrix and breaks the current flow to the resistor at the end of one of the rows. Since the current is applied to the columns sequentially, a simple counter is all that is needed to determine the point in the matrix where the circuit has been opened.

**Vive la différence!** "All of our competitors work with contacts, but we have no contacts—we don't generate any signal, and that is the big difference," says Serras enthusiastically. He goes on to explain that the parasitic resistance of the diode is not critical, because the threshold voltage that determines whether the circuit is open or closed is 2.5 v. He adds that since the circuit is opened only when a key is depressed, and since the tolerance is so great, there

is no need for expensive contact materials. In fact, "the most expensive element in our keyboard is the key cap, which needs a double-injection plastic process to imprint the character," he notes.

Keyboard testing also becomes much simpler, Serras points out. "If there is something wrong, it will show up immediately when the keyboard is not in use," he stresses. "If there is nothing on the screen, then the keyboard is fine."

Sigma Industries expects to start large-scale production of its keyboards—tradename K-Serras—in June or July. By next year, it expects to be producing some 150,000 push-button telephone keyboards and 45,000 alphanumeric-terminal-type keyboards annually.

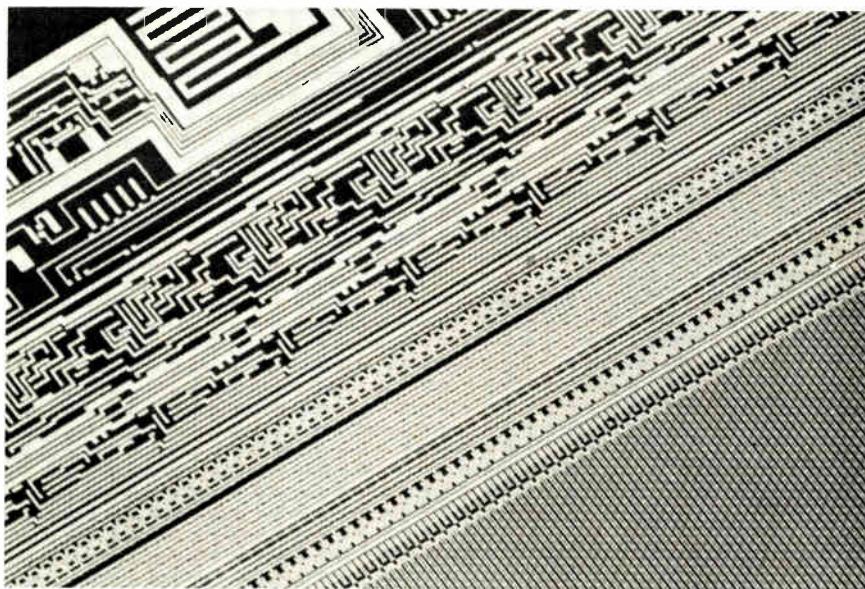
With production and testing time at about one minute per keyboard, and with assembly costs roughly one third to one quarter of those for traditional techniques, Serras believes the future is bright.

His firm has commissioned Arthur D. Little Inc., Cambridge, Mass., to study setting up production facilities in North America. Meanwhile, U. S. distribution will be handled by Seacor Inc., Norwood, N. J.

### Japan

**VLSI labs unveils last E-beam unit . . .**

A prototype design that can soon be used to make speedy electron-beam wafer-exposure systems for production rather than for merely showing feasibility is how Masashi Nakamu-



**Shaped to fit.** This fine-line circuit was exposed by a direct-writing machine that combines vector scanning with a variable-dimension rectangular electron beam.

ra, a laboratory head of Japan's VLSI Cooperative Laboratories, describes the final direct-writing machine developed by his group. It is a vector-scanning system incorporating the variable-dimension rectangular beam technique developed by the labs [*Electronics*, June 9, 1977, p. 33].

The new prototype system includes a cassette feed and is designed to directly expose 4-inch wafers, each containing about 50 1-megabit memory chips, at a rate of four wafers an hour [*Electronics*, March 27, p. 63]. The estimated complexity of each chip is 5 million pattern elements—for 250 million per wafer.

**Variable.** The individual elements are rectangles with sides variable from 0.5 to 5 micrometers. The elements can be positioned electronically within a square that is nominally 2.5 millimeters on a side but that may be somewhat smaller for convenience in stitching patterns together.

Pattern element size and position can be varied in increments of about 0.05 or 0.1  $\mu\text{m}$ . Built-in corrections enable fields to be stitched together with an error of less than 0.2  $\mu\text{m}$ , and the use of registration marks allows a similar accuracy in aligning patterns, even for wafers distorted during processing.

The variable-dimension rectangular beam is the key to the system's

high speed, as it writes the equivalent of a large number of points on the wafer simultaneously. Furthermore, a single compacted long word, rather than the four words usually required for each element, is used. Thus the compacted word, its access in one fetch, and the simultaneous processing of all the data for one shot contribute to the high speed.

The speed is thus higher than for a raster- or vector-scanning unit using a Gaussian beam. These are essentially serial systems, with the pattern developed one point at a time. Normally, the minimum feature dimension of these systems is four times the beam diameter. Therefore they require 16 shots to expose their minimum size rectangle, which takes just 1 shot by a rectangular beam.

**Memory.** In order to achieve the full potential of the shaped-beam system, a large-scale integrated read/write memory with a speed similar to that of the main memory of a large central processing unit has been developed to act as a buffer for the pattern information from the system disk. This memory, which was designed using the technology employed for mainframe memories, has a capacity of 10.5 megabytes and uses error-correcting code for increased reliability. Furthermore, the system includes fast, high-resolu-

tion digital-to-analog converters.

The prototype has all the necessary hardware and software, including provisions for adjustment of the beam current to compensate for proximity effects and for negative-positive inversions to match the resist being used. Other software enlarges or reduces the pattern or turns it into a mirror image of itself. Software is also provided to convert pattern data for the widely used David Mann PG3000 pattern generator to the format in this system.

The VLSI labs set the goals, drew up the specifications, and made the basic design for the system; it also performed the overall fine tuning and evaluation. JEOL Ltd., which made an earlier variable-dimension electron-beam machine, carried out the detailed design and fabrication, and the memory was fabricated by Fuji Electrochemical Co. under the supervision of majority owner Fujitsu Ltd.

-Charles Cohen

### East Germany

## ... as Zeiss shows similar system

An electron-beam exposure system from East Germany's VEB Carl Zeiss Jena combines vector scanning with a programmable-dimension rectangular beam and other design features to print lines as fine as 0.1 micrometer with virtually no loss in speed. Designated ZBA-10/1, the prototype is the successor of the ZBA-10 [*Electronics*, March 30, 1978, p. 55], of which there are some 10 models installed in Eastern Europe.

Zeiss officials insist that the system was co-developed with the Soviet Union. Indeed, some hardware such as microprocessors and other control devices is of Soviet origin, as are systems-related products like the electron resist, polymethyl methacrylate (PMMA). But according to Western experts, the system is really of East German design, with the bulk of the hardware coming from Jena-based Zeiss, the famed

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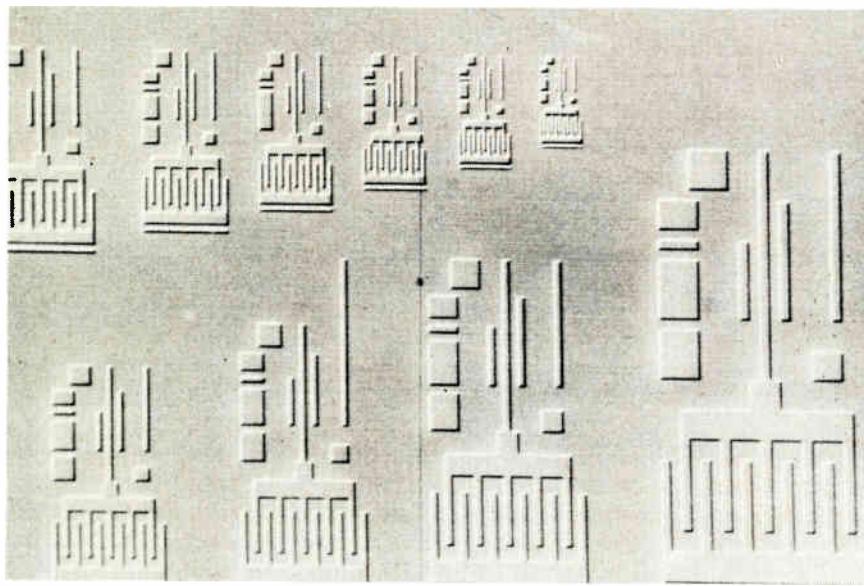
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## Innovations for Electronics





**Teamwork.** Vector scanning is combined with a variable-dimension electron beam to produce a direct-writing system for VLSI circuits like the experimental one shown here.

130-year-old optical equipment maker now also known for its work in planetariums.

Conceived to fulfill the requirements of very large-scale integrated-circuit technologies, the ZBA-10/1 sports a respectable set of performance characteristics. Under ideal conditions, Zeiss says, it can generate patterns with minimum feature dimensions of 0.1  $\mu\text{m}$ . The maximum exposure speed with 10,000 shots per square millimeter and a resist sensitivity of 1 microcoulomb per square centimeter is 1 square millimeter per second.

The fully automatic computer-controlled system accommodates masks up to 4 by 4 inches in size and wafers up to 4 in. in diameter. Beam deflection, controlled by a Zeiss-developed 15-bit digital-to-analog converter, is in 0.05- $\mu\text{m}$  steps over a 1.5-by-1.5-mm area. By butting a number of such areas, any size chip can be handled. Deflection distortion is less than 0.1  $\mu\text{m}$  and the registration accuracy is within  $\pm 0.1 \mu\text{m}$ . The same holds for the feature position repeatability.

**Range.** Pointing up the system's versatility is its wide range of applications. In addition to directly exposing wafers and making high-precision masks, it can be employed to produce reticles for wafer and

mask repeaters. Other jobs include the production of shadow masks for X-ray lithography and the generation of patterned junction photocathodes, optical test and holographic patterns, and integrated optic and thin-film device patterns.

The throughput is less than one hour for a 3-in.-diameter wafer with 1- $\mu\text{m}$  lines and with about 25% of its total area exposed to the beam. Significantly, that throughput remains the same for narrower line widths—in contrast to other systems on the market, with which the process times increase substantially with decreasing feature dimensions.

Knut Kaschlik, the man behind Zeiss's development effort, sees direct wafer exposure for IC production with fast turnaround times as the prime function for electron-beam equipment in general "because that's where their potential can best be exploited." As for the ZBA-10/1, he feels it is well suited in work aimed at the development and fabrication of experimental 256-k random-access memories.

Contributing to system efficiency and productivity are several factors. Vector scanning boosts throughput, as it scans only those chip or mask areas that require exposure. With raster scanning, on the other hand, the whole area is scanned.

**Programmable.** More important perhaps is the use of a beam whose dimensions can be programmed. With this technique a beam of rectangular cross section can generate large-area patterns in one exposure cycle, which is not possible with a pointlike beam, and the beam's cross section can be varied according to the dimensions of lines generated.

**Shaping the beam.** In the ZBA-10/1, the rectangular beam shape is obtained by limiting condensers in the beam-generating column. The side lengths of the cross-sectional areas are variable between 0.1 and 10  $\mu\text{m}$ . Since the beam has a quasi-rectangular current distribution over its cross section (instead of the somewhat uneven distribution characteristic for pencil beams), line edges can be well defined.

Further enhancing productivity—by a factor of four compared with the ZBA-10—is improved data transfer from the magnetic control tape to the computer. This was achieved by adding another buffer memory to the existing one.

While the control data is transferred from the tape to one buffer, the other buffer feeds its data to the exposure control units. After the 4-K data blocks are dumped, the roles of the buffers are reversed. Thus, the data transfer and exposure processes are carried out simultaneously and independently of each other. The data blocks are transferred in 170 milliseconds.

-John Gosch

## Great Britain

### ICL unwraps new low-end mainframes

International Computers Ltd. has taken the wraps off its ME29. With a raw speed of 3 million basic machine instructions per second, the new computer could more than re-establish its competitiveness in the low- to mid-range mainframe sector.

ICL uses this power to transform its successful but aging 2903 and 2904 from batch- to interactive terminal-processing systems. Thus the

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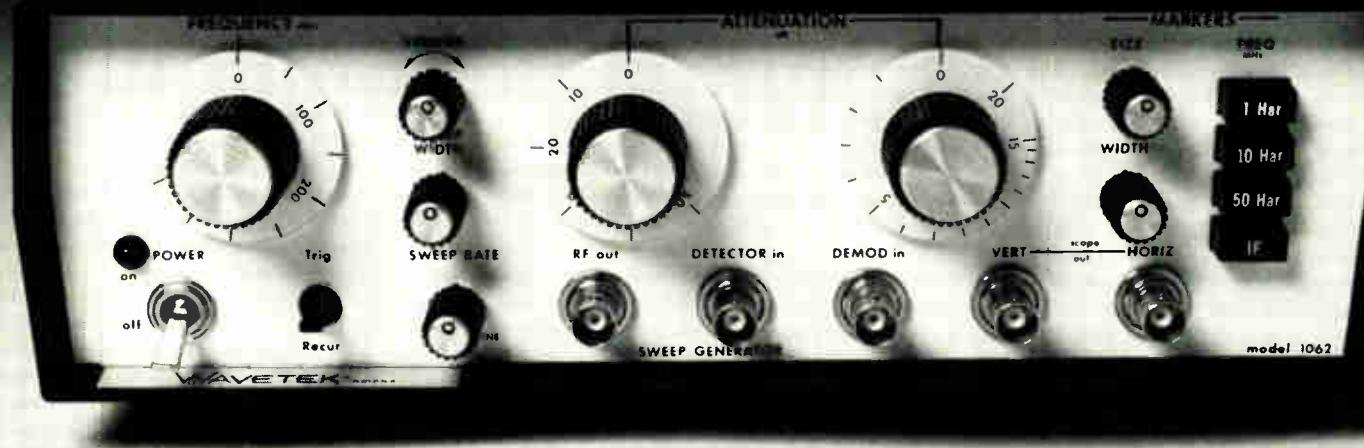
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A microprocessor system and a novel oxygen-concentration sensor, both developed at City University, London, have been combined in a compact boiler efficiency monitor from a small British company, Neotronics Ltd., in Bishop's Stortford, Herts.

The instrument's probe can be inserted into the flue of a boiler fired by oil, gas, or solid fuel and within seconds will give a direct reading of the boiler's fuel efficiency. Adjusting the airflow to the optimum can cut fuel bills by 3% to 5%, quickly repaying an initial outlay of \$1,000, says the company.

In the final production version, an Intel 8022 single-chip signal processor accepts inputs from a thermocouple and from the oxygen-concentration sensor—which was developed from work on lightweight zinc-air batteries—to directly drive a light-emitting-diode display.

-K. S.

larger ME29, the model 45, can sport up to 200 display terminals and run over 50 user's programs simultaneously. ICL has also thrown in a private viewdata capability, so that cheap viewdata terminals giving access to a company's data base can be widely dispersed about its offices.

The ME29 has a big role to play in ICL's marketing strategy: it both forms the entry-level system of its 2900 series and lays the groundwork for a single unified architecture based on a 32-bit-word structure and extending from the smallest to the largest of the firm's models.

**32 bits.** The now defunct 2903 and 2904 were 24-bit machines, whereas the bigger models in the 2900 series are all 32-bit systems. The ME29 follows this pattern and is a 32-bit micropogrammed machine that can efficiently emulate its 24-bit predecessors—with a five times greater throughput.

"It's a fast, high-revving emulator engine," explains project leader Bill Beard, who masterminded the new range. The speed comes from a central processing unit built with 10K

emitter-coupled logic, and the flexibility from microcode.

The microcode is stored in a high-performance control store. Engineered in 4-K static random-access memories, the store cycles at a nominal 155 nanoseconds, with an instruction-prefetching mechanism that enables most operations to take place in 93 ns. At 128 kilobytes, the model 45's control store is twice the size of that of the model 35.

Microcode and intermediate results in the control store are used to emulate the older machines. And to speed the processor, explains Beard, "we move more of the high-level applications and operating system code from main memory into microcode." As a result, the ME29 can run either the old or the new operating system, enabling users to migrate at their own speed to the new. Also, often used instructions like jump are hardware-decoded.

**Partitioned.** In hardware terms, the design is highly partitioned functionally. The CPU comprises three 8-by-12-inch four- to six-layer printed-circuit boards—one control-

ler board and two processor boards that each operate on 16 bits of data.

An ECL-level bus transfers data at about 128 megabytes per second between the CPU and the microprogram controller, and a TTL-level bus links main memory and input/output channels. The design, says Beard, "is a judicious mixture of ECL, TTL, and MOS technology."

The main store uses 16-K random-access memories and is extensible in 128-kilobyte steps from 256 kilobytes to 1 megabyte. The word access time is 750 ns.

**Operating.** In addition to new hardware, there is also a new operating system, called Transaction Machine Environment. Based on the well-proven Exec 3A operating system, it adds features that give the ME29 a terminal-processing and a powerful networking capability. For example, it has a built-in teleprocessing monitor, and it can access files on other ME29s in a network.

Furthermore, there is a new memory management scheme, which ICL calls leaf addressing, that bears similarities to virtual memory systems found on larger machines; it allows the basic operating system to be expanded a leaf at a time. Thus the ME29 can evolve as needed.

The new range begins at about \$78,000 and extends to some \$555,000. Delivery is scheduled to start in the fall.

**Complete system.** Fully configured, a system would comprise a 1-megabyte main store, 16,000 megabytes of disk storage, up to three line printers, magnetic tape storage, and other peripheral units and support 24 locally attached work stations, plus numerous other terminals over remote communications lines. The five storage options range from a 35-megabyte fixed disk to a 500-megabyte fixed disk.

Says Keith Bull, marketing manager for the Putney, London, firm, "The ME29 is comparable with the IBM System/34 at its low end, with the System/38 throughout, and at the top with the IBM 4331. It has significant price-performance advantages over the equivalent IBM product at all levels."

-Kevin Smith

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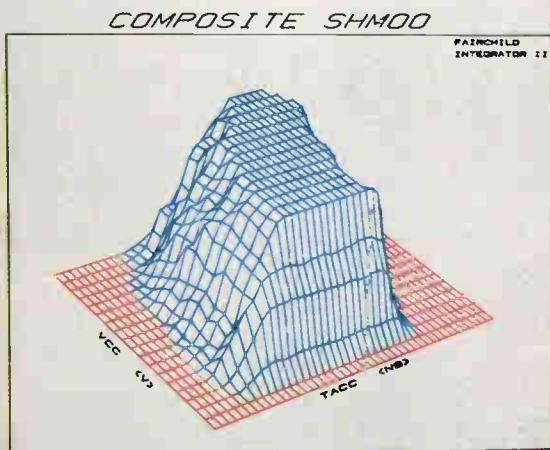
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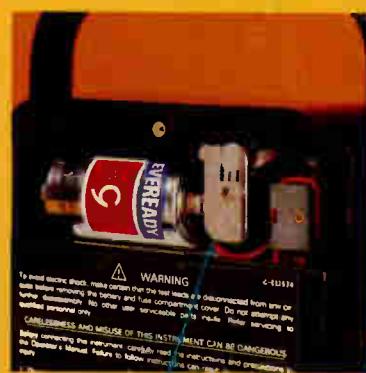
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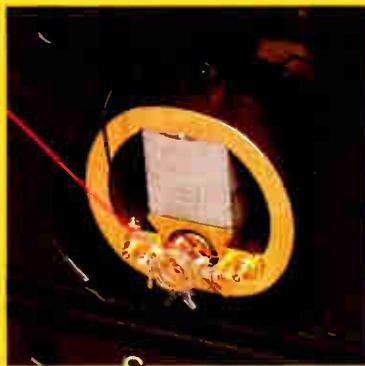


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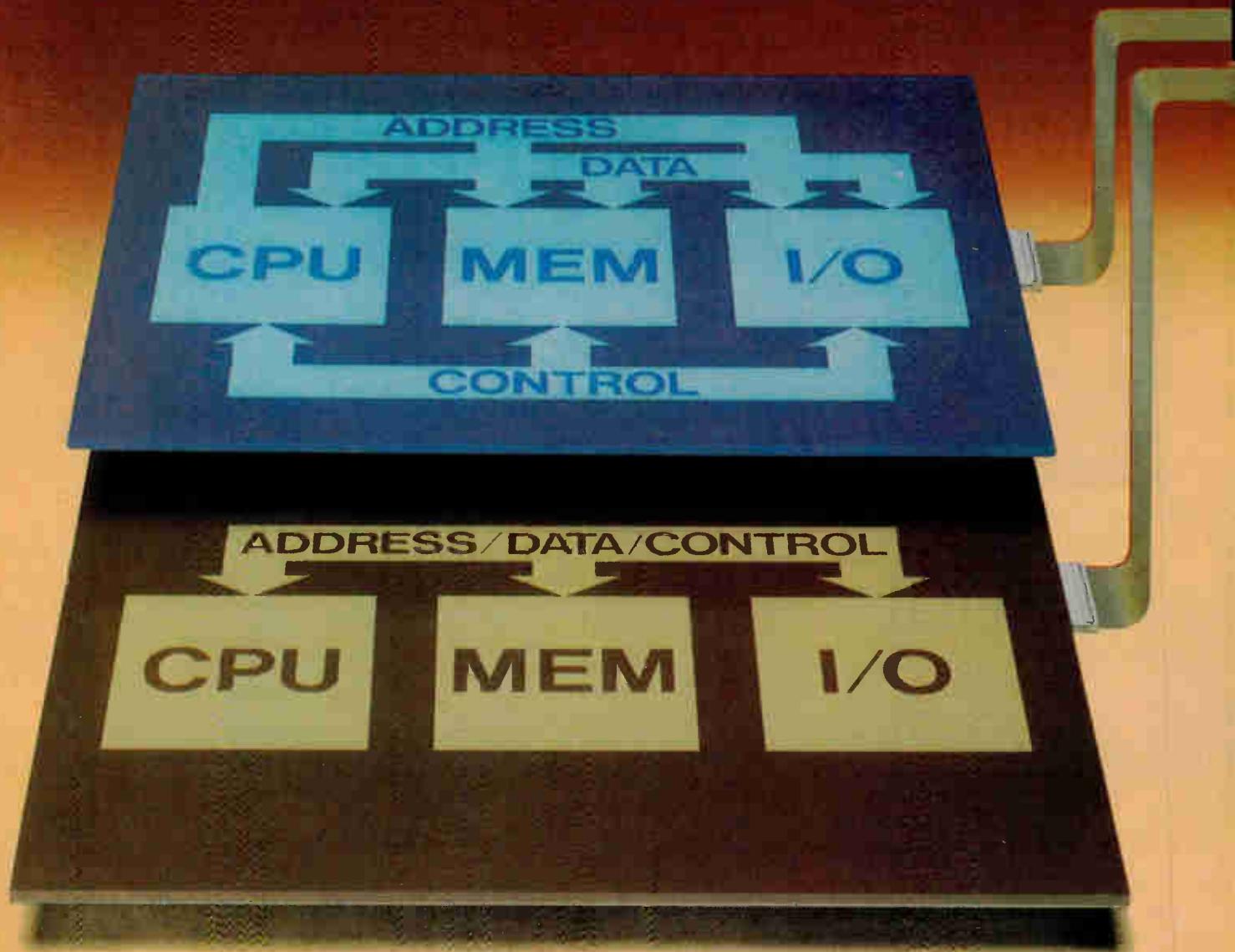
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# and leave the analyzing to HP's 1610B.



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But unlike other analyzers, the HP 1610B can also handle multiplexed-bus analysis just as effectively. The reason? Because with multiplexed buses, addresses and data appear at different times on the same lines. And first-generation logic analyzers, with their single-clock design, simply cannot demultiplex these correctly.

One popular solution to this problem has been to build a two-clock sequential acquisition system into a single package. While this approach will separate out address and read/write functions, it is still inferior to the 1610B. Why? Because this is still not true demultiplexing, in that this technique cannot correct for the real-time differential between the capture of address information and the capture of read/write data.

This means address and data information can be interleaved in the display. It requires the operator to interpret read or write functions. And it means that triggering may occur on false address/data combinations. In other words, it complicates analysis and may lead to false conclusions.

In comparison, the HP 1610B incorporates not two — but three clocks — plus a buffered memory to deliver true demultiplexing. In short, the 1610B can independently monitor addresses, plus read and write data, to demultiplex in real time for efficient and accurate analysis.

So with the 1610B, addresses and corresponding data are displayed as a single line of information, for easy comparison with your original programs. And you're sure that if you trigger on an address-data combination, the data is present at that address at that specific point in the program.

#### Other important capabilities.

In addition, the HP 1610B delivers other capabilities required for efficient state flow analysis of both bus structures. It will store information on a qualified basis, to permit selective editing. Which means you don't have to sort through unnecessary data. And it makes functional measurements, such as time

interval analysis, on the state flow, which speeds analysis and troubleshooting.

#### Flexibility for the future.

Because the 1610B is a 32-bit analyzer with user-selected parameters, and a variety of options, you can use it with both mini and micro based systems, including 8-bit microprocessors such as the Motorola 6800 and the Intel 8085, as well as the newer 16-bit microprocessors such as the Z8000. And, of course, it includes HP's popular menu program format that speeds set-ups and analysis.

#### An economical solution to microprocessor-based systems analysis.

Another good answer to the problem of microprocessor demultiplexing is the 1611A Logic State Analyzer, with HP's general-purpose module. This module incorporates a seven-clock system that allows multiplexed information on common bus structures to be latched into 1611A inputs at the appropriate time for display. If you're already using an HP 1611A, you'll

find this module to be both an effective and cost-efficient solution.

#### For complete details.

The HP 1610B is priced at \$12,500,\* while the 1611A (including the general-purpose module) is \$6,000.\* For more information on these, and for an application note on state analysis of multiplexed microprocessors, write: Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 944-1500, Canada (416) 678-9430.

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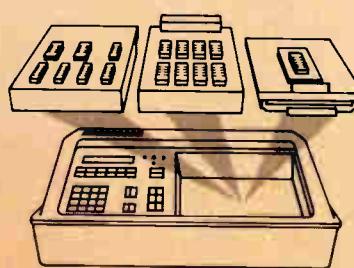
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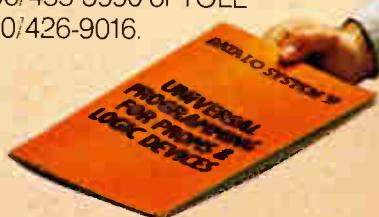
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# DATA I/O

# Probing the news

Analysis of technology and business developments

## Japanese make quality-control pitch

EIA-J tells Washington seminar that secret is no secret, and that IC makers would like to share know-how with U. S. rivals

by Ray Connolly, Washington bureau manager

Japan's semiconductor manufacturers are coming to Washington to correct "misunderstandings" about their rising share of the U. S. market and thus deflect the kind of political criticism that accompanied their countrymen's earlier U. S. sales successes in stereo components, television receivers, motorcycles, cars, and steel. Their message: Japan's quality control is better and productivity is higher—and they would like to share these benefits with their American rivals.

That message got strong support from Hewlett-Packard Co. during a day-long quality-control seminar sponsored by the Electronic Industries Association of Japan. It was conducted at the end of March for an invited audience of approximately 150 congressional staffers, Federal agency officials, and a handful of U. S. industry executives. They were told that HP's in-house tests of 4-K and 16-K random-access memories bought from three Japanese and three U. S. suppliers showed the Japanese ICs to be "consistently better," according to Richard W. Anderson, general manager of the Data Systems division in Cupertino, Calif. The HP test data (see table) represents, Anderson said, "A frightening set of statistics" for U. S. semiconductor markets.

When HP qualified its first Japanese vendor in mid-1977 "to fill the gap in domestic supplies," Anderson said, "prices were competitive with the U. S., but Japan was never the low bidder." After determining that quality of 4-K and 16-K RAMs from Japan was "superior to that of the U. S. devices," Anderson said, HP qualified two more Japanese

suppliers during the 1979 domestic shortage and had the same experience. For HP, the "excellent" results with Japanese RAMs meant fewer rejects, less costly rework, and, most important, "happier customers."

**Called politics.** Peter McCloskey, president of the Electronic Industries Association in Washington, representing U. S. producers, found the HP statistics "very impressive," but he contends that the primary purpose of the EIA-J meeting was "more political—to reduce U. S. protectionist pressures rather than to stress quality control or productivity." In that broader political context, McCloskey believes the Japanese failed to address the primary problem in U. S.-Japanese industrial relations. That, he says, is "fair and equal access to markets" in Japan for U. S. electronic products, including the multibillion-dollar market of Nippon Telegraph & Telephone Public Corp., which is now effectively closed to U. S. producers.

But EIA-J's Washington counsel, H. William Tanaka, suggests that McCloskey may have missed the true message of the Japanese quality-control seminar. "If the U. S. users of IC memories exercise the same discrimination as Hewlett-Packard and find a difference in U. S. and Japanese failure rates," Tanaka points out, "why cannot NTT and other Japanese equipment manufacturers do the same?" While acknowledging some difference between U. S. and Japanese trade policies—differences that are the crux of American makers' complaints—Tanaka argues that a greater threat to U. S. access to Japanese markets in the future "may lie in the perception of Japanese buyers—including NTT—that they cannot be completely confident that they will get U. S. products with failure rates equivalent to those that they can get in Japan."

Intel Corp.'s Robert Noyce, long a critic of Japanese trade policies,

### HP TESTS FAVOR JAPANESE DEVICES

In-house tests by Hewlett-Packard Co.'s Data Systems division of 4-K and 16-K random-access memories from three Japanese and three U.S. manufacturers are shown. Except for the qualification index, figures are in percentages. The index, on a scale of 100, is a composite based on IC quality and repair costs.

Vendor	Incoming tests	Field failure/1,000 h	Qualification index
J1	0	0.01	89.9
J2	0	0.019	87.2
J3	0	0.012	87.2
A1	0.19	0.09	86.1
A2	0.11	0.059	63.3
A3	0.19	0.267	48.1

## Probing the news

"knows the true story of Japanese quality control and what it is achieving," Tanaka maintains. "Otherwise, he would have filed dumping charges against Japan a long time ago."

**Stevenson swings away.** But the political issue of Japanese trade barriers was also raised during the EIA-J session by Sen. Adlai E. Stevenson (D., Ill.), chairman of both the banking subcommittee on international finance and the Commerce subcommittee on science, technology, and space. After delivering a series of biting criticisms of Carter Administration economics, technology, and trade policies (see p. 56), Stevenson urged Japan to "do more to create a climate for cooperation by loosening constraints on the free flow of trade and technology."

Specifically, the senator called for opening of Japanese government procurement, including NTT, to foreign bidders. Japan's "arbitrary customs uplift could be eliminated, tariff reductions accelerated, product standards and product testing and certification systems clarified, and 'buy Japan' attitudes discouraged," Stevenson declared. He also proposed that Japan "invite subsidiaries of foreign firms to participate in its new software cartel" in order to "diffuse tensions."

Japanese semiconductor industry leaders at the meeting held firmly to

their premise that quality control is at the heart of the "misunderstandings" about U.S.-Japanese IC trade. Hitachi Ltd.'s Toshihiko Kubo, leader of the EIA-J contingent, said the Washington seminar for congressional and Federal officials was designed to "lessen misunderstandings" and reduce U.S.-Japanese "frictions" that he believes "stem from segments of the U.S. semiconductor industry."

Increased emphasis on quality control coupled with automated production of ICs could help the U.S. industry overcome its shortage of engineering talent as those techniques have in Japan, said Toshiba Corp.'s executive director Teruyuki Nishijima in a post-session press briefing. Nishijima also proposed that U.S.-Japanese industrial relations be improved by companies in both nations by agreements to share patents, developmental work, and production as second sources.

**Made in America.** Matsushita Communication Industrial Co.'s Hajime Karatsu pointed out that 50% of the automated production equipment, including large-scale integrated-circuit bonding machinery, used in Japanese plants to achieve high quality control was manufactured in the U.S.

Karatsu's message for U.S. manufacturers and engineers was that the key to quality control is not to increase production line tests and inspection to weed out inferior prod-

ucts. Rather, he advised them to eliminate potential failure sources at the point of product design, thus precluding the need for extensive inspection and testing.

Karatsu's stress on design and automated production as quality control keys was supported by HP's Anderson, who recalled being asked by a Japanese engineer, "Why do you Americans inspect so much? Don't you have confidence in your products and processes?" Anderson argued that Japan's competitive IC position in the U.S. stems from the Japanese turn to production automation in order to counter rising costs in the 1970s, whereas U.S. products turned instead to low-cost offshore assembly. In Anderson's view, Japan gained an advantage by employing quality control to "build ICs right in the first place," but American producers employed quality control for the more costly process of "finding and fixing" defective circuits produced offshore.

**Is there time?** Though J. M. Juran, one of the pioneers of modern quality-control techniques and a consultant to Japanese producers, told the session that he believes Japan is now too far ahead in automated quality output of ICs for the U.S. to catch up, Anderson believes American producers could cut IC failure rates and match Japanese quality over a three-year cycle. "You have to invent out defects" in product design, Anderson told the seminar audience, "not beat on production people."

For the U.S. to match Japan's IC quality levels, however, Anderson believes American producers must change their attitudes and commit themselves to new goals, and then work with the Federal government to increase levels of research and development. The HP executive then reiterated for the audience of Government officials a list of Federal support programs for industry being pushed by the American Electronics Association, including tax reductions to enhance investment capital, as well as accelerated depreciation schedules for new plant and equipment. Nevertheless, Anderson conceded that he sees no chance of adoption of any of these proposals by Congress this year. □



**Quality words.** J. M. Juran, left, the quality-control expert, at the EIA-J seminar in Washington with Hajime Karatsu, managing director of Matsushita Communication Industrial Co.

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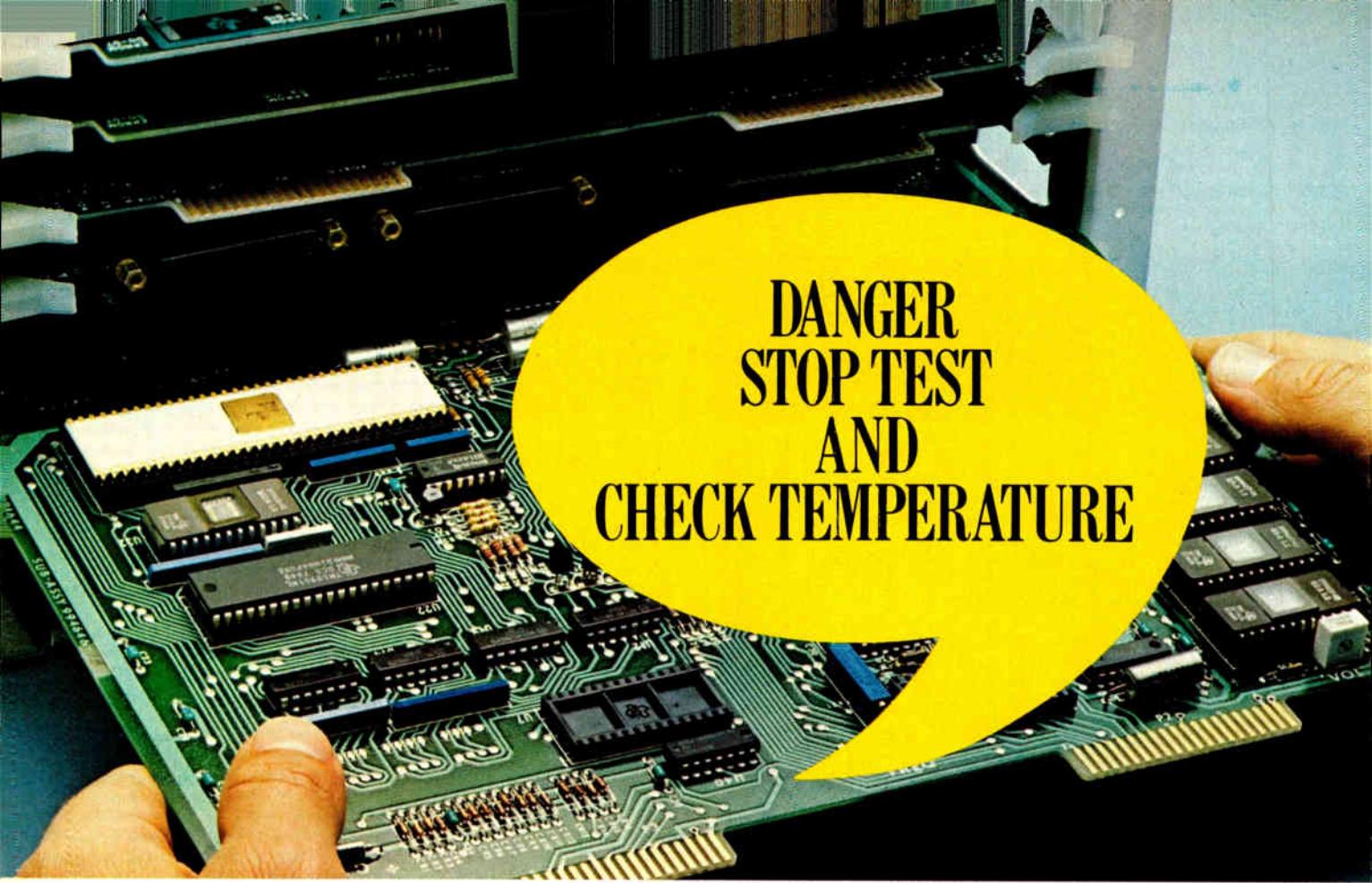
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Circle 83 on reader service card



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**TEXAS INSTRUMENTS**  
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Letter from the Midwest

## Weather milder, prices wilder

Component makers and customers find rising cost of materials means changes in design as well as purchasing arrangements

by Larry Marion, Chicago bureau manager

The cold hardly touched the Midwest this winter, but executives from the region's electronic component makers found themselves in a cold war—between buyers and sellers of switches, connectors, and other components. Sharply escalating raw-material costs led to surcharges on precious metals and frequent general price increases.

At one point, one component maker had to add a 30-cent silver surcharge to a 40-cent switch, for example, and 10% surcharges are still prevalent despite the recent respite from February's \$800-an-ounce gold prices.

Skyrocketing prices of gold, silver, other metals, and plastic resins in the last few months shattered the serenity of the industry and some of its basic operating principles. Materials costs now exceed manufacturing manpower costs and are closing in or equaling total labor costs. Explains Walter L. Cherry, chairman and president of Cherry Electrical Products Corp., Waukegan, Ill., "It all happened so quickly. Materials costs used to be secondary to manufacturing costs."

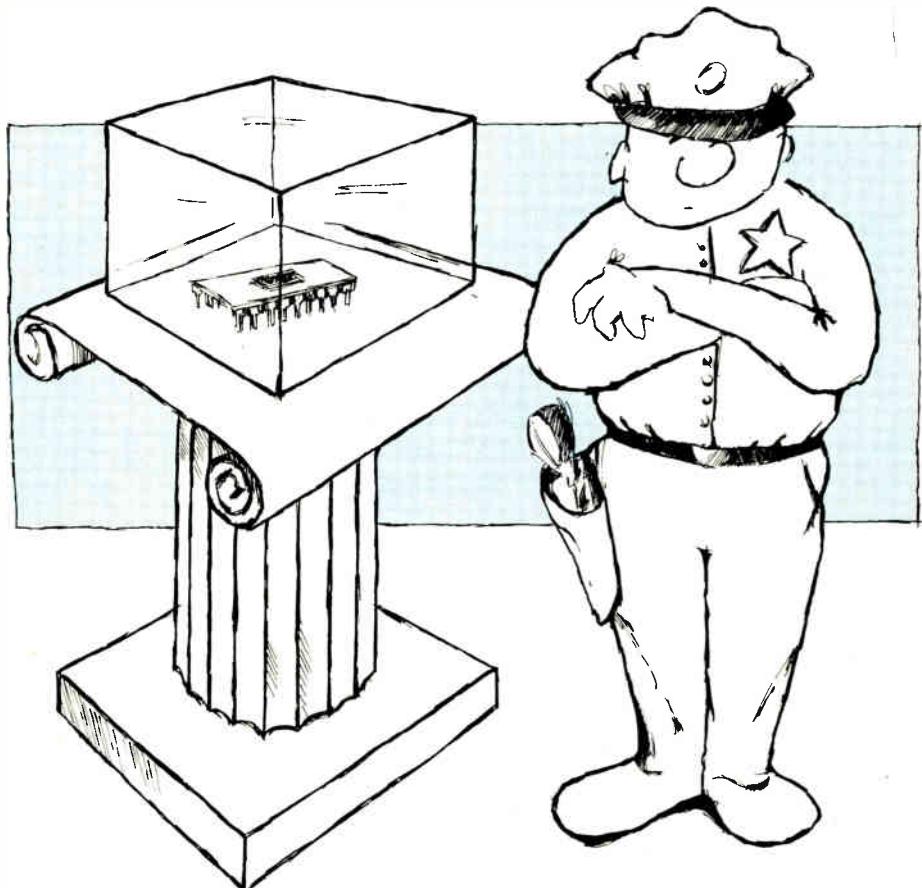
In the good old days—six months ago—most component makers included a small precious-metal surcharge on bills to some, but not all, of their customers. Consumer product assemblers, such as chronically hard-pressed television set makers, were frequently exempted from the adders based on gold and silver content of connectors and switches. But as gold and silver prices doubled and almost tripled on the commodity markets, the component makers tried to incorporate across-the-board surcharges to their customers.

"Some people got quite nasty about it," recalls Don J. Fleming, marketing vice president at Robinson Nugent Inc., New Albany, Ind. Though the majority of customers of component suppliers like Robinson Nugent, Cherry, and Nolex Inc. of Lisle, Ill., reluctantly accepted the surcharges, a few switched suppliers.

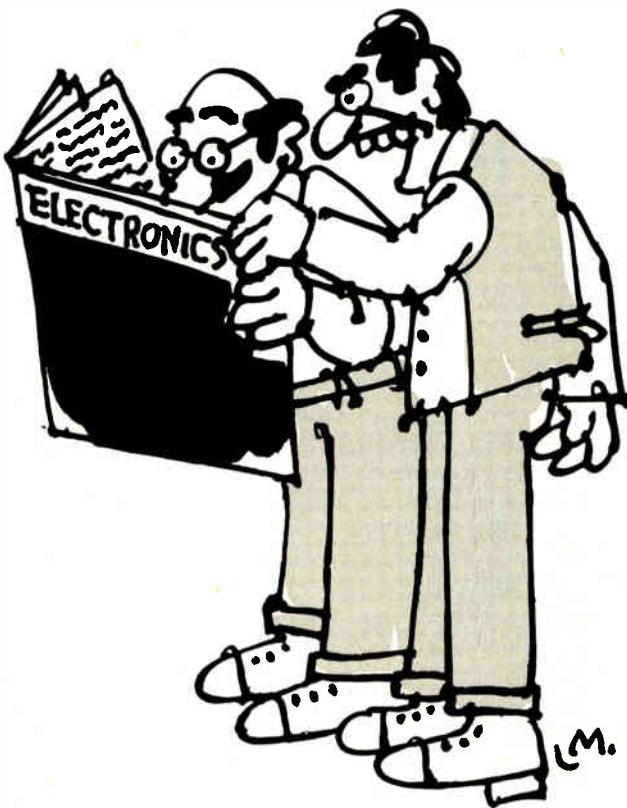
However, some consumer electronics companies stuck to their contract terms, refusing to accept surcharges. Charles Quinn, purchasing manager of RCA Corp.'s Consumer Electronics Group in Indianapolis,

says that RCA's combination of multisource agreements, purchasing power, and a firm policy of insisting that suppliers honor contract agreements shielded it from paying the adders that suppliers requested.

**Fast rises.** Surcharges are not the only sore points between component makers and their customers. Frequent price increases were unknown in the industry until a few years ago, but semiannual boosts of 5% to 6% each are now the rule, as past productivity and technology improvements fail to keep pace with the



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## Probing the news

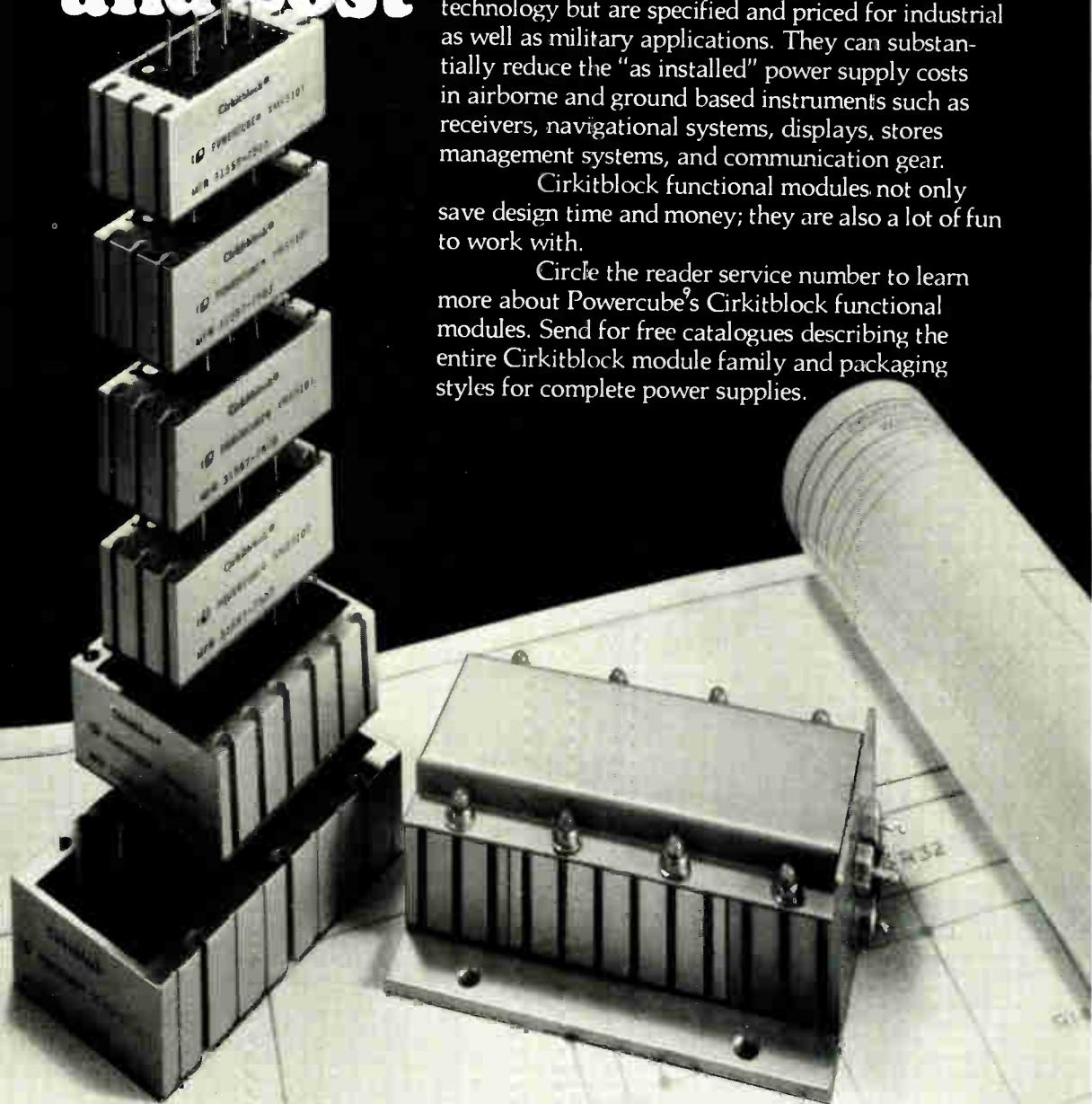
escalating cost of plastic resins.

Materials substitution, something component makers suggested to unwilling customers several years ago, is suddenly catching on, says John H. Klein, materials manager at Molex. Selective gold plating of contacts, and substituting tin over nickel for gold in some applications, has rapidly become an attractive alternative, he reports. Reduced materials costs from selective plating enable Robinson Nugent to drop its gold surcharge, and Molex has two new alternative technologies under development that produce conductivity and anticorrosive characteristics similar to gold, Klein reports. And instead of depending on materials substitution to contain their prices, component makers are also redoubling cost-reduction efforts in areas like purchasing.

**Automation helps.** Increased automation is another step to lower production costs, and companies like Panduit Corp. of Tinley Park, Ill., are planning increased capital expenditures to improve productivity. Walter Cherry says he is cutting back inventories to reduce costs and become a more efficient operator, and Molex is boosting inventories to reduce lead times and improve delivery rates. Oak Technology Inc. in Crystal Lake, Ill., a division of Oak Industries, is doing some of each—the company shows a 50% reduction in the number of custom rotary switch parts in the inventory, and new equipment to automate the production of the new standard items in its catalog.

The price of these wrenching changes has been high—profit margins at Cherry, Methode Electronics Inc. of Chicago, and CTS Corp. of Elkhart, Ind., have shrunk in the last quarter. However, despite the vanishing profits, frazzled nerves, and chaotic conditions, the cold war is leading to a warming thaw: Cherry reports that his customers and internal designers now have "healthy cooperation," as both sides fine-tune procurement specifications and examine alternative materials and processes to replace gold, silver, and other volatile commodities. □

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Companies

# UTC's parts add up to \$2.5 billion

That's what United Technologies' newly formed Electronics Group, with Mostek at its core, expects to gross this year

by Pamela Hamilton, New York bureau manager

An electronics giant has quietly been put together in Hartford, Conn., that can now claim 53,000 employees and expectations of \$2.5 billion to \$3 billion in sales this year. That could put it ahead of Digital Equipment Corp. (\$1.8 billion in 1979) and Hewlett-Packard Co. (\$2.36 billion).

The Electronics Group of United Technologies Corp. is the result of a major reorganization late last year that has left the corporation in a better position to integrate leading-edge technology into all of its varied product lines. The group's blue chip is the recently acquired Mostek Corp. [Electronics, Oct. 11, 1979, p. 100], the Carrollton, Texas, semiconductor manufacturer, which promises to fuel the group's growth

and to be the focal point of much technological innovation.

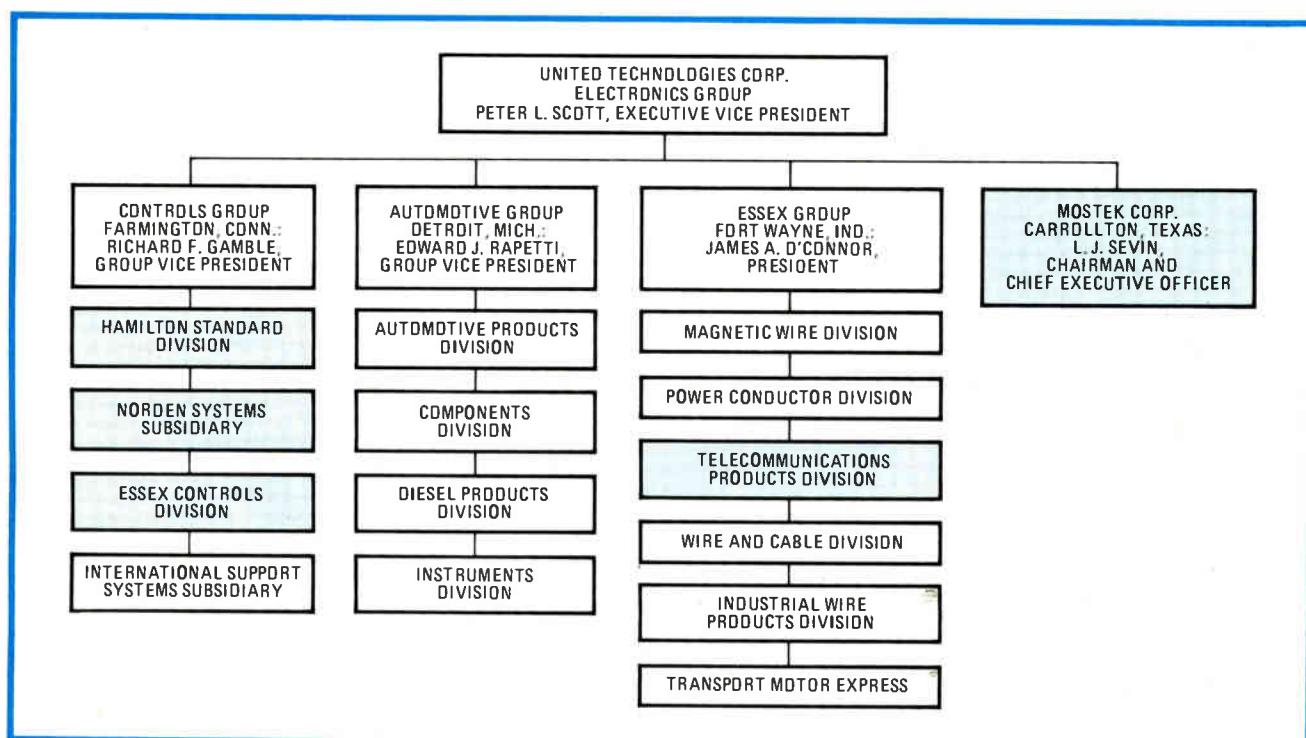
The conglomerate known as UTC has long been known for its expertise in the aircraft and space industries, most notably its Pratt and Whitney division. And with the acquisition of Otis Elevator Co. in 1976, and Carrier Corp. in mid-1979, UTC has positioned itself well in the commercial-industrial marketplace. Also a key element lately has been Norden Systems, the military supplier in Norwalk, Conn. [Electronics, March 2, 1978, p. 82]. In fact, the man who has the line responsibility for the new group comes from Norden.

Peter L. Scott had led Norden during the five years since he joined UTC, changing it from a sluggish

product-oriented military supplier to a dedicated systems bidder. And in those five years it has doubled in sales—from \$50 million in 1975 to about \$100 million this coming year.

Scott, who has been heading the Electronics Group since the end of November, has similar plans for this enterprise; the group should be one of the primary areas of growth for UTC during the 1980s. Last year, UTC had total revenues of \$9.1 billion, up from \$6.1 billion in 1978. The net income for 1979 was \$325.6 million, up 39% from \$234.1 million.

**Leadership.** Although the acquisition of Mostek gains UTC an immediate source of semiconductor knowledge and products, Scott is quick to point out that this was not



the primary reason for the purchase. "We bought Mostek because it was a leader in its market segment. We didn't buy it just as a captive source for our own [semiconductor] needs." But with semiconductor technology expected to spread throughout various industries over the next 10 years, Scott readily admits that Mostek puts UTC in a much better position.

"The common thread of the next decade's growth will be semiconductor-oriented, especially in LSI and VLSI," says Scott, who considers himself, along with chairman and chief executive officer Harry J. Gray, a prime mover in acquiring the semiconductor firm. "We recognized that trend and the fact that we needed that capability." He adds, "Mostek will definitely be a benefit to the rest of United Technologies."

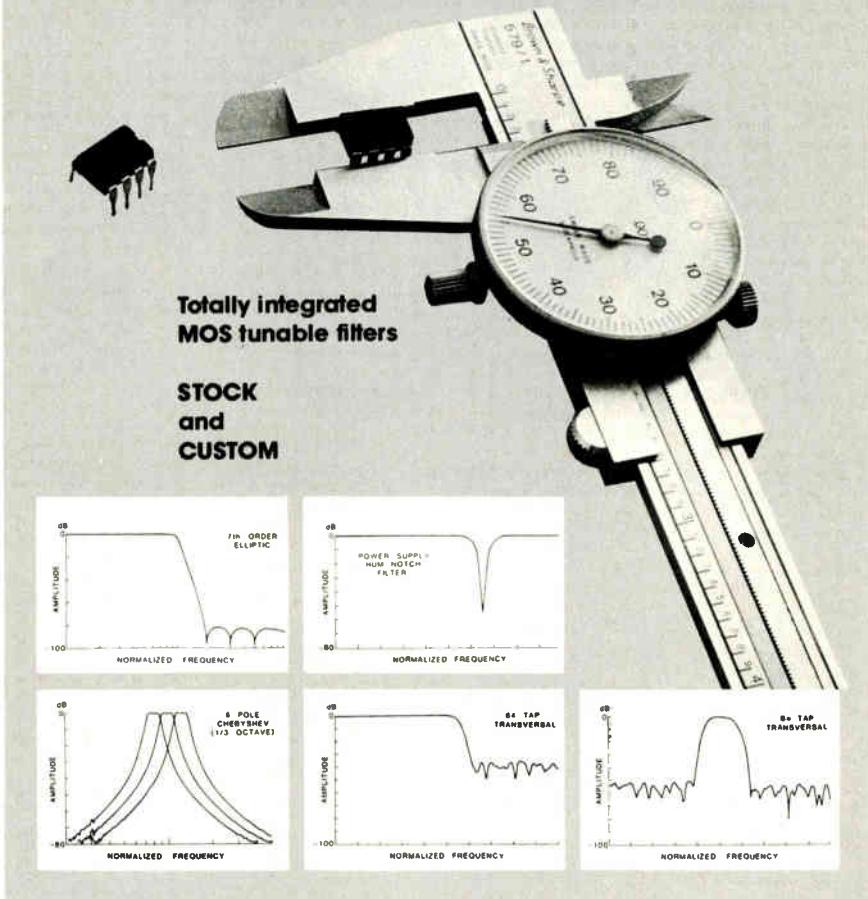
Mostek is expected to do \$350 million to \$380 million in sales over the next year, according to Scott. That is an increase from \$134 million in sales in 1978. But UTC will have pumped over \$120 million in capital investment into the semiconductor concern during the coming year, including building a new 250,000-square-foot facility in Colorado Springs.

**Technological edge.** As far as technology goes, Mostek will give UTC an edge in its current projects, as well as longer-term endeavors. "It was a good acquisition for both," notes Michael J. Krasco, vice president, securities, at Merrill Lynch, Pierce, Fenner & Smith of New York. "Mostek needed access to cash, and United Technologies needed access to technology."

Areas where Scott sees semiconductor technology being applied in the near future include military systems ("the impact of VLSI on military systems will be great," he observes), the next generation of jet engines, and telecommunications systems using fiber optics. "The semiconductor business is a flywheel for prolonging and increasing growth," Scott declares.

Scott intends to set up an advanced research and development center for his Electronics Group, to look at applications for microelectronics. He plans to use this applied research laboratory to explore areas such as semiconductor technology;

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### **Probing the news**

optical advances—including aspects of fiber-optic research—as well as all kinds of sensor development; he sees sensors being used in such diverse environments as measuring manifold pressure in cars, calculating the number of people in an elevator and for use in military applications.

Scott does not, however, intend the center to operate as a research facility for all of UTC, but primarily for the benefit of the Electronics group. He will also be directing the group toward more software development, an area in which he believes costs will skyrocket over the next few years. "Systems development is personnel-oriented because of the software. And to understand software, you have to know hardware," he explains. Once again, Scott is convinced Mostek should be able to give some direction in this area. Mostek also sees the center as a boon as the company enters the high-priced VLSI era. Says Gordon Hoffman, Mostek's manager of strategic planning, "Our view of future technologies fits well with UTC's view of R&D spending."

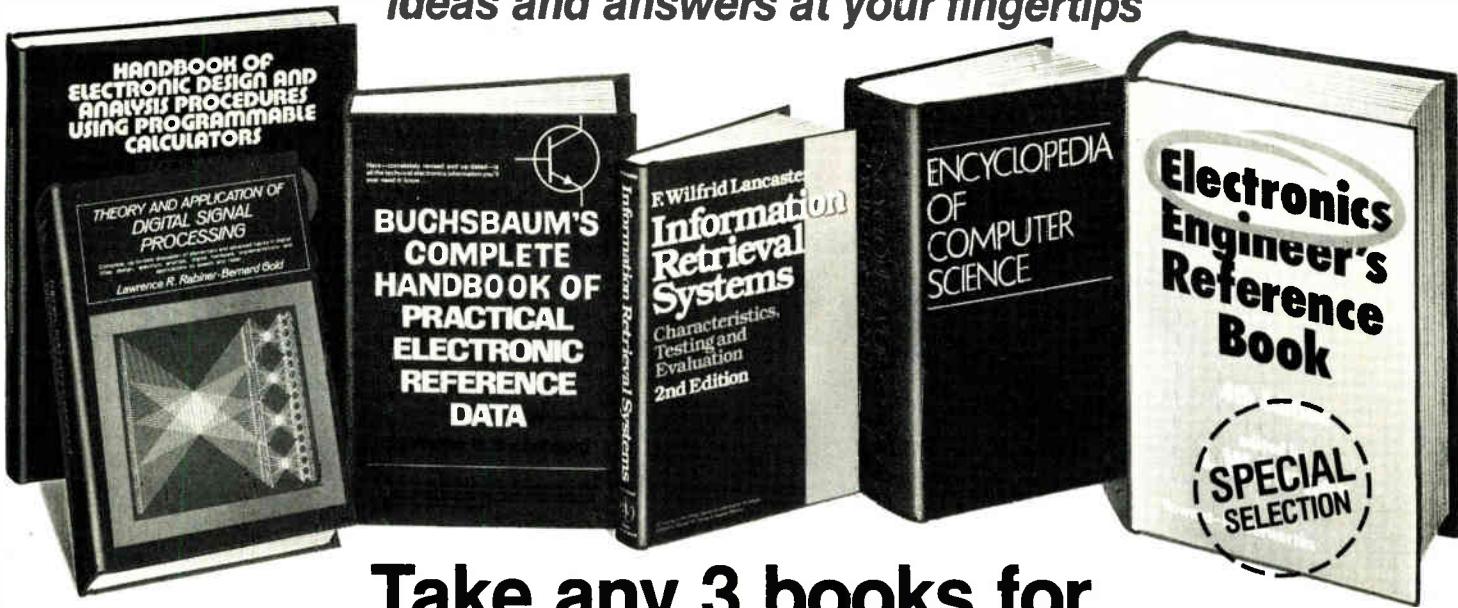
As more and more of UTC's products and services become electronics-based, Scott's group will become of greater value to the corporation. "It was a reasonable, intelligent move on United Technologies' part," says Howard Mager, vice president at New York investment firm L.F. Rothschild, Unterberg, Towbin, in regard to the realignment at UTC. "The company is trying to get the most out of its internal strengths, and is looking at how best to utilize that [high-technology] capability. The acquisition of Mostek makes for a centerpiece," he adds.

And for Scott, who is aiming at doubling the size of the Electronics Group over the next five years (much as he did at Norden), the growth curve of the group may well exceed the overall growth of UTC. "Doubling in five years means growing at a rate of 15% per year. If you're growing at that rate, you're staying at the leading edge of technology," he says. And Scott fully intends to keep his group at that leading edge. □

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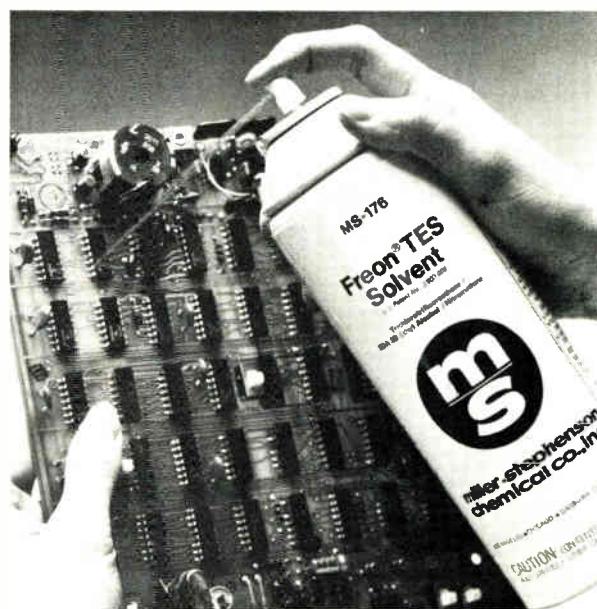


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The Economy

# Carter program leaves 'em cold

Electronics executives say it does not go far enough, or that it will have no effect; actions of Fed draw more interest

**Reactions of electronics industry executives to President Carter's economic package range from calmly resigned to unprintably exasperated. But the consensus in a nationwide sampling is that it is not going to help much.**

Briefly, what the President announced on March 14 was a multi-pronged attack on inflation. He called for reduced Federal spending, curbs on credit, increased energy conservation, and voluntary restraints on prices and wages. Says Bernard L. Schwartz, chairman of Loral Corp. of New York City, "The Administration overpromised and underdelivered." More charitable was Reginald H. Jones, chairman of General Electric Co. in New York, who decided that the program was "a step in the right direction but inadequate." And Robert A. Lineberger, vice president for finance at Beckman Instruments Inc. of Fullerton, Calif., believes that "the President's program did not take a heroic stance, so it will have no effect."

Getting down to specifics, Richard Campbell of TRW Inc.'s Electronics

group in Los Angeles agrees that the program will not trigger major changes. Campbell, executive vice president, points out that sales even to the strong markets—such as telecommunications equipment—have softened with those customers about to spend big money on capital equipment showing "a good deal of watch and wait."

But TRW may be peculiarly suited to cope with the 20% inflation rate of the U.S. because it has experience with operating in nations with high inflation rates, like Brazil. In fact, Campbell jokes that "maybe the answer is we have to start importing Brazilian accountants." As for predicting inflation's impact, TRW has what it calls the rule of 72: divide 72 by the inflation rate to determine how long it will take for costs to double. At 20%, the answer is 3.6 years; at 12%, 6 years.

Among computer makers, most are reluctant to have their votes recorded. However, one who is not is Frank S. Madren, director of product planning and management at Prime Computer Inc. in Wellesley

Hills, Mass. He does not think that the computer community faces the hard times of, say, the auto or housing industries, but he is concerned about the availability of money. To Madren, the role of the Federal Reserve Board in regulating the money supply and the discount rate matters more than any presidential initiative (see "The Fed's action gets results," below). He believes that we are now on the leading edge of the recession, but has not seen any softening of orders. "We don't even have any solid evidence of stretch-outs," he says.

**Volcker fan.** In the Midwest, the accent too is on Federal Reserve action. Walter L. Cherry, president of Cherry Electrical Products Corp. in Waukegan, Ill., says that "[Federal Reserve Chairman] Paul Volcker is the lifesaver in Washington" and any Carter budget cuts are too little and too late. Cherry says that the weak auto market, among other factors, means that the recession is here now and that it will stay a year, but Kerry M. Krafthefer, vice president for sales and marketing at Molex Inc., a Lisle, Ill., connector and component maker, is more pessimistic. He says a recession lasting 20 to 30 months is on the horizon.

Curbs on consumer credit are of major concern to companies like RCA Corp.'s Consumer Electronics division in Indianapolis. There, Jack K. Sauter, vice president and general manager, assesses the possible affect against a background of booming color-television sales. Customers buying replacement sets have led that industry to a first quarter where sales moved along at a 10-million-set annual rate; however, Sauter expects

## The Fed's action gets results

Even before President Carter decided to offer a program to help cure the nation's economic ills, the Federal Reserve Board made a move of its own. Last October, the Fed decided to tighten credit. Among its actions were an increase in the discount rate from 11% to 12%, a tightening of some reserve requirements, and a policy of slowing the growth of the money supply.

The result, according to a survey made in January and February by the McGraw-Hill Publications Co. Economic Department, has been a reduction by about \$1.5 billion in 1980 capital spending plans of U.S. companies. As for electronics companies, they fall into several classifications in the survey. For example, 9.4% of electrical machinery makers responding will reduce outlays a total of 5%, while 33.3% of the instrument makers will chop 35.8% out of their budgets. The aerospace industry plans no cuts.

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Look back - 31 words  
Breakpoint location - 1 word
- 30-channel data collection - recording microprocessor's address bus, data bus, four status bus lines, two user selectable inputs.
  
- Six modes of operation: Step, Read /Write, Breakpoint, Examine/Trap, Examine/Read, Window/Read.
- Recorded instructions cycles are displayed sequentially
- Multiple selected breakpoint condition, generated by combinations of selected data, control address and external inputs
- Offers bit-picking capability

- "Bit Select" selection switches in the data, address, control, external input lines for setting up selected breakpoint conditions
- Selected address, selected instruction, selected command or an external input can be used to generate the selected breakpoint condition
- A selected breakpoint can be initiated after the breakpoint condition has been present a selected number of times
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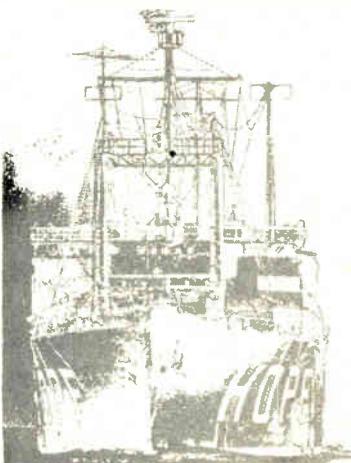
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## Probing the news

the year to close out with 9.2 million units moved, an indication that TV demand will soften even beyond the recessionary level as credit procedures tighten.

At Analog Devices Inc. in Norwood, Mass., Selwyn Rabins, manager of strategic intelligence, expects the consumer sectors of his company's markets to suffer. Analog's best insulator against any sales loss due to Carter's curbs is the fact that about half its business is export based. But, Rabins says, "we still haven't seen the top prime rates. I expect 21% or 22% fairly soon, and prime could go much higher. However, I think it could be on the way back down in six months or so."

**Lookin' good.** The eyes of Texans are focused upward. For Texas Instruments Inc. in Dallas, "there has not been any slowing of our order rates," says a spokesman. "our semiconductor backlog is strong and the same is true of our minicomputer business."

Richard V. Palermo also exudes optimism. Palermo, executive vice president for operations of Datapoint Corp. in San Antonio, says, "Our order rate continues to be higher than ever before. We have been watching for cancellations, switches from purchase to lease, or any of the signs that might indicate that tighter money and recession may be starting to affect our portion of the computer business, but so far we don't see any signs."

In the semiconductor industry, the President's promise of hard times will not change the price situation, says Ben Anixter, director of product marketing at Advanced Micro Devices Inc., Sunnyvale, Calif. "Prices in the industry have been going down, and hard times won't change this," he says. But money will cost dearly for a long time, he maintains, disagreeing with those who say a recession is here. "Until we have a recession—and who knows when that will be—we won't see a lessening of interest rates." □

Reporting for this article was provided by Larry Marion in Chicago, Wesley R. Iversen in Dallas, James B. Brinton in Boston, Larry Waller in Los Angeles, and Bruce LeBosc in Palo Alto.

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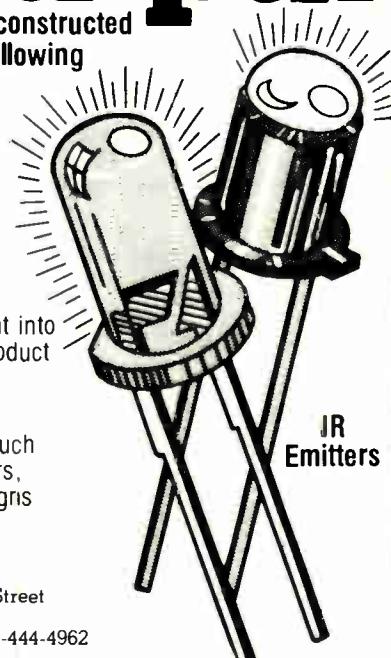
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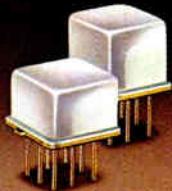
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# At Boeing, forty dedicated systems Tektronix 8001s

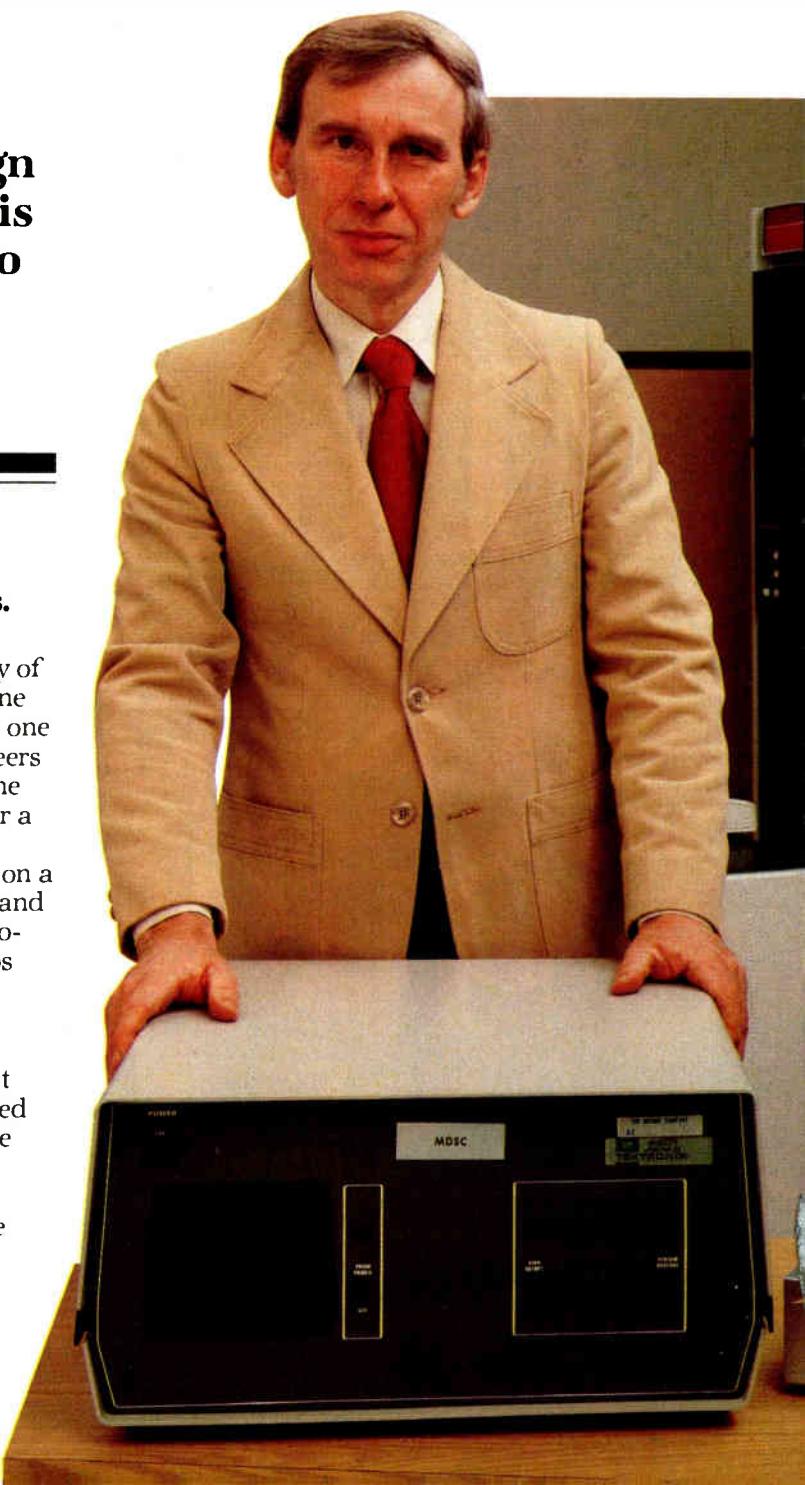
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Before the creation of the MDSC, Boeing used a variety of different vendors' stand-alone development systems. Each one supported only three engineers at a time, and more than one system was often needed for a single project.

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# PMI Introduces Buffers Designed As Buffers for Buffer Applications

*Another Invention from  
The White Knights of Linear Wonderland*



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Lewis Carroll fashioned the White Knight in *Through The Looking Glass* after himself: a kindly soul who compulsively invented ways to do things better. Like spiked iron anklets for horses to guard against shark bites. Or pudding made from blotting paper because it absorbed more flavor. Or a way to keep hair from falling out by training it to grow up a stick in the center of the head.

"Things never fall upward," he told Alice. "It's a plan of my own invention!"

It's easy to see why Carroll identified with the character, since the author had a few inventions that were ahead of their time: a traveling chess set with

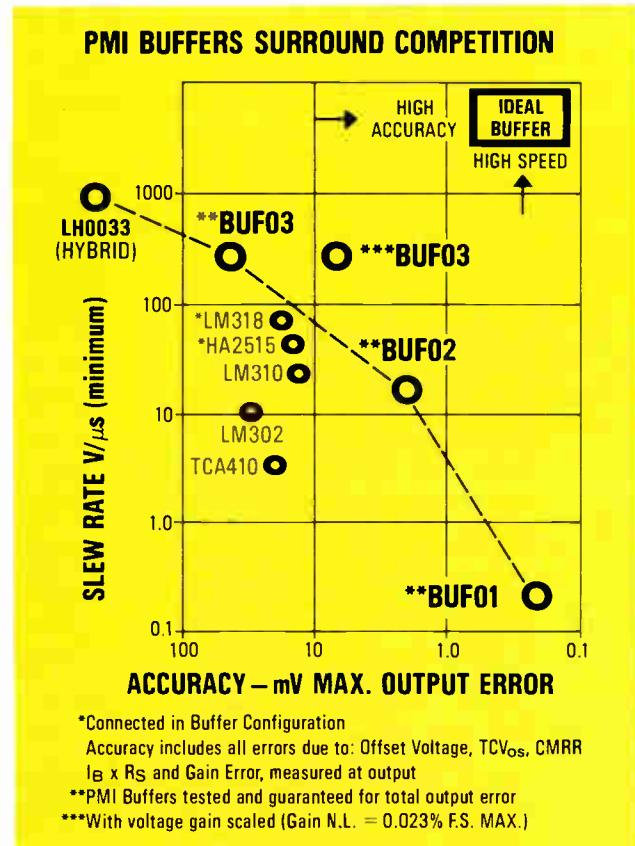
holes to hold pegged pieces; an organ that played when you pulled punched paper tape through it (long before player pianos); and a game in which you moved letters around a board to form words, a century before "Scrabble" became the rage.

It's also easy to see why PMI identifies with the White Knight. We've got a room full of them, all trying to find better ways of doing things for design engineers. Their latest invention is a family of analog buffers that are designed to be buffers, not just op amps which have to be connected in a voltage follower mode.

Consider the wonderment of their inventions: the BUF-03, BUF-02, and BUF-01, the first buffers in all

of Linear Wonderland specified with a guaranteed maximum error. Our White Knights came up with a buffer for everyone, so pick the one that's right for your speed requirement, plug it in, and forget about any error analysis.

The BUF-03 is for those engineers who are really looking for speed. With a slew rate of 300V/ $\mu$ sec, it offers a 5-to-1 increase in speed over any other monolithic buffer now available, while maintaining excellent DC accuracy. Not only that; it will handle any capacitive load you care to attach to it.



Our White Knights have made the BUF-03 available in both packaged and chip form so that your White Knights could use it in high frequency filters, to build super-fast sample and holds, to drive cable shields, or in a variety of video applications.

The BUF-02 is the right buffer if you want accuracy but don't care about all that speed. It has a specified maximum error of 2.5mV over the full temperature range and a slew rate of 24V/ $\mu$ s. Use it in any buffer application requiring better than 0.025% accuracy (10V full scale) when processing full power frequencies less than 350kHz. You no longer have to settle for a slew rate that's lower than your frequency requirements dictate, just to improve accuracy!

As for the BUF-01, PMI's White Knights knew there were those in Linear Wonderland who needed

a buffer just right for low-speed applications where super accuracy was still important. That's why the -01 couples an 0.3V/ $\mu$ sec slew rate with a guaranteed maximum error less than 250 $\mu$ V. This performance makes it perfect for A/D or D/A systems with 12 to 14 bit accuracy requirements, for data acquisition systems whose full power signal frequencies are less than 3kHz, or any high accuracy system where stability really counts.

If all this sounds like the impossible dream, challenge our White Knights. Just fill in our "BUFFER IN SHINING ARMOR" coupon to get a free sample—either in packaged or chip form. Or go ahead and order now, if you like, from your favorite PMI distributor. And while you're at it, be sure to ask for the AN-40 application note, which will show you how our buffers that are really buffers can be used in a variety of applications.

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# Calculatorlike controller teaches precision multimeter new steps

Optional keyboard lets user configure 5½-digit unit for physical as well as electrical measurements using program storage modules

by Lee Meyer, *John Fluke Manufacturing Co., Mountlake Terrace, Wash.*

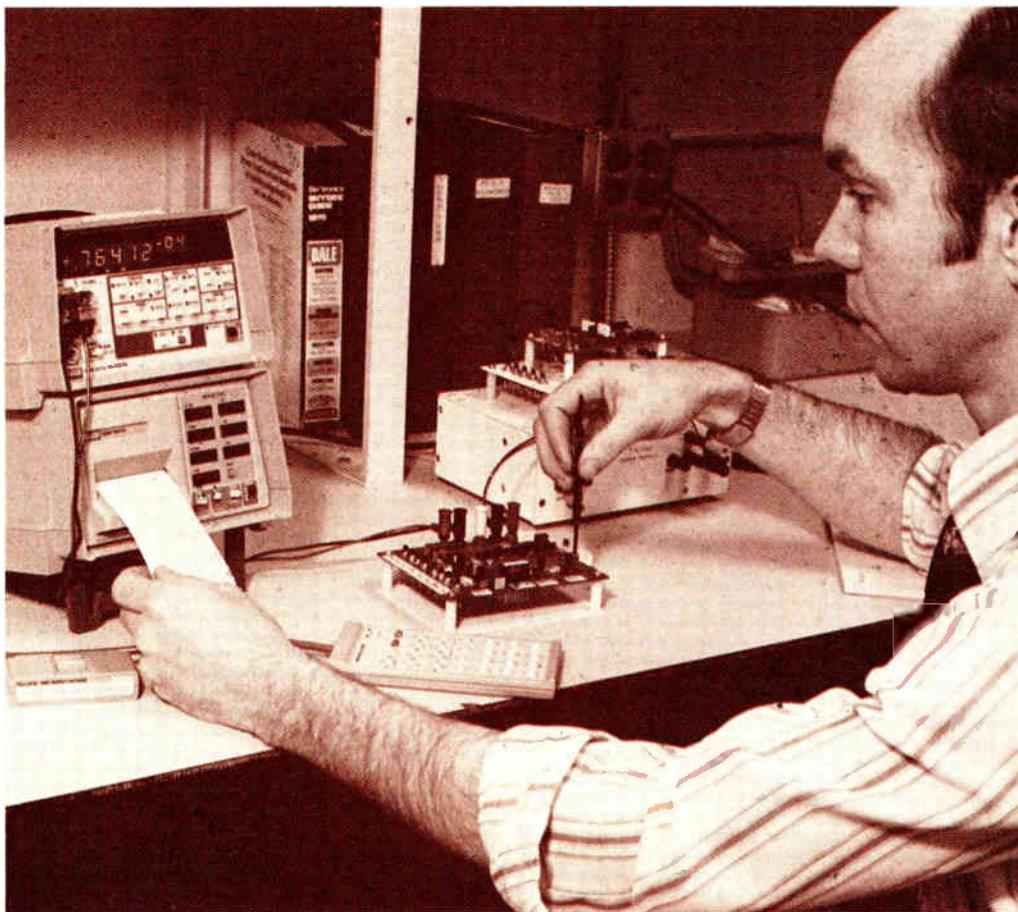
□ In a relatively short time, the microprocessor has greatly expanded the capabilities of instruments. It has been used not just to enhance their reliability by reducing their parts count but, more significantly, to increase their accuracy by means of special algorithms. This development has improved instrument performance in a most fundamental way, one that benefits all engineers.

Now, the introduction of the 8860A and its calculating controller option points the way for intelligent digital multimeters. A 5½-digit meter, the 8860A has all the capabilities of precision voltmeters, but enhances them with a keystroke-programmable, calculatorlike detachable

keyboard that gives users access to an internal processor. The keyboard allows users to write and execute programs that configure the DMM, store readings, and solve complex algebraic, trigonometric, and statistical formulas.

For DMMs, the label "intelligent" encompasses a number of hard (or built-in) mathematical functions, including display offset modes, where a constant is subtracted from the reading before it is displayed, and automatic scaling, where the reading is multiplied by and added to a constant.

Automatic math functions such as conversion to deci-



**A meeting of minds.** To check out a measurement program that controls the 8860A DMM, the author uses the easily attached 2020A instrumentation printer on which it rests. Programs for the 8860A—entered on the keyboard shown—are stored in detachable, battery-powered modules like the one near the author's left hand.

## Tandem processing

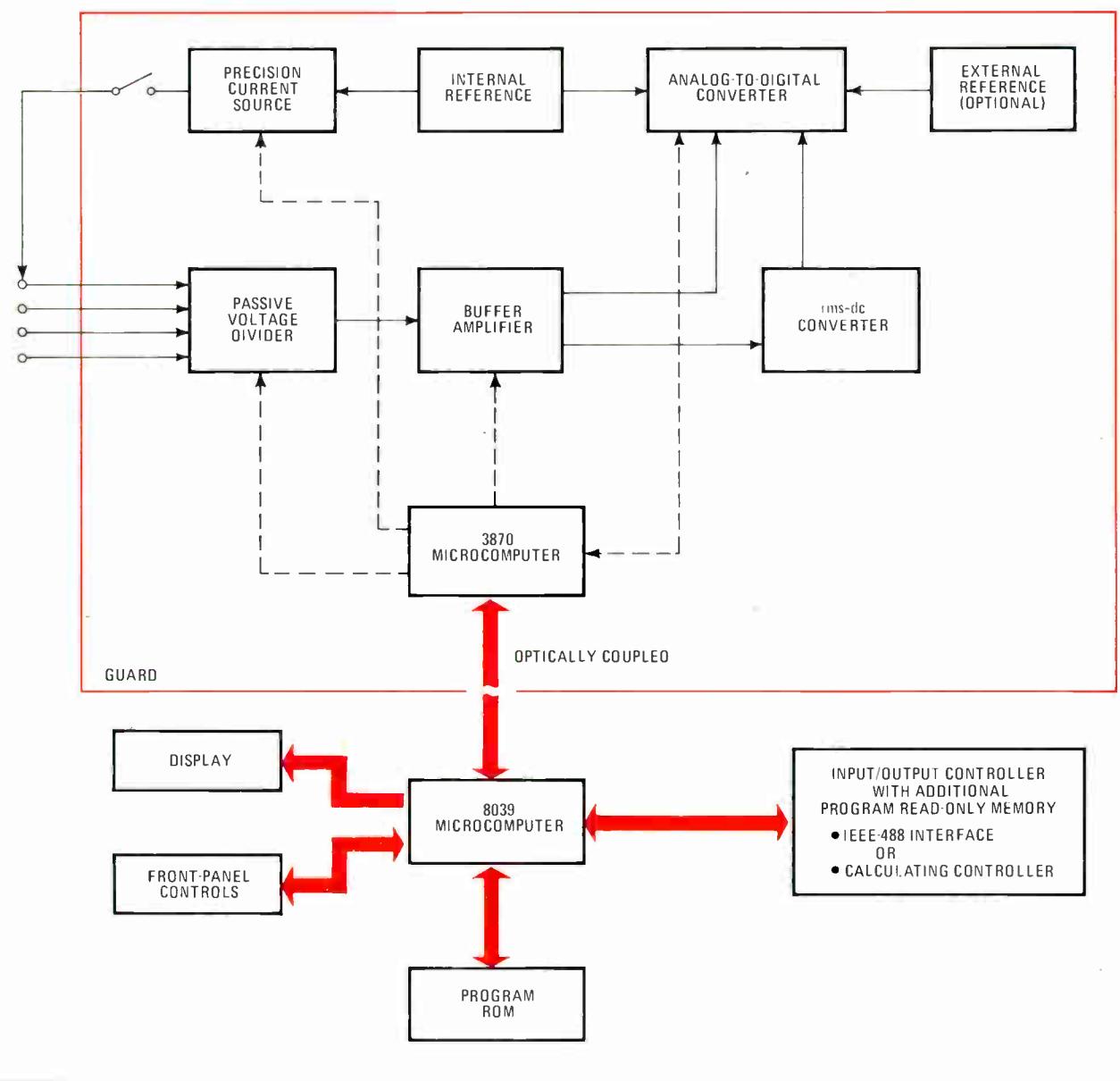
Operation of the 8860A is controlled by two one-chip microcomputers, Mostek's 3870 and Intel's 8039. The 3870 configures the meter's analog section, setting the passive voltage divider and buffer amplifier and providing the timing, counting, and control functions for the a-d converter. Since it deals with the analog portion of the meter, this processor is located inside the analog guard enclosure that prevents the incoming signal from being distorted by outside interference.

A single input circuit made up of a passive input divider, and a buffer amplifier provides input scaling and buffering for all measurements. This approach allows the 8860A to have a 200-millivolt ac voltage range, which is unusual for a 5½-digit multimeter, and therefore a 1-microvolt resolution. It also allows a 10-megohm input resistance for ac measurements, which is 5 to 10 times greater than that of most 5½-digit meters. The ac bandwidth is 300 kilohertz.

The 3870 acts on information from and supplies mea-

surement results to the 8039, which is external to the guard circuit. To maintain the guard's integrity, the communication path between the two processors is optically coupled. The 8039 scans the front-panel controls for control input, or receives control commands from an input/output option card. It transmits configuration and trigger commands across the guard; receives measurement data back; performs offset, limits test, peak-to-peak or other math functions if required; and sends the result to the display or an input/output option.

One edge-card connector in the instrument accepts either the IEEE-488 interface option or the calculating controller option: the two I/O options have similar architectures. In each case, the circuit board contains circuitry specific to the I/O function, and a program ROM. The option is operated by the 8039 microprocessor in the basic instrument, using the program in the ROM on the optional circuit board.



bels, thermocouple linearization, automatic limit testing, and average and standard-deviation calculations are becoming common, and the 8860A handles them, too. Functions such as these make the user more efficient by automatically performing the calculations he would otherwise have to grind out himself.

An area of instrument intelligence that has developed more slowly than the other has been soft, or user-definable, math functions. Soft functions provide the user with the means to program into the DMM whatever formula or test he requires for his application. The 8860A offers that capability, which allows the user to read the output of optical sensors directly in lumens or foot candles, calculate force from the output of an accelerometer, or analyze the output of a power supply to determine the percentage of ripple.

The 8860A is an excellent indicator of the progress that is being made in intelligent DMMSs. It has three overall configurations—bench DMM, user-definable DMM, and IEEE-488 DMM.

### **The bench DMM**

Like other laboratory DMMSs, the 8860A is a precision high-performance meter. Adding intelligence to a meter of lower quality would have been like harnessing a greyhound to a dogsled: the swift and capable processor would be held back by the meter's low performance.

The basic 8860A is a 5½-digit unit with a dc-voltage-range accuracy specification of  $\pm 0.01\%$  of reading guaranteed for one year. It can measure the true rms value of ac voltages as high as 700 volts using dc as well as ac coupling. Resistance up to 20 megohms can be measured using either two-terminal or four-terminal techniques.

For the basic bench meter, adding intelligence makes the DMM easier to use in traditional ways. Many meters have used microprocessors to automatically switch to the optimum range—autoranging—and the 8860A does this also, but with a pleasant twist. By having the processor disable the display until the correct range is determined (typically in little more than a second), the user is spared the annoyance of having the meter display values that vary in apparently random fashion—a phenomenon generally referred to as range flashing.

The processor is also used to set up the meter to make different types of measurements. A particularly good example of this involves initial zeroing of the meter. Before processors, zeroing the meter meant shorting the inputs and then using a tuning tool inserted through the front panel to adjust the meter until the display read zero. Now that operation is performed by simply pressing a button after the terminals are shorted. The processor does the rest.

### **Preprocessed data**

In addition to controlling range and configuring the meter for voltage or resistance readings, the microprocessor simplifies the measurement process by allowing readings to be modified before they are displayed. Offset values can be stored in internal registers—either by entering a number at the front panel or by storing an actual reading—and subtracted from the measurement before display. High and low limits for tolerance testing

can also be set in the same way, and when readings are made, a separate annunciation in the display will present an H, L, or P—high, low, or pass conditions—as well as the measured value. This feature adds a dimension to go/no-go testing in that over- or under-value trends can be spotted easily, without the operator having to check whether a reading falls within a specified tolerance.

The processor also permits storage of high and low values in the peak-peak mode. Here the processor continually compares the latest reading to the previous high and low values of the measurement, storing the new reading in place of the old whenever the old is exceeded. This frees the user from having to wade through reams of chart paper on long-term tests, such as overnight power-supply regulation checks in a temperature chamber. It also allows him to capture changes at the maximum sampling rate of the meter.

A selectable sampling rate also is due to the processor. For continuous sampling, the user can choose sample rates of 2½ or 12½ samples per second. In the former case he gets the meter's full 5½-digit resolution; in the latter, the processor automatically limits the reading to 4½ digits, in keeping with the accuracy of the faster conversion rate.

Such functions as autoranging, offsetting, limit setting, and sampling rate selection are becoming more common in meters. But with the addition of these functions, the need for front-panel controls is multiplying and the data content of the display is increasing. These changes would bury the face of the instrument in a mass of light-emitting diodes and switches, were it not for the cause of the changes itself—the processor.

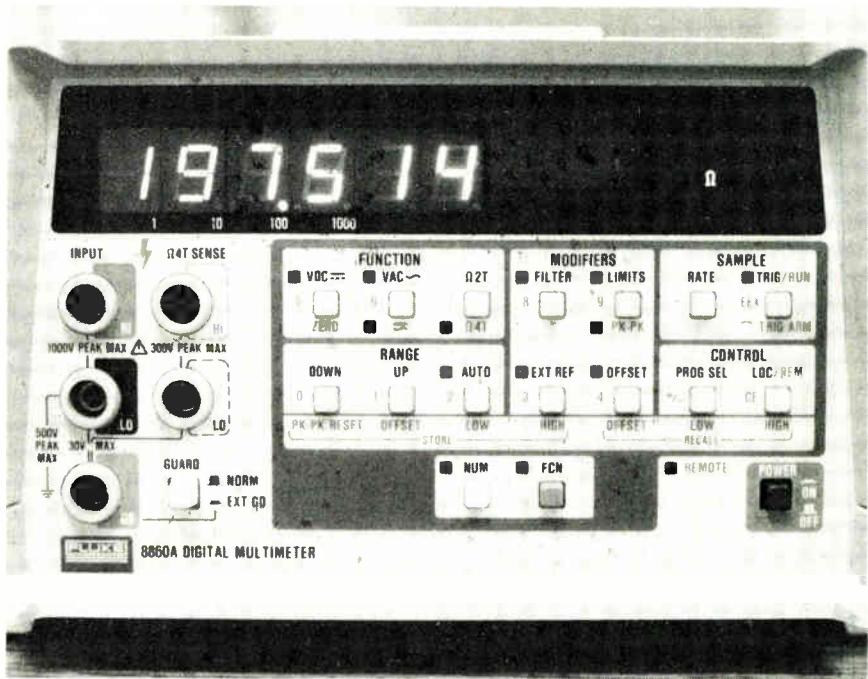
### **A front panel with differences**

The front panel of the 8860A is somewhat different from previous 5½-digit bench DMMSs made by Fluke. Function, range, and operating mode—all 44 possibilities—are called into operation separately or in combination by only 17 push buttons. This is possible because the push buttons configure analog circuitry indirectly through the processor, allowing it to interpret combinations of push button entries, rather than directly, by controlling reed switches.

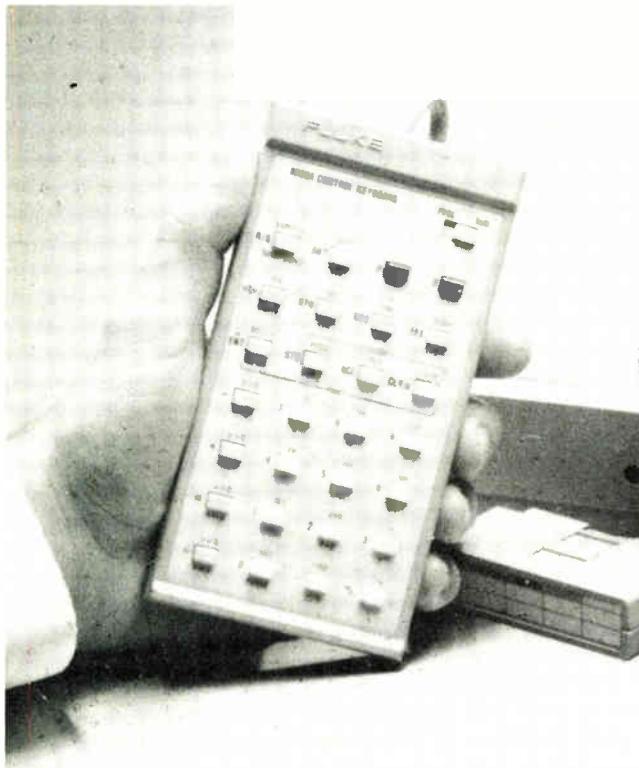
Which metering function or parameter a button selects is determined by two color-coded push buttons—analogous to shift keys on many scientific calculators—at the bottom of the front panel (Fig. 1). The orange shift-function button calls into play the orange-lettered functions below the keys on the front panel. These include store and recall of limits and offset constants, peak-to-peak mode reset, four-terminal resistance measurement, meter zero, dc coupling, and trigger arm. Once one of those functions is selected, the shift mode is deselected and the push buttons revert to the functions described above them in black.

The other shift button is white, and it prepares the meter for entry of a numerical value prescribing, say, limits or offsets. The numeric value of each button is printed on a white background to its left.

So that the status of each function with which the operator might be concerned is clearly visible, annunciation LEDs are positioned next to critical-function meter-



**1. Smart set.** Even though there are only 17 of them, the front-panel push buttons can call 44 different functions. The two buttons at the bottom center set the secondary functions of the buttons printed below and beside each one; color coding shows which second function the button selects.



**2. Smarter set.** An optional keypad lets engineers write measurement programs in RPN that can be stored in detachable modules for later use in the field or on a production line. Operators appear as matrix coordinates on the display or in program printouts.

monics. They light when the function is operative. Range annunciation is accomplished by means of separate annunciators incorporated in the display.

By allowing user reconfiguration of operating software, the next generation of meters will be able to

perform soft math functions and thus become more versatile. The 8860A, with the optional addition of a calculating controller—an internal logic card and an external, calculatorlike keyboard and program storage module—enters this next generation.

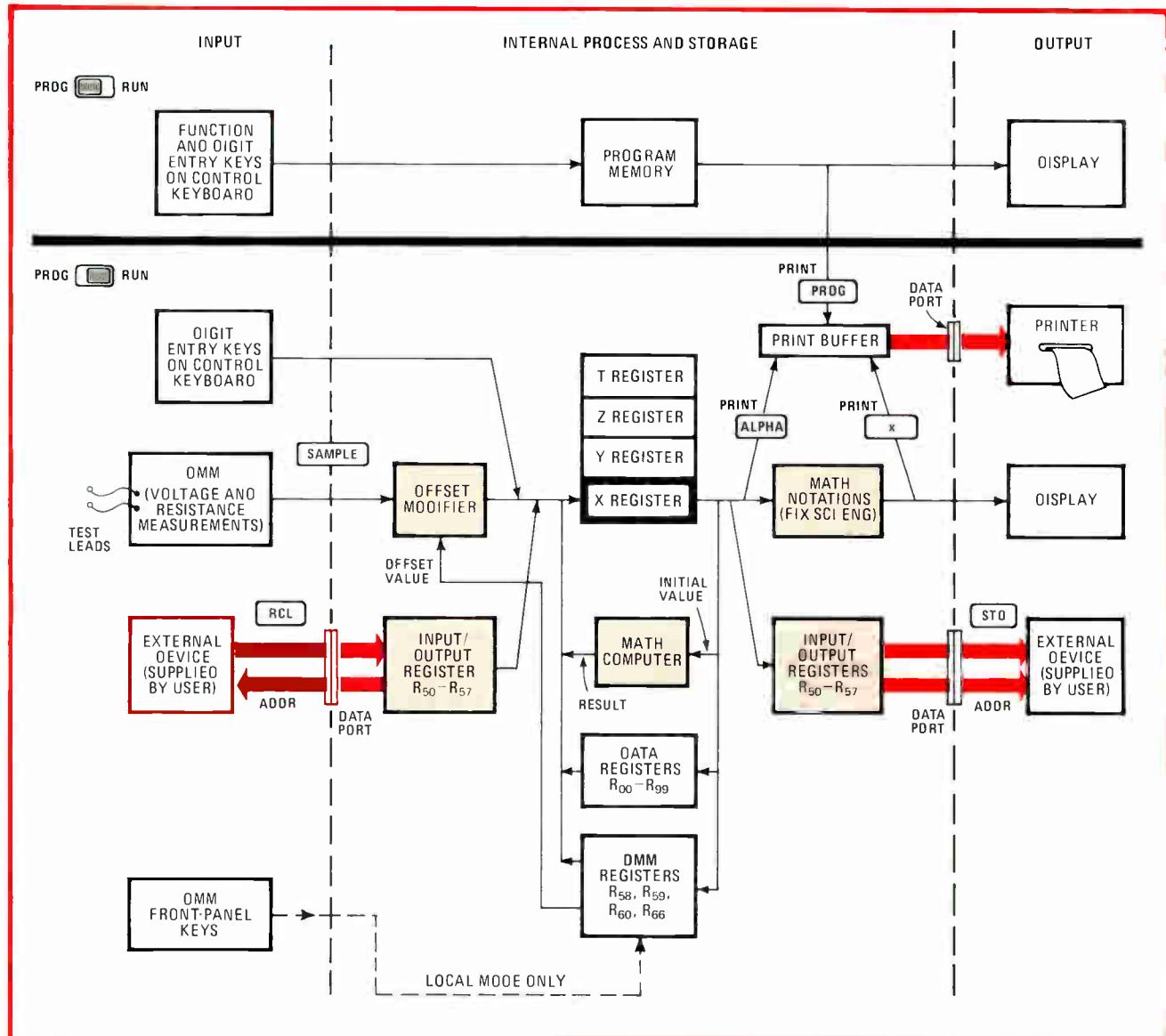
Through the calculatorlike keyboard (Fig. 2), the user gains access to the controlling microprocessor within the 8860A (see "Tandem processing," p. 106). The internal logic card provides number-crunching power and additional instructions on how to interpret the keyboard inputs. The processor can either store these inputs in the nonvolatile program memory module for later use or else act on them directly. With the option installed, the meter takes on the architecture shown in Fig. 3.

Instructions are keyed in with reverse Polish notation (RPN), and the instruction set includes trigonometric, logarithmic, and arithmetical functions. It also provides programming functions such as conditional branching, direct and indirect addressing, editing, and display and format control.

The calculating controller option also provides an input/output port through which the 8860A can communicate with an instrumentation printer such as the Fluke 2020A so that program instructions and measurement results can be listed. For the printout, the controller provides a 64-character ASCII alphanumeric set; it can also receive digital inputs through the I/O port.

With this calculating controller capability, the 8860 becomes more than a precision, benchtop multimeter—it becomes a measurement system. Its flexibility can best be demonstrated by examining a few of the many measurements a smart meter simplifies.

A simple example of the user-definable application of the 8860A is its use to measure the output power of an audio amplifier. As shown in Fig. 4, the 8860A can be programmed to take a voltage reading across a standard load, in this case an 8-ohm resistor, and calculate the power output of the amplifier using the equation  $P =$



**3. X marks the spot.** The X register is the center of activity with the calculating controller option installed and program running. Note that input/output registers R<sub>50</sub>-R<sub>57</sub> may be accessed by a user-supplied external device through the data port also used by the printer.

V<sup>2</sup>/R. In effect, then, the 8860 can be made into a power meter with a 10-step program.

The program illustrates a key aspect of the 8860A: the ability to configure the meter from software. Step 2 of the program shown in Fig. 4 recalls the ac-volts/auto-range configuration of the meter previously stored in a special 10-register segment of the memory module. Storing the five-digit code eliminates the need to write the numbers that configure the meter in each program and thereby reduces the number of steps per program. In step 3, the recalled code is simply addressed to the front panel, which is treated just like any other register, and the meter is configured for the measurement.

There are a number of possible embellishments that could be made to this program. Power could be measured in dBW, for example, by adding some steps. The meter could be configured for peak-to-peak storage and, with extra steps, response flatness calculated.

To increase measurement accuracy the meter could be

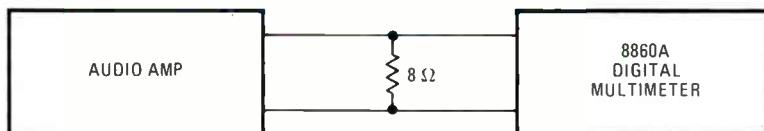
configured to measure and store the value of the resistor before it was set up for the voltage measurement. After reading the resistance, an external trigger could signal the meter that the resistor was back in the circuit and to proceed with the measurement.

With easily inserted program modules, the 8860A can replace a host of dedicated bench meters. A slightly more complex program is that for measuring reactive components, such as capacitors or inductors. Figure 5 shows a test configuration for measuring capacitance.

### Measuring capacitance

To measure capacitance, the 8860A is used with a signal generator that can be set to any frequency. The fact that the capacitance is measured at any frequency means that the measurement can be taken under typical conditions, so the value measured would be that of the capacitance in the final circuit.

The program shown in Fig. 5 is based on the equation:



PROGRAM		
Line No.	Key entry	Comments
01	d LBL 01	Labels the program for access
02	RCL 01	Recalls DMM configuration code previously stored in nonvolatile register 01
03	STO 66	Configure DMM ( $V_{ac}$ , autoranging)
04	d LBL 02	Label for return jump
05	u SAMPLE	Take a reading in volts
06	d $X^2$	Square the reading
07	8	Value of resistor in ohms
08	÷	Divide $X^2$ by 8
09	d DISPX	Display result
10	GTO 02	Jump back to step 04 and repeat

**4. Power.** A simple 10-step program turns the 8860A into an accurate power meter, here set up to measure output across a standard 8-Ω load. By changing step 7 to RCL 60, the load's value can be entered at the front panel as an offset value before each measurement.

$$C = 1 \div \{2 \pi f[(V_A R / V_B)^2 - R^2]^{1/2}\}$$

The constants of the equation— $V_A$ , the voltage output of the signal generator;  $f$ , its frequency; and  $R$ , the resistance across which the measurement is taken—are metered by the operator at the time the measurement is made. These can be stored by pressing buttons on the front panel as well as on the calculator.

Once these constants have been entered, the program executes as much of the formula calculation as it can and stores the three results to speed calculation later in the program. It then configures the meter to make the measurement, makes it, calculates the capacitance using the precalculated results, and displays the final result—capacitance.

### Display details

Note that in Fig. 5 the numerics that come up on the display as the program is written are shown next to the key entries. Entries are displayed with numbers that correspond to their row and column location on the keyboard: 14, for example, refers to the first row's fourth key, the down-shift key. Numerical entries appear as numbers and the code 66 refers to the front panel, which is treated as a register for configurations. The program line number also appears on the display to the right of the key codes and is automatically changed with insertions or deletions.

Keying in an individual program can take some time but needs to be done only once, as the program can be stored in a detachable program memory module. Not only is this convenient, but engineers can thereby write programs for use on the production line, where they can

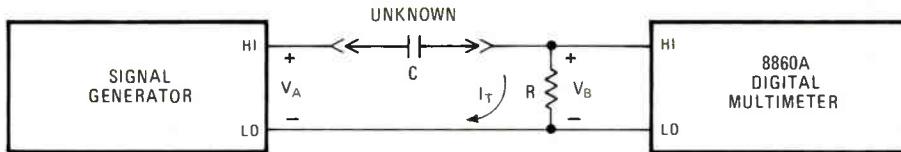
be run without the use of the calculatorlike keyboard. In the capacitance program, for example, the operator would store  $V_A$  in the high limit register,  $R$  in the low limit register, and  $f$  in the offset register. He would then switch to remote and push the trigger-run button, and the test would be performed automatically.

Operator instructions could be given verbally or attached to the program module. But a more elegant way of instructing the operator in what to do is stored in the program for measuring power-supply load regulation. In this program, shown with the test setup in Fig. 6, the meter instructs the operator by sending commands to an external instrumentation printer. The printer tells the operator first to connect the power supply and, after the meter has checked the no-load value, to connect the load. The program halts at each of these steps until the operator presses the run button to indicate he has completed the instruction.

After completing both measurements, the meter performs a calculation and commands the printer to print out GOOD or BAD and the percentage regulation. The criterion that determines whether the power supply passes or fails can be changed from the front panel by the operator, who simply stores a new reference as an offset.

### Program specifics

The program starts by calling up the DMM configuration stored in register 9, which among other things will set the meter for peak-peak operation, and by storing it in register 66. The program is structured as an operating program (lines 01–39) and four subroutines labeled 13, 12, 10, and 11 (lines 40–68). Subroutine 10 is a loop routine that the program uses to output CONNECT LOAD



#### PROGRAM

Line No.	Key entry	Displayed code
00	d LBL 00	14 22 00
01	u ENG 5	13 23 05
02	RCL 58	33 58
03	RCL 59	33 59
04	X	61
05	STO 00	32 00
06	RCL 59	33 59
07	d $X^2$	14 44
08	STO 01	32 01
09	RCL 60	33 60
10	2	02
11	X	61
12	u $\pi$	13 64
13	X	61
14	STO 02	32 02
15	RCL 03	33 03

#### PROGRAM

Line No.	Key entry	Displayed code
16	STO 66	32 00
17	d LBL 19	14 22 19
18	u SAMPLE	13 11
19	RCL 00	33 00
20	$X = Y$	21
21	$\div$	71
22	d $X^2$	14 44
23	RCL 01	33 01
24	-	41
25	u $\sqrt{X}$	13 44
26	RCL 02	33 02
27	X	61
28	u $1/X$	13 74
29	d DISPX	14 21
30	GTO 19	22 19

and CONNECT P/S to the printer. It does so by calling numeric codes for the ASCII characters previously stored by the programmer in registers 2, 3, 4, and 5.

Subroutines 12 and 13 are also print subroutines. In step 36, the measurement result is compared to a reference value stored in the offset register, register 60. (The operator can store this reference value from the front panel.) If the reference value is greater than or equal to the measured value, the program proceeds to the next step and goes to subroutine 12, which prints GOOD, whose code is stored in register 8. It then proceeds to subroutine 13, which prints % REG and the measured regulation. If the reference value is less than that measurement, the program skips subroutine 12, prints BAD, and continues with subroutine 13.

Since measurements have to be made twice—for the no-load and the load condition—the actual measurement is performed by subroutine 11 to save program lines. In this subroutine the input is sampled a number of times so that, in measuring full load conditions, the lowest voltage output would be measured.

It is possible that output voltage fluctuations could occur due to internal heating of the power supply caused by the load. So it was decided that multiple samples of the output should be taken over time. Before entering the sample routine, the operating program stores the number of samples to be taken in register 00. The DSZ function in the subroutine uses this number to count off the number of samples taken. A pause operator in the sample subroutine halts operation for about 1 second, which becomes the approximate time between samples. Therefore, determining the number of samples sets the sample

#### REGISTERS

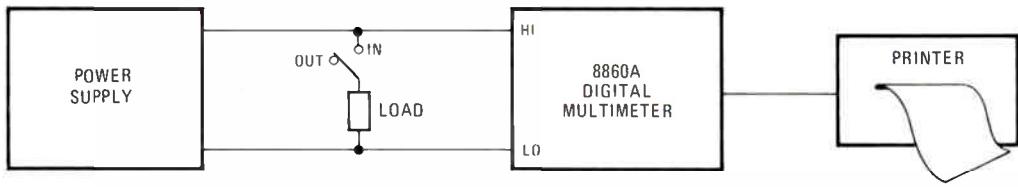
No.	Content	Comments
00	$V_A$ R	{ Filled in by program
01	$R^2$	
02	$2\pi f$	Meter configuration entered by programmer
03	20002	
58	$V_A$	
59	R	
60	f	{ Filled from front panel or keyboard

5. Capacity. Before measuring unknown capacitance,  $V_A$ , R, and the output frequency, f, must be stored in registers 58, 59, and 60, respectively. The 8860A manipulates these constants before going into the measurement loop that starts at step 17.

interval. Since the meter is configured to run in the peak-to-peak mode, it automatically captures the highest and lowest values sampled and stores them in registers 58 and 59. As part of the sample subroutine, these registers are checked and the appropriate parameter used in the program.

With this program stored in a module and the register values entered, all an operator on a production line need do is follow the printed instructions given to him or her by the meter-printer combination. After each printed instruction, the program halts to allow the operator to make the necessary changes in the setup. When the operator is through with making the changes, he simply pushes the trigger-run button on the meter's front panel, and the meter continues with the measurement.

These three measurement programs for power, capaci-



PROGRAM	
Line No.	Key entry
01	RCL 09
02	STO 66
03	u FIX 0
04	3
05	STO 00
06	RCL 04
07	STO 01
08	GSB 10
09	1
10	R/S
11	CLR X
12	STO 58
13	STO 59
14	5
15	STO 00
16	GSB 11
17	STO 10
18	RCL 05
19	STO 01
20	3
21	STO 00
22	GSB 10
23	2

PROGRAM	
Line No.	Key entry
24	R/S
25	u FIX 4
26	CLR X
27	STO 58
28	STO 59
29	5
30	STO 00
31	GSB 11
32	RCL 10
33	4%
34	STO 10
35	RCL 60
36	d X ≥ Y
37	GTO 12
38	RCL 07
39	d PRINT ALPHA
40	d LBL 13
41	RCL 06
42	d PRINT ALPHA
43	RCL 10
44	d PRINT X
45	d PRINT LF
46	R/S

PROGRAM	
Line No.	Key entry
47	GTO 00
48	d LBL 12
49	RCL 08
50	d PRINT ALPHA
51	GTO 13
52	d LBL 10
53	RCL (i)
54	d PRINT ALPHA
55	DSZ 00
56	GTO 10
57	d PRINT LF
58	d PRINT LF
59	d RTN
60	d LBL 11
61	u SAMPLE
62	d PAUSE
63	DSZ 00
64	GTO 11
65	RCL 58
66	u X = 0
67	RCL 59
68	d RTN

REGISTERS		
No.	Content	Comments
01	(varies)	Filled by program
02	454364	ASCII "ect (space)"
03	43575656	ASCII "Conn"
04	601763	ASCII "P/S (space)"
05	54574144	ASCII "load"
06	85624547	ASCII "% reg"
07	424144	ASCII "bad (space)"
08	47575744	ASCII "good"
09	10042	Meter configuration
10	no load value	Filled by program
60	reference	Filled from front panel or keyboard

**6. Regulation.** With this setup, the 8860A instructs the operator to connect the power supply and load in sequence and then prints out measurement results. Both printing and measurement are done by subroutines (labels 10 and 11 respectively) to save program steps.

tance, and regulation indicate some of the possibilities of an intelligent meter. They eliminate the need for different types of meters to measure electrical parameters and could similarly do away with the need for other instruments dedicated to measuring electrically translated physical parameters. So in addition to making it simpler

to take the measurement, the 8860A decreases overall instrumentation costs.

The 8860A can also be configured for use as a precision meter in IEEE-488 systems with an optional interface card that replaces the calculating controller card. The tradeoff of one set of functions for another was based on the fact that, in an IEEE-488 system, a calculating capability in a DMM would be superfluous since the bus controller would be able to perform the calculations more quickly.

Since the customer has already paid for intelligence in the controller, he does not need the extra cost of having it in the meter. By eliminating it, the 8860A becomes the lowest-cost fully programmable 5½-digit voltmeter (with both talk and listen functions) available today.

In the IEEE-488 configuration, the 8860 can take measurements at rates up to 45 readings per second with 3½-digit accuracy. All front-panel controls are programmable, including trigger-mode selection, and the meter can be used in the learn mode, with an operator going through a test and controller remembering how he configures the meter. □

# Speech-synthesis chip borrows human intonation

Specialized processor fetches pulse-code-modulated speech from ROM; compression keeps data rate competitive with linear-predictive coding

by David W. Weinrich, *National Semiconductor Corp., Santa Clara, Calif.*

□ The electronic synthesis of human speech represents another step in the continuing evolution of the interface between man and machine. Though human hands and eyes have sufficed to manage mechanical input and output in the past, the artificially manufactured voice is becoming increasingly important and will ultimately be indispensable.

Essential to the pervasiveness of voice synthesis is the availability of low-cost integrated circuits able to transform 1s and 0s stored in memory into words and phrases. One such set of chips is described in this article.

The speech-synthesis chip set consists of a speech processor and a read-only memory. With external filtering, the system generates fine quality speech, including the natural inflection and emphasis of the original sound. Any voice can be synthesized—adult or child, both male and female.

The speech processor is based on ordinary sampling and digitizing of an input signal at twice its highest

frequency. This is the technique employed for pulse-code modulation (PCM). However, straight PCM would produce far too many bits in proportion to the amount of talking. Therefore, a comprehensive data-compression scheme is used to condense the speech data significantly. The speech processor recreates the original waveform from the compressed data.

The speech ROM contains compressed speech data as well as frequency and amplitude information. The speech processor generates an interrupt at the end of each utterance so that several sequences or words can be cascaded to form different spoken expressions.

## Digitization and compression

The system uses waveform digitization and compression techniques (see "Techniques of speech synthesis"). This minimizes the hardware cost, but at the expense of memory. However, the compression techniques and algorithms developed by Forest Mozer at the University of

## Techniques of speech synthesis

Three main techniques are presently being used to synthesize human speech. They are formant synthesis, linear-predictive coding (LPC), and waveform digitization with compression. With these techniques, vocal utterances, or phonemes, can be linked by linguistic rules to generate words. With vocabularies of over 200 words, these rules and the electronic overhead from their implementation become cost-effective. For smaller vocabularies, however, full-word generation is generally most economical. As memory costs are reduced, the size of the vocabulary for this tradeoff will increase.

Formant synthesis is a technique for modeling the natural resonances of the vocal tract. For recognizable speech, at least three formants should be used for each voice utterance.

With formant synthesis, voiced sounds are generated from an impulse source that is modulated in amplitude to control intensity. The resulting signal is passed through two levels of filtering. The first is a time-varying filter composed of cascaded resonators that correspond to the source-spectrum and mouth-radiation characteristics of the speech waveform.

Unvoiced sounds are generated as white noise is passed through a variable-pole-zero filter. The second

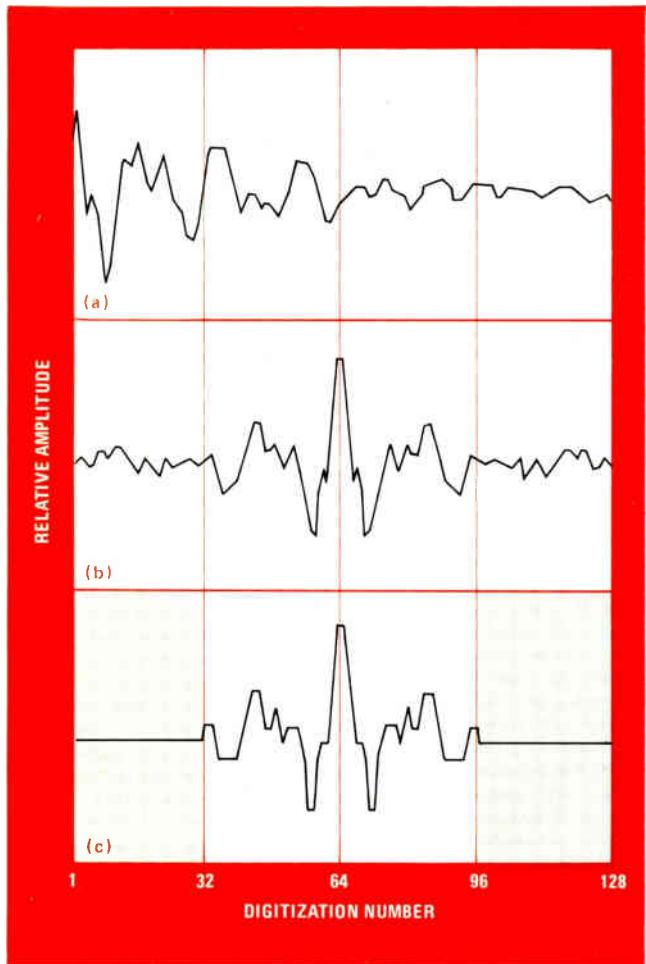
filter used for voiced sounds can be reused for the unvoiced sounds. The coefficients for these filters are stored in ROM. An approximate number of memory bits required for a second of speech is 400.<sup>1</sup>

Linear-predictive coding is very similar to formant synthesis. Both are based in the frequency domain and both can use similar hardware. A basic difference is that LPC uses previous conditions to determine present filter coefficients. The quality of the synthesis improves as the number of coefficients is increased. With ten coefficients, an approximate number of bits per second required for speech is 1,200.<sup>2</sup>

Waveform digitization is the earliest approach taken for speech synthesis, and this is the technique used by the devices described in this article. It relies on nothing more than sampling of the waveform in the time domain at twice the highest frequency of interest (this is known as the Nyquist rate). However, critical to the use of this technique is data compression; otherwise, memory requirements are prohibitive.

## References

1. L. R. Rabiner, *et al.*, "Computer Synthesis of Speech by Concatenation of Formant-Coded Words," Bell System Technical Journal, 1971.
2. Richard Wiggins, "Low Cost Speech Synthesis," Speech Recognition Synthesis Session, 1978 Midcon Professional Program.



**1. Squeeze.** Fourier analysis transforms the original speech waveforms (a) into a signal that is symmetric about its center (b) and twice as compact as the original. Another factor of two in compression is achieved by reducing quiet periods to silence (c).

California significantly reduce memory requirements so they are competitive with those of linear-predictive coding, or LPC. Also, the semiconductor industry continues to lower memory costs.

With waveform digitization and compression, the speech is not only intelligible, but also recognizable as individual male and female voices. Typically, male voices require about 1,000 bits per word of speech. Because of the higher frequency of a female voice, a greater number of bits per second are required for synthesis. By trading off some quality for certain groups of words, this requirement can be reduced by 20%.

The intent of a compression algorithm is the subjective discarding of redundant speech information. The speech processor employs three compression techniques. One removes redundant pitch periods, portions of pitch periods, redundant phonemes, and portions of phonemes. This is accomplished by using repetition periods: one period, produced  $n$  number of times, replaces  $n$  number of very similar periods. An average value for  $n$  may be 3 or 4 for voiced waveforms and 7 or 8 for unvoiced waveforms.

A distinction should be made between voiced and unvoiced utterances. Unvoiced utterances are indepen-

dent of the speaker; once a set of these has been created, they can be used repeatedly. It is critical to speech quality that a sufficiently large set of unvoiced utterances be developed. Voiced utterances are closely aligned to the speaker and must be created for each speaker and phoneme-meld combination.

Another compression method used by the processor is known as adaptive delta modulation. Because the speech waveform is relatively smooth and continuous, with the difference in amplitude between two successive digitizations generally small, less information needs to be stored if the difference in amplitude between successive digitization is used instead of the actual values. That is, the next amplitude in the new waveform is obtained by adding a delta value to the previous value.

The third major compression technique is to remove the direction component of a speech waveform through phase angle ( $\phi$ ) adjustment. This is done by taking each pitch segment of the speech waveform (see Fig. 1a) and finding its Fourier series. Each pitch segment is then represented by the equation:

$$F(t) = \sum_{n=1}^N b_n \cos(\omega t + \phi_n)$$

The intelligibility of the speech is not determined by the phase angle ( $\phi_n$ ) of the Fourier components, so these values can be adjusted to produce a waveform that has mirror symmetry and low amplitude for at least half of the period. An example is shown in Fig. 1b, where a factor of two in compression is achieved. Even though the waveforms in Figs. 1a and 1b look completely different, they both produce the same sound.

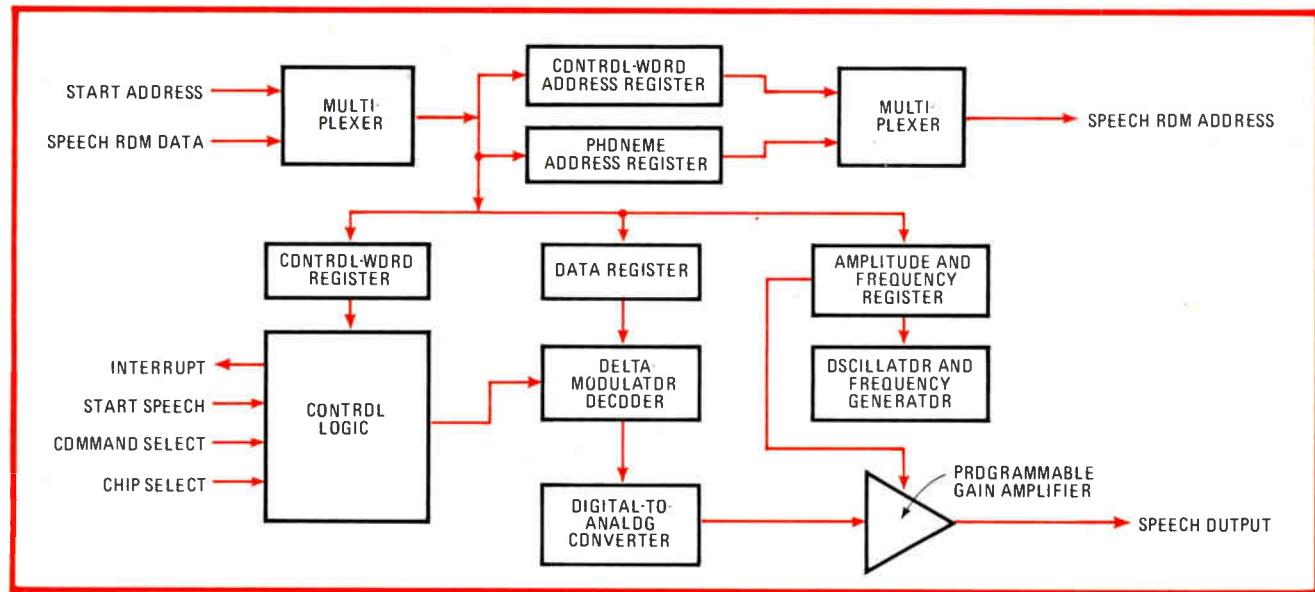
A final scheme for decreasing the information content in a speech waveform without degrading its intelligibility is called half-period zeroing. The low-amplitude portion of the signal is reduced to silence. An example of this is shown in the transition from Fig. 1b to 1c. In (b), most of the amplitude or energy of the waveform is contained in the center half of the pitch period. It is consequently possible to delete the remainder of the waveform without causing a noticeable effect on the quality of the speech that has been produced. Another factor of two in compression appears in (c).

In summary, the waveform in Fig. 1c shows the cumulative effects of phase-angle adjustment, half-period zeroing, and adaptive delta modulation. Three-quarter-period zeroing and the use of silence and of the stored duplication of pitch waveforms provide even further reduction.

#### Analysis and generation

To generate speech data using these compression techniques, it is first necessary to speak into a microphone and produce the analog signals representing the basic speech information. These are then passed through a differentiator to retain the higher-frequency components. This differentiated waveform is then sampled and digitized.

The next step is to interpolate the digitization until all pitch periods contain a fixed number of them—in this case, 128. This process may dictate adding or removing points as necessary. A computer program is then applied to the data to perform phase-angle adjustment, delta



**2. Processor blocks.** The starting address of the speech is loaded from the ROM into the processor's control word address register. The control word register is next filled with the address of the first block of actual speech data that is subsequently processed.

modulation, and half-period zeroing. The last step is used to select the periods that will be able to serve for multiple playbacks.

The data generated by the analysis methods are stored in the speech ROM along with control information. Up to 128 kilobits of ROM can be directly addressed without any additional hardware. Memory requirements of greater than 128 K are served with few external components, and both static and dynamic (clocked) ROMs can be used in any case.

#### Chip configuration

Figure 2 is a block diagram of the speech processor chip. Each block of speech data has a control word that gives a complete description of how to process the data. It contains the frequency and amplitude information vital in recreating the natural inflection of human speech. It also specifies the ROM location, the type of waveform to be generated, the number of times to repeat it, and a bit to indicate whether or not this is the last control word. This bit enables the control logic to cascade blocks of speech data in such a way as to form words and sentences.

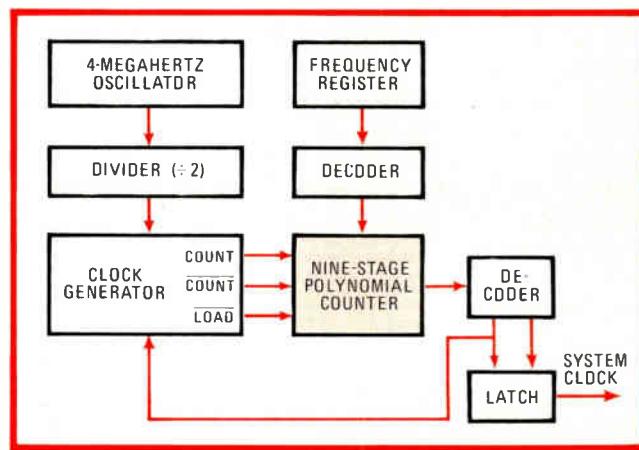
Speech ROM sequences begin with an 8-bit starting address that allows up to 256 expressions to be synthesized for each 128 K of ROM. Additional expressions are achieved with minimal external components. The starting address is first loaded into the control-word address register of the speech processor with a start pulse. The processor then fetches from the ROM the control word pertaining to the first block of speech data. The control word contains the address of the delta-modulated speech data that is loaded into a 14-bit up/down counter called the phoneme address register. The processor is now ready to fetch the actual speech data.

Before the data is processed, the type of speech waveform must be decoded to determine its format—male or female, voiced or unvoiced, half-period-zeroed or not—as well as such characteristics as silence content.

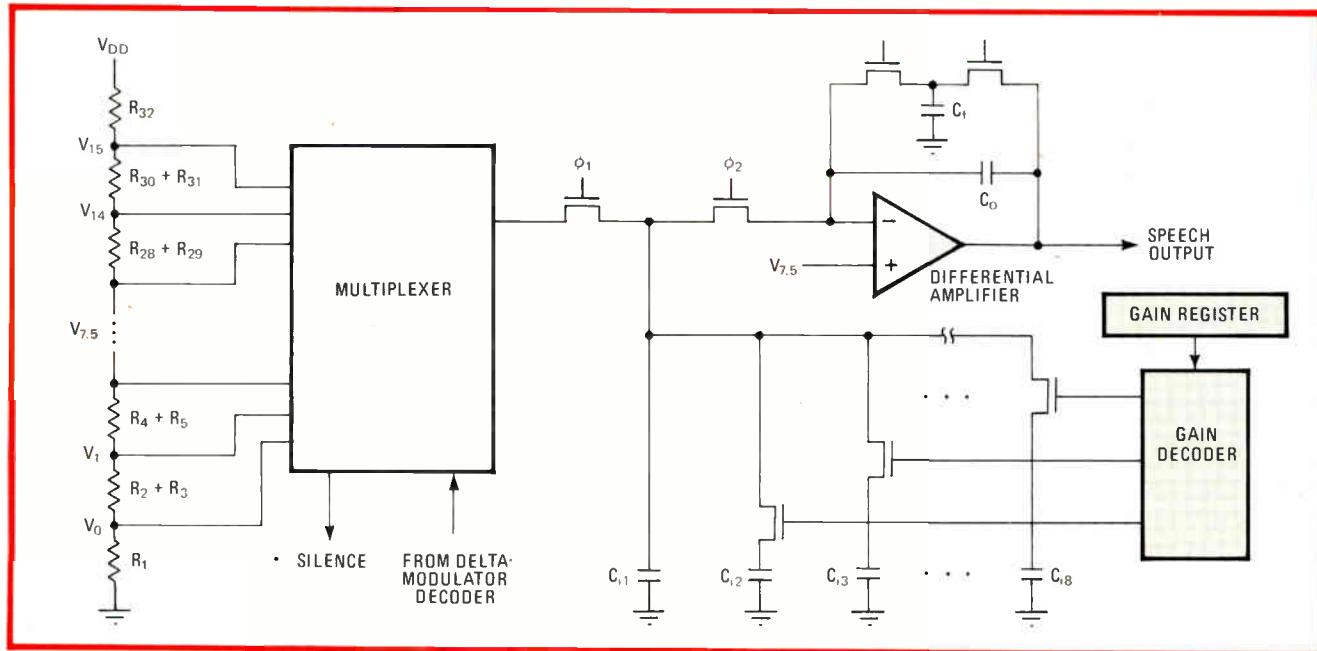
If the decoded waveform is male with half-period zeroing, the speech output waveform will assume the shape shown in Fig. 1c. In this figure, the delta-modulated speech-data processing is delayed for the first 32 digitizations. That is, for one quarter of the output waveform the speech processor puts out silence, which requires no ROM space.

#### Fetching the data

After this silence, speech data from the ROM is loaded into the processor's data register and passed on to the delta modulator decoder, which in turn converts the data into a 4-bit binary number for use by the digital-to-analog converter. Data processing continues to the midpoint—or 64 digitizations into the waveform—at which time the processor begins to fetch the speech data in the reverse direction. Fetching the data backwards continues for 32 more digitizations to the three-quarter point of the waveform, and then there is silence until the end of the



**3. Frequency synthesis.** The frequency generator aboard the speech processor includes a nine-stage polynomial counter, register, decoder, and oscillator. Thirty-two frequencies can be generated for male and female voices having different pitch periods.



**4. Back end.** Just before speech emerges from the processor, it passes through a digital-to-analog converter and a programmable gain filter. The converter uses a precision ladder network; the step between the seventh and eighth resistors serves as a threshold value.

waveform. Finally, the processor decides whether or not to repeat the preceding waveform. This information too is contained in the control word. The point is that at most only 32 digitizations are required to produce a waveform 128 digitizations long.

If and when the waveform is repeated a specified number of times, the processor fetches the next control word and generates the waveform it specifies. This is done in real time, with no discontinuities in the output waveform. After all waveforms are generated, the processor idles in silence.

To provide natural inflection, a programmable frequency generator is incorporated into the speech processor. Changing the frequency accents syllables and creates rising or falling pitches in different words. Each waveform can be synthesized at a different frequency if necessary.

A diagram of the programmable frequency generator is shown in Fig. 3. It consists of a nine-stage polynomial counter, register, decoder, and oscillator. The frequency to be generated is loaded from the speech ROM into the processor's frequency register at the beginning of each block of delta-modulated data. The register is decoded to set up a binary number that represents the desired modulus for the polynomial counter. An additional decoder is used to generate the desired duty cycle of the system clock waveform.

Thirty-two different frequencies can be generated with this circuit to synthesize male voices with pitch periods from 80 to 200 Hz and female voices with pitch periods from 160 to 400 Hz.

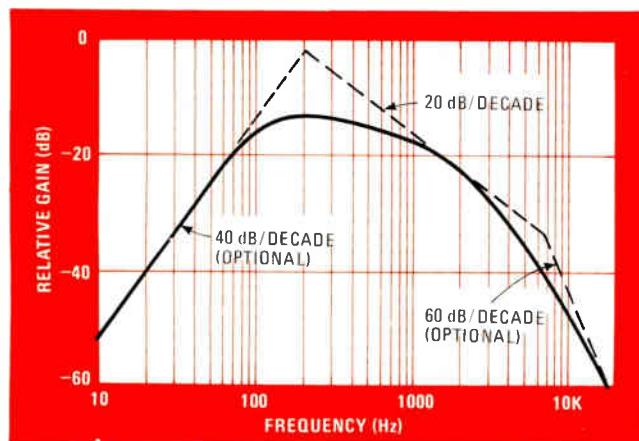
#### Variable gain d-a converter

The d-a converter and programmable gain amplifier are shown in Fig. 4. The converter uses a precision resistor ladder network connected between  $V_{DD}$  and  $V_{SS}$ . Resistors 2 to 31 are small and of equal value.  $R_1$  and  $R_{32}$  are large enough so that most of the voltage is dropped across them. The multiplexer selects the appropriate value from the resistor network based on the information from the delta modulator decoder.

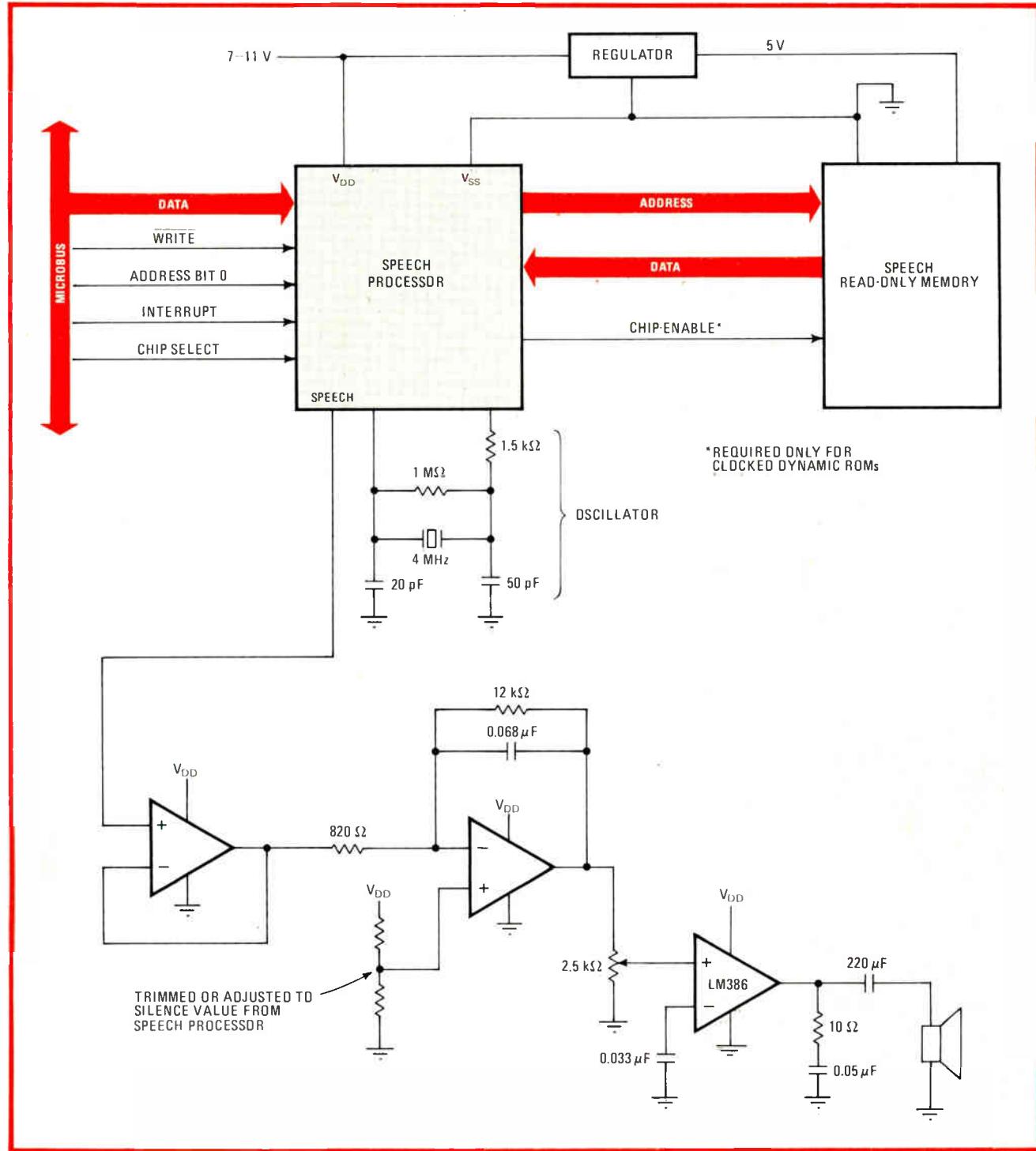
There are 17 discrete voltage values in the converter. Sixteen of these,  $V_0 = V_{15}$ , are equally spaced. The 17th value, between steps  $V_7$  and  $V_8$ , has a normalized weight of 75. Thus for an equal range of values above and below silence,  $V_{7.5}$  is used as a threshold.

The amplifier uses switched capacitors for gain control. This approach lends itself nicely to MOS integrated circuit technology. Capacitor ratios can be controlled very easily and the proper frequencies can be derived from the main oscillator.

Conventional amplifier designs use resistors to control the dc gain, but it will be shown that switched capacitors are equivalent. For instance, if gain is given by:



**5. Response.** Some external filtering of the speech obtained from the processor is necessary for the highest quality sound. The minimum external requirement is a low-pass filter with a cutoff frequency around 200 Hz. Higher-frequency filtering might also be desirable.



**6. Slave.** The speech processor and associated components are controlled by a master microprocessor attached to National's Microbus. The speech chip is activated with a chip-select signal, the start pulse comes over the write line, and the address ( $A_x$ ) carries the mode.

$$A_{VDC} = -(\text{feedback resistance}/\text{input resistance}) \\ = -(R_f/R_i)$$

these resistors can be replaced by capacitors and switches such that:

$$R = 1/(f_s C)$$

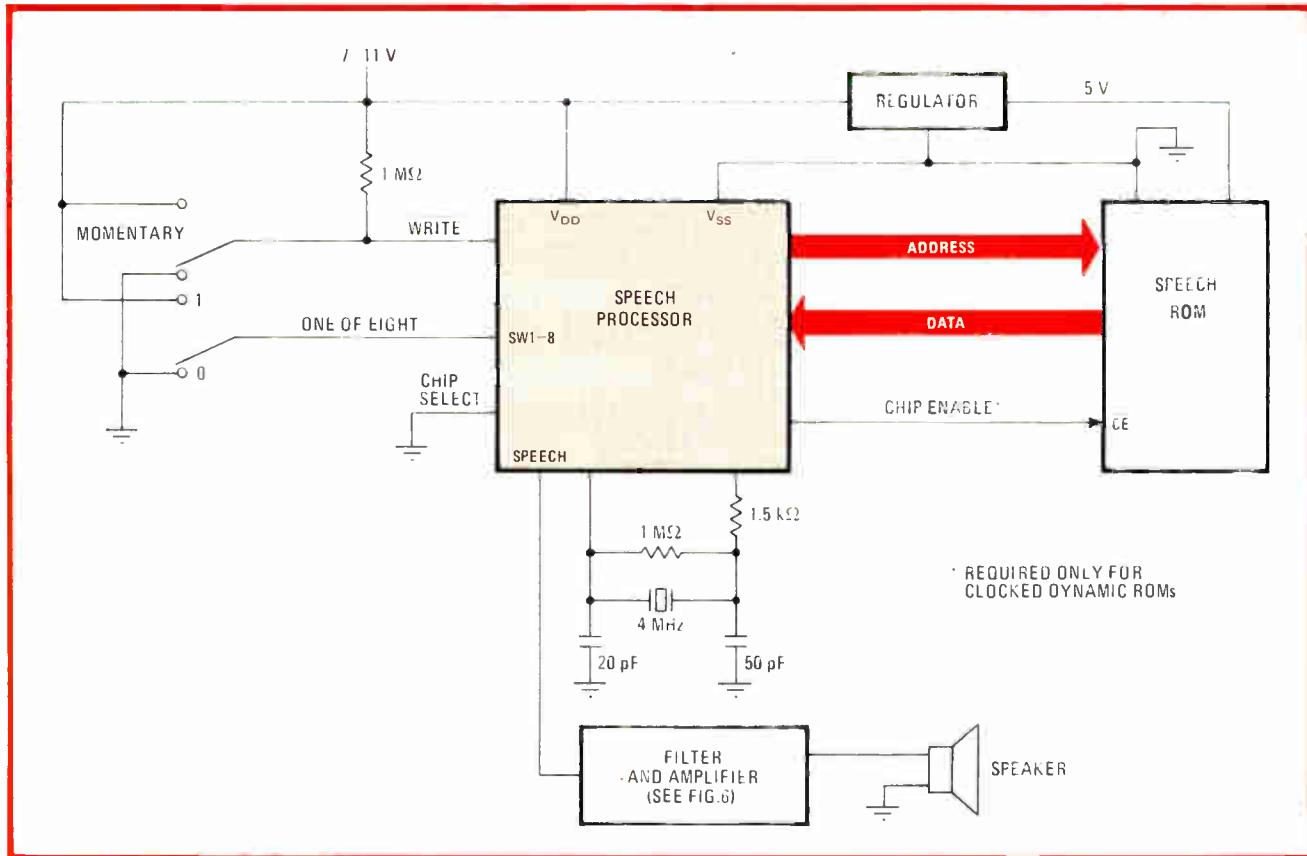
where  $f_s$  is the frequency of operation for the switches and  $C$  is the capacitor value. Substitution gives:

$$A_{VDC} = -[1/(f_s C_f)]/[1/(f_s C_i)] = -(C_i/C_f)$$

To filter the clock and to add stability to the circuit, a capacitor  $C_o$  can be added. The gain with  $C_o$  included is:

$$A_V = -(C_i/C_f)[1/(1 + \omega C_o/f_s C_f)]$$

From this equation, the gain could be controlled by varying either  $C_i$  or  $C_f$ . In this case, however,  $C_f$  is held constant to ensure a uniform filter cutoff frequency; so



**7. Stand-alone.** Switches are manually manipulated here to control the speech processor. The pull-up resistor on the write line is all that is needed for switch debouncing. An application for this circuit might be a toy or game that talks when a button is pushed.

the gain is changed by varying  $C_i$ . Therefore, minimum gain is when  $C_i = C_{ii}$  (see Fig. 4) and maximum gain is when all of the capacitors are switched into the circuit in parallel such that  $C_i = C_{ii} + C_{i2} + C_{i3} + C_{i4} + C_{i5} + C_{i6} + C_{i7} + C_{i8}$ .

The dc gain with switched capacitors can be expressed as:

$$A_{VDCn} = \left( \sum_{x=1}^n C_{ix} \right) / C_f$$

Eight different gain values are used and each gain value is 1/3 the previous gain value. Stray capacitances can easily alter the gain of the amplifier, so these are kept to a minimum.

#### Frequency response

Some external filtering of the speech output is necessary. In the synthesis procedure described earlier, the original speech was differentiated; therefore, the minimum external requirement would be a low-pass filter with a cutoff frequency of approximately 200 Hz (see Fig. 5). This cutoff frequency would be tuned for the particular voice being synthesized. For low-pitched male voices it may be 100 Hz, and for high-pitched female or children's voices it might be 300 Hz.

Some additional filtering may be desirable depending upon the speaker used in the system. Optional filters include a two-pole high-pass filter with a cutoff frequency of 200 Hz and a two-pole low-pass filter with a cutoff frequency of from 6,000 to 8,000 Hz.

The speech processor is easily attached to all popular

microprocessor systems. It also has the added feature of on-chip debouncing for interfacing to manual switches.

Figure 6 shows a configuration whereby a microprocessor controls the speech processor via National Semiconductor's Microbus [Electronics, July 20, 1978, p. 113]. The starting address of the speech sequence is placed on the data bus (D<sub>0</sub>–D<sub>7</sub>) lines. The speech chip is selected via chip select ( $\overline{CS}$ ) when the start-speech pulse is given over the write (WR) line. The speech processor then executes the command specified by the command select input given over A<sub>0</sub>. A use here might be in a talking clock, where the messages depend upon the time of day.

If A<sub>0</sub> is a logic 0, the interrupt line is reset and a speech sequence begins. When the end of the sequence has been reached, the interrupt line goes high (generating an interrupt) to indicate that the speech sequence has been completed. The microprocessor can then start another sequence, if so desired, to cascade words or phrases together for different messages. If A<sub>0</sub> is a logic 1 when the start pulse is received, the interrupt line will be reset; however, a speech sequence will not be generated.

#### Applications

Figure 7 shows the system with a manual switch interface. The addition of a pull-up resistor on the write input (WR) completes the on-chip debouncing of the momentary contact. An application of this circuit might be a toy or game where the speech is required only when a switch is depressed. □

# ECC menu adds processing, materials

Electronic Components Conference also serves up thermistors, Hall-effect switches, tantalum capacitors, and CAD for hybrids

by Roger Allan, *Components Editor*  
and Jerry Lyman, *Packaging & Production Editor*

□ Important developments in discrete components tend to get lost among the dazzling advances in monolithic integrated circuits—but not at the annual Electronic Components Conference.

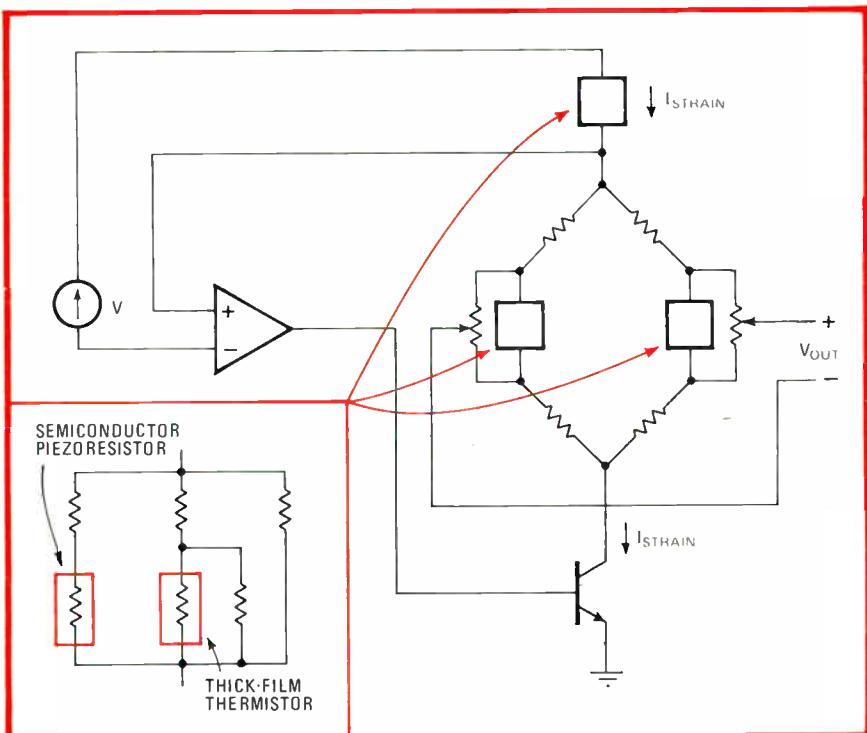
That is not to say the range of topics covered at the San Francisco gathering is a narrow one. In three days (April 28–30), sessions cover materials, processing, wiring, computer-aided design and manufacturing, packaging and reliability, and of course the latest in discrete and hybrid components. The yearly conference, sponsored by the Institute of Electrical and Electronics Engineers and the Electronic Industries Association and held this year at San Francisco's Hyatt Regency Hotel, may have outgrown its traditional name; but then the industry has changed radically since the first ECC.

Many of the component developments announced at the ECC parallel those of integrated circuits, making use of monolithic and thick- and thin-film techniques for their realization. In fact, an entire session is devoted to semiconductor processing, where semiconductor anneal-

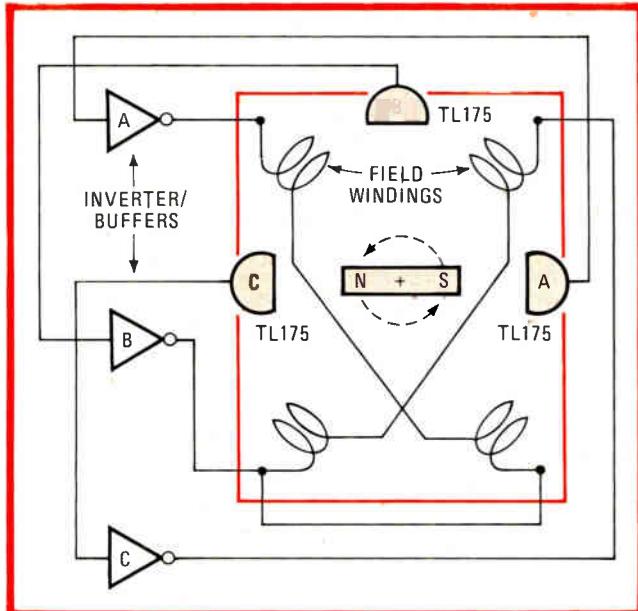
ing, ion implantation, and crystal processing are discussed. An opening session on computer-aided design for hybrid circuits is further evidence of the close tracking of discrete technologies with those of monolithic ICs.

Two of the more interesting developments in discrete devices are covered in Session 3, "Discretes." One of these includes a thick-film thermistor described by Akira Ikegama and colleagues at the Production Engineering Research Laboratory of Hitachi Ltd., Tokyo, Japan. The thermistor offers high accuracy, stability, and reliability levels for a number of applications.

Composed of a semiconducting oxide, precious metal, ruthenium dioxide, and glass, Hitachi's thermistor is said to meet increasing demands for a simple means of temperature compensation in hybrid thick-film circuits for consumer, automotive, and control-system applications. The Hitachi researchers have proven the thermistor's usefulness by applying it as a sensor in semiconductor strain gages (Fig. 1) and hybrid air-flow circuits. Various shapes of thermistor chips were made, including



**1. Strain bridge.** A newly developed low-cost thick-film thermistor can be used in the bridge circuit of a strain-gage pressure transducer. Each shaded area consists of a single-crystal silicon diaphragm on whose surface piezoresistors are formed by a semiconductor diffusion process.



**2. Commutation.** Three TL175 Hall-effect switches can be used in a four-pole brushless dc motor. Commutation occurs when the rotor is in a neutral zone, midway between field poles. The inverter/buffers increase the Hall switches' current-handling capabilities.

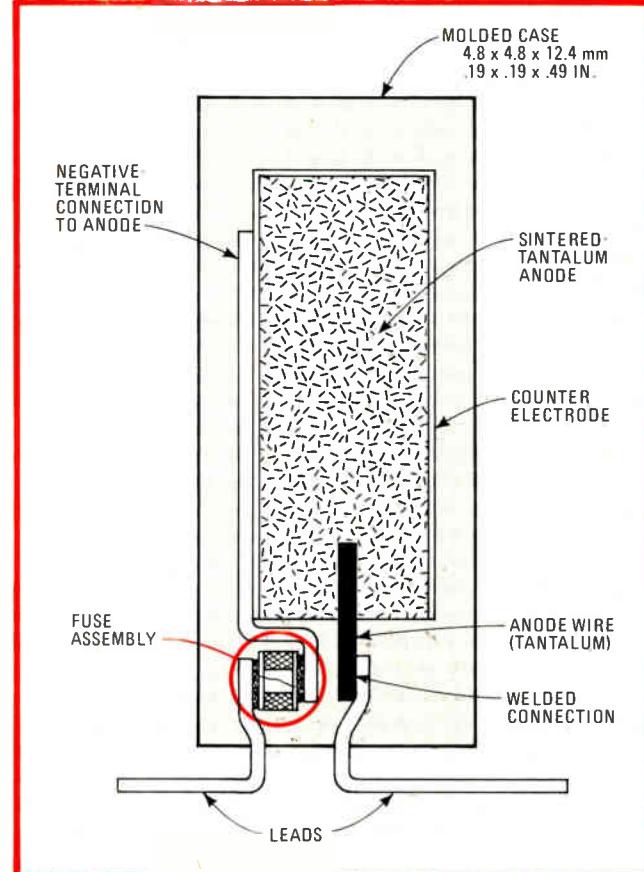
sheet, comb, and sandwich types, the smallest being 1 by 2 millimeters. Resistivity ranges from 1 ohm-centimeter to 10 megohm-cm while the resistor constant spans 100 to 4,500. Accelerated life tests showed less than 0.02% shift per year in the resistance value.

Another Session 3 paper, by John L. Di Filippo, Texas Instruments Inc., Dallas, describes a low-cost monolithic silicon Hall-effect latching switch. The component, the TL175, is a vast improvement over present monolithic Hall-effect switches. The device uses an orthogonal-array Hall element said to be considerably less sensitive to mechanical stress and offer smaller offset voltages and tighter distributions than conventional Hall-effect switches. The result is a component with guaranteed minimum switching thresholds that remain bipolar, with a tight hysteresis loop, over  $-40^{\circ}$  to  $+125^{\circ}\text{C}$ . This allows it to be used in automotive and industrial environments. Figure 2 shows a novel use for the switch in a brushless dc motor.

Initial evaluation of TL175 samples has shown a Hall-array sensitivity of approximately 20 microvolts/gauss with less than 10% variation from device to device. Over the device's wide operating-temperature range, Hall-array sensitivity over power-supply levels of 8.2 to 16.5 v was less than 5%. Additional data includes a trip-point variation of about 0.7 gauss/ $^{\circ}\text{C}$ , 20 milliamperes of output current, and an operating frequency of at least 10 kilohertz.

#### Activity galore in capacitors

Session 12, "Resistors and Capacitors," highlights interesting developments in tantalum capacitors. A paper by L. G. Feinstein and R. J. Pagano, Bell Laboratories, Allentown, Pa., described researchers' success in extending the useful range of precision thin-film tantalum capacitors up to 1 MHz through the use of an



**3. Fuse.** The fuse module in this solid-tantalum capacitor protects the circuit the capacitor is hooked across when the capacitor overheats because of increasing leakage currents. The fuse, a palladium-clad aluminum wire, opens up when its temperature reaches  $650^{\circ}\text{C}$ .

aluminum underlay that reduced the capacitor's series resistance by a factor of 20. Conventional thin-film tantalum capacitors are limited to frequencies below 10 kHz, because of the frequency dependence of tantalum-anode series resistance.

The researchers built a thin-film RC test circuit in which an aluminum underlay 0.25 to 10 micrometers thick was used. The underlay is deposited by evaporation or magnetic sputtering onto a glazed ceramic substrate with a tantalum-oxide layer in between.

According to the researchers, the presence of the aluminum underlay did not affect the electrical properties and life characteristics of the RC test circuit. Test results showed a series resistance of 2.9 ohms at 10 kHz, increasing to 3.2  $\Omega$  at 400 kHz, to 4.5  $\Omega$  at 4 MHz, and to 5.3  $\Omega$  at 10 MHz, without the use of the aluminum underlay. With the underlay in place, these values dropped to 0.17, 0.20, 0.21, and 0.21  $\Omega$ , respectively.

Another Session 12 paper, by H. V. DeMatos, Union Carbide Corp., Greenville, S. C., reports on the design of an internal fuse for a high-frequency solid-tantalum capacitor. The fuse module is intended for high-frequency bypass applications and consists of a fine bimetallic wire that reacts exothermically upon reaching a critical initiation temperature (Fig. 3).

Typically, solid-tantalum capacitors are widely used in filtering and frequency bypass applications, where often

they are connected across a power-supply bus. Despite their low failure rates, solid tantalum capacitors can overheat and fail catastrophically, in turn causing much damage to the ever more complex power-supply circuits they are hooked across. The incorporation of the internal fuse module increases a circuit's protection.

To minimize the equivalent series resistance (ESR) and inductance values of the fuse element, fuse connections are kept as short as possible. The use of short ribbon leads allows for low ESR and inductance values of  $0.1\ \Omega$  and  $0.5$  nanohenry, respectively, for a 40-microfarad  $10\text{-v}$  tantalum capacitor.

The fuse element is a palladium-clad aluminum wire that traverses an isolating cavity within the tantalum capacitor to link two conductor planes. The planes are parts of the capacitor's negative ribbon lead (anode). When increasing leakage currents heat the fuse material to  $650^\circ\text{C}$ , the palladium-aluminum junction opens up.

One penalty is a slight increase in capacitor impedance at high frequencies, although this increase is not severe for frequencies much less than  $10\text{ MHz}$ . At a frequency of  $10\text{ MHz}$ , impedance rises from about  $0.1$  to  $0.2\ \Omega$ , and at  $100\text{ MHz}$ , from about  $0.4$  to about  $1\ \Omega$ . The comparison is for an unfused ribbon-lead tantalum capacitor of the same value.

### Improvements in optoelectronics

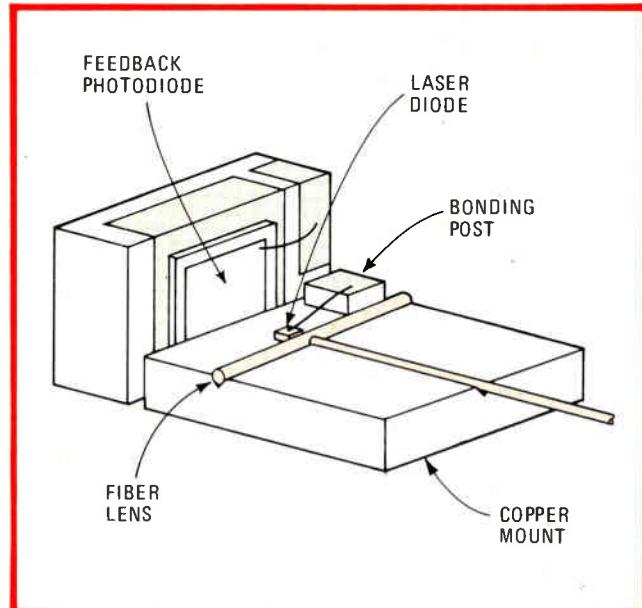
Optoelectronic components are finding their way into more and more circuits. Two sessions, Session 6, "Optoelectronics: Energy Conversion," and Session 8, "Lightwave Devices and Packaging" are on the agenda.

In Session 6, K. Firor and S. Hogan from the Solar Energy Research Institute, Golden, Colo., present an excellent overview of thick-film technology for making solar cells. Thick-film techniques are low-cost alternatives to more expensive thin-film techniques that are now applied to solar cells.

The researchers conclude that thick-film screen printing can be used for the metal contacts and back-surface fields of solar cells. New base-metal inks under investigation promise to reduce the cost of putting metal contacts on silicon solar cells. Depositing (by screen printing) dopants, anti-reflective layers, and protective coatings have all been shown feasible. When combined with the high-production-throughput advantages of thick-film processing, the technology appears a likely candidate for low-cost silicon solar cell processing.

A related paper by N. K. Annamalai, C. C. Chao, and M. Brown, Clarkson College of Technology, Potsdam, N. Y., shows that it is possible to fabricate high-efficiency solar cells by sequential evaporation of cadmium sulfide and copper sulfide. The technique yields high-performance solar cells that nevertheless are economical to manufacture.

The conventional method of making  $\text{CdS-Cu}_2\text{S}$  solar cells is by vacuum deposition of the  $\text{CdS}$  material onto a substrate, followed by a wet-dip-barrier formation of the  $\text{Cu}_2\text{S}$  layer. Although this process yields high-efficiency cells (about 10% efficiency), cell performance is not high and is subject to further degradation over time due to the presence of oxygen at the  $\text{CdS-Cu}_2\text{S}$  interface. The new process discussed involves the formation of a planar



**4. Laser module.** Designed for fiber-optic systems, this dual in-line hybrid laser module includes double-heterostructure gallium-aluminum arsenide diodes with oxide-insulated contact stripes. The fiber tail is coupled to the laser diode through a microlens.

junction instead of the conventional textured junction. The use of an *in situ* resistance-monitoring technique allows the studying of  $\text{CdS}$  and  $\text{Cu}_2\text{S}$  sheet resistivities while they are being deposited (not after deposition, as with conventional wet-dip-barrier methods). This makes possible individual solar-cell characterization.

In another optoelectronic energy topic, a paper by M. M. Robertson, Sandia National Laboratories, Albuquerque, N. M., shows the feasibility of transmitting power on optical-fiber components. The effort involves the conversion of electrical power to optical power, transmitting the optical power through fiber-optic components, and reconverting it to electrical power by means of photovoltaic cells.

The initial step of electrical-to-optical power conversion is performed with xenon arc lamps and injection laser diodes. The xenon lamps are used for power levels of a few hundred milliwatts to a few watts, and the injection laser diodes produce a few milliwatts. Gallium arsenide and silicon diodes are used as photovoltaic cells.

Test results show conversion efficiencies as high as 33.4%, when  $1.34\text{ mw}$  of injection-laser optical power is converted to  $0.45\text{ mw}$  of electrical power by a  $\text{GaAs}$  cell. The use of a xenon lamp putting out  $3.55\text{ w}$  of optical power results in an output of  $0.81\text{ w}$  for a maximum conversion efficiency of 22.8%. Xenon lamps with  $0.43\text{ w}$  of optical power in conjunction with silicon photovoltaic cells result in an electrical output of  $76\text{ mw}$ , for maximum conversion efficiency of 17.7%.

### Linking optical sources with fibers

Session 8 contains several interesting papers reporting improvements in linking optical sources with fibers. In one paper, R. Stephen Speer and Bobby M. Hawkins from the Spectronics division of Honeywell Inc., Richardson, Texas, describe a planar gallium-aluminum

## Pinpointing failure mechanisms

The most impressive performance specifications are meaningless if the part cannot also claim a satisfactory level of reliability. Electronic devices have come a long way in this regard, but the search goes on for elusive failure mechanisms that tarnish the good name of component reliability. An idea of the sophisticated scientific tools and investigative techniques being brought to bear on this problem emerges from ECC Sessions 4 and 11, titled "Reliability I" and "Reliability II."

The first of the two sessions includes papers on the effect of flame retardants on the reliability of molded-plastic packages, corrosion mechanisms of plastic packages, quasi-hermetic sealing of integrated circuits and its effect on reliability, and gross-leak hermeticity testing with helium. The performance of digital MOS and bipolar ICs at

temperatures up to 340°C, life-testing TTL and complementary-MOS ICs at 300°C, and reliability-assurance testing with a scanning laser acoustic microscope are the subjects of other papers.

Papers in the second session address operating-temperature characterization of devices by transient analysis, reliability considerations of thermal resistance, diffusion behavior in platinum-gold thin-film layers, the reliability of 250-watt pulsed L-band microwave transistors, and the characterization of electrical overstress in automobile power systems and the resulting destruction of semiconductor devices. The final paper looks at the performance of a thin-film aluminum oxide humidity sensor. Test results show that drift in the sensor's calibration curve caused by water vapor can be significant.

arsenide double-heterostructure light-emitting diode whose packaging allows it to be plug-mated with a fiber-optic cable without too much concern for alignment accuracy, thanks to generous mechanical alignment tolerances. The packaging concept is said to be compatible with common high-volume manufacturing techniques. It also provides a hermetic seal for the LED. The diode reportedly has internal quantum efficiencies as high as 100%.

R. C. Hooper, D. R. Smith, and B. R. White of the British Post Office Research Centre, Ipswich, England, report on a hybrid laser transmitter module for use in fiber-optic systems. The dual in-line laser module (Fig. 4), intended for communication systems with high transmission rates, has the laser-control and drive circuitry within the same package. A graded-index optical fiber tail is coupled into the laser diode through the package and is terminated with a demountable fiber connector.

A GaAs metalized semiconductor FET (MES FET) is used as the drive element. A feedback control circuit in the module stabilizes the laser's output power against variations resulting from laser degradation and temperature fluctuations.

Multilayer wiring is the topic of Session 9. As inte-

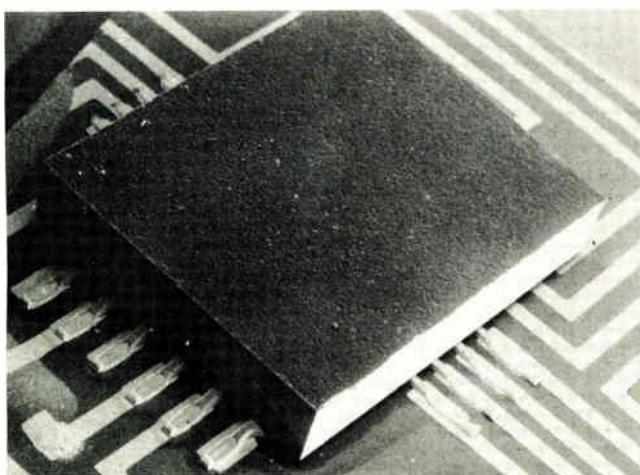
grated circuits head into the VLSI era, 100,000 devices per chip will become common. This tremendous density will be reflected in an increased circuit board or substrate wiring density.

### PC improvements called for

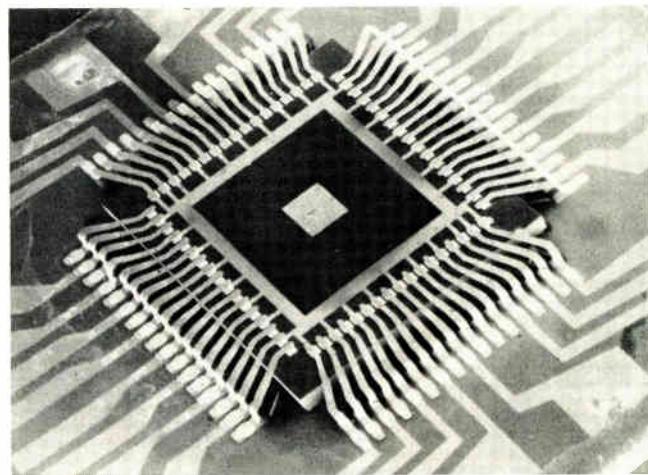
Two of the more important papers of this session are "A Status Report on Multilayer Circuit Boards," by John C. Mather of Rockwell International Corp.'s Interconnect Systems division, and "A Method of Manufacturing High Density Fine Line Printed Circuit Multilayer Substrates which can be Thermally Conductive," by Sanford Lebow, Pactel Corp., Newbury Park, Calif.

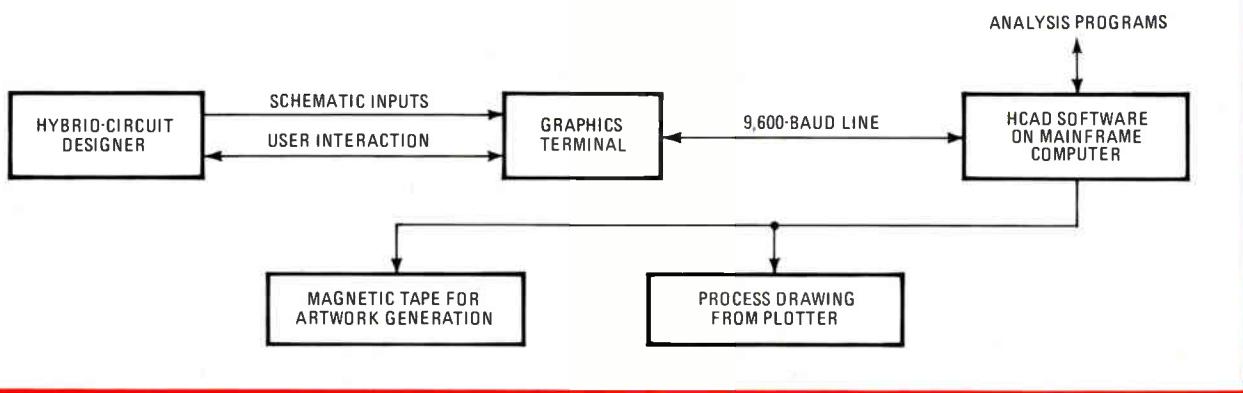
In the first paper, Mather presents an overview of today's capability in multilayer boards. He concludes that for the PC industry as a whole, it would be difficult to produce large volumes of boards with 7-mil lines and spaces, 14 conductive layers and plated through-holes with a length-to-diameter ratio of 4.

What is needed, the paper points out, is breakthroughs in technology that will leapfrog today's methods. Mather suggests the following: replacing plated through-holes with economical interstitial vias; making a heat sink an integral part of the multilayer assembly; imaging 1- to



5. Face-to-face. Tape-automated bonding may be applied to hybrids in two ways. In face-up TAB (right), the chip's back is epoxy-bonded to the ceramic substrate. In face-down TAB (left), leaded chips are bonded to the ceramic face down and covered with a silicone coat.





**6. CAD for hybrids.** The Hybrid Computer Aided Design (HCAD) system is used on most thick- and thin-film hybrids at Tektronix. HCAD combines interactive graphics, component modeling, design analysis, and documentation. The software resides in a Cyber 175 computer.

2-mil features without the cost of photoresists; using unreinforced resins with a high softening temperature for improved high-frequency performance; and hermetically sealing entire circuit-board panels.

Lebow's paper describes a multilayer system that has two of the technical breakthroughs called for by Mather. The Pactel structure is composed of sequential layers of polyimide with ultrafine copper conductors additively plated on. Solid plated vias, a feature Mather suggests, connect the layers. Thermal columns incorporated in the multilayer substrate are bonded to a metal heat support.

Units in production at Pactel have 3- to 5-mil line widths, 4-mil vias, and up to six conductive layers. In the future, the same technology may fabricate denser units with 1-mil lines and spaces and 1-mil vias.

The major advantage of this board-fabrication system is that the small vias allow greater density than can be obtained by conventional multilayer plated-through-hole pc boards or thick-film approaches. A further advantage is that vias, unlike the holes, need not go completely through the substrate, thus saving more valuable board real estate.

Heat management in this type of structure has proven superior to that in ceramic types. A copper heat column that goes through the multilayer substrate to a laminated metal heat sink allows ICs to transfer heat directly to the sink without degrading the polyimide insulation material's performance.

The starting point of board fabrication is a stainless-steel carrier with a thin coat of copper plate. A negative film resist is laminated to this surface and then exposed to a circuit pattern by an ultraviolet source. The unexposed resist is then removed and the unexposed area is additively plated with copper. The exposed photoresist is removed and polyimide is added to fill in these spaces. The process is repeated to build up successive conductive layers connected by vias. In the last step the carrier is removed from the stack of polyimide layers.

#### About face

Tape-automated bonding (TAB) came in for a share of ECC papers. One of the more innovative TAB papers was "Face-Down TAB for Hybrids" by J. L. Dais, J. S. Erich and D. Jaffe of Bell Laboratories, Allentown, Pa. It describes the use of a new face-down approach that

results in a structure that resembles a beam-leaded semiconductor. This IC packaging method appears preferable for hybrid applications where cost or area considerations dominate. Conventional face-up TAB appears better where higher thermal conductivity or backside electrical contact are required.

In a face-up TAB, specially bumped chips are mass-bonded to chip sites on patterns etched from a thin layer of copper laminated or plated on an insulating film [Electronics, Sept. 28, 1978, p. 121]. In a hybrid application, a chip and its copper interconnect are first excised from a frame of tape; then, with chip and interconnect facing up as in the Fig. 5, the back side of the chip is epoxy-bonded to a ceramic substrate and the TAB interconnect's outer leads are wire-bonded to conductive pads on the substrate.

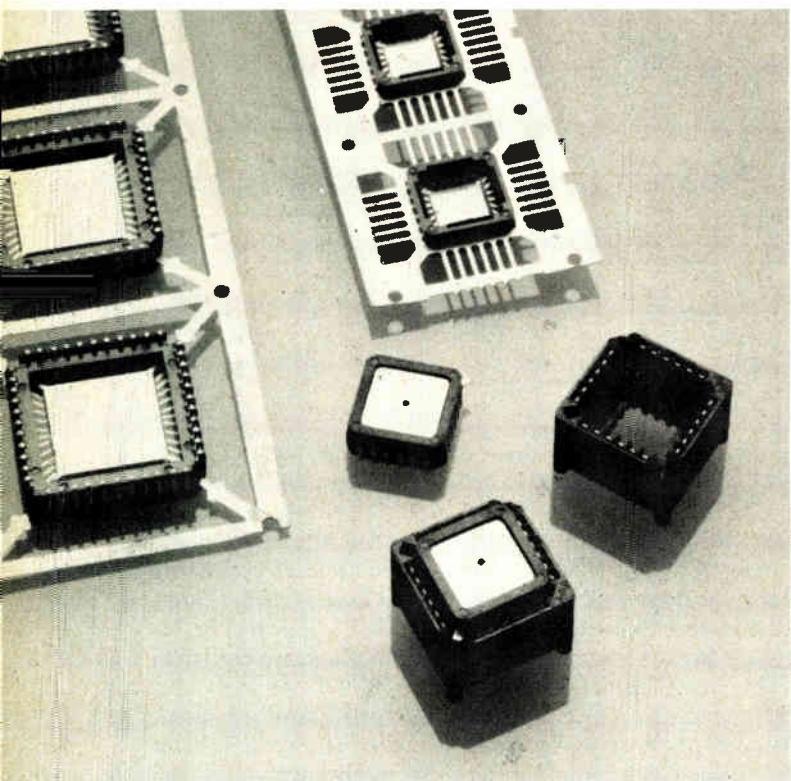
In Bell Labs' new approach, bumped chips are inner-lead-bonded to tape sites on a gold-plated copper tape. Then leaded chips are excised from the tape. The resulting package is placed face-down onto a ceramic substrate and its leads are attached to thin-film pads on the substrate with a manual beam-lead-bonding machine. After TAB bonding is complete, the circuit is cleaned and encapsulated in a Dow-Corning RTV silicon rubber.

The authors note that the face-up TAB requires five operations (chip excising, lead forming, preplacement, backside attachment, and lead bonding). By comparison, the face-down approach only needs the chip-excising and lead-bonding steps. Since the newer approach has fewer operations, it should lead to a lower assembly cost and higher yield.

Face-down TAB has one more important advantage over its rival TAB techniques. More chips per substrate area can be mounted with face-down TAB. The analysis from Bell Labs includes a comparison of face-up and face-down TAB and beam-lead packages as to the substrate area required for packages with varying numbers of leads. Face-down TAB and beam-lead packaging are shown to be comparable in required substrate area, and both offer a considerable space saving over face-up TAB.

However, face-up TAB has a much lower chip-to-substrate thermal resistance than either face-down TAB or beam-leaded chips. Thus face-up TAB is suitable for hybrids with higher power dissipation.

The authors conclude that the face-down TAB tech-



**7. Plastic under attack.** Plastic chip-carriers made by AMP Inc. with test chips coated with various protective materials were tested for 1,000 hours at 85% humidity. Of 24 samples with passivated chips and a Dow-Corning Q-3-6257 coating, none failed the test.

nique is suitable for attaching MSI and LSI chips to multichip hybrids; its size, cost, and reliability factors are comparable to those of beam-leaded chips.

Like ICs, thick- and thin-film hybrids are growing larger, denser, and more complex. The hybrid designer, therefore, is turning to the computer for help. Responding to this trend, the ECC's organizers are devoting an entire session to this topic for the first time. John C. Hurt and Clayton L. Mohr of Tektronix Inc., Beaverton, Ore., are presenting one of the more extensive and informative papers on this subject: "A Computer-Aided Design for Hybrid Circuits."

#### Software aids hybrid design

The paper describes a software system called hybrid computer-aided design (HCAD), which is currently being used for nearly all thick- and thin-film designs at Tektronix. A hybrid-circuit designer sitting at a graphics display terminal can go directly from a schematic to artwork and documentation. Component design is automatic, but component placement and interconnections are worked out interactively by the user.

The HCAD system (Fig. 6) combines interactive graphics, hybrid component modeling, design analysis, pattern-generator output, and documentation. The software, which contains about 30,000 lines of code (primarily in Fortran), resides in a Cyber 175 computer and uses a minimum of 25 kilowords. The automatic component design relies on stored models and algorithms. If necessary, the user can interactively alter these designs.

HCAD can do a thermal analysis of the layout and

interactively change the layout if necessary. A routine that handles potential fields can be called up to analyze special resistor shapes or to study methods of laser trimming. Nodal capacitance-to-ground calculations are also available.

When design and layout are completed, the system generates a magnetic tape that will run a pattern generator directly. A user can obtain a plot of the layout with undesired lines removed; the plot includes labels, title block, and process data.

#### Plastic chip-carriers

Chip-carriers, a topic new to the ECC, now rate a complete session composed of an overview and five papers. One of the papers at this session, "Humidity Test of Pre-molded Chip Carriers," by Jacob H. Martin and L. David Hanley of the Charles Stark Draper Laboratory Inc., Cambridge, Mass., could have long-term impact on chip-carrier uses. Packaging specialists have long wanted to replace the expensive, leadless, hermetically sealed ceramic chip-carrier with a low-cost leaded plastic version with a nonhermetic seal. The tests reported by Martin and Hanley demonstrated that the plastic chip-carrier has the potential to protect the semiconductor chip.

The paper describes carefully controlled humidity tests at 85°C, 85% relative humidity, and 40 volts bias. The tests were run on 24-lead premolded chip-carrier packages made by AMP Inc. and containing test chips coated with various protective materials. The same test chips were also housed in plastic and ceramic DIPs for comparison. Chips in the plastic chip-carriers survived better than those in plastic DIPs. One chip-carrier group using passivated chips and a silicon-gel potting compound had no failures at all.

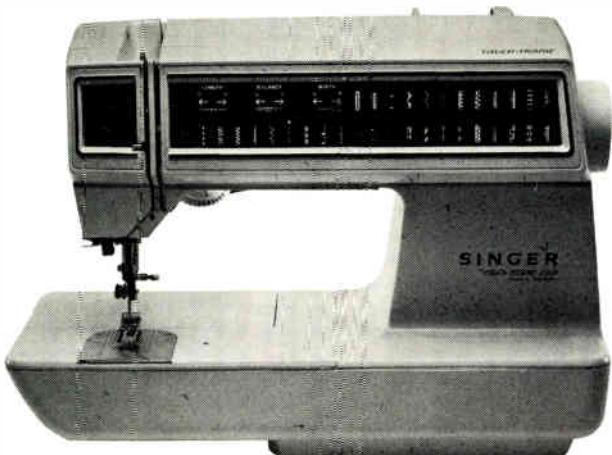
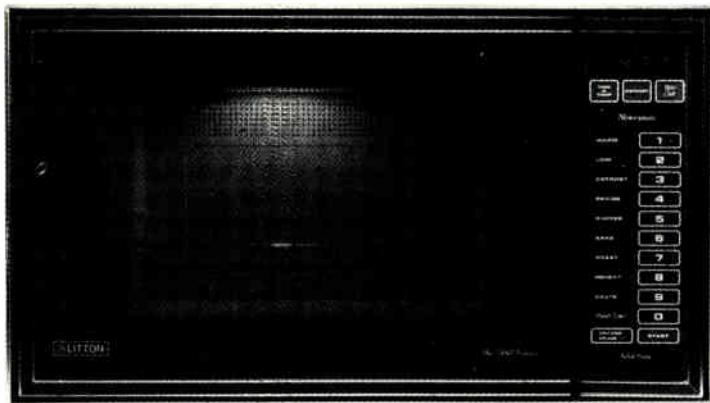
Twelve groups of 24 parts each were used in the tests. The first eight groups were AMP chip-carriers (Fig. 7) containing either passivated or unpassivated chips. Six of these eight groups used one of three common silicone potting compounds from Dow-Corning; the remaining two had no silicone protection against humidity. Two other groups were composed of plastic DIPs with passivated and unpassivated chips. The last two groups had passivated and unpassivated chips housed in hermetically sealed ceramic DIPs. Those served as the control to isolate any chip problems.

One group of plastic carriers with a Dow-Corning Q3-6527 coating and passivated chips had no failures for the full test time. Another group of carriers with the same gel and unpassivated chips had 10 failures at 30 hours, 2 failures at 100 hours, and no failures at 1,000 hours. In fact, among the carriers with silicone protection, no failures occurred during the last 700 hours of testing.

Plastic carriers with unprotected unpassivated chips had only six units left after 30 hours and were withdrawn from the test. The unprotected carriers with passivated chips fared somewhat better—10 failures in 1,000 hours.

Epoxy DIPs had the next two highest failure rates after the unprotected chips in plastic carriers. Chips in sealed ceramic DIPs survived 1,000 hours with no failures, as expected. □

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# Designer's casebook

## Converter in feedback loop improves voltage regulation

by David Abrams  
Winchester, Mass.

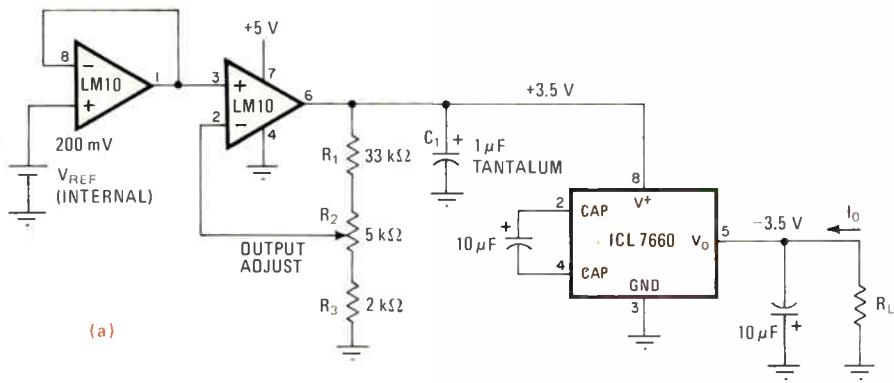
One of the most frustrating experiences a designer faces is to discover that his TTL or complementary-MOS circuit, which he intended for single-supply operation, actually requires a minus potential at some minuscule current for one or two of its integrated circuits. A new chip, Intersil's 7660 voltage converter, now enables the designer to obtain the minus voltage at low currents from a positive supply without the need for a transformer or other complicated inverter circuitry, and at low cost. In addition, placing the converter in a feedback loop that includes the chip's power—or driving—source permits a degree of voltage regulation that is not possible with the

conventional stand-alone driver configuration.

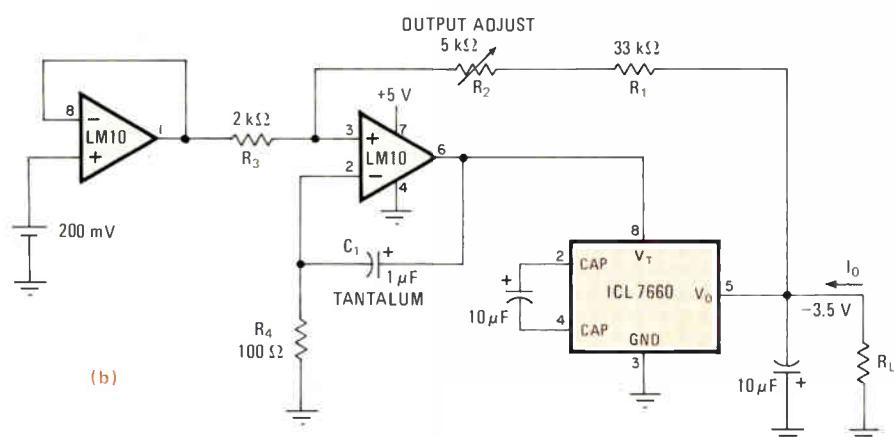
As shown in (a), the 7660 can supply  $-3.5$  volts to a single chip in a C-MOS or TTL system. The chip requires  $+3.5$  V, which is generated by the LM10 operational amplifier from the  $+5$ -V supply. Although some other low-voltage op amp and an external reference could be substituted, the LM10 will run off a single supply, has its own reference, and has an output stage that can swing within  $\frac{1}{2}$  V of the supply while delivering  $-20$  milliamperes to the 7660.

Though this circuit performs well at very low load currents, its output voltage drops rapidly as load currents increase (see table) because its output impedance is fairly high. At a no-load output voltage of  $-3.5$  V the converter exhibits an output resistance of about 100 ohms, but it will increase 50% for  $V_{out} = 2$  V. This value will render the 7660 useless in systems where more than a few milliamperes are required.

By adding a single resistor and configuring the circuit to the topology in (b), however, the converter can be made to perform much as an ideal voltage source for



R <sub>L</sub> (kΩ)	I <sub>L</sub> (mA)	V <sub>O</sub>
∞	0	3.50
10	0.34	3.45
6.8	0.47	3.37
4.7	0.74	3.36
3.3	1.02	3.34
2.2	1.60	3.30
1.5	2.22	3.26
1.0	2.97	3.20
0.68	4.48	3.08
0.47	6.12	2.94
0.33	8.23	2.73
0.22	10.38	2.48
0.15	13.50	2.06



R <sub>L</sub> (kΩ)	I <sub>L</sub> (mA)	V <sub>O</sub>
∞	0	3.50
4.7	0.76	3.50
3.3	1.06	3.50
1.5	2.35	3.50
1.0	3.20	3.50
0.68	5.06	3.52
0.47	7.02	3.42
0.33	9.38	3.19
0.22	12.13	3.02
0.15	17.42	2.81

**Regulatory loop.** Intersil's 7660 voltage inverter provides a negative output from a positive source without transformers (a), but voltage regulation is poor. Placing the 7660 in a feedback loop that includes the driving source (b) improves operation markedly.

loads of 1 kilohm or greater. The regulation for loads less than 1 k $\Omega$  will be much superior to that in (a), as seen in the table.

Here the circuit works as an inverting amplifier with a gain of -17.5, which is set by  $(R_1 + R_2)/R_3$ . The converter provides a gain of -1, requiring that the noninverting input of the op amp be used as the summing junction. Thus the circuit can still be run from a single supply because the LM10's input common-mode range includes the negative supply (ground, in this case).

$R_4$  and  $C_1$  provide local feedback around the op amp to stabilize the loop. Without these components, the delay between input and output voltage changes of the 7660 would cause the output of the LM10 to oscillate

between ground and +5 v.

In operation, the feedback loop will force the op amp to try to hold the negative output voltage constant. Even at the higher currents, the output resistance is half of what it is in (a).

The circuit may also be used to supply negative voltages other than -3.5 v. If higher voltages are desired, it is necessary to choose a supply voltage for the LM10 that will provide sufficient output from the op amp under the expected load conditions. In this case, the effective voltage gain of the 7660 drops from -0.99 v to zero, and so the output voltage of the op amp must rise as the load current increases in order to compensate for the loss of gain. □

## PLL's lock indicator detects latching simply

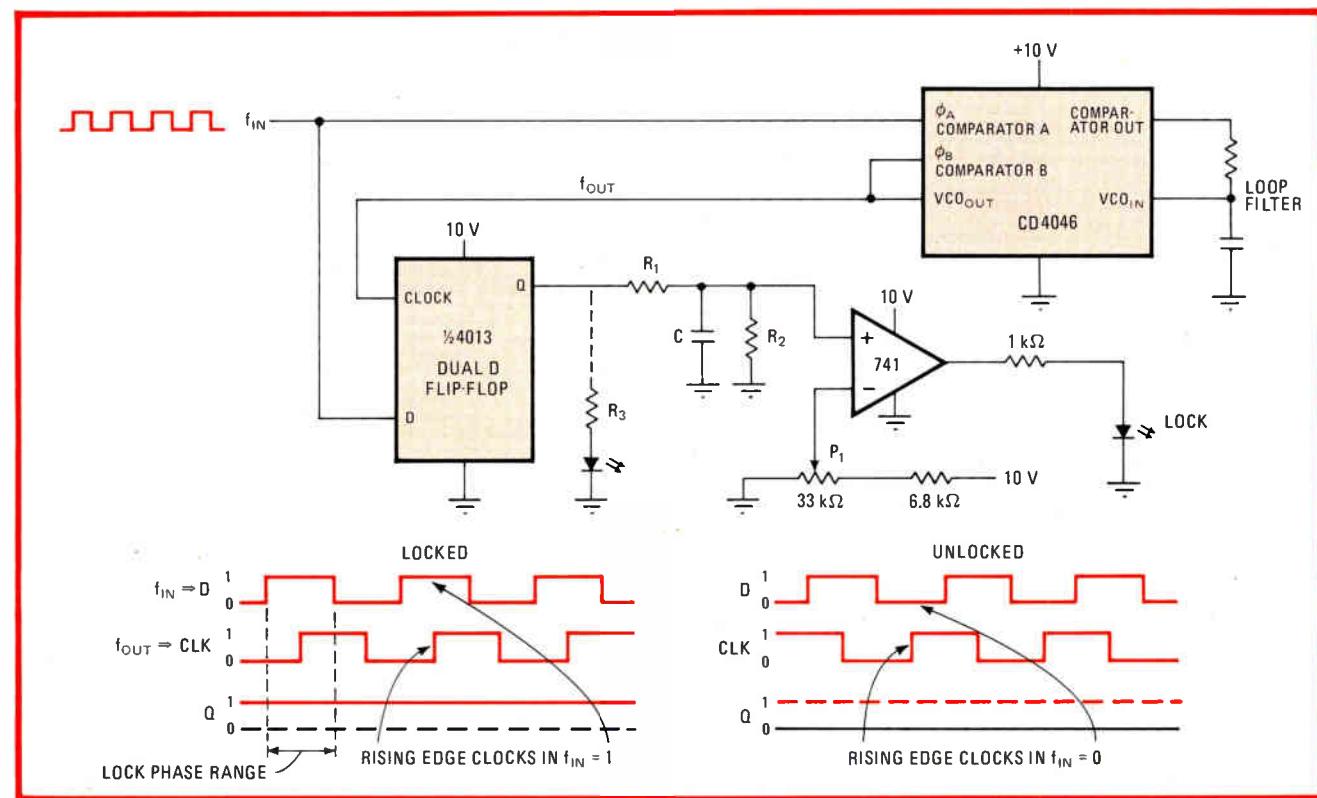
by Steve Kirby

Department of Electronics, University of York, England

Much less complex than some of the previously described lock indicators for phase-locked loops,<sup>1</sup> with no need to derive and utilize a multiple of the input frequency<sup>2</sup> for phase-comparison purposes, this circuit is easier to set up and use. It sacrifices nothing in the way of

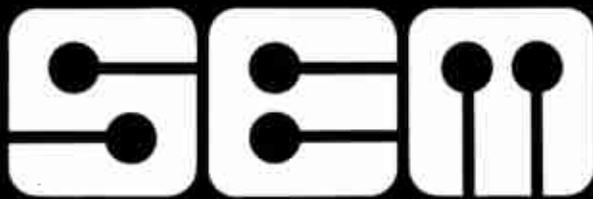
accuracy and offers other advantages, such as the ability to lock onto harmonics of the input signal.

The locking technique is illustrated for the C-MOS CD4046 PLL, whose output leads the input by 90° when the lock state is achieved. The loop's capture ratio is such that lock can be maintained for a square-wave input signal no greater than +90° and no less than -90° out of phase with respect to  $f_{out}$ . The 4013 D flip-flop detects phase differences by clocking the state of  $f_{in}$  at  $f_{out}$ 's rising edge. Assuming the PLL and its associated loop filter are working properly, a steady  $Q = 1$  at the output of the flip-flop indicates the PLL is in or will shortly be in the lock state. The noninverting input of the 741 comparator will then rise to 10 volts through integrator



**Monitor.** Only two chips, flip-flop and comparator, are needed to detect lock condition in phase-locked loop. Rising edge of  $f_{out}$  clocks in logic 1s to D input of flip-flop under lock condition, causing A<sub>1</sub> to go high and LED to light. Output of flip-flop is otherwise a random train of pulses, causing the voltage at the noninverting input of A<sub>1</sub> to drop below P<sub>1</sub>'s threshold, bringing A<sub>1</sub> low and turning off the LED.

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$R_1 R_2 C$ , and its resulting high-going output will light the light-emitting diode.

If the PLL no longer locks on frequency, the phase of  $f_{in}$  with respect to  $f_{out}$  will be random. The output of the flip-flop will thus be a train of variable-width pulses. The comparator input thus drops to approximately 5 V, and because potentiometer  $P_1$  sets the inverting input at approximately 7 V,  $A_1$  moves low, extinguishing the LED.

The lock detector will lock onto higher harmonics of  $f_{in}$ . With a 50/50 mark-to-space square-wave signal,

locking has been observed to the fifth harmonic.

If a less precise indication is tolerable, lock detection can be achieved with even fewer parts by placing an LED at the output of the flip-flop and eliminating the comparator circuitry. Resistor  $R_3$  should be selected to hold the LED dim for the out-of-lock condition. □

#### References

1. J. A. Connelly and G. E. Prescott, "Phase-locked loop includes lock indicator," *Electronics*, Sept. 5, 1974, p. 112.
2. R. P. Leck, "Logic gates and LED indicate phase lock," *Electronics*, May 29, 1975, p. 106.

## Three-chip logic analyzer maps four-input truth table

by C. F. Haridge  
University of Ottawa, Ontario, Canada

Providing an extremely simple and low-cost alternative to the use of an oscilloscope, this logic analyzer will determine the truth table of circuits with as many as four inputs. The state of the circuit for a single monitored output is displayed by a four-by-four array of light-emitting diodes arranged in a Karnaugh-map configuration. Resistor-, diode-, and transistor-transistor-logic circuits can be checked directly, and only one input/output buffer is required to check complementary-MOS designs.

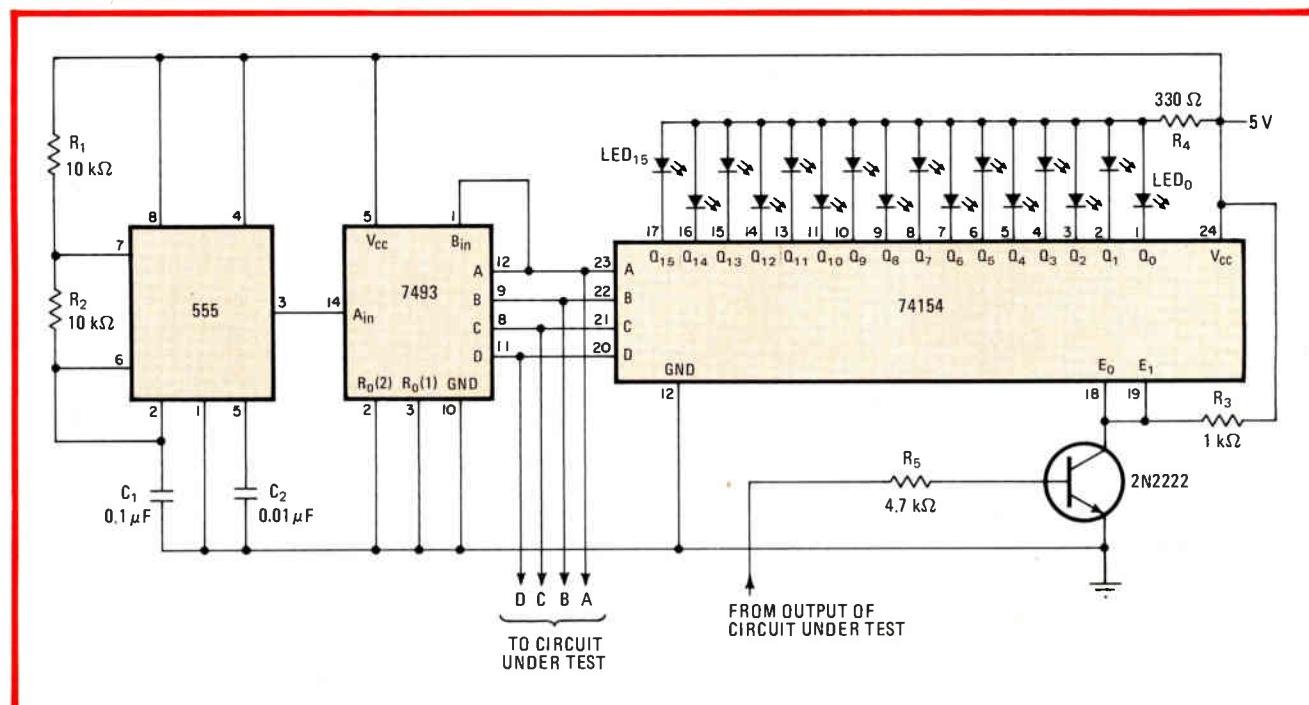
The analyzer's three basic functions—timing, scanning, and display—are achieved with only three chips: the 555 oscillator, the 7493 4-bit counter, and the 74154

4-to-16-line decoder. The 555, running at a minimum frequency of 480 hertz to eliminate display flicker, clocks the 7493 through its 16 states continuously. As a result, a binary sequence of 0–15 periodically drives the four inputs of the circuit under test. These logic signals are also applied to the decoder chip. Consequently if the instantaneous output of the circuit point under test is high for any given set of input variables A–D, the LED corresponding to the 4-bit output number of the 7493 will light up.

The analyzer may be easily expanded to test circuits having more than four inputs by adding the appropriate number of counters, decoders, and LEDs. The clock frequency must also be increased to minimize flickering in the display.

A higher clock frequency will reduce the on-time of each LED, however. In order to compensate for this reduced brightness, resistor  $R_4$  must be made proportionally smaller. □

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**Logic functions.** Low-cost logic analyzer, complete with light-emitting diodes arranged in Karnaugh-map configuration, monitor four-input circuit response. RTL, DTL and TTL circuits may be checked directly; only one I/O buffer is needed for C-MOS designs.

# Managing memory to unloose the full power of microprocessors

Memory-mapping scheme doubles Z8000's addressing capability and creates 64 megabytes of logical memory space

by Jeffrey J. Roloff  
*Central Data Corp., Champaign, Ill.*

With the memory-addressing capabilities of microprocessors reaching to 16 megabytes—the maximum currently available on an IBM System/370 mainframe—simple memory organizations are no longer sufficient. If the full power of these processors is to be realized, they must be backed up by the concepts of memory management used by mainframes and minicomputers. Otherwise the programmer would be swamped with the task of keeping track of the assigned memory.

A powerful example of the application of these concepts is a memory management circuit designed specifically for the Zilog Z8001 16-bit microprocessor. Incorporated into a recently announced single-board microcomputer, this circuitry can support up to 16 megabytes of physical main memory—twice as much as the basic Z8001. In addition, it can handle 16 logical address spaces of 4 megabytes each, for a total logical memory capability of 64 megabytes. This hardware, combined with special memory management routines incorporated into the operating system software, provides a sophisticated memory management scheme that falls just short of virtual memory.

The segmented memory architecture of the Z8001 (see "The Z8000 processors," p. 132) facilitates this management scheme. Thus this design cannot be directly carried over to other systems, but the concepts employed can just as easily be used with other processors.

## On board

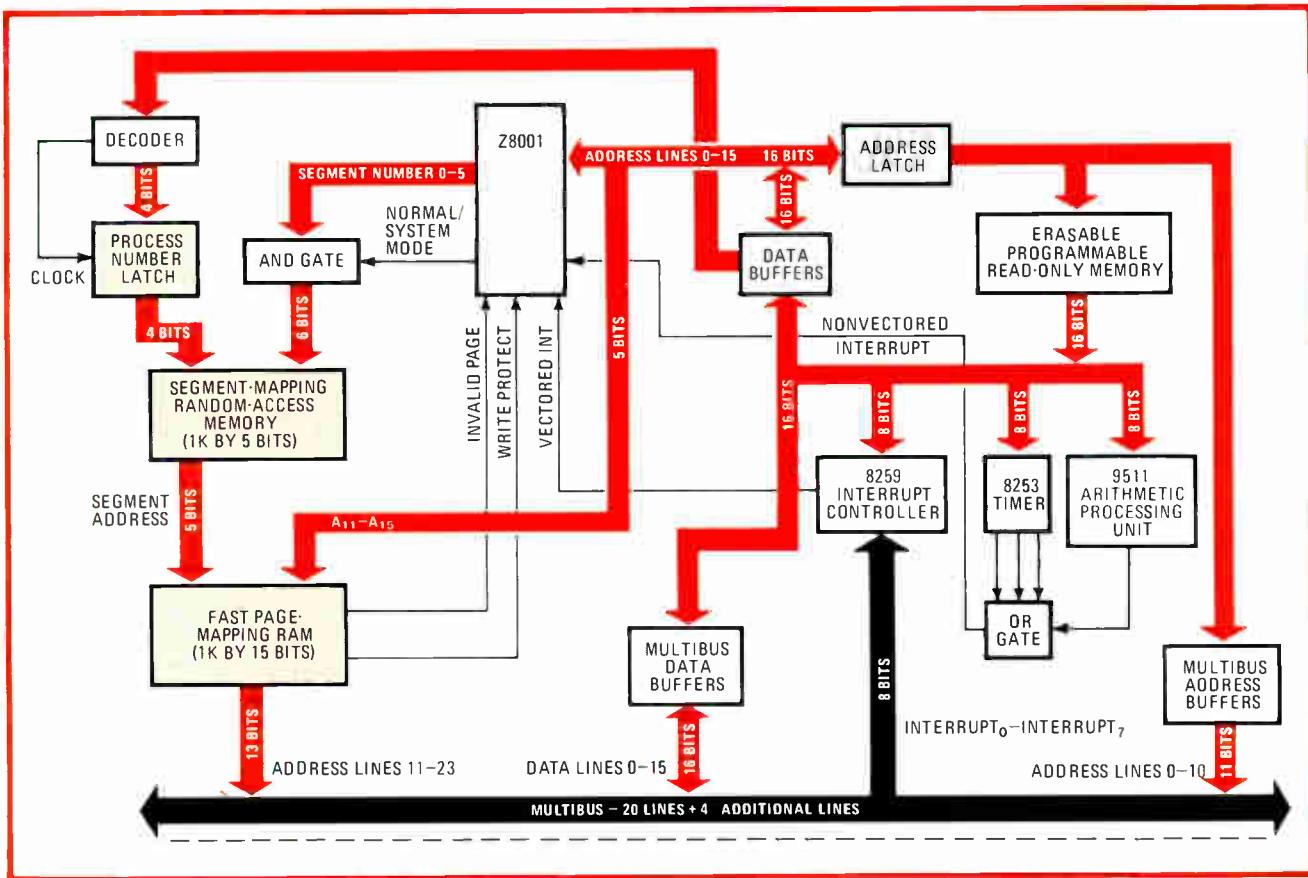
The Central Data microcomputer board can be the main central processing unit of any Multibus system (Fig. 1). The Z8001 runs at a speed of 4 megahertz, and its lines are gated to be completely compatible with the Multibus. The board also allows the user to have several of these processor boards and direct-memory-access devices on the bus at one time.

The microcomputer board can handle two 16-K 2716 erasable programmable read-only memories to hold any monitor or bootstrap program. These E-PROMs are automatically selected when the system is initialized and can be deselected by writing to an output port.

Among the peripheral chips used on the board are an Intel 8253 programmable interval timer, with which interrupts with delayed starts of from 1 microsecond to 65 milliseconds can be generated. An Intel 8259A interrupt controller enables the program to set various interrupt priority levels to the Multibus's eight interrupt lines. An optional Advanced Micro Devices Am9511 arithmetic processor allows the user to perform complex floating-point arithmetic operations outside of the Z8001 microprocessor chip.

Central to the board's memory management circuitry are two fast random-access memories that function as the segment and page maps. A 4-bit latch holds the process number, a new portion of the address that was added just for this memory management scheme. Furthermore, to allow for the 24-bit addresses necessary to access 16 megabytes of memory, 4 lines were added to the 20 lines of the Multibus.

The memory management circuit functions as an address translator for any memory request. Logical addresses used in programs and generated by the Z8001



**1. Specialized hardware.** Among the special circuitry added to this Z8000-based microcomputer board to manage memory are the process number latch and two mapping RAMs. Four extra lines were added to the Multibus to handle the 24-bit addresses.

are changed to physical addresses to reflect where in physical memory the required data actually resides. The basic Z8000 addressing structure accesses 8 megabytes of memory through a two-tiered segmentation scheme. A 7-bit segment number points to 1 of a total of 128 segments, and a 16-bit offset, or address, refers to 1 of the 65,536 bytes contained in each segment.

### The process number

As mentioned above, this design adds one more level of addressing: a 4-bit process number. This extra level was developed to allow more than one program or user to run on the Z8001 at a time. It establishes 16 separate logical address spaces that are completely independent; that is, one user or program cannot unintentionally access another's memory. Furthermore, both the logical memory and the physical memory are divided into pages 2 kilobytes in size.

The process number points to the address space currently in use (Fig. 2). Each address space is subdivided into 64 segments, indicated by segment numbers. The segments are further subdivided into pages, which are referred to by page numbers. Finally, each individual byte in the page can be addressed.

The process number enables the operating system to manage memory more efficiently. This is especially evident when switching between different programs in a timesharing environment. All that needs to be done is to save the contents of the registers and the CPU status and

to change the process number stored in the latch. Once the process number is changed back and the other process is again being executed, it will have the same address space it had before it was interrupted.

The first memory map (process number 0000) is reserved for the operating system. To further differentiate the operating system's address space from the others and ensure its independence, its segments are numbered 064 to 127. All the other spaces use segments that are numbered 000 to 063.

When the operating system is running, the Z8001 is said to be in the system mode; in the normal mode, a user's program is being executed. To prevent any user's program from interfering with the operating system, any references to segment numbers over 063 are trapped when the Z8001 is in the normal mode.

### The mapping process

Essentially, the mapping process manipulates the three components of the logical address to generate a physical address (Fig. 3). First, remember that the operating system running on the Z8001 in the system mode assigns 1 of the 15 available process numbers to each user of the system. It also sets up tables to keep track of the amount of memory requested by each user and the number of segments he intends to use and establishes the memory maps that allocate physical memory pages to those segments. Then, as the operating system lets another program, or process, become active, it writes the

## The Z8000 processors

The basic architecture of the Z8000 16-bit microprocessor includes 16 16-bit general-purpose registers and seven types of data, ranging from single bits to 32-bit-long words and word strings [Electronics, Dec. 21, 1978, p. 81]. Eight addressing modes are available, and the instruction set includes 110 instructions that, when combined with the various data types available, offer a total of 414 instructions.

The Z8000 operates in two modes: system and normal. The system mode allows certain privileged operations that the normal mode does not, facilitating the isolation of operating system software from applications software.

The chip comes in two versions. The Z8002 can address

only 64 kilobytes of memory and is called the nonsegmented version. The Z8001, used with this memory management system in the Multibus Z8000 CPU board, has a segmented memory that can directly access 8 megabytes of memory.

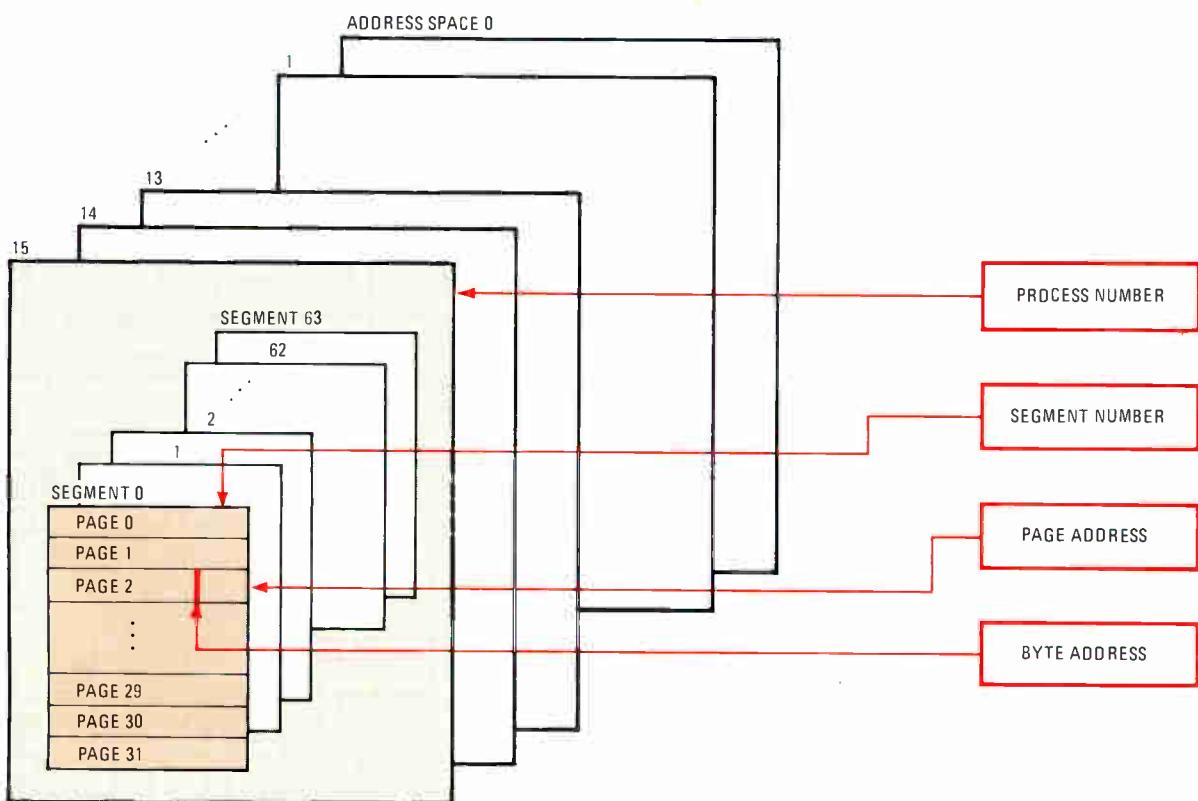
To support this segmented-addressing technique, the Z8001 uses a 23-bit address: the basic 16-bit address, plus a 7-bit segment address. The segment address points to 1 of 128 segments that contain up to 64 kilobytes each; the 16-bit address, or offset, indicates which of the bytes in the segment is being sought. The two parts of the address may be manipulated separately, facilitating the memory-mapping technique explained in the main text.

appropriate process number into the latch and changes the Z8001 to the normal mode.

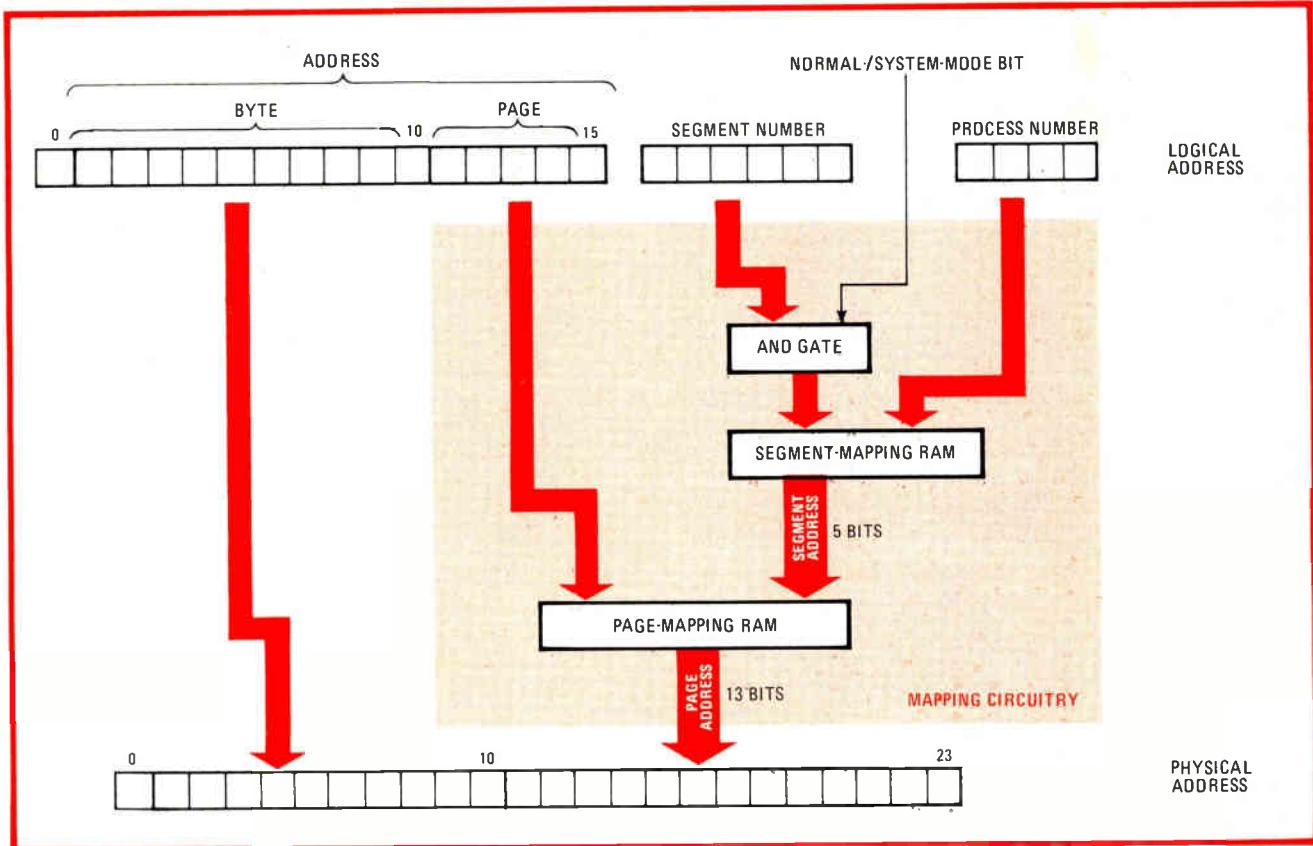
For each memory access, the Z8001 places the segment number out on its segment pins one clock cycle before the address lines become valid. When the segment number becomes valid, 6 of its bits are fed into the address lines of the segment-mapping RAMs, along with the output from the process-number latch. The seventh bit is not used in this mapping scheme, but the Z8001's normal-/system-mode signal is gated with the segment number to ensure a valid reference. The output of the segment map is the 5-bit segment address.

The segment address is then sent to the address lines of the page-mapping RAM, along with the upper 5 address bits from the Z8001. The page-mapping RAM determines exactly which page of a program's segment is being accessed. The output of this RAM, called the page address, joins the lower 11 Z8001 address bits to form the 24-bit expanded Multibus address.

Two additional outputs from these RAMs prevent an unmapped page from being accessed and memory from being mistakenly written into. If any page in a segment has not been assigned a corresponding physical address space, it is considered unmapped, and one output goes



**2. Multilevel concept.** Logically there are 16 address spaces of 4 megabytes each, indicated by the process number. The segment number points to one of the 64 segments, whose 64 kilobytes are divided into 2-kilobyte pages, each byte of which is selectable.



**3. Mapping.** Segment-mapping RAM turns process and segment numbers into a segment address, which is added to the upper 5 bits of the Z8000 address to find the page address in the page-mapping RAM. That plus rest of Z8000 address makes up the 24-bit physical address.

low. Likewise, if a write is attempted into a read-only page, the other output goes low. Either of these outputs causes a segment trap to occur, interrupting the Z8001 so that the problem can be resolved.

Also, segment address 31 always causes a trap because all 32 of its pages are kept unallocated and reserved for the operating system to keep track of unused pages of physical memory.

### More than enough

Although each user can logically use 64 segments, he is limited to the number of segments that are active, or mapped, at any one time. The reason is that only 32 real segment addresses are available, since the segment address from the segment map is 5 bits long. Each process can therefore generally have only 2 of its 64 segments active at any time. But because the circuit is designed with RAM, the number of segments assigned to each program is not dependent on any other program (except that the total of 32 cannot be exceeded). This means that one program could have 17 active segments and the other 15 programs 1 segment each, or any other combination totaling less than 32 segments.

Because most programs will need to work with only a total of one or two segments, there should be no need to have more than 32 process and segment combinations active at one time. Should that be necessary, however, the operating system software can remove certain maps from the segment-mapping RAM until they are needed. In this manner, one process can easily access 32 seg-

ments at once—which is 2 megabytes of storage if each page of each segment is allocated.

If a program needs more than 32 segments, the memory management software routine can map only those segments currently in use. This procedure allows a full addressing capacity for each program of up to 64 segments. However, virtually every system will use far less than the 32 segments available, making it unnecessary to swap maps in and out. Still, the board has been designed to allow larger numbers of segments with relatively little overhead. Remember that each program has its own set of segment numbers, each independent of the other programs or processes. The unique segment address assigned to the process and segment number combination by the mapping hardware takes the place of the address relocation required during program loading in systems with a single address space.

### Not virtual

What keeps this scheme from being a complete virtual memory system is the fact that it does not actually swap pages of data into and out of physical memory. Instead, it leaves all the data in physical memory and merely changes the maps to reflect which pages are active at any one time. Also, whereas virtual memory systems can automatically detect that the required data is not in physical memory and take the actions necessary to locate it, this system requires the user to handle those house-keeping chores. When other pages are needed, the user must issue a system call to tell the operating system to

## Another way to go

Recognizing that memory management would be critical to the success of its 16-bit microprocessor in large systems, Zilog has developed its own memory management circuit, the Z8010. It will be available later this year.

The Z8010, called a memory management unit, or MMU, supports a single address space containing 64 segments that can vary in size from 256 to 65,536 bytes. These segments can be mapped into a total physical address space of 16 megabytes. Two MMU chips must be paired to support the entire 128 segments available on the Z8001, and multiple memory management units can be used to support the translation tables needed for multiple logical address spaces.

Using 22 special input/output instructions, the Z8001 in the system mode controls the memory management unit. The system software sets up the translation table in the MMU by arbitrarily assigning program, or logical, seg-

ments to blocks of physical memory. It can also provide those segments with special attributes, such as read only, that protect the memory.

The MMU translates the 23-bit logical address of the Z8001 into a 24-bit physical address that maps into physical memory. The MMU's management scheme divides physical memory into 256-byte blocks and assigns segments to contiguous blocks.

A translation table in the MMU, set up by the operating system, starts the memory-mapping process by converting the 7-bit logical segment number into the base address of that segment in physical memory (see figure). The 16-bit base address is then added to the upper 8 bits of the logical address, or offset. The result is the upper 16 bits of the 24-bit physical address, while the lower 8 bits of the logical offset are carried forward to complete the physical address. By having this low-order portion of the address bypass the memory management unit, the number of pins on that chip is reduced.

Each memory segment is assigned several attributes that serve to protect it. When the chip detects that any of these attributes are being violated, it generates a segment trap. In the case of an access violation, the MMU activates a suppress condition that inhibits memory writing or flags special data to be returned on a read access. The segment trap remains activated until acknowledged by the processor.

When multiple MMUs are used, several schemes are employed to choose the correct chip. The first approach, used to pair MMUs to support the full 128 segments, employs the upper-range-select flag in the MMU's mode register, in connection with the seventh bit of the segment number, to indicate that a second MMU is handling an additional 64 segments.

When multiple MMUs are used to hold several translation tables, or maps, the multiple-segment-table and normal-mode-select flags in the mode register, together with the normal-/system-mode signal, are used to select the appropriate MMU. Special external circuitry must be added, however, to monitor the Z8001's status lines and manipulate the MMU's normal-/system-mode line to perform this selection.

-Anthony Durniak

change the map and activate them. The primary reason for this limitation is that the Z8001 cannot be interrupted in the middle of an instruction in order to complete the memory management chores. It requires the instruction to be finished, even if the proper data is unavailable, and a complete context switch to be performed. This inherent part of the design would make a true virtual memory system inefficient.

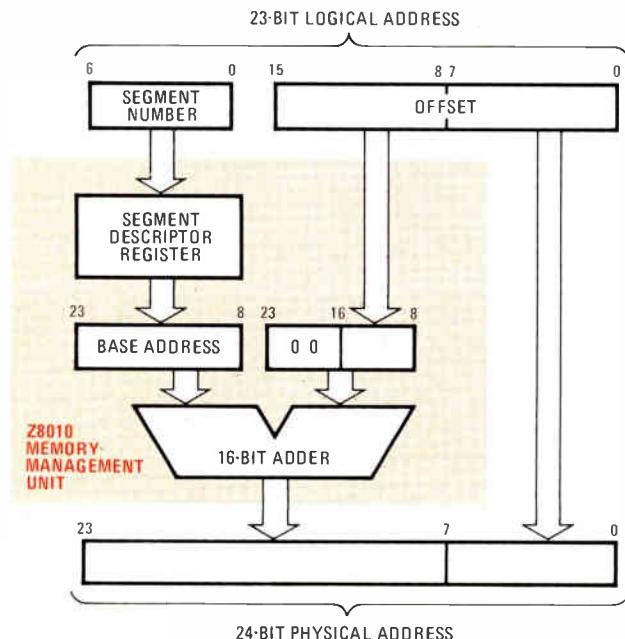
As mentioned earlier, the user must tell the operating system how many segments are required. Before the process, or program, can access any memory, the operating system must construct a map allocating physical memory to each segment in use. If not enough physical memory is available, the user is placed in a queue to wait until another process stops and the memory assigned to it becomes available.

Rather than use some of the physical memory addresses to refer to the mapping RAMs, these RAMs are treated as input/output ports of the Z8001. Since the

two RAMs require just 1,024 addresses each, and the Z8001 can address some 64-K I/O ports, that amount of overhead poses no problem. To set up the maps, then, the operating system executes output instructions. The segment map starts at output-port address  $8000_{16}$ , and the page map uses output-port addresses starting at  $A000_{16}$ .

Because of the structure of the translation process, memory sharing between processes can be accomplished easily. Since all logical addresses must be mapped to their physical counterparts, it is a simple procedure to map two different logical pages from different processes to occupy the same physical address location.

Likewise, since each combination of process number and segment number is assigned an arbitrary segment address by the mapping circuitry, two or more processes can share an entire segment by simply assigning the same segment address to each process's segment map. Yet these shared segments need not have the same logical segment numbers for the processes involved. □



# Special-function modules ride on computer board

Smaller cards donate floating-point processing or added serial and parallel I/O to primary single-board computer; memory is extensible on the main card

by Gary Sawyer, Jim Johnson, David Jurasek, and Steve Kassel, *Intel Corp., Hillsboro, Ore.*

□ In the design of board-level computers, two basic methods coexist. One is to pack each card with integrated circuits to the limits of its capacity, and the other is to distribute the computer functions among other boards occupying additional card slots.

Both approaches have their advantages. The single powerful module conserves space and expensive connectors, while the decentralized boards allow the user to pick and choose functions—and add them incrementally—although the expense of one board might spell overkill for one particular application.

A new concept in single-board computer architecture strikes a neat compromise between both camps. Rather than cram more chips on an already overstuffed board, the idea is simply to provide it with a connector for plugging in smaller modules having limited functions for specialized applications.

## Best of both worlds

This is the idea behind iSBX Multimodule boards, which cost from \$155 to \$450 apiece. Plugging into a primary processor card, 10.5-square-inch boards with various types of memory or input and output functions provide the larger single-board computer with more versatility. Linking the base board and these Multimodule boards is a new 36-line bus called the iSBX bus, for single-board expansion. This interface is destined to match the popularity of the main board's Multibus interface connector (Fig. 1).

The iSBX bus is derived directly from the on-board microprocessor system bus and, as such, an iSBX-compatible board becomes an integral element of the single-board computer. The physical interface uses a unique connector designed specifically for the iSBX bus. The bus is brought to a female connector on the single-board computer; its male equivalent is resident on the iSBX board (Fig. 2).

The iSBC 80/10B board in Figs. 1 and 2 is the first single-board computer to be compatible with the iSBX bus. Upwardly compatible with its predecessor, the iSBC 80/10A, the iSBC 80/10B is functionally equivalent but offers significant enhancements.

The iSBC 80/10B board offers direct functional expansion in three dimensions—not only read-only memory (as in the iSBC 80/10A), but also static random-access memory and input and output, as facilitated by

the Multimodule boards. One kilobyte of static RAM is provided along with sockets for expansion in increments of 1-K bytes to 4-K bytes using standard 2114A-5 memories. Read-only memory may be expanded with standard ultraviolet-light-erasable and mask-programmable types to 16-K bytes.

The iSBC 80/10B also features an on-board 1.04-millisecond timer with ongoing clocking that users may optionally configure for microprocessor interrupts. In addition, power-fail control is provided for the 2114A-5 static RAMS, enabling the user to add battery backup if the memory contents must be preserved.

## Three Multimodule boards

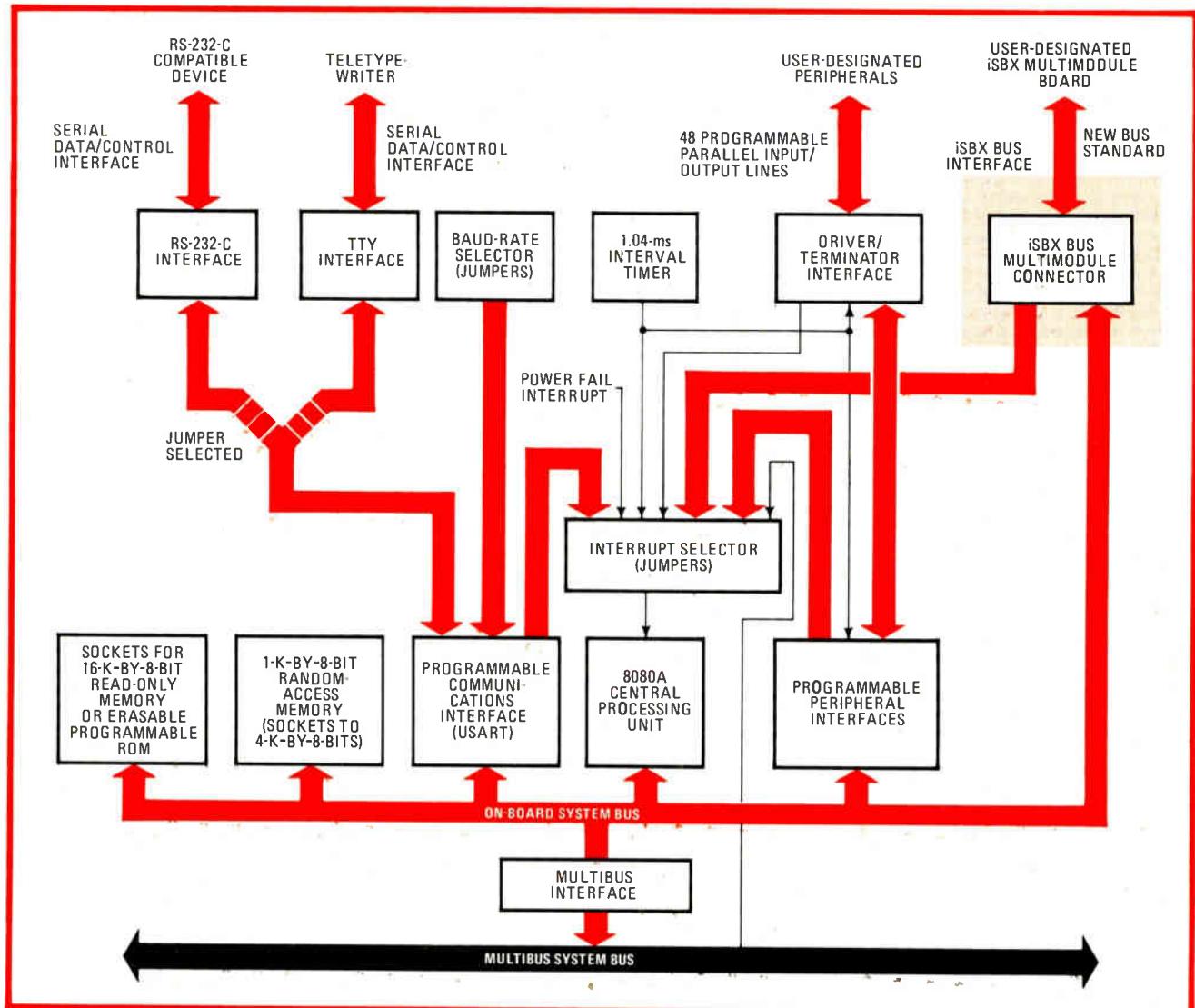
Being introduced along with the iSBC 80/10B are three Multimodule boards that expand the functional capacity of the single-board computer. Two of these, the \$155 iSBX 350 and \$230 iSBX 351, provide the same kind of input/output functions as are to be found on the processor board, only more of them.

For example, the 48 programmable I/O lines on the iSBC 80/10B board may be expanded to 72 lines by simply plugging in the iSBX 350 module—a 50% increase. Serial I/O is similarly expanded with the iSBX 351 module, which provides a programmable universal synchronous-asynchronous receiver/transmitter, or Usart (an 8251A), for compatibility with the RS-232-C and RS-449/422 interfaces. The iSBX 351 module further offers software-selectable baud rates and two programmable 16-bit binary or binary-coded decimal timers.

The third Multimodule board adds otherwise unavailable high-speed math capabilities to the iSBC 80/10B board. The \$450 iSBX 332 board uses the 8232 floating-point processor for arithmetic compatible with the standard currently being proposed by the Institute of Electrical and Electronics Engineers.

Many applications require a custom design. To complement the standard family of Multimodule boards, the iSBX 960-5 is provided. This includes five male iSBX connectors, and a full bus specification is available for custom interfacing by the user. This combination permits a user to satisfy his or her requirements for specialized I/O interfaces with the Multimodule concept.

The Multimodule concept can be divided into two logical elements: base boards and Multimodule boards.



**1. Distributed.** The first processor card to receive the iSBX bus connector is the iSBX 80/10B, a follow-on to the iSBX 80/10A. The off-board system bus is the Multibus, which interfaces to the on-board system bus. This, in turn, connects to the Multimodule board connector.

The base board is the master of the system in that it controls communication between the base's microprocessor and the Multimodule board's port. Though the first base board is a single-board computer—the iSBX 80/10B—Multibus-compatible slaves and intelligent I/O boards will also incorporate iSBX bus interfaces. The Multimodule board is a slave of the system in that it carries out I/O commands from the base board.

### The iSBX interface

The iSBX bus specification includes both electrical and mechanical characteristics. The mechanical interface is convenient and rugged; the Multimodule board is mounted to the base board in two places, at the top with a screw and at the bottom by the iSBX bus connector. The connector is extremely reliable. It has gold-plated phosphor-bronze contacts, it is keyed to assure proper orientation, and a shroud protects its pins during handling. The connector also incorporates interlocking tabs to ensure a solid mechanical interface.

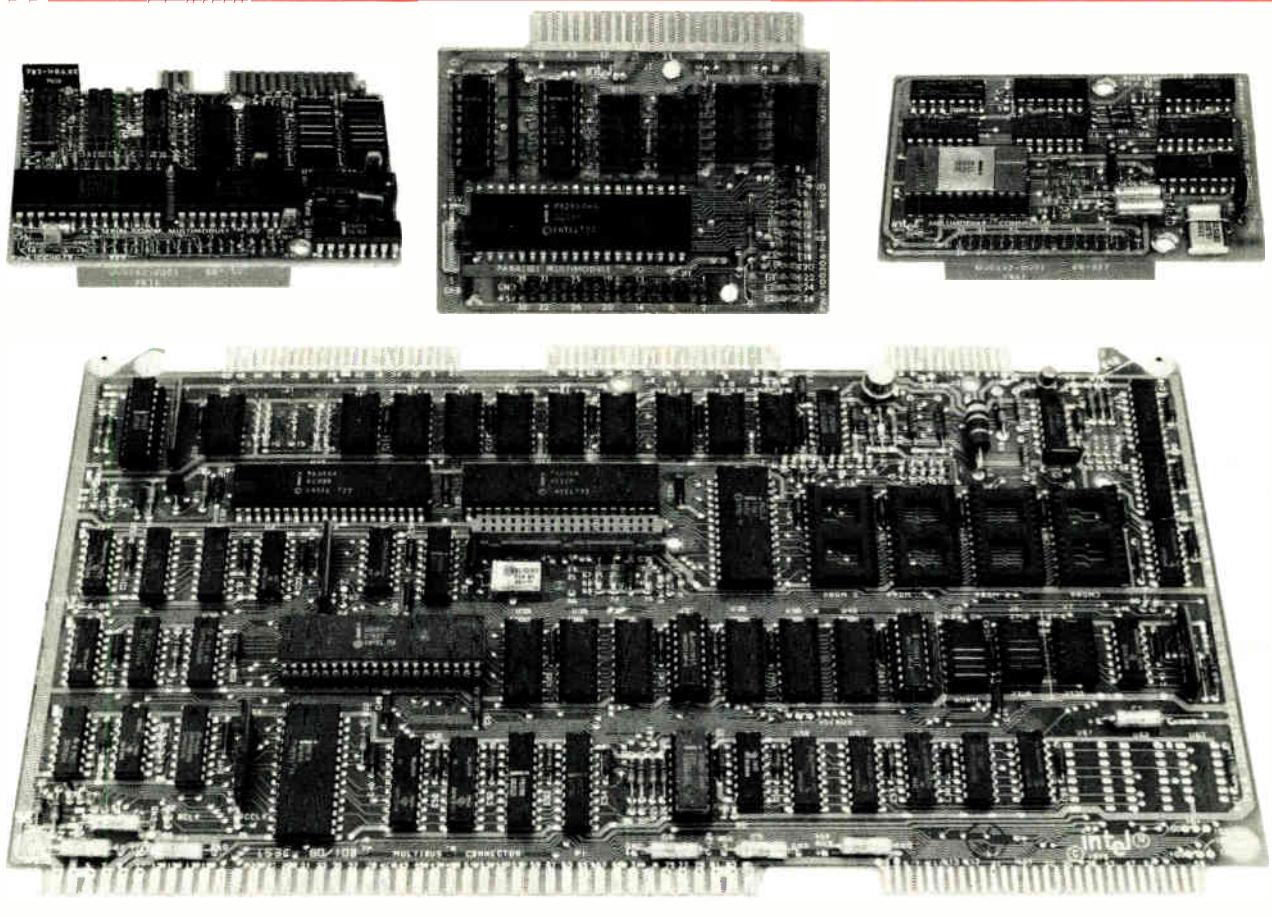
Electrically, the iSBX bus interface lines can be

grouped into six classes—control, address and chip select, data, interrupts, options, and power—for a total of 36 signal lines.

Control lines can be further grouped into those for commands, initialization, a clock, and system control. The two command lines (IORD/ and IOWRT/) are active-low I/O-read and -write signals that control the communication link between the base board and the Multimodule board. With a chip-select signal, an active command line indicates that the address lines are valid and that the Multimodule board should perform a specified operation.

The initialize line (reset) is an active-high input line from the base board that puts the Multimodule board into a known internal state. The clock line (MCLK) has a frequency of 10 megahertz, +0% or -10%. Being asynchronous with respect to all other Multimodule signals, this frequency can vary from base board to base board.

The remaining control lines, MWAIT/ and MPST, are output signals from the Multimodule board that control the state of the system. MWAIT/, active low, puts the



**2. Three to one.** Below is the iSBC 80/10B main processor board, and above it are the three new Multimodule boards. They are, from left to right, the iSBX 351 serial I/O module, the LSBX 350 parallel I/O module, and the iSBX 332 floating-point mathematics Multimodule board.

base-board processor into a wait state, allowing the Multimodule board extra time to perform a requested operation, if necessary. MWAIT<sub>/</sub> is generated from address and chip-select information only. MPST is tied to ground on the Multimodule board to inform the base board that a Multimodule board has been installed.

The second class of iSBX bus lines includes the address lines ( $MA_0$ - $MA_2$ ) and the chip-select lines ( $MCS_0$ , and  $MCS_1$ ). The base board decodes I/O addresses to generate the chip-select signals for the Multimodule boards. In so doing, it normally decodes all but the three lowest-order addresses ( $MA_0$ - $MA_2$ ). A base board normally reserves two blocks of eight I/O ports for each iSBX bus connector provided.

#### Defining the lines

Eight bidirectional data lines ( $MD_0$ - $MD_7$ , active high) carry information to and from the Multimodule ports.  $MD_0$  is the least significant bit. The two active high interrupt lines from the Multimodule board,  $MINTR_0$  and  $MINTR_1$ , make interrupt requests to the base board.

Two optional lines,  $OPT_0$  and  $OPT_1$ , are connected to wire-wrapped posts on both the base and Multimodule boards. They may serve either as additional interrupts from the Multimodule board or as special signals from the base board.

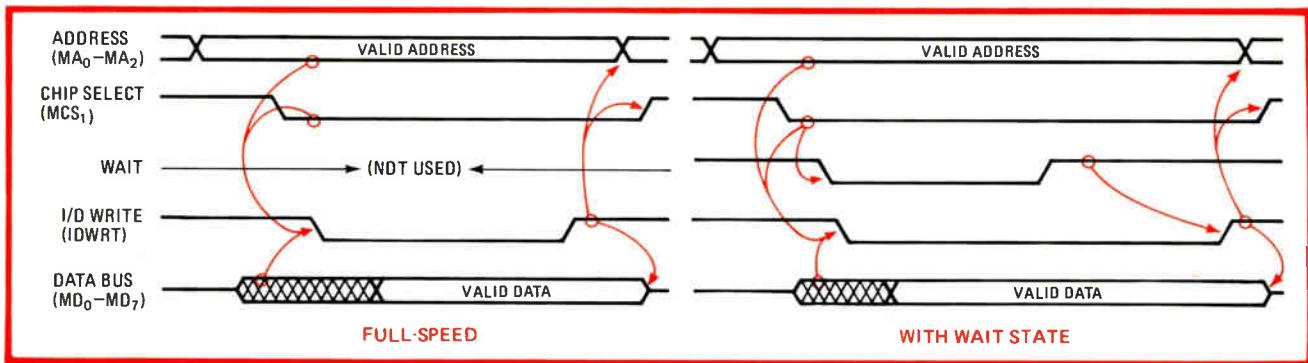
Finally, all base boards provide +5 and  $\pm 12$  volts to the Multimodule boards. These power lines complete the six iSBX bus classes.

The primary function of the iSBX bus is to provide a path for I/O-mapped data between base board and Multimodule board. This happens when the base board performs an I/O-read or I/O-write operation. There are two types of I/O-write operations, and the Multimodule board determines which is performed.

#### Data transfers

The first is a full-speed I/O write (Fig. 3). The base board generates a valid I/O address and chip-select and activates the  $IOWRT_1$  line after the set-up times are met. The  $IOWRT_1$  line will remain active for a minimum of 300 nanoseconds and the data will be valid for a minimum of 250 ns before  $IOWRT_1$  is removed. The base board then removes the data, address, and chip-select signals after the hold times shown in the timing diagram.

The alternative I/O write is a write-with-wait, used by Multimodule boards that cannot write into an I/O port at full speed. Again, the base board generates a valid address and chip-select. The Multimodule board activates the  $MWAIT_1$  signal based on address and chip-select information. This will remove the ready condition from the processor, causing it to go into a wait state after the write command has been activated and valid data



**3. Write types.** Two modes of sending information to a Multimodule board are available: full-speed and with a wait state. The wait line is not used for peripherals that meet the full-speed specifications. The wait signal extends the time for which data remains valid.

provided. The Multimodule board will remove the MWAIT/ signal—allowing the processor to leave its wait state—when it has satisfied the write-pulse-width requirement. The base board removes the write command, then the data, address, and chip-select signals, after the hold times are met.

There are two types of I/O-read operations as well, and again they are determined by the Multimodule board. The first is a full-speed I/O read (Fig. 4). The base board generates a valid I/O address and chip-select and, after the set-up timings are met, it activates the IORD/ line. The Multimodule board must generate valid data from the addressed I/O port in less than 250 ns. The base board reads the data and removes the command, address, and chip-select signals as indicated in the timing diagram.

Read-with-wait, whose timing is at right in Fig. 4, is used by Multimodule boards that cannot perform a read operation under the full-speed specifications. The base board generates a valid address and chip-select, just as with a full-speed read. However, the Multimodule board now activates the MWAIT/ signal, which in turn removes the ready input to the base's processor, putting it into a wait state. The processor activates the IORD/ signal before going into a wait state.

The Multimodule board will remove the MWAIT/ signal when valid data can be read from the data bus. After reading the data, the base board removes the command, address, and chip-select signals.

The iSBX 351 serial I/O board is a good example of how easily large-scale integrated circuits may be interfaced by the iSBX bus. It presents the iSBC 80/10B

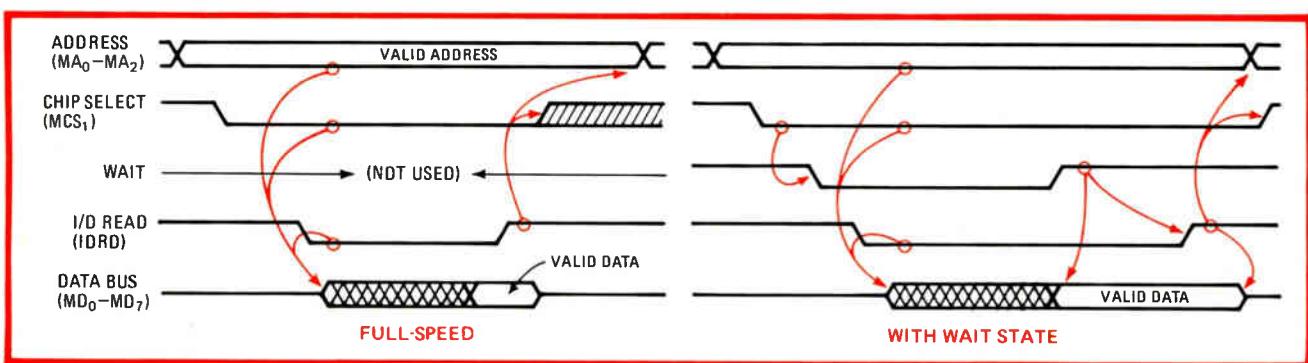
board with a second serial port.

The iSBC 351 board (Fig. 5) provides a synchronous or asynchronous serial communications channel with programmable format and baud rates up to 64 kilobits per second. In the synchronous mode, the user selects via software the number and format of the synchronization characters and the number of data bits. Parity may be even, odd, or disabled. In the asynchronous mode, the number of data bits and stop bits, as well as parity generation and detection, may be specified under program control. The added channel is compatible with either the RS-232-C or RS-422/449 interface.

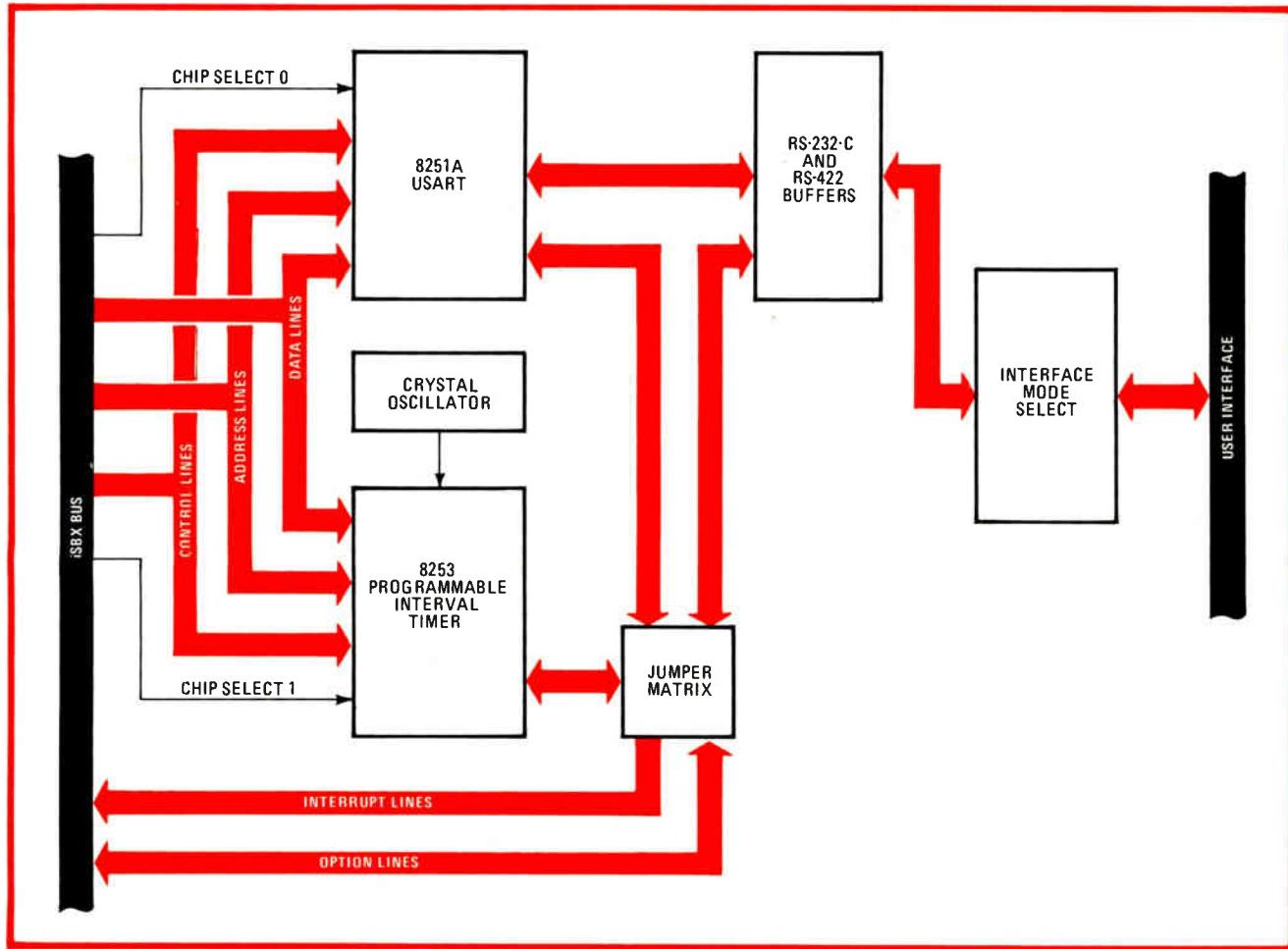
Two additional 16-bit counters are on the board for other uses. Their mode of operation and count value may be written or read under program control. With the interrupt lines provided by the iSBX bus, they may also be used as real-time interrupt sources (see Table 1).

As stated earlier, an 8251A Usart gives the iSBX 351 module a high-performance communications channel. In addition, an 8253 programmable interval timer (PIT) provides the three counters for clock generation and timing. Note in the block diagram of Fig. 5 that both devices are connected directly to the data, address, and command buses with no buffers. (Each chip, however, has its own chip-select line, preventing data bus contention.) The absence of buffers keeps the parts count down and the speed up.

Also shown in the extra block diagram are two optional lines that may be used as additional interrupt lines or to interface to the additional timer/counters. There are four interrupt sources on the board. Two, from the 8251A, indicate either that a character has been received



**4. Read types.** As in writing data into a Multimodule board, information is read from it in one of two ways: full speed or read-with-wait. The wait state extends the length of time that data is valid. This is necessary for slower transactions such as analog-to-digital conversions.



**5. More serial I/O.** The iSBX 351 serial input/output Multimodule board provides the base processor with an additional synchronous or asynchronous communications channel—one that is compatible with either the RS-232-C or the RS-422/449 interface specifications.

for reading or that the transmitter buffer is empty and ready for transmission. Two other interrupts may be generated by the timer/counters. The timers count from an on-board crystal-controlled oscillator.

#### Compatible with both

The iSBX 351 module uses a unique split-edge connector to provide compatibility with both RS-232-C and RS-449 interfaces. RS-232-C is commonly used to communicate with terminals, modems, and other equipment up to a distance of 50 feet away. RS-422 is a new interface that allows high-speed data transfers of up to 4,000 feet through differential lines that reduce noise such as crosstalk. The iSBX 351 module is the first expansion board to offer both interfaces.

The iSBX 351 module is programmed by a series of I/O-read and -write commands. Table 2 shows the I/O port assignments on the iSBX 351 module by way of explaining the code sequences in Table 3 that run on it. The first routine in Table 3, INIT, initializes the 8251A for asynchronous operation and programs the 8253 to generate a baud rate of 9,600. XMIT takes a character from the C register of the 8080A and sends it to the Usart for transmission. RECV gets a character from the Usart and places it in the accumulator. Note that in both data-transfer routines the Usart status register is check-

ed to ensure proper operation.

The iSBX 350 programmable I/O Multimodule board provides 24 general-purpose I/O lines (or three 8-bit ports) via a standard 50-pin edge connector, giving the iSBX 350 a total of 72 I/O lines. The 8255A is the only LSI component on the board, and six sockets are provided for line drivers or terminators.

Two bidirectional inverting 4-bit bus transceivers are provided for one of the three ports; sockets for the other two are TTL-compatible, allowing the use of inverting, noninverting, or open-collector drivers. When either of these other two ports is used as an input, the lines may be terminated either with 1-kilohm pullup resistor packs or with 220/330-ohm pullup/pulldown resistors.

TABLE 1: iSBX 351 SERIAL INPUT/OUTPUT BOARD'S BAUD RATES AND INTERVAL TIMES

	Minimum values	Maximum values
Baud generator	18.75 bauds	64 kilobauds (limited by 8251A)
Single timer	1.63 $\mu$ s	428 ms
Dual cascaded timers	3.26 $\mu$ s	7.8 h

TABLE 2: iSBX 351 ADDRESS ASSIGNMENTS

Universal synchronous/asynchronous receiver-transmitter	data port control port	F0, F2, F4, or F6 F1, F3, F5, or F7
Timer	counter 0	F8 or FC
	counter 1	F9 or FD
	counter 2	FA or FE
	control port	FB or FF

TABLE 3: SERIAL INPUT/OUTPUT ROUTINES

INT:	MVI OUT MVI OUT MVI OUT MVI OUT RET	A, 96 0FB A, 8 0FA A, 0FE 0F1 A, 27 0F1	Mode word to 8253 counter 2 Divide value to 8253 counter 2 Mode word to 8251A Usart Command word to 8251A
XMIT:	IN ANI JZ MOV OUT RET	0F1 01 XMIT A, C 0FO	Check Usart status to make sure it's ready to transmit a character Loop until ready Get data character Send it
RECV:	IN ANI JZ IN ANI JNZ IN RET	0F1 02 RECV 0F1 38 ERROR 0FO	Check Usart status to see if a new character has been received Loop until data is available Check framing, overrun, and parity error bits Jump to an error handler if there are any problems Get data

The iSBX 350 module supports all three 8255A modes: basic I/O, strobed I/O, and strobed bidirectional bus I/O. Several of the handshaking signals are available as interrupt sources, and an additional external interrupt may be brought in via the edge connector.

Programming this board is as simple as programming the 8255As on the iSBX 80/10B itself. First, a mode word is written to the control port to specify the operational mode for each port. Data transfer may then begin, in the form of I/O-read or -write operations.

The iSBX 332 module is an accurate 32- or 64-bit floating-point processor that performs arithmetic operations in accordance with the proposed IEEE floating-point standard. It uses the 8232 floating-point processor.

The math module uses one data format that has two word lengths of 32 or 64 bits. The board will add, subtract, multiply, and divide for both word lengths.

TABLE 4: COMMAND MNEMONICS OF iSBX 332 FLOATING-POINT MATH MULTIMODULE

Command type	Mnemonic	Command description <sup>1</sup>
32-bit	SADD	Add TOS to NOS. Result to NOS. Pop stack.
32-bit	SSUB	Subtract TOS from NOS. Result to NOS. Pop stack
32-bit	SMUL	Multiply NOS by TOS. Result to NOS. Pop stack.
32-bit	SDIV	Divide NOS by TOS. Result to NOS. Pop stack
64-bit	DADD	Add TOS to NOS. Result to NOS. Pop stack.
64-bit	DSUB	Subtract TOS from NOS. Result to NOS. Pop stack.
64-bit	DMUL	Multiply NOS by TOS. Result to NOS. Pop stack.
64-bit	DDIV	Divide NOS by TOS. Result to NOS. Pop stack.
—	CLR	Clear status register.
32-bit	CHSS	Change sign of single-precision operand on TOS.
64-bit	CHSD	Change sign of double-precision operand on TOS.
32-bit	PTOS	Push single-precision operand on TOS to NOS.
64-bit	PTOD	Push double-precision operand on TOS to NOS.
32-bit	POPS	Pop single-precision operand from TOS. NOS becomes TOS.
64-bit	POPD	Pop double-precision operand from TOS. NOS becomes TOS.
32-bit	XCHS	Exchange single-precision operands TOS and NOS.

1. abbreviations: NOS = next on stack, TOS = top of stack

Table 4 shows the instruction mnemonics and functions, as well as the positions in the stack (top of stack or next on stack) the operands and results occupy.

The 8232 runs at 4 MHz for maximum throughput. A multiplication of two 32-bit quantities takes about 50 microseconds, excluding data entry and retrieval. In addition, two interrupts signal the base-board processor of completion of an operation or an error.

#### Floating-point math

The two word lengths of the floating-point standard were chosen for the highest speed and accuracy. If speed is the primary objective, the 32-bit format gives a dynamic range of approximately  $10^{-38}$  to  $10^{+38}$ . If range and accuracy are required, the 64-bit format spans in excess of  $10^{+300}$  to  $10^{-300}$ . This wide dynamic range, in conjunction with highly accurate rounding algorithms, renders the iSBX 332 module ideal for scientific problems and other applications requiring high speed, accuracy, and range. □

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## Tricked interrupts speed processor's data transfer

by G. Rodriguez-Izquierdo

*Department of Electronics, University of Santiago, Spain*

Programs that transfer data to the memory of a microprocessor-based system first wait for a ready command from the external device to which the data is sent, then transfer the data, and finally check that the transfer is completed before exiting from the loop. This process is often unnecessarily time-consuming. As shown here, the time required to complete the wait phase of the routine may be reduced by synchronizing the external device to the system. A second improvement reduces the number of instructions in the re-enter loop by eliminating the check stage through simulated or "tricked" interrupts, and performing the check with hardware.

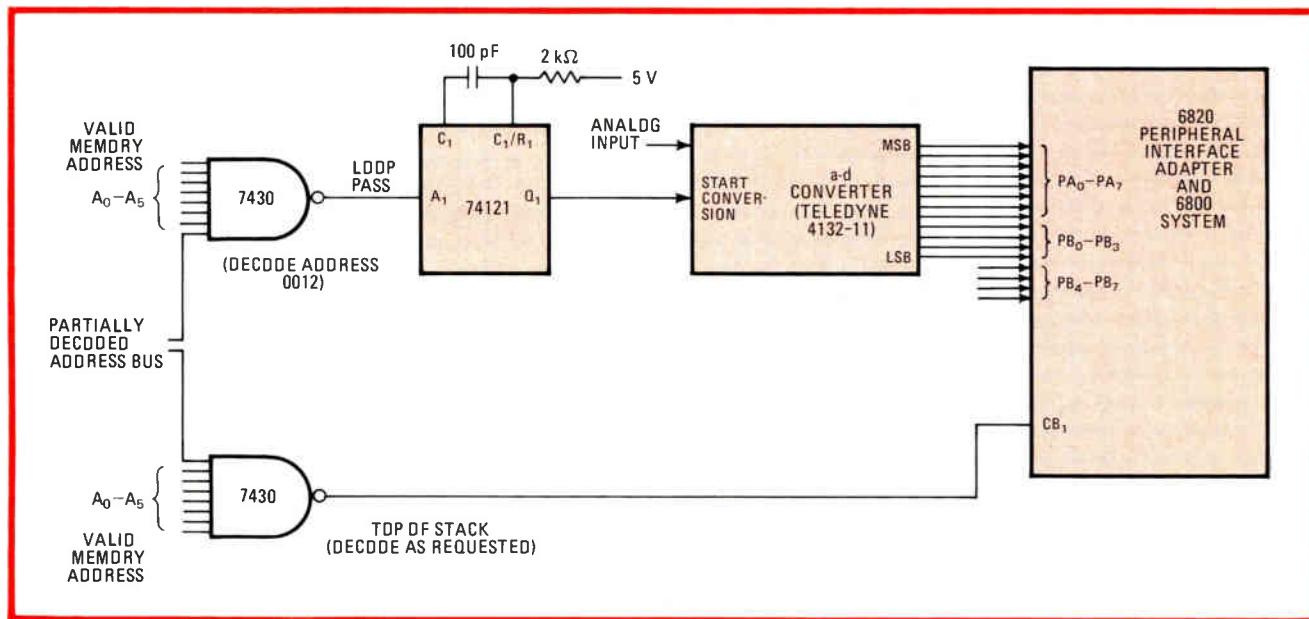
To illustrate the technique, the required interface is shown with a program that transfers a number of data samples from a fast 12-bit analog-to-digital converter—the Teledyne 4132-11, which has a 2-microsecond cycle time—to a 6800 microprocessor system, which has a 1- $\mu$ s cycle time. Data transfers and interrupts are transmitted through the 6820 peripheral interface adapter for handling one sample every 19  $\mu$ s. Two 7430 AND gates decode the address bus (which is assumed to have been partially decoded previously) jointly with the valid-memory address lines,  $A_0-LA_5$ . The first decoder detects

the occurrence of address 0012<sub>16</sub>, which corresponds to one of the instructions in the program loop. The second decoder serves as a top-of-stack detector.

After system initialization, the program enters the read-data loop. As the system goes through address 0012 on each pass, the first decoder delivers a pulse which initiates a new conversion cycle. Meanwhile, the microprocessor executes the PSHA and JMP instructions. The time required to execute these instructions is seven machine cycles, and this period is greater than the converter's settling time. In this way, data is ready when requested by the LDA A instruction, and no wait interval is required.

As for saving the time normally required to perform a check, note the program reenters the loop with the instruction JMP. This operation is faster than any using the branch instructions contained in the 6800 system. The system thus reenters the loop unconditionally, and it therefore saves at least three microprocessor cycles (3  $\mu$ s per cycle) that would otherwise be required to verify a data transfer.

At the same time, detection of the read-loop exit condition is done by the top-of-stack decoder, which causes an interrupt when the specified number of samples has been transferred into the stack. Normally, after servicing an interrupt, a program returns to the address where the interrupt originated and then returns to the read loop. The interrupt routine shown prevents this by changing the return address corresponding to the interrupt return location in the stack when the interrupt first occurs. Thus, after returning from an interrupt, the processor may be diverted at once to another task. □



**Quickly.** Interface activates a-d converter synchronously through decoder on each program read cycle in order that 4132-11 may transfer one data sample to the peripheral interface adapter (PIA) without need for a data-ready command. Top-of-stack detector, in conjunction with program, terminates transfer quickly by issuing an interrupt that simulates data-block transfer acknowledgment by PIA.

## 6800 PROGRAM: FAST DATA TRANSFER

Location	Label	Op code	Operand	Comments
0000	LOOP	LDA A	04H	Initialize PIA
0002		STA A	PIACRA	
0005		STA A	PIACRB	
0008		LDS	STACKP	Initialize stack
000B		LDA A	PIADA	Read least significant byte (8 bits)
000E		PSH A		
000F		LDA A	PIADB	Read most significant byte (4 bits)
0012		PSH A		Pulse is generated to start a-d cycle
0013		JMP	LOOP	
INTERRUPT ROUTINE				
00A0		STS	MEM	Load stack pointer in index register
00A2		LDK	MEM	
00A4		CLR A		Change most significant byte of return address
00A5		STA A	5, X	
00A7		LDA A	COH	Change least significant byte of return address
00A9		STA A	6, X	
00AB		LDA A	PIADB	Clear interrupt
00AE		RTI		Go to address 00C0

**Calculator notes****Bucket curve program speeds noise-figure analysis**

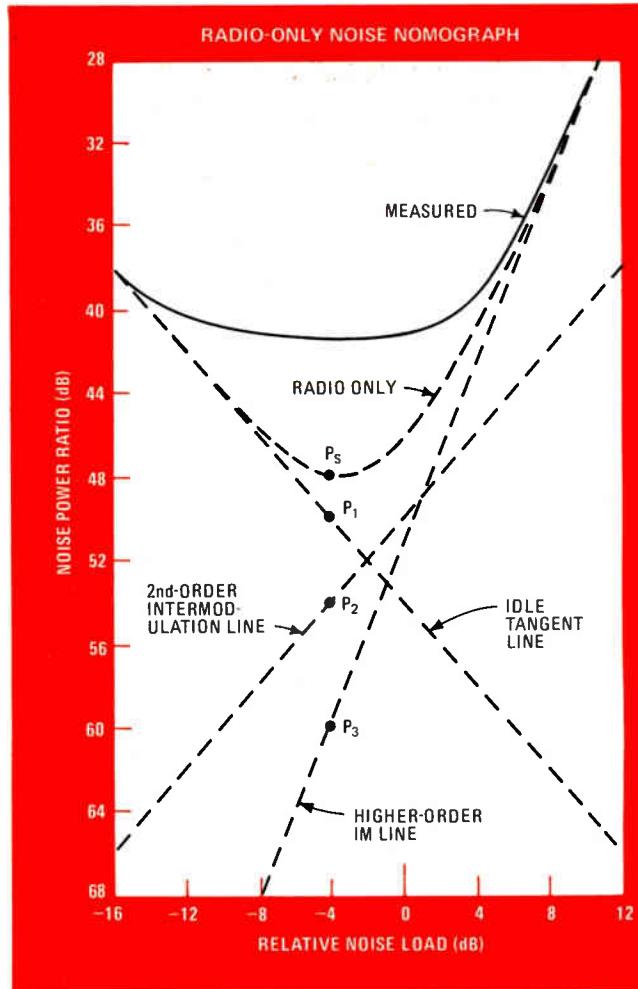
by M. Fraser

Department of Transport, Brisbane, Australia

Plotting a microwave system's noise-power-ratio (NPR), or bucket, curve to relate the individual components of system noise—tangential idle, intermodulation, and echo—is a tedious task. The graphical procedure, needed to identify the noise generated by the receiving equipment from that present in the receiving path, thus helping the designer locate noise sources and optimize system performance, may be eliminated entirely with this HP-25 program. With it, information on the type and amplitude of noise may be secured in minutes, rather than the hours normally required.

As shown in the graphical approach (see nomograph) once the high- and low-slot white-noise measurements have been made and the NPR curve plotted according to the standard procedure,<sup>1</sup> the tangential idle ( $T_n$ ) line and the intermodulation ( $I_n$ ) lines are drawn. These three lines are then summed to produce the so-called radio-only curve, which gives the noise characteristics of the stand-alone receiving equipment.

Inconsistencies between the NPR curve and the radio-only curve are the result of echo distortion due either to mismatches in the receiving equipment system or to radio path anomalies. The shape of the echo curve, which provides clues to the source of the echo, is found by determining the logarithmic difference between the



radio-only and NPR curves (see second chart).

The aforementioned procedure is easily performed by the calculator so that the radio-echo and echo-distortion noise figures can be found for spot values of  $T_n$  and  $I_n$ . Given the measured or calculated values of the tangential idle noise figure and the noise components created by intermodulation, the program finds the noise figure of the receiving equipment for a given relative noise load from iterative application of the equation:

$$P_s = P_i - 10 \log(1 + \log^{-1}[(P_i - P_{i+1})/10]) = P_i'$$

where  $P_i = P_1$  = tangential idle noise in decibels,  $P_{i+1} = P_2$  = second order intermodulation component in decibels, and where  $P_{i+2}$  would equal  $P_3$  = high-order intermodulation value in decibels.

Having  $P_s$ , the program then finds the system's echo distortion from:

$$P_d = P_m - 10 \log(1 - \log^{-1}[(P_m - P_s)/10])$$

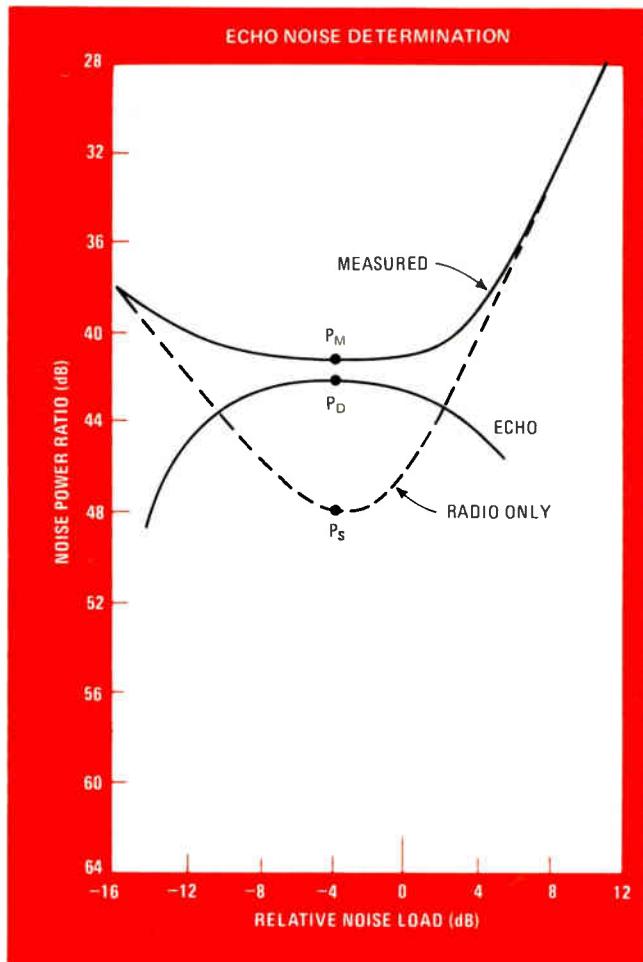
where  $P_m$  is the total (system) measured noise (NPR) value. The method for finding  $P_1$  and  $P_2$  are described in the mentioned Lenkurt note.

As a check on the program, consider the case where  $P_1 = 50$  dB,  $P_2 = 53.5$  dB, and  $P_3 = 59.5$  dB for a relative noise load of -4 dB. Entering these values into the program as instructed yields  $P_s = 48.07$  dB and  $P_d = 41.95$  dB.  $\square$

#### References

1. "Bucket Curves," GTE Lenkurt Demodulator, March and April 1976.

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay \$50 for each item published.



#### HP-25 PROGRAM: BUCKET-CURVE ANALYSIS

Line	Code	Key
01	24 00	RCL 0
02	24 01	RCL 1
03	41	-
04	01	1
05	00	0
06	71	$\div$
07	15 08	$g 10^x$
08*	15 74	$g$ NOP
09	01	1
10	51	+
11	08	f log
12	01	1
13	00	0
14	61	$\times$
15	32	CHS
16	24 00	RCL 0
17	51	+
18	23 00	STO 0
19	24 02	RCL 2
20	23 01	STO 1
21	24 03	RCL 3
22	23 02	STO 2
23	24 01	RCL 1
24	15 61	$g x \neq 0$
25	13 01	GTO 01
26	24 00	RCL 0

\*CHS, to find  $P_d$

Registers	
$R_0$	$P_1$
$R_1$	$P_2$
$R_2$	$P_3$

#### Instructions

- Key in program
- Specify noise figures corresponding to tangential idle noise and components due to intermodulation so that magnitude of noise generated in communications equipment can be determined:  
 $(P_1)$ , STO 0,  $(P_2)$ , STO 1,  $(P_3)$ , STO 2, f PRGM R/S  
 $P_s$  (dB) is displayed
- To find echo distortion, replace NOP instruction at location 8 with CHS, key in noise figures corresponding to measured system noise and radio-only value:  
 $(P_m)$ , STO 0,  $(P_s)$ , STO 1, f PRGM R/S  
 $P_d$  (dB) is displayed

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Material: ABS Plastic Dimensions: 297W x 210H x 7T mm

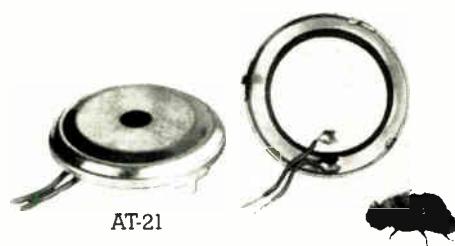
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## **IEPS holds workshop on power hybrids**

Thick-film power hybrids are rarely covered in any book or trade journal, but the International Electronics Packaging Society will present a workshop on the subject at the New York Coliseum on June 16. Addressing the design and manufacture of power hybrids for switching power supplies, the one-day session's topics will include hybrid design using discrete components, hybrid manufacturability, a survey of thermal-analysis techniques, and automatic laser trimming. A discussion of the availability of power hybrids in the marketplace is also on the agenda, as is one on military procurement of power supplies. For additional information, call Steve Konsowski, (301) 765-2191, or Robert Newton, (301) 765-2203.

## **Division of Heath bent on selling self-study materials**

The Heath Co., purveyor for years of those do-it-yourself electronic kits, is capitalizing on its teaching expertise by offering a range of self-study courses that may be purchased individually or in quantity for company training programs. The Benton Harbor, Mich., firm has elevated its educational efforts to full division status and now offers more than 20 courses.

Each course consists of text material, programmed instruction sequences, audio-visual aids, self-checking quizzes, and hands-on experiments. None is priced over \$100 and most are under \$50. Subjects range from operational amplifiers and digital techniques to programming in the high-level language of Basic. The advanced electronics courses can be bought directly from Heath/Zenith Educational Systems, Benton Harbor, Mich. 49022. Call (616) 982-3411.

## **Laser Institute conducts scattered lightwave seminars**

Numerous locations throughout the country will witness the Laser Institute of America's efforts to keep engineers and scientists abreast of the laser art this spring and summer. The series of week-long seminars begins with "Laser Radiometry and Beam Diagnostics," to be held May 5-9 at the National Bureau of Standards, Boulder, Colo. The topics include temporal and spatial characteristics of lasers, measurement techniques, and measurement equipment. "Laser Optics," scheduled for May 19-23 at the LaFonda Hotel, Santa Fe, N. M., addresses principles of geometric and wave optics.

"Modern Optics for Scientists and Engineers," at The Lodge, Vail, Colo., during the week of June 9, delves into new developments and techniques in optics, including beam propagation, information processing, detection and recording, and nonlinear phenomena; it is followed by "High Power Lasers," June 16-20, at the Holiday Inn in Vail.

"Laser Safety" is examined July 7-11 at the Quality Inn in Washington, D. C., and the "Fundamentals and Applications of Lasers" will be taught at the Ramada Inn in Montreal, July 21-25. Back again at The Lodge in Vail, "Adaptive Optics and Phase Conjugation Methods," which includes optical imaging and isotope separation among its topics, will be given Aug. 4-8. The road show winds up at the LaFonda Hotel in Santa Fe, with a seminar on "Carbon Dioxide Lasers" Aug. 18-22.

Each course carries a fee of \$550. For more information, contact the Short Course Director, Laser Institute of America, P. O. Box 9000, Waco, Texas 76710.

-Vincent Biancomano

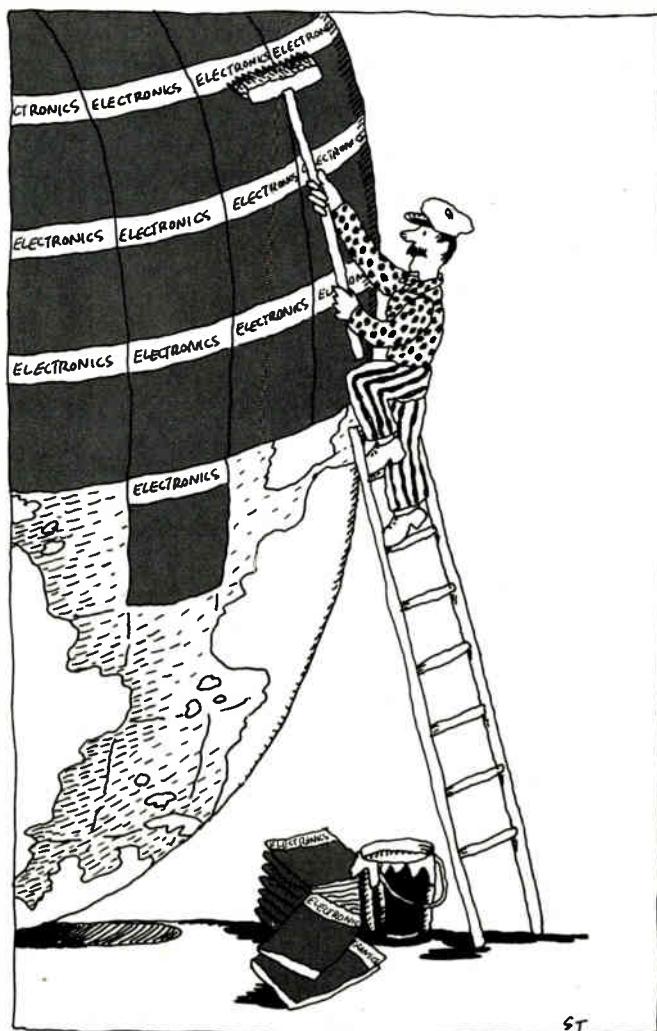
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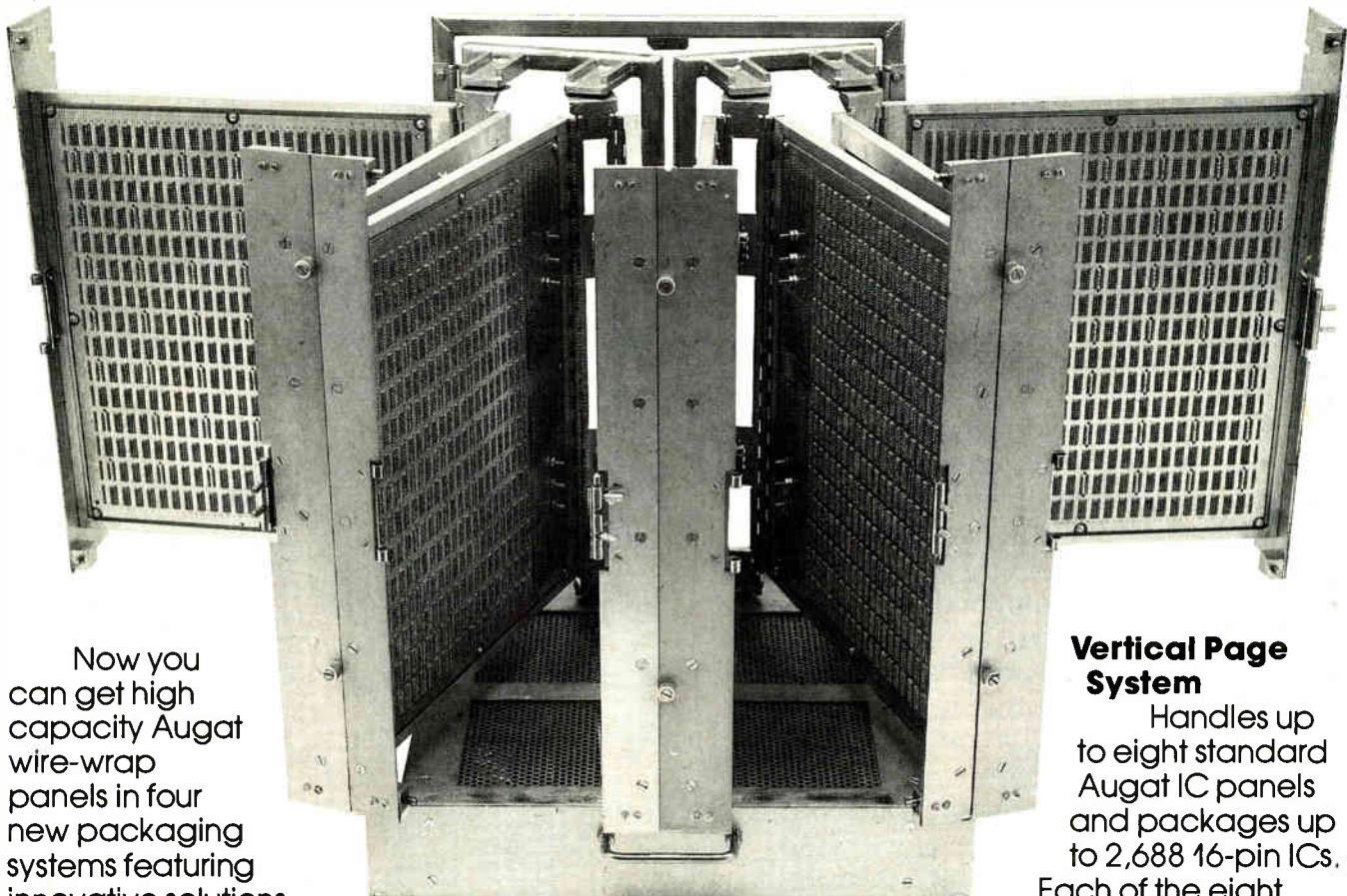
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# GET THE WHOLE PACKAGE FROM AUGAT.



Now you can get high capacity Augat wire-wrap panels in four new packaging systems featuring innovative solutions to your design problem.

The "whole package" approach reduces total system design time because Augat has already engineered your packaging. And, you can utilize the same "off-the-shelf" system for both prototyping and production. Quick, easy access to each panel simplifies testing, repair and modification. These new packaging systems are designed in accordance

with RETMA spacing and fit into standard 19" cabinets.

Augat packaging systems are ideal for applications in digital data processing, process control, aerospace ground control... almost any application where it is essential to move quickly from schematic to finished product.

## Vertical Page System

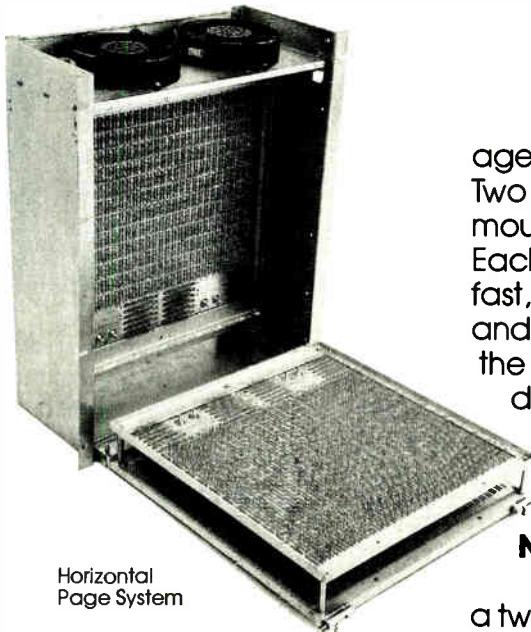
Handles up to eight standard Augat IC panels and packages up to 2,688 16-pin ICs.

Each of the eight pages opens quickly for easy access.

Cabling is located at the pivot point of each page allowing unrestricted air flow. Provisions in the chassis allow the user to strain relief the cables to prevent flexing. Heavy-duty slides are standard. Optional fan and filter are available.

## Horizontal Card Cage

This flexible system lets you combine analog and digital; wire-wrap and



Horizontal  
Page System

stitch-weld; and single, double and triple width boards in the same enclosure.

Choose either a continuous backplane or three separate backplanes to provide the different voltages and grounds needed to mix analog and digital boards. All are assembled with 96-pin I/O connectors. Flexible spacing lets you use up to four wire-wrap boards (.12" spacing) or 7 stitch-weld boards (.6" spacing) or a combination of the two. Guide separators let you mix different width boards. Fans are optional.

### Horizontal Page System

Handles up to four Augat panels and pack-

ages up to 1,560 16-pin ICs. Two systems can be mounted back-to-back. Each page folds down for fast, easy troubleshooting and IC replacement. And, the whole system was designed to make cabling easy. Two top-mounted fans are optional.

### New Drawer Systems

Available in two sizes... a two-board and a three-board version. Each board packages up to 390 ICs; both feature a standard rear-mounted back plane for easy cabling between boards or other systems. Cabling in rear allows unrestricted air flow. Optional slides are offered for easy accessibility. Four fans with filter are available for cooling. Terminal block is provided for DC power entry.

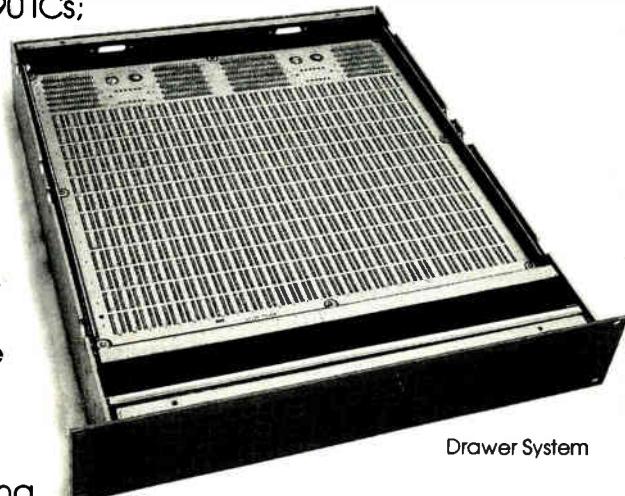
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Designed specifically for our vertical page, horizontal page, and drawer systems and provide maximum I/O to IC ratio. ICs are oriented to provide maximum cooling efficiency. Augat boards feature 24, 40-pin feed-thru I/O fields, DC power entry

at two locations and provisions nearby for installing both tantalum and disc capacitors.

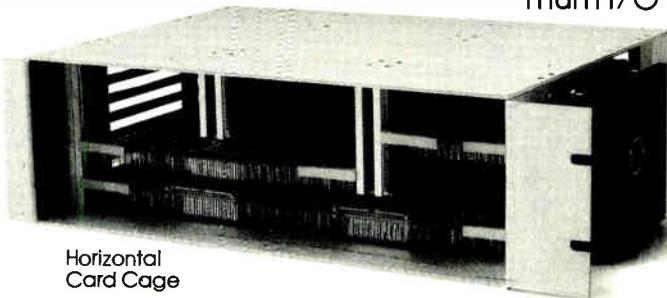
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Horizontal  
Card Cage

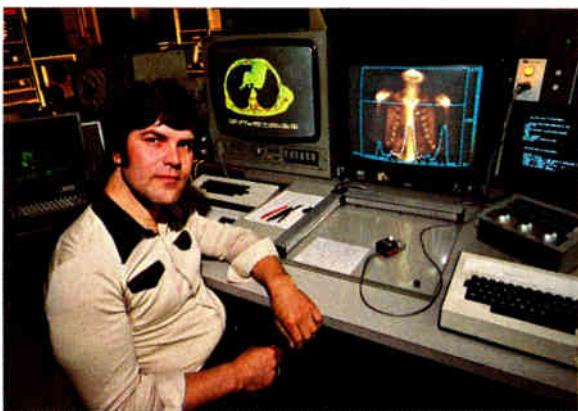
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# Real-Time on VAX. Ask any user.

**"With our intensive real-time demands, VAX is clearly the machine for the job."**

*Willfried Muller, VAX System Manager  
Institute of Nuclear Medicine  
German Cancer Research Center  
Heidelberg, Germany*



The Institute for Nuclear Medicine at the German Cancer Research Center uses gamma cameras, ultrasonic scanners and X-ray computer tomography for the detection of tumors. These processed medical images are also used as input data for surgery and radiation therapy treatment planning.

For these applications, the Institute needed a powerful computer.

Willfried Muller, VAX System Manager, tells why they decided on Digital's VAX-11/780: "We needed a machine that would not only process images quickly, but also help us develop new programs for our applications. In both areas, VAX seemed to be ideal."

VAX's accessibility was also critical: "Our user community includes many different types of people. The fact that VAX is interactive and easy to use is very important to us.

"Also," Muller continues, "our image processing work made VAX's large program

capacity very attractive. It can hold several big matrixes simultaneously. Equally important, VAX can be expanded to meet our requirements for years to come."

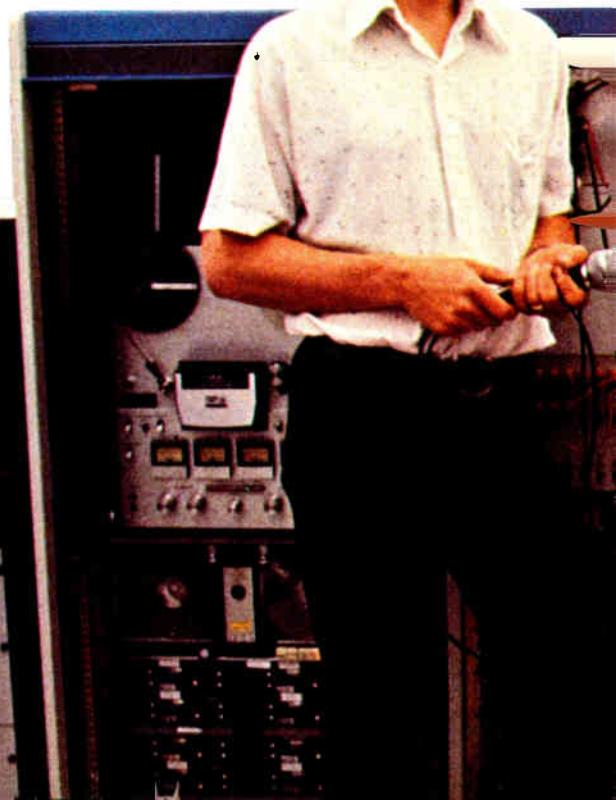
On ease of program conversion, Muller says, "We're finding it as simple as Digital promised."

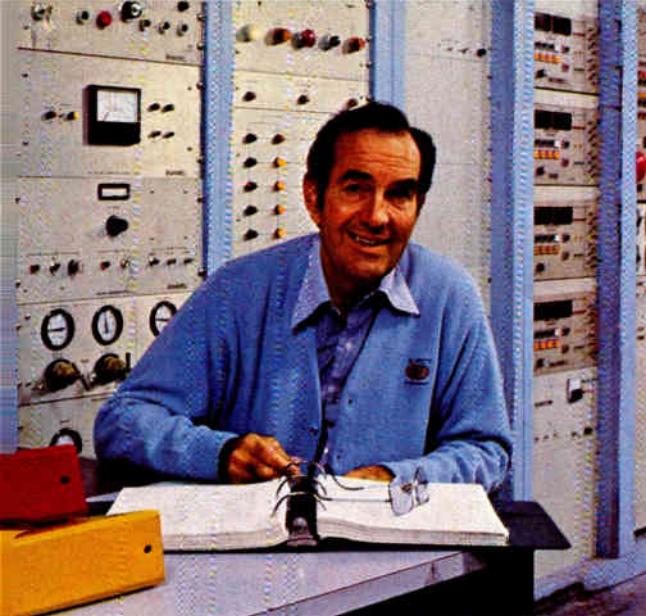
And according to Muller, VAX's price/performance ratio has proved "very favorable."

Concludes Muller, "We don't know of another machine anywhere that could handle the job as well as VAX."

**"VAX's real-time capabilities are even better than we expected."**

*Dr. Jim Larson, Technical Staff  
Electronics Research Center  
Rockwell International  
Anaheim, California*





Scientists at the Information Sciences Laboratory at Rockwell International Electronics Research Center are developing computer applications such as target-spotting identification and tracking, image enhancement, and speech processing.

For such state-of-the-art research they needed a state-of-the-art computer. They chose Digital's VAX-11/780.

According to Dr. Jim Larson, member of the technical staff at Rockwell International, "VAX gives us great real-time response. With our old mainframe computer, we had to suspend all of our other user processes during real-time digitization. But VAX's FORTRAN is a lot more powerful. On VAX you never even know when something is being digitized."

The fact that VAX is able to handle real-time and interactive analysis simultaneously is a feature that's especially attractive. Says Larson, "Our people only have to learn and use one computer."

## "VAX's large address capacity makes it a powerful real-time machine."

*Dr. William E. Drummond, Chairman  
Austin Research Associates  
Austin, Texas*

At Austin Research Associates in Austin, Texas, plasma physicists are using VAX to conduct far-ranging scientific research on the collective acceleration of sub-atomic particles.

"We chose VAX because it provided the ability to directly address very large data arrays. And that is crucial to each of our applications," explains Dr. Drummond, Chairman at Austin Research.

"VAX has the capacity to acquire data simultaneously from 15 different experimental sensors, digitize it, and immediately present results to our researchers. And furthermore," Drummond adds, "VAX gives us a perspective we never had before by rapidly providing data comparisons with thousands of earlier test results."

"In addition, while VAX is supporting several interactive users it can also handle our large number-crunching simulation programs, allowing us to off-load a CDC mainframe," says Drummond.

Digital's VAX-11/780 has redefined the level of performance you can expect from computers in its price range.

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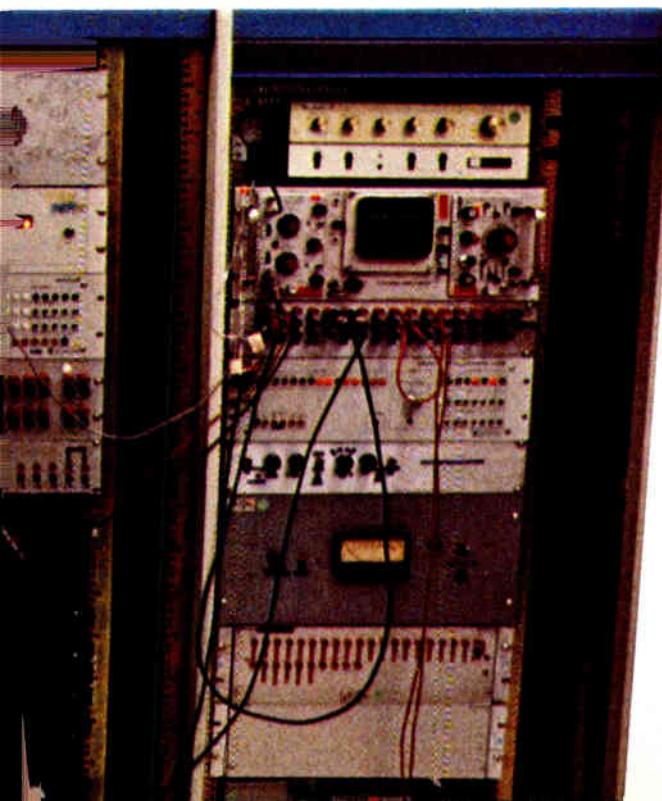
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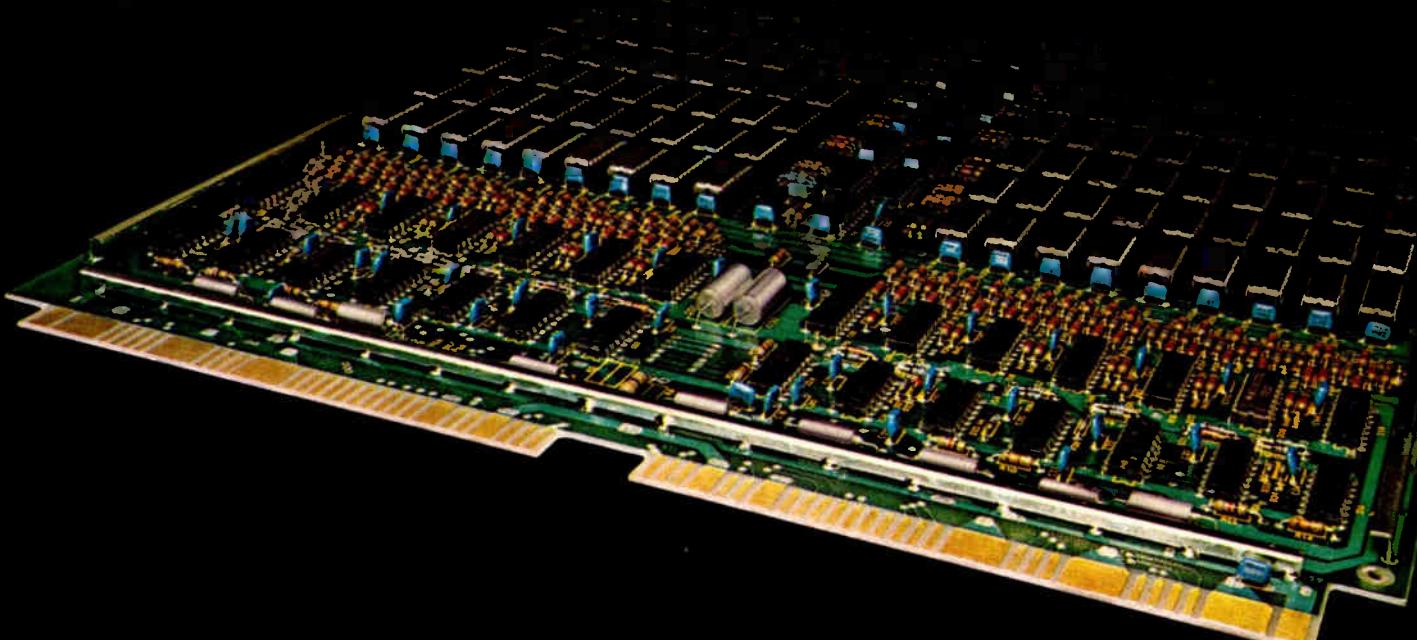
As a result, these conditions favor the use of MLC's in place of tantalum capacitors for the full range of decoupling needs.

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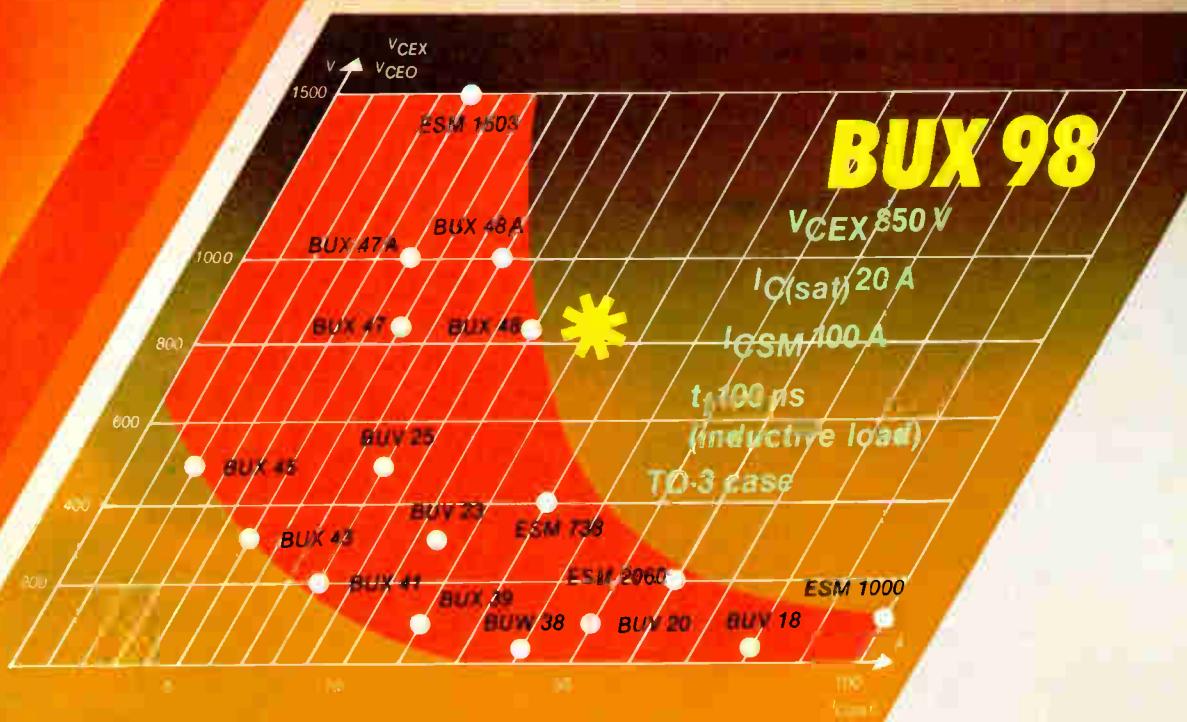


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# NEC enters U. S. fiber optics market

Starting with three products that are new even in Japan, Nippon Electric will begin selling its fiber-optic components directly within the U. S.

by Ana L. Bishop, Assistant New Products Editor

**Japan's Nippon Electric Co.** is finally going to sell its fiber-optic components directly within the U. S. Among the many products the Tokyo-based company will be selling here through its U. S. subsidiary, NEC Electron, are components just recently introduced in Japan: an optical directional coupler, a step optical attenuator, and an optical-fiber terminating kit.

"The growth of the fiber optics industry in America has reached

such dramatic proportions that to keep up with demand we just had to start distributing from within the continental U. S.," says Norio Kurochi, engineering manager for fiber-optic communications development in Tokyo.

One of the new products to be sold here is the OD-8501 step optical attenuator. The unit has four cells that come with attenuations of 0, 3, 7, and 17 dB and can be combined in groups of any three for maximum

values of  $3.0 \pm 0.5$  to  $20.0 \pm 1.0$  dB.

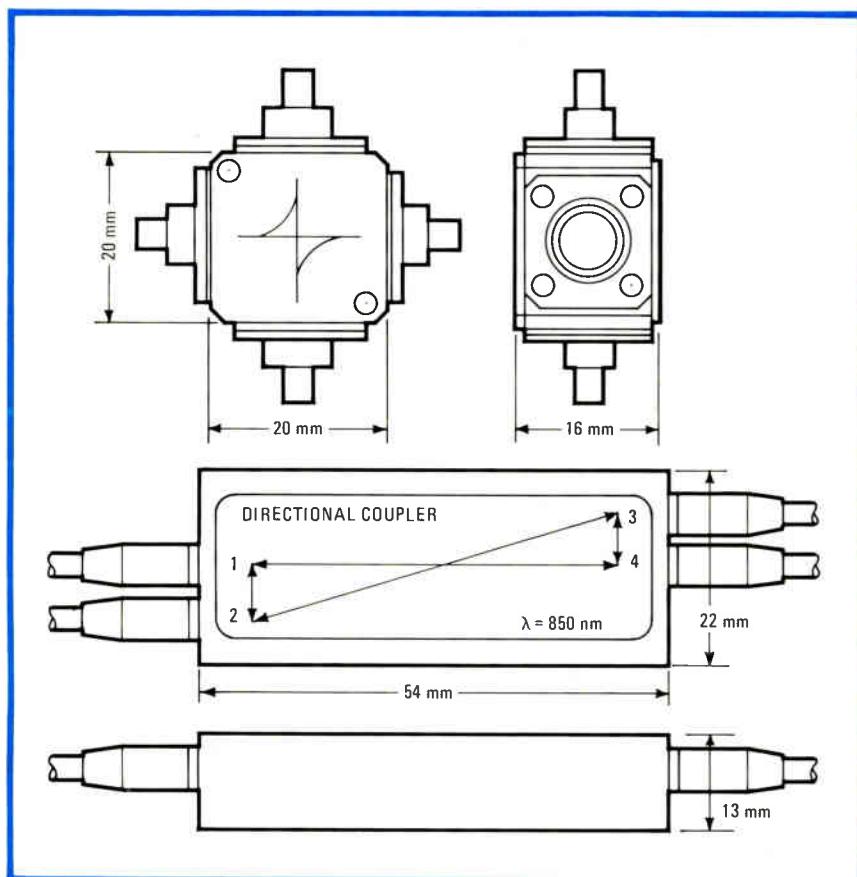
The attenuators are specified to have bidirectionality and accuracy of 0.5 dB or less and come with their own D-4-type optical connectors. They can be used for 800-to-900-nm-wavelength light with optical fibers of the step- and graded-index types.

**Coupler.** An optical directional coupler comes in three versions: models OD-8601 and OD-8602 have three and four receptacles, respectively; models OD-8603 and OD-8604 have four and three pigtails, respectively.

Each of the four couplers has three different splitting ratios. Type A couplers have a splitting ratio of 1:1, type B's ratio is 10:1, and type C couplers have a splitting ratio of 100:1. The accuracy of type A units is to within  $\pm 0.5$  dB; it is to within  $\pm 1$  dB in type B couplers and to within  $\pm 2$  dB in type Cs. The insertion loss for the models is less than 2 dB. The isolation ranges from 13 to about 40 dB, depending on the model. In quantities of 10 or more, the couplers sell for \$506 to \$630 apiece. Single units sell for \$565 to \$707.

For terminating optical fibers in the field or laboratory, NEC has the OD-9500 kit, which consists of connector parts, a lapping tool, an assembling tool, and resin. The kit's connection loss is 1 dB or less. The kit, which terminates glass-clad fibers with  $125 \pm 2\text{-}\mu\text{m}$  or  $150 \pm 2\text{-}\mu\text{m}$  outside diameters, will sell for \$800.

NEC will also offer its entire line of optical devices, described in the company's new comprehensive catalog. NEC Electron Inc., 3120 Central Expressway, Santa Clara, Calif. 95051 Phone [339]



**Compact.** The compact optical directional coupler from NEC Electron comes in three versions—with three or four receptacles or three or four pigtails.



# Signal synthesizer sells for \$995

2-MHz digital source aimed at benchtop use spins out both sine and square waves with 1-Hz resolution

by Richard W. Comerford, Test, Measurement & Control Editor

**Anyone buying a general-purpose benchtop signal source has always had to make some undesirable trade-offs.** Simple oscillators sacrifice accurate tuning to ensure a low-distortion output, and function generators obtain higher accuracy at the cost of sine-wave distortion.

But Comstron Corp. plans to end that situation with a no-tradeoff signal source that is completely digital. Called the model 1002 precision signal source, it is a 2-MHz synthesized-signal generator—a practical bench tool that sells for only \$995.

The generator can put out both sine and square waves whose frequency can be read to a resolution of 1 Hz from a 6½-digit light-emitting-diode display. With frequencies that are accurate to within 1 ppm, the 1002 produces sine waves whose harmonics are suppressed by 60 dB below 100 kHz and 50 dB above;

spurious frequencies are 55 dB down below 5 kHz and 60 dB down above 5 kHz. Phase noise, or jitter, is suppressed 50 dB for a 30-kHz band centered at 1 MHz (excluding 1 Hz on either side) at full output. Square waves, produced by clipping, are symmetrical to within  $\pm 5\%$ , have rise and fall times of under 3 ns, and have a fixed amplitude of 2 V into a 50- $\Omega$  load.

Two aspects of the design allowed the firm to keep the unit's price low, according to Len Borow, executive vice president. "One is Comstron's patented, direct-programmed differential synthesis technique," says Borow, "and the other is the sine-wave amplitude setting technique."

The differential synthesis technique mixes the outputs of two phase-locked loops to produce the final frequency. Both the main and vernier PLLs—which set the gross

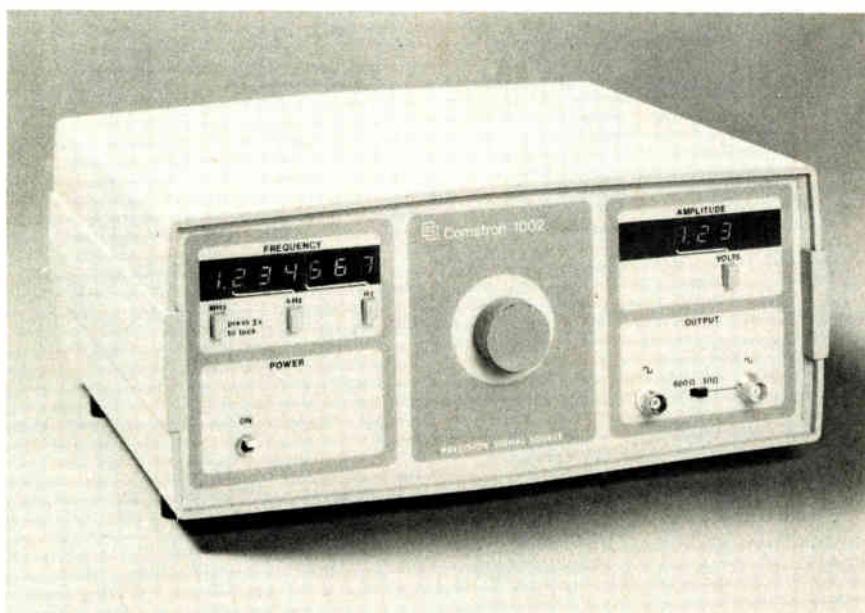
and fine components of the frequency, respectively—have an N multiplier directly programmed using a binary-coded decimal number.

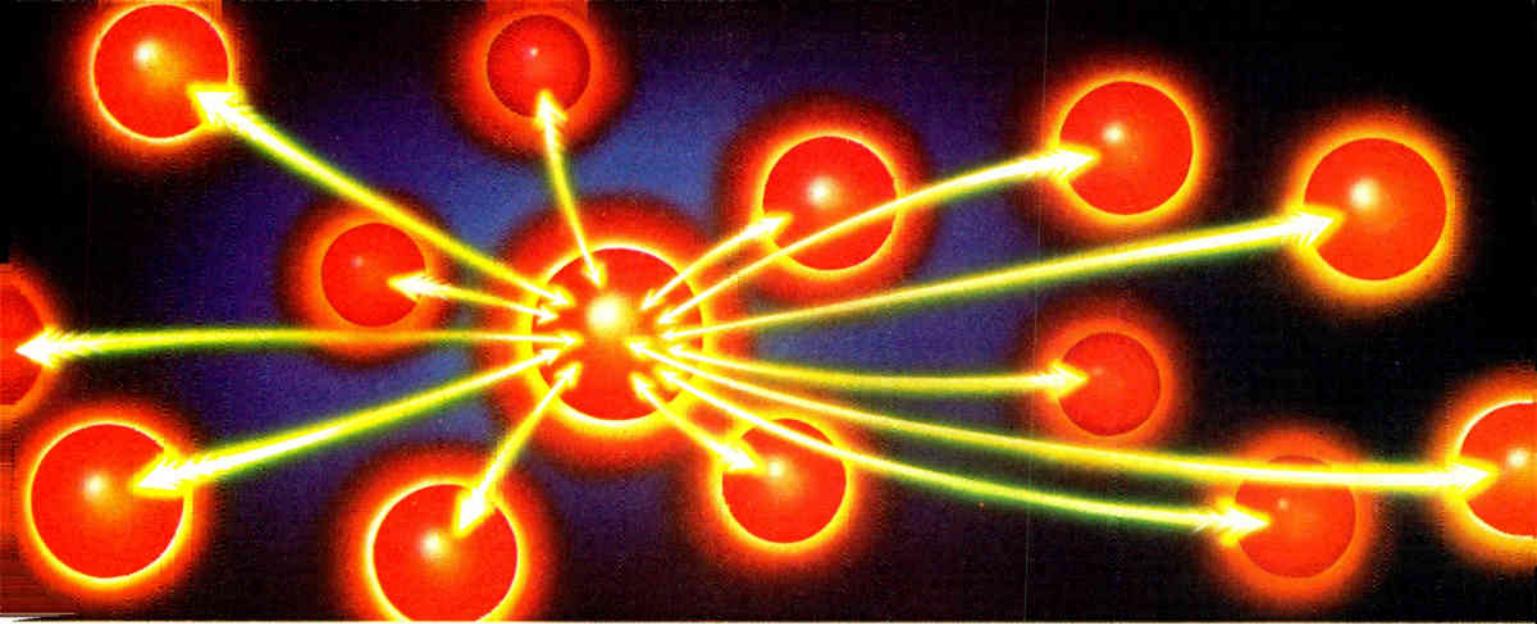
The BCD number is obtained from a spinwheel tuner that operates much like an optical shaft-angle encoder. Comstron eliminated a lot of analog circuitry and simplified operation by using the same tuner to set sine-wave amplitude.

For amplitude, the BCD counter output is used to address a read-only memory directly. The ROM contains a lookup table of settings for a digitally programmable attenuator at the output and an amplifier between the vernier PLL and the mixer. For the amplifier, a digital-to-analog converter is needed to change the stored setting to an analog control voltage, but the use of two devices to fix the final output level optimizes precision, Barow notes. The end result is that amplitude is easily set in 10-mV root-mean-square steps up to 1.99 V for a switch-selectable output to a 50- or 600- $\Omega$  load. Read from a separate 2½-digit display, it is accurate to within  $\pm 2\%$ .

Completely setting up the 1002, then, is simply a matter of pressing a few keys and spinning the dial. Pushing one of the keys twice locks the setting, a nice feature on a busy bench. The source, which will be on display at next month's Electro/80, comes with a crystal time base stable to within 5 ppm per year; a more precise, 1-ppm/yr crystal is optional. Also offered optionally is a \$495 IEEE-488 interface. Delivery in the U.S. takes 30 days.

Comstron Corp., 200 East Sunrise Highway, Freeport, N.Y. 11520. Phone (516) 546-9700 [340].





# Managing to cover all bases.

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## The knowledge business



## New products

### Microcomputers & systems

## Development systems thrive

Three entries supporting 8-, 16-bit processors offer more memory and languages

Almost every week brings forth new tools for more efficient development of software to run on microprocessor-based products. The latest period brings to market three such systems, each presenting a different approach to the problem.

E-H International Inc., entering this market with a minicomputer-based system, sees the use of stand-alone emulation as key to future product design. Intel Corp., on the other hand, is moving to a 4-MHz processor to increase code-generating efficiency of its development system family by 50%. And Texas Instruments Inc. is taking yet a third tack, offering a system to prompt third-party development of software for its home computer, the 99/4.

Following on the heels of the lower-cost version of the Hewlett-Pack-

ard 64000 logic development system announced last month [*Electronics*, March 13, p. 166] is the E-H Micro-Support development system, which includes a stand-alone emulator in its \$22,000 package. The terminal-sized system has a keyboard, a cathode-ray-tube display, a minicomputer, a 10-megabyte 8-in. Winchester disk and controller, and 0.5 to 1 megabyte of backup floppy-diskette storage.

**Flexible.** Its primary language is Pascal, but the system can be programmed with Fortran, and assembly language and Pascal can be mixed to fine-tune the program. The system's cross-assembly capabilities allow it to develop programs for virtually any of today's microprocessors, limited only by its companion stand-alone emulator, the Micro-Support model 800 [*Electronics*, March 13, p. 168]. The model 800 can currently support the Z80, the 8080, or the 8085 and by October will be able to support the 8086 and Z8000 as well.

The system's minicomputer uses bit-slice logic to assemble 1,000 lines of instructions in 4 s. It has 32 K by 16 bits of random-access memory, which, with a 125-ns cycle time, is four times faster than the Shugart SA1004 Winchester disk the system

also employs. The back end is configured as a 12-slot Multibus.

The U.S. price of \$22,000 is comparable to HP's base price of \$18,500 plus \$4,800 extra for an emulator and 16 kilobytes of emulator memory. "We build nearly everything from the ground up," E-H president Joseph McDowell notes, adding that the Xebec operating system used on the minicomputer has been field-proven over eight years.

This year, E-H will also give users the options of going to a higher-capacity 8-in. disk (about 20 megabytes), as well as to multiterminal, multi-user applications.

"Whether we go up to eight terminals," explains McDowell, depends only on the bus speed and the amount of storage on the disk." To allow it to adapt to a wide variety of terminals, the system has software-selectable baud rates.

**Speed up.** Meanwhile, Intel's Intellec development system series, which has already been upgraded by the addition of a 5440-type cartridge disk [*Electronics*, Sept. 13, 1979, p. 41] and an 8-in. Winchester disk [Feb. 28, 1980, p. 222], now offers the 4-MHz 8085A-2 microprocessor in the model 225, rather than the 2.6-MHz 8080A-2 used in previous systems. The net result, according to Intellec series II product manager Chris Zing, is that "when combined with a model 740 hard-disk drive, the new unit offers about a 50% performance increase over the hard-disk model 240."

The model 225 uses the same wait states, one for a read and two for a write, as previous systems. In addition, it makes three functions accessible via the Multibus to an in-circuit emulation (ICE) module that was previously inaccessible. These functions include two 8259 local interrupt controllers, a programmable interval timer, and two channels for universal synchronous/asynchronous receiver-transmitters.

As a stand-alone unit, the 225 has a \$10,990 price tag that does not compare favorably with the \$8,990 tag of the model 220, but then the 225 has 64 kilobytes of RAM on the CPU board, whereas the 220 has only



## New products

32 kilobytes. This means that an extra 32-kilobyte RAM board is not necessary for ICE-86 applications. Thus, the three-board ICE-86, two-board disk controller, and CPU all can fit into the six slots available in the mainframe.

The 225 represents a \$600 savings for the designer who makes use of an 8086 and 8088 in a system when 64 kilobytes of memory, an ICE package, and either an additional floppy diskette (model 235, \$25,230 with software and ICE-86) or the cartridge disk (model 245, \$32,730 with software and ICE-86) would be required.

The basic model 225 also contains a single-sided, single-density 250-kilobyte floppy-disk drive that has been integrated into the console. The 220 does not have an integrated floppy drive. A simple switch of CPU boards upgrades current Intellec systems. The model 505 integrated processor card (\$2,990), containing the 8085A-2 processor and 64 kilobytes of RAM, can be ordered separately.

In an effort to ensure the widespread development of software that will be needed to drive hardware sales of its 16-bit 99/4 home computer, Texas Instruments has assembled a support package that includes a new development system.

**A broader base.** Using a TI hard-disk-based DS990/10 minicomputer as a host, the development system package includes software that allows third parties to develop 99/4 programs using TI's Graphic Programming Language (GPL). That ability is important, since GPL is necessary to fully exploit the 99/4's advanced color graphics and program capabilities.

The 99/4 itself supports Basic as a development language; programs written on the 99/4 can be housed on cassette tape, on minifloppy disk, or in semiconductor memory. But the structured GPL supported on the 990/10-based development system package is optimized to produce a significantly more compact code for color graphics implementation than can be obtained using Basic.

This compact GPL code cannot be placed on disk or cassette but can be

### Mini link for Intellec

With 16-bit architecture adding to their burden, developers of microcomputer-based systems would benefit from sharing a minicomputer or mainframe. Users of the Intellec development system will benefit this June, when Intel begins deliveries of its MDS-383 upload or download link. Consisting of interconnecting cabling and a single- or double-density diskette, the MDS-383 sells for around \$2,250. It connects any Intellec series II directly to any mainframe or minicomputer that uses bisynchronous communications.

This arrangement becomes beneficial when more than eight programmers are working on the same development project. The upload or download link allows their development systems to share a common file management system through the mainframe. "Now all programmers can be assured of working with the latest version of a program," notes Eric Michelman, an applications engineer at Intel. All the development systems systems can be accessed through the network of terminals connected to the mainframe.

To set up an Intellec system with MDS-383 a user must supply a 9,600-baud modem. Intellec 800 series users must in addition employ the iSBC-534, priced at \$750. **M. M.**

housed on the p-channel MOS read-only memories that are used in the 99/4's plug-in solid-state Command Program Modules. Thus the use of GPL enables much larger programs to be developed for the command modules, each of which has a maximum of 30 kilobytes of p-MOS ROM, plus an additional 8 bytes of faster, more expensive n-channel ROM.

The development system's configuration is designed to allow programs to be written on terminals attached to the 990/10, which also supports Basic and the 9900 assembly language, in addition to GPL. Once written, a program is downloaded into dynamic RAM housed in a box with appropriate interface circuitry for simulating a 99/4 ROM command module. With the simulator box cable plugged into the command-module socket, program debugging can be done using a specially modified 99/4 debugging station and making use of a software development aid that comes with the package. Interface circuitry and software for RS-232 communications between the 990/10 and the 99/4 debugging station are also included.

For buyers who already have a DS990/10 minicomputer, the 99/4 debugging station hardware and associated software sells for \$12,280, including a week-long training class at TI's Consumer Products group

operation in Lubbock, Texas, as well as toll-free telephone support.

The addition of a bare-bones, one-station DS990/10 raises the total purchase price of the development system package with software and 99/4 debugging hardware to about \$43,000. A higher-capacity package that includes the 990/10 with four development stations and two 99/4 debugging stations is about \$82,000.

The new development system configuration is part of an overall push by TI aimed at encouraging independent 99/4 software development for both resale and end-use applications. In third-party contracts, it is pursuing a multimedia approach in promoting development of software to be housed in a cassette, a minifloppy disk, or solid-state memory. Although more expensive, the 99/4's program command modules do offer advantages like relative security from pirating, durability, ease of use, and direct executability without downloading into RAM in the 99/4. Lower-priced 99/4 development systems are in the works.

Advant Inc., E-H International Inc. 696 Trimble Rd., San Jose, Calif. 95131. Phone (408) 946-9300 [371]

Intel Corp., 3065 Bowers Ave., Santa Clara, Calif. 95051. Phone (408) 987-8080 [372]  
Texas Instruments Inc., Consumer Relations, P. O. Box 53, Lubbock, Texas 79408. Phone (800) 858-1802; in Texas, (800) 692-1353 [373]

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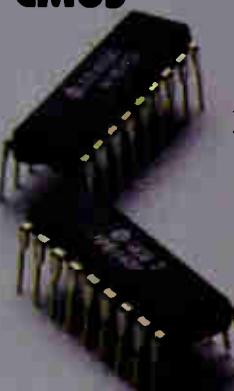
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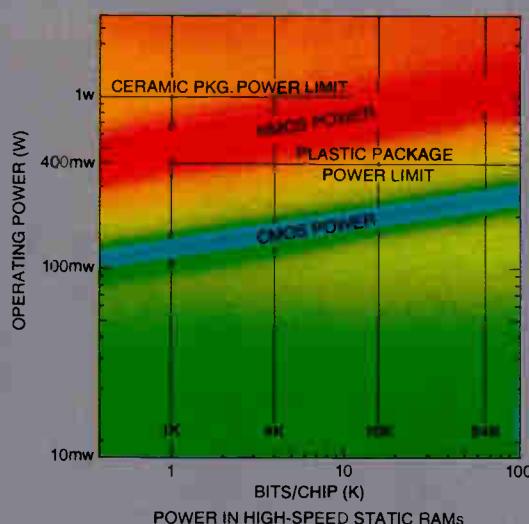
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4334	1K x 4	300/450	20mw	Now
4315	4K x 1	350/450	20mw	Now

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## New products

### Communications

## Audio distortion measured faster

Analyzer and oscillator join forces to measure harmonic distortion without adjustments

The process of making audio measurements is generally considered to be quite costly in terms of time and the level of operator skills required to perform such tests. Broadcast industry officials clamor that most, if not all, existing instruments capable of making the measurements require continual manipulation by highly skilled technicians. However, a new system to be formally unveiled at the National Association of Broadcasters (NAB) convention, which begins in Las Vegas on Sunday, April 13, should make attendees sit up and take note.

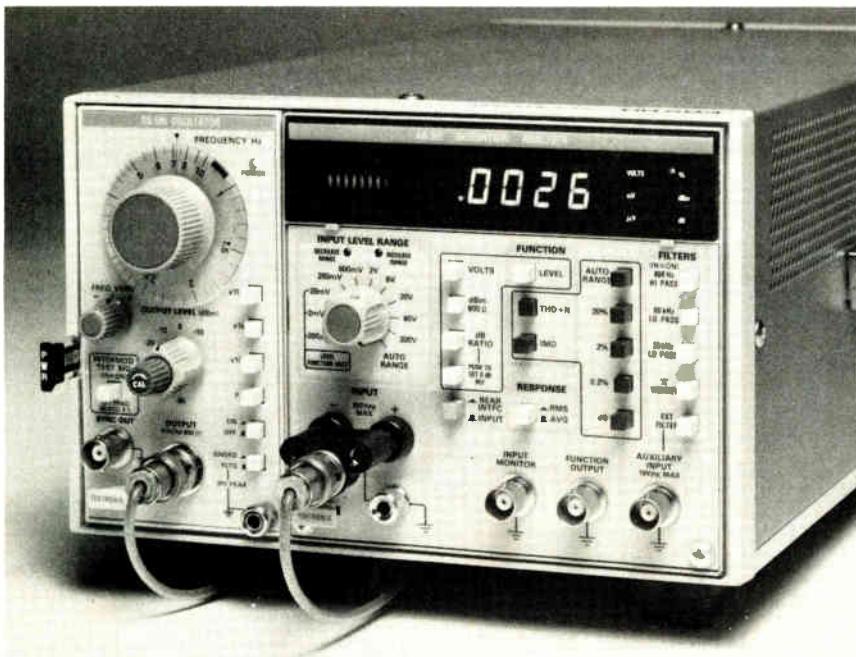
The heart of the system is the AA 501, an automatic total-harmonic-distortion (THD) analyzer from Tektronix. When used with the firm's recently introduced SG 505, an

extremely low-distortion oscillator, it establishes a new performance level by permitting quick automatic THD measurements without operator assistance.

According to Warren Beals, audio market specialist at Tektronix, the AA 501/SG 505 system "dramatically lowers the cost of measuring signal distortion by reducing measurement time." What's more, he adds, steps such as level setting, tuning, and nulling, "which previously required a skilled operator, are done automatically by the AA 501's internal circuitry."

To simplify the operator's tasks further, the AA 501 3½-digit light-emitting-diode display can read out distortion in percentages or decibels (autoranging). Signal input to the audio analyzer is displayed in decibels, decibels per minute, or volts. The detector is selectable—true root-mean-square or average—in all modes, as are four filters that minimize extraneous-signal effects.

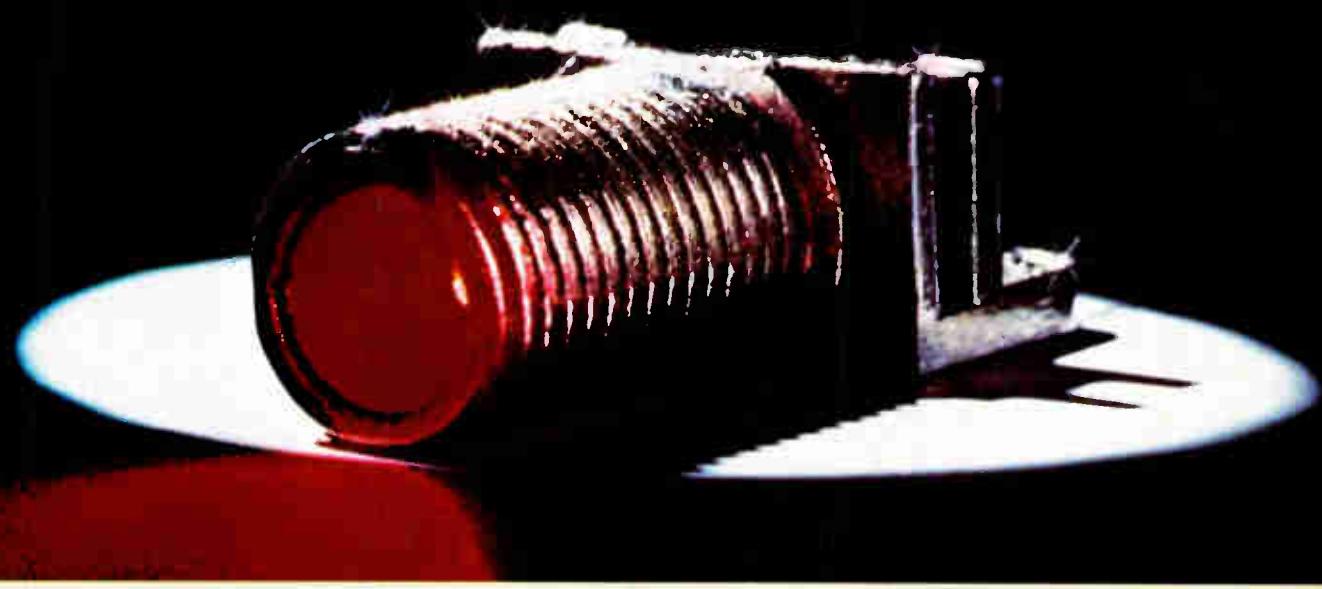
The AA 501 has several unique features, among them a special zero-reference-memory circuit that simplifies measurements such as gain and loss, frequency response, and signal-to-noise ratio. It also features a bar graph display, which makes



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## New products

trend information easy to see to aid in making peaking and nulling adjustments. Other significant features of the AA 501 include its ability to measure 3-μV to 200-V ac voltage with autoranging and less than 0.0025% (-92 dB) residual distortion and noise over a full fundamental-frequency range of 10 Hz to 100 kHz.

The SG 505 oscillator significantly boosts the measurement accuracy of the AA 501 because it has a specified distortion of 0.0008% THD (typically 0.0003%) from 20 Hz to 20 kHz. Continuous dial tuning and vernier frequency control allows for finer frequency adjustments over the AA 501's full frequency range. The SG 505 also has an extremely flat frequency response—within 0.1 dB from 10 Hz to 20 kHz—and a precise step attenuator that provides a calibrated output from +10 to -60 dB in 10-dB steps plus variable attenuation between steps.

Both the AA 501 and SG 505 are packaged as plug-ins for Tektronix's TM 500 family of modular test and measurement instruments. Thus, they can be readily combined with the user's choice of more than 40 instruments—including oscilloscopes, counters, and digital multimeters—in a single package. "Modularity also permits remote testing, especially important in audio field applications," notes Beals. An example of this is a studio-to-transmitter link with only one oscillator. In fact, the AA 501 automatically tunes to the SG 505 signal whether the two devices are housed side by side or miles apart, he adds.

Priced at \$1,750, the basic AA 501 is available 18 weeks after receipt of order, as is a \$600 option that allows measurement of intermodulation distortion on signals that conform to standards such as those of the Society of Motion Picture and Television Engineers (SMPTE), DIN, or the International Telephone Consultative Committee (CCIF). The SG 505, available now at \$600, also comes with an intermodulation test-signal option for \$125.

Tektronix Inc., P. O. Box 1700, Beaverton, Ore. 97075. Phone (503) 644-0161 [401]

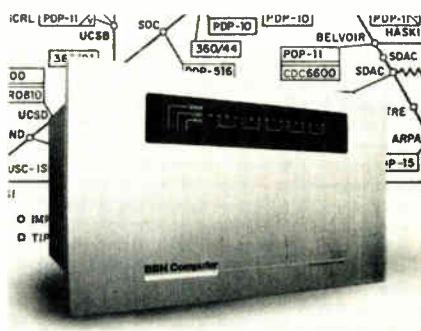
## Medium-speed switcher sells for under \$25,000

Even though the C/30 packet-switching processor system sells for under \$25,000, it offers twice the throughput of competitive systems that may cost twice as much, according to Martin Oakes, director of marketing for BBN Computer Corp. Not only does the processor move data at speeds in excess of 130 packets a second (each packet is 1,008 bits or less), but it also offers adaptive routing. In addition, the C/30 supports up to four host computers through as many as four Arpanet ports, six lines of rates of up to 56 kb/s to other nodes, and 64 asynchronous/synchronous terminals. It can be used either as a primary packet processor in a small network, or as a node in a larger network like Arpanet.

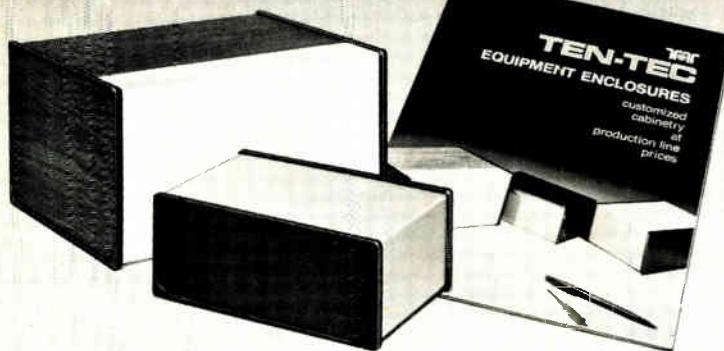
Many of the traditional input/output hardware functions are implemented in the processor's firmware, or microcode. This allows a single high-speed communications port to serve asynchronous, synchronous, and binary-synchronous devices with speeds from 50 to 19,200 b/s by changing the random-access-memory-based microcode.

The C/30 is based on a microprogrammable central processing unit with an instruction set. The basic elements are a 1-K-by-20-bit register file; a 512-by-32-bit microcode read-only memory containing the loader, debugger, and console logic; and a microcode memory of 2, 4, or 8 K by 32 bits that contains the macroinstruction set and I/O emulation.

The basic C/30 also includes two



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## New products

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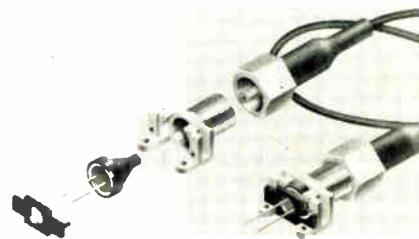
BBN Computer Corp., 33 Moulton St., Cambridge, Mass. 02238. Phone Martin Oakes at (617) 491-1850 [402]

## Fiber-optic components have fast response times

The MFOD104F p-i-n photodiode and the MFOE103F infrared light-emitting diode are both designed for use in fiber-optic systems. Capable of detecting infrared radiation, the MFOD104F detector has a typical response time of 2 ns at 20 v and 6 ns at 5 v. It is useful in analog fiber-optic systems that require a 100-MHz bandwidth and in digital systems with up to 200-Mb/s speeds. The MFOE103F, used as an infrared source, has a typical response time of 15 ns. In data-communication links operating at 5 v, the detector can be used at a speed of up to 110 Mb/s and the emitter at up to 20 Mb/s.

Both devices are packaged in Motorola's fiber-optic active-component (FOAC) plastic cases and are designed to fit directly into AMP Inc.'s P/N 227240-1 fiber-optic Optimate connectors. In quantities of 100 to 499, the MFOD104F and MFOE103F sell for \$30 and \$35, respectively.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone Harry Koshi at (602) 244-4304 [406]



# THE MULTIPLE CHOICE TESTER

## THE PRODIGY PT900 SYSTEM FROM 3H INDUSTRIES TESTS:

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## New products

### Instruments

## Scope processes waveform data

Multichannel oscilloscope with 16-bit microcomputer samples transients every 2  $\mu$ s

The Smartscope is an intelligent hybrid instrument—a cross between a multichannel oscilloscope and a 16-bit microcomputer—that is able to mathematically manipulate waveforms into more useful forms. The Smartscope can work in conjunction with high-speed transient recorders or sampling oscilloscopes, sampling transients at 2- $\mu$ s intervals.

Versions are available with both two and four input channels, with each channel capable of sampling 1,000 data points per measurement with a sensitivity range of  $\pm 100$  mV to  $\pm 20$  V. Since the Smartscope samples a single transient waveform rather than a repeated one, it can sample transients at the 2- $\mu$ s intervals while achieving 10-bit resolution on each data point.

The fun only begins with the acquisition of the data—once a waveform is captured, the Smartscope's 9900-based microcomputer can go to work. It has 16 16-K read-only memories and 16 16-K random-access memories. The basic model 3220, which sells for \$7,495, can record two arrays, each representing a captured waveform or a waveform constructed by mathematically manipulating the input data. Model 3280 (\$7,995) has more RAM and can handle eight arrays of data, while model 3281 (\$8,495) can store a total of 10,000 data points distributed among eight arrays.

The hybrid instrument can calculate and display convolved waveforms ( $F^*G$ ), as well as local maximums, minimums, and the area under a curve between two cursors. The cursors can be used to seek a specified amplitude value or time location. The scope can also display peak-to-peak value, root-mean-square values, slope, 10-to-90% rise time, mean, and one/delta time values. Any array of data can also be integrated, differentiated, smoothed, shifted, and rotated. Transcendental operators such as trigonometric, logarithmic, inverse, square root, and exponential operators can also be

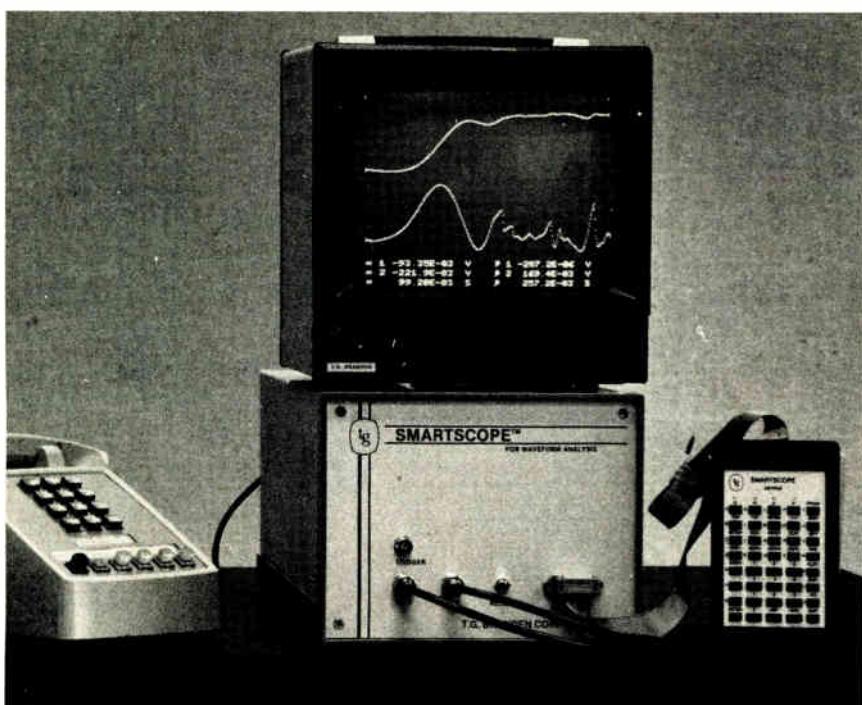
applied to any stored waveform.

The Smartscope has such features as the translation of time factors into the most convenient units. Instead of having to determine the 10% and 90% points on a waveform to calculate rise time, the user need only place cursors over the 0% and 100% points on the pulse in question. All bookkeeping information, such as labels for horizontal and vertical axes, date, title, and time of data acquisition may be displayed to further document the measurement. The trigger may also be offset in time, so that both post and pre-trigger information can be displayed.

The Smartscope includes a 9-in. cathode-ray tube, but its composite video output signal can be hooked up to larger displays for demonstration purposes. Information is manipulated by means of a hand-held calculatorlike keyboard, and user errors evoke a signal to try again instead of a branch to an error code.

The Smartscope contains an RS-232 communications capability, with an IEEE-488 communications link as a \$995 option. For an additional \$1,500, a fast-Fourier-transform software option allows a power measurement to be made in 40 s. A plotter option (\$1,695 more) creates a hard-copy record of the stored information, while 5.25- and 8-in. floppy-disk drives are also available for off-line storage.

T.G. Branden Corp., 5565 S.E. International Way, Portland, Ore. 97222. Phone (503) 659-9366 [351]



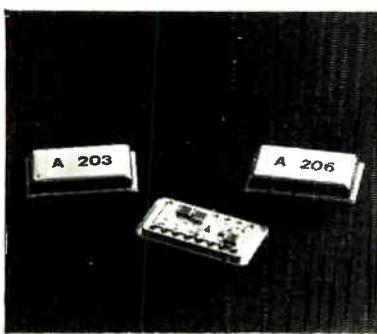
## 40-channel logic monitor has selectable thresholds

The model LM-3 logic monitor permits the simultaneous monitoring of up to 40 logic points, works with all logic families, and offers triggerable latching modes and selectable thresholds. Because it is less complex than logic analyzers, yet more sophisticated than fundamental logic probes, says the manufacturer, the LM-3 can be used at many testing levels.

Three modes allow the unit to fol-

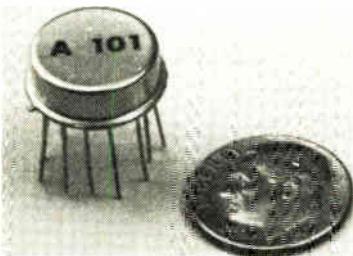
## NEW PRODUCT

### CHARGE SENSITIVE PREAMPLIFIERS



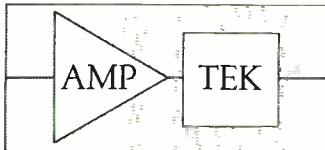
Models A-203 and A-206 are Charge Sensitive Preamplifier/Pulse Shaper and a matching Voltage Amplifier/Discriminator developed especially for instrumentation employing solid state detectors, proportional counters, photomultipliers, channel electron multipliers or any charge producing detectors in the pulse height analysis or pulse counting mode of operation.

These hybrid integrated circuits feature single supply voltage, low power dissipation (16mW), low noise, pole zero cancellation, unipolar and bipolar outputs and adjustable discrimination level.



Model A-101 is a Charge Sensitive Preamplifier-Discriminator and Pulse Shaper developed especially for instrumentation employing photomultipliers, channel electron multipliers and other charge producing detectors in the pulse counting mode. Its small size (TO-8 package) allows mounting close to the collector of the multiplier. Power is typically 15 milliwatts and output interfaces directly with C-MOS and TTL logic. Input threshold and output pulse width are externally adjustable.

All Amptek, Inc., products have a one year warranty.



AMPTEK INC.

6 DeAngelo Drive, Bedford, Mass 01730  
Tel: (617) 275-2242

## New products

low data and to latch on each trigger, on the first trigger only, or manually by means of a pushbutton. Three logic threshold levels can be set: a fixed +2.2-v dc threshold, a variable, monitored threshold between -5 and +10 v dc, and a supply-dependent threshold, determined as 70% of the V<sub>cc</sub> of the circuit under test.

All channels present a constant input impedance of 0.5 MΩ shunted by 6 pF, offer 5-MHz speeds, and are capable of capturing 100-ns events. Channel patterns are shown on 40 discrete light-emitting diode displays. The suggested U.S. resale price is \$585.

Global Specialties Corp., 70 Fulton Terrace, New Haven, Conn. 06509. Phone (800) 243-6077 [353]

### Controller interfaces

#### IEEE-488 bus to disk drive

An intelligent, single-board controller interfaces the IEEE-488 bus with two SA4000-series Winchester drives that store up to 58 megabytes each. The new MSC-1088 controller provides error correction and self-testing, and it upgrades from 14.5 Mb to over 100 Mb. It offers an alternative to floppy-disk storage for small business computers and micro-computer-based instrumentation. It controls Shugart Associates' 14.5-Mb SA4004, 29-Mb SA4008, and 58-Mb SA4100 drives.

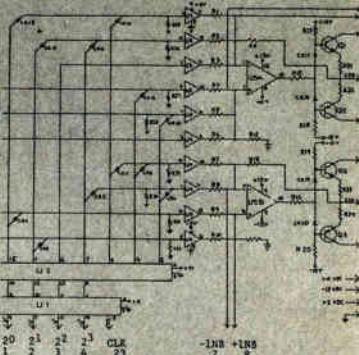
The unit is based on a bipolar microprocessor, as are other MSC-1080-series controllers that interface to other buses. For software compatibility, the unit's high-level command set can be used to write disk-operating tasks, or the manufacturer can supply special software-integration versions with custom firmware for the microprocessor as an option.

Prices of the controller range from \$2,650 in single-unit quantities to less than \$2,000 in original-equipment-manufacturer quantities. Delivery takes from 60 to 90 days.

Microcomputer Systems Corp., 432 Lakeside Dr., Sunnyvale, Calif. 94086. Phone Don Sumner at (408) 733-4200 [356]

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## New products

### Components

## Optical fiber has two windows

Fiber transmits light at 850 and 1,300 nm with 3.0 and 1.5 dB/km attenuation

Most optical fibers for communications currently carry light signals from sources operating at about 850 nm, but since a fiber can carry more data farther if it is using sources operating at 1,300 nm, the greatest commercial interest at present lies in light sources operating at either 850 or 1,300 nm.

To straddle the wavelength gap, Corning has developed an optical fiber that transmits light well at 850 nm and even better at 1,300 nm. It is a result of improvements at Corning in glass-composition control and in manufacturing techniques. The company claims the fiber offers "superior performance at the wavelengths of present sources and improved attenuation performance at wavelengths proposed for second-generation operation."

With a 50- $\mu\text{m}$  core and a 125-nm outer diameter, the new fiber conforms to generally accepted international standards for dimensions. The fibers are standardized according to a matrix that includes both attenuation and bandwidth. Thus, any one of five bandwidth specifications could be categorized with any one of three attenuation relationships, and vice versa.

The three nominal attenuation rates, at 850 and 1,300 nm, respectively, are: 2.5 and 1.0, 3.0 and 1.5, and 3.5 and 2.0 dB/km. The five nominal bandwidths (measured at 1 km) are 200, 400, 600, 800, and 1,000 MHz. The lower attenuation will always be at 1,300 nm, a feature that the company says makes the double-window fiber upgradeable, even when in use. In a paper presented at the International Conference on Fiber Optics in Industry in

London last month, Leslie Gunder-son, Corning's director of optical wavelength technology, predicted that sometime in the near future "it will be possible to specify a fiber having perhaps three 'windows' of operation, thus virtually tripling the signal-handling capacity compared to a single-window product."

The two-window fiber's bandwidth is equal to or greater than the amount specified throughout the entire spectral band between 850 and 1,300 nm. The fibers are coated with cellulose acetate lacquer and come on reels in 1,100-m lengths. Nominal numerical aperture of the fiber is 0.20.

As an example of the prices, the Corguide 3008D, which has an attenuation of 3.0 dB/km in the first window and 1.5 dB/km in the second window, will sell for \$1.40 per meter in 100-km quantities. This fiber has an 800-MHz minimum bandwidth (measured at 1 km) in both windows. Delivery time is four weeks after receipt of order.

Corning Glass Works, Telecommunications Products Department, Corning, N.Y. Phone (607) 974-9000 [341]

## Op amps have 0.3 mV p-p input noise voltage

A family of operational amplifiers is intended to replace Precision Monolithics Inc.'s OP-01, OP-05, OP-07, and OP-10. Designated the MP5501/OP-01, MP5505/OP-05, MP5507/OP-07, and MP5510/OP-10, they are pin-compatible with the PMI line. The MP5507 has a low input noise voltage of 0.3 mV peak to peak from 0.1 to 10 Hz. It will not drift more than 1  $\mu\text{V}$  per month.

For the MP5505, encased in a plastic miniature dual in-line package, the price is \$3.20 each in 100-piece quantities. In the same package and quantity the MP5507/OP-07 sells for \$4.50 and the MP5510/OP-10 for \$11.28.

Micro Power Systems Inc., 3100 Alfred St., Santa Clara, Calif. 95050. Phone (408) 247-5350 [343]

## Quad comparator has current offset of 10 nA

Designed to offer twice the precision of most comparable quad comparators, the model CMP-04 has a maximum offset voltage of 1 mV and a maximum offset current of 10 nA. The CMP-04 has a typical output sink current of 16 mA and a typical 1.3  $\mu\text{s}$  signal response. Operating either from a single 5.0-v supply or a dual supply of up to  $\pm 18.0$  v, the comparator is useful in set-point indicators, analog-to-digital converters, oscillators, and zero-crossing detectors. The maximum power-supply current of 2 mA remains almost constant even with changes in supply voltage and temperature.

Available in a 14-pin hermetic package, the model CMP-04 FY operates over the temperature range from  $-25^\circ$  to  $+85^\circ\text{C}$  and the CMP-04 BY from  $-55^\circ$  to  $+125^\circ\text{C}$ ; the CMP-04 BY/883 operates over the same range and meets MIL-STD-883 specifications.

In a quantity of 100 units, the CMP-04 BY sells for \$9.95 each, the CMP-04 BY/883 for \$11.95 each, and the CMP-04 FY for \$6.50 each. Delivery is from stock.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050. Phone David Gillooly at (408) 246-9222 [346]

## Quartz-crystal oscillator consumes only 50 mA

Designated model LQXO-4, this quartz-crystal oscillator that consumes only 50  $\mu\text{A}$  of current is useful in battery-powered products requiring a 10 kHz to 250 kHz timebase for precise frequency control. Self-contained in a TO-5 package, the hybrid unit consists of a tuning fork crystal, a complementary-MOS amplifier, capacitors, and resistors mounted on a thin-film substrate. The oscillator can operate over a temperature range from  $-55^\circ$  to  $+125^\circ\text{C}$ , can withstand shock to 1,000 g, and is accurate to within  $\pm 0.01\%$ .

# THE 60-SECOND PLANT TOUR.

( $\pm 0.02\%$  typical). In quantities of 1,000, the LQXO-4 sells for \$12.50. Delivery is from stock.

Statek Corp., 512 N. Main St., Orange, Calif. 92668. Phone (714) 639-7810 [344]

## Capacitors withstand 300°C temperatures

A line of capacitors with ranges from 1 to 250,000 pF and 50 to 2,000 v dc can withstand temperatures as high as 300°C and as low as -55°C. Tolerances go as low as  $\pm 1\%$ . The devices are manufactured from virgin ruby mica and the leads are brazed to the element.

Prices vary with specifications. For example, one model, the FT44CM102K, is priced at \$10 each in 10-piece quantities.

KD Components, 3016 Orange St., Santa Ana, Calif. 92707. Phone (714) 545-7108 [345]

## Transistors aid negative voltage supply

Two pnp silicon transistors, the PN4002 and the PN4003, have collector-emitter sustaining voltages of 80 and 100 v, respectively, with continuous collector currents of 30 A and peak-collector currents of 40 A. Suitable for regulating negative-voltage power supplies, the PN4002 has a collector-base voltage of 100 v and the PN4003 has one of 120 v. Both devices have an emitter-base voltage of 8 v and a continuous base current of 10 A. Saturation voltage is 1.2 v. Turn-on time is 600 ns with a fall time of 250 ns. At 30 A, the minimum gain is 10; at 15 A, the minimum gain is 20.

Power dissipation is 100 w at a 100°C case temperature; the devices derate at 1 w/°C above that point. In 100-piece quantities, the PN4002 sells for \$40 each and the PN4003 sells for \$44 each. Delivery is from stock to 30 days.

Solid State Devices Inc., 14830 Valley View Ave., La Mirada, Calif. 90638. Phone (213) 921-9660 [347]

**BUILDING #1606-267**  
19,087 sq. ft., 7 years old. Tilt-up concrete floor, 19' ceiling. City water/sewer, natural gas, 100% sprinklered. Minutes to interstate. Community size: 33,580. Eastern Region.

**BUILDING #1606-270**  
18,000 sq. ft., 1-1/2 acres. Metal construction, 20' ceiling at center, 6' concrete floor. Municipal water/sewer available. Former sewing plant. Community size: 2,160. Western Region.

**BUILDING #1606-281**  
120,000 sq. ft., 3 acres. Brick construction, 16' to 18' ceilings, bay spacing 32' x 30'. 100% air conditioned and sprinklered. Total space 10,000 sq. ft.

municipal water, sewer. Rail siding for three cars. One-half hour to major airport, minutes to interstate. Community size: 8,680. Piedmont Region.

**BUILDING #1606-271**  
15,000 sq. ft., 53 acres. Metal construction, 120' x 120' clear span, 22' ceiling at center and end, 6' concrete floor. Municipal water/sewer, rail siding for eight cars. Community size: 19,410. Eastern Region.

**BUILDING #1606-277**  
46,500 sq. ft., 5.25 acres. Pre-cast concrete construction, completed in 1977. 24' ceiling, bay spacing 25' x 40'. 6,500 sq. ft. office, air conditioned. Total space 10,000 sq. ft.

siding for two cars, levelers on truck loading docks. Community size: 2,210. Western Region.

**BUILDING #1606-229**  
86,400 sq. ft., 40 acres. Metal construction, 24' ceiling at eaves, bay spacing 30' x 240'. Less than five minutes from major airport and interstate. Community size: 148,450. Piedmont Region.

**BUILDING #1606-266**  
44,090 sq. ft., 20 acres. Under construction, insulated concrete panels with interior completed to occupant's specifications. 18' ceiling, bay spacing 40' x 30'. Community size: 22,520. Eastern Region.

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AN/FPS-20-75  
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AN/SPS-6C  
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- 200-2000 MHz 40 W CW
- 210-225 MHz 1 MW 5 us
- 385-575 MHz 1.5 KW CW
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- 950-1500 MHz 1 KW .06 DC
- 900-1040 MHz 5-10 KW .006 DC
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- 1.5-9.0 GHz 150 W CW
- 3.2-3.3 GHz 10 KW .002 DC
- 2.7-2.9 GHz 1 MW 1 uS
- 3.1-3.5 GHz 1 MW 1.3 uS
- 2.7-2.9 GHz 5 MW 2-3 uS
- 4.4-5.0 GHz 1 KW CW
- 5.4-5.9 GHz 5 MW .001 DC
- 6 GHz 1 MW 1 uS
- 6.2-6.8 GHz 200 KW .37 uS
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- 3 MW 50 KV 60 A; .30 uS
- 10 MW 76 KV 135 A; .001 DC
- 66 MW 160 KV 400 A; .00

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X BAND NIKE AJAX/HERCULES  
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X BAND MOBILE 40 KW AN MPQ-29  
X BAND BEACON 100 W AN/DPN-52  
S BAND 10' DISH 500 KW AN/MPQ-18  
S BAND 250 KW AN/MPQ-10A  
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S BAND HGT FINDER 5 MW AN/FPS-6  
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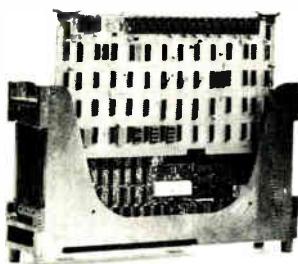


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<b>MSBC-512</b>	512 x 512 graphics
<b>MSBC-1024</b>	1024 x 256 graphics
<b>MSBC-24/320</b>	24 x 80 alpha; 320 x 240 graphics combined
<b>RGB-256</b>	256 x 256 x 4; 16 color or grey graphics

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## New products

### Packaging & production

## System controls crystal thickness

Automatic lapping of crystals is accomplished with automatic frequency control

Lapping is one of the most critical yet least modernized processes in the manufacture of quartz crystals. This process is used to adjust the few-mil thickness of quartz wafers to within a few millionths of an inch from the target width. It involves placing wafers in a lap machine and grinding them between two flat plates in the presence of a slurry, or liquid abrasive. Many methods for monitoring crystal thickness have been tried, but none are suitable for reliably and precisely automating the production process of AT-cut quartz crystals whose useful frequency spectrum goes up to over 40 MHz.

Because of this and the increasing demand for precision crystals, Transat Corp. has come out with a patented automatic lapping controller (ALC). The system consists of a special indicator/controller and a special probe/mounting assembly.

A sweep-frequency signal is in-

jected into an electrode on a lapping plate and resonances are observed as blanks pass under the electrode. Resonance frequencies of individual blanks are shown on the indicator's light-emitting-diode display and are compared with an adjustable target frequency. Lapping is terminated automatically when the highest observed blank frequency exceeds the target frequency.

The ALC provides automatic lapping control of up to 43 MHz (extendable to 80 MHz) for fundamental, third, and fifth crystal overtones at an accuracy of 0.1%. It also indicates when the difference between the highest and lowest frequency gets too large during and after lapping. This difference is called the spread. Knowledge of the spread is important for two reasons. First, it determines when the lapping plates need to be re-flattened. Second, it is needed to set the cutoff frequencies related to the spread.

The ALC works with planetary and eccentric laps and with oil- and water-based slurry. According to customer information, the ALC requires less operator skill and increases the output per operator by a factor of about two when used with one lapping machine and about three when timeshared between two lapping machines. Presently, Transat is evaluating its machine's application to semiconductor materials.



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## New products

The price of the ALC is \$6,200. Delivery takes 10 weeks.

Transat Corp., 3713 Lee Rd., Shaker Heights, Ohio 44120. Phone (216) 991-7300 [391]

Probe tester has 0.0001-in. resolution in X-Y stage

Designed for the probe testing of semiconductor devices in either a wafer or packaged configuration, the REL-4000 failure analysis test station with the Bausch & Lomb Microzoom microscope offers high resolution and precise linear motions. The microscope offers the user magnification ranges from 22.5X to 3000X via 10X, 15X, or 20X eyepieces.

The test station consists of a 4-by-4-in. micrometer X-Y stage with 0.0001-in. resolution, turret Z-θ device stage with 1-in. linear Z motion, and a theta rotational motion of 360°, 4-in.-diameter vacuum chuck, delayed probe ring lift with 1-in. linear Z motion for probe ring positioning, and vertical support posts. The REL-4000 will accept up to 10 Alessi microprobes.

An average price for a complete station with probe, including the microscope, is \$12,500.

Alessi Industries, 3195 Airport Loop Dr., Building C, Costa Mesa, Calif. 92626. Phone (714) 979-8912 [395]

## Bus bar ties together wire-wrapped posts

A spring-tempered modified copper bar ties together wire-wrapped posts by just being in contact with them, eliminating the soldering process. The posts snap-fit into the notches on the bar. In a quantity of 100 lots, the back plane bus sells for \$3.50 each.

Delivery is from stock for prototype use. All other deliveries are from four to six weeks.

Buss-Tronics, 261 St. Mihiel Dr., Unit One, Riverside, N.J. 08075. Phone (609) 764-9750 [400]

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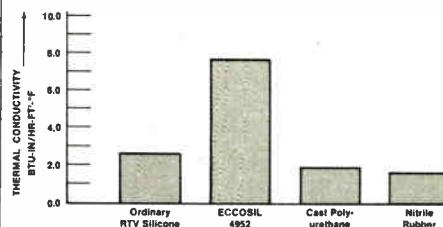
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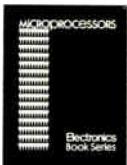
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## New products

### Data acquisition

## A-d converter has 10-ns speed

Parallelled 6-bit units, each sampling at 110 MHz, achieve resolution over 7 bits

A typical sampling rate of 110 MHz and a conversion time of less than 10 ns are the prime features of a self-contained monolithic analog-to-digital converter that Siemens AG is now offering in sample quantities. Its resolution is 6 bits. But by adding one or more converters of the same type in parallel, resolutions of 7 or more bits can be achieved without affecting the sampling rate.

The high speed, says Helmut Güntner, a product-marketing specialist in the company's Munich-based components group, makes the SDA 5010 well-suited for handling the fast analog signals encountered in radar and X-ray equipment, in ultrasound and medical systems, and in test and measuring instruments such as storage oscilloscopes and transient recorders. For slower signals, Siemens is also offering samples of a 50-MHz, 6-bit, 12-ns a-d converter—the SDA 6020.

In order to appeal to as wide a market segment as possible, and to offer ease of application, the 5010's designers have paid particular attention to these aspects: a wide input-voltage range, small power dissipation, and convenient packaging. The

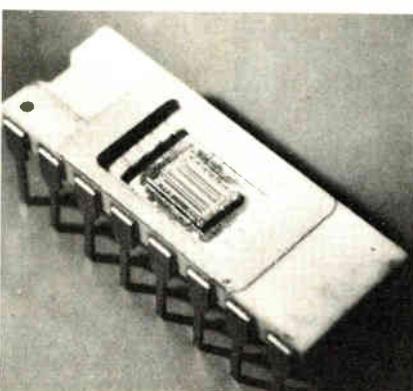
device, in a standard 16-pin, dual in-line ceramic package, handles input voltages from +2.5 to -2.5 V—"a relatively wide range for a monolithic converter," says Güntner. It dissipates only 450 mW and the non-linearity is  $\pm \frac{1}{4}$  least significant bit. This accuracy hardly changes with temperature.

The 5010 packs a powerhouse of functions on an 11-mm-square chip. It incorporates a block of 64 comparator stages, one with the same number of latches. It also has AND and OR encoders as well as output stages. For all this, the device contains only 1,100 components—transistors and resistors. Its supply voltages are +5 and -5.2 V.

**Fast.** The key to the device's high speed, says Peter Rydval, one of the designers of the 5010, is the combination of emitter-coupled-logic technology and the parallel conversion technique. In this method, the analog signal is compared in the 64 comparator stages with internal reference voltages, the latter derived from voltage dividers. The results of the comparison are transferred to the 64 subsequent latches.

The comparison and transfer occur during the sample mode—that is, when the strobe input is at a low logic level. When that input changes to a high level, thereby initiating the hold mode, the latches are separated from the comparators. The memory contents are then transformed in the AND and OR encoders and finally appear at the output as a digital word. With parallel conversion, which is inherently faster than successive approximation, the linearity changes negligibly with temperature because resistance ratios rather than absolute resistance values are involved, Rydval explains.

Since the latches are separate from the comparators during the hold, or storage, mode, the analog signal is always present at the converter input. This obviates the need for a sample-and-hold circuit at the extremely short conversion times. The relatively low switching noise inherent in ECL technology makes for minimum crosstalk between the converter's digital and analog parts.



Which analog-signal range undergoes 6-bit resolution is determined by the potential at the voltage reference terminals. When the analog signal is greater than the positive reference voltage, the signal is evaluated in the overflow comparator. The encoder circuits are designed so that when the positive reference voltage is exceeded, the data outputs zero through five are blocked and the overflow output becomes the 7th bit. This way, resolutions of 7, 8, and more bits can be achieved by simply adding an appropriate number of 5010 converters in parallel.

Samples of the 5010 are available now and volume quantities can be obtained in a few months, Güntner says. The unit price is \$400. In lots of 10, the price drops to \$285 and then to \$200 in lots of 100 pieces. Siemens Corp., 186 Wood Ave. South, Iselin, N.J. 08830. Phone (201) 494-1000 [381] Outside the U.S.: Siemens AG, Components Group, D-8000 Munich 80, P.O. Box 801709, West Germany [382]

## 8085-based parallel-to-serial converter sells for \$1,990

A microprocessor-based parallel-to-serial converter—the PSC/4000—sells for \$1,990 in single quantities. The converter interfaces a variety of measuring devices with mini- and micro-computers, cathode-ray tubes, teletypewriters, and serial printers.

The PSC/4000 uses an Intel 8085 microprocessor with up to 8 K of erasable-programmable read-only memory and 256 bytes of random-access memory. It has a buffered input and output, with 13 input lines, 16 I/O lines, and 3 interrupt lines for its parallel programming. Programmable RS-232, 20-mA, or two-wire direct interfaces are provided. Data can be edited and reformatted by the unit prior to output. Programmable elements in the serial interface are baud rate, parity, character length, and the number of stop bits. Delivery takes about 60 days.

The Standard Register Co., Data Systems, P.O. Box 1167, Dayton, Ohio 45401. Phone J.A. Cornely at (513) 223-6181 [385]

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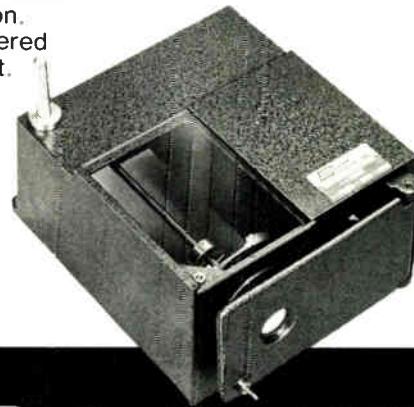
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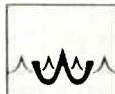
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### New products/materials

This low-density, two-part epoxy system is designed for molding by the liquid-transfer method. Eccomold LTM 1090 can encapsulate such devices as coils, glass diodes, flat-packs, semiconductors, and integrated circuits at pressures less than 100 psi. At this pressure, the micro-balloon filler of the material will not be damaged. The Brookfield viscosity of the epoxy is 40,000 and the mold shrinkage is 0.012 in./in. The epoxy system can be cured in 1 to 3 minutes at 250° to 340°F. After being cured, Eccomold LTM 1090 displays such properties as a volume resistivity of greater than  $9 \times 10^{14}$  ohm-cm, a specific gravity of 0.8, and a Shore D hardness of 85. In addition, it has a dielectric constant of 2.5 and a dissipation factor of 0.03, both at 1 MHz.

Emerson & Cuming Dielectric Materials, Dewey and Almy Chemical Division/W. R. Grace & Co., Canton, Mass. 02021 [476]

This thermometer strip indicates a rise in temperature by changing from whitish gray to jet black in eight steps. Providing a permanent, nonreversible record, the Thermax strip is accurate to within 1°C or 1%, whichever is greater. Response time is less than 1 s. These self-adhesive strips are available in five standard ranges between 37°C (99°F) and 260°C (500°F). Measuring 2 in. by 0.75 in., they come in packets of 10 strips or in reels for as low as 60¢ per strip.

BH Frank Co., 3733 W. 139th St., Hawthorne, Calif. 90250 [477]

A 99% alumina ceramic, 502-1400, can be machined and is operable at temperatures up to 2,600°F; at 3,400°C, it shrinks 12% to 14%. Aremcolox is useful for prototype work. The material has a compressive strength of 10,000 psi, a flexural strength of 8,000 psi, a dielectric strength of 100 v/mil, and a resistivity of  $10^{10}$  ohm-cm. The machinable ceramic is available in rods ranging from 0.5 in. in diameter by 6 in. long to 2½ in. in diameter by 3 in. long. Prices range from \$32 to \$45 each.

Aremco Products Inc., P. O. Box 429, Ossining, N. Y. 10562 [478]

# Products newsletter

## Improved analyzer troubleshoots data networks faster

A much improved version of Hewlett-Packard Co.'s model 1640 serial data analyzer is coming soon from the company's Colorado Springs division. The new **model 1640B** is a menu-driven troubleshooting instrument that can monitor or simulate elements of digital data-communications networks and that simplifies functional analysis of systems using serial interfaces. Two branching modes in the simulation operation allow a user-generated message to be transmitted repeatedly until a reply is received, while two other messages are kept on hold. A new memory bit shift allows bit-by-bit checking of transmitted or received data and other functions. Price of the 1640B is \$5,800, with availability in four weeks.

## TI's 99/4 will put on 64 kilobytes of RAM

Texas Instruments Inc. plans to introduce later this year an add-on memory peripheral for the 99/4 home computer that will provide up to 64 kilobytes of additional random-access memory. This will boost potential 99/4 RAM capacity to a total of 80 kilobytes. Also planned is a new plug-in solid-state command module containing Extended Basic codes. TI hopes the additions will answer some users' complaints that the 99/4 by itself makes slower and harder work of developing cassette or disk programs than some competing personal computers.

## OEM printers from Data Printer get tougher

Data Printer Corp., Malden, Mass., is offering an original-equipment-manufacturer version of its 3000 series line printers—the **3001 series of four models, which offer speeds from 150 to 900 lines/min** with a standard 64-character ASCII font. Aimed at minicomputer and mainframe systems in the \$50,000 to \$150,000 class, the Bandline printers exhibit heavier duty-cycle capabilities than the smaller 3000s. Features include changeable and customized fonts, as well as Chaintrain-type hammer-and-actuator combination to aid in resisting horizontal printing stress. Prices range from \$5,805 to \$10,215 per unit depending on speed. Delivery is in 60 to 90 days.

## Price changes

- **Motorola Semiconductor** is chopping prices about 40% on its fiber-optic components, believing that costs are still holding back faster customer growth. The emitter model MFOEL03F goes from \$47 to \$30.50, and an integrated-circuit detector-preamp, MFOD402, goes to \$32.50 from \$50. Officials at the company's optoelectronics group in Phoenix feel that stronger demand would justify automation, leading to much lower prices.
- **Intel Corp., Santa Clara, Calif.**, reduced the prices of its 2732 and 2732A 32-K ultraviolet-light-erasable programmable read-only memories by as much as 50%.
- **Spectronics Inc., a division of Honeywell Inc.** in Dallas, has cut the price of its Sweet Spot SE3352-2 and -3 light-emitting and SD3322 photo diodes by over 20% for volume and 50% for single-quantity orders.
- **Verbatim Corp., Sunnyvale, Calif.**, increased prices by 3% to 10% on all of its magnetic media products—data cartridges, cassettes, and diskettes.
- **SD Systems, Garland, Texas**, announced a price reduction in its Z-80-based computer, the SD-100, to \$6,995.
- To make way for the double-window optic fibers just introduced (see p. 176), **Corning Glass Works, Corning, N. Y.**, decreased prices on its standard (850-nm) wavelength Corguide fibers as much as 33%.

# Classified section

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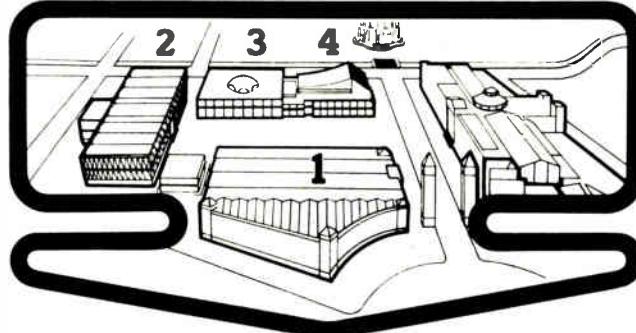
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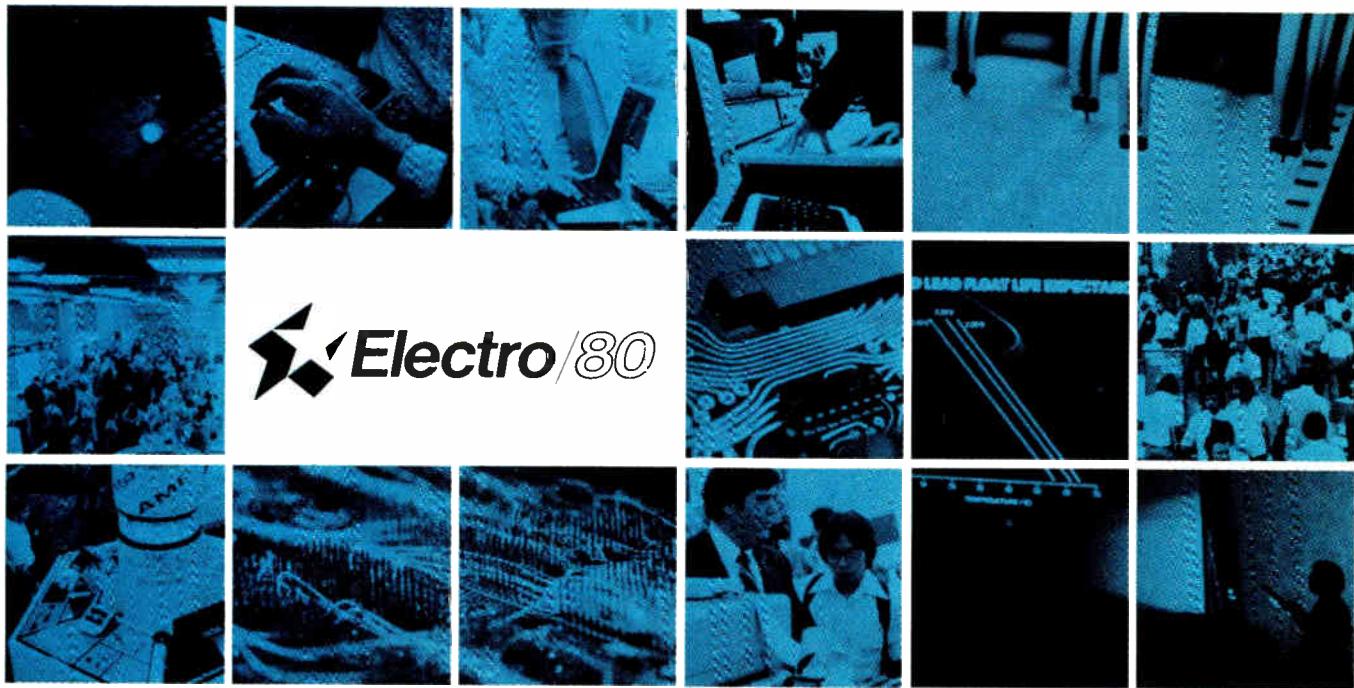
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- b Communications Equipment & Systems
- c Navigation, Guidance or Control Systems
- d Aerospace, Undersea Ground Support
- e Test & Measuring Equipment
- f Consumer Products
- g Industrial Controls & Equipment
- h Components & Subassemblies

**5 Source of Inquiry—DOMESTIC**

- j Independent R&D Organizations
- k Government

**Your design function (check each letter that applies):**

- x I do electronic design or development engineering work.
- y I supervise electronic design or development engineering work.
- z I set standards for, or evaluate electronic components, systems and materials.

**Your principal job responsibility (check one)**

- t Management
- v Engineering

**Estimate number of employees (at this location):** 1.  under 20    2.  20-99    3.  100-999    4.  over 1000

1 16 31 46	61 76 91 106	121 136 151 166	181 196 211 226	241 256 271 348	363 378 393 408	423 438 453 468	483 498 703 718
2 17 32 47	62 77 92 107	122 137 152 167	182 197 212 227	242 257 272 349	364 379 394 409	424 439 454 469	484 499 704 719
3 18 33 48	63 78 93 108	123 138 153 168	183 198 213 228	243 258 273 350	365 380 395 410	425 440 455 470	485 500 705 720
4 19 34 49	64 79 94 109	124 139 154 169	184 199 214 229	244 259 274 351	366 381 396 411	426 441 456 471	486 501 706 900
5 20 35 50	65 80 95 110	125 140 155 170	185 200 215 230	245 260 275 352	367 382 397 412	427 442 457 472	487 502 707 901
6 21 36 51	66 81 96 111	126 141 156 171	186 201 216 231	246 261 338 353	368 383 398 413	428 443 458 473	488 503 708 902
7 22 37 52	67 82 97 112	127 142 157 172	187 202 217 232	247 262 339 354	369 384 399 414	429 444 459 474	489 504 709 951
8 23 38 53	68 83 98 113	128 143 158 173	188 203 218 233	248 263 340 355	370 385 400 415	430 445 460 475	490 505 710 952
9 24 39 54	69 84 99 114	129 144 159 174	189 204 219 234	249 264 341 356	371 386 401 416	431 446 461 476	491 506 711 953
10 25 40 55	70 85 100 115	130 145 160 175	190 205 220 235	250 265 342 357	372 387 402 417	432 447 462 477	492 507 712 954
11 26 41 56	71 86 101 116	131 146 161 176	191 206 221 236	251 266 343 358	373 388 403 418	433 448 463 478	493 508 713 956
12 27 42 57	72 87 102 117	132 147 162 177	192 207 222 237	252 267 344 359	374 389 404 419	434 449 464 479	494 509 714 957
13 28 43 58	73 88 103 118	133 148 163 178	193 208 223 238	253 268 345 360	375 390 405 420	435 450 465 480	495 510 715 958
14 29 44 59	74 89 104 119	134 149 164 179	194 209 224 239	254 269 346 361	376 391 406 421	436 451 466 481	496 701 716 959
15 30 45 60	75 90 105 120	135 150 165 180	195 210 225 240	255 270 347 362	377 392 407 422	437 452 467 482	497 702 717 960

# Electronics

April 10, 1980 This reader service card expires July 10, 1980

NAME \_\_\_\_\_ TITLE \_\_\_\_\_

PHONE ( \_\_\_\_\_ ) COMPANY \_\_\_\_\_

STREET ADDRESS (Company  or home  check one) \_\_\_\_\_

CITY \_\_\_\_\_ STATE \_\_\_\_\_ ZIP \_\_\_\_\_

Was This Magazine Personally Addressed to You?  Yes  No

**Industry classification (check one):**

- a Computer & Related Equipment
- b Communications Equipment & Systems
- c Navigation, Guidance or Control Systems
- d Aerospace, Undersea Ground Support
- e Test & Measuring Equipment
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15 30 45 60	75 90 105 120	135 150 165 180	195 210 225 240	255 270 347 362	377 392 407 422	437 452 467 482	497 702 717 960

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## TYPICAL SPECS FOR SPECTRONICS' EMITTERS AND DETECTORS

### LED

Peak # Emission	850 nm
I <sub>o</sub>	0.6 mA
High efficiency silicon grown	
P <sub>d</sub>	3 mW @ I <sub>o</sub> = 100 mA
High pulse current	30 A

### Photodiode

I <sub>o</sub>	5 mA
I <sub>o</sub>	40 μA @ I <sub>o</sub> = 2 mA and V <sub>D</sub> = 20V
Application	Linear, analog or frequency

### PHOTOTRANSISTOR

I <sub>o</sub>	5 mA
I <sub>o</sub> (SAT)	10mA @ I <sub>o</sub> = 5 mA and V <sub>D</sub> = 5V
Application	0.7V @ I <sub>o</sub> = 4 mA General Purpose Detection

### PHOTODARLINGTON

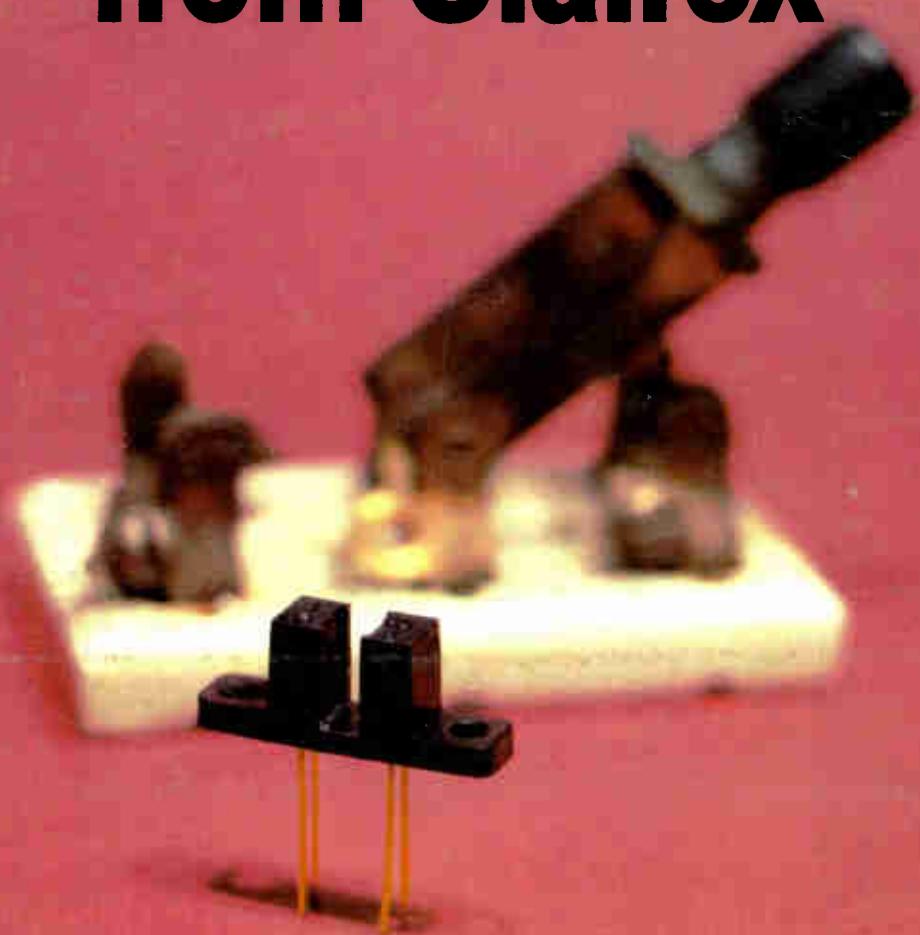
I <sub>o</sub>	100 μA
I <sub>o</sub>	4 mA @ I <sub>o</sub> = 0.2 mA/cm <sup>2</sup>
V <sub>D</sub> (SAT)	5V
Application	1.7V @ I <sub>o</sub> = 1 mA High current or high-light sensitivity requirements

### PHOTO IC

Schmitt Trigger Output	50 ns
I <sub>o</sub>	10 mA load @ V <sub>D</sub> < .4V
Output Drive	5 μA
Propagation Delay	> 55 ns + 100%
I <sub>o</sub>	Data Switching

Switch from the old to the new!

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Switch from slow switching, moving parts and arcing problems to fast switching, solid-state, low-cost optical switches from Clairex.

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