

DECEMBER 4, 1980

CAN JAPANESE-STYLE QUALITY CIRCLES WORK IN THE U. S.?/95

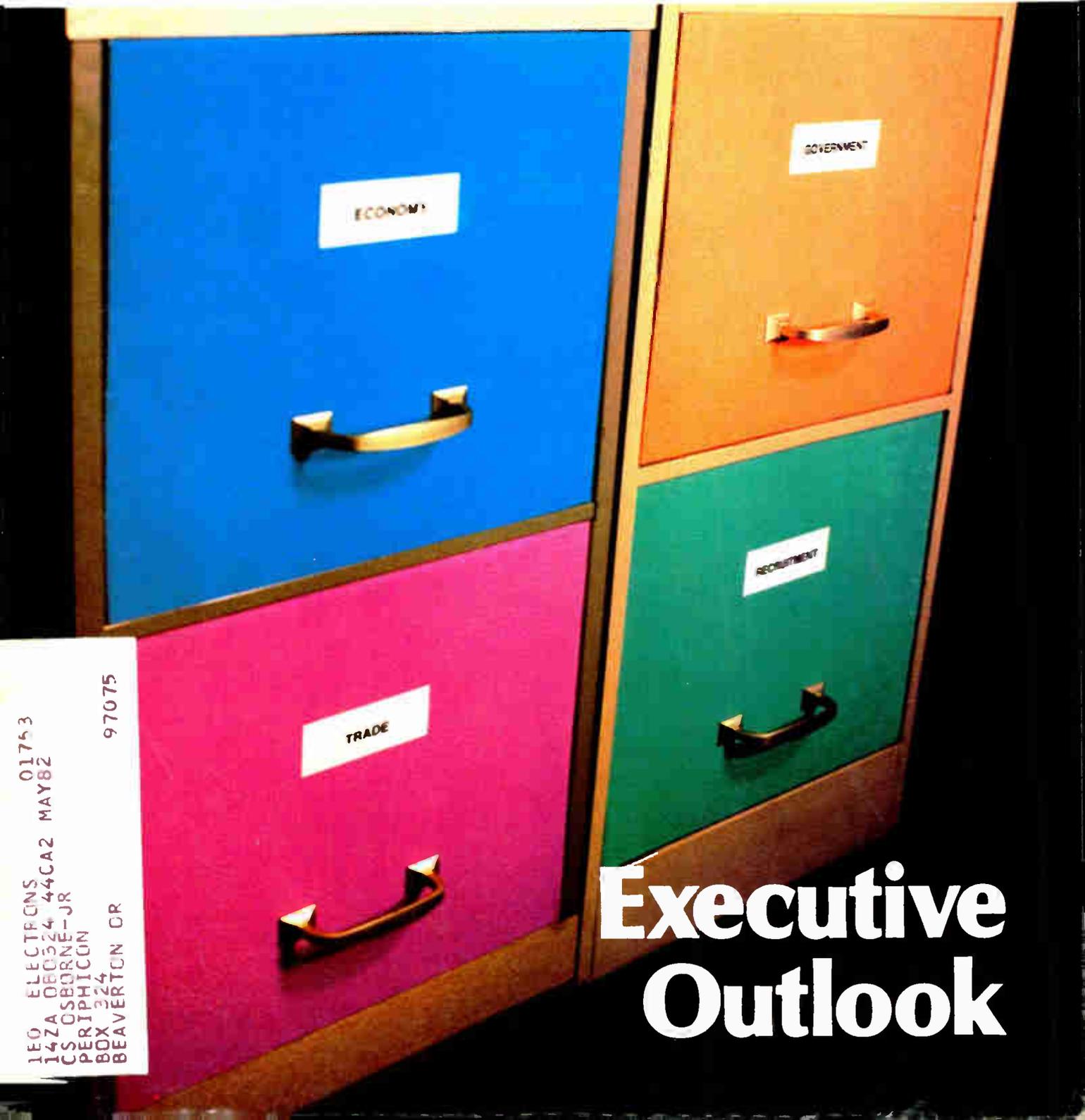
Three solutions to RAM testing/ 132

Subprograms structure Fortran for top-down design/ 150



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Executive Outlook

6.

Circuit Board Testing Update/No. 6 in a series from Hewlett-Packard.

HOW DEPENDENT SHOULD YOU BE ON THE ATE SUPPLIER?

Automatic board test equipment can provide a powerful solution to today's testing needs. But choosing the right system can be a complex and bewildering task, because of all the non-hardware factors to be assessed.

Purchase alternatives.

One factor is the question of system responsibility. At one end of this spectrum is a turnkey system. Here the ATE manufacturer assumes total responsibility and the user is dependent upon the supplier for hardware, software and system implementation. At the other end is the do-it-yourself system tailored to your exact application, in which case the user is almost self-sufficient. Other alternatives also exist. So how can you choose the right one?

Some helpful criteria.

The three most important criteria are: your environment, departmental resources, and the system supplier.

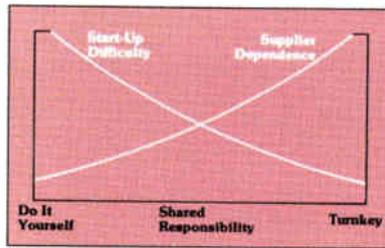
Production environment is critical. How high is the PC board volume? Are the boards extremely complex? How many new products are anticipated? For example, if you have fairly simple boards and few requirements for changes, a turnkey solution may be your answer. But for highly complex boards and a stream of new products, you may wish to keep expansion and revision control in-house. What about departmental resources? Do you have the technical people to assemble and program a do-it-yourself system?

Finally, the

system supplier should be evaluated. Does the company have knowledge of your business and applications engineers familiar with your needs? Will service and support personnel be available when and where you need them?

The concept of shared responsibility.

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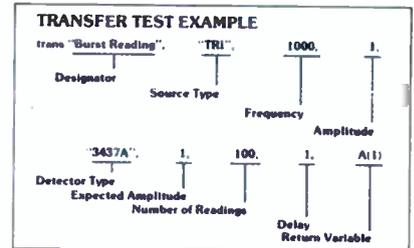
Program Generator (IPG) does the rest, selecting appropriate test methods, determining uncertainty, generating the test program and more.

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Cover: Executives see patches of gray among the blue, 119

The weather report looks good, say top executives of the electronics industries around the world in this, our annual Executive Outlook. Still, there are some clouds, primarily the economy, government activity and regulations, and the growing shortage of electronics engineers.

Cover photograph by Art Director Fred Sklenar.

Closing the circle for quality, 95

Prodded by the success of Japanese products on their home ground, U.S. companies are going after a key Japanese selling point: high quality. To do so, they are adopting Japanese methods, and one of the most noteworthy is Quality Circles, small groups of workers and supervisors who meet regularly to solve production problems.

Automated testing keeps up with RAMs, 132

In the fast-moving world of electronics, among the leaders of the pack in terms of speed, complexity, and demand is the random-access memory. But all that adds up to major problems for test engineers. This three-part series presents some of the latest automatic test solutions: a flexible system employing accurate, precise signals, for designers and high-volume users (p. 137); a tester that checks both RAMs and the logic that is usually employed with them, for those who use only a few parts (p. 137); and a manufacturer's system test program that ensures quality RAMs and frees purchasers of the parts from having to test them (p. 142).

Adapting Fortran to accept structured assignments, 150

Fortran, one of the most popular high-level languages, can be made to yield the well-known advantages of top-down structured programming, while still offering its own virtues of machine code efficiency, portability, and easiness to learn. In essence, subroutines are substituted for hierarchic blocks, and the use of jumps is eliminated.

Pascal enrolls for real-time system software, 157

Micro Concurrent Pascal brings the ease of high-level languages and the efficiency of assembly languages to the writing of microprocessor and microcomputer operating systems. By switching rapidly between program elements and assuming device driver functions, this derivative of Pascal copes with the real-time needs of multiple system tasks.

And in the next issue . . .

A low-cost fiber-optic data link . . . tape automated bonding: a special report . . . bipolar versus power MOS field-effect transistors . . . 16-bit single-chip microcomputers for high-performance control.

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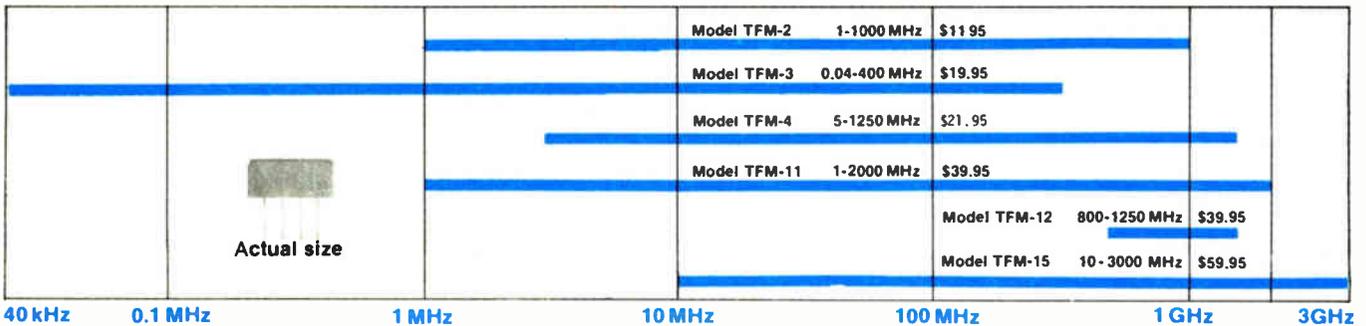
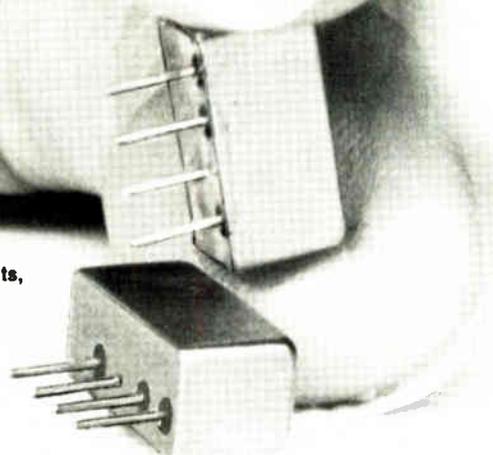
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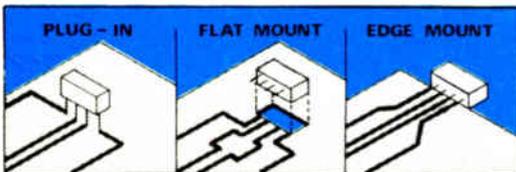
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| Model No. | LO | RF | IF | Typ. Max. | Typ. Max. | LO RF | LO IF | LO RF | LO IF | LO RF | LO IF | Quantity | Price | | | | | | | | |
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Publisher's letter

Twenty-two electronics industry leaders from the United States, Europe, and Japan participated in this year's Executive Outlook (p. 119) and it is interesting to note how alike their viewpoints now are.

Assistant managing editor Howard Wolff, who put together this report from interviews conducted by our reporters around the world, observes, "In recent years there has been more of a consensus over problems. Previously, opinions ranged all over the place."

For example, the concern over the short supply of electronics engineers voiced by Americans is shared by executives overseas. Even in Japan, where the schools are turning out large numbers of engineers, one company president fears a shortage. Top brass in both Japan and the U.S. see a chronic EE shortage as a major hindrance to research and development. Intel Corp.'s president Andrew Grove, for one, blames industry's failure to interest high school students.

There is also general concern over the state of the economy. French executives are just as worried as their American counterparts. Another common cause is impatience with government regulations and with lack of government support for R&D. A British manager decrying the decline of R&D spending sounds much like managers in the U.S.

But there are usually some unique national characteristics, Howard points out. This year, for instance, a West German chief executive sees a danger in a growing resistance to technology by workers. This anti-automation thinking harkens back to the Luddites of early 19th-century England, who destroyed labor-saving machinery to protect their jobs.

A worry that unites U.S. and European executives is trade with Japan. Says Howard, "Attitudes in America have mellowed a bit. Concern is still there, but some have backed off from the anger and fear expressed in previous years. Instead, American leaders have come to realize that they can compete with the Japanese and beat them at their own game, which is centered around

quality control. The argument about product quality differences seems to have abated."

One of the reasons that the quality issue has faded is that a number of U.S. companies have adopted the Japanese Quality Circle concept. In fact, the trend is something of a stampede, as the Inside the News story indicates (p. 95).

Needless to say, Japanese firms operating in the United States are also setting up Quality Circles—groups of employees who meet to analyze and help solve various production problems. Los Angeles bureau manager Larry Waller had a chance to visit some of their facilities here and to talk to employees.

"U.S. employees of Japanese companies can't say enough about how they like to work for these firms," Larry remarks. "I was also impressed by how candid the Japanese managers were. In that sense, they were more like Americans."

He observes that the U.S. companies setting up Quality Circles are aiming for faster results than the Japanese expect to gain. The Japanese managers caution that it takes time for the right frame of mind to set in, especially when translating subtle culturally based relationships from Japan to America.

"Yet the Quality Circle concept seems to touch an unmet need for an outlet—a means of participating in decisions and contributing to company operations," Larry concludes.

Ironically, quality control concepts that everyone now sees as part of the Japanese system were originally developed in the U.S. and exported to Japan in the late 1940s. It was there that participation in Quality Circles became voluntary and, like many new ideas introduced into Japan, grew into a major national movement.

Catch the Bus for Completely Automatic Distortion Measurement

Designers and ATE people requested it — a NEW distortion analyzer with IEEE-488 bus compatibility. Now Krohn-Hite responds with the first *totally* automatic instrument for measuring low distortion, voltage, and frequency.

Here's What "Completely Automatic" Means. The 6880 self-tunes to the frequency of an external signal over the entire range of 1 Hz to 110 kHz, so manual frequency tuning is unnecessary. Distortion, AC voltage, and frequency measurements can be made with input levels from 0.1 – 130 V RMS. And by eliminating operator functions, the 6880 cuts time and costs.

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Readers' comments

Waiting for standards

To the Editor: In the Packaging & Production Technology Update [Oct. 23, p. 222], the author wrote of Mostek's leadless chip-carrier that "not being square, this carrier does not conform to the standards for chip-carriers established by the Joint Electron Device Engineering Council," implying that the Mostek carrier does not conform to Jeduc standards. The fact is that there are no Jeduc standards for rectangular carriers. These are now being defined, and we are certain that when they are established, our rectangular carriers will conform to them.

Michael Honea
Mostek Corp.
Carrollton, Texas

Don't dump the dinosaur

To the Editor: I disagree with Henry G. Baker [Nov. 6, p. 8] that giving each university student a microcomputer is the best way to teach a first software course. The so-called dinosaur computers are useful not only for learning a language, but also for acquainting the student with the computer facility. Later the student can use it to program in many different languages and have access to many software packages (business, statistics, and so on). Most microcomputers are limited to one high-level language and an assembly language that does not give a register dump when a program fails. Also, by studying only microcomputers, one is just as likely to enter the "real world" designing more microcomputers with the architectural shortcomings of mainframe computers.

Steven Hunter
Cleveland, Ohio

Correction

A typographical error (Oct. 23, p. 294) gave the price of the Lasar Artmaster Generator from the Eocom division of American Hoechst Corp. as \$6,600 instead of \$660,000.

In the special report on automotive electronics (Nov. 20, p. 113), Trevor O. Jones' 1985 electronics market forecast was wrongly given as \$100 billion instead of \$10 billion.

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COHERENT and all of its associated software are written totally in the high-level programming language **C**. Using **C** as the primary implementation language yields a high degree of reliability, portability, and ease of modification with no noticeable performance penalty.

Features

COHERENT provides **C** language source compatibility with programs written to run under Seventh Edition UNIX, enabling the large base of software written to run under UNIX (from numerous sources) to be available to the **COHERENT** user. The system design is based on a number of fundamental concepts. Central to this design is the unified structure of i/o with respect to ordinary files, external devices, and interprocess communication (pipes). At the same time, a great deal of attention has been paid to system performance so that the machine's resources are used in the most efficient way. The major features of **COHERENT** include:

- multiuser and multi-tasking facilities,
- running processes in foreground and background,
- compatible mechanisms for file, device, and interprocess i/o facilities,
- the shell command interpreter—modifiable for particular applications,
- distributed file system with tree-structured, hierarchical design,
- pipes and multiplexed channels for interprocess communication,
- asynchronous software interrupts,
- generalized segmentation (shared data, writeable instruction spaces),
- ability to lock processes in memory for real-time applications,
- fast swapping with swap storage cache,
- minimal interrupt lockout time for real-

*UNIX is a trademark of Bell Labs

time applications.

- reliable power failure recovery facilities,
- fast disc accesses through disc buffer cache
- loadable device drivers.
- process timing, profiling and debugging trace features.

Software Tools

In addition to the standard commands for manipulating processes, files, and the like, in its initial release **COHERENT** will include the following major software components: **SHELL**, the command interpreter; **STDIO**, a portable, standard i/o library plus run-time support routines; **AS**, an assembler for the host machine; **CROSS**, a number of cross-assemblers for other machines with compatible object format with 'AS' above; **DB**, a symbolic debugger for **C**, Pascal, Fortran, and assembler; **ED**, a context-oriented text editor with regular expression patterns; **SED**, a stream editor (used in filters) fashioned after 'ED'; **GREP**, a pattern matching filter; **AWK**, a pattern scanning and processing language; **LEX**, a lexical analyzer generator; **YACC**, an advanced parser generator language; **NROFF**, an Nroff-compatible text formatter; **LEARN**, computer-aided instruction about computers; **DC**, a desk calculator; **QUOTA**, a package of accounting programs to control filespace and processor use; and **MAIL**, an electronic personal message system.

Of course, **COHERENT** will have an ever-expanding number of programming and language tools and basic commands in future releases.

Language Support

The realm of language support is one of the major strengths of **COHERENT**. The following language processors will be supported initially:

- **C** a portable compiler for the language **C**, including stricter type enforcement in the manner of LINT.
- **FORTRAN** portable compiler supporting the full ANS Fortran 77 standard.
- **PASCAL** portable implementation of the complete ISO standard Pascal.

- **XYBASIC**™ a state of the art Basic compiler with the interactive features of an interpreter.

The unified design philosophy underlying the implementation of these languages has contributed significantly to the ease of their portability. In particular, the existence of a generalized code generator is such that with a minimal effort (about one man-month) all of the above language processors can be made to run on a new machine. The net result is that the compilers running under **COHERENT** produce extremely tight code very closely rivaling that produced by an experienced assembler programmer. Finally, the unified coder and conformable calling sequences permit the intermixture of these languages in a single program.

Operating System

In part because of the language portability discussed above, and in part because of a substantial effort in achieving a greater degree of machine-independence in the design and implementation of the **COHERENT** operating system, only a small effort need be invested to port the whole system to a new machine. Because of this, an investment in **COHERENT** software is not tied to a single processor. Applications can move with the entire system to a new processor with about two man months of effort.

The initial version of **COHERENT** is available for the Digital Equipment Corporation PDP-11 computers with memory-mapping, such as the PDP 11/34. Machines which will be supported in the coming months are the Intel 8086, Zilog Z8000, and Motorola 68000. Machines for which ports are being considered are the DEC VAX 11/780 and the IBM 370, among others.

Because **COHERENT** has been developed independently, the pricing is exceptionally attractive. Of course **COHERENT** is completely supported by its developer. To get more information about **COHERENT** contact us today.



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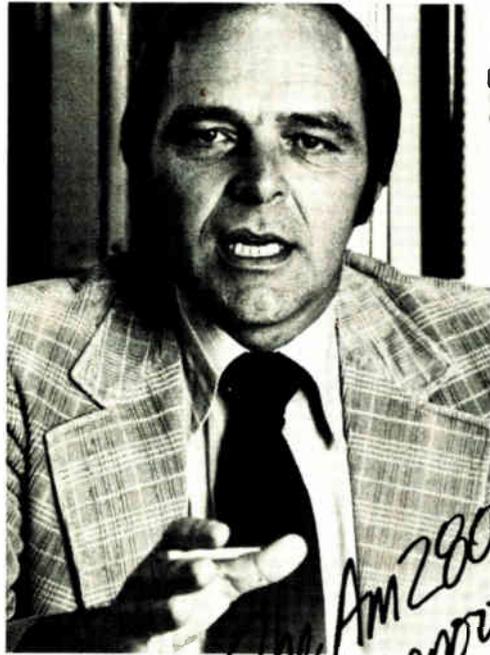
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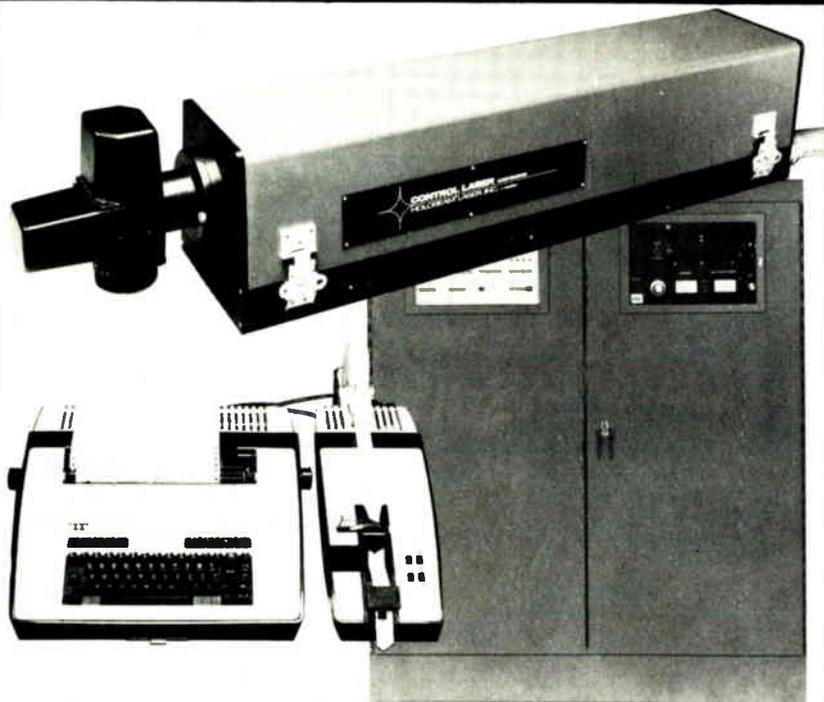
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News update

■ Toy makers and their retailers should have a very merry holiday season this year. Manufacturers' figures for overall sales are running about 12.5% ahead of last year's, with electronic games expected to account for \$500 million of the overall \$4.5 billion wholesale toy and game market for 1980.

Last year, electronic game sales were a quarter less, at \$375 million. One reason for this anticipated jump is that toy manufacturers have not experienced 1979's chip shortages [*Electronics*, Nov. 22, 1979, p. 96]. With integrated circuits now in ample supply, toy makers will not suffer from unfilled orders for parts and retailers should enjoy a brisk business.

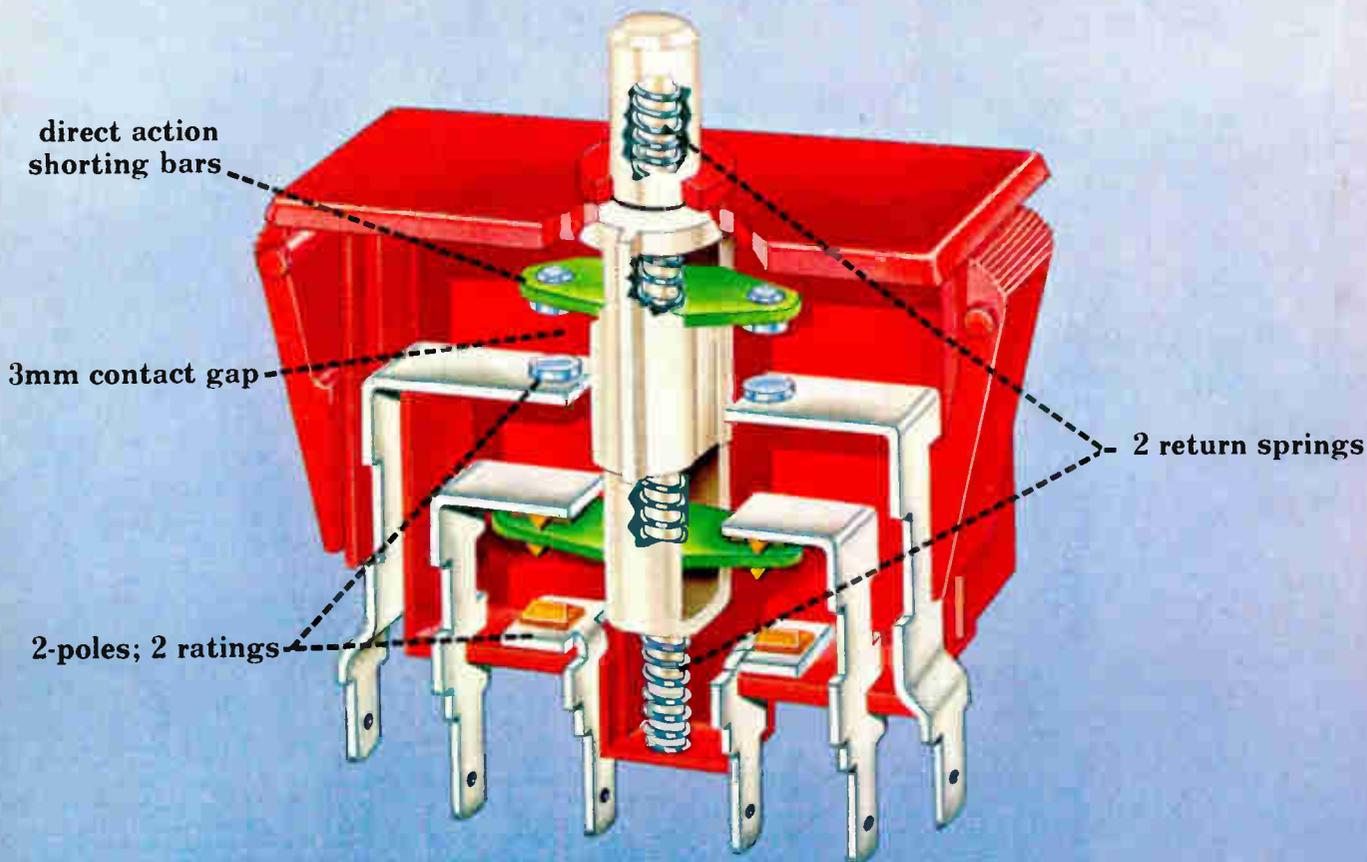
Good news. "Based on everything I've been able to observe, both here and overseas, I don't see any shortage of chips," reports Douglas Thomson, president of the Toy Manufacturers Association. "The [semiconductor] industry has matured enough to absorb these bumps." He cautions, however, that any custom parts used in a runaway bestseller could experience a shortage.

Doing their bit, semiconductor makers have added production capacity to meet a growing worldwide demand for parts, especially microcomputers and read-only memories. Recent slumps in automobile sales have also relieved the production pressure on IC manufacturers.

More. "We've added capacity," says a spokesman for Texas Instruments Inc. in Dallas. "Front ends have been brought on line for the TMS 1000 series." The TMS 1000 is a line of 4-bit processors that are mask-programmed according to software developed in this case by the toy makers, making it applicable to a multitude of electronic games.

A similar move was made at General Instrument Corp.'s Microelectronics division in Hicksville, N. Y., where adding capacity also meant upgrading its production facilities. Last year's shortage has encouraged the use of larger, 4-inch wafers and automated wafer-handling equipment to keep up with the rising demand for silicon. **-Gil Bassak**

LINE-INTERRUPT switch meets latest specs... WORLDWIDE



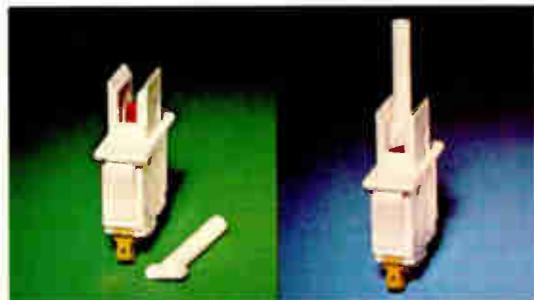
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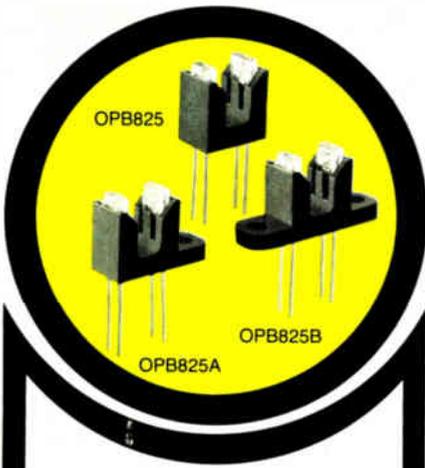
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People

Microcomputer nets attract Crook back to electronics

Once it gets into the blood, silicon fever is extremely difficult to shake. Colin Crook, a 38-year-old Englishman and managing director of a Zynar Ltd. in Uxbridge, England, has a chronic case of it. Two years ago he resigned as director of advanced systems and group operations manager at Motorola Semiconductor Inc.'s Austin, Texas, facility to return to the United Kingdom. There, as managing director of optical instrument maker Rank Precision Industries Ltd., he retained little direct involvement in semiconductor technology.

But on a visit to California's Silicon Valley he suffered a relapse. He met Harry J. Sall, president of little-known Nestar Systems Inc. of Palo Alto, Calif., and was immediately infected by Nestar's vision of marrying the personal computer and local networking technologies. Returning to England, the persuasive Crook sold Rank on the idea of taking a stake in Nestar and launching a venture capital spinoff company to exploit the software tools Nestar had developed. Crook also gave up his top managerial position with Rank to head the startup with a staff of less than a dozen.

Says Crook, "I met a group of engineers out there who I found were absolutely outstanding." All had worked on timesharing networks and now aimed to apply their software skills to microcomputer networks. Their first system, the Cluster/One model A, connects up to 65 Apple II computers in a local network configured as a straight bus, star, or tree.

Introduced in the second quarter of this year, the system is just the first arrow in Zynar's quiver, however, for Crook believes the microcomputer revolution has bred wide-ranging opportunities in software engineering and systems technology.

Zynar is now setting up a design and consultancy service for customers developing microprocessor-based products and will introduce new products of its own. Crook also



Back in harness. Colin Crook is eager to capitalize on what he considers a hot idea.

intends to rapidly build a software team at his Uxbridge headquarters to develop high-quality software that will fill a gap left by the chip suppliers and will sell in volume.

Bowen sees problem solving as automatic test target

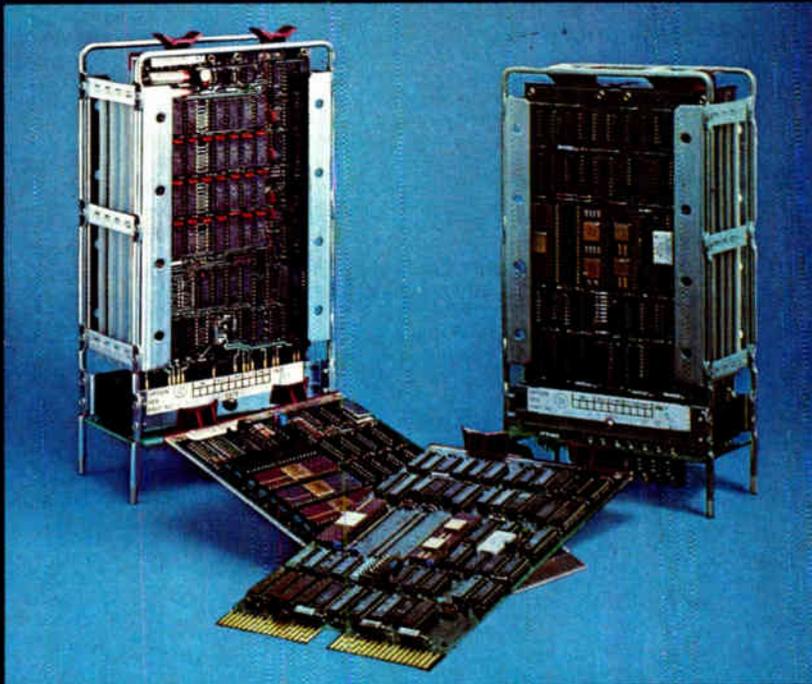
When James Bowen took on the job of vice president and general manager of Eaton Corp.'s Semiconductor Test Systems group five months ago, he brought to the position strong ideas on what the automated test business is not, as well as what it is. Those ideas, formed through his experience at Fairchild Camera & Instrument Corp.'s Xincom Test Systems group, have already begun to take Eaton's memory test system line in new directions.

Fairchild, Bowen believes, became preoccupied with the idea that automatic testing was nothing more than being in the computer business. "I decided that was the wrong way to go," he says self-assuredly.

The 52-year-old native of Chicago contends that "you could get into the ATE business without building any hardware." The various parts of a test system are typically built elsewhere for assembly. "So really, the ATE business is understanding the problem that testing entails and solving that problem," he says.

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People

total solutions," he insists. The initial step in that direction is the Detective series, unveiled last month at the Institute of Electrical and Electronics Engineers' Annual Test Conference in Philadelphia [*Electronics*, Nov. 6, p. 89]. The series also tackles the problems of production costs and programming for memory testing and includes some products made by the Woodland Hills, Calif., group when it was still the Macrodata Corp.

The systems are aimed at wooing away some customers from the dominant memory test company, Teradyne Inc. Bowen believes that that company's latest introduction, the J389 test system, is more powerful and expensive than necessary. "I think what Teradyne has done is to build a Concorde," he says wryly.

Tougher challenges. In going for the total solution, Bowen's next step will probably be one that addresses the thrust of electronics into wider, more demanding markets like the automotive one. For instance, he says, "we're looking at environmental testing, at combining the oven with the test system for testing at higher temperatures."

He will also concentrate on devising better ways of moving parts through production and interfacing them to the test system. "Parts are down to test times of about a minute or so—they spend much more time being handled by people," he notes.

One thing that probably won't be part of Bowen's solution, however, is a system with modules that can be swapped out to meet the needs of technological advances. While he admits that the idea is great in theory, "users would have to pay quite a price for it. I believe a dedicated system will prove to be the most economical solution."

While his group's thrust will remain in the area of memory component and board testing, Bowen is keenly aware of the addition of more digital logic to memory boards. When he is eventually forced to add logic testing to his systems, Eaton will likely continue its march into technology by acquiring a small ATE house already in logic testing. □

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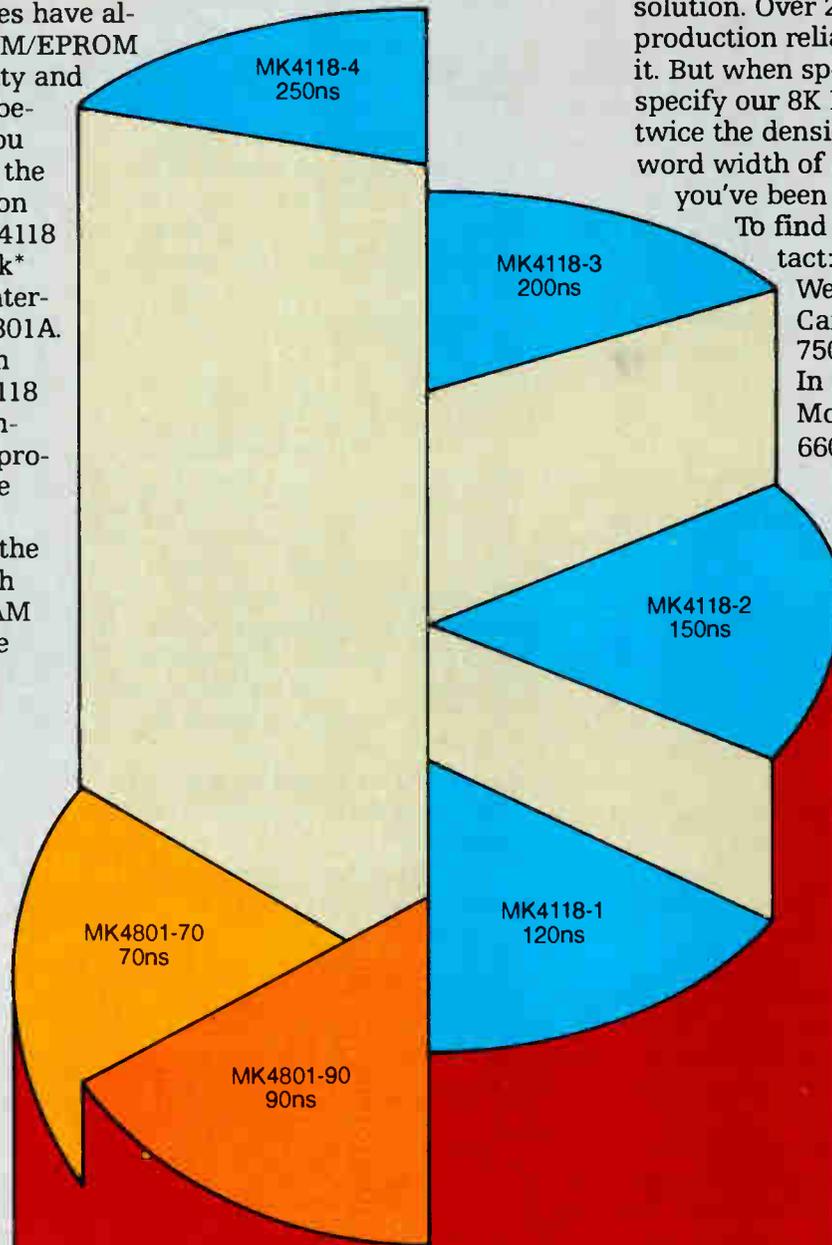
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TMOS. Real technology from the SuperPower.[™]

TMOS is an advanced, Motorola version of double-diffused, vertical-structured, silicon-gate MOS. The critical, N-conducting channel length is determined by an easy-to-control, ion implant/diffusion process achieving high yield, good reliability, high breakdown voltages and better conductance per unit area.

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The unique process overcomes many of the top surface disadvantages of planar: long channel length, low transconductance,

mask layout problems, cooling, capacitance and breakdown complications. TMOS also outshines V-structured FETs by immunity from breakdown of gate oxide around the V-groove tip.

TMOS. Genuine production and availability.

Volume production of TMOS requires the marriage of two distinct capabilities. First, the MOS wafer processing requires the complexity of large area MOS ICs. Second, power technology is necessary from wafer metallization through package assembly and testing.

Motorola has command of both areas.

Major investments have been made in wafer facilities completely separate from bipolar. These include the latest equipment and processes employed for our in-house expertise in ICs. Computer-aided design and process simulation... automated wafer handling... projection print lithography... ion-implantation... MPU-controlled diffusion and metallization... polysilicon, low-pressure chemical vapor deposition.

Initial wafer production will have an annual capacity of millions of units.

When we say we've got them, we've got them.

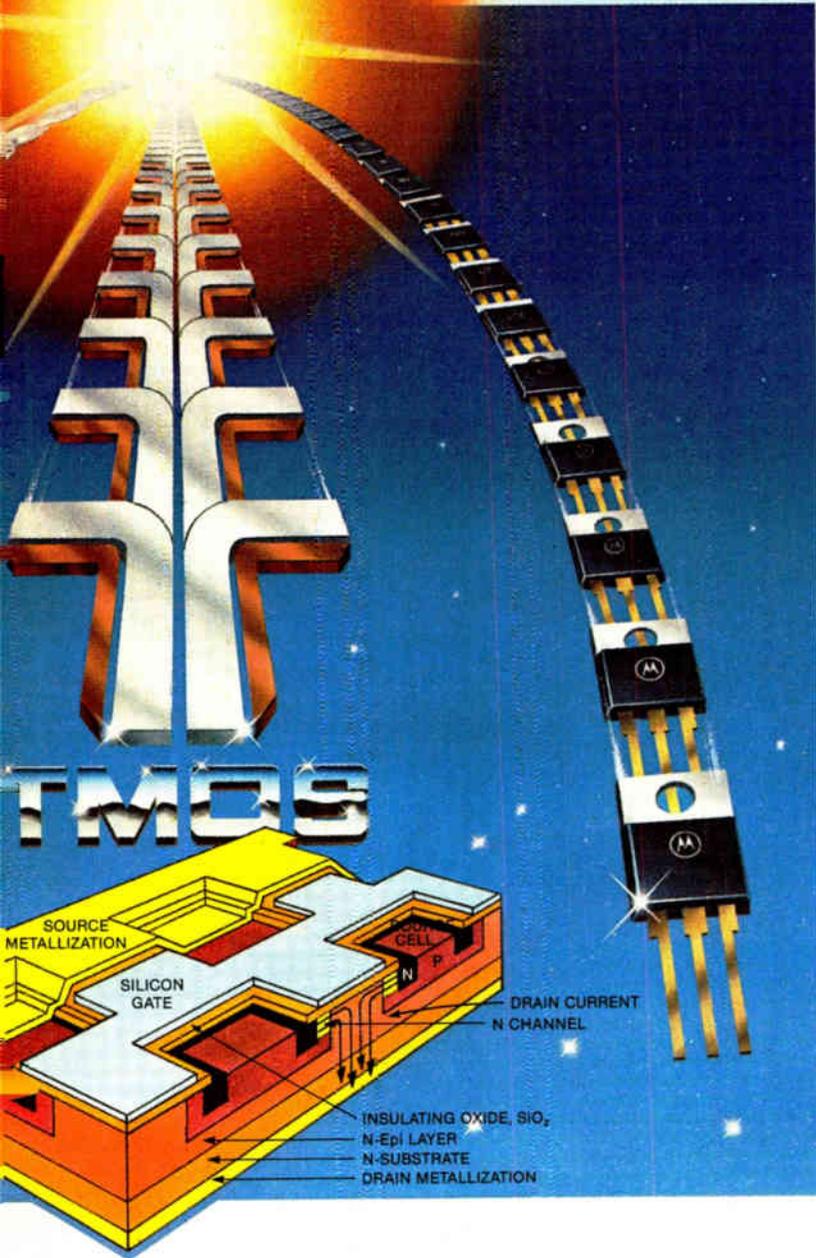
TMOS. Authentic SOA to 500 V.

Bipolar breakdown from current hogging or very high current operation, particularly during reverse-biased turn-off with an inductive load, doesn't trouble TMOS. These power FETs are inherently less susceptible to secondary breakdown due to positive TC of $r_{DS(on)}$. They like to shut down when overloaded.

And, with the introduction of its MTM/MTP-series, Motorola offers high BV_{DSS}/SOA ratings—up to 500 V. You can operate an MTM475 or MTP475 directly from ac lines with a bigger edge in



power FETs in volume. now in production.



ity or any of the above. TMOS fits almost anywhere: power supplies, inverters, amplifiers, motor controllers, regulators, servo amps, line drivers, choppers and logic buffers, to name a few. Anywhere bipolar's done such a tremendously valid job for years.

We've prepared a brochure to help you decide where this technology's best for you. Contact Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.

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|------------------------|----------------------------|---------|---------|--|-------------------------|-------------------|
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| 4 | 400 | MTM474 | MTP474 | 2.25 (1.5 typ) | 75 | \$8.50 |
| | 500 | MTM475 | MTP475 | | | \$9.75 |
| 5 | 350 | MTM564 | MTP564 | 1.50 (1.0 typ) | 75 | \$8.50 |
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| 12 | 60 | MTM1224 | MTP1224 | 0.25 (0.15 typ) | 75 | \$8.50 |
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TMOS. The industry made it necessary. Technology made it possible. Motorola makes it real for your

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safety when calculating peak line voltages of 185 V or more or guardbanding against stray inductive surges.

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Zehntel announces three new advancements for the industry's most production-minded in-circuit tester.

New! THE PRODUCER™ reduces programming time and costs.

In a few days or even a few hours, you can generate complex test programs that might take weeks or months with other testers. An extensive test template library lets you produce an entire digital/analog test program by simply calling up test elements stored in memory.

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New! DATA DIRECTOR™ simplifies complex LSI testing.

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TEST COMPLETE...
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TROUBLESHOOTER 800

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combined with today's most sophisticated in-circuit test technology. For full details, send for our TROUBLESHOOTER 800 brochure, or call Plantronics/Zehntel, 2625 Shadelands Drive, Walnut Creek, CA 94598, (415) 932-6900.



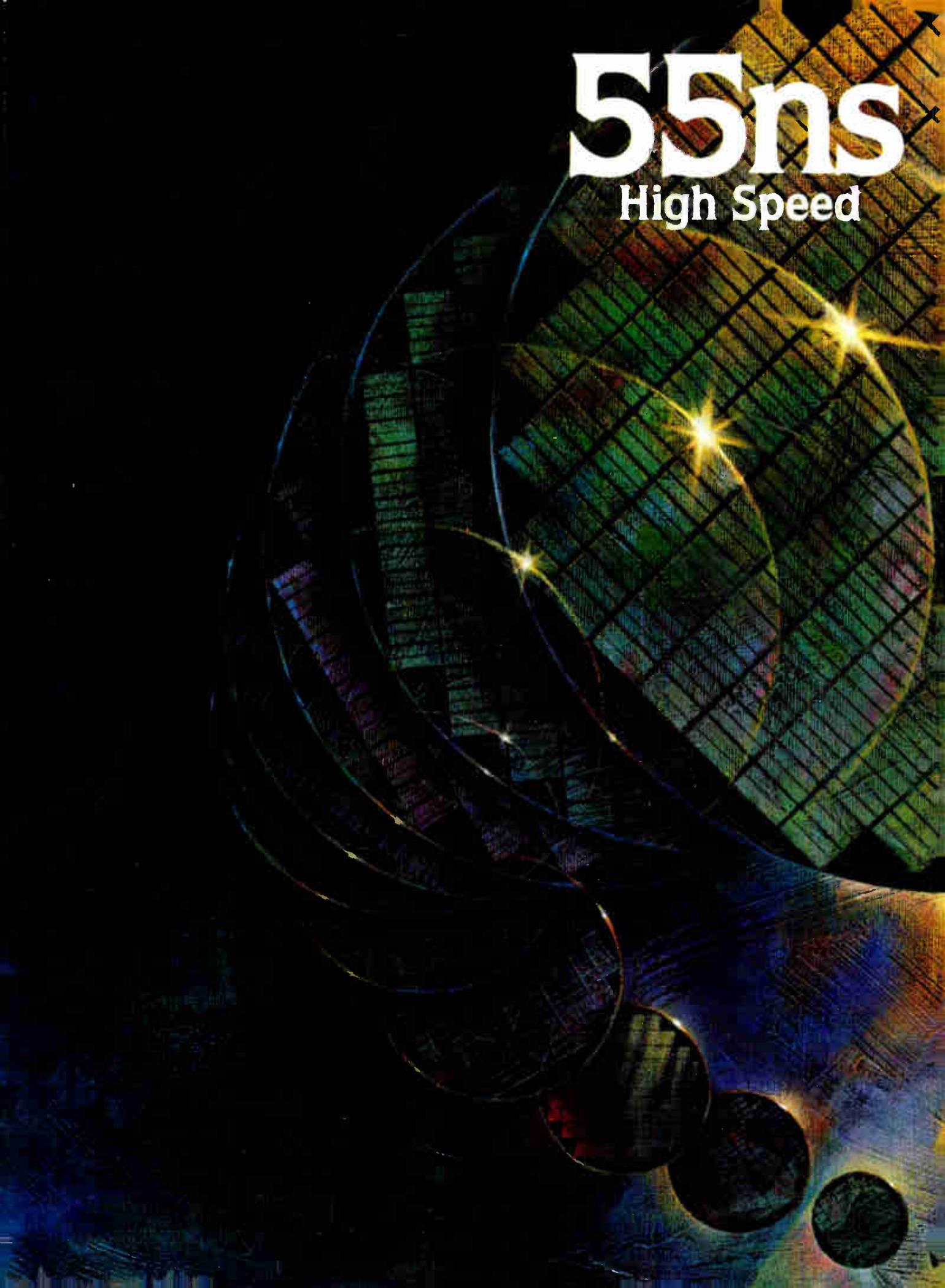
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Circle 23 on reader service card

The name of the game is quality

Last April, the U. S. semiconductor industry was embarrassed to learn that important customers were finding some Japanese memory products equal in performance and superior in quality to their own [*Electronics*, April 10, p. 81]. Considerable undercapacity then existed, and the Japanese had seized the chance to parlay their devices' high quality and availability into a significant share in the 16-K MOS random-access memory market; now they are poised to enter the emerging 64-K market with highly competitive products.

Originally, several semiconductor manufacturers denied that there was any significant difference between U. S. and Japanese quality and accused the Japanese industry of unfair tactics based on a government-industry partnership that gave them an edge in absorbing the cost of quality. At the time, we decried such rationalizations. "The U. S. semiconductor industry will put to rest the quality issue, because it must," we said then. And we suggested that, despite differences in culture and philosophy, we ought to learn something from the Japanese and use it to solve the problem.

Making it clear to the IEEE

The Institute of Electrical and Electronics Engineers has clearly received a mandate to listen more closely to its members and incorporate their views into any position it may wish to take. According to the latest member opinion survey conducted by the institute's U. S. Activities Board, 69.1% of the members want to be polled on a regular basis to provide guidance to IEEE's leadership (see p. 232).

Pointedly, only half of the members who responded believe that the IEEE often takes the views of the general membership into

Since then, numerous companies have done just that. As we report in this issue (p. 95), many U. S. firms have adopted Japanese Quality Circle methods for involving production workers more closely in upgrading product quality, and others are considering using them. Major semiconductor firms such as Advanced Micro Devices, National Semiconductor, Intel, Motorola, and Texas Instruments are putting a big effort into improving product quality.

And those efforts are beginning to pay off. Richard Anderson of Hewlett-Packard—the source of the original bad news about U. S. quality—recently reported that, although a gap still exists, American semiconductor quality has improved significantly [*Electronics*, Nov. 6, p. 46]. Though there is still a way to go, if the announced goals of the semiconductor companies are achieved by next year, quality will no longer be a "red herring" to divert the U. S. industry from the innovative efforts that have carried it to world dominance. As we said, we should be grateful to the Japanese for reminding us so forcibly of the importance of quality.

account when developing and carrying out programs meant for the members. Even more lamentable is the fact that only one third thinks that the IEEE listens to the thoughts of the general membership when making public statements or taking public positions. The polled members do agree the IEEE should take stands on controversial issues—overwhelmingly so. After all, the IEEE does have a base from which to speak, and it should take stands where the consequences of social, political, and economic issues merit a unified electrical engineering voice.

"We built these two new counters for design engineers like us"

You'd expect our engineers to be biased in favor of our new counters. But when we challenged them, they quickly pointed out why they're becoming favorites of design engineers everywhere.
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represent the best combination of counter performance, pricing and packaging that a design engineer could want. Both incorporate Fluke-designed thick-film hybrid circuits for excellent sensitivity and flat response. Stainless steel RFI

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| Model | Resolution | Max. Sensitivity | Price |
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| 7260A | 100 ns | 10 mV | * \$895 |
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"Fluke's exclusive portable test instrument (PTI) packaging design lets us stack and latch multiple instruments on top of our counters. And by using the new Fluke 1120A Translator, we can assemble an inexpensive IEEE-488 system."

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Our engineers are sold on our new counters. How about you? For more information call toll free 800-426-0361; use the coupon below; or contact your Fluke sales office or representative.

*U.S. prices only.



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Meetings

1981 International Consumer Electronics Show, EIA (CES, 2 Illinois Center, Suite 1607, 233 N. Michigan Ave., Chicago, Ill. 60601), Las Vegas Convention Center, Las Vegas, Nev., Jan. 8-11.

PTC '81—Pacific Telecommunications Conference, Pacific Telecommunications Council (PTC '81 Director, 2424 Maile Way, Rm. 704, Honolulu, Hawaii 96822), Ilikai Hotel, Honolulu, Jan. 12-14.

National Radio Science Meeting, IEEE and U.S. National Committee for the International Union of Radio Science (URSI), University of Colorado, Boulder, Jan. 12-15.

AVEC 81—Seventh International Audiovisual and Communications Salon, Société pour la Diffusion des Sciences et des Arts (20 rue Hamelin, 751 16 Paris, France), Palais des Congrès, Paris, Jan. 12-17.

High Speed Digital Technologies Conference, IEEE Electron Device Society and American Vacuum Society, San Diego Hilton Hotel, San Diego, Calif., Jan. 13-15.

Southcon/81 Show and Convention, IEEE, Georgia World Congress Center and Omni International Hotel, Atlanta, Jan. 13-15.

Automatic Test Equipment Seminar-Exhibit, Benwill Publishing Corp. (Test Conference Registrar, 1050 Commonwealth Ave., Boston, Mass. 02215), Pasadena Center, Pasadena, Calif., Jan. 19-22.

Eighth Plating in the Electronics Industry Symposium, American Electroplating Society (1201 Louisiana Ave., Winter Park, Fla. 32789), Adams Hotel, Phoenix, Ariz., Jan. 20-21.

Annual Reliability and Maintainability Symposium, IEEE Reliability Society, American Society for Quality Control, American Institute of Aeronautics and Astronautics, et al., Marriott Motor Hotel, Philadelphia, Jan. 27-29.

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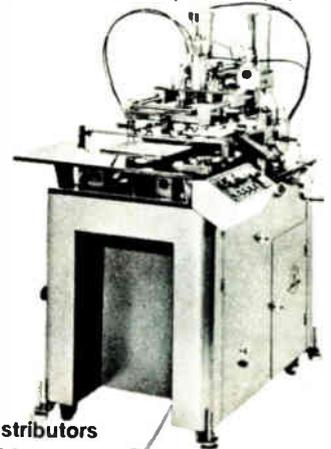
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“What if we...”

What if we built a versatile new 5½-digit multimeter that you could expand into a fully-programmable measurement system?

You'd call it an excellent value, and wonder why nobody thought of it before. Our product designers call it the Fluke 8860A Digital Multimeter, an excellent new 5½-digit DMM that easily becomes either a programmable benchtop

system or a powerful **IEEE-488** instrument.

A powerful benchtop DMM.

As a precision DMM, the 8860A is an excellent value: a practical, hard-working voltmeter with 0.01% basic dc accuracy, five functions,

autoranging, and four advanced math functions - offset, peak-to-peak, limits testing and dc and ohms zero. All in a portable package.

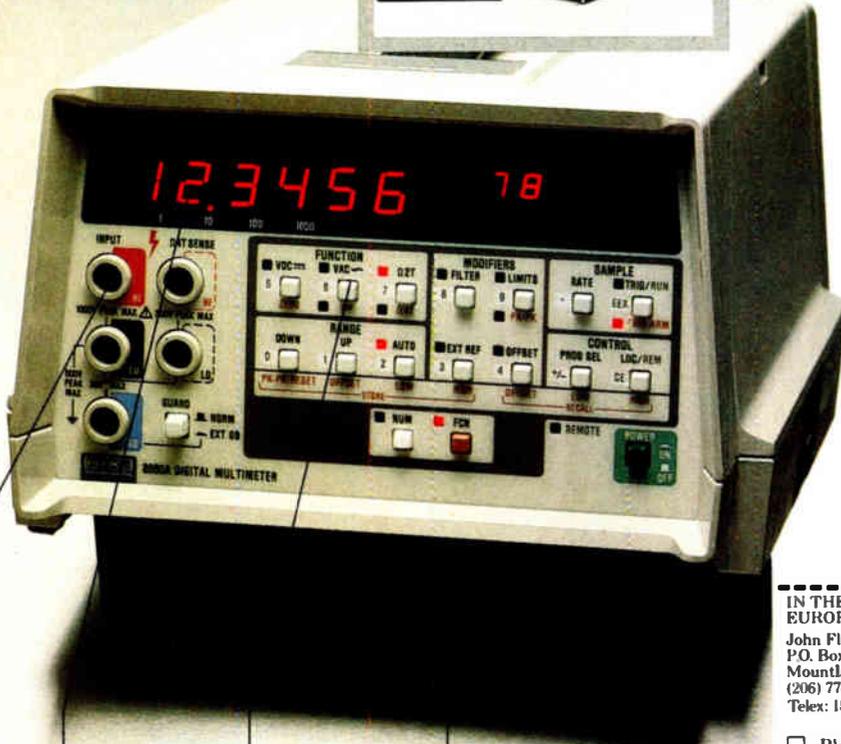
A stand-alone multimeter system.

To make your 8860A fully programmable, we offer an optional calculating controller that ties the program execution capabilities of an RPN scientific calculator to the analog measurement power of the precision DMM. This allows you to develop software for your specific application. To integrate the 8860A into a larger system, we also offer an inexpensive talk/listen IEEE-488 interface for use with an IEEE instrument controller.

“Tell me more!”

Any way you configure your new 8860A DMM, you'll streamline your applications today and leave the door open for new opportunities tomorrow. For more information, call toll free 800-426-0361; use the coupon below; or contact your Fluke sales office or representative.

“We designed the 8860A to be a powerful, accurate multimeter, with low-cost options that make it fully programmable. This kind of flexibility makes the 8860A a practical solution for a wide range of measurement needs.”



Input protection to 1000V; safety design uses recessed input jacks and eliminates four-terminal ohms and guard shorting links.

5½-digit resolution with function annunciators.

Five-function DMM features autoranging, four advanced math functions and 0.01% basic dc accuracy.

Exclusive Portable Test Instrument Packaging lets you stack-and-latch the 8860A with other Fluke PTI Instruments.

Excellent value in an easy-to-operate DMM. The basic 8860A is \$1395; add \$295 for the IEEE-488 interface, or \$550 for the calculating controller.

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For technical data circle no. 27

Fluke introduces two new advanced synthesized signal generators you

With 20 years experience in RF instrumentation, we're driving down the cost of high performance.

The 6070A and 6071A are designed to fill a critical gap in today's signal generator market: the price/performance gap that separates \$10,000 synthesizers with limited capabilities from the more sophisticated, state-of-the-art units costing \$25,000 and up. As such, they represent a new generation of RF synthesizers from Fluke that deliver the industry's

most-wanted features at a very affordable price.

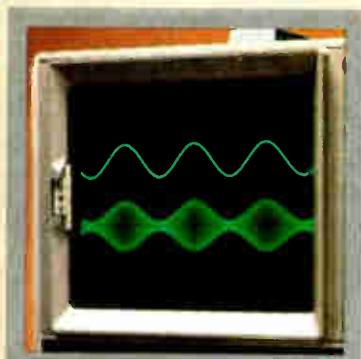
Innovative design achieves signal purity and broad frequency coverage.

Fluke engineers developed a number of unique and cost-effective synthesis techniques for the 6070A and 6071A that deliver a high degree of spectral purity without sacrificing broadband range.

The frequency range of the 6070A is 200 kHz to 520 MHz and the 6071A extends the range to 1040 MHz. Yet both

instruments have spurious output levels of 90 to 100 dB below carrier, performance equalling or exceeding the best cavity-tuned generators on the market today. Microprocessor control — which Fluke introduced to signal generator design in 1975 with the 6010A — allows precision resolution and settability you can't find from any other manufacturer.

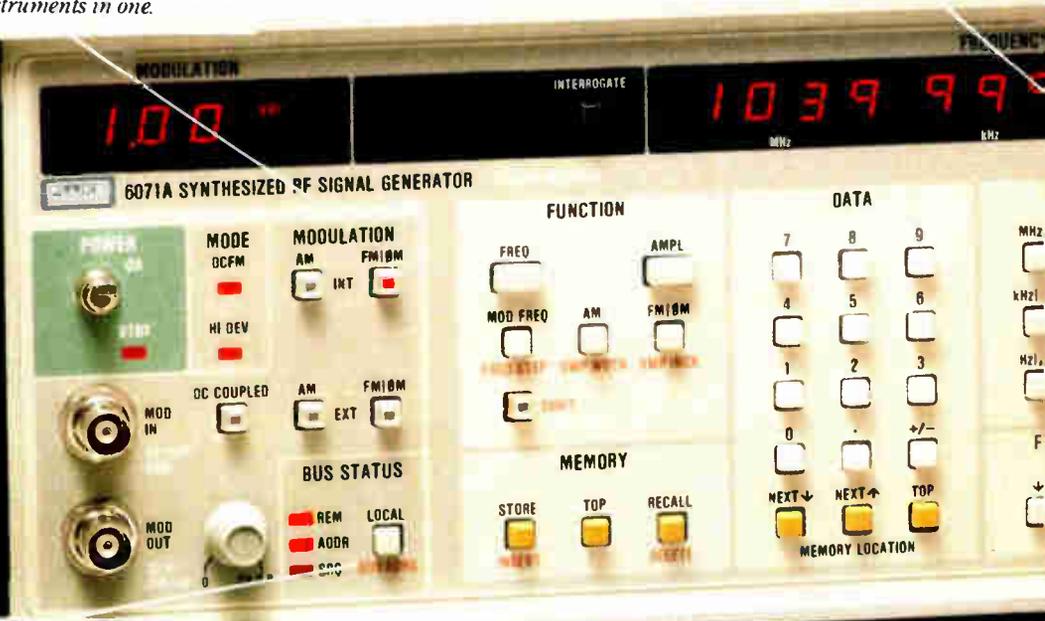
Fluke's new approach to synthesis in the 6070A and 6071A combines several unique elements: a refined single loop de-



Internal modulation is fully programmable from 20 Hz to 200 kHz with 3 digits resolution. The generators can also function simultaneously as signal generators and independent audio oscillators — two instruments in one.



Pinpoint frequency tuning provided by optically coupled, magnetically detented spin knob. Combines digital precision with the speed and convenience of analog control.



Built-in, easy-to-program IEEE-488 interface ties the signal generator capability of the instruments to the power of automated system control. Talk/Listen capability provides "learn" and "teach" modes



Output level adjustable in 0.1 dB steps from +19 dBm (13 dBm above 520 MHz) to -140 dBm — displayed in dBm or volts and in relative or absolute units.



Advanced technology can specify with confidence.

design that both improves reliability and lowers maintenance costs; a Surface Acoustic Wave (SAW) device to achieve low noise performance; and a delay line discriminator in a phase-locked loop that improves spectral purity and increases the modulation flexibility of the instruments.

A major emphasis on packaging design minimizes RF leakage and insures spectral purity. Fluke's own thick film hybrids improve RF performance and keep the parts count low. And a high

efficiency power supply helps reduce weight, volume and heat rise.

Versatile modulation brings you two instruments for the price of one.

AM, FM and θ M are internally selectable. Modulation frequencies from 20 Hz to 200 kHz can be selected. Modulation can be applied separately or simultaneously for frequency, amplitude or phase, and the internal signal can also be used as an independent signal source, separate from the RF output, giving the user two

instruments — a signal generator and an audio oscillator — in one high performance package.

A high deviation mode of up to 1 MHz or 100 radians is provided for frequency of phase modulation. External dc coupling for AM and FM is also available.

More microprocessor benefits.

The advanced 16-bit microprocessor control of the 6070A and 6071A makes these signal generators easy to operate and a pleasure to use.

Complex functions are executed rapidly from simple, direct keyboard commands.

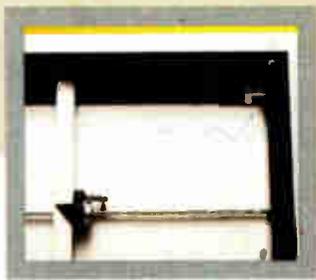
A remarkably fluid-feeling spin knob gives even greater precision and control by allowing you to tune around any frequency, amplitude or modulation parameter, or spin quickly to another setting: rapid-tuning convenience with digital precision.

A built-in memory for storage of front panel set-ups is provided to save time and reduce operator errors. And the 6070A and 6071A also include a relative units function that allows you to define a zero point for subsequent programming, useful in both the frequency and amplitude domains.

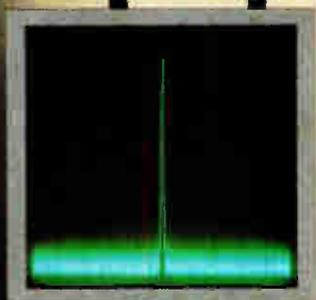
Both instruments are IEEE-488 programmable for complete system use. Plus self-diagnostics, error code displays, digital sweep and other special functions combine to simplify testing in any RF design application. A full line of options and accessories is available to expand the capabilities of the 6070A and 6071A.

For more information on these new signal generators, call toll free 800-426-0361, use the coupon below or contact your nearest Fluke sales office.

Digital frequency sweep for sophisticated testing of narrowband crystal filters, wideband amplifiers and other devices: manual, single and auto modes are standard.



Noise performance exceeds the cavity-tuned generators: SSB phase noise -138 dBc/Hz at 20 kHz offset from the carrier at 500 MHz broadband noise floor -150 dBc/Hz.



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8086 Strike Force

Intel announces the M8086, the most powerful 16-bit military microprocessor available today.

Intel's new M8086 now gives designers the architectural base to launch an attack on previously inaccessible military applications. Offering up to an order of magnitude higher performance than previous devices, the M8086 is the most powerful 16-bit military microprocessor available today.

But just as importantly, Intel also offers the M8086-compatible support components and development tools you need to build complex VLSI systems for military applications. Components such as those shown in the table. Plus the industry's most complete array of hardware/software support tools. That's the system solution you need to deliver your military products—hitting time, budget and performance targets precisely. That's the 8086 Strike Force.

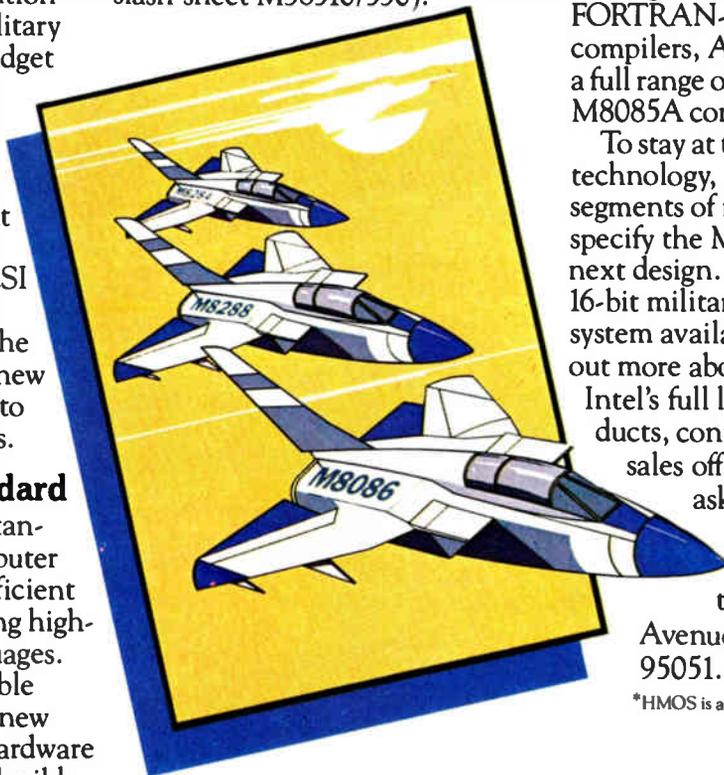
Proving once again that Intel puts military equipment manufacturers in command of the latest advances in VLSI technology. From our JAN-approved 8080A, through the M8085 and M8048, to the new M8086: Intel is committed to delivering military solutions.

The new military standard

The M8086 sets a new standard for military microcomputer applications. With super-efficient architecture for implementing high-level block-structured languages. A full megabyte of addressable memory space. A powerful new instruction set, including hardware Multiply and Divide. Plus flexible system configurability through the Multibus™ interface. All of which makes it possible to use the M8086 in applications that used to require multiple-chip CPUs, such as bit-slice designs and mini-computers. And because Intel designs M8086 systems for future

expansion, you'll be able to take advantage of further enhancements—such as co-processors and IO processors—as military versions become available.

The HMOS* process M8086 and support components are ready today to be drafted into your hi-rel military systems. All components conform to Class B standards of MIL-STD-883B, Method 5004, while meeting all military inspection criteria and lot conformance testing requirements of Method 5005. Furthermore, the M8086 family has been selected for military standardization under the MIL-M-38510 program (JAN slash sheet M38510/530).



Getting your products off the ground

You can begin designing your next generation of 16-bit military microcomputer systems today, using Intel's total hardware/software support tools. Hardware support such as the Intellec® Series III

| The M8086 Family (Class B, MIL-STD-883B T _A : -55° to 125°C) | |
|--|---|
| Microprocessor/Support Components | |
| M8086 | Microprocessor |
| M8282/3 | Octal Latches |
| M8284 | Clock Generator and Driver |
| M8286/7 | Octal Transceivers |
| M8288 | Bus Controller |
| Standard Memories | |
| M2114A | 4K Static RAM (1K x 4) |
| M2148H | 4K Static RAM (1K x 4) |
| M2147H | 4K Static RAM (4K x 1) |
| M2118 | 16K Dynamic RAM (16K x 1) T _A : -55° to 85°C |
| M2716 | 16K EPROM (2K x 8) |
| M2732 | 32K EPROM (4K x 8) |
| M3636 | 16K Bipolar PROM (2K x 8) |
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| M8251A | USART |
| M8253 | Counter/Timer |
| M8255A | Programmable Peripheral Interface |
| M8259A | Interrupt Controller |

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Electronics newsletter

Bell researchers claim GaAs speed with silicon parts

The hottest news at next week's International Electron Devices Meeting in Washington, D. C., may well be that silicon can compete very effectively with gallium arsenide in the processing of high-speed integrated circuits. Researchers at American Telephone & Telegraph Corp.'s Bell Laboratories in Murray Hill, N. J., have succeeded in producing an MOS ring oscillator with 1- μ m line widths that will operate at 40 ps. They have also devised a 2.5-GHz divide-by-8 counter. Plans are to take this technology into the large-scale and very large-scale integration arenas for memories and logic as soon as possible.

Honeywell offers 32-bit superminis 16 bits at a time . . .

Taking a different approach to the 32-bit superminicomputer market, Honeywell Information Systems Inc. is about to introduce its new DPS-6 16-bit computers, several of which can be upgraded by users to 32-bit machines. Evolved from the Waltham, Mass., firm's Level 6 computers, **the 10 DPS-6 machines offer two to three times the throughput of their Level 6 counterparts at about the same price.** In their 32-bit configurations, the new machines' rated performance is said to exceed that of Digital Equipment Corp.'s VAX-11/780, and "in Cobol, there's no contest," according to insiders. The DPS-6 series spans a broad range of characteristics, offering from 128-K bytes to as much as 16 megabytes of main memory, up to a gigabyte of disk storage, the ability to serve up to 64 communications lines, and full hardware and software compatibility with Honeywell's existing Level 6 systems.

. . . as it enters office automation with new machines

Using its new DPS-6 computers, Honeywell Information Systems is moving quickly into the office automation field. The Administrative System 4, based on the 16-bit DPS-630 or -632, will offer four work stations, two printers, and up to 26 megabytes of disk storage. The Administrative System 16, using the DPS-638 or -648, will manage 16 work stations, six printers, and up to a gigabyte of disk storage. **Both systems will combine word and data processing with electronic mail and other office-of-the-future features.** The company also plans to introduce two models in its new WP-6 word-processing family. Its key feature: it can tap data files for inclusion in word-processed documents.

Codec, filters combined on chip at Bell Labs

Continuing efforts to reduce the cost of per-line signal processing, Bell Laboratories engineers at Murray Hill, N. J., have integrated onto a single chip a charge-redistribution codec and associated filter functions. The complementary-MOS chip containing the codec, filters, and trimmed voltage references **requires only a few nonprecision off-chip capacitors.** The power dissipation of the complete function is 60 mW, which reduces the operating costs of the line interface. Samples of the new device, to be described in February at the International Solid State Circuits Conference in New York, are now being used within the Bell System.

Computer-controlled laser printer coming from HP

Hewlett-Packard Co. of Palo Alto, Calif., will take the wrapping off a new computer-controlled laser printing system this week. Developed by HP's Boise (Idaho) division, the laser printer is said to be able to print reports **directly from the computer, on letter-size paper, at the rate of nearly one copy per second.**

High-temperature parts to explore atmosphere of Venus

The National Aeronautics and Space Administration's projected 1984 orbiting imaging radar mission to Venus may carry instrumentation to measure atmosphere conditions. Encouraged by recent developments in a circuitry for high operating temperatures [*Electronics*, Aug. 14, p. 41], a design team at the Jet Propulsion Laboratory in Pasadena, Calif., is working on an instrumentation package able to withstand the 325°C temperatures 18 km above the planet's surface. As part of an experiment designed by France's space agency, the package would ride on balloons released from the probe module. Already in development or screening are a 915-MHZ microwave oscillator from General Electric Co.'s Microwave Tubes division; a high-stability pulser/modulator from Quartex Inc.; a 6-to-1,000-v transformer from General Magnetics Inc.; and analog switches from Harris Corp.'s Semiconductor Products division.

Standard Interfaces give many options for data systems

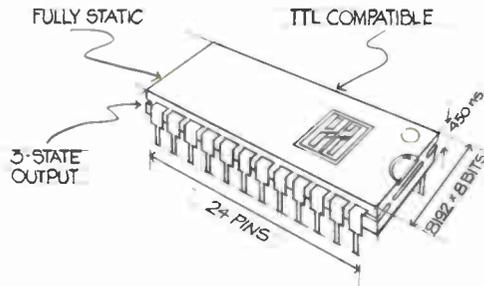
Crydom division of International Rectifier Co. is entering a new business with a line of standard interface parts that can be configured into many distributed data and control systems. Up to 127 microprocessor-controlled stations along a mile of cable can manage more than 2,000 data points at half the cost of custom networks, say officials of the El Segundo, Calif., division. Interface boards in each station monitor up to eight pieces of power equipment (motors, actuators, and so on) and multichannel instruments and controls. With commands stored in read-only memory, each station also can function as a stand-alone processor. Evaluation hardware for RIOS (remote input/output systems) will be available next month for \$1,249.

Dial-up CATV program selector foreseen for 1980s

A digital video switching system that can sit atop a television set and allow viewers to call up individual programs should become available before decade's end. That's the word from David Hardwick, vice president of marketing and planning at Valtec Corp., West Boylston, Mass. He says such an approach is what is needed for rapid growth of the cable TV industry. Selection now is limited to what comes into the house over the 60 or so channels that are available, but with a telephone-like push-button system the viewer would be able to choose via fiber-optic cables from hundreds of selections available at a central office.

Hand-held calculators could save Air Force \$40 million in fuel

Some 4,000 hand-held calculators soon will be helping the Air Force to save up to \$40 million yearly in fuel costs, and at a price less than a tenth that of on-board fuel management computers. Under the Aeronautical Systems division's Simplified Fuel Management System program, modified programmable printing calculators with aircraft characteristics encoded in read-only memory would accept real-time data; they would then print out the combination of altitude, air speed, and engine management for minimum fuel use. The whole effort, including the calculators and digitization of the flight characteristics of the C-141, C-5A, B-52, and KC-135, is expected to cost about \$1.3 million. SFMS thus could begin to pay for itself in less than a month. The digitized flight characteristics will be delivered in January by Infotec Development Inc., Huntington Beach, Calif.; the calculators, probably from Texas Instruments Inc. or Hewlett-Packard Co., should be delivered in August.



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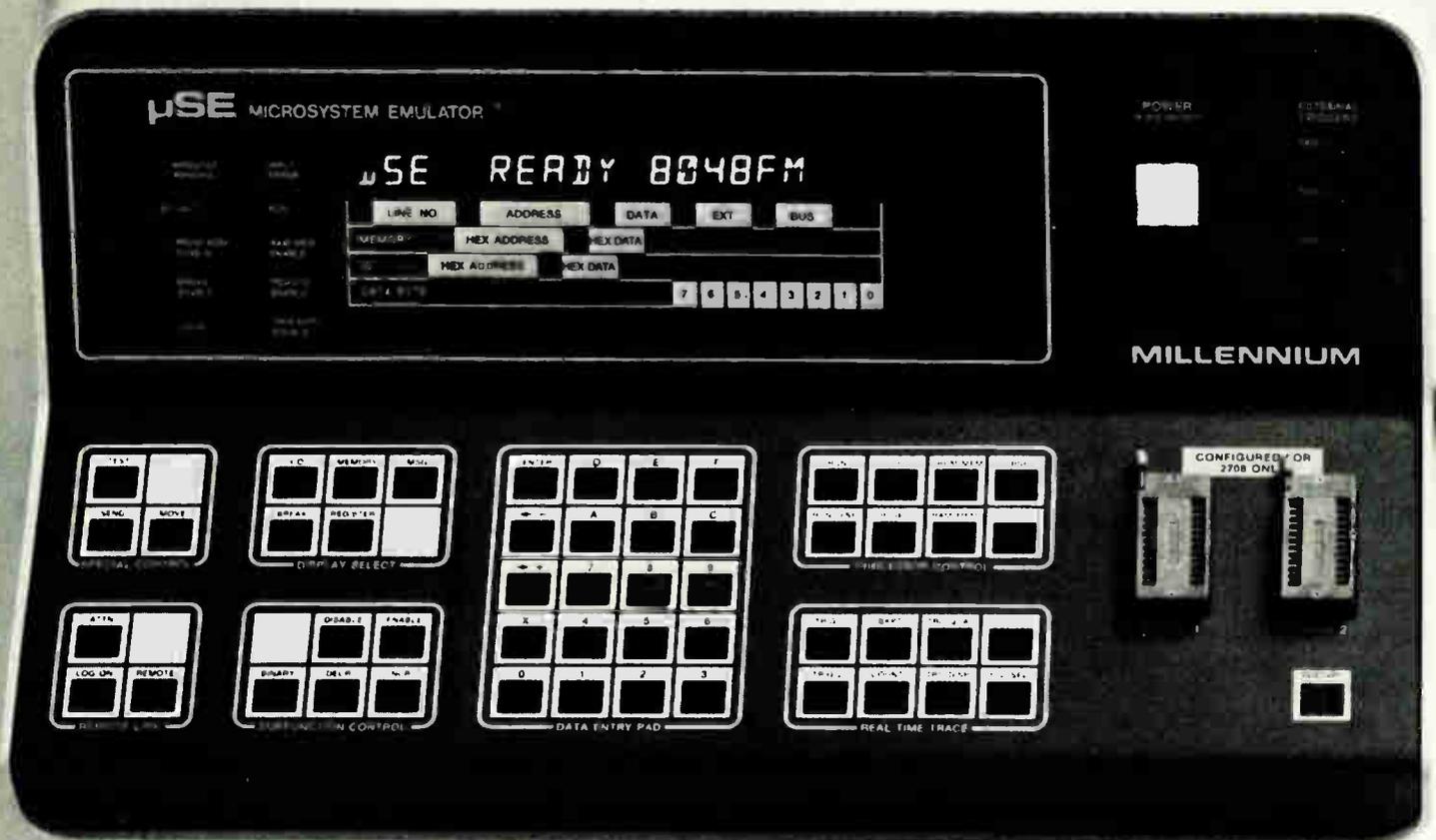
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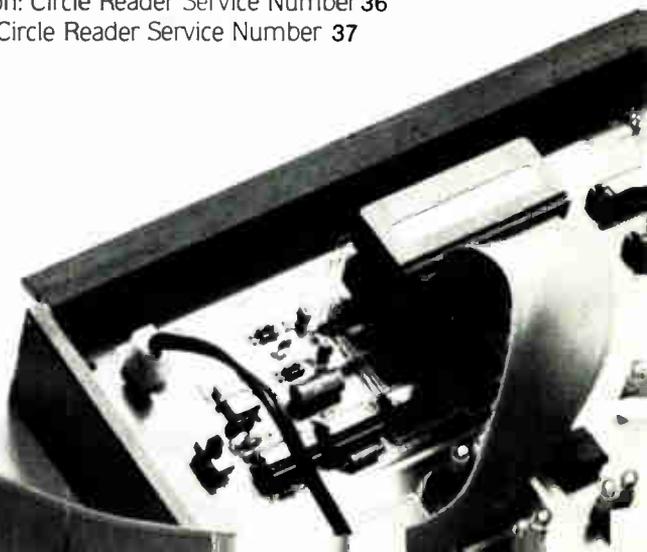
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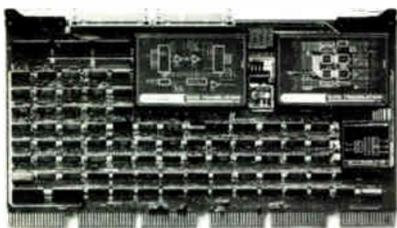
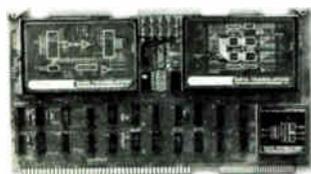
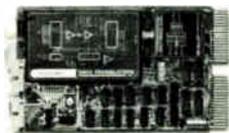
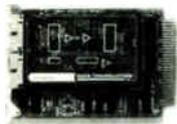
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Circle 38 on reader service card

N-well technology turns bulk C-MOS inside out

by John G. Posa, Solid State Editor

With p-FETs in n wells and n-FETs on a p substrate, new approach capitalizes on n-channel's advantages

Semiconductor makers are exchanging all p-doped regions for n-doped ones and vice versa in bulk complementary-MOS, thereby realizing a technology that combines C-MOS's low power with n-channel MOS's speed and familiar fabrication methods. The resulting structure, called n-well C-MOS, already is in fast random-access memories being developed in the U. S. and Japan.

The n-well process still stumbles over the latchup problem that plagues bulk C-MOS, and it might be even more susceptible to soft errors caused by alpha radiation. But countermeasures are possible, and the new technology will compete with n-MOS in the era of very large-scale integration, since its processing complexity is hardly greater than the fully tweaked n-channel processes.

Parts. The Matsushita Electric Industrial Co. of Osaka, Japan, is using n-well C-MOS and 2-micrometer gate lengths to build a 64-K static RAM—the biggest static part around [*Electronics*, Nov. 6, p. 145]. It also turns out that Intel Corp.'s anticipated high-performance C-MOS process has n wells (see figure).

The Santa Clara, Calif., company will use the process for 4-K and larger static RAMs and for microprocessors. Moreover, every other chip maker with a C-MOS program is weighing the switch to n wells.

N-well C-MOS gets its speed by

putting the faster n-MOS field-effect transistors in a high-resistivity p-type substrate and the p-MOS FETs into diffused n wells that give the process its name. High resistivity minimizes drain- and source-to-substrate parasitic capacitances and their associated delays. In contrast, conventional C-MOS processes have the slower p-MOS transistors in an n-type substrate, thereby bogging down n-MOS FETs in more heavily doped p wells.

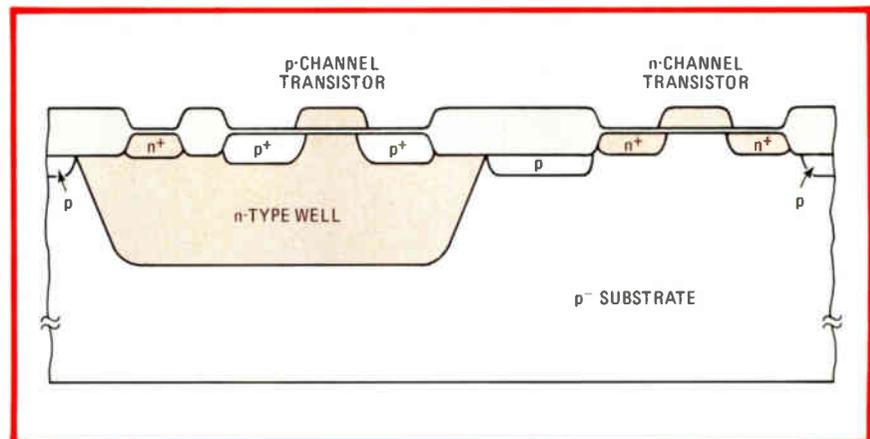
Since C-MOS followed n-MOS, it is reasonable to question how p wells ever caught on in the first place. The explanation most often offered is that, before ion implantation, only p-type boron could be diffused for a sufficiently low impurity concentration in wells. Even if an n-type dopant had been available, adjusting device and field thresholds would have been unwieldy without today's implantation methods.

Proponents of the n-well approach point out that in some LSI C-MOS circuits, the n-FETs greatly outnumber

their p-type counterparts. Also as n-MOS processing, too, uses p-type starting material, n-well C-MOS should be an easily understood fabrication method. Indeed, Intel uses the same substrate for its high-performance H-MOS and its C-MOS, with a few additional process steps.

"Pipe dream." Still, Donald L. Wollesen, manager of C-MOS research and development at American Microsystems Inc. of Santa Clara, calls n-well C-MOS an "n-channel guy's pipe dream" on the grounds that it sacrifices alpha particle immunity. When a RAM is built with conventional C-MOS, the n-channel FETs making up the cells can be put into a large p-type ubiquitous well, as it is called.

The reverse-biased junction formed between the well and the n-type substrate sweeps away carriers generated by an alpha hit. In fact, the Musashino Electrical Communications Laboratory of the Nippon Telegraph & Telephone Public Corp. is making dynamic RAMs with



Intel's n-well. With p-FETs in n wells and n-FETs in a p-type substrate, Intel's bulk complementary-MOS process is a simple extension of its high-performance MOS process.

n-well C-MOS; it actually puts p-MOS FETs in an ubiquitous n well to get back the alpha screen.

However, Sheng Hsu, a member of the technical staff at RCA Corp.'s Princeton, N. J., laboratories, argues that ubiquitous p-well protection may be a moot point, since any memory that uses polysilicon pull-ups is vulnerable to alpha hits, regardless of the polarity of the wells. That may be why Intel's initial C-MOS part, a 4-K static RAM with a 25-ns minimum access time, uses p-channel load devices in the array for a full six-transistor cell.

Stable. With p-MOS pull-ups and n-channel drivers, one device is nearly shorted while the other is virtually off. Alpha radiation is rarely strong enough to upset this stable situation. Moreover, if soft errors were to persist, the die could be coated with a material like polyimide, a tactic already employed.

Although proponents claim that n wells eliminate latchup, this assertion has yet to be substantiated. Latchup, which results from thyristor-like action in the bulk C-MOS, arrests circuit switching when an input or power-supply node goes out of bounds because of noise spikes.

For latchup to occur, the product of the parasitic npn and pnp transistors must exceed unity, notes AMI's Wollesen. RCA's Hsu explains that "with p wells you have a high-gain vertical npn and low-gain lateral pnp. With n wells, you have the opposite: strong vertical pnps and weak lateral npns. So in one case you may have 100 times 0.01; in the other case, you might have 50 times 0.03." Since both products equal or exceed unity, latchup is still present.

It is said that Hitachi Ltd. uses n-type wells in its Hi-C-MOS process. Actually, the Japanese company and Bell Laboratories in Murray Hill, N. J., are putting both n- and p-type wells into a substrate so lightly doped that it is called intrinsic. Hsu of RCA comments that a dual-well approach is really a single-well structure, as the substrate must lean toward one polarity or the other, albeit ever so slightly. Hitachi probably uses n-type starting material.

Solid state

Speedy metal-gate C-MOS process uses self-aligning and oxide-isolation techniques

One of the semiconductor industry's leading silicon foundries has added a new high-speed metal-gate complementary-MOS process to its mixed bag of solid-state technologies. Monosil Inc.'s process uses both self-aligning and oxide-isolation techniques—new to metal-gate C-MOS—to achieve more than a tenfold improvement in operating speeds.

The process could achieve speeds in excess of 20 megahertz in the foreseeable future in the custom gate arrays and configurable microprocessors to which the Santa Clara, Calif., firm is applying it. Thus these parts will rival in speed silicon-gate circuitry made with much finer lines.

Gate hike. Self-aligned processing can boost C-MOS metal-gate speed in two ways, says Jerry Van, the company's design manager. It eliminates the device tolerances that are necessary for alignment but that increase capacitance, and it eliminates the overlapping of gate areas on the source and drain diffusions and their attendant capacitance.

"The result is about a two to three times speed improvement, just in the gate, over conventional metal-gate C-MOS logic arrays that typically operate at 2-MHz speeds" at 5 volts, Van says. Another result is denser circuitry: a dynamic shift-register cell shrinks 25% in channel length and 38% in area.

Using an oxide-isolation technique akin to Mitel Corp.'s Iso-C-MOS process, Monosil halves the surface area of the diffusion, thereby reducing interconnection capacitance. "This results in another twofold speed improvement, allowing us to build metal-gate logic arrays that typically operate at speeds of 8 to 12 MHz," Van says.

The next step likely will be two layers of metalization, with a speed boost that will come from the shorter interconnections due to increased

density and from the elimination of the interconnecting cross-unders. "This will result in another twofold speed improvement" (to 16 to 24 MHz), Van says.

Such steps will put Monosil's arrays into the 20-MHz range of International Microcircuit Inc.'s new silicon-gate arrays [*Electronics*, July 3, p. 119], which are built with the Iso-C-MOS process and with 2-micrometer channel lengths. However, Monosil is achieving these speeds with a 6- μ m metal-gate process "that is much simpler, less expensive, and higher yielding and will lend itself to further speed enhancements with tighter design rules," Van says.

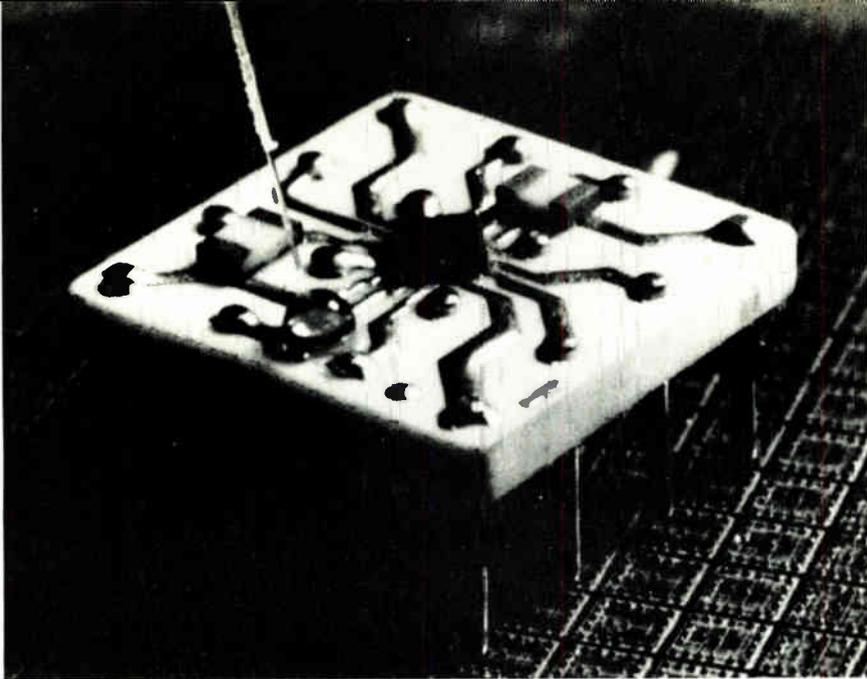
The basic speed improvements should be completed by mid-1981, Van believes, but in the first quarter Monosil plans to offer logic arrays with 8-to-12-MHz speeds and 100 to 650 gates, paralleling present C-MOS metal-gate arrays in complexity. They will be targeted at extremely low-power applications with 5 to 10 microwatts dissipation.

The new process will also be used in customizable 4-bit microprocessors—core central processing units surrounded by peripheral circuits specified by the customer. The M100 C-MOS version will be available in 1981's first quarter, with a p-channel version available in the following quarter. **-Bruce LeBoss**

Fiber optics

Monolithic receiver boosts data rate

Looking for a cost-effective optical-fiber link that can keep up with computer data-transfer rates, IBM Corp. researcher Dennis L. Rogers has built the prototype of a monolithic



High performance. Experimental optical receiver from IBM uses current-mode amplification to achieve greater bandwidth and sensitivity than has previously been possible with ICs.

optical receiver that can match the performance of hybrid designs. Key to the experimental receiver design is the use of current-mode amplification in place of the usual integrating or transimpedance amplifiers.

IBM's Thomas J. Watson Research Center in Yorktown Heights, N. Y., claims the new design [*Electronics*, Nov. 20, p. 34] can take full advantage of the information-carrying capacity of fiber-optic cables. Both broad bandwidth and high sensitivity have been achieved in a receiver (see photograph) built from a bipolar master slice geared for emitter-coupled-logic circuits.

Such a combination of specifications has been found only in discrete and hybrid designs. The inherently cheaper integrated circuits have been useful in low-end applications only [*Electronics*, Oct. 9, p. 155].

Better. "The data rate of the new receiver is 200 megabits per second," Rogers says, noting that this is an improvement by more than a factor of 13 over commercially available integrated receivers that produce digital outputs. It is equivalent to a -26-dBm sensitivity at a bit error rate of 1 in 10^9 .

The optical input is provided by a commercial p-i-n silicon photodiode bonded with the chip on a 1.2-by-1.2-centimeter ceramic substrate. Manufacturers like Motorola integrate a pn-diode-like detector into the receiver substrate, and a production version of the IBM design could

do the same with its diode.

Like conventional current amplifiers, the Rogers design uses a differential pair of bipolar transistors as the primary amplification element. But, instead of resistors, the inputs of common-base amplifiers are used as the resistive loads in each amplifier stage. The output currents of these amplifiers are added to the outputs of the differential pair.

Limit. "The speed of a conventional differential amplifier is limited by the base spreading resistance of the transistors," Rogers says. In the current-mode amplifier, this resistance is canceled because of the high input impedance of a high-frequency common-base amplifier.

The IBM receiver also integrates the decision logic and the level-restoring circuits needed to make a complete digital receiver. So, while it is not available for sale, it represents what can be done in state-of-the-art integrated receivers.

Further work on the receiver will look into improving the optical and electrical specifications for even greater sensitivities and data rates. IBM, of course, would be interested in developing a device that would handle the signals from computers at their natural data rates over as long a distance as possible.

The current-mode amplifier is well suited to integration because it uses few resistors. Also, its gain and bandwidth do not depend on precisely fabricated electrical values of the

integrated-circuit devices.

Because the design places few demands on the integrated components, it can be implemented on standard ECL master slices or gate arrays. "The design can also be extended to higher-performance master slices," Rogers says. "Up to 1,000 Mb/s may be possible." The present master slice is a 1976 design, in fact.

-Harvey J. Hindin

Computers

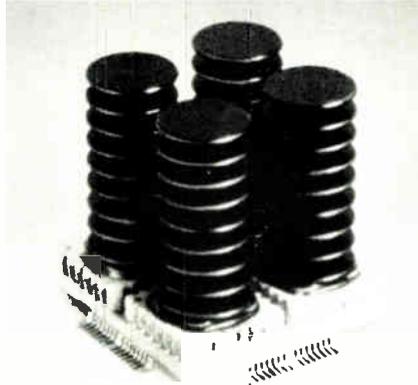
Amdahl leapfrogs IBM with technology . . .

With numerous technological advances and performance advantages, Amdahl Corp.'s new top-of-the-line mainframes have seized the gauntlet thrown down by IBM's 3081. The Sunnyvale, Calif., company took the wrappings off its 580 series plug-compatible machines less than a week after IBM announced the 3081.

The 580 series contains advances in processor chip density, distributed microcoding, and high-speed random-access memory, with the promise of significant software enhancements to come. The rapid response to the 3081 contrasts sharply with the lukewarm reaction from other IBM competitors, particularly from the computer makers who do not make plug-compatible machines (see following story).

Modules. The new 5860 is available with 16 or 32 megabytes of main memory and 18 to 34 data channels. It is upgradable to the other new machine, the 5880 dual processor, which can have 36 data channels and, in future, a maximum main memory of 64 megabytes. The IBM 3081 [*Electronics*, Nov. 20, p. 41] bowed with a maximum 32-megabyte main memory and 24 channels.

The prices of \$3.8 million for the 5860 with 16 megabytes and 18 channels and \$7.5 million for the 5880 with 16 megabytes and 36 channels put the 580 series well above the price-performance ratio of the 3081. The 5860 has an end-user performance range 1.2 to 1.6 times better than the equivalently priced



Air-cooled. Amdahl continues with air cooling in its new computers, now with 10-tiered towers on both the CPU chips (left) and on the four-chip RAM clusters.

3081, which gives it a 1.2 to 1.6 better price-performance ratio. The 5880's performance range of 2.0 to 2.9 times better than the 3081 gives it a price-performance advantage ranging from 1.0 to 1.4.

Amdahl has engineered a fourfold density jump for its emitter-coupled-logic central-processing-unit chips to 400 gates per chip. The 400-picosecond gate delay compares with 700 ps on the older 470 models.

The three-tiered cooling tower on the CPU chip, which became the trademark of Amdahl's 470 series, has become a 10-tiered tower (see photograph). Thus the 480 series continues with air cooling instead of moving to the bulky and expensive chilled-water system of the 3081.

Storage. The CPU integrated circuits are on a multichip carrier board alongside new very high-speed RAMs. These memories are clustered, with four 1-K ICs to a substrate. Used for cache storage and microcoding, they provide a 7-nanosecond access time to the CPU chips.

The microcoding streamlines processing, so that in many cases the CPU achieves the ideal of executing one instruction per machine cycle. The 24-ns cycle time compares with 26 ns for the 3081.

Amdahl's promotional literature for the 580 series lists a new class of firmware called macrocode, but "for now we prefer that the definition of macrocode remain somewhat mysterious," a company spokesman says. It is likely that macrocode will permit implementation of a relational

data base and that it will be introduced before the anticipated April 1982 delivery date of the 5860.

The company also introduced an entry-level large mainframe, the 470V/7C, to compete with IBM's new 3033S mainframe (which was announced with the 3081). With similar pricing, the 470V/7C is specified as performing 1.6 times faster than the 3033S. -Martin Marshall

. . . as debate starts on 3081, follow-ons

The 3081 represents a new performance height for computer giant International Business Machines Corp., but last month's unveiling left many competitors underwhelmed. They expect more announcements of significantly better machines as part of the continuing saga of the long-expected H series—indeed, IBM is already talking of follow-ons.

"I don't believe this is really the H series. We were expecting a much different announcement out of IBM," says one top executive at a competitive company. Although there are some interesting circuit innovations, "the architecture is not exciting. When the real H series stands up, it will likely be a bus architecture system, with different types of processors that can be put on the bus."

"It is the H series, but it is only the tip of the iceberg," argues Thomas J. Crotty, vice president for research for the IBM-watcher Gart-

er Group of Greenwich, Conn. "What IBM has done is to slip a new-technology machine into the marketplace without disturbing its own backlog for 1981.

"I expect the real announcements will come in mid-1981, and some features, such as native-mode software, will be operative in the 3081." Crotty also notes that industry observers had expected a data-base processor to be introduced, and that may come in mid-1981.

Of the computer makers at the top end of the market, only the leading maker of plug-compatible machines, Amdahl Corp., countered the 3081 with an announcement (see preceding story). Other manufacturers responded coolly:

■ **Hitachi:** Katsumi Fujiki, group executive for computers, notes that "IBM will almost certainly add channels and memory capacity, and Hitachi will work out appropriate countermeasures." This means increasing the performance of Hitachi's plug-compatible M-200H mainframe, introduced in the U. S. as the National Advanced Systems AS/9000.

■ **Siemens AG:** The Siemens 7882, a Fujitsu-designed plug-compatible machine, runs at 10.2 million instructions per second, slightly faster than the 3081. A spokesman for the West German company says that it will adjust its price to that of IBM. Fujitsu, which markets the mainframe in Japan, says its M-200 multiprocessor version can be as much as 2.2 times faster.

■ **Nippon Electric Co.:** An NEC spokesman claims that the ACOS 1000, introduced in September, bests the H series in its price-performance ratio. The non-IBM-compatible systems are sold only in Japan and have 15- and 29-million-instruction/s processing rates.

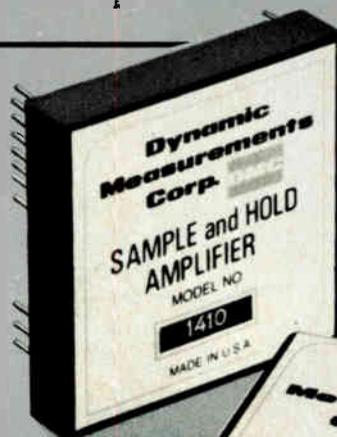
■ **Honeywell Information Systems:** President Stephen G. Jarritts notes "we expected the IBM pricing to be lower." The 3033S holds a slight performance advantage over the Honeywell DPS-8. Outside sources believe that Honeywell will introduce a larger mainframe in 1981.

■ **Burroughs:** No comment, except that Burroughs can configure sys-

12 bit throughput at 500 KHz.

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tems to compete with the new IBM series by tying together two more processors into the dual-processor B7821 system. The company has talked of a new top-of-the-line model, the B7900, for 1981.

■ Sperry Univac: The IBM announcement contained "no price-performance breakthroughs and no surprises and will give rise to no strategic changes," a spokesman says. The 3081 is slightly more powerful than Sperry Univac's 1100/84 four-processor system.

Apparently the next announcement on the H series will concern an added pair of coupled central processing units and a total of 64 megabytes of main storage—IBM already is quietly passing the word to key customers. The four-processor setup will be handled by a forthcoming 3082 processor controller, which will manage the main memory and house the interface logic for each data channel. *-Electronics staff*

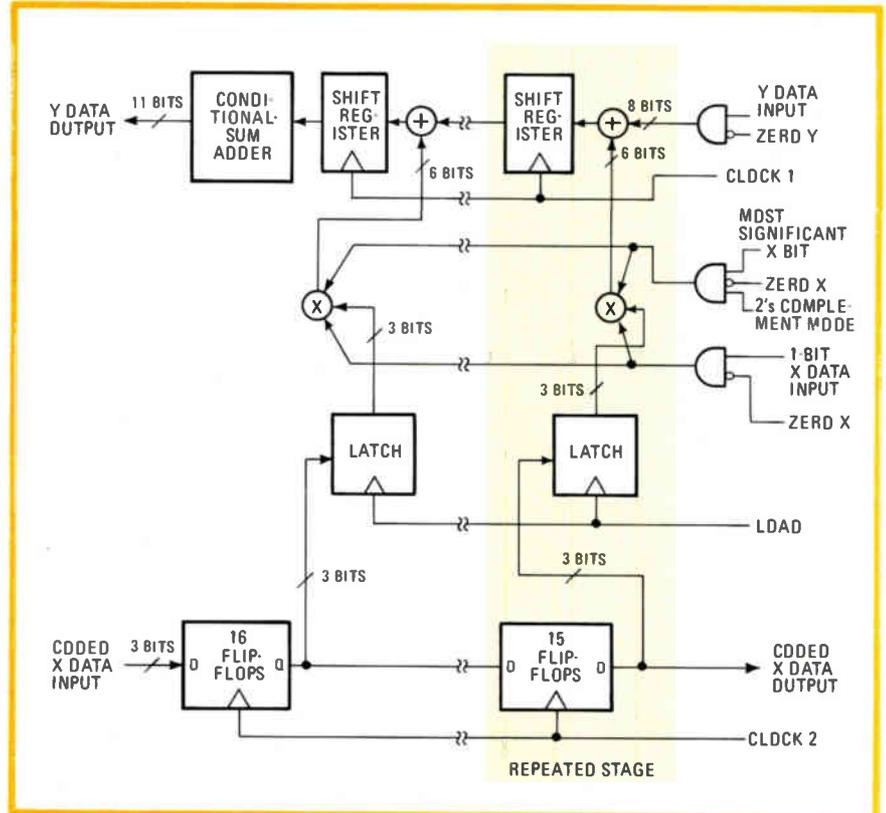
Solid state

Convolver on a chip pipelines its work

Even as mainframe architectural techniques are spreading to micro-processors, they are popping up in other logic circuitry. Very large-scale integration makes it possible to introduce methods like parallel processing to such specialized integrated circuits as TRW Inc.'s new bipolar VLSI convolver.

With 16 stages in a pipelined architecture, the 245-by-133-mil IC does 96 million additions and multiplications a second. Such a chip could be a boon to signal processing in military communications systems like radar, sonar, and pattern-recognition gear in missile guidance, where data-acquisition capabilities have outstripped processing ability.

Convolution implements a more complex mathematical process than the more widely used correlation techniques, which essentially compare only two data sequences—incoming data, represented by a



Mighty midget. TRW's single-chip bipolar convolver has pipelined architecture of 16 stages, giving a processing capability of 96 million mathematical operations a second.

waveform, and a fixed reference—and determine similarities. Correlation can sort out a variety of real-time responses from varying waveforms, comparing them against a variable reference to extract a useful signal from noise, for example.

Up to now, convolvers based on discrete ICs have been both bulky and power-hungry. Moreover, typically both convolution and correlation, which are examples of digital matched filtering, depend on extensive software to do the processing.

Demonstration. TRW selected the convolver to demonstrate "reduction of these fundamental algorithms to regular structures in silicon," says Robert E. Scott, manager of the bipolar products department at the Defense and Space Systems Group's Redondo Beach, Calif., Microelectronics Center.

The new IC (see figure) has a fully pipelined internal architecture, using 16 parallel tracks, or stages, to do shifting, adding, multiplying, and delaying. The signals do not move

serially through the entire chip; rather they can be processed in parallel by the 16 stages.

"The processing makes use of the entire chip continuously, rather than switching signals from one part to another," says Barry Dunbridge, director of the Microelectronics Center. "This might be a portent of the future."

With the 16-stage VLSI chip, designers can do away with 6 medium-scale integrated circuits per stage, or altogether 96 ICs that would achieve the same speed. Moreover, the dozens of medium-scale ICs that the convolver chip can replace would draw 5 to 10 watts for real-time signal processing in a radar, posing vexing heat dissipation problems in tightly packed avionics compartments. The TRW chip consumes only 700 milliwatts for its 16,200 devices, and a forthcoming 32-stage version will take just 1 W for double the density and speed.

TRW says it is using bipolar processing techniques that will permit

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scaling down of future designs, but it will release no details. The 16-stage design is ready to be put into new equipment by engineers in the neighboring applications units, according to TRW sources.

The company developed the chip with its own funds, but it appears that the techniques used and perhaps even the chip itself could find a home in the Pentagon's Very High-Speed Integrated Circuits program, on which TRW is bidding. Also, an objective of the design procedure was to create structures with 1- μ m geometries to be the basis of a library of modules for computer-aided design. -Larry Waller

Bubble memories

Bubble-laden boards start to take off

After nearly a decade's warmup, bubble memories appear poised for launch. Thanks to the availability of controller chips and high-density multichip boards and, most importantly, reduced prices, semiconductor makers are experiencing a marked upturn in interest in these nonvolatile mass storage parts.

Absence of the vital support circuitry slowed the takeoff. Although Intel Corp. was the first to begin delivering 1-megabit bubbles about 18 months ago, it has only recently made available its controller chip, the 7220. The company is incorporating it on a new iSBC 254 board that houses up to four 1-Mb 7110 bubble-memory chips and other control circuitry.

Versions. The board will be available in three capacities—128-K, 256-K, or 512-K bytes. Janice Carnes, strategic marketing manager at Intel's Memory Systems operation in Sunnyvale, Calif., says a fully loaded 512-K-byte board will sell for \$6,300 in 100-piece lots in January. In line with its policy of guaranteeing future prices [*Electronics*, Aug. 14, p. 35], Intel will drop the price to \$4,200 by mid-1981.

Also by mid-year, National Semi-

conductor Corp. of Santa Clara, Calif., is expected to unveil its BLC9081 board. It will pack eight of National's 1-Mb NBM2011 bubble memories, the INS82853 controller chip, and all the associated support circuitry on a board equivalent to Intel's popular Multibus board.

Another. Meanwhile, Texas Instruments Inc. of Dallas is offering its TM990/211 board that can hold six TIB1000 1-Mb bubble-memory chips, a TIB0903 controller chip, and other support circuitry for \$15,200. A redesign available soon will house eight TIB1000s, for a full 1-M byte capacity, and will cost about \$20,000.

Additionally, Rockwell International Corp.'s Electronic Devices division in Anaheim, Calif., is offering its RMS family of boards with capacities of 32-K, 64-K, 128-K, and 256-K bytes, using a specially programmed single-chip microcomputer that serves as a controller and other support circuitry. The firm will be bringing out an expanded family of controllers and modules in 1981 with a half-megabyte maximum capacity.

Rockwell reports good acceptance of its module family, and a TI spokesman says business is steadily improving. Nonetheless, he adds, "people are still slow to embrace the technology, probably because of pricing."

Gathering steam. By contrast, Intel's Carnes notes that "all of a sudden, the business is gathering lots of steam," and that Intel's "brazen policy on guaranteeing prices was a missing link. Now that people know the numbers, they are going ahead and making a commitment." The principal markets that are developing are in numerically controlled machine tools, industrial controls, instrumentation, and telecommunications, as well as in computer terminals and business equipment, she says.

Equally enthusiastic is Frank Stempki, National's product marketing manager for magnetic bubble products. He sees a big surge after a year of "pregnant pauses, when prices didn't go down and volumes didn't increase as expected." What's

Electronics review

more, users are calling for standardization. "When that occurs, the market will truly break open, and more designers and buyers will belly up to the bar and start designing in and placing volume orders for bubbles," he says.

-Bruce LeBoss

Packaging

Chip-carriers move into prototyping

Interest in leadless chip-carriers as a dense packaging technique for large-scale integrated circuits is spreading to the prototyping stage of systems using printed-circuit boards. A leading interconnection manufacturer is developing a new version of stitch wiring for a family of hardware to be oriented to chip-carriers.

Stitch wiring promises greater sys-

News briefs

U. S. lead slips as demand for process control climbs

Both the sale and the purchase of industrial process control equipment in the U. S. are slipping as a percentage of the world market figures in the face of growing demand and increased competition abroad, a leading market research firm says. More technological and business acumen on the part of foreign companies, rather than a lack of aggressiveness on that of domestic manufacturers, is one cause, says a new report from Creative Strategies International, San Jose, Calif. For 1980 the worldwide market for industrial process equipment is estimated at \$6.751 billion, 47% of which is supplied by the U. S. The market is forecast to grow at an annual compound rate of 10.1% to \$10.9 billion in 1985, with a U. S. market share of 45%.

Xerox introduces Ethernet-compatible office gear

Increasing its strength as a leading supplier of integrated electronic office systems, Stamford, Conn.-based Xerox Corp. has added five new products, all with built-in Ethernet interfaces. Collectively called the Xerox 8000 network systems, these products will provide services to be shared among groups of Xerox model 860 information-processing work stations on the Xerox-originated local network scheme. They are an electronic filing and mail system, a letter-quality laser printer station, and three communications modules that provide gateway internetwork connections with other networks, including other Ethernets, or Ethernet interfaces for earlier Xerox products and products of other manufacturers using the standard RS-232-C interface.

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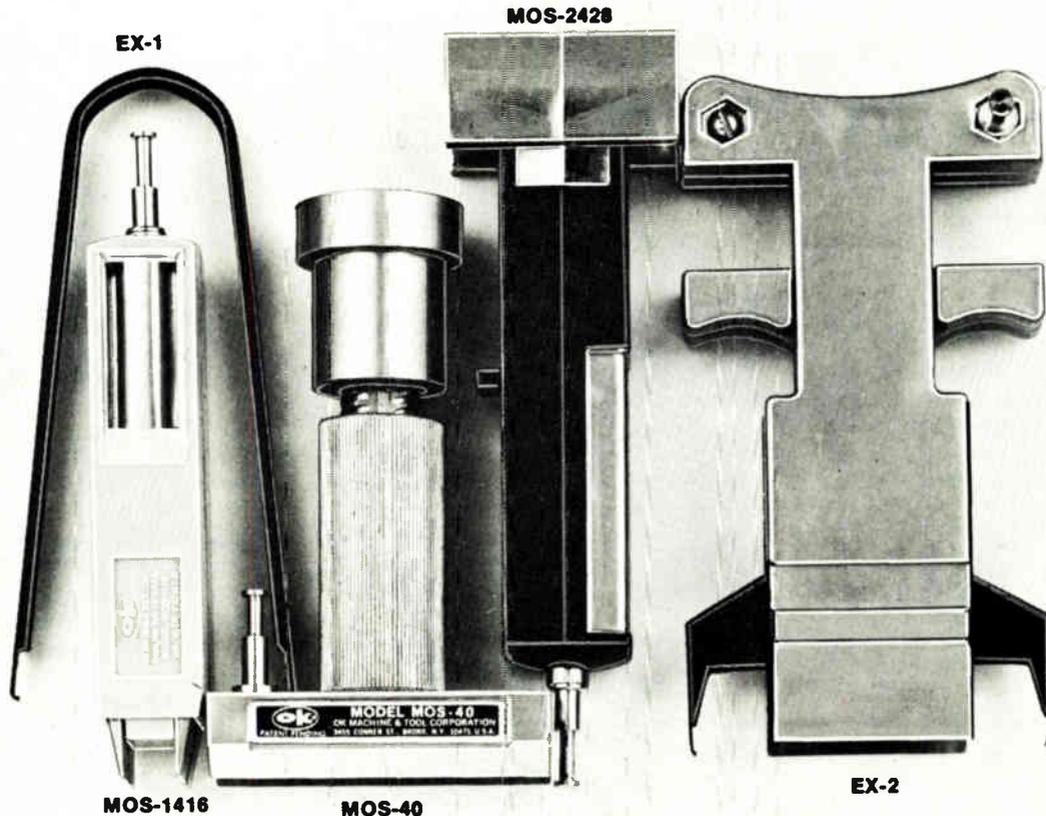


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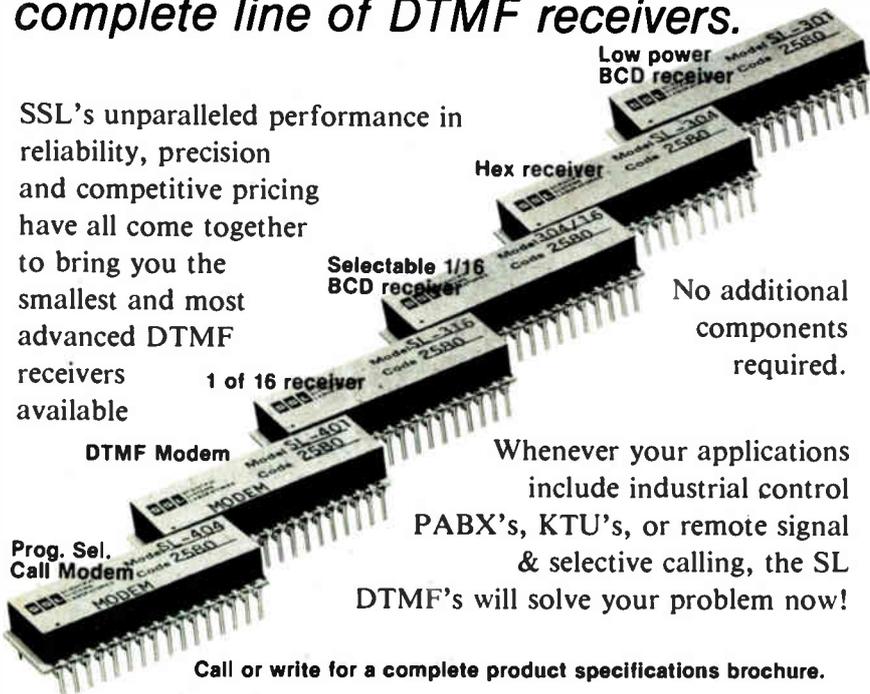
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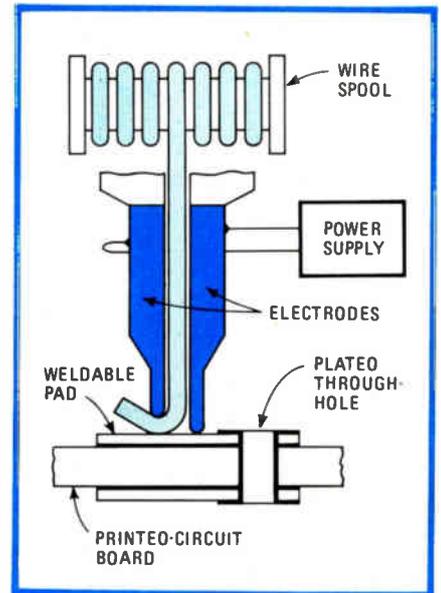
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Electronics review

tem densities than the wrapped-wire technique because it interconnects IC package leads to metal pads on the pc board instead of wrapping wires around the lengthy input/output pins of dual in-line sockets. With no long pins, the resulting low profile lets boards in a card cage be as little



Stitch in time. In Augat's new version of stitch wiring, both welding electrode halves work on the same pc-board surface. Boards in a system can be closer together with both components and wiring on the same surface.

as 500 mils apart, whereas the typical wrapped-wire pin alone requires a 500-mil clearance and thus significantly wider board spacings.

Surface. The new stitch-wire version, under development at Augat Inc., aims at even greater system densities by running its welded wire interconnections on the top surface of the board - the same surface that the chip-carriers inhabit. Also, using chip-carriers promotes greater board densities because of their small size and since their I/O interconnections are on 50-mil centers. Conventional dual in-line packages have leads on 100-mil centers.

Thus, the chip-carriers can better accommodate the higher I/O counts of LSI chips and the coming very large-scale integrated circuits.

Typically, stitch wiring makes point-to-point interconnections by electrically welding lengths of insu-

lated nickel wire to stainless-steel pads on an epoxy-glass pc board. The wiring head Augat used previously had to contact both the top and bottom of the board with electrodes for a complete circuit [*Electronics*, Jan. 18, 1979, p. 133].

New technique. In the new top-side method, the insulated wire automatically feeds through a hollow split electrode (see figure), one half of which displaces the insulation to make a contact with the weld pads running to the reflow-soldered contacts of the carrier socket. The other electrode half is already in contact with the pad, and so the weld circuit is complete.

The new wiring head is smaller than the older one, says Frank C. Rydwansky Jr., marketing manager of advanced packaging for the Attleboro, Mass., firm. The smaller head permits closer spacing of the welds, which in turn facilitates welding on 50-mil centers. Rydwansky and his associate, John A. Braun, unveiled the new parallel-gap stitch wiring when they presented a paper at the recent Nepcon Northwest '80 in San Mateo, Calif.

The technique is aimed at both prototyping and small-scale production. Augat will supply boards having pads on 50-mil centers for 68-pad chip-carrier sockets and plated through-holes on 100-mil centers for 300-mil-wide DIPs. The company has designed a special card cage with a back plane that can use wrapped wiring to accept the new boards.

Boards. "A need for a board or board family for surface-mounted components having a mix of small chip-carrier memories, larger carriers for logic chips, and gate arrays has been building for some time," Rydwansky says. It is almost certain that the future will see boards of this type containing only positions for chip-carriers on 50-mil centers.

Augat expects that LSI and VLSI systems in big production runs would use custom multilayer pc boards. However, it is possible that stitch wiring and socketed chip-carriers could move into full-scale production runs, as has wrapped wiring of DIPs on IC socket panels. -Jerry Lyman

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| | | CDP18S023 power supply 0.6A @ +5V, no fans required ... | \$ 25. |

*Intel OEM price list July 14, 1980

| Factor | Intel | RCA Microboard |
|----------------|-----------------|----------------|
| Power required | 61.7 watts | 0.3 watts |
| Volume | 1190 cu. inches | 173 cu. inches |
| Weight | 41 pounds | 6 pounds |
| Cost | \$6110 | \$1643 |

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RCA

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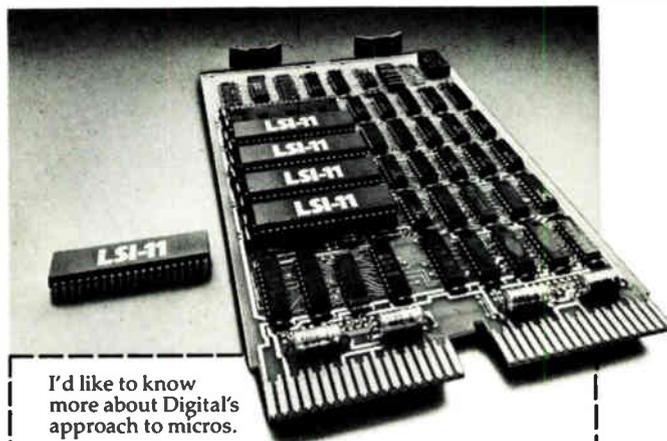
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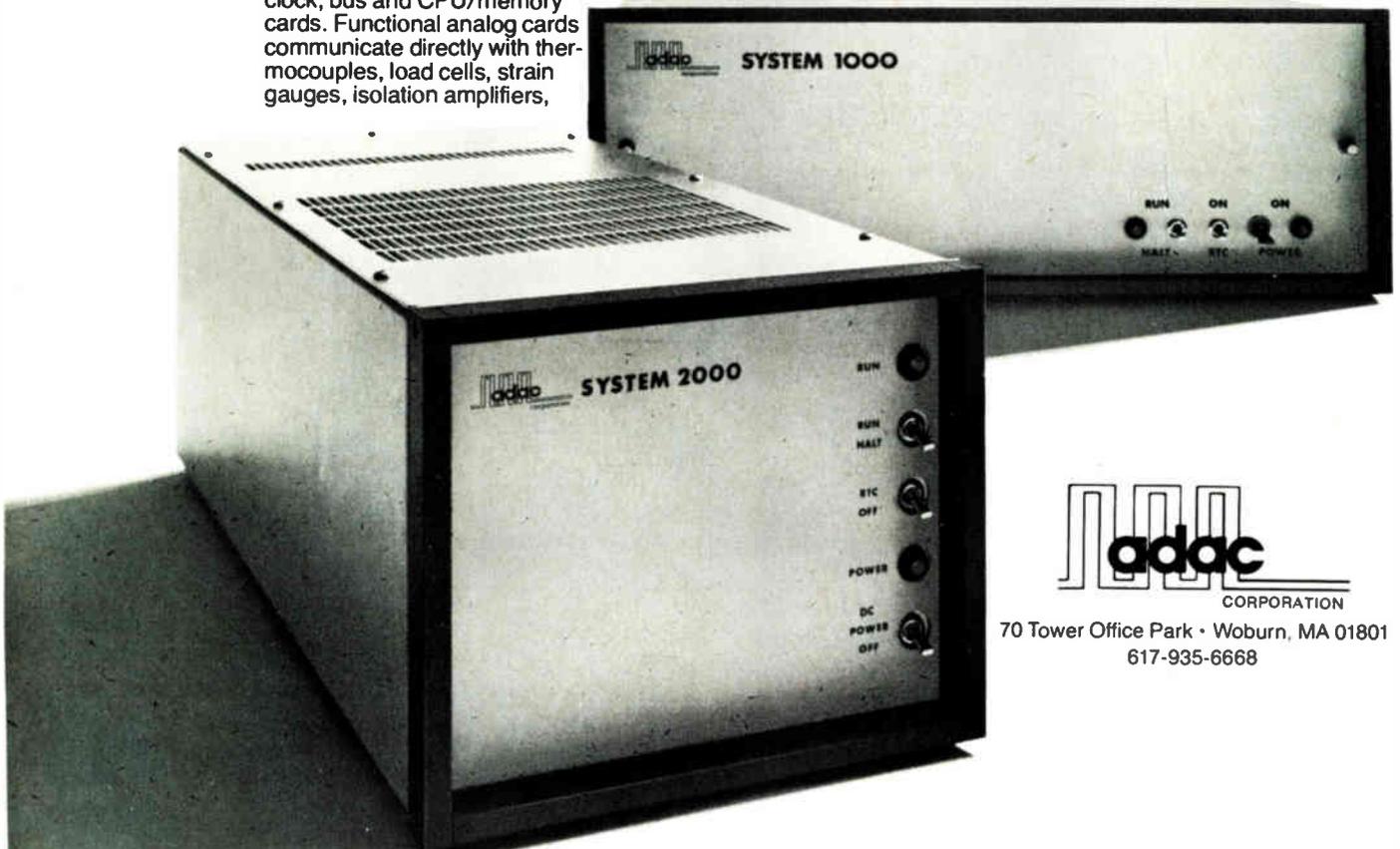
The compact ADAC System 2000 is built to hold 13 half quad cards. If you need greater capacity, slave units can be utilized or you can go to the larger System 1000 which accommodates any combination of 11 quad size cards or 22 half quad size cards. Both systems can be bench top or rack mounted and have a universal power supply that can support up to 256 kilobytes of memory.

The real heart of both System 1000 and ADAC System 2000 is their incredible number of analog, digital, serial I/O, clock, bus and CPU/memory cards. Functional analog cards communicate directly with thermocouples, load cells, strain gauges, isolation amplifiers,

transmitters and strip chart recorders to name a few. Discrete cards communicate with switch contacts, relays, thumb wheel switches, pumps, motors and other devices. All cards can be purchased as separate items.

A single System 1000 can be supplied with up to 700 high level analog input channels, or 128 analog low level input channels, or 700 digital I/O functions. A typical ADAC System 2000 contains a CPU, 64 kilobytes of memory, floppy disc controller, 16 channel A/D, 4 channel D/A, 32 TTL I/O lines, two serial I/O ports plus room for another six cards of your choice.

Another nice thing about both systems is their prices. Contact ADAC for full details so you can choose the combination of price and capability that's just right for your application.




CORPORATION

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Washington newsletter

\$80 million In VHSIC awards due in spring . . .

Four to six contracts worth approximately \$80 million are scheduled to be awarded during April and May 1981 for Phase 1 of the triservice Very High Speed Integrated Circuits (VHSIC) program based on proposals due Dec. 5, says Larry W. Sumney, director of the Pentagon program. **Winners of the three-year awards will be drawn from proposals of the nine Phase 0 study contractors, each of which must bid on a minimum of three military systems—one for each service—to maintain eligibility.** Phase 0 contractors studied up to 19 systems [*Electronics*, March 27, p. 41]. VHSIC is exploring silicon bipolar and MOS technologies [*Electronics*, Jan. 3, p. 81], but Sumney says that “n-MOS may not be hardenable” for radiation-resistant circuits. However, he adds that n-MOS, “the workhorse of the industry, with the lowest cost,” is not being ruled out, since hardening may not be required in some applications like Army manpack communication systems.

. . . Phase 3 awards reach \$26.5 million; Hughes gets nine

Technology support contracts to industry and universities under Phase 3 of VHSIC now number 48, totaling almost \$26.5 million, according to the program office. **Electron-beam processing and lithography received heavy emphasis in the awards, which range from 9 to 48 months long.** Hughes Aircraft won nine awards totaling \$6.5 million, whereas Westinghouse Electric and Cornell University each got four, worth \$1.4 million and \$998,000, respectively. Individual awards exceeding \$1 million (and their time spans in months): \$2.7 million (48) to the University of Illinois for a reliable high-performance VHSIC system; \$1.5 million (15) to Perkin-Elmer to extend microlithographic technology; \$1.5 million (24) to Hughes for electron-beam lithography components for direct writing; \$1.37 million (15) to TRW for electron-beam systems software; \$1.2 million (48) to Varian Associates for a direct-writing electron-beam lithography system; \$1.2 million (20) to Electron Beam Microfabrication Corp. for an ultrahigh-speed submicrometer direct-writing electron-beam exposure system; and \$1.1 million (24) to Hughes for static-induction-transistor, or SIT, logic technology, low-temperature silicon epitaxy, and improved resists for electron-beam lithography.

NSF to set up engineering directorate; IEEE urges more funds

Reorganization of the National Science Foundation will include the creation of a Directorate for Engineering that “will seek more resources for the engineering disciplines,” says NSF director-designate John B. Slaughter. Responsibility for applied scientific research projects, now administered by the NSF’s existing Directorate for Engineering and Applied Sciences, will be added to the other research directorates’ primary function of supporting basic research. **The reorganization will begin immediately under NSF acting director Donald N. Langenberg until Slaughter, an engineer who was provost of Washington State University before his appointment by President Carter, can be sworn in.** Slaughter is expected to keep the NSF post under the Reagan Administration.

Leo Young, president of the Institute of Electrical and Electronics Engineers, who has long been urging more NSF support for engineering sciences, says he is delighted with the move and believes that the new engineering directorate should get a funding increase of approximately 50% to about \$150 million. Engineering overall now gets about 10% of the NSF’s \$1 billion budget. He also wants to see the NSF’s \$26 million computer sciences programs made part of the engineering directorate.

The Air Force MATE mission

Automatic test equipment people from industry and Government got a taste of Gen. Alton D. Slay's refreshing candor during the Autotestcon meeting in Washington, D. C., last month. The Air Force Systems Command chief's comments on the controversial issue of military ATE was made substantially more palatable to his industrial audience by a touch of earthy humor.

After citing ATE standardization as the solution to the USAF's problems of systems proliferation, soaring costs, and personnel shortages, the general paused. But no one applauded. "Well, I'm disappointed!" he went on. "At AFSC, such a pronouncement about standardization is generally accompanied by great fanfare with massed trumpets, waving of flags, marching of troops in review, and a flyby of 10 squadrons of our finest new aircraft. I really didn't expect that here—a simple 10-minute standing ovation would have done nicely—but what really hurt was when I saw several of you surreptitiously throwing up in your briefcases."

However upsetting the drive for ATE standardization may be to some design engineers and manufacturers, Slay is determined to make it a reality, because, he notes, the Air Force cannot continue spending nearly 75% of its support equipment budget—almost \$1 billion annually—just for ATE, for more than 400 system configurations that require over 40 different program languages using over 100 programming aids. As for personnel, he points out that "last fiscal year we didn't have a single first-term ATE technician reenlist. Why? You [in industry] pay him or her three times the salary that we can pay in the Air Force."

First applications

To resolve the money and proliferation problems, the Air Force is counting heavily on MATE, the Modular Automatic Test Equipment system that has been in competitive design and development by Sperry Corp. and Westinghouse Electric Corp. for over two years [*Electronics*, Aug. 3, 1978, p. 8], with the winning concept to be selected next year. Modular ATE was tried once before by the Air Force but did not work, Slay recalls, because the modules were unique to individual systems and therefore could not be used across systems. As a result, proliferation continued. MATE, he insists, will be different, employing interchangeable "MATE-qualified"

black boxes and software limited "to a few select languages and ultimately, in the future, to a single language."

MATE will be phased in during 1981, with first applications in the Fairchild A-10 attack aircraft. It will be used for the inertial navigation system, called Lantirn, for Low Altitude Navigation and Targeting Infrared System for Night, recently awarded to Martin Marietta Corp., plus two support depot systems, Slay disclosed.

For makers of commercial instrument modules, the AFSC commander believes that MATE will become "a way to enter the Government marketplace with fewer military procurement strings attached. The market for those modules, whether commercial or mil-spec, is very large. Because of this, competition between large and small instrument houses should be keen and the motivation to have their modules placed high on the MATE preferred module list should be equally high." Conversely, the Air Force hopes its program will sharply reduce the number of sole-source procurements for spares and replacements, because of the stress in MATE on modular design and standardization.

The coming guidebooks

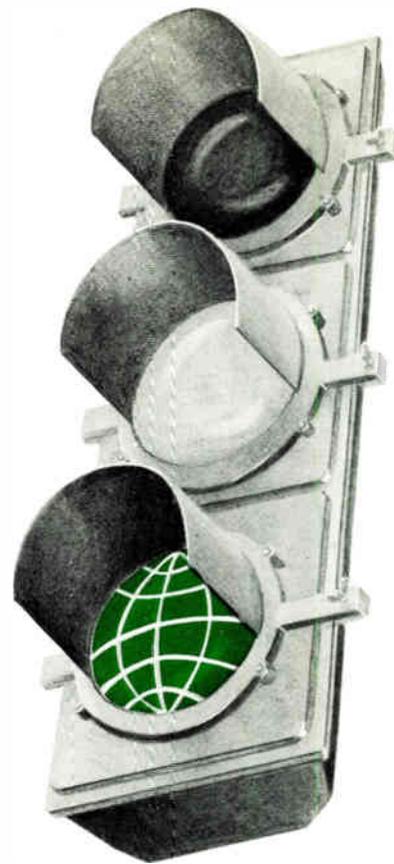
In August 1981, Slay says, the Air Force will move closer to resolving the ATE sole-source problem with the publication of five new guides for commercial test equipment houses. They will provide what he calls "the cornerstone for MATE—a management philosophy and a disciplined approach for the identification, acquisition, and support of all automatic testing capabilities for all future weapons systems." Areas covered by the five guides will be: electronic test equipment acquisition, MATE development, avionics testability design, a MATE production operational guide, and—the greatest potential cost-saver in AFSC's view—the test-program set acquisition for software.

"With these guides in hand, there will be no excuse for fielding unsupportable avionics or unusable ATE," says the general unequivocally. While calling for industry support to ensure ATE flexibility and continuing innovation, the AFSC command is nonetheless convinced of what its mission is: "The bottom line of all this is that we are dead serious. And we intend to push MATE all the way."

-Ray Connolly

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|--|--|--------------|----------------------------|-------------------------------|
| | UDN-6116A-2, 6126A-2 UDN-6116A, 6126A | 6 6 | + 60 V + 80 V | 16 lead 16 lead |
| | UDN-6118A-2, 6128A-2 UDN-6118A, 6128A UDN-6118A-1, 6128A-1 Anode driver, gas discharge displays | 8 8 8 | + 60 V + 80 V +110 V | 18 lead 18 lead 18 lead |
| | UDN-6138A-2, 6148A-2 Split supply (+20 V, -40 V) UDN-6138A, 6148A Split supply (+40 V, -40 V) | 8 8 | 60 V* 80 V* | 20 lead 20 lead |

*Output BV referenced to V_{EE} Max. $V_{EE} = -40\text{V}$

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| TMM315D-1 (2147-3) | 4,096 x 1 | 55 |
| TMM2016P-1 (2016-1) | 2,048 x 8 | 100 |

CMOS Static RAMs

| DEVICE | ORGANIZATION | ACCESS TIME (ns) |
|---------------------|--------------|------------------|
| TC5501P (5101L) | 256 x 4 | 450 |
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| TC5047AP-1 (5047-1) | 1,024 x 4 | 550 |
| TC5504AP-3 (6504) | 4,096 x 1 | 300 |
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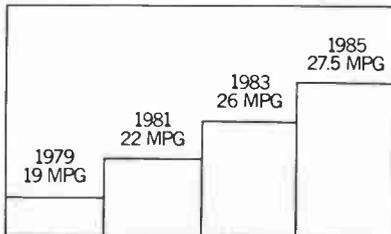
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Circle 65 on reader service card



MOTOROLA HELPS STRETCH GAS MILEAGE

Automotive manufacturers are caught between a rock and a hard place. They are obliged not only to reduce fuel consumption, but also, at the



Government-mandated Corporate Average Fuel Economy (CAFE) standards. Source: NHTSA

same time, to reduce harmful exhaust gas emissions. And these objectives seem to be mutually exclusive.

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BY MAKING ENGINES THINK.

that particular moment.

It's a real computer in miniature, with a memory and the ability to manipulate what it learns in terms of what it already knows. Motorola's electronic engine-management system is so efficient that some domestic car makers are already using it in their current models. Other car and heavy-duty-equipment manufacturers in America and Europe are planning to use it in the near future.

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Circle 67 on reader service card

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RCA's new VP-3301 is a professional quality, ASCII encoded, interactive data terminal, suitable for a wide variety of industrial, educational, business and individual applications requiring interactive communication between computer and user. Connects directly to a computer or to a standard modem for over the phone access to time sharing networks and data bases! Micro-processor intelligence and LSI video control integrated circuits bring performance, features and flexibility at a low price. Power supply included.

Unique color locking circuitry creates sharp, jitter free, true color graphics and rainbow free characters

Displays the entire field of characters in any of 8 colors against any of 8 background colors (7 gray scales with monochrome monitors).

Individual letters, words, or lines in different colors or in reverse video can be displayed.

The VP-3301 offers a choice of two software-selectable display formats: Either 40 characters by 24 lines. Or 20 characters by 12 lines.

The terminal's resident character set consists of 52 upper and lower case alphabetic, 10 numerals, 32 punctuation/math symbols, and 31 control characters. You can also define a total of 128 of your own characters.

* OEM Pr.ce

Including: Greek letters and other foreign alphabets, graphic symbols, large graphics building blocks, playing card suits, and unique character fonts.

The keyboard section features flexible-membrane key switches with contact life rated at greater than five million operations. A finger positioning overlay and positive keypress action give good operator "feel".

An on-board sound generator and speaker provides aural feedback for key presses and may also be activated with escape sequences to provide an audio output.

The sealed keyboard surface is spill proof and dust proof. This combined with high noise immunity CMOS circuitry makes the VP-3301 ideal for hostile environments.

Output is industry standard asynchronous RS232C or 20 mA current loop with six switch selectable baud rates and 8 selectable data formats.

The terminal can be connected directly to a 525 line color or monochrome monitor. Or to a standard TV set using an Rf modulator.

For more information, contact RCA MicroComputer Marketing, New Holland Avenue, Lancaster, PA 17604.

Or call our toll-free number: 800-233-0094.

RCA

International newsletter_____

West Germany starts to monitor satellite radio transmitters

As Europe's first authority to do so, West Germany's post office, the Bundespost, has started a radio-monitoring service that keeps tabs on satellite-based transmitters from a ground terminal in Leeheim, near Frankfurt. A Siemens-built antenna system spots, tracks, and identifies communications satellites and determines their orbits and their transmitters' frequency, polarization, and radiated power. With the increasing number of communications satellites aloft—around 200 at present—this monitoring task is becoming more and more important **to ensure that satellite operators keep the transmitters adjusted to the assigned specifications** and thus to prevent interference with other radio communications. In its present configuration, the Leeheim antenna system monitors three frequency ranges: from 130 MHz to 1.3 GHz, from 1.5 to 2.3 GHz, and from 10.95 to 11.8 GHz. Later, the system will cover the entire 130-MHz-to-13-GHz range.

British electron-beam annealer enters production

Conventional thermal annealing of ion-implanted semiconductor materials is time-consuming and can cause unwanted sideways diffusion of the implanted dopants. So to shorten this troublesome integrated-circuit fabrication stage and eliminate its damaging effects, Lintech Instruments Ltd. of Cambridge, England, is introducing an electron-beam annealer, called Seza, that **in a production form would have a throughput of 200 wafers per hour**. A first small-scale production version will shortly be delivered to the Martlesham Research Centre of British Telecom, part of the British Post Office, and a second system is going to an unnamed U. S. West Coast semiconductor manufacturer. In the U. S., Spire Corp. of Bedford, Mass., makes similar equipment.

Seza, which is based on equipment developed under H. Ahmed of Cambridge University, scans a 30-kV electron beam with a spot up to 200 μm in diameter over an up-to-5-inch wafer with an equivalent beam power of 1 kW, sufficient to restore crystal dislocations and activate the dopants. Selling for between \$86,000 and \$120,000, the system will likely cost more than upcoming laser-annealing systems, but work at Cambridge shows that it can yield devices of superior electrical performance. It was described at Semiconductor 80 in Brighton, England, Nov. 25-27.

UK seeks to link U. S. technology, own entrepreneurs

An unusual method of providing seed money for high-technology joint ventures is to be attempted by Britain's National Enterprise Board together with venture capitalist Jack L. Melchor of Los Altos, Calif. The scheme is aimed at U. S. companies with an already successful product but without the financial stature to launch an overseas operation. The board will provide a \$4.8 million fund and will also look for British entrepreneurs wishing to set up operations in high-unemployment areas. Melchor, meanwhile, will **seek out interested U. S. companies such as makers of computer peripherals**. Each startup will be financed jointly by the NEB fund, the British entrepreneur, and the U. S. company.

Telidon service to begin next April In Canada

The world's first commercial Telidon service—Canada's version of interactive teletext—will begin next year in April in southern Manitoba. Working with the provincial government, Infomart Ltd., a Toronto-based electronic publishing organization, **will offer the area's 30,000 agricultural producers 25 free terminals giving them direct access to Project Grassroots—**

International newsletter

specialized information that will help them run their businesses better. Meanwhile, the Manitoba Telephone System is going ahead with its plan to install 150 terminals in the Elie-St. Eustace area of the province next summer, as part of a trial it and the Canadian Department of Communications are conducting of the use of fiber optics for the delivery of Telidon, television, fm radio, and other communications services. Infomart says all Elie field-trial users will be able to access Grassroots information.

Phillips makes Austria's first domestic computer

With the start of production of the P200 table-top computer at NV Philips Gloeilampenfabrieken's Vienna-based facilities, Austria now has for the first time computer manufacturing activities of its own. The P2000, developed at Philips Austria, is an easy-to-operate, widely applicable system with an alphanumeric keyboard, video terminal, printer, and floppy-disk store. Depending on configuration, the system sells for between \$1,430 and \$10,300. **It will initially be marketed in Austria, Great Britain, the Netherlands, and West Germany and will later be available on all markets in which Holland-based Philips Data Systems is active.**

French fiber optics plans stalled

An industrial stalemate is blocking French government hopes for a mostly French optical-fiber manufacturer and **delaying the country's ambitious Wired City experiment** [*Electronics*, July 17, p. 80]. The government agency in charge, the Direction Générale des Télécommunications (DGT), is pushing for a joint venture involving the Electronic Products division of Corning Glass Works, Corning, N. Y., the Lignes Télégraphiques et Téléphoniques (LTT) subsidiary of Thomson-CSF, and possibly the Quartz et Silice subsidiary of the St.-Gobain-Pont-à-Mousson industrial group. The problem is an exclusive technical and marketing agreement between Corning and Les Cables de Lyon, a subsidiary of the Compagnie Générale d'Electricité, which neither is willing to cancel.

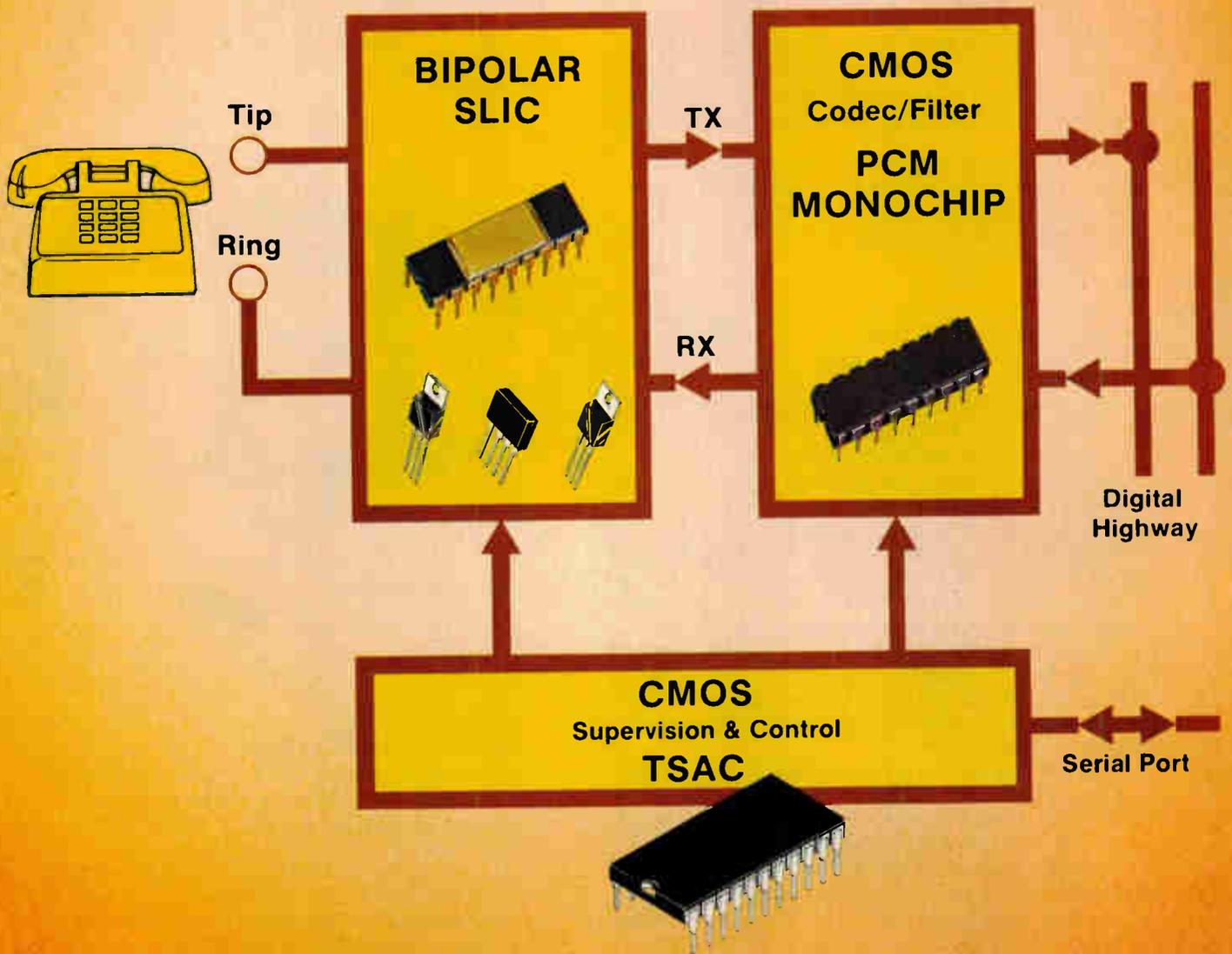
Siemens puts secure phone on market

A telephone set that is almost impossible to bug is commercially available from West Germany's Munich-based Siemens AG. All openings and normally removable covers are either sealed or so designed as to foil any attempt to install objects in the S-phone. **Moreover, specially designed speech and ring circuits prevent electromagnetic parts from producing microphonic effects even with the receiver on the hook.**

Addenda

The Swedish government has appropriated \$7 million to finance the **definition phase of an experimental communications satellite called Tele-X**. Present plans are for it to be built mainly by Sweden's Saab-Scania and L. M. Ericsson for an eventual cost of \$100 million and to be launched in 1986 by France's Ariane 3. . . . The European market in short-haul fiber-optic data links—those less than 10 km long—will **grow to a less than spectacular \$13 million by 1985**, making it a very poor second to the several-hundred-million-dollar market there in telephone fiber optics, says J. Morris Weinberg, president of Fibronics Ltd., a Haifa, Israel, fiber optics manufacturer.

**Some day the digital
switching line circuit
will be this simple.**



You can design it today...

Technological leadership.

Cost-effective LSI simplifies central office and

First monolithic SLIC performs BORSHT functions and more . . . MC3419 now available in quantity.

Motorola's bipolar MC3419, the heart of the monolithic SLIC function, is available in quantity. Now production of the world's first transformerless, all-monolithic LSI digital switching line circuits can begin.

The 18-pin MC3419, with support from the Motorola MDA220 transient protection bridge and the specially-designed MJE270 and MJE271 Motorola power Darlington transistors, is all the silicon necessary to perform the BORSHT functions. In fact, the resulting SLIC can do more than the transformer-based circuit.



Availability of the unique new MC3419 SLIC completes the requirements for production of the world's first all-monolithic digital switching line circuits.

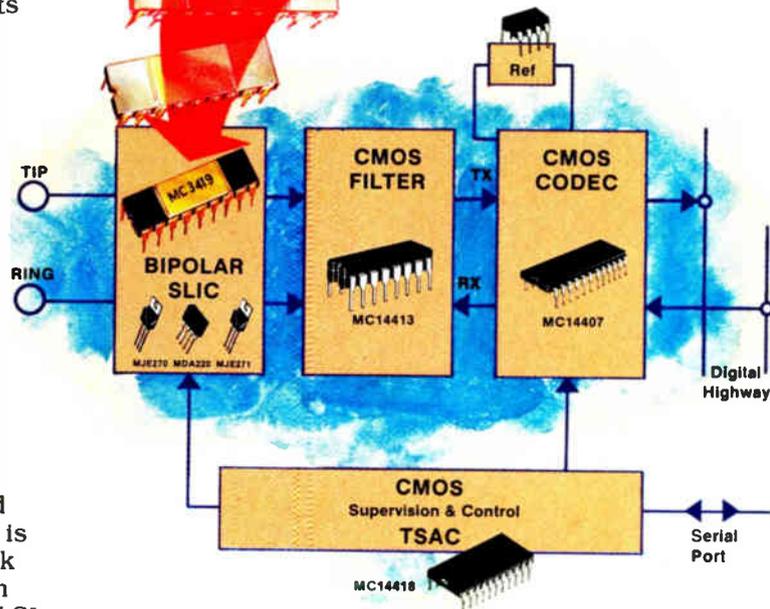
Battery-feed features include the options of feeding the loop resistively, in a current-limited mode or in a constant-current mode. The SLIC is automatically powered down during an on-hook condition. On a line card designed entirely with fully-compatible Motorola telecommunications LSI, one signal will power down the entire card. The power-down features not only save power, they also enhance reliability by minimizing average junction temperature.

Even when powered down, the line is continuously supervised for changes in hook status. That's also useful in line testing. Hook status and Ring trip outputs are provided.

Implementation of the 2-to-4-wire conversion hybrid function is fundamental to the SLIC. In fact, the IC technique used to provide this function is patented. Ground-fault, power line cross and 1500 V lightning protection are all features of the overvoltage and fault protection of the circuit.

The MC3419 is fabricated with Motorola's standard, well-characterized, high-volume linear bipolar process. Additional reliability is achieved by nitride junction sealing.

We recognize the importance to users of a strong second-source. A second-source announcement is anticipated during the first quarter of 1981.



System savings.

When the bipolar MC3419, with its three discrete power devices, is teamed up with Motorola's CMOS families of codecs, filters and TSACs, a cost-effective, low-power and space-efficient, quad line card can be realized. In fact, a bank of eight 7" x 7" quad line cards can be mounted within the area of a 7" cube. Even in such a compact configuration, heat dissipation is absolutely no concern thanks to the lower-power design approach.

In order to minimize component count and save board space, Motorola has taken the system approach to the design of components for the digital line card from the outset. Generic functions were identified, technologies carefully selected, and components designed to interface efficiently with each other as well as with the components of

design, saves space in PABX subscriber channel units.

Announcing the upward-compatible CMOS codec/filter PCM Monochip.

Codec, filter and voltage references are all combined in the MC14400 family PCM Monochips we will sample in Q1, 1981. These space- and power-saving CMOS components are completely compatible with existing Motorola codecs and filters, and with other industry-standard devices.

The general-purpose, 16-pin MC14400 provides on-chip voltage reference, pin-selectable TTL and CMOS levels, A-law and Mu-law companding and D3/D4/CCITT/Sign Magnitude formats, synchronous and asynchronous operation, on-chip transmit bandpass and receive low-pass filters.

The others, in 18-pin and 22-pin packages, offer all features of the MC14400 and more. The MC14401 adds selectable

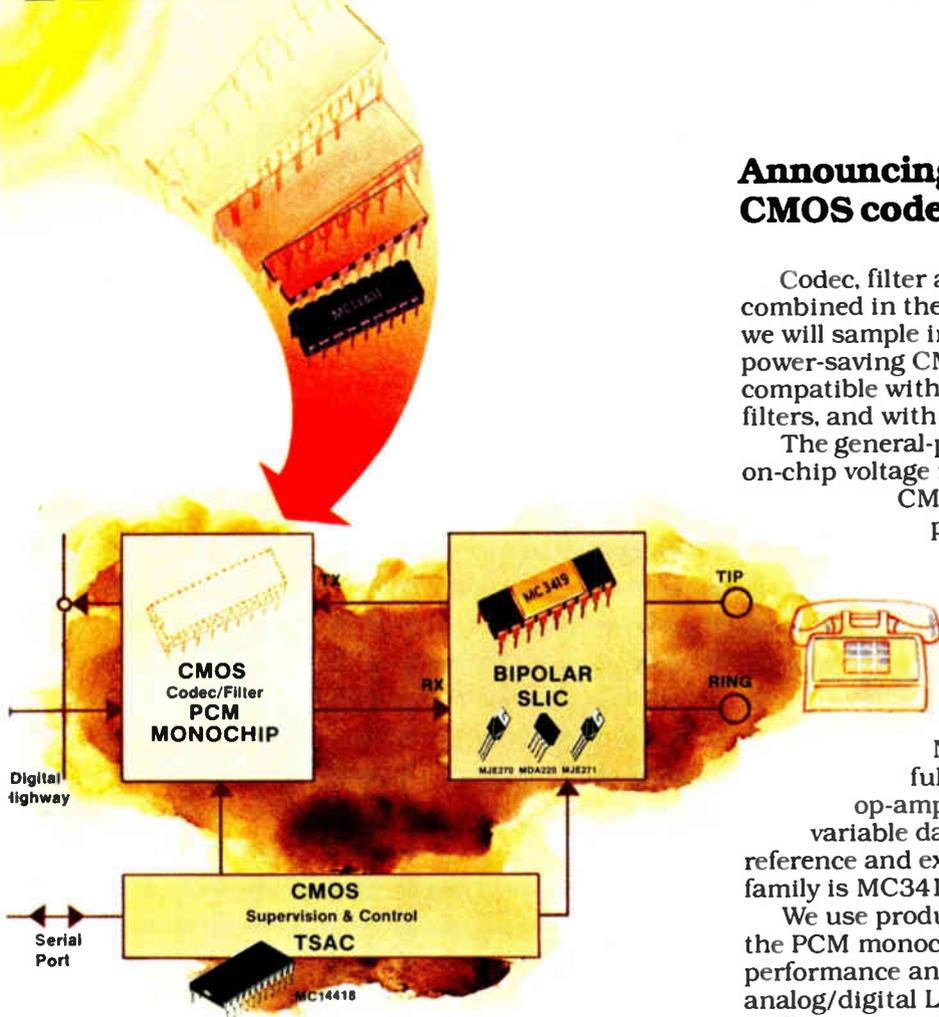
full-scale voltages and an input op-amp. The MC14402 also accepts

variable data clocks, external voltage reference and external gain adjust. The entire family is MC3419-compatible.

We use producible, tried-and-true CMOS for the PCM monochips for its reliable low-power performance and proven success for complex analog/digital LSI.

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other suppliers. Features like the single power-down control were designed in from the beginning.

We also recognized that not all functions were generic. The technique for assigning time slots, for example, was seen as heavily dependent on system architecture. Consequently, time slot assigner functions are not integrated into the generic parts, but are offered in a family of stand-alone Time Slot Assigner Circuits (TSACs).

Motorola's commitment to supporting the telecommunications switching market continues into the future. We project, among other things, that the ultimate codec/filter standard will be a 16-pin CMOS PCM Monochip.

Your next opportunity for refining digital switching line circuits will come soon with our MC14400 family of low-power CMOS codec/filter PCM Monochips.



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with remarkable ease. A light pen, data tablet or high-performance digitizer give you flexible options for entering data. And 3-D rotations allow you to view objects on the CRT from any desired angle.



HP Series 9800 desktop to focus on the facts.

For monochromatic applications, the System 45B, as well as our new, low-cost HP 85, also provides advanced graphics software. And when you add an input peripheral and our four-color plotter, you've got a full-function graphics workstation—a completely integrated computing system that operates under your own personal control.

Power you can get your hands on.

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start solving problems as soon as you turn the computer on; and reliable, low-maintenance operation.

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Our new S2200 introduces a whole new dimension in 4-bit microcomputers for control applications. With a combination of software and hardware features so incredible, you'll wonder how we got them all on one chip.

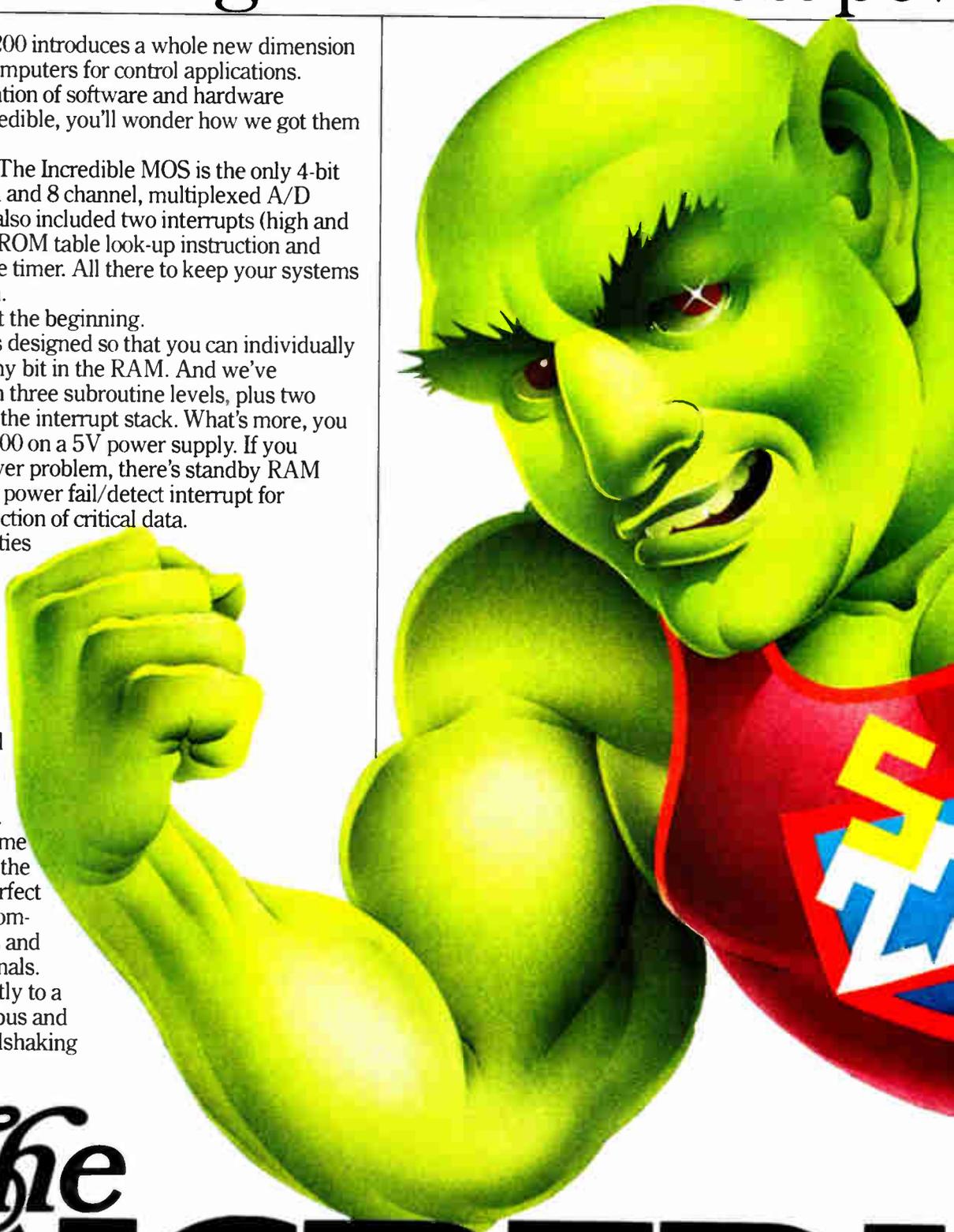
For starters, The Incredible MOS is the only 4-bit MCU with D/A and 8 channel, multiplexed A/D on chip. We've also included two interrupts (high and low priority), a ROM table look-up instruction and a programmable timer. All there to keep your systems costs way down.

But that's just the beginning.

The S2200 is designed so that you can individually test and clear any bit in the RAM. And we've equipped it with three subroutine levels, plus two more if you use the interrupt stack. What's more, you can run the S2200 on a 5V power supply. If you ever have a power problem, there's standby RAM capability and a power fail/detect interrupt for maximum protection of critical data.

With capabilities like these you can use The Incredible MOS for everything from appliance and home entertainment products to industrial controls and automotive instrumentation.

And we've come up with a clone (the S2300) that's perfect for distributed computing networks and intelligent terminals. It connects directly to a microprocessor bus and does all the handshaking automatically.



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| S2210/S2310 | 1.0 | 64 | |
| SA2210/SA2310 | 1.0 | 64 | X |
| S2215/S2315 | 1.5 | 96 | |
| SA2215/SA2315 | 1.5 | 96 | X |
| S2220/S2320 | 2.0 | 128 | |
| SA2220/SA2320 | 2.0 | 128 | X |

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Digital n-MOS chip handles analog signals at record 200 kHz

by Raymond P. Capece, Technical Managing Editor

Fast arithmetic and logic unit, two data buses let processor sample input fast enough for stereo audio applications

The high-speed digital processing of analog signals has long eluded n-channel MOS technology. But now, through the use of fast multiplier hardware and a multiple-bus structure, a single-chip processor from Intermetall GmbH of Freiburg, West Germany, achieves a sampling frequency of 200 kilohertz, unprecedented for an n-MOS device.

"That's more than adequate for two multiplexed channels of stereo audio, plus a third channel that might be used for matrixing or other information," explains Edmund Zähringer, head of hardware concept engineering at the company, which is the lead house of the ITT Semiconductors Group. A full 16-bit input and output certainly brings high-fidelity audio within reach of the MAA 1000, whose other targets include telecommunications, speech analysis and synthesis, radar and sonar, and biomedical applications.

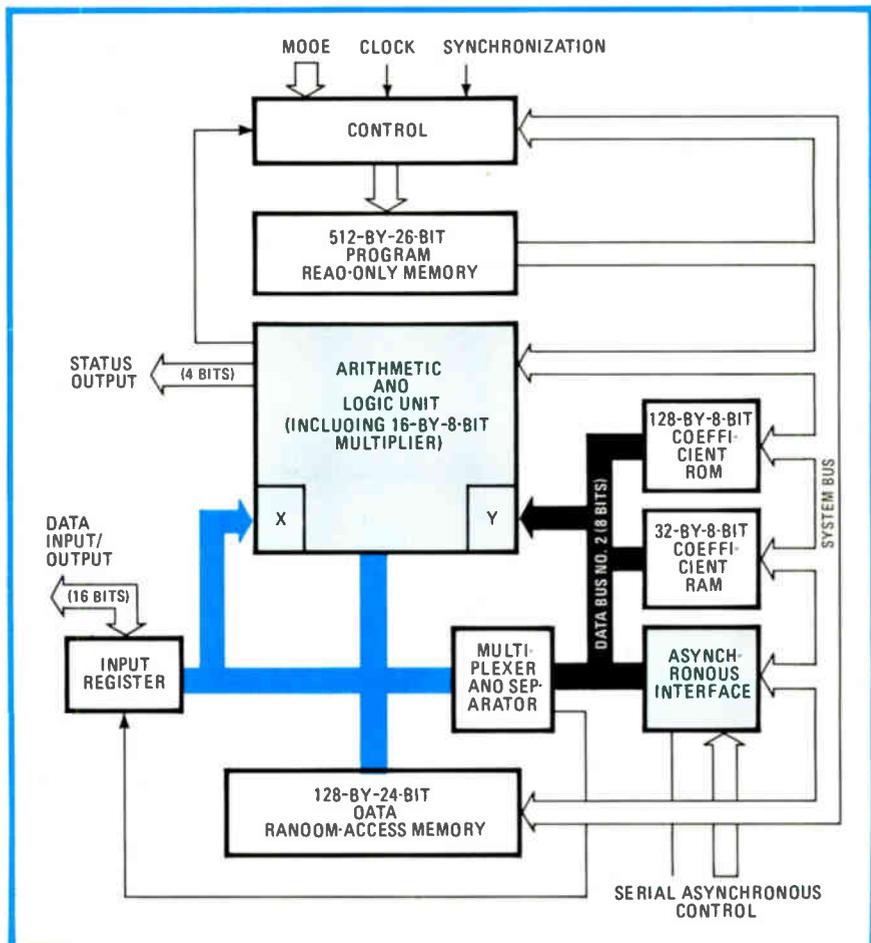
Details. The 35-square-millimeter (54,250-square-mil) device is fabricated conventionally enough with a standard enhancement-depletion n-MOS process and 3-micrometer gate lengths. It owes its very high sampling rate, derived from a 20-megahertz clock, entirely to its architecture. As Zähringer notes, "signal processing is essentially multiplication and addition," and even filtering speech may require over 100,000 multiplications and addi-

tions per second.

Accordingly, the MAA 1000 relies on a fast arithmetic and logic unit that performs a 16-by-8-bit multiplication with accumulation in 250 nanoseconds. By comparison, the fastest competitive n-MOS signal processor, Nippon Electric Co.'s μ PD7720, takes that long just to multiply. Other MOS signal processors, such as Intel Corp.'s n-MOS

2920 and American Microsystems Inc.'s v-MOS S2811 [*Electronics*, Feb. 14, p. 100], barely get to an 8-kilohertz bandwidth and are not nearly adequate for digital audio.

Two buses. But, as shown in the figure, the Intermetall part also gets its speed from two data buses that can load the ALU with two operands simultaneously to save time. The basic operation of multiplying and



Performer. Intermetall's n-MOS signal processor attains its 200-kHz sampling rate by combining a fast 16-by-8-bit multiplier with a dual-bus structure that speeds data flow.

adding is performed unlocked in the ALU. Key to the dual-bus architecture is the multiplexer and separator function, which lets both data buses be active simultaneously and also allows the first bus to transfer data to the second bus a byte at a time whenever calculations with multiple-byte accuracy are needed. Internally, calculations are made with an accuracy of 24 bits.

The personality of the MAA 1000 is determined by an on-chip masked read-only memory holding a maximum of 512 26-bit microprogramming words. "The wide instructions save time," Zähringer explains, "since they employ direct addressing and are not decoded." Another masked ROM of 128 bytes stores fixed coefficients, variable coefficients are stored in a 32-byte random-access memory, and finally, a 124-by-24-bit RAM serves as the work space for ALU calculations.

One use. In a typical application, the MAA 1000's program ROM would contain several subprograms, each serving a specific task. Unlike Intel's 2920, however, which runs through its entire program once in each sampling instant, the MAA 1000 allows program branching that is dependent either on internal results or on external conditions provided via the mode input, for example. Further flexibility is afforded by the device's asynchronous serial input, over which coefficients can be loaded into it, for example.

In a digital stereo system, a single MAA 1000 could handle both channels as well as any digital information used for, say, quad matrixing or station identification. All the actions of a stereo system's controls, such as balance, treble, base, and volume, could be digital and entered through the MAA 1000's serial port. Finally, the chips could be cascaded with no loss of fidelity.

Intermetall is involved in developing a portfolio of digital signal-processing chips. A simpler version of the MAA 1000, providing 12-bit resolution on a 27-mm² (41,850-mil²) chip, is intended for stereo systems and video processing.

For its telecommunications busi-

ness, the company has also developed a pair of complementary-MOS signal-processor chips—a programmable multiplier and a processing register IC—that dissipate a maximum of 70 milliwatts. With maximum clock rates of 4.5 MHz and an internal accuracy of up to 41 bits,

the parts are intended for such applications as adaptive echo canceling, programmable delay, and speech analysis and synthesis.

The two C-MOS devices will be made available next March, and the MAA 1000 will bow around the middle of the year.

Japan

Magneto-microwave plasma etcher can define 0.2- μ m line widths without undercutting

To judge by the newest wafer lithography equipment to come on the market in Japan, even submicrometer chip geometries will soon be commonplace. Half a micrometer is the line width for which Hitachi Ltd. has optimized its magneto-microwave plasma-etching system [*Electronics*, Nov. 20, p. 63], though the equipment can produce devices with 2- to 0.2- μ m features.

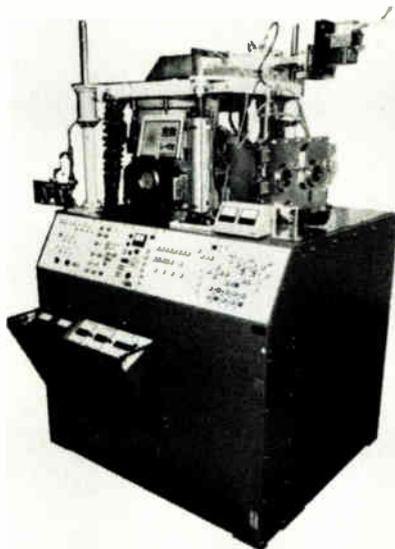
Unique. The first of its kind in the world, the HE-818 system uses a combination of electric and magnetic fields to sustain the plasma. The process requires an overall gas pressure of only 10^{-4} torr, or one hundredth the pressure required by parallel-plate reactive-ion etchers like

Toshiba's recently announced 1- μ m system [*Electronics*, Nov. 6, p. 76]. One advantage of this low pressure is that the uncharged reactive radicals that hit the wafer at oblique angles are reduced a corresponding 100 times in density, so that they cannot undercut even lines much less than a micrometer wide, thus guaranteeing the system's capability for submicrometer features.

The microwave electric field that helps generate the plasma is produced by a cooker-type magnetron operated at a reduced power output of about 80 watts. The magnetic field is generated by solenoid electromagnets and permanent magnets. Suitably adjusted, the two fields yield cyclotron resonance that causes a cloud of electrons to trace circular paths in the region over the wafer to be etched. Collisions between the electrons and gas molecules provide both the reactive ions that do the desired anisotropic etching and more electrons to keep the process going. The resulting ion density is higher than in other systems, despite the lower gas pressure.

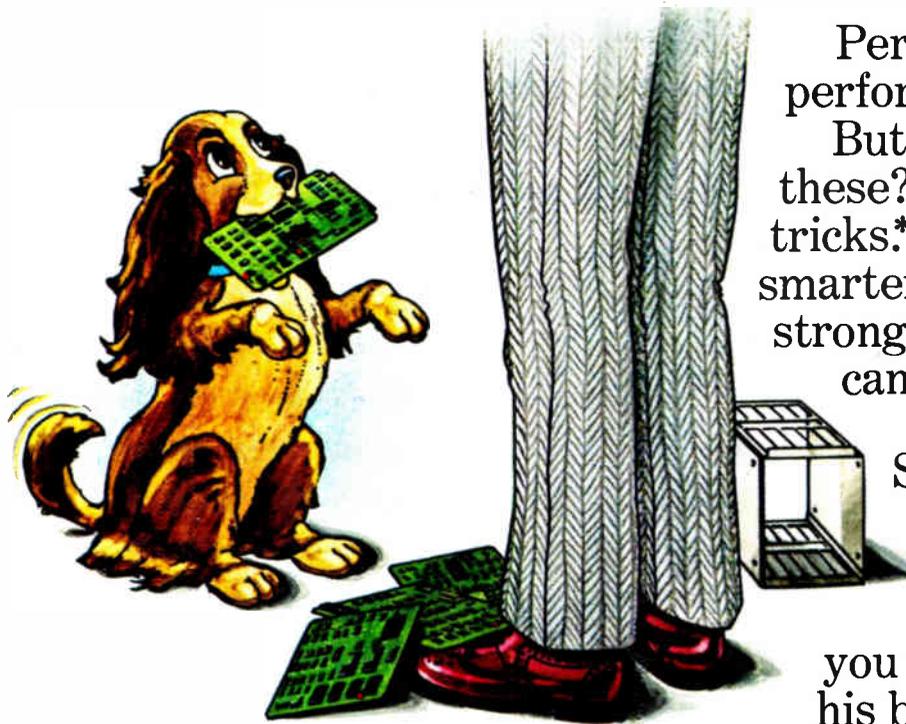
Any electrons attempting to rise out of the desired region are reflected back into it by a component of the magnetic field called a mirror field. Those electrons that strike the wafer below charge it negatively to a voltage of -20 v.

Negative attraction. It is this -20-v charge that attracts the positive ions that do the anisotropic etching. Because their energy, too, is so low, they cannot damage even resists of the type with a low melting tem-



Double blessing. In Hitachi's plasma etcher, magnetic and electric fields boost reactive-ion density, and low gas pressure reduces incidence of damaging radicals.

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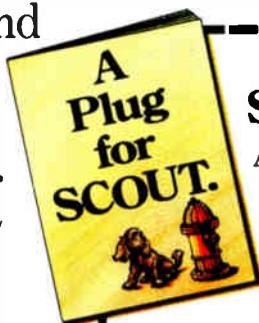
If you were an OEM, would you like SCOUT? Of course you would.

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perature that are used for electron-beam lithography.

With the proper choice of gas, the material that must be removed is etched away rapidly and other materials are removed more slowly. For example, silicon hexafluoride, or SiF₆, etches polysilicon 30 to 100 times faster than silicon dioxide, 10 to 30 times faster than silicon nitride, and 6 to 10 times faster than a typical electron-beam resist. Furthermore, the gas given off by the reaction of silicon and fluorine until the etching is completed indicates the endpoint of the process, for its blue-green glow can be monitored by a photosensor looking through an optical filter.

The plasma covers the area of only one of nine wafers carried on a rotating turntable but takes only 3 or 4 minutes to etch it. That is less than double the per-wafer time of other plasma-etching systems that process

all wafers simultaneously but use the less efficient carbon fluoride gas to do so. Moreover, the wafers cool between passes through the plasma, eliminating any need for forced cooling. The turntable can handle 3- and 4-inch wafers, which are transported automatically to and from it by 25-wafer cassettes.

Cleaner. Since electrodes are not used to generate the plasma, they cannot sputter contaminants onto a wafer that later need to be cleaned off. Also, so little gas is needed by the low-pressure system—about 1 cubic centimeter per minute as against the 100 cc/min of other plasma-etching equipment—that less of it goes to waste or ends up as soil on the system's interior, reducing maintenance costs.

The HE-818 will sell for \$235,000 in Japan and will be available there in the second half of next year at the earliest.
-Charles Cohen

Great Britain

Microcoding lets 2900 computers switch fast between different architectures

A perennial problem for computer manufacturers is how to preserve a customer's existing investment in software when he moves up to an architecturally more advanced system. One of the more elegant solutions is Concurrent Machine Environment, a new operating system announced last month by Britain's International Computers Ltd.

CME enables various 2900 mainframes from ICL to run application software written for the earlier-generation system 4 or series 1900 computers simultaneously with application and development programs written for the 2900 native-mode Virtual Machine Environment. The development depends on an extension of the microprogramming techniques that the Putney, London-based company has long put to use on its low- and mid-range 2900 machines with the goal of providing former users of older systems with an easy migration path to VME. (In essence, micropro-

gramming defines a computer's architecture in terms of look-up tables stored in read-only memory and may in effect give the machine a choice of two or more architectures—an impossibility with hardwiring.)

Forerunner. As a first step toward encouraging that shift to VME, ICL developed the Direct Machine Environment, also a microprogrammed operating system. By enabling the low- to mid-range 2900s to emulate the previous generation of machines, DME permits former users of those earlier machines to run their old software on their new computers. Then to develop and run new programs, the users can switch back to the 2900's native-mode VME. But the fact that the 2900 has to be run in either DME or VME a shift at a time makes it hard to schedule jobs for different operating systems while developing new application programs.

With CME, ICL engineers have

moved a stage further in microprogramming technology. By time-slicing between, or interleaving, the microcoded architectures, they have produced a completely chameleon-like computer whose user can adjust the proportion of time it spends in either the CME or the VME mode to match its work load. Thus, they explain, "specialist systems written for 1900 operation can run in a portion of the machine to the end of its useful life," while the major work load can exploit the VME mode.

Extra. Moreover, an additional facility called Adram 1900 allows programs running in the VME mode to access data files stored in the 24-bit-word data format of the 1900 series. It automatically converts them into the byte-oriented 32-bit-word format of the 2900.

Basically, "CME is a microcode harness that permits operating systems to run in parallel within the same hardware environment, at the same time," says ICL. The microcode is modular and can be tailored at load time to provide a configuration suitable for the support of specific work-load regimes. This facility, explains product marketing manager Terry Ward, allows the user to gradually transfer resources from one operating system to the other.

The modules include one that interprets and executes DME instructions, another that interprets VME order code, and a third for CME. The CME module is the controlling microprogram—it integrates the functioning of all the other modules and controls the sharing and switching of peripherals and central processor time. There are also input/output and error-handling microprogram modules.

CME will now be available on all of ICL's microcoded 2900 models up to the 2966 [*Electronics*, Nov. 20, p. 64]. More powerful machines than this will likely remain hardwired. "Eventually one has to trade the flexibility of microprogramming for the inherently higher performance of hardwired systems," explains one ICL marketer. So to run older application programs on its largest 2972 and 2982 models, ICL twins a

ROI — Two actual cost/engineering studies*

| | Electronics Manufacturer | Appliance Manufacturer |
|--|-----------------------------|---------------------------|
| Quantity of PC board designs | 9 | 2 |
| Quantity of boards run/year/design | 47,000 (Av.) | 120,000;180,000 |
| Quantity of components/board | 83 (Av.) | 89;50 |
| Total boards produced/year | 420,000 | 300,000 |
| Grand total component insertions | 34,860,000 | 19,680,000 |
| Operating costs/year | | |
| Manual assembly | \$577,942. | \$254,761. |
| Automatic assembly | \$ 74,714. | \$ 41,526. |
| Net capital requirement (Investment in Universal automatic assembly equipment, less estimated equipment & tooling costs for manual assembly) | \$198,329. | \$ 92,590. |
| Net Savings | \$304,899. | \$120,645. |
| Payback | 5.6 months | 6.3 months |
| Return on Investment | 253% | 230% |

*These 1979 studies were made by Universal for two well-known producers of equipment for the consumer market. We will be glad to send you copies of the complete studies, with the names of the customers deleted. They include detailed cost analyses based on actual labor rates, assembly time studies, overhead costs, etc.

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Nearly 90% of all printed circuit boards can be automatically assembled at high speed with systems that Universal has developed. And rapid pay-back can be obtained on short runs with a high mix of products as well as on long high volume applications. Our customer files include dozens of cost analyses like the two briefly summarized here. Send us your production requirements and costs. We'll be glad to work up a complete analysis to show you how much "going automatic" can save your company.

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Electronics international

2960 microcoded processor with the hardwired processor.

ICL announced the CME operating system last month as part of a package of 30 new hardware and software products. Also unveiled were two new mid-range mainframes: the 2966, with a performance up to three times that of the 2956 from which it is derived, and the 2955, which is 20% more powerful than the 2950.

Included in the package were new high-density 780-kilobit-per-second tape drives plus a downward extension of ICL's larger system-program development aids for smaller systems in the 2900 range. The package may help to boost the company's sales, which have slipped in the second half of 1980 as a result of a home recession and an expensive pound in export markets. **-Kevin Smith**

Great Britain

Low-cost terminal aims to enlarge the market for viewdata services

To date, fewer than 7,000 viewdata sets have been sold in Britain, and businessmen have bought most of them—which adds up to a disappointing demand for telephone access to remote data bases. According to Plessey Telecommunications and Data Systems Ltd., the fault lies with the high cost and inappropriateness for office use of most of the terminals developed so far—mainly modified color television chassis selling for over \$2,000.

The new Vutel terminal from the Beeston, England, company is therefore little more than "a feature tele-

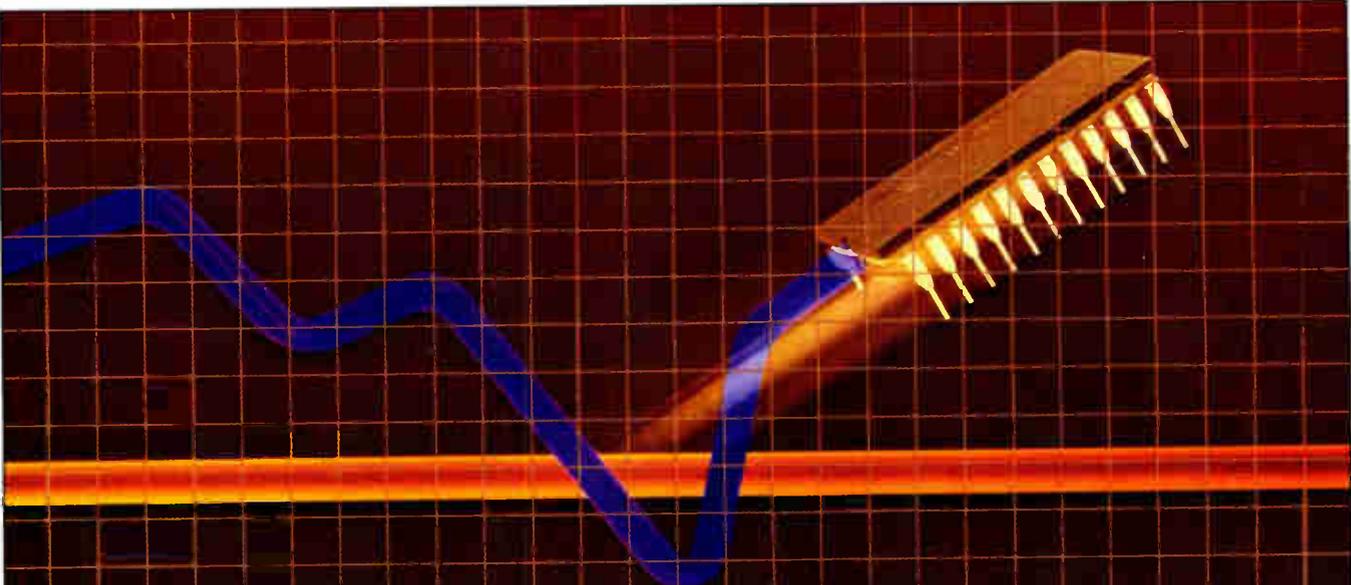
phone," to quote marketing manager Roger Boardman. Incorporating a 6-inch black and white TV screen, a telephone handset, a keypad with loop disconnect or multifrequency dialing, and a modem that receives 1,200 bits per second and transmits 75 b/s, it could sell for as little as \$720 when in volume production.

Legal aid. Moreover, Plessey expects its sales will be helped by the legislation about to go through Parliament that will liberalize the telephone terminal monopoly of British Telecom, part of the British Post Office, and so allow the company to



Good for business. With its small black and white TV screen and inexpensive membrane keyboard, Plessey's Vutel terminal lowers the cost of gaining access to viewdata services.

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Whether you're ready for factory networking now, or choose to develop a layer at a time, TSA will take you there at your own pace, with solid value and maximum productivity all along the line.

To help you get more out of your test systems and learn more about our Test System Administrator, we've put our thinking about distributed industrial management systems into a new booklet, yours for the asking. Write Teradyne, 21255 Califa Street, Woodland Hills, CA. 91367, or call your nearest Teradyne sales office.

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OE CRYSTAL OSCILLATOR ELEMENTS

International's OE Series of Crystal Oscillator Elements provide a complete crystal controlled signal source. The OE units cover the range 2000 KHz to 160 MHz. The standard OE unit is designed to mount direct on a printed circuit board. Also available is printed circuit board plug-in type.

The various OE units are divided into groups by frequency and by temperature stability. Models OE-20 and OE-30 are temperature compensated units. The listed "Overall Accuracy" includes room temperature or 25°C tolerance and may be considered a maximum value rather than nominal.



All OE units are designed for 9.5 to 15 volts dc operation. The OE-20 and OE-30 require a regulated source to maintain the listed tolerance with input supply less than 12 vdc.

Prices listed include oscillator and crystal. For the plug-in type add the suffix "P" after the OE number; eg OE-1P.

OE-1, 5 and 10 can be supplied to operate at 5 vdc with reduced rf output. Specify 5 vdc. when ordering.

Output — 10 dbm min. All oscillators over 66 MHz do not have frequency adjust trimmers.

| Catalog | Oscillator Element Type | 2000 KHz to 66 MHz | 67 MHz to 139 MHz | 140 MHz to 160 MHz | Overall Accuracy | 25°C Tolerance |
|----------------|-------------------------|-----------------------|-------------------|--------------------|---------------------------|---|
| | | | | | | |
| 035213 | OE-1 | \$15.66 | | | ± .01% -30° to +60°C | ± .005% |
| 035214 | OE-1 | | \$17.99 | | | |
| 035215 | OE-1 | | | \$22.63 | | |
| 035216 | OE-5 | \$19.44 | | | ± .002% -10° to +60°C | ± .0005% 2 - 66MHz ± .001% 67 to 139 MHz ± .0025% 140 to 160 MHz |
| 035217 | OE-5 | | \$22.91 | | | |
| 035218 | OE-5 | | | \$30.17 | | |
| Catalog Number | Oscillator Element Type | 4000 KHz to 20000 KHz | | | Overall Accuracy | 25°C Tolerance |
| 035219 | OE-10 | | \$22.91 | | ± .0005% -10° to +60°C | Zero trimmer |
| 035220 | OE-20 | | \$33.65 | | ± .0005% -30° to +60°C | Zero trimmer |
| 035221 | OE-30 | | \$69.63 | | ± .0002% -30° to +60°C | Zero trimmer |



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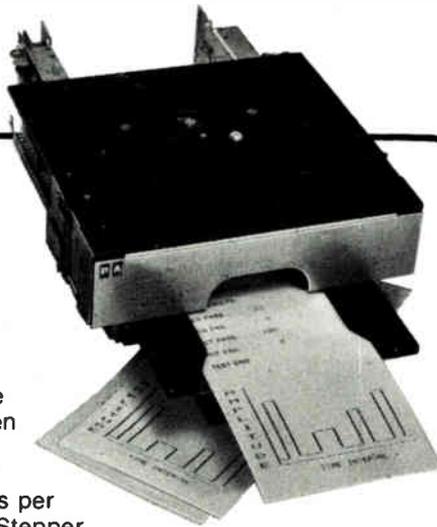
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Our Alphanumeric Ticket Printer

For total versatility use our DMTP-9 programmable ticket printer to print the full alphanumeric ASCII character set. Print with ribbon on standard tickets, cards or single-sheet forms, or use impact-sensitive paper for multiple copies. Even program character pitch to handle standard or enhanced printing of up to 48 characters per line on 39- to 59-line tickets. Stepper motor advance for 6 lines to the inch or .110" for graphics.

Mountable on tabletop or wall, the DMTP-9 does it all with advanced stepper motor control electronics and a long-life needle matrix print head. For still more versatility, get it with the optional controllers, power supplies and interconnect cables systems for complete microprocessor/microcomputer compatibility, too. But first, write or call to get more details. Ask for Bulletin 924.



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86 Circle 239 on reader service card

Electronics International

sell the device directly to the public.

Introduced initially for \$840, the first version provides a loudspeaker and on-hook dialing facilities, as well as single-button access to the Prestel data base provided by British Telecom. Later models will incorporate a full alphanumeric keyboard, short-number dialer, printer and cassette interfaces, number display, and time and alarm, call-cost and -metering, and notepad facilities. The nearest competitors are Pye TMC Ltd. and Standard Telephones & Cables Ltd., both of whom have produced black and white business terminals selling for around \$1,300.

To cut costs, Plessey has leaned heavily on its own telephone manufacturing expertise. An example is the low-cost membrane keypad developed originally for what is called the inexpensive telephone project, a joint venture by Plessey, GEC Ltd., and Pye TMC Ltd.

Smart. The terminal also uses a viewdata chip set developed by Glenrothes, Scotland-based General Instrument Microelectronics Ltd. and built around GI's PIC 1650 8-bit microcomputer. To this Plessey has added a second microcomputer chip in order to provide the full Vutel complement of facilities.

Included in the chip set is a feature that could double the height of the characters displayed on the small Vutel screen. Plessey notes that for close viewing at infrequent intervals, the screen's definition is adequate. But should continuous viewing prove to be in demand, the system could be adapted to display each viewdata page in two enlarged halves.

Through the Vutel terminal, businessmen will be able to access over 150,000 pages of information on banking, insurance, shipping, the stock market, and commodities available through the Prestel data base. Just as significantly, the terminal could be used to access internal viewdata systems and thus be central to the Beeston company's emerging strategy for entering future markets in office systems in which voice, text, and data equipment will converge. The Vutel terminal will go on sale next year.

-Kevin Smith

Now CMOS cuts your design time.

Now there's another good reason to switch to CMOS.

COSMAC System IV: The complete 1802 hardware, software Microprocessor Development System.

Full-screen editing. The COSMAC System IV features an integral CRT display screen with built-in "true" full-screen editing.

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Choose from three high-level languages: BASIC 1, BASIC 2, or PLM-1800.

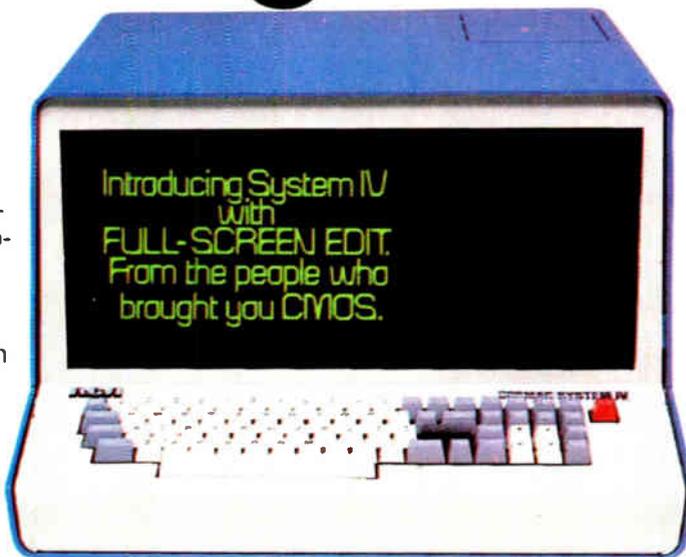
If you already own our 005 or 007 system, move up to full-screen editing with our smart CRT terminal upgrade (CDP18S040).

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The \$12,000* total System IV price also includes total design support from the people who brought you the 1802.

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For more information or a System IV (CDP18S008) demonstration, contact your local RCA Solid State sales office or distributor. Or contact RCA Solid State Headquarters in Somerville, New Jersey. Brussels, Belgium. Hong Kong. Sao Paulo, Brazil. **Or call Microsystems Marketing toll-free (800) 526-3862.**



*optional resale price

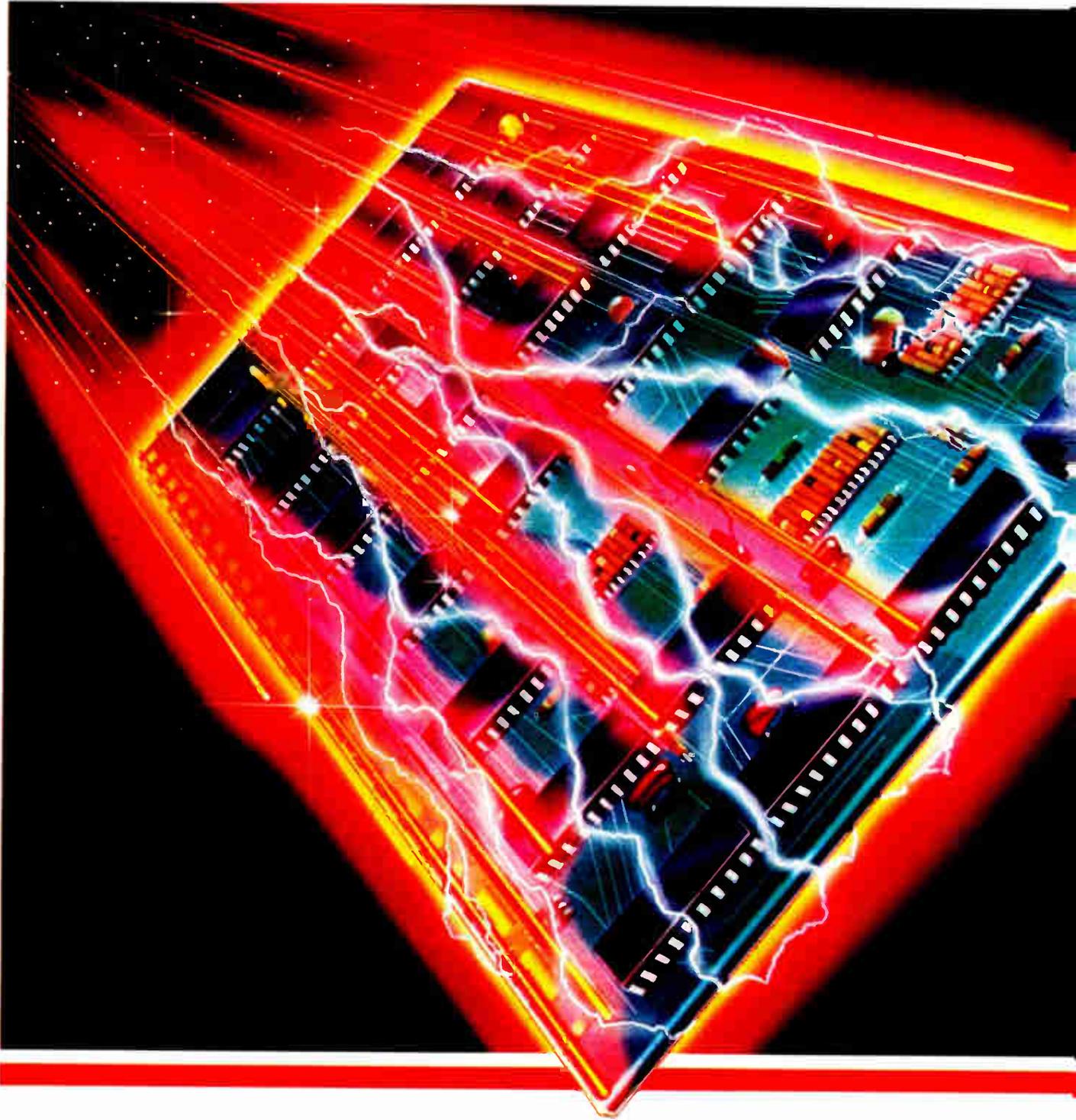
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across the board.

How STC speeds production testing by a factor of five to one . . .

Storage Technology Corporation's revolutionary 8650 Winchester disc subsystem for big, main-frame computers utilizes double-density recording to pack twice the normal amount of data in the same space as a conventional, single-density disc.

Critical to the success of this technology are complex, high-speed, analog read/write and servo boards. In fact, STC's read/write board contains more than 350 separate active and passive components.

When conventional methods were used, it took approximately 15 minutes to test each board. As this testing time became more and more unacceptable, the decision was made by STC to switch to automatic testing.

Paul Zieschang, Manager of Hardware Development, recommended that the company assemble its own system using 12 HP-IB compatible instruments, an HP 9835A Desktop Computer as system controller and a 9885 Disc. Zieschang reports that the 9835A was chosen because its large CRT display made it easy for an operator to interface with the system, and



because of its programming ease. What's more, STC incorporated diagnostics into the system which help STC technicians better understand the testing procedure. This software even helps technicians locate — via a flashing cursor and a graphic display of the board's topology — the position of any component on the board. Finally, the 9835A also delivers a print-out of the component's value and STC part number.

Documentation simplifies system configuration.

According to Zieschang, some of the many application notes supplied by Hewlett-Packard were helpful both in deciding the first configuration and speeding assembly of STC's first HP-IB system.

Flexibility that reduces the chance for obsolescence and speeds assembly.

Twelve HP-IB compatible instruments were chosen for this system, according to Zieschang, because HP's bus architecture and programming ease permit the flexibility necessary to make changes within the system as STC's requirements change and, thus substantially reduce the possibility of system obsolescence.

HP instruments also provide STC with speed of assembly. The company assembled and programmed its first automatic



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 for systems”
 instruments
 and computers.

test system faster than other comparable ways of solving its system test needs. Zieschang believes they will be able to assemble and program future systems even faster.

The bottom line.

Just as important, Zieschang says the STC HP-IB compatible system will reduce testing time from 15 minutes per board to approximately three minutes. A factor of five to one. The system is also expected to reduce the time required to debug faulty boards from 45 to 20 minutes. In short, STC's HP-IB system will help the company turn out more boards per day.

Why not consider the HP-IB solution for your production test needs? For complete details, send for our brochure, “Do your own system design in weeks, instead of months.” Simply write to Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.



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NEC NEWSCOPE



RAPID START IN HIGH-SPEED G3 FACSIMILES

NEC is supplying domestic and overseas customers with high-speed facsimile equipment that meets newly established international standards (G3).

The first overseas user of NEC's G3 equipment is a major broadcasting network in the United States. The equipment has been specially design-

ed for the American market and is sold under the brand name NEFAX 180.

In Japan and other countries, NEC's G3 facsimiles are called NEFAX-6200. The first domestic units were delivered to a Tokyo whisky distilling company in February 1980.

High-speed facsimile equipment has a great potential for intra-country or

international communications because it offers higher efficiency than medium or low-speed products. However, incompatibility between the models of different manufacturers was a problem until the CCITT set international standards last November.

Since the G3 standard was adopted manufacturers have been racing to market equipment that meets it. By taking the lead in this race, NEC has proved that its facsimile equipment is one crucial step ahead in a highly competitive market.

Circle 259 on reader service card

ADVANCED RADAR
SYSTEM FOR
SINGAPORE

Singapore's new Changi Airport is putting safety first with an advanced approach control radar (ACR) system to control taking-off and landing. The NEC system consists of primary surveillance radar (PSR) with a range of 64 nautical miles, and secondary surveillance radar (SSR) with a coverage of 128 nautical miles. The system can display aircraft at altitudes up to 40,000 feet.

The new ACR system features special bright displays with digital scan-converters to reduce eyestrain for air controllers. Conventional displays are operated in a darkened room. NEC display screens can be easily observed even in a bright room because they are ten times brighter than conventional equipment.

Another significant feature of the system is its ability to track and display aircraft positions using alpha-numeric symbols on a large (40 cm) flat display screen. Better tracking and less eyestrain add up to an extra margin of airport safety.

The ACR system is integrated with the airport's long range radar and display system to improve the flexibility and efficiency of air traffic control.



Circle 260 on reader service card

MNC-80A PORTABLE CAMERA
FOR ACTION TV.

TV audiences are demanding more dynamic and varied programs. This, in turn, creates a need for versatile, high-performance cameras that can be used with equal ease in the studio or out on location. NEC has been responding to this need with a growing line-up of advanced television cameras.

The latest offering is the MNC-80A series fully self-contained portable color camera. Light enough for hand-held operation, it is engineered for maximum stability and reliability both in the studio or out



in the open air.

The MNC-80A weighs only 4.5 kg and measures 260mm (h) x 100mm (w) x 293 mm (d).

Yet it produces pictures of astounding clarity, and because its circuitry is based on extensive use of LSIs, the MNC-80A consumes significantly less power than comparable cameras. In fact,

it runs on a mere 24 watts.

The MNC-80A series comes with a wide range of accessories; models are available for NTSC, PAL, PAL-M and SECAM standards. Circle 261 on reader service card

INDIA SWITCHES TO
SPC PHONE SYSTEM

In a determined move to improve both domestic and international telephone services, India is introducing its first electronic switching systems.

NEC will manufacture and supply four ND 10 toll switching systems for the Posts and Telegraphs Department. In addition, NEC will supply three NXE 20 international switching systems to the Overseas Communications Service. Both ND 10 and NXE 20 are space-division, fully-stored-program controlled electronic switching systems.

Circle 93 on reader service card

The four ND 10 systems will be installed in New Delhi, Bombay, Calcutta and Madras. They will open a total of 15,000 circuits. The ND 10 is capable of accommodating up to 160,000 local or 64,000 trunk lines.

The three NXE 20 systems will be installed in Bombay, New Delhi and Madras. Accommodating a total of 925 international circuits, they will improve telephone services and traffic to and from India. The NXE 20 system has the capacity to handle up to 4,000 terminals.

NEC

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A/D



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TL507 Converter

At \$0.66* it's our lowest cost converter. Single-slope for use with TI's TMS1000 and virtually all microprocessors. I²L

technology makes it possible to offer this monolithic chip at such low cost, and in a small 8-pin DIP. 7-bit resolution, 1-ms conversion speed, single supply operation and 25-mW (typ) power consumption at 5 V are more good reasons to design in TL507.

TL500 Series

Converter systems consisting of analog and digital processors, as follows:

- TL500/TL501 analog processors . . . TL500 is a high-performance converter for high accuracy applications with features such as:

- full 4½-digit accuracy
- 0.005% linearity
- automatic zero and polarity
- high input impedance — 10⁹ Ohms (typ)
- use with TL502 for complete 4½-digit system

TL501 is a low-cost converter with all the features of TL500 except accuracy is 3½ digits, linearity 0.02%.

- TL502/TL503 digital processors . . . TL502 logic control interface is designed for use with TL500, TL501 or TL505 converters and drives common anode 7-segment displays such as TIL321. Single 5-V supply, 20-mA

digit-base drive outputs and 100-mA internal segment drivers round out a long list of features and functions. TL503 controller shares TL502 features, except TL503 offers BCD outputs.

TL505 Converter

A low-cost, dual-slope converter for high volume applications, TL505 is ideally suited for use with TMS1000 and most microprocessors, and/or TL502/TL503 digital processors, 3-digit (0.1%) accuracy, high impedance MOS input, automatic zero and single supply operation — and more.

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Quality Circle concept leads the way as new wave of management techniques reaches the U. S.

by Larry Waller, Los Angeles bureau manager

When Japanese manufacturers started to sharply increase their share of American markets, particularly in semiconductors, the reaction in the U. S. ranged from concern to hysteria. Then a consensus was reached that Japanese products sell well not only because they are readily available, as with semiconductors, but also because they are of high quality. And by now there is a new willingness to try to incorporate into American practice some of the management and production styles that led to the Japanese success. Of the many techniques being tried, perhaps the most popular and most misunderstood is the Quality Circle.

Although some skeptics believe that the growth of the QC movement in the U. S. is only a quick-fix reaction to Japanese quality standards, others see it as the first test of a more basic question: can the U. S. learn from the Japanese by adapting their management techniques to its own quality problems?

QCs themselves, in which small groups of workers meet to solve problems, seem simple to copy, but in Japan they grew out of a value system that is in direct conflict with Western attitudes. Those who draw this distinction most sharply are native Japanese executives with experience in running businesses in

both countries. They warn that the most treacherous pitfall is thinking it easy to ape what works well in Japan. For this reason, such veterans as Arthur Jonishi, vice chairman and chief executive of Kyocera International Inc., San Diego, caution against rushing into Quality Circles and other Japanese approaches without patient preparation.

"The differences are large—histo-



Take it easy. Kyocera vice chairman Arthur Jonishi, noting cultural differences between Japan and U. S., advises caution with Quality Circles.

ry, geography, size, and ethics all are involved," says Jonishi. "People in the United States are very individualistic; they largely came from Europe and are self-reliant. The advantage is creativity and originality; the disadvantage is a lack of faith in each other and distrust."

He knows whereof he speaks, heading what is recognized as likely

the most "Japanicized" firm in the U. S. A subsidiary of Kyoto Ceramic Co., with annual sales of its ceramic packages and substrates nearing \$200 million, the San Diego firm did not arrive quickly at its present balance between East and West. It went through a series of missteps, first trying to be too American and later moving too fast to embrace Japanese methods. Jonishi's admonition to would-be imitators: take it slow. "The first three or four years are by far the toughest," he advises.

With its panoply of Japanese management trappings (see "Managing the Japanese way," p. 100), Kyocera could serve as a model, but Jonishi and others note these are only an outward sign of more fundamental conditions. "Everything comes from unity and harmony. What we work for is not just putting the individual ahead, but a common cause, a company that will support us," he says. As is common in Japanese companies,

attitudes are judged most important, coming before even performance in salary reviews. Such priorities are likely to be difficult for U. S. managers to adopt, Jonishi admits.

They like QC. Nevertheless, many companies are rushing to try out Quality Circles, regardless of their deeper implications. An examination of the experiences of some American

Inside the news

electronics firms that have them offers a guide to some of the circles' benefits and pitfalls.

In Beaverton, Ore., Tektronix Inc. is moving fast to implement the program. William D. Walker, executive vice president and chief operating officer, sees it as conflicting little with American ways. The Japanese methods "will work here in the States, because many of them are simple, straightforward, common-sense things that need to be done and not neglected." Tapping employee skills and suggestions to improve quality and reliability, in fact, can work anywhere.

In this area, however, Tektronix might have a headstart. According to Walker, its workers always "have participated heavily in the decision-making processes." Certainly, from a 1979 start, the company now has some 250 Quality Circles made up of some 2,500 volunteers and growing so fast supervisor training cannot keep pace with them. Moreover, Tektronix sees even more potential in extending them to include vendors. "The me-first attitude can be largely overcome if companies begin

to work to make their goals compatible with those of individuals," Walker thinks.

Silicon circles. Semiconductor firms in California's Silicon Valley also have been quick off the mark with Quality Circles. Already reporting first-rate results is Fairchild Camera & Instrument Corp. in Mountain View, which started QCs in its Advanced Bipolar division early this year and now has 18 throughout the company. Although admitting it is hard to measure results precisely, Fairchild is sure its program is having a major impact. In a single bipolar department, for instance, production losses are down to 1% to 2% a day from the pre-QC level of 20%.

Advanced Micro Devices Inc. in nearby Sunnyvale has also instituted QCs and like Fairchild sees them as a critical part of an overall quality awareness. Both firms believe their survival in the world semiconductor market could hinge on how well the QCs work, but both also admit that implementing the circles is neither simple nor inexpensive, as it involves training and time.

Still, the welcome the QCs have received from workers has been eye-opening. At Fairchild, management

and supervisors alike claim to have discovered "incredible" amounts of talent on the line. "We've overlooked this resource in the past," admits high-reliability business unit manager Al Woodhull.

What especially makes Fairchild employees enthusiastic is being asked to solve problems and having their answers listened to by managers. Problems have run the gamut from setting up procedures for handling emergencies to correcting wafer fabrication runs, and solutions began developing within three weeks of startup, to the surprise of supervisors. Furthermore, the scope of the QCs quickly broadened to encompass interactions between departments, particularly in relation to new projects whose problems are now foreseen and dealt with before they become serious.

Would-be participants are volunteering for new circles faster than the company can set them up, forcing it to draw names from a hat to pick new members. Fairchild says it is delighted with its QCs. One of its production workers, a 19-year veteran, agrees: "Without these meetings, we wouldn't get such quick action on problems. We're not afraid to speak up now."

Wider circles. Honeywell Inc. is probably the U.S. electronics firm with the longest track record in QCs, although others not entirely in electronics have been there first. It has had circles since 1974 and by now has taken them beyond manufacturing into areas as remote from the factory as marketing communications. The Minneapolis computer and information systems company, in fact, sees the technique as generally applicable to more than just quality. "It has tremendous potential for training," says James Widfeldt, corporate QC coordinator. These meetings, on company time, are the fastest way of bridging the information gap between hourly workers, supervisors, engineers, and managers, he says. From the first meeting, "people began to vibrate and their eyes light up."

Honeywell has been careful not to attempt to pin down the specific effects of QCs on costs, productivity, or personnel turnover, in order to preserve spontaneity of the programs

Quality Circles: a common-sense approach?

For all the mystique with which U. S. industry now enshrouds them, Quality Circles are simple organizations rooted in down-to-earth practices that successful firms often employ informally. While QCs differ somewhat from company to company, each is a group of about 5 to 13 employees doing similar work who meet regularly with their supervisor to investigate quality problems and try to solve them. A key aspect is their voluntary nature.

The idea originated in Japan after World War II, when the Union of Japanese Scientists and Engineers formed a QC research group in 1948. In 1962 this group put QCs on a formal basis, and now its QC headquarters serves to spur and coordinate these activities. A noteworthy feature in Japan is the circles' "bottom-up" nature, essentially a means through which workers can contribute their skills and loyalty to their companies. Observers comment on their spontaneity, a feature lacking in the U. S. movement.

Since 1974, when Lockheed Missiles & Space Co. pioneered the idea, QCs have also caught on in the U. S. Besides growing out of a firm's own efforts, they have been spurred by a consulting company, Quality Control Circles Inc., founded by Wayne S. Rieker, who was instrumental in setting up the Lockheed program. To date, his company in Saratoga, Calif., has set up more than 90 QC programs and the pace is quickening.

Not only do the QCs rapidly repay the cost of setting them up, but they also improve morale, communications, and attitudes in ways that promote longer-term benefits, reports Rieker. "There should not be too much emphasis on tomorrow's dollar savings or short-term results," he says. "If the emphasis is instead that we're out to create a change in the style we manage, the movement will sustain itself and grow."



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Circle 97 on reader service card

Inside the news

at the division level. But observably better employee relations leave their positive contribution in no doubt. The few results that are quantified are spectacular, says Honeywell. In two large plants, machine utilization rose from 50% to 85% and 90%. In another, productivity increased from 70% to 98%.

While semiconductor firms are claiming immediate results—possibly because of their faster-moving nature—other companies are moving at a more measured pace. RCA Corp.'s Picture Tube division, for example, gives its QC groups as much as six months to get up to speed before each makes a formal presentation of suggestions to managers. "We're not viewing Quality Circles as another zero-defects program," notes Jeffrey C. Trullinger, manager of organizational training and development for the Lancaster, Pa., division.

Instead, "we're looking at them as a management philosophy and a way of life, and for that reason we're moving slowly." Still, RCA has 17 circles and claims efficiency and cost improvements in the 1½ years since starting. Problems addressed concern tube salvage and how best to evacuate air from tubes to create a vacuum.

At its Scranton plant, RCA uses a module approach to train workers, spending about an hour a week on each skill module. There are 9 or 10 of the modules, teaching the workers about such matters as bar charts, histograms, and other problem-solving techniques. Supervisors, who are trained first, take part in six or seven training sessions before they and the hourly personnel are ready to begin tackling problems.

"The QC members make the final decision on what problems to look at,

although management sometimes makes suggestions," says Trullinger. "Then, three to six months after they have started, the group will make a formal presentation before the operations and manufacturing managers." Thus far, there have been three or four presentations.

Trullinger says, "The primary objective is to involve the hourly worker in a decision-making process and in turn to improve the quality of the products they turn out. The key feature is that it's voluntary."

There have been some observable efficiency and cost improvements, though Trullinger is reluctant to discuss them in detail. He does say that many of the 1,400 hourly workers in Scranton wish to participate in the circles and that there is a waiting list

tough and highly competitive consumer market.

The new Japanese management moved fast and within six months a program for improvement was underway, recalls Richard A. Kraft, who is president of the operation and also ran it under Motorola. The first phase sought to revamp production with automated equipment and a new TV chassis design that facilitated automatic insertion. This improved productivity and significantly reduced the labor content of color receivers, he says. The change took three years, with a jump in automatic insertion of components from about 15% under Motorola to 65% to 75%.

While improvements that substitute capital investment for labor costs are closely identified with U.S. management, observers note that many publicized Japanese techniques in fact grew from close study of American practices, the difference today stemming from their further perfection and more rigorous application by Japanese managers.

Look at people. After getting better equipment into place, Matsushita turned to the people



Making it better. At RCA's tube plant in Scranton, Pa., from the left, John Mackie, Lloyd Rosengrant, Tom Rafalko, and circle leader Paul Graham at a meeting.

to start up new ones. However, RCA will probably limit the number in Scranton because there is only one supervisor at the plant now to implement suggestions.

Other techniques. For the present, most U.S. receptiveness to Japanese management techniques focuses on Quality Circles, but other examples can already be found. By any standard, a turnaround has taken place at Matsushita Electric Industrial Co.'s television manufacturing facility at Franklin Park, Ill. Once the Consumer Products division of Motorola Inc., it was sold to the Japanese firm in May 1974 because of its mounting losses and Motorola's unwillingness to make the new investment needed for it to compete in a

factor. Curiously enough, in the several new programs it has been emphasizing over the past two years, Quality Circles have not played a central role, because "they need a substantial amount of training to be fully effective," says Kraft. Instead, Matsushita has "quality emphasis months" each spring and fall, and "a model line concept." In the first, workers are saturated with exhortations for better quality through publications, contests, signs, and other devices. The model line is one chosen to set and achieve goals that other lines can try to match. This promotes healthy competition between workers and foremen, it is claimed by managers there.

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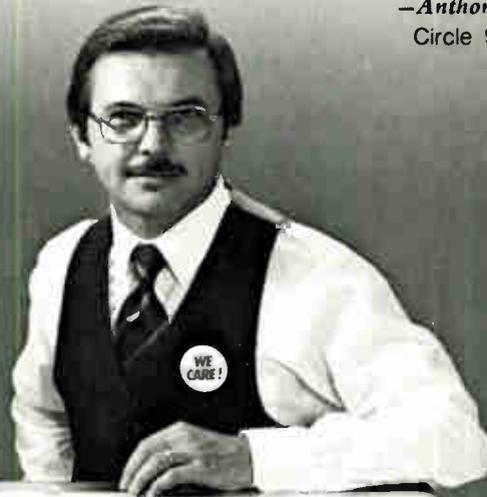
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has attained a more productive plant, which Kraft says "absolutely" may be attributed to Japanese techniques. The in-line reject rate, or the cumulative number of rejects from start of production to finish, has dropped to 4% to 6% of all receivers, compared with a 120% to 140% rate (1.2 to 1.4 rejected for each accepted) for Motorola. Further, one receiver in pre-Matsushita days took up to 135% more labor per unit. Not only are Quasar television sets selling well, but new microwave ovens and projection TV also now roll off the lines.

Along with most executives associated with a Japanese enterprise, Kraft does not play down the difficulty of transferring Oriental methods based on harmony to a society where individual values prevail. Without "time, dedication, and interest by management," the techniques will not work. Generally, he figures it takes two to three years' training before U.S. workers have the skills to be effective in this type

of team-player system.

As the Quality Circle trend widens, it also raises deeper questions about its causes and implications. For one thing, if its benefits are now so obvious, how could U.S. companies have ignored them for years, during which their competitive positions were eroded by poor quality and productivity and, in the consumer sector especially, by high prices? Most top U.S. executives put the blame on workers and supervisors, rather than take some of it on themselves.

Texas Instruments Inc., which has the most experience of any U.S. firm in manufacturing inside Japan, thinks it has identified what is wrong. The fault lies with inefficient middle management, says Ralph Doshier, manager of TI's worldwide training and education. Such inefficiency does not exist in TI's Japanese operations and did not exist 20 years ago in the U.S., he says. Whatever its origin, and Doshier thinks it can be traced to social upheavals in the 1960s causing breakdowns in responsibility and discipline, its effects set serious limits to U.S. efficiency. TI

is attacking it with a widespread program that includes Quality Circle-like units. But in the opinion of TI, top management in the semiconductor industry measures up to Japanese counterparts. "They're just as competitive, innovative, and hard-working," says Doshier.

Japanese opinion. Such is not the view, however, of one of the "wise men" of Japanese electronics, Akio Morita, chairman of Sony Corp. "The problem in the United States is management," he charged recently in an interview with a visiting U.S. financial editor.

U.S. managers do not understand the source of the strength of Japanese firms, which starts with the policy of lifetime employment on which loyalty and performance can be built. Lack of this weakens American firms, he says, noting that Sony's experience with U.S. workers has shown them to be the equal of Japanese when they are dealt with fairly. Sony kept its U.S. workers on the job even during a recession, and its plants in San Diego and Dothan, Ala., are producing on equal terms with those in Japan. "The fault is not with the worker, the fault is with the management," maintains the Japanese executive

No panacea. A key admonition raised about transfer of Japanese organizational techniques centers on this point. To a person, managers most experienced in the Japanese way of doing things keep bringing it up. Their caution: do not depend on Quality Circles or any other method successful with Japanese operations to solve deep-seated productivity troubles without fundamental changes to support them.

What must be built, they say, is a mutual trust and loyalty between workers and the company without which any QC-like techniques cannot take firm root. This view is summed up by Eric Lidow, chairman of International Rectifier Corp. of Los Angeles, which started the first semiconductor manufacturing plant in Japan during the late 1950s. "The advantages will not transfer without more paternalism within our companies and less of the Harvard Business School approach. The accent must be on people, as in Japan, and not on numbers," he says. □

Managing the Japanese way

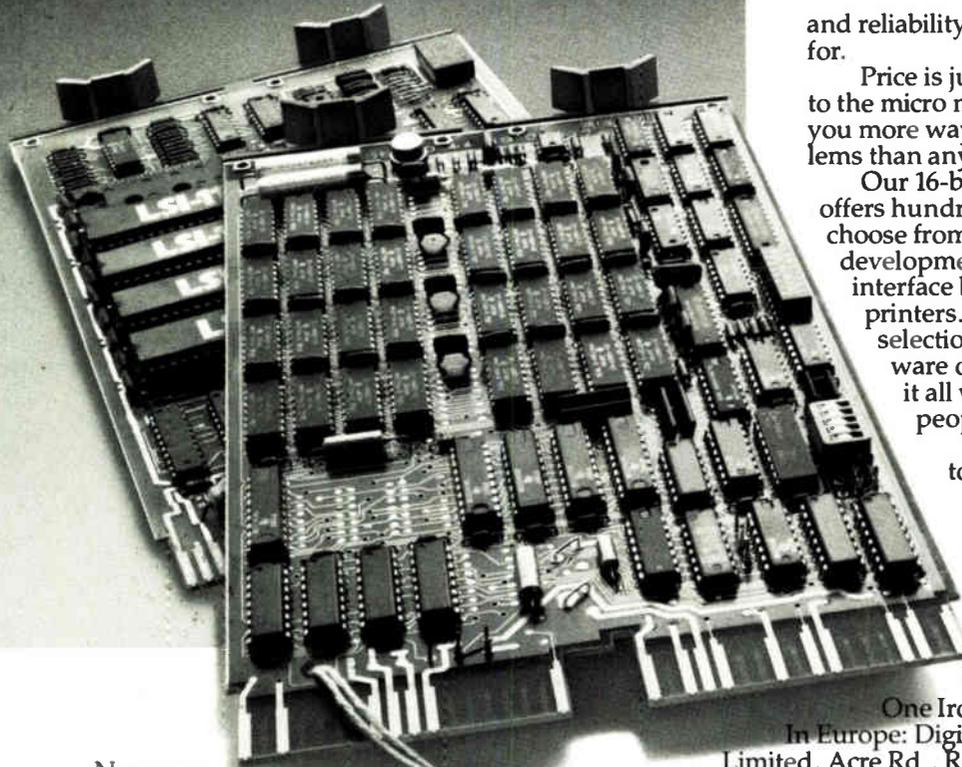
Kyocera International Inc. has taken Japanese management ways further than any other firm operating in the U.S. One reason for its success with them, says personnel manager George E. Woodworth, is the slow step-by-step approach the firm has taken since it moved to San Diego, Calif., in the early 1970s. Another is that 48% of its workers are Asian-American, primarily wives of servicemen. (San Diego itself is the favorite U.S. expansion site for Japanese firms and the area is working to attract more.)

The techniques used at Kyocera are based on those that succeed in Japan, and all are directed toward building unity and harmony, says Woodworth. They include:

- Daily meetings between outgoing and incoming shifts, to keep a flow of information constant.
- Daily stand-up meetings in each department, with a different topic and speaker each day.
- Company jackets worn by everybody, up to and including executives, and group exercises.
- Honor employee status won by six months of perfect employment by hourly workers. The prize is exemption from punching the time clock and immunity from firing.
- Special raises given by supervisors on their own authority.
- A cultural exchange program with Japan for children of employees who have won exempt status.
- No layoffs.

Furthermore, Kyocera uses a meeting system, called a "compa," that is like a Quality Circle in its group dynamics, but focuses on other problems. It helps iron out any personality or attitudinal conflicts and is held outside work hours. Other hallmarks of this type of operation are a lack of a formal chain of command and more meetings of all kinds than for any U.S. company. Also, executives work long hours, averaging a 55-hour week.

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Military moves to integrate ATE

Study by three services and industry recommends policy, programs to limit proliferation of test systems and speed readiness

by Ray Connolly, Washington bureau manager

The people who make automatic test equipment for the military as well as their customers now have a script to put together a sharper act. It tells them how to establish a joint logistics policy that will hold down ATE proliferation and costs, create and enforce standards, and train and retain personnel better. Yet both groups acknowledge that much still needs to be done before they get the show on the road.

After three years of preparation

by more than 500 industry and military ATE specialists, the newly published report—the "Industry/Joint Services Automatic Test Project"—is getting strong support from such top-level military leaders as Gen. Alton D. Slay, chief of the Air Force Systems Command. Slay's praise for the program at the Institute of Electrical and Electronics Engineers' Autotestcon in Washington last month represented the first public support "by four stars," notes Paul

J. Giordano. A member of the project steering committee and president of consultants Giordano Associates Inc. in Midland Park, N. J., he calls the program "the most important event in ATE history."

The support is equally encouraging to members of the 86 companies that participated in the effort under the leadership of Sperry Corp.'s Frank McGinnis, product assurance director at the Sperry division. It is also encouraging people like Air

Force Capt. Ralph H. Freeman of the Aeronautical Systems division, who notes "there are over 400 major automatic test systems deployed by different users" in the Air Force alone whose "technology spans the history of ATE."

Freeman cites the "logistical nightmare" of some 50 C-141A transport payloads that would be required today to move seven F-15 fighter intermediate avionics shops, their support equipment, and portable buildings to Europe from the U. S. Even the older F-4 Phantom, he notes, "has over 4,000 pieces of support equipment. Some of this, particularly the ATE,

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SOURCE: DEPARTMENT OF DEFENSE, "INDUSTRY/JOINT SERVICES AUTOMATIC TEST PROJECT"

Complexity. System complexity is the most commonly identified problem in ATE, according to 14 of the 16 task groups in the industry-military study. However, management-oriented problems outnumbered technical ones.

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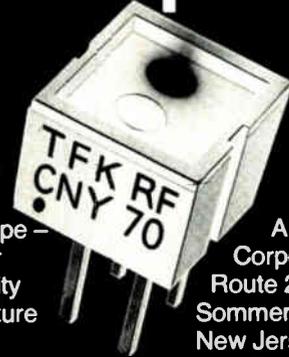
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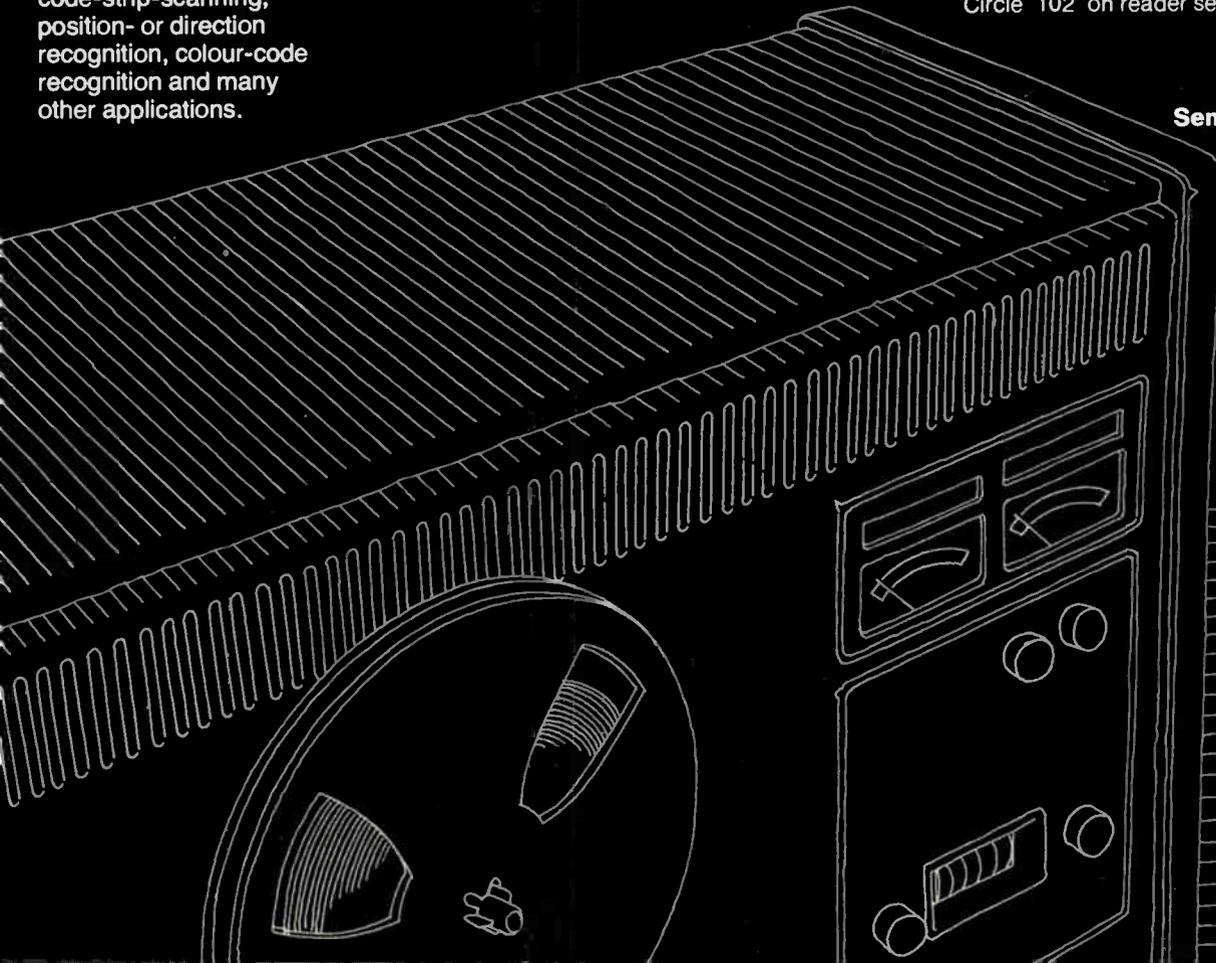
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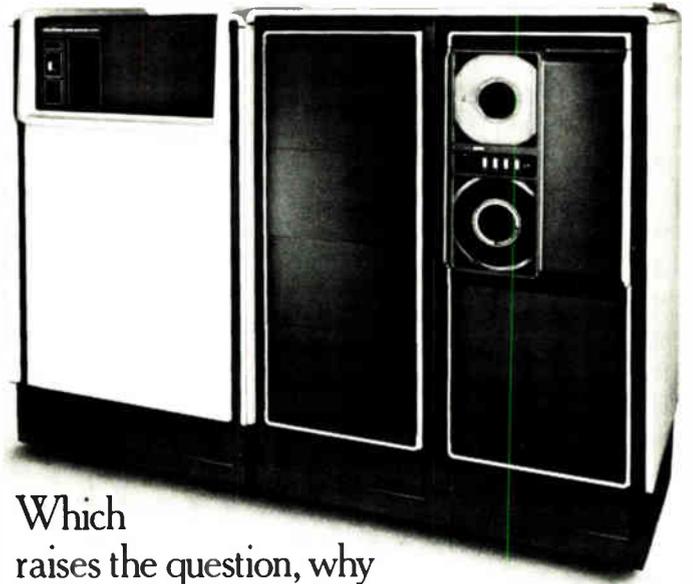
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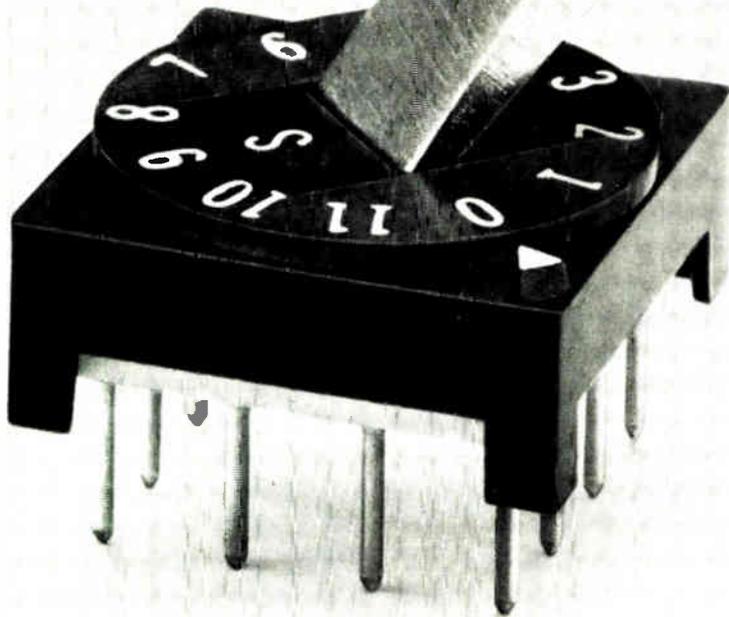
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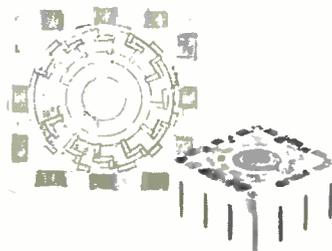
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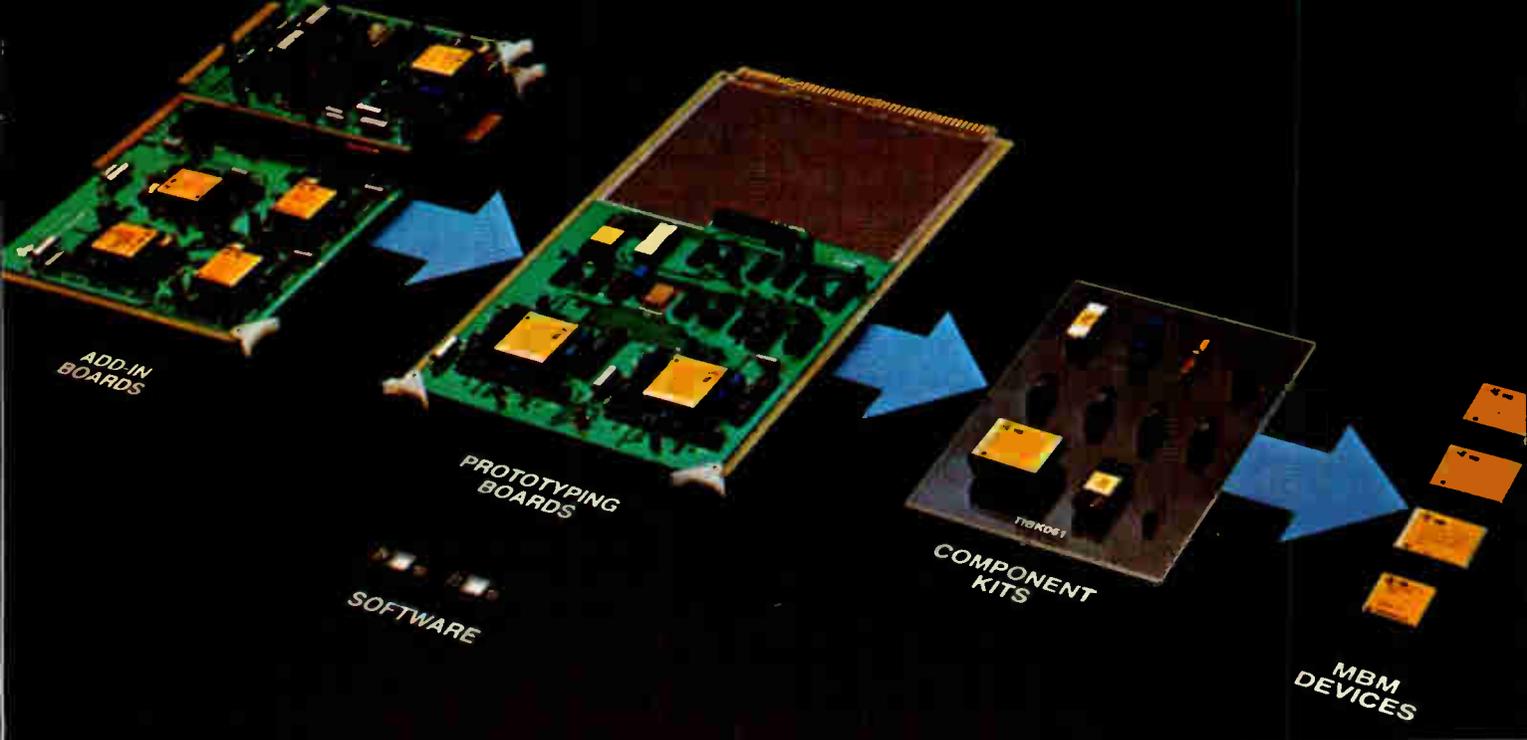
hour, the cost of spare equipment could drop by 20%, and fuel consumption could be reduced by 10%.

In the area of technology, the Defense Department is urged to set aside 10% of the joint services' automatic-test R&D funds for unconventional, or blue sky, approaches. Such funds could be used to identify the techniques and facilities needed to support emerging technologies, study distributed systems, and advance technology for automated calibration systems, as well as investigate advanced software for ATE. Moreover, the project also proposes developing a methodology for trade-off studies between internal BIT and external ATE, as well as studies of universal interface pin arrays and the establishment of a methodology for the self-checking of microprocessor-based BIT systems.

Establishment of common industry-military data banks and standard models for determining life-cycle costs, logistics support analysis, and technology assessment would permit ATE developers and users not only to learn from experience themselves, but also to give program managers and contractors a better picture of a weapon's total cost—including ATE and other logistics support.

This view is supported in the comments of the Air Force's Freeman, who notes "there still exists no comprehensive data bank of USAF ATE capabilities. Current systems record the ATE name, quantity, and current usage but not its ability to handle other test requirements. ATE is purchased on a program-by-program basis rather than under a planned corporate approach." As a result, Freeman says, "the impacts of various approaches and trades between alternative test philosophies are often 'guesstimated' on the basis of individual experiences rather than on standard procedures."

Of the five industry trade associations representing aerospace, electronics, and shipbuilding that participated in the project, the National Security Industrial Association in Washington has been named liaison to the military as it moves to implement the program. □



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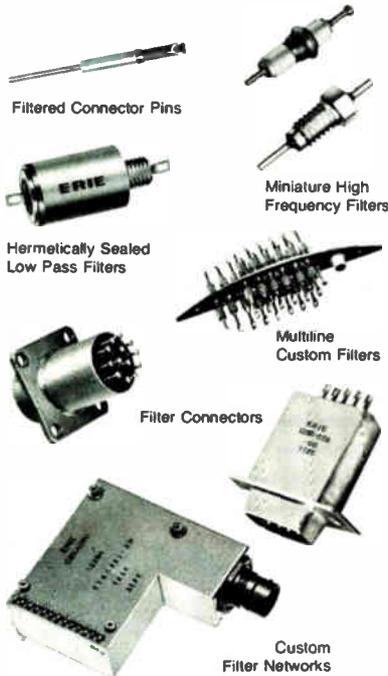
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Probing the news

[*Electronics*, Nov. 6, p. 74].

Before the advent of today's very high-density memories, technological and circuit design innovations held the number of bits per wafer start on its upward yearly slope (see graph). But these alternative approaches are hitting the stops, despite a demand for bits that "interestingly, we do not see subsiding," says MacKenzie. He cautions that to make up the difference with lithography is "risky and expensive" because the right equipment may be unavailable or too slow for volume production. As for circuit design innovations, not many new twists can be put on the dynamic RAM cell in particular, since it has "already been reduced to a single transistor and capacitor," adds MacKenzie.

Yet another way to push more bits out the door is simply to parallel-process chips with more production equipment—these days perhaps the least attractive solution. To keep bit volumes up without redundancy, "basically, you have to add fabrication capacity as you never did before," asserts MacKenzie. In fact, "by 1984 or '85, this may mean a difference of up to 10 fab lines, each costing \$50 million."

Amortizing this \$500 million outlay over the next two to three years—assuming each fabrication facility has a capacity of 10,000 wafer starts—could mean a per-bit price hike of 1 to 2 millicents, or from 65 cents to \$1.30 extra for each 64-K RAM component. But that is almost half the price of some 16-K RAMs now being sold on today's soft spot market.

Hanging on. "Redundancy," on the other hand, "gets you back on the curve for at least a few more years," claims MacKenzie. Spare circuits also allow bigger chips with relaxed tolerances, helping to reduce the number of levels demanding advanced lithography machines like those that step and repeat patterns directly onto wafers. Conservative layout also curtails noise and alpha radiation better; but just in case, Intel will stick a piece of polyimide tape atop its memories [*Electronics*, Nov. 20, p. 33]. □

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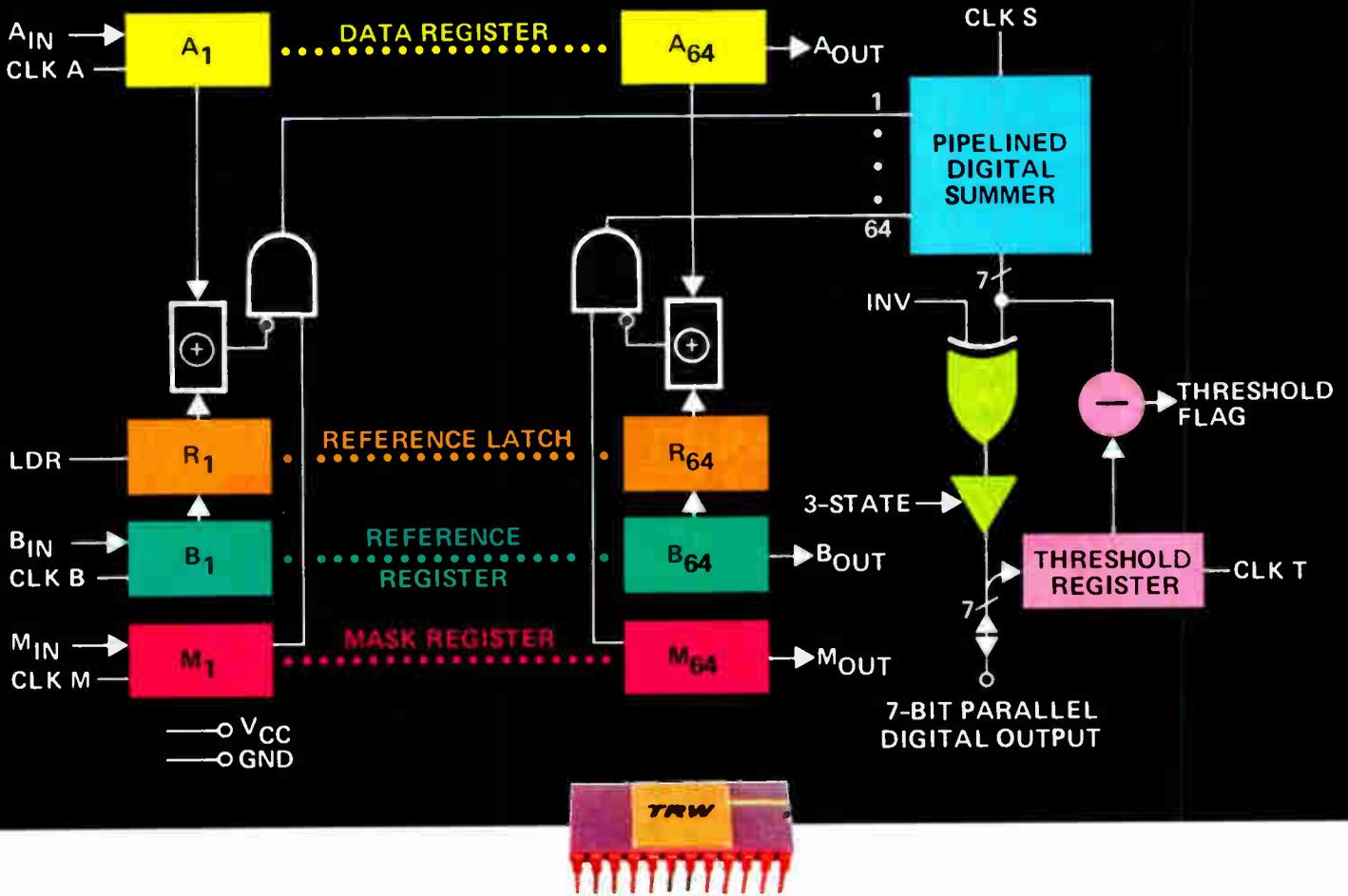
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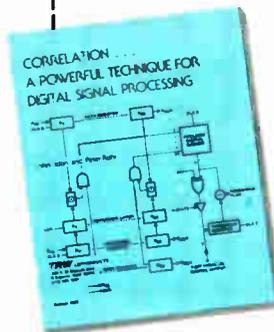
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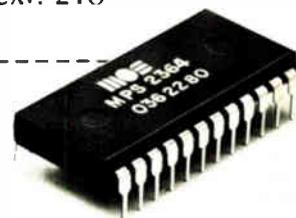
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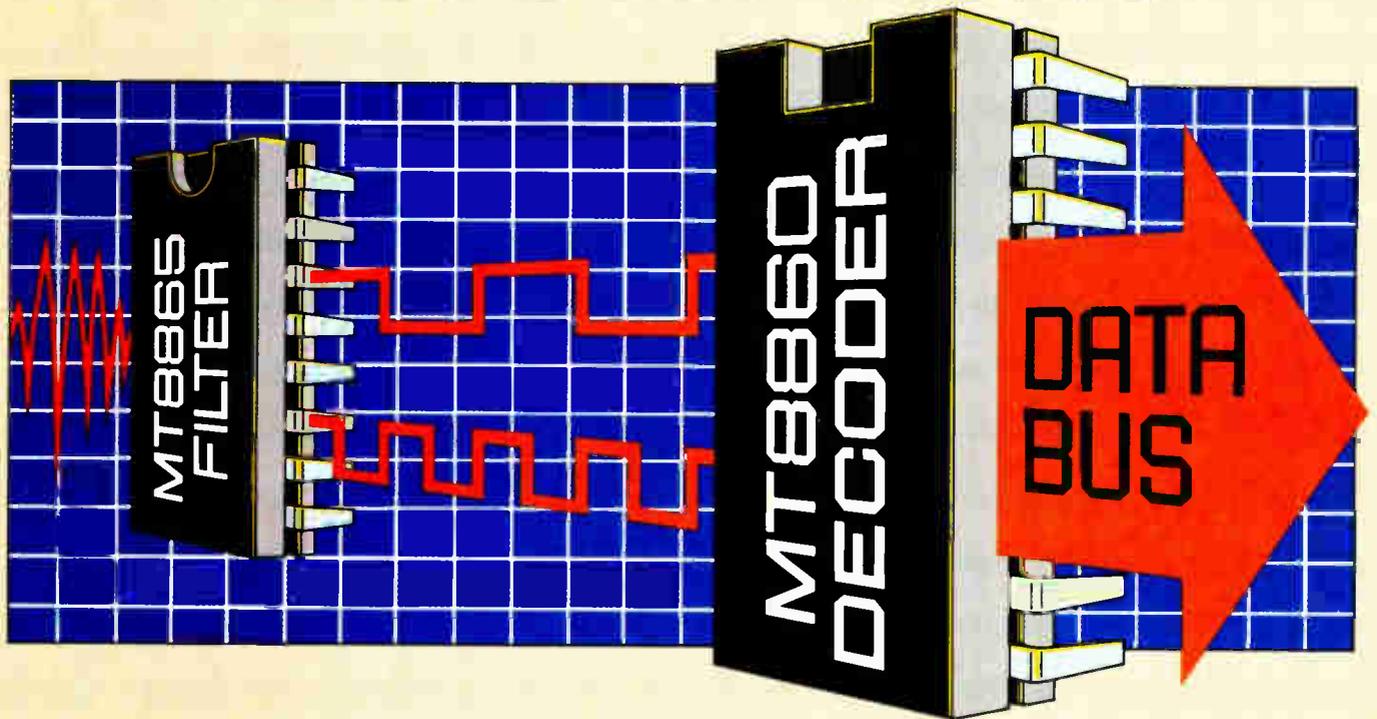
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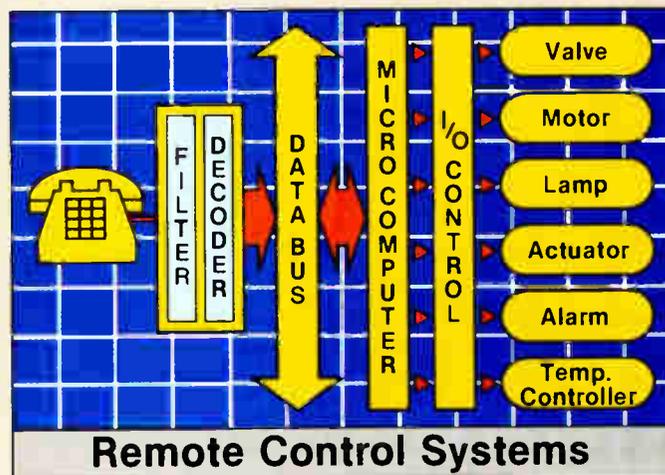
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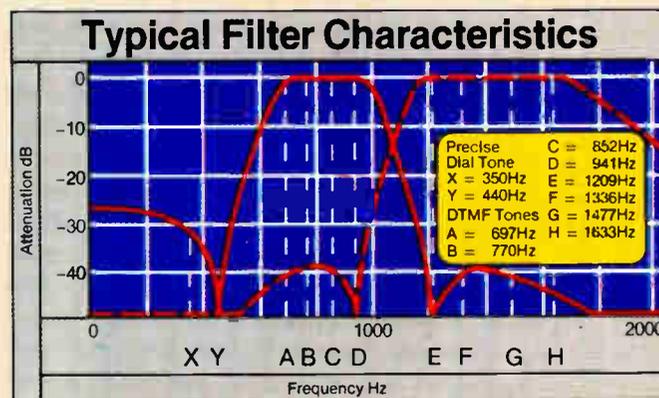
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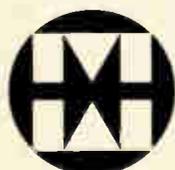
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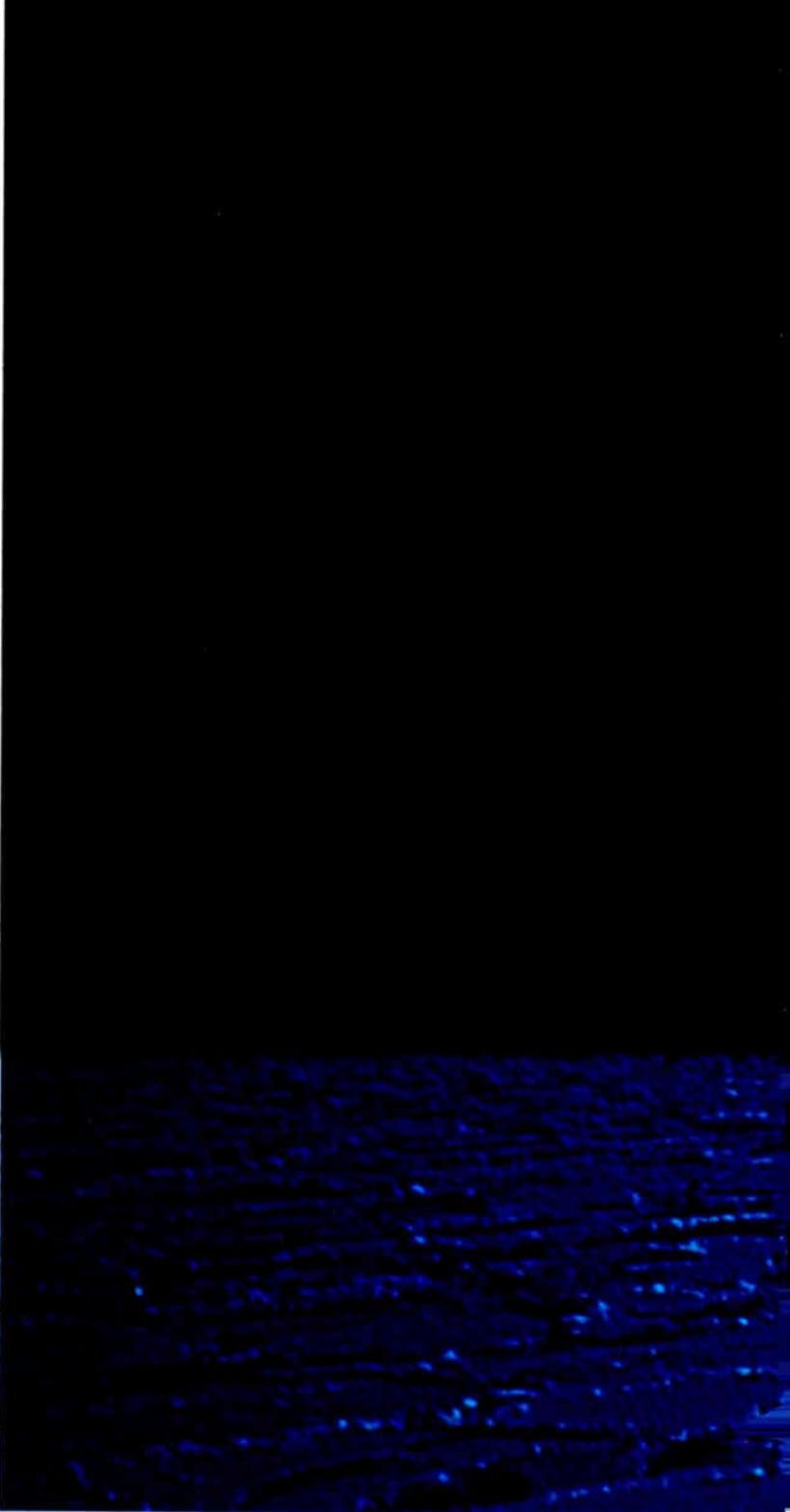
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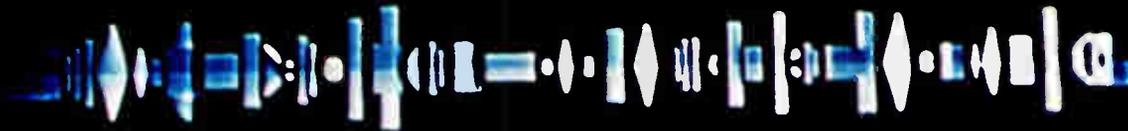
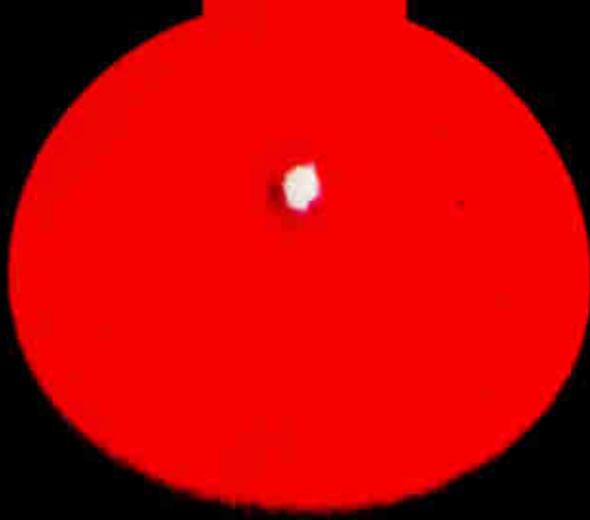
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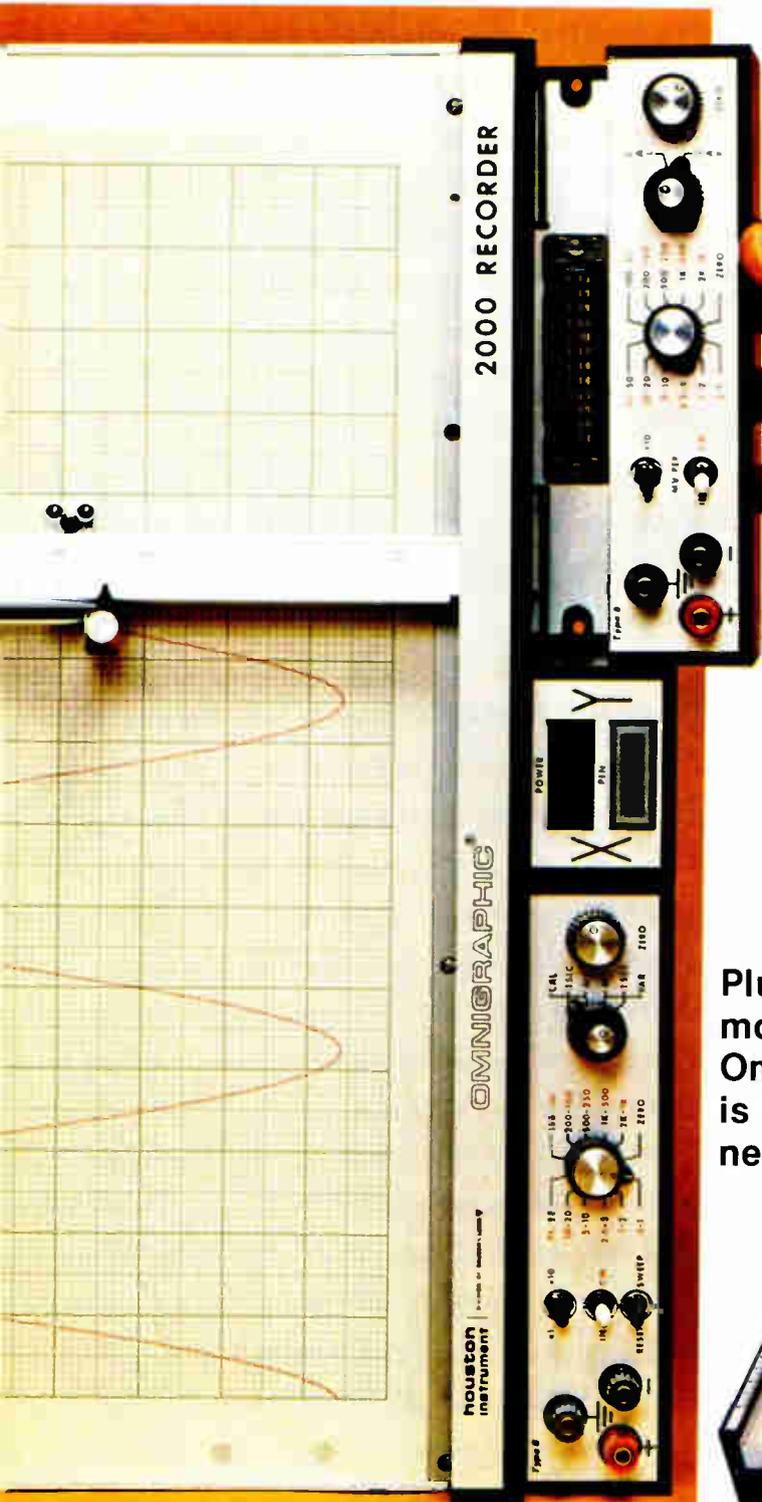


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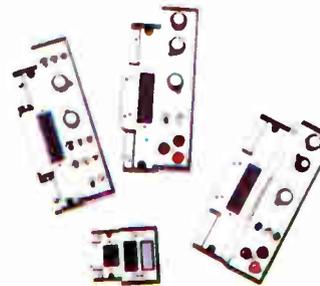
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Concern for the economy tempers industry leaders' overall optimism for 1981

Government's attitude toward business, deepening shortage of professionals, and sharp competition for world markets also loom as obstacles

JOHN W. ZEVENBERGEN

*president,
John Fluke Manufacturing Co.*

The economy, the shortage of engineers, Government action—these top the list of concerns for a majority of electronics executives looking ahead to 1981, and Zevenbergen is no exception. "I don't see the U. S. economy straightening out until April," he says. "And the European economy is still headed downward, which will slow the instrumentation industry's recovery." But Zevenbergen does anticipate a boom after the first quarter.

That recovery, on the other hand, will only exacerbate the shortage of engineers. "We are seeing a little relief due to the recession and the tight business situation," he explains. "But when the economy turns around, the shortage of professionals will only become worse."

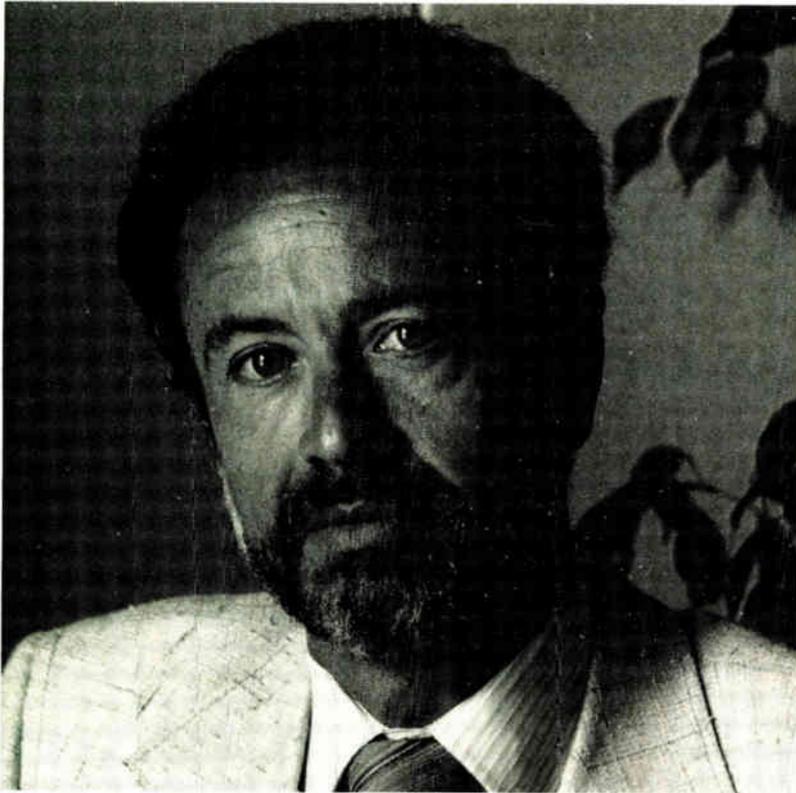
Contributing to it, says Zevenbergen, is the inability of American universities to graduate enough technicians and engineers. "The Government should step in and provide money for more facilities. The most important job, however, is to convince state legislatures of the problem, since they are the main support for the schools."

Zevenbergen also would like some changes in trade and Government-business relationships. "Political trade embargoes such as the one on South Africa are stupid—we shouldn't mess with the internal affairs of a country that is not against us. And in the U. S., we should end the adversary relationship between Government and business. In Japan, they work together; here, business is constantly under the scrutiny of the Federal government. And there should be a tax break for products that are exported. Other countries allow their manufacturers this kind of break, but in the U. S. we pay the same tax no matter where the product goes."

Zevenbergen says his company is also feeling the effect of the energy crisis in that "the cost of travel is going through the roof." Fluke is finding that it must rely more on people in the field for user feedback and technical input because it cannot afford to send as many staff from the factory to user sites as it once did. This hurts particularly with trips to Europe, where Fluke does 25% of its business.



Executive Outlook



ANDREW S. GROVE
president, Intel Corp.

Grove, too, thinks most about the economy and wonders "whether it will return to a normal healthy growth, or continue to fluctuate or be listless." In his opinion, many decisions are now influenced by "the uncertainty hanging over everybody" and "the vagueness associated with the fact that the vigor of the last few years isn't there."

Grove expects the recession to continue into 1981. "It's certainly not a one-quarter phenomenon." Although he is not eager to see "too many quarters of a downturn," Grove believes the current soft period has its benefits. "Having a breather after several years of strong growth can be beneficial for companies in our industry. When you're growing as fast as we have, a lot of inefficiencies can come about. And if you don't clean them up, they can become part of the normal way of doing business." The Intel official expects a gradual upturn in the industry and an eventual boom.

His views on capital formation are less gloomy than those of some fel-

low executives. Pointing to recent stock offerings by Intel and other semiconductor makers that quickly sold out, Grove notes, "Capital formation is not all that hard. We probably have seen the worst of it, largely because the change in the long-term capital-gains tax has made a shift in the thinking of the investment community."

As for the shortage of engineers, it is not going to have an impact on business in 1981, according to Grove. "It's more of a long-term problem." In fact, "the shortage of engineers and technically educated professionals, including that in the software community, is a catastrophic problem." The industry has been unable to penetrate the school system and interest students in electronics, Grove says. "Even if we were successful in interesting them, the university machinery isn't equipped to handle them. The appropriate physical facilities aren't being built, because the technical institutions aren't getting their share of the money."



GEORGE M. BERMAN
*chairman and president,
Unitrode Corp.*

In Berman's view, a principal side effect of the recession might be neglect of research and development or delayed spending to build up and automate manufacturing and marketing operations in 1981. "This is no time to let up," he asserts. "The current economic climate may hold steady for another three to six months, and we may need nine months more to return to normal. But in another year or two, I think we'll see demand running high again, deliveries stretching out, and prices firming." Companies must act now if they are to be ready, Berman says.

Another worry—an incentive for U. S. firms to strengthen their capacity—is the prospect of stiff foreign competition. "The Europeans and Japanese are tough rivals, and that's good. We don't need protection from them. We need wider markets." The problem of lagging U. S. innovation and productivity, he maintains, would find quick and natural resolution in a free-trade environment. Domestic firms and the Government need to push hard for a lowering of trade restrictions worldwide.

Government can help in other ways, too, and Berman is optimistic that help is on the way. Tax breaks and more favorable asset-depreciation schedules designed to free corporate cash for investments should fare well in Congress next year, he believes. With many industries, including the semiconductor sector, becoming more capital-intensive all the time, such incentives are essential for the kind of progress that pays big dividends.



PASQUALE PISTORIO

*managing director,
SGS Componenti Elettronici SpA*

Looking on the semiconductor business as a global one, Pistorio sees two major uncertain factors in the 1981 scenario. The first is "a hell of a lot of capacity that will come on stream" and exceed demand; the second is "the appearance of other players in the game"—specifically, the Japanese.

Pistorio, who was both a vice president and general manager of the International division at Motorola Semiconductor Products before joining SGS-ATES, traces the potential capacity problem to the recession of 1974-75 and the reluctance of most semiconductor makers to add capacity after they were stuck with excess inventory in that dip. The result was a realization in 1978 that demand was outstripping capacity and a subsequently huge worldwide investment in new plants and lines through 1979. Even the slowdown at the end of 1980 has not deterred heavy investment.

Turning to worries caused by the growing Japanese influence, Pistorio sees them as astute entrepreneurs and marketing people. "Next year they will sell less if everybody sells less, but their penetration will not diminish. They will gain in areas of high-volume, repetitive products, rather than where a variety of design is essential. They will not grow in specialty applications—they will grow in large commodities and broad-range applications."

There is some optimism in Pistorio's outlook, however. He feels the overcapacity squeeze will be only a temporary aberration. "Semiconductor growth is so strong and people so cautious that demand and supply will be rebalanced by 1982." And there will be a major difference between 1981 and 1975, in Pistorio's view: "In 1975 demand stopped; in 1981 it will be a question of the huge supply of semiconductors outstripping demand."



JACQUES BOUYER

*managing director,
RTC-La Radiotechnique Compélec*

There are plenty of uncertainties for French electronics executives to worry about in the coming year. Consumer and automotive markets are soft, the country will undergo the shock of a presidential election in April, and production costs continue to rise. But Bouyer insists on stressing "the intrinsic value of the electronics market." Thanks to the basic underlying need for electronics in more and more areas, Bouyer predicts a good year in 1981.

Still, he is not without cares. The principal worries from the perspective of the Paris-based subsidiary of the Netherlands Philips group involve uncertainties on the international scene: the Iran-Iraq war and the state of the U. S. economy.

While Bouyer expects Europe to avoid a real recession regardless of what happens in the U. S., he notes that European electronic component and equipment makers suffer a strong indirect impact when the U. S. economy is sour. "Europe is used as an overflow market for American companies when the U. S. markets are slack," he explains.

While the 1978 national elections in France seriously hampered economic activity, Bouyer is not worried that there will be a rerun this time around. "The key difference is that the odds in '78 were very uncertain. If the Left had won, there would have been a real change in economic policy." But this time, says Bouyer, "there is not much of a risk. Very few people doubt that President Giscard d'Estaing will make it."

Executive Outlook



WILLIAM D. WALKER
*executive vice president and
chief operating officer, Tektronix Inc.*

"Our No. 1 concern is the current recession and the slope of its recovery," notes Walker, "and our No. 2 concern is whether the Government will do the kinds of things that will allow more investment in buildings, equipment, and R&D."

Walker thinks the Government can make changes in three areas that will help business. "It can allow us faster depreciation schedules, give investment credits, or reduce the basic taxation level. It can also limit inflation, since our funding of expansion must include both real growth and inflation. With a real growth of about 15% and inflation of 10%, that amounts to a 25% investment.

"The Government has never fully comprehended the importance of market share. The Japanese do. The Europeans do. But we, as a country, have given away market shares, one by one, to the Japanese." Concerning competition from abroad, "I don't look for a lot of changes in 1981. The Japanese, however, will continue to apply pressure."

On the recession, Walker claims, "I am not a proponent of the double-dip recession point of view. I see that the general recession may have a long bottom, and some may find a W-shaped curve in that. I just expect a longer bottom and a slower recovery. I see an upslope already."

Another of his concerns is the shortage of engineers. "It gets deeper through the decade. I think we will see the U. S. go abroad for some recruiting. It will also do more offshore engineering as a recruiting tool."



FEDERICO FAGGIN
president, Zilog Inc.

"Clearly, the recession has to be a big worry in 1981," agrees Faggin, who since outlining these views has moved to Zilog's parent, Exxon Enterprises, as a vice president. He is not only concerned about its depth and length, but also about the pattern of recovery.

Most recently, Faggin notes, there has been an increase in electronics business as it relates to orders with short-term release schedules, or quick shipments. "That indicates a lot of users are hand-to-mouth with respect to their inventories," as they are only buying what is needed. Faggin sees this as a positive sign, "because when the economy shows signs of improvement, they'll be back with larger, long-term orders."

Unquestionably, competition from abroad will increase, says Faggin, with Japan taking the lion's share of the increase. Though the computer industry is the ultimate target, penetration of that market will not be as fast as in the semiconductor industry, he predicts. Looking eastward, he says, "In the near term, I don't see European manufacturers taking a larger share of the market."

Of greater concern, however, is whether there will be a reversal of the trend toward more Government regulation and less incentive for industry. "I would like to see more incentives going to high-technology industries along with a recognition of their contribution to the economy and industry as a whole. There seem to be some encouraging signs, but we still have a long way to go."



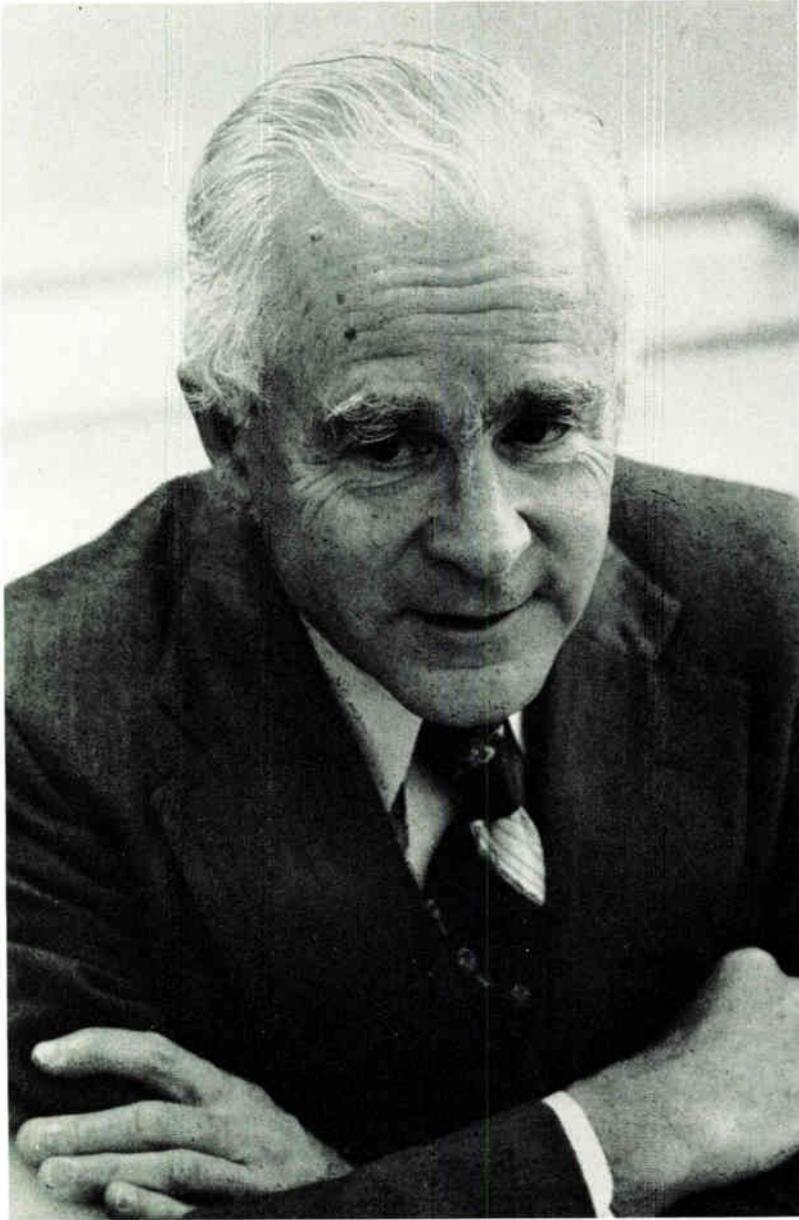
EDGAR A. SACK
*senior vice president,
General Instrument Corp.*

For the large-scale integrated circuit manufacturer, says Sack, troubles come in threes.

First is the infiltration of Japanese semiconductor products into the U. S. and what that means for American manufacturers. He sees the Japanese penetration of the random-access memory area continuing throughout 1981. The solution to this problem: "Seek out market niches that are more accessible to us than to the Japanese."

His second concern is the change in ownership of American semiconductor makers: where the trend used to be to independent suppliers, now it is to captive vendors. He lists Mostek and Intersil as examples of former independents that are now captive. "That captivity of capacity will inevitably change the marketplace. It may very well make the ups and downs in supply and demand cycles much more severe for merchant suppliers," he observes. "This kind of change in ownership increases the tendency for overcapacity. Capital investment to a large systems house is often peanuts, and therefore the tendency to overcapacity is there." Sack believes this trend will keep the competition for good equipment and skilled workers a hot issue into the next year.

His third worry is meeting Federal requirements on environmental and health issues. "It's going to distract management's attention, because they can't put compliance off. Nevertheless, you've got to work for strict compliance."



WILLIAM R. THURSTON

president, GenRad Inc.

"My chief concern is uncertain demand. Electronics traditionally lags behind other sectors of the economy in a slowdown, and we appear to be seeing our slowdown now. I look for six to nine months of softness, but that's a very loose projection—it could be longer or shorter." Since the end of such a slowdown cannot be predicted accurately, Thurston notes that electronics managers will have to be alert and poised to capture the opportunities coming with the expected upturn.

Thurston is as worried about management reactions to a slowdown as he is about the slowdown itself—especially given the United States' world market position. "The best counter to competition, inflation, and recession is a strong commitment to research and new-product development; I fear that some managers will sacrifice new-product development for good-looking quarterly statements. If they do, their companies will come out of this slowdown weaker than they were going in, and that

could make us less competitive in world markets."

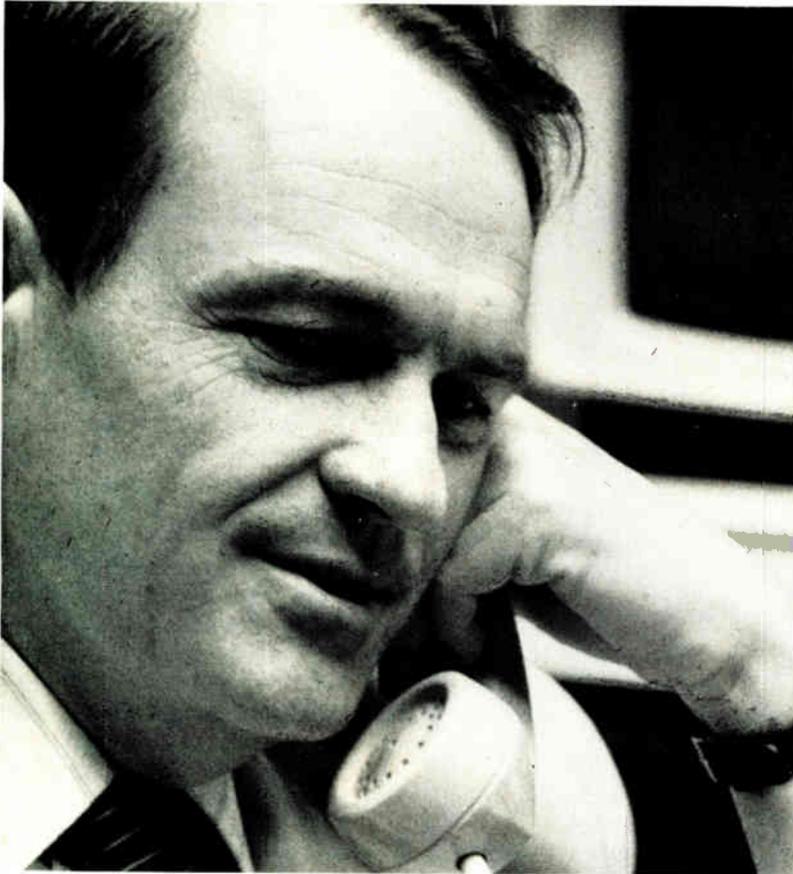
Another unsettling factor Thurston cites is the relative scarcity of computer science personnel, electrical engineers, and programmers. He calls this a "chronic problem and an acute concern," pointing to the large number of EEs graduating each year in Japan compared with the U. S. Not only are the Japanese graduating about 50% more yearly, but the number is even more impressive when viewed as a proportion of population; also, "Japanese engineers are highly motivated, productive, and capable of high-quality work—as good as ours."

If forced to choose, he would spend his time boosting the quality of U. S. engineering rather than productivity. "Productivity is almost impossible to measure," he says. "What counts for a company is market share, what counts for a country is world market share, and I think it is quality that sells. I think I could be convinced to sacrifice half my engineers' productivity to gain a twofold improvement in quality."

As for the shortage of personnel, he feels that it is being addressed, though not too visibly. "Graduating classes are growing larger," he says, "and there is increasing interaction between industry and the campus. More academics recognize our needs, and more managers are trying to help supply colleges and universities with the money and equipment that they need to meet these needs."

Through 1981 and beyond, Thurston hopes the industry's managerial talents grow as rapidly as its opportunities. "I'm basically an optimist, and I see growing opportunity out there and hope that our electronics managers' skills increase in proportion. If so, we will have a healthy industry; if not, many firms won't be able to expand as rapidly as their markets. And if the latter happens, we will see companies with all sorts of growth glitches: money problems, turnover, and generally a degraded ability to compete. And our industry must bolster its ability to compete; we can't give world markets away on a silver platter."

Executive Outlook



L. J. SEVIN
chairman, Mostek Corp.

Though he still considers foreign competition a paramount problem, the Texas executive has decided to end his counterattack in Washington. Known as an outspoken critic of "Japan Inc." and of perceived U. S. government failure to enact policy and legislation to enable American semiconductor firms to be effective against competition from abroad, Sevin says he has given up promoting the cause on Capitol Hill. He notes several pending measures that could be beneficial—most notably proposed rules for accelerated equipment depreciation and for changes in capital gains tax policy.

But Sevin is not holding his breath in anticipation. "If some of these things come to fruition, fine. But if not, we won't be disappointed because we didn't get anything from 'em [legislators] in the past," Sevin allows. Instead, he advises the electronics industries to roll up their sleeves and do battle against foreign

competition. "They're here to stay and we're going to have to keep fighting them."

In terms of technological leadership, Sevin says the Japanese have pulled "dangerously close" to parity with the U. S., if they haven't already reached that point. But with or without Government help, Sevin says he's optimistic about U. S. companies' chances. "We're going to maintain parity [with the Japanese] and we're going to be competitive. At least a few of us are," he adds.

Sevin is also anxious about the U. S. economy in general. He expects it to remain essentially flat through at least April or May of 1981. The semiconductor industry—though buoyed somewhat by the cost-cutting and productivity improvements that its products can bring—will basically track the rest of the economy, remaining flat as the New Year unfolds, according to Sevin's overall estimates.



PAUL C. ELY
*executive vice president,
Hewlett-Packard Co.*

"My main concerns are the uncertainty in the U. S. economy, the economic situation in Europe, and their effect upon the rest of the world. The European economy lags the U. S. economy by four to six months, and it has a reasonably steep decline under way. Each cycle seems to be more tightly coupled than the last."

Looking at the general economy, Ely says he thinks the worst is not yet over. "Remember, the Government declared that the recession was over before it admitted that the recession was here. I think there could be a double-dip [recovery followed closely by another slump] to this one. There will be a boom period, however, sometime between now and 1983. There are two major factors involved in this that affect us in the computer industry. The first is industrial automation, which doesn't seem to be properly accounted for in current predictions, and the second is the use of small computers in business applications."

Adopting a global outlook, Ely believes that the Mideast represents a potential for catastrophe. "This makes it harder to predict for 1981 than for any of the past five years—even 1980 predictions were easier."

In terms of worries about competition from abroad, Ely says that the Japanese will compete everywhere in the world. However, European firms will compete more on a national basis, and primarily in their own home territories because there they possess nontariff advantages.



FRITZ A. LOHMANN
director, Philips GmbH

Like other executives in West Germany, Lohmann is concerned about the lack of qualified technicians and engineers, as well as the antipathy toward technological change shown by many people. The demand for qualified personnel "is a worldwide problem, and in some instances, it is not money that's limiting the progress of a project but the lack of qualified brains."

Lohmann, who is also vice president of his country's Electronic Components Association, gives credit to the industry for training university graduates not versed in semiconductor technology and to the government for contributing funds to universities for electronics studies. "However, there still is much hostility toward innovations, and that is keeping young people from using the opportunities offered to study electronics."

Regarding the attitude of labor unions toward labor-saving devices, Lohmann feels that they are beginning to soberly evaluate the facts and are treating the issues involved with less emotion.

Are the West Germans, with their increasing labor costs, pricing themselves out of foreign markets? Practically all semiconductor manufacturers have assembly operations in low-labor areas, Lohmann says. "In semiconductors, I think that Germany is in a good position and well up to world standards. Worldwide, we will be able to stand up to our competitors, if open-market conditions are maintained."



JOHN H. RICHARDSON
president, Hughes Aircraft Co.

Opportunities to conceive and sell new defense electronics programs have seldom been better. But Richardson foresees a troublesome bottleneck, familiar to executives who deal with the Government while striving to manage expansion, especially in a boom period. "Our surge capacity is nonexistent," explains Richardson. This capability to meet upgraded Department of Defense demands, in fact, already has acquired a title, "industrial responsiveness," which the Hughes official calls "the most significant thing now affecting our industry."

Richardson is a leader in defining the problem to Pentagon and congressional officials. A major cause, based on a Hughes in-house study, is that "suppliers view the defense marketplace as a less attractive place to do business than other market sectors." Excessive paper work, exacting requirements, and uncertainty about the future of any given

contract award all play a part. These specific disincentives are compounded by general shortages of labor and material, and a Federal tax policy that discourages capital formation and investment.

Concern about the impact of such troubles on national defense, however, has reached flashpoint; reform moves are now under way, and Richardson thinks improvements could start soon. One promising proposal is "multiyear contracting," whereby systems houses can get Government backing to ensure continuity from their suppliers through guarantees of funding and protection from sudden program termination. Also, he is hopeful about tax law changes and budget boosts.

In technology, Richardson does not sense that the U. S. is falling behind. "On the contrary, our problem is coping with it, with the right product at the right time at affordable cost."

Executive Outlook



KENNETH F. YONTZ

*vice president and general manager,
Allen-Bradley Co.*

Like many of his fellow executives, Yontz continues to cautiously watch the economy. He expects the coming year will be one of economic recovery, but the improvement will be gradual, with a potential for some backsliding along the way. As momentum builds, 1981's third- and fourth-quarter sales figures will come in higher than this year's last two quarters, he says. But total 1981 business will be off due to 1980's first-quarter strength.

Despite being "cautiously optimistic" for the near term, Yontz maintains that "our economy for the next four or five years is going to be a very uncertain situation." In such an environment, he predicts a gradual shift in purchasing policies by which electronics distributors will pick up larger market shares. Original-equipment manufacturers faced with high-

priced money will be striving to hold inventories down, Yontz reasons, and will thus be more willing to pay the premium associated with distributors as a supply source.

On the international scene, Yontz warns that "from a technological standpoint, I think the U. S. is losing its edge." One reason is that "the absolute number of new engineers coming into the industry is clearly less" here than it is in Japan, he points out, where the government "subsidizes the education of their technical people."

Yontz would favor, among other actions, a U. S. program of tax credits to encourage students to enter undergraduate technical degree programs. In general, he observes, "our Government has got to become more of an ally and less of an adversary to business."



JOHN F. MITCHELL

president, Motorola Inc.

Judging from his forecast, Mitchell is fairly sanguine about 1981. Prospects for a general economic turnaround depend heavily on the actions of the banking system, he stresses, forecasting a downward drift for interest rates, slightly subsidizing inflation, and an economic recovery beginning early next year that will build to a strong finish during the third and fourth quarters. Overall, the 1981 economy will top 1980 performance, he predicts.

Despite that outlook, Mitchell fears that "we're headed toward a bigger crisis" in the next cyclical downturn, unless some fundamental problems can be turned around. Prominent among his concerns is the business environment created by Government.

Another serious worry is the negative U. S. trade balance, which "is now the single biggest cause of inflation," Mitchell declares. "It's only coming down now because of the recession in this country," he continues. As the economy picks up, the trade deficit is likely to increase and will be "very bad again" by the middle of 1981.

Mitchell says he is heartened, however, by some recent signs of changing attitudes on the part of some in Congress. That deterioration in U. S. industrialization, trade capability, and competitiveness was a major problem in the 1970s is "just beginning to dawn on a lot of people," he says. This may lead to actions aimed at correcting the problems in the decade to come.



KLAUS LUFT

*vice chairman,
Nixdorf Computer AG*

Luft is no different from electronics executives in the rest of the world in being acutely aware of the strong Japanese presence. But unlike many others, he is not one to fret over it. In fact, he is optimistic.

"Sure, the Japanese will gain wider access to European and U. S. computer markets, but that is one sector where they cannot use their lower labor cost to full advantage," Luft says. To provide service and sales support, they must tap the same local reservoir of high-cost personnel as must native or other foreign firms. Besides, it will be difficult for the Japanese to crack the customer base that local companies have already built up.

For all his confidence, Luft is not without worries. One is the lack of a consensus in West Germany on the benefits of technology and the dubious reputation it has attained in some quarters. That, he says, has led to a severe personnel shortage.

Luft notes that there is not enough awareness of the need for intensive job training—in electronics, for example—and a lack of knowledge among people on what new technologies can do for society. As a result, science and engineering are viewed with suspicion, if not hostility.

Should the government step in to alleviate these problems? "Yes," Luft asserts. "It must devise policies aimed at reaching a consensus on the significance of technology and provide incentives for better job training."

EUGENE F. MURPHY

*president,
RCA Global Communications Inc.*

"The year 1981 will be the first full year that the total effect of the Federal Communications Commission's deregulation decisions will be felt. The commission should recognize this," says Murphy.

Those decisions affect international record (nonvoice) carriers like RCA in three ways. First, they permit the domestic-monopoly-based Western Union to operate in an overseas environment. Secondly, they allow AT&T to offer other than voice communications services overseas. And third, they let Comsat offer services to private customers.

The last two decisions do not stand out as problems for Murphy in 1981. "The FCC has authorized AT&T to provide international Data-phone service, which will compete with international Telex service. But I think AT&T's customers were probably already using their phone lines as data lines before that decision was made," he says. For Comsat, Murphy notes that the satellite services company has stated that it is not ready to go into business to provide service to individual customers as yet.

However, of ultimate concern for Murphy is the decision whereby Western Union will be allowed into the international record carrier market. "It does not make sense for the FCC to introduce this further competition at least until we [the already established international record carriers] have had an opportunity to establish our own domestic Telex market. In this way, we'd be in a position to pick up traffic directly from customers outside of the gateway cities," he says.

There were five of those cities until this year, when 16 were added. Some two to three years would be needed to set up such a network, and Murphy says that much of what the international carriers will be doing early in 1981 will be aimed at setting up centers in the 16 new cities. Then, the next step would be domestic Telex service, telegram, leased line, and facsimile.



Executive Outlook



HAROLD S. GOLDBERG
president, Data Precision Corp.

The recession is far down the list of Goldberg's concerns. His main apprehension is instead over a growing proliferation of products and companies in the low-cost end of the instrumentation market and a sense that the market could become "less technology-driven than marketing- and price-driven."

Goldberg perceives the picture as one of advancing technology reducing the potential excellence of the market. "Low-cost analog-to-digital converters and display drivers are making the cost of market entry lower, luring more new companies. Now, because of this there will be the usual proportion of ill-considered entries and products that will disappoint their customers and fail in the marketplace."

As a result, he foresees a shakeout. "I am looking for the low-end instruments market to fall to four or five companies within the next two to three years. Only the ones that can offer worthwhile technology in the face of heavy price competition will last." But until that shakeout occurs, Goldberg expects "more in the way of hotshot marketing than hot products in the low-end instrument market." He does not see the market as a whole softening, though he does expect change: as the low end becomes crowded, the high end should open up.

As for politics, he expects the American presidential election to have little effect on the economy. But continuing problems around the world, especially in the Middle East,

will force the U.S. to pay more attention to its own posture. And "sooner or later, this will translate into a realization that we could be economically and militarily better prepared, which in turn will mean larger corporate and Government R&D budgets."

Such a situation would benefit the instrumentation business, but would it lead to a boom? Goldberg is on the fence. "I expect that a combination of continuing fear of recession and inflation will force Government policies aimed at suppressing any general boom which might appear. But it's harder to hold back electronics today. The Government has less leverage in our business than it did 10 years ago, and our markets are now more nearly international. We may not boom, but we'll prosper."



DEREK ALUN-JONES
*managing director,
Ferranti Electronics Ltd.*

In what has become one of the worst recessions for the British since World War II, the military sector, in which Ferranti does 60% to 70% of its business, has looked comparatively well-insulated against the rigors of the times. But now even defense—a government sacred cow—is cause for concern as it undergoes a spending moratorium through April 1. "It has not affected major programs already under way," says Alun-Jones, but what he does fear is the cancellation of new programs.

Echoing what is becoming an increasingly strong plea from many British high-technology companies, Alun-Jones says he would like to see the government and state industries pushing high-technology by adopting defense techniques of placing orders large enough for new developments to encourage companies to engage in the necessary R&D to do such work. "A purchase-led development is always best," he says of the kind of support he would like to see adopted.

The recession, however, has brought with it some consolations. The supply of skilled engineers, once a major headache, has improved immensely in the past year. Wage expectations, too, have been reduced. But longer term, the prospects for an improving flow of better-quality engineers, believes Jones, have suffered a setback from the government's lukewarm response to the proposals for advancing the engineering profession contained in the Finiston report [*Electronics*, March 13, p. 94].



WALTER J. ZABLE
president and chairman, Cubic Corp.

"Three things bother me most," says the San Diego, Calif., executive, and the Federal government is at their center. "High interest rates are a concern to all business; nothing good can happen from them." Similarly, high taxes penalize the investor and inhibit capital formation as, for example, in the double taxation of dividends.

But Zable's main gripe is one he shares with most firms striving to boost foreign sales. "American companies in general should be doing more, but our own government regulations tie our hands in competing against overseas firms." In particular, the restriction on paying legitimate commissions to consultants and agents is an almost insurmountable barrier in some countries. There is a basic difference between blatant

bribery and honest commissions necessary to make a sale, says Zable. "No question, our evangelistic laws hurt us." Nothing less than changing those laws will help, he thinks. Cubic does business in a number of countries, selling computer-operated training systems for fighter pilots and fare-collection systems, among other things.

On the brighter side, the recession has not touched Cubic. "Business is better for us and the entire high-technology market than it has ever been," Zable notes. Funding of defense programs is looking up, and Zable sees the nation as a whole pulling out of the dip by the end of 1981. The San Diego area itself has sailed through any recent decline, he points out, and is still attracting new firms.

Executive Outlook



SIR JOHN CLARK

*chairman and chief executive,
Plessey Co.*

Clark's foremost worry — and pet peeve — is the industrial policy of the British government. Prime Minister Margaret Thatcher's government came to power a year ago with the most radical "Conservative" policy since the war, he says. Its cures for Britain's woes include a cutback of expenditures in the public sector to relieve the tax load on the private sector, an onslaught against inflation by strict adherence to monetarist policies, and a disengagement from the "interventionist" policies of earlier governments.

But, says Sir John, the government has failed in its plans to cut back in the public sector and, as a result, is cutting long-term capital programs, while continuing to borrow to finance its expenditures. Consequently, the only weapon for controlling the money supply is a massive 15% interest rate leading to an overvalued pound. In the meantime, he says, "the private sector is being slaughtered."

Sir John also doubts the appro-

priateness of the government's non-interventionist stance in a modern capital-intensive society dominated by technology. "Interventionism is a word based on dogma, and there is no place for dogma in government, only pragmatism. Government support has a proper place in the success of a capitalist-run economy." He admires as the supreme example of this philosophy the policies of the French. "They have chosen the sectors they are going to concentrate on, and they are going at it with enormous success. I would place the French ahead of everybody in this respect."

However, one of the largest military communications contracts ever placed in Britain — for the new Ptar-migan battlefield trunk communication system — went to Plessey, despite a moratorium on defense spending. Sir John is hopeful that this signals a change in government thinking on the need for the nation's government and industry to work and plan together.



KAZUO IWAMA

president, Sony Corp.

If only there were enough engineers to go around, Iwama would be a man without a care in the world. Sony plans to hire 400 engineers and scientists next spring, but has difficulties in recruiting them because of competition from such other technology areas as the machine tool, office machine, and automotive industries.

Iwama considers himself fortunate that Sony has no plans for large-scale software development in 1981 because software engineers are in even shorter supply. Still, he points out, there has been such a shortage for about 10 years, and Sony still has managed to develop new products and increase sales on old ones in that period.

On the bright side, says Iwama, is the fact that Japan has more consumer electronics engineers than any other nation, making it strong in both development and production technology. Thus, while for political reasons Sony will continue to manufacture in other countries, Iwama maintains that it would be much more efficient to build high-technology products in Japan.

Sony's chief executive also would like another company to invest heavily in video disk technology, the way Sony invested in video cassette development, to get the disk industry started. While his company will wait for the software to become available and then make players, Iwama says that Sony does not intend to be the big spender.



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USER OR
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TEST

Dynamic is certainly an apt description for random-access memories that need refreshing. Demand for these parts continues to grow at a phenomenal rate and everything about their design seems to be constantly moving up. Their addressing and data-transferal schemes grow more flexible and complex, and their density increases. But the resultant device complexity and the huge demand are putting test engineers between a rock and a hard place.

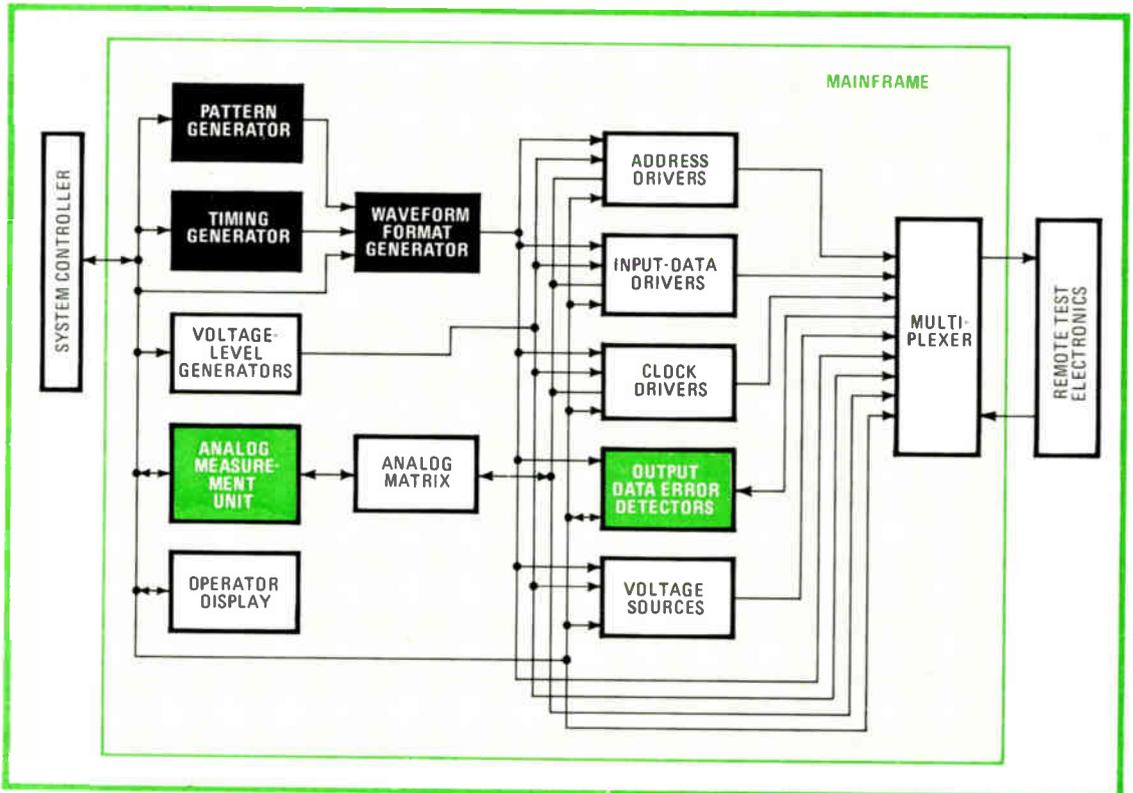
This series presents some of the latest tools and techniques to let engineers get the best of dynamic RAM testing. High-volume users, as well as designers, can use the flexible Teradyne system. Users who need to check relatively few parts will be better off with a GenRad system that handles memory and the logic usually accompanying it, discussed second. And regardless of the number of RAMs used, the testing methodology explained by National Semiconductor can supply better parts that need less testing.

-Richard W. Comerford

□ The speed and complexity of continually evolving random-access memories demand increased flexibility and accuracy from memory test systems. Waveforms now shown on device data sheets describe a complex interrelationship among input address, data, clock and control signals, and output data. These waveforms, usually with edges specified to within 1 nanosecond, must be accurately reproduced if a test system is to do its job.

The J389 memory test system was built to handle those tasks, both now and for the foreseeable future, in both design and high-volume testing. Its architecture provides a combination of flexibility and accuracy heretofore unattained in such systems.

For example, it is able to generate input waveforms whose edges can be programmed in 0.5-ns steps over the range from 0 to 32 microseconds and to deliver them accurately (to with-



1. Mainframe architecture. The pattern, timing, and waveform format generators (top left) share the signal formation process for greater flexibility. The format generator combines timing and pattern data to control the various drivers, whose outputs are multiplexed to the memory under test. The analog measurement unit ensures signal accuracy.

in ± 250 picoseconds) to the pins of the memory under test. It can also compare actual and expected output data at three independent strobe times, providing results accurate to within ± 500 ps and, by means of a programmable-interval detection mode, catch glitches.

Analyzing RAM performance

Functionally testing RAMs involves complex sets of information that a test system must be able to generate and compare. Different sets of addresses and data, referred to as test patterns, are used to verify the operation of individual segments of the memory under test.

These patterns are applied over a number of cycles that make up a functional test. In a full functional test, there are several types: write, read, read-modify-write, page mode, refresh, and so forth. Each cycle involves many activities: sending address information, various clock and enable pulses, and data to the device pins; and reading data out from the pins.

The device user must perform functional tests over a range of timing conditions—in which the cycle duration and the time of occurrence of activities are varied—and voltage levels. These tests reveal under what conditions the RAM will operate.

Functional testing therefore demands that the tester be able to create and handle data in a highly flexible manner. Furthermore, a high degree of accuracy must be attained consistently. An example of a typical RAM specification illustrates both requirements.

The data sheet for Intel's 2147H, a fast static RAM 1 bit wide by 4 K deep, specifies that output data is valid for the interval beginning 35 ns after the leading edge of the chip-select signal and ending at the signal's trailing edge. But according to the data sheet, the minimum chip-select signal the RAM can recognize is one with a 35-ns interval between leading and trailing edges. Thus, if the specs are interpreted literally, the data-valid interval would shrink to 0 ns.

Of course, the system designer would not build a memory board with a 0-ns data-valid interval, but the part allows him to shrink the interval to only a few nanoseconds or to extend it for as long as is necessary. And in this freedom lie some of the difficulties with which a test system must cope.

On the one hand, the test system must be able to verify the presence of high or low signal levels that may occur for only a few nanoseconds. On the other hand, the data-valid interval can be lengthened to tens or hundreds of nanoseconds (it may even extend into the next memory cycle), and the test system must be able to check this type of performance, too.

In either case, a thorough functional test involves verifying that the correct data appears precisely at the beginning of the data-valid

interval and is valid throughout it. Thus, the test system must check that while the data is present no glitches occur that could invalidate it—for example, a positive glitch on a data-low (0) signal could be interpreted as a 1 if the data is read when the glitch occurs. This capability takes on added significance today because glitches are often caused by internal or external waveform transitions that occur during the data-valid period and, as already noted, such activities can occur within each memory cycle.

Another device function that must be checked is that the output pins go to a high-impedance state after the device is deselected. This check must be done because memory board data transfers rely on a device's being deselected to prevent it from interfering with data transmitted by another part.

High impedance

For the 2147H, the spec sheet states that the output pin should enter this state not later than 30 ns after the trailing edge of the chip-select signal. If the board design is tight, as is usually the case with fast memory systems, this specification must be verified precisely.

With the growing importance of wider parts, it is no longer sufficient for a system to maintain accurate timing for one input and output data pin. For the 4- and 8-bit-wide devices already available and for the even wider memories coming, data transitions at all input and output pins must be practically simultaneous. That is, timing differences between pins—or skew—must be extremely small compared with the performance times being measured. Looking at these present and projected aspects of memory parts, Teradyne developed a system in which complex waveforms could be easily generated and the part's response to them easily compared.

This goal was accomplished through the use of a highly modular architecture, which also permits system capability to be enhanced as the users' needs demand.

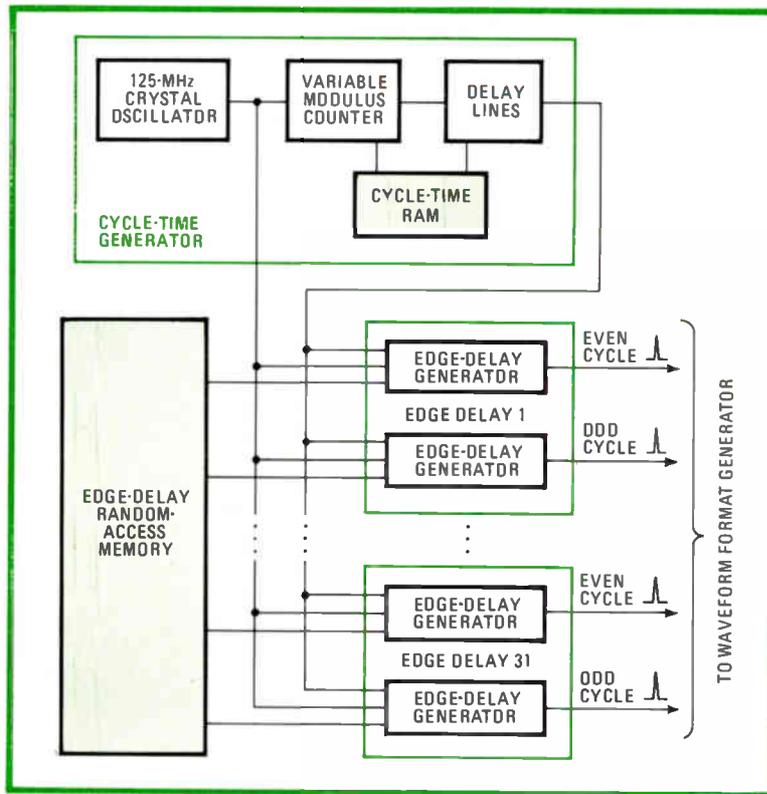
The individual components of the system must, of course, be capable of producing and checking waveforms with the accuracy that the parts being tested demand. But to be certain that that accuracy is maintained, an automatic edge-lock (AEL) capability was incorporated into the design. With this capability, timing and voltage levels are continuously monitored automatically, thus ensuring not only that the test results are accurate but also that the system is ready to perform when needed (see "Automatic edge lock," p. 136).

The J389 consists of a minimum of three units: the mobile system controller, the mainframe, and the test-head electronics. An additional test head can be added to the system.

The mainframe is the heart of the tester. It contains the pattern, timing, and waveform for-

USER OR
SUPPLIER
TEST

USER OR
SUPPLIER
TEST



mat generators, as well as the various drivers, analog measurement units, and switching matrices. The architecture of the mainframe, shown in Fig. 1, permits each of the testing requirements to be met by individual modules.

For functional testing, the most critical modules in the system are the pattern, timing, and waveform format generators. These three parts work together to produce the basic information need to generate and compare the waveforms for the memory under test. The pattern generator produces the cycle-by-cycle sequence of addresses, input data, and expected output data. The timing generator precisely defines the time for each cycle of the test and the set of edge delays—times at which events occur during the cycle. The waveform format generator combines the information supplied by both, in order to determine which events occur at what times within the cycle (the format) and to control the drivers and detectors.

In addition to generating the address and data needed, the pattern generator selects the cycle time and set of edge delays to be provided by the timing generator. It also selects the format set to be used by the waveform format generator. Its activities are controlled by a microprogram that is entered into its 64-word pattern-control RAM by the main computer.

The timing generator (Fig. 2) provides precise edges to clock information to and from the memory under test. These edges are derived from a 125-megahertz (8-ns period) clock using precision delay lines that divide the period into

2. Timing generator. Using a 125-MHz clock, data from the cycle RAM sets the length of each test cycle; the edge-delay RAM determines when in the cycle an edge is generated. Dual edge delays permit test events to extend from one cycle to another.

intervals of 0.5 ns each.

The timing generator is also microprogram-controlled, using values that are supplied by the main computer and stored in its cycle-time and edge-delay RAMs. The cycle-time RAM stores instructions for creating 16 different cycle times, and the edge-delay RAM holds instructions for creating 16 different sets of edge delays.

Each edge-delay set can consist of up to 31 edge delays. In order to allow a delay to extend into the cycle following the one in

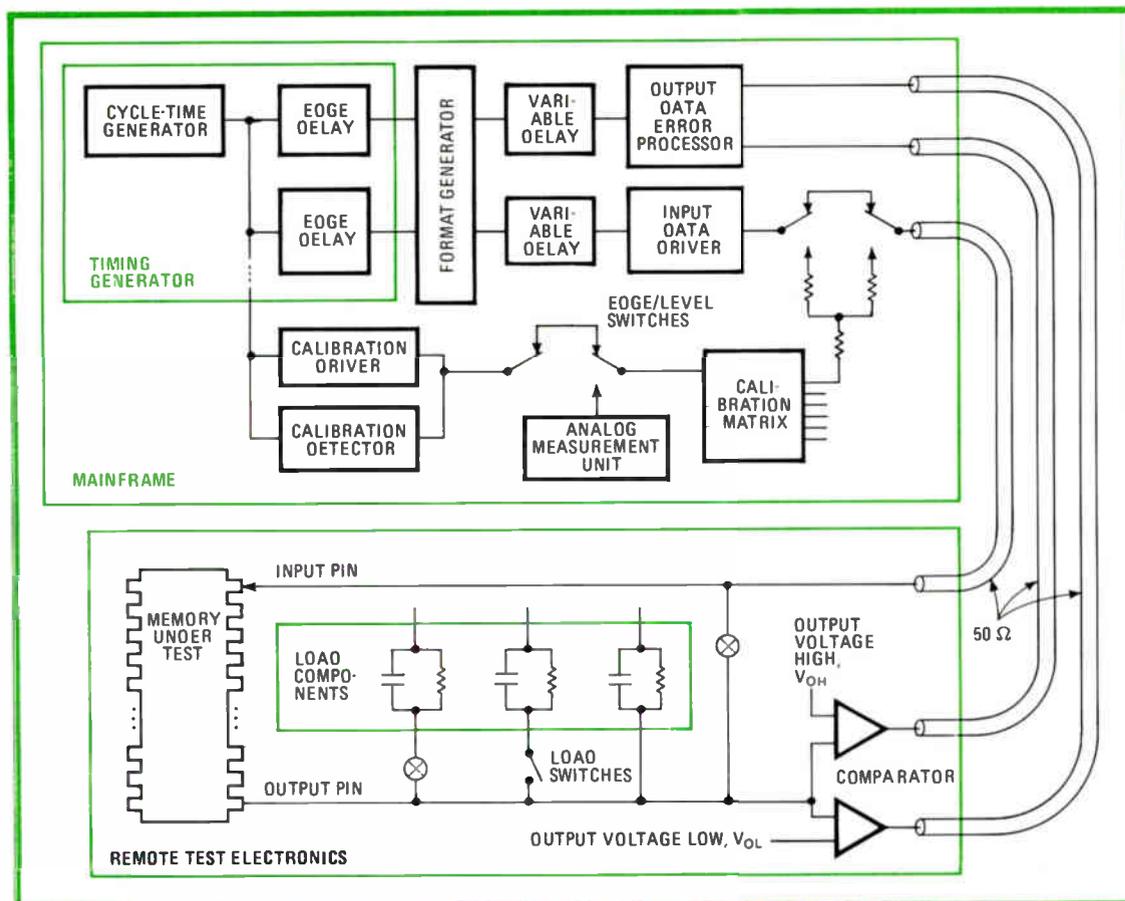
which it originates, a separate set of timing circuits is used for one cycle, and another set for the cycle following it. The use of two sets of circuits also permits the generation of two clock pulses in one cycle.

For each cycle of a functional test, the waveform format generator takes the information supplied by the pattern generator and, in accordance with the pattern generator's instructions, pulls a cycle time and a set of edge delays from the timing generator. With this information, the format generator can control the waveform transitions at the pins of the device under test. It also controls the times at which actual output data is compared with expected output data from the pattern generator.

Separate control

There is separate waveform format control, using microinstructions, for 8 X-address channels, 8 Y-address channels, and 12 input-data channels. At each of the six edge delays that define address transition times, the X-address or Y-address channels can remain at their format level, switch to the high or low level, or switch to the state of the corresponding pattern-generator address output or its complement. The same possibilities exist for the input data channels at each of the nine edge delays that define input data transition times.

There are two independent edge delays for each clock pulse. At each edge delay, a clock can remain at its former level, switch to the high or low level, or switch to the complement of its



3. Automatic check. The simplified schematic shows the output and the input path for a pair of memory pins. In the interval between device tests, the calibration circuitry is automatically switched to measure the path delay and variable delays are automatically set to equalize travel time, thus calibrating each line and greatly reducing skew.

former level. Independent control of the voltage transitions at each clock-edge delay allows single transitions within a memory test cycle, as well as a positive-going pulse in one cycle followed by a negative-going pulse in the next. The times at which output data from the memory under test is compared with the expected data is determined by three independent edge delays.

Format control also determines what output data comparisons are to be made for each edge delay. It can instruct the error detection circuitry to compare output data with:

- The programmed high detection level, detecting an error if any device output is lower than the detection level.
- The programmed low detection level, detecting an error if any device output is higher than the detection level.
- The programmed high impedance level, detecting an error if any device output is higher or lower than the detection level band.
- The expected data from the pattern generator and the programmed high and low detection levels.
- The complement of the expected data from the pattern generator and the programmed high and low detection levels.

It is also possible to make no comparison at all at any combination of edges.

In each format set, two detector formats are programmed for each of the three strobe times. One of these two sets is assigned to each detector, allowing different formats for data and control outputs of pseudostatic devices.

Outputs from the waveform format generator control the address, input data, and clock driver transitions. Each driver has a 50-ohm output impedance matched to the remote electronics.

High and low

The voltage level generators determine the high and low levels of address, input data, and clock waveforms and the levels with which the output data of the memory under test are compared. Any combination of input drivers and output detectors can be programmed to auxiliary voltage-level generators to allow individual characterization of pin voltage levels. Programmable voltage sources in the mainframe provide power to the power supply pins of the memory being tested.

The output data detectors are located in the test-head electronics cabinet as shown in Fig. 3. They compare output data from the memory

Automatic edge lock

With some random-access memories having access times of 20 nanoseconds or less, specified to within 1 ns, accurate timing within a memory test system is extremely important. In the case of 4- and 8-bit-wide RAMs, the skew, or timing difference, between input pins and skew between output data detection must be held to an acceptable minimum.

In the J389, the automatic edge lock (AEL) monitors edge-timing accuracy and automatically compensates for errors in address waveform edges, input-data waveform edges, clock waveform edges, output-data strobe times, input/output switching times, and load switching times. If a voltage error or a timing error occurs that is too great for correction by the variable delay circuits, an immediate warning appears on the operator display.

All time edges at the device's pins and at the data output detectors originate from the crystal-controlled oscillator of the waveform timing generator. Each system component between the oscillator and the pins of the memory under test contributes to a delay. Although the absolute value of this delay is unimportant, the same delay

in all paths is needed to control skew.

As shown in Fig. 3 (p. 135), in the J389 memory test system a variable delay in every path compensates for different inherent delays. This variable delay is under computer control and is automatically adjusted until all delays between the oscillator and the pins of the memory under test are within a 0.25 ns of each other.

Each variable delay circuit is controlled by an 8-bit register and has a resolution of 30 picoseconds. There are two variable delay circuits for each device driver and detector to allow for separate correction of the timed edges. Separate variable delay circuits for each format delay are provided for the address, data detection, input/output, and load control functions.

Built-in time-domain reflectometry (TDR) measures the delay for every waveform transition that can occur at a device's pins. This measurement is distributed among the short intervals between testing devices. If an error exceeds 0.25 ns, the variable delay in that path is changed under computer control to correct it. A warning message appears on the operator display if an error is too large to be corrected.

under test with the data expected. The detectors analyze the memory's output data in terms of level and time.

Up to 12 dual-comparator circuits in the remote test electronics module compare the output data levels from the memory under test with specified levels. One comparator of each pair compares output levels with the specified high level (V_{OH}), and the other compares output levels with the expected low level (V_{OL}).

When the device's output crosses a comparison level, the comparator generates an edge that is transmitted to the output data error processor in the mainframe. Each pair of comparators transmits detection edges to a separate error processor. The error processors use three separate edge delays to analyze the detection edges. These edge delays are programmable with a resolution of 0.5 ns and can be placed anywhere in a test cycle or deep into the next cycle.

A different detection mode can be assigned to each of the three edge delays. Edge detection occurs in a narrow window of approximately 100 ps at the time of the edge delay. In addition to edge detection, an interval detection mode can be programmed to detect any output data glitches that might occur during a data-valid interval for a memory under test.

Traditional memory test systems use either a single edge strobe or a window to detect glitches. With a single edge strobe, output data is verified at one instant within a read cycle. This type of detection can be very accurate but requires a functional test to be executed three

times in order to verify output data at the beginning and end of the data-valid interval and to verify the high-impedance condition. Any glitches in output data can be detected only by repeating a test several times with the strobe set at various positions in the cycle.

Window detection can verify the presence of output data during the entire data-valid interval and detect glitches during the interval. It has the disadvantage that it is inherently less accurate than edge strobe detection and is not useful when the data-valid interval is smaller than the minimum window width, usually 10 ns or more.

Strobes and window

The J389 uses three edge strobes and a window, or interval, to detect glitches, combining the advantages of both approaches. With three separately programmable strobe times, it can verify data throughout the data-valid interval and can test for the subsequent high-impedance condition all in the same test. This test replaces two or three separate tests required with less versatile output data detection, thus reducing test times.

Interval detection can be combined with strobe detection to detect output data glitches during intervals as short as 6 ns. Combining the two allows very precise verification of data at the beginning and end of the interval. For devices in which the data-valid interval is shorter than 6 ns, the edge strobe detection mode is still sensitive enough to detect output data errors. □

Microprogramming helps check LSI RAMs and logic

by Philip J. Eugene, *GenRad Inc., Concord, Mass.*

□ Companies that use LSI memories in small quantities generally must test not only those parts but large-scale integrated logic-oriented circuits as well. Both types of device demand a tester that is smart, stores patterns, and can generate complex clock signals.

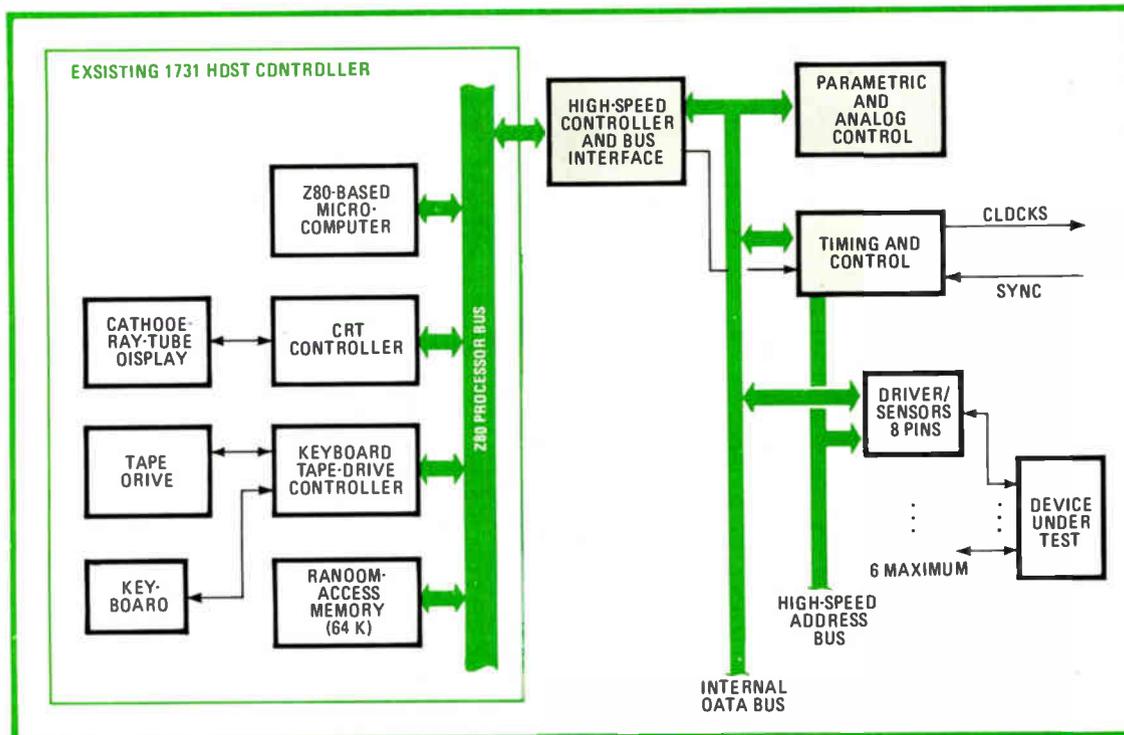
The GenRad 1732 fills the bill for both, while meeting the additional requirement of low cost. To do so, it has been given a distributed architecture based on a microcomputer tied to a fast microprogrammed controller. The latter controls and drives the smart (memory-behind-the-pin) driver/sensors and the synchronous pattern and clock generation. The microcomputer controls software generation, testing decisions, and display and data outputs.

In general, the stimuli needed to test digital medium- and large-scale ICs vary with the chip circuitry. The required stimuli can take two forms, either synchronous input (requiring a free-running clock) or sequential patterns (requiring setup-and-hold times) as in microprocessed instruction streams. Some LSI devices,

including microprocessors, require fast clocks for operation. Also, in the case of microprocessors, other logic-oriented devices, and dynamic random-access memories, the tester must be synchronized to the operation of the part.

Conventional testers using a minicomputer or a microcomputer to load or read driver/sensor pins are too slow to test LSI devices because of program overhead. This overhead may reduce the effective testing speed to a few hundred kilohertz when the host controller is directly coupled. Also, synchronization can be difficult because of the program overhead needed to sense and respond to status flags being manipulated by the device under test (DUT).

Testers using a stored pattern for each driver/sensor pin overcome the speed and synchronization problems but require a large memory capacity for complex test sequences. GenRad's microprogrammed 1732 test pattern processor uses only 4 K by 4 bits of memory behind each of 48 driver/sensor pins. This small test-pattern memory allows input and output testing, three-



1. Distributed testing. The 1732 digital IC tester uses a distributed architecture with a Z80-based microcomputer as the host controller and a microprogrammed controller for controlling and sequencing the driver/sensor electronics.

state testing, and "don't care" operations on consecutive test steps for any pin. Multiple passes and extra test vectors are eliminated by having complete cycle-to-cycle control of each pin. Program steps are further reduced by the use of microprogrammed control.

Further help is provided the user by a unique learn mode. Output portions of a test pattern are recorded from a known good device and this response becomes part of the test pattern.

Incorporating hardware and software

To cut the development time of the 1732, the host controller, a Z80-based microcomputer used in the older GR 1731 linear IC tester, was incorporated into the 1732 (Fig. 1). Added were a larger power supply and a keyboard overlay. The only hardware that had to be developed was the driver/sensor test electronics. Located in a second enclosure, it can be placed close to the handler or wafer prober.

The cathode-ray-tube display and keyboard allow interactive operations, for program entry or modification, and failure mode analysis, for functional, parametric, or bin (sorting) control. The new parametric and analog test section contains two sets of voltage drivers to allow testing of level translators, and a diode bridge to allow current loads to be connected as a device is functionally tested. In addition, a connect/disconnect feature permits the device to be driven on a pin-by-pin basis by a sequence of truth table steps to a desired state for parametric

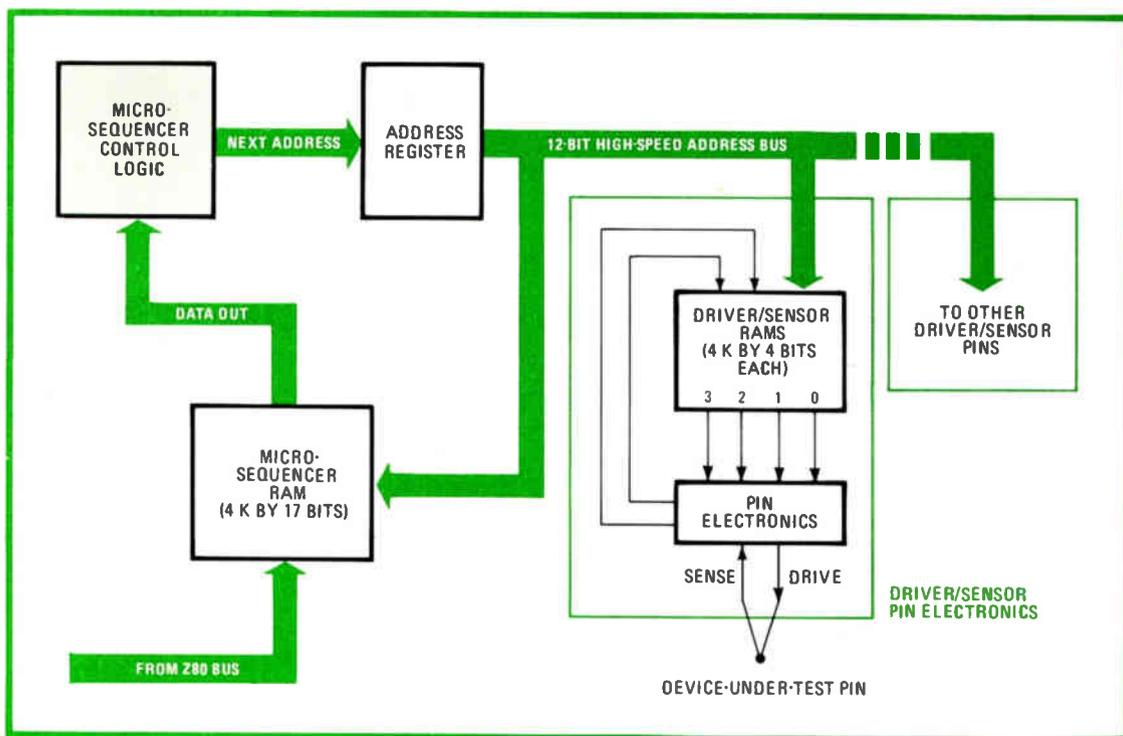
testing. Finally, a dual-level sensor is available for sensing mid-range or three-state (high- and low-voltage and high-impedance) conditions.

The high-speed controller interfaces with the Z80 processor bus. It takes the host processor's microprogrammed commands and drives the timing, control, and driver/sensor electronics. The timing and control module generates all clock and synchronization signals, and the driver/sensor modules (up to six each with eight pins) control the device being tested and store either pattern data or the device's response.

A unique feature of the 1732 and important for high-speed testing is its ability to microprogram the driver/sensor RAM's address sequence. This sequence, in turn, determines the operating mode of each pin (driver or sensor) and the signals that are to be applied to it. Microprogramming, with its relatively few program steps, permits a much higher testing speed than if the pins were addressed by the host computer.

The microprogram includes a wait command, to repeat a particular step, and a loop command, to repeat a series of instructions. It also includes a subroutine command, which is used to logically insert (into the microprogram) steps derived from a truth table that is developed for each type of device under test.

Figure 2 is a simplified diagram of the high-speed controller's interface with a typical pin module. The controller receives microinstructions, which the Z80 has converted from truth table states. These instructions are fed into the



2. Fast control. A 12-bit high-speed address bus links the driver/sensor electronics and its RAM to the high-speed controller. Microprogrammed commands from the host microcomputer are first stored in the microsequencer RAM and then shifted into the microsequencer. This unit then drives the driver/sensor electronics.

| TRUTH TABLE | | | | | | | | | | | | | | | | |
|-------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|--|--|
| PIN | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | FROM THE DESCRIBE DISPLAY | |
| STEP | 1 | 1 | 0 | 1 | 1 | 0 | G | 0 | 1 | 1 | 0 | 1 | 1 | V | FROM THE DEVICE TRUTH TABLE AND PACKAGE PINOUT | |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | G | 1 | 1 | 0 | 0 | 1 | 1 | V | | |
| 2 | 0 | 1 | 1 | 1 | 0 | 1 | G | 0 | 1 | 1 | 1 | 0 | 1 | V | | |
| 3 | 1 | 0 | 1 | 1 | 1 | 0 | G | 1 | 0 | 0 | 1 | 1 | 0 | V | | |
| 4 | 1 | 1 | 0 | 0 | 0 | 1 | G | 1 | 0 | 1 | 1 | 0 | 0 | V | | |

| MICROCOMMAND | | | | SOFTWARE CONVERTS INTO MICROSEQUENCER COMMANDS AND DRIVER/SENSOR COMMANDS | | | | | | | | | | | | | |
|--------------|-------------|------------|----------|---|----|----|----|----|----|---|----|----|----|----|----|----|---|
| ADDRESS | INSTRUCTION | DATA FIELD | HALT BIT | | | | | | | | | | | | | | |
| 0 | IPC | | 0 | OL | OL | SH | OL | DH | SH | X | OH | OH | OL | DL | DH | OH | X |
| 1 | IPC | NOT USED | 0 | OL | DH | SH | OH | OL | SH | X | OL | DH | OH | DH | OL | OH | X |
| 2 | IPC | | 0 | DH | DL | SH | DH | OH | SL | X | DH | DL | DL | DH | DH | DL | X |
| 3 | IPC | | 1 | DH | DH | SL | DL | DL | SH | X | DH | DL | DH | OH | DL | DL | X |

IPC = INCREMENT PROGRAM COUNTER
DL = ORIVE LOW
OH = ORIVE HIGH
SL = SENSE LOW
SH = SENSE HIGH
X = DON'T CARE



3. Truthful display. The CRT terminal of this tester has two display modes. The describe menu identifies the function of each device pin, and the truth table menu shows all possible logic states. Software converts this information into microsequencer and driver/sensor commands compatible with the high-speed controller.

microsequencer RAM, which stores them until the high-speed controller needs them; the address register simply holds addresses for the microsequencer or for the driver/sensor RAM.

The microsequencer control logic sends the microinstructions to the proper address in sequence in the driver/sensor electronics attached to each pin. This logic selects both the RAM contents for the pin electronics and the

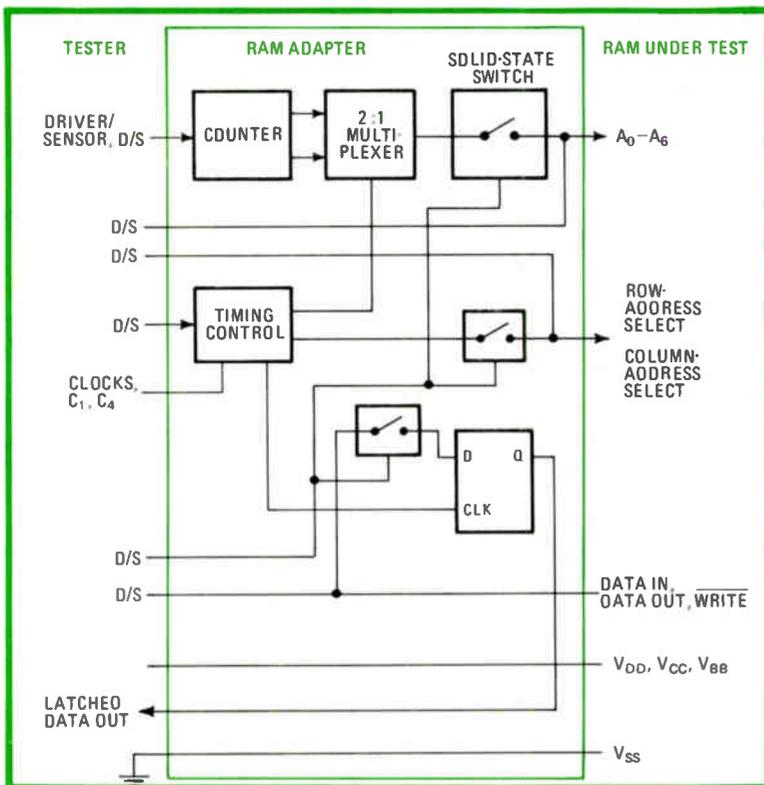
next microinstruction from the microsequencer RAM. Note that the contents of the driver/sensor RAM and the microprogram commands can be displayed on the system's CRT terminal.

Common addresses for the driver/sensor and microsequencer RAM address enables the microinstruction to control the flow of truth table execution. Also, the commonality of address results in an extremely wide microword containing the contents of the driver/sensor RAM control fields.

The width of the microword varies with the number of the tester's pins. For example, a 16-driver/sensor-pin system would have a microword $17 + (4 \times 16)$ bits, or 81 bits wide. A fully configured system with 48 pins would contain a 209-bit-wide microword.

The microsequence logic is built around an Am2910 microprogram controller chip. Although its instructions are 4 bits wide (giving 16 possibilities), only six

4. Memory test. The 1732 can test dynamic RAMs with the addition of this module, which provides an address counter and a timing generator for the row- and column-address select requirements of RAMs. The solid-state switches isolate TTL outputs.



types of instruction are used. The memory behind each driver/sensor pin is 4 bits wide and controls, at testing speed, pin operations.

A D/S pin can change direction (from driving to sensing or from sensing to driving) every cycle (program step) or whenever the first control bit of the driver/sensor RAM address changes. The second bit allows selected cycles to be sensed for error, and the third provides a means of checking that the output of the device under test is in a three-state mode.

Three-state outputs are checked by sensing that the output level does not swing to the high or low state. Mid-range sensing allows buses to be tested during times that the normal sense-high or -low mechanism cannot be used.

To generate test patterns automatically, the tester can be placed in the learn mode. Data from a known good unit is placed in the driver/sensor RAM and compared with data from other devices to see if they pass or fail.

Input sequences for the stimuli of the learn mode can be either hand- or software-generated. Software-generated patterns include binary count and gray code. A binary-count pattern was included to allow the contents of a test read-only memory to be learned. With the gray-code pattern, only 1 bit can be changed at a time, permitting unknown devices to be stimulated while preventing a race condition. Editing features let the user mix machine-generated (software-generated) patterns and manual patterns.

Synchronizing tester and device

Synchronizing the tester with the device is critical, otherwise test patterns are meaningless. Two synchronization methods are used: forced synchronization for most devices and self-synchronization for special devices.

Forced synchronization involves connecting a free-running clock to the tester's synchronization input and letting the driver/sensor pin force the device into a known initialized state (usually by forcing a reset). The desired pattern sequence can then be executed.

Most LSI devices, including microprocessors, can be handled that way. For microprocessors, the power-on reset line is used to bring the device to a known state. The tester then drives the data lines to force the microprocessor to execute the desired instruction stream.

Free synchronization is used when the tester cannot force the device under test to a known state or the device has an inaccessible clock. In these cases, the tester is synchronized by a key event that occurs at a given time in each device cycle. Examples of such events are the $\phi 2$ clock output of the 8080 clock generator chip and the M1 signal of the Z80 microprocessor.

Forced synchronization is more desirable, since it gives better pattern resolution—that is,

| STEP | COMMENT |
|------|--|
| 8 | RESET COUNTER TO 0 |
| 9 | READ LOCATION FOR 0 |
| 10 | WRITE LOCATION 1, CHECK READ DATA, INCREMENT COUNTER |
| 11 | REPEAT STEPS 9 AND 10 4,096 TIMES |
| 12 | RELOAD LOOP CONSTANT, RESET ADDRESS TO 0 |
| 13 | READ LOCATION FOR 1 |
| 14 | CHECK THAT DATA READ IS 1, WRITE ZERO, DECREMENT COUNTER |
| 15 | REPEAT LOOP 4,096 TIMES |

5. Adapter programming. A section of a test program listing for the dynamic RAM adapter gives the up-down sequence from a march test for a 4 K RAM. Note the use of the loop counter to repeat steps 9 and 10 4,096 times. With this technique, RAMs of up to 64 K can be tested.

the ability to change pattern within a device cycle—and more flexibility in terms of driving bidirectional lines. Free synchronization is limited because the state of the driver/sensor pins can be changed only once in a program step.

Before considering programming examples, it will be helpful to describe several operational aspects of the 1732, to show how the different CRT entries relate to the high-speed controller and driver/sensor RAMs.

Although there are many display menus to fill in with values, the two that most affect the high-speed controller and D/S RAMs are the truth table and describe displays. The former shows programmed logic output states versus input states for a specific device. The latter simply lists each of the truth table (TT) pins, and the operator defines their function. Any of eight types of pin may be defined: V for power, G for ground, C for clock, X for don't care, I for a device-under-test input, O for a DUT output, T for three-state, and B for bidirectional. The C pin allows the internal clocks brought out to the DUT adapter to drive the device. The clock pin must be specifically defined to permit software to adjust truth table operation for parametric measurements. The first two lines of the truth table of Fig. 3 show the pin functions of a typical quad two-input gate. These functions were previously entered on the describe display.

Once each device pin has been defined via the describe display, the truth table presentation can be loaded with the desired commands. As seen in Fig. 3, the truth table can be loaded from the package device pinouts with their appropriate input/output responses. The truth table represents a conversion into and from the driver/sensor commands. The reason for the two



MICROPROGRAM CONTENTS

| ADDRESS | MICROSEQUENCER COMMAND | DRIVER/SENSOR COMMANDS | | | COMMENTS |
|---------|---------------------------------------|------------------------|-------|----------------|---|
| | | RESET | CLOCK | TERMINAL COUNT | |
| 0 | CONTINUE | DL | DL | DDN'T CARE (X) | RESET COUNTER |
| 1 | LOAD LDDP COUNTER WITH 15 | DH | DL | SL | LOAD LDDP COUNTER |
| 2 | CONTINUE | DH | DH | SL | CLOCK |
| 3 | DECREMENT COUNTER | DH | DL | SL | RESET CLOCK |
| 4 | BRANCH \neq 0 TO STEP 2 CONTINUE | DH | DL | SH | END LDDP CHECK, CHECK TERMINAL COUNT |
| 5 | REST OF PROGRAM | | | | |

6. Microprogramming counts. The looping and subroutine capabilities of a microprogrammed tester can be seen in this example of the test program for a 74161 counter. Microprogramming requires only 5 program steps, versus the 33 steps of a conventional stored-pattern tester.

directions is that items like logic states, ground, and voltage entered on the keyboard are converted into DS commands, and items in the truth table display, which is loaded from a tape (or down-loaded from a development system), are converted from the DS command.

In a simple sequential truth table, the high-speed controller's microword gets loaded with a series of increment (INC) commands that advance the truth table to the next step. The end (E) command entered in the truth table causes a halt bit (step 3) to be added to the microword; this bit signals the logical end of the truth table.

A pair of IC types—a RAM and a 4-bit counter—illustrates the versatility of the 1732. A partial description of the programs used to test each device will show how microprogramming can reduce test-generation time.

Memory testing

The 1732 can test RAMs and ROMs directly if the address depth is not too large. A total of 4,095 vectors can be generated in the truth table, allowing a ROM of 4,095 locations to be verified (one vector to address each location). Since the majority of ROMs (and erasable programmable ROMs) are below this maximum vector amount, they can be verified against a known pattern without comparison with a known good device.

RAM testing usually requires more than 4,095 vectors. To execute a march test (a memory test pattern for minimal functional testing) on a 1-K device (1,024 locations) would require at least 3-K vectors—1 K to write background data and 2 K to write and read the complement for each cell. Consequently, a dynamic and a static RAM adapter were designed for the 1732. As dynamic adapter is a more complex version of the static one, only it need be described here.

The two main functions of the dynamic RAM adapter (Fig. 4) are to provide an address counter and a timing generator for the row-address

select (RAS) and column-address select (CAS) requirements of RAMs. Solid-state switches isolate TTL outputs, to allow parametric measurements on the pins of the device being tested. Both the counter (up-down) and the timing generator are under control from the driver/sensor pins; therefore, writing a truth table program is actually writing a memory test program (Fig. 5).

Also, in Fig. 4 note the use of the loop counter to repeat the step the required number of times. The loop count can be repeated up to 4,096 times, thereby enabling large RAMs (up to 64 K) to be tested. The program section in Fig. 5 is the up-down sequence from a march test for a 4-K RAM. If steps 8, 9, 12, and 13 were duplicated four times, a 16-K RAM could be tested.

The state (timing) generator runs off of the divided-by-4 version of the clock (found on the DUT board). Thus the speed of testing can change and all edges will remain in the same relation to each other.

Because of the clocked nature of the RAM, data out of it has to be latched to be examined. The latching requires the data be checked a cycle after it is read. Hence, in Fig. 5, although the data is read in steps 9 and 13, it is not checked until steps 10 and 14, respectively.

4-bit counter

The testing of a 74161 4-bit synchronous counter illustrates the use of the looping and subroutine capabilities. Figure 6 shows all the microprogram steps needed to test the counter. The terminal count (TC) output is used as the function to be tested, and a conventional stored test program is given to illustrate the efficiency of the microprogrammed approach to testing. (Both approaches allow the clock to be generated in a two-step, drive-low-to-drive-high pattern [steps 2 and 3].)

The microprogrammed approach needs only 5 steps, versus 33 steps for the conventional one.

And the microprogram can be used for any size counter (of similar design) by changing only the loop constant loaded in step 2; a conventional program would have to be regenerated and reloaded for the additional steps required. □



RAM maker's system tests ensure quality, free users

by Walt Milnor and Bill Johnston, *National Semiconductor Corp., Santa Clara, Calif.*



□ Current test regimens for dynamic random-access memories as they travel from the manufacturer's production floor to the user's final product will be too costly to handle the memory onslaught of the 1980s. To reduce the number of steps and thus the time and expense that are usually involved in those regimens, the Memory Test System program aims to create a new alliance between supplier and user that will streamline the process of testing increasingly dense RAM chips.

The MST program is a service for purchasers of 8-K and denser dynamic RAMs from National Semiconductor that adds about 35 cents to the

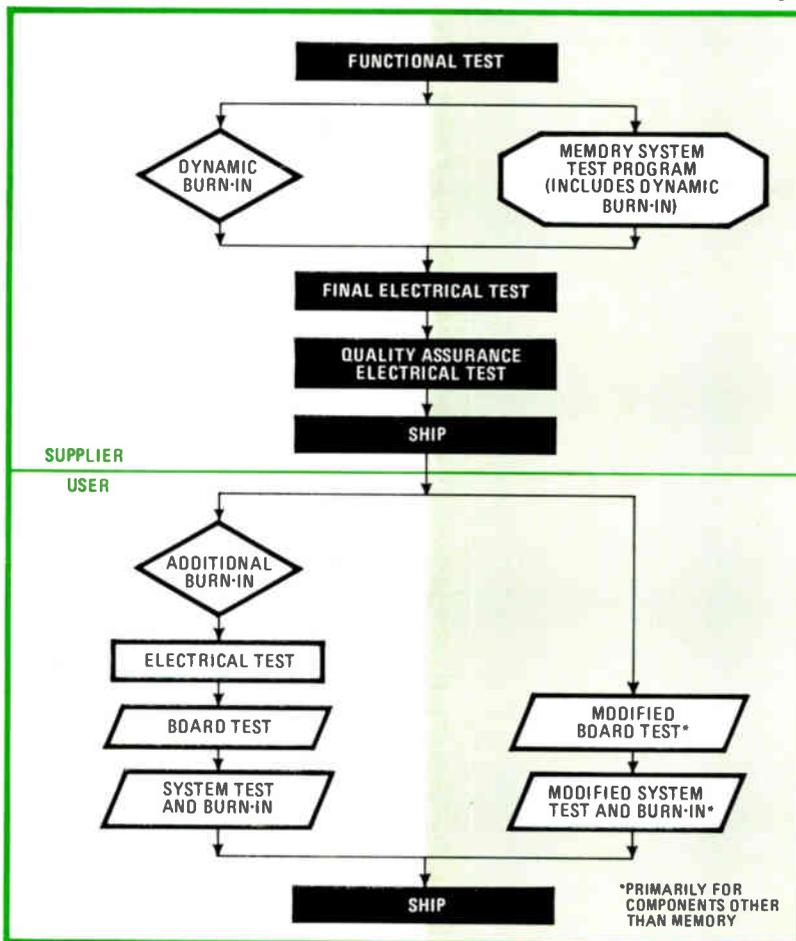
cost of the device. Before shipping, parts are tested on a special test system to make sure they operate both individually and as components of a future user's memory boards. The program eliminates the need for incoming inspection of RAMs and reduces the user's system-level rejects, speeding production and lowering costs.

Enhanced test combination

The MST program is based on a combination of tests that suppliers and original-equipment manufacturers typically perform on such parts. But those tests have been enhanced—they are performed at higher temperatures, at greater voltage margins, and in larger system environments than the user would employ. Further, while still in a system environment, the RAMs undergo a new functional test, Milpat (for Milnor's pattern), which detects errors caused by memory cell disturbance more thoroughly than previous tests have done.

An estimated 1.4 trillion bits of dynamic RAM were used in systems last year, and this year the figure is expected to more than double to 3 trillion bits. This increase in use will probably accelerate throughout the decade, presenting semiconductor suppliers and users with a monumental, costly test obstacle.

The upward trend in memory density has meant an increase in testing time. Operational complexity is increasing too. The latest devices have multiplexed data and address lines, for example. Test systems must be able to generate complex waveforms to



1. Growth path. When suppliers use the memory system test programs (right) in processing dynamic RAMs (left), users can bypass additional burn-in and electrical testing, putting higher-quality parts directly on boards and checking for correct insertion and peripheral component operation at the board and system level.

fully exercise the memory under test. This, as well as the requirement for greater test system capacity to handle larger memories, is forcing up the cost of test systems.

Figure 1 compares the testing usually done by manufacturers and users with the testing flow of the MST program. With the MST program, National tests at both the component and the system level so the user need only verify the performance of memory board components other than the RAMs during board and system test.

Of course, not all users now perform the burn-in and 100% electrical tests shown in Fig. 1; some sort out failures at the board level. For these users, too, MST program dramatically reduces problems at the board and system level.

The test program begins after the RAMs have undergone a functional test to ensure that parts on test boards will work, at least initially. These boards, called storage boards, can hold as many as 9 megabytes of 16-K RAM each.

Once loaded, the cards are plugged into the test system, which is checked at room temperature (25°C) to confirm that the RAMs have been properly loaded onto the storage cards and that the system is functioning correctly.

The RAMs are then subjected to an accelerated burn-in at 125°C while power supplies are operated at maximum, to ensure maximum internal voltage stress during switching transients. Under these thermal and operational conditions, any parts subject to infant mortality are screened out.

After this, parts are cooled to 70°C instead of room temperature and then functionally tested again—but this time as parts in a system. Keep-

ing the parts hot ensures that any drift mechanism caused by heat cannot heal before further testing begins. Most users perform system tests at 50°C or below. By performing those tests at 70°C, the MST program provides an extra margin of quality assurance.

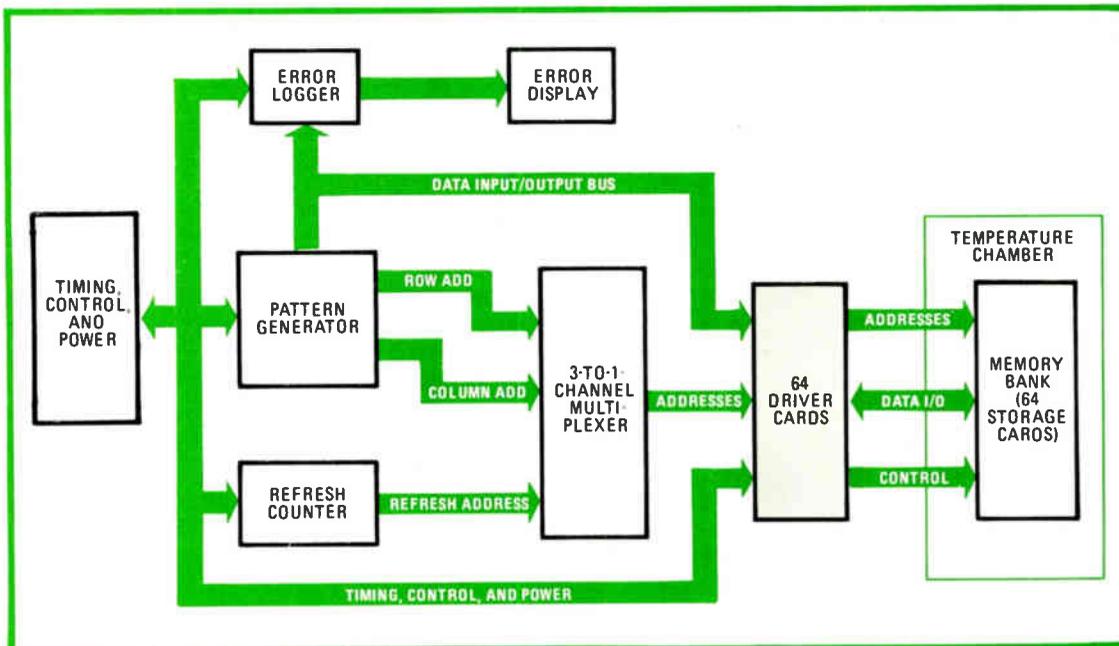
A user can request any of a number of test patterns for the RAMs and also ask that chips be tested for a specific time with those patterns. This means devices can be tested to the demands of a particular system design. As part of all functional tests, the voltage margins are varied beyond those of the specifications so that the RAMs are certain to meet the specs.

Errors are continuously logged during system test so any single-bit errors, even those due to soft (nonrecurring) failures, can be found. Both system testing and error logging take place as the parts cool to room temperature at the end of the test cycle, adding to the total test time and further checking the effects of thermal variation. Units that pass these tests then undergo parametric and ac testing, as well as the usual quality assurance tests, before shipment.

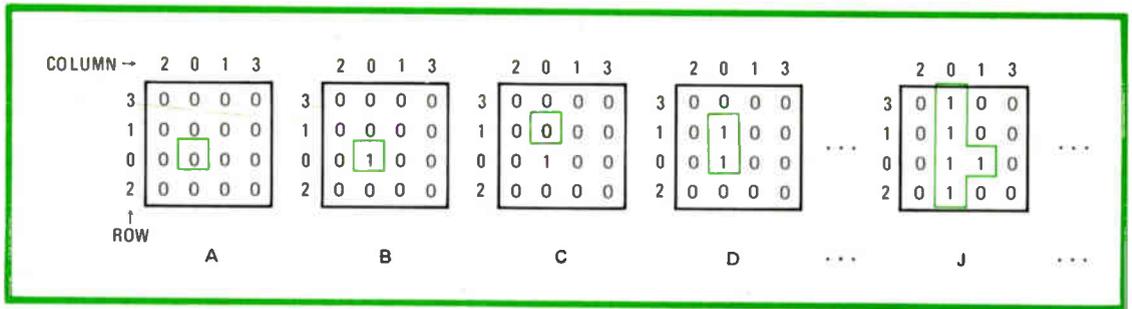
A special test system was constructed for the MST program. Architecturally, it is similar to most memory test systems, as shown in Fig. 2. But as indicated in the diagram, it has a unique mechanical arrangement.

To be certain any failures logged are in the RAMs being tested and not in driver electronics and other parts of the test system, only the memory storage cards are placed inside the temperature chamber. These are specially designed multilayer printed-circuit boards that are reliable to 150°C. The temperature chamber holds

SUPPLIER TEST



2. Mass memory tester. The architecture of the program's test system is similar to that of other test systems, but the tester can handle over 9 megabytes of 16-K RAMs. Driver cards are insulated from the temperature chamber so that they operate in a very stable manner; only memory storage cards are placed inside the chamber.



3. Milnor's pattern. This special pattern checks effects of cell disturbance on memory operation. After background of 0s is written into RAM, a cell is read (a) and 1 is written into it (b) and read several times until the end of the refresh cycle. Then a new cell in the column is read (c), 1 is written into it (d), and the cell is read until end of refresh cycle. Process repeats until column is filled and new column begun (j). The refresh time will elapse before any bit is refreshed.

64 such cards, each with up to 72 devices. The driver electronics for each card is on its own card outside the temperature chamber.

The pattern generator, also a key part of MST testing, can generate a wide variety of patterns. The usual patterns—galpat, skippat, checkerboard, and so on—are available, as is Milpat.

A real-time error logger continuously monitors the memory system, accumulating and retaining failure records until testing is complete. During testing, failed parts can be located using two light-emitting-diode arrays called a card map and a chip map. The card map comprises 64 LEDs and indicates which cards have failed parts. The chip map shows where on that card the failed RAM chip or chips are.

Among the errors detected and logged are those from refresh failures and improper operation within specified voltage margins. The refresh function is automatically checked the entire time the system is being tested; a distributed refreshing scheme is used. Voltage margins are also tested automatically using the system's programmable power supplies. Varying supply voltage over a range broader than that specified for the devices during the test is better than the fixed-supply approach often used to burn in and test a system.

Functionally testing dynamic RAMs for reliable system operation means checking each storage cell for a gain or loss of charge during the maximum refreshing time while cells around it are read. This cell-disturbance check closely monitors the memory under conditions it will most likely encounter in a system.

Cell-disturbance tests usually repeat a read or write operation at a given cell many times, trying to create a gain or loss of charge in other nearby cells. The activity used to disturb a cell can be a read or write cycle, since experience shows that the nature of the activity does not effect the failure rate.

Most disturbance tests have several disadvantages, however. They usually depend on device topology—addresses must be translated so that adjacent cells are written into or read. This requires an address translator and makes the

test system more complex and expensive. The topological dependence also requires unique counter sequences instead of straightforward binary counting. Further, while the memory under test is refreshed as required, the tests are performed without regard to the refresh state.

Milpat overcomes these disadvantages. The test pattern, chosen to be independent of device topology, can be applied without address translation and special count sequences. But most important, the test is based on the refresh condition, allowing maximum time for charge gain or loss before checking the cell's state.

Cell changes during a Milpat test are shown in Fig. 3 for a four-by-four-cell memory array with an arbitrary sequence of row and column addresses. The memory is initialized by writing a background of all 0s into the array, setting up a known state from which to begin.

The next step in the test is to read a cell and see that it has the value 0. A cell (0,0) is read and then a 1 is written into it. The cell is then read X times, where:

$$X = \left\lceil \frac{\text{maximum refresh time}}{(N-1)(\text{memory cycle time})} \right\rceil - 2$$

where N is the number of rows in the device.

Once this first cell is read X times, the next in the column numerically (1,0) is read and written into in the same way, followed by (2,0), (3,0), and so on until all cells in the column have been exercised.

This procedure continues, testing all columns until all the 0s initially entered are 1s. With this background, a MILPAT test is performed, which exercises the entire memory system by keeping a cell, once tested, alive with the pattern left in it. The next time through, when MILPAT is performed, any bits that have failed during the rest of the system test are detected. Not only is every cell tested for excessive gain or loss of charge with maximum refresh time, but the test also recognizes that cells tested during the first refreshing interval are merely exercised and repeats that test to fully test them. □

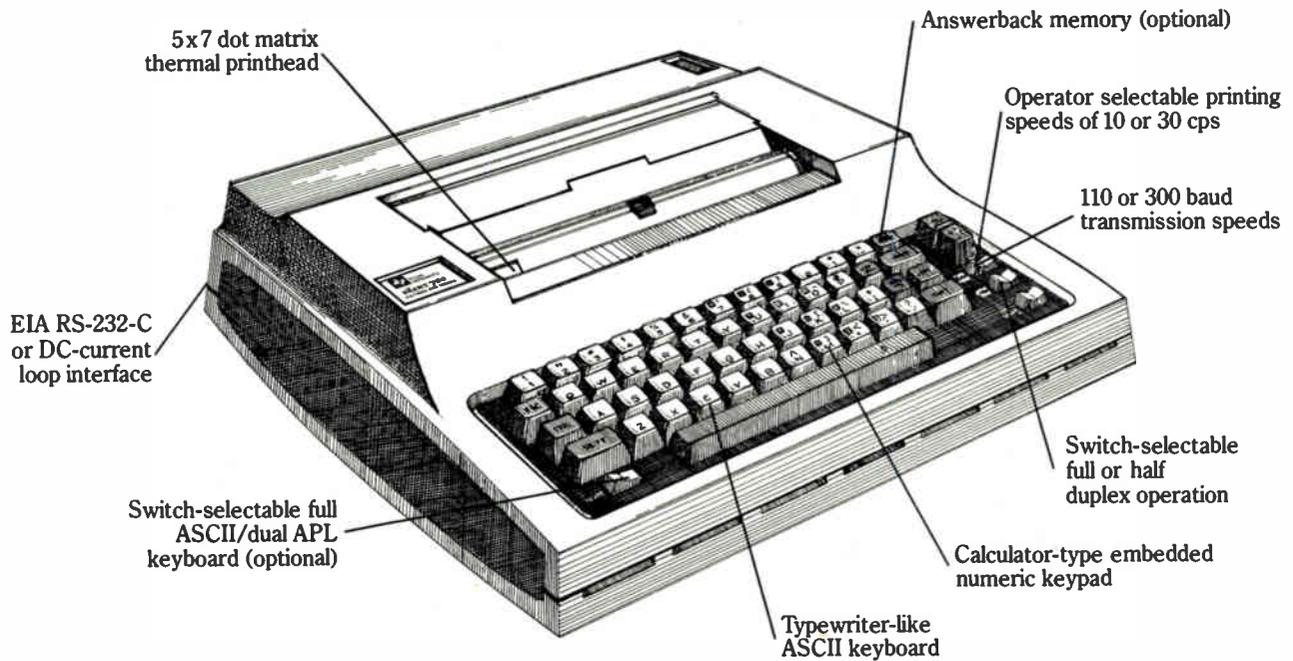
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Circle 145 on reader service card

Op-amp summer forms simple high-speed phase generator

by Dieter R. Lohrmann
Department of the Army, Harry Diamond Laboratories, Adelphi, Md.

A simple operational-amplifier summing circuit can generate an output voltage that is a rectangular- or sine-wave function of a dc source potential. For analog applications such as the direct phase modulation of a radio-frequency carrier, this circuit combines fast response with low throughput delay, making it superior to the often-used method of digitizing and reconverting an input signal with the aid of a microprocessor. In digital uses it can generate a pulse train having almost any pulse voltage-versus-dc input voltage characteristic.

In the circuit's general configuration, which for simplicity omits the stabilizing circuitry like bypass resistors and capacitors, resistors R_1 - R_7 form a voltage divider whose taps are alternately connected to the inverting and noninverting inputs of the adjacent comparators A_1 - A_6 . The outputs of the comparators are simply summed via resistors R_8 - R_{13} .

For a digital application (a), the incoming ramp is

used to generate a variable pulse-width train. When the ramp voltage is below the node voltage at point 1, comparators A_1 , A_3 , and A_5 are low (-7 volts), whereas A_2 , A_4 , and A_6 are high ($+7$ v). Thus, the output voltage will be midway between the two supply voltages, or at zero.

As the ramp rises above the node voltage at point 1, comparator A_1 switches, activating a fourth comparator, while two remain off. The output voltage thus jumps to 2 v, assuming resistances R_8 to R_{13} are of equal value. This voltage remains constant while the ramp voltage increases, until it exceeds the potential at the divider's second node, causing comparator A_2 to switch off. At this time, A_2 , A_3 , and A_5 are low, and A_1 , A_4 , and A_6 are high, returning the output voltage to zero.

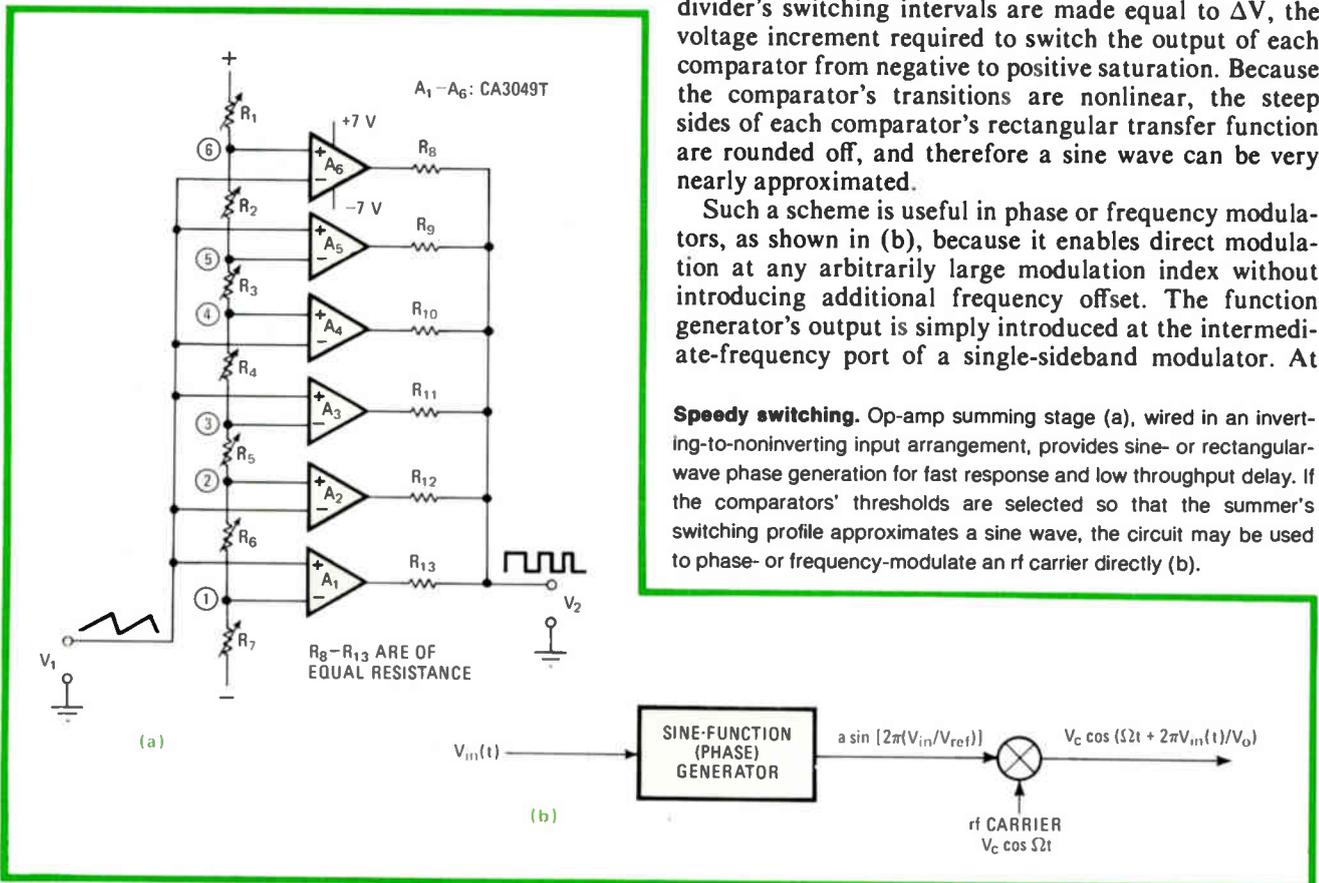
As the ramp voltage climbs past the potential at the third node, a similar operation moves the output to 2 v, because four comparators will be on and two will be off. The output drops to zero again when the ramp moves to a potential higher than at node 4.

The duration of each transition will be dependent upon the node and dc input voltages, which may be appropriately selected by the user. Consequently, a pulse train having almost any set of variable-width characteristics can be ordered.

In analog applications, a good approximation of a sine-wave function can also be generated if the voltage divider's switching intervals are made equal to ΔV , the voltage increment required to switch the output of each comparator from negative to positive saturation. Because the comparator's transitions are nonlinear, the steep sides of each comparator's rectangular transfer function are rounded off, and therefore a sine wave can be very nearly approximated.

Such a scheme is useful in phase or frequency modulators, as shown in (b), because it enables direct modulation at any arbitrarily large modulation index without introducing additional frequency offset. The function generator's output is simply introduced at the intermediate-frequency port of a single-sideband modulator. At

Speedy switching. Op-amp summing stage (a), wired in an inverting-to-noninverting input arrangement, provides sine- or rectangular-wave phase generation for fast response and low throughput delay. If the comparators' thresholds are selected so that the summer's switching profile approximates a sine wave, the circuit may be used to phase- or frequency-modulate an rf carrier directly (b).



the output of the modulator will appear the sum of the i-f and rf frequency, which is a cosine function applied to the modulator's rf port.

In this case, the function generator performs a phase modulation, because the phases of the generator and the rf carrier are added in the modulator. Thus, V_{in} causes a phase modulation of the rf carrier. The maximum modulation index is determined by the number of amplifiers in the phase generator. For a maximum modulation index

of M , $2M/\pi$ amplifiers are necessary.

If the SSB modulator is of the phasing type (which cancels the lower sideband by phase-shift mixing), orthogonal signals will be required at its i-f and rf ports. This function generator can be easily modified to generate a cosine-function signal, instead of a sine-wave output. Thus, a sine- and cosine-function generator may be combined to provide the orthogonal signals required for the SSB mixer. □

Optical agc minimizes video measurement errors

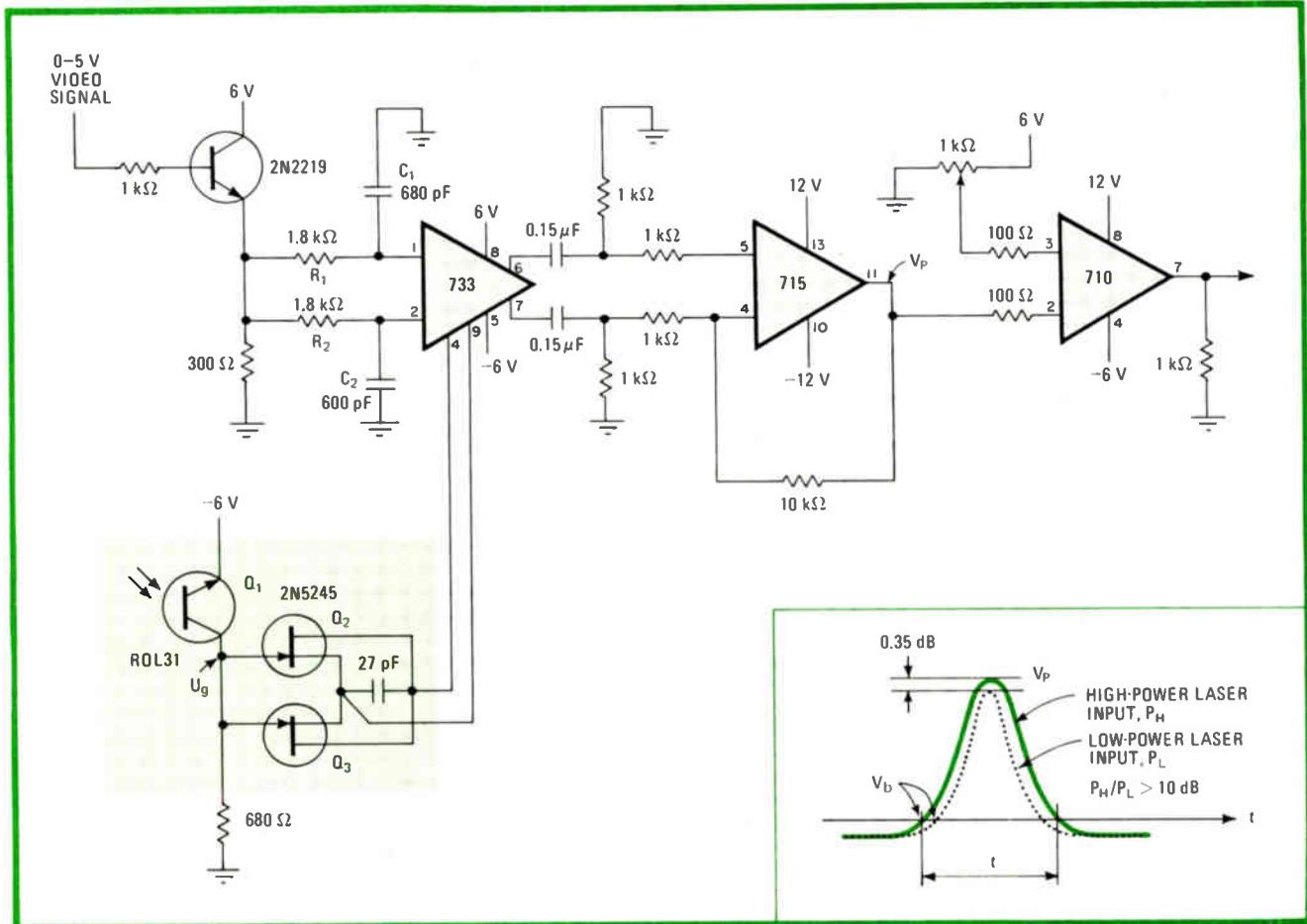
by D. Sporea and N. Miron
National Center of Physics, Magurele, Rumania

In an optical system, pulse width and peak amplitude are two information-bearing parameters that must be measured accurately for intensity-distribution and frequency-domain analysis—parameters that are difficult to determine when variations occur in the intensity of the

signal's laser light source. This difficulty may be virtually eliminated by using the unmodulated laser signal to provide automatic gain control of the amplifier that processes the optical signal from a video camera. Such a scheme rejects the black level of the optical input signal, minimizes drift of low-level detector thresholds, and reduces noise caused by light scattering through optical components for near-zero level signals.

Signals are applied in a balanced fashion to the $\mu A733$ video amplifier, as shown. R_1C_1 , R_2C_2 , and the excellent common-mode characteristics of the operational amplifier reject most optical noise and bias the black level below the amplifier's active region.

The gain is controlled by a phototransistor operating



Lightbeam leveler. Phototransistor sets gain of input amplifier, ensuring that variations in output power of unmodulated laser light source have little effect on pulse-width measurements of optical input signal, which is derived from video camera. Change in output amplitude is only 0.35 dB for laser-power variations of more than 10 dB. Detector's threshold voltage varies to a similar degree.

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in its linear region and two field-effect transistors whose drain-to-source resistance varies directly as a function of the reference laser signal. If the laser power increases, amplifier gain will be proportionally lowered, and vice versa, so that the output amplitude for a given video signal will be relatively independent of changes in the reference level. The signal is then amplified by the $\mu A715$ operational amplifier and presented to the $\mu A710$ high-speed comparator, where the switching threshold is set by the user.

In operation, the circuit provides excellent agc charac-

teristics. Typically, the peak voltage (V_p) at the output of the 715 (see inset) will vary only 0.35 decibel for a given video signal and a change in laser input power of more than 10 dB. The roll-off response of filters R_1C_1 and R_2C_2 is such that the detector's threshold voltage, V_t , varies to a similar degree. Consequently, the ratio of V_p/V_b is virtually unchanged, a condition required for accurate measurements of width versus intensity. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay \$50 for each item published.

V-MOS oscillator ups converter's switching frequency

by Bill Roehr
Siliconix Inc., Santa Clara, Calif.

The benefits of switching a flyback converter at high frequency to increase its efficiency and minimize its size may be realized by employing a V-groove MOS field-effect transistor as its power oscillator. Unlike bipolar power transistors, where storage-time effects hamper device turn-off, the turn-on and turn-off times for V-MOS units are fast—typically a few nanoseconds. Thus, switching speeds of 250 kilohertz can easily be achieved.

The circuit configuration is very simple, as shown. When the circuit is first energized, a positive voltage is capacitively coupled to the gate, turning on the VN10KM V-MOS device. Enhancement voltage is maintained by the potential across the transformer's primary, which is reflected onto its feedback winding. The FET continues to conduct until the core saturates, whereupon the feedback voltage collapses and turns the device off.

With the FET off, energy stored in the magnetic field

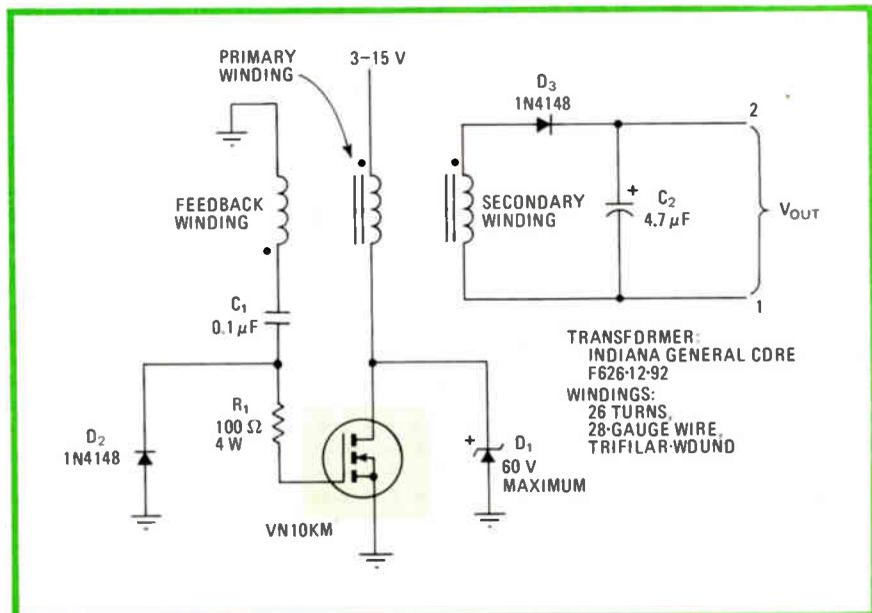
surrounding the primary winding is transferred to the secondary winding. Zener diode D_1 clamps the primary winding voltage to the desired potential and limits the voltage across the V-MOS gate to some value below its 60-volt breakdown rating. The energy transferred to the feedback winding has the proper polarity to hold the FET in cutoff. When the transformer comes out of saturation, the operating cycle repeats. Diode D_2 prevents negative spikes from damaging the gate of the FET. Resistor R_1 suppresses any parasitic oscillations caused by switching.

Energy transferred to the secondary winding delivers power to filter capacitor C_2 via rectifying diode D_3 . A single 4.7- μF capacitor provides sufficient filtering at the 250-kHz operating frequency. The dc output voltage may be made positive with respect to the main rail by grounding terminal 1 and negative with respect to the main rail by grounding terminal 2.

A dc output of up to 60 v can be developed by simply selecting a zener diode of that same value, although practically any voltage can be obtained by altering the transformer's turn ratio. The supply voltage should be set between 3 and 5 v dc.

Note that the physical size required for this flyback converter will be minimal, since the reactive components will be small and light because of the high operating frequency. □

High-flying. V-MOS power-FET converter easily operates at switching frequencies of 250 kHz and can work up to several megacycles, thereby increasing the efficiency of the flyback converter and also minimizing its size. Dc output potentials of up to 60 v may be ordered by appropriate selection of zener diode D_1 .



Adapting Fortran to top-down programming

Use of subroutines only, avoidance of all jumps are enough to create a structured format

by Wolfgang Nooss
Siemens AG, Munich, West Germany

□ Although the popular Fortran language is not block-oriented, its users can easily meet software engineering standards for microprocessor programming. They need only substitute subprograms for the hierarchic blocks basic to structured top-down program design.

Since this modular programming method does not require new language elements, it ensures full portability. It produces extremely small modules that force a structured approach on the program designer, yet it requires not much more computer capacity than unstructured programming. And the extra time it takes to write a program is more than offset by savings during program test and maintenance.

The advantage of designing a computer program with a top-down structure of hierarchic blocks is that it can be studied by an outsider (a new member of the design team, for instance) down to the level, or depth, necessary for his concern only. Another rule—never use a GO TO statement—allows a program block to be altered safely, without affecting other blocks. Both top-down and GO TO-less program design permit a software project to be divided efficiently among several team members.

Fortran and some other older programming languages, like Algol, Basic, and Cobol, were designed and standardized before these rules were established. However, users of these languages can do something to modernize them for the microprocessor scene.

In praise of Fortran

Fortran in particular seems worth updating. Not only is it the most common programming language among engineers, mathematicians, physicists, and scientists in many areas, but it is said to have drawn more users than any other programming language since its introduction in 1954. Its strong points are undoubtedly its machine code efficiency, its portability between different computers, and the ease with which it can be learned. Its weak points are allegedly its inability to support top-down program design or well-structured GO TO-less encoding and difficulty of program maintenance.

But structured programming is possible in Fortran. It does not require new language elements like the IF-THEN-ELSE, BEGIN, END, CYCLE WHILE, and CASE statements of the structured languages but only well-known standard Fortran-IV statements. Thus portability and compatibility are ensured. However, the number of Fortran instructions the user has to know for this purpose is

| SWITCH CONDITIONS CHECKED BY STRUFO PROGRAM | | | | |
|---|-------------------|------|------|---|
| Case | Switch conditions | | | Strufo's reaction |
| | C1 | C2 | C3 | |
| 1 | down | down | up | Prints message case 1 and goes on cycling. |
| 2 | down | up | down | Prints message case 2 and goes on cycling. |
| 3 | down | up | up | Prints message case 3 and goes on cycling. |
| 4 | up | down | down | Prints message case 4 and goes on cycling. |
| 5 | up | down | up | Prints message case 5 and goes on cycling. |
| 6 | up | up | down | Prints message case 6 and goes on cycling. |
| 7 | up | up | up | Prints nothing and goes on cycling, at most 10,000 times, then: |
| 8 | down | down | down | Prints conditions, run time, number of cycles, and stops. |

Cyclic blocks in Fortran

Cyclic blocks are easily constructed in Fortran by writing a universally applicable subroutine. It could look like this:

```
SUBROUTINE WHILE(ON,SUB,P1,P2,P3,P4,P5,P6,P7)
  LOGICAL*1 ON
  DO 11= 1,2
  IF(.NOT.ON(P1,P2,P3,P4,P5,P6,P7)) RETURN
  CALL SUB(P1,P2,P3,P4,P5,P6,P7)
1  I=O
  END
```

ON is the name of an external logical function, and SUB is the name of an external subroutine. In place of ON and SUB, the programmer may call the specific routines to be executed in the cyclic block. When the subroutine WHILE

is called, the subroutine replacing SUB is repeatedly carried out as long as the function replacing ON is true; otherwise control is passed back to the program that called WHILE.

The arguments of WHILE are the common set of arguments for both ON and SUB. For example, P1 through P4 might be arguments for ON and P3 through P6 the arguments for SUB. Both routines have to be supplied with the complete set of arguments when they are called, but they will use only their own subsets.

This universal subroutine can be extended. If the common set of arguments exceeds seven, more can be added. If cycles are to be nested, additional WHILE subroutines called WHILE1, WHILE2, and so on can be created.

rather smaller than for unstructured programming because structured programming requires abstinence from all tricky features a language offers. It is even possible to construct a cycle resembling an endless WHILE, which can be interrupted by an external or internal event, without using the GO TO statement.

Instead of GO TO and IF statements, the program designer has nearly always to introduce a new subroutine, and that necessity automatically prevents him from detailing a deeper part of his program too early. This is what top-down design actually means and what even a block-oriented programming language does not inevitably force since it offers nested BEGIN . . . END instead of CALL . . . However, it takes more time to design a Fortran program with subroutines instead of unlimited use of GO TO statements, and it is for the user to decide whether this investment is rewarded by an adequate increase of transparency.

Block structure in Fortran

To construct hierarchic program blocks in conventional Fortran, some simple means are available, all involving extensive use of the Fortran subroutine mechanism.

First, instead of the block structure of a sequence of statements between the BEGIN and END statements of other structured high-level languages, the programmer uses the Fortran subroutine structure. The subroutine's name can be thought of as a block identifier and the subroutine statements become a sub-block. An outsider planning to alter the program need not study the sub-block if it is not affected by the alteration.

Likewise, whenever a block is to handle an IF-THEN-ELSE condition, new subroutines are created. Also, if a number of cases are to be distinguished within a part of the program, instead of a CASE statement the case numbers are passed to a subroutine that calls up another subroutine with changed case numbers.

Finally, a loop that is to be interrupted by some event can be constructed by means of a general-purpose subroutine. In the example to follow, this subroutine is called WHILE because it simulates the function of a CYCLE WHILE statement.

To illustrate the principles involved, a program named Strufo (for structured Fortran) was designed to check

three external events represented by the positions of switches 1, 2, and 3. The three corresponding conditions are noted as C1, C2, and C3. A condition is defined as false if the switch is up and true if the switch is down. While the program is running, eight different cases can be created by changing the switches. As long as at least one of the switches is up, Strufo examines the conditions C1 through C3 and prints a message reporting on the switches' positions unless all switches are up, in which case it prints nothing. It also counts the loops it makes. As soon as all three switches are down or 10,000 loops have been performed, Strufo stops cycling, prints the switch positions and the run time, and then stops.

All the conditions checked for are listed in the table. Figure 1 is a Nassi-Shneiderman diagram, or structured flow chart of the program. This is a new type of flow chart developed in 1973 for structured programming by I. Nassi and B. Shneiderman.¹

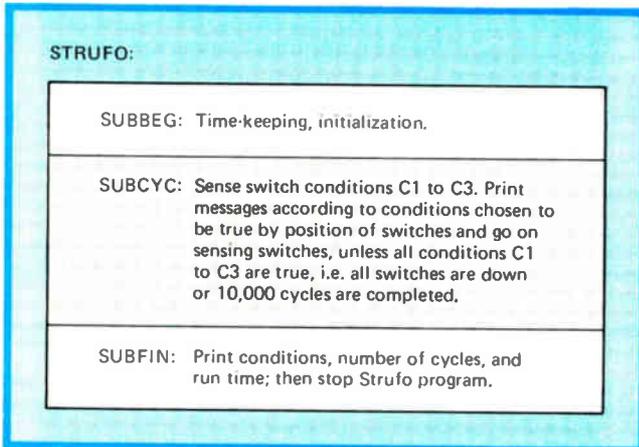
In structured programming a program is made by linking small independent modules called blocks. The Nassi-Shneiderman diagram in Fig. 1 shows an initial block called SUBBEG, the cyclic block SUBCYC, and the ending block SUBFIN in the order of execution in the computer. Since SUBBEG and SUBFIN have no sub-blocks and need no further detailing, there are no Nassi-Shneiderman diagrams necessary for them.

The Fortran source code for the main program of Strufo is simply this:

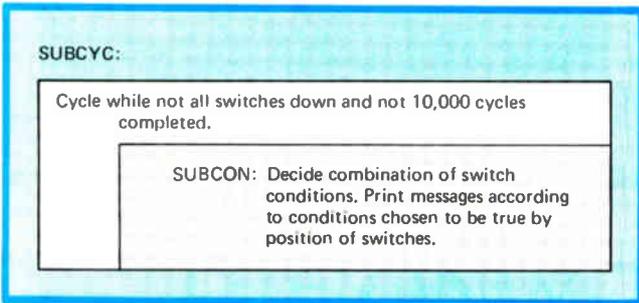
```
PROGRAM STRUFO
C  STRUFO CALLS SUBBEG, SUBCYC, SUBFIN
  LOGICAL*1 C1, C2, C3
  WRITE (6,1)
1  FORMAT(//7X,'STRUFO:')
C  (INITIALIZE TIME T AND NUMBER OF CYCLES N)
  CALL SUBBEG (T,N)
C  (CYCLE)
  CALL SUBCYC(C1,C2,C3,N)
C  (END)
  CALL SUBFIN(C1,C2,C3,T,N)
  CALL EXIT
  END
```

The entire program for this example is simply the linking of three blocks—in Fortran that means calling

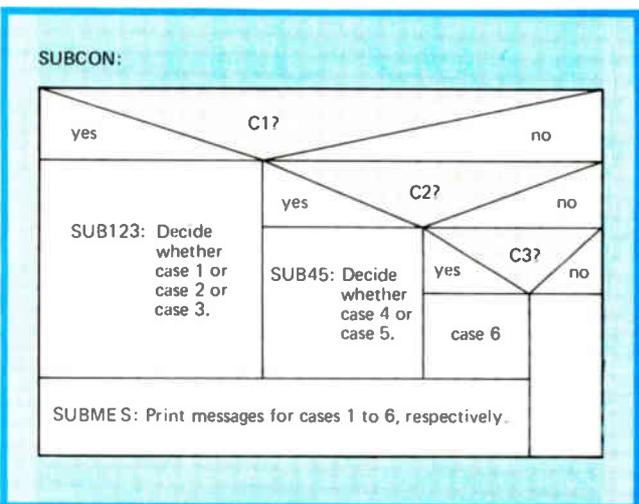
three subroutines in the order in which they are to be performed. As is clear, a block can have a structure, meaning that it has sub-blocks, and those sub-blocks may have sub-sub-blocks and so on. The Fortran equivalent is nested subroutine calls.



1. Top level. The main program, called Strufo for structured Fortran, is structured at the top level in an initialization (SUBBEG), a cycle (SUBCYC), and an end (SUBFIN) block. The SUBCYC block is the heart of the program and has a hierarchical structure of sub-blocks.



2. In deeper. The cycle block (subroutine SUBCYC) calls the subroutine SUBCON, which uses the subroutine WHILE to keep cycling through the sub-block that tests the switch conditions and prints out the results until all switches are up or 10,000 cycles are completed.



3. Hierarchical. SUBCON has another structural level containing three sub-blocks. There are two decision blocks, called SUB123 and SUB45, and the message-printing block, called SUBMES. SUB123 decides among the first three cases and SUB45 selects the next two.

The heart of the program is the loop, SUBCYC, which continues until interrupted by either of the following two conditions: all switches are down or the loop has been performed 10,000 times. This concept is called a cyclic block and is constructed with a CYCLE WHILE statement in many structured high-level languages. Since standard Fortran has no CYCLE WHILE statement, it is simulated (see "Cyclic blocks in Fortran," p. 151). The details of SUBBEG and SUBFIN are not shown.

The Nassi-Shneiderman diagram for the cyclic block SUBCYC is shown in Fig. 2. It has just one sub-block, called SUBCON.

The subroutine SUBCYC uses the general-purpose WHILE subroutine with the logical function COND determining the conditions and the subroutine SUBCON selecting the messages to be printed for the first six cases. In this specific use of the general-purpose subroutine WHILE, COND replaces ON and SUBCON replaces SUB. The Fortran source code for the module SUBCYC is written thus (again, note how small the module is):

```

SUBROUTINE SUBCYC(L1,L2,L3,I4)
  C SUBCYC CALLS FUNCTION COND, SUBCON, WHILE
  LOGICAL*1 L1,L2,L3
  EXTERNAL COND, SUBCON
  CALL WHILE(COND, SUBCON,I4,L1,L2,L3)
  RETURN
END

```

The logical function COND is written as:

```

FUNCTION COND(I1,L2,L3,L4)
  LOGICAL*1 COND,L2,L3,L4,SWITCH
  COND = .FALSE.
  L2 = SWITCH(1)
  L3 = SWITCH(2)
  L4 = SWITCH(3)
  IF(I1.GE.10000) RETURN
  IF(.NOT.L2.OR..NOT.L3.OR..NOT.L4) COND = .TRUE.
  RETURN
END

```

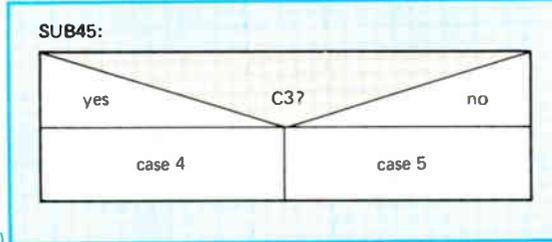
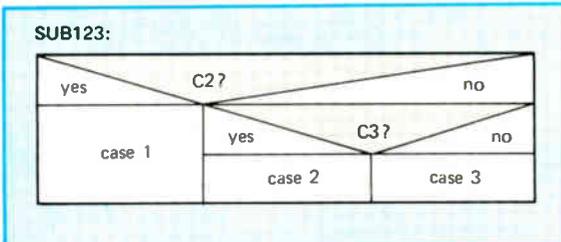
The logical function COND is false if all switches are down or 10,000 cycles have been run; otherwise it is true with the positions of the switches being indicated by the variables, L2,L3 and L4. COND uses the function SWITCH, not shown, which senses the switch positions.

SUBCON has three sub-blocks, SUB123, SUB45, and SUBMES, shown in the Nassi-Shneiderman diagram in Fig. 3. The source code for SUBCON follows. The variable I1 counts the cycles.

```

SUBROUTINE SUBCON(I1,L2,L3,L4)
  C SUBCON CALLS SUB123, SUB45, SUBMES
  LOGICAL*1 L2,L3,L4
  I1 = I1 + 1
  IF(L2) CALL SUB123(L3,L4,I)
  C (L2 = TRUE; C1 DOWN: CASE 1,2 OR 3)
  C (SUB123 DETERMINES WHICH)
  IF(L2) CALL SUBMES(I)
  C (SUBMES PRINTS MESSAGE FOR CASE 1,2, OR 3)
  IF(L2) RETURN
  IF(L3) CALL SUB45(L4,I)
  C (L2 = FALSE, L3 = TRUE: CASE 4 OR 5)
  IF (L3) CALL SUBMES(I)

```



(a)

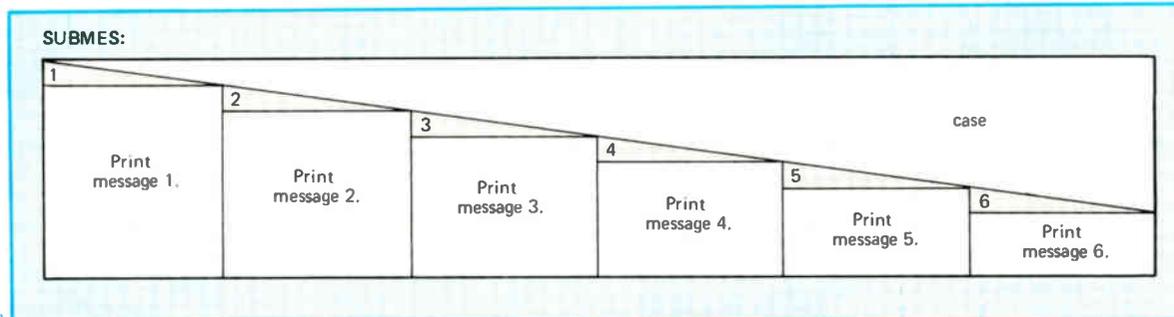
```

SUBROUTINE SUB123(L1, L2, I3)
SUB123 DECIDES FOR CASE I3= 1 TO 3 ACCORDING TO
COMBINATION OF CONDITIONS L1, L2
C
C LOGICAL *1 L1, L2
I3 = 1
IF (L1) RETURN
(L1 = TRUE: CASE 1)
I3 = 2
IF (L2) RETURN
(L1 = FALSE, L2 = TRUE: CASE 2)
I3 = 3
RETURN
(L1 = L2 = FALSE: CASE 3)
END
  
```

(b)

```

SUBROUTINE SUB45(L1, I1)
SUB45 DECIDES FOR CASE I1 = 4 OR 5 ACCORDING TO
CONDITION L1
C
C LOGICAL *1 L1
I1 = 5
(L1 = FALSE: CASE 5)
IF (L1) I1 = 4
(L1 = TRUE: CASE 4)
RETURN
END
  
```



(c)

```

SUBROUTINE SUBMES(I1)
SUBMES PRINTS 6 MESSAGES ACCORDING TO 6
CASES I1 = 1 TO 6
C
C IF (I1.EQ.1) WRITE(6,1)
1 FORMAT(7X,' SW1 AND 2 DOWN, SW3 UP')
IF (I1.EQ.2) WRITE(6,2)
2 FORMAT(7X,' SW1 AND 3 DOWN, SW2 UP')
IF (I1.EQ.3) WRITE(6,3)
3 FORMAT(7X,' SW1 DOWN, SW2 AND 3 UP')
IF (I1.EQ.4) WRITE(6,4)
4 FORMAT(7X,' SW1 UP, SW2 AND 3 DOWN')
IF (I1.EQ.5) WRITE(6,5)
5 FORMAT(7X,' SW1 AND 3 UP, SW2 DOWN')
IF (I1.EQ.6) WRITE(6,6)
6 FORMAT(7X,' SW1 AND 2 UP, SW3 DOWN')
RETURN
END
  
```

4. Bottom level. Details of the three lowest-level blocks in the structure of Strufo are shown in Nassi-Shneiderman diagram form and in Fortran source listings. As is the case with all the modules in the program, these three are short, easily understood subroutines.

```

C IF (L3) RETURN
IF (L4) CALL SUBMES(6)
C (L2=L3=FALSE, L4=TRUE: CASE 6)
RETURN
END
  
```

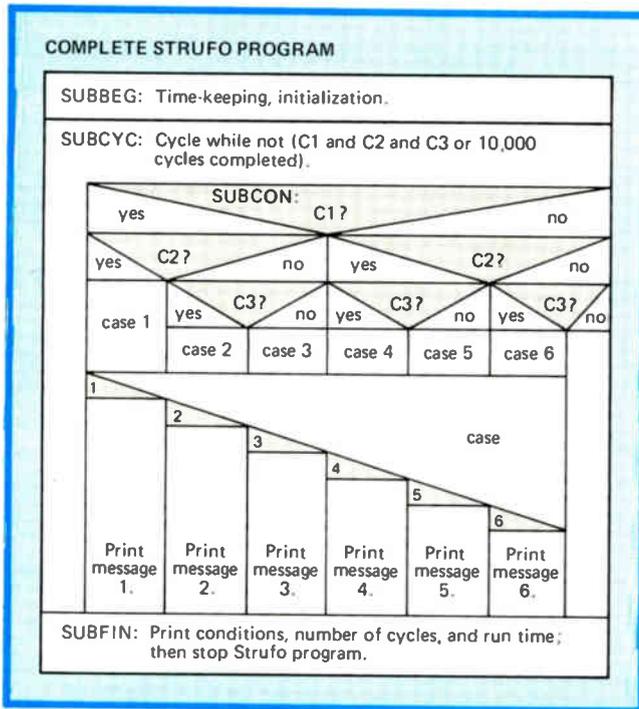
The subroutine SUB123 determines which of the first three cases exists after the subroutine SUBCON has determined that switch C1 is down (see Table 1). The subroutine SUB45 determines whether it is the fourth or the fifth case when C1 is up and C2 is down. And SUBMES is the subroutine that prints each of the six messages for each of the six cases. The Nassi-Shneiderman diagrams and the source code for these three subroutines are shown in Fig. 4.

The total assembly of the program Strufo is shown in the Nassi-Shneiderman diagram in Fig. 5. All the decision paths shown in this diagram are easily satisfied

without the use of the GO TO statement.

In order to check how much memory space and computer run time is invested in this kind of top-down structuring, an unstructured version of the program Strufo was written (Fig. 6). Both programs were compiled, linked to load modules, and run. The structured program occupied approximately 12.5% more memory space than Unstru, the unstructured one. However, with larger, more realistic programs, the discrepancy will be smaller since there will be more productive statements than administrative ones.

The differences become more evident with run time. When the three switches were constantly left up to suppress printing of messages, it took the structured program more than twice the computer time to perform 10,000 cycles. But when switches were moved during the running of the programs and put down after five cycles,



5. All together now. Combining all the blocks into one Nassi-Shneiderman structured flow chart shows the structure of the entire Strufo program. All the "no" answers down the right side mean that all switches are down and control falls through to the last block.

the discrepancy decreased to less than half a percent. Unstru's lead went on decreasing as the number of cycles producing printed messages was increased.

In realistic programs that have to do more than just sense switches, structuring by conventional Fortran subroutines will not cost much computer capacity. In addition, long lists of arguments may be replaced by COMMON blocks, thus cutting run time as well as memory requirements. Further, the method inevitably produces very small and simple blocks, preventing the program designer from prematurely going into detail more strictly than block-oriented programming languages do.

Time ratios

It should also be noted that Strufo and all its subroutines took 10 times longer to write than Unstru, the unstructured version of the same program. Unless lower time ratios were typical of other programmers, only long-life programs that needed to be altered often by a changing staff would be worth such an investment.

On the other hand, when the method was applied to a practical problem requiring several WHILE cycles to be nested, it was felt to work quite conveniently. The top-down structuring procedure (not the programming procedure) was first pushed forward in the direction of the kernel containing the productive cycles, as was done between SUBCYC and SUBMES in the simple example. Then the more administrative parts like SUBBEG and SUBFIN were detailed, and the program input came the last. The requirements encountered in the very depth of the kernel could still be satisfied when the outer shell was detailed. This is not "hardest first" but "top-down" and "hardest first down" structuring.

```

C      PROGRAM UNSTRU
C      UNSTRU DEMONSTRATES MEMORY AND RUNTIME BENEFITS DUE
C      TO UNSTRUCTURED CODING AT THE EXPENSE OF TRANS-
C      PARENCY, COMPARED WITH GO-TO-LESS TOP-DOWN STRUCTUR-
C      ING AS IN STRUFO (SEE THERE). UNSTRU TOOK APPR. 1 H
C      TO BE WRITTEN; STRUFO TOOK APPR. 10 H.
C
C      LOGICAL*1 C1,C2,C3
C      WRITE(6,200)
C      200 FORMAT(//7X,'UNSTRU:/' )
C      N=0
C      (NUMBER OF CYCLES)
C      T=-1.
C      (FOR JUMP TO 400)
C      300 CALL TIME(I,K)
C      TOLD=T
C      (FOR 900)
C      T=(1#32768.+K)/50.
C      (COMPUTER TIME IN SECONDS)
C      IF(TOLD) 400,900,900
C      (900) 2. TIME-KEEPING FOR RUNTIME PRINT AFTER LAST
C      CYCLE)
C      400 CALL SSWTCH(1,I)
C      C1=I.EQ.2
C      (C1=TRUE WHEN SWITCH 1 DOWN)
C      CALL SSWTCH(2,I)
C      C2=I.EQ.2
C      (SWITCH 2)
C      CALL SSWTCH(3,I)
C      C3=I.EQ.2
C      (SWITCH 3)
C      IF(C1.AND.C2.AND.C3.OR.N.GE.10000) GOTO 300
C      (ALL SWITCHES DOWN OR 10000 CYCLES RUN: NO CYCLE OR END
C      OF CYCLE)
C      N=N+1
C      (NUMBER OF CYCLE)
C      IF(C1) GOTO 500
C      IF(C2) GOTO 600
C      IF(C3) WRITE(6,420)
C      420 FORMAT(7X,'SW1 AND 2 UP, SW3 DOWN')
C      GOTO 400
C      (NO PRINT; WHEN ALL SWITCHES UP)
C      500 IF(C2) GOTO 700
C      IF(C3) GOTO 800
C      WRITE(6,520)
C      520 FORMAT(7X,'SW1 DOWN, SW2 AND 3 UP')
C      GOTO 400
C      (NEXT CYCLE)
C      600 IF(C3) GOTO 850
C      WRITE(6,620)
C      620 FORMAT(7X,'SW1 AND 3 UP, SW2 DOWN')
C      GOTO 400
C      (NEXT CYCLE)
C      700 WRITE(6,720)
C      720 FORMAT(7X,'SW1 AND 2 DOWN, SW3 UP')
C      GOTO 400
C      (NEXT CYCLE)
C      800 WRITE(6,820)
C      820 FORMAT(7X,'SW1 AND 3 DOWN, SW2 UP')
C      GOTO 400
C      (NEXT CYCLE)
C      850 WRITE(6,870)
C      870 FORMAT(7X,'SW1 UP, SW2 AND 3 DOWN')
C      GOTO 400
C      (NEXT CYCLE)
C      900 T=T-TOLD
C      (RUNTIME)
C      WRITE(6,920) C1,C2,C3,N,T
C      920 FORMAT(//7X,'STOP BY ',3L1,' ' ) RUNTIME FOR',I6,
C      ' CYCLES:',F10.3,' S')
C      CALL EXIT
C      END

```

6. Unstructured. An unstructured version of the Strufo program looks more familiar to Fortran users. But though easier and quicker to write, it is harder to understand and also to modify because a change in one place may cause unexpected trouble elsewhere.

The programming time ratio, which was 10:1 for Strufo/Unstru, thus seemed much lower in the case of this practical project. Of course, the ability to develop any program within a time proportionate to its size decreases as both its size and the number of programmers involved increase. But the larger the program and the greater the number of programmers, the better the payoff from this modular programming method.

With the practical project mentioned, some other bonuses emerged. For instance, the method reduced the time necessary for program test and maintenance. It was also extremely simple to cut the program into several overlays to fit the computer's memory and to save data periodically for restarting a long run. □

References

1. I. Nassi and B. Shneiderman, "Flowchart Techniques for Structured Programming," Association for Computing Machinery SIGPLAN Notices (1973), Vol. 8, No. 8, pp. 12-26.

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High-level language takes on most of real-time system software

Pascal extension can handle operating system functions like peripheral device drivers and data sharing

by Cynthia Fulton and Richard Whiffen, *Enertec Inc., Lansdale, Pa.*

□ Operating systems for microprocessors and minicomputers can be written in a derivative of Pascal that combines the ease of high-level language programming with the efficiency of the assembly language approach. Designed for the purpose, Micro Concurrent Pascal (mCP) responds to the demands of multitasking by adopting a highly structured approach to protecting shared data areas.

Standard high-level languages perform tasks sequentially and provide no facilities for real-time responses to interrupts or even bit-level manipulation. They therefore make it cumbersome to handle the real-time concurrent events of a multitasking operating system. For this job, assembly language has been the traditional choice, despite the difficulty of debugging, maintaining, and modifying programs written in it. But a simpler means of system implementation has become necessary as the growth in the variety of microprocessors has caused a corresponding increase in the variety of assembly languages.

Basically, a mCP program takes over the multitasking and device driver functions of a conventional operating system, leaving just the scheduling functions behind in what is called a kernel. This kernel and a mCP interpreter are written in the assembly language of a given microprocessor. But the mCP programs can be run on any suitably equipped microprocessor.

Concurrent Pascal

Micro Concurrent Pascal is a modification of Concurrent Pascal, which was developed by Per Brinch Hansen on the basis of the ideas of Niklaus Wirth, C. A. R. Hoare, and E. Dijkstra. Concurrent Pascal can handle multiple processes that run independently but share data and communicate with each other. In other words, it is designed for system programming. Yet as a superset of Pascal, it also satisfies the requirements for application programming.

Concurrent Pascal is more modular than its parent, Pascal, and even better suited for top-down structured design. It adopts and enforces that philosophy on the programmer even more heavily than Pascal does—an important asset in the real-time programming world of the operating system, where process scheduling and resource management are critical. Its structured nature also makes it easy to divide a large software project

among a team of programmers. Like Pascal, Concurrent Pascal offers the programmer not just the standard data types (integer, real, character, and boolean) but also user-defined data structures with strong data-type checking by the compiler to prevent programmer errors in this area.

Concurrent Pascal differs from Pascal in making use of processes and monitors. These processes and monitors are system component types—that is, the programmer defines their make-up and format, later creating specific

TABLE 1: HOW MICRO CONCURRENT PASCAL DIFFERS FROM SEQUENTIAL PASCAL

| Constructs added | Description |
|-----------------------|--|
| Processes | the system components that execute code |
| Monitors | shared-data structures plus the routine that processes call to operate on that data |
| Device monitor | variant of a monitor through which processes communicate with peripheral devices; it permits the writing of device drivers directly in mCP |
| Class | a monitor that can be accessed only by a process that is specified at compilation time |
| Delay | a statement used to stop execution of a process until some external event such as an interrupt occurs |
| Continue | a statement used to restart a process stopped by a delay statement |
| Queue | a variable type used with delay and continue statements to determine when a process should execute (similar to a semaphore) |
| DOIO | a statement permissible only in a device monitor that causes execution to wait for an interrupt |
| Initial | a statement that creates instances of system component types (variables, processes, monitors, etc.) |
| Structured constants | memory-saving feature that allows fixed constants to be initialized and used in place of variables or immediate values |
| Constructs deleted | Description |
| Recursion | recursive routines are not allowed |
| Dynamic heap | all memory allocation is done at compilation time; no POINTER data types or NEW procedures are allowed |
| Standard input/output | standard Pascal I/O routines do not appear since users are now expected to be able to write their own custom versions easily |

TABLE 2: DEVICE MONITOR FOR A UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER

| PROGRAM | COMMENTS |
|---|--|
| *UART WRITE* | THIS ROUTINE WRITES A LINE TO A MICROCOMPUTER'S B251 UART. |
| CONST | DEFINE SEVERAL CONSTANTS. |
| LINELENGTH = 72; | LENGTH OF LINE IS 72 CHARACTERS. |
| NUL = '(0)'; | A NUL IS ALL ZEROS. |
| TBE BIT = 2; | TRANSMITTER-BUFFER-EMPTY IS BIT 2. |
| REQ_TO_SEND = #26; | REQUEST-TO-SEND INITIATED BY 26 ₁₆ . |
| WAIT_TO_SEND = #27; | TERMINATE REQ_TO_SEND BY 27 ₁₆ , THEN WAIT. |
| TYPE | DEFINE SYSTEM COMPONENT TYPES. |
| LINE = ARRAY [1..LINELENGTH] OF CHAR; | LINE IS A 1-BY-72 ARRAY OF CHARACTERS. |
| UART_WRITE = DEVICE_MON (CTRL_WORD; | UART_WRITE IS DEVICE MONITOR: CTRL_WORD AND |
| DATA_WORD: ADDRESS; | DATA_WORD ARE ADDRESS OF UART'S CONTROL AND |
| SELECTOR: INTEGER); | DATA REGISTER; SELECTOR IS INTERRUPT NUMBER. |
| PROCEDURE ENTRY WRITE (MESSAGE: LINE); | WRITE A MESSAGE OF TYPE LINE TO UART. |
| VAR I: INTEGER; | DECLARE COUNTER VARIABLE I. |
| BEGIN | ENTER BLOCK THAT TRANSMITS A LINE. |
| REPEAT UNTIL (INN (CTRL_WORD) AND TBE_BIT) (<) 0; | TEST UNTIL TRANSMITTER BUFFER IS EMPTY. |
| OUT (REQ_TO_SEND, CTRL_WORD); | MAKE REQUEST-TO-SEND ACTIVE. |
| OUT (WAIT_TO_SEND, CTRL_WORD); | THEN DE-ACTIVATE |
| DOIO; | AND WAIT FOR CLEAR-TO-SEND INTERRUPT. |
| I := 1; | SET CHARACTER COUNTER TO FIRST CHARACTER. |
| WHILE (MESSAGE [I] (<) NUL) AND (I (<= LINELENGTH) DO | CHECK FOR NUL OR COUNTER > 72 |
| BEGIN | AND SEND MESSAGE. |
| OUT (ORD (MESSAGE [I]), DATA_WORD); | TRANSMIT I TH CHARACTER. |
| DOIO; | WAIT FOR CLEAR-TO-SEND INTERRUPT. |
| INC (I); | THEN INCREMENT CHARACTER COUNTER. |
| END; | CONTINUE SENDING MESSAGE. |
| END; | EXIT WRITE PROCEDURE. |

instances or variables of these component types.

Processes are application programs written to communicate through monitors instead of a conventional operating system. They represent system activities, and several of them may run simultaneously and are continually operative. For example, a typical Concurrent Pascal program would contain a process for the real-time clock, an operator process representing possible operator actions, and other processes as needed to represent various other system tasks (see "The basics of Micro Concurrent Pascal," p. 159).

Role of the monitors

A monitor is the only means through which the processes can communicate with each other. It is an area of shared data and a group of procedures and functions that can operate on that shared data. Different processes gain access to data in a monitor by calling a procedure or function resident in it and thereby operate on and share its data. For instance, the process for a time-of-day clock might call a procedure in a monitor to write the time into that monitor, making it available for access by another process—for example, one that prints the time of day on a user's program listing.

Data protection is enforced by the language itself. Only one process at a time may be executing code within a monitor—the kernel code implementing the procedure call ensures that. If a process calls a procedure in an

active monitor in which another process is executing code, that process is blocked until the current one exits or delays. Delay and continue statements, permissible only within monitors, enable processes to be blocked and resumed, respectively. They serve much the same purpose as the traditional semaphores—flags that are set before entering a routine to signal that it will be in use.

Monitors further support structured design by isolating data formats. Since the logical organization of a shared data structure is known only to its monitor, only procedures within that monitor need be modified to operate on updated data formats. If interfaces to external processes are preserved, then no code outside of the monitor is affected by changes in the data representation within it. In other words, Concurrent Pascal correctly assumes that it is safer to communicate via calls to monitors than via shared data structures, which would require all routines that use that data to be changed so as to recognize updated versions.

Micro Concurrent Pascal

In concept and general implementation, Concurrent Pascal is an excellent language for the dedicated real-time application programming that can take over many of the functions of the operating system. But it does have limitations. It requires that all processes be declared at compilation time, and it is therefore not a suitable language for timesharing operating systems, in which the

The basics of Micro Concurrent Pascal

The high-level language called Micro Concurrent Pascal has been designed to handle system as well as application software. It takes over two key functions of the operating system of a microprocessor-based system—its data-sharing and device-driver capabilities. To implement them, mCP employs software modules called monitors. The mCP application programs, or processes, used to read and write devices like a time-of-day clock and a user's terminal, communicate with one another only through a shared-data monitor and with their associated hardware through the device monitors. Shorn of all but its scheduling functions, the operating system is called a kernel. The kernel is written in assembly language and is accompanied by an interpreter.

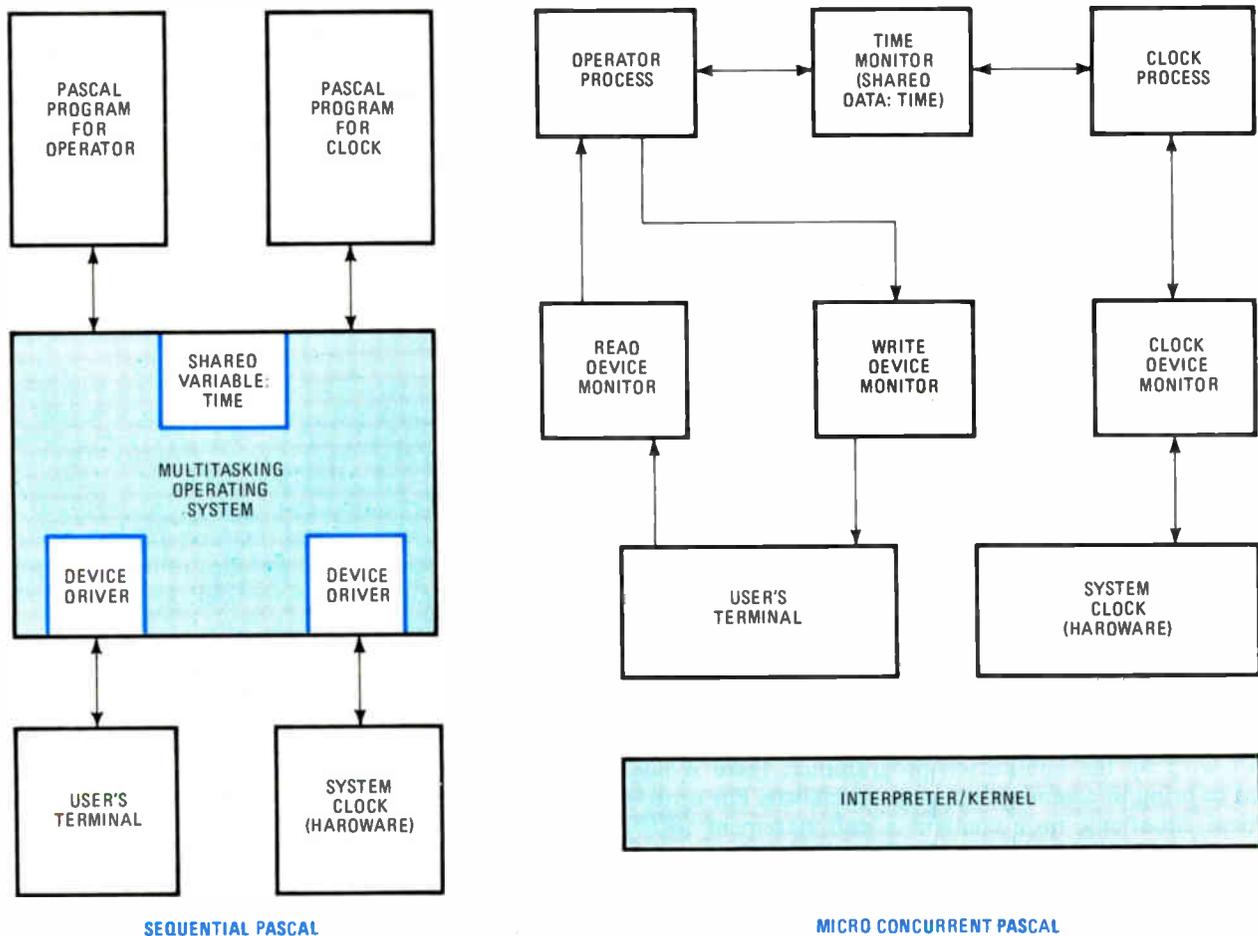
The two diagrams refer to a simple microprocessor-based system that allows a time-of-day clock to be set and read from a user's terminal. The first illustrates the conventional distribution of software functions between an assembly language operating system and application programs written in Pascal. The second shows the redistribu-

tion of functions made by the Micro Concurrent Pascal approach.

A possible sequence of events in the mCP system might be as follows. The clock interrupts the microprocessor (not shown), alerting the kernel, which promptly transfers system control to the clock process. This process first uses the clock device monitor to find out the time and then puts the information in the shared-data time monitor. In performing these two tasks, the process uses the interpreter to turn its compiled mCP statements into executable machine code.

The clock data might in this way be routinely updated by the system every second. Meanwhile, the operator of the terminal may at some point ask for the time. As before, the kernel deduces that the microprocessor has been interrupted by the terminal and transfers system control to the terminal process. That process collects the current time from the shared-data time monitor and passes it on to the terminal via the terminal device monitor for display to the user.

-R. Colin Johnson



number of operator processes varies. mCP at present also has this limitation, though a version that allows processes to be created and destroyed dynamically is under development.

The mCP language is derived from Concurrent Pascal, but specifically tailored for mini- and micro-computer

use (Table 1). The most important extension (and one of the primary goals) of mCP was to adapt the language for writing device drivers—routines designed to communicate with peripherals. Thus the task of writing device drivers and other system-level software need no longer be viewed with foreboding because the mCP language

Pulse-width meter displays values digitally

by Paul Galuzzi
Beverly, Mass.

Built only with standard logic elements and solid-state displays, this meter provides digital readout of pulse width, a widely sought-after feature in instruments of this type. Measurement accuracy is one part in 10,000.

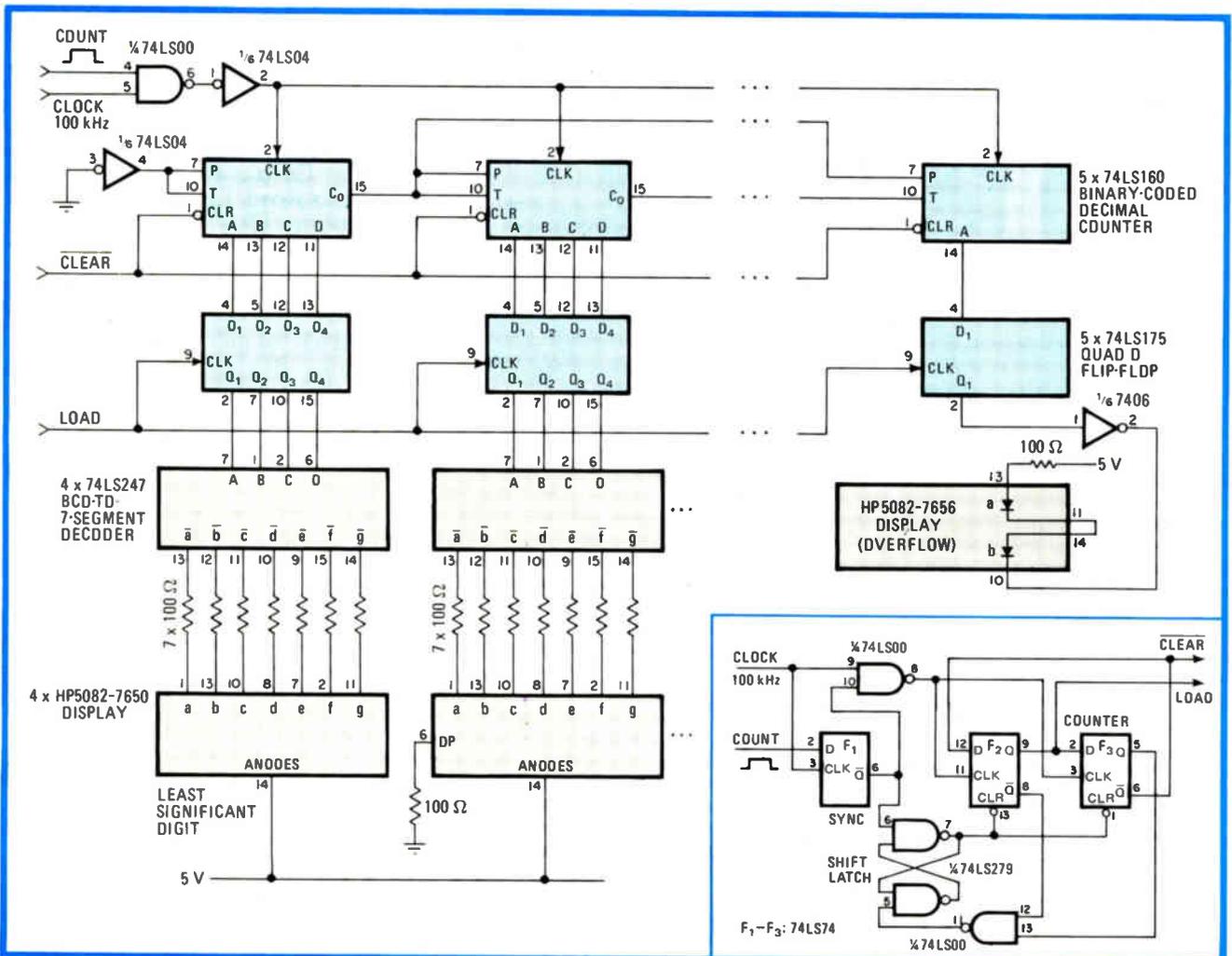
As the figure shows, this circuit is relatively straightforward, being made from several cascaded binary-coded decimal counters, flip-flops, BCD-to-seven-segment decoders, and the corresponding displays. In operation, the pulse (count) to be measured gates the 100-kilohertz system clock, which steps the 74LS160 counter bank.

transfers the BCD data to the 74LS175 flip-flops that serve as a storage register.

At this time, the BCD data, whose value is directly proportional to the width of the count pulse, is decoded by the 74LS247 chips and the corresponding displays. A clear pulse then resets the counter bank, and the measurement cycle repeats.

The circuitry for generating the clear and load pulses is shown in the right-hand inset. As shown, sync flip-flop F_1 is enabled by the inverted count signal, thereby gating the 100-kHz system clock so that flip-flops F_2 and F_3 can shift through a two-stage cycle. Thus, the load and clear pulses are generated in sequence after the falling edge of the pulse whose width must be measured.

With the 100-kHz clock, the meter will display 100.00, its full-scale reading, for a pulse width of 100 milliseconds. Pulses as small as 10 μ s in width can be measured accurately with the given clock rate, and more narrow pulses can be detected if the clock frequency is made proportionally higher. □



Count time. Digital meter measures pulse width by counting number of 100-kHz system clock cycles during time that pulse is present. Solid-state displays provide direct readout of time in milliseconds. Measurement accuracy is 1 part in 10^4 over range of 10 μ s to 100 ms.

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For demonstration circle 162
For additional information circle 163

MODEL 5801 520MHz Bench/Portable Frequency Counter...\$495.

Operating from optional rechargeable NiCd or C cell batteries, as well as AC line, this unit will meet most of your measurement requirements in the subaudio to UHF spectrum. The 5801 features direct reading in MHz for fast, error-free measurement over the frequency range of 10Hz to 520MHz, input sensitivity of 10mV (min), easy-to-read 0.43" 8-digit LED display, and external clock input capability at either 1 or 10MHz. Optional precision TCXO.

MODEL 5800...\$449.

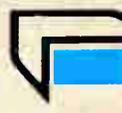
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Engineer's newsletter

Slide rule handles communications calculations

Knowing a good thing when they see one, communications system designers grabbed up the Antenna/Communications Systems Calculator distributed by Scientific Atlanta Inc. at its 1980 Earth Station Symposium, held in Atlanta last month. The handy slide rule takes care of calculations of antenna beam width and gain, free-space attenuation and gain reduction, antenna torque and wind pressure, noise input and temperature, power, return loss, and voltage standing-wave ratio in but one pull of its plastic slide. It's **useful for antenna and receiver specialists, as well as for those folks who simply want to do a first pass at an electrical design budget for a communications system.** Write to the company at 3845 Pleasantdale Rd., Atlanta, Ga. 30340 for more information.

IEC issues more standards for pc boards

Printed-circuit boards are used by every manufacturer of electronic equipment. To facilitate agreement on how these boards should be built, especially those meant for international trade, three more international specifications have been issued by the International Electrotechnical Commission. These standards contain fundamental information on characteristics to be assessed and construction requirements for three types of board: single- and double-sided with plain holes, single- and double-sided with plated through-holes, and multilayer. The specifications form parts 4, 5, and 6 of the IEC Publication 326 series. As with the previously published parts, which cover other types of pc boards, each provides **information for the designer, recommendations for the specification writer, and test methods** for the particular type to which it refers.

Further information is available from the Information Officer, Central Office of the IEC, 1 rue de Varembé, 1211 Geneva 20, Switzerland.

Government offers help for technical information retrieval

No one has yet come up with a foolproof system for completely solving the working engineer's problems of technical information retrieval, and it may well be that the latest attempt by the National Bureau of Standards won't do the whole job either, but it's worth a try. A report on what the NBS calls an **"easy-to-use computerized system for indexing, classifying, retrieving, and editing citations of research papers"** can be had by sending \$4.25 for "A Computer Data Base System for Indexing Research Papers" (Order No. 003-003-02245-4) to the Superintendent of Documents, U. S. Government Printing Office, Washington, D. C. 20402. The data-base system is written in level one Fortran 4 and requires a terminal in your office or lab. The NBS claims that since "all copies of research papers are used as a general data base," the user can "reduce the administrative and clerical work involved" in information retrieval.

Dictionary pins down fiber-optic terms

Data-communications and telephony engineers active in the burgeoning field of fiber optics have needed a comprehensive dictionary, since there is often much confusion about just what the new terms mean. Until now, this need has been met by glossaries at the back of technical books or by short dictionaries, but the "Fiber Optics and Lightwave Communications Standard Dictionary" should provide the last word for the foreseeable future in its 304 pages of cross-referenced material. One special feature: **not only is the written language covered, but the spoken word of the designer is also taken into account.** The Van Nostrand Reinhold book by Martin H. Weik costs \$18.50.

-Harvey J. Hindin

Why you should talk to us the next time you need an electromechanical relay.

You'll find us easy to deal with.

We're big enough to supply a broad selection of general-purpose, power and miniature relays. But small enough to be really responsive to your technical questions. Or to your request for delivery information.

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Price and delivery that's more than competitive. Chances are, we can deliver relays quicker than you might imagine. We often let you slice a week or two off the best delivery you can find elsewhere.

You'll also find us competitive when it comes to price.

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Miniature high-current relays. Large switching capacity in a small package. With a typical UL-rating of 10 amps at 240 volts ac, these relays are ideal for motor controllers and similar high-power applications.

Available in SPDT to 4PDT configurations with 10 to 20-amp contacts. Terminal options include PC, solder, quick-connect or octal base.



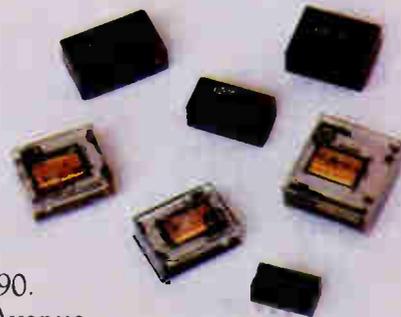
General-purpose relays. One will fit your needs exactly. For many applications, you'll find one of our general-purpose relays will precisely fill your requirements. You have a wide choice of contact types, coil voltages and sensitivities, and terminations.

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The VERSAmodule Monoboard Microcomputer flagships the VERSAmodule family. Combining an MC68000 MPU, full VERSAbus interface, multiprocessor capability, substantial ROM/RAM, serial and parallel I/O and timer/counter functions, it's easily the most powerful single-board microcomputer yet offered. For designs requiring up to

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to a total, 16-bit system VERSAmodule.™



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Inherent Reliability/ Maintainability.

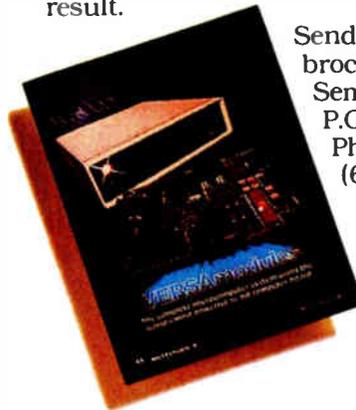
VERSAmodule products support an unmatched level of system integrity. This includes reliability of the MC68000 with its advanced architectural features such as exception-processing and interrupt handling. These allow for graceful handling of common system problems such as bus error, illegal instruction, divide-by-zero, privilege violation, spurious interrupt, etc. This "soft-failure" capability alerts operating personnel and, in many cases, allows recovery before critical failure.

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What's more, these savings are all yours without sacrificing reliability. That's because Flexlok connectors feature Burndy's patented GTH™ contact design that delivers gas-tight, high-pressure, good-as-gold contact even under adverse environment. Hard to believe? The proof is in the cost comparisons and performance data shown below.



*Flat-flat and flat-round types.

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Here's proof!

FLEXLOK COST COMPARISON

| | GTH Flexlok FC & RC | Clamp Type Pressure Tin | Insulation Displacement | Insulation Piercing | Solder Connections |
|--|---------------------|-------------------------|-------------------------|---------------------|--------------------|
| Piece Price* (per line) | 1¢ † | 2¢-3¢ | 3¢-5¢ | 5¢-10¢ | 5¢-10¢ |
| Special Conductor Preparation | None | Required | None | None | Required |
| Installation Tooling (Purchase/Rental) | None | Yes | Yes | Yes | Yes |
| Operator Training Required | None | None | Skilled | Skilled | Skilled |

*In Quantity

†Average price

FLEXLOK PERFORMANCE DATA

| Contact Resistance Test Data | | MIN. | MAX. | Avg. |
|------------------------------|--|--------|-------|-------|
| Test Group 1 | Initial Contact resistance | 7.00 | 7.60 | 7.25 |
| | After thermal shock | 7.10 | 7.50 | 7.25 |
| | After durability (5 cycles) | 7.10 | 7.80 | 7.39 |
| | After moisture resistance (10 days) | 7.20 | 8.70 | 7.68 |
| | After vibration | PASSED | | |
| | After mechanical shock | 8.20 | 25.20 | 12.30 |
| | Insulation resistance (megohms X 10 ⁶) | .002 | 9.50 | 5.26 |
| Test Group 2 | Dielectric withstanding voltage No breakdown @ 500V AC | PASSED | | |
| | Initial contact resistance | 7.00 | 7.50 | 7.25 |
| | After thermal shock | 7.20 | 7.90 | 7.46 |
| Grp. 3 | Ammonium Sulfide exposure (3 min.) | 7.20 | 8.00 | 7.59 |
| | Initial contact resistance | 7.10 | 7.50 | 7.25 |
| | After gas tightness | 7.00 | 7.60 | 7.24 |

Report No. G7515-755 (Summary) Mated with tin/lead plated flexible printed circuitry.

FLEXLOK DESIGN FEATURE COMPARISON

| Design Simplicity | 1 piece | 2 pieces or more |
|------------------------------|-----------------------|------------------|------------------|------------------|----------------------|
| Conductor Types Accommodated | Round Flat Flex. P.C. | Flat Flex. P.C. | Round | Round Flat | Round Flat Flex P.C. |
| Top or Side Entry Available | Yes | No | No | No | No |

For details, call or write: Burndy Corporation, Norwalk, Connecticut 06856 (203-838-4444).

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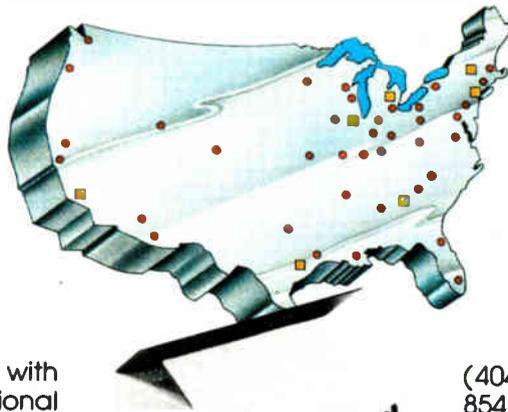
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Chip controls floppy-disk drives

Dedicated microcomputer has memory-mapped interface, needs very few additional parts to control four IBM-compatible drives

by R. Colin Johnson, *Microsystems & Software Editor*

Floppy-disk controllers are moving from board-level implementations toward monolithic devices that conform to the standard IBM formats. The TMS 9909 is an instance: it requires very few additional components to achieve compatibility with the IBM formats for single- and double-density drives.

The single-chip unit controls up to four drives of one or two configurations, which are defined by whether the disks are single- or double-sided, hard- or soft-sectored, and 5¼ or 8 in. in diameter. It is capable of handling all three popular encoding formats—fm, modified fm (mfm), and modified mfm (m²fm)—and it uses a

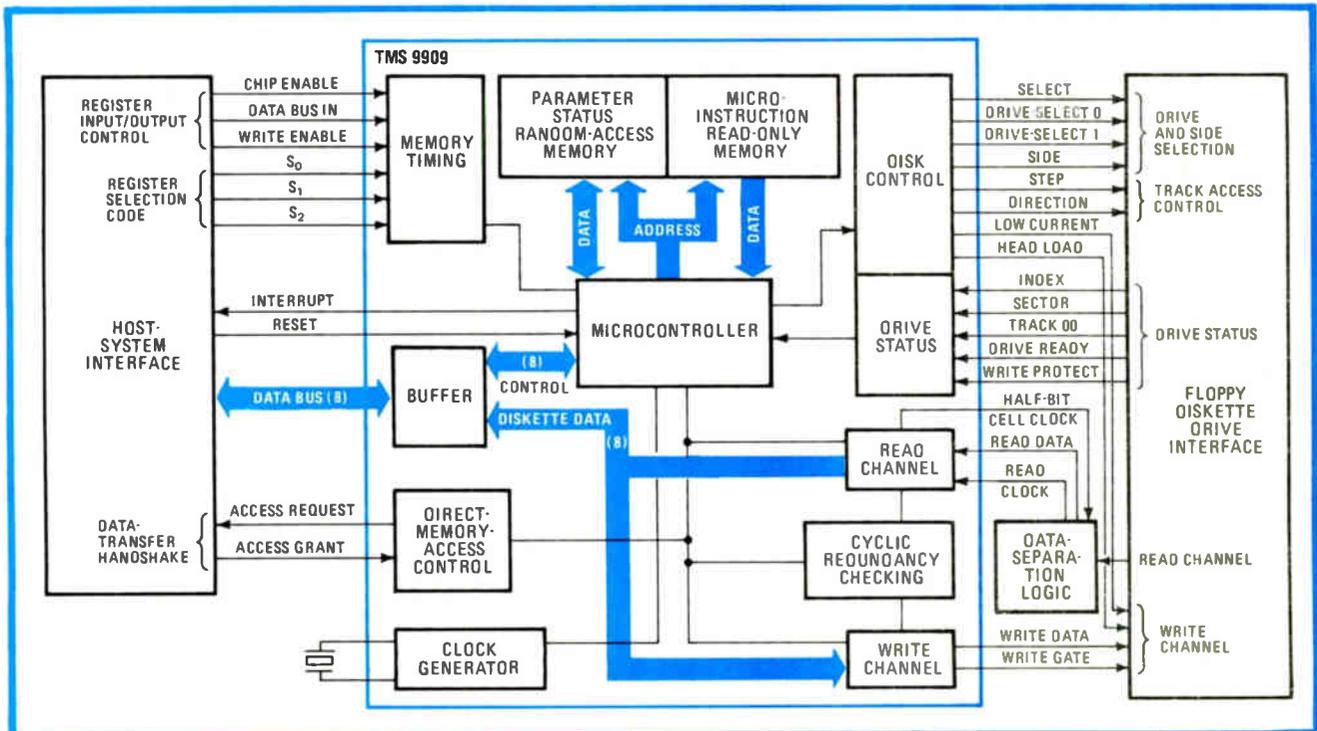
memory-mapped host interface that is compatible with all the popular microprocessors.

Actually a microcomputer dedicated to floppy-disk control, the 9909 responds to commands from the host processor, performing the specified task without further intervention. It accomplishes these tasks under the supervision of a microcontroller read-only memory that defines the steps taken to execute each command and to load the status register. Upon completion of the task, the 9909 can signal the host with an interrupt; in polled situations, the status register is used to flag the host upon completion.

The drive controller can be instructed to: step to any track, format a track, read data, write data, send status to the host, and abort the previous command. The current command is also aborted whenever a system reset is initiated.

Procedure. The host ordinarily reads the status of the 9909 to determine whether it is busy and then writes the desired command, followed by whatever parameters are appropriate. When the last parameter is received, the controller begins execution of the command, using direct memory access for reading and writing operations.

The status register tells the host



Diskette chip. The TMS 9909 dedicated microcomputer controls up to four floppy-disk drives of two configurations, performing tasks requested by the host system without intervention and signaling the host when finished. Reading and writing use direct memory access.

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whether or not the 9909 is busy, whether or not the selected drive is ready (its door might have been left open, for instance), whether that drive's head is positioned over track 0, whether the last operation involved data under- or over-flow, and whether or not the desired sector-identification marker was found. Data-transfer rates are programmable from 125 to 500 kb/s.

Other programmable features include the step, settle, and head-load times; these are variable over a range of 0 to 255 ms. Format options include those for gap, synchronization, and identification. Data-field lengths and contents are also completely programmable.

After the host issues a format-a-track command, the 9909 fetches the length and contents of the track from system memory using direct memory access. This allows the use not only of the standard IBM formats but also of custom formats.

Reliability aids. Write precompensation and the low-write-current signal are also programmable features. When selected, 167 ns of precompensation is provided for write operations to any track. The low-write-current pin notifies the drive that a write operation is now commencing on one of the inner tracks (track number greater than 43). In that way, writes to the low-velocity inner tracks can be greatly improved in terms of reliability.

Also enhancing reliability is the automatic generation and validation of cyclic-redundancy-check bits. In write operations, the check bits are written onto the disk and read operations regenerate and compare them with those recovered from the disk. If an error is detected, a flag is set in the status register.

The on-chip clock generator needs only a 6-MHz crystal. The part comes in a 40-pin package and runs on a single 5-v supply.

Samples of the TMS 9909 are available now, and production quantities are to become available during the first quarter of 1981. The price is \$34.50 each in lots of 100 or more.

Texas Instruments Inc., P. O. Box 225012, MS 308, Dallas, Texas 75265 [338]

Circle 176 on reader service card

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Yes, Data General, we saw your ad.

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But Cromemco produces state-of-the-art MICROcomputers.

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And our micros have some outstanding advantages.

For example, Cromemco is the only microcomputer manufacturer to support a broad range of microcomputers with (a) 5-inch

double-sided, double-density floppy disk drives and with (b) 8-inch double-sided, double-density floppy disk drives AS WELL AS (c) 8-inch Winchester hard disk drives.

That means, of course, that our customers have a wide choice of disk storage capability.

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- CROMIX (a UNIX-like operating system)
- RPG-II (IBM-compatible)
- COBOL
- BASIC
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- LISP
- C
- Macro Assembler

APPLICATION SOFTWARE

- Word Processing System
- Data-Base Management
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- Accounts Receivable
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All of this is available now with more coming all the time.

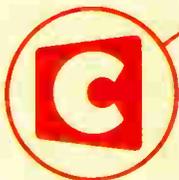
So there you are, D.G.

You can see why we know our microcomputers will stand the test.

Cromemco eagerly accepts the challenge.



Reproduced from the July 31, 1980 issue of *Electronics* magazine.



Cromemco logo on computer board shown in original ad



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Hitachi 6800/68000 Series (available in all popular speed grades: 1, 1.5, and 2 MHz).

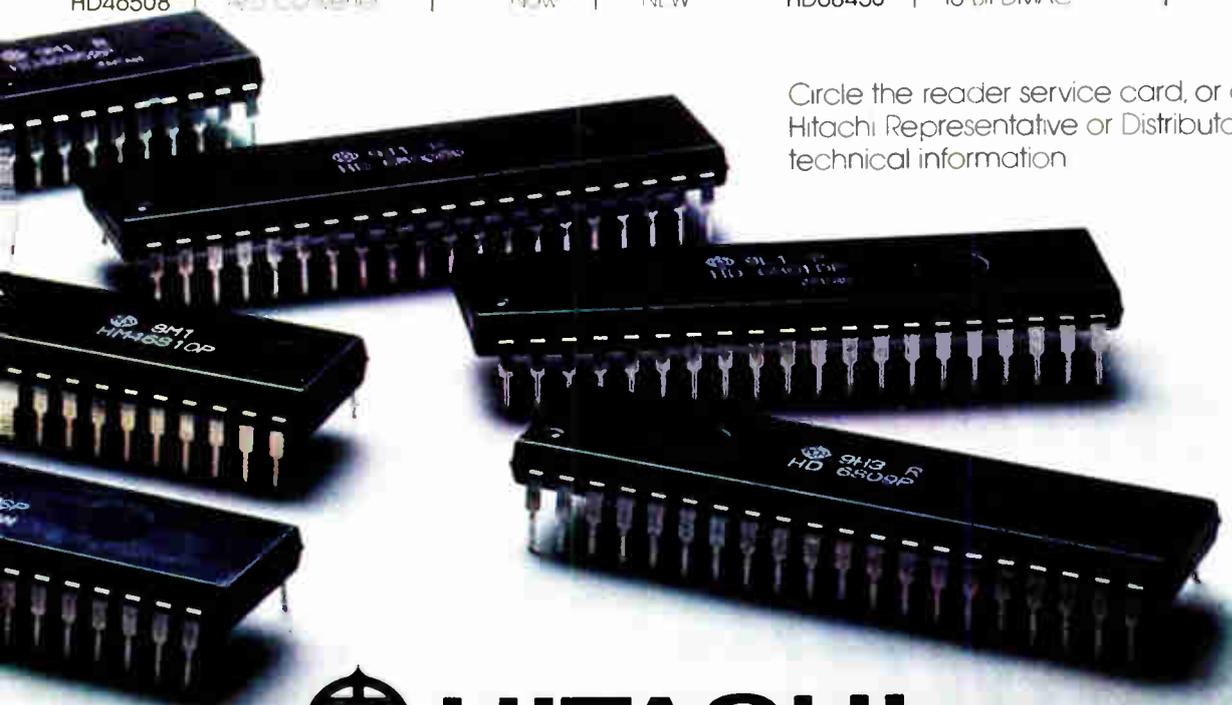
| Part No. | Description | Availability | Replaces |
|-------------------------|---------------|--------------|----------|
| 8-Bit Multi-Chip | | | |
| HD46800 | CPU | Now | 6800 |
| HD46802 | CPU Clock RAM | Now | 6802 |
| HM46810 | 128 x 8 RAM | Now | 6810 |
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|--------------------------|---|--------------|----------|
| 8-Bit Single Chip | | | |
| HD6801 | 1 chip clock 2K byte ROM 128 byte RAM I/O | Now | 6801 |
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|------------------------------------|---------------------------------|-----|------|
| HD6809 | High performance microprocessor | Now | 6809 |

| 16-Bit Multi-Chip | | | |
|--------------------------|-------------|-------------|-------|
| HD68000 | 16-Bit CPU | 4th Quarter | 68000 |
| HD68450 | 16 Bit DMAC | TBA | 68450 |

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CLICK A

Scotchflex® interfaces with a positive

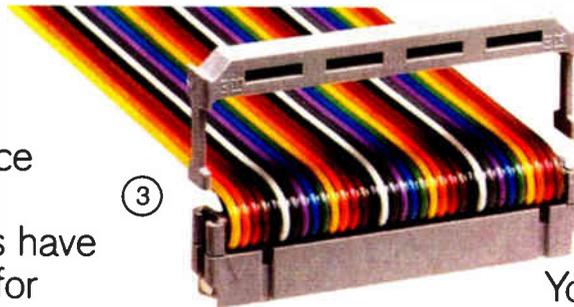
"Click" is the sound of decisive socket-to-header interface in Scotchflex® Brand connectors from 3M, The Source for premium mass termination systems. Sockets and headers have important design features for easier assembly and greater mechanical dependability than ever before.



First, Scotchflex headers (.100" x .100" grid series) now have built-in retainer/ejector latches (1).

② They snap up to lock sockets firmly in place. They snap down to disconnect sockets quickly and easily . . . good news where density makes access tough.

Second, mating socket connectors have designed-in metal spring clips (2) that lock the covers to the bodies for maximum cover retention. The clips double cover retention strength, and let the connector be disassembled and reused if necessary.



Third, one-piece strain relief clips (3) take fewer steps to assemble.

You get higher productivity and lower inventory costs since you need only one type of socket and a supply of efficient, inexpensive clips.

Fourth, connectors snap into polarized headers with an audible "click" without pin loss, for the lowest possible cost per line. The

unique 3M keying system (4)



① provides positive electrical polarization, prevents even a partial mismatch, and helps reduce equipment damage and field maintenance.

AND EASY.

sound for 6-way better assembly.

Fifth, 3M's patented U-contact is ultra-simple. But it's superbly functional, proven reliable in thousands of applications.

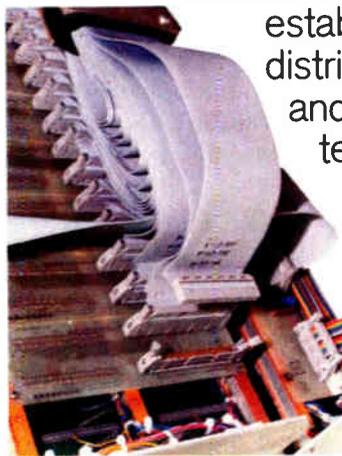
Sixth, Scotchflex Brand sockets and headers in this grid range include 10, 14, 16, 20, 26, 34, 40, 50, and 60-pin sizes. They give you the same dependable mechanical and electrical performance as other 3M components.



Long service life is a prime measurement as well; only Scotchflex products have successfully passed 40-year life-cycle testing. (Test data available on request.)



Click and Easy: words that describe these products' capabilities right down to the pins. Combine with off-the-shelf availability (from our

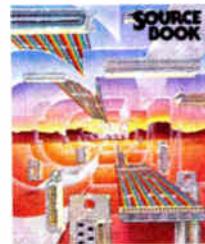


established national distributor network) and superlative technical assistance, and you can see why 3M is The Source for the very best mass termination has to offer the electronic

designer. And there's one more thing.

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All the technical data you'll need for Scotchflex Brand mass termination products is in our complete Scotchflex catalog. It's yours free. Ask your 3M Scotchflex distributor, or write Electronic Products Division/3M, Building 225-4S, 3M Center, St. Paul, MN 55144.



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Computing nodes share peripherals

Interactive ring network gives each user a 32-bit processor and access to shared data, programs, and expensive peripherals

by James Brinton, Boston bureau manager

Apollo Computer Inc.'s Domain system is an evolutionary step forward in data processing, according to John William Poduska, president of the firm. Domain is an acronym for distributed-operating multiple-access interactive network.

Domain [*Electronics*, Nov. 20, p. 34] is said to combine the responsiveness of a dedicated computer with the resource- and data-sharing advantages of a large mainframe timesharing system, but with none of their drawbacks. "Using powerful 32-bit computers connected by an ultrahigh-speed ring network, we not only offer users large amounts of local, ready processing power, but the ability to share peripherals, con-

trollers, programs, and data—and their cost," he says.

Because each node is a complete 32-bit computer dedicated to local use, there is none of the queuing that often accompanies timesharing. Thus, not only does Apollo hope to offer the best features of today's two major data-processing approaches, but it also expects to do so at low cost. "One of our \$24,000 computational nodes has about one third the power of a VAX-11/780," says David L. Nelson, vice president for systems development. "A typical 10-node Domain system, costing between \$300,000 and \$400,000, would have a good deal more throughput than an equivalently

priced VAX system and offer more user convenience in the bargain."

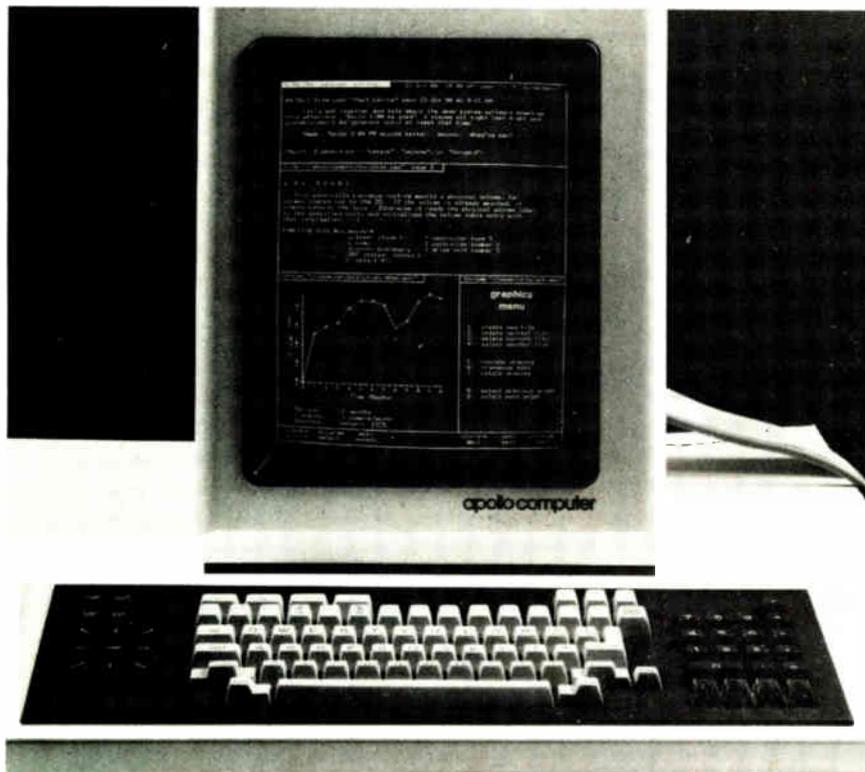
Each node in a Domain system is a multiprogrammed 32-bit computer based on two Motorola MC68000 microprocessors, plus an AMD 9512 floating-point processor. Initial nodes will hold from 256-K bytes to 1 megabyte of MOS main memory based on 16-K random-access memories; when 64-K RAMs become available, nodes could offer up to 4 megabytes of main memory.

Each node also includes a high-resolution cathode-ray-tube console. It has a bit-mapped display of 800 by 1,024 picture elements for graphics and alphanumerics.

The nodes are capable of running a number of programs concurrently and the display screen can be divided into so-called windows. This allows users to operate in several unrelated modes simultaneously. Display management and refreshing are the task of a display microprocessor and a high-speed 1-Mb RAM.

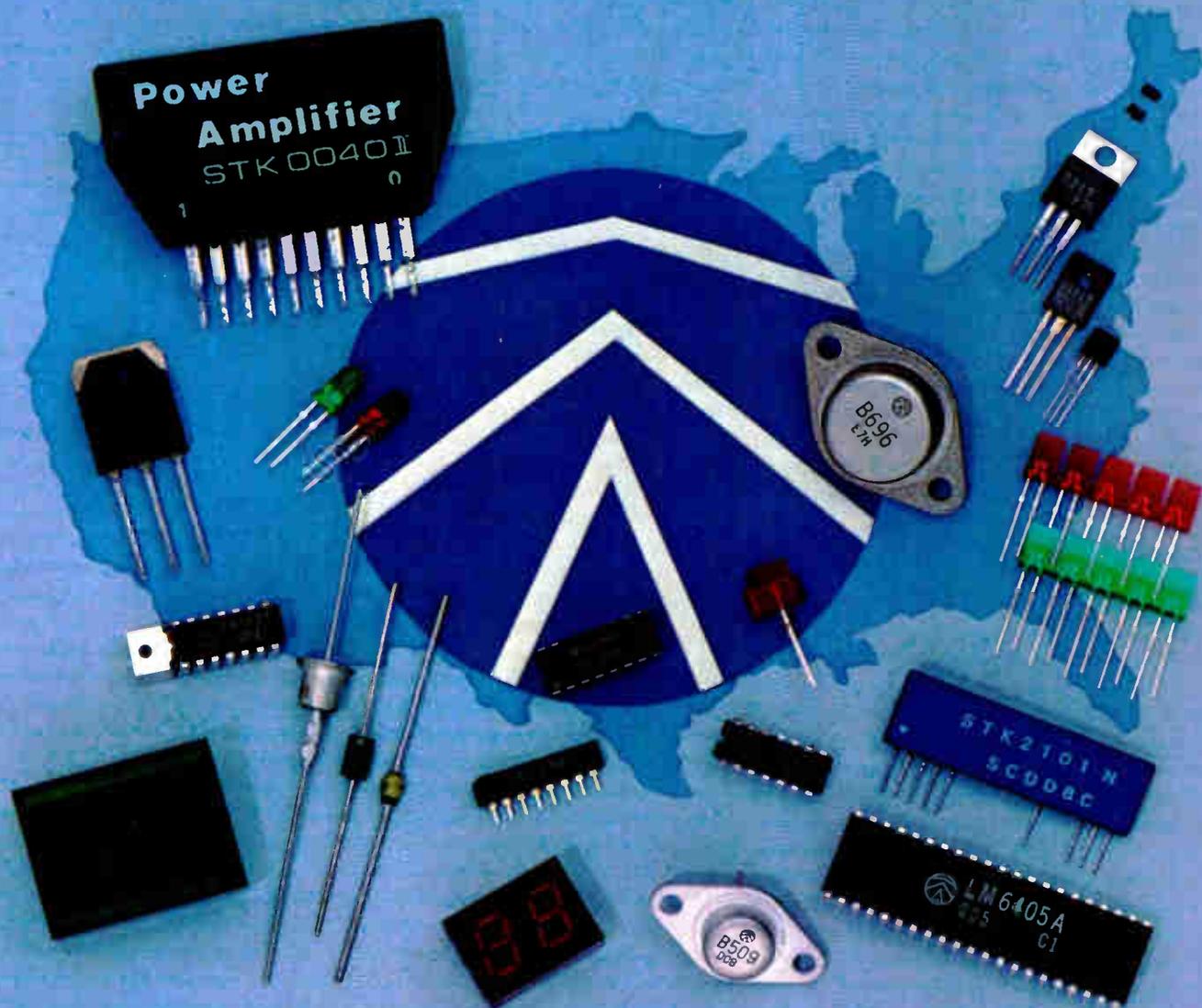
Power. The two 68000s in each node can operate on 32-bit data and clock at 8 MHz. Apollo has developed a custom memory-management subsystem that turns the 68000 into a virtual-memory machine with a 24-bit virtual-address capability. Each node has three serial input/output ports and an interface with the Domain network.

Nelson notes that the nodes are independent of the microprocessor used. Therefore, as more capable units become available, Apollo plans to use them. Retrofit boards may then be offered, eventually increasing virtual addressing to a full 32 bits, and, it is hoped, increasing throughput. Domain software is



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New products

structured to make central processor changes easy.

A minimum node costs \$24,000 with discounts of as much as 25% available on quantity purchases. Another \$10,000 buys an optional 14-in. 33-megabyte Winchester disk drive and a 1-megabyte diskette, both of which fit within a node's 29-in.-high standard cabinet. At least one such bulk-memory package is required in a Domain network.

Users with applications software already in Fortran 77 or Pascal can run their programs directly on a Domain node. A library of software tools—control statements, procedures, standard functions, and so on—might include a simple instruction like SEEK, which would be entered to find a specific file, class, or entry in a data base. With these tools, each acting like a Fortran or Pascal subroutine call, brief programs equivalent to many lines of code in Fortran or Pascal could be written quickly.

Networking. Domain nodes are connected by coaxial cable; the only network architecture available is a ring. Data is sent at 10 Mb/s in packets, including error-detection and -correction codes. Each node receives and retransmits each packet until it reaches its destination. At this point, an acknowledgement is added to the packet and it is sent onward to its originating node, where it is checked for errors.

If a node fails, packets pass through it without interference. Data rates are so fast that polling is not necessary, nor should it be for networks of any size foreseen by Apollo. All the system's resources, except for protected ones, will be available with latency time approximately equivalent to that incurred when accessing a local node's disk file, Nelson says, and this should hold for nets of 100 or more nodes.

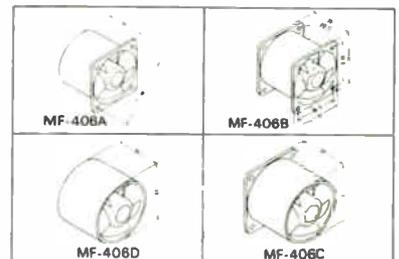
Options include three types of printers, an adapter that converts a standard node into one for control of peripheral equipment, and various software licenses. Deliveries are planned for the first quarter of 1981. Apollo Computer Inc., 5 Executive Park Dr., North Billerica, Mass. 01862 [339]

THE SMALLER AND THE LIGHTER THE FAN, THE MORE THE EQUIPMENT MICROMINIATURIZED:

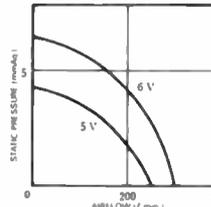


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Rated Speed 6,000rpm
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Weight 50 grams

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Finish Black

APPLICATION

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“How many 31-year-old engineers do you know who have saved \$100,000 in salary?”

A very successful young engineer tells how he accumulated a fat bank roll and took a career shortcut that put him miles ahead of people he graduated with.

At 31 years of age, Mike Erspamer, an electrical engineer with Aramco in Saudi Arabia, has saved \$100,000.

Think of it. Thirty-one years old, six years out of college, lives in a well-furnished townhouse, drives a nice car, no big bills hanging over his head, and a hundred thousand saved.

How on earth has he done it?

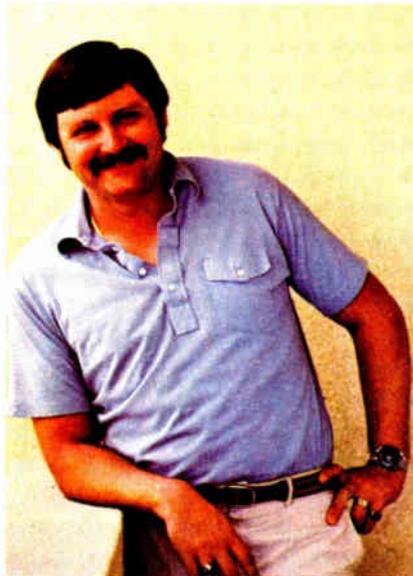
And Mike is not alone. Many of the young Aramco engineers he works with are doing as well.

How Mike saved \$100,000

“Aramco pays me a base salary that’s competitive with what I could expect in the States. But Aramco also pays employees in Saudi Arabia a 40 percent premium on the first \$30,000 of base pay and 20 percent premium on the next \$20,000. That amounts to quite a chunk. And the clincher is this: The whole premium is tax-protected. If I want to, I can save it *all*.”

Mike’s saving will be even more productive now. After 60 months of service he became vested in Aramco’s Savings Plan. Aramco adds 50 percent to the first 6 percent of salary saved. The contribution increases to 100 percent after 10 years of service.

And now new hires make even more. Today, newly hired employees for Aramco in Saudi Arabia receive a lump-sum, fully tax-protected Overseas Employment Bonus of as much as \$5,000. A flying



Mike Erspamer is one of many young engineers working for Aramco in Saudi Arabia who have saved a sizable chunk of money in a very few years; and taken big strides in their careers.

start on an already lucrative compensation plan.

Came for a tryout, decided to stay

“Obviously, Aramco’s compensation package was excellent. Still, I wondered if it was really worth it,” says Erspamer. “I had no idea what Saudi Arabia would be like.

“But there was no contract, no long-term commitment. So my wife and I decided to try it. If the life there wasn’t to our liking, I could always quit and go home.

“We’re still here after six years and planning to stay.”

Today it’s even easier for families to find out if they’ll like Aramco in Saudi Arabia. There’s a one-year tryout plan.

If you don’t want to move your whole family over at once, come and work for us on “bachelor status” for one year. We’ll fly you home three times so you can keep the family informed about your adjustment to life in Saudi Arabia. Then at year’s end or sooner all of you can decide whether the life is for you or not.

It’s a way to get firsthand experience of life in Saudi Arabia without committing the whole family to a move.

“Aramco put me in the spotlight right away”

When Mike Erspamer landed in Saudi Arabia, he got in on the ground floor of a multibillion-dollar gas gathering project. “The scope of the activity and the expenditures were incredible. Aramco immediately gave me more responsibilities than someone my age would be likely to get in the States.”

Aramco has projects that are mind-boggling in size, complexity and cost, ranging from development of the world’s largest onshore and offshore oilfields to construction of a vast electrical power system, and to the building of entire communities.

Aramco is simply too busy to waste young talent and give all the important projects to older hands. If you have skill and commitment,

Aramco has assignments to challenge that skill and commitment.

"I'm only 31, and I'm far ahead of my classmates," Erspamer says. "Maybe not in job title, but certainly in terms of professional growth. And financially, I'm well ahead of the game."

Vacations that most people can only daydream

Are the Erspamers living a Spartan life so they can pinch pennies? Hardly.

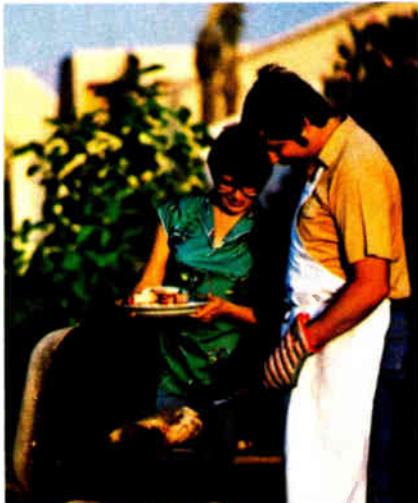
Like all Americans in Saudi Arabia, they get 40 days' paid vacation every 12½ months. Plus about 12 paid holidays.

Vacation trips have taken Mike and his wife, Patti, to 15 different countries during their six years with the company. England, most of Europe, Turkey, Greece, including the fabulous Greek islands, and more.

They even get home to the States often. Aramco pays air fare for annual "repatriation" trips. And from Saudi Arabia, Aramco people travel easily to places they used to think of as "halfway around the world." Their idea of an outing for a long weekend is a trip to Egypt.

It's like a small American town in Saudi Arabia

The Erspamers live in Dhahran, an Aramco community. At first glance



The Erspamers live a comfortable, casual lifestyle. Their well-furnished townhouse is a carbon copy of a house in Arizona, Texas or California.

you could mistake the place for a small town in the U.S. Their townhouse is a carbon copy of a home in Texas or Southern California. On his way to work, Mike drives along

tree-lined streets, past people tending their lawns and gardens (artificial irrigation, of course). A yellow school bus stops and picks up kids at the corner. It's hardly the picture many Americans see when they hear "Arabia."

In their free time, the Erspamers have an active social life with

medical facilities. Our Dhahran hospital is one of only three hospitals outside the U.S. to be accredited by the Joint Commission on Accreditation of Hospitals.

Find out more about the Aramco head start

If you think you might be interested



There's an abundance of recreation for Aramco employees in Saudi Arabia: golf, tennis, water sports, bowling, jogging, camping, riding, and more.

Aramco people from a dozen countries. There's plenty of golf, tennis, riding, every kind of water sport. There's even delayed NFL Football on TV.

First-rate schools and medical facilities

Mike and Patti don't have children. But for those who do, Aramco has an excellent school system in Saudi Arabia. Three-quarters of the teachers hold master's degrees. When our SAT scores were compared with a group of U.S. schools, we ranked with the top 25 percent.

The Aramco schools go through ninth grade. For older children, Aramco pays 80 percent of expenses for boarding schools in Europe or the U.S., up to \$4,900 per student per year.

If somebody gets sick while in Saudi Arabia, the individual is covered by Aramco for *all* medical expenses, even prescriptions, which are incurred while in Aramco

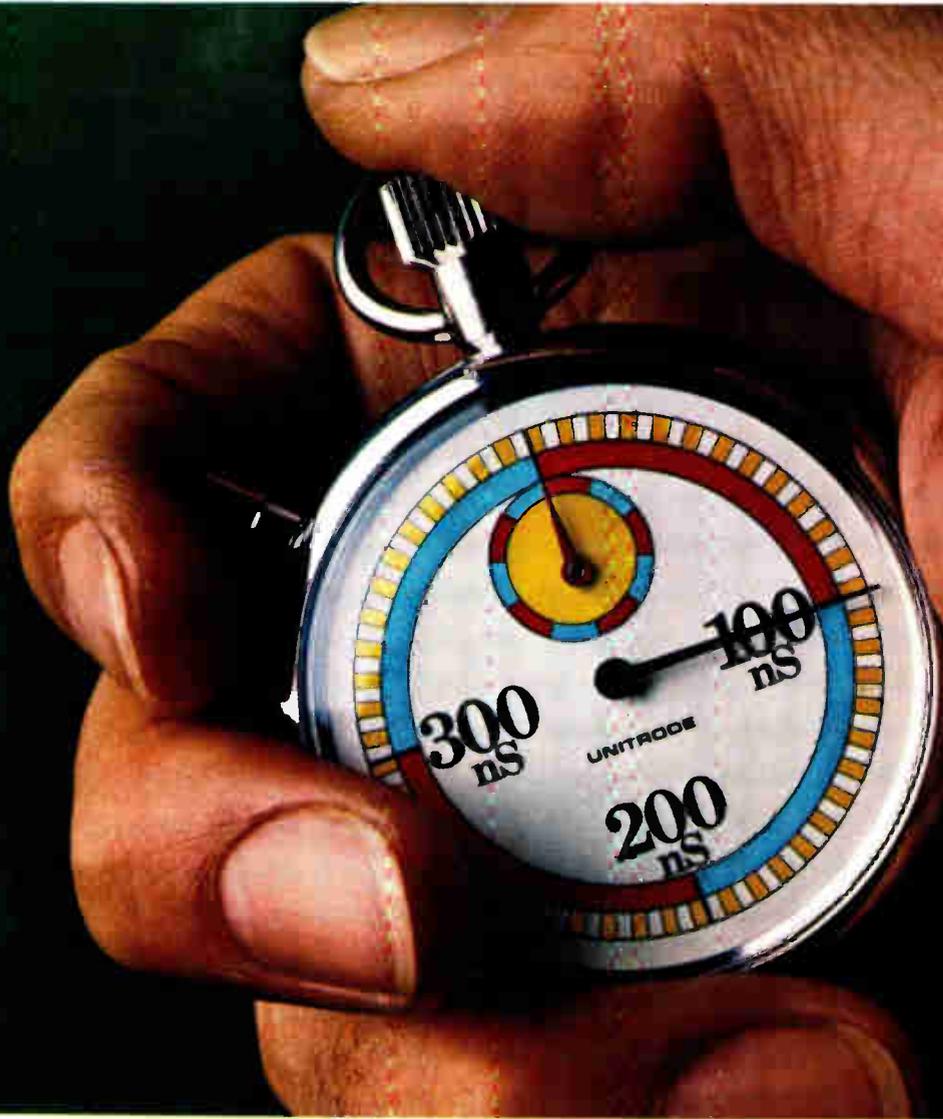
in following Mike Erspamer's example, give us a call. It's confidential and there's no commitment. We have openings for engineers in just about every discipline. Call (713) 654-3264 any time. Or call toll-free, (800) 231-7577, Ext. 3264, Monday through Friday between 7 AM and 5 PM Central Time.

If you prefer, send your résumé or write for more information to: Aramco Services Company, Department ELT120480MCLA, 1100 Milam Building, Houston, Texas 77002.

Watch this publication for stories about other engineers who have taken a career shortcut with Aramco in Saudi Arabia.

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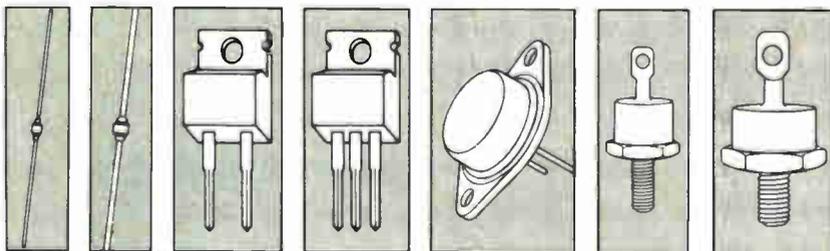
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A-d unit survives 200 hours at 200°C

12-bit hybrid converter for high-temperature duty is backed by year of field tests

The demand for electronic components and subsystems that work at temperatures of 200°C and higher is accelerating in such applications as oil-well drilling, jet-engine testing, nuclear instrumentation, and industrial process control. Although some manufacturers have been quick to proclaim the development of such components, they have not necessarily been extensively field-tested. One company that has been testing a high-temperature subsystem component in the field over the last year and is now ready to make it commercially available is Micro Networks Co., Worcester, Mass. The firm has a 12-bit analog-to-digital hybrid converter that is rated to operate from -55 up to 200°C.

Originally developed for use by the oil industry in down-hole instrumentation systems, the MN5700 is screened and burned-in at a temperature of 200°C to ensure its rated lifetime of more than 200 hours at that temperature. It is also rated for 500 hours at an ambient operating temperature of 175°C.

The thin-film hybrid product has guaranteed absolute accuracy to within ±1% of full-scale range without the use of external trimming potentiometers. Linearity error is a

maximum of ±0.05% of full-scale range at 200°C. The converter has a 250-μs conversion time (350 μs maximum) and includes four user-selectable input ranges of 0 to -10, 0 to -20, ±5, and ±10 v.

The converter includes a built-in reference, a low-power complementary MOS switching network, a proprietary discrete comparator, and a thin-film nichrome resistor ladder network. To handle the high operating temperatures, a proprietary three-metal interconnection system was developed.

The MN5700's output is compatible with low-power TTL and complementary-MOS. The converter dissipates a maximum of 455 mw (typically 311 mw) while operating from ±15- and 5-v supplies.

Available in a hermetically sealed 32-pin ceramic package with dual-in-line spacing of 0.600 in., the MN5700 is guaranteed to be monotonic for 10 bits over the entire operating temperature range of -55 to +200°C. Differential linearity error is ±½ least significant bit (±0.05% of full-scale range). Zero error is ±0.3% over the range from -55 to +200°C (±0.5% maximum).

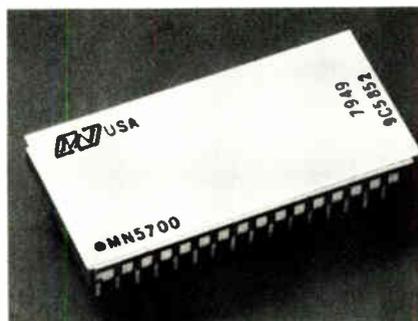
The MN5700 is priced at \$595 in unit quantities and is available from stock to four weeks.

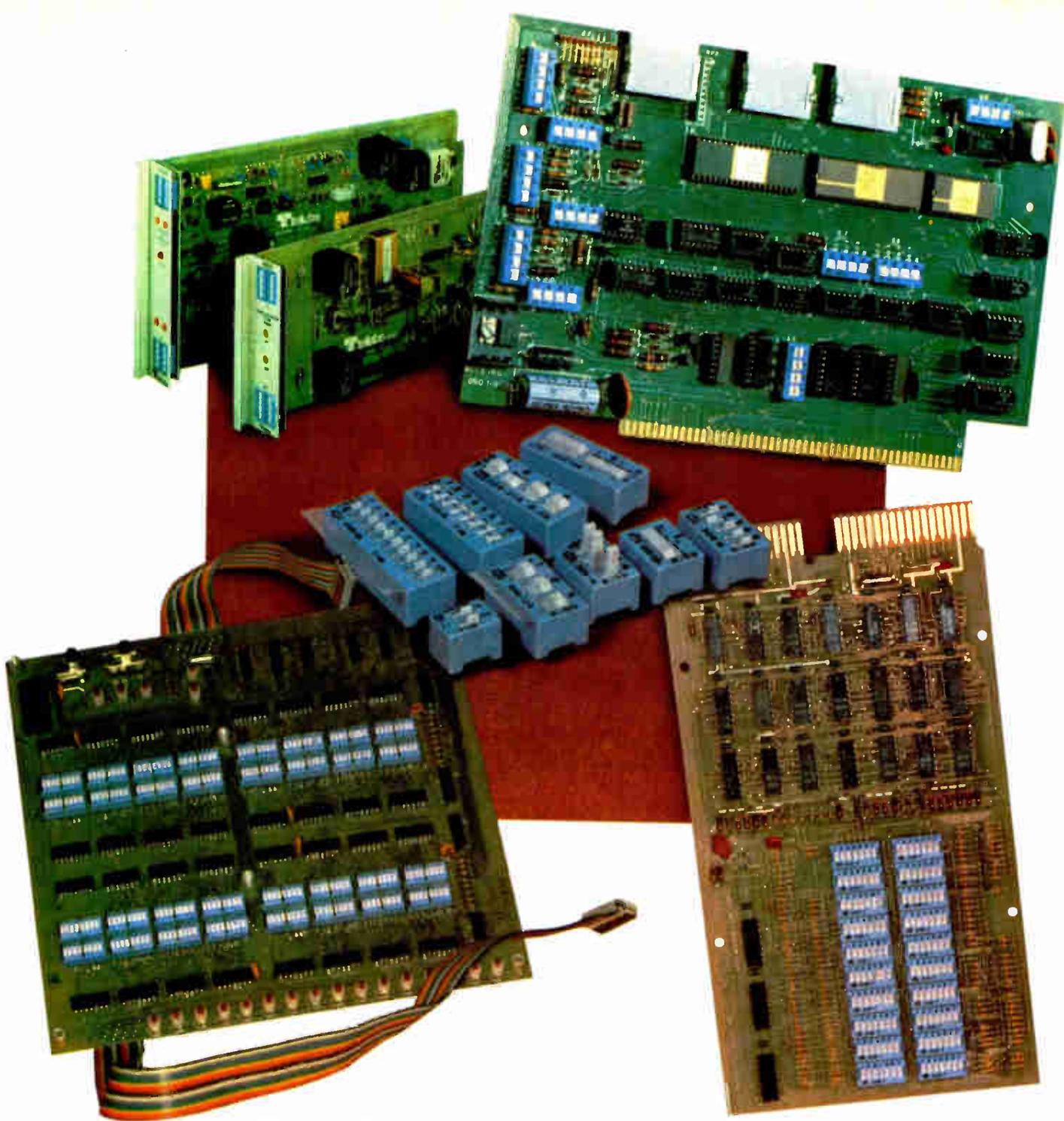
Micro Networks Co., 324 Clark St., Worcester, Mass. 01606. Phone (617) 852-5400 [381]

12-bit a-d has ±½ LSB over full temperature range

Instead of having an accuracy that is guaranteed only at a single specified temperature, the H15712A 12-bit analog-to-digital converter is guaranteed to have ±½ least significant bit of maximum and differential nonlinearity over both its commercial (0° to +75°C) and military (-55° to +125°C) temperature ranges. The converter offers a 10-μs maximum conversion time and a gain temperature coefficient of 15 ppm/°C.

The device can be software-programmed to operate as a 10-, 8-, or





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New products

6-bit converter with a corresponding reduction in conversion time. It will accept either unipolar or bipolar inputs and is compatible with diode-transistor, transistor-resistor, and complementary-MOS logic. The converter offers both serial and three-state parallel outputs and can furnish either binary or 2's complement binary output codes. Prices for the HI-5712A in lots of 100 are \$200 each for the commercial version, \$340 for the military, and \$408 for units meeting MIL STD 883.

A lower-priced version of the device is available for less critical applications. The model HI-5712 is identical to the -A, except that its gain temperature coefficient is 25 ppm/°C, and its guaranteed nonlinearity and differential nonlinearity are $\pm 1/2$ LSB only at 25°C. Prices for this model in 100-unit lots are \$99.50 each for commercial units, \$210 each for the military temperature range versions, and \$252 for the MIL STD 883 grades. Production deliveries start this month.

Harris Semiconductor Products Division, P. O. Box 883, Melbourne, Fla. 32901 [383]

12-bit d-a converter interfaces with microcomputer

The HS3120 monolithic 12-bit multiplying digital-to-analog converter interfaces with either a 4-, 8-, or 16-bit microprocessor's data and address buses. The device has two-stage internal input registers and 12 data inputs organized as three independently addressable 4-bit input registers for added flexibility. The complementary-MOS circuit has a resistor-ladder network that gives it linearity within $\pm 0.01\%$ without laser trimming. Monotonicity is



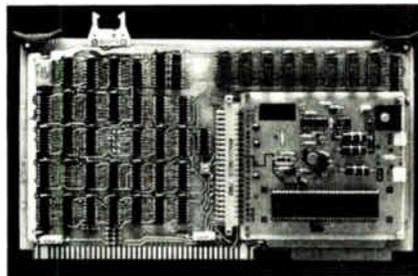
guaranteed over the entire operating temperature range. Commercial versions of the chip will operate from 0° to 70°C and military versions from -55° to +125°C. Prices for orders of 25 pieces or more range from \$23 to \$65. Delivery is from stock but may take up to four weeks.

Hybrid Systems Corp., Crosby Drive, Bedford Research Park, Bedford, Mass. 01730. Phone (617) 275-1570 [384]

20-MHz transient recorder is Multibus-compatible

A single-board digital transient recorder, the model SBDTR-820 is iSBC-multibus-compatible. The unit contains an 8-bit, 20-MHz analog-to-digital converter, 4-K bytes of high-speed memory, and digital control logic. Under software control, it triggers an external device and digitizes and stores in memory 4,096 points from an analog input.

Binary submultiples of the 20-

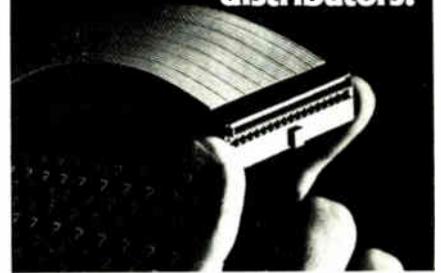


MHz rate can be selected by software up to a maximum divisor of 2⁷, thus achieving the following digitization rates: 20, 10, 5, 2.5, 1.25, 0.625, 0.312, or 0.156 MHz. Rates below 0.156 MHz can be obtained by changing the a-d clock oscillator to operate below 20 MHz.

The board's price is \$2,790. Four other products to be announced in the next few months include a Multi-bus-compatible high-speed multiply-and-accumulate board, a portable high-speed signal processor, a portable transient data-acquisition instrument, and a multi-axis stepping motor and servo-controller.

Adaptronics Inc., 1750 Old Meadow Rd., McLean, Va. 22102. Phone (703) 893-5450 [386]

ADVANCE TIP: the Quickie™ II connectors on the next two pages are available from these Berg Electronics distributors:



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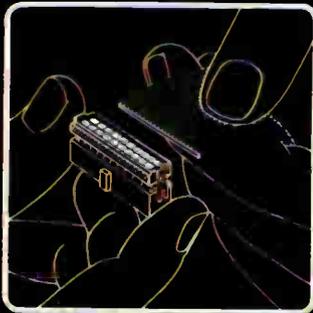
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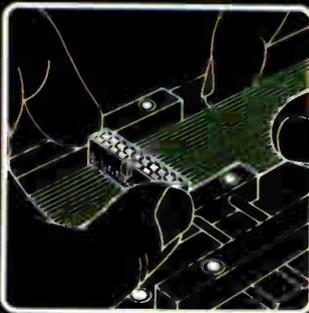
Berg Electronics



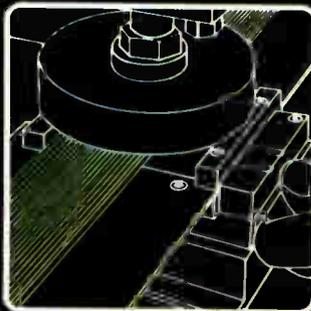
If mass termination 7 seconds...switch



Insert cable.



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The Berg "Quickie" connector was well named. But it soon had many imitators. Now meet "Quickie" II, the new connector that makes the others play catch-up all over again while you save even more time and money. Because "Quickie" II terminates in just 7 seconds with the Berg QP 106 pneumatic applicator.

It's a simple two-step operation. One: Insert the cable into either lead-in slot. Two: Place the cable/connector in the press and terminate. It's that

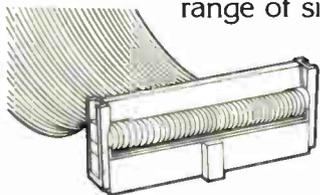
easy! A pre-assembled cover and base gives you fewer parts to assemble and fewer chances to damage components. The cable installs quickly and accurately through an exclusive double-serrated slot with lead-in from either side. The serrations guide the cable to assure precise positioning over the contacts. As a result, mis-assemblies are virtually eliminated.

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takes you more than to Berg's new Quickie* II.



connectors, and other standard and low profile females, female IC, edge card, male DIP, PCB, right angle and vertical headers...all in a broad range of sizes. And all designed to provide utmost flexibility, fast assembly and reliable connections. Choose semi-automatic or hand-operated presses to match your operational re-



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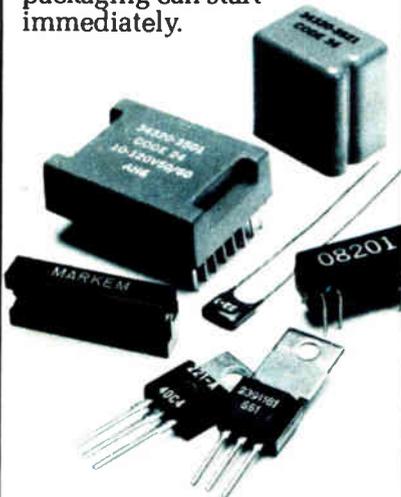
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New products

Instruments

Video camera speeds CAD work

Time-consuming digitizing of pc board designs shrinks to tracing on CRT display

The digitization process in printed-circuit board design can be the most painstaking and time-consuming part of the computer-aided design cycle. If a design is laid out on an oversized drawing, it must be reduced to a size the CAD digitizer can handle, and the point-by-point reconstruction must be exact—pencil renditions, engineering changes of a drawing, and undocumented boards all must undergo a rigid layout process.

To shorten this process, Nicolet CAD Corp. has a video camera tracing attachment for its Graphic System 80. The high-resolution monochromatic camera transfers a drawing or object directly onto the CAD system's display terminal, so that the designer can digitize it directly from the cathode-ray tube, instead of on

the drafting table. "This eliminates the step of a precise pencil-up," says Victor Kley, Nicolet CAD's executive vice president. "The designer need only do a precise calculation of the placement of elements, while leaving a rough sketch with wavy lines."

The video system also makes the user more efficient by consolidating his chores: he performs the digitizing and editing processes in one and the same place, the CRT, rather than on a digitizing table and a CRT. "Our next step with this system is to bypass some of the digitizing process through software that performs specific feature abstraction directly from the video input," says Kley.

Joystick. With the camera, digitizing amounts to a tracing process. It can also involve the use of macro-commands, such as the placement of connections for a 22-pin dual in-line package by defining one connection point of the DIP. The user makes these definitions by manipulating a joystick or small tablet control. The process "can even handle the tracing of objects, such as pc boards, rather than drawings," notes Kley. "That way, even if a pc board is totally undocumented, it can be entered into the system."

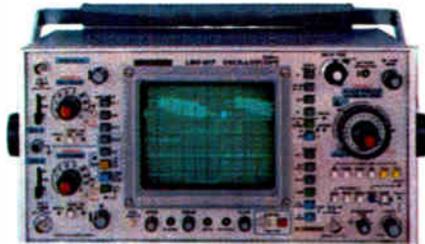
Another advantage of the video system is its zoom feature. Drawings



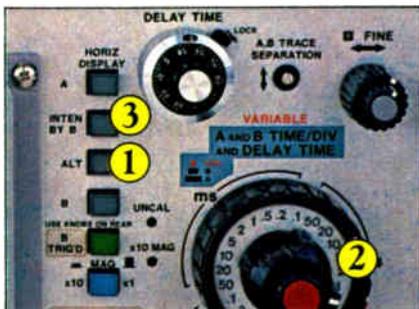
No other 50-MHz oscilloscope gives you as many features as the LBO-517.

Compare the LBO-517 with all other 50-MHz oscilloscopes. Only Leader gives you total capability with:

- Calibrated delayed time-base
- Simultaneous display of main and delayed time-bases.
- Two trigger-view channels.
- 1 mV sensitivity (<10-MHz).
- Alternate/composite triggering.
- Variable trigger hold-off with B-ends-A mode.
- 20 kV accelerating potential dome-mesh CRT.
- Two-year warranty.



It's the surprising leader for under \$2000.



Very low-level signals, complex waveforms, fast pulses at low rep rates, asynchronous signals... no other 50-MHz oscilloscope handles such a wide range of demanding applications, and does it so well as the Leader LBO-517.

Simultaneous Dual Time Base Viewing.

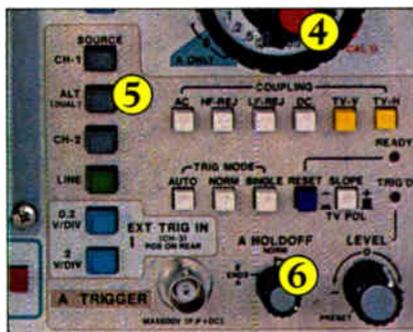
Unlike many other 50-MHz units, the LBO-517 has an alternate time-base mode, (1) above. This permits simultaneous viewing of both the main "A" and delayed "B" time bases (2). The delayed time-base is also shown as an intensified portion of the main time-base display (3). Ideal for studying and measuring complex waveforms.

Fast Sweep Rates, Alternate Triggering, Hold-off and B-ends-A Mode.

The LBO-517 provides main sweep rates from 0.5 sec/cm to 0.05 μ sec/cm in 22 steps (4). Delayed sweep rates

are from 0.1 sec/cm to 0.05 μ sec/cm in 20 steps. For displaying very rapid phenomena, both can be increased to 5 nsec/cm with the X10 magnifier.

The LBO-517 also offers alternate (composite) triggering (5) for stable viewing of two asynchronous signals, along with variable trigger hold-off with a B-ends-A mode (6). Variable hold-off ensures stable triggering of complex signals by ignoring intermediate false trigger points. B-ends-A is used to increase the sweep repetition rate for brighter displays of low-frequency signals.

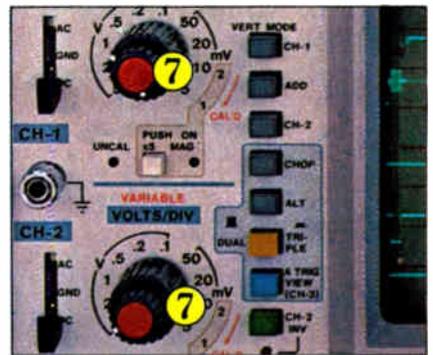


Outstanding Small Signal Performance.

The vertical amplifiers of the LBO-517 offer calibrated deflection coefficients from 5 mV/cm to 5 V/cm in 10 steps (7). A X5 vertical multiplier delivers a

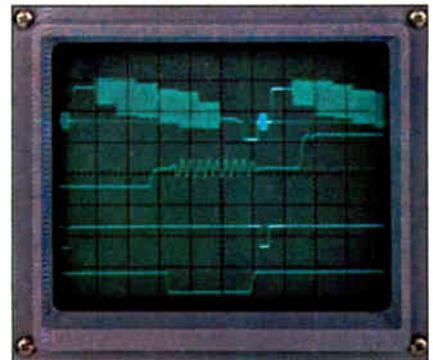
maximum sensitivity of 1 mV/cm up to 10 MHz... 5 times the sensitivity of more expensive oscilloscopes.

An amplified output of channel 1 is also available at a rear panel BNC connector for using the LBO-517's high sensitivity to drive frequency counters and other less sensitive instruments.



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The LBO-517 uses a recently developed dome-mesh CRT operating with a 20-kV accelerating potential. The result is an exceptionally bright, sharp display... with an illuminated internal graticule.



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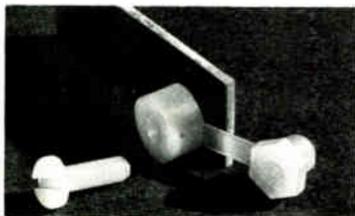
Circle 195 for product demonstration

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New products

that are too small can be magnified and those that are too big can be reduced. Moreover, even though it uses a black-and-white camera, the video attachment can separate colors with different gray-scale values, such as blue and red, so modifications can be clearly distinguished from the original design.

The system 80 that supports the video tracing attachment is built around a proprietary bit-slice mini-computer whose 16-bit processor operates on 32-bit data words. The machine has a 16-K-byte writable control store, 768-K bytes of random-access memory, an LSI-11 front-end processing system, and an 8048-based keyboard and cursor controller. The system's image resolution is 1-K-by-1-K picture elements, upgradable to 2-K-by-2-K; the video camera's horizontal resolution is selectable from 600 to 800 lines. Mass storage consists of two dual-density floppy disks and an optional 30-megabyte hard disk.

The system 80 can cost from about \$44,000 to \$85,000, depending upon choice of peripherals. The video camera tracing attachment is priced between \$8,400 and \$11,900, depending upon the resolution desired. Deliveries will begin in January 1981.

Nicolet CAD Corp., 2530 San Pablo Ave., Berkeley, Calif. 94702. Phone (415) 848-6600 [401]

Noncontact meter reads dc, ac, ripple currents to 200 A

The model CG100D hand-held non-contact current meter reads dc, ac, and ripple currents to 200 A, from dc to 400 Hz. The 9-by-4.5-by-1.4-in. unit has a 3½-digit liquid-crystal display in its handle. It can be clamped around conductors that are up to ¾ in. in diameter, reading through any nonmagnetic insulation without disturbing the current that it measures. Jacks are provided, making it possible to use the CG100D gun probe with an oscilloscope. The CG100D is available from stock for the domestic price of \$249, plus an



extra shipping charge of \$3.50.

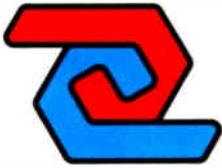
F. W. Bell, 6120 Hanging Moss Rd., Orlando, Fla. 32807 [403]

Measurement unit has programmable functions

A panel-mounted microcomputer called Chameleon can be programmed by the user to convert quickly from one measurement function to another, automatically executing the arithmetic and logic functions common in process measurement and control applications. Since the instrument has 43 programmable constants, it can be used for such wide-ranging applications as: temperature- and pressure-compensated gas-flow measurement, automatic zero updating for differential pressure measurements, corrections for gas expansion, and efficiency calculations. It can also calculate BTUs and heat-transfer coefficients, do batch dispensing, control interface levels, compute boiler-drum levels, and perform frequency-to-current conversion.

The multichannel instrument uses a high-level language for programming. It has no operating controls except a keypad for checking and changing program constants and system display modes. A very basic Chameleon costs \$1,575. The manufacturer calculates that one with a typical selection of options will go for under \$2,000.

Fischer & Porter Co., Jacksonville Rd., Warminster, Pa. 18974 [404]



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The MICRO language is designed to do precisely what you are trying to do — develop microprocessor based products. It has all of the control structures and data types that you need to accomplish true high order, block structured design. MICRO also gives you simple and efficient conformance to ROM and RAM segmentation and location requirements, separate module compilation, and inclusion of embedded assembly language blocks.

The MICRO language generates *efficient code*. When you combine the MICRO compiler with the C-OPT Code Optimizer, we don't know of any comparable compiler that can compete for either speed of operation or efficiency of code produced. That's not all...the MICRO compiler produces the source assembly language of the target processor, with MICRO source statements included as assembler comments. MICRO doesn't change your symbols. And the MICRO listing output includes a structure profile, autoindentation, and symbolic cross-reference.

S-BASIC We've added block structured control statements, extended variable names, powerful string manipulation, and both interpretive and compilative modes of operation to give you system development capability in the efficient and familiar BASIC language.

Within the environment of the S-BASIC Command Processor/Line Editor, you can develop and logically debug your programs. When you're ready, you can compile them into source assembly language. Then you can assemble, link, load, and verify them with your customary development system tools. And the assembly language output of the S-BASIC compiler can be compressed with the C-OPT Code Optimizer.

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Environment All our products are available to run on the GenRad/Futuredata 2300 Development System, and the Tektronix MDL. Target processors are Z-80 and 8080/8085. The Z-80 versions of our products take advantage of the Z-80 architectural features to produce smaller, faster code.

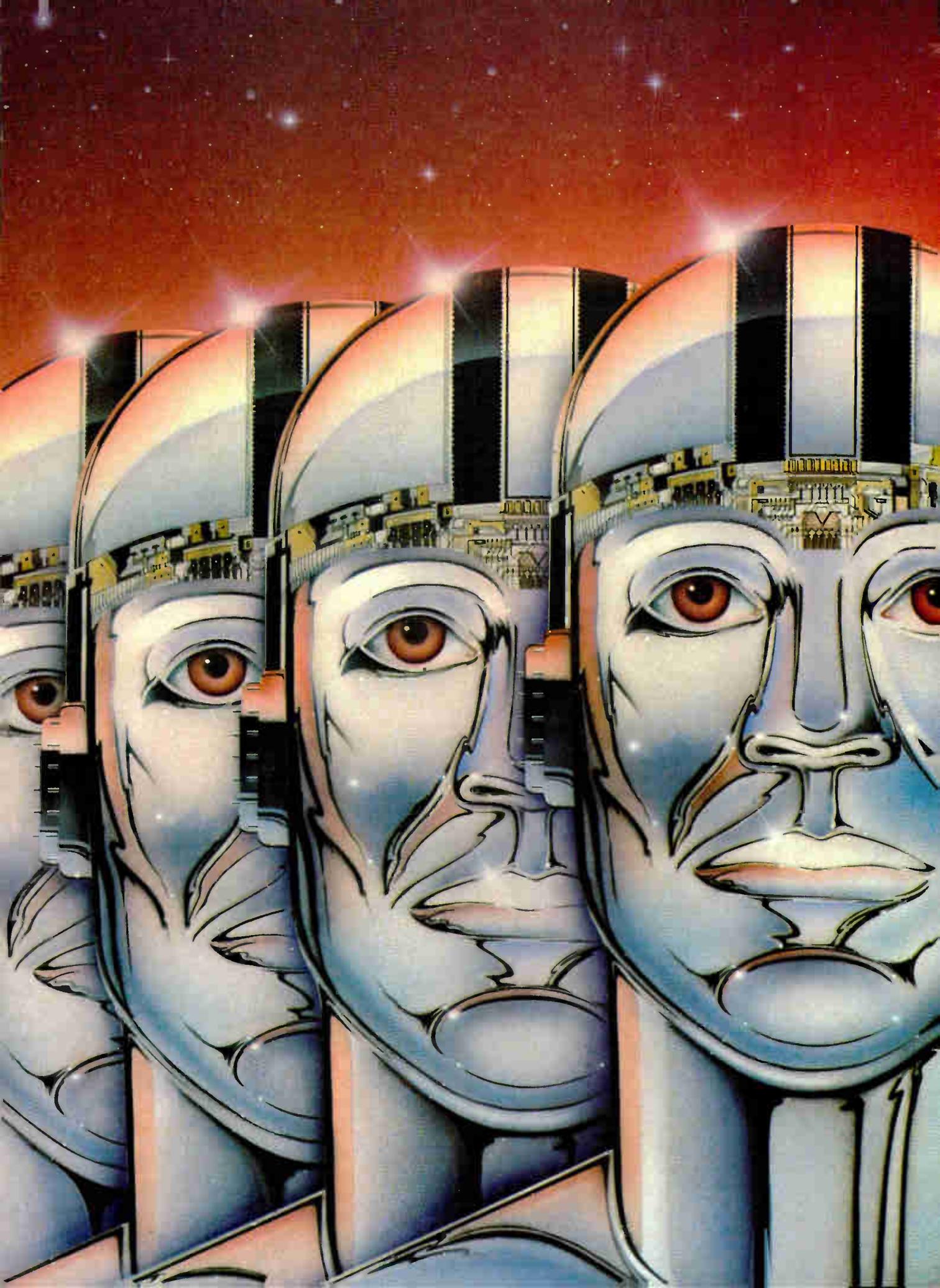
We're currently working on supporting more target processors on more hosts with our products. We're also building new software development tools. So, if you didn't see your favorite processor or host above, chances are we're working on it. Give us a call and we'll discuss your requirements with you.

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| Part Number | Access Time | Cycle Time |
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| μ PD416-2 | 200ns | 375ns |
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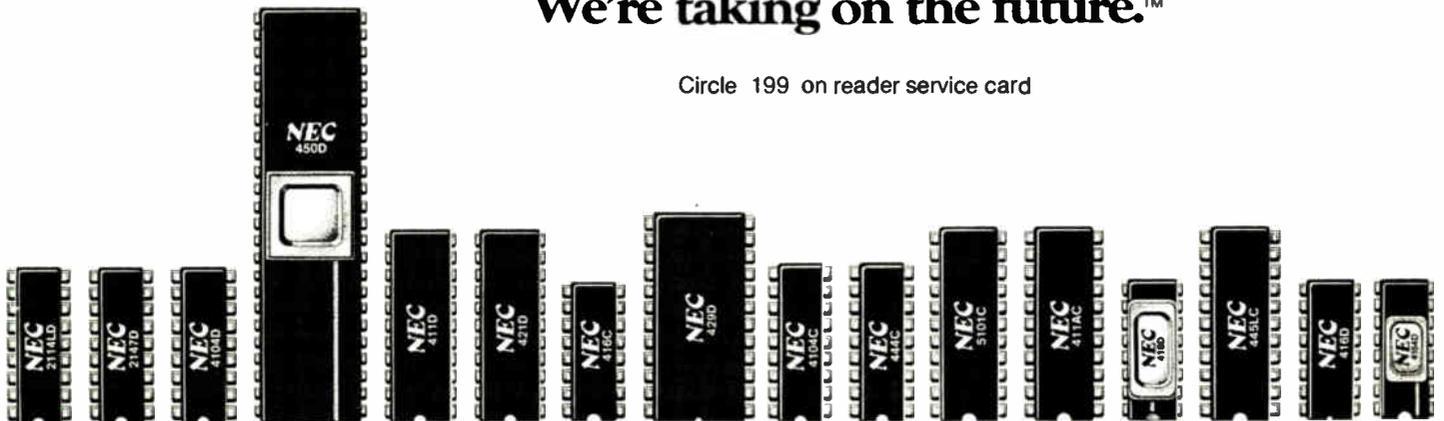
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Circle 199 on reader service card



Semiconductors

ECL family halves gate delay

Faster replacements for 10K circuits dissipate about the same power

Running several months ahead of previously stated plans, Motorola Semiconductor Group's Bipolar Integrated Circuits division is putting the first sample parts of its new emitter-coupled-logic family, MECL 10KH, into the hands of prospective customers this month. Based on a high-density process called Mosaic, the 10KH parts have half the gate-delay times of the 10-year-old MECL 10000 (10K) circuit family—1 instead of 2 ns.

The division pushed hard to sustain momentum "to keep the ECL banner flying," as L. J. Reed, manager of bipolar logic design, puts it. Early completion of the 10KH production line was aided by the fact that it is the second family to be manufactured in the division's new Mesa, Ariz., bipolar fabrication facility. MECL Macrocell arrays are already being turned out there; this work helped smooth out production kinks. Motorola expects a major application of the 10KH family to be the "glue," or associated circuitry, for the Macrocell array parts.

The Mosaic process gets its density and thus performance advantages

in part from the fact that it is based on oxide-isolation technology rather than the junction-isolated technology used for the 10K family. Transistor area with Mosaic can in fact be reduced by an approximate factor of seven. The new process can be used for circuits with up to 1,000-gate complexity.

Even though speed is up, the 10KH family keeps almost the same power requirement—22 to 25 mW per gate, compared with 25 mW for 10K devices. Rise and fall times are 1.5 ns, or about 75% of the 10K times. Although this increased speed may generate more system noise, the new parts have 20% better noise margins to compensate: 150 mV, compared with 125 mV.

Direct substitution. Replacing 10K circuits with 10KH equivalents can improve overall system clock rates by 25% to 30%, typically, according to Reed. And since the new line is pin-compatible with the older parts, systems where 10K logic is already incorporated can be upgraded without redesign.

The only characteristic not matching its counterpart in the 10K line is the specified temperature range of 0° to 75°C, compared with -30° to 85°C for the older parts. The narrowed range is dictated primarily by limitations of memories and other logic parts with which the 10KH logic will be used, notes Reed. "But I haven't heard any complaints yet about temperature, because mostly they will be run at 50° to 60°C ambient." On the other hand, the new line is voltage-compensated, "a significant feature to all the custom-

ers we have talked to."

For the first sampling of the new family, 11 parts have been scheduled, with 5 of them available immediately. The first group includes the MC10H101, a quad OR/NOR gate; the MC10H102 quad NOR gate; the MC10H105, a triple OR/NOR gate that has two gates with two inputs and a third with three inputs; the MC10H109 dual OR/NOR gate with one four-input gate and one five-input gate; and the MC10H116 triple line receiver.

Parts to be available in January are the MC10H104, a quad AND gate; the MC10H107 triple-exclusive OR/NOR gate; the MC10H130 dual D-type latch; and the MC10H131 dual D-type flip-flop. Another 13 products will be added to the line during 1981.

Prices of the 10KH parts will initially be about 30% higher than those of their counterparts in the 10K family in large production quantities. The 10K family will continue in production.

Motorola Inc., Bipolar Integrated Circuits Division, 2200 W. Broadway Rd., Mesa, Ariz. 85202, or P. O. Box 20906, Phoenix, Ariz. 85036. Phone (602)962-2202 [411]

Chip contains all active elements of a-m/fm radio

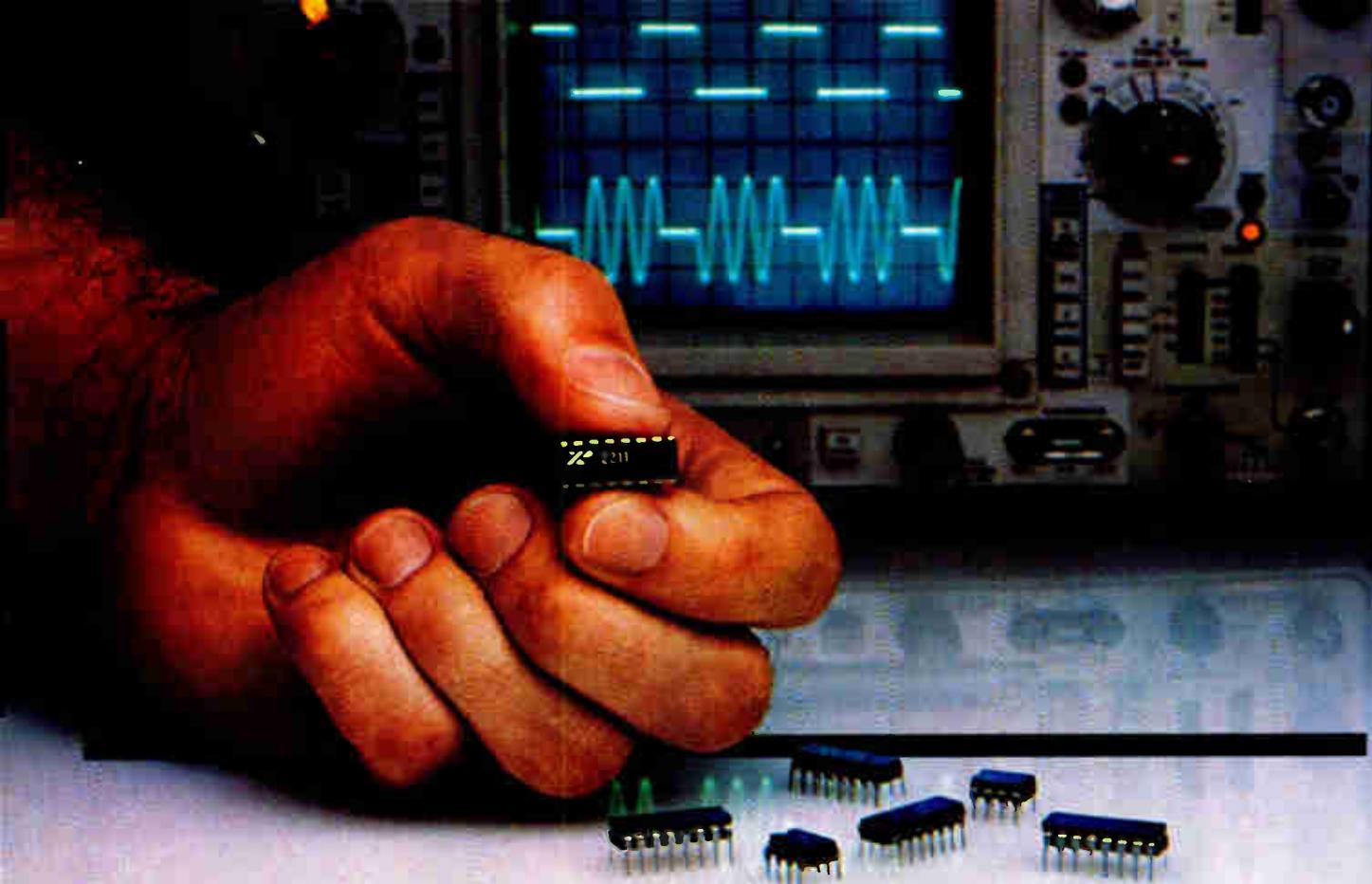
The LM1868, a single chip containing all the active elements of an a-m/fm radio, is useful for line- or battery-operated radios as well as weather and multiband radios. It can also be joined with digital alarm clock chips for clock radios.

An LM1868 combined with an fm tuner and other passive devices constitutes a complete 0.5-w a-m/fm radio. It maintains performance over a 70-dB range of input signals and 4.5- to 15-v supply voltages. The integrated radio circuit contains a power audio amplifier that can drive an 8-Ω load to a 700-mW level when operating from a 9-v supply.

Housed in a 20-pin plastic dual in-line package, the LM1868 is priced at less than \$1.00 in high volumes. Delivery is in 8 to 10 weeks

MOTOROLA'S EMITTER-COUPLED-LOGIC GENERATIONS COMPARED

| Parameter | MECL 10,000 | MECL 10 KH |
|--|-------------|------------|
| Propagation delay per gate (ns) | 2 | 1 |
| Power per gate (mW) | 25 | 22-25 |
| Noise margin (mV) | 125 | 150 |
| Operating temperature range (°C) | -30° - +85° | 0° - +75° |
| Emitter dimensions (μm) | 4 by 20 | 3 by 8 |
| Transition frequency (maximum at which β = 1; GHz) | 1.6 | 3.5 |
| Capacitances (pF) | | |
| Collector-base | 0.46 | 0.16 |
| Emitter-base | 0.18 | 0.07 |
| Collector-substrate | 0.83 | 0.18 |



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ELX 12/4/80

EXAR'S PLL CIRCUITS

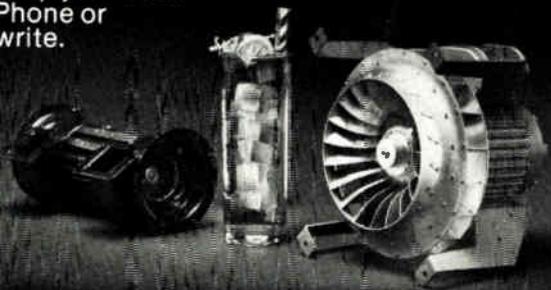
| CIRCUIT TYPE | PART NO. | FREQUENCY LIMIT | TYP. TEMP. STABILITY (ppm/°C) |
|----------------|----------|-----------------|-------------------------------|
| High Frequency | XR-210 | 20 MHz | ±200 |
| | XR-215 | 35 MHz | ±250 |
| High Precision | XR-2211 | 300 kHz | ±20 |
| | XR-2212 | 300 kHz | ±20 |
| | XR-557 | 500 kHz | ±140 |
| | XR-LS67 | 50 kHz | ±150 |
| | XR-2567 | 600 kHz | ±100 |

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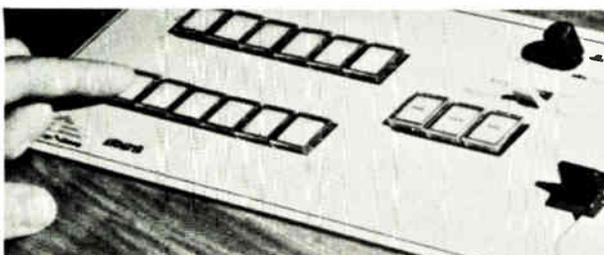


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National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 737-5000 [413]

80-ns 16-K ROM can replace bipolar PROMs

Since a large portion of all programmable read-only memories sold are really being used as ROMs, switching to a lower-cost ROM after prototyping with PROMs may help reduce system costs. Now there is an MOS 16-K device, organized as 2,048 by 8 bits, that can replace bipolar PROMs in many applications. The SY3316 H-MOS ROM with an 80-ns maximum access time is fully compatible with 16-K bipolar PROMs.

The unit is fully TTL-compatible and operates on a single +5-V power supply. It has three-state outputs, fully static circuitry and operates asynchronously. The device is priced at \$56 in quantities of 250 and is available now.

Synertek, 3001 Stender Way, Santa Clara, Calif. 95051 [414]

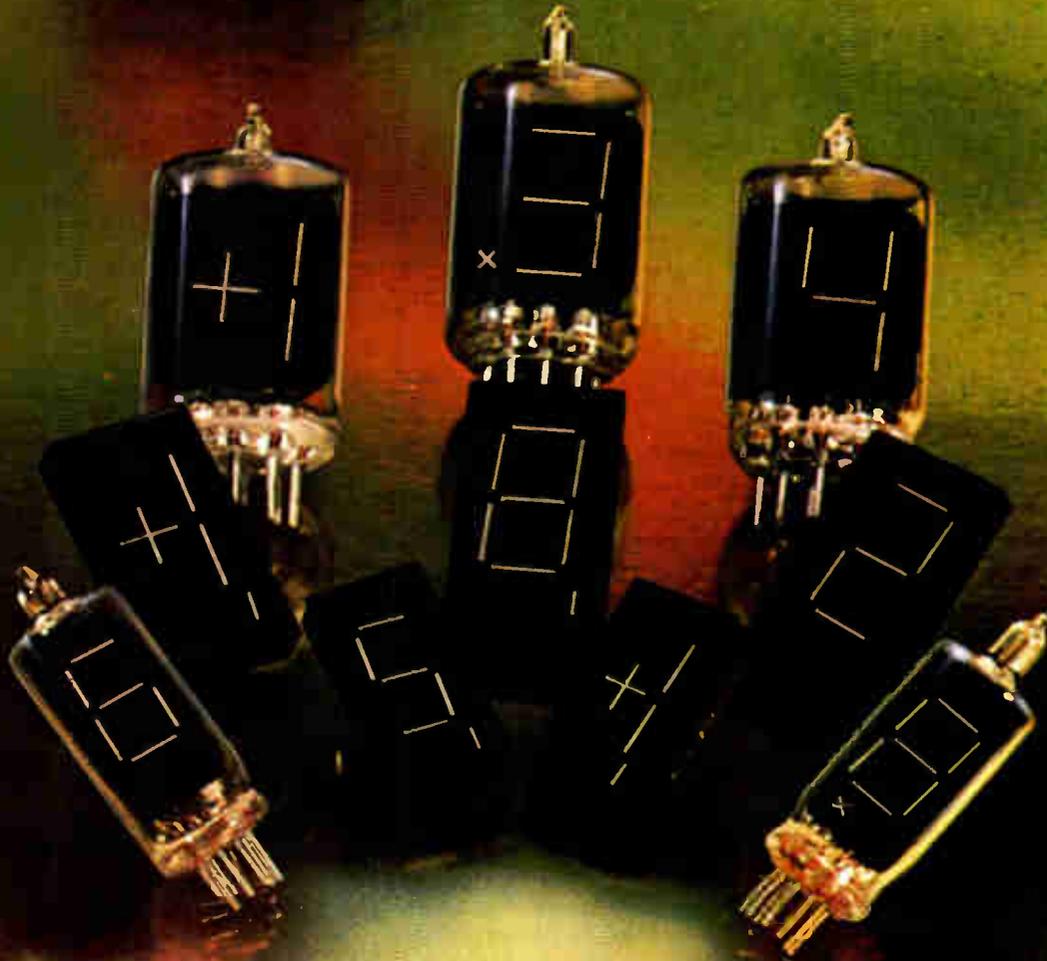
Quad op amps' current range is fully programmable

Three quad operational amplifiers for use in active filter applications each feature four programmable amps and operate at supply voltages ranging from ± 1.5 to ± 12 v. The TAB 1044 and 1042 are both programmed by current to a common bias pin; the TAB 1043 is programmed by means of two different bias supply pins. The 1042 operates at supply voltages as low as ± 1.5 v and with power as low as $\pm 40 \mu\text{A}$. In addition, its operating frequency range goes up to 1 MHz.

The TAB 1044 utilizes a Darlington output stage to boost its current-drive capability. In quantities of 100, the TAB 1042, 1043, and 1044 are priced at \$2.64, \$2.84, and \$2.86, respectively.

Plessey Semiconductors, 1641 Kaiser Ave., Irvine, Calif. 92714. [415]

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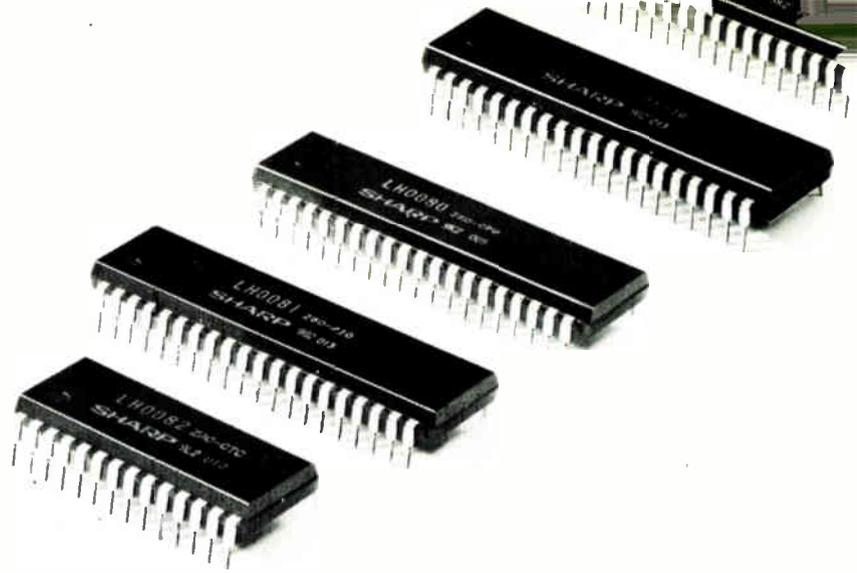


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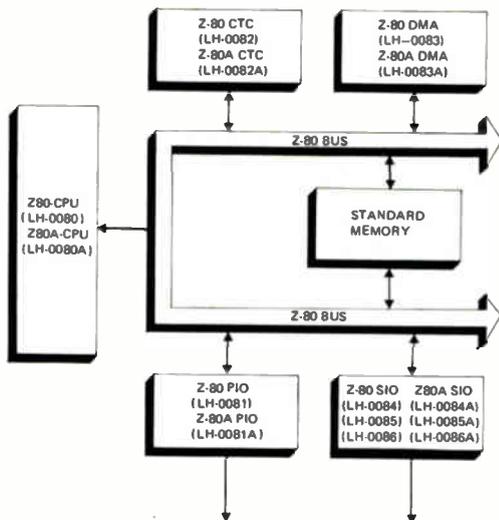


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| ZILOG | SHARP Type No. | Explanation | Features | Package |
|---|----------------------------------|-------------------------|--|---------|
| Z-80 CPU Z-80A CPU | LH-0080 LH-0080A | Central Processing Unit | • 158 instructions — includes all 78 of the 8080A instructions • Three modes of maskable interrupt plus a non-maskable interrupt • 22 internal registers • • | 40 DIP |
| Z-80 PIO Z-80A PIO | LH-0081 LH-0081A | Parallel I/O Controller | • Two independent bidirectional ports • Any one of the following modes of operation may be selected for either port: Byte input/output, Byte bidirectional bus, Bit Mode • • | 40 DIP |
| Z-80 CTC Z-80 CTC | LH-0082 LH-0082A | Counter Timer Circuit | • Four independent programmable 8-bit counter/16-bit timer channels • Single phase clock • • | 28 DIP |
| Z-80 DMA Z-80A DMA | LH-0083 LH-0083A | Direct Memory Access | • Single channel 2 port • Three classes of operation • 3 Modes of operation • Up to 1.25MB search rate • • | 40 DIP |
| Z-80 SIO/0 Z-80 SIO/1 Z-80 SIO/2 | LH-0084 OH-0085 LH-0086 | Serial I/O Controller | • Two full duplex channels • Asynchronous operation • Binary synchronous operation • HDLC IBM SDLC Mode • 0 ~ 550k bits/Sec • • | 40 DIP |
| Z-80A SIO/C Z-80A SIO/1 Z-80A SIO/2 | LH-0084A LH-0085A LH-0086A | | | |

Vcc (V): +5

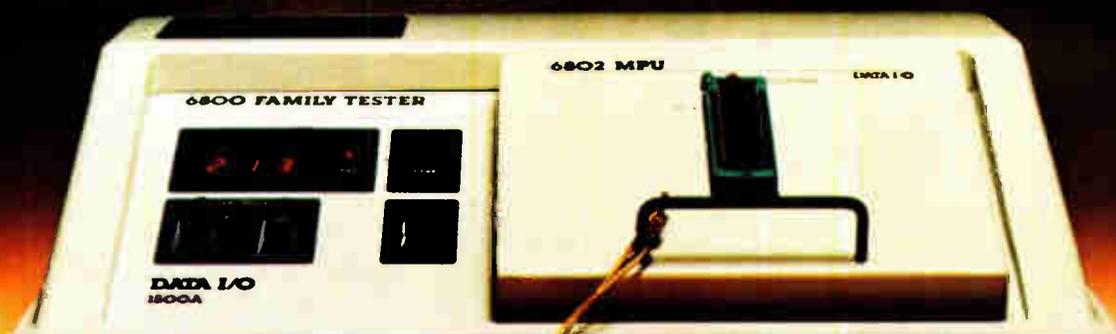
• Z-80: clock frequency 2.5MHz Z-80A: clock frequency 4MHz

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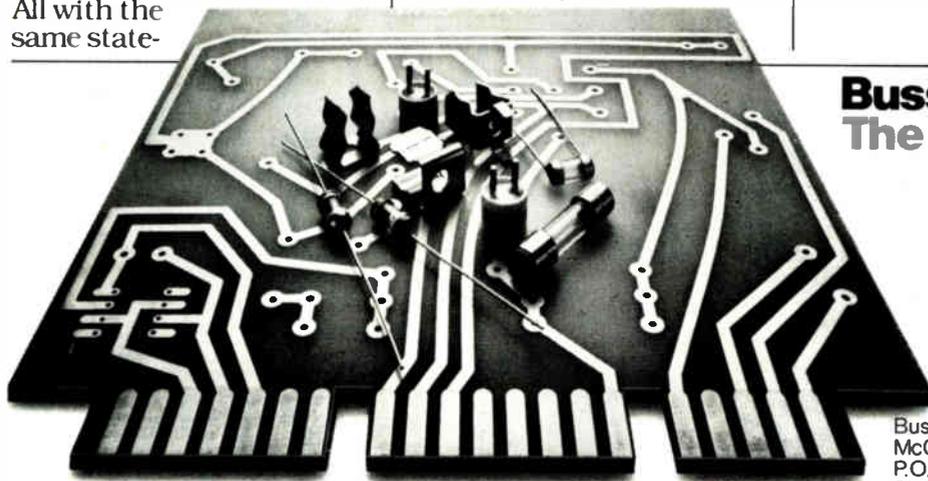
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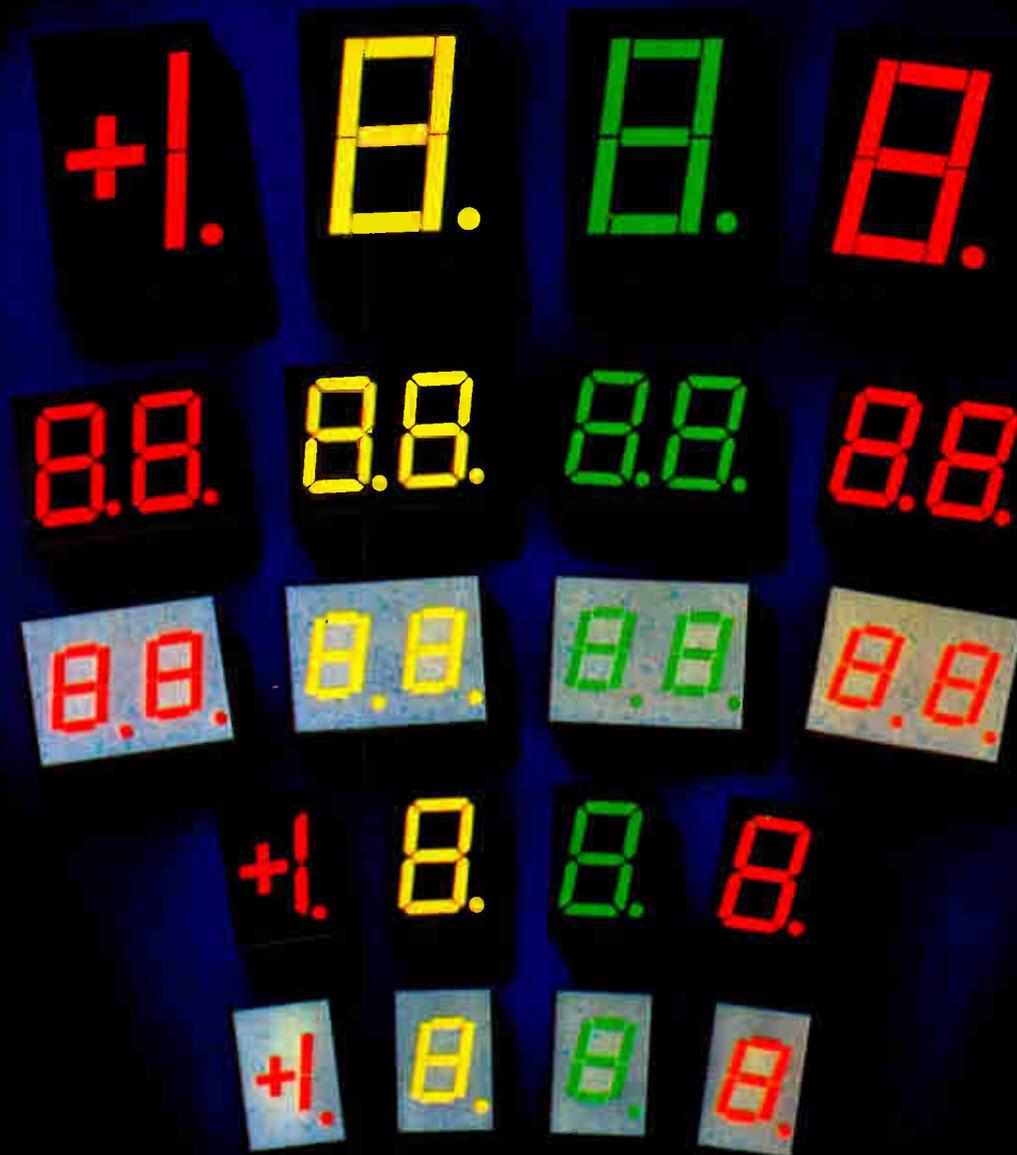
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Circle 207 on reader service card

Power supplies

25-W supplies are 80% efficient

\$69 encapsulated modules
are 1.25 in. high, do not
need external heat sinks

A family of compact 25-w line-operated switching power supplies from Power General have reached the 80% mark in overall efficiency, according to George C. Chryssis, engineering vice president, but they are also low in cost at \$69 each. The level of efficiency in itself is not new, but it is at this price. Two small switchers from Datel-Intersil [*Electronics*, Aug. 30, 1979, p. 246], the 15-w USM-5/3 and the 25-w USM-5/5, are similar in most respects to the Power General modules, including the 80% efficiency, but they cost \$98.50 and \$114.50, respectively.

The efficiency of the Power General 125-series modules results in relatively cool operation without external heat sinks. The cool operation, along with the units' compact design, allows designers to plug the modules right into printed-circuit boards. The epoxy-encapsulated switchers measure 2.5 by 3.5 by 1.25 in. high and weigh 14 oz.

A modified half-bridge switching configuration developed by the firm contributes to improved efficiency by minimizing rise and fall times in the switching transistors. Use of switching transistors derated by as much as 50% of their maximum ratings reduces voltage drop at the input, and Schottky rectifiers minimize voltage drop at the output. Switching is at 20 kHz.

The half-bridge switching configuration also holds down ripple and noise (50 mV p-p, or 10 mV rms) by preventing output capacitors from discharging completely at any time in the switching cycle. All four models accept inputs ranging from 85 to 130 v or 170 to 260 v ac, 47 to 470 Hz. Outputs are: 5 v ac at 5 A (mod-

el 125); 9 v dc at 2.8 A (model 126); 12 v at 2 A (model 127); and 15 v at 1.7 A (model 128). The power modules have floating outputs that can be referenced to be either positive or negative.

Full rated outputs are maintained over an ambient temperature range of 0° to 50°C; derating is 2%/°C to 70°C. The temperature coefficient is $\pm 0.02\%$ of output per °C. Line and load regulation are $\pm 0.1\%$ and $\pm 0.4\%$, respectively, and transient response is 300 ms to within 1% of final output. All supplies in the series have soft start, current limiting, and overvoltage protection. Input-to-output isolation is 1,500 v ac.

The 125 series should compete particularly well in modem, cathode-ray-tube terminal, electronic game, and biomedical equipment markets, thinks John C. Gallagher, president of the company. They will be delivered in four to six weeks.

Others. The firm has recently introduced other switching supplies of the same high efficiency, among them the 1060 and 2050 models. The former supplies 12 A at a level adjustable from 4.5 to 5 v. It is available from stock on a printed-circuit board for \$105, in an open frame for \$109, and enclosed in an aluminum case for \$117.

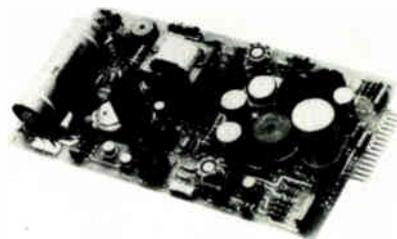
The 2050 comes in two versions, each with two outputs. The 2050-1 is designed to power the Rockwell AIM-65 microcomputer and ancillary equipment; it puts out 5 v at 6 A and 24 v at 0.5 A average, 2.5 A peak. The 2050-2 is intended to power Digital Equipment Corp.'s LSI-11-based systems, supplying 5 v at 8 A and 12 v at 1.5 A. The 2050 series is priced at \$123 in an open frame and \$133 enclosed; delivery is within four weeks.

Power General Corp., 152 Will Dr., Canton, Mass. 02021. Phone (617) 828-6216 [351]

Five-output switchers have 50-to-65-W ratings

The Etatech series of open-frame switching power supplies provide up to five outputs and are available in

eight standard models rated from 50 to 65 w. Maximum output power totals 65 w distributed in the following output configurations: the primary output, which is 5 v at up to 8 A, and secondary outputs of ± 12 to ± 15 v at up to 12 w, -12 to -15 v at up to 12 w, 5 to 15 v up to 18 w, and substrate bias at up to 0.25 w. The units' input voltage range is from 85 to 135 v root mean square at 47 to 440 Hz, single phase, or 115



to 185 v dc. The primary output's line and load regulation are 10% of full scale. Ripple and noise are 100 mV peak to peak in the primary output and 2% or 200 mV p-p on secondary outputs.

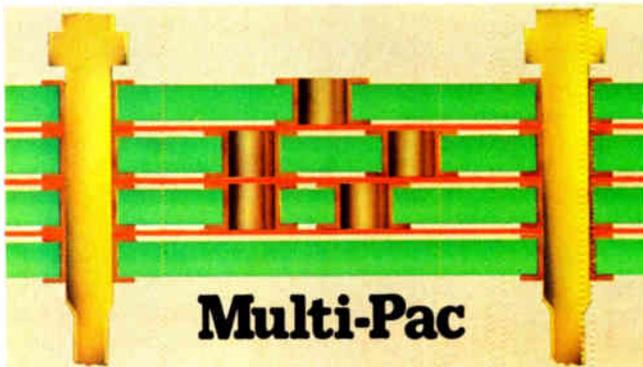
Each switching power supply measures 5 by 9 by 2 in., operates over a 0° to 50°C range, and has short-circuit and overload protection. In quantities of 100, the supplies are \$132 apiece and can be delivered from stock in 30 days.

Adtech Power Inc., 1621 S. Sinclair St., Anaheim, Calif. 92806. Phone (714) 634-9211 [355]

75-W, five-output switcher has fully, semiregulated versions

The ESQ-75 five-output switching power supply provides 75 w of continuous power for floppy disks, printers, and other electromechanical system applications. The series includes both fully regulated and semiregulated models, with the fully regulated models offering $\pm 1\%$ load regulation on all outputs for a 10%-to-100% load change. At an input of 90 to 132 v ac or 180 to 264 v ac at 47 to 440 Hz, line regulation is $\pm 0.2\%$. Outputs are +5 v at 8 A, +12 or +15 v at 1.5 A, -12 or

Multi-Pac[®] edges out Multilayer in the photo finish.



Even though Multi-Pac is used by many O.E.M.'s some people still consider us a dark horse. That's OK ... a winner has to come out of the pack to be recognized. At Elfab, we've done it with press-fit technology. We were the first. And since that time we've set a fast pace as a leader in the industry. Now we want to set the pace with Multi-Pac, our innovative assembly of stacked PC boards held together in a "sandwich" with press-fit contacts.

Multi-Pac or multilayer. At Elfab you can win either way, no matter what your preference, because we do make them both. Examine the competitive differences closely and see if you don't agree with us that Multi-Pac comes out ahead.

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- Pole Position: Multi-Pac costs 10-15% less.
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 - Third: Guaranteed controlled impedance with uniform board spacing. Great for high speed logic circuits.
 - Fourth: Multi-Pac lets you build Hybrid systems into any part or all of the board. Unlike multilayer, with Multi-Pac you can stack additional circuit layers on sections of the backpanel or daughter board where additional density is needed.
 - Fifth: Because Multi-Pac is a stack of discrete PC boards, any board can be changed right up to assembly time (when the contacts are pressed in place).
 - Sixth: Repairability — Contacts can be removed with Multi-Pac, and circuit layers can actually be assessed for changes or repairs.
 - Seventh: Moisture-in-Moisture out. Multi-Pac meets MIL-STD 202 method 103 test B for humidity; and 101 test B for salt spray.
 - Eighth: Properly done, your art work can be interchangeable with multilayer and Multi-Pac. Thus, you always have two sources.
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-15 v at 1.5 A, 24 v at 1.5 A, and -5 v at 1.5 A. The manufacturer can also make customized units that feature user-specified voltages and regulation.

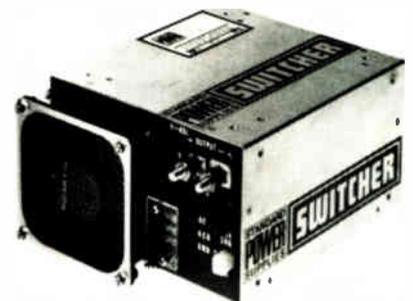
Each power switcher weighs 2 lb 10 oz and measures 9.6 by 5.25 by 2.25 in. Its operating temperature range is from 0° to +71°C. Noise and ripple are 1% maximum peak to peak, and efficiency is rated at 75%. The price of the open-frame supply begins at \$189. Available options are thermal cutout, logic inhibition, ac transient suppression, and crowbar protection.

Power/Mate Corp., 514 S. River St., Hackensack, N. J. 07601 [353]

750-W switchers are built
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The series SWS 751 switching regulated dc power supplies, which are rated at 750 w, have been granted recognition by Underwriters Laboratories under file number E50284.

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pressed at the source with line filters.

The SWS 751 supplies are priced at \$695 each and are available from stock.

Standard Power Inc., 1400 S. Village Way, Santa Ana, Calif. 92705. Phone Carroll Goldsworth at (714) 558-8512 [356]

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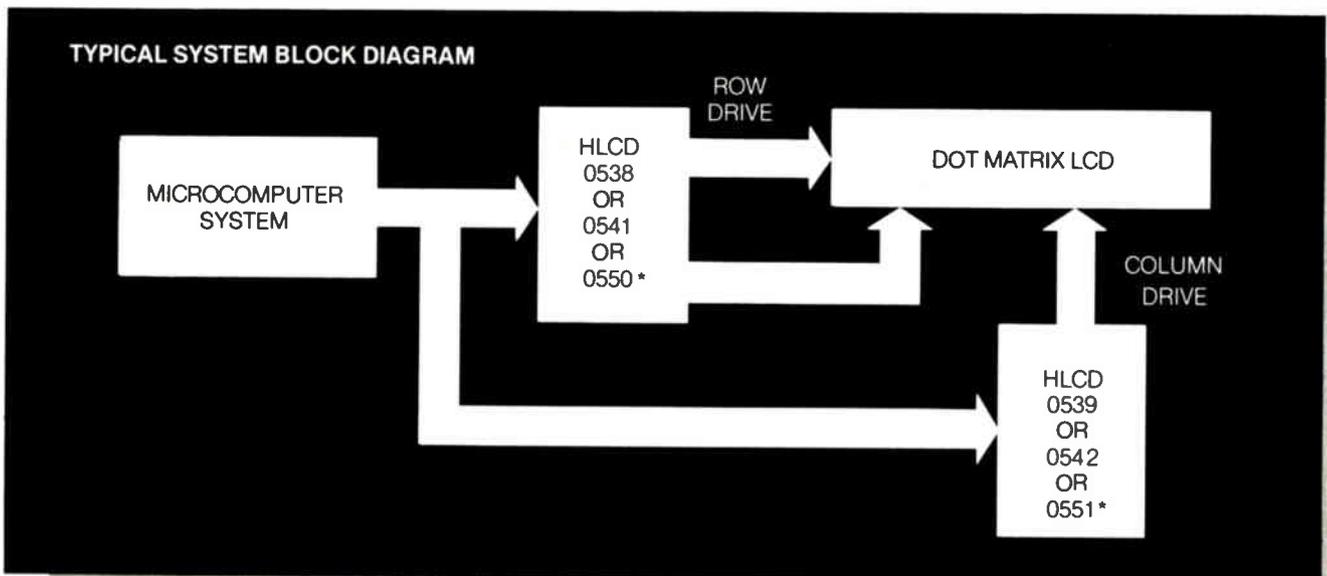
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Analog Devices, Inc., Box 280, Norwood, MA 02062, East Coast: (617) 329-4700; Midwest: (312) 894-3300; West Coast: (714) 842-1717, Texas (214) 231-5094; Belgium: 031/37 48 03; Denmark: 02/84 58 00; England: 01/941 0466; France: 01 687 3411; Germany: 089/53 03 19; Japan: 03/263 6826; Netherlands: 076/87 92 51; Switzerland: 022/31 57 60, and representatives around the world

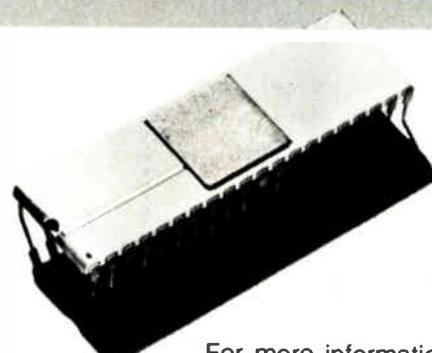
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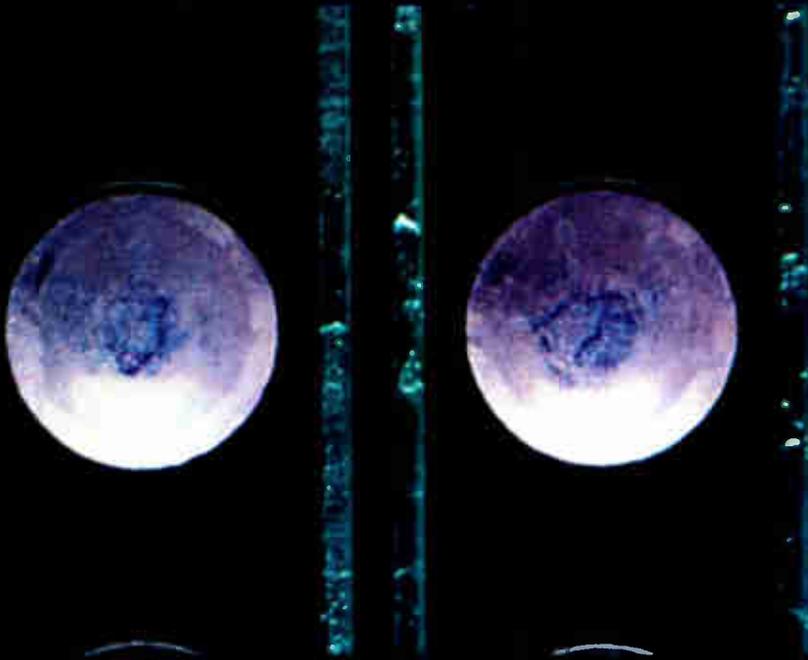
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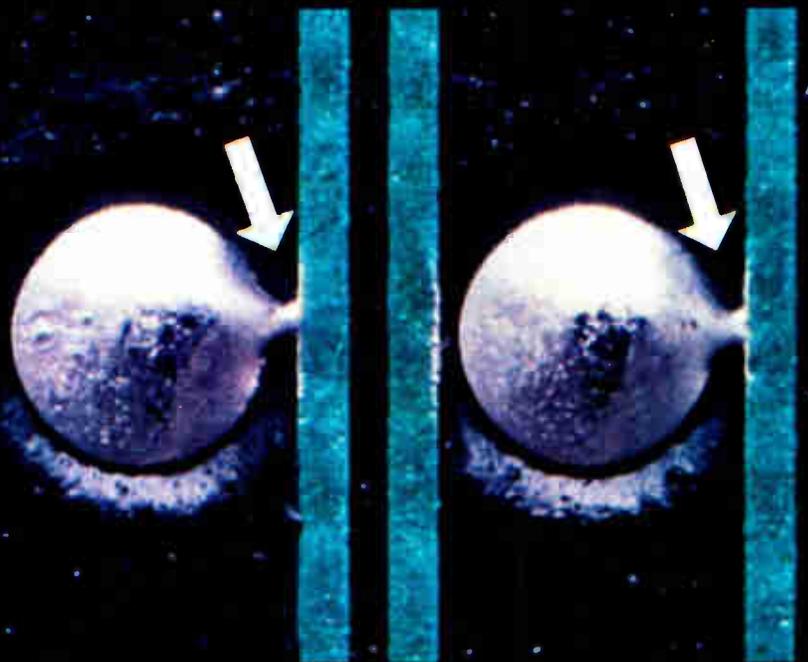
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Innovations for Electronics



Circle 213 on reader service card

Components

Smart LED system has own latches

Alphanumeric display system needs no maintenance by host, has editing capabilities

A self-contained alphanumeric display system from Litronix comes in a portable package and performs many of the functions of a cathode-ray-tube terminal. According to its developers at the affiliate of West Germany's Siemens AG, the new intelligent display system (IDS) easily interfaces with any minicomputer or microcomputer-based system.

Designated the IDS-2416 series, the system combines Litronix' intelligent display assembly (IDA) concept [*Electronics*, June 5, p. 243] with a controller board mounted piggyback behind the display board containing a preprogrammed microcomputer chip and associated circuitry. The microcomputer, Intel Corp.'s 8-bit 8035, "eliminates the requirement for host system display maintenance and interaction normally required for multiplexing alphanumeric displays," according to product design engineer Conner Vlakancic.

The display panel board uses Litronix' DL-2416 four-character, 17-segment (16 segments plus decimal point), intelligent light-emitting-diode display modules. Each module has its own complementary-MOS chip containing a memory for storing character codes, a read-only memory for generating ASCII characters, and a display multiplexer. The board can be configured as 16, 24, or 40 characters. Because it uses intelligent displays, a concept that Litronix pioneered three years ago, the IDS does not require, among other devices, additional segment drivers and ASCII-character decoders, Vlakancic says.

Depending on their operating mode, conventional alphanumeric display systems may make the host computer wait from 500 to 700 μ s before they will accept new input data; hardware latches may be designed into the system to overcome this shortcoming. The IDS, however, incorporates its own latches, which may be disabled by a jumper if it is to replace a conventional display.

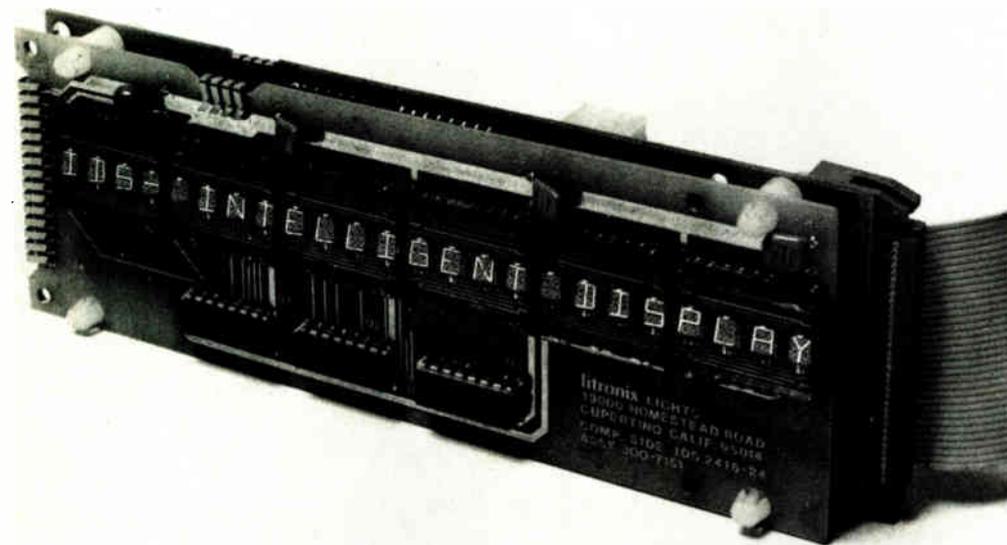
A second jumper puts the IDS through an internal diagnostic check of its display and program memory. This "lap test," as Vlakancic calls it, "is particularly good for aviation and limit-alert panels, where it is important that all segments be operating. "Otherwise," he adds, "a vital message could be changed from 'critical' to 'noncritical.'"

Among other unique features of the IDS, Vlakancic notes, are fully buffered input, output, and control lines, as well as software in a separate programmable ROM used in conjunction with the 8035 microcomputer. "This allows substitution of a custom program ROM for special functional requirements." Other intelligent display systems that use an 8048 microcomputer with mask-programmed ROM do not let users change the program without a mask change, which typically requires a minimum purchase of 1,000 ROMs.

The IDS has display-editing capabilities that include: flashing cursor, back space, forward space, insert, delete, carriage return, and line feed. In addition, it has five data-entry modes—left, left-expanded, block, right, and random-access-memory. Whereas the left mode is similar to that of a typewriter, the left-expanded mode is used with multiline displays. It has a cursor that moves from one line to another, and messages on one display can be repeated on another via a keystroke command. In the right-end mode, data is loaded at the right while shifting previous data to the left, as on a marquee, with RAM keeping track of as many as 36 spaces to the left of the display for recall.

The block mode is similar to the left mode, only without the cursor and editing features, and is intended for applications where the host computer is sending a message. The RAM mode is for data-editing applications and lets the user access a location in the 8035's RAM to change a character without having to rewrite the entire message. In all modes, the contents of the RAM can be sent to a host computer or peripherals by a single keyboard command.

The IDS is tailored to applications in electronic test and medical instruments, data-entry terminals, computer peripherals, and process control systems. TTL- and C-MOS-compatible, it draws 425 to 700 mA from a single +5-V supply, depending on the mix of characters (350 mA when idle). An IDS-2416-24 with a 24-character display will be priced below \$300 in quantities of



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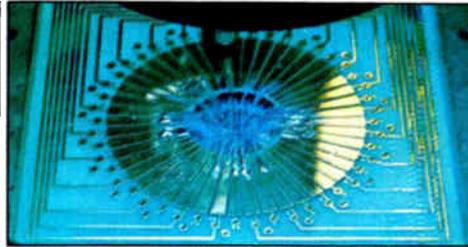
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Litronix Inc., 19000 Homestead Rd., Cupertino, Calif. 95014. Phone (408) 257-7910 [341]

Flat-panel display is 1.6 inches thick

A 240-by-320-line flat-panel display is only 1.6 in. (40 mm) thick and has a 10,000-hour lifetime. The model ED-6240 electroluminescent display module provides flicker-free graphics or alphanumeric (24 lines of 53 characters) and can write or erase a full frame in $\frac{1}{60}$ of a second.

The unit, which consumes 13 w, provides 25 ft illumination with output in the yellow region of the spectrum. Housed in a 7.5-by-6.3-by-1.6-in. case, the 3.4-by-4.7-in. display weighs about 0.5 lb (250 g) and is available in limited quantities for \$2,800. Prices for volume orders are expected to fall in the \$800-per-unit range. Interface board accessories to enhance display functions will be available later.

Hycom Inc., 16841 Armstrong Ave., Irvine, Calif. 92714. Phone (714) 557-5252 [343]

500-W miniature transformer switches at 100-kHz rate

Designed specifically for driving high-powered MOS field-effect transistors, the model 7-0068 miniature transformer provides 0.5-v output with 100-A capacity at a 100-kHz switching rate. The transformer has a split primary winding, enabling use with either 150- or 300-v ac input voltages. Dc resistances for the primary and secondary windings are 65 and 0.3 m Ω , respectively. Primary to secondary capacitance is 55 pF, and primary-winding inductance is a minimum of 3.75 mH. The manufacturer has not set prices on the 1.6-by-1.7-by-1.8-in. unit, but says that deliveries can be made from stock.

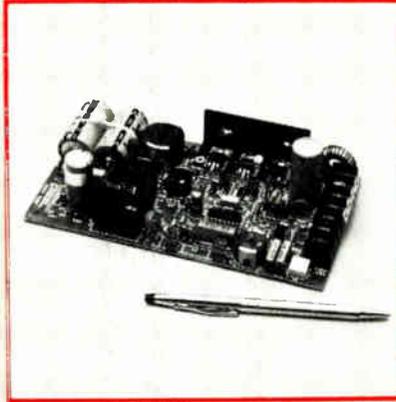
Tranex Inc., 1601 Stierlin Rd., Mountain View, Calif. 94043. [344]

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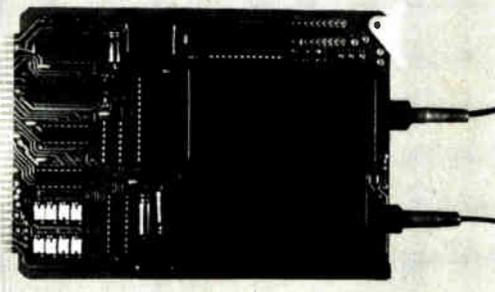
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Model 1861 simultaneously programs 8 ganged MOS.

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| Baud rate: | | 110, 300, 600, 1200, 2400, 4800, 9600 | |
| Size, weight | | 280 (W) x 208 (D) x 65 (H) mm, 2.5kg | 280 (W) x 208 (D) x 75 (H) mm, 3.5kg |



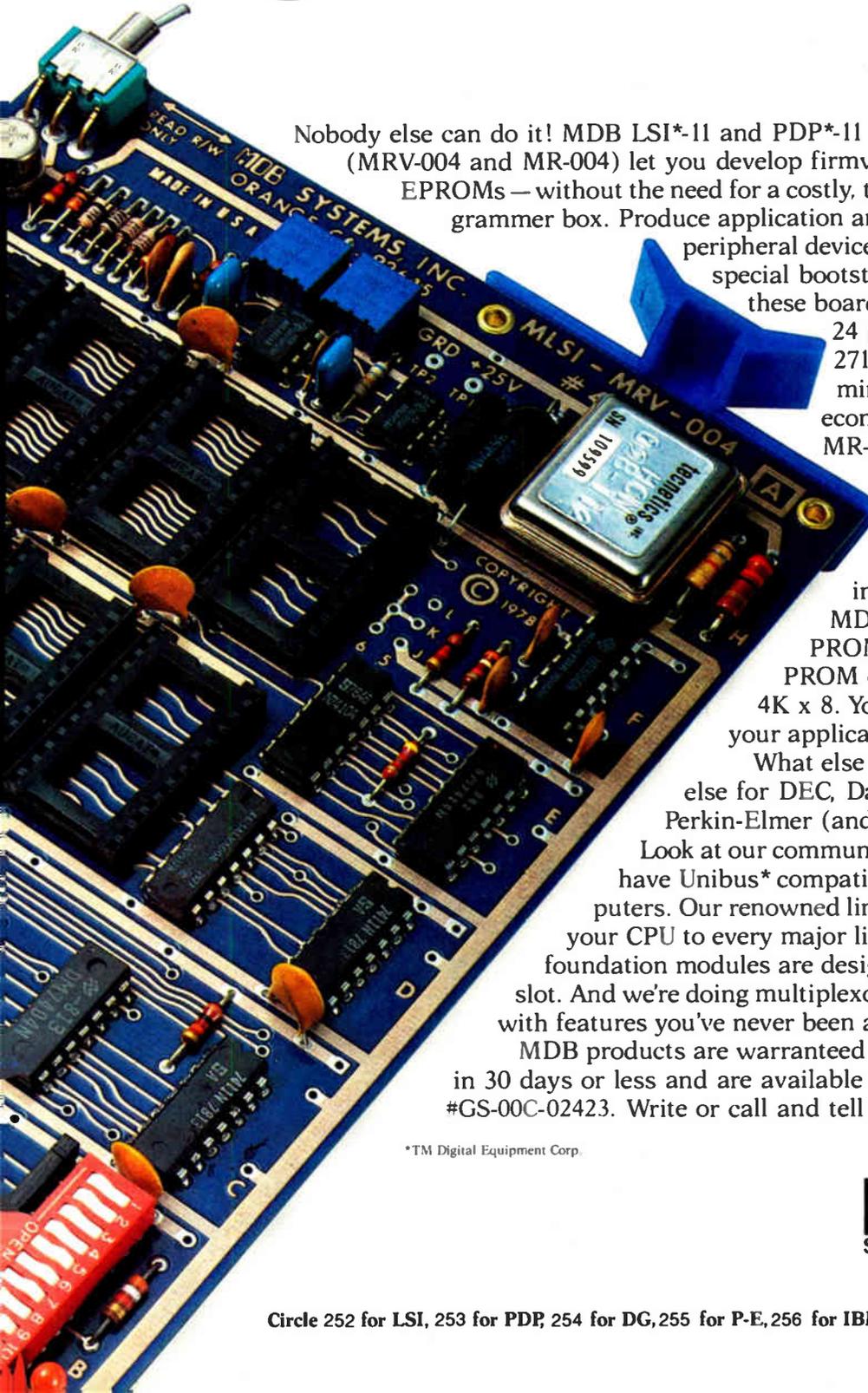
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Circle 252 for LSI, 253 for PDP, 254 for DG, 255 for P-E, 256 for IBM.

New products

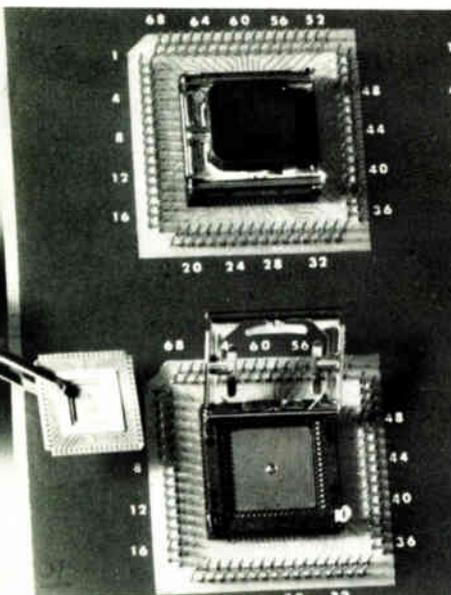
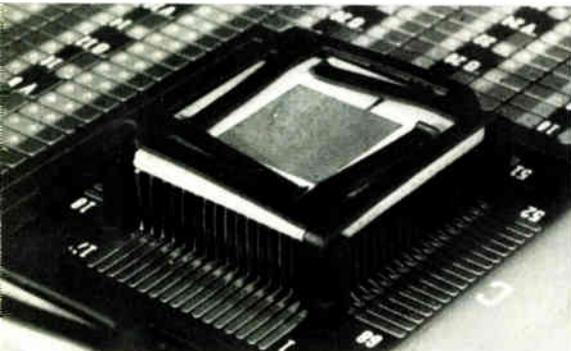
Packaging & production

Chip-carriers get choice of sockets

Two firms develop connectors for surface attachment of chips to pc boards

Until a method is developed for soldering large chip-carriers to printed-circuit boards, either sockets or small leaded motherboards will have to accommodate these packages. AMP has been the sole supplier of sockets for leadless chip-carriers, but now two other firms have entered the

Density. Two companies are offering new lines of sockets for leadless chip-carriers: Augat and Methode Electronics (bottom).



field: Methode Electronics and Augat.

Methode's entry is a series of lid-ded polyphenylene sulfide sockets with gold-plated beryllium-copper contacts. There are two versions: a surface-mount socket held in place by a screw plate that allows variation of board thicknesses, and a solderable type held to the board by soldering contact tails. Contacts numbering 28, 44, 52, 68, 84, 100, 124, or 156 per socket are spaced on 50-mil centers. The sockets accommodate a lead frame that is a maximum of 70 mils thick.

Methode is making available an evaluation board with four 68-contact sockets and a board with six printed input/output patterns and 0.025-in.-square wrapped-wire terminals. The kit is priced at \$375; in production quantities (50,000 units or more), 68-pin sockets will cost about \$3.50 each. The company is now in limited production with deliveries in three to four weeks.

Augat's socket uses a novel spring-clip cover to hold the leadless chip-carrier. Called Loc-Mite—for lockable chip-carrier miniature interconnector, top entry—it comes in 52- and 68-contact configurations. Tin-lead-plated feet allow easy soldering to or through boards; the open design permits probing and efficient cooling. Quantity prices vary (with materials) from \$1 to \$10.

Methode Electronics Inc., 7447 W. Wilson Ave., Chicago, Ill. 60656. Phone (312) 867-9600 [391]

Augat Inc., Interconnection Components Division, 33 Perry Ave., P. O. Box 779, Attleboro, Mass. 021703. Phone (617)222-2202 [392]

Jedec type A packages get elastomeric connectors

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*Part number describes component/connector assembly

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Contact Spectronics for more information at 830 East Arapaho Road, Richardson, Texas 75081. Telephone (214) 234-4271.



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Circle 221 on reader service card

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We've developed workable wire, cable and cord answers for a lot of extraordinary new products. In fact, a lot of designers have found that working with Belden in the early stages of a design project usually pays dividends in compatibility, workability and lower overall costs.

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problems to help insure that your idea makes it to market economically.

You see, Belden's capabilities in wire, cable and cord are comprehensive. Sure, we make thousands of standards, but we can also provide just about any custom that you can imagine. And our technical knowhow ranges from innovative packaging to in-depth value analysis.

Just imagine a wire, cable or cord—and we'll come through with it. Belden Corporation, Electronic Division, P.O. Box 1980, Richmond, IN 47374; 317-983-5200. Out West, contact our Regional Sales Office in Irvine, CA at 714-833-7700.

8-7-9C

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what we
can do
for you*

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Coming through...

with new ideas for moving electrical energy

Circle 222 on reader service card

New products

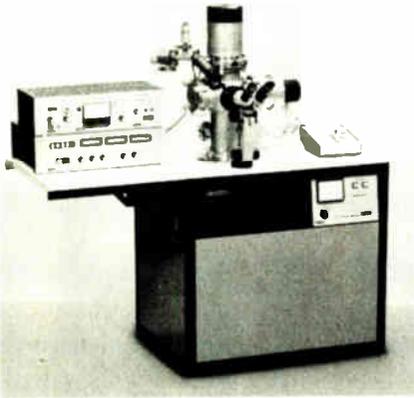
and laminated to the silicone substrate. They are self-aligning, allowing their use in automatic positioning systems and connection with zero insertion force.

The connectors are available in lots of 10,000 units for 25¢ each with nickel pads and 35¢ each with pads consisting of copper, nickel, and gold. Connector resistance using nickel is 0.1 Ω , and with copper-nickel-gold composition, it is 25 to 30 m Ω .

Hulltronics Inc., 333 Byberry Rd., Hatboro, Pa. 19040. Phone (215) 672-0787 [393]

Ion-beam etcher mills surfaces to under 0.5 μm

An ion-beam etching instrument enables milling of surfaces to depths of less than 0.5 μm for scanning electron microscopy and other materials studies. The model IEU 100 etcher uses positively charged rare-gas ions produced by glow discharge that are focused and accelerated by an electrostatic lens. The instrument ceases etching operations automatically if any specimen being milled gets

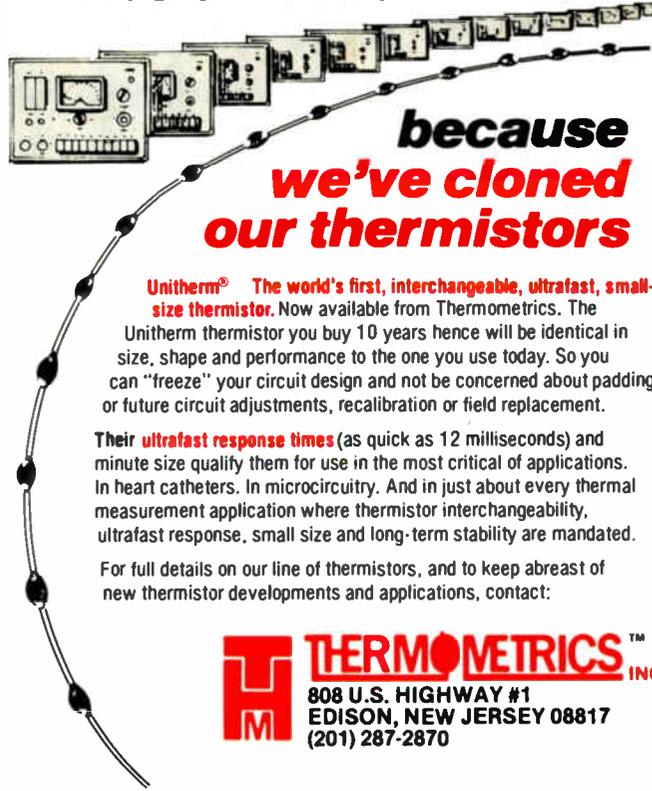


punctured.

Energy and diameter ranges for the ion beam are 2 to 6 keV and 1 to 25 mm, respectively, with current density fluctuations smaller than 5% across the beam diameter.

The IEU 100 includes a 30 \times binocular microscope and a motor-driven cross table. It can be joined to a mass spectrometer for analyses of sample composition. Prices have not

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(201) 287-2870

Circle 223 on reader service card

"SURGE FREE"

SURGE ABSORBABLE DISCHARGE TUBE (FOR CIRCUIT PROTECTION)

● POINT

- (1) Usable at wider ambient condition, especially good under high humidity
- (2) Visibility for operation
- (3) Compact and easy assembly
- (4) Stable characteristics

● APPLICATION

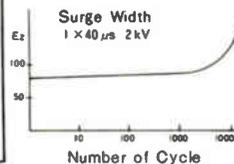
- Computer circuit
- Communication equipment
- Home Appliance
- Aircraft and Automobiles

● TYPE

| Type | Discharge starting Voltage (VDC) | Tolerance | Insulation Resistance (Ω) | Discharge Current (A) |
|--------|----------------------------------|--------------|------------------------------------|-----------------------|
| SA-80 | 80 | $\pm 10\%$ | 10^{10} min | 2,000 |
| SA-140 | 140 | $\pm 10\%$ | 10^{10} min | 2,000 |
| SA-200 | 200 | $\pm 10\%$ | 10^{10} min | 2,000 |
| SA-250 | 250 | $\pm 10\%$ | 10^{10} min | 2,000 |
| SA-300 | 300 | $\pm 10\%$ | 10^{10} min | 2,000 |
| SA-350 | 350 | $\pm 10\%$ | 10^{10} min | 2,000 |
| SA-7 K | 7,000 | $\pm 1,000V$ | 10^{10} min | 2,000 |
| SA-8 K | 8,000 | $\pm 1,000V$ | 10^{10} min | 2,000 |
| SA-10K | 10,000 | $\pm 1,000V$ | 10^{10} min | 2,000 |

Change of Ez by cycling discharge

(case) SA-80



● MAIN PRODUCT

NEON GLOW LAMP, XENON FLASH LAMP, RARE GAS, DISCHARGE LAMP, MINIATURE : BLACK-LIGHT, UV-LIGHT, FLUORESCENT COLOR-LIGHT.

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New products

been quoted on the system.

Balzars Corp., 8 Sagamore Park Rd., Hudson, N. H. 03051 [394]

Assembler places chips within $\pm 10 \mu\text{m}$ on X and Y axes

The head design of a microprocessor-controlled assembly machine permits placement of devices to within $\pm 10 \mu\text{m}$ in the X and Y axes on thick- and thin-film substrates. The HBA 1-NC features a probe head with device-centering jaws in both axes. The pressure exerted by the probe on components being placed is programmable. Some 2,000 to 12,000 devices per hour can be fed to the machine from vibratory feeders, tape carriers, and wafer magazines.

The unit's microprocessor control has a basic 4-K-byte memory that can be expanded in 4-K-byte steps. An RS-232 connection is available for the built-in cassette recorder.

Since the product is imported from Zevatech AG in Solothurn, Switzerland, pricing is relative to the Swiss franc. A basic HBA 1-NC sells for 109,800 Swiss francs, or under \$65,000 at the current rate.

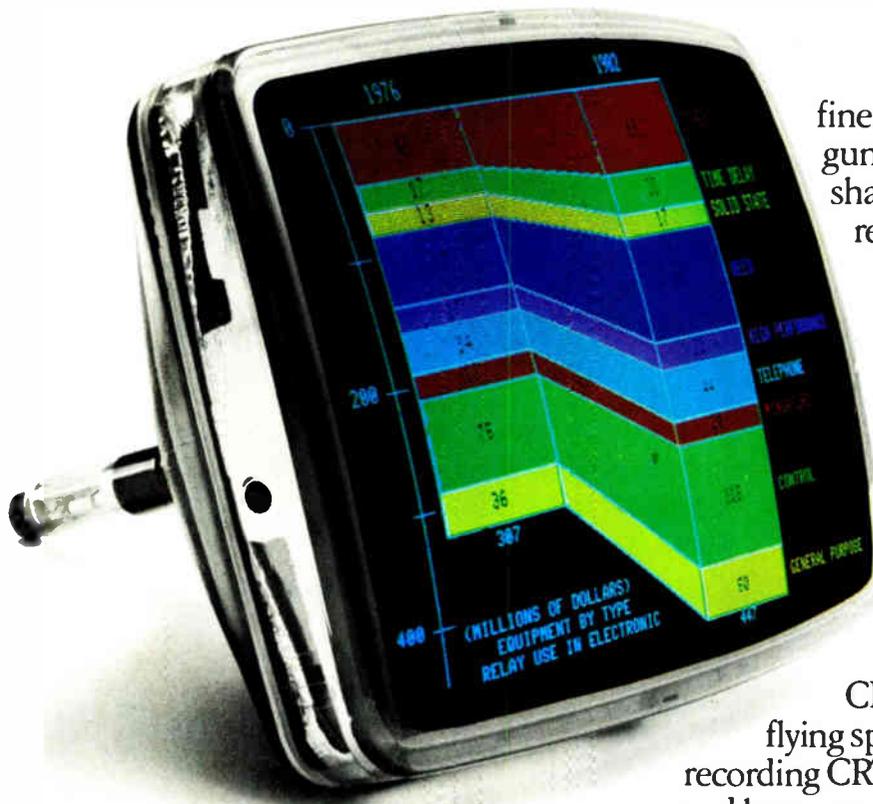
Gardiner Solder Co., 4820 S. Campbell Ave., Chicago, Ill. 60632 [395]

Static-free dispenser accepts any standard 2- to 64-pin IC

The MDD series of dual-in-line-packaged integrated-circuit dispensers for MOS, complementary-MOS, and other devices accept any standard IC shipping tube and can accommodate any standard chip with 2 to 64 pins and 0.300-, 0.400-, or 0.600-in. spacing. The dispenser is made of conductive carbon-filled thermoplastic with steel supports. A grounding lug is included. The MDD series includes 1-, 5-, and 10-channel versions priced at \$21.85, \$83.43, and \$160.45, respectively. Delivery is from stock.

O. K. Machine and Tool Corp., 3455 Conner St., Bronx, N. Y. 10475 [396]

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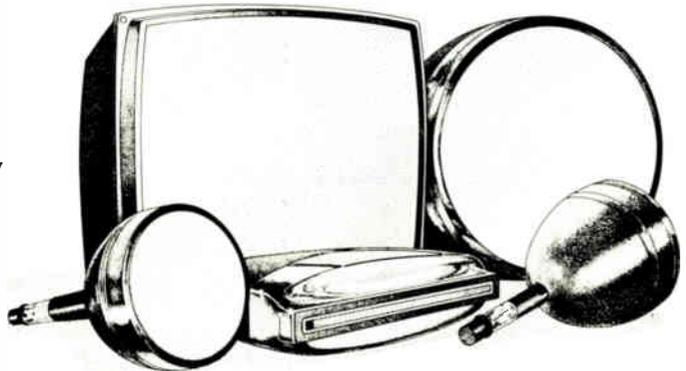
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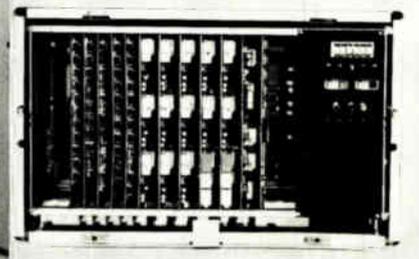
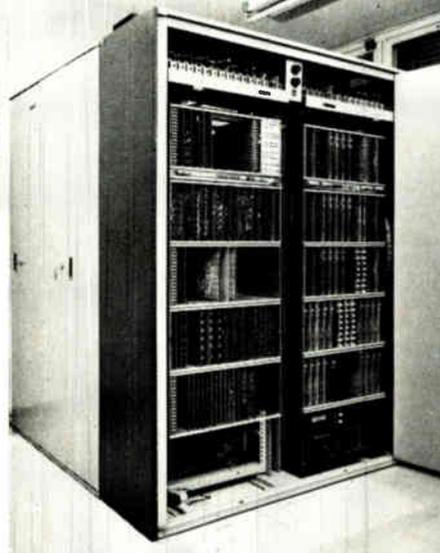
For more information on a display that's worthy of your data system, call our Display Products Group at (213) 979-6055 (or in New Jersey, call (201) 753-1600) or write Mitsubishi Electronics of America, Inc., 2200 W. Artesia Blvd., Compton, CA 90220.

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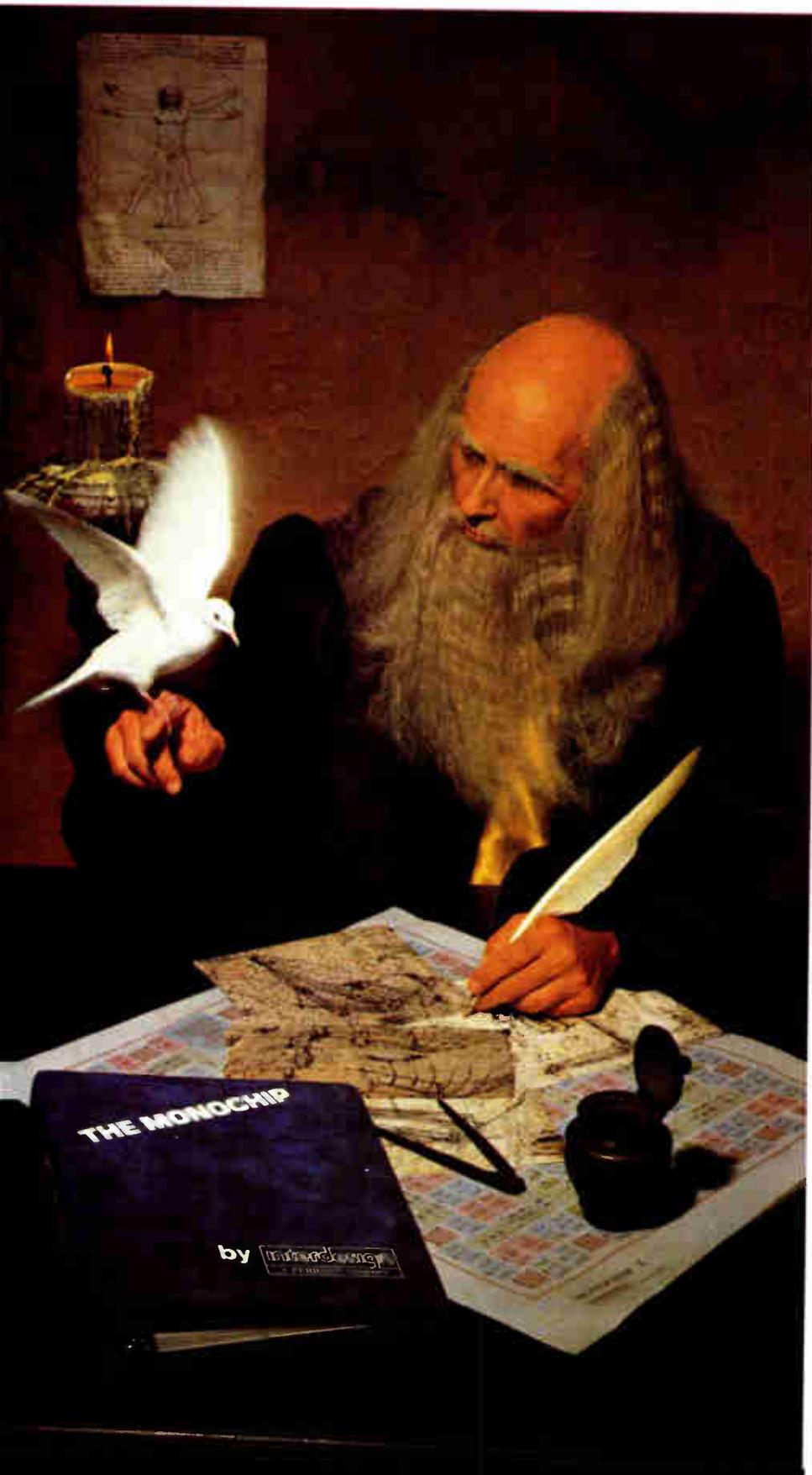
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Iskra

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Circle 227 on reader service card

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New products/materials

A substrate material with a high-dielectric constant of 10.2, Epsilam-10 is designed for microwave applications at the L-, S-, C-, and X-band frequencies. For use in microstrip and strip-line designs, it is made from a ceramic-filled Teflon compound that combines the physical properties of a plastic with electrical properties similar to those of alumina and conforms easily to a variety of shapes. The substrate material reduces the amount of water absorbed to 0.05%. This results in a reduced dielectric loss and prevents loss of gold plating.

Epsilam-10 comes in a standard 9-by-9-in. sheet size, permitting multiple circuit layout and processing with typical resists and etchants. Available with 0.010-, 0.025-, 0.050-, 0.075-, and 0.100-mil thicknesses, the material can be easily machined, drilled, or routed and can be cut with shears or a razor.

3M, P. O. Box 33600, St. Paul, Minn. 55133. Phone (612) 733-9214 [476]

A conductive polyimide silver paste, EPO-TEK P-10 is designed for chip bonding in microelectronic and optoelectronic applications. For use in Cerdip packages, transfer molding, or thermocompression operations, it has a high thermal conductivity of 17.1 BTU/in./ft²/h/°F, a high electrical conductivity of 0.00006 to 0.00007 Ω-cm, and a high glass transition temperature of 235°C. The soft thixotropic paste, applied by screen printing, stamping techniques, or machine dispensing equipment, can be cured at 150°C in one hour.

EPO-TEK P-10 does not bleed out and has a shelf life of at least six months when stored at room temperature in tightly closed containers. Refrigeration is not required.

Epoxy Technology Inc., 14 Fortune Dr., P. O. Box 567, Billerica, Mass. 01821. Phone (617) 667-3805 [477]

A water-soluble foaming flux, Hydro-X, made for high-speed wave-soldering systems, operates at high speeds for aqueous cleaning systems and leaves low levels of ionic contaminants, says the manufacturer. It

provides icicle- and web-free joints when soldering on badly tarnished boards. Hydrox-X, available in concentrations of 10%, 20%, and 40%, can be applied with a foam fluxer. The lowest concentration of 10% is used for single-sided printed-circuit boards. Highly tarnished surfaces and component leads, as well as multilayer boards or double-sided plated through-holes, need the higher concentrations of 20% or 40%.

Multicore Solders, Westbury, N. Y. 11590 [478]

An alumina-based adhesive, Cerama-Dip 538 is used as an end-seal material for cartridge heaters and other high-temperature devices such as feed-throughs and thermocouples. The thixotropic material, which can be injected, brushed, or dipped, will cure at 180°F and is usable to 3,200°F. It has a thermal expansion coefficient of 14×10^{-6} in./in./°F, higher than most metals, such as stainless steel or copper.

Cerama-Dip 538 is available from stock at \$40 per quart. A thinner, 538-T, is offered at \$20 per quart.

Aremco Products Inc., P. O. Box 429, Ossining, N. Y. 10562. Phone (914) 762-0685 [479]

A potent chemical stripper, De Poxy is designed to remove tough epoxies and polyurethane paints, glues, foams, resins, and finishes. The formulation contains no benzenes, creosotes, phenols, alcohols, or chlorinated or fluorinated hydrocarbons. De Poxy will dissolve many plastics with the exception of polyethylene, polypropylene, and Teflon; therefore, it should be used in glass, Teflon, high-quality stainless steel, monel, or titanium receptacles. Working more efficiently at high temperature, De Poxy should be heated to 120° to 130°C. The coated substrate should be dipped into the solvent until the coating dissolves and then removed. Any remaining De Poxy should be washed off.

De Poxy is available in pint, gallon, or drum containers.

Atomergic Chemetals Corp., 100 Fairchild Ave., Plainview, N. Y. 11803. Phone (516) 349-8800 [480]

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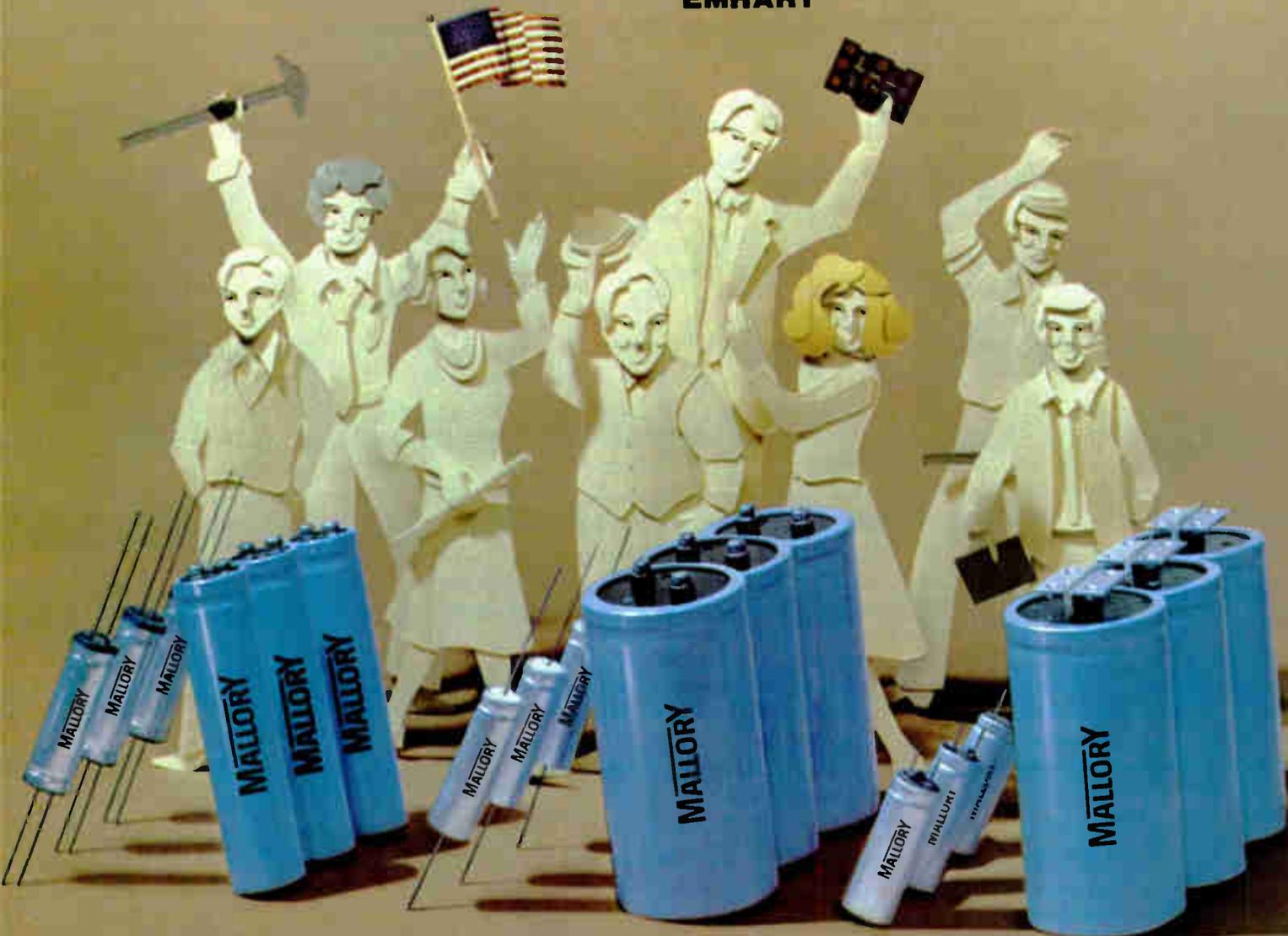
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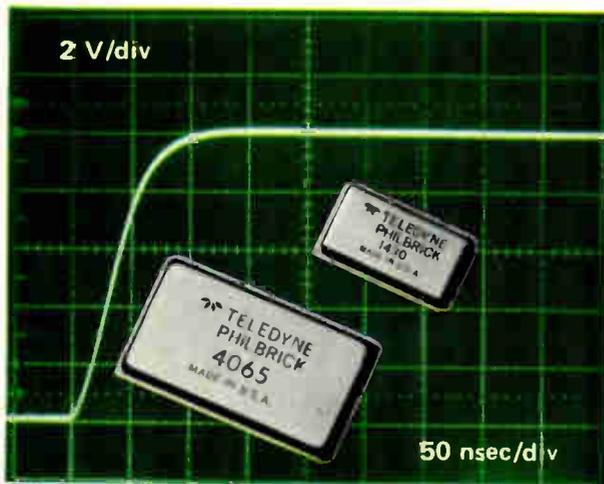
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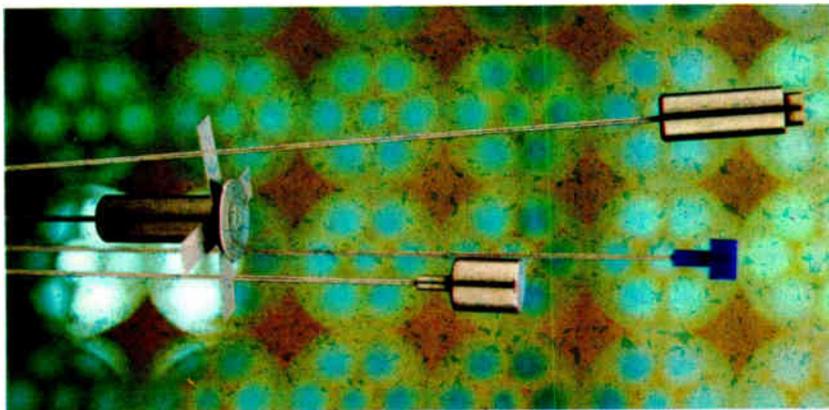
230 Circle 230 on reader service card

Electronics / December 4, 1980

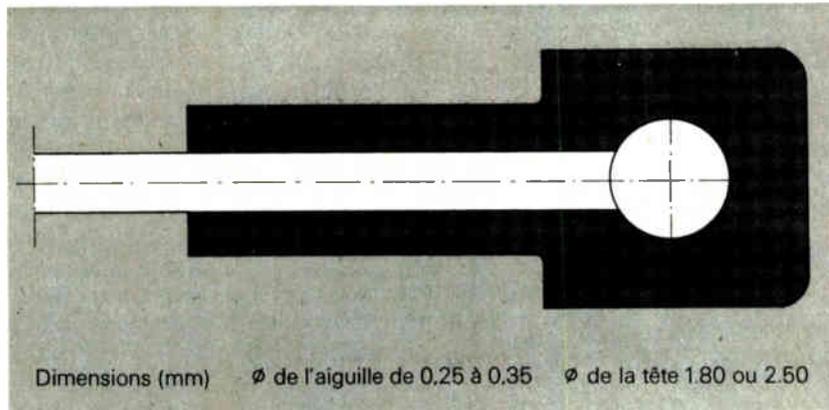
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Circle 231 on reader service card

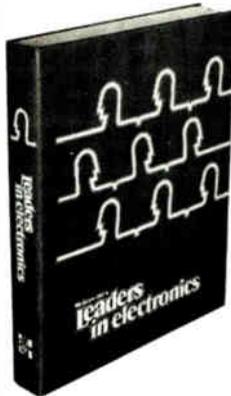
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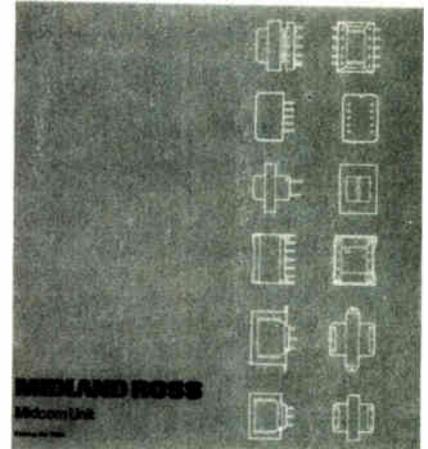
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New literature

Audio transformers. Information on products such as couplers, repeater coils, hybrids, and inductors is available in a 24-page catalog from the Midcom Unit of Midland-Ross Corp. "Transformers for Telecom-

Transformers for Telecommunications



munications" explains the terminology and methods of testing for audio transformers and includes an electromechanical design outline that can be used to request design proposals that meet the end user's specifications. For a copy of the catalog, write to Midland-Ross Corp., Midcom Unit, 1650 Tower Blvd., North Mankato, Minn. 56001. Phone (507) 625-6521. Circle reader service number 421.

Audio digital-to-analog converters. The MP1926 high-speed 16-bit digital-to-analog converter and the MP201A audio distortion suppressor, used for reconstructing audio signals from digital data with virtually no distortion, are discussed in two data sheets from Analogic Corp. Besides listing product specifications and performance features, the bulletins describe code selection, operation, and typical applications. Block diagrams and graphs for the converter and the distortion suppressor are included with their respective data sheets. Analogic Corp., Audubon Road, Wakefield, Mass. 01880. Phone (617) 246-0300 (422)

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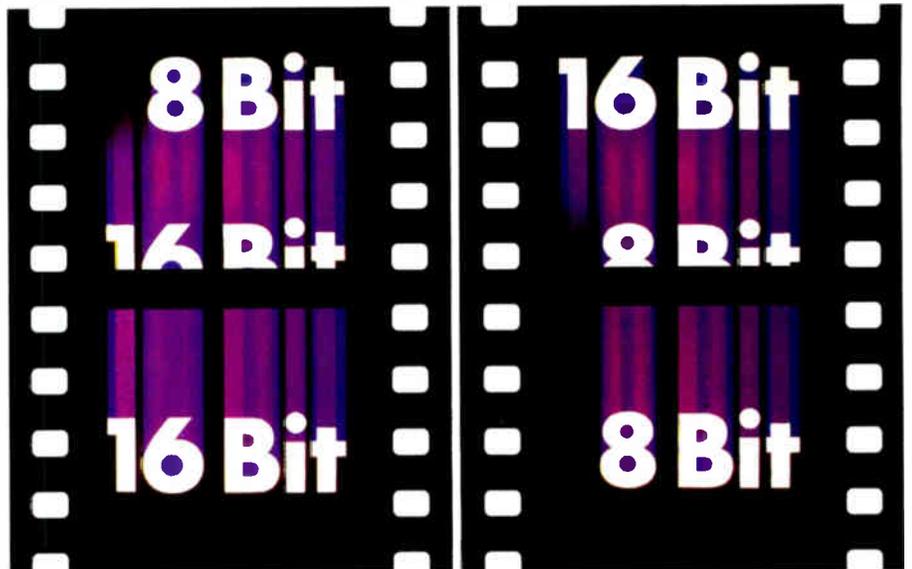
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Products Newsletter

National uses advanced C-MOS in a-d converters . . .

National Semiconductor Corp., Santa Clara, Calif., is applying an advanced complementary-MOS process, which **makes use of silicon-chromium thin-film technology**, to analog-to-digital converters it will unveil in the first half of 1981. Among the entries are the Naked-10, a high-accuracy 10-bit a-d unit, and a new version of the 8-bit Naked-8, upgraded to convert in 25 μ s and to include a programmable multiplexer. Also coming is a two-channel 8-bit control-oriented processor (COP-8) in an 8-lead miniature dual in-line package, plus 14- and 20-lead versions with a multiplexer option. The 14- and 20-lead COP-8s (ADC0833 and ADC0834, respectively) can access eight single-ended or analog differential signals or any combination that totals eight channels.

. . . and AMD uses its oxide-isolated process for memories

For its part, Advanced Micro Devices Inc.'s Bipolar division, Sunnyvale, Calif., is putting its proprietary oxide-isolated IMOX-II (implanted micro-oxide) technology to work on a wide range of memory and microprocessor chips slated for introduction in 1981. The firm's first 16-bit-slice controller, the Am29116, will be flanked by an interruptible sequencer (Am29112) and a first-in, first-out controller (Am29153). The process will also yield what is expected to be **the industry's first 4-K-by-4-bit (Am27S40/41) and densest 2-K-by-8-bit (Am27S190/91) programmable read-only memories in production**, as well as a 2-K-by-4-bit PROM (Am27S184/85) with a maximum access time of 35 or 50 ns and a 1-K-by-8-bit PROM with registers (Am27S35) for pipelined controllers.

Intel supplies samples of 35-ns 16-K PROM . . .

Intel Corp.'s Special Products division in Santa Clara, Calif., is beginning to offer samples of a very fast version of its 16-K bipolar programmable read-only memory. Organized as 2 K by 8 bits, the 3636B will have a **worst-case access time of 35 ns, or nearly twice as fast as the firm's prior 16-K PROM, the 3636**. It is expected to be available in volume quantities early in the second quarter of 1981.

. . . while Toshiba offers samples of 64-K dynamic RAM

Toshiba America Inc.'s Memory and Microprocessor division in Irvine, Calif., has begun to provide samples of the TMM4164C 64-K dynamic random-access memory. Fabricated using Toshiba's double-polysilicon n-channel silicon-gate technology, two versions of the 1-bit-wide RAM have worst-case access times of 120 or 150 ns. The chip, operating from a single +5-V power supply, dissipates a maximum of 250 mW when active and 20 mW in the standby mode. **Production quantities will be available in the first quarter of 1981.**

Standards come to STD bus, yielding new market strength

Getting diverse microprocessors and data-acquisition subsystems to play together could be easier now that a set of standardized protocols, voltage levels, and physical dimensions for the STD bus has been put together by a team of industry representatives and Prolog Corp. of Monterey, Calif., developer of the bus. First evidence of results may be **the introduction late this year or early next of a line of almost 60 data-acquisition modules** from Data Translation Inc., Marlboro, Mass. Spokesmen for the firm say that original-equipment manufacturers using a variety of microprocessors will now have to add only an STD processor and a peripheral controller card to the appropriate data-acquisition subsystem card.

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The Cyclotron Institute at Texas A&M University will have a position open in the near future for an Assistant Research Engineer. This position requires a person with at least a B.S. degree in Electrical Engineering with emphasis on digital electronics. The successful applicant will be expected to design, construct and/or supervise the construction of digital instruments as required to support our continuing research in nuclear physics. This individual will also supervise the development and maintenance of realtime data acquisition interfaces to a DEC VAX 11/780 and a DEC PDP-15/40 and coordinate computer maintenance. Experience in the design and layout of printed circuit boards is desirable. Send resumes to: Employment Manager, Personnel Department, Texas A&M University, College Station, TX 77843. EEO/MF.

Career outlook

IEEE members demand a voice

■ According to a recent Institute of Electrical and Electronics Engineers survey, members want more of a say in institute matters. They want to be polled on an on-going basis for their opinions on engineering issues, and they want leadership to take positions on certain controversial topics based on these opinions. Conducted on a biennial basis by the U.S. Activities Board, the survey was sent to more than 12,000 members, with a response rate of 55.7%.

Over two thirds—69.1%—of the responding members want to be polled regularly on current engineering issues to provide on-going guidance for the IEEE leadership. However, only 49.2% believe that the institute often takes the views of the general membership into account in developing and carrying out programs. In fact, 20.6% are not sure, and 27.1% believe the leadership seldom considers members' views.

In developing public statements and positions, only 35.4% of the polled members believed that the IEEE often takes their views into account; 36.1% believe the institute seldom considers their opinions; and almost a quarter—23.4%—are not sure whether their views are considered at all.

Public statements. As a total organization, the IEEE should take definitive stands on issues according to 87.1% of the responding members. Nearly three fourths—74.7%—believe that major boards of the institute such as the USAB and the Technical Activities Board should take a stand, while 55.3% favor sections, technical societies, and committees taking a stand as well.

A whopping 87.9% believe positions should be taken on technical issues with which engineers may be particularly familiar and which may affect the public interest. Over three fourths—77.1%—believe that the institute should also take stands on issues involving the career environment of employed members, and nearly that percentage—74.8%—thinks the IEEE should voice an opinion on issues of importance to indus-



tries employing engineers. Just over two thirds—67.4%—believe the group should emphasize its position on political, social, and economic issues that may have an effect on the electrical engineering profession.

High on the list of important issues for many members are: U.S. technological leadership (87.9%), patent rights for employed inventors (79.5%), age discrimination in the profession (77%), and professional innovation and productivity (76.1%). Low on the list was the requirement to take a stand on the 1934 Communications Act—only 37% believed an opinion should be voiced.

The list of top priority projects that should receive funding include: the promotion of U.S. leadership in electronic technology (33.6%), and the improvement of pension levels for members who change jobs before becoming vested (26.9%).

Heading up the list of projects that should be given high priority are insuring older professionals against discriminatory practices (51.2%) and the establishment of a yearly technological conference with congressional leaders to provide technical advice (45.3%).

Interestingly enough, a good many members give only low priority to projects associated with the Professional Activities Committees: establishment of national workshops for PACs (46.1% rank it low) and promotion of PAC activities at all levels (43.5%).

—Pamela Hamilton

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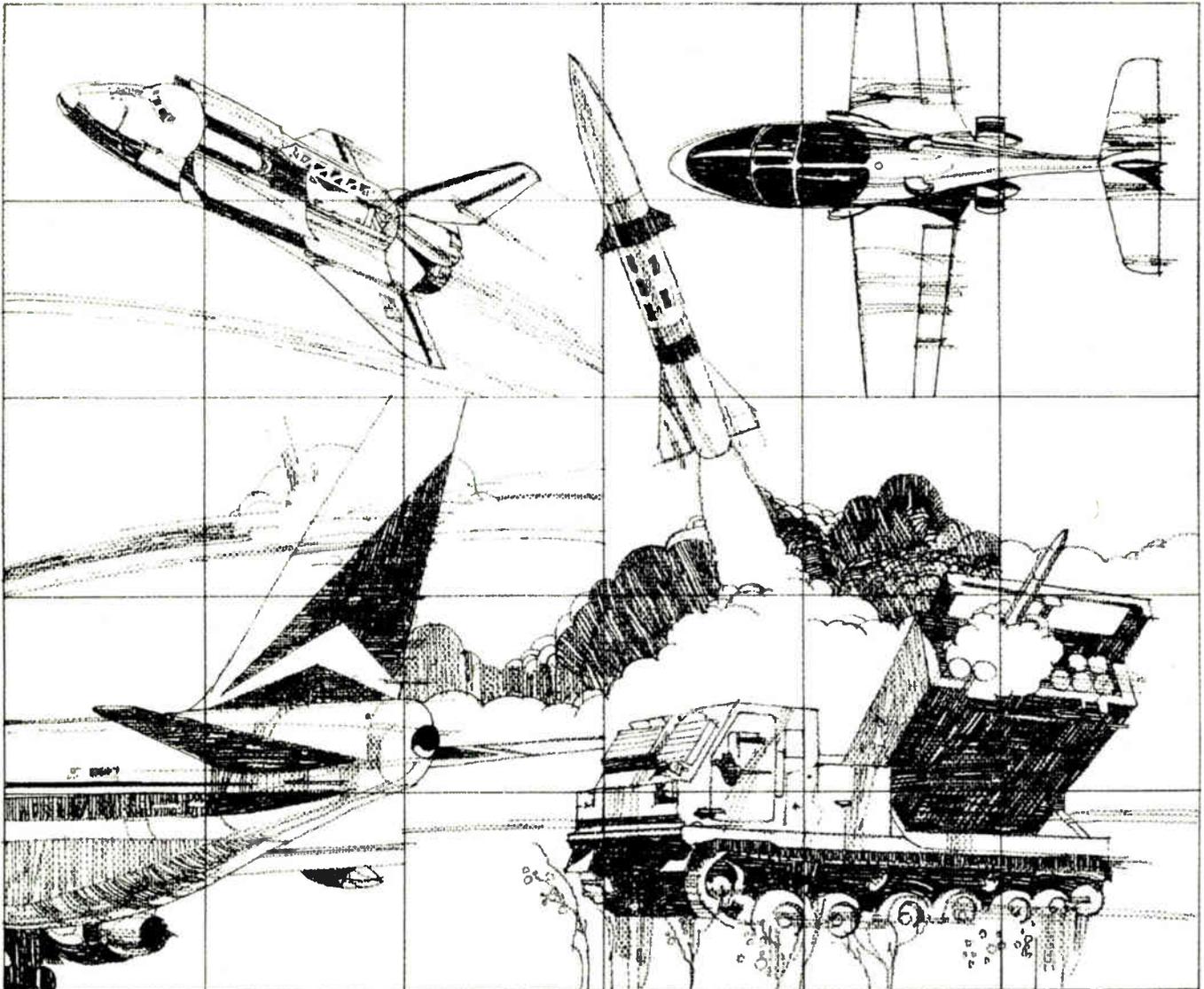
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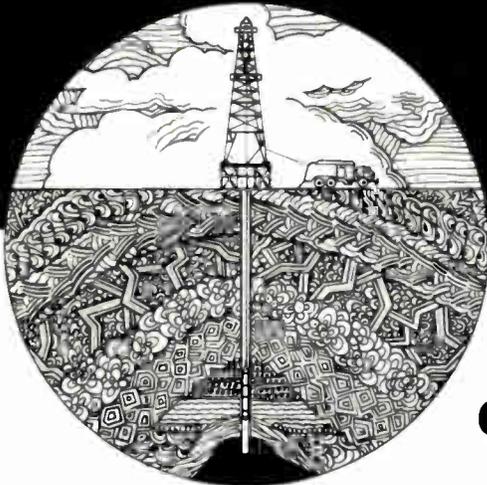
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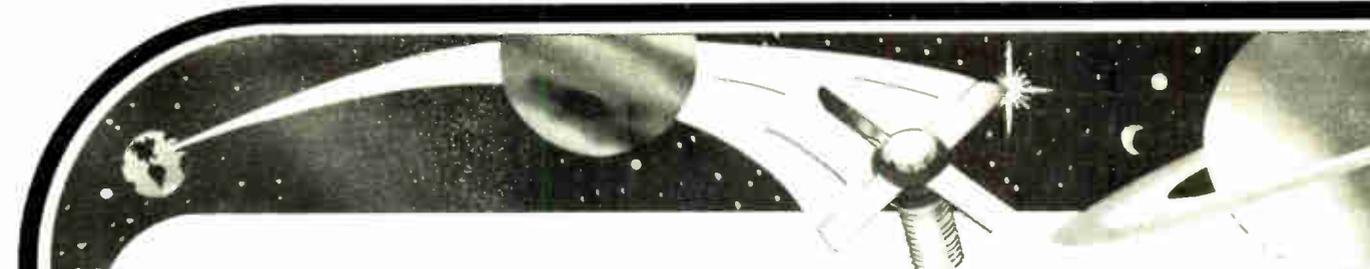
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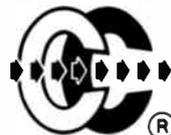
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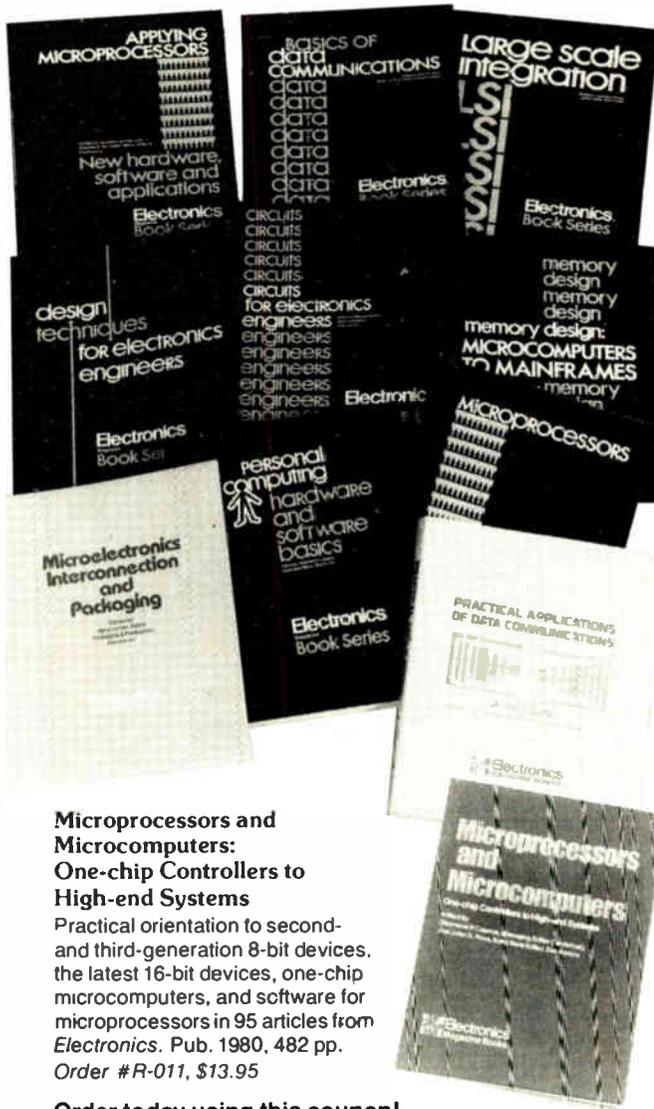
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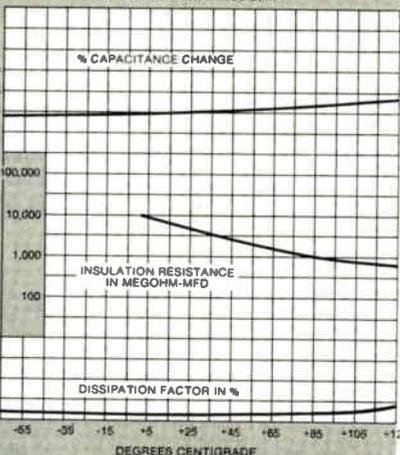
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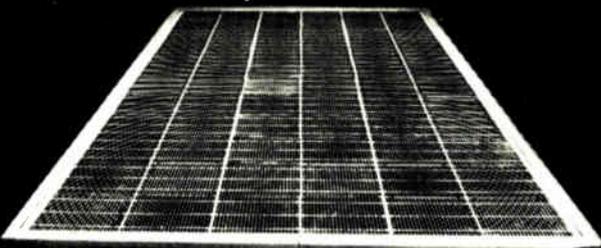
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| 4 19 34 49 | 64 79 94 109 | 124 139 154 169 | 184 199 214 229 | 244 259 274 351 | 366 381 396 411 | 426 441 456 471 | 486 501 706 900 |
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| 12 27 42 57 | 72 87 102 117 | 132 147 162 177 | 192 207 222 237 | 252 267 344 359 | 374 389 404 419 | 434 449 464 479 | 494 509 714 957 |
| 13 28 43 58 | 73 88 103 118 | 133 148 163 178 | 193 208 223 238 | 253 268 345 360 | 375 390 405 420 | 435 450 465 480 | 495 510 715 958 |
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| 2 17 32 47 | 62 77 92 107 | 122 137 152 167 | 182 197 212 227 | 242 257 272 349 | 364 379 394 409 | 424 439 454 469 | 484 499 704 719 |
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| 5 20 35 50 | 65 80 95 110 | 125 140 155 170 | 185 200 215 230 | 245 260 275 352 | 367 382 397 412 | 427 442 457 472 | 487 502 707 901 |
| 6 21 36 51 | 66 81 96 111 | 126 141 156 171 | 186 201 216 231 | 246 261 338 353 | 368 383 398 413 | 428 443 458 473 | 488 503 708 902 |
| 7 22 37 52 | 67 82 97 112 | 127 142 157 172 | 187 202 217 232 | 247 262 339 354 | 369 384 399 414 | 429 444 459 474 | 489 504 709 951 |
| 8 23 38 53 | 68 83 98 113 | 128 143 158 173 | 188 203 218 233 | 248 263 340 355 | 370 385 400 415 | 430 445 460 475 | 490 505 710 952 |
| 9 24 39 54 | 69 84 99 114 | 129 144 159 174 | 189 204 219 234 | 249 264 341 356 | 371 386 401 416 | 431 446 461 476 | 491 506 711 953 |
| 10 25 40 55 | 70 85 100 115 | 130 145 160 175 | 190 205 220 235 | 250 265 342 357 | 372 387 402 417 | 432 447 462 477 | 492 507 712 954 |
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