SUPERCHIPS STEAL SOLID STATE SHOW

WORLD PREMIERE

- SINGLE-CHIP MAINFRAMES
- 4-MB DRAMS
- SIGNAL PROCESSORS
- 4-K GaAs GATE ARRAY

A NEW WAY TO SOLVE THE TEST PROBLEM IN DISK DRIVES/35
IS TOM ANGELUCCI'S BIG GAMBLE FINALLY PAYING OFF?/38
The only thing small about it is its size!

The RTP-650A is the only portable data recorder that gives you bigger performance than a reel-to-reel.

- **DC to 40kHz frequency response on 14 (or 21) channels** — at a 76.2cm/sec (30 ips) on Beta format video cassette tape. Covers twice the IRIG WBG1 bandwidth on any of the other six tape speeds. WBG1 is selectable for an even better SN ratio.

- **Superior vibration resistance (tested in conformity with MIL-STD-810C)** plus a compact and lightweight design give you a wholly new latitude of applications.

- **FM, DR and PCM recording** — three modes in all
  A first for a desktop data recorder.

- **Optionally available GP-IB port** lets you easily configure a computer-controlled data acquisition and processing system.

And it's easier to use than any other data recorder.....

- **Bright easy-to-read menu style EL display** provides the window for easy access to the multi-microprocessor intelligence.

- **Programmable settings for simpler operation**
  Even an unskilled operator can use it on site.

Learn more about the RTP-650A and its many other exciting features. Write or call:

KVOWA.
KYOWA ELECTRONIC INSTRUMENTS CO. LTD
Toranomon 2-chom3, Minato-ku, Tokyo
Phone: 03-502-3551
Cable: KYOWASTRAINGAGE TOKYO
Telex: 222-3854 KYOWAT J

RTP-650A
VIDEO CASSETTE DATA RECORDER
Circle 900 on reader service card
BASICALLY FAST
With Infotek's new compiler, Hewlett-Packard BASIC (for Series 200/300 computers) runs dramatically faster.

Increase productivity and throughput! Now, you can make your 4.0 version of HP BASIC run most programs 3-5 times faster without altering or compromising any of the program attributes. It's done with the BC 204 compiler from Infotek, the company that specializes in making your HP computer even better.

The new Infotek BC 204 compiler is 100 percent compatible with all Series 200/300 computers. All BASIC statements and extensions are supported. Once a program is compiled, the execution is identical to standard interpreted BASIC. Typical performance improvement factors with floating point support are 10-40 for integer statements, 5-10 for real statements, 2-10 for string statements, and 1.5-3 for CRT DRAW statements. The BC 204 supports all floating point hardware configurations including Infotek's floating point processors, HP's math card and the MC 68881 microprocessor (internal to Model 320). Infotek also manufactures compilers for the BASIC 2.0 and 3.0 operating systems.

And you can make your HP better yet with another innovative Infotek product, the Matrix Binary (MB 203) software package which increases the speed of MAT operations from 1.5-3 times.
So make your HP system BASICally fast. Call Infotek Systems today for information on BC 204 and our other enhancement products for the HP 9000 Series 200/300 computers. Infotek Systems, 1400 North Baxter Street, Anaheim, California 92806-1201, (714) 956-9300, (800) 227-0218, in California (800) 523-1682, TELEX 182283.

INFOTEK SYSTEMS
A DIVISION OF ALI CORPORATION

Circle 1 on reader service card

World Radio History
SILICON SYSTEMS’ NEW
READ DATA PROCESSOR CHIP BREAKS
THE PRICE/PERFORMANCE BARRIER

MFM and RLL Capability at Data Rates
up to 15 Mbits/sec
Now Silicon Systems introduces the SSI 541—the industry’s most advanced Read Data Processor chip for high performance disk drive applications. Its high level integration allows it to perform both amplitude and time pulse qualification for MFM and RLL encoded systems—and do it all at data rates up to 15 megabits per second.

Complete Integration of High Performance Functions
Packed inside of the 541 are all these high performance functions: a wide dynamic range AGC amplifier, a dual rate AGC charge pump, an active differentiator, an adjustable hysteresis comparator, a feed-forward hysteresis control circuit, and a gating circuit with output width control. By utilizing amplitude and time pulse qualification, the 541 is able to gate out shouldering induced noise errors in a high resolution disk drive system.

Costs Less to Buy, Less to Apply—Reducing the User’s Part-Count and Size
The 541’s complete integration of the read data processor functions cuts down on the user’s part-count and manufacturing costs, while boosting reliability and saving real estate. Even with its high performance and cost-saving benefits, the 541 costs less when you buy it and far less when you apply it.

The SSI 541 is designed for application in high performance MFM and RLL encoded disk drives, disk drives that utilize plated media or thin film heads, and disk drives that offer advanced interface standards.

Price and Availability
Silicon Systems also offers a very low cost sister chip to the 541. It is the SSI 540 with a time domain filter that makes it an optimum solution for low cost, low resolution systems. Both devices are available in production volumes now. In OEM production quantities, the SSI 541 is priced under $10, and the SSI 540 is priced under $5.

For complete product information, call us now, or send for more information.

Silicon Systems, 14351 Myford Road, Tustin, CA 92680. (714) 731-7110, Ext. 575.

Circle 2 for Product Information
Circle 35 for Careers Information
<table>
<thead>
<tr>
<th>Newsletters</th>
<th>INSIDE TECHNOLOGY</th>
<th>NEW PRODUCTS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology, 9</strong></td>
<td>Solving the test problem in SCSI disk drives, 35</td>
<td>Newsletter, 13</td>
</tr>
<tr>
<td>• Now it's Fairchild that's joining the BiCMOS camp</td>
<td>Flexstar's tester correlates information from a disk drive's data path, thereby overcoming a major problem with the Small Computer System Interface protocol: difficult access to critical test points</td>
<td>• Apollo launches a volley of new products</td>
</tr>
<tr>
<td>• Pixel count of solid-state CCD sensor approaches that of tubes</td>
<td>Is Tom Angelucci's big gamble finally paying off? 38</td>
<td>• Ferranti to provide 18-V CMOS gate arrays</td>
</tr>
<tr>
<td>• Intel's Bitbus standard gets a boost from makers of factory-automation gear</td>
<td>Chips with 100 leads or more need tape automated bonding as an assembly and interconnection method—good news for Tom Angelucci, who has been pushing TAB for 15 years</td>
<td>• Aida's work station aims at design analysis and testing</td>
</tr>
<tr>
<td><strong>Electronics, 11</strong></td>
<td>PROBING THE NEWS</td>
<td>Communications, 53</td>
</tr>
<tr>
<td>• Sony and AMD may be swapping devices soon</td>
<td>Are EEPROMs finally ready to take off? 40</td>
<td>Here comes a one-chip modem that Silicon Systems claims it is set to ship</td>
</tr>
<tr>
<td>• Chip bookings surpass shipments for first time since 1984</td>
<td>Greater availability, higher densities, and steadily dropping prices may mean that the market for EEPROMs will start its long-predicted climb</td>
<td>Instruments, 54</td>
</tr>
<tr>
<td>• The slide in Japan has stopped, IBM says</td>
<td>Automated meter reading starts to make sense, 42</td>
<td>Tektronix' portable scope can show events as short as 1 ns</td>
</tr>
<tr>
<td><strong>ICs, 14</strong></td>
<td>COVER</td>
<td>CAD, 54</td>
</tr>
<tr>
<td>• Fujitsu pushes HEMT devices into LSI-level logic</td>
<td>Special report: Superchips steal solid-state show, 23</td>
<td>Now IBM PCs can simulate or model over Cadnetix' Ethernet CAE system</td>
</tr>
<tr>
<td>• Two new ways to increase chip utilization</td>
<td>This week's International Solid State Circuits Conference will be the debut for some spectacular superchips that push the upper limits of density and speed. This special report provides first details of these important developments, including:</td>
<td>Memories, 56</td>
</tr>
<tr>
<td>• Behind the density push: solid work on mundane matters</td>
<td>• Mainframe ICs that shrink big systems</td>
<td>AMD's 256-K DRAM can be accessed in three ways</td>
</tr>
<tr>
<td><strong>Computers, 15</strong></td>
<td><strong>Electronics index, 49</strong></td>
<td><strong>People, 50</strong></td>
</tr>
<tr>
<td>NEC's latest CPU keeps Honeywell's mainframe line going</td>
<td></td>
<td>• An aggressive risk-taker follows Oshman at Rolm</td>
</tr>
<tr>
<td><strong>Telecom, 16</strong></td>
<td><strong>Companies, 44</strong></td>
<td>• How Japan's Ascii is dealing with the loss of Microsoft</td>
</tr>
<tr>
<td>• Will AT&amp;T deal help French industry?</td>
<td>• General Computer girds for another battle</td>
<td>Bottom lines, 46</td>
</tr>
<tr>
<td>• Forging a network of European alliances helps AT&amp;T rebuild its base</td>
<td>• How Japan's Ascii is dealing with the loss of Microsoft</td>
<td>TI plans $225 million stock offering</td>
</tr>
<tr>
<td>• The FCC enhanced-services proposal stirs debate</td>
<td><strong>Medical, 19</strong></td>
<td>Electronics index, 49</td>
</tr>
<tr>
<td><strong>Fabrication, 18</strong></td>
<td>Speeding up NMR imaging to watch a kidney work</td>
<td></td>
</tr>
<tr>
<td>Laser may simplify thin-film growth</td>
<td><strong>Networking, 21</strong></td>
<td>• Moore takes his knack to Kontron Electronics</td>
</tr>
<tr>
<td><strong>Medical, 19</strong></td>
<td>Power-line LAN comes without rfI problems</td>
<td><strong>Textrnx cofounder Vollum dies at 72</strong></td>
</tr>
<tr>
<td>Speeding up NMR imaging to watch a kidney work</td>
<td><strong>Microsystems, 20</strong></td>
<td>• People on the move</td>
</tr>
<tr>
<td>Backup keeps microprocessor-based equipment working</td>
<td></td>
<td><strong>New literature, 60</strong></td>
</tr>
<tr>
<td><strong>Networking, 21</strong></td>
<td><strong>Special report: Superchips steal solid-state show, 23</strong></td>
<td><strong>Meetings, 62</strong></td>
</tr>
<tr>
<td>Power-line LAN comes without rfI problems</td>
<td>This week's International Solid State Circuits Conference will be the debut for some spectacular superchips that push the upper limits of density and speed. This special report provides first details of these important developments, including:</td>
<td><strong>Electronics week, 64</strong></td>
</tr>
<tr>
<td></td>
<td>• Mainframe ICs that shrink big systems</td>
<td>• National Semiconductor and Xerox set joint deal</td>
</tr>
<tr>
<td></td>
<td>• DSPs that handle images, run motors</td>
<td>• Computervision names new president</td>
</tr>
</tbody>
</table>
Sometimes it’s hard to go back for a scope!

60-MHz full-function field-service Attache Case Oscilloscope is so light and small it will be taken everywhere, every time.

LBO-325 packs all the power and performance of a cumbersome, backbreaking, 60-MHz workbench oscilloscope into an easy-to-carry, ultracompact, featherweight unit. Although its 3½-inch CRT is as big and clear as screens on large field-service scopes—LBO-325 weighs only 9 lbs. So it won’t weigh field-technicians down, no matter how far afield they go! LBO-325 is so small it fits inside a 3-inch deep attache case with room to spare for a multimeter, service manuals and some tools. The ideal full-function scope for a cramped work area or crowded bench.

Outperforms all other portables:
- 60 MHz • Dual channel • ALT TIME BASE simultaneously displays main waveform and any expanded portion • ALT TRIG for stable display of 2 asynchronous signals • Bright, sharp 12-kV trace • Large 3½-inch PDA CRT • Illuminated graticule • Comprehensive triggering • TV-V and TV-H sync separators • Variable trigger hold-off • Delay line shows sharp leading edges • CH-1 output drives low-sensitivity instruments • Measures only 3 x 9 x 11⅝ inches • Weighs 9 lbs.

Two-year warranty.
Built tough to provide long use, LBO-325 is backed by Leader’s 30-year reputation for reliability and by factory service depots on both coasts.

Reduces the cost of service calls.
Time is money. A scope left in the vehicle takes time to retrieve. One kept in the shop causes repeat service calls. The LBO-325

Attache Case Oscilloscope is so easy to carry and use, techs will take it everywhere, every time. And the time saved translates into extra profits for years to come.

LBO-325 CRT is shown actual size.

Call toll-free
(800) 645-5104
In NY State
(516) 231-6900

Request an evaluation sample, our latest Test Instrument Catalog with over 100 outstanding products, the name and address of your nearest “Select” Leader Distributor, or additional information.

For professionals who know the difference.

LEADER Instruments Corporation
380 Osler Avenue
Hauppauge, New York 11788
Regional Offices: Chicago, Dallas, Los Angeles, Boston, Atlanta
In Canada call Omnitronix Ltd.
(514) 337-9500
Covers a meeting as important as the International Solid State Circuits Conference calls for extraordinary editorial teamwork involving editors on both U.S. coasts as well as overseas. That, in a nutshell, is the story behind our ISSCC Special Report that starts on p. 23 of this issue.

But that bare outline doesn’t do justice to the hours of toil involved. The effort was coordinated by Sam Weber, our technical executive editor, and involved much hard work by solid-state editor Bernie Cole in Palo Alto and Tokyo bureau manager Charlie Cohen in Japan.

The action started last December at the International Electronic Device Meeting in Washington, where Bernie met with ISSCC chairman Alan Grebene and organizer Louis Winner to go over the program and get early indications of the important developments to be featured at the conference. The preliminary result of that was a Probing the News feature discussing the technical trends that would emerge at the ISSCC [Electronics, Dec. 23, 1985, p. 50]. Then came the job of tracking down the authors and persuading them to give us a peek at what they were going to tell the conference. It became the job of Sam, Bernie, and Charlie to follow up to get copies of the papers.

Once the two editors reported on those papers, they had to catch up with the ones submitted late. Bernie says he agrees with Grebene’s observation: “It seems that the number of papers from Japan is increasing, both in number and in the ratio of those accepted to those submitted. They seem to do their job better than the Americans and adhere to the rules about previous publication more scrupulously. On the other hand, they are late more often with their papers than the Americans are with theirs.”

The Inside Technology on p. 38, about how Tom Angelucci invested his energy and his company in a 15-year crusade to get tape automated bonding a place high on the technology map, does more than show how strong belief in oneself can be rewarded. It also illustrates that there is no substitute for knowledge and experience in an editor.

The editor in this case is Jerry Lyman, who covers packaging and production and has done so for a decade and a half—about the same period that Angelucci has been doing his missionary work for TAB. Jerry followed the story with interest, writing about the technology until finally his instincts, based on those years of journalistic involvement, told him that the time that Angelucci has been working toward is finally near.

That’s an example of the experience coupled with deep knowledge that Electronics has been known for throughout its 56-year history.
"We did it!"

"It's our competitors' faces I want to see. We've really cracked this market now."

"Like National's 32-bit microprocessor family?"

"I knew we'd close that sale. Did you see their faces?"

"Looks like we made all the right decisions at the right times."

"You can't build a system out of data sheets and promises. National had it, they delivered it, and they got us here first."

While you're still dreaming about success, Sequent is delivering it. With National's Series 32000 family.

On January 17, 1983, eighteen people started a new company called Sequent Computer Systems. They had no product, no plan, no backing. Only a dream.

Two years later, that dream came true. They delivered their first system—a sophisticated parallel processing computer. A full year ahead of their competitors.

How'd they do it? Hard work. Calculated risks. Belief. And a critical decision. They chose the Series 32000™ microprocessor family.

It offered them a complete 32-bit microprocessor family, including demand paged virtual Memory Management, Floating Point, and other peripherals with full UNIX™ support.

But the Series 32000 wasn't just the right engineering decision, it was the right business decision. It helped Sequent get their system to market fast. First.

Sequent hit their window of opportunity. And that window is still open—for now. So find out how the Series 32000 can help you build your own success story. Contact National Semiconductor today.

National's Series 32000, MS 23-200
P.O. Box 58090
Santa Clara, CA 95052-8090

National Semiconductor
We're doing it.

Circle 7 on reader service card
LETTERS

Equal time for CBS

To the editor: I would like to express my dismay upon reading "The drive to sharpen NTSC TV picture begins" [Electronics, Dec. 23, 1985, p. 59].

In the first reference to CBS, the author states, "To date, 19 U.S. satellite programmers plan to use 525-line BNTSC, and Home Box Office and CBS Inc. are using it now." This statement is both erroneous and misleading. Some of the satellite transmissions of the CBS Television Network are encrypted using the M/A-COM VideoCipher I encryption system. However, these transmissions do, in fact, utilize an aural subcarrier and do not place digital audio in the horizontal blanking interval. Thus, CBS is not using the BNTSC system.

In the second reference to CBS, the article states, "To display BNTSC in the 5:3 aspect ratio used by HDTV, an augmentation channel, which combines the bandwidths of two adjacent NTSC channels, is necessary to carry the additional sections of the horizontal lines. However, this description is erroneous in that:

1. The signal format proposed by CBS utilizes a form of multiplexed analog components. The signal format is not, however, either B-MAC or BNTSC.
2. There are no requirements to the effect that I am aware of to provide a 5:3 aspect ratio using a BNTSC signal. I doubt that M/A-COM intended to represent that they will provide a TV system with a 5:3 aspect ratio.
3. The system developed by CBS proposed the use of two 24-MHz satellite channels to transmit HDTV. The term "NTSC channels" is both incorrect and undefined.
4. The HDTV system currently under study by the International Radio Consultative Committee (CCIR) uses an aspect ratio of 16:9.

As regards the statements concerning HDTV, I believe a monumental international effort to establish a production standard has been misrepresented. Broadcasters and manufacturers worldwide are trying to achieve something never before accomplished—the establishment of a worldwide electronic studio production standard. A transmission format for HDTV will be the subject of study in the next four-year CCIR cycle.

Finally, three statements in the article would leave the uninitiated confused as to what equipment was necessary to receive BNTSC signals if transmitted to the home. To clarify the facts, only M-NTSC signals (M specifying the precise characteristics of the radiated signal per CCIR report 624) can be received by existing TV receivers. Any modification of the transmitted signal, such as the elimination of the horizontal synchronizing pulse or the aural subcarrier, would necessitate the use of some special receiver or decoding device.

Howell W. Mette
Manager, Information Services
CBS Engineering & Development
Department New York

☐ M/A-COM maintains that BNTSC is indeed capable of a 5:3 aspect ratio, it should be noted that 16:9 approximates 5:3. The article clearly states that BNTSC and B-MAC both require decoders.

CMOS bipolar since 1971

To the editor: In your excellent "CAD, CMOS, and VLSI are changing analog world" [Electronics, Dec. 23, 1985, p. 35], you discuss mixed bipolar and CMOS processes.

AWA Microelectronics is the Microelectronics Division of Amalgamated Wireless Ltd. As well as standard CMOS and bipolar TTL processes, the division has offered a CMOS bipolar-compatible process since 1971. The process features daisy-fused junction-isolated bipolar transistors on a double epitaxial (n on n+ on p) substrate with gate CGMOS, allowing vertical npn transistors and npn transistors as well as junction FETs and p-channel n-MOS transistors. First described in 1971, the process has been revised many times. The process has been used for several designs, including combined analog comparators with multiplexers for military applications.

The AWA facility is qualified to four fabrication standards: commercial, professional, military, and high-reliability. The military standard is equivalent to MIL-STD-883C; the facility is approved to AS1821 (equivalent to MIL-STD-Q9858A). The hi-reli standard is a higher standard for implantable prosthetics.

Graham B. Darley
Amalgamated Wireless Ltd.
North Ryde, Australia

Correction


Circle 8 on reader service card
NOW IT’S FAIRCHILD THAT’S JOINING THE BiCMOS CAMP

The number of companies in the mixed bipolar-CMOS digital and memory circuit camp continues to increase. Now Fairchild Semiconductor Corp. is hinting it will enter the market with a mixed process it has had under development for two years. It is virtually certain that its first products using a proprietary BiCMOS process will be in the memory area, although it could be used in at least two other product lines, which the company won’t specify. When the BiCMOS program is up and running, the company plans to use it in at least two manufacturing facilities. Hitachi and Motorola have made major commitments in BiCMOS, and Texas Instruments has indicated it will enter the fray also.

SOLID-STATE CCD SENSOR DOUBLES RESOLUTION OF PREDECESSORS

NEC Corp. says its newly developed charge-coupled-device image sensor demonstrates that silicon sensors can have the high definition needed to replace camera tubes in all applications. The device has a vertical overflow drain that forms an antiblooming structure beneath the pixels so as not to preempt valuable surface area, as many antiblooming methods do. The CCD sensor has a resolution of 1,280 pixels horizontally and 980 vertically, twice that of earlier models. It is suited for use in a 2:1 interlaced high-definition system with 1,049 scanning lines and a 4:3 aspect ratio. It could also be used for more rapid pickup of letter-size documents—valuable for optical-disk file systems—than is possible with line sensors at a resolution of 4 lines/mm. The pixel resolution achieves the Nyquist limit of 960 lines vertically and horizontally. The device has a photosensitive area of 12.7 mm horizontally by 9.5 mm vertically—equivalent to a 1-in. tube—on a 14.5-by-12.0-mm chip.

BITBUS STANDARD GETS BOOST FROM FACTORY-AUTOMATION OEMs

Bitbus looks as if it’s becoming a de facto standard for the lowest level of factory automation. Seven original-equipment manufacturers will announce this week that they intend to work Intel Corp.’s standard into products requiring distributed data acquisition and control. The seven OEMs are Analog Devices, Digital Equipment, GMF Robotics, Honeywell, Toshiba, Varian Associates, and Westinghouse Electric. Because Bitbus is designed to function at the lowest level of factory automation—sensors, transducers, and manipulators—it can accept and control data at a level not addressed by the Manufacturing Automation Protocol or other multilayered local-area networks. Bitbus can, however, support such LANs.

LASER AND PHOTODIODE OPERATE IN FIBER’S LOW-LOSS 1.55-MICRON BAND

High-speed fiber-optical communications at the low-loss window located at 1.55 µm can begin whenever dispersion-shifted glass-fiber cable becomes available; NEC Corp. has developed the laser and photodiode needed at the two ends of the link. Distance between repeaters should be more than 100 km—about twice that possible in the widely used 1.3-µm band. The indium-gallium arsenide phosphide double-heterostructure laser diode features the relatively low threshold current of 40 mA typical and the high output power of 5 mW typical. Selected units can be operated at peak pulse output power of 30 mW for instrumentation and other noncommunications applications. The InGaAs avalanche photodiodes are fabricated in a single vapor-phase epitaxial process that is better suited to production than is the more common liquid epitaxial process. External quantum efficiency is 80%, a marked improvement over germanium photodiodes, and dark current is only 1/10th as large. Gain bandwidth product of the avalanche photodiodes is 30 GHz.
Electronics is back—with the industry's best reporting on technology. In the first half of 1985 alone, Electronics featured hundreds of important articles with news and analysis that leaders in the field can't afford to be without:

- Full coverage of computer technology, with 86 articles on computer systems, 50 on software, 33 on boards and peripherals, and 28 on CAD/CAM
- 140 articles on international technology
- 30 articles on military technology
- 27 articles on the latest developments in test and measurement equipment
- Over 100 articles on communications technology
- 40 articles on components technology
- More than 100 articles on worldwide events in semi-conductor technology.

Readers depend on us for this full scope of technology coverage worldwide. Shouldn't your selling message be in Electronics' environment of pivotal technology reporting and analysis?

Put your advertising where the electronics attention is. Call Electronics today, at 212/512-3140 (U.S.), to reserve your ad space. Outside the U.S. contact your sales representative.

Electronics is back. Shouldn't you be back as well?
AMD AND SONY MAY BE SWAPPING DEVICES SOON

The deal was billed as a joint technology-development agreement in a letter of intent signed last week, but Advanced Micro Devices Inc. and Sony Corp. may be swapping devices well before their strategic alliance results in new chips. AMD, bottled up in a slumping market, gets an opening into a new market—consumer electronics—through the deal as well as a toehold in Japan, where it is embroiled in a trade dispute over erasable programmable read-only memories [Electronics, Oct. 7, 1985, p. 14]. Sony, a leading Japanese captive supplier on a mission to enter the merchant market, will have access to part of the AMD product line. The two will jointly develop and market next-generation very large-scale integrated circuits, but an AMD representative added that some existing chips of the Santa Clara, Calif., firm may be adapted for the consumer market, where it does not now compete. Sony, in the second year of a push into merchant ICs, last year grew by nearly 50% and became one of the top-10 IC producers in Japan—or very close to it. In another deal with a U.S. producer, Sony will produce 64-K dynamic random-access memories designed by Vitelic Inc. of San Jose.

CHIP BOOKINGS SURPASS SHIPMENTS FOR THE FIRST TIME SINCE 1984

The much-watched book-to-bill ratio of the worldwide semiconductor industry exceeded parity in January for the first time in 17 months. Recording its fifth monthly increase in a row, the ratio hit 1.04:1. But the rise came for the wrong reason: shipments in January declined 12.5%—to $546.2 million—from December, says the Semiconductor Industry Association. Still, average monthly shipments for the three-month period ended Jan. 31 totaled $610.6 million, up 5.1% over December. James L. Barlage, who follows the chip industry for Smith Barney Harris Upham & Co., New York, says the ratio was "very much on target," and industry shipments should improve this month. "It's no longer an issue of whether the industry has turned around," Barlage says, but whether the industry can sustain the increase.

IBM SAYS IT HAS STOPPED SLIPPING IN JAPAN

An IBM Corp. executive says Big Blue has stopped its slide in the Japanese computer market and asserts that the computer giant will continue its global fight to protect "intellectual property rights," primarily in software. George H. Conrades, group executive and head of IBM's Asia-Pacific Group, contends that 1985 sales increases for IBM in Japan will be at least as large as those of its Japanese competitors—estimated at between 20% and 25%—when the figures are released in March. IBM had fallen from first to third place in Japan's large-computer market. In its drive to protect its patents, Conrades says that IBM was forced to take Fujitsu Ltd. to arbitration after what he describes as "significant disagreements" over the use of software.

JAPANESE WANT TO CASH IN ON EXPECTED BOOM IN 'SMART CARDS'

Four Japanese chip makers are either entering or getting ready to enter the market for electrically erasable programmable read-only memories. They'll try to capitalize on what some analysts see as an impending boom in "smart cards" (credit or bank cards with built-in memory) and point-of-sale equipment designed to verify credit records. Fujitsu Ltd. already is delivering samples of a 64-K EEPROM for use in smart cards; Toshiba Corp. says it has both 64-K and 256-K versions ready for sample deliveries; and NEC Corp. and Mitsubishi Electric Corp. are developing 64-K EEPROMs for the same market. Hitachi Ltd. and Oki Electric Industry Co. were the first two Japanese makers to market EEPROMs (see related story, p. 40).
What a performance! Seven new data acquisition and control boards for your IBM PC™

Encore! Encore!

Data Translation has done it again. Our first two analog and digital I/O boards for IBM personal computers received rave reviews.

So we extended our product line to seven ... starting at $295 for quantity purchasers.

While most of the personal computer world focused on home and office applications, we lifted the curtain on two other key areas. Laboratory data acquisition and industrial control.

Now, no matter what you need for your IBM PC, we have it. Each board is a complete data acquisition and control system. With A/D, D/A, digital I/0, and a programmable clock. You simply choose the board offering the speed and resolution you need most. Just plug it into your PC’s backplane and it’s showtime.

With on-board intelligence, all seven are software compatible and supported by Data Translation’s PCLAB software package.

<table>
<thead>
<tr>
<th>Price ($)</th>
<th>Class</th>
<th>Model</th>
<th>Resolution (bits)</th>
<th>No. of Channels</th>
<th>Speed (kHz)</th>
<th>Resolution (bits)</th>
<th>No. of Channels</th>
<th>Digital I/O</th>
<th>Digital In/Out</th>
<th>Programmable Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>295 (OEM)</td>
<td>Low Cost</td>
<td>DT2808</td>
<td>16</td>
<td>8</td>
<td>2</td>
<td>16</td>
<td>yes</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>495</td>
<td>General Purpose</td>
<td>DT2801</td>
<td>16</td>
<td>8</td>
<td>16</td>
<td>16</td>
<td>yes</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>995</td>
<td>High Speed</td>
<td>DT2801-A</td>
<td>16</td>
<td>8</td>
<td>16</td>
<td>33</td>
<td>yes</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1095</td>
<td>High Resolution</td>
<td>DT2800/5716</td>
<td>16</td>
<td>8</td>
<td>16</td>
<td>16</td>
<td>yes</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1095</td>
<td>Low Level</td>
<td>DT2805</td>
<td>16</td>
<td>8</td>
<td>16</td>
<td>16</td>
<td>yes</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2070</td>
<td>Low Level, High Resolution</td>
<td>DT2805/5716</td>
<td>16</td>
<td>8</td>
<td>16</td>
<td>16</td>
<td>yes</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1695</td>
<td>Simultaneous S/H</td>
<td>DT2819</td>
<td>12</td>
<td>4</td>
<td>27.5</td>
<td>13.7</td>
<td>yes</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes: 1. PCLAB software supports all models. 2. Programmable gain is standard for all DT2801 and DT2805 models.
3. Screw terminal and signal conditioning panels available for connection of all I/O signals.

Data Translation is playing the leading role in personal computer data acquisition and control. Find out how we can help your performance today.

VISA and MasterCard accepted.
Call (617) 481-3700

See our new 646 pg. catalog/handbook or see us in Gold Book 1986. Or call for your personal copy today.

DATA TRANSLATION

World Headquarters: Data Translation, Inc., 100 Locke Dr., Marlboro, MA 01752 (617) 481-3700 Tlx 951 646.
European Headquarters: Data Translation, Ltd., 13 The Business Centre, Molly Millars Lane, Wokingham Berks, RG11 2QZ, England Tlx A51849862 (#D)
In Canada: (416) 625-1907.

IBM PC is a registered trademark of IBM.
APOLLO LAUNCHES VOLLEY OF NEW PRODUCTS

Under heavy competitive fire in the work-station market it pioneered, Apollo Computer Inc. will respond later this week by announcing new products across the price spectrum. The Chelmsford, Mass., company's new low-end computer will offer compatibility with IBM Corp.'s Personal Computer AT and computing performance comparable to Apollo's DN 660, previously the company's most powerful work station. In the midrange, Apollo will boost its graphics capability and claim the industry's fastest three-dimensional real-time performance. Topping off the company's new line will be a parallel-processing server compatible with Apollo's Domain architecture, but which was developed by a third party.

FERRANTI TO PROVIDE 18-V CMOS GATE ARRAYS

Look for Ferranti Interdesign to address a market sector that has been largely overlooked by other gate-array makers: high-voltage silicon-gate CMOS. The MH series of arrays from the Scotts Valley, Calif., company targets applications that require up to 18-V capability rather than conventional 5-V operation. These include industrial and automotive control. In the latter case, the arrays can operate directly from 12-V car batteries. Ferranti uses an enhanced oxide-isolated polysilicon-gate high-voltage CMOS process to fabricate the chips. The HL series consists of eight arrays, ranging in complexity from 70 to 1,600 equivalent two-input gates and from 18 to 84 bond pads. Engineering charges will start at $5,000, with prototypes ready in 6 to 16 weeks.

AIDA'S WORK STATION AIMED AT DESIGN ANALYSIS AND TESTING

Aida Corp.'s new high-performance computer-aided-design work station is especially suited for design analysis and testing. Aimed at designers of medium- to very-large-scale ICs, the Aida Design System is built around an Apollo Computer Inc. work station and uses hardware coprocessors. It includes more software for testing than other CAD systems do. Design analysis software includes a logic design-rule checker, automatic test-pattern generator, and simulation accelerator. A typical system will cost $140,000 when available from the Santa Clara, Calif., company in April.

NOW POWER MOS FETs COST LESS THAN COMPARABLE BIPOLAR DEVICES

Price cuts announced by International Rectifier Corp. on its power Hexfet II line of MOS FETs make them less expensive than comparable workhorse bipolar power transistors the El Segundo, Calif., company aims to replace. For example, the 50-V IRFZ22 drops to 49¢ each in lots of 10,000. This 39% reduction makes the IRFZ22 cheaper than a comparably rated bipolar chip, the industry-standard D44H5. Higher volumes and yields made the price cuts possible on the eight-member family.

PROTOTYPING CARD SIMPLIFIES DESIGN OF PRODUCTS FOR IBM PC AT

The pad-per-hole layout pattern on Vector Electronic Co.'s prototyping card makes it easier to design specialized circuitry and high component densities into board-level products for the IBM Corp. Personal Computer AT. Pads and buses are made of 2-oz copper with reflowed solder plating, and card-edge connector contacts are gold over nickel plate. The model 4617-3 has 0.042-in. plated through-holes, which accept any width DIP or Vector's wire-wrap terminal, on 0.1-in. centers. The board sells for $43.53 each. Delivery is from the Sylmar, Calif., company's stock.
FUJITSU PUSHES HEMT DEVICES INTO LSI-LEVEL LOGIC

HIGH-ELECTRON-MOBILITY TRANSISTORS BUILD 1,500-GATE ARRAY

ANAHEIM, CALIF.

No sooner have manufacturers in the U.S. and Japan entered production with high-electron-mobility transistors in discrete form than researchers have leapedfrogged their efforts by generations—jumping straight to the large-scale-integration level.

At this week’s International Solid State Circuits Conference in Anaheim, researchers from Fujitsu Ltd., Atsugi, Japan, will announce they’ve fabricated the largest HEMT-based logic circuit—a 1,500-gate, 6,650-transistor array using enhancement/depletion-type direct-coupled FET logic (DCFL). Created as part of Japan’s National Research and Development Scientific Computing System Program, this impressive LSI HEMT circuit culminates a Fujitsu effort that also produced 1- and 4-K static random-access memories using the same technology.

Fujitsu is not developing the gate array as a product, but HEMT technology mostly likely will be used in critical portions of its national-project supercomputer systems, says a senior research official. Fujitsu is working under a timetable that calls for demonstration of 3,000-gate arrays and 16-K memories—tasks of equivalent difficulty, although the RAMs have more transistors—by the end of March, to show the feasibility of using such devices in a computer.

Fabricated using 1.2-μm design rules, the 1,500-gate array features an average delay time of 85 ps for a three-input NOR gate at 300 K (room temperature). Using this LSI HEMT gate array, Fujitsu has implemented an 8-by-8-bit parallel multiplier that finishes a multiplication in 4.9 ns. The total chip power consumption of this implementation is 5.8 W at room temperature.

But it is at lower temperatures that the technology shines. At 77 K, the temperature at which many future supercomputer systems may operate, multiplication time is improved by almost 40%, to 3.1 ns, with a total chip power consumption of 3.2 W and a supply of about 1 V, instead of the 2.2 V used at 300 K.

The first reported successful LSI-level HEMT logic chip immediately shows competitive technology in terms of speed and power consumption. In a roughly comparable gallium arsenide device, the 1,000-gate DCFL array that Toshiba Corp., Kawasaki, Japan, described at last year’s ISSCC, three-input NOT gates have delay times that range from 42 to 255 ps. And Toshiba’s GaAs array dissipates less power, about 400 mW per chip. Silicon technology has been pushed to comparable speeds: in a 2,500-gate bipolar macrocell array from NTT Corp., the average equivalent three-input NOR gate delay is about 75 to 80 ps.

Fujitsu has put 72 input/output cells and 1,320 basic cells on its 5.5-by-5.6-mm HEMT chip. Each three-input NOT cell incorporates one depletion-mode and three enhancement-mode HEMTs. Each I/O cell includes three D-HEMTs and five P-HEMTs, configurable by a metal mask as either an input or an output buffer. The basic array is arranged as 20 columns of 76 cells each, with 15 interconnection lines between columns.

The HEMT array was fabricated using molecular-beam-epitaxial processing techniques. Oxygen-ion implantation was used for device isolation, while self-terminating selective dry etching was used for the aluminum-gallium arsenide and GaAs layers that control HEMT performance. For the

TWO NEW WAYS TO INCREASE CHIP UTILIZATION

As popular as it has now become, the “sea-of-gates” approach for improving chip utilization in gate arrays and standard-cell designs is still not good enough for some circuit designers.

The sea-of-gates approach typically improves chip utilization from 50% to 75% by eliminating the space wasted by underutilized dedicated interconnections and running lines over or through the individual gates.

Still dissatisfied, two research groups at Mitsubishi Electric Corp., Itami, Japan, have developed alternatives that are even more efficient—one for bipolar master slices and the other for CMOS arrays. Both techniques will be described this week at the International Solid State Circuits Conference in Anaheim, Calif.

In the bipolar master-slice gate array, the designers used what they call a variable-size-cell approach to eliminate the wasted space that often exists in underutilized cells in an array. In this approach, the array is constructed from basic cell units containing three transistors and four polysilicon resistors. By changing the number of transistors and resistors, the size of the cell units can be varied to suit their task. The value of every polysilicon resistor for logic function is determined, and the unused resistors are converted to intracell wiring by running a platinum-silicide interconnection line over them.

In the bipolar master-slice fabricated using this technique, about 40,000 transistors and 33,000 resistors are grouped into 13,312 basic cell units. The master slice is fabricated using the company’s silicide-base contact technology and four layers of metallization.

The first metal layer formed on the unused polysilicon resistors is PtSi, and the remaining layers are fabricated using aluminum-silicon and aluminum-silicon-copper silicide alloys.

In the CMOS array, the designers have developed a basic-cell-buffer approach that accommodates the 20% of any semicustom design dedicated to input/output. This is done by implementing the 1/O circuitry using the same basic cells in the periphery as in the internal array. In a 1.2-μm double-metal CMOS array, almost 430,000 transistors are arranged in 126 rows of basic cell chains.

The CMOS chip has surge-protection circuitry built with parasitic lateral diodes formed between the source or drain region and the p or n well. Resistors are formed from the polysilicon gates contained in each basic-cell transistor pair. –B. C. C.
interconnection lines, aluminum-gate metal was used on the first layer. The second layer is a titanium-platinum-gold silicide on a silicon oxynitride insulating film.

In tests of several types of ring oscillators fabricated on the array, the basic gate delay has been pegged at 85 ps at room temperature and 53 ps at 77 K. With a fan-out of three and 2-μm interconnection lines, typical internal delay time between gates is 138 ps at 77 K and per-gate power use is 2.6 mW.

Fujitsu HEMT logic work will push on to the 3,000-gate level, and then the team will turn to refining the devices of that complexity. Fabrication of 3,000-gate arrays is expected in the next few months. After that, designers of the upcoming national-project supercomputer will spend nearly two years deciding where to use the HEMT parts.

Designing HEMT logic circuits is harder than building memory devices, and the fabrication-process control is more difficult, too, Fujitsu researchers believe. The DCFL circuit, which they consider the best for HEMTs, consists of normally-off switches and normally-on load devices. Both E- and D-HEMTs are needed, and their thresholds are controlled by the thickness of silicon-doped epilayers. Thicker layers increase the electron supply in the channel and turn it on, and the critical thickness margins are small.

—Bernard C. Cole
and Charles L. Cohen

### COMPUTERS

**NEC's LATEST CPU KEEPS HONEYWELL LINE GOING**

PHOENIX, ARIZ.

Japan's NEC Corp. has never been known for modesty. True to form, it bills its new 36-bit general-purpose mainframe as the world's fastest: it says the ACOS 2000 executes up to 170 million instructions/s. Though NEC will not market the computer in the U.S., Honeywell Inc. now says it will use the 2000's central processing unit as the heart of its new top-of-the-line DFS.

"Honeywell will integrate elements of this new technology family with GCOS operating-system software and Honeywell peripherals, communications, and services," says James R. Bloom, vice president and general manager of Honeywell's Large Computer Products Divi-

**BEHIND THE DENSITY PUSH: SOLID WORK ON MUNDANE MATTERS**

While eyes are glued on the giddy push to higher densities and speeds at this year's International Solid State Circuits Conference in Anaheim, a number of presentations address the more mundane issues such as alpha-particle immunity, system-level compatibility, and low-power operation. These efforts may have greater impact than device shrinks and the like on the industry's ability to proceed to higher densities and speeds, believes Alan Grebene, president of Micro Linear Corp., San Jose, Calif., and chairman of the meeting.

"Pushing the [density and speed] limits of the technology is fine," Grebene said. "But it must go hand in hand with attention to these other issues."

Designed with the need for alpha-particle immunity and power savings in mind is a 1-Mb CMOS dynamic random-access memory from Toshiba Corp., Kawasaki, Japan. The chip can operate as either a 1-Mb-by-1-bit or a 256-K-by-4-bit array. It has an n-diffused structure for the bit line and memory cell that has been combined with a deep-channel boron implant to improve alpha-particle immunity by 50%, compared with the standard n**+** approach.

The part's standby power has been reduced to no more than 250 μW, and active power use held at 175 mW, through the use of a novel dual-stage voltage-generator design, which consists of a bias stage and a driver stage. The key is the suppression of the current through the bias stage by increasing series resistance.

The DRAM's 56-ns access time is achieved without a power penalty through the use of a new sense-amplifier design. In this array, a pair of barrier transistors with fixed gate voltages is inserted between n- and p-channel flip-flop pairs, reducing capacitance and thus delay times.

Aiming at improving system-level performance, engineers at Mitsubishi Electric Corp. have developed a 47-ns 256-K DRAM with relaxed timing requirements. In general it is not possible to design a memory system that can take full advantage of a DRAM's cycle time, no matter how short it is, because conventional DRAMs require wider timing margins for critical edges of input signals to absorb the clock skew and noise of the system.

In Mitsubishi's design, critical timing edges are reduced and timing requirements relaxed by keeping the internal row-address-strobe clock active until completion of the internal operation, even if the external RAS clock has since become inactive.

Static RAMs, as they move toward longer-word organizations, tend to eat up more power. Toshiba has designed an 8-K-by-9-bit n-MOS SRAM that can access data in 18 ns while drawing only 500 mW, and can stand by on 50 mW. These figures roughly equal the power used by a 64-K-by-1-bit chip. Using present techniques, power dissipation would have been at least nine times greater, say the designers. To build such a fast byte-wide SRAM with acceptable power dissipation, Toshiba has developed a new shared-word-line technique in which the 72-K cell array is divided into 18 blocks of 4-K each, with a row decoder circuit located in the center.

Each block is divided into two sets of eight columns, and each set is linked by a polysilicon wiring line that makes it possible to select only one fourth of the memory cells at once, releasing cell current by 75%.
NEC licensed the architecture from Honeywell

AT&T FORGES A NETWORK OF ALLIANCES TO BUILD ITS EUROPEAN BASE

When AT&T Co. was forced by the U.S. government to divest itself of the Bell operating companies and open up the U.S. telecommunications market to competition, the giant equipment manufacturer started paying a lot more attention to overseas markets.

Its strategy to gain a foothold in the difficult European market was clear from the very beginning: to establish an international presence as quickly as possible by forging complementary co-operative arrangements with native companies. The first was in its bread-and-butter public-switching business when it teamed up with Dutch multinational electronics producer Philips to create the joint-venture company that will supply switches to the French market.

The U.S. company then asserted itself in office automation and data processing by taking a 25% interest in Ing. C. Olivetti & C. The basis for that deal was a trade of technology much needed by the Italian company for the high-powered and Europe-wide marketing expertise AT&T lacked.

AT&T's first European incursion into the components business was another joint venture formed with Telefónica SA, the Spanish national telephone company, for the construction of a MOS integrated-circuit production facility near Madrid. The Spanishards will thus receive desperately needed semiconductor technology as AT&T sets itself up as a components manufacturer within the European Communities.

The most recent alliance was announced just last week, when the American company signed an accord with Italy's SGS Microwavelectronica SpA. The Italian company will market world-wide, with exclusive rights in Europe, bipolar chips produced in AT&T's facility near Reading, Pa. The agreement will cover some 35 circuits based on AT&T's exclusive complementary bipolar technology. -R. T. G.
al presence of Alcatel and its parent, the Compagnie Générale d'Electricté. Government sources say that, in a couple of weeks, the government, the CEG, the Compagnie Générale des Constructions Téléphoniques (CGCT), AT&T, and ATP will sign a memo of understanding that will serve as the basis for future contracts. AT&T initially will fill 16% of the French public-switching market with its 5ESS PRX switch. This will be in place of equipment that CGCT normally would supply—switches it makes under license from Alcatel. AT&T will then help Alcatel adapt its switch to the U.S. market and help the French company sell it. In the long term, however, AT&T and Alcatel would be competitors both in France and in the U.S.

In a side deal for microwave equipment, AT&T will become a major customer of Alcatel, with which Philips plans to merge its French microwave manufacturing activity.

**Cries of Sellout.** With a general election due March 16, opposition parties are sure to criticize CEG's cooperation with the U.S. giant. In a televised debate held several months ago, one of the opposition leaders, Jacques Chirac, accused Prime Minister Laurent Fabius of planning to "sell the CGCT to AT&T."

Nonetheless, it is widely believed in French government and industry that the only way to have a world-class switch manufacturer is to establish a significant presence in the U.S. market, which mandates a team-up with AT&T.

**FCC's Enhanced-Services Proposal Stirs Debate**

**Arlington, Va.**

A debate is heating up over the best way to encourage competition in enhanced telecommunications services. And its outcome could go a long way toward shaping the increasingly deregulated telecommunications industry proposed by the Federal Communications Commission in its current Third Computer Inquiry.

Arguing on one side are the FCC and the Justice Department. They espouse a murky concept called "comparably efficient interconnection" (CEI), which they say will neutralize the advantage that ownership of the switching facilities gives the phone companies over third-party providers of enhanced services. But critics counter that CEI is vaguely defined and should supplement, not replace, the structural-separation requirements that require phone companies to establish arms-length subsidiaries for their enhanced services business.

The FCC imposed those requirements in its 1980 Computer II decision when it cut the seven regional Bell operating companies (BOCs) from the newly open-market AT&T Co. Now it proposes to replace the requirements with a combination of CEI, co-location of third-party equipment in central-office switching facilities, and accounting safeguards to guard against BOC's subsidizing enhanced services [Electronics, Jan. 20, 1986, p. 48]. The FCC says that CEI would require a BOC to engineer an open network that gives third parties access to central-office equipment comparable to their own access. Then the commission would allow the regions to offer enhanced services on a competitive basis. Such services are bounded by the imaginations of the vendors; they could include anything from electronic phone books to computer dating.

CEI "has very broad support," says Herbert Marks, a Washington telecommunications lawyer representing independent equipment manufacturers in the inquiry, better known as Computer III, where CEI was first proposed. The problem is there are as many definitions of CEI as there are interested parties, he adds.

**Equal Access.** Marks and others shun the term "comparably efficient interconnection" in favor of a more traditional phrase—equal access. "Equal access should clearly be the objective," agrees Dennis W. O'Shea, a telecommunications consultant with IBM Corp. "If the goal isn't equality, then we won't achieve anything like CEI."

For instance, many potential vendors consider co-location crucial to assuring third parties the same delay-free connections available to a BOC whose equipment sits in a room next to the switches. Though the FCC advocates co-location, BOCs may have other plans.

Thus far, regional U.S. West Inc. and American Information Technologies Corp. (Ameritech) have come up with CEI plans. U.S. West's open-network architecture would make the necessary carrier switching and transport services available to users and vendors. It already has been endorsed by the Justice Department's Antitrust Division, which oversees AT&T's divestiture. Chicago-based Ameritech's scheme would give access to its enhanced-service host computers through nodes owned by the third-party vendors.

During an Electronic Industries Association session on CEI in Arlington early this month, U.S. West's Larry Kapple told 100 telecommunications industry executives that Ameritech's scheme is surveying customer needs and local exchange capabilities before implementing its open-architecture plan. Once the appropriate interfaces exist, U.S. West would implement its plan, said Kapture, the BOC's vice president for technical strategy development. It is just this absence

**Deal will be breakthrough for AT&T in Europe**

AT&T and the CEG reached the original accord toward the end of last year. CEG president Georges Pecubere then lobbied the French government to accept it. Signing will take place when technical details and pricing are completely ironed out, say government sources.

Government sources also see the agreement with AT&T as part of a larger plan to restructure CGCT, the now-nationalized ITT Corp. subsidiary which has been the sole blemish on the Socialist government's performance record in the electronics sector. France nationalized its major electronics companies soon after the 1981 election and the improvement in those companies since then is one of the government's principal electoral assets: Thomson SA and Bull are back in the black after a long series of net losses, and CEG has improved its profitability. CGCT, on the other hand, showed a net loss of $25 million in 1985.

The restructuring plan calls for CGCT to split into two companies. One will be devoted to public switching, and the other will handle private telecommunications equipment. AT&T will take a minority interest in the public-switching company, with the French government retaining control. Matra SA is close to concluding an accord for taking a controlling interest in the private-telecommunications company, says an advisor to President François Mitterrand. The government maintains a controlling 51% interest in Matra.—Robert T. Gallagher
of concrete details in the two BOCs' plans for open architecture that leaves many observers wondering when CEI will become a reality. "What CEI means in technical terms is still not clear," said John W. Hinkle, president of Centel Business Systems' Pisk Division in Houston. In any event, Hinkle told the EIA session, CEI will not offset the advantages of enhanced services technology residing in the BOCs' central offices. Nor, in his opinion, will CEI prevent cross-subsidization of AT&T, whose equipment might already be co-located with the BOCs'. So the structural-separation requirements of Computer II should be retained, he argues.

Undeterred, FCC officials continue to explore the role co-location might play in providing equivalent interconnection and the extent to which the FCC will have to define CEI's specifications. Albert Halprin, chief of the FCC's Common Carrier Bureau, told the EIA session that the commission will commit "mammoth resources" to solving the technical issues.

The Department of Justice wants the commission to force the CEI issue while providing the flexibility to find technical solutions. And it acknowledges that the technical issues are murky. "You've got to keep some flexibility in this process, because right now no one can say what the technical solution is," warns Kevin Sullivan, assistant chief of the Justice Department's communications and finance section.

"George Leopold

LASER MAY SIMPLIFY THIN-FILM GROWTH

CHAMPAIGN, ILL.

G rowing thin metal films on chip substrates soon may be easier and cheaper to do if an experimental laser-based deposition process works as planned. The next six months will tell whether the system can select one particular metal from a mixed gas containing a variety of metal alkyls. "You could mix all these alkyls together in one big pot, and with a laser just go in and get the atom you want," says Eden. "And another beauty of this thing is that you're ionizing only the metal atoms. So the junk—the things that you don't want, like the carbon-bearing radicals—just goes flaming off."

Like other experimental laser-based methods, such as photodissociation, the Illinois method does not require the target substrate to be at high temperatures, as do conventional methods such as metal-organic chemical-vapor deposition (MOCVD). Growing thin films at room temperature may eliminate a key source of impurities: thermal breakdown of gaseous molecules near the hot substrate surface.

The Illinois method would eliminate the need for complex gas-flow systems found in other laser-based techniques. The selective deposition is a simple thing—we plan to do that within the next six months," says Eden.

Scientists familiar with the work think that Eden and his group have a good chance of succeeding. Eden believes the process could easily be ready for commercial use in semiconductor manufacturing within five years.

Varying the wavelength of the laser would determine which metal is deposited from a gaseous mixture containing a variety of metal alkyls. "You could mix all these alkyls together in one big pot, and with a laser just go in and get the atom you want," says Eden. "And another beauty of this thing is that you're ionizing only the metal atoms. So the junk—the things that you don't want, like the carbon-bearing radicals—just goes flaming off."

Like other experimental laser-based methods, such as photodissociation, the Illinois method does not require the target substrate to be at high temperatures, as do conventional methods such as metal-organic chemical-vapor deposition (MOCVD). Growing thin films at room temperature may eliminate a key source of impurities: thermal breakdown of gaseous molecules near the hot substrate surface.

The Illinois method would eliminate the need for complex gas-flow systems found in other laser-based techniques. The selective deposition is a simple thing—we plan to do that within the next six months," says Eden.

Scientists familiar with the work think that Eden and his group have a good chance of succeeding. Eden believes the process could easily be ready for commercial use in semiconductor manufacturing within five years. Varying the wavelength of the laser would determine which metal is deposited from a gaseous mixture containing a variety of metal alkyls. "You could mix all these alkyls together in one big pot, and with a laser just go in and get the atom you want," says Eden. "And another beauty of this thing is that you're ionizing only the metal atoms. So the junk—the things that you don't want, like the carbon-bearing radicals—just goes flaming off."

Like other experimental laser-based methods, such as photodissociation, the Illinois method does not require the target substrate to be at high temperatures, as do conventional methods such as metal-organic chemical-vapor deposition (MOCVD). Growing thin films at room temperature may eliminate a key source of impurities: thermal breakdown of gaseous molecules near the hot substrate surface.

The selective deposition is a simple thing—we plan to do that within the next six months," says Eden. "Scientists familiar with the work think that Eden and his group have a good chance of succeeding. Eden believes the process could easily be ready for commercial use in semiconductor manufacturing within five years.
MW/cm²—possible with UV laser light.

At the high-intensity blue-light levels, five photons are delivered to each alkyl, says Eden. The energy from two of these photons goes toward breaking the bond between the metal atom and the ligands, while the other three convert the freed neutral ground-state metal atom into a positive ion. Then the target substrate is negatively biased to attract the ions to the surface. In the Illinois experiments, a gallium arsenide substrate was bonded to a cathode, which was separated from the anode by about 1 cm; and the applied voltage can be varied between 0 and 2 kV.

Because the Illinois system uses an electric field to propel positively charged ions to the substrate, rather than depending on thermal energy to deposit neutral metal atoms as do UV-laser systems, the ions can be made to strike the substrate surface at much higher energy levels than can the atoms. The enhanced surface mobilities and energy levels of the ions may produce higher-quality films, notes Howard Schlossberg, physical science administrator at the Air Force Office of Scientific Research, who is overseeing the University of Illinois contract.

Eden's group is the only one now developing multiphoton ionization techniques for growing thin films, according to Schlossberg. And though other researchers are cautious in their assessment, some agree that the idea makes sense. "You may be able to reduce impurity formation with this technique, since you're attracting only the material you want," says Bruce Vojak, a staff research engineer who works at Amoco Corp.'s Amoco Research Center in Naperville, Ill.

MEDICAL

SPEEDING UP NMR IMAGING TO WATCH A KIDNEY WORK

GÖTTINGEN, WEST GERMANY

Nuclear magnetic-resonance imaging, a medical diagnostic tool in use since the late 1970s, has made a quantum leap: cross-sectional images of parts of the body can now be taken in seconds instead of minutes. Researchers at the Max Planck Institute for Biophysical Chemistry have achieved this feat by reducing the strength of the radiofrequency excitation pulses used in NMR imaging.

The 50- to 100-fold reduction in imaging time "opens new possibilities in clinical diagnosis," says Jens Frahm, head of the Göttingen research team. Now, he says, NMR methods can be used to record dynamic processes in the body. That means it is possible to image such physiological processes as the secretion of the kidneys and the movements of the heart. The fast imaging technique is safer than computerized axial tomography, which subjects the patient to X rays. It also shortens the time needed to make the multiple "slice" images used to build three-dimensional pictures—to about the time conventional NMR machines take to produce a 2-d image.

Frahm's group has been involved in fast-imaging NMR methods only since the spring of 1984. But already, manufacturers of medical electronics equipment—among them, General Electric in the U.S., Philips in the Netherlands, and Siemens in West Germany—are implementing the Göttingen technique in NMR imagers. Frahm says first versions of fast-imaging tools may come out before the end of this year.

In NMR imaging, atomic nuclei, when placed in a magnetic field and excited by an rf pulse, emit measurable radio signals. This phenomenon is characteristic of all stable atomic nuclei that contain an odd number of protons, neutrons, or both. These particles have two vital properties: a spin and a magnetic moment, properties similar to those of a spinning magnetic gyroscope. Hydrogen nuclei generally are used for medical NMR imaging. Hydrogen atoms, the most abundant elements in the body, have protons that are highly sensitive to magnetic forces and, when excited, emit well-defined radio, or NMR, signals. A receiver detects these signals and feeds them to a computer, which, in turn, converts the signals into pixels to form an NMR image on a monitor.

By choosing suitable values for frequency, amplitude, and duration of the exciting rf pulses, an imager operator can record a specific cross-section of parts of the body. Depending on the resolution chosen, a recorded image consists of either 128 or 256 lines, with each line containing 128 or 256 pixels, respectively. The slice thickness ranges from 5 to 10 mm.

A strong excitation pulse must be used to get meaningful NMR signals from the protons, however. This pulse tilts the proton's spin axis, and hence its magnetization vector, by 90°. After the rf pulse is applied, it takes about one second for the proton to return to its equilibrium position and to reach its original magnetization. Then is a new rf pulse applied.

Because of this 1-s relaxation time, it takes 236 s, or a little more than four minutes, to produce a 256-line image, for example. And because each pixel is recorded twice to improve the picture quality, it takes more than eight minutes to produce an image.

For that reason, clinical NMR diagnostic methods have been limited mainly to imaging immobile parts such as the head or spine, Frahm explains. Images of internal organs are blurred by the movements of, say, the heart, intestines, and lungs. Therefore, doctors had to rely on the much faster, but risky, CAT methods to image such organs.

WEAKER BUT FASTER. The Göttingen team has overcome this limitation by slashing the imaging time. "We figured that, instead of the strong rf excitation pulses needed for a 90° tilt of a proton's spin axis, it must be possible to use weaker, but more rapidly occurring pulses to get an image," Frahm says. The team uses pulses that deflect the spin axis by only 15° or so. That makes for a 75% weaker NMR signal, but the original magnetization is almost entirely retained. This means rf pulses can be applied and data for an image line obtained every 10 to 20 ms instead of every second.

This fast-imaging, or Flash (fast low-angle shot), technique cuts the recording time for a 128-line image from the two minutes or so needed with conventional methods to about two seconds; for a 256-line image, the reduction is from more than
four minutes to five or six seconds. Frahm says this is a significant advance in medical diagnostics.

Images that coincide with the phases of the heart cycle can also be taken by letting the heart currents (which may be derived from an electrocardiograph) control the NMR equipment. This way, if it takes, say, 20 ms to produce an image, the heart’s movements and functions can be registered in 50 steps per second. Also observable is the flow of blood to and from the heart, because blood contains water, hence, protons that are basic to the imaging process.

Another application is producing a series of kidney images. Here, “paramagnetic” substances are used as a contrast medium, Frahm explains. The medium’s passage through a kidney and its ducts can be traced over longer periods of time by means of a sequence of images.

In its NMR work, the Göttingen team is using a magnet whose superconducting, liquid-helium-filled main coil, cooled to -270°C, generates a magnetic field of 2.3 tesla. That is equivalent to 50,000 times the earth’s magnetic field. The magnet’s bore—the tube into which an animal body or, say, a part of the human body is placed—is 4 cm in diameter. The excitation pulses come from a nearby rf transmitter, which generates pulses of from 2 to 10 ms. The resonant frequency of the protons is about 100 MHz.

Aside from the advantages of the Flash technique, NMR furnishes sharp soft-tissue contrast—hence, more data than an X-ray image—and the NMR image can be arbitrarily oriented, which facilitates the search for particular details. CAT, by contrast, always shows an image perpendicular to the body’s long axis.

---

**MICROSUSMESSS**

**BACKUP KEEPS MICROSYSTEMS WORKING**

**DALLAS**

Dallas Semiconductor Corp. is borrowing an idea from big mainframes to satisfy the need for a crash-proof backup system to support microprocessor-based equipment.

The two-year-old company’s Integrated Battery Backup set is in essence a scaled-down version of the uninterruptible power-supply systems long used in data-processing centers to guard the work of mainframes. Dallas Semiconductor says the three-piece set, which will be introduced later this month, has both the power and the intelligence to keep microsystems ranging from personal computers to engineering workstations to factory equipment—from crashing and losing their data.

The key to this set is the DS1260 SmartBattery, which employs a twist on the concept of battery backup. For about a year, Dallas Semiconductor has been selling random-access memories in dual in-line packages that contain lithium batteries for nonvolatile memory. The SmartBattery is a sort of reversal of that idea: a lithium battery pack that contains an integrated circuit for voltage sensing and power switching.

SmartBattery can protect data in standard static RAMs for more than 10 years without system power. Packaged for a low ½-in. profile, the battery is connected to printed-circuit boards by 16 pins arranged in the footprint of a conventional DIP.

The crash-protection set also has a power monitor and nonvolatile controller-decoder, both made in CMOS. The monitor gives host microprocessors early warning of impending power failures. The nonvolatile controller-decoder IC protects RAM data and switches 4 to 16 memory chips to the protective lithium-cell backup.

“We are offering a way to orchestrate an orderly shutdown and then a graceful automatic restart of microprocessor-based systems in the event that system power is disturbed,” says marketing vice president Michael Bolan, who cofounded the spinoff with other former employees of nearby Mostek Corp. Once the power monitor measures a return of acceptable system power, the components work in concert to return the host processor and its programs exactly where they left off prior to the power shutdown, says Bolan.

The automatic restart and the ability to continue work flow without human intervention are “extremely critical for industrial applications,” adds Bolan, who also expects the battery-chip set to be used in office/personal-computer designs. “One of the things that has held back electronics in the industrial area is power glitches and the fact that semiconductors are volatile. We think this will help solve that problem.”

Many systems have been designed to deal with power losses, but they use discrete components, and not all of the implementations work properly under all conditions, notes Bolan, whose company has added a number of on-chip features to make its ICs and SmartBattery systems applicable to a wide variety of systems.

One such feature is the power-monitor chip’s ability to adjust the amount of warning time it grants microprocessors. This means there is no need to program it for the warning time needed for a specific system or to have the part customized.

The DS1231 contains two on-chip comparators to monitor power in two different locations—on the low-voltage system bus and on the upstream of the regulator near or at the power supplies. The upstream higher-voltage tap provides early warning that ac power is beginning to fail. This condition causes the power-monitoring IC to send an alarm, or interrupt signal, to the host processor, which then begins a subroutine to organize and safely store data in battery-protected RAMs.

When the second comparator detects that power has fallen below Vol specifications, the monitor IC sends a reset signal to the microprocessor for an unconditional shutdown. The shutdown

---

*John Gosch*
Electronics/Fehrttiery 17. 1986 21

The set protects static RAM data for 10 years

POWER-LINE LAN SOLVES ERROR PROBLEMS

DANBURY, CONN.

A fledgling local-area-network supplier claims it has succeeded where others have failed in achieving reliable, error-free data transmission by using a building's power wiring as the medium. By eliminating the cost of installing new LAN cables, GridComm Inc. says it can halve the cost of system implementation. The company solved the problem by achieving a very low error rate with a new modulation scheme called GCM, for GridComm Modulation.

GCM lets the 23-kb/s full-duplex networking system detect and correct single-bit errors on the fly, says the company. A patent has been allowed on GCM, but not yet awarded. The modulation scheme overcomes the carrier-dropout and error problems that have haunted others who tried to use a building's power lines to broadcast LAN data, says Kenneth Lewis, GCM inventor and GridComm's cofounder and president.

The allure of the power line as a data transmission path is simple: installing dedicated lines for data is expensive. The cost of new cabling is often equal to about 75% of the value of the microcomputers and peripherals the network will serve, says Lewis. In contrast, the cost of a GCM network is about 20% of the value of the network's processors and peripherals, he maintains.

The system's line drivers transmit a burst-type signal of 8 V peak to peak, which propagates to all points on a building's wiring up to the first voltage stepping transformer it encounters. The net uses 16 digitally synthesized carrier frequencies between 100 and 490 kHz and loads the powerline as a waveguide. The fact that one side of a powerline pair is a ground means that the pair does not radiate as an antenna does, points out Lewis.

GridComm also has developed extremely sensitive double-superheterodyne receivers for the system. The receivers' dynamic range makes it practical to use very low radio-frequency power levels at the line drivers.

Also figuring into the design are analog signal switches, extensive channel filtering circuitry, and a large (180 mils on a side) custom chip carrying both analog and digital components. The company is now having the components of GridNet—its first product since incorporation in 1983—tested for compliance with emissions regulations by the Federal Communications Commission.

Last fall, Apex Communications Ltd., a British competitor, introduced a half-duplex network system that enables communications over installed power lines. But that system—the Nectar Ring, which operates at only 4,800 b/s—is not nearly as fast as GridNet.

Another company hawking a similar product was Mollard Systems Design Inc., San Jose, Calif., launched in 1983 by Roy Mollard, a former Apple Computer Inc. executive. The system was plagued by bugs and repeatedly delayed, however, and late last year the company filed for protection from creditors under Chapter 11 bankruptcy laws.

EIGHT USERS AT ONCE. The GridNet, which thwarts eavesdroppers with data encryption, operates in areas up to 30,000 ft² using standard single-phase power wiring or three-phase 240-V lines, provided the correct coupling is used. The LAN can support up to 60 addressable nodes but only eight users at a time, so the company says a 32-node network is optimal. Future plans, Lewis says, call for an expanded bandwidth, perhaps as high as 1 MHz, that will permit the system to support twice as many users.

Each address, whether computer or peripheral, must be outfitted with two boxes that together make up what Lewis calls a communicator. Gridcomm has communicators for personal computers (the GC-1400, list price $549), for peripherals (the GC-1100, $449), and a third for interfacing the network with a telephone line for long-distance communication (the GC-Zero, $799).

Each communicator consists of both a wall-mounted unit that holds a power supply and the line drivers, and a desktop box that contains a Z8 8-bit microcontroller, a modem, up to 48-k bytes of internal memory, a real-time clock/calendar for electronic mail, and, in the case of the GC-1400, a small liquid-crystal display for status reports.

The network supports IBM Corp. Personal Computers, PC ATs, and their compatibles, as well as computers from Apple (including the Macintosh), AT&T, Digital Equipment, Hewlett-Packard, NCR, Tandy, and Wang. In addition, the network will support most printers and plotters with serial and parallel interfaces, says GridComm.

—Tobias Naegele
The industry’s leading coverage of international technology.

In Electronics.

Electronics is back—with the industry’s top reporting on international electronic technology. In the first half of 1985 alone, Electronics—with its worldwide bureau of correspondents—published more than 140 articles on international technology. Important articles with news and analysis that leaders in the field can’t afford to be without, such as:

**January**
- Philips Uses MBE for Lasers
- Siemens Readies Commercial ISDN
- Japanese Chemical Firm Moves from Soap to Floppies
- Italian Firm Seeks Allies to Crack U.S.
- Japan Pursues Role in Space
- Bellman Switches on Italtel for Expansion
- Robots get Smart in Japan
- ITT Invests in European Units Crack U.S.

**February**
- Europe’s Esprit Finally Sets Sail
- LSI Logic Counts on Sandfort to make its Mark in Europe
- Upstart Vendor Makes Waves in Japan’s Robot Market
- NEC Fashions New Fab Process
- Olivetti’s Vti Directs ET Designs that Marry Bus & Art
- German Startup’s Success Surprises Europeans

**March**
- British GaAs Chips Go to Market
- NEC’s CPU Leapsfrog IBM
- Hitachi CPU Challenges IBM
- France’s Lansat Rival Set for Fall Launch
- Olivetti Stakes Claim in Video Typewriters
- Italian VLSI Chip has the Right Accent
- Koreans Try for VCR Replay
- Germans Push X-ray Exposure
- There’s Life in Resistors, German Company Finds
- UK Beats a Path for Europe’s Race

**April**
- German System Meets New ICAO Standard
- West Germans Squabble Over Choice of IFF
- Britain Promotes Open Architecture
- US Makes Progress in Japan Telecom Talks
- Japan’s Lead in Optical Disks: It’s Part of the System
- Daisenberger Guides US Firms through Red Tape
- Asia: It’s No Longer Just Japan That Threatens US Markets
- Malaysia: Top Shipper of Discretes
- Indonesia: Domestic Sales are the Lure

**May**
- Thomson’s VCR System Clears Up Doubts
- ICL Banks on Networks and Japanese Chips
- Min Blazes Bright Path for Korea’s Gold Star
- Singapore Casts Lot with Software
- Philips’ Eurom Chip Finally Debuts
- Japanese Quit on IBM Software, Turn to UNIX
- Stronger Prices Stir Japanese Producers
- British Telecom Spreads Its Wings with Mitel
- South Korean IC Maker Seeks World Markets

**June**
- Plessey Switches Off Flash ADC, Saves Power
- Sony Campaigns Hard for BMN Camcorders
- Japanese Quit on IBM Software, Turn to UNIX
- Apple Tries Again to Blast Off in Japan
- Has the End Come for European Chip Makers?
- SIA Protest May Not Stem Trade Tide
- Now It’s Korea’s Turn in the Robot Market

And that’s only in six months!

Readers depend on us for this full scope of technology coverage worldwide. Shouldn’t your selling message be in Electronics’ environment of pivotal technology reporting and analysis?

Put your advertising where the electronics attention is. Call Electronics today, at 212/512-3140, to reserve your ad space. Outside the U.S. contact your sales representative.

**Electronics is back. Shouldn’t you be back as well?**
Anyone looking for a blueprint laying out future trends in semiconductor products will certainly find it at this week's International Solid State Circuits Conference. Partly obscured by the torrent of technical details being presented at the Anaheim, Calif., meeting to the worldwide semiconductor community will be a host of significant new products that are to be introduced shortly in the marketplace and are expected to appear in the next generation of equipment designs.

Leading the pack will be some surprising and spectacular superchips—very large-scale-integration memory and digital designs that push the upper limits of density and speed. These include single-chip mainframe central processing units, digital signal-processing CPUs of comparable sophistication, 4-Mb dynamic random-access memories, 1-Mb and 256-K DRAMs pushing down toward 50-ns access times, static RAMs moving aggressively down into the 1- to 30-ns range, and gate arrays that are demonstrating access times in the hundreds of picoseconds.

The digital world will share the spotlight with an impressive array of analog superchips, including a variety of modem front-end chips for telecommunications and an assortment of data converters that break new ground in speed and resolution.

The six stories that make up this special report are the first look at some of the most exciting and significant developments to be unveiled at this week's premiere semiconductor event. They include:

- Mainframe microprocessors such as IBM Corp.'s 32-bit Micro-370, a single chip that implements or supports emulation of the entire instruction set of the System 370 mainframe, and Sperry Corp.'s six-chip set that implements the Sperry C-series architecture.
- 32-bit digital signal processors such as National Semiconductor Corp.'s de-motor controller and Toshiba Corp.'s 170,000-transistor image processor.
- Entries from Texas Instruments, NEC, and Toshiba in the still sparsely populated 4-Mb dynamic RAM race.
- Blazingly fast static RAMs that push CMOS, Bi-CMOS, and emitter-coupled-logic processes below 10 ns.
- Application-specific chips, derived from mixed processes or gallium arsenide, that set new levels of performance.
- Complex telecommunications and data-communications chips, including a powerful trio from AT&T Co.—a 1-μm 2-Gb/s laser driver IC and 50-Mb/s optical data-link driver and receiver circuits.
Of all the designs presented at this year's ISSCC, the general-purpose CPU designs are unequaled in their sophistication and complexity. These mainframe-derived CPU chips can truly be called superchips.

A good example is the Micro-370, a 32-bit single-chip microprocessor from IBM Corp.'s Thomas J. Watson Research Center, Yorktown Heights, N. Y. (Fig. 1). This microprocessor not only directly implements 102 instructions of the System 370 mainframe, but also supports emulation of the entire instruction set. Fabricated in a 2-μm, silicon-gate n-MOS process using single-level-polysilicon and double-level-metal interconnections, the Micro-370 incorporates the equivalent of 200,000 transistors onto a 10-by-10-mm chip that features a 3-W power dissipation and a 200-ns cycle time at 10 MHz.

Designed using standard-cell methodologies and automatic placement and routing, the Micro-370 incorporates a three-stage pipeline and a microprogrammed structure that consists of a bus controller, a sequencer, a control unit, an execution unit, a clock generator, a special-function unit, an instruction decoder, and control-store logic. It uses full 32-bit internal data and address paths, which link with 32-bit asynchronous, nonmultiplexed, external data and address buses.

The execution unit contains a 32-bit arithmetic logic unit, a 64-bit shifter, nine special-purpose registers, a 32-bit adder, and two 16-piece sets of 32-bit general-purpose registers, with two 32-bit dual-rail buses running across the entire execution unit. The standard-cell-based sequencer determines the next address for the control store and provides the processor command to the bus controller. The special-function unit contains three instruction prefetch registers and special-function registers connected by a sense-amplifier bus.

Under microword control, the instruction prefetch registers drive the instruction-decode logic and the control unit. The control store consists of two mask-programmable read-only memories with a total storage capacity of 94-K. One ROM provides an 18-bit word to the sequencer for selecting the next address and generating processor commands. The other provides a 71-bit word for generating control signals. The clock generator uses a four-phase eight-output configuration to provide clocking phases for the microprocessor from an external TTL-level clock reference.

From Sperry Corp.'s Micro Products Development Group, Eagan, Minn., comes a six-chip set that implements the full Sperry Computer Systems C-series architecture and executes all 504 of the series 1100 mainframe's 36-bit instructions (Fig. 2). Four of the chips—the ALU, the address-generator unit, the decode and control chip, and the cache and interface unit—implement the basic series 1000 mainframe architecture.

The ALU chip contains a full 72-bit data path with a 72-bit ALU, a 72-bit shifter, a 128-word general register stack, and a hardware-assisted microengine with on-chip control storage. The address-generator unit incorporates a hardware sequencer to accelerate the basic instructions, a microengine with on-chip control storage and a 144-bit microcode word, three independent RAM arrays, and a full-width data path. The decode and control chip (Fig. 3) contains the instruction-decode ROM, miscellaneous control sequencing, and instruction-decode and interrupt logic. The cache and interface unit incorporates on-chip memory for controlling a 4-K-word cache block, a 64-word content-addressable memory for memory page-address translation, and interface logic for an external parity-checking 36-bit bus.

Containing its own microengine and control store, an optional extended-instruction-set chip implements bit, byte, decimal,
3. CONTROL

The decode and control chip decodes instructions and sequences control for Sperry's six-chip set. It contains ROM, control sequencing, and decode and interrupt logic. and string instructions, and it incorporates a triple-word 108-bit-wide decimal data path and a separate 36-bit binary data path. The sixth chip is the integer-multiply and -divide chip, designed to accelerate floating-point and integer-multiplication and -division operations. It can perform a floating-point multiplication in one clock cycle, or a double-precision multiplication with 72 operands in two clock cycles. In addition, external RAM can be used to store cache data, and the cache is expandable from 4-K words to 16-K words by adding more cache-interface chips and RAM arrays in 4-K increments.

Fabricated with a 1.2-μm double-level-metal CMOS process, a typical seven-chip configuration with an 8-K-word cache using a four-phase clock has a cycle time of 80 to 108 ns. The chip set boasts throughput rates ranging from 0.4 million to 1.5 million instructions per second. This performance rating is comparable to the Sperry 1100/71 mainframe and is 80% that of the 1100/81 mainframe.

Joining the many general-purpose 32-bit microprocessor designs now on the market is the long-awaited V60 from NEC Corp.'s Microcomputer Products Division. Fabricated using a 1.5-μm double-level-metal CMOS process, this 375,000-transistor design incorporates a 32-bit execution unit; a 4-GB demand-paged virtual-memory-management unit; a 191-K microprogram ROM; and a 32-bit floating-point multiplier implemented using the IEEE-754 standard.

Running at a 16-MHz clock rate, the NEC microprocessor executes 3.5 million instructions per second and consumes 1.5 W. The 273-instruction processor incorporates six functional blocks—the prefetch unit, the instruction-decode unit, the effective-address generator, the memory-management unit, the bus-control unit, and the execution unit—into a pipeline structure.

The on-chip memory-management unit has a 16-entry full-associative translation look-aside buffer that translates the virtual address into real addresses in 36 ns, worst case. The execution unit is a microprogrammed data-path generator with thirty-two 32-bit general-purpose registers, sixteen 32-bit scratchpad registers, a 64-bit barrel shifter, a 32-bit ALU, and a number of control registers. The ALU implements a second-order Booth algorithm for 16-clock multiplication on 32-bit data. Typical instruction-execution time is 62.5 ns, and power dissipation is 1.5 W.

DIGITAL SIGNAL PROCESSORS

High densities and sophisticated designs are marking the emergence of digital signal processing into the mainstream of circuit design. Some of the circuits described at this year’s ISSCC approach the complexity of their general-purpose 32-bit CPU counterparts.

For example, from National Semiconductor Corp. and SDA Systems Inc., both of Santa Clara, Calif., comes the first in a family of 32-bit, algorithm-specific, single-chip DSPs based on a reduced-instruction-set-computer architecture. The first chip in the family is the LM628, a special-purpose RISC digital signal processor that contains all the functions required for dc motor control in such applications as servo systems, automated manufacturing, and robotics.

Fabricated using a relatively conservative 3-μm single-level polysilicon, single-level-metal n-MOS process, the 50-instruction LM628 operates at a respectable 8-MHz clock rate, with typical instruction-execution cycle times ranging from 500 ns to 1.5 μs. Containing the equivalent of 25,000 transistors, the 30,200-mm² DSP dissipates only 250 mW. Included on the chip is a 32-bit ALU, ALU control logic, support circuitry that enables the ALU to perform 16-by-16 2's complement multiplication, 32 by 32 bits of data RAM, and 1-K by 16 bits of instruction ROM, as well as the core sequencer programmable logic array, which contains the algorithm-specific instructions that support motor control.

This core processor block (Fig. 4) is linked by an internal 16-bit bus to on-board peripheral blocks dedicated to particular applications. In the case of the motor-control-specific LM628, these on-board peripherals include a motor-position decoder that converts encoded quadrature signals from an external incremental position encoder to track motor position; an 8-bit pulse-width modulator that supplies analog control voltage to the motor or, when reconfigured, provides 8-bit parallel data for an off-chip digital-to-analog converter; and an input/output control block for servicing requests and data transfers to and from a host CPU. With a special-purpose orthogonal instruction set tailored to tasks common to motor-control appli-
The LM628 is designed to perform such functions as trajectory generation, loop filtering, and system control. Another special-purpose algorithm-specific DSP, from Toshiba Ltd., Kawasaki, Japan, is aimed at high-performance image-processing applications such as medical diagnosis and remote sensing. This image processor contains 170,000 transistors and incorporates a 32-bit ALU, a 64-bit barrel shifter, a 32-by-32-bit modified Booth algorithm multiplier, a 64-by-16-bit ROM for storage of sequence-control programs, a 16-by-99-bit RAM for microcode storage, four 16-bit loop counters, and a 32-bit data multiplexer. Fabricated using a 1.2-µm n-well CMOS process with two levels of aluminum interconnection, this image-processing DSP chip typically processes a 1,024-point complex fast Fourier transform in 1 ms—about 10 to 100 times faster than present single-chip DSPs, according to the designers. Operating off a 20-MHz clock, it dissipates 150 mA at 5 V.

A more general-purpose single-chip DSP comes from NEC IC Microcomputer Systems Ltd., Kawasaki. Fabricated using a 1.5-µm, double-metal-layer CMOS process, it performs 32-bit floating-point arithmetic operations with an on-board 32-by-32-bit floating-point parallel multiplier and a 55-bit floating-point ALU (Fig. 5). In addition, the chip contains a 64-K program ROM, a 32-K data ROM, and two 16-K data RAMs. This 15.4-by-8.4-mm chip, which has the equivalent of 370,000 transistors, operates with a 13-MHz clock and dissipates 1.5 W.

The on-chip 32-bit floating-point multiplier contains a 24-bit fixed-point parallel multiplier for mantissa calculations, and it can multiply either 32-bit floating-point data or 24-bit fixed-point data. The floating-point ALU consists of an 8-bit exponent arithmetic unit, a 47-bit bidirectional barrel shifter, and a 47-bit ALU associated with eight 56-bit working registers and two flag registers. It contains both a serial and a parallel I/O interface. The serial interface is used to link with codecs, DACs, and analog-to-digital converters, as well as for cascading multiple processors. The parallel interface supports the chip when operating as either a master CPU or an intelligent peripheral, or slave, processor. The chip executes a transversal filter function at 150 as per tap, or node, and a 512-point complex fast Fourier transform within 4.5 ns, about 15 times faster than similar functions done on current single-chip DSPs, according to the designers.

**BIG MEMORIES**

**DRAMs ADVANCE TO 4-Mb LEVEL**

Though this year's ISSCC cannot compete with last year's cornucopia of advanced memory designs, it is every bit as rich in quality and imagination. At the top of the list are two DRAM designs from Texas Instruments Inc., one a mask-programmable 1-Mb DRAM design and the other a 4-Mb circuit incorporating the company's new cross-point trench transistor cell.

Key to both designs is the company's advanced 1-µm twin-well CMOS process, which features clad moats and second-level gate polysilicon. The 1-Mb design has one level of aluminum interconnection, and the 4-Mb design has two. Lightly doped drains are used to suppress injection of hot electrons into the gate oxides, and simultaneous deposition of silicide on the moats and gate polysilicon provides low resistance and higher signal strength.

Using this process as the starting point, design manager Joseph Neal and his team at TI's advanced memory development group in Houston have developed a mask-programmable 1-Mb circuit that incorporates an imaginative combination of techniques aimed at achieving low cost, high reliability and testability, and high performance in a single design. The array in this 1-Mb design uses the company's contactless field plate cell that employs depletion-mode trenched capacitors and buried n⁺ bit lines with the top plate tied to ground for improved slew margins. Typical column-address access time is 20 ns. Read access time is 70 ns. Active power is 45 mA and standby is 0.8 mA.

At the circuit level, this design incorporates two techniques to improve reliability. One is a variation on the standard
approach, which incorporates redundancy circuits. The other is incorporation of several design-for-test modes.

Similar to other redundancy approaches, the TI technique uses laser-programmed fuses. In this design, however, the fuses are eliminated from the densely packed array section and located only in the periphery, where the extra spacing keeps damage to the silicon away from all critical nodes.

To implement the design-for-test methodology, each quadrant of the array is logically divided in half, resulting in eight miniarrays. Ten design-for-test modes can be initiated after the appropriate request from the tester: 8-bit parallel read, 8-bit parallel write, static refresh disturb, static and dynamic field leakage, external sense amp timing, redundancy roll call, sense amp margins, reset to memory mode, external oscillator to substrate voltage pump, and overvoltage detection.

To allow easy implementation of an 8-bit parallel read and write in the design-for-test mode, each miniarray communicates with the external I/O lines through an internal data I/O line. The 8 bits accessed on any cycle are separated by 256 columns, minimizing the interaction between selected cells. In the parallel read mode, the eight internal bits are compared against the expected data, which the tester enters through the data-in pin. If all bits agree, the expected data appears at the output. If there is disagreement, its complement appears. In the parallel write mode, all 8 bits are written simultaneously, with no restrictions on the data pattern that is applied during the parallel test.

The second aspect of this design is that Neal and his designers have incorporated a metal-mask option that allows the company to customize the memory to particular applications, instead of having to fabricate different circuits. In addition to configuring the array as either a 1-Mb-by-1-bit or a 256-K-by-4-bit array, the functional options also include page, static-column-decode, or serial modes. In addition, the 1-Mb-by-1-bit configuration has two additional options that allow it to operate in the nibble or byte modes.

Representing what the company believes to be the wave of the future in both memory and logic design is a 4-Mb DRAM (Fig. 6), a novel trench-transistor and folded-bit-line design [Electronics. Dec. 2, 1985, p. 50] that for the first time allows a true crosspoint memory array, according to Ashwin H. Shah, manager of TI's VLSI Design Lab Memory Concepts Group in Dallas. Using the same basic CMOS process with the addition of another aluminum interconnection level, the 4-Mb DRAM achieves its high density through the use of a trench transistor cell in which the charge is stored on the polysilicon plug inside the trench, and the pass transistor is formed around the collar of the trench, with the substrate forming the supply plate for the capacitor. The resulting cell size is only 8.9 \( \mu \text{m}^2 \) and the die size is 99.96 \( \text{nm}^2 \). Row-address access time is 150 ns, and access time is 30 ns in the static column-decode mode and 60 ns in the page mode.

To complement the trenchless transistor, Shah and his coworkers have implemented a unique double-ended adaptive folded bit line that allows a cell to be placed at every intersection of the word line and the segmented bit lines, a departure from the conventional segmented scheme. As a result, a word line selects two cells for every pair of global bit lines, one on each of the adjacent segmented bit lines, says Shah. These adjacent bit lines are connected to global bit lines through a special set of four segment-select transistor switches. When a word line is selected, the corresponding segment-select transistors are turned on and off, thus breaking each of the global bit-line pairs into two shorter bit lines. Each of these shorter bit lines is connected to sense amplifiers at each end. The selected segment-select transistors connect the segmented bit lines to the global bit lines such that each of the selected cell pairs is routed to one of the two sense amplifiers. The result is a density comparable to the open bit line but with all the advantages of a folded-bit-line architecture, says Shah.

The TI memory circuit is divided into four blocks of 1 Mb each, with odd and even row decoders located in the center. The sense amplifiers are divided into five rows, with three located between the array blocks and one each outside the top and bottom blocks.

The row decoders select word lines simultaneously in alternate blocks. This was done so that the inner sense amplifiers could be multiplexed, according to Shah. By contrast, the column decoders are embedded in the sense amplifiers and data line-driver circuits. This allows all 4 bits to be accessed from the same array of sense amplifiers and data-line drivers, reducing peak currents and power dissipation. To reduce the peak current surge, even further, the bit-line recovery during a read cycle has been staggered among the four blocks.

A more aggressive approach comes from NEC Corp., Kawasaki, Japan: a 4-Mb DRAM designed using a double-polycide NMOS process with 0.8-\( \mu \text{m} \) geometries, double-level polycide, and a single level of aluminum interconnection on a p/p++ epitaxial substrate.

### ONE-TRANSISTOR STRUCTURE

A key element in this design is the use of a new one-transistor, one-capacitor, buried-storage-electrode cell structure in which a storage capacitor is formed in a 5-\( \mu \text{m} \) deep trench measuring 0.8 by 1.2 \( \mu \text{m} \). A dielectric is then laid down on the inside wall of the trench, which is refilled with polysilicon. The polysilicon is then connected directly to the transfer transistor, which is fabricated in a 1.5-\( \mu \text{m} \)-thick p-type epitaxial layer on a p-substrate.
Such a design has its drawbacks. One is that it is difficult to control the high-voltage driving bit line that causes degradation of the gate cell transistors. Another is the voltage bounce of the cell capacitor electrode substrate, which results from the basic structure of the buried-structure-electrode transistor. Such problems are partially resolved by the way Masahide Takada and his co-workers at NEC have partitioned the internal memory into sixteen 256-K blocks, half of which are selectively activated during each access cycle, leaving the other blocks in the standby mode. This not only reduces power consumption but also suppresses the substrate voltage bounce to some extent. The design also incorporates internal voltage-converter circuitry that allows the limited voltage to be preset at a relatively low voltage, about 3 V, which enables constant voltage generation over a wider supply range without causing gate-cell degradation.

The results of such aggressive efforts have been mixed. On the one hand, typical access time—95 ns—is faster, and power consumption—425 mW active and 15 mW standby—is lower. But the die area—99.2 mm²—is not much smaller than TI's 4-Mb design, and the cell area—10.58 µm²—is about 20% larger.

Another entry in the still sparsely populated 4-Mb DRAM race is an experimental design from Toshiba's Semiconductor Device Engineering Laboratory and VLSI Research Center, Kawasaki. Fabricated using a 1-µm twin-tub CMOS process with two levels of polysilicon, one level of molybdenum, and one level of aluminum, the array is divided into eight 512-K blocks and consists of trench, n-channel depletion-type cells in a p-channel well. Using 3-µm-deep trenches, storage capacitance is 40 fF for a 17.4-µm² cell. At the center of each 512-K block are column decoders and sense amplifiers, allowing row-access times as low as 80 ns and column-access times in the 40-ns range. In the cell array, molybdenum polysilicon is used for the bit lines, and the word lines are made of aluminum and the second-level polysilicon. The first level of polysilicon is used for making the cell plate on the trench capacitor cell. Power consumption is 300 mW active, and 2.5 mW standby.

Also from Toshiba is one of the more imaginative designs: a 128-K-word-by-8-bit virtually static RAM, or VSRAM, that features typical address-access times of 62 ns with refresh, and 45 ns without refresh. Similar to "pseudo-static RAMs," this 1-Mb design incorporates all refresh circuitry on-chip. But unlike such designs, in which refresh operation is performed serially, the VSRAM is configured to allow the refresh operation to occur in parallel with either address decoding or output driving, when the word and bit lines are not occupied by normal access operation. Because the refresh operations are transparent to the user, the VSRAM frees users from thinking about refresh timing and the loss of time caused by refresh, according to its designers.

In this design, the on-chip refresh timer signals when a refresh operation is needed and generates a refresh-request signal intermittently. If the memory-cell array of the RAM is busy with a normal access, the refresh waits until the cell data is handed to a buffer register, which drives the output circuits. Similarly, a normal access request waits until the refresh operation ends.

Fabricated using a 1-µm twin-well CMOS process with double layers of polysilicon and aluminum, the VSRAM has an active power dissipation of 105 mW, 2 mW standby.

---

**FAST MEMORIES**

**RAMs PUSH TOWARD PICOSECOND SPEED**

Aside from the few high-density exceptions, most efforts in the design of both static and dynamic RAMS described at this year's ISSCC have focused on ever-higher speeds.

In the DRAM area, for example, designers have been pushing speeds toward 50 ns and below to eliminate the wait states between the slower memory and the inherently faster CPU access times. Two 1-Mb designs described at this conference have come close to this goal. One is a 65-ns CMOS design from Intel Corp., Hillsboro, Ore., that uses a 25.8-µm² transistor cell with self-aligned contacts where the array has been placed in an n-well to achieve access times of 65 ns. The other, from Toshiba Semiconductor, Kawasaki, Japan, uses a triple-polysilicon-layer n-well CMOS process to achieve an access time of 56 ns. And by eliminating the positive-going row-access signal edge from the internal timing, designers at Mitsubishi Electric Corp., Itami, Japan, have developed a 256-K CMOS DRAM with access times approaching 45 ns.

With SRAMs, the results have been even more impressive, especially at the 16-K level. From NEC Corp., Kanagawa, Japan, comes a 4-K-by-4-bit SRAM that features 4-ns access times and a power dissipation of 1.6 W. The memory uses 1.25-µm-polysilicon self-aligned process techniques in order to fabricate very shallow junction transistors with low collector-base capacitances, low base resistors, and a cutoff frequency of 9 GHz. The key element in the design is resistor loads formed from paralleled Schottky barrier diodes that offer high-speed switching characteristics. As previously implemented, this approach has not found popularity because of low density. However, the NEC designers have found that high densities are possible by using trench isolation—to allow closer spacing of the transistors—and two-layered polycrystalline silicon for interconnections and resistors. The result is a memory-cell size of only 700 µm², about half that of conventional resistor Schottky barrier diode-type cells and comparable to the size of typical bipolar memory cells with pn-transistor loads.

A similar 16-K design from Hitachi Ltd.'s Central Research Laboratory, Tokyo, features 3.5-ns access times, but at the cost of higher power dissipation—about 2 W. The key to this design is a 1-µm U-groove isolation process and a new memory cell fabricated with tantalum oxide film. The result is a cell of about 495 µm², 30% smaller than that of a conventional...
At the 64-K level, SRAM designers are using a variety of processes—CMOS, Bi-CMOS, and ECL—to push access times down to 10 to 15 ns. From IBM’s Research Center in Yorktown Heights, N. Y., and the company’s General Technology Division in Essex Junction, Vt., comes a 4-K-by-16-bit SRAM with an access time of 15 ns. It uses an advanced 1.35-μm CMOS process with silicide and single-level metal, thin p/p+ epitaxial layers, and a shallow retrograde n-well. The key to the circuit’s performance, however, is a new row and column decoder with two stages of decoding. The first stage is a NOR decoder with the higher-order address bits as inputs, and the second state is a two-input NAND decoder with the output of the NOR decoder as one input and either the true or complement of the least significant bit as the other. Nominal delay times through the two-stage decoder, from the rising of the higher-order address bits to the word line rising, is 2.6 ns.

Using a combination of ECL and Bi-CMOS, researchers from Hitachi Ltd.’s Device Development Center, Tokyo, have produced a 64-K SRAM that features a 13-ns access time, with an active power of about 500 mW—about half that of a conventional 64-K bipolar ECL RAM (Fig. 7).

Standby power is 350 mW. In the memory array, each cell has four n-MOS transistors with two high-resistance polysilicon loads. The word-driver circuit used to drive a word line with a high load capacitance, however, is fabricated with a combination gate consisting of buried twin-well CMOS transistors and bipolar transistors with a 4-GHz cutoff frequency. To minimize delay time in the data line, a special control circuit reduces the signal-voltage swing level of the common data lines to no more than 30 mV. This small signal is propagated directly to a full bipolar ECL output circuit through a bipolar differential sense amplifier.

However, comparable speeds have been obtained in two 64-K SRAs from Motorola Inc.’s MOS Memory Group in Phoenix, Ariz. (Fig. 8). Moreover, the 13-ns access times are achieved with an active power of only 100 mW at 40 MHz. Fabricated using a double-polysilicon, double-metal, 1.5-μm p-well CMOS process with graded drains, these devices gain their speed improvement through a new SRAM architecture that allows the use of extremely short bit lines with only 64 cells per line. A vital element in this architecture is the use of low-capacitance bit lines, decoded onto 16 local operational amplifiers that drive four global data lines. These global data lines are fed into second-stage analog amplifiers that have the capability of either 64-K-by-1-bit or 16-K-by-4-bit configurations. The local op amps are n-channel devices with p-loads, while the second-stage amplifiers use p-channel devices with n-loads. And because the two circuits are P/N complements of each other, there is optimum matching of common-mode I/O levels. Utilizing a combination of ECL and Bi-CMOS, Motorola combines traditional CMOS with new array architecture for its version of a 13-ns 16-K-by-4-bit SRAM. The access times are achieved with an active power of only 100 mW at 40 MHz.

Schottky barrier diode capacitor cell.

At the 256-K level, researchers in the semiconductor group at Sony Corp., Kanagawa, have achieved access times as low as 30 ns in a full-CMOS design, combining 1-μm design rules, a retrograded p-well structure, and n-channel transistors with lightly doped drains. The effective channel length of the transistors is 0.8 μm with a gate-oxide thickness of 200 Å.

Utilizing a divided-word-line scheme, in which the memory array is divided into 16 sections, only one section is activated at a time; the others remain in a standby state. The result is an active power dissipation of 85 mW at 10 MHz and only 500 mW on standby. The key to the design is a unique readout scheme in which a single-stage sense amplifier, consisting of a current mirror differential amplifier and a CMOS inverter, is placed at every four columns in each section. Because one sense amplifier is connected to only four pairs of bit lines, the data-line capacitance is very small, enabling rapid sensing of information on the selected bit lines within each section.

Designers from NEC Corp. have gone one step further with a 25-ns 256-K-by-1-bit SRAM, based on a high-performance, short-channel, double-aluminum-interconnection-level CMOS process employing n- and p-channel transistors with channel lengths of 1.3 and 1.7 μm, respectively. To squeeze as much speed as possible out of the process, the SRAM uses a unique array layout: 256 rows and 1,024 columns. In this design, two-bit-line circuits share 256 memory cells, while a main word line, made of the top aluminum interconnect layer, distributes word-select signals to 32 short block word lines, made of polycide, each of which controls 32 memory cells. This configuration reduces the word-line delay to about half that required in conventional 512-by-512-bit SRAMS, and the bit-line delay is reduced by 30%. In addition, power dissipation is reduced to 350 mW active and 10 mW standby, 1/32 the amount of conventional designs.
Unlikely many of this year’s memory and analog designs, which focus on evolutionary improvements in circuit design and processing, a few reconfigurable gate arrays and semicustom logic arrays represent efforts to push toward the limits in optimum power/speed tradeoffs.

Representative of the first trend is an offering from National Semiconductor Corp., Santa Clara, Calif., that uses both bipolar and CMOS techniques to fabricate a 16-input, 8-output, 64-product-term, field-programmable logic array circuit (Fig. 9). In this approach, a standard junction-isolated bipolar process is merged with a standard local-oxidation CMOS process to form partially isolated bipolar transistors, p-channel CMOS structures isolated in an n-type epitaxial layer, and n-channel devices in p-isolation regions (Fig. 10).

A mixed process was chosen to take advantage of the company’s tungsten-fuse technology for the field-programmable elements. Bipolar npn transistors are used in a combined bipolar-CMOS sense amplifier and in an internal data latch that holds the state of the AND/OR terms when the part goes into the standby mode. Typical propagation delay through the array is 24 ns, with an active power dissipation of 625 mW, and 5 mW standby.

Altera Corp. has developed a family of CMOS electrically programmable logic devices with the equivalent of 2,000 gates. Using Intel Corp.’s CHMOS-HE erasable programmable read-only memory technology, the Santa Clara company plans to introduce the devices as the EP1800 family. The line incorporates some novel circuits to provide zero standby power and optimum speed, including an input transition detector to power up bit lines, sense amplifiers, and data latches; an unbalanced latch that captures the programmed state of the architecture EPROM bit during power up but consumes no dc power; and amplifiers that combine sensing and NOR functions to reduce layout area and increase speed.

At the other end of the spectrum are efforts to push semicustom arrays toward their speed limits through the use of such materials as gallium arsenide. From NEC Corp., Kawasaki, Japan, comes the prototype design of a current-mode-logic-compatible GaAs array with a 3,000-gate density, gate delays in the 50- to 200-ps range and data rates up to 1.32 Gb/s (Fig. 11).

Such density and performance has been achieved through the use of the company’s sidewall-assisted self-alignment technology, in which tungsten silicide gates are used in combination with the GaAs FET structures in order to suppress the short-channel effect and decrease the gate capacitance. Active layers for the FETs, diodes, and electrodes were formed using selective Si. In the internal array, two buffer FET logic gates using depletion-type FETs are combined with level shift diodes to form the basic four-input NOR-gate circuit. Each cell in the array contains 14

9. BIMOS PLA. In a new family of programmable logic, National Semiconductor Corp. combines a bipolar logic array with CMOS circuitry to fabricate a 16-input, 64-product-term, 8-output field PLA.
GaAs ARRAY. Using its sidewall-assisted self-alignment process, NEC achieves 3,000-gate density and gate delays in the 50 to 200-ps range in a gallium arsenide array.

Designed using 2.2-μm line widths, the gate array contains 1,500 basic cells (3,000 buffered-FET logic, four-input NOR gates), 48 input buffers, and 48 1/O buffers—the equivalent of about 23,000 FET structures. Using 2-μm line lengths and fan-outs of 3, the propagation delay time per gate is 134 ps with a power dissipation of 4.6 mW per gate.

From TI's Central Research Laboratory in Dallas comes a 4,000-gate bipolar GaAs array. Using a critical feature size of 5 μm, the gate array is fabricated on an n+ GaAs substrate with an aluminum gallium arsenide emitter and GaAs base and collector, all grown with molecular-beam epitaxy. Instead of using all grown junctions, the necessary p-type base and extended p-base contacts were achieved using a beryllium ion implant.

The basic gate cell was implemented using a variation of the heterojunction inverted transistor integrated-logic technique TI has had under development since 1980. Researchers were able to quadruple the equivalent gate density from 1,000 to 4,000, separating the switching transistors in the basic cell from the output Schottky diodes with two isolated moats, which allowed the gate to be moved closer together. In addition, a second level of interconnection has been added, and the Schottky diodes have been stacked on top of the collector. At 0.2 mW per gate, propagation delay per gate with a fan-out of 4 was 1.25 ns. At 1 mW per gate, propagation delay is improved threefold—down to 400 ps per gate.

ANALOG

ICs SHOW OFF A NEW SOPHISTICATION

Oining almost every other category at this year's ISSCC in terms of total number of papers—22 out of 86—and number of sessions—four—are the analog circuit designs. The voiceband communications ICs described at the meeting come closest to the digital and memory superchips in terms of complexity and sophistication.

From Oki Electric Industry Co., Tokyo, comes a single-chip analog front end for 1,200- and 2,400-b/s modems that contains analog-to-digital and digital-to-analog converters, microprocessor interface logic, 50-pole filters and equalization circuitry, tone generators, and a call-progress detection filter in a 6.5-by-6.37-mm² area. Fabricated using a 5-μm polysilicon-gate CMOS process, the circuit has 80 amplifiers and 1,100 logic gates, and it dissipates 100 mW.

France, is offering a three-chip full-duplex analog front-end chip set for split-band and echo-cancelling modems, fabricated using 4-μm CMOS. The chip set performs both ADC and DAC functions, analog subtraction of replicated echo signals, filtering, automatic gain control, and analog carrier detection for split-band modems up to 2,400 baud and for echo-cancelling modems up to 16,800 baud.

Equally impressive is the monolithic data-access and line-interface IC for modems and private-branch-exchange trunk lines from Harris Semiconductor Corp., Melbourne, Fla. Fabricated using a 200-V bipolar process, the circuit incorporates on-chip radio-frequency modulation to isolate capacitively up to 1,500 V on the line and uses electrothermal techniques to transfer supervisory information.

Data-conversion circuitry is also still very much alive at this year's meeting. From Digital Equipment Corp., Maynard, Mass., comes a triple 4-bit video DAC with on-chip video shift registers, palette memory, and cursor logic. Fabricated using a 2-μm CMOS process, it can drive 75-Ω cables directly at pixel rates up to 106 MHz with a full settling time of only 4 ns.

Aiming at a different set of applications is an 80-MHz 8-bit DAC from Mitsubishi Electric Corp., Hyogo, Japan, a current-switching design fabricated using a 2-μm CMOS process. In the analog-to-digital area, Hewlett-Packard Co., Palo Alto, is offering an 8-bit ADC, fabricated with a 5-GHz oxide-isolated bipolar process, that features a full power bandwidth rating of 125 MHz and a power dissipation of 12 W.

A 3.5-μm CMOS slope- adaptive delta-modulation ADC configuration from the Massachusetts Institute of Technology, Cambridge, features a dynamic range of 90 dB in the audio band, 15 bits of resolution, and total harmonic distortion of only 0.17% at 1 MHz. Featuring 11-bit linearity and resolution is a 120-kHz sigma/delta ADC from Siemens AG of Munich, with a 15-MHz clock rate. And Harris Semiconductor offers an ADC design that incorporates a unique digital error-correction scheme to increase the speed of successive-approximation operations from 12 to 7 μs.

Finally, optical data communications is coming into its own this year. In an entire session devoted to this subject, three designs from AT&T Co. promise to attract attention: a 2-Gb/s n-MOS laser-driver IC from AT&T Bell Laboratories in Holmdel, N. J.; a 50-Mb/s CMOS light-emitting-diode driver circuit from Bell Labs in Allentown, Pa.; and a 50-Mb/s CMOS optical-data-link receiver circuit from Bell Labs in Reading, Pa.

Of the three, the design that most closely approaches superchip status is the 2-Gb laser driver, a 1-μm n-MOS device fabricated using ultraviolet lithographic techniques. The circuit consists of three differential amplifiers and two pairs of source-follower buffers in which two diode-connected MOS FETs set the voltage gain of the input stage and properly bias the succeeding O-decoupled, nonsaturating gain stages. Depletion-mode MOS FETs are wired in parallel with the diode-connected MOS FETs to increase the drain current of input drivers, thus increasing overall gain. When driving a 25-Ω load, rise and fall time of the circuit is about 320 ps, which can be improved by almost 40%, to 200 ps.
A Powerful Set of
for VME Applications

A Powerful Set of for VME Applications

Powerful VME Hardware
- 32 Bit MC68000 processor
- 1 MByte DRAM with byte parity
- Up to 64 KByte EPROM space
- Intelligent mass storage controller for floppy disks, hard disks and tape drive
- Three RS232C serial ports
- 40 programmable I/O lines
- VMEbus to Intelligent I/O Channel converter

Open System Architecture
- 19" desktop housing
- 200 W power supply
- 9 slot VMEbus + rear card cage
- 6 slot Intelligent I/O Channel (IIOC) rear card cage
- Single high Eurocards in industry quality full VMEbus/IOC compatible

All Software Tools for Real-Time Applications
- Choice between OS-9/68000 or VERSAdos multi-tasking, multi-user operating systems
- C compiler, PASCAL compiler
- MC68000 macro assembler, Linker
- Screen editor
- Symbolic debugger
- Debugging monitor firmware with line assembler/disassembler
- Driver software for standard PEP modules

Extensive Mass Storage
- 640 KByte formatted DSDD floppy disk drive, half-height 5¼"
- 20 MByte formatted hard disk drive, half-height 3¼"
- 25 MByte formatted tape drive full-height for ¼" tape cartridge

For $ 8,9... Ask for our

We have the Complete OEM Product R...
Flexible System Expansion
- 5 spare VMEbus P1 slots
- 5 spare I/O C slots
- 200 W power supply
- Space for full-height 25 MByte tape drive
- More than 100 OEM modules for VMEbus/I/O C available

Plus
- Worldwide support and service through our dedicated technical specialists
- Extensive software support
- Integration of your target system in the development system saves costs for in-circuit emulation
- Easy switch between operating systems without any hardware/firmware changes
- Development tools and OEM modules for 8 bit applications
- Intelligent I/O Channel supports local CPUs

One Choice of two Options
Option 1:
Complete VME development system with OS-9/68000

Option 2:
Complete VME development system with VERSAdos

Either option 1 or 2 includes:
- Screen editor, 68000 macro assembler/linker, symbolic debugger
- C compiler, driver software for standard PEP modules, VME debugging monitor firmware with line assembler/disassembler full documentation

Also recommended but not included:
PASCAL compiler
EPROM programmer
CRT2000 terminal
ST2000 tape drive
Our new AD7572 12-bit, 5μs CMOS A/D Converter.

Analog's new 12-bit ADC dissipates a mere 135 milliwatts. Low enough, in fact, to allow us to fit the AD7572 into a narrow 0.3" 24-pin DIP, or an even smaller 28-pin LCC. So you have a mini-package that saves board space. With no worries about the heat buildup associated with 1100 milliwatt hybrid ADCs.

The "blistering speed" of the AD7572 also means very fast 90 ns bus access time. So you can forget the hardware or software fixes normally required to compensate for slow (or non-existent) ADC bus interface logic. At last, you have a µP compatible converter that is truly µP compatible.

Also, for ease of design-in, consider the AD7572's flexible logic interface. It allows data to be taken as a full 12-bit parallel word, or in two bytes (8 bits + 4 bits).

There's more. The AD7572 features a stable on-chip buried Zener reference that eliminates the hassle of adding external components. All this at a price that settles the "make or buy" argument once and for all. In quantities of 1,000, 5μs versions from $39.10 and 12.5μs versions from $29.75.

Getting all this speed without the blistering heat into our A/D Converter is our main business. Ordering the easy to design-in AD7572 is good for your business. Do it with blistering speed.

Contact us for more information by calling Applications Engineering (617) 329-4700 Ext. 3596 or 3597 or write Analog Devices, P.O. Box 280, Norwood, MA 02062.

Analog Devices, Inc., Two Technology Way, Norwood, MA 02062-0280; Headquarters: (617) 329-4700; California: (714) 643-9391; (619) 268-6626; (408) 947-0633; Colorado: (303) 590-8000; Illinois: (312) 653-5000; Maryland: (301) 992-1994; New York: (716) 475-4101; (315) 643-5777; Ohio: (440) 764-6775; Pennsylvania: (215) 643-7790; Texas: (214) 231-5094; (713) 664-6704; Washington (202) 251-9550; Beijin: (8) 237 4013; Devlinark: (212) 950-5600; France: (1) 687-34-11; Holland: (1626) 40900, Isam: (0) 282740; Italy: (22) 315760; Japan: (3) 283 6826; Sweden: (8) 283 250; Switzerland: (22) 35 16 60, United Kingdom: (01) 940466, West Germany: (09) 570950

Blistering speed without blistering heat.
A NEW TESTER CHECKS ANALOG AND DIGITAL SIGNALS SIMULTANEOUSLY

The Small Computer System Interface (SCSI) protocol may have given computer makers an easier way to add a disk drive to their products, but it also created a whole new set of testing problems. It is no longer enough for a tester to test a system's peripherals piecemeal. A tester now has to gain access to the test points inside the drive, between the on-board controller and the intelligent interface, to check its operation and to test the phase margin of signals from the head and disk assembly, read/write channel, phase-locked loop, and signal decoder. Equally important is a thorough test of the data flow through the interface with the computer.

Such testing requires breaking into the data path at the interface of the analog and digital signals, which is difficult because both signal types must be tested simultaneously. The problem is compounded if the test points are buried inside a custom large-scale-integration chip. To test complete systems and provide access to the necessary test points, Flexstar Corp. has designed a product that correlates information from various points in the data path to give a coherent measurement of the system's parameters.

The FS6000 tester from the Milpitas, Calif., company has a TECHNOLOGY TO WATCH is a regular feature of Electronics that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.

1. SYSTEM TESTER. Flexstar's FS6000 tests signals from different points along the data path within the Winchester disk drive to evaluate the entire system. The data-margining card is the system's actual test element.
2. BINDING ARBITRATION. An arbiter on the data-margining card chooses between the evaluation of early or late delay and checks the phase margin.

The signal-pickup card, data-margining card, and tester control card (Fig. 1). The signal-pickup card is customized to match the physical layout and logic levels of the drive model that is to be tested. It typically mates directly to a test connector on the drive and contains only signal buffers.

The data-margining card is the actual test element. It contains an arbiter circuit, fixed clock-delay circuit, and two programmable data-delay circuits—all of which check the drive's phase margin. Additional circuitry calibrates the programmable delays and checks the amplitude margin (Fig. 2).

Using the drive interface, the tester control card issues such commands as seek, write, and read. It also controls such test functions as margin testing with the data-margining card, data-error detector, logger, and various timing measurements. In disk-drive subsystems, analog data from the disk read/write head goes through a zero-crossing differentiator, or pulse detector, and is digitized. The digitized signal then travels to the PLL, where a clock signal is generated. The decoder uses the clock signal to extract the data. The FS6000's signal-

"We are not only testing the read/write channel but also the head and disk assembly, the PLL, and decoder in total," says George Robinson, Flexstar's president. "Let's assume that the read/write channel is perfect but there is a problem with the PLL. The PLL is part of the data path and it can have its own errors, like not locking directly to the center of the ideal bit position. If this occurs, the phase-locked loop decreases the margin."

3. PHASE MARGINING. The system splits a data pulse into ascending and descending segments and sends them through the proper delay circuit.

36 Electronics/February 17, 1986
Other testing includes missing pulse detection and extra pulse detection for media defect mapping.

But to test a whole system, it is necessary to measure the timing of events on the bus and making sure that they fall inside the limits of the SCSI specification. It also means checking all the SCSI commands to ensure they function properly.

“One difficulty with SCSI is testing its bus arbitration capability,” says John Hoeppner, vice president of operations. “The tester is trying to emulate both sides of the SCSI bus. In one instance, it’s emulating a host interface or the initiator function, but it must also emulate the target function on the SCSI bus in certain test modes.”

To the system, the tester is just another device on the bus. But this device tests the ability of the other devices on the bus to arbitrate. The SCSI bus can support up to eight devices, and all can try to arbitrate at the same time. If contention arises, the tester must determine which device is not arbitrating correctly. In checking the bus, the tester transmits a set of commands and receives status messages that indicate whether the bus is operating correctly.

Other bus testing includes measuring the timing of certain signals. The tester selects the timing events to be measured, creates the appropriate conditions, and records the results. The tester also checks for opens and shorts on the bus.

Ultimately, the bus testing is to check compliance with the SCSI protocol. At present, however, the peripherals manufacturer will not be testing for a full implementation of the SCSI, says Robinson. “The current generation of disk drives will not support full bus arbitration. Even though there are variations of the SCSI, most disk drive manufacturers are agreeing to support what is called the common command set of the SCSI on their individual products.” There will be implementations outside the common command set, either for the company’s own diagnostic purposes or for different devices.

The common command set is intended mainly for Winchester disk drives. Flexstar will support the set on its tester; it also plans to provide the user with an editor to establish his own set of commands. The common-command-set test is stored in read-only memory; the customer stores special commands in electrically erasable programmable ROM.

Flexstar’s experience with the Extended Storage Device interface, which has the same margin-testing requirements and problems as the SCSI, “is that 60% to 70% of the drives on the market allow our kind of testing,” says Susan Brousseau, marketing vice president. SCSI drives are still in development, so few have been shipped in quantity.

The company also plans to accommodate systems in which test points are buried in silicon. In that approach, the tester is inserted between the head and disk assembly and the controller. To check the head and disk assembly, the tester simulates the controller function. To check the controller, the tester simulates the drive.

Another method of checking buried test points involves inducing a phase shift in the analog data signal coming off the disk read/write channel—although it is not precisely known how the zero-crossing detector will react to the phase-shifted signal. Flexstar’s designers rejected this method because it may not be sufficiently accurate for resolution in the 100-ps range.

Yet another way to test intelligent interface drives without actually probing in the data path is to perform a margin test on the raw data using an external PLL. Hoeppner says this method does provide a test of the head and disk interface, but it does not perform a functional test of the drive in total. For example, propagation delays inside the decoder and other parameters are not tested.

To be sure the drive can be expected to operate reliably over the long term, the manufacturer has to probe inside the drive and determine the margins of components in the critical read/write channel inside the head/disk assembly and in the sensitive phase-locked loop. “These components make or break a drive,” Robinson says.

The growth of the test equipment division has financed much of the privately held company’s growth. Early on, the founders had looked for outside investors. “We went out looking for funding for the company during a time when there was plenty of venture money available, and we had no takers,” Brousseau says. Disk-drive testers must not have had the glamour of thin-film media or startup disk drive companies. However, she adds, once the disk-drive tester started to sell, “venture money came looking for us. By that time, we found we could finance the company ourselves.”

WHEN THEY COULDN’T FIND THE RIGHT TESTER, THEY BUILT ONE

Testing disk drives is something Flexstar Corp. founders, George Robinson and John Hoeppner, have been doing for a long time. Robinson headed the worldwide service and maintenance operations at Shugart Corp., where Hoeppner was responsible for controller and test equipment development. In 1982, when Shugart’s glory days were waning, the two founded Flexstar to repair floppy-disk drives. They were joined by Susan Brousseau, who had been the Western region sales engineer for Shugart responsible for sales of Winchester and floppy-disk drives.

The three soon realized that floppy disks were quickly becoming commodity products, so they broadened their service to include repair of Winchester disk drives as well. “In repairing disk drives, we realized that there was no commercially available test equipment that could provide both analog and digital testing together,” Robinson says. Moreover, they found that they needed an accurate tester. They decided to develop their own.

“We knew we had to build a test system that produced consistent results that could be accurately correlated over time and between different test systems,” Hoeppner says. The company came up with a self-calibrating tester for ST-506 disk drives, which checks its accuracy against a precision crystal and factors out the error before each measurement.

Now the company has developed the FS6000 for testing intelligent disk drives and is pushing the drive manufacturers to make the necessary test points available for such checks. “A manufacturer cannot test these new disk drives at the intelligent interface to see if all the commands and signal lines work,” Hoeppner explains. “Many drives with marginal operating characteristics would pass [a less thorough] test easily, only to fail six months later in the customer’s system.”

To be sure the drive can be expected to operate reliably over the long term, the manufacturer has to probe inside the drive and determine the margins of components in the critical read/write channel inside the head/disk assembly and in the sensitive phase-locked loop. “These components make or break a drive,” Robinson says.

Electronics / February 17, 1986
t long last, U.S. makers of integrated circuits are embracing tape automated bonding as an assembly and interconnection method. And for Thomas L. Angelucci, who has struggled for 15 years to get it off the ground in the U.S., TAB's rising popularity is sweet victory.

The main reason for TAB's flowering is the appearance of high-speed very large-scale ICs with upward of 100 leads. Without TAB to bond bare ICs to spidery copper patterns on sprocketed frames of polyimide film, these advanced chips simply cannot be assembled and tested; nor can they work to their maximum capability.

Angelucci stands to reap big benefits. The TAB pioneer is president and chief executive officer of International Micro Industries, Cherry Hill, N.J. The 50-employee company is perhaps the only fully vertically integrated TAB company in existence. It can supply the whole spectrum of equipment and supplies—bare and etched tape, inner- and outer-lead mass bonders, and plating machines for bumping wafers—and can even do contract TAB assembly. Other companies, such as 3M, Microbond, and Messi, supply tape only. Another, Jade Corp. of Huntington Valley, Pa., concentrates on inner- and outer-lead TAB bonders.

Ever bullish on TAB, Angelucci predicts that in five years, 30% to 50% of all chip interconnections will use the technology. In fact, IMI has compiled a data base of TAB applications worldwide that contains 300 applications, and Angelucci expects to add more this year.

International Micro Industries is very much a family affair, involving Tom, his cousin, Joseph L., executive vice president, and his brother, Nicholas K., vice president of sales. Tom and Joe, both longtime employees of equipment maker Kulicke & Soffa Industries Inc. in Horsham, Pa., had extensive experience in mechanical engineering and design, and they thought enough of TAB to start their own company in October 1971. Their first product was an inner-lead bonder for bonding chips to tape.

The machine was shown to Fairchild, General Electric, Honeywell, Motorola, National Semiconductor, and Texas Instruments, the only companies interested in TAB at that time. But as Tom recalls, "We very quickly found that nobody was making tape for our machine. We were in the position of making a great gun with no source of bullets."

So IMI went looking for ammunition. Tom and Joe approached Eastman Kodak Co. and F. I. du Pont de Nemours & Co. to try to sell them on the idea of producing sprocketed polyimide film for the infant technique. Kodak turned thumbs down because it feared that polyimide films might contami- nate its entire photographic-film operation.

But it chanced that du Pont was deciding to get out of the photo-film business, and it sold IMI 15 machines for perforating films. IMI adapted them to its own needs for slitting and sprocketing and within a year was in the tape business, purchasing its polyimide raw materials from du Pont.

IMI managed to hold its own in whatever TAB business was available through 1975. The action consisted predominantly of TAB assembly of low-power Schottky devices fitted onto TAB film before being put into 14-pin plastic dual-in-line packages. Schottky parts were in heavy demand at the time, and an automated process such as TAB could handle high volumes. The introduction of the first fast, fully automatic wire bonders from Kulicke & Soffa, however, took some of the wind out of TAB's sails. The wire-bonding machines were more cost-effective than TAB in "jelly bean" types of assembly work—that is, turning out hundreds of thousands of devices.

JAPAN TAKES NOTICE

By that time, the Japanese had begun to take a strong interest in TAB. "We began being contacted by Japanese firms" around 1972, says Tom Angelucci. First was Sharp, quickly followed by Hitachi, Mitsubishi, Toshiba, and Seiko. The next step was predictable: in the next few years, those companies made TAB a force in Japan, particularly in such consumer products as calculators and watches. Through it all, TAB languished in the U.S., as big companies such as Amp Inc. and Rogers Corp. got in and out of the business.

Even though IMI did sell several TAB machines to Japanese companies at the time, Tom did so reluctantly, sensing that they simply served to set up competitors. In fact, to this day
he believes "there is no lasting business in Japan unless you make something they can't produce or make." So IMI does very little business in Japan.

In the U.S., meanwhile, ICs were moving toward very large-scale integration, and by the early 1980s, these VLSI chips began to proliferate. A big assist came from the Defense Department's Very High Speed Integrated Circuits program. The new chips bristled with 100 to 300 leads and operated at data rates ranging from 25 to 50 MHz. Suddenly, a host of new forces began to awaken the TAB business in the U.S., as it appeared to be the only way to work with those multi-

leaded chips.

Angelucci says that the sheer number of leads in VHSIC chips makes wire bonding impractical. For example, wire bonding typically produces a 98% yield of good bonds. So in a 50-pad chip requiring 100 bonds, two could be bad, and as the lead count goes even higher, so does the number of bad bonds. The only satisfactory alternative is TAB, where leads are mass bonded with a thermode tool that results in 100% yield.

Another force driving TAB to the fore is testability. With TAB, chips can be tested and even burned-in on tape before final assembly on substrates. Also, tape-bonded chips can be tested by probing their tape leads rather than with a probe wire, which risks scratching a high-priced chip. Even bond pads are becoming a factor. In the early 1970s, 14 pads measuring 4 by 4 mils on 4-mil spaces posed no problem because plenty of surface area was available for circuitry. But nowadays, chip size actually can be limited by circuit density than by the excessive amount of chip surface used for hundreds of wire-bond pads. With TAB, it is possible to go to 2-by-2-mil bumped pads.

Also favoring TAB is its potential for high-speed performance. Above 50 MHz, a round wire, typical of wire bonding, has too much lead inductance. At such frequencies the preferred beam shape is rectangular, which is inherent with TAB.

Finally, an often overlooked advantage of TAB is its increased chip hermeticity due to bumped input/output pads. The bump's added metallization layers prevent intermetallic corrosion, which is responsible for 60% of all field failures in plastic-packaged ICs, according to a study by RCA Corp.

NEW DIRECTIONS

IMI has parlayed these benefits into a strong position in the industry while coming up with innovations such as three-layer testable tape and, more recently, a bumping process that can be used for either TAB or flip-chip bonding. But the company's latest development, multichip TAB, could have a significant effect on high-speed, high-density packaging in general.

In this system, which is to be used on a VHSIC package by Texas Instruments Inc., an advanced tape structure with multiconductive layers, called Multitab, linearly joins two or more TAB tapes in synchronous sprocket-hole alignment. All conductive layers are interconnected by a deflected conductive lead. The novel structure eliminates expensive thick-film multilayer hybrids, plated through-holes, and crossovers. In addition, it allows individual test or programming of each chip because the lines between chips are open until the deflected leads are connected.

IMI is currently producing a state-of-the-art three-layer tape with 2-mil lines and spaces etched from 1-mil copper. This is a considerable advance in printed-circuit-board imaging and lithography, says Angelucci, because today's rigid and flexible production-variety pc boards are about at the 5-mil line and space plateau.

And tape is getting wider. Though most types are still in 35-mm formats, the dual drivers of VHSIC and multilayer TAB are pushing 70-mm tape to the fore because 35-mm types can't accommodate the latest generation of chips with more than 200 leads. For example, IMI has demonstrated a 224-lead TAB frame in that width. Perhaps two years away are 105- and 140-mm tapes, to be used for even larger ICs and perhaps as tape motherboards for multilayer TAB applications. Still another development that could lead to lower-cost tape is the possible use of 4-mil-thick epoxy film instead of polyimide. This film, still in development, could cut tape prices in half.

Stil to be decided, as chip lead counts gradually grow past the 300-lead barrier, is whether TAB interconnections will be peripheral (that is, with leads along the periphery) or area (where a multilayer tape provides an interconnection between the grid of solder bumps of a VLSI chip and the bonding pads of a ceramic package). Angelucci favors the peripheral type.

IMI's experts believe area TAB interconnection will be rejected by the military—a major customer—because the bonds cannot be inspected visually to check conformance to military standards. Aligning, bonding, viewing, examining, and confirming a bond connection through a distorted polyimide film is nearly impossible. Also, with area TAB, leads can cause bonding problems because the polymer film above and around the copper leads can overheat, expand, and delaminate them.

Angelucci still has not run out of ideas or nerve. For example, he is convinced that the largest single TAB application five years from now will be in smart cards, the plastic credit cards with embedded memory or microprocessor chips, a market that has not yet taken off in the U.S. The upshot is that his company is backing a new operation he started up in 1983—Smart Card Systems Inc. With the aid of IMI's multilayer TAB—better suited than peripheral or area TAB for multichip jobs, such as smart cards—it has successfully demonstrated smart-card assemblies carrying both an 8-bit microprocessor and a 64-K electrically erasable programmable read-only memory. Whatever the payoff, Angelucci hopes that it won't take another 15 years.

**TABBED.** The popular Intel 8086 microprocessor chip bonded to an IMI tape. The lead attachments are gold to gold.

**DENSTER TAB.** Area TAB combines the flip-chip and tape automated bonding technologies for an extremely dense interconnection.
ARE EEPROMS FINALLY READY TO TAKE OFF?

A BIG DISAPPOINTMENT SO FAR, THE NONVOLATILE MEMORY GETS DENSER

by J. Robert Lineback

DALLAS

One of the biggest disappointments of late in the semiconductor business is the electrically erasable programmable read-only memory. It turns out that the EEPROM market did not take off as most forecasters originally had predicted because there were not enough products and what was being turned out came from too few makers. Not only that, but EEPROM prices didn’t come down fast enough.

Makers were also far too optimistic. “People in the EEPROM market brought some of the doubts upon themselves by projecting back in 1981 and 1982 that this business would reach $1 billion annually by 1985 and 1986,” says James Oliphant, marketing manager for Xicor Inc., San Jose, Calif., EEPROM manufacturer.

Now, a growing number of manufacturers and market researchers believe the EEPROM is finally about to take off with the same pizzazz they had originally expected. As late as two years ago, Dataquest Inc., like many of the manufacturers, was still predicting a booming EEPROM market. The San Jose, Calif., market researcher expected global sales to reach $373 million in 1985 and $583 million this year. Now it is being more conservative. Dataquest estimates that worldwide shipments of EEPROMs last year hit only $158 million, and will grow in 1986 to just $185 million (chart). “The industry has been a little overoptimistic and things have had to be adjusted down a bit,” acknowledges Susan Scibetta, a Dataquest researcher.

“EEPROMs have also turned out to be the kind of part that cannot be used just to replace an existing technology, namely the ultraviolet-light-erasable PROMs,” she says. Makers are now hotly pursuing new designs such as the flash EEPROM as one means of making this product live up to its unfulfilled promise as a replacement part to UV-PROMs. Notes Dan McCranie, marketing vice president of Seeq Technology Inc., San Jose, Calif.: “In 1981 and 1982, when Seeq and Xicor were going heavily into EEPROMs, it was our impression that we would eventually make them at the same price as EPROMs, and once we did, there would be a cannibalization of the very large EPROM. Obviously, that did not occur and that is what kept EEPROMs from being the billion-dollar market.”

But McCranie, Dataquest, and a growing number of manufacturers believe that EEPROMs are finally going to take off now as they had originally expected. True, some EEPROM veterans are even rethinking their stake in this business. But new players keep moving into the field. Most of them are aiming at higher-density parts, and all agree that EEPROM’s market potential has barely been scratched. “There are more companies getting into the market and a wider acceptance by major customers,” Scibetta says. Also expected to help matters are the new 256-K EEPROMs and ultimately the new low-cost designs.

SAFE HAVEN? The less than dazzling start has taken a toll as recession-plagued chip makers divvy up engineering and manufacturing resources. Though more chip producers are viewing EEPROMs as a safe haven from the price wars of commodity markets, some early entrants are having second thoughts. Inmos Corp. put its 64-K EEPROM, the IMS 3630, “on the back burner,” says product marketing manager Douglas M. Mitchell. The Colorado Springs company believes lithium batteries packaged with CMOS static random-access memories offer a more attractive solution for nonvolatile storage.

In Austin, Texas, Motorola Inc. wonders if EEPROMs are the one exception to the bigger-is-better memory rule, says John Barnes, director of memory design. With small blocks of EEPROM storage—especially onboard monolithic microcomputers—systems can automatically reconfigure software and the work they perform. System reconfiguration typically requires smaller blocks of storage than applications aimed at replacing volatile RAMs or EPROMs, he notes.

Motorola has halted production of its 32-K EEPROM and this year began handing out samples of its new 64-K chip, the MCM2864, to see if the commercial marketplace is ready. “The search is still on as far as I’m concerned,” Barnes adds. He says the major hurdles still facing EEPROMs are high prices compared to EPROMs, slow erase-rewrite speeds, lagging transitions from n-MOS to CMOS, and perhaps most important, reliability limitations on the number of write cycles to the array.

Conventional thin oxide wears away after repeated write cycles, eventually causing some bad cells in the array. Typically, only a few cells become unreliable. Thicker oxides and cell-swapping redundancy schemes are being used to ensure longer lifetimes in some high-density EEPROMs. But Barnes believes these schemes make it more difficult to lower the cost of full-featured EEPROMs that can compete directly with EPROMs.
Still, Motorola is more than willing to step up its EEPROM production if greater commercial sales surface this year. In addition to the 2-μm n-MOS 2864, Motorola has in the wings a second 64-K chip using a redundant array of 128-K memory locations for greater write cycles.

Whether EEPROM volumes finally take off, 1986 is destined to be the year for 256-K introductions. Two major competitors are already in the arena, taking early shots at high-density applications. Last month, Xicor announced it had begun sending out samples of one of the industry's first 256-K EEPROMs, the X28256. Volume production of the 2-μm n-MOS chip is expected to begin this summer. Seeq says it will also make available samples of its CMOS 256-K EEPROM this winter.

AMD, Excel, General Instrument, and NEC are all planning to introduce full-feature 256-K EEPROMs later this year. Advanced Micro Devices Inc., Sunnyvale, Calif., plans to introduce the 2K256 in the second half. The CMOS chip will have a conventional thin-oxide tunneling structure, providing critical radiation hardness for the large military market.

This spring, Excel Microelectronics Inc. will debut the L28C512, a 512-K chip that features a die-saving single-transistor storage cell, intended as a cost-competitive alternative to UV-EPROMs. Fujitsu, Intel, National Semiconductor, and NCR are preparing CMOS and other nonvolatile product entries during the year. The new round of optimism has other chip giants, including Hitachi Ltd. and Texas Instruments Inc., studying possible products.

For TI, the major attraction is the 256-K generation, although it has started a 64-K design. "We are toying with the decision of making a 64-K entry into the EEPROM business," states Ramesh Gidwani, semiconductor vice president in TI's U.S. Memory Product Center in Houston. What TI likes about the 256-K generation is that a variety of configurations is likely to find niche applications. "We are looking very strongly at the so-called flash EEPROMs," adds Gidwani, referring to a low-cost design pioneered by Japan's Toshiba Corp.

Toshiba's 256-K flash EEPROM, disclosed a year ago, reduces cell size by a third by using three levels of polysilicon instead of two. The first layer makes an electrically erasable Fowler-Nordheim tunneling gate similar to those of conventional EEPROMs. The second has a floating gate to write a bit in the cell, much like a conventional UV-EPROM, using avalanche-injection programming. The third layer operates the word-select line for programming and reading.

Toshiba has had difficulty in getting a working chip and declines to discuss the status of the 256-K flash EEPROM; it says only that it has no current product. The flash design is important in EEPROM's battle to replace EPROM because reducing size is the primary way to cut costs. And the difference in both between EPROMs and EEPROMs is shrinking. Seeq engineers, for example, have reduced the company's EEPROM cells from 423 μm² to less than 60 μm² in three years. EPROMs, however, still measure about 23 μm². But more than the remaining size differences, price wars between Japanese and U.S. EEPROM makers are stalling a jump in EEPROM sales resulting from the smaller die sizes, notes McCranie.

Others are discounting significant volume potentials resulting from the replacement of UV-EPROMs. "It has taken some time to understand how to use the device where it fits most effectively," says Xicor's Oliphant. "About a year and a half ago, we began positioning the byte-wide EEPROMs to be used not as a replacement but in conjunction with UV-EPROMs. We then began to see something change."

Large corporations, confident that de facto standards for pinouts and on-board timing features were emerging and that new suppliers would keep the EEPROM pipeline flowing, started designing the chips into systems to aid field servicing or manufacturing, says Oliphant. "EPROMs came into the market during the 1970s as an aid to designers, enabling them to change their programs in the early prototyping stages. EEPROMs, with the ability to do in-circuit changes to software and reconfiguring systems, have enormous implications in manufacturing, serviceability, and end-user benefits."

The maturing 64-K generation is just beginning to open new applications for nonvolatile system code storage, says Bruce McCormick, product marketing manager for Intel Corp.'s EEPROM operations. The greater chip densities, pinout standards, and common chip features among different vendors now have large equipment houses comfortable with the technology.

"Large EEPROMs still require some education in commercial markets," says Anna Appleby, National Semiconductor Corp.'s EEPROM product marketing manager. "Smaller chips are generally used for data storage, higher densities for program storage—a more traditional use for memory," she says.

NATIONAL CMOS. National sees such a large business potential in low-power low-density EEPROMs that it is planning to introduce by year end a new CMOS family of small memories in surface-mountable small-outline packages. At the same time, the Santa Clara, Calif., chip maker is also readying higher-density parts, including a CMOS 64-K EEPROM slated for the second half of the year and a follow-on 256-K part.

High-density EEPROMs are now the fastest-growing segment of the chip industry, claims Bernhard J. Rohrbacher, vice president and general manager of General Instrument Corp.'s Microelectronics Division. "If I had to put a stake in the ground, it would be at least 30% compound growth per year," he estimates. The Palo Alto company is offering samples of a 1.5-μm CMOS 64-K EEPROM and plans to introduce a 256-K chip around the third quarter.

Charles L. Cohen provided reporting from Japan.
AUTOMATED METER READING BEGINS TO MAKE SENSE

AFTER DECADES OF TRYING, UTILITIES GET BOOST FROM LOWER COSTS

by Tobias Naegele

HARRINGTON PARK, N.J.

For years, utility companies have looked forward to the day when computers, instead of people, would automatically read their meters. Many schemes have been tried, but the high cost of the technology, coupled with a regulated AT&T that had little interest in the business that automatic meter reading had to offer, kept that dream from coming true.

But with the development of very large-scale integrated circuits cutting the cost of electronics, and the breakup of the Bell system leaving the regional operating companies hungry for new sources of income, automatic meter reading is getting renewed attention.

The Hackensack Water Co., which serves 164,000 customers in suburban Bergen County, N.J., could be the first to install such a system universally. The company will decide by May if it should go ahead with an $18 million project to end manual reading in Hackensack in favor of a system that can be accessed by a computer using existing telephone lines. Don Schlenger, director of research and development for the Hackensack project, has studied the idea since 1978 and says installation could begin early next year; it would take 30 months to complete.

Although the technology for automatic meter reading has been around almost as long as utility meters—the first such system was patented in 1899—none of the many experiments made over the years ever lived up to expectations. Typical of such early attempts was the 1969 experiment by San Diego Gas and Electric, which read meters over dedicated phone lines. San Diego abandoned the study in 1971 because it could not make it cost-effective.

However, a number of utilities are now working in tandem with local telephone companies in a new wave of tests, and they're being courted by a handful of electronics firms hoping to edge their way into a new market.

First system may soon get go-ahead in New Jersey

Among those exploring automated meters are Brooklyn Union Gas and New York Telephone in Brooklyn, and ITT and Southern New England Telephone in Stratford, Conn. Tests in Colorado and Texas are also under way.

"Automatic meter reading will either be a home run or a scratch hit," says Brian Yurkiw, marketing and sales manager for Base Ten Telecom Inc., Trenton, N.J., which is vying for the Hackensack contracts. "There won't be a two- or three-bagger there." The company, a wholly owned subsidiary of Base Ten Systems Inc., was formed last year to design and build hardware for meter automation. Base Ten is among a small group of companies jockeying for position in what Schlenger says represents a $10 billion business opportunity if automatic meter reading really catches on. In the Hackensack project, Base Ten's main competitor is Neptune Water Meter Co., Tallassee, Ala. Typically, water rates are set according to consumption, using one of several mechanical solutions, such as rotating disks or oscillating pistons that move proportionately to the water flowing through their chamber. Through a magnetic coupling, the meter is connected to a register similar to the odometer in an automobile.

In 1965 Neptune began offering an electronic encoder on all its meters, replacing the mechanical wheels in the odometer with wheels that feature electrical contacts, thus creating a switch. The system was improved in 1972 when a custom synchronous CMOS integrated circuit was added that, when activated by a clock pulse, "reads" the switches on the odometer and outputs the reading in a serial data stream (see "How your water meter will talk back").

SUDDENLY POPULAR. A number of factors have come together to intensify this new interest in automated meter reading. Perhaps the biggest is the development of very large-scale integrated circuitry, which offers the possibility of overcoming inherent technological roadblocks at a cost the utilities can afford. But there are many other, more mundane, elements at play here.

Searching for new sources of income, telephone companies are recognizing the hidden value of their installed base of telephone lines, which service nearly every American home and lie dormant almost 80% of the time, according to officials at Southern New England Telephone. Using those lines for meter reading may be a prime way of capitalizing on existing equipment.

For the utilities, meanwhile, the appeal lies in avoiding some common head-
aches of their business—including estimated bills and high labor costs. More than 70% of all meters in the Northeast are shielded from the cold either inside or underground, according to Joel Ash, director of telemetry systems at ITT's Advanced Technology Center in Shelton, Conn., meaning meter readers must enter homes to record usage data.

Remote meter access thus seems the simple answer. But the problems involved are tremendous, hence the snail-like pace at which the automated-meter players are proceeding. "It's such a big job, the utilities can't afford to be wrong," says Yurkiw, of Base Ten Telecom. "They could bury themselves in just one step." Yurkiw says the sales cycle for an automated meter-reading system, from contract to contact, is likely to be five years.

At the Hackensack water company, Schlenger's list of requirements for an automated reader is a long one. Among his concerns are polarity-protection, so that wires can be switched without the threat of damage to system components; power-surge protection for all equipment to guard against lightning damage; and the ability to run off the power on a standard telephone line.

And that's not all. Yurkiw points out a number of other requirements, such as the need for the utility to read its meters even if telephone service has been discontinued. Other "special loop" conditions that must be dealt with include the ability to provide service over private branch exchanges and multiparty lines. In addition, the system must be compatible in the long term with integrated services digital networks.

But the bottom line, says Yurkiw, will be cost. Automated meter reading will take off only when utilities can use it to offer customers improved service at an equal or better price. If the systems remain too expensive, Yurkiw says, automated meter reading will be relegated to a select number of out-of-the-way customer locations for which manual readings are simply not cost-effective.

The Hackensack project, if implemented, will cost about $105 per customer. Schlenger and Yurkiw say later projects may cost less, as the telephone companies and equipment suppliers learn the technology and as the demand from utilities increases.

Once Hackensack Water has installed its system, for example, the road will be open for Public Service Electric and Gas Co., Newark, N. J., which supplies electricity and gas to the region, to experiment with the system. If PSE&G eventually decides to tie into the system, customers could possibly benefit from reduced costs based on volume; also, PSE&G would have to pay Hackensack a fee to access the water company's meter interface unit.

There are already indications that costs will be dropping. Just two years ago, Yurkiw says, the meter-interface units alone cost about $400. Today, VLSI circuits such as single-chip modems and microprocessors have cut the unit cost of a meter interface unit to about $40.

However, the heart of the system is the meter access circuit, the interface between the telephone company and the utility. The access circuit, which connects to the telephone company's test trunk, accepts requests for readings from the utility over a normal telephone connection and then dials customer locations over the test trunk, accessing the meter without ringing the customer's telephone. It takes less than 5 s to retrieve the data and forward it to the utility's computer system. Base Ten's Meter Reading Access Circuit, which is currently under consideration by New Jersey Bell for Hackensack's pending installation, costs between $15,000 and $20,000 with software, serves up to 10,000 telephone lines, and can be expanded to handle 100,000 lines, according to John McShane, director of corporate development at Base Ten.

McShane is optimistic. He says large-scale installation of automated systems is just around the corner. "The technology has been there for a long time, but the cost was too high, and the telephone companies didn't have the motivation. The difference today is the phone companies really want to do something."

---

**GAS AND ELECTRIC ARE ON SLOWER TRACK**

Gas and electric utilities are not likely to automate their meters as quickly as water companies.

Gas companies have a safety issue to keep in mind and so are likely to wait to keep closer tabs than other utilities on their on-premises equipment. Electric companies, on the other hand, enjoy lower reading costs than water companies simply because there are usually more electricity meters in a given location than water meters. In an apartment complex, for example, there may be only one water meter for the landlord, but there can be hundreds of electricity meters for the individual tenants. That density lowers the reading cost per meter for the electric companies, removing the financial impetus to convert.

Furthermore, encoder-equipped electric and gas meters are not commercially available. Gas meters can be retrofitted with an electronic encoder similar to the one Neptune International Corp. builds into its water meters. But electricity meters cannot, since they do not measure the physical flow of a commodity like their gas and water counterparts. And since electricity meters cannot support a power load, they must be fitted with some sort of optical encoder that can "read" the meter's four dials.

But in three or four years, says John McShane of Base Ten, conventional electricity meters will be replaced by solid-state meters that have serial outputs for remote reading.

---

_T.N.
GENERAL COMPUTER GIRDS FOR ANOTHER BATTLE

OPEN MACINTOSH ARCHITECTURE MEANS VIDEO-GAME SURVIVOR WILL GET COMPETITION IN PERIPHERAL MARKET IT HAD TO ITSELF

CAMBRIDGE, MASS.

General Computer Corp. has already survived the market collapse in video games. But now the five-year-old company faces an even bigger challenge: Can it survive a surge of new competition in a market—peripherals for Apple Computer Inc.'s Macintosh personal computer—that until now it has had virtually to itself?

The Cambridge company emerged from the video game business' downturn by introducing Hyperdrive, the only available internal hard-disk drive for the Macintosh. Now, General Computer again finds itself in a precarious market position. Apple has committed to an open architecture for the Macintosh. Small Computer System Interface ports on Apple's new Macintosh Plus open the door to other peripherals vendors. General Computer has responded by exploiting its technical prowess as a vendor of high-performance products and is moving to turn itself into "a full-featured computer company," says Kevin Curran, its 21-year-old president and co-founder.

Last month, General Computer brought out the $3,195 Hyperdrive 2000, which couples a 20-megabyte internal disk to a high-performance coprocessor board. The option is said to double the Macintosh's processing speed, positioning it for use as a low-end work station. The company also unveiled Hypernet, a file-server software package that lets up to 32 Macintoshes share hard disks and files. It sells for $295 per host.

TO COME. Curran sees a high-end computer in General Computer's future.

COMPANIES

OPEN MACINTOSH ARCHITECTURE MEANS VIDEO-GAME SURVIVOR WILL GET COMPETITION IN PERIPHERAL MARKET IT HAD TO ITSELF

BRINGING IN VETERANS. And there is more to come. General Computer plans to triple its engineering staff of 20 by the end of the year. To position itself for smooth growth in the future, the company has recruited industry veterans for key slots. Gary Boone, a veteran of Texas Instruments Inc. and Ford Motor Co., is the company's new vice president of engineering. Thomas O'Donnell, formerly a vice president with IBM Corp. in charge of personal computer development, General Computer has been profitable since its founding in 1981, with 1985 revenue of about $20 million.

Curran began his association with co-founder Doug Macrae—who is chairman and vice president of new-product development.
Most suppliers sell their power discretes. SGS is willing to give them away to prove a point: We're not just one of the biggest suppliers of power devices, we're the friendliest.

We mean business. Just send us your card and a note explaining how your company uses power discretes. If you qualify, we'll send you a free $100-value 9-drawer Power Pak case containing 60 of the industry's most popular power discretes.

Better hurry! We've got thousands of Power Paks, but they'll go fast.

Pre-qual programs, indepth tech notes, nationwide distributors and Reps, free power discretes -- SGS is backing engineers with everything it takes to make your job easier. That's why we're known as The Friendly Power.
HOW ASCII IS DEALING WITH LOSS OF MICROSOFT

Dropping all other business activities in order to calm the fears of nervous customers is an unaccustomed action for senior executives at Ascii Corp., a nine-year-old software developer and magazine publisher that developed into a $65 million company in fiscal 1985. But that was exactly what managers at the Japanese company had to do after they found themselves in the unenviable position of losing one of their largest and best-known business segments: Microsoft Corp. decided to replace Ascii as its sole representative in Japan with a wholly owned subsidiary [Electronics, Feb. 10, 1986, p. 11]. Ascii executives are busily assuring customers that their company will continue to support products from the Bellevue, Wash., software developer during the transition period. They also must establish the Tokyo company’s reliability as a supplier, because users of Microsoft products may be customers for Ascii’s own products and because the market looks askance at vendors who abandon customers. These factors—and the status that Ascii derived as sales agent for Microsoft—mean that severing the relationship between the two companies will weigh more heavily than simply losing the 15% of revenue that Microsoft products represented.

NO SURPRISE. Ascii president Akio Gunji admits that the breakup was bound to happen sometime, because of a difference in styles between the two companies and Ascii’s growth in other businesses. Gunji notes that his company, which started in 1977 as a publisher of computer magazines, continues developing new software products for the Japanese market and also represents companies other than Microsoft. Thus it is inevitable that as applications programs from Microsoft proliferate, some are going to compete with either Ascii’s products or those from other manufacturers it represents.

One thing that Gunji hopes to salvage from the rupture is the MSX computer standard it developed with Microsoft. Instrumental in developing the standard was Kazuhiro (Kay) Nishi, 30, a cofounder and vice president of Ascii, who also played a major role in bringing the two companies together. During this period, he also served as an unpaid vice president at Microsoft. MSX home computers have become Japan’s best-selling 8-bit machines, and Gunji expects even better performance for MSX2, an enhanced system brought out last year [Electronics, July 1, 1985, p. 19].

“The original MSX is a fine low-end computer,” Gunji says, but he believes that the MSX2 has even greater market potential. An adapter and modem turn the new model into a videotext terminal and, with other peripherals, it can be either a word processor, telecommunication terminal, music synthesizer, or home control terminal.

To date, 1.1 million MSX computers have been sold in Japan and sales are now increasing at a rate of about 80,000 units per month. According to Masahiro Morimoto of Tokyo’s Digital Research Corp., the company’s president, the Macintosh’s built-in processor, Alsop says, “For them to redirect all those resources is not going to be easy.” But Alsop also says the company has had some problems with product reliability and customer service. And although General Computer sees the need for experienced managers in building a larger company, Alson wonders if that need has been met. The biggest pitfalls for firms such as General Computer, he warns, are to become arrogant “and expand too quickly.” —Craig D. Rose

BOTTOM LINES

TI PLANS $225 MILLION STOCK OFFERING

Texas Instruments Inc. plans to raise $225 million through an offering of preferred stock. The Dallas electronics giant filed a registration statement with the Securities and Exchange Commission outlining the offering. It says that proceeds will be used to redeem $200 million in debentures.

UNGEMANN-BASS TO TAKE OVER LINKWARE

Local-area-network supplier Ungermann-Bass Inc., Santa Clara, Calif., has agreed to buy Linkware Corp., a privately held supplier of advanced network application software. Ungermann-Bass already owns 22% of the Waltham, Mass., company. It will buy the remaining stock in exchange for an undisclosed amount of Ungermann-Bass stock and cash. After the acquisition, Ungermann-Bass says, Linkware will operate as a wholly owned subsidiary. Linkware markets software products with which users can transfer information among a variety of minicomputer, personal computer systems over multiple network topologies.

MEGATEK ACQUIRES GRAPHICS COMPANY

Graphics-system manufacturer Megatek Corp., a San Diego subsidiary of United Telecommunications Inc., Westwood, Kan., has acquired the assets of Perspective Technologies Inc., a Columbia, Md., developer of a high-performance three-dimensional graphics system. Terms of the acquisition were not disclosed.

UNISOFT BUYS PART OF JAPAN DISTRIBUTOR

UniSoft Systems, the Berkeley, Calif., supplier of Unix System V software-development services, has acquired what it describes as a “substantial equity interest” in Nippon UniSoft, Tokyo. Nippon UniSoft is a joint-venture set up by three Japanese companies—Digital Computers, Microboards, and Ricoh—to distribute UniSoft Systems’ products in Japan. Terms of the deal were not disclosed. Nippon UniSoft is working on a Kanji implementation of AT&T Bell Laboratories’ Unix operating system for Ricoh Co., UniSoft said. This will be similar to an implementation that Nippon UniSoft and UniSoft Systems completed last year for AT&T. UniSoft also plans to open a West German subsidiary, UniSoft GmbH, in March.
"For 40 Howmedica distributors worldwide, Shannon is the centre of the universe."

Dermot Whelan
Managing Director, Howmedica International Inc., Ireland.
Division of Pfizer Chemical Corp.

In 1971, Howmedica International Inc. centralised all ex-US distribution of its range of orthopaedic implants and instruments at Shannon International Airport, Ireland. From Shannon, Howmedica profitably and effectively supports its distributors, not only in Europe, but in the Far East, Japan and Australia.

The decision to locate at Shannon was brought about by the unique incentives it offers...

- Direct access to Shannon International Airport and priority customs attention.
- Duty-free access for goods in transit—which minimises documentation procedures and helps cash flow.
- Europe's lowest corporate tax rate—Shannon/Ireland is the most profitable location in Europe for American investors.
- An unrivalled package of non-repayable capital, R&D and training grants.
- Low operating costs.

To find out how your company can benefit by distributing through Shannon, mail the coupon or call Eugene Brennan at I.D.A. Ireland, 2 Grand Central Tower, 140-148 E. 45th St., New York, NY 10017. Tel: 212-972-1000.

SHANNON, IRELAND

Electronics / February 17, 1986
Brand New LCD From Sharp

With contrast up to 7.0 and viewing angle from $-10^\circ$ to $+45^\circ$, it's twice as easy to see why LCD readability can now be twice as good for your portable computers and OA equipment. The demand for this LCD is expanding rapidly — due to Sharp's success in improving LCD performance in direct response to market demand.

IBM PC® Compatible LCD Monitor

This new LCD monitor comes with an RGB video signal interface cable, completely eliminating the cost and time needed to design and develop an interface to IBM PC® or PC clones. This monitor enables you to instantly display your PC software on our 640×200 LCD by just plugging the RGB interface cable into an IBM PC® or PC clone.

<table>
<thead>
<tr>
<th>Type No.</th>
<th>LM64014W</th>
<th>LM64016W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dot pitch ratio</td>
<td>1:1.4</td>
<td>1:2</td>
</tr>
<tr>
<td>Type</td>
<td>Reflective Type</td>
<td>Reflective Type</td>
</tr>
<tr>
<td>Contrasting</td>
<td>7.0 (TYP.)</td>
<td>7.0 (TYP.)</td>
</tr>
<tr>
<td>Viewing angle</td>
<td>$-10^\circ$ to $+45^\circ$ (Co-2, TYP.)</td>
<td>$-10^\circ$ to $+45^\circ$ (Co-2, TYP.)</td>
</tr>
<tr>
<td>Unit outline dimension</td>
<td>256×128×13.3</td>
<td>256×164×13.3</td>
</tr>
<tr>
<td>Display format(W×H)</td>
<td>640×200</td>
<td>640×200</td>
</tr>
</tbody>
</table>

* Compared with earlier Sharp models.

SUPER TWISTED
HIGH CONTRAST LCD

NOW AVAILABLE

IBM PC is a trademark of International Business Machines Corporation.
Screen image printed with permission of Microsoft Corporation.

SHARP CORPORATION, JAPAN

SHARP CORPORATION International Sales Dept. Electronic Components Group
22-22, Nagakri-cho, Abeno-ku, Osaka 545, JAPAN Tel: (06)621-1221 Cable: LABOMET OSAKA Telex: J63428 Atn: OSKPA(LABOMET A-B)
U.S.A.: SHARP ELECTRONICS CORPORATION Electronic Components Division
Sharp Plaza, Mahwah, New Jersey 07430 Tel: 201-529-8200 Telex: 4269039(SHARP AMERICA)
EUROPE: SHARP ELECTRONICS(EUROPE)GMBH Electronic Components Dept.
Sonninstrasse 3, 2000 Hamburg 1, F.R. Germany Tel: (040)23775-0 Telex: 2161876(HEEG D)
The Electronics Index, a seasonally adjusted measure of the U.S. electronics industry’s health, is a weighted average of various indicators. Different indicators will appear from week to week.

**U.S. ELECTRONICS SHIPMENTS**

<table>
<thead>
<tr>
<th>Shipments ($ billions)</th>
<th>December 1985</th>
<th>November 1985</th>
<th>December 1984</th>
</tr>
</thead>
<tbody>
<tr>
<td>Communications equipment</td>
<td>5.951</td>
<td>5.621</td>
<td>5.528</td>
</tr>
<tr>
<td>Radio and TV receiving equipment</td>
<td>1.030</td>
<td>1.003</td>
<td>0.935</td>
</tr>
<tr>
<td>Electronic and electrical instruments</td>
<td>4.967</td>
<td>4.789</td>
<td>4.523</td>
</tr>
<tr>
<td>Components</td>
<td>3.254</td>
<td>3.220</td>
<td>3.892</td>
</tr>
</tbody>
</table>

The statistics continue to improve for the U.S. electronics industry. Following last week’s report of a 2.3% increase in equipment production in November comes news that shipments of U.S.-made electronics products jumped 3.9% in December, according to the government’s latest information. Shipments for communications gear, radio and TV equipment, and components have set the pace. As a result, the Electronics Index again moves up.

December’s boost in shipments comes after a 4.9% boom in November, keeping alive hopes that the long-awaited recovery in domestic electronics markets could be under way. It is off to a slow start, however: shipments of electronics goods in December were only 2% ahead of December 1984’s level. Nonetheless, it was the first month since last February that gains in shipments were spread so evenly throughout the domestic industry—every sector showed some increase.

For the second month in a row, manufacturers of communications equipment shipped products at an increased clip. Sales in that industry were up nearly 6% in December, after a 7% gain in November. And suppliers of communications equipment not only turned in the most vigorous sales performance of the U.S. electronics industry in 1985 but also managed to match the brisk pace set in 1984. In both years, shipments increased by greater than 13%.

Helped by the continuing free-spending habits of U.S. consumers, shipments of radios and TVs by U.S. manufacturers rose 2.7% in December. This monthly performance brought shipments for all 1985 to a level 7.3% higher than they were in 1984, thus representing the electronics industry’s second most vigorous growth rate last year. Still, this latest annual growth rate pales in comparison with 1984’s 21% shipment surge.

December marks the third consecutive month that component shipments edged higher from the preceding month, even though production in the U.S. has fallen every month for the past year from levels a year earlier and total 1985 component shipments were down 13%. Up 1.1% in December, semiconductor shipments were ahead nearly 5% from September 1985. As customer inventories continue to sink and as book-to-bill ratios rise, production of components could soon embark on the same growth track that shipments have been on.

For all 1985, shipments of U.S.-manufactured electronics products were 3.4% ahead of the preceding year. This increase is far behind the 16.8% surge in 1984. But the end-of-the-year strength in so many sectors could be a sign that the industry upturn has begun.

Electronics / February 17, 1986
AGGRESSIVE RISK-TAKER FOLLOWS OSHMAN AT ROLM

SANTA CLARA, CALIF.

Dennis D. Paboojian says it was not his 13 years of management experience at Rolm Corp. that got him the job of president at the big supplier of digital business communications systems. He was selected, he says, because of "the kind of individual I am and the aggressiveness, the risk-taking that I've succeeded with."

He will certainly need those skills. "I'm replacing Ken Oshman and he had a fairly big shadow," Paboojian explains. "That makes the job very difficult and challenging." In his new post, he will concentrate largely on integrating Rolm with IBM Corp., which bought the company in November 1984.

His work is cut out for him, Paboojian says. He points out that his company's two biggest opportunities with IBM are to capitalize on IBM's marketing force and to jointly develop complementary products. The marketing direction has been defined, he says, "but a lot of work needs to be done to make it real and effective."

Paboojian, 42, came to Rolm in 1972, just three years after its founding. A Stanford University graduate, he worked at Hewlett-Packard Co., then was responsible for engineering and purchasing at Arcata Communications, a Bay Area interconnection vendor. At Rolm, he worked his way up through various positions, including general manager of the Mil-Spec Computer Division, now a separate operation. There, his early conviction that Ada would become important led to a risk that paid off—Rolf came up with the first work station to run the Defense Department's language.

Most recently, he was general manager of the Systems Development Group, which encompasses telecommunications products. During that time he took Oshman as Rolm president a big order.

DENNIS D. PABOOJIAN: Finds replacing Ken Oshman as Rolm president a big order.

MANAGER AT ROLM

Croxon's responsibilities at the Natick, Mass., company will include the development and marketing of work stations and the coordination of Prime's efforts in artificial-intelligence applications. He had been president of Newport Systems Ltd., Hampton, N.H. Earlier, he spent 10 years at Digital Equipment Corp. in a variety of roles, including group manager of engineering for the VAX line.

WILLIAM A. WHITWARD

The Philips Industrial & Electroacoustic Division, Eindhoven, the Netherlands, has appointed William A. Whitward as general manager of its Test and Measuring Group. Whitward moved to the Netherlands in 1978 from South Africa, where he was commercial manager of Philips' Professional Products Division. He says he expects continued expansion of the group's marketing base outside Europe, including Australia, Canada, China, Hong Kong, and India.

MALCOM R. CURRIE

The task of overseeing the transfer of Hughes Aircraft Co. electronics technology and systems expertise into General Motors Corp. products and plants will fall to Malcolm R. Currie. The 58-year-old Hughes executive vice president has been named president of GM Hughes Electronics Corp. The GM subsidiary owns Hughes Aircraft and Delco Electronics Corp. Currie's career at Hughes spans 23 years, interrupted by an eight-year stint starting in 1969, when he served in a research and development position at Beckman Instruments Inc. and later as under secretary of defense for research and engineering. Currie will continue in his current position with Hughes Aircraft.

PETER C. SKERLOS

The new vice president of engineering for consumer products at Zenith Electronics Corp. is Peter C. Skerlos. Skerlos, who holds 21 patents, many in the TV tuning field, joined Zenith in 1969, where he held a variety of engineering and engineering management positions before being named an executive director at the Glenview, Ill., company in 1984.

PEOPLE ON THE MOVE

SUGIICHIRO WATARI

After building a solid reputation for efficient management in his 38 years with Toshiba Corp., Sugichiro Watari will become the company's president and chief executive officer on April 1. Watari, who will be 61 years old next month, is moving up from executive vice president to succeed Shoichi Saba. Saba will become chairman of the board after having served as the Kawasaki, Japan, company's president and CEO since 1980.

BRIAN F. CROXON

Prime Computer Inc. has named Brian F. Croxon to the position of vice president of work-station programs.

Eve Bennett
MOORE TAKES HIS KNACK TO KONTRON ELECTRONICS

MOORE: He was attracted by the excitement of "this jungle of CAE."

MOUNTAIN VIEW, CALIF.

Evett E. Moore has a knack for combining various elements to produce a better whole. "I'm pretty good at handling complex products," he says. "A lot of work that's interrelated needs a boundary put around it—then it can be done." As the new president of Kontron Electronics Inc., he will need that talent as the Mountain View company struggles to integrate its logic analyzers and microprocessor-development systems.

The goal is to produce development systems that will integrate all engineering phases from software and hardware design through testing—something that could bring Kontron a greater presence in the rapidly expanding realm of computer-aided design, engineering, and manufacturing. The U.S. subsidiary of Kontron Elektronik GmbH, Munich, needs to develop such a niche—its sales have stayed between $10 million and $15 million annually for the past five years.

IN THE JUNGLE. Moore comes to Kontron from John Fluke Mfg. Co., the Everett, Wash., components and equipment manufacturer, where he was a division manager of the Components Manufacturing and Support Division. He goes from managing 700 employees at Fluke to 85 at Kontron, but he says of his new task, "I was attracted by this jungle of CAE. The excitement level is greater."

Under Moore's direction, there will be more interaction between Kontron in the U.S. and its West German parent, which holds a dominant position in the European microprocessor-development market. "They're looking for this group to provide input for the next product developments," says Moore.

Though the U.S. arm will look into technological developments here, its main charter for the near term is to bolster the software that connects the German-developed hardware. "The challenge here is to put together a lot of very good pieces that will sell in the U.S. But we have some more software to do to tie the pieces together—networking-type software," adds Moore.

"The engineer's design task should not end at his bench—it should tie into manufacturing," he goes on. "Also, more and more inspection technology will be used." Moore believes Kontron has a step up in that department because of Kontron GmbH's heavy investment and developments in medical-imaging technology. He says the core of this technology could be worked into real-time inspection systems. "That's where the future is going to be in all CAE."

Moore, 54, understands the design engineer's point of view because he was a pioneer in the development of the first CMOS integrated circuits at RCA Corp.'s Solid State Division. He left there for Fairchild Camera & Instrument Corp. in 1965, eventually becoming operations manager of its Microprocessor Division before he left for Fluke in 1977.

But he says, "I'm glad to get back to Silicon Valley. I prefer to live in a warmer climate." -Eve Bennett

TEKTRONIX COFOUNDER VOLLMUT DIES AT 72

Howard Vollum, who parlayed development of a rudimentary oscilloscope into giant Tektronix Inc., died on Feb. 3 from a stroke. After serving in the U.S. Army Signal Corps, where he was involved with the development of high-resolution radar, Vollum founded Tektronix with M. J. (Jack) Murdock in 1946 to produce oscilloscopes. It quickly took over the scope market from such leaders as RCA Corp. and Dumont Electronics. The Portland, Ore., native was company president from 1946 until 1971. When Murdock died in a seaplane accident that year, Vollum became Tektronix' chairman, a post he held until 1984, when he became vice chairman. Tektronix has grown to a $1.4 billion company selling a wide range of test and measurement, information display, and computer-aided engineering gear.

A guide to semiconductor strategies in the 80's!

CUSTOM & SEMICUSTOM VLSI:
Survival Strategies For The New Era asks the question: Are you equipped to meet the challenges of an ever-changing industry? Radical change in industry can mean radical growth if you understand these changes.

Order this book today for an inside line on the challenges of change in the semiconductor market.

Send $150 or your company purchase order to:

Electronics Books
P.O. Box 541
Hightstown, NJ 08520
**SPICE up your PC**

**Z/SPICE professional circuit simulation**
- Full version $245
- Student version $79

**ZTEC**
- box 737, college place, wa 99362
- (509) 527-1025

**FREE DEMO DISK**

SCHEMA is a complete, integrated schematic drawing software package for IBM Personal Computers. Use SCHEMA with your PC to draw schematic drawings, and automatically generate design documentation including Wire and Net Lists, Bills of Materials, Design Rule Checks, etc. SCHEMA is $495 and supports most common PC hardware configurations. Call or write today for a free demo disk and brochure.

**OMATION, INC.**
1701 N. Greenville Ave., Suite 809
Richardson, TX 75081
(214) 231-5167

**WIRE WRAPPING SOFTWARE RUNS ON IBM PC**
Conversion from schematic, either CAE or hand drawn, for wiring by wrapping or other termination on AAC wiring machine. Optimizes wire paths and provides full documentation. For prototyping or production.

**HOT LINE**
To place your 
**Computer Software Ad** in 
**Electronics**
call Ilene Fader at 212/512-2984

**POSITIONS VACANT**
South? Technical/Professional Placement

**POSITIONS WANTED**
Electronic Expert For Hire. I do Microprocessor hardware/software, assembly language. Analog, digital design in my N.Y. lab or worldwide. Project rates. Mr. Barry Masel (718) 476-1516.
SILICON SYSTEMS SAYS VOLUME QUANTITIES WILL BE READY IN MARCH

Speak softly but carry a big stick was Silicon Systems’ motto in developing the full-function single-chip modem it is about to deliver in quantity. Instead of announcing a product before it could deliver one, the company began low-key sample deliveries of its K212 modem to 100 potential customers in late 1985.

The company chose not to discuss the single-chip modem publicly until manufacturing was well under way. “We especially didn’t want to get out there too emotionally with a piece of paper, when we can’t follow up with the silicon,” says Rick Goerner, senior vice president of marketing and sales. Even though the company waited, it is not late. Silicon Systems will have production quantities ready by next month, right on schedule with competitors such as Sierra Semiconductor Corp., which promises to go into production later this month [Electronics, Nov. 4, 1985, p. 46].

The first member of a modem family to be brought out during the next year, the K212 suits either free-standing products or systems and either synchronous or asynchronous communications over the two-wire switched telephone network. The family will cover the entire Bell and International Telegraph and Telephone Consultative Committee (CCITT) range of full-duplex standards for 300- to 2,400-b/s communications, says Gary Kelson, senior vice president and general manager of the company’s Telecommunications Division.

The K212 operates at 300 and 1,200 b/s and performs basic phase-shift- and frequency-shift-keying functions. It requires only the addition of a phone-line interface, control microprocessor, and RS-232-C level converters to build a complete Bell 212A standard full-duplex modem, the company says.

ADVANCED CMOS. The chip uses an advanced CMOS process that integrates analog, digital, and switched-capacitor arrays. “As many functions as deemed economically feasible were included in order to simplify implementation into typical modem designs,” says Goerner.

All modem chips in the family will be hardware and software compatible, “allowing designers to plug in upcoming SSI modems in the same sockets to upgrade performance,” Kelson notes. In the fall, Silicon Systems plans to introduce the single-chip model K224, which will handle 300-, 1,200-, and 2,400-b/s transmission rates and support not only Bell 103 and 212A but also CCITT V.22 bis, V.22, and V.21 protocols. And the company will follow that with the model K222, a 300-, 600-, and 1,200-b/s modem that supports CCITT V.22 and V.21 communications protocol standards.

Designed to appear as a microprocessor peripheral to the systems designer, the K212 interfaces with such standard microcontrollers as the Intel Corp. 8048 and 8051. Control of modem operation takes place through an 8-bit multiplexed address and data bus or through an optional serial-command bus. An address-latch-enable control line simplifies address demultiplexing, the company says, and data communications occur only through a separate serial port. Test modes are provided for diagnostics.

Another feature is a dual-tone multifrequency tone generator that allows the modem to dial its own calls. A call-progress detection feature further expands this capability, the company says, because the modem can detect dial tones, busy signals, or ringback, and change its calling action in response to these detected signals. Also, a Direct Access Arrangement interface approved...
by the Federal Communications Commission provides the connection to the dial-up phone line.

CMOS technology keeps power consumption to a low 120 mW, and a low-power idle mode drops that to less than 10 mW. A single +12-V supply is required. The K212 is available in 22- and 28-pin DIPs and in quad packages. The K212 currently costs about $40 in hundreds, but Silicon Systems predicts that will quickly fall to $30 with quantity production. By year end, the price could hit $20, which the company says is the level needed to fully exploit the market.

—Larry Walter

Silicon Systems Inc., 14351 Myford Rd., Tustin, Calif. 92680. Phone (714) 731-7110 [Circle reader service number 338]

PORTABLE SCOPE SHOWS EVENTS AS SHORT AS 1 NS

A new Tektronix oscilloscope is the first portable scope with a writing speed fast enough to display single-shot events that are as short as 1 ns, its maker claims. The 350-MHz model 2467 makes visible single-shot 1-ns pulse transitions, such as crosstalk and erratic timing margins, in normal room light. It owes its visual writing rate of 4 divisions/ns to microchannel-plate technology. Conventional CRTs have visual writing rates of about 0.05 division/ns, according to the company.

The model 2467 uses a microchannel plate behind the CRT to intensify transients and display rare single-shot events even when they are superimposed on highly repetitive signals. At the same time, the enhanced CRT reduces the masking effect of these normal events. The microchannel-plate technology, which has been around since 1979, is common in laboratory scopes, says Robert S. Galvin, a spokesman for Tektronix' Portable Instruments Division. The Tektronix lab scope, the 1-GHz model 7104, uses microchannel technology and writes at a rate that is fast enough to show a 6-division/ns single-shot 500-ps step.

HIGH ACCURACY. With this technology in the 21-lb scope, an engineer can perform the same tests on site with the same degree of accuracy that formerly only a bench instrument could deliver. In addition, special pulse-mode firmware automatically accommodates narrow pulses that otherwise would not be displayed. The 2467 has been ruggedized to take extremes in heat and humidity, and movement from one area to another won't affect performance.

Glitches that once took weeks of testing to spot now light up instantly, thanks to the microplate technology, which Tektronix calls adaptive-intensity. The company says that in one case, the technology revealed the existence of a 4-ns glitch occurring every 0.33 s—just large enough to trigger the oscilloscope but invisible on its standard CRT—that had been wrongly ascribed to a transmission-line or crosstalk problem. In this case, the engineer had been on the point of having the pc-board layout reworked before the true source of the triggering error was discovered.

Sophisticated triggering is also available on the 2467. The scope triggers on pulses less than 1 ns wide at frequencies beyond 500 MHz. The standard onscreen trigger-level readout eliminates trial-and-error triggering—a valuable feature for single-shot events. A counter-timer-trigger option, with or without word recognizer, enhances performance, and a single button lets the user set the trigger level midway between the positive and negative signal peaks.

Another feature, Save-Recall, saves as many as 20 complex instrument setups in nonvolatile memory. The 2467 has several such single-button features; Cursors After Delay lets the user spot a single point of interest within the signal, magnify that point with the delayed sweep, and then accurately measure the signal characteristic with voltage or time cursors.

The 2467 oscilloscope can be delivered in eight weeks. The base price for the four-channel scope is $11,900. Options include the counter-timer-trigger for $1,000; with the word recognizer, it goes for $1,400. A video trigger adds $1,050, and an IEEE-488 interface bus adds $900.

—Ann Jacobs

Silicon Systems Inc., Marketing Communications Dept., P.O. Box 1700, Beaverton, Ore. 97077. Phone (800) 426-2200; in Oregon, (503) 627-9000 [Circle 340]

NOW IBM PC CAN SIMULATE OR MODEL VIA ETHERNET

Through computer-aided-engineering systems based on personal computers ably handle such pockets of system design as schematic capture, they have been less successful with compilation and simulation. Now Cadnetix is introducing software products that turn the IBM Corp. Personal Computer/XT and PC AT into complete CAE work stations [Electronics, Feb. 10, 1986, p. 13]. In addition, the company is adding an enhanced routing engine that routes in half the time of its predecessor.

The key concept behind the product portfolio is that of a CAE network. Cadnetix' network supports local data entry and manipulation and provides remote compilation, simulation, and modeling resources over an Ethernet. It provides the back-end power for the more complex portions of the design process through its 68020-based intelligent file server.

"Until now, the choice has been to accept poor performance during compilation and simulation of a design locally—
on a PC-based system, or add an expensive coprocessor with large memory to the PC to accommodate typical applications requirements," says marketing vice president Buck Feltman. Stand-alone PC-based systems quickly run out of steam for compilation and simulation, and are not even equipped for device modeling.

The CDX-3100 package makes the PC a complete facility for schematic capture and extraction of net lists for use by pc-board design systems. The CDX-3150, which requires a CDX-3100, transforms the PC into a full-function CAE work station that can access Cadnetix' virtual logic analyzer.

MORE DISK SPACE. Cadnetix' networking strategy for PC-based work stations solves a number of other problems, says Feltman. For example, the PC's relatively small disk-storage space cannot accommodate the 60- to 80-megabyte library that engineers typically require for efficient design. PC-based work stations on the Cadnetix network have either 140 or 280 megabytes of disk space for the library on the CDX-7100 or CDX-7200 network-server engines.

With stand-alone PC-based systems, users who required more disk space had to buy dedicated external disk drives for each PC. Alternate solutions have attempted to segment the library among several PCs, but heavy communication among them degrades performance, and a distributed library is difficult to maintain and update.

In lots of 10, the CDX-3100 sells for $7,900; it will be available in April. The CDX-3150 adds another $2,500 and will be available in June. They run under PC-DOS on a standard PC/XT or PC/AT enhanced with an IBM high-resolution color monitor and IBM's Enhanced Graphics Adapter card. When the computer and required file server are figured in, the cost for a three-node network is about $29,000 per node.

Feltman says that cost is less than Daisy Systems Corp.'s work stations and slightly more than such stand-alone alternatives as Futurenet systems. And Daisy customers have to buy their dedicated monitors and graphics card, he points out.

Cadnetix' cost advantage really comes into play in network expansion, Feltman says. Each new node will cost about $16,000, including the cost of the PC, compared with $20,000 for Daisy's IBM PC-based systems.

Cadnetix' new CDX-75000 Route Engine-Plus is a software and hardware enhancement of the company's original CDX-7500. Based on a 68020 microprocessor, the CDX-75000 has a new memory subsystem with a 32-bit data

You're designing for volume production — and you want high pot performance without running up costs. Answer: our new servo base CP 22, and bushing mount ECP 22. Both feature premium-quality MystR conductive plastic elements in cost-saving packages. Independent linearities to ±0.25%. Infinite resolution. Three standard resistances. Polymide bearings never need lubrication. Send for information, or call (617) 358-2777.

Waters Manufacturing, Inc.
Longfellow Center, Wayland, MA 01778 • (617) 358-2777 - Telex 948441

CIRCUITS AND SOFTWARE FOR ELECTRONICS ENGINEERS

Easy, reliable solutions to your design problems! Covers a vast range of design problems, organized into 25 vital categories by function. Contains hundreds of circuits and computer programs. Design appropriate circuitry to meet the most challenging specifications. Cut design time by adapting proven circuits and software to a wide range of applications. Save money and increase productivity by avoiding costly design errors.

These creative, new ideas and approaches keep you on top of what's happening in the latest circuitry developments.

Order your copy of R370-Circuits and Software for Electronics Engineers today! Send $19.95 to:
Electronics Magazine Books
P.O. Box 541
Hightstown, NJ 08520
609/426-5070

Attn: ECC
McGraw-Hill House
Maidenhead, Berkshire SL6 2QL England

Ten-day money back guarantee. Allow 4 to 6 weeks for delivery.

World Radio History
path to dual-ported RAM and a memory-address capacity of up to 16 megabytes. The company says its testing has shown from 10% to 60% routing-time improvements using customers' designs, along with via reductions of 50% to 60%.

The CDX-75000 uses a multilayer routing algorithm rather than the earlier system's layer-pair technique. The multilayer algorithm evaluates all layers simultaneously and finds the optimum trace path for making the connection; location systems look at only two board layers at a time. Not only does the new technique keep the number of vias low, but it also keeps the traces shorter. In some cases, the router can eliminate a layer altogether.

In one case, an eight-layer board with an equivalent IC count of 281 took 14 hours to route to completion using the layer-pair router on the older CDX-7500. Routed using the new 75000, the same board took just seven hours and had 59% fewer vias. The CDX-75000 is available now for $77,000.

The new products implement the Cadnetix mouse- and icon-based user interface, which is accepted as the CAE industry standard. The interface is based on the manipulation of icons and objects that represent intuitively recognizable operations within the schematic-capture and CAE editors.

Steve Zollo
Cadnetix Corp., 5757 Central Ave., Boulder, Colo. 80301.
Phone (303) 444-8057 [Circle 339]

Phone (408) 732-2400 [Circle 341]

The Golden Common Lisp network software package ties an Ethernet connection between IBM Corp. Personal Computers and Symbolics Inc. Lisp machines. GCLisp is a subset of Common Lisp, a widely used language for developing artificial-intelligence applications. Distinguishing services that the network provides are the session-layer interface and Symbolics' remote evaluation. GCLisp also performs file transfer, remote-terminal log-on, electronic mail, and remote printing.

A companion release, GCLisp 286 Developer, is a Common Lisp development system for IBM PC ATs. The package includes a large-memory interpreter and compiler, editor, and tutor, and it has an on-line help system.

The price of the GCLisp network, on two non-copy-protected disks, is $395 per PC node. The 286 Developer costs $1,195, and both are available now.

Phone (617) 492-2071 [Circle 354]

AMID'S 256-K DRAM CAN BE ADDRESSED THREE WAYS

A

dvanced Micro Devices' CMOS 256-K dynamic RAM can be addressed three different ways, two of which provide effective data rates as high as 18 MHz. The DRAM has a basic 100-ns access time, is configured as 256-K by 1 bit, and comes in versions with n-bit enhanced-page, or static-column-address modes. Also, lower-power versions of each type are available with standby current consumption of just 100 µA.

The 1.4-µm CMOS design produces addressing modes that are not feasible in n-MOS. AMD says that the conventional addressing scheme for commercial DRAMS is a page mode, which allows only 50 to 60 bits in a row to be addressed before the processing has to be interrupted to refresh the row-address strobe. With their static-column and enhanced-page modes, the AMD parts can address all 512 bits in a row without time out for refresh.

Also in their design, some critical time parameters found in conventional DRAMS, such as setup and hold times, are eliminated from timing consideration. This makes the buffer circuitry very fast on all the parts. The Am90C255 nibble-mode RAM allows for greater bandwidth with high-speed serial access of up to 4 bits of data. In nibble mode, the RAM has a 20-ns access time and a 40-ns total cycle time. This is twice the speed of conventional nibble-mode RAMs, AMD claims.

The RAM's speed makes it suitable for high-performance applications such as mainframe memory, computer graphics, and in buffer memory. The RAM is processed with a fully regulated substrate bias generator which, in addition to giving better transistor performance, functions as a power-up clamp to protect the chip from latchup.

The enhanced-page-mode version, the Am90C256, is designed for graphics applications, digital signal processing, and cache operations. Its addressing scheme allows for either random or sequential access of up to 512 bits in a row. This makes possible a continuous data rate of over 18 MHz, giving a typical cycle time as fast as 55 ns.

The static-column-address RAM, the Am90C257, also has a continuous data rate of over 18 MHz. In static column addressing, the RAS latches the row address; the column addresses are read directly from the address bus. By changing the column address, all 512 bits in a row can be accessed either randomly or sequentially.

The low-power versions—Am90CL255, -256, and -257—have a maximum standby-power dissipation of 101 µA, making them suitable for use in portable products. Their data-retention current need not exceed 200 µA. The RAMs are available now in standard 16-pin plastic DIPs for $15.25 each in lots of 100 pieces. In the second quarter, versions in ceramic DIPs will also be available, to be followed in the third quarter by military-temperature-range versions.

In June, the company plans to introduce faster versions having access times of 80 ns, which will sell for $16.50 each in 100-piece lots.

Eve Bennett
Phone (408) 732-2400 [Circle 341]
Be Sure Your Chips Come Off The Right Block.

TDK Chip Components.

With any automated production process only as good as the parts it works with, be sure to make reliability your top priority when choosing chip components for automatic PCB production. Chip Components from TDK.

Placed at strategic locations on your PCB's TDK Microbeads provide efficient noise suppression in sensitive circuits. Decades of experience in ferrite materials have been combined with advanced design technology to bring you, for the first time, auto-mountable chip type microbeads.

In Leadless Inductors, TDK has been occupying a position of technological and market leadership for a number of years. Famous for their extremely compact dimensions, constant quality levels and accurate adherence to specs, TDK Leadless Inductors with their wide range of available inductances and ratings have been instrumental in permitting extremely high circuit board densities and flexible automation.

TDK Ceramic Chip Capacitors utilize multilayer techniques in extremely compact dimensions, enabling space saving board design while maintaining narrow tolerances. Tape or magazine packaging is available for all TDK chip components for an optimum match to your production facilities. But whatever the package, three reassuring letters will be printed on it at no extra charge.

---

**Ferrite Chip Inductors**

<table>
<thead>
<tr>
<th>Type</th>
<th>Chip beads</th>
<th>Leadless Inductors</th>
<th>Class I</th>
</tr>
</thead>
<tbody>
<tr>
<td>NL</td>
<td>NLF (shielded)</td>
<td>MLF (shielded)</td>
<td></td>
</tr>
<tr>
<td>2.0 x 1.2 x 0.9</td>
<td>Zo: 5 - 90 at 100MHz</td>
<td>L: 0.1 - 1.2µH</td>
<td></td>
</tr>
<tr>
<td>3.2 x 1.6 x 0.6</td>
<td>Zo: 14 - 26G at 100MHz</td>
<td>L: 0.39 - 27µH</td>
<td></td>
</tr>
<tr>
<td>3.2 x 2.5 x 1.1</td>
<td>Zo: 25 - 26G at 100MHz</td>
<td>L: 12 - 56µH</td>
<td></td>
</tr>
<tr>
<td>3.2 x 2.5 x 1.3</td>
<td>Zo: 37 - 77G at 100MHz</td>
<td>L: 12 - 56µH</td>
<td></td>
</tr>
<tr>
<td>3.2 x 2.5 x 2.2</td>
<td>L: 0.12 - 100µH</td>
<td>L: 68 - 220µH</td>
<td></td>
</tr>
<tr>
<td>3.2 x 2.5 x 2.5</td>
<td>L: 1 - 1,000µH</td>
<td>L: 68 - 220µH</td>
<td></td>
</tr>
<tr>
<td>3.2 x 3.2 x 1.5</td>
<td>Zo: 55 - 130G at 100MHz</td>
<td>L: 1 - 1,000µH</td>
<td></td>
</tr>
<tr>
<td>3.2 x 3.2 x 2.2</td>
<td>L: 1 - 1,000µH</td>
<td>L: 68 - 220µH</td>
<td></td>
</tr>
<tr>
<td>3.2 x 3.2 x 3.2</td>
<td>L: 1 - 1,000µH</td>
<td>L: 68 - 220µH</td>
<td></td>
</tr>
</tbody>
</table>

**Ceramic Chip Capacitors (Typical)**

<table>
<thead>
<tr>
<th>Type</th>
<th>Class I</th>
<th>Class II</th>
</tr>
</thead>
<tbody>
<tr>
<td>CH</td>
<td>PH</td>
<td>RH</td>
</tr>
<tr>
<td>3.2 x 1.6</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>2.0 x 1.25</td>
<td>0.5</td>
<td>0.5</td>
</tr>
</tbody>
</table>

**Ferrite Micro Inductors (Typical inductance value)**

<table>
<thead>
<tr>
<th>Type</th>
<th>OL</th>
<th>L (µH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3 x 1.6 (mm)</td>
<td>L: 8µH at 1kHz</td>
<td></td>
</tr>
<tr>
<td>3.3 x 2.2</td>
<td>L: 15µH, 25µH at 1kHz</td>
<td></td>
</tr>
<tr>
<td>4.0 x 2.0</td>
<td>L: 25µH (Rdc: 600µH) at 1kHz</td>
<td></td>
</tr>
</tbody>
</table>

Dimensions, L x W x T (mm)

TDK CORPORATION OF AMERICA HEAD OFFICE 4711 West Golf Road, Skokie, IL 60076, U.S.A. Phone: (312) 679-8200 CHICAGO REGIONAL OFFICE Phone: (312) 679-8200 INDIANAPOLIS REGIONAL OFFICE Phone: (317) 872-0370 LOS ANGELES REGIONAL OFFICE Phone: (213) 500-1600 NEW YORK REGIONAL OFFICE Phone: (516) 625-0100 DETROIT DISTRICT OFFICE Phone: (313) 353-9393 HUNTSVILLE DISTRICT OFFICE Phone: (205) 539-4351 SAN FRANCISCO DISTRICT OFFICE Phone: (415) 943-9335 TDK UK LIMITED COMPONENTS DEPARTMENT Phone: (01) 891-2486 TDK ELECTRONICS EUROPE GmbH. Phone: (0210) 4870 TDK TAIWAN CORPORATION HEAD OFFICE AND TAIPEI SALES OFFICE Phone: (02) 712-5090 TDK SINGAPORE (PTE) LTD. Phone: 2735-022 TDK HONGKONG CO., LTD. Phone: 3-65 041 TDK CORPORATION KOREA BRANCH Phone: 785-6705 TDK CORPORATION NEW YORK REGIONAL OFFICE Phone: 500-1504 TDK CORPORATION BEIJING REPRESENTATIVE OFFICE Phone: 500-1504 TDK CORPORATION TOKYO JAPAN.

Circle 57 on reader service card
A Comprehensive Guide to Semiconductor Strategy in the 80’s!

Executive; Strategic Planners; Designers; Technicians; Don’t Miss This Book

Custom and semicustom IC’s have advanced to the center of the forum. Are you equipped to meet the challenges of an ever-changing industry?

Here now is the authoritative and official transcript from the seminar — Custom & Semicustom VLSI: Survival Strategies For The New Era,

A prestigious panel of industry experts presents up-to-date, significant information that probes major technological concerns such as:

- Company benefits by custom design
- Economical appropriateness for tackling custom
- Evaluation of gate arrays and standard cells
- Alternate processes to explore
- Suitability of CAD systems to your particular company

Custom & Semicustom VLSI: Survival Strategies For The New Era is a dependable, knowledgeable source that puts exclusive research highlights at your disposal. Offering a wealth of information effectively drawn and diagrammed, it is an absolute must for anyone who wishes to know:

- How is their growth ability accelerated by custom IC’s?

These questions are ones of survival. And OPPORTUNITY! Radical changes in industry result in radical growth for companies that understand these changes.

Let Custom & Semicustom VLSI: Survival Strategies For The New Era keep you informed.

Don’t hesitate - Order # R360 today!

This significant report is essential to anyone who acknowledges the value of custom and semicustom integrated circuits in today’s changing semiconductor market.

Send $150 or your company purchase order to:

Electronics Magazine Books
P.O. Box 541
Hightstown, NJ 08520

U.S. residents please include local sales tax.
Delivery will take 4-6 weeks.
Money-back guarantee if not satisfied.
ANNOUNCING
THE CONTEST TO END
ALL CONTESTS
The First Annual Electronics
Advertiser Audit Contest

As you know, the battle of January advertiser contests is once again in full swing. Top 10 Contests. Reader's Vote Contests. Excellence in Advertising Contests. But Electronics takes the ad contest idea one step further with its unique new advertising study program and contest for March.

In each of the five March issues of Electronics, a ballot will be included asking readers to choose their three favorite ads in that issue. Returned ballots or reasonable facsimiles will be entered into a drawing for $1,000 cash.

Top Three Winners In Each Issue Earn Free Ad Reruns.
The three advertisers receiving the most votes in each issue will receive a free rerun of their winning ads and a plaque commemorating their achievement. Since we're publishing five issues in March, there will be a total of 15 winning ads.

Grand Prize Winners Receive Free Reruns Of All March Ads.
After all the ballots are in, we'll determine the three ads that scored the highest over the course of the entire contest.

These three Grand Prize Winners will receive a special award, plus a free rerun of all the ads they ran during the entire month.

Win $1,000 Cash In A Separate Contest For Advertisers.
All advertising and marketing personnel in companies and agencies are invited to participate along with our readers by filling out a Special Advertiser's Ballot included in each March issue. Whoever comes closest to picking the 15 winning ads for the month in this Special Advertiser's Contest will receive an award acknowledging their skill in evaluating advertising, plus a free ad for their company—and $1,000 cash!

Remember, as an advertiser in our March issues, the greater your frequency, the greater your chance to become a Grand Prize Winner. And as an advertising or marketing professional, the March issues offer you an opportunity to test your skill, a free ad for your company, and $1,000 cash.
So, don't miss out—the March issues of Electronics could be your best-read advertising value of the year.

March Scheduling Guide

<table>
<thead>
<tr>
<th>Issue Date</th>
<th>Feature</th>
<th>Closing Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Semiconductor Technology</td>
<td>February 10</td>
</tr>
<tr>
<td>10</td>
<td>Supercomputer Technology</td>
<td>February 17</td>
</tr>
<tr>
<td>17</td>
<td>Semiconductor Processing</td>
<td>February 24</td>
</tr>
<tr>
<td>24</td>
<td>Instruments Special Issue SAS Lab Power Supplies</td>
<td>March 3</td>
</tr>
<tr>
<td>31</td>
<td>Local-Area Networks</td>
<td>March 10</td>
</tr>
</tbody>
</table>


ELECTRONICS IS BACK. EVERY WEEK.

McGraw-Hill Information Systems
1221 Avenue of the Americas
New York, New York 10020
(212) 512-6642
The next time you travel, bring along a cheap friend, the AT&T Card. It's the most inexpensive way around to make AT&T Long Distance Service calls from a public phone. Cheaper than coins for out-of-state calls. Cheaper than calling collect. The AT&T Card—a tight wad you could learn to love.

Apply today. Dial 1 800 CALL ATT  Ext. 4585

**DIRECTORY.** To meet the research needs of the high-technology community, Corporate Technology Information Services Inc. has just released the 1986 edition of the Corporate Technology Directory. The set consists of two volumes of corporate profiles of more than 12,000 U.S. and overseas manufacturers, including major private companies, plus an index volume. Each company's listing includes its startup date; a brief business description; the names, titles, and responsibilities of up to eight top executives; annual revenue and number of employees; the company's status (public or private and subsidiary, division, or independent); and the product or products that are manufactured.

The "products manufactured" category is coded by CorpTech's proprietary high-technology classification system, which replaces the U.S. Standard Industrial Classification product code with 3,000 industry-specific codes. In this way, the directory's user can locate companies in categories as narrow as fiber-optic repeaters or medical ultrasound imaging.

The CorpTech Directory will also be available on April 1 as a data base. For a free brochure that gives more information, including price, for the hardcopy set or the electronic version, call (617) 235-5330 or write the publisher at 2 Laurel Ave., P. O. Box 281, Wellesley Hills, Mass. 02181. [Circle reader service number 421]

**FAST PULSES.** Picosecond Pulse Labs Inc. is offering free copies of its short-form catalog, which describes such products as very fast pulse generators and other laboratory instrumentation. Coaxial components for communications applications outside the lab are also listed. Call (303) 443-1249 or write the company at P.O. Box 44, Boulder, Colo. 80306. [Circle 422]

**CONNECTORS.** Heavy-duty multipin connectors for machine tools, robotics, process control, and other stressed-environment purposes are described in a free 24-page catalog from Electrovert. For a copy of literature number 304-02, write Electrovert Inc., 466 Main St., New Rochelle, N.Y. 10801. [Circle 425]
ANALOG DESIGN. Valid Logic Systems is offering a free data sheet on the Analog Designer S-320, a computer-aided engineering system that features a computer-modeled lab bench on the screen. This work station interfaces with personal-computer layout systems and runs Valid’s version of Spice circuit-simulation software. Write to Valid Logic Systems Inc., 2820 Orchard Park Way, San Jose, Calif. 95134 for a copy; phone (408) 945-9400. [Circle 423]

PLOTTERS. A 16-page, full-color users’ report describes applications for electrostatic color and monochrome plotters from Versatec Inc. The plotters can be used in scientific and engineering graphics, architecture, mapping, and geophysical surveys. Requests should be sent to the company at 2710 Walsh Ave., Santa Clara, Calif. 95051, or call (800) 538-6477; in California, (800) 341-6060. [Circle 424]

MIL/JAN. This free brochure presents the manufacturer’s qualifications as a supplier of military linear products—its specification system, quality policies, and procedures. Also included is a 232-item military-parts list for components manufactured in both bipolar and CMOS technologies. To receive a copy, write to Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, Calif. 95035; phone (408) 942-0810. [Circle 426]

TEST. A free application note, “Characterize Amplifier Compression, Gain, and Impedance Match,” describes a gain-compression test set that operates in the range of 500 MHz to 26.5 GHz. Copies are available from Wiltron Co., 490 Jarvis Dr., Morgan Hill, Calif. 95037; phone (408) 778-2000. [Circle 427]

ASSEMBLY SYSTEMS. A 16-bit intelligent control terminal for automatic electronic assembly systems is detailed in free literature from Universal Instruments. The terminal operates as part of a Universal Instruments Control System. For a copy, call Universal Instruments Corp. at (607) 775-1102 and ask for bulletin 8341; or write the company at Kirkwood Industrial Park, P. O. Box 825, Binghamton, N. Y. 13902. [Circle 428]

VAX CONTROLLERS. A free “Pocket Guide to Controllers” describes Distributed Logic Corp.’s controllers for VAX and other Digital Equipment Corp. computers. The line includes Storage Module Drive controllers, asynchronous communications controllers, and ¼-in. and ½-in. tape couplers. The company is located at 1555 S. Sinclair St., P. O. Box 6270, Anaheim, Calif. 92806, or call (714) 937-5700. [Circle 429]
NEW EDITION
All standards are new, revised, or reaffirmed since the previous edition

DATA
COMMUNICATIONS
STANDARDS
All 123 interface protocol standards set by:
• CCITT • ISO • ECMA
• ANSI • EIA
• U.S. Government

Special feature for instant access to the applicable standards:
Cross-reference tables of the similar and interfacing standards of each standards organization.

Hardware and software that improve the productivity of work station systems will be a topic of big interest at the 1986 IEEE Work Station Technology & Systems Conference in Atlantic City, March 18-20.

Wolodymyr Luciw, a computer scientist at Sperry Corp., in Blue Bell, Pa., and program chairman for the conference's steering committee, says one important paper will describe an interface between Apple Computer Inc.'s Macintosh personal computer and AT&T Co.'s Unix operating system. The interface combines the Macintosh's graphics environment with the power of Unix, Luciw says, and it lets several applications run concurrently. He expects that the paper "will generate a lot of interest because of the relatively low cost" of setting up a work station using the Macintosh and the interface.

Besides hardware and software, the conference's 30 papers will cover such topics as data security, signal processing, very large-scale integration, print-ed-circuit-board design, mainframe interfacing, and networks. There will even be a paper on work stations and the handicapped. Luciw says that "handicaps have something to teach us" about the best ways to enter data. "Maybe we're not taking full advantage of touch and sound," he says.

One of the conference's seven sessions will focus on VLSI and pc-board design. It features a paper by Edward Gold of ITT Corp., who will also chair the session on networks. Gold's paper will describe a work-station-based VLSI design system that includes tools for layout, simulation, and data translation.

Luciw points out that system designers are paying more attention to artificial intelligence, and one paper will deal with ways to apply AI to existing VLSI design tools. Next year, Luciw expects to have an entire session devoted to AI.

IEEE TARGETS WORK-STATION PRODUCTIVITY

ESC '86: Eastern Simulation Conference, Society for Computer Simulation (P.O. Box 17900, San Diego, Calif. 92117), Omni International Hotel, Norfolk, Va., March 10-12.

Cimtech '86: Computer and Automated Systems of the Society of Manufacturing Engineers (Cheri Willeits, SME, 1 SME Dr., Dearborn, Mich. 48121), Boston Sheraton, Boston, March 10-13.


IZS '86: International Zurich Seminar on Digital Communications, IEEE Computer Society et al. (Albert Kundig, Swiss Federal Institute of Technology, Gloriastrasse 35, Ch-8092, Zurich, Switzerland), Swiss Federal Institute of Technology, Zurich, March 11-13.


TCA Northwest Telecommunications Conference, Telecommunications Association (TCA, Northwest Chapter, P.O. Box 4301, Seattle, Wash. 98104), Westin Hotel, Seattle, March 12-14.

19th Simulation Symposium, IEEE Computer Society et al. (Linda A. Holbrook, GTE Data Services, P.O. Box 1548, Tampa, Fla. 33601), Bay Harbor Inn, Tampa, Fla., March 12-14.


Work Station Technology & Systems Conference, IEEE (Helen Yonan, Moore School of Electrical Engineering, University of Pennsylvania, Philadelphia, Pa., 19104) Bally's Park Place Hotel, Atlantic City, March 18-20.

Advertisers Index

Order your copy today for the industry's most often-used directory:

- It's three directories in one
- Includes more than 4,000 product listings (approx. 700 pages)
- Contains over 5,000 company listings (approx. 400 pages) including:
  - Company name, address and phone number.
  - Name and title of contact for sales information.
  - Number of engineers at plant and number of employees.
- Annual dollar sales volume.
- Local sales offices and manufacturers representatives.
- Local distributors.
- Instant referral to company's advertisements.
- Offers FREE current catalog retrieval service (approx. 1300 catalogs)

Price: $40 USA & Canada
$50 elsewhere (add $30 for airmail)

Send order with payment to:
Regina Hera
Electronics Buyers' Guide
1221 Avenue of the Americas
New York, NY 10020

Advertisers Index

<table>
<thead>
<tr>
<th>Company Name</th>
<th>Pages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Devices</td>
<td>34</td>
</tr>
<tr>
<td>ATT Communications Public Program</td>
<td>60-61</td>
</tr>
<tr>
<td>Data Translation</td>
<td>12</td>
</tr>
<tr>
<td>Deutsche Messe-und Ausstellungen - A. G.</td>
<td>6E</td>
</tr>
<tr>
<td>Elek-Tek</td>
<td>8</td>
</tr>
<tr>
<td>Fujitsu Ltd.</td>
<td>7E</td>
</tr>
<tr>
<td>Futurenet</td>
<td>3rd C</td>
</tr>
<tr>
<td>Infotek Systems</td>
<td>1</td>
</tr>
<tr>
<td>Kyowa Electronic Instruments Co., Ltd.</td>
<td>2nd C</td>
</tr>
<tr>
<td>Leader Instruments</td>
<td>4</td>
</tr>
<tr>
<td>National Semiconductor</td>
<td>6,7</td>
</tr>
<tr>
<td>OKI Semiconductor</td>
<td>4th C</td>
</tr>
<tr>
<td>PEP GmbH</td>
<td>32,33</td>
</tr>
<tr>
<td>Philips Elcoma</td>
<td>5E</td>
</tr>
<tr>
<td>Philips T &amp; M</td>
<td>4E</td>
</tr>
<tr>
<td>Rohde &amp; Schwarz</td>
<td>1E</td>
</tr>
<tr>
<td>SGS Semiconductor Corporation</td>
<td>45</td>
</tr>
<tr>
<td>Shannon Development</td>
<td>47</td>
</tr>
<tr>
<td>Sharp Corporation</td>
<td>48</td>
</tr>
<tr>
<td>Siemens AG</td>
<td>2E,3E</td>
</tr>
<tr>
<td>Silicon Systems Incorporated</td>
<td>2</td>
</tr>
<tr>
<td>TDK Corporation</td>
<td>57</td>
</tr>
<tr>
<td>Waters Manufacturing</td>
<td>55</td>
</tr>
</tbody>
</table>

Classified and employment advertising

- Asia, Inc.
- Automatic Connector
- Data Systems Inc.
- Omation, Inc.
- Radio Research Instrument
- ZTEC

Classified and Employment Advertising

- For more information of complete product line see advertisement in the latest Electronics Buyers Guide
- Advertisers in Electronics International
- Advertisers in Electronics domestic edition

Available!

1985-86 Electronics Buyers' Guide

Order your copy today for the industry's most often-used directory:

- It's three directories in one
- Includes more than 4,000 product listings (approx. 700 pages)
- Contains over 5,000 company listings (approx. 400 pages) including:
  - Company name, address and phone number.
  - Name and title of contact for sales information.
  - Number of engineers at plant and number of employees.
- Annual dollar sales volume.
- Local sales offices and manufacturers representatives.
- Local distributors.
- Instant referral to company's advertisements.
- Offers FREE current catalog retrieval service (approx. 1300 catalogs)

Price: $40 USA & Canada
$50 elsewhere (add $30 for airmail)

Send order with payment to:
Regina Hera
Electronics Buyers' Guide
1221 Avenue of the Americas
New York, NY 10020

Electronics / February 17, 1986
NATIONAL, XEROX IN JOINT DEAL

Xerox Corp. and National Semiconductor Corp. intend to become close partners in semicustom application-specific integrated circuits, following the trend of pairing off by chip makers and their systems-house IC customers. Under the deal, Xerox will buy the majority of its semicustom chips from National. In return, the Santa Clara, Calif., chip maker will turn over ASIC technology to Xerox's Electronics Division in El Segundo, Calif., which will fabricate some chips in-house. The technology transfer involves National's 2-μm CMOS process, design, tooling, and chip-packaging information as well as design automation software that will be adapted to Xerox's proprietary work stations. Xerox will use its systems expertise to create new standard-cell designs, which will be placed into National's library. Some will be kept proprietary.

RESHUFFLE AT COMPUTERVISION

There is new leadership at Computervision Corp., a computer-aided design and manufacturing pioneer that has fallen on hard times. Last week, the Bedford, Mass., company announced that vice chairman and chief operating officer Robert L. Gable was elected president and CEO, succeeding James Barrett. Also last week, Computervision reported a $21 million loss in the fourth quarter on revenue of $117 million, down from a profit of $14.9 million on revenue of $163 million in the previous year.

U.S. ELECTRONICS DEFICIT GROWS

The U.S. worldwide trade deficit for electronics products increased to $8.6 billion in 1985, 39% more than the $6.2 billion negative balance reported for 1984, according to an estimate by the American Electronics Association. The U.S. electronics trade deficit with Japan is estimated to have been $17.6 billion, an increase of 17% over the $15 billion shortfall in 1984. Worldwide, there was a deficit in every electronics category but computers. Japanese imports outsold U.S. exports in every category. The largest deficit was posted in consumer electronics. The U.S. imported $11.7 billion worth of products in this category ($7.9 billion from Japan) and exported $600,000.

STEVEN JOBS TAKES OVER PIXAR

Pixar, the computer graphics division of Lucasfilm Ltd., has been spun off and sold as a separate company to Apple Computer Inc. founder Steven P. Jobs and to Pixar employees. Jobs, who bought a majority interest for an undisclosed amount in the millions, will be Pixar's chairman of the board. Lucasfilm will continue as a major customer of the new company. Pixar has also announced that it will soon bring to market a high-power graphics engine called the Pixar Image Computer called thePixar Image. The company claims it can outperform supercomputers at specialized image-processing tasks.

KODAK TIGHTENS ITS BELT

Eastman Kodak Co. said it will roll back worldwide employment by 10% this year, eliminating almost 13,000 of the company's 128,950 jobs. In addition, the Rochester, N.Y., photographic giant ordered a 5% cut of all departmental budgets, a freeze on pay raises for 130 top executives, and a change in the way wage-division bonuses are paid out to more closely tie the benefits to earnings. "Call it a major acceleration of our cost-cutting measures," a spokesman said.

"We've been cutting costs back since 1983, when we reduced worldwide employment by 11,000 jobs," Kodak is hoping voluntary retirement incentives will account for a major portion of the cuts.

MATSUMITA SELLS SEQUENT MACHINES

Matsushita Electric Trading Co., Osaka, Japan, will import and distribute parallel-parallel computer systems made by Sequent Computer Systems Inc., Beaverton, Ore. The systems—Sequent's Balance 8000 and 21000—will be imported by Armco Corp., a Matsushita subsidiary. The Balance 8000 and 21000 are high-performance, general-purpose, parallel-computer systems that include from 2 to 30 tightly coupled NS 32032 32-bit microprocessors.

IBM MAINFRAME SALES DECLINE

IBM Corp. has disclosed that both sales and rentals for its mainframes and superminicomputers declined 9.7%, to $6.76 billion, in the U.S. last year, offsetting gains in sales of software and peripherals. The news comes on the heels of last month's announcement that worldwide net income for the big computer maker declined 0.4% compared with 1984—from $6.58 billion to $6.55 billion on sales that were up from $45.9 billion in 1984 to $50.1 billion in 1985. To spur sales of its high-end processors, IBM last week cut the price of its new mainframe series, the 3090, by 10%, and reduced the price of its older mainframe computers by up to 21%. It also introduced two new lower-cost 3090 models and new versions of its 4381 mid-range processing family, the 4381 models.

ISRAEL UNVEILS IBM PC CLONE

An extremely low-cost IBM Corp. Personal Computer-compatible, which its makers say will do everything the 1C does for a fraction of the price, has been introduced by Moah Computer Systems, Petah Tikva, Israel. Dubbed the Brain 88, the machine includes 256-K of memory and a single disk drive, but no monitor. It is being offered first to importers in Britain for $350.

BIG EUROPE DRIVE MARKET SEEN

Thanks to the new technologies of thin-film heads, plated media, and vertical recording, computer users in Europe will create a 30% annual growth rate for disk drives and controllers through 1989, according to New York market researcher Frost & Sullivan Inc. By 1989, there will be an annual market of 27 million units worth $3.5 billion, compared with 1985 levels of 9.5 million units worth $4.5 billion in magnetic disk drives. Bubble memories, semiconductor memories, and magneto-optics are among the major threats to rotating magnetic disk drives, say the researchers, but through 1989, the first two are unlikely to offer serious competition to disk drives.

COMMODORE TAKES 25% OFF AMIGA

In a bid to be taken seriously in the college microcomputer market, Commodore International Ltd. is slashing 25% off the $1,985 retail price of its Amiga 1000 personal computer with one disk drive, a color monitor, and a 256-K random-access-memory expansion cartridge. The discount will be available to students and faculty until June 30. Commodore has bet heavily that the Amiga, introduced last summer, would help save the struggling company, but limited software availability has held sales down. The Amiga has less than 1% of the U.S. specialty-store retail market.
MAINFRAME PCB LAYOUT POWER ON YOUR DESKTOP IBM PC.

FutureNet's new DASH-PCB™ is an innovative pc-based layout "expert." Now, features of a proven PCB layout system are yours to complement our famous DASH Schematic Designer. Exclusive features, previously available only on an expensive mainframe, are combined in a package that is cost-effective, easy to learn, easy to use, and highly productive.

Here's an "Expert Multi-Strategy”™ router without equal. Your choice of routing strategies, plus trace hugging, rubber-banding, fine line rules, 45 degree routing, large board capacity, 18 trace layers, and easy to use command menus. It's truly auto-routing with the mind of an expert.

FREE BROCHURE!
Call today for your copy of the complete description of FutureNet's exciting new DASH-PCB — the "expert" system that puts mainframe power on your IBM PC.
Available now: Board savings of greater than 50% on equal high densities! OKI'S off-the-shelf SIMMs* supply megabits of DRAM in the most popular 256K x 8/9 organization. In addition, each module contains built-in chip capacitors.

Instant surface-mount capability: Get surface-mount density and reliability without risk, capital expense or delay. OKI's advanced SIMM technology has completely automated the process for you: die, packaging, assembly, full testing, all from a single source — to make DRAM modules much easier to get, easier to use, easier to handle in the field. (And, soon, easier to upgrade to megabyte modules too, through OKI TAB breakthroughs.)

FREE SOCKET with every OKI DRAM SIMM sample ordered.

Limited Time Offer: Ask OKI to send you a sample set of our MSC 41256 SIMM for just $44, and we'll include its socket without charge. OKI'S SIMM Sample Set consists of 2 modules, each with nine 256K DRAMs & nine capacitors, plus the free 60-pin carrier and full technical data.

Please send ___ OKI DRAM SIMM Sample Sets( with socket. Price per set is $44.00, plus $4.00 for shipping/handling: $48.00 Set/total, sales tax included. Offer limited to 3 sets per customer. Check or money order for $ ____ enclosed. (Sorry, no company purchase orders please)

Send technical data on the OKI 256K DRAM SIMM.

Name/Title ____________________________
Company ____________________________
Address _____________________________
City __________________ State ______ Zip __________
Tel. ( ) _____________________________