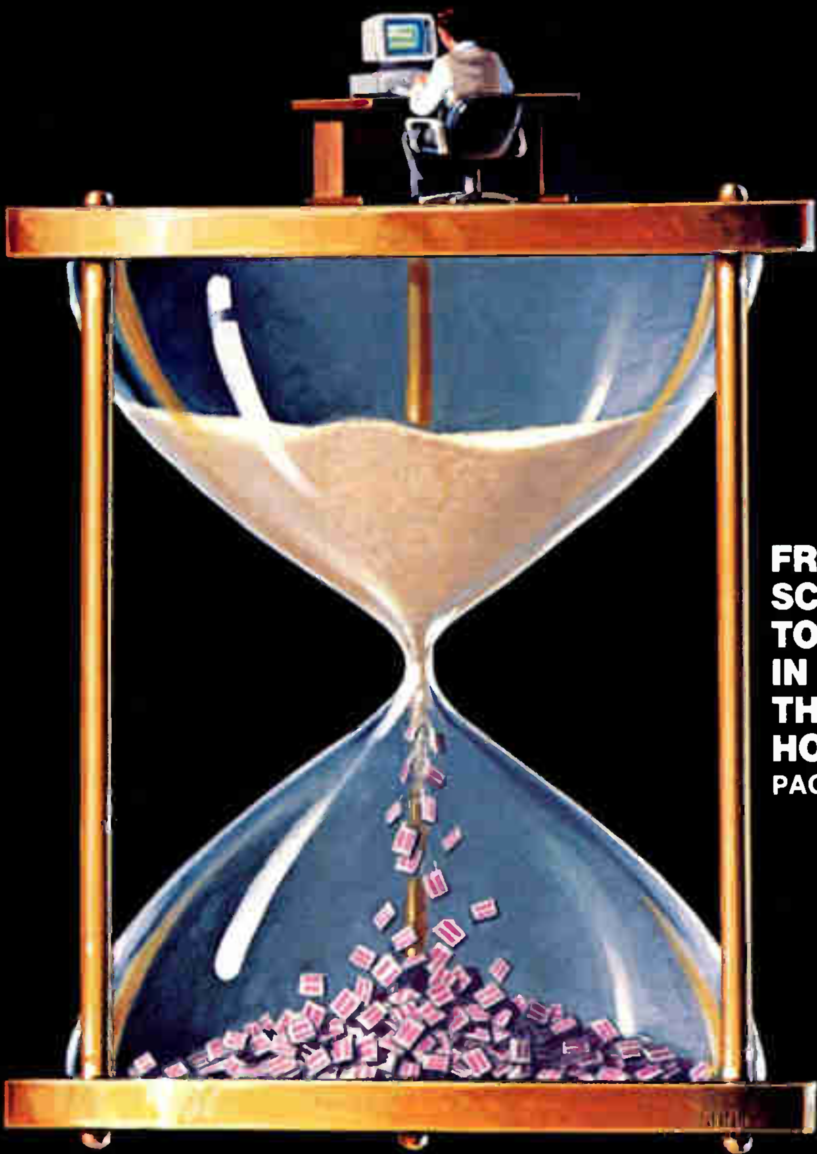
A McGRAW-HILL PUBLICATION THREE DOLLARS

# Electronics

THE WORLDWIDE TECHNOLOGY WEEKLY JUNE 16, 1986

# TURNING A PC INTO A SILICON COMPILER



FROM SCHEMATIC TO FOUNDRY IN LESS THAN AN HOUR

PAGE 37

See us at NCC
Booth #1534
Featuring Software
SIEMENS


*"Success! Another order."*

*"Systems with our kind of power and upgrade potential are difficult to resist."*

*"Certainly, we've covered all their needs today, and well into the future."*

*"And that's good for us, too. Software re-writes are totally unnecessary."*

*"There is no doubt—Series 32000 was the right decision. National was on target from the beginning..."*

*"...And now, so are we."*

# How Siemens builds multi-user systems compatible with the future. Using National's Series 32000® family.

Not long ago, Siemens faced a difficult challenge in the emerging office automation market: How to build a family of compatible micros and minis that cover the entire spectrum of business applications—from single-user systems to high performance, multi-user SINIX™ systems. And without having to reinvent the software "wheel" for every product.

Such a demanding objective required demanding specifications: true 32-bit architecture; a complete computing cluster, including memory management and floating point coprocessors; full software compatibility, both upward and downward; high level language support; and comprehensive development tools.

The Siemens design team investigated a range of 32-bit solutions, and found only one that met all their needs: National's Series 32000 family.

Unlike other 8- and 16-bit processors being extended upward, the Series 32000 has no programmer-visible changes in architecture—throughout the entire family. So Siemens could develop any application the market demanded, now or in the future, without depreciating its existing software investment.

Which means the Series 32000 was not only the right *engineering* decision for today, but was also the right *business* decision for tomorrow.

But find out how you can build the future into *your* next 32-bit design. Contact National Semiconductor today.

National's Series 32000, MS 23-200
P.O. Box 58090
Santa Clara, CA 95052-8090

**National Semiconductor**
We're doing it.

Circle 1 on reader service card

# CAN YOU PASS THIS DTMF TRANSCEIVER QUIZ?

## Q. The best DTMF transceiver on the market today:

| | | *True* | *False* |
|---|---|---|---|
| 1) | Has a Central Office quality DTMF receiver on-chip. | ☐ | ☐ |
| 2) | Has a low-distortion/high-accuracy DTMF generator on-chip. | ☐ | ☐ |
| 3) | Has a complete 6800 microprocessor interface on-chip. | ☐ | ☐ |
| 4) | Can transmit DTMF tone bursts with precise timing. | ☐ | ☐ |
| 5) | Has a call progress tone filter which outputs tones in digital wave form. | ☐ | ☐ |
| 6) | Can generate single or dual tones. | ☐ | ☐ |
| 7) | Has excellent dial tone rejection. | ☐ | ☐ |
| 8) | Has superb third tone tolerance. | ☐ | ☐ |
| 9) | Permits adjustable guard times. | ☐ | ☐ |
| 10) | Operates from a single 5 volt power supply. | ☐ | ☐ |
| 11) | Operates from −40°C to +85°C. | ☐ | ☐ |
| 12) | Employs high-speed/low-power ISO²-CMOS™ fabrication in a 20-Pin ceramic or plastic package. | ☐ | ☐ |

## A. It's all true of the Mitel MT8880 DTMF Transceiver!

This robust performer is the natural choice for such applications as intelligent modems, remote-controlled devices, telephone-enhanced personal computers, PABXs, Central Office switches, intelligent telephones, paging systems, mobile radio systems and programmable autodialers. Contact your local Mitel sales office for further information.

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Electronics

# Electronics

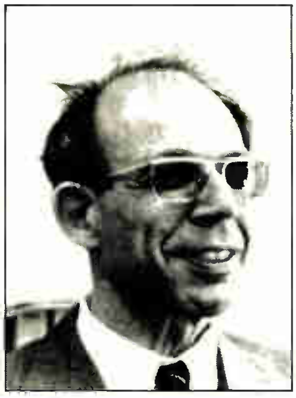
## International edition






Charlie Cohen is back on station in Japan, and this week's issue is enhanced by a news story from our veteran Tokyo bureau chief. On p. 28, Charlie describes a system for testing ultralarge-scale integrated circuits developed jointly by Hitachi Ltd. and Toyohashi University of Technology.

Charlie had taken a month's vacation back in the States, part of which he spent renewing old acquaintances on the staff and matching the faces of new members to the names that appear on messages to him. The Brooklyn native also ate some good New York pastrami sandwiches, stocked up on computer books, and bought a computer (AT&T PC 6300+) as well as the hardware needed to set up a mailbox in his office. In addition, he visited Silicon Valley, describing our new San Mateo office as "convenient to nothing but equidistant to everything," and looked in on the Vancouver Expo.



**COHEN:** An observer of change in two cities.

Charlie's regular vacation trips between two of the largest and most internationally influential cities in the world give him a unique perspective on change. New York is going through a convulsion of construction, but what about Tokyo? There, too, change has become rampant.

As Cohen describes it, "Not far from our office, behind the American Embassy, a whole hillside of old buildings has just been transformed by a renewal program that covered it with a large hotel, office buildings, and apartment houses. Across the street from this project, twin office towers went in a couple of years ago. Construction is going on full speed with more major projects planned. But the higher yen and increased protectionism in the U.S. and elsewhere could force a slowdown in the economy within a few years as more manufacturing is moved to consuming nations and offshore procurement is increased."

Some 40 months ago—Feb. 24, 1983, to be exact—we ran a four-page questionnaire entitled "The Changing Engineer." Readers were asked to reply to questions designed to let us know how practitioners were affected by changes in the industry and how they perceived themselves and their profession. The results were printed in a 20-page special report, "The Changing Face of Engineering" [*Electronics,* May 31, 1983, p. 125].

This week, we received what we strongly believe will be the last questionnaire from that report. It came from an engineer who works for NCR Corp. in Madrid. The sender offered no explanation of why it took so long to reply. But we like to think he is just a typically faithful—and thoughtful—reader.

Laurence Altman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# WEEK 34

AMD wants to put power back where it belongs: In your hands.

We're proud to announce the Am29C821 10-bit CMOS Bus Interface Register. It's a member of the high performance Am29C800 Family: The family that delivers the performance you expect from the bipolar Am29800 Family but with stingy power demands.

### Am29C821

## Seize power.

The register requires a low power stand-by current of 80 microAmps. But AMD promises that taking power from it won't slow it to molasses. The Am29C821 has a propagation delay of 12ns.

You can also use it in place of, or along with, the Am29800 bipolar counterpart to match your drive and power requirements. Used where an Am29821 provides 48mA drive, the Am29C821 provides 24mA drive.

Get yourself the Am29C821. And then give the leftover power to someone who can really use it. You.

# WEEK 35

Announcing the Am29C116: The 16-Bit CMOS Microprocessor that uses only 25 percent of the power of its bipolar counterpart. The rest of the power is yours. And the Am29C116 costs less than the bipolar. The savings are yours.

### Am29C116

## Satisfy your lust for money and power.

The Am29C116 is one more member of AMD's CMOS Microprocessor Family. It's the pin- and function-compatible version of the bipolar Am29116. Coming from such a heritage, you'd expect the Am29C116 to have the same computing power and flexibility. It does. And it has a system cycle time of 125ns.

It's microprogrammable so you have the flexibility of designing your own instruction codes. Plus, its architecture provides powerful insert/extract and bit manipulation capabilities for complex bit control. It has a three input ALU, barrel shifter and a priority encoder.

If you want to build in blazing speed, another member of the Am29100 Microprocessor Family might be for you. Like the high speed bipolar Am29116A with a system cycle time of 80ns.

And once you've acquired all that power and money from using the Am29C116, you can lust for something else.

# WEEK 36

In the daily trial between high performance and low power, a winner has emerged: The Am29C843 9-Bit CMOS Bus Interface Latch. Part of the Am29C800 Family of products, it keeps performance high on a meager power diet.

### Am29C843

## An open and shut case.

The latch waits patiently on a stand-by current of 80$\mu$A. But when it comes to speed, the propagation delay is 11ns.

The Am29C843 can also be used along with or in place of its Am29800 bipolar counterpart. Get just the balance of speed and power you need for your design. The Am29C843 provides 24mA drive, compared to the Am29843 which provides 48mA drive.

When design flexibility is important, the Am29C843 9-Bit CMOS Bus Interface Latch can be just as helpful. It has flow-through architecture. The ninth bit can provide error detection or diagnostics capability.

Why not see the Am29C843 9-Bit CMOS Bus Interface Latch and judge for yourself?

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# WEEK 37

The digital telephone and ISDN are going to revolutionize voice and data communications. AMD gives you the cleanest way to go digital. Our ISDN Family of five devices gives you the standard interfaces plus power controllers for Integrated Services Digital Network.

**Am7936**

## The power behind ISDN

The first member of the family is the Am7936 Subscriber Power Controller. It's the world's first ISDN power feed controller on a single chip.

The Am7936 meets the ISDN CCITT power recommendations. Including emergency conditions when local power is lost. As a matter of fact, it works in any phantom-feed system.

By the end of the year our ISDN Family will include the Digital Subscriber Controller, Digital Exchange Controller, ISDN Data Controller, and Quad Exchange Power Controller. They'll use both bipolar and CMOS technology to give you the optimum balance of system performance and efficiency with the lowest chip count.

Check out AMD's ISDN Family. And feel the power.

On October 1, 1985, Advanced Micro Devices told the world it would deliver fifty-two new products in one year. A new product every week. Tall order.

So where's seeking the impossible gotten us? Right where we expected. After twenty-six weeks, we're 26 for 26. Batting a cool 1,000. And here's what the world is telling us:

"Reduced networking costs." "State machines that have simplified the state-of-the-art." "More powerful, smaller air traffic control systems." "Extraordinary graphics for ordinary workstations." "PC's with fax capabilities."


And more. But that's only half the story. Watch this space for more chances to make your best idea better than you hoped it could be.

More new products. One a week. Every week. On the shelf. In volume.

Watch us open up the lead.

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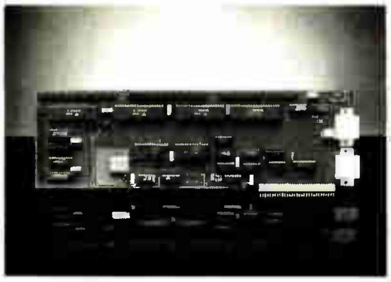
For more information, contact the sales agent nearest you or write the word "Thirty-seven" on your letterhead and mail to Advanced Micro Devices, Mail Operations, P.O. Box 4, Westbury-on-Trym, Bristol BS9 3DS, United Kingdom.





## MEETINGS

**Design Automation Conference,** IEEE (J. D. Nash, Raytheon Co., Bedford, Mass. 01730), Las Vegas Hilton, Las Vegas, June 29-July 2.

**International Conference on Radio Receivers,** Institution of Electronic and Radio Engineers (99 Gower St., London, WC1E 6AZ, England), University College of North Wales, Bangor, England, July 1-4.

**Compass '86**: Computer Assurance Conference, IEEE (Albert W. Friend, P. O. Box 3815, Gaithersburg, Md. 20878), Georgetown University, Washington, July 7-11.

**14th International Optical Computing Conference,** IEEE Computer Society (Joseph Shamir, Department of Electrical Engineering, Technion, Haifa 32000, Israel), Hebrew University, Jerusalem, July 7-11.

**Cable '86:** 4th International Conference and Exhibition on Satellite and Cable Television, Online International Ltd. (Pinner Green House, Ash Hill Drive, Pinner, Middlesex HA5 2AE England), Metropole Centre, Brighton, England, July 8-10.

**PC Expo,** PC Expo (Steven Gross, 333 Sylvan Ave., Englewood Cliffs, N. J. 07632), Jacob K. Javits Convention Center, New York, July 9-11.

**Britec 1986:** British Information Technology Exhibition and Conference on Engineering Software, Computational Mechanics Ltd. (Elaine Taylor, Computational Mechanics Ltd., Ashurst Lodge, Ashurst, Southampton, SO4 2AA, England), Hilton at Colonial Rte. 128, Wakefield, Mass., July 14-16.

**Net/Comm Security '86,** Computer Security Institute (360 Church St., Northborough, Mass. 01532), Marriott Crystal Gateway, Arlington, Va., July 14-16.

**International Computers in Engineering Conference,** American Society of Mechanical Engineers (ASME, 345 E. 47th St., New York, N. Y. 10017), Hyatt Regency, Chicago, July 20-24.

**7th European Conference on Artificial Intelligence,** European Coordinating Committee on Artificial Intelligence and Society for the Study of Artificial Intelligence and Simulation of Behaviour (Conference Services Ltd., 130 Queens Rd., Brighton, Sussex BN1 3WE, England), Brighton Conference Centre, Brighton, July 21-25.

**ACM Conference on Lisp and Functional Programming,** Association for Computing Machinery (Robert Halstead, Massachusetts Institute of Technology, 419 Technology Square, Cambridge, Mass. 02139), MIT, Cambridge, Aug. 4-6.

**National Conference on Artificial Intelligence,** American Association for Artificial Intelligence (445 Burgess Dr., Menlo Park, Calif. 94025-3496), University of Pennsylvania, Philadelphia Civic Center, and Franklin Plaza Hotel, Philadelphia, Aug. 11-15.

**30th International Technical Symposium on Optical and Optoelectronic Engineering,** Society of Photo-Optical Instrumentation Engineers (P. O. Box 10, Bellingham, Wash. 98227-0010), Town and Country Hotel, San Diego, Aug. 17-22.

**Siggraph '85,** Association for Computing Machinery and IEEE (Siggraph Conference Management, 111 E. Wacker Dr., Chicago, Ill. 60601), Dallas Convention Center, Dallas, Aug. 18-22.

**International Conference on Parallel Processing,** IEEE Computer Society and Pennsylvania State University (IEEE Computer Society, 1730 Massachusetts Ave., N. W., Washington, D. C. 20036-1903), Pheasant Run Resort, St. Charles, Ill., Aug. 19-22.

**ICSSDM:** 1986 International Conference on Solid State Devices and Materials, the Japan Society of Applied Physics (1986 ICSSDM, c/o Business Center for Academic Societies Japan, 4-16, Yayoi 2-chome, Bunky-ku, Tokyo 113, Japan), Tokyo Prince Hotel, Tokyo, Aug. 20-22.

**3rd International Congress on Advances in Non-Impact Printing Technologies,** Society of Photographic Scientists and Engineers (Samuel W. Ing, Xerox Corp., 800 Phillips Rd., Webster, N. Y. 14580), Fairmont Hotel, San Francisco, Aug. 24-28.

**International Symposium on Electromagnetic Theory and 8th Colloquium on Communication,** International Union of Radio Science and the Hungarian Academy of Sciences (Research Institute for Telecommunication, 1525 Budapest 114, POB 15, Hungary), Research Institute for Telecommunication, Budapest, Aug. 25-29.

**8th Quartz Devices Conference and Exhibition,** Electronic Industries Association (2001 Eye St., N. W., Washington, D. C. 20006), Westin Crown Center, Kansas City, Kan., Aug. 26-28.

**Interconnect '86,** United States Telecommunications Suppliers Association (333 N. Michigan Ave., Suite 1618, Chicago, Ill. 60601), San Mateo Expo Center, San Mateo, Calif., Aug. 26-28.

**IFIP Congress '86:** International Federation for Information Processing (Philip H. Dorn, Dorn Computer Consultants Inc., 25 E. 86th St., New York, N. Y. 10028), Trinity College, Dublin, Ireland, Sept. 1-5.

# SIEMENS

## Subject: innovative LED text display

# ...with underlining too

Headlines, titles, bold face – in printing it's a fairly simple matter to give aids for orientation, to differentiate, to emphasize and focus attention.
Quite different to LED text displays. They haven't been too versatile on these points. Until now, that is.

Because here comes the **8-character intelligent PD-2816 LED display for 64 characters in ASCII code with programmable features:**

- underlining of any characters or the entire readout
- simultaneous blinking and underline
- display dimming (25, 50 or 100 %)
- blanking of the display without loss of memory content
- lamp-segment test at half intensity without memory loss.

The high-intensity red characters are 4.1 mm high and magnified by lenses. The eight text positions are driven in ASCII.

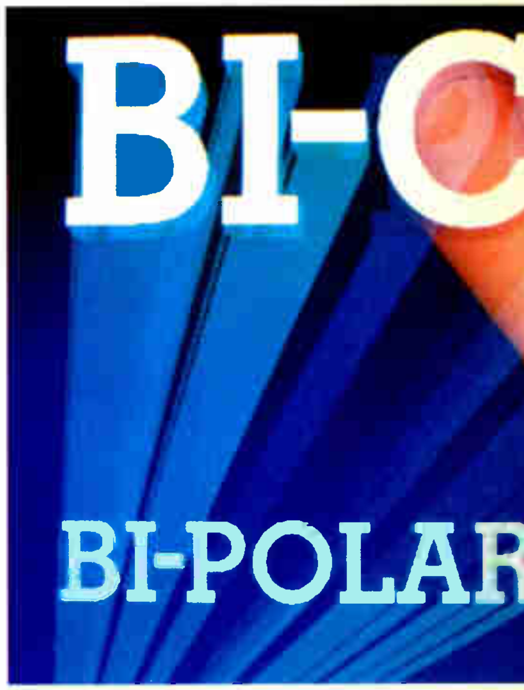
The entire control logic is integrated into one CMOS circuit, containing the character-generator ROM, the display multiplexer, the timing logic plus the LED driver. PD-2816 devices are furthermore easily cascaded in steps of eight to form any number of character places.

Send for a data sheet and find out more. Just write to Siemens AG, Infoservice 12/1103, Postfach 156, D-8510 Fürth, quoting "programmable LED displays".

12/1103.101

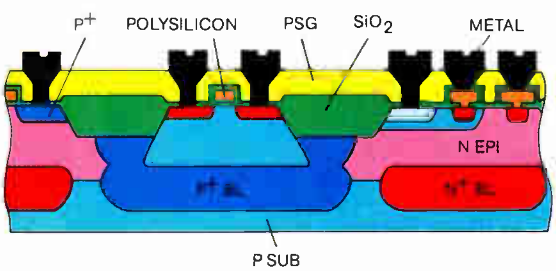
Circle 80 on reader service card

# Leading BI-CMOS



NEC's revolutionary BI-CMOS Gate Array puts an end to compromise solutions. NEC have combined the two major gate array technologies to give you the best of both worlds: the high speed and driving capability of bipolar arrays and the low power consumption associated with CMOS technology.

High speed is a standard feature with up to 160 MHz operation, 0.45 ns internal gate propagation delay time (fan out of 1) and power dissipation per internal gate of only 18 μW/MHz. The gate array family consists of four masters with gate counts between 623 and 3140 and up to 140 I/O buffers with a maximum of 24 mA sink capability per output.

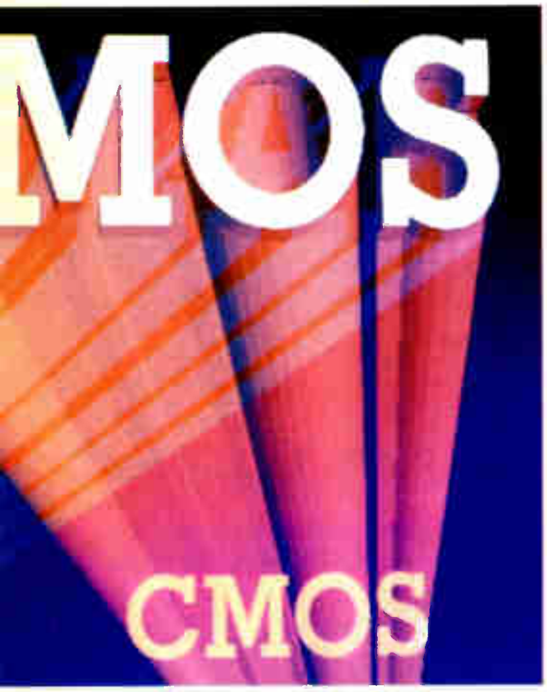



A new process technology specially developed for the BI-CMOS Gate Array production uses a high resistivity epitaxial layer combined with n- and p-type buried layers to eliminate the latch-up effect.

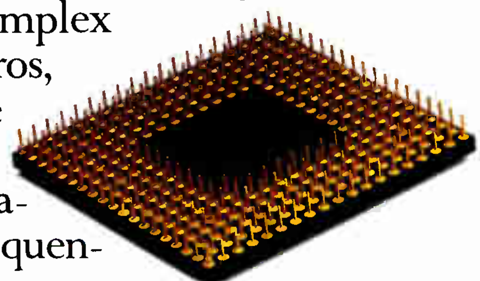
NEC's new BI-CMOS Gate Array family is the latest in a long tradition of high performance ASICs that include 1.5 μ CMOS gate arrays

# the field

# Gate Arrays




with packing densities of up to 20,000 gates, standard cell ICs with the provision of highly complex on-chip megamacros, and super-fast gate arrays in ECL technology for gigahertz operating frequencies. NEC's gate arrays are backed up by professional design centres throughout Europe working with sophisticated hardware and software systems to ensure fast and trouble-free design implementation. NEC fully supports Daisy Systems, Valid, Mentor, and Micad engineering workstations and utilizes simulation and software tools such as Hilo, Silvar Lisco and Future Net.



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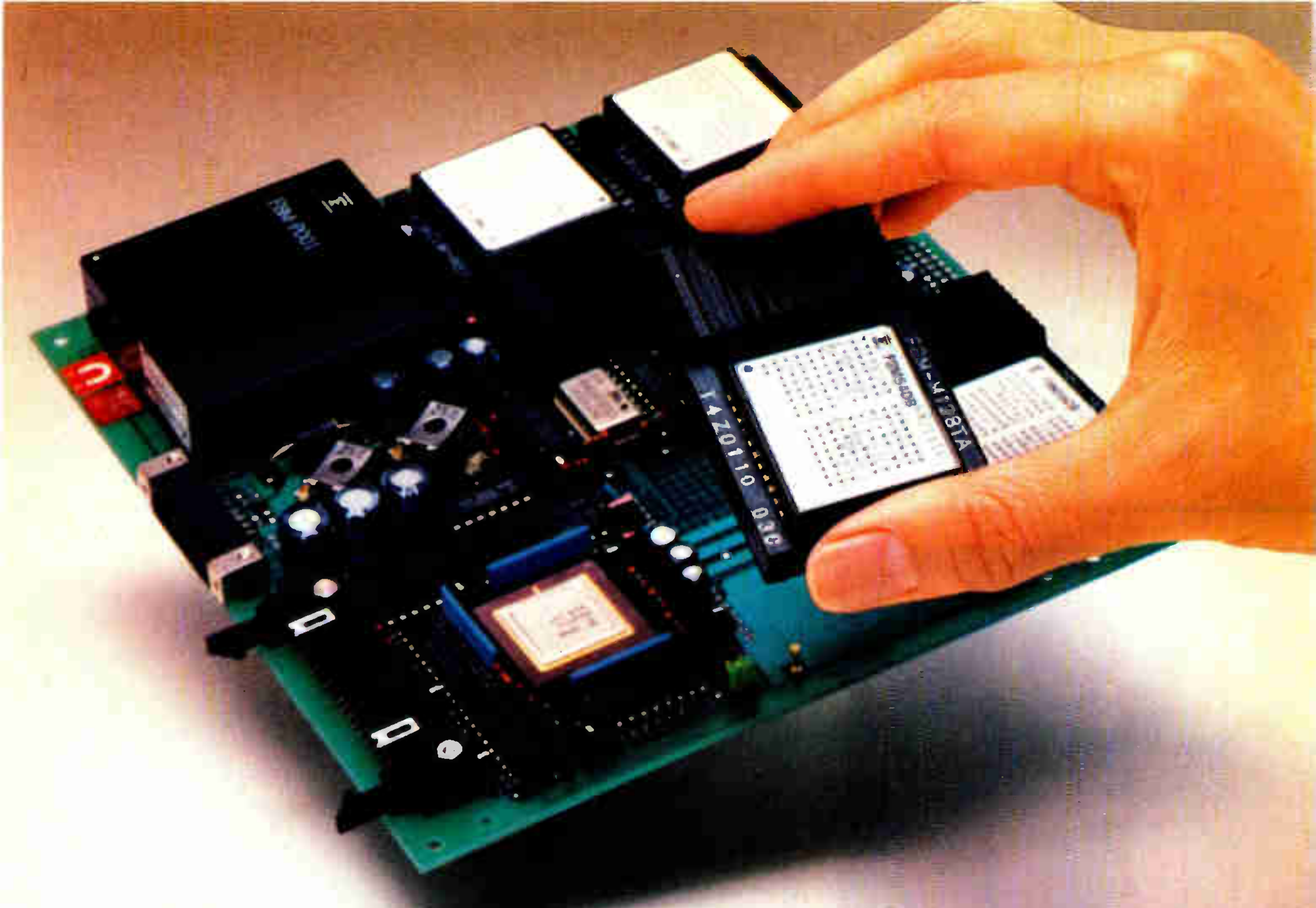
**NEC**

Circle 81 on reader service card



# *Now, take design work into your own hands.*

Fujitsu's BMM Series bubble memory modules: FBM-M128 TA/TC let you design boards just the way you want them. Each module consists of a bubble memory device and peripheral linear ICs. Operation is performed at the TTL level, so simply by adding control LSIs you can now create solid-state file memories tailored to your exact needs.

- Bubble memory devices and peripheral linear ICs mounted on same package, usable just like ICs
- TTL level I/O, enabling easy board design by the user
- Mixed mounting of RAMs, CPUs, etc. possible
- Memory capacity easily expandable (from 128KB to 4MB)
- High-density mounting possible
- Fast access time (12.5ms)
- Low cost achieved by mass production technology

***Fujitsu BMM Series bubble memory modules are offered as a kit containing the following components:***


1. Controller: MB60702 (64-pin RIT, CMOS) 2. Sequencer: MBL6801/W2 (40-pin, DIP-NMOS) 3. Timing generator: MB14506 (22-pin DIP, LS-TTL) 4. Voltage detector: DV-1451 (8-pin SIP, HYB-IC) RD2.7EB1 (Zenor diode)

***Power supply module:*** *The optional FBM-P001 power supply module permits dramatic simplification in circuit design by reducing the number of requisite power supplies from four to one (+5VDC).*

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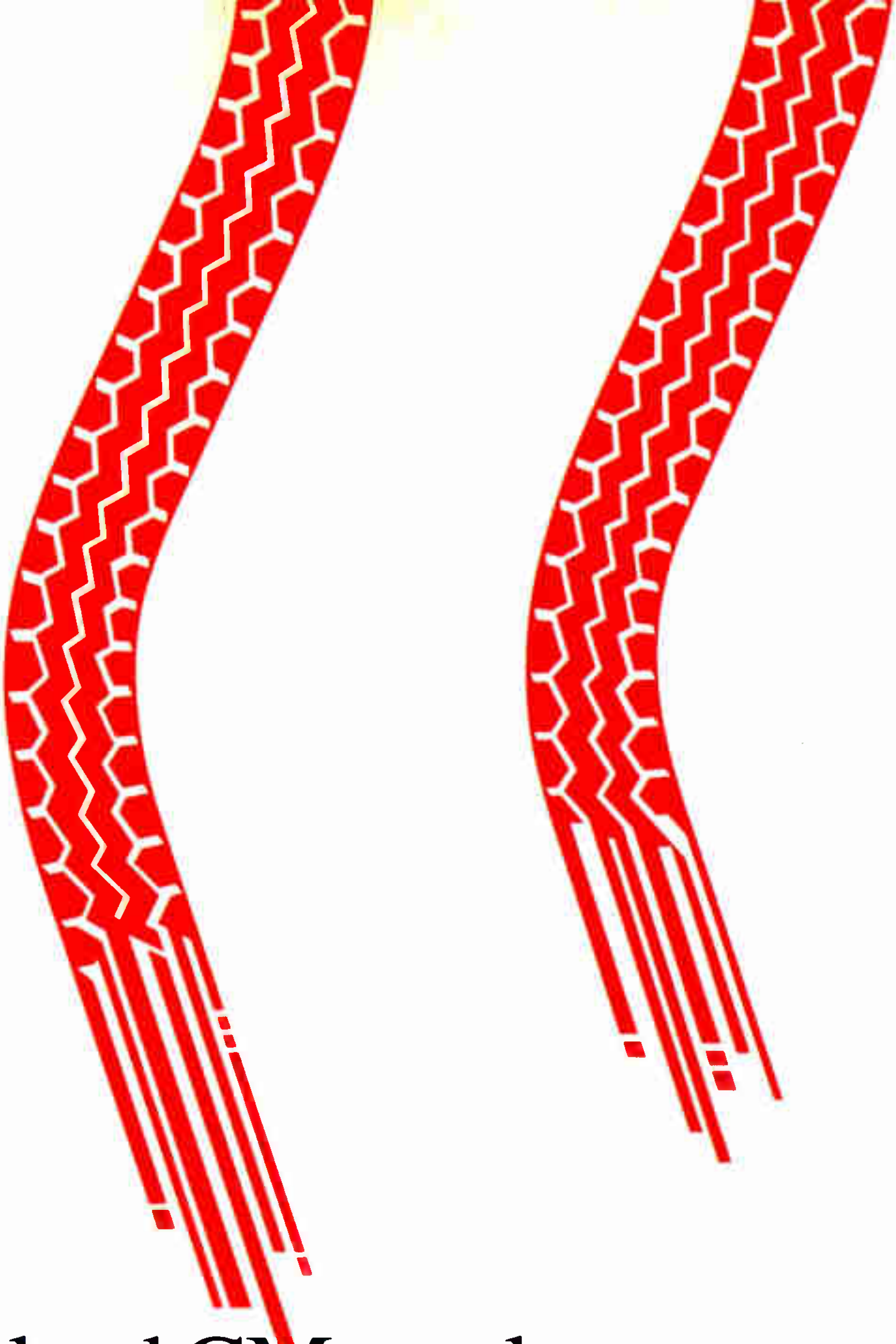
Circle 82 on reader service card



# We helped GM accelerate.

**W***e can do the same for you.*

General Motors started breaking ground on its $500 million truck assembly plant in Fort Wayne just two months after choosing the new location.

That's how geared up we are for new business. And that's why we offer creative financial and development incentives to assist business. With state support programs for investment capital. Infrastructure improvement. Tax incentives. Job training. Research and development assistance.

We also have all the resources that make a favorable business climate. One of the highest work ethics in the nation. High standards of living. Low taxes.

We could go on and on. With even more reasons why the Big Three — GM, Ford and Chrysler — have invested over three billion dollars in Indiana in the last three years alone.

If you're ready to get rolling, we can help you get started.

**Call 317-232-8888.**

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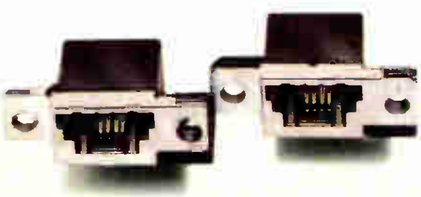

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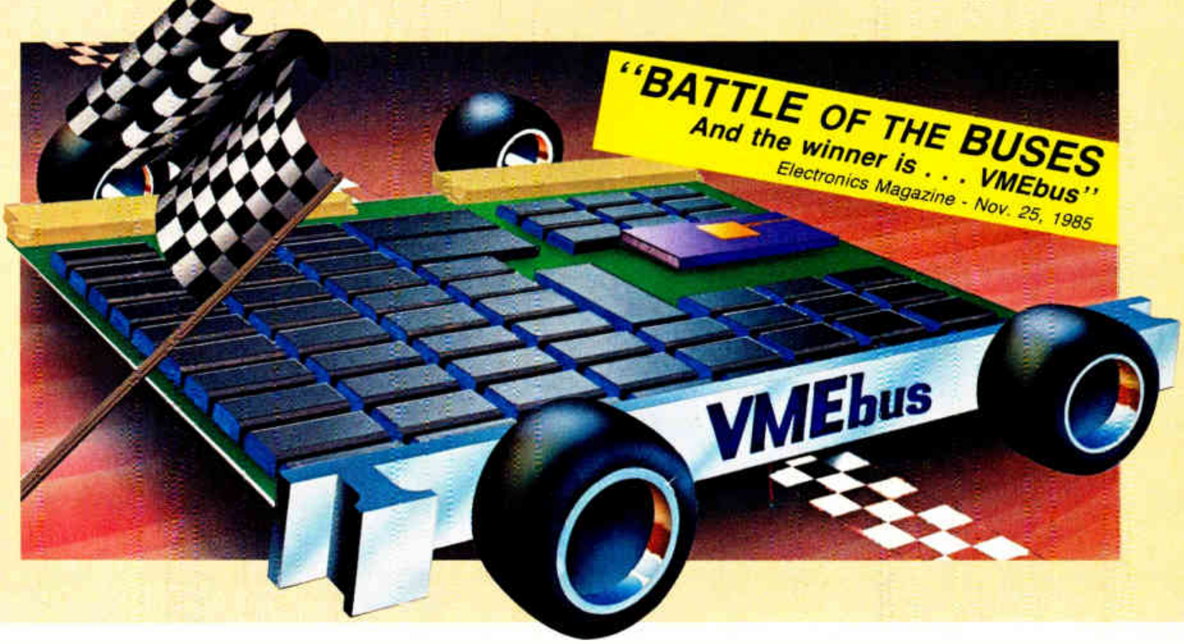


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# TECHNOLOGY NEWSLETTER

## SOFTWARE CAN QUICKLY SHIFT ASIC DESIGN TO ANOTHER LOGIC FAMILY

Designers who feel most comfortable using CMOS logic packages for prototyping new hardware can now have Hitachi Ltd. convert their designs into another logic family for incorporation into application-specific integrated circuits. The job takes just a day or two. It would normally take a designer with five years' experience about 30 days. The Japanese company's swift conversion comes from a computer-aided-design package developed at its Systems Development Laboratory in Kawasaki. The program, which is written in Hitachi's Language Oriented Language Inferencer logic-programming language, runs on the company's IBM-compatible mainframes. Hitachi has used it to translate CMOS digital circuits into integrated-injection logic for ASICs that combine digital and analog processing—its lowest-cost product for consumer applications. But by changing rules in its knowledge base, the same program could be used for translation between other logic families. ☐

## IBM AND HITACHI ADD NEW SPIN TO DISK DRIVES AT NCC

IBM Corp. hasn't said a word officially, but industry watchers think that the Armonk, N. Y., company will introduce a brand new Winchester disk drive at the National Computer Conference in Las Vegas this week. The word is that the drive, whose platter diameter is unknown, will not be an upgrade of IBM's top-of-the-line 3380 disk drive and could mark a shift to a standard interface. It will boast new technology that will make it competitive in cost per megabyte and quite high in capacity. Also at NCC, Hitachi will show the DK815-10, a unit that pushes the capacity of an under-14-in. drive over the 1-gigabyte mark. The $14,700 8.8-in. disk drive boasts 1,050 megabytes of unformatted capacity, twice that of the company's current high-end model. ☐

## BROOKHAVEN PUSHES HARDER FOR NATIONAL X-RAY LITHOGRAPHY EFFORT

Momentum will build this summer in the Brookhaven National Laboratory's drive to launch a government-industry X-ray lithography program using a synchrotron storage ring. Following up on its initial workshop to size up prospects for a project [*Electronics,* March 24, 1986, p. 18], Brookhaven has scheduled a second meeting for July 21, aimed at producing design options for a system. Attendees will be machine physicists and industrial executives; they'll address the choice between superconducting versus conventional magnets on the storage ring coils. A third workshop, attended primarily by design engineers, will be convened soon after, perhaps in August. Its mission will be to take the designs that emerge from the July workshop and produce a proposal incorporating detailed schedules, cost estimates, special resource requirements, and critical paths. The goal is a working plan to present to government and industry. ☐

## NEC TO INTRODUCE SUPERMINI WITH DUAL PROCESSORS

NEC Corp. has developed a superminicomputer, with performance similar to that of Digital Equipment Corp.'s MicroVAX, that's built around a custom CMOS processor with some 50,000 gates. It operates at 1.2 million instructions/s. NEC will also come out with a dual-processor model—a world first for a microprocessor-based superminicomputer, the Tokyo company maintains—with a speed of 2.2 mips. NEC offers a choice of its proprietary real-time operating system or one based on AT&T Bell Laboratories' Unix System V. Deliveries of the $40,000 single-processor MS4110 are scheduled to start this October, those of the $74,700 dual-processor MS4220 at the end of next April (a Unix coprocessor board costs an additional $6,000). NEC expects to export the machines. ☐

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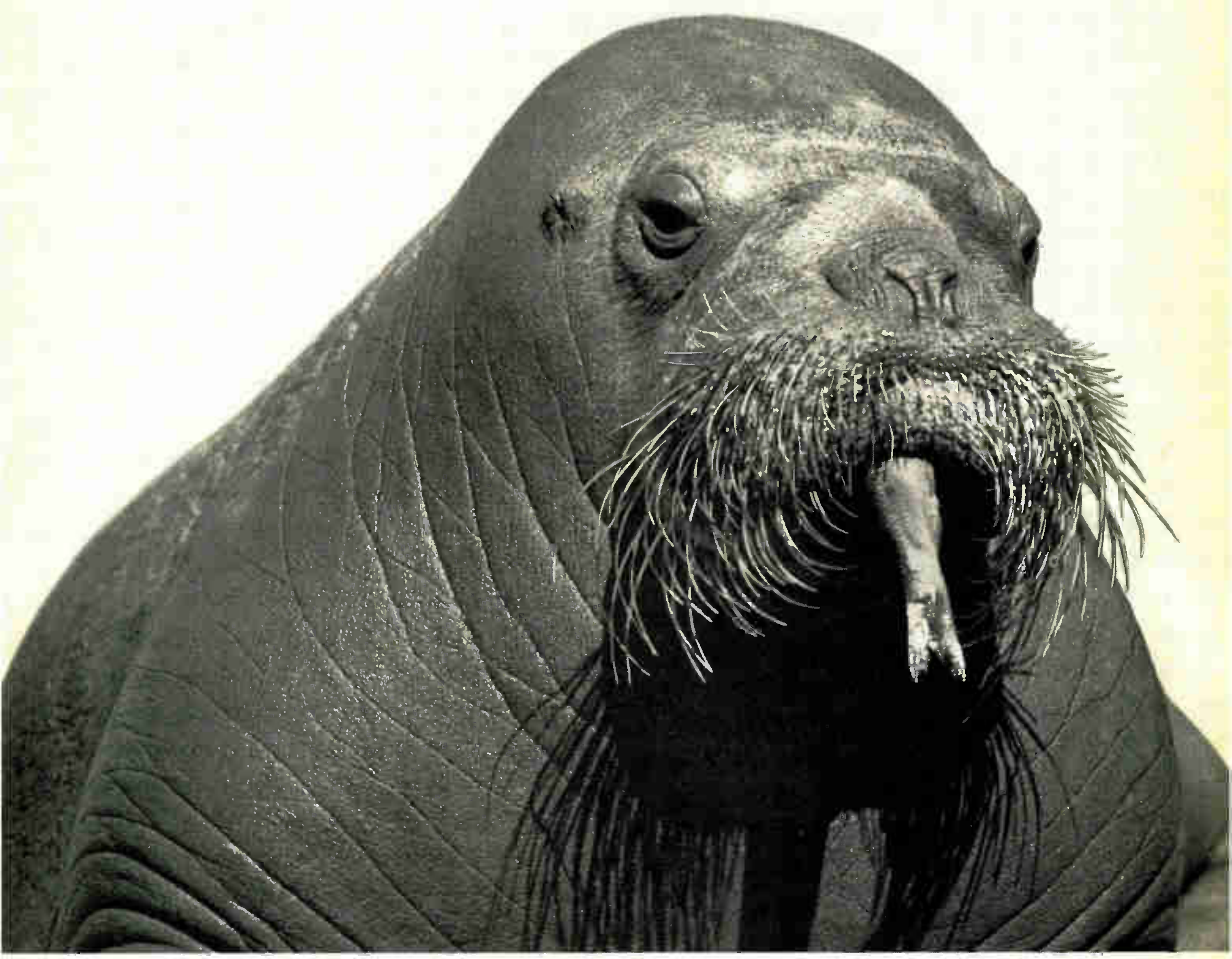

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# ELECTRONICS NEWSLETTER

## SEMICONDUCTOR BOOK-TO-BILL RATIO SLIPS IN MAY...

This summer could well turn into a new season of uneasiness for U.S. semiconductor makers. In May, for the first time in nine months, the book-to-bill ratio for the semiconductor industry eased as the three-month rolling average "flash figure" compiled by the Semiconductor Industry Association slipped to 1.10, a drop from the 1.17 ratio (revised from a flash figure of 1.15) reported in April. On the plus side, the decline was caused mainly by an increase in shipments; billings rose 7.4% over April to $741.8 million, while bookings edged down only 1.1% to $805.6 million. □

## ...AND PART OF THE PROBLEM MAY BE CONTINUING SOFTNESS IN COMPUTERS

The dip in the book-to-bill ratio figures to trigger reassessments of the outlook for the computer industry, which industry analysts earlier expected would begin to pick up during the second half and bring a lift to the semiconductor business. "The recovery was led by the distributors, but not followed by the computer industry, which is still in a slump," says Andrew Kessler, an analyst for PaineWebber, New York. "It looks as though the great 1986 recovery is turning into a great 1987 recovery. . . . I would not be surprised if the book-to-bill ratio went under 1.0."

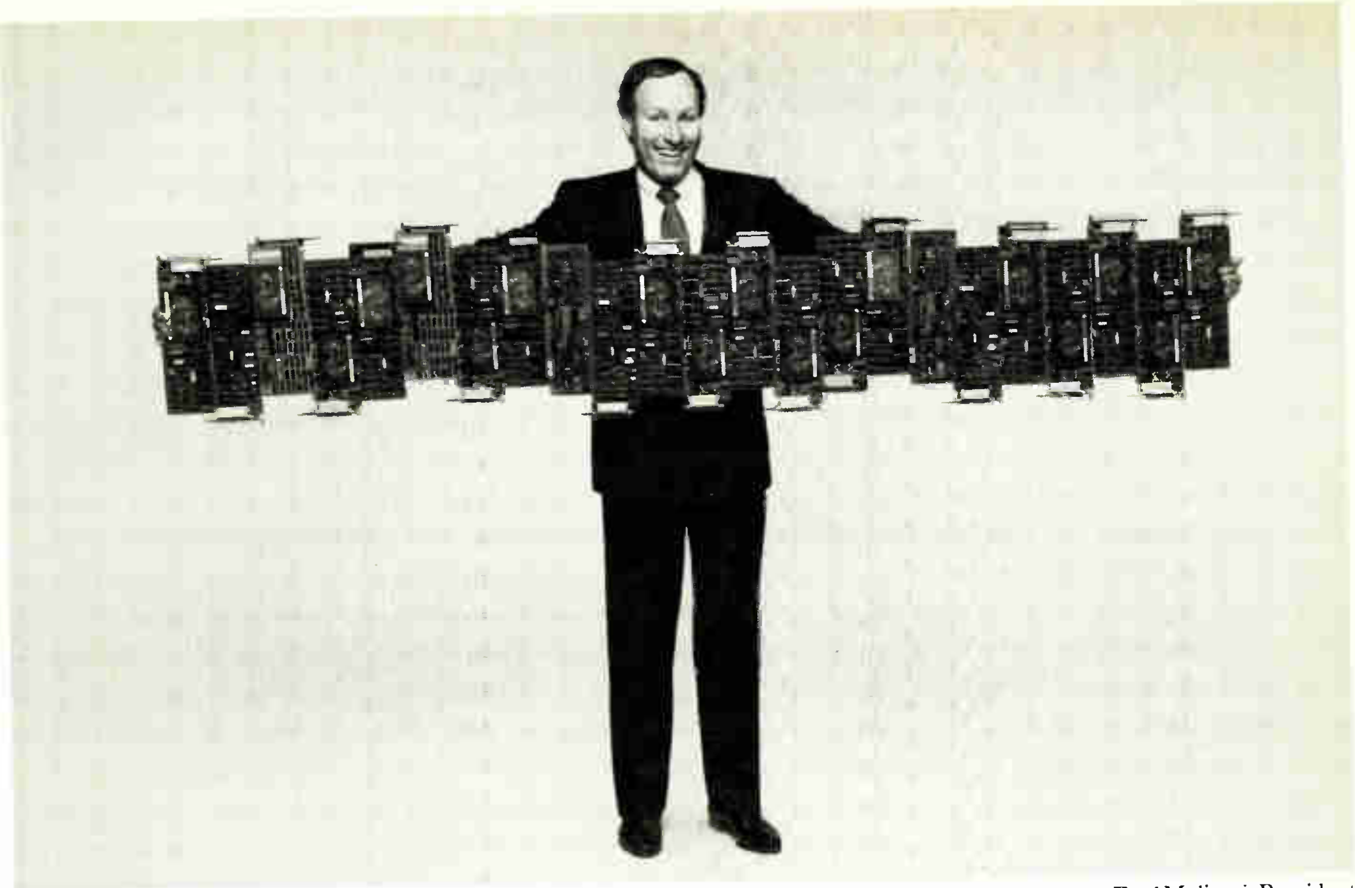
The industry's largest distributor, Hamilton-Avnet Electronics Inc., is reporting much softer bookings in May, with little improvement in sight. Even the Electronics Marketing Group of Wyle Laboratories Inc., generally among the most bullish forecasters, has lowered its sights. "Bookings have plateaued; we're looking for a flat summer," concedes Ralph L. Ozorkiewicz, president of the group. He does point out that bookings remain substantially above last year's depressed levels, however. Much the same view comes from Douglas Rankin, vice president for marketing at Signetics Corp., Sunnyvale, Calif. "The problem is that the EDP [electronic data processing] industry in the U.S. is very weak. It's looking as though it won't recover in the second half." □

## AT&T TO ADD NETWORK FEATURES TO UNIX

The 80,000 or so users of Unix operating systems around the world can expect good news from AT&T Co. at this week's National Computer Conference in Las Vegas. The company will add two powerful networking features to the operating system in Unix System V Release 3.0. The first of these is Streams, a feature invoked from the Unix shell that allows application software to be independent of the underlying network hardware. Programmers can select Streams modules that implement communication protocols such as Ethernet with no need to modify the application programs. The second of these, Remote File Sharing, allows transparent file sharing. A user can access files and data on remote computers in the network as if they were on the local machine. □

## EC MINISTERS REJECT $10 BILLION R&D PROPOSAL

Research and development executives in Western Europe will have to wait several months at least before they can get a fix on how much money the European Communities will lay out for R&D programs between 1987 and 1991. In early June, research ministers of the 12 member countries rejected the most recent research program proposed by the EC Commission as being too costly and too general. Aimed at providing a framework for all EC-sponsored research, the proposal called for a budget of some $10 billion to serve existing EC efforts in biotechnology, information technologies (Esprit), broadband communications (Race), and industrial technology (Brite), as well as a number of new programs. □



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# PRODUCTS NEWSLETTER

## 16-K AND 64-K CMOS STATIC RAM RACES HEAT UP

Thomson Components Mostek Corp. is taking an early speed lead in 16-K static RAMs organized as 4-K by 4 bits, while Lattice Semiconductor Corp. and Cypress Semiconductor Corp. are vying for top honors in the 64-K SRAM market. Mostek, Carrollton, Texas, is offering samples of its CMOS MK41H68 for $34.30 each in lots of 100, claiming it has the fastest access time—20 ns, 5 ns faster than Cypress's 4-K-by-4-bit CY7C171. Production begins this month. On the 64-K front, Lattice, Portland, Ore., has samples of a 35-ns part, the SR64K8, for $59, and Cypress, San Jose, Calif., says it will have samples of a 35-ns SRAM in the fourth quarter, priced at less than $100. Mostek is working on 16-K SRAMs that operate from 3.3 V and meet the new Jedec low-power standards. □

## FAST DATA-BASE SOFTWARE WORKS IN NETWORK ENVIRONMENTS

Sybase Inc. is set to launch data-base-management software for networked computers, and the Berkeley, Calif., company says its product works faster than dedicated data-base computers. Based on SQL, the system runs on off-the-shelf computing hardware and consists of the Dataserver, which maintains the data base, and the Data Workbench, a set of graphical tools that allows users to query the system. Dataserver runs on Sun-3 work stations from Sun Microsystems Inc. and performs more than 35 transactions/s, compared with 25 transactions/s for Britton-Lee Inc.'s dedicated computer. Data Workbench runs on either the Sun work stations or any bit-mapped terminal. Dataserver ranges from $18,000 to $90,000 and Data Workbench from $1,000 to $3,000. Delivery will begin in the third quarter. □

## SEEQ SHIPS FIRST 16-K-BY-8-BIT FLASH EEPROM

Seeq Technology Inc., San Jose, Calif., is first into production with a 16-K-by-8-bit flash EEPROM. Its 48128 QPROM aims at replacing the EPROM, which is difficult to reprogram, rather than the traditional two-transistor EEPROM. Available now, it sells for $6 apiece. For follow-on parts with higher densities, the two-transistor EEPROM cell will be replaced with a single-transistor cell that combines the hot-electron write mechanism used in EPROMs with the Fowler-Nordheim tunneling-based erase mechanism of EEPROMs. The tradeoff is in the number of write/erase cycles; at about 100 to 1,000, it falls between those of EPROMs (less than 100) and EEPROMs (1 million). Intel, Texas Instruments, and Toshiba are working on similar parts. □

## ZYMOS TO MARKET STANDARD CELL PERIPHERALS FOR 8086 PROCESSORS

Zymos Corp., bolstered by the resources of its new majority stockholder—the $7 billion Korean conglomerate Daewoo Corp.—will be expanding its standard-cell offerings. Over the next few months, the Sunnyvale, Calif., company will ship a range of supercells, mostly CMOS peripheral chips for systems based on 8086 microprocessors. Among the new additions: bus controllers, timers, and direct-memory-access controllers. □

## DYNAMIC RAM CARD BOOSTS VMEBUS SYSTEM PERFORMANCE 40%

A dynamic RAM board called Wait-Less can improve the performance of VMEbus-based computers by as much as 40%, claims Alcyon Corp., the developer. By synchronizing the memory with the computer's clock, the San Diego company has eliminated wait states in the memory, which stores 2 megabytes. Writing to memory takes 40 ns and reading takes 125 ns. Wait-Less is priced at $1,995 in single quantities. □

Electronics

# FLAT-PANEL DISPLAY BUILT THAT COULD COMPETE WITH CRTs

## FRENCH LAB USES SRI's COLD CATHODES TO REPLACE ELECTRON GUN

**GRENOBLE, FRANCE**

Serious competition may be in the offing for the cathode-ray tube as a high-quality color display. A team of French engineers has developed a new way to fabricate tiny field-emission cathodes atop a glass substrate for a type of vacuum-tube flat-panel display that eliminates two of the CRT's principal drawbacks: large size and high voltage requirements.

Developers at the Laboratoire d'Electronique et de Technologie de l'Informatique (LETI) in Grenoble call the new screen a microtips fluorescent display. LETI uses the same kind of conical cathode structure that is called a Spindt cathode at SRI International, Menlo Park, Calif., where it was first developed by researcher C. A. Spindt (see p. 19). SRI builds the cathodes on silicon rather than on a glass substrate.

SRI International has several active projects using these field-emission cathodes in different types of devices. One of the projects aims to develop a color flat-panel display within about two years. But LETI, which maintains an informal relationship with SRI, has pushed ahead with work on displays and has built working monochrome prototypes.

Such displays use the low-voltage field-effect electron emission of an array of microtips to replace the electron gun of a CRT. Electrons from the microtips stimulate luminous anode phosphors on the inside of a front glass plate, which in turn emit light.

This arrangement far outperforms flat-panel vacuum-fluorescent displays, says Guy Labrunie, manager of the LETI's input/output components laboratory. Vacuum-fluorescent displays depend on complex internal filament arrangements, thus making full-color high-definition displays impractical.

The idea of using microtips to produce low-voltage field-effect electron emission is about 20 years old, Labrunie points out, but fabrication techniques have not been available until quite recently [*Electronics*, Dec. 16, 1985, p. 26]. The principal thrust of LETI's work was to take current field-emission-cathode technology, which is based on a monocrystalline silicon substrate, and transfer it to a glass substrate to decrease the cost for high-volume use while increasing the potential display size.

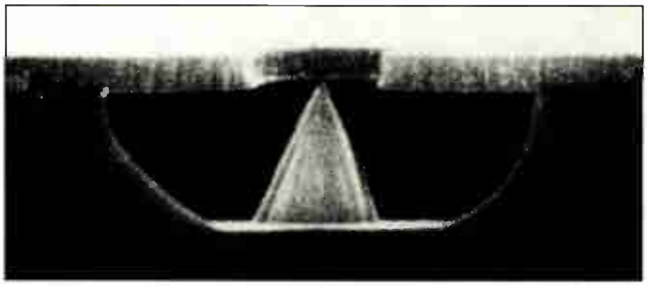
Fabrication begins with a glass substrate on which chemical-vapor deposition places a thin film of silicon. On the silicon is laid a series of parallel nickel lines, which correspond to the display matrix's lines and function as the cathode connections. The microtips are later deposited on the nickel lines. After a silicon dioxide insulating layer is grown on the entire surface, niobium gate (or, in tube parlance, grid) columns are deposited.

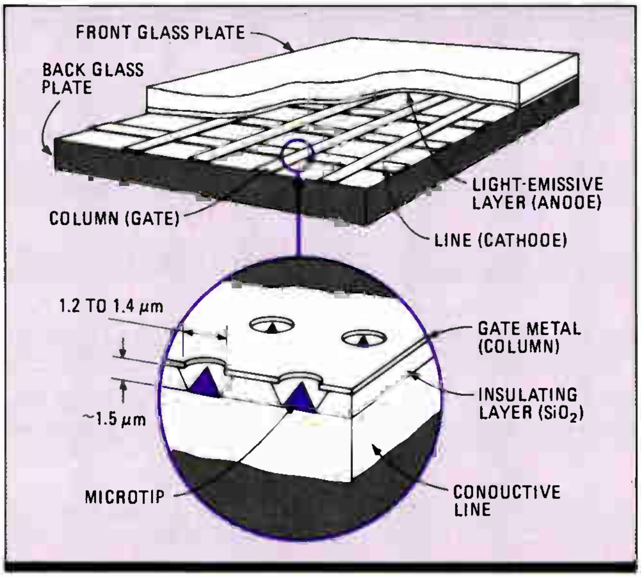
At the intersection of the cathode lines and gate columns, holes 1.2 to 1.4 µm across are etched in the gate metal, and the oxide underneath the holes is etched down to the nickel. The hollowed-out oxide leaves an empty bowl-shaped space about 1.5 µm deep in which the microtip is formed by vacuum deposition. A phosphor anode layer is deposited on the front glass plate, and the two glass layers are sandwiched together with a vacuum between them.

The process requires only one critical masking step—the etching of the holes in the gate metal. Also, the yield of the structures can be far from perfect without a significant loss of picture quality, because there are about 1,000 microtips behind each pixel.

With a peak operating current density of 1 mA/mm², a 1,000-line display would require an operating anode voltage of some 80 V. But the voltage that must be switched to turn pixels on and off—the voltage between the cathode and the gate—is no more than 40 V. Labrunie expects commercial flat-panel drive circuits that can switch 35 V to appear as early as this year; so 40-V chips should not be far off.

So far, LETI has produced small flat panels 1 cm thick using zinc oxide/zinc (green) phosphors. With anode voltages in the range of 50 to 200 V, they exhibit luminous efficiencies of 1 to 10 lm/W, a figure that Labrunie says is superior to that of any other emissive flat-panel display. Full-color operation can be added by using zinc, cadmium, and sulfur-based red, green, and blue phosphors, he says. *–Robert T. Gallagher*






**CROSSROADS.** Where cathode lines and gate columns cross in LETI's display, some 1,000 tiny field-emission cathodes congregate.

# SRI HAS HOT PLANS FOR ITS COLD CATHODES

**MENLO PARK, CALIF.**

The "microtips" being used to build a flat-panel display by French researchers at the Laboratoire d'Electronique et de Technologie de l'Informatique in Grenoble, France, were developed at SRI International, Menlo Park. The California research organization is also working hard now to adapt them for a display, as well as for several other applications.

The technology can be used "anywhere you want electrons," says senior SRI researcher C. A. "Capp" Spindt, who has worked on the field-emission-cathode array technology at SRI since 1968. It's particularly useful where high current densities are needed, Spindt says. "We have produced several hundred amperes per square centimeter from our cathode."

SRI, which calls the tiny structures Spindt cathodes, is now working on electron-microscope and mass-spectrometer applications, as well as a free-electron laser. A mass spectrometer has actually been built with the cold-cathode devices by a group at the University of Arizona and East Germany's Max Planck Institute. Intended for the U.S. Galileo probe of Halley's comet, it ultimately flew on two Soviet Vega probes when Galileo was scrubbed.

**TUBE ICs?** So far as Spindt knows, this was the first operational use of the cathode arrays. A number of other applications, both proprietary and military, are reportedly close to fruition at SRI. Work on another intriguing application, considered possible for years, has recently been revived: integrated circuits built from tiny 1-$\mu$m vacuum tubes.

"Solid-state circuits are limited by the speed of electrons in solid materials," Spindt explains. "In a vacuum, the speed is higher by an order of magnitude." The French learned of the technology in an SRI paper, Spindt says, and immediately saw it as a natural vehicle for flat displays. "We had noticed that, too, but were busy with other applications," says Spindt. "They have done a very good job in building the prototype. They have shown that the technology does work."

Now, however, SRI itself is working on putting the arrays into a flat display, in an effort funded by Boeing Corp. The program calls for development of a 6.75-by-6.75-in. screen less than 1 cm thick. The screen will have a bit-mapped color display of 675 by 675 pixels, says Spindt. LETI's prototype is monochrome and can display 32 lines of 32 alphanumeric characters.

However, Spindt says, SRI has been working on the display application for just a couple of months. "We'd like to see something working in a year and a half or two years," he adds.

SRI has fabricated an array of 100,000 cathodes in an area 1 mm in diameter. In principle, Spindt says, putting the cathodes into a working device is a straightforward engineering activity. Control electronics, he says, are similar to those used in plasma displays.

Spindt says the SRI panel will be as bright as or even brighter than a conventional cathode-ray-tube display, but with substantially lower beam currents and switching voltages. Cold-cathode tubes may use up to 25% less energy than a comparable thermionic electrode device, he calculates.

Even at that level, the devices still may not be ready for commercial applications, says Joseph A. Castellano, publisher of *Electronic Display World*, an industry newsletter.

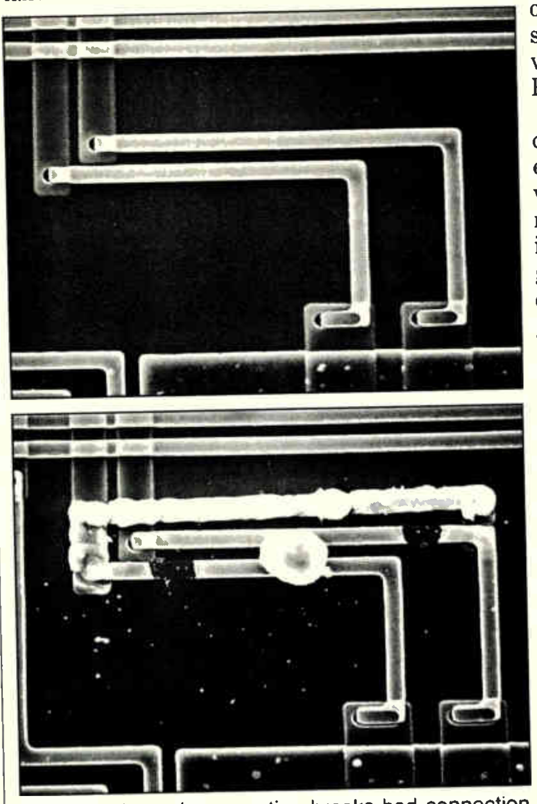
"Active displays all have the same problem: If you drive an X-Y matrix, you still need a large number of high-voltage row and column drivers, and they are not cheap." Castellano adds, however, that the devices may find favor in the military, where price is not such a consideration, and that the prices of drivers will drop as more suppliers enter the field. *–Clifford Barney*

***INTEGRATED CIRCUITS***

# CUT-AND-PATCH LASERS SPEED CHIP REPAIRS

**ALBUQUERQUE, N. M.**

A recurring headache for integrated-circuit designers is prototypes that don't work because of faults in the aluminum interconnection lines. Such defects can put projects behind schedule and run up their costs; often, redoing masks and repeating fabrication can take weeks of corrective work.



**FAST FIX.** Laser/gas reaction breaks bad connection (top); a second reaction deposits conductive material.

But a remedy for this particular headache has now come to hand. Sandia National Laboratories has devised a speedy method of on-chip repair that uses low-power lasers to cut and patch the metal lines. With the Albuquerque lab's cut-and-patch technique, small quantities of chips can be analyzed and fixed, and the design verified in a day, assuming that only a few repairs are needed, says A. Wayne Johnson, supervisor of the Laser & Atomic Physics Division.

"After determining where the conducting line should be routed, we simply remove the part we don't want by carefully directing pulsating laser light onto it in the presence of a reaction gas," he explains. Another type of laser and a different reaction gas are used to rewire the circuit. The entire procedure takes minutes.

Although repair by laser seems straightforward at first glance, simply blasting the metal interconnection lines with a laser would risk damage to adjacent and underlying regions of the chip, Sandia researchers say. So Johnson's division spent 18 months developing its technique, which has been proven out on prototype chips Sandia fabricated with 3-$\mu$m geometries.

Emergence of the Sandia development comes at an opportune time for designers of advanced ICs, observes semiconductor process consultant William I. Strauss of Forward Concepts Inc., Tempe, Ariz. "The reason is bigger dice and VHSIC-size chips as large as 400 mils on a side," says Strauss, referring to parts produced under the Defense Department's Very High Speed Integrated Circuits program. The prototypes are very costly, built in small quantities, and each one is important. "Any chips you can salvage, so much the better. It's an inexpensive way to repair them."

**CHAMBER-MADE.** The cut-and-patch process is relatively simple, with both steps taking place in a small vacuum reaction chamber that holds silicon wafers. In the cutting step, which uses a krypton-fluoride laser, chlorine gas fills the chamber. The laser is aimed through a quartz window with a microscope and computer-aided positioner, then pulsed between 20 and 30 times a second. Each pulse delivers about 0.1 J of energy per square centimeter.

Pulsed by the laser, the aluminum line heats and cracks the oxide coating (about 20 Å thick). The exposed aluminum and the chlorine spontaneously react to form aluminum chloride, a volatile vapor that is pumped out of the chamber. Cutting occurs only where the laser hits the aluminum, and the underlying silicon dioxide insulating layer is left.

For line patching, the Sandia approach uses a continuous-wave ultraviolet argon ion laser operated up to 0.4 W, and the chamber is filled with a mixture of diborane and silane gases. On the wafer, the laser traces and heats a path over the insulating layer. When the path reaches 700°C to 800°C, the two gases decompose and deposit conducting polysilicon on it. For test chips, this type of line is an adequate conductor.

*'It's an inexpensive way to repair costly VHSIC chips'*

This deposition technique is similar to processes done elsewhere, says Sandia. At Massachusetts Institute of Technology's Lincoln Laboratory, for example, researchers are working with tungsten deposition on poly for commercial circuits because it is a better conductor [*Electronics*, June 9, 1986, p. 15]. This process also was developed at Sandia.

In its initial application at Sandia, the repair technique quickly fixed prototype random-access-memory chips implemented in n-MOS, which did not work because of reversed control lines, says Raymond E. Bair, manager of the IC Design Department. "It already has proven its worth to us," he adds. To fix the chips otherwise, Sandia would have had to go outside for new mask sets.

Sandia researchers expect their cut-and-patch technique will also lead to more flexible design of redundant memories, which have auxiliary transistors and conducting lines. In addition, it could reduce time needed to evaluate gate-array chips, which are fabricated to about 70% completion. Final wiring on test gate arrays could be done more quickly with laser-assisted conductor writing.

Work will continue on the Sandia technique, which, with further refinements, has the capability to handle submicron line sizes. But whether it is suitable for production ICs remains unclear, although the hardware itself doubtless could be improved with better computer-controlled gear. *–Larry Waller*

*MICROPROCESSORS*

# 32-BIT BUILDING BLOCKS CATCH FIRE

**SAN ANTONIO, TEXAS**

Billowing demand for the microprogrammable building-block chips used to construct sizzling new 32-bit processors is turning a nice little niche business into a steamy market. This arena appears destined to become a magnet for some of the most advanced CMOS and bipolar technologies as well as a proving ground for new processor architectures.

The latest to complete a 32-bit-processor building-block set is Advanced Micro Devices Inc., Sunnyvale, Calif., which this week officially rolls out a 32-bit arithmetic logic unit produced at its most advanced bipolar fabrication lines in San Antonio. But Analog Devices, Fairchild Semiconductor, Texas Instruments, Weitek, and others are already positioning building blocks to serve a new batch of 32-bit applications, including reduced-instruction-set computers and parallel processors, that most conventional single-chip microprocessors can't handle.

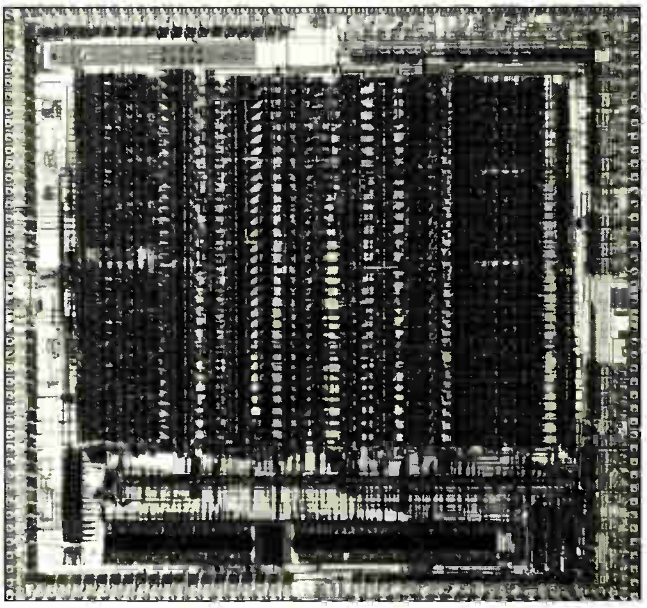
The Am29300 family will be as vital to AMD's next 10 years as the bit-slice 2901 processor has been during the last 10, says John East, vice president and head of the General Logic Group. Unlike the 4-bit 2901 family, the new building blocks have a fixed 32-bit width.

Since the middle 1970s, the company's 2901 processor has become the bit-slice workhorse for applications where fixed-instruction-set microprocessors fell short. "People never really wanted to use bit-slice processors, but bit-slice was the only flexible way of achieving high speeds," notes East.

"Now a similar set of decisions will be made when it comes to 32-bit microprogrammable building blocks," he adds. "Just as in 1975, those that can use single-chip 32-bit fixed-instruction-set processors will use them, and those that can't will beat a path to our door."

That trade will probably come from work-station vendors who see the building blocks as a good way to differentiate themselves from the competition. Small firms, however, are still likely to use standard microprocessors because of the time it takes to design processors with separate ALUs, sequencers, and other building blocks.

"The traditional single-chip, fixed-instruction-set microprocessors—like Motorola's 68020, Intel's 80386, and National Semiconductor's 32032—are continuing on their own growth path," says Will Strauss, president of Forward Concepts Co., a Tempe, Ariz., consulting firm. "But the systems companies now wish to have an advantage over the



**BLOCKED OUT.** AMD completes its set of bipolar 32-bit-processor building blocks with the unveiling of its Am29332 arithmetic logic unit.

guy down the street. Assuming one company is smarter than the other, these building blocks can be used to achieve a proprietary advantage."

The competition for market share will pit some of the industry's fastest CMOS processes against new oxide-isolated bipolar technologies and emitter-coupled logic. But most market observers agree the design hurdles won't be enough to keep microprogrammable chip sets down. Sales of processor building blocks will climb from $217 million in 1986 to $700 million in 1990, estimates Gnostic Concepts Inc., San Mateo, Calif.

"This market started out as a niche, and now it is exploding primarily because of the growth in new computer markets, such as superminis, supercomputers, high-performance work stations, and graphics," notes John F. Rizzo, marketing vice president at Weitek Corp. The Sunnyvale company has been shipping 16-, 32-, and now 64-bit chips for processors to the likes of Alliant Computer Systems, Apollo Computer, Floating Point Systems, and Sun Microsystems. Weitek, which has its ICs fabricated by several CMOS foundries, has 50 engineers and technologists focusing on floating-point processors.

**EXACT SOLUTIONS.** "Weitek's approach is to offer exact solutions to applications. Once you get into the market, you find each application requires something different in architecture and functionality," says Rizzo. Weitek now has three 32-bit and two 64-bit families.

Texas Instruments Inc., which last fall disclosed its intention to enter the market with a 32-bit AS748832 family, aims to quickly lower prices along volume-manufacturing learning curves in hopes of opening up new applications for building blocks, says Bob Bailey, strategic marketing manager for logic in Dallas. TI has made available its first part, the 8838 barrel shifter, and has working silicon on the 8832, a 208-pin, 180,000-mil$^2$ ALU chip.

TI's ALU is built with the company's 1.5-$\mu$m Impact-X bipolar technology [*Electronics*, Dec. 23, 1985, p. 45], as are the family's funnel shifter, barrel shifter, register file, microsequencer, and shuffle exchanger. A floating-point processor and 32-bit multiplier-accumulator will be made in 1-$\mu$m CMOS.

The eight-chip set will boast 50-ns cycle times and include double-precision floating-point capability. TI is paying particular attention to the emerging parallel-processing market and has incorporated a subinstruction set on the 8832 for single-instruction-stream, multiple-data-stream architectures.

"The building-block market has been constrained by the lack of suppliers and design tools," says Bailey. "Now we are seeing more suppliers enter the market. New design tools have really helped, with the likes of Step Engineering and Hewlett-Packard supporting these microprogrammable products."

AMD is counting on its early jump in the market to beat out TI for design wins. "I am most worried about TI, not because I think they are going to beat us but because TI is a tough competitor," states East. "However, we have been sampling chips for nearly a year."

AMD is also counting on higher levels of integration to counter TI's 50-ns family. The AMD parts' cycle is 80 ns, but the new 168-pin 32-bit Am29332 ALU performs more functions than TI's 8832. The 29332 has a funnel shifter, a barrel shifter, and an encoder, so it can do more in a cycle, says East. It is available now for $495 in 100-piece lots.

The ALU joins a 32-bit multiprecision parallel multiplier, a 32-bit single-precision floating-point processor, a 16-bit interruptible microsequencer, and a dual-access four-port register file. AMD also intends to bring out two other building-block families, one built with ECL and featuring cycle times of 50 to 60 ns, and a CMOS set with 100-ns cycle times but using less power. *–J. Robert Lineback*

**DESIGN AUTOMATION**

# NEW SIMULATION ENGINES TAKE AIM AT ZYCAD

**ST. PAUL, MINN.**

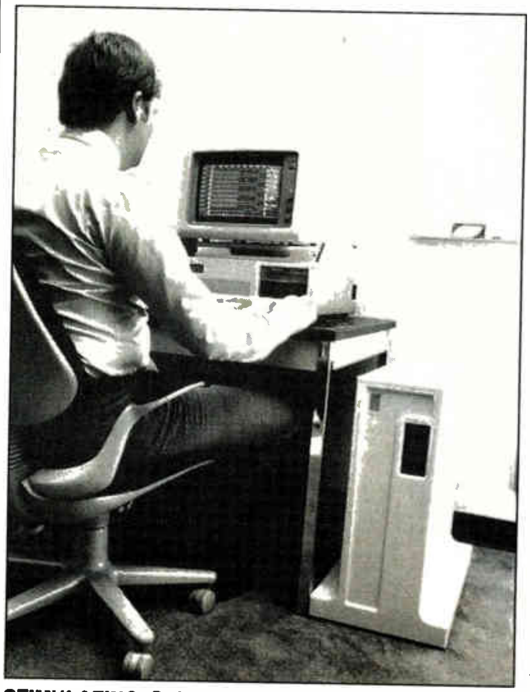
Competition is getting stiff in the market for hardware accelerators for logic and fault simulation. Despite the downturn in sales of computer-aided-engineering equipment, those attending the Design Automation Conference in Las Vegas later this month will see at least three companies roll out systems that take dead aim at the embattled industry leader, Zycad Corp. of St. Paul. Two startup companies will unveil products and another competitor, Silicon Solutions Corp.—which Zycad is suing for patent infringement over products introduced at last year's show—will also introduce an accelerator product.

At stake is a market for application-specific CAE hardware that could total $530 million by 1990, up from $83 million this year, according to projections by Technology Research Group Inc., a Boston market researcher. With sales of $26.7 million last year, five-year-old Zycad held about a 45% share of last year's $60 million market for CAE hardware accelerators. But the company has been hit hard lately by slumping CAE sales, and its new competitors claim to offer performance equivalent to Zycad's for a fraction of the price. The startups also say their products are easier to use and have more features than Zycad's Logic Evaluator and Fault Evaluator.

At the show, a year-old Minneapolis company known as Xcellerated Computer Aided Technology Inc. will introduce a line of hardware-specific logic and fault accelerators that will feature simulation at up to 2 million events/s on as many as 64,000 modeling elements. At $120,000, XCAT's high-end MX-100 will equal the performance of Zycad systems that sell for about five times as much, says Richard P. Davenport, vice president of sales and marketing.

IKOS Systems Inc., a 20-month-old Sunnyvale, Calif., company, claims it has an even better deal. For $70,000, its IKOS 800 system will simulate logic at up to 2 million events/s in timing mode and 20 million events/s in unit-delay mode on 64,000 primitives, the firm says.

But IKOS isn't even stressing the price/performance ratio of its system, which will also be rolled out at the Design Automation Conference, says president William Loesch. Instead, the emphasis will be on a new capability for stimulus generation and acceleration that the



**STIMULATING.** Software for IKOS Systems' logic simulator makes it easier to enter stimulus programs.

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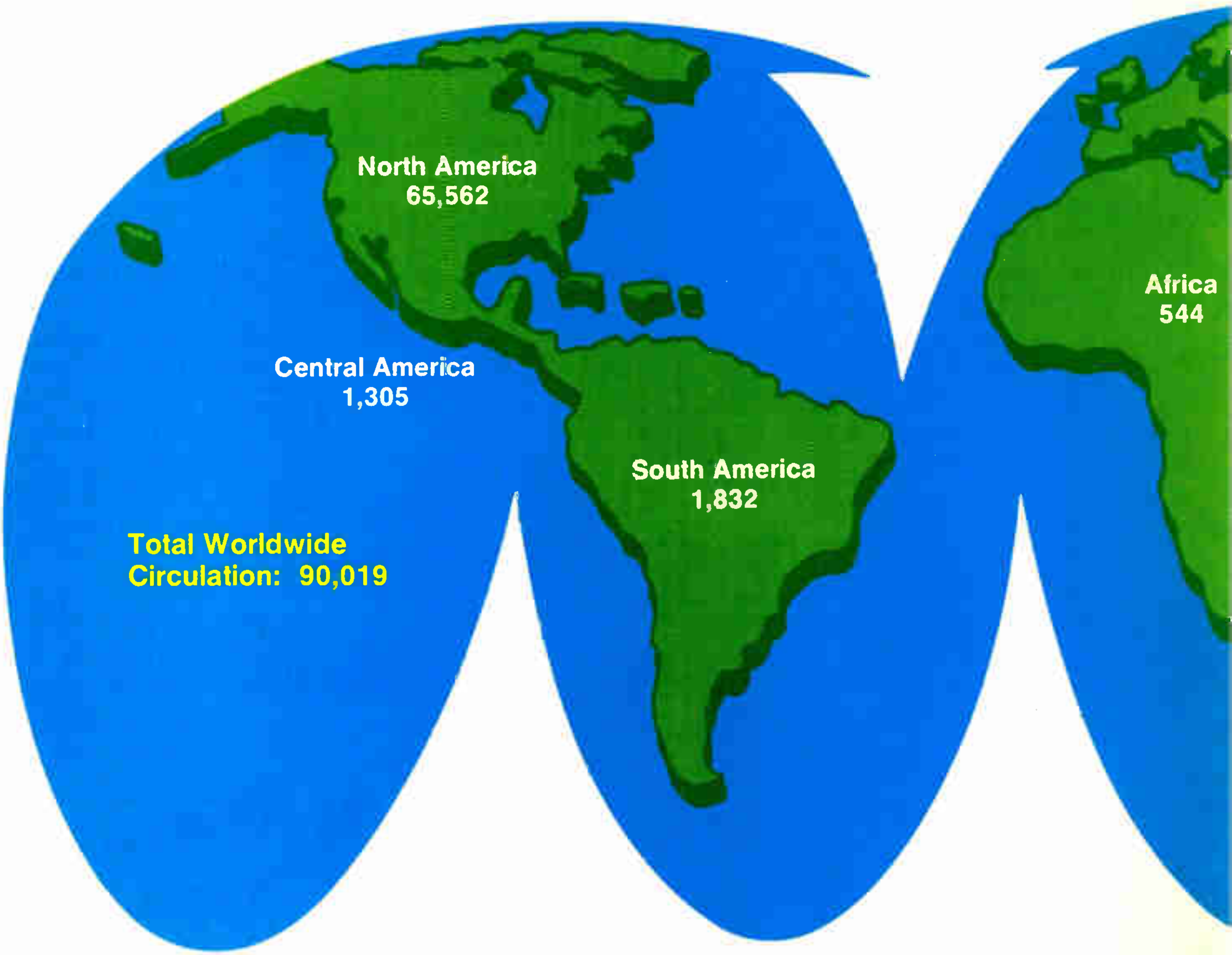

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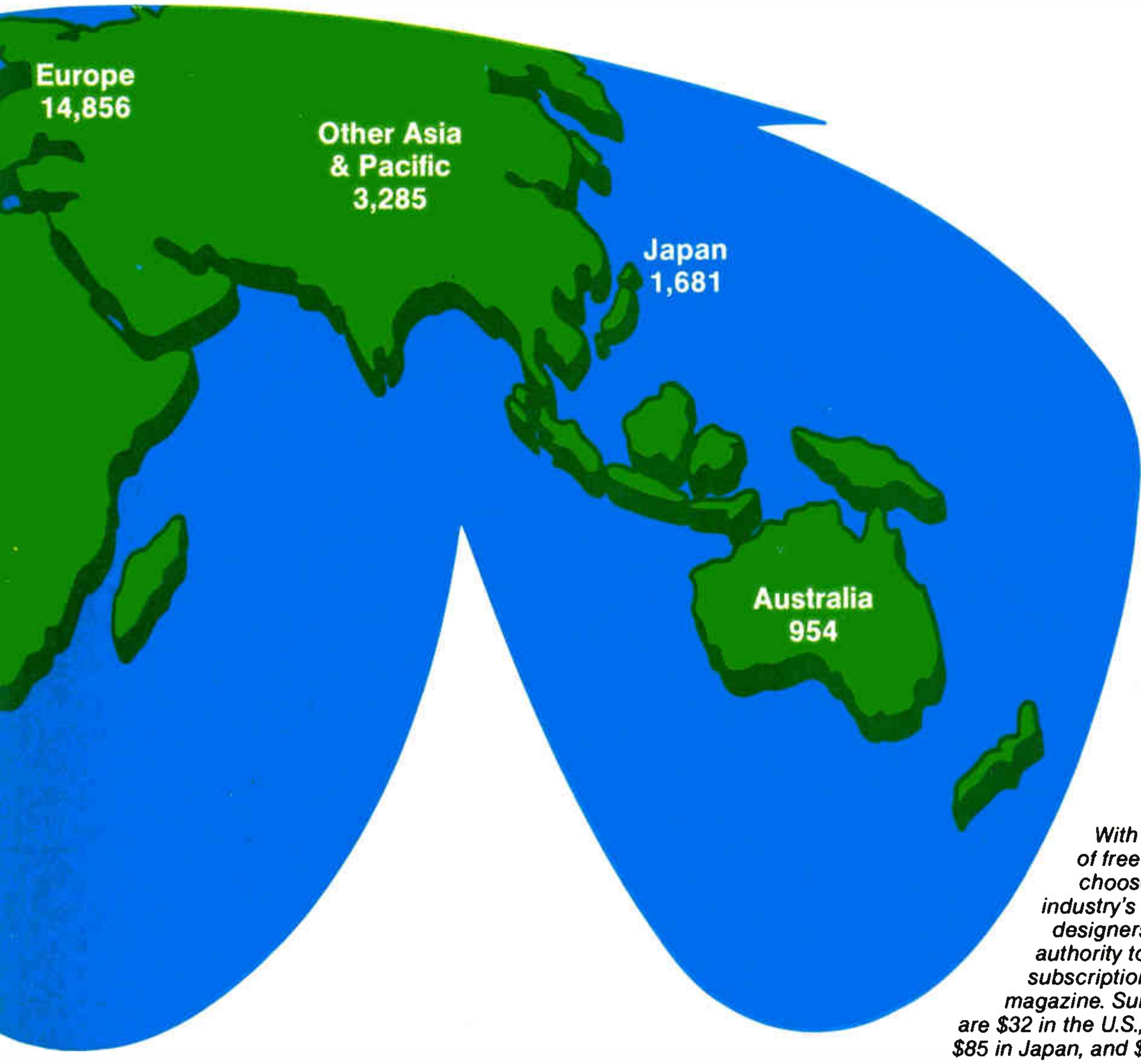


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IKOS 800 will bring to the marketplace.

The IKOS 800 package includes software for an IBM Corp. Personal Computer AT that will allow complex hierarchical stimulus programs to be entered graphically with a mouse, unlike the more time-consuming keyboarding of 1s and 0s typically required for a Zycad system, Loesch says. When transferred from the AT host to the connected IKOS 800 system, the stimulus programs are interpreted by what IKOS calls a stimulus-processing hardware accelerator board. By compressing the stimulus vectors, the board makes possible extremely dense storage of vectors, which are then sent to up to four simulation accelerator boards.

Loesch says the technique makes possible the use of simulation sets of billions of vectors that can represent from several seconds to minutes of real-time device operation. By contrast, he says, other accelerators, such as Zycad's, are typically used to provide only 1 to 5 ms of real-time simulation.

XCAT is also stressing the ease of use of its MX-100. The system comes with a software shell that will make the product easy to integrate into existing CAE networks, says Davenport. The MX-100 can be connected to either a PC AT or an Apollo DN 3000. And like the IKOS 800, the MX-100 will come with software translators that can accept netlists in a variety of formats, including the Tegas design language and the formats used by Mentor and FutureNet. First shipments of the IKOS system are planned for August, and XCAT's MX-100 is available now on a 45-day delivery schedule.

For Zycad's part, chairman and president Richard E. Offerdahl concedes that the features promised by firms such as IKOS and XCAT look good on paper. But, he adds, "There have been 13 companies over the past five years that have announced something that was claimed to be as good as our systems at half or a quarter of the price." So far, he contends, none has panned out.

Until last year, Zycad held the high end of the market. The company has a $54 million installed base, with a customer list that includes Data General, Digital Equipment, IBM, Sperry, and Texas Instruments.

But Zycad sales began stalling out during last year's fourth quarter. In March, the company was forced to lay off 18% of its 250-person workforce and slash the 1986 research and development budget by a third. In this year's first quarter, Zycad suffered its first quarterly loss since it began shipping products in 1981.

At Silicon Solutions Corp., Menlo Park, Calif., marketing vice president Mark Parsinen says his company probably has had something to do with Zycad's slumping business. Silicon Solutions introduced its Mach 1000 line of logic and fault accelerators a year ago, with prices about one third of those Zycad charges for equivalent performance [*Electronics*, June 24, 1985, p. 27].

Silicon Solutions has put 20 to 30 systems in the field since December and plans to unveil at next week's show the Mach 1000F system, which has improved fault-simulation capabilities.

In April, Zycad slapped Silicon Solutions with a lawsuit that charges the California company with violating Zycad patents. But Parsinen denies the charge and calls the lawsuit "harassment." Silicon Solutions recently countersued.

Suits aside, Zycad's Offerdahl concedes an industry shift toward accelerator systems that emphasize better software and ease-of-use features as well as multiple-vendor connectivity. Early Zycad systems essentially left software and network integration to the user.

Zycad is working hard on both fronts, Offerdahl says. About half its technical people are now software specialists, he notes. Furthermore, the company has formed alliances with a number of CAE work-station, software, and semicustom-logic vendors to promote integration of its system. *–Wesley R. Iversen*

**PERSONAL COMPUTERS**

# THE RETAIL CHAINS FIND A NEW WAY TO FIGHT BACK

**SAN JOSE, CALIF.**

Another sign that the tough times aren't over in the personal computer business came earlier this month in the introduction of IBM Personal Computer AT compatibles by Businessland and Computerland. The private-label systems from the two big national business-computer retailers are a way of hiking profits in the fiercely competitive PC market.

Private-label products are a way of survival, says Jon Holtzman of the Gartner Group in Stamford, Conn., because the profit margins are higher than on either IBM's machines or the brand-name compatibles that Businessland and Computerland retail. "The dealers have had a rough time making any kind of profit," he says. Their margins on personal computers have been as low as $100 to $150.

*Private-label PCs help retailers hike profit margins*

Businessland Inc. last week announced that it will market an AT-compatible machine built in Taiwan by its San Jose neighbor, Wyse Technology. Price of its PC286 will range from $3,295 for a basic version with a 1.2-megabyte floppy disk, a hard-disk controller (but no drive), eight expansion slots, a clock, and a dual-speed (6- or 10-MHz) Intel 80286 microprocessor to $4,795 for a version with a 30-megabyte hard disk and serial and parallel ports.

Computerland Corp. should undercut that price this week with a modular AT-compatible machine expected to cost about $2,900 for a stripped-down version. The Computerland box reportedly also accepts an Intel 8088 processor, so it can be made compatible with the PC/XT as well; that version reportedly will sell for under $1,500. Trigem Ltd. is building the system in South Korea.

Industry analysts see the new machines as profit channels for Businessland and Computerland. "The prices aren't much better than IBM's," says Holtzman, "but the margins will be very competitive. The stores will be pushing the brands that make them the most money and are the easiest sales."

Norm DeWitt of Dataquest Inc., San Jose, says that the chains will become small-systems integrators and tailor their private-label machines as alternatives to AT&T, IBM, and Compaq products. "We hear that the Computerland machine will sell for $200 to $300 below IBM and still yield more profit dollars to the dealers," he says. "It's a way for the dealers to increase profits. They can add memory and add-on boards and build a machine that goes out the door at $5,000 to $6,000."

DeWitt also points out that Computerland franchises are free to cut prices independently if they wish. The private labels will definitely have an impact on established brands, he says. "The retailers will sell IBM if that's what the customer wants. But they will push their private label whenever they can."

Nonetheless, bargain hunters will probably buy elsewhere. Wyse itself introduced an AT-compatible last week selling for $600 to $800 under the Businessland machine, depending on the amount of mass storage. And smaller discount dealers have been far below the retailers' prices for some time.

"The marketplace is two-tier," points out Richard Dalton of Keep/Track, a San Francisco market researcher. "There are so many cheap ATs around that Computerland is getting chewed up by the small discounters."

Fry Electronics in Sunnyvale, Calif., for example, sells a Korean CompuStar AT with 20 megabytes of storage at $2,495, including monitor and graphics card. Mainstreet Computer, a Bastrop, Texas, mail-order house, advertises an AT-compatible with a 1.2-megabyte floppy disk and a hard-disk controller for $1,975. And Wells America, a mail-order discounter in West Columbia, S. C., sells an AT-compatible configured like Businessland's minimum version for $1,495.

The key to success of the private label will be customer belief that the machines are IBM-compatible, Holtzman says. "There are so many low-cost clones out there that have proven compatibility, that there shouldn't be much resistance," he adds. *–Clifford Barney*

# THE LAPTOP MAKERS ARE SHARPENING THEIR CLAWS

**GLENVIEW, ILL.**

Now that IBM Corp. has shown its hand in the laptop personal computer market, competing vendors are moving in with products that exploit what they see as the IBM Convertible's weaknesses. Zenith Data Systems points to the Convertible's display and its inability to run many programs written for the standard desktop IBM PC as areas it has improved upon with the laptop it introduced last week.

The subsidiary of Zenith Electronics Corp. last week rolled out its Japanese-built Z-181—an 11.8-lb PC/XT-compatible machine that, unlike the company's Z-171 laptop, has 3½-in. floppy-disk drives matching those used in the Convertible. The Z-181's electroluminescent-backlit liquid-crystal display, which emits blue light, offers a 12:1 contrast ratio and can be read easily even if the viewer is 45° off the center axis.

**BRIGHT.** Zenith's Z-181 laptop sports 3½-in. floppy-disk drives and a backlit display.

The 25-by-80-character screen's contrast ratio rivals that of cathode-ray tubes, Zenith says. This, coupled with a 10½-in. screen size, makes for a display that beats any other portable on the market, says John Frank, Zenith Data Systems marketing vice president. "And because the shape of the screen provides the same aspect ratio as you see on a CRT, you don't get egg-shaped circles and stretched-out characters as you do on a 9-in. display," he adds.

As for software, "The Convertible is not fully PC-compatible. The Z-181 is," says Andrew Czernek, director of marketing. "The Convertible has had enough compatibility problems that it may not be an acceptable solution to many customers' problems," he adds.

The Z-181 comes with 640-K bytes of memory, separate serial and parallel ports, and a video controller for an external monitor. It sells for $2,399. A similarly equipped IBM PC Convertible with its maximum of 512-K bytes of memory would carry a price tag close to $3,000.

When opened, the 13.4-by-11.6-by-3.1-in. Z-181 reveals two pop-up 3½-in. disk drives, each able to store 720-K bytes on one disk. The company says it doesn't plan to miss the boat if the IBM entry touches off a widespread industry move to a new 3½-in. standard. For transferring information from 5¼-in. disks, the current industry standard, to the smaller 3½-inch disks, the Z-181 has an interface for an external 5¼-in. disk drive.

Zenith's Z-171, a laptop with dual 5¼-in. floppy-disk drives, was introduced last year and is already off and running hard on the strength of a recent contract won by Zenith over IBM to supply portables to the Internal Revenue Service [*Electronics*, March 3, 1986, p. 16]. Since the IRS deal, Z-171 sales have been running far ahead of company projections, Frank says. The Z-171 got an added boost when it was picked up recently by Computerland Corp. for sale in its 600-store chain, he adds. Computerland will also sell the Z-181.

With a foot now in both the 5¼- and 3½-in. floppy camps, Zenith Data Systems appears well positioned to play in whatever laptop market develops. But Frank, for one, thinks an industry transition to the 3½-inch format could be rapid, despite the huge installed base of 5¼-in. desktop machines.

"The feedback we're getting is that there is very little reluctance on the part of the market to move from 5¼ in. to 3½ in., particularly on the portables," Frank says. *–Wesley R. Iversen*

***OPTOELECTRONICS***

# SWITCH MAY SPEED OPTICAL COMPUTING

**SAN FRANCISCO**

Researchers investigating methods of putting optical computing theory into practice may now have the answers to some of their problems—specifically, circumventing high power consumption and developing the ability to cascade devices so they can be used to implement logic. David Miller, a technical staff member at AT&T Bell Laboratories in Holmdel, N.J., has come up with an optoelectronic device structure that he says addresses those problems directly.

Using molecular-beam epitaxy, Miller produced an optoelectronic switching device made up of 2,500 alternating layers of gallium arsenide and aluminum gallium arsenide. "It's a relatively practical device," he says. "It runs at room temperature; we can make very uniform devices; and it's cascadable."

Miller described his work at last week's Conference on Lasers and Electro-Optics in San Francisco, saying he has produced a two-by-two array using the structure—called SEED, for Self Electro-optic Effect Device—and that the technology has potential in optical solutions to high-speed computing and telephone switching. The array has a switching threshold that can be set between 40 pW and 1 mW, depending on the power of the external light source used to operate it. The array needs only two electrical connections.

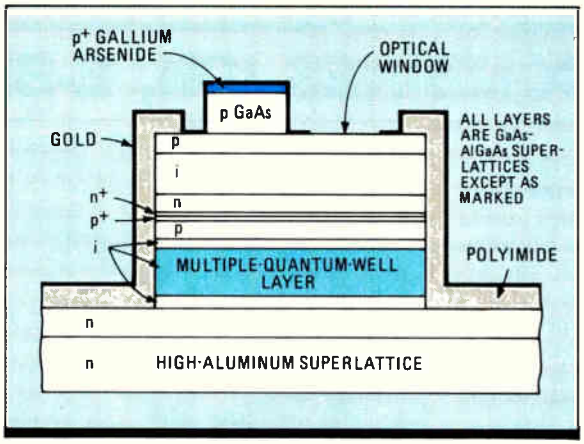
The SEEDs are activated when light from a laser diode is applied to their optical windows, Miller says. "You shine light into that window, and some of it will be detected, and some will pass right through the device and out the other side. Internally, it converts some of the light into electricity and uses that current to help operate a switch. The switch operates by positive feedback."

A multiple-quantum-well layer is "the magic part" of SEED, Miller says. It is across this region that a voltage appears, and, when light is applied to the optical window, this layer tries to absorb it. "As we increase the light, we generate a photocurrent in the quantum wells," he explains. "And as the photocurrent is increased, the voltage is diminished."

The result is a regenerative action in which the quantum wells eventually absorb so much light that the voltage falls to near zero and activates the switch. At that point, however, the device has reached its most saturated state.

When the light's power is increased, the regenerative process reverses itself, and the switch starts to restore itself to its original highly transmissive state. Miller calls this the quantum-confined start effect, defining it as an inverse relationship in which the SEED's ability to absorb light increases as its ability to carry a voltage diminishes.

The key to the device is that it is cascadable. "What we've demonstrated here is a vertical optoelectronic integration technology," he says. "The output wavelength is an acceptable wavelength to trigger the next device—the next switch. That has not been done before. And to make any logic system, you have to be able to stack devices."




**LIGHT SWITCH.** The SEED is a bistable device that switches an electric current in response to light hitting its top side.

Miller's initial experiments have been limited to an array of four devices, each 200 by 200 μm, built on a GaAs wafer. An insulating layer of polyimide separates the individual devices, and it in turn is covered with a common gold contact. The substrate connects to the positive terminal of a power supply and the gold contact to the negative terminal. These are the only electrical connections needed. The bistable switching threshold is set by the light source; wavelengths of from 834 to 859 nm can be transmitted, and threshold voltages from 4 and 40 V can be obtained.

Switching speed, which is currently variable from 1 μs to 10 s, can be set by adjusting laser power and device size. Miller's devices were built larger than necessary so that their operation could be observed easily. "The obvious thing to do now is to make it smaller," Miller says. The technology "provides a means, a potential, for very good, complex devices that can perform different kinds of functions—memory, for example." *–Tobias Naegele*

***BOARD PRODUCTION***

# CAD DATA MAKES INSPECTION FLEXIBLE

**BOSTON**

A new breed of machine-vision inspection systems may soon enable designers of printed-circuit boards to improve yield and reliability without limiting design features or slowing down production lines. The new systems will rely on computer-aided-design data bases for a standard of comparison and on powerful new computer architectures to do inspection. They'll provide process-control information in real time.

One such system, announced at last week's Nepcon East Conference, can inspect typical bare pc boards in 20 seconds with a resolution of 0.5 mil, according to its developer, Cambridge Robotic Systems Inc. To allow the Foresight 18.5 system to use data generated by a wide variety of CAD equipment, the Watertown, Mass., company set it up to read formats used by photoplotters from Gerber Scientific Instrument Inc. So the system accepts data from the preponderance of board-CAD systems, which also use the Gerber formats.

**CAD HEATS UP.** Other companies have also moved in the CAD direction. DIT-MCO International Corp., Kansas City, Mo., was first to market a CAD-based visual-inspection system—the P-SEE—in 1985. It inspects boards in 45 s to 3 min. And Optotech Inc., Billerica, Mass.—the acknowledged installed-base leader in visual board-inspection systems—offers a design-rule-based system with some data-base-technique features.

Visual inspection systems provide the only means of identifying many existing or potential board problems, such as "mouse bites" or hairline shorts. In other cases, such as the checking of unfired ("green") ceramic, only optical inspection techniques can be used without damaging the material.

Most existing vision systems check what they see, not against specific data, but against design rules. These systems require the establishment of criteria for all board features. Their chief advantages are higher speed and lower cost.

But design-rule systems impose serious limitations on design features. For example, design-rule techniques can be stymied by boards with variable line widths. In other cases, it may be extremely difficult to develop sophisticated feature-recognition algorithms that allow for interconnection variations. Surface-mount components that do not terminate in pads, for example, present special problems.

*CAD-based vision systems provide design flexibility*

CAD-based vision systems provide for unlimited design flexibility. They need no machine learning because CAD tapes may be loaded into them, so that they perhaps require only some adjustments for the variety of possible formats.

Large amounts of computer power are required for such systems, however, and they can be thrown off by features that have shifted slightly from their designated locations because of environmental or processing stress, which can alter the board shape. What a person can account for by eye "often takes man-years to [emulate] electronically," says Ralph Taylor, chief of engineering at DIT-MCO's research and development division.

Richard Sheroff, vice president of sales and a designer at Cambridge Robotics, says the problem of shifting was solved with a proprietary metrology method that combines a forward scanning pass with a return pass.

To solve the computing problem, which in the case of the Foresight system requires the comparison of up to 2 billion 0.5-mil pixels with the data base, Sheroff says a reduced-instruction-set parallel architecture has been employed. The hardware includes twenty 32-bit computers, 18 of which are proprietary very large-scale integrated circuits, that combine to execute up to 180 million instructions per second.

As boards are inspected, error information is forwarded to inspection-verification stations, where colored lights point out regions containing errors. Sheroff says the system lets no errors get by and reduces false alarms to the industry minimum. *–Craig D. Rose*

# SYSTEM COMBINES ION, E-BEAM STEPS

**TOKYO**

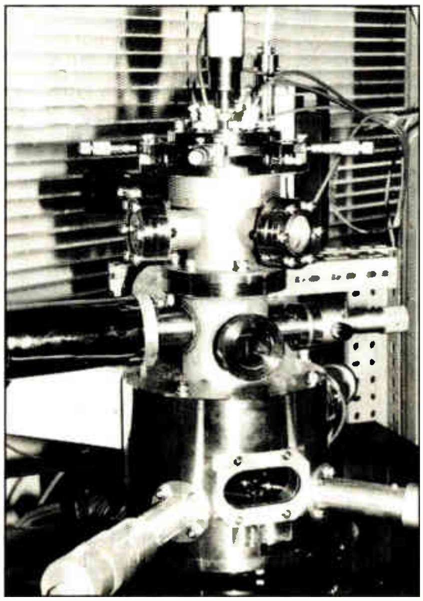
A scanning-beam system that can switch almost instantly between ion- and electron-beam generation could make it a lot simpler to turn out ultra-large-scale integrated circuits. The hybrid system can do operations that now take separate pieces of production equipment—for example, ion-beam implantation or machining followed immediately by observation of the results through electron-beam-based measurement techniques or by an electron-beam annealing step. It will be able to produce line widths even smaller than those required by 16-Mb memory chips, a key requirement for ULSI processing.

Furthermore, the hybrid system can produce electron beams with more than 10 times the current intensity previously attainable. And because the electron source is about 1/100 the size of other sources, an improved electron-optic lens system should produce a much finer beam, making possible observations down to atomic levels, say the researchers. The system's ability to generate electron beams was not envisioned when the first prototype of the system was announced almost three years ago as an improved scanning ion-beam system [*Electronics*, Oct. 6, 1983, p. 90].

The first commercial versions of the system, which Hitachi Ltd. has been developing jointly with Toyohashi University of Technology, will probably be ready in about two years, says Masahiko Ogirima, department manager of the Fourth Department at Hitachi's Central Research Laboratory here. A paper describing the system is scheduled to be given by Satoshi Nishigaki, a Toyohashi assistant professor, at the International Field Emission Symposium in Berlin July 7 to 11.

Switching the system from ion-beam to e-beam operation is primarily a matter of reversing the polarity of voltages applied to the beam-extraction and acceleration electrodes (diagram). The simplicity of conversion makes it possible to instantly change mode of operation on the fly for sequential operations requiring an ion beam on the one hand and an electron beam on the other.

Along with ion machining, the system should prove valuable for the generation of submicron patterns by unmasked ion-beam implantation and by electron-beam lithography in photoresists. Mask repair is another possible application.



**HYBRID.** The Hitachi-Toyohashi scanning-beam system can generate an ion beam one instant and an electron beam the next.

Observation and measurement can be done using ion beams but resolution is poor compared to that available using e-beams. The electron beam also can be used to improve alignment accuracy. Because of its light particles, it can anneal the damage caused during implantation with heavy ion dopants.

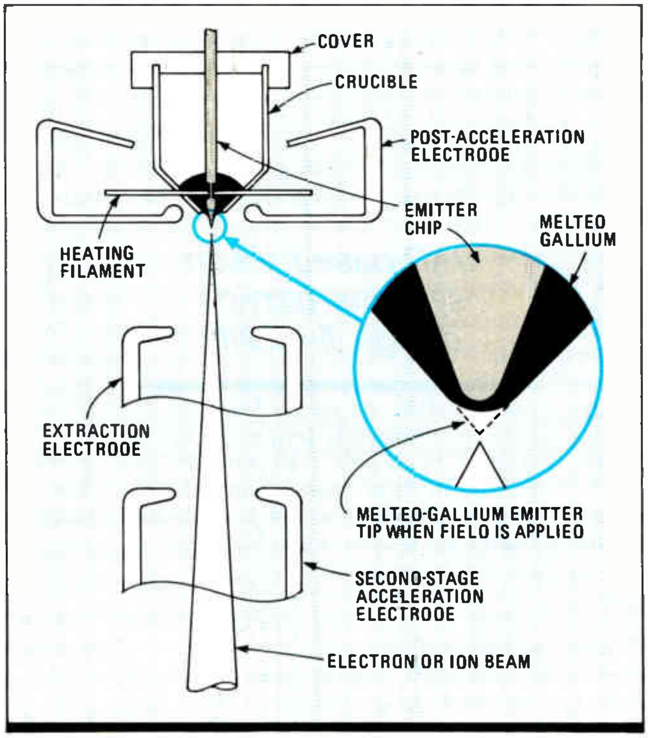
It is possible to generate a negatively charged ion beam with the system. Simultaneous ion implantation and annealing should be possible with simultaneous emission of electrons and negative ions, Ogirima speculates.

**LOW CONTAMINATION.** The hybrid system's means of ion-beam generation is reasonably conventional, except that the metal ion source is heated by electron bombardment rather than by a resistor heater, which removes a source of contamination. Electrons from a filamentary cathode are accelerated by an applied voltage to a crucible containing the metal, where they give up their kinetic energy as heat, melting the metal in the bottom of the crucible.

Surface tension holds the metal in the crucible, despite the opening around the needle-shaped tungsten chip that protrudes through the center of the opening. The electric field from the extraction electrode pulls the molten metal to a fine point less than 10 Å in diameter, forming the tip of the emitter just below the point of its tungsten support, and positive ions of the metal are emitted.

With the extraction-electrode and accelerating-electrode voltages reversed for electron-beam emission, the molten metal is again drawn down to a fine point less than 10 Å in diameter, compared with perhaps 1,000 to 2,000 Å for a conventional tungsten electron-beam cathode. The smaller source is what should make possible future reductions in beam diameter for higher-resolution work.

Moreover, an extremely low-pressure vacuum is needed with a conventional cathode to prevent generation of gas ions, which wear down the emitting point and further increase its radius. The liquid-metal cathode retains its shape even with a relatively low vacuum because new material flows in to replace any small amount lost. The greater durability of the emitter makes it possible to increase beam current by a factor of ten. The ability to work at lower values of vacuum is advantageous in semiconductor-processing equipment because less vacuum pumping is required after loading wafers, making for much cheaper equipment. *–Charles L. Cohen*




**FINE POINT.** A field pulls melted metal on the emitter tip into an extremely sharp point for generation of narrow electron beams.

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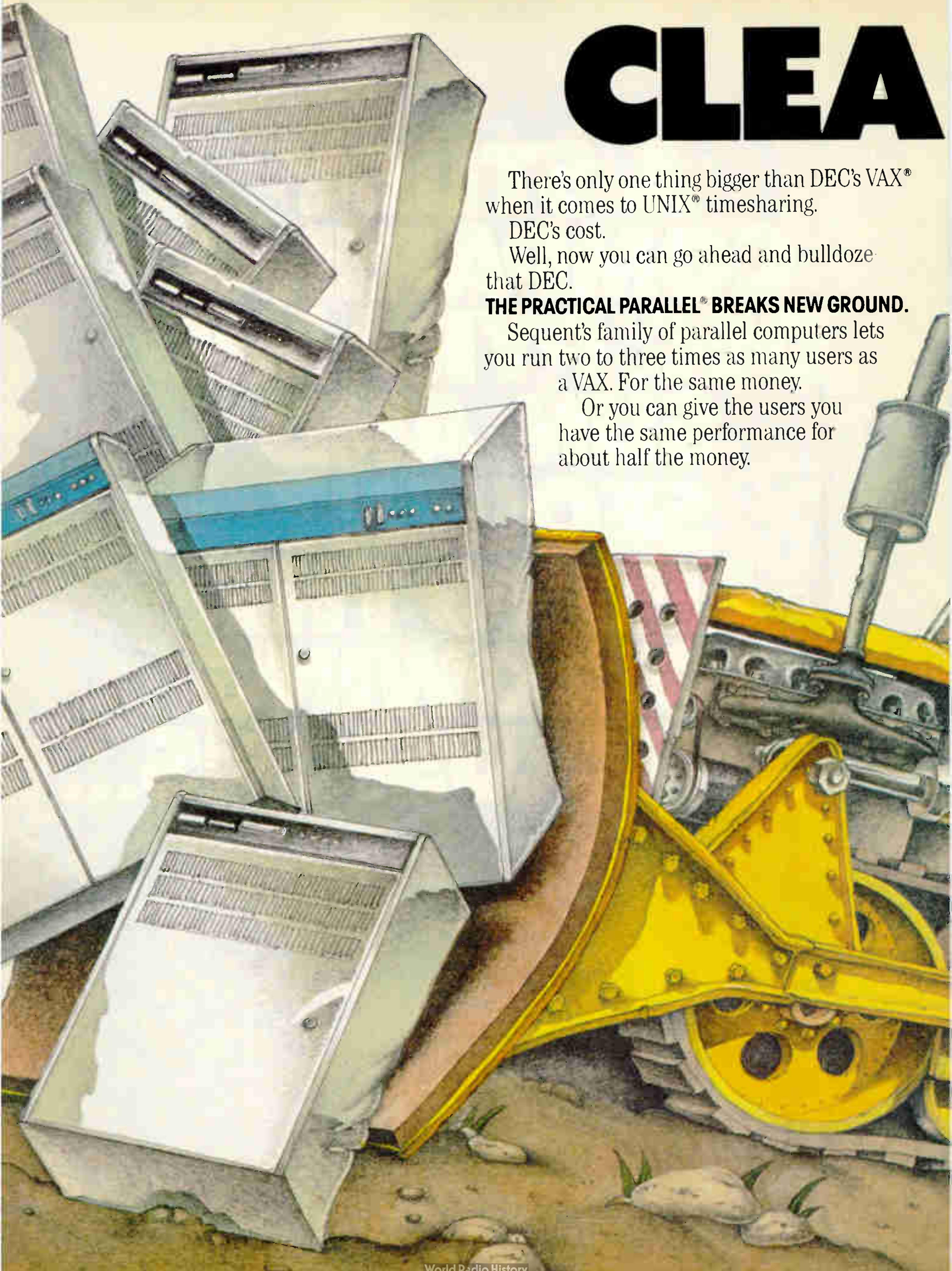
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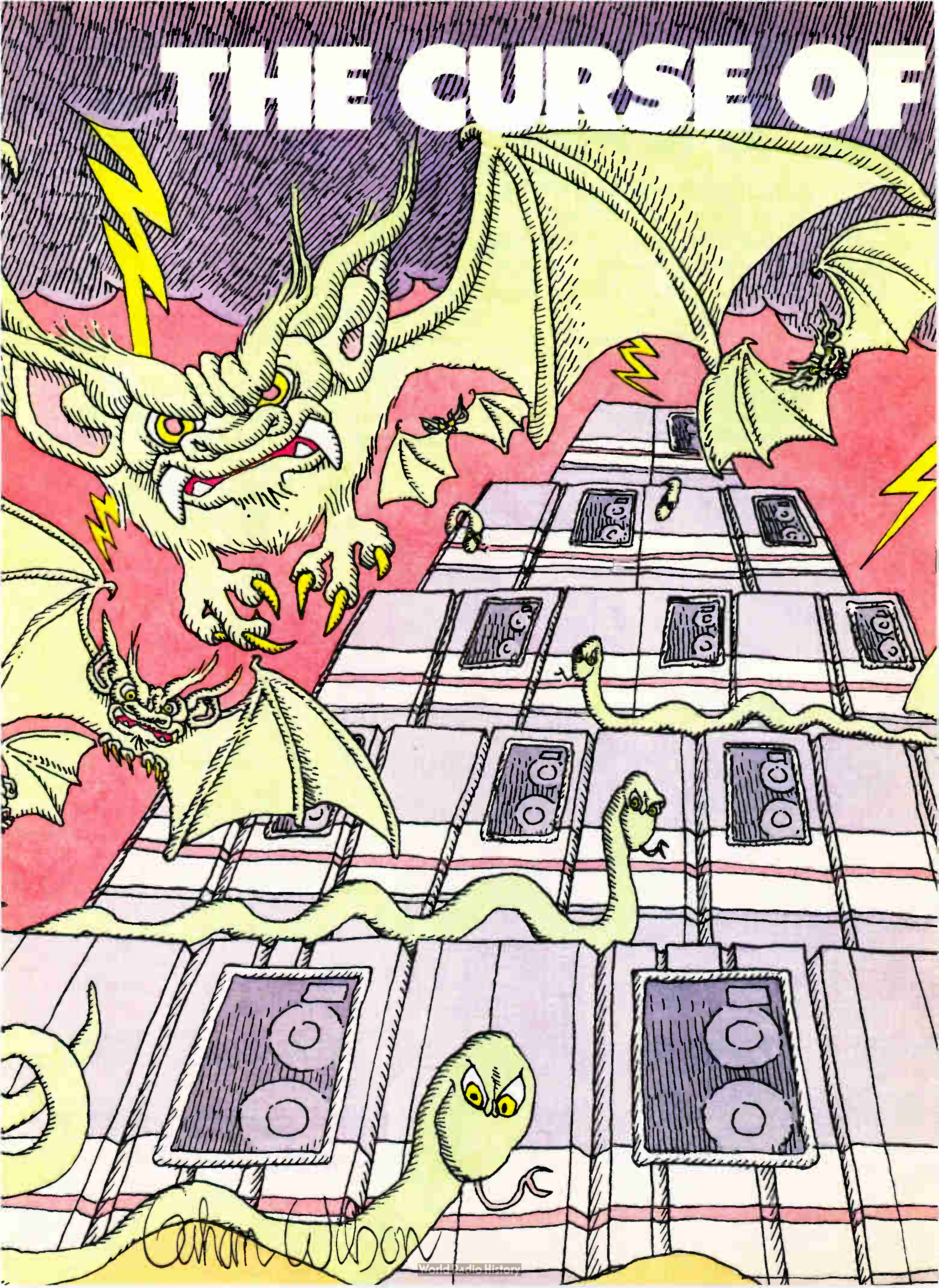
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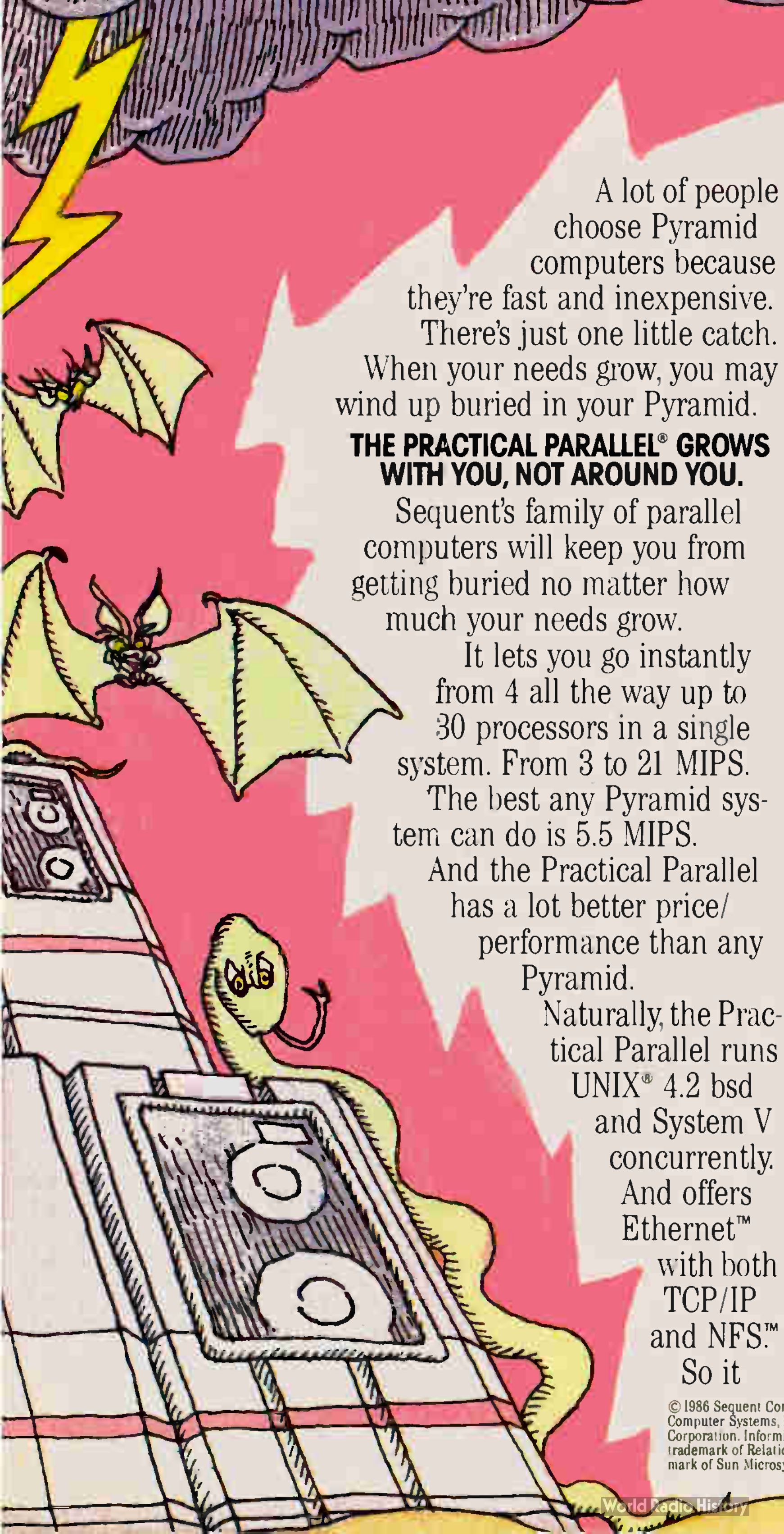

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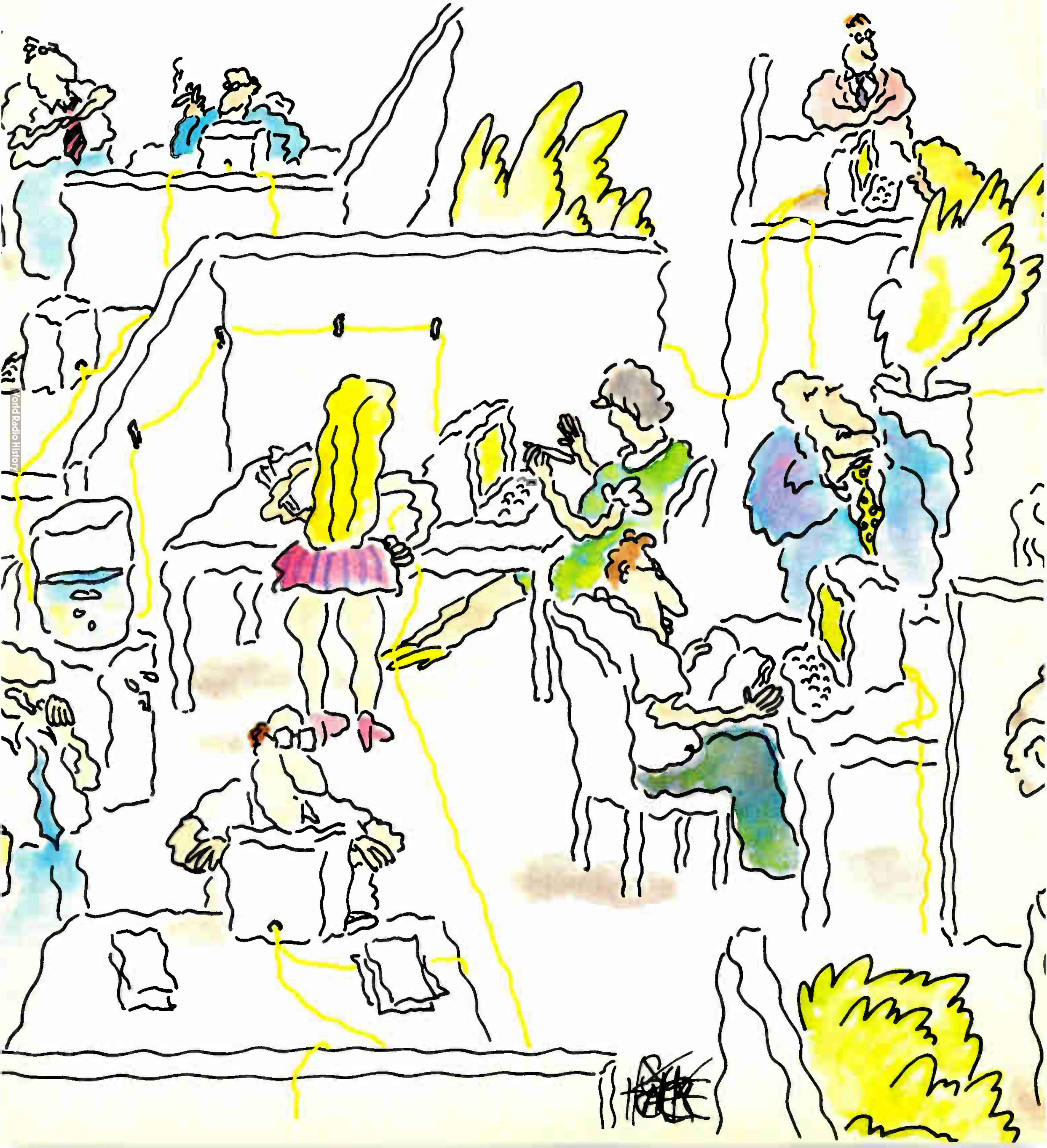

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Circle 35 on reader service card

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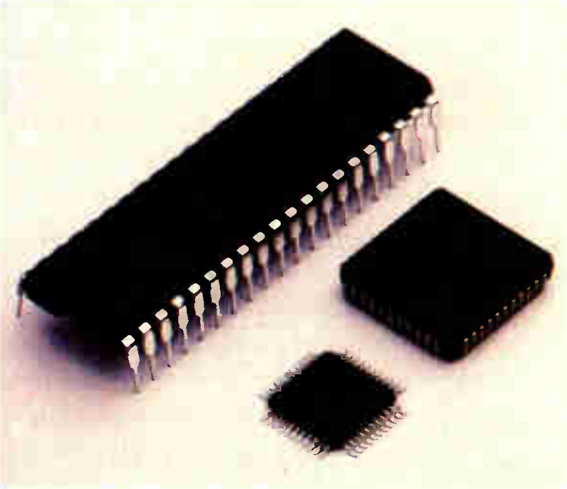
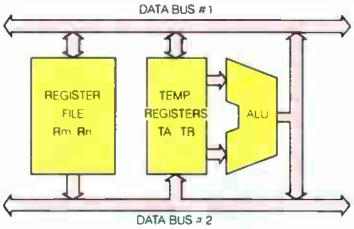


The V20/V30 are powerful CMOS microprocessors providing high-speed performance at vastly reduced power consumption. Internally 16-bit, the V20 has an 8-bit external bus, and the V30 is a full 16-bit machine. Both feature NEC's unique dual bus architecture, two program counters, and a super-efficient address generation logic, making them up to 50% faster. Low heat dissipation allows flexible plastic or ceramic-based packaging in three different configurations.

Pin compatible with µPD8086/88 devices, the V20/V30 incorporate an enhanced instruction set giving that extra performance edge required by time-critical applications. A complete range of compatible CMOS peripherals keeps engineering effort to a minimum. Heavy computational loads will be catered for by a CMOS floating point processor. There is a choice of 5,8 and 10 MHz clock rates for different operating environments.

| V20/V30 CMOS peripherals. | |
|---|---|
| µPD71051 | Serial control unit |
| µPD71054 | Programmable timer/counter |
| µPD71055 | Parallel interface unit |
| µPD71059 | Interrupt control unit |
| µPD71071 | DMA controller |
| µPD71011 | Clock pulse generator/driver |
| µPD71082/83 | 8-bit latch |
| µPD71086/87 | Bus driver/receiver |
| µPD71088 | System bus controller |

Compatibility of development tools safeguards investments and provides familiar and time-proven methods of reaching powerful new solutions. NEC support software includes an in-circuit emulator package, relocatable assembler plus a C-Compiler µPD8086/88 code written for both the Small and Large model can be run without modification on the V20/V30. The migration path to the V40/V50 microprocessors underlines NEC's overall V-Series software compatibility strategy. In addition, the V20/V30 are supported by development systems from Hewlett-Packard and Tektronix. NEC's V-Series devices are secondsourced by Zilog and Sony.

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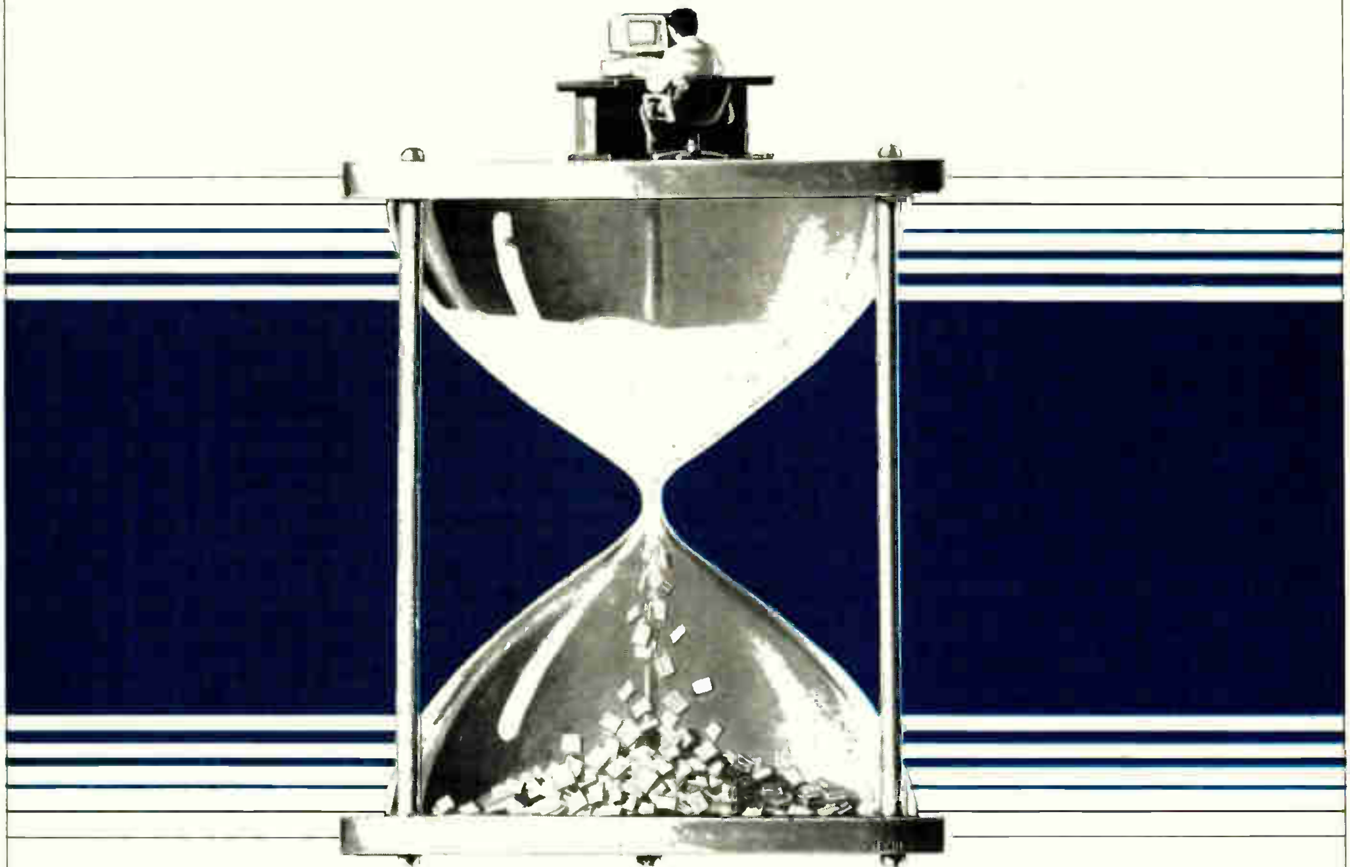
Circle 88 on reader service card

# INSIDE TECHNOLOGY



# TURNING A PC INTO A SILICON COMPILER

## FROM SCHEMATIC TO FOUNDRY IN LESS THAN AN HOUR

Circuit designers undoubtedly dream often of having their very own silicon-compilation system—a desktop computer that would give them a spreadsheet-style "what-if" capability near at hand. With it, they could alter a circuit description or physical layout and choose different manufacturing processes and design approaches. Then, a short time later, designers could see the results and decide either to make more changes or go with what they've got.

Lattice Logic Ltd. says its Silicon Compiler Spreadsheet can make all that happen. Now a logic designer can generate a design, enter the schematic, simulate the circuit, and in roughly half an hour have it automatically placed and routed on a 3,000- to 5,000-gate array. Best of all, this capability is available complete on a $25,000 work station. The system includes an IBM Corp. Personal Computer AT-compatible computer and a 32032-based processor to run Chipsmith, the Edinburgh, Scotland, company's silicon-compiler software.

Once the designer keys in his initial design specification, the design data is displayed on a large 1,280-by-800-pixel monochrome display by means of a GEM windowing system from Digital Research Corp., Pacific Grove, Calif. The window interface makes the system easier to use for designers accustomed to developing circuits on boards or for those who are using computer-aided engineering for the first time. The company says color capability will be introduced later.

Designs can be entered in two ways with Chipsmith. Users can write a circuit description in Model, the company's proprietary hardware description language. There is a strong parallel between Model and the block-structured programming languages of the Algol family such as Pascal, Algol-W, Algol 68, and PLI. If the circuit designer is more

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familiar with schematic entry, he can use the system's schematic editor, which takes a pictorial representation of the circuit in block diagram or schematic form and automatically converts it into Model statements.

Model describes the circuit hierarchically in terms of parts, or basic building blocks. The most complex part is the entire circuit; the simplest are the primitives—gates at the base of the hierarchy. Gates are described internally in terms of transistors. Between these extremes, a part can be defined as any coherent portion of the circuit with input and output signals. A part's definition specifies its internal structure as instances of simpler parts and their interconnections.

## HIGH-LEVEL LANGUAGE FEATURES

An instance is the use of a part within the definition of a more complex part. Any number of instances of a particular part may occur in the same design. Primitive parts such as NAND and NOR gates, inverters, and other logic elements are predefined in the system libraries and need not be defined by the designer. Included in Model are many features of high-level programming languages, such as loops, control structures, and parameterization.

Parameterization, for example, enables Model to code a part as an n-bit ripple counter (Fig. 1). The number of bits can be determined at will simply by giving a value to n. Thus by simply editing the Model program that describes it, a design can be changed substantially, much like numbers are changed by a spreadsheet. Users can edit the actual code or the schematic representation on the display screen.

Once the user is satisfied that the circuit has been fully described, either by hardware description language or the schematic editor, the Model program is compiled. The compiler checks the design for errors in the same way a high-level-language compiler checks program source code. It can detect such errors as wrong syntax, incorrectly formed Model statements and structure, illegal use of signals, unconnected inputs or outputs, and shorted nets.

If no error is found, or once errors have been corrected, the compiler generates a netlist file in intermediate design language (Fig. 2). The netlist contains all the transistors and their interconnections. This becomes the system's internal data base and is read by both the integral switch-level simulation environment and the physical design subsystem.

Chipsmith simulates at the switch rather than gate level to more accurately model the individual performance characteristics of transistors, the basic building blocks of MOS technology. Called Exert, the switch-level simulator has the advantage of permitting virtually all digital logic designed for MOS processes to be simulated in a reasonable time. When a designer is working with a MOS process and using a gate-level simulator, which is primarily intended to work with bipolar technology, he must often code up a dubious gate-level equivalent or a part that does not lend itself to such modeling. In addition, the switch-level simulator can deal with load capacitance on nets to give a more accurate timing simulation.

Rather than being just a unit-step-delay switch-level simulator—a tool for evaluating a design's functionality—Exert is a hybrid simulator. It offers the speed of switch-level simulation with much of the accuracy of circuit-level simulation. Exert is only slightly less accurate than circuit-level simulators, which are too slow to be useful for large- or very large-scale-integration designs.

The simulator ensures the engineer of the design's functional and temporal correctness. It can produce vectors during simulation for postfabrication tests with industry-standard testers. Lattice Logic's system typically simulates 4,000- and 5,000-gate arrays in about the same time as a Digital Equipment Corp. VAX-11/780 superminicomputer. With that much processing power on his desktop, the designer need not submit his job to a central processor and wait for his simulation results.

Having the simulator resident on the desktop system also means that the designer can make changes to his circuit design and resimulate at any time and as often as he wishes, manipulating it like a spreadsheet. During simulation, the designer develops the stimulus patterns used to verify the circuit's operation. He then runs a timing simulation that approximates the circuit's operation at its final operating clock rate. For timing analysis, Exert uses two models. In the simpler of these, the simulator assumes that all transistors in the design are the same size and the wiring capacitance is proportional to the number of gates attached to the wire.

In the second model, the designer supplies wire-capacitance information and individual transistor size to produce a simulation that more realistically reflects the actual design. Finally, he performs a circuit fault simulation to weed out any errors that may adversely affect the long-term reliability of the circuit. Exert, used as a fault simulator, will apply "stuck-at" fault types to a circuit to evaluate the fault coverage provided by a specific set of test vectors.

Once an appropriate set of vectors has been developed, the simulation results can be combined with the circuit description

```
Part d type flip flop [clock, d,preset, clear] → q,qnot
{ D-type flip-flop with set and clear made with crosscoupled nand gates }
    Signal w,x,z,a
    nand[d,clear,x] → a
    nand[a,clock,w] → x
    nand[clock,clear,z] → w
    nand[w,a,preset] → z
    nand[x,clear,q] → qnot
    nand[qnot,w,preset] → q
End
Part ripple counter (n) [clock,reset] → q out(1:n)
    Signal last qbar(0:n),n reset
    Integer loop
    not[reset] → n reset                   {gives an active-high reset signal}
    not[clock] → last qbar(0)              {for part to be active on negative-going edge}
    For loop 1:n Cycle
        d type flip flop[last qbar(loop-1),  {clock input pad from last flip flop}
                         last qbar(loop),    {d-input pad from own qbar}
                         Vdd,                {preset tied high}
                         n reset] → q out (loop), {to output of part}
                                 last qbar(loop)
                         {ripple counter formed by using D-type flip-flops
                         with q-bar output fed back}
        Repeat
End
Constant n=4
Input Pad clock,reset
Output pad q out(1:n)
ripple counter(n) [clock,reset] → q out(1:n)
Endoffile
```

**1. MODEL CODE.** The Model language's parameterization feature makes it possible to represent a ripple counter as a circuit with n number of D-type flip-flops.

to develop a test program to run on a Sentry tester from Fairchild Test Systems Division, San Jose, Calif. The process is automatic and is carried out by a program called Totest (Fig. 3). The time required to debug the design depends on how exhaustively the designer wishes to simulate his circuit before final implementation.

Once the design has been sufficiently debugged, Chipsmith can begin placing and routing the circuit. At this point, the designer has the choice of three design modes based on gate arrays, optimized arrays, or standard-cell libraries.

In the first, a program specifies the chip image for the basic CMOS array, leaving only the single-metal interconnection layer to be personalized as the final step. The gate array's basic unit or stage is a pair of discrete p- and n-type transistors with a common polysilicon gate and independent source and drain connections. The array consists of rows of stages arranged in cores—or columns—separated and surrounded by standard-sized wiring channels built from groups of poly underpasses. Stages are wired up by metal interconnections to form the basic library parts. These in turn are wired vertically by the poly underpasses and horizontally by the single metal layer. The underpasses are arranged in such a way that unused polysilicon is not connected.

This design mode suits small production runs of less than 10,000 chips over the life of the final product or instances where the gate array is used as a prototype circuit in a larger printed-circuit board design. Here, the designer can create a gate array and use it to debug his breadboard. Gate-array prototyping also helps find problems not detected by simulation alone.

## CUSTOMIZED CHIPS

The second mode turns the gate array into an optimized custom implementation after the board design has been debugged. In creating a custom chip, the circuit design is used to produce an accurate gate count and wiring channel map. This, in turn, automatically generates a fully personalized array. This mode uses the same row-and-column floorplan as the first, but a different basic stage design.

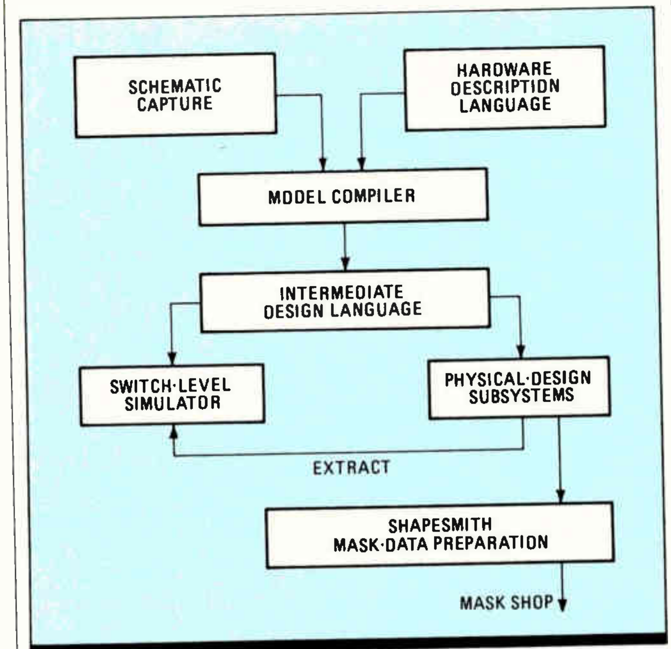
Though the stage consists of a pair of p- and n-type transistors with a common poly gate, adjacent transistors share a source and drain. Wiring channels do not consist of standard-sized underpasses but are built as required to satisfy the wiring demand. All unused poly and diffusion, including transistors, are removed.

The standard-cell mode again uses a similar floorplan. Wiring channels are built as in the optimized design mode. But instead of stages, the rows consist of standard cells whose inputs and outputs connect to the poly layer's wiring channels from the top or bottom. Internal wiring is generally predetermined in standard cell libraries, though users may have the option of altering it to suit particular needs. In this mode, Chipsmith will make the most efficient use of silicon area in placing and routing the cells and keep the wiring to a minimum.

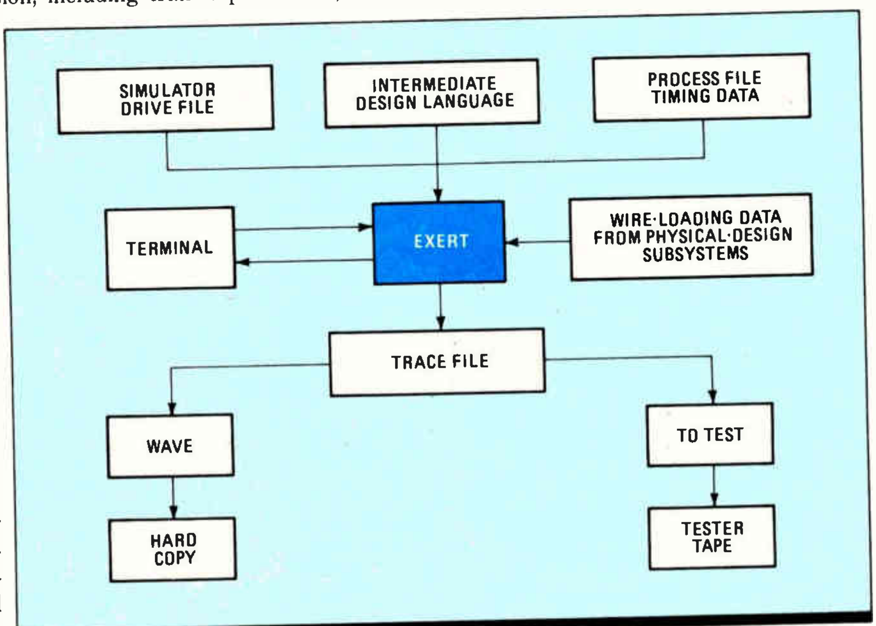
In all three modes, design time is relatively short—under an hour, even with complex arrays. The tradeoff is between die size and yield and the complexity and expense of the different manufacturing processes—single-metal layer personalization for gate arrays versus full processing for optimized arrays and standard cells. The Chipsmith physical-design subsystem will place components and wire them up through the routing channels without any user intervention whatsoever. But certain mechanisms are provided to allow the user to assist or influence placement and routing. In this way, the designer can interact with the design to affect the size, cost, and performance of the final chip. The sheer speed of the layout system allows the designer to try out design variants without incurring an unacceptable time overhead in using the manual options.

One instance where it is desirable to have control over the placement of components in the final design is in accommodating critical signals in a design. In the Model program describing a circuit, certain nets—clock signals for example—can be designated as critical. Such nets are then given priority by the routing program and are wired up before noncritical nets, thus getting the best available wiring paths.

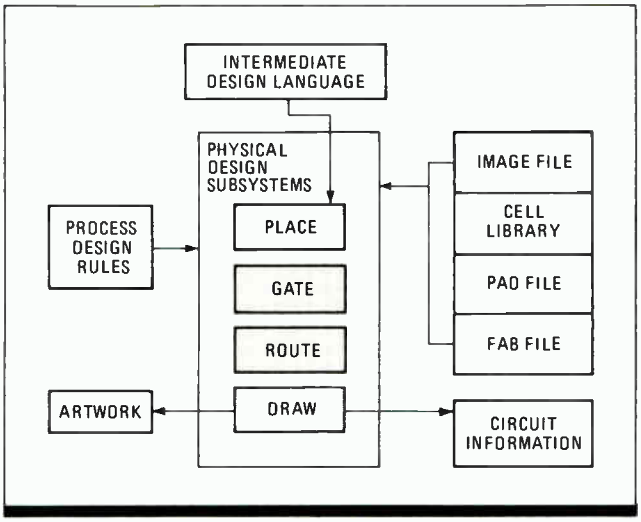
An optional method that affects layout directly is manual placement, which lets the user position part instances be-




**2. COMPONENTS.** The netlist of transistors and interconnections forms the data base for the simulator and physical-design subsystem.




**3. SIMULATION.** The simulator uses stimulus patterns to verify circuit operation and produce test vectors. Vectors and the circuit description form a test program for an LSI tester.




**4. PHYSICAL DESIGN.** The netlist is combined with process design rules to create the artwork needed by a silicon foundry.

fore any automatic placement occurs or rearrange instances after initial placement. Either option allows the designer to experiment with what-if placements and see their effects on the final chip. In particular, the effects of alternate placements after routing can be determined to ascertain optimum channel densities.

Manual intervention can be used during routing to influence the paths that selected nets take between an array's routing channels. Wiring between adjacent horizontal channels is automatically routed through the poly feedthroughs inherent in the array structure. The manual option allows selected signals to be routed through the vertical channels rather than through the transistor area. These routing options are geared to aid performance—metal's resistance is considerably lower than poly's—but will also have an effect on die size.

The designer can also change the placement of pads around the array's periphery through Model commands. This is useful when specific pinouts are required. Manual pad placement can also be used in "what-if" experiments.

The layout is generated according to the design rules of any target MOS process, the relevant parameters of which are read from and stored in a process file, a machine-readable description of the design rules (Fig. 4). The Chipsmith software is process-independent and can produce artwork to implement designs according to the parameters of any MOS process, provided that the relevant subset of the process design rules in the process file can be read by the simulator and by the physical design subsystem. Process portability is an important spreadsheet option for the design engineer.

Using Chipsmith, the engineer can easily experiment with the design rules of different silicon processes to determine their effects on area, performance, and cost. In this way an engineer can shop around for the best cost on silicon.

One final feature of the physical design subsystem is that it allows back-annotation to the simulator of the loads and wire lengths for each net in the design. This allows simulation of the actual silicon layout using the characteristics of the target process to yield more accurate timing estimates than would be otherwise possible. □

## HOW THE PC SILICON COMPILER ARRIVED TWO YEARS FASTER

**The Silicon Compiler Spreadsheet** began life as a project code-named Ace shortly after Alex Bennett joined Lattice Logic Ltd. as president and chief executive officer. "I was sitting with Mike Jenkins [executive vice president of Lattice Logic U.S.A. in Santa Clara, Calif.] in an Edinburgh hotel one weekend, reviewing the performance of the U. S. company and putting together a long-range business plan," he says.

Bennett believed that a packaged system with software on a low-cost platform was still two or three years away. "But Mike had already done his homework," he says.

Says Jenkins, "I had been working on this product for nearly two years on my own. When Alex joined the company, I had a man with the vision to bring it into being."

With the general movement of CAE tools onto lower-cost platforms such as the IBM Corp. Personal Computer AT, Bennett recognized that the window of opportunity was at hand. He could use the hardware to promote software sales and increase the company's credibility in the market.

More to the point, lower-level managers could buy the product without higher management's approval. "The price is within the discretion of the department manager, but the system does not compromise performance or technology for low cost," Jenkins says. He developed the product for designers building circuits in gate arrays or custom chips with 6,000 gates and below.

"Believe it or not, the bulk of design being done in the U. S. today is still 2,500 gates and below," Jenkins says. "Most engineers today are building boxes, and they need a tool that helps realize these designs. We're going after the engineer who wants to replace a printed-circuit board with a piece of silicon."

Lattice's two corporate partners, Ferranti and Cambridge Electronics Industries, asked Bennett to head the company when founders Irene Buchanan and John Gray left to set up the software division of European Silicon Structures, a European custom-chip company. A native Scot with a degree in mechanical engineering from Edinburgh's Heriot Watt University, Bennett was attracted to Lattice Logic because it was an indigenous company with a leading-edge technology product. "I've always been a champion of homegrown companies," he says.

Bennett previously put in 20 years at Ferranti; 10 years at Bourns, where he became director of European operations in France, Scotland, and Ireland; and four with Burr Brown, where he established a new business unit to design products using Scottish engineers.

Jenkins was tapped to run the U. S. operations. In 1970, he was a senior mask designer at Comtec Data Systems Inc. in Rockville, Md. Since then he has set up CAD departments for Paradyne Corp., Largo, Fla., supervised mask layout designers, and started two companies of his own, one of which he sold to CGIS, a Washington communications satellite company.

The second, Independent Resource Corp., had to be closed down in 1985 because Jenkins lacked the venture capital to fund operations. IRC was the exclusive distributor for Lattice Logic at the time, and the Scottish company approached him to head the U. S. subsidiary.

**MIKE JENKINS**

**ALEX BENNETT**

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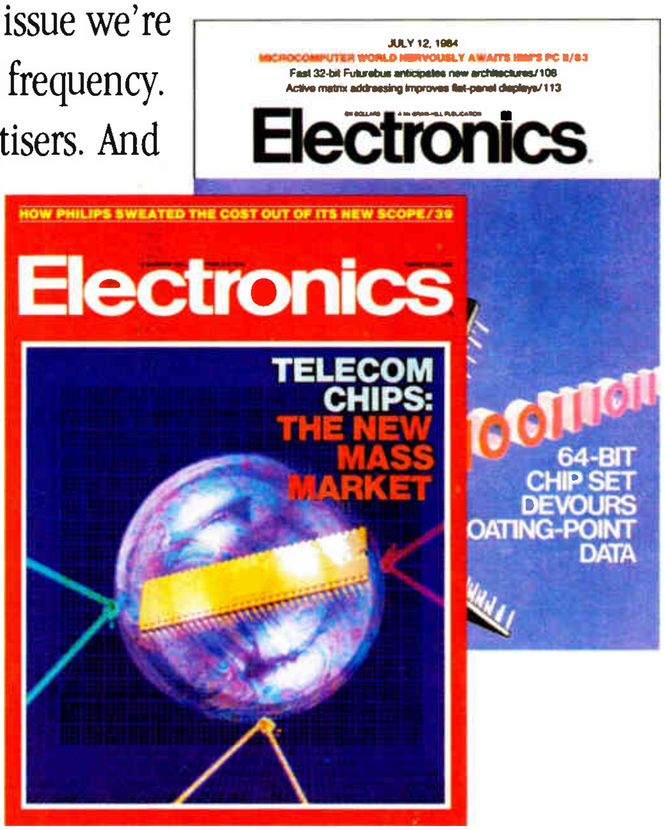



# The job is done.

# OPTOELECTRONICS BUILDS VIABLE NEURAL-NET MEMORY

## COUPLED WITH HIGH-RESOLUTION RADAR, IT YIELDS NEW SMART SENSOR

Efforts to develop artificial neural networks modeled on the brain's highly fault-tolerant, massively parallel computing capability are quickly picking up speed. But researchers trying to build these networks with very large-scale integrated circuits are running into a spate of signal-distribution problems. Now a team at the University of Pennsylvania has taken a big step forward in this work by turning to optoelectronics instead of VLSI to build what chief researcher Nabil H. Farhat calls the first practical artificial neural net.

The Penn researchers were able to avoid the problems that cropped up in an artificial neural network's prodigious interconnections when implemented in silicon. They accomplished this by taking advantage of a simple principle of physics: light multiplexes and integrates through lenses without crosstalk. The team's work goes beyond such a neural network memory; by teaming it with a high-resolution imaging radar—which they developed—they can produce images showing details as small as 50 cm on full-sized aircraft—the highest resolution reported in the unclassified literature.

The Pennsylvania neural-net memory is an optical content-addressable associative memory (CAM), where the elements are searched in parallel by their content rather than by address. The radar and CAM work with a library of aircraft characterizers and need as little as 10% of the radar's full data set to find the closest match to a characterizer and thereby successfully identify a target model aircraft (Fig. 1).

Based on recent laboratory tests, the Penn researchers believe their system should be able to identify an incoming target aircraft at a range of a few hundred kilometers. "Its range is limited only by transmitter power and that will be extended considerably as equipment is developed," Farhat says. In commercial applications, imaging radar operating in the S or X bands with a 0.5-GHz bandwidth could prove useful for a variety of near-airport tasks, such as telling a pilot if his landing gear has been deployed.

The system will not be limited to interrogating large objects, however. When upgraded to operate in the 60- to 100-GHz bandwidth, it will be able to discern millimeter-sized detail at a range of several meters through many opaque materials. Such a capability makes the nondestructive evaluation of microwave-penetrable materials a natural application, Farhat says.

Over the past few years, theorists have taken giant strides in describing how a simple neural network might process information. But attempts to implement neural nets in VLSI circuitry have been mired in the maze of complex signal-distribution and interconnection problems among the many artificial neurons. For example, scientists at AT&T Bell Laboratories who are grappling with these problems in VLSI are making progress, according to a representative, but they have yet to engineer a solution they are willing to discuss publicly.

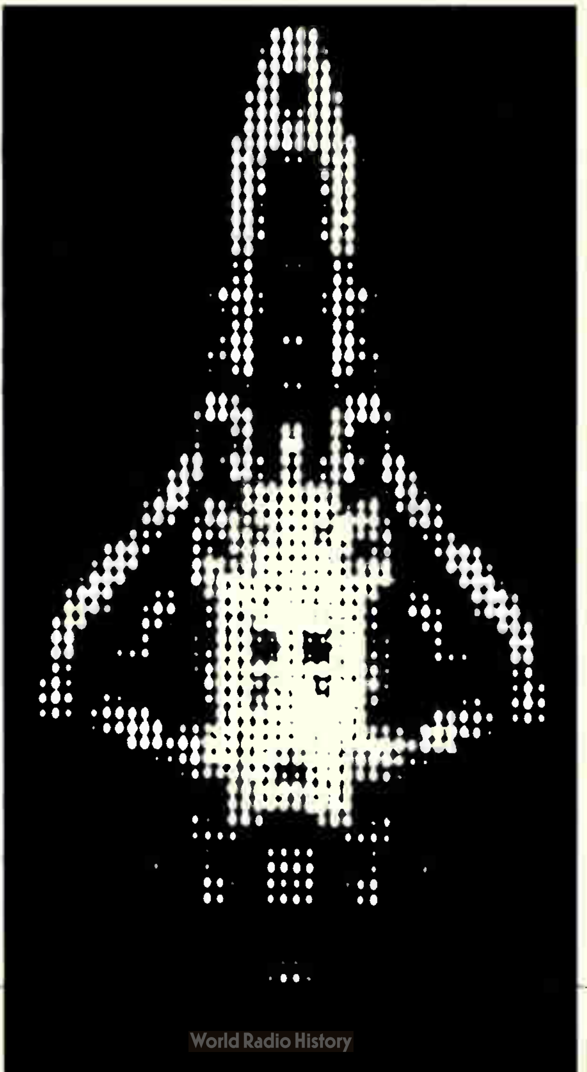
### TWO DECADES OF RESEARCH

The need for a powerful parallel processor grew out of two decades of research at Penn into imaging radar. Farhat, zeroing in on his goal of near-visual-quality images, knew that real-time data generated for nearest-neighbor image searches would overwhelm all but the most powerful serial computers. A visit to the Jet Propulsion Laboratory, Pasadena, Calif., in 1983 introduced him to the neural-network concept, which resulted in lab versions of the CAM. The CAM can pare and interpret the flood of real-time data from the radar.

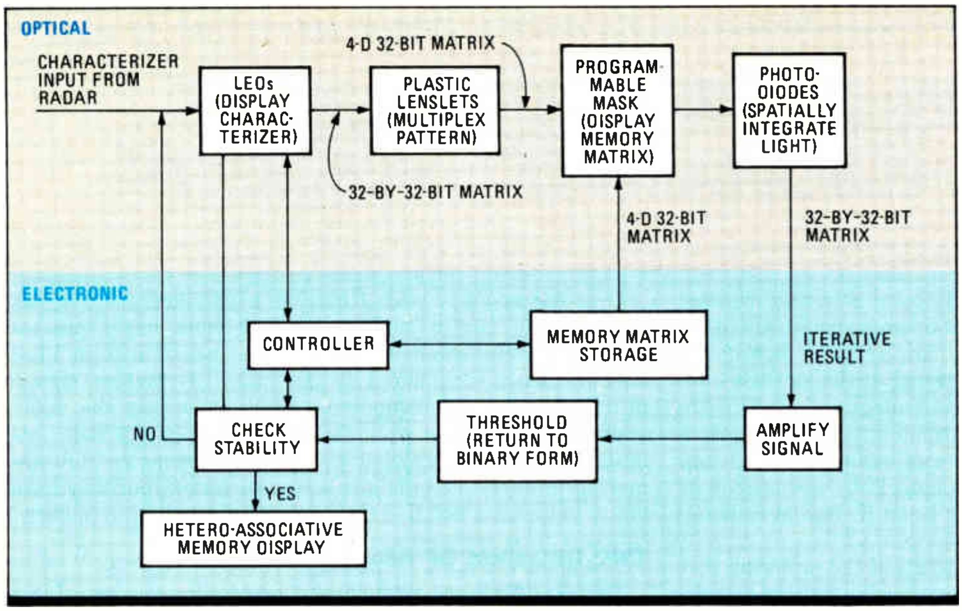
Dovetailing imaging radar and optical-memory technology and refining the CAM are the tasks at hand in Penn's lab. Although Farhat will not speculate on a commercialization time line, he is confident the CAM can be transferred from the lab to an optoelectronic circuit with present-day fabrication technologies. The CAM has uses in a wide spectrum of image-identification tasks, he says, especially those plagued by substantial amounts of missing or incorrect data.

Using off-the-shelf hardware such as light-emitting diodes, magneto-optic spatial light modulators, anamorphic lenses, photodiodes, and an electronic nonlinear feedback loop, Farhat's team of graduate students is probing the limits of the CAM's associative powers. In several tests, it has identified a scale-model aircraft from 10% of the full data set used to characterize the model aircraft with the high-resolution radar. Under real-world conditions, the memory will have to deal with spurious data from target vibration and wind buffeting, but Farhat expects its fault tolerance to be equal to the task.

The memory's phenomenal fault tolerance and robustness can be traced to a binary-coded memory



**1. RADAR IMAGE.** The optical neural-net memory creates an identifiable space shuttle image from limited data.




**2. BIG FIVE.** The five major subsystems in the optical neural memory are 32-by-32-bit arrays of LEDs, lenslets, photodiodes, a digital memory device, and a medium upon which to record the memory matrix mask.

matrix that attempts to mimic the synaptic connections in a simple biological neural network. The memory matrix is computed from the Hopfield algorithm, which is the basis for all neural-network-memory implementations. In its simplest form, the algorithm creates a two-dimensional memory matrix from a library of one-dimensional binary inputs known as characterizers. For practical image-identification problems, Farhat uses 2-d characterizers that expand to 4-d memory matrices.

Given a library of binary-coded characterizers each having n bits, the algorithm begins by taking the first characterizer and computing a simple numerical relationship between each bit and the remaining n–1 bits. This yields an expression of $n^2$ bits arranged in a matrix twice the dimensions of the input characterizer's matrix. The same operation is performed for each characterizer, with each result summed in the memory matrix's relevant position to create a decimal expression. After the algorithm has churned through the entire library of characterizers, it "clips" each matrix element—that is, it sets any positive numbers to one and any zeroes or negative numbers to zero—to return the matrix to binary form. As a finishing touch, the memory matrix's self-products are set to zero. This satisfies the algorithm's recipe—and the intuitive deduction that in this simplified model neurons do not communicate with themselves.

Once the memory matrix is created, the CAM can begin the real work of identifying objects through nearest-neighbor searches. These nearest-neighbor image searches are not conducted in the serial, bit-by-bit progressions used by a conventional recognition scheme. Edge enhancement plays a role in the identification process, but it is a derivative of the radar—not of data manipulation within the CAM. Edge-enhanced information about the target is formatted into a 2-d matrix, which forms the target's characterizer. The memory begins its search by multiplying the 4-d memory matrix by this 2-d characterizer. Then the 4-d result is reduced to a 2-d first approximation by summing array elements according to the Hopfield algorithm. This yields a decimal result that is clipped and fed back to the algorithm. The iteration ends when the result stabilizes—usually in two to four iterations—on a version very close to one of the library characterizers. When the CAM does not have enough information for a successful search, the result may oscillate between two characterizers.

Although minimum matrix dimensions for library characterizers will depend on identification tasks, Farhat says a 32-by-32-bit matrix should be large enough for most radar applications. Nevertheless, calculations inherent in a library of 32-by-32-bit characterizers would challenge most serial computers.

It is the massively parallel computing capability of an optical search that makes Penn's CAM shine. Data throughputs will most likely be limited initially by the cycling capabilities of magneto-optic light modulators used as the programmable masks that display the memory matrix. Farhat expects to meet his near-term goal of reprogramming the masks at 1,000 frames per second. Using 32 masks in parallel, each displaying a 32-by-32-bit matrix, yields a throughput of about 3.2 million bits per second.

The extensive interrelationships created by the algorithm give a sense of the memory's ability to fill in missing data. Explaining the CAM's ability to compute an accurate approximation of one particular library characterizer is not as easy. Neural-network theorists generally return to the analogy of the neuron's state as firing or not firing (on or off). Each characterizer, then, is equal to a stable energy state for the memory matrix. When excited by partial information, the matrix comes to rest at or near the closest stable energy state of the input.

The precise commercial architecture for an optical CAM is still to be determined but will probably include two major functional systems—one to create the memory matrix, the other for nearest-neighbor searches.

## FIVE MAJOR SUBSYSTEMS

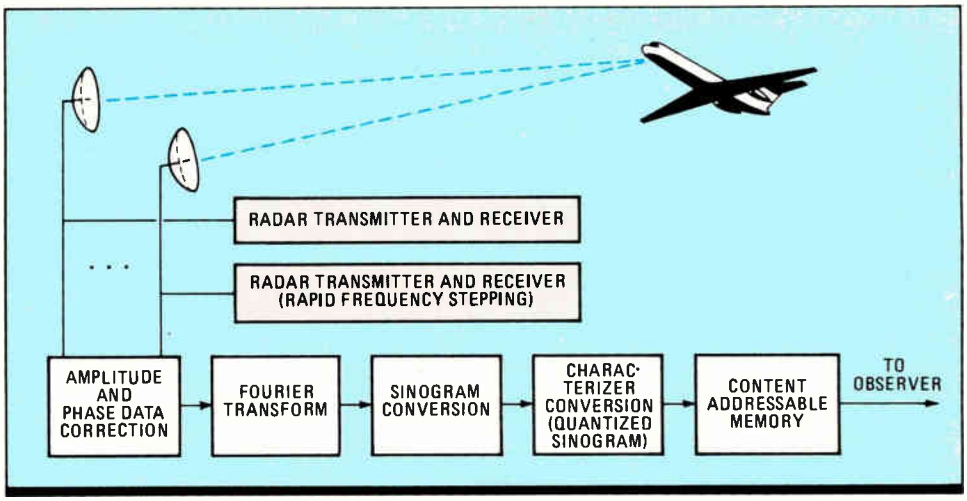
To create and store a memory matrix from a series of library characterizers consisting of a 32-by-32-bit array of data points, an optoelectronic processor would consist of five major subsystems (Fig. 2):

- A single-chip, 32-by-32-bit array of GaAs LEDs for the display of each characterizer pattern.
- A 32-by-32-bit array of molded plastic anamorphic lenslets to multiplex the displayed pattern.
- A 32-by-32-bit photodiode array to record the output of the memory mask and integrate the result.
- A digital memory device to drive the LED display with characterizers. When the programmable mask is implemented, another memory unit will be used to store the memory matrix.
- In a primitive version, photographic transparency film on which the memory matrix mask is recorded. Eventually, programmable, nonvolatile, magneto-optic spatial light modulators will be used for real-time operation.

To create a memory matrix, a library characterizer is displayed on the LED array. Lenslets serially multiplex the image (all but one lenslet is covered at a time). The multiplexed image interacts with the mask programmed to the represent the characterizer. The result recorded by the photodiode represents the first submatrix. The same procedure is followed for each lenslet. The results from each characterizer are summed in the matrix but finally clipped.

Nearest-neighbor searches require the addition of more electronic components. The two most notable are an array of masks, so the memory can be displayed in its entirety, and a nonlinear feedback loop to amplify multiplexed optical signals attenuated in the iterative cycles. Other circuits address the memory matrix and monitor the stability of the iterative result. During the search, the target's characterizer is multiplexed simultaneously by the entire lenslet array to interact with the complete memory matrix. Single photodiodes positioned behind the masks integrate the light, which, when clipped, yields a 32-by-32-bit iterative result.

Once the CAM stabilizes, it still has to interpret the result in terms of one of the library characterizers. There will seldom be an exact match. In a remarkably clever solution, Farhat has utilized the human observer's ability to recognize a less-than-perfect image. In addition to creating homo-associative memories—relationships of the information with itself—the CAM can form a hetero-associative memory. This means it can relate the same information to another image on the screen, such as an alphanumeric expression. In other words, the system output displayed on a cathode-ray tube is an imperfect four-character code for the object being identified—but something a technician can interpret nonetheless.




**3. GRABBING AN IMAGE.** The University of Pennsylvannia's highest-resolution imaging radar steps across a range of frequencies to provide data to the CAM for generating the final image.

The CAM's ability to zero in on a target depends on the memory matrix's size and the number of characterizers that the matrix incorporates. For a 32-by-32-bit matrix, the CAM has a near-100% probability of stabilizing on a hit if the library consists of 30 or fewer characterizers, says Farhat. Though fewer than the hundreds needed for a library of characterizers to identify military and commercial aircraft, it is not a limitation. The CAM simply loads the first 30 into the memory matrix. If it doesn't succeed with that matrix, it loads additional sets.

As robust as the CAM is, to meet the needs of its intended applications in aircraft image identification, robotics, and a variety of other recognition tasks, it requires relatively precise images drawn by smart sensors that eliminate unimportant information. By harnessing an innovative combination of frequency diversity, holography, and Fourier analysis, Farhat hurdled three persistent problems besetting imaging radar: enormous aperture size (and its correspondingly high cost), noise, and image orientation.

The high resolution of Farhat's imaging radar is itself a breakthrough, achieved by a combination of frequency diversity, polarization, and multiple views of the target. His chief innovation is wavelength diversity—stepping across a range of frequencies and using different polarizations (Fig. 3). Fourier analysis turns that data into the mathematical equivalent of the impulse response of the target.

Edge enhancement is a natural by-product of microwave frequencies and the scattering mechanism of the target. "The radar produces a primal sketch of the object," says Farhat. "Edges are enhanced and information about the object's flat parts is discarded because most of the radiation that hits a smooth surface scatters forward. In contrast, in the optical regime I would see the entire object because the surface is very rough compared to the wavelength."

To obtain a 2-d image, the radar must view its target from more than one aspect angle, or look. "Each look gives one frequency response," says Farhat. "When we perform a Fourier transform on that, we get the equivalent range profile. By repeating the measurement for many looks and putting the frequency responses one next to the other in polar format, we get a Fourier space slice." The system's tomographic capa-

LIBRARY WORDS (4 BY 20 BITS)

| A | B | C | D |
|---|---|---|---|
| 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 |

MEMORY MATRIX (20 BY 20 WORDS)

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | -2 | 0 | -2 | -2 | 2 | 0 | 2 | 0 | 4 | 0 | 4 | 0 | 0 | -2 | 2 | 2 | 0 | -4 | 0 |
| -2 | 0 | -2 | 0 | 0 | 0 | -2 | 0 | 2 | -2 | -2 | -2 | 2 | -2 | 4 | 0 | 0 | 2 | 2 | -2 |
| 0 | -2 | 0 | 2 | -2 | 2 | 4 | -2 | 0 | 0 | 4 | 0 | -4 | 0 | -2 | -2 | 2 | 0 | 0 | 0 |
| -2 | 0 | 2 | 0 | 0 | 0 | 2 | 0 | -2 | -2 | 2 | -2 | -2 | 2 | 0 | -4 | 0 | -2 | 2 | 2 |
| -2 | 0 | -2 | 0 | 0 | -4 | -2 | 0 | -2 | -2 | -2 | -2 | 2 | 2 | 0 | 0 | -4 | -2 | 2 | 2 |
| 2 | 0 | 2 | 0 | -4 | 0 | 2 | 0 | 2 | 2 | 2 | 2 | 2 | 2 | 0 | 0 | 4 | 2 | -2 | -2 |
| 0 | -2 | 4 | 2 | -2 | 2 | 0 | -2 | 0 | 0 | 4 | 0 | -4 | 0 | -2 | -2 | 2 | 0 | 0 | 0 |
| 2 | 0 | -2 | 0 | 0 | 0 | -2 | 0 | -2 | -2 | 2 | 2 | 2 | 2 | 0 | 0 | 0 | -2 | -2 | 2 |
| 0 | 2 | 0 | -2 | -2 | 2 | 0 | -2 | 0 | 0 | 0 | 0 | 0 | -4 | 2 | 2 | 2 | 4 | 0 | -4 |
| 4 | -2 | 0 | -2 | -2 | 2 | 0 | 2 | 0 | 0 | 0 | 4 | 0 | 0 | -2 | 2 | 2 | 0 | -4 | 0 |
| 0 | -2 | 4 | 2 | -2 | 2 | 4 | -2 | 0 | 0 | 0 | 0 | -4 | 0 | -2 | -2 | 2 | 0 | 0 | 0 |
| 4 | -2 | 0 | -2 | -2 | 2 | 0 | 2 | 0 | 4 | 0 | 0 | 0 | 0 | -2 | 2 | 2 | 0 | -4 | 0 |
| 0 | 2 | -4 | -2 | 2 | -2 | -4 | 2 | 0 | 0 | -4 | 0 | 0 | 0 | 2 | 2 | -2 | 0 | 0 | 0 |
| 0 | -2 | 0 | 2 | 2 | -2 | 0 | 2 | -4 | 0 | 0 | 0 | 0 | 0 | -2 | -2 | -2 | -4 | 0 | 4 |
| -2 | 4 | -2 | 0 | 0 | 0 | -2 | 0 | 2 | -2 | -2 | -2 | 2 | -2 | 0 | 0 | 0 | 2 | 2 | -2 |
| 2 | 0 | -2 | -4 | 0 | 0 | -2 | 0 | 2 | 2 | -2 | 2 | 2 | -2 | 0 | 0 | 0 | 2 | -2 | -2 |
| 2 | 0 | 2 | 0 | -4 | 4 | 2 | 0 | 2 | 2 | 2 | 2 | -2 | -2 | 0 | 0 | 0 | 2 | -2 | -2 |
| 0 | 2 | 0 | -2 | -2 | 2 | 0 | -2 | 4 | 0 | 0 | 0 | 0 | -4 | 2 | 2 | 2 | 0 | 0 | -4 |
| -4 | 2 | 0 | 2 | 2 | -2 | 0 | -2 | 0 | -4 | 0 | -4 | 0 | 0 | 2 | -2 | -2 | 0 | 0 | 0 |
| 0 | -2 | 0 | 2 | 2 | -2 | 0 | 2 | -4 | 0 | 0 | 0 | 0 | 4 | -2 | -2 | -2 | -4 | 0 | 0 |

RECOVERY FROM PARTIAL INPUT

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PARTIAL INPUT OF D |
| -2 | -4 | 6 | 4 | -8 | 4 | 6 | -4 | 2 | -2 | 10 | -2 | -10 | -2 | 0 | -8 | 8 | 2 | 2 | -2 | FIRST ESTIMATE } FIRST ITERATION |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | FIRST THRESHOLDING } FIRST ITERATION |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | SECOND ITERATION |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | THIRD ITERATION — STABLE |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | FOURTH ITERATION |

**4. ROBUST.** The CAM's ability to fill in missing information is illustrated by setting the last 12 bits of library word D to zero. After only four iterations, the CAM found the correct word in a library of four.

bility makes it possible to produce a near-visual-quality projection image from any Fourier slice of the object, even though the radar's looks are from a variety of slant angles. "If you've looked at a target from head on to broadside, which is 90°, you've probably characterized it totally because aircraft are symmetrical," says Farhat. "You might argue that you have to look at it from the rear, but in most cases you aren't interested on identifying something that left you. We store 90° characterizers in memory—60° would be enough, but we're looking at 90°."

Visual representation of the projection image does not provide the best CAM characterizers. Range profile data can also yield sinograms—sinosoidal traces that produce a more distinctive signature. The research team currently constructs characterizers from sinograms; but options such as polarization are worthy of consideration and are being studied, says Farhat.

The imaging radar is closer to commercial implementation than the CAM. Existing radar technology operating between 300 and 500 MHz in 3-MHz steps could be adapted to achieve 30- to 50-cm resolution, says Farhat. "What would be required would be precise, rapid frequency stepping to acquire the data. But using our laboratory equipment and the proper radio-frequency amplifiers, you could set up such a system." Several radar tracking stations would independently measure the target's frequency response from different directions. The data would be transferred to a central computer bank and corrected for phase differences to access a slice in the target's Fourier space.

About 200 frequency steps and 500 looks within a 90° azimuthal angle would generate a complete high-resolution image for a 50-m aircraft. The number of looks is determined by the target's size: the larger the target, the more looks are required. But this does not mandate a system of 500 discrete sensors distributed around the target. First, the aircraft's motion allows each sensor to address the target at more than one angle. Second, the CAM's sinogram-derived associative memory can be counted upon to fill large blocks of missing information (Fig. 4). Using actual radar-retrieved data of a model airplane, the CAM (simulated on a computer because the optical version has not attained a 32-by-32-bit array size) has identified the target with as few as 12 looks when 128 looks and 128 frequency steps were used to create the library characterizers.

Having coaxed the imaging-radar system through research to the verge of development, Farhat has two remaining goals: achieving millimeter-level image resolution in the laboratory and refining the optical CAM to process the radar data in real-time.

A Department of Defense University Research Instrumentation Grant is funding a major upgrading of the radar laboratory to add equipment for millimeter-level image resolution, scheduled for completion this fall. It will facilitate frequency stepping as high as 60 GHz and enable the study of such real-world problems as target vibration.

Another advantage is economic: millimeter resolution will give researchers the ability to characterize full-sized aircraft from detailed models in the laboratory, says Farhat.

The CAM technology must be upgraded in two key areas to mesh with the radar for real-time operation. Using a simple 5-by-5-bit neural network, researchers have finished ironing out the generic wrinkles of optoelectronic CAMs. Next they will implement a 16-by-16-bit neural network; within a year, Farhat expects to be using 32-by-32-bit sinogram characterizers derived from five target aircraft models available in the radar lab. "At that point, we will want to find out how well it recognizes the models on a statistical basis from any aspect angle," he says. Computer simulations indicate the 32-by-32-bit optical CAM might make do with 10% of the total characterizer data.

### MOVING TO A MASK

In principle, moving from the present technique of storing interconnection data on transparent photographic film to a programmable mask should not pose serious difficulties, says Farhat. Litton Industries, Van Nuys, Calif., markets 48-by-48-bit magneto-optic spatial light modulators that can be used as the storage mechanism for 1-d neural networks, he says, and adapting the system to a 2-d neural network is a relatively simple matter of partitioning the 4-d memory matrix into 2-d components.

Over the long-term, the CAM could have an impact on such technologies as robotics, machine vision, artificial intelligence, and supercomputers. Recognition schemes could include ultrasound, colors, textures, infrared, and—perhaps the CAM's first commercial application—speech processing. Coupled with the imaging radar's smart sensing of primal images, the research will prove fruitful in gaining insights into imaging as a whole, including the eye-brain system, says Farhat. □

## TAKING LESSONS FROM MOTHER NATURE

**For more than** 20 years, Nabil H. Farhat has been extracting images through opaque media with constantly improving results. Beginning with microwave holography in 1964, he and his ever-changing team of University of Pennsylvania graduate students managed by 1969 to derive fuzzy holographic views of concealed objects such as a handgun in a suitcase. Though the images were impressive, his research convinced him that single-wavelength holography was stuck with the inherent limitations of speckle noise, range, and cost.

Turning to nature, Farhat reasoned that if bats and dolphins can resolve their environment with great precision using multifrequency clicks and chirps, then spectral diversity might also provide a key for high-resolution radar imaging.

From the project's holographic beginnings, Farhat was constantly on the lookout for a hybrid optical and

**FARHAT:** The clue came from bats and dolphins.

electronic system for real-time data processing. While on a sabbatical trip to the California Institute of Technology in 1983, Farhat visited the Jet Propulsion Laboratory and became intrigued by the work in associative memory and neural networks that was being done by John Lamb and his colleagues. "They handed me a paper on the Hopfield model [an algorithm developed by John J. Hopfield], and everything fit together," he recalls. "It was perfect, especially for an optical model."

A week later, he discovered that Caltech's Demetri Psaltis had similar interests. "We put our heads together and wrote a paper drawing the optical community's attention to how well neural networks dovetail with optics." In the human brain, individual neurons can become inoperative without damaging the neural network's integrity—a highly desirable trait for computer or imaging systems that must function for extended periods, as on future space missions that could last 50 to 100 years.

Together, imaging radar and associative memory have numerous applications from determining the condition of heat-resistant panels on the space shuttle to checking rush-hour traffic conditions around New York. Yes, Farhat says, a representative of New York's Port Authority has already contacted him.


FEW REMEMBER
WHO WAS SECOND
ON THE MOON...
OR SECOND
IN THE MARKET...

# AT&T DOESN'T THE MOON...JUST AT BEING FIRST

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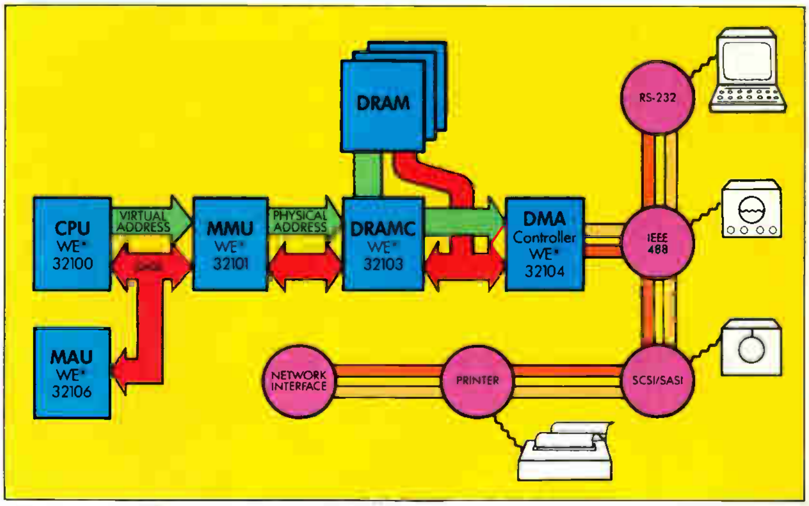


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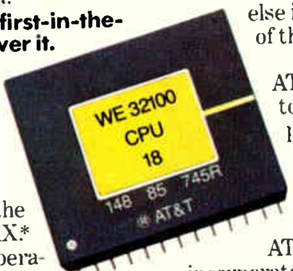


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# THE MINICOMPUTER IS DEAD! LONG LIVE THE MINICOMPUTER!

## TRADITIONAL MINI MAY BE DISAPPEARING, BUT ITS DESCENDENTS FLOURISH

*By Tom Manuel*

Reports of the death of the minicomputer are greatly exaggerated. While the traditional mini may not be with us all that much longer—thanks to the surging microcomputer—its descendents, the midrange or department-level machines, live on stronger than ever. Still positioned between the mainframe and personal computer in performance and price, the mini is now being driven by some of the most significant research and development going on in the computer industry.

This new mini is turning out to be a gang of powerful 32-bit multiuser, multiprocessor systems, and even includes parallel machines. Starting to fall under the mini classification are such categories as parallel computer, reduced-instruction-set computer (RISC), supermicrocomputer, and minisupercomputer, which are all moving from their original niche markets into general-purpose computing. These models are doing a lot now to broaden and blur just exactly what a mini is.

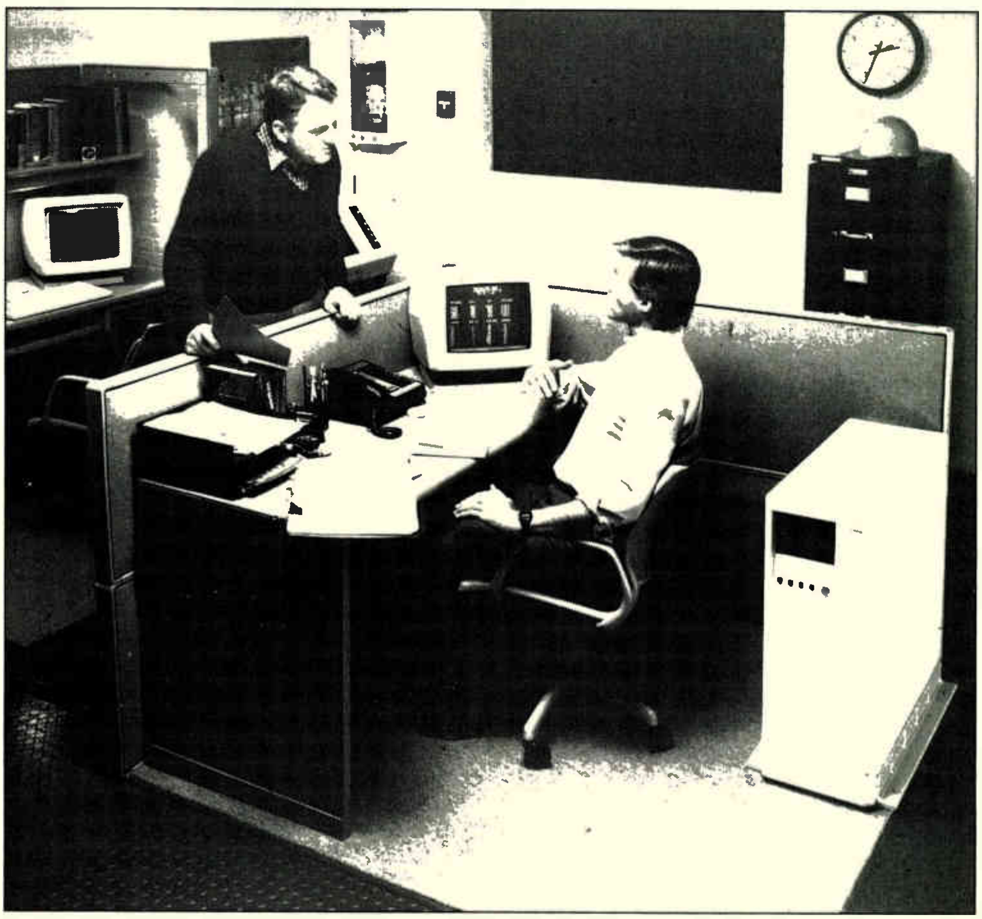
Yet the minicomputer never was a very precise term. In fact, the first true personal computer was the mini. Born in the early 1960s, 8-bit models selling for less than $25,000 turned out to be low enough in price that many people bought a computer for the first time to do a single, specific job. The mini was embedded into such specialized applications as control systems, flight simulators, and laboratory and medical instrumentation. During the 1970s, the mini market became the fastest-growing part of the entire computer business. The 8-bit models were joined by 16-bit machines, and their "bang-for-the-buck" soared as power soared and prices declined.

With the advent of increasingly complex integrated circuits and higher-capacity disk drives, minis started closing in on small mainframes. The more powerful 32-bit superminis arrived and spurred the evolution of general-purpose departmental computers to greater performance that could handle far more users.

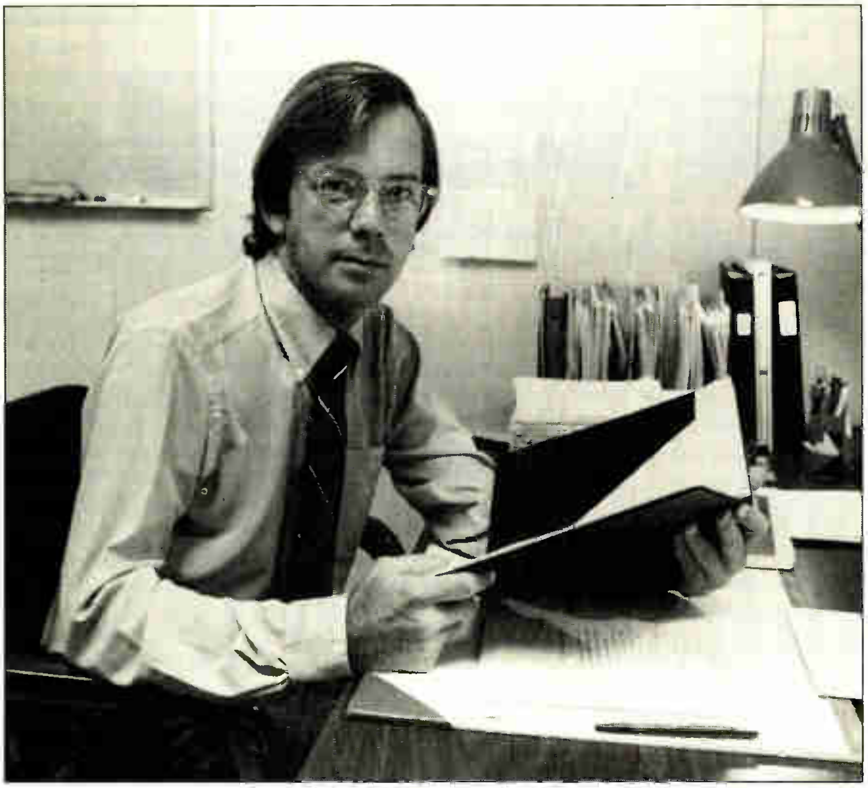
In the 1980s, industry pundits started sounding the death knell for the traditional 8-bit and 16-bit minis when powerful microprocessor chips made possible microcomputers with even greater price/performance benefits. With the traditional single-processor, multiuser minicomputer beginning to become far less important, minicomputer needs a broader definition. One that seems to fit the bill is a midrange multiuser computer system that in performance and cost falls between single-user computers—including personal computers and work stations—and the big corporate mainframes.

At the personal-computer and work-station level, the user is an individual. Midrange computer systems can be called departmental computers or servers—especially when they are positioned in a network of work stations and personal computers. The top tier, mainframes, is used primarily at the corporate level. Typically, a management-information-systems department uses these machines to do the data processing for an entire organization. Mainframes are often centralized in one big computer center, and frequently they share one giant data base containing a company's key business information.

The millions of personal computers now pouring into business have generated a new role for the midrange computer. Because personal computer users are clamoring for access to corporate data, the trend is to use midrange computers as intermediaries to provide controlled access to corporate data. In



**1. FOR THE GROUP.** Departmental computers are coming on strong for use by groups of workers. An example is this Prime model 2450 low-end departmental computer for office functions in manufacturing.



**2. A TRADITIONALIST.** Tom West, Data General Corp.'s Systems Group vice president, a well-known computer designer and engineer, defends the traditional views on minicomputers.

AT serves as both the front end for the Series/1 and as a personal computer, sells for $10,695.

New vendors and new applications are only two aspects of the shakeup that is facing the traditional proprietary-processor mini and its makers. Even more important, technology advances are moving in fast. Parallel computers and a new class of number crunchers, called mini-supercomputers, are beginning to apply pressure at the high end of the performance range, while RISC architecture principles could soon influence the way many midrange computers are designed. At the low end, meanwhile, microprocessors are applying pressure.

Makers of midrange machines also must come to terms with the impact of developments in artificial intelligence and in vector processing. AI—or, the more general term, symbolic processing—will be the main vehicle for providing much better user interfaces to computer applications. The midrange computer makers will have to determine how to fit symbolic processing into their future systems, whether through symbolic coprocessors or by some other means. In addition, many midrange applications require increasing amounts of fast numerical processing, and one way to provide it for many applications is through vector processing. Again, midrange system makers must decide how to incorporate vector processing into their systems. And further down the road, the most advanced midrange systems will probably include both symbolic and vector processing.

many cases, a midrange computer also serves the functions of departmental computers—doing computation unique to a particular department and performing as data-base, computational, and communications servers for the personal work stations.

The upshot is that departmental computers allow work groups and departments to access resources richer and more powerful than personal computers and work stations (Fig. 1). "Now we can organize computers the way we organize people," says Guy A. Daniello, president of Datamedia Corp., a Nashua, N. H., vendor of departmental computer systems based on 32-bit microprocessors. "This three-tier structure has only recently been made economically possible," says Daniello, a veteran of the computer industry. "It is where the technology is taking us. It allows us to draw the computer organization chart like the people organization chart."

Digital Equipment Corp., the inventor of the minicomputer, has kept up with, and often led, the many changes that minicomputers have gone through over the past 25 years. The Maynard, Mass., company still remains the leading vendor of traditional minis. But if the definition is expanded to include all computers that lie between personal computers and mainframes, then another leader emerges—IBM Corp. The company has sold hundreds of thousands of its various midrange computer systems—100,000 of the System/36 alone. Under the broader definition, IBM's midrange lines also include the Series/1, Systems 3, 7, 34, and 38, and, to really stretch the definition of midrange, even the 4300 series.

*Parallel computers are easier to expand than typical midrange systems*

An example of the aggressiveness IBM is showing in the midrange field is the three new models of the Series/1 line, introduced early this month along with new peripherals and software. One of the new models is the desktop 5170 model 496. This system combines a board containing a Series/1 microprocessor and 1 megabyte of memory with the newest IBM Personal Computer AT, the model 339 with a 30-megabyte hard-disk drive. This integrated system, in which the PC

Not surprisingly, there are two viewpoints on the impact of new technologies on midrange computers. People associated with the traditional minicomputer companies hold a rather conservative view. They do not see machines built with these new technologies quickly dominating the mainstream of midrange computing. These designers, however, do generally concede that the new technologies are significantly influencing their businesses.

The other camp consists of representatives of newer companies that are offering parallel computers, RISC machines, and supermicrocomputers. The designers of such machines are, of course, sure that their technologies will soon dominate the midrange market.

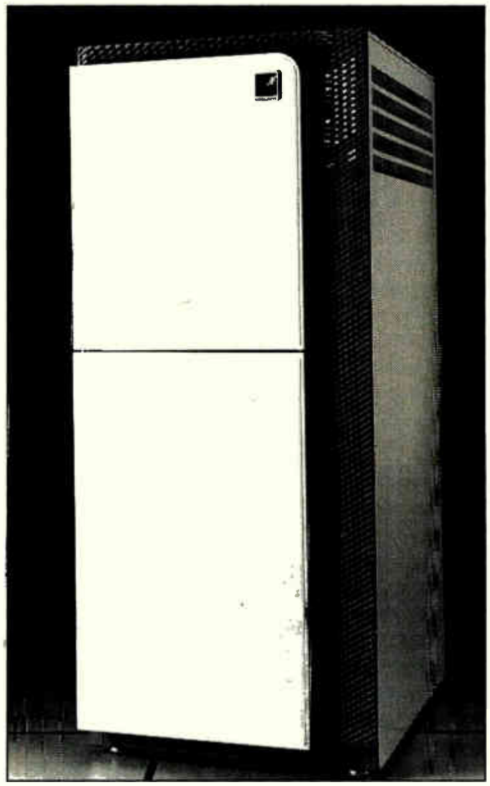
One strong defender of the traditional view is Tom West, vice president of the Systems Group at Data General Corp., Westboro, Mass. (Fig. 2). "There are a couple of new mousetraps out there—parallel and RISC. At least, they are the ones you hear the most about," says West. Parallel machines are still too experimental to present a serious threat to the mainstream mini market, he maintains. "Parallel machines are really in their infancy. They are going into niche markets now—such things as modeling large systems, the Strategic Defense Initiative, weather forecasting, and particle physics."

At Prime Computer Inc., Natick, Mass., Walter A. Jones, director of central processor development, also sees parallel computers as being on the fringe. "We have looked at the whole spectrum of parallel computing, and one thing that stands out clearly is that it's very application-specific now—parallel computers don't fit in the mainstream of computing."

Some experts believe that parallel architectures will expand into some of the larger markets for general-purpose computers, including those for midrange machines. West agrees that this could happen but says it will take a while. "Many people are looking at them [parallel architectures]—Data General certainly is," says West.

One industry figure who believes that parallel processing has already infiltrated mainstream computing in both technical and commercial applications is Casey Powell, president of Sequent Computers Inc., Beaverton, Ore. Sequent has over 70 installations of its Balance 8000 and Balance 21000 parallel-computer systems (Fig. 3), many doing mainstream applications.

Another vendor that has been offering parallel computers for several years is Concurrent Computer Corp., the former Data Systems Division of Perkin-Elmer Corp. Virgil Hornstein, senior manager of high-performance systems at Concurrent in Tinton Falls, N. J., says that parallel machines are going to take over in the midrange world. "In the next three to five years, there won't be too many uniprocessor machines," says Hornstein. The parallel machines will be a mixture of types—ranging from pure master/slave arrangements to pure parallel machines such as Concurrent's, he says.



**3. MANY IN ONE.** The Balance 21000 system by Sequent Computers is one of the parallel computers that are starting to seep into the mainstream.

Powell and Hornstein say that the trend toward multiple processors and parallel architectures comes from the need for ever more computing power for increased business and industrial productivity. The multiprocessor trend started a few years ago as the largest mainframes and supercomputers started to add a second, a third, and then a fourth central processing unit.

A very important attribute of parallel computers is their ability to be expanded over what can be called a very wide dynamic range—that is, machines of the same design covering the range from low power to very high power. Unlike the single-processor systems that had to be replaced when more power was needed, parallel computers are simply added to. "The era of the very large, very fast, throwaway uniprocessor is nearly over—or maybe it is over," says Hornstein.

A parallel architecture can satisfy users' demands for a wide dynamic range and for uniformity in operating systems, programming languages, and data communications. Once a company makes a significant investment in application software, it does not want to throw away the old when new technologies present better and faster machines to run them on. Parallel computers are a natural path to increasing the performance of systems incrementally without discarding existing hardware. As Hornstein puts it, "with parallel architectures, you can always add something."

*Will RISC principles influence the design of midrange machines?*

Another trend that figures in the rise of parallel machines is the move to build solutions to problems rather than building machines first and then looking for applications, says Powell. Putting together systems to solve specific problems almost always means that the computing capability must grow over time—more processing power, larger memory, and more, different, or faster I/O devices. "A range of capability is the thing [that users want and need]," says Powell.

By providing a wide dynamic range, parallel computers automatically meet the expansion needs of users. Since the vendors of parallel computers are adopting industry standards for software and communications, they are meeting that user need as well. So if these companies can flourish in the dog-eat-dog world of midrange computers, parallel machines should make inroads into the mainstream.

Though parallel computers may be poised to enter the mainstream, Data General's West believes that RISC is different. "It doesn't seem to be going anywhere," he says. He clearly is not one of the many believers in RISC as a new wave of computer architecture [*Electronics*, May 5, 1986, p. 28]. The goal of RISC, according to West, is better silicon utilization by maximizing the number of instructions per second per square centimeter of silicon. "That may be of no practical interest for general-purpose computer builders," he says. RISC architectures may be able to implement a central processing unit in half as much silicon as other approaches—but the CPU is a very small part of all the silicon in a complete computer system, so, in that context, RISC does not buy the system designer very much. For real savings, "We need to look at factors of 10 in silicon utilization at the system level."

However, he does concede that "RISC is likely to have a role to play in midrange systems such as providing coprocessor accelerators." But he doesn't believe a RISC processor could function as the kernel processor in a system—running the operating system and taking care of the system housekeeping. RISC microprocessors could, however, join the current merchant microprocessors in serving as core processors in work stations and personal computers, he believes.

One of the problems of RISC processors, West holds, is that they do not have any dynamic range in performance. But dynamic range could be achieved in a parallel RISC design where processors are added as needed to hike performance.

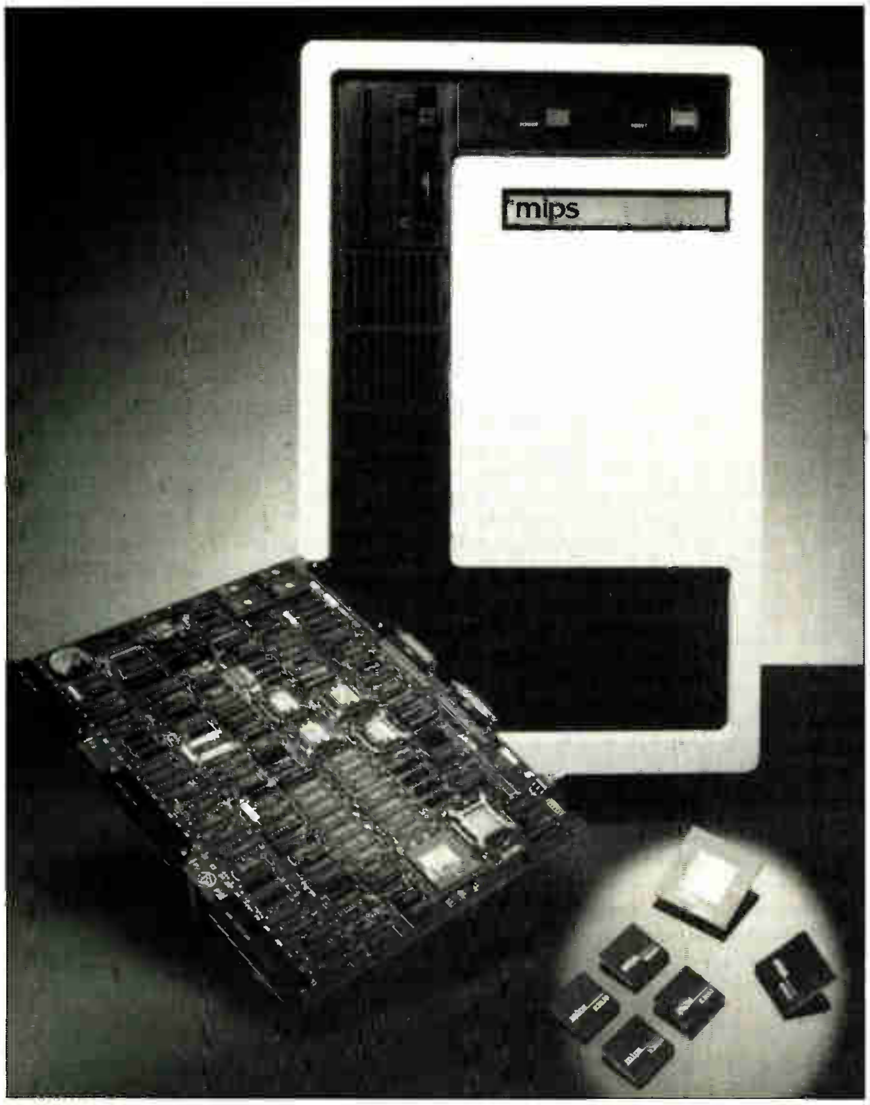
A key concern for the major minicomputer makers is compatibility with existing customer software. "For a company like DG to change program architecture, it would mean scrapping a lot—besides customer software, it would include such vendor software as diagnostic programs and software development tools," says West. So vendors and users are reluctant to change program architecture.

At least one major computer maker sees a way to use RISC principles and still maintain software compatibility. Systems designers at Hewlett-Packard Co. have put a lot of effort into developing a RISC-inspired architecture, called HP Precision Architecture. It will be the basis for the company's future computer systems [*Electronics*, March 3, 1986, p. 39]. The Palo Alto, Calif., company will use it to meld its present disparate lines, the HP 3000 business computers, HP 9000 engineering computers, and HP 1000 technical and manufacturing computers. Some of the new computers will be compatible with existing software, but other users will have to convert programs with HP-supplied conversion aids. None of these RISC-based systems will be delivered before late 1986.

Most computer companies aren't faced with the dilemma of three different computer lines, notes HP president John Young. They needed to be unified because it would be too costly to support and improve three lines. "One of the big benefits of our Precision Architecture is that we have been able to make it a unified, scalable architecture which HP can use to provide customers with completely interchangeable products expandable over a wide range of performance," says Young. "Now we will have just one machine and two operating systems [HP 3000 MPE and HP UX (Unix)] to support."

In contrast to HP's new computers, other RISC machines, like parallel computers, are most likely to be applied first to special applications. One example is the RT Personal Computer from IBM Corp. [*Electronics*, May 5, 1986, p. 34]. This first RISC product from the company that invented the concept is meant to serve the high-performance work-station market—in which the company is just getting started. So IBM doesn't have a lot of user software to worry about.

In another example of a specialized application, Prime Computer is building a work station using the RISC chip set (Fig. 4) recently developed by Mips Computer Systems Inc., Sunnyvale, Calif. [*Electronics*, May 5, 1986, p. 56]. But, says Paul R. Jones, Prime's vice president of hardware development, "We don't see a lot of RISC impact on our 50 series," Prime's mainline multiuser minicomputer family. "We haven't seen anything now nor in our plans for the next several years in our main market that would require us to do anything more with our current architecture because of RISC advances. We have already used the things we think are important."




**4. RISC.** Several reduced-instruction-set-computer products such as the chips, boards, and system from MIPS Computer Systems are ready to enter the midrange computer market.

The RISC principles already applied to the evolving Prime architecture include use of general registers as well as optimizing compilers to use these registers efficiently, according to Walter Jones, Prime's director of central processor development. "We put a new mode on our machines several years ago to make efficient use of the registers," he says. "But we can't go to pure RISC. Our systems also need some complex instructions for the mix of applications that Prime systems address." Prime, like other established companies, must also keep its systems compatible with existing programs.

One new class of midrange machines that is jumping right into the mainstream is the supermicrocomputer. A multitude of companies are building multiuser midrange computers with powerful 32-bit microprocessors such as the Motorola 68020, National 32032, Intel 80286, Fairchild Clipper, and soon the Intel 80386. One very recent example is the DMC/932 2640 multiuser computer (Fig. 5) just announced by Datamedia. Its 2640 can handle up to 32 users doing commercial computing without degradation of system performance, the vendor claims. A microcomputer system with such basic specifications can replace a minicomputer but not the biggest superminis.

For its CPU, the 2640 uses a 16.7-MHz MC68020 processor rated at 2.5 to 3 mips in raw performance. But system performance depends on system features, such as memory speed, memory management techniques, bus speed, and whether buffering, caching, or coprocessors are employed. For example, to match the speed of the processor, the Datamedia system has up to 16 megabytes of 80-ns main memory and a 20-megabyte/s bus. Also, two MC68000 auxiliary processors, which each have half a megabyte of dedicated memory, do communications processing and manage the storage subsystem in parallel with the CPU. All this is available for prices from $28,500 up to low-end mini territory of $50,000.

## USING MERCHANT CHIPS

The traditional minicomputer companies are not scrambling to change their entire product lines because of the onslaught from supermicrocomputers. They are, however, feeling some pressure at the low end of their product lines. One reason both DEC and Data General implemented their 32-bit processors on VLSI chips is to be able to match microsystems in price, performance, and size.

Companies that cannot afford the time nor the money to implement their architecture in VLSI are turning to the merchant microprocessors to beef up the low end of their product lines. Hornstein says, "We are using microprocessors for some low-end products because they do two things for us: first, they make product development easy; and second, they bring the low end up in performance." The microprocessors available today are more powerful and much smaller than the proprietary processors they are replacing in low-end and middle minis. "Microprocessors, gate arrays, and other semicustom chip solutions are the best channels for product development for companies like us as we condense our machines to a few chips on one board," adds Hornstein.

Even the design of high-end midrange machines likely will reflect the impact of supermicrocomputers, especially now that microprocessors soon will hit 6 mips. Sequent's Powell notes that, when minis started catching up, mainframes took a big jump in performance and continued to improve faster than before. Now that microcomputers are biting at the heels of minis, the designers of minis will have to take a new tack on architecture development in order to stay ahead, says Powell. And before they can do that, they will have to discover what that new tack may be.

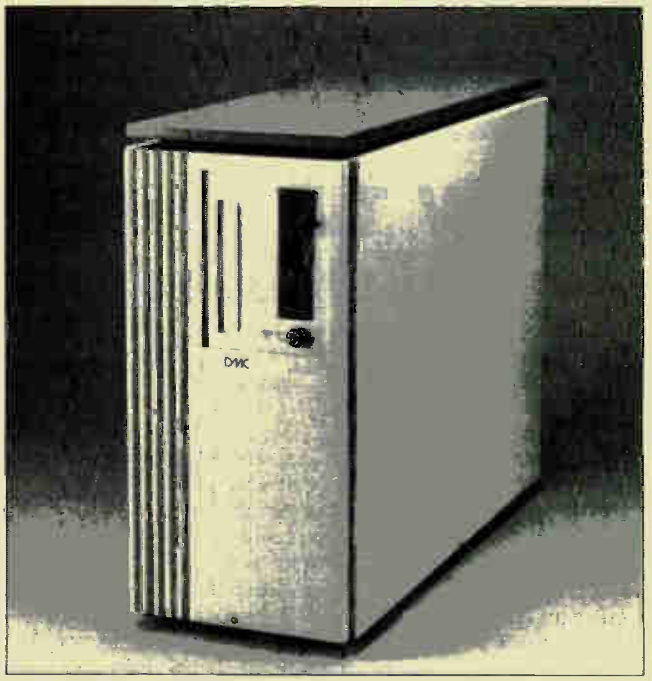
Another way microprocessors are influencing minicomputers is in the move to what Jeffrey S. Burnett, product marketing manager at Masscomp, calls multimicros with coprocessors. In the Westford, Mass., company's systems (Fig. 6), for example, one processor may be dedicated to high-speed real-time data acquisition, while other processors perform other jobs. DEC is also going that way with its top-of-the-line 8000 series of multiprocessor superminis—one CPU may run a real-time kernel and the other will run the VMS operating system. Burnett says the coprocessor trend includes specialized processors for graphics, for communications interfaces for such standards as Ethernet or the Manufacturing Automation Protocol, and for running multiple operating systems.

Parallel processing, RISC architectures, and microcomputers are hardly the end of the technological ferment roiling the midrange world. "The next thing is artificial intelligence," says West. "AI machines and techniques are what will be needed for the next step in user interfaces." AI-based interfaces will vastly simplify the task of using a computer, thereby expanding the number of users. He says new Lisp machines will be needed to meet the requirements for AI in future midrange systems—both for software development and delivery. Much applications software for this next step in user interfaces will be needed for the AI parts of midrange systems. In addition to user interfaces, "some AI machines will probably be added to systems to act as information [or knowledge] servers," says Prime's Walter Jones.

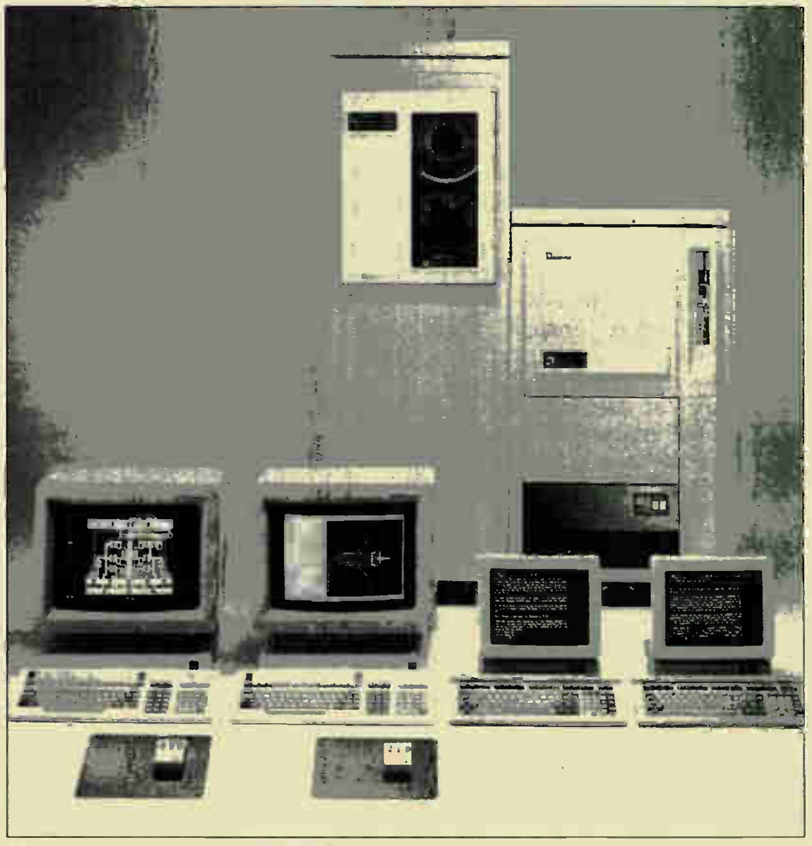
Along with AI, a major development that midrange computer vendors have to address is vector processing for computation-intensive applications. Vector processing used to be the purview of giant supercomputers and a handful of attached array processors. Now a new class of computers, called minisupercomputers [*Electronics*, July 29, 1985, p. 26], is hitting the market. Although their genesis was to fill the performance gap between superminis and supercomputers, minisupers are beginning to compete with high-end superminis. Therefore, midrange computer companies will have to start thinking about the ways to incorporate vector processing in their systems. IBM has recently added the Vector Facility option [*Electronics*, Feb. 3, 1986, p. 35] to its largest mainframe line, the 3090 series. It would not take much effort for the computer giant to add the same facility to the high end of its midrange 4300 systems.

The first parallel vector computer in the midrange field is the FX/8 from Alliant Computer Systems Corp. Ron Gruener, president and founder of the Acton, Mass., company, believes that computers with vector-processing capability will soon represent a large enough market at the high end of midrange computing to bring the established suppliers, such as IBM and DEC, into this market. Gruener thinks that IBM may add a vector facility to its next 4300 machine.

The spread of vector processing is an example of how changing technology continues to shake up the midrange computer field. Just as minicomputers were forced to evolve by the appearance of parallel architectures, supermicrocomputers, and, perhaps, RISC concepts, so will AI, vector processing, and other new developments force the midrange computer to move to another plane of performance. So, if the mini is dead, long live the mini! □




**5. DEPARTMENT MICRO.** One multiuser supermicro departmental computer is the MC68020-based DMC/932 2640 from Datamedia.



**6. MULTIMICRO.** The Masscomp MC5700 is a multiprocessor 68020-based midrange computer for scientific, laboratory, and engineering applications.

PROBING THE NEWS

# NEW TECHNOLOGIES CROWDING AUTOMATED-WIRING LEADER

## MICROWIRE AND UNILAYER II CHALLENGE WIRE-WRAP, LONGTIME NO. 1

by Jerry Lyman

It's a brand new race in the business of providing automated discrete wiring equipment for printed-circuit boards and backplanes. The longtime leader, Wire-Wrap, is being seriously challenged by Multiwire. And coming up strong is a pair of new techniques, Microwire and Unilayer II.

The process that started it all, Wire-Wrap, was developed in the 1950s by Gardner-Denver Co., Grand Haven, Mich. It is still the most heavily used method of automatic wiring. In it, an automated wiring tool wraps the stripped end of a solid wire five to seven times around a square post mounted in a pc board to form a gas-tight bond.

"The reason Wire-Wrap has continued to do so well is that anybody can do it," notes John Marshall, president of Data-Con Inc., Burlington, Mass., the largest independent wire-wrapping service in the U. S. The machines, wire, and software are all commercially available, and no licenses are required, as in the case of Wire-Wrap's competitors. In addition, there are multiple sources of wire-wrappable panels in standard and ECL versions readily available.

Its days of growth may be ending, however. "Wire-Wrap is now a mature product," says Gordon Wilmington, national sales manager for EPE Technology of Manchester, N. H., whose company manufactures what used to be the line of Gardner-Denver machines. "We are seeing a few pockets of growth, primarily in international telecommunications. In the U. S., the market is saturated, and the only growth that we see is in military and military-related applications."

Challenging for the top spot is Multiwire, which was introduced in 1970 in answer to objections that pins used with Wire-Wrap were too high. Developed by the Photocircuits Division of Kollmorgen Corp., Glen Cove, N. Y., it uses a numerically controlled machine. The machine lays a customized pattern of 6.3-mil-diameter insulated wires into a bed of adhesive covering an epoxy glass board. After a heat cure of the adhesive, holes are drilled through the wire and board and plated with electroless copper to connect the two.

At what is now the Multiwire division in Hicksville, N. Y., J. Philip Plonski, division vice president, sees three markets: quick-turnaround prototypes of high-density boards, high-speed emitter-coupled-logic circuits, and surface-mountable versions of ECL circuits for military use with leadless ceramic chip carriers.

Also, unlike Wire-Wrap, Multiwire still has room for technical growth. Two recent developments bear this out.

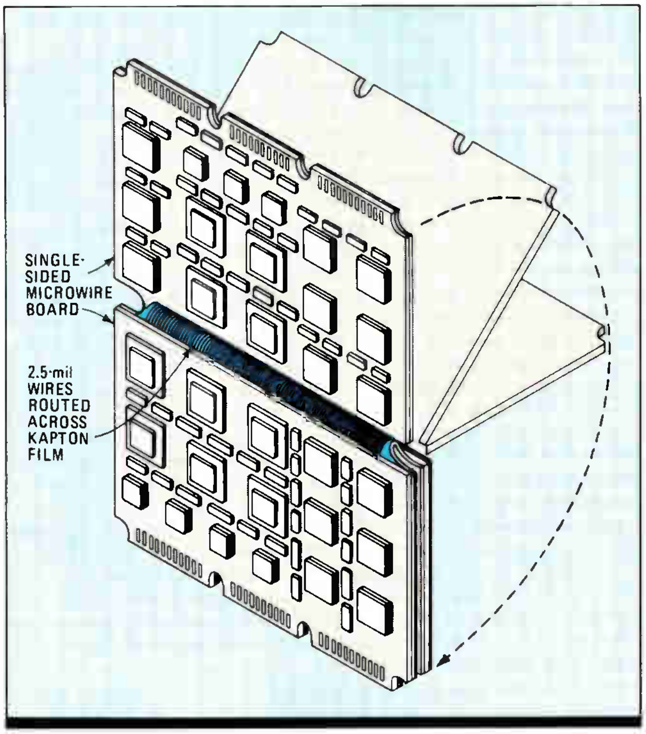
One is a coaxial Multiwire [*Electronics*, Jan. 27, 1986, p. 56], where miniature coaxial wires with a low dielectric constant are embedded in an adhesive. This technique was intended for gallium arsenide circuitry, but Plonski says that it is generating interest for use with silicon-based high-speed logic.

**OFF THE SHELF.** The second development is an off-the-shelf family of IC boards that can be customized by multiwiring. Initially, the Multiwire operation is offering 15 panel formats, including ones compatible with the VME, Multibus, Mupac, Eurocard, and the IBM Corp. Personal Computer. This is the Multiwire operation's first standard product to move away from its usual business—development and production of customized discrete wired boards.

Against this picture of change at the top, the newcomers are arriving. Developed and brought into production in the past few years are PCK Technology's Microwire, which is targeted at fine-pitch leaded chip carriers, and Augat Inc.'s Unilayer II, especially suited for high-speed logic families.

Like all discrete wiring techniques, these two are based on automated or semiautomated machines that have computer-controlled wiring heads feeding insulated wire to the surface, or to pins mounted on the surface, of an epoxy-glass board. Microwire, primarily for military applications, is aimed at boards fully populated by ceramic leadless chip carriers, although pin grid arrays can be accommodated.

It offers high density—it is based on 2.5-mil insulated wire conductors on a 12.5-mil grid, ideal for the fine-pitch leadless ceramic chip carriers. Microwire boards are built up from copper-Invar-copper cores, which offer good thermal conductivity and match the thermal coefficient of efficiency of alumina carriers.




**MATED.** The Microflex version of PCK Technology's Microwire connects single-sided substrates with a Kapton layer common to both boards.

The sandwich construction starts with an outer component pad layer and a power and ground distribution layer using conventional pc processing. Between them is a high-density signal-wiring layer—the 2.5-mil wires—encapsulated in a compliant resin. Electrical access to the conductors is through laser-drilled copper-plated vias 10 mils in diameter.

**MICROWIRE OFFSHOOT.** Microwire is now in full production. In fact, a year ago PCK, itself a Kollmorgen division, created a subdivision called Microwire Interconnect Technology to handle the technology; the objective is to elevate it to full division status. It already has one licensee, and it hopes for three or more by 1987.

Microwire boasts the most advanced technology of the discrete wiring techniques. Its initial attractions to potential users were its lessening of the thermal mismatch between large leadless chip carriers and their substrate and its efficient heat dissipation. Now, says Marc Motazedi, product manager of Microwire Technology, "Most users and potential users are attracted by the high-speed, controlled-impedance, and low-noise properties."

The technique is also flirting with the leading edge of integrated-circuit technology: Motazedi says his operation is looking into using it for GaAs circuitry. Microwire can handle 400- to 500-MHz digital signals, which makes it suitable for the fastest ECL commercially available.

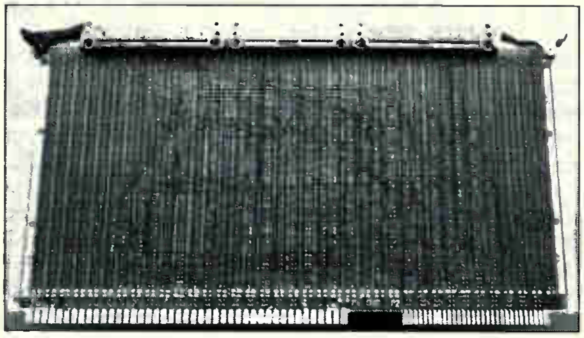
The technique has also spawned two advances, Microflex and Microshield. Microflex is a flexible interconnection between substrates with an extremely high density unobtainable in any present connector. In addition, it maintains a controlled-impedance, low-noise link between the two boards that standard connectors cannot accomplish. It works by connecting two single-sided Microwire substrates with an integral Kapton layer common to both circuits, the same technique used in conventional flex-rigid multilayer printed-circuit boards.

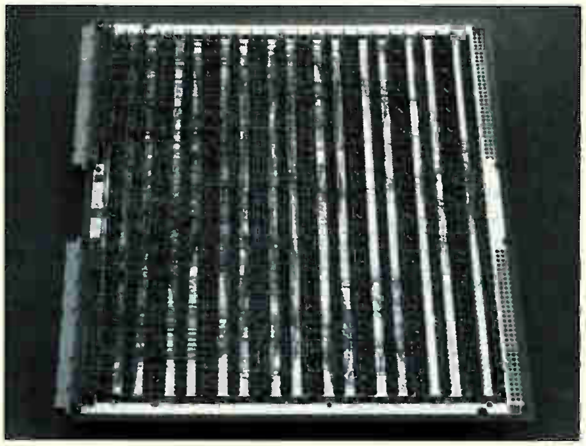
Microshield, a shielded version of Microwire, provides Microwire circuits with a shielded wiring level having a 50-Ω ±5% controlled impedance with a backward crosstalk value of less than 2%. To implement Microshield, an extra copper plating step is added after the usual "wiring" of the Microwire signal layer.

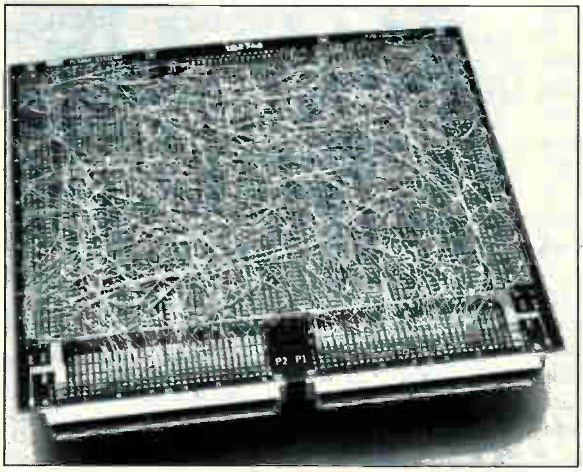
The second recent development, Unilayer II from Augat, offers a low-profile, controlled-impedance circuit board. It is based on 4-mil-diameter polyurethane insulated wires applied under computer control to an adhesive layer covering a special steel fixture. The wire net, embedded in an adhesive, is then transferred to a board with a ground plane on one side and a power plane on the other. Each side has a pattern of isolated plated through holes connected to an adjacent solder bump. A soldering head removes the insulation above a solder bump and reflows the wire to the bump where an interconnection is needed.

Unilayer II already is being used industrially, in computer equipment, and in some cases by military customers. It is ideal for people with small production runs who want to keep design costs low and get to market fast, according to Larre Nelson, marketing manager at Augat Interconnection Systems in Attleboro, Mass.

**SPEEDY AND INEXPENSIVE.** For example, after receiving a wiring net list with its design data base, Augat says it can deliver a typical 8-by-9-in. board in 3 to 4 weeks for a design cost of $500 to $1,000. This compares with $5,000 to $10,000 for a multilayer board of the same circuitry interconnections. However, Nelson admits that Wire-Wrap is better for prototyping because it costs less and is easier to repair and modify than Unilayer.







**AUTOMATED-WIRING COMPETITORS.** The wired undersides of printed-circuit boards using, from the top, Augat's new Unilayer II and two of the established techniques: Wire-Wrap, which is the longtime market leader, and stitch wire.

Nevertheless, he says, "We have come close to tripling our Unilayer business in the last 12 months. We are now in a real production phase, and the process is now stable and predictable and meets the claims made for it."

The discrete wiring technique with the smallest share of the market is the oldest, variously known as stitch wiring or welding. Despite its small market share—limited to low-volume, high-reliability, military and aerospace applications—at least three companies are still using it. They are Augat, Interconnection Technology Inc., and Moore Systems-Stitch Weld Corp.

Stitch wiring originally was favored for military and aerospace work because of the reliability of its welded joint and its high resistance to shock and vibration. "Now the main feature that allows stitch wiring to displace Wire-Wrap in military and commercial applications today is its ability to run at extremely high clock rates with a clean signal" (clean of reflections and with good rise and fall times), says Jerry Hammel, president of Interconnection Technology.

He notes that his company does stitch wiring with sockets with stainless steel wiring pins inserted through isolated plated-through holes on a ground plane on the wiring side of the board. This plane, along with the short point-to-point wiring, means high speed.

Hammel says he is seeing a mix of about 70% military to 30% commercial (computer and medical instruments) in his company's sales. Use is mostly with dual in-line packages, but a few applications include pin grid arrays and in-line packages. □

# HOW STORAGE TECHNOLOGY ENGINEERED ITS RECOVERY

## SMALLER, TIGHTER COMPANY IS ABOUT TO TURN THE CORNER

*by J. Robert Lineback*

**LOUISVILLE, COLO.**

In less than a year, Storage Technology Corp. has turned around from what loomed as the worst financial failure in the history of the electronics business to what may be the industry's biggest and fastest exit from Chapter 11. How the quick change was engineered by turnaround veteran Ryal R. Poppa in his short tenure as chairman and chief executive officer is a story of making a company bigger by first making it smaller.

What Poppa and his staff did was discontinue some products, set realistic goals for research and development, and tighten fiscal policies. So far it seems to be working: the company expects an agreement with its creditors in time to get out of Chapter 11 by Jan. 1, and it has a new strategy to combat IBM and a new product to do it with.

Only 14 months after the 17-year-old manufacturer of IBM-compatible mainframe storage and printer peripherals filed under Chapter 11 of the bankruptcy laws in October 1984, it emerged from an arduous period of downsizing with a fourth-quarter profit of $2.22 million on sales of $168.62 million. That compares with a loss of $406 million on sales of $151.95 million for the same quarter of 1984.

The first quarter of 1986 was good, too, with profits of $5.02 million on revenues of $161.96 million. By way of comparison, in the first three months of 1985 the company scored almost identical revenue but lost $29.69 million. And that's not the end of it: Storage Technology expects to make three profitable quarters in a row at the end of June.

Employees are no longer fleeing. Attrition at the end of 1984 ran at an astonishing annual rate of 57%. It slowed, partly because of the industrywide recession, to near 25% by last summer and now is at a more normal 9%. "The drop in attrition is the result of more knowledge of the facts. Perhaps we have overcommunicated," jokes Poppa (pronounced POP-ee), who joined the company in January 1985 after founder Jesse I. Aweida left.

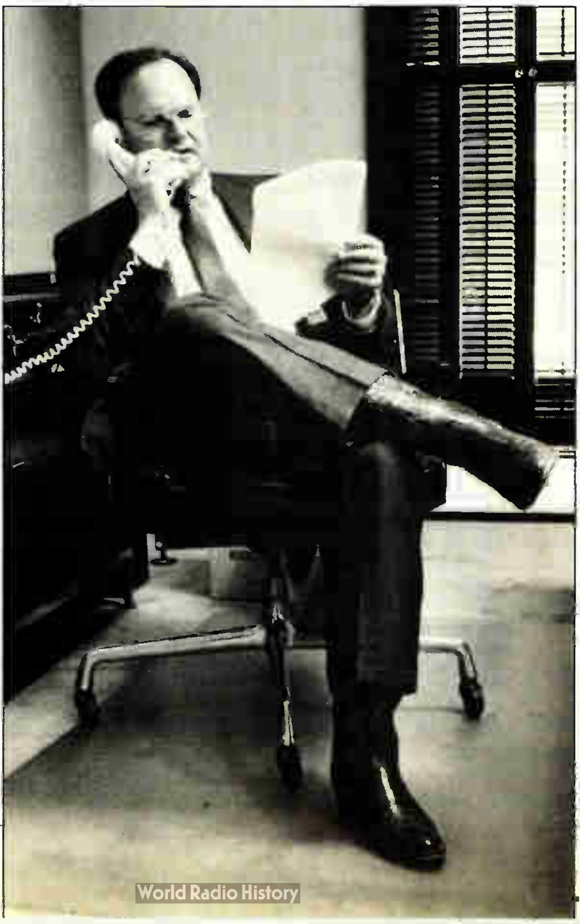
Cash reserves are once again at a healthy level—$240 million, against a low of less than $20 million in the first half of 1985. Customer confidence is back too, says Poppa, and once the shadow of Chapter 11 is lifted, perhaps as soon as January 1987, the company expects to go head-to-head with IBM Corp. for new accounts.

**BATTLE READY.** But more important than the first profits in nine quarters is what Poppa believes is a new Storage Technology, which the aggressive chairman says is not only lean but also ready for the battle with its giant archrival. Gone are the days of attempting gigantic but risky leaps in systems and mass memory technology over IBM. That's what tripped up the company, according to Poppa: biting off indigestibly large chunks of computer and peripheral technology following unprecedented growth in profits and revenues at the start of the 1980s.

In those heady days, IBM delays in shipping a new mainframe disk drive opened the door to an unexpected wave of 1981 sales for Storage Technology's 8650 plug-compatible disk units. The company quickly expanded. Profits hit their high-water mark in 1981, up 81% to $82.4 million on revenues that were up 53% to $921 million. Revenues peaked the following year at $1.08 billion, but net income ebbed to $64.7 million; in 1983 the company started to bathe in red ink, and losses reached half a billion dollars in 1984. Still, research and development funds streamed into an ill-fated CMOS-based mainframe project, a new semicustom chip business, and a 4-gigabyte 14-in. optical disk system. All three efforts were dropped in 1985.

"Three hundred million dollars thrown away. I don't see anything for any of it," says a still disbelieving Stephen G. Jerritts, Storage Technology's president and chief operating officer. He was recruited by Poppa and the board early in 1985 from Lee Data Corp. of Minneapolis, where he was president. He also is a former president of Honeywell Information Systems.

**COLORADO COWBOY.** Ryal R. Poppa came riding in on his white horse to rescue Storage Technology from Chapter 11.



The weakening position was compounded toward the middle of the decade by aggressive price cuts and new products from IBM. But, says Poppa, "What got Storage Technology was not IBM, but that the company got overaggressive, launching new businesses into semiconductors, the central processing unit project, and optical storage." Poppa outlines a simple new game plan: "You don't have to announce on the same day that IBM does. Customers will often take as much as a year to evaluate these kinds of products," he says. So from now on, Storage Technology's strategy will be geared toward turning out an equal or slightly better product within a year after IBM's introduction. "We then will concentrate to get the products out quickly and finish out the product lifetime with acceptable margins."

Unlike the small-computer market, Poppa says, mainframe peripherals have active product lifetimes of a decade. Storage Technology's yet-to-be-announced Cimarron tape-cartridge system—which is actually a rare move in the Poppa era to leapfrog IBM—will be unveiled in the fall and is expected to have a life exceeding 10 years.

Cimarron, which includes an automatic cartridge tape library system that changes cartridges without human intervention, will be a major test of Storage Technology's ability to catch and pass IBM, which introduced its competing 3480 tape cartridge system a year ago. Cimarron, which the company says is denser than the 3480, will be Storage Technology's most important new product since it filed under Chapter 11, according to analyst Donald Sinsabaugh, managing director at Swergold, Chefitz & Sinsabaugh Inc., New York.

"Obviously, the company's real strength has been the tape market. That's where they found a home at the beginning," says Sinsabaugh, who believes product introductions and shipments play a more critical role in Storage Technology's survival than a quick exit from Chapter 11.

**ALTERNATE SOURCE.** "Needless to say, if they don't come out with an archival product which is comparable to the 3480, then there will be major problems," he adds. Sinsabaugh agrees with Poppa's strategy of aiming to equal or match IBM within a year of product introduction. "The point here is that the customers really need a threat or alternative to IBM, and they will continue to buy or lease compatible equipment as long as it is in good working order at a fair price. It is in the customer's own interest to keep people like Storage Technology in business," Sinsabaugh says.

Still, Storage Technology faces a stiff challenge to ramp up production quickly in order to stay in step with IBM's pricing, cautions analyst Michael J. Geran of E. F. Hutton & Co., New York. With at least one product, it seems to be succeeding. The company is pushing up delivery of a new double-density 8380E disk drive to match IBM's 3380 double-density drives. Storage Technology originally announced the drives would be available at the end of 1986; now it's saying July. "We needed that to tell everyone that the company is alive and well," says Jerritts.

He says R&D will be held at 9% of revenues in 1986 for products slated to be introduced over the next couple of years. In 1984, the rate was about 13% of a much greater revenue base. Company executives expect those revenues to be in the range of $725 million to $750 million. "I believe we are poised well on a four-legged stool [disk drives, tape subsystems, printers, and solid-state cache]. And we might be in a position to add another leg when we get out of Chapter 11," Jerritts says.

Despite all the optimism, the company acknowledges that there's a degree of uncertainty inherent in competing with IBM. "No assurance can be given that [Storage Technology] will be able to develop such products within the desired timeframe or that, if developed, the new products will have price/performance advantage comparable to those of new IBM products," the 1985 Form 10-K states. But now Poppa believes that IBM's recent reduced financial performance will make price cuts less likely, giving his company time to ramp up production.

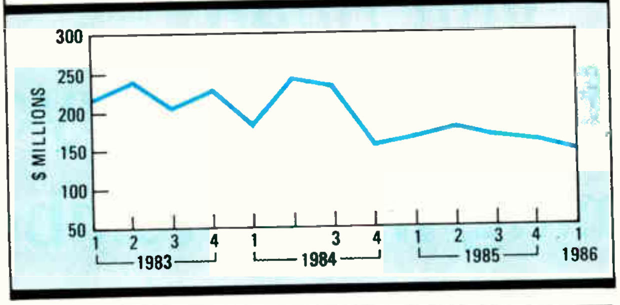
"IBM is the 400-lb gorilla that we must live with every day in this business. There is a misperception that IBM poses some kind of a new threat," says Poppa, who once worked for Big Blue. After that, he became chairman of Pertec Corp., where he engineered a merger with Triumph-Adler of West Germany. Then he moved on to BMC Industries before coming to Storage Technology. "IBM has been a 400-lb gorilla ever since I can remember. It was when I was with them, and yet Storage Technology got into business and was successful before."

"The perception from industry news stories was it would be Chapter 7 [liquidation] or, if we survived, that IBM would roll over and kill us," says Poppa, who personally made 287 customer calls in 1985 to help rebuild market confidence. "In February and March of 1985, I was not so sure," he recalls. "Then in March, rates picked up and continued to rise in April. They were again pretty good in May. I was certain about the recovery by last May."

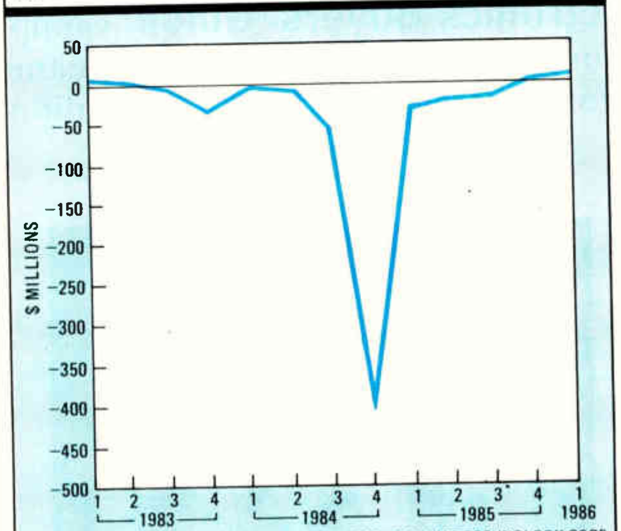
The recovery won't be complete until Storage Technology's exit from Chapter 11 is completed. Poppa believes an agreement could be signed with creditors as early as this month and no later than July.

"A friend of mine recently suggested that we are writing the book on how to reorganize a high-technology company in Chapter 11. That might be so, but I hope it does not become a best seller," Poppa says. □

*REVENUES WERE UP AND DOWN . . .*




*. . . WITH EARNINGS REACTING SHARPLY*




SOURCE: STORAGE TECHNOLOGY CORP.

*STORAGE TECHNOLOGY'S BIG SHIFT IN REVENUE (in $ millions)*

| | 1982 Revenue (%) | 1983 Revenue (%) | 1984 Revenue (%) | 1985 Revenue (%) |
|---|---|---|---|---|
| Disk | 559.9 (52) | 358.3 (41) | 295.1 (37) | 228.6 (34) |
| Tape | 379.2 (35) | 401.7 (45) | 407.5 (50) | 344.7 (51) |
| Printers | 85.4 (8) | 99.4 (11) | 100.4 (12) | 99.0 (15) |
| Other | 54.7 (5) | 27.2 (3) | 5.6 (1) | 1.1 (–) |
| Total | 1,079.2 | 886.6 | 808.6 | 673.4 |

SOURCE: STORAGE TECHNOLOGY CORP.

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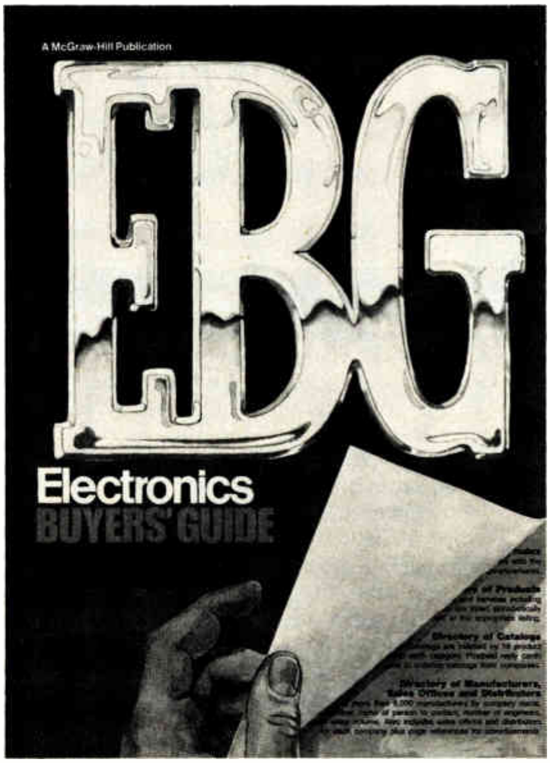


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- Japanese Chemical Firm Moves from Soap to Floppies
- Italian Firm Seeks Allies to Crack U.S.
- Japan Pursues Role in Space
- Bellman Switches on Italtel for Expansion
- Robots get Smart in Japan
- ITT Invests in European Units Crack U.S.

**February**
- Europe's Esprit Finally Sets Sail
- LSI Logic Counts on Sandfort to make its Mark in Europe
- Upstart Vendor Makes Waves in Japan's Robot Market
- NEC Fashions New Fab Process
- Olivetti's Viti Directs ET Designs that Marry Bus & Art
- German Startup's Success Surprises Europeans
- Britons Seek Tolerant Chips
- OBI Rains on IBM's Parade
- Mega's Friedrich Aims to Cut Asian Lead in Memories

**March**
- British GaAs Chips Go to Market
- NEC's CPU Leapfrogs IBM
- Hitachi CPU Challenges IBM
- France's Lansat Rival Set for Fall Launch
- Olivetti Stakes Claim in Video Typewriters
- Italian VLSI Chip has the Right Accent
- Koreans Try for VCR Replay
- Germans Push X-ray Exposure
- There's Life in Resistors, German Company Finds
- UK Beats a Path for Europe's Race

**April**
- German System Meets New ICAO Standard
- West Germans Squabble Over Choice of IFF
- Britain Promotes Open Architecture
- US Makes Progress in Japan Telecom Talks
- Japan's Lead in Optical Disks: It's Part of the System
- Daisenberger Guides US Firms through Red Tape
- Asia: It's No Longer Just Japan That Threatens US Markets
- Malaysia: Top Shipper of Discretes
- Indonesia: Domestic Sales are the Lure

**May**
- Thomson's VCR System Clears Up Doubts
- ICL Banks on Networks and Japanese Chips
- Min Blazes Bright Path for Korea's Gold Star
- Asia: The Four Dragons Rush to Play Catch-up Game
- Singapore Casts Lot with Software
- Philips' Eurom Chip Finally Debuts
- Sagging Prices Sting Japanese Producers
- British Telecom Spreads Its Wings with Mitel
- South Korean IC Maker Seeks World Markets

**June**
- Plessey Switches Off Flash ADC, Saves Power
- Sony Campaigns Hard for BMM Camcorders
- Japanese Quit on IBM Software, Turn to UNIX
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# SGS PICKS ITSELF UP AND GETS GOING AGAIN

## CHECKED BY THE RECESSION, IT IS RENEWING ITS PUSH INTO THE RANKS OF THE TOP 15 IC MAKERS

**AGRATE, ITALY**

Shaken by one of the worst recessions in the history of the electronic components industry, Italy's principal semiconductor maker is regrouping to complete its run at what company executives still consider a reasonable goal: a place among the world's top 15 semiconductor producers.

Although the industrywide hard times have nudged SGS Microelettronica SpA back into the red, the company has made definite strides since mounting its campaign in 1980 for the top rung. Since then, it has consistently gained market share with sales growth that has outpaced the international market as a whole (top chart). And in 1983 and 1984, it turned a profit for the first time in its nearly 30-year history.

Long considered one of the industry's underachievers, SGS is on a roll thanks to an ambitious program to transform this producer of power technology traditionally awash in red ink into a profitable, broad-range merchant semiconductor house. Despite the wrinkle in the master plan caused by the recession, it is no exaggeration to say that a good part of this task has been realized.

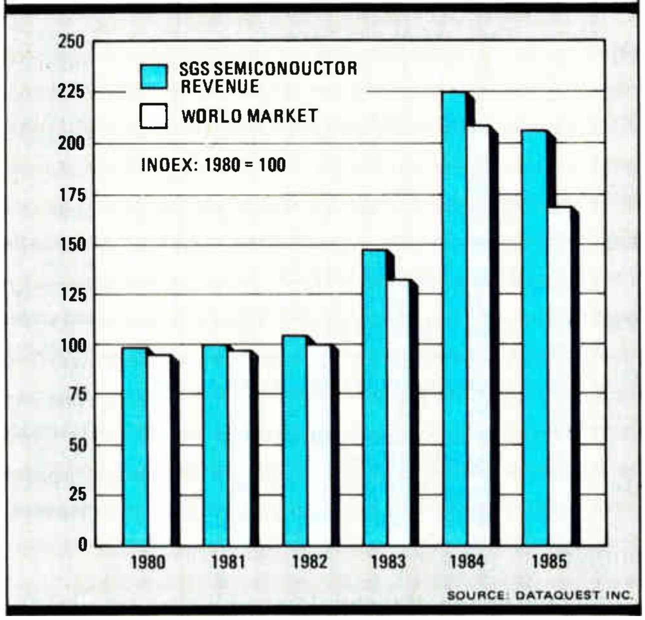
The magician who masterminds the program is the ebullient Pasquale Pistorio, who, until taking over the helm of SGS in July 1980, was general manager of Motorola Inc.'s International Division in Phoenix, Ariz. Asked why he left an attractive job at Motorola for the presidency of a company few thought could turn a profit, Pistorio quips, "Some people are crazy."

More seriously, he says, "It was simply the professional challenge to turn the company around. Technologically, SGS had an enormous amount of potential, so it was basically a business challenge to change what was at the time a very good laboratory into a mass-marketing and mass-production company."

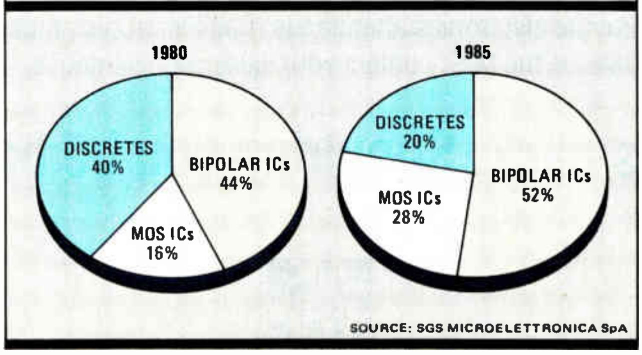
SGS slid back into the red in 1985, under the pressure of the industry crisis, but Pistorio is looking for a profit in the second half of this year and thinks there's a reasonable chance of a positive net result for 1986.

SGS doesn't have to release sales figures because it is owned by IRI-STET, the Italian government's holding company. But at Integrated Circuit Engineering Corp., the Scottsdale, Ariz., market researcher, analyst Dean Winkelman estimates that the company did $230 million in IC sales and $350 million in total semiconductor sales last year. "That ties it in about twentieth place with Siemens AG in ICs alone," he says, noting that No. 15 in ICs last year was Signetics, a Philips subsidiary. "So climbing five positions is quite difficult and optimistic—companies thought of as fast growers, like AMD and Intel, have not been able to do that recently," he says.

*SGS SHARE GROWS FASTER THAN WORLD MARKET . . .*




*. . . AS BIPOLAR AND MOS ICs OUTPACE DISCRETES*




Still, the inability to maintain at least a profit-and-loss balance during the recession underlines the company's most serious weakness: a lack of the critical mass of resources necessary to weather the roller-coaster ups and downs of the world semiconductor market. Proof of this is the fact that although SGS's total sales for 1985 slipped only to $306 million from the previous year's $325 million—not bad for the bad days—its 1984 operating profit of $23 million was virtually wiped out by a $19 million loss.

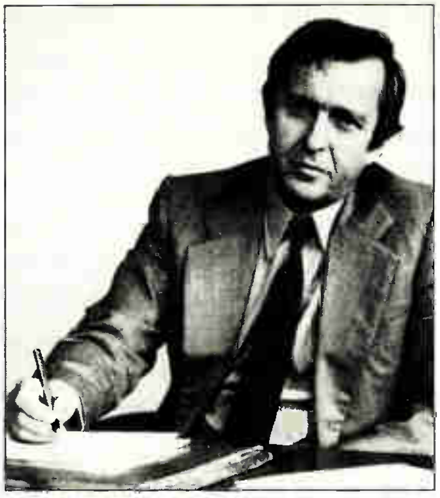
**DASHED HOPES.** That loss all but dashed hopes of achieving Pistorio's original objective—admittedly a very ambitious one—of becoming a $1 billion company and one of the world's top 15 semiconductor suppliers by 1988. Pistorio has now shifted his sights to 1990.

Despite the company's sensitivity to market turns, even its rivals see SGS as a much stronger competitor than it was six years ago. But many say Pistorio is too ambitious and SGS too specialized to compete across the board in the semiconductor market.

"There is no doubt about it—what SGS does best is power technology in general and linear in particular," concedes a top executive for one of its European competitors. "But its strategic weakness is that it makes an enormous portion of its sales in that area, and it's a weakness that is likely to diminish in importance in the future as the power-capabilities of standard MOS technologies gradually increase."

Predictably, SGS general manager Raimondo Paletto disagrees. He points out that one of the principal trends in the semiconductor market—and one on which SGS is spending a significant amount of its resources—is the integration of power devices on the same chip with MOS logic. This, he argues, is more easily achieved by companies like SGS, with a large variety of power technologies, than by producers of standard MOS circuits.

Pistorio, for his part, makes no apologies for the concentration in power devices. "If you look down the list of all the major semiconductor producers, you can always find one single strong point, something peculiar they have to offer the market, that distinguishes them from the rest," he says. "We are the world leaders in power technologies, from the discrete transistor to the most complex IC." The only problem in such a profile, he says,



**PLANNERS.** President Pistorio, left, wants SGS to join the top 15 chip makers. General manager Paletto, right, believes putting power devices and MOS logic on a chip will help.

comes "if you get too absorbed in your own strength, you reach a point where you have difficulty responding to changes in the market. But I don't see that happening to us."

If the power-technology department was strong when Pistorio took over, the company as a whole was in need of a massive reorganization, he says. It was producing in the same wafer fab five discrete technologies and six varieties of chips; the six IC processes were used to produce only 10,000 wafers per month. "There is no way you're going to make a penny on any technology like that," says Pistorio.

So he pared the operation to two discrete processes—small-signal metal and power transistors—and two IC technologies: CMOS and bipolar. Next, he turned to the product line. He made no changes in the bipolar selection, but dropped dynamic random-access memories from MOS production. Untouched were microprocessors, erasable programmable read-only memories, and dedicated circuits for market sectors like telecommunications, consumer, data processing, and automotive.

**QUEYSSAC:** Plans for MOS diffusion in Phoenix have been put off.

Gradually, he began increasing SGS's concentration in bipolar circuits, particularly linear, while decreasing discretes (bottom chart, p. 60). To bolster the company's technological weakness in MOS circuits, he made a design and technology-transfer alliance with Japan's Toshiba Corp.

Before Pistorio's arrival, more than 75% of SGS components wound up in consumer and industrial equipment. Now there's a more balanced distribution, credited principally to the growth of products for telecommunications and data-processing applications.

Pistorio's other principal efforts were aimed at modernizing SGS's production and expanding its sales force. He moved testing and assembly from Italy to Malta and Singapore—albeit reluctantly. "That was a very painful decision. But with the cost of labor in Italy 10 times that in Singapore and 5 times that in Malta, if I do my test and assembly here and my competitors do it there, I lose."

In addition to modernizing and automating the company's front-end diffusion centers in Agrate and Catania, Sicily, SGS opened a new center in Singapore. The Sicilian and Singapore plants produce 5-in. wafers, but Agrate was recently converted to 6-in. wafer fabrication. The cycle time from order to delivery is down to eight weeks from the six months it typically took just a few years ago. The new cycle time is still too long, and Pistorio vows to continue to trim it even further.

On the sales side, Pistorio replaced distributors with a sales force of more than 300 spread over 33 offices in 15 countries. As a result, SGS sales—84% of which were in Europe in 1980—are now more equitably distributed around the world. About 20% now come from the U.S., with 15% from Asia and the Pacific.

But despite the growth in U.S. sales, a major casualty of the 1985 crisis was SGS's plans for U.S. expansion. Daniel Queyssac, general manager of the U.S. subsidiary, says plans to begin MOS diffusion at its facility in Phoenix, slated for the first quarter of this year, have been put off. *–Robert T. Gallagher*

*BOTTOM LINES*

## REL CORP. ACQUIRED BY WHITTAKER

REL Corp. of Boynton Beach, Fla., a closely held manufacturer of electronic defense and communications equipment and systems, has been acquired by Whittaker Corp. of Los Angeles. Terms were not disclosed. Joseph F. Alibrandi, Whittaker's chairman and chief executive officer, called the acquisition consistent with his company's growth strategy in high-tech areas. REL is Whittaker's fourth electronics purchase in the past year, and all are in the defense electronics business.

## SILVAR-LISCO GOES INTO BLACK

Silvar-Lisco, the Menlo Park, Calif., developer of software for computer-aided engineering, has announced a profit of $470,000 on sales of $19,519,000 for the fiscal year ended April 30. For the previous year, it had a loss of $416,000 on revenues of $15,576,000. President Paul F. Seckendorf attributes the increase in revenues to a modest improvement in business and inclusion of licensing and maintenance fees from the Design Verification Products Group, acquired in March 1986 from NCA Corp.

## RIDGE RECEIVES $2 MILLION FUNDING

Ridge Computers Inc. has received $1 million each from Hambrecht & Quist, the San Francisco venture-capital firm, and Groupe Bull of France. The sum is part of a $10 million refinancing package from the two companies. The money will be used to recapitalize the business, says Vernon Anderson, chairman of the Santa Clara, Calif., computer maker. "This refinancing revitalizes Ridge as a manufacturer of affordable superminicomputers," says Anderson, and will help the company expand its markets and product line. At the same time, Bob O. Evans, a general partner in Hambrecht & Quist, is joining Ridge as chief executive officer. He has 33 years of experience at IBM Corp., most recently as vice president of engineering, programming, and technology.

## PRIME TO SELL 447 SUPERMINIS TO U.S.

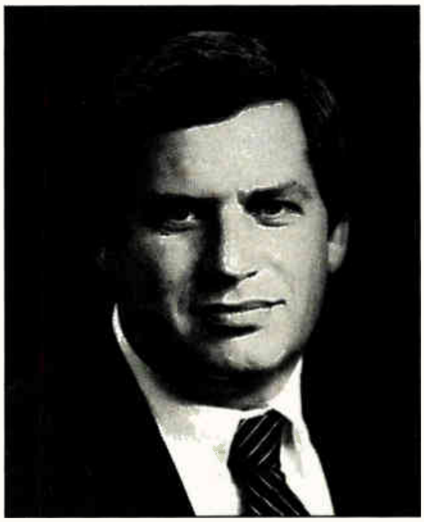
Prime Computer Inc. has signed an agreement with the U.S. Department of the Interior to supply over the next five years up to 477 superminicomputers valued at $64 million. This is the largest single contract ever signed by the Natick, Mass., company.

# FOR STEPHEN COOPER, WAFER FAB IS JOB ONE

**TUSTIN, CALIF.**

Stephen E. Cooper makes no bones about which of his daily management tasks at Silicon Systems Inc. gets the most attention. "I'm oriented toward wafer fabrication—it's the core of the business, where the capital is spent," says the company's president and chief operating officer.

It's hardly a surprising point of view, given that he is a recognized authority in chip processing. But Cooper, who joined Silicon Systems in 1980 as vice president of wafer fabrication, maintains that this focus is more than a personal interest. In today's supercompetitive marketplace, he says, nothing ranks higher than manufacturing a quality semiconductor product. It is the bedrock skill required to fulfill what Cooper terms "our top priority—establishing a profit culture."



**COOPER:** Basing a profit culture on a quality semiconductor product.

Chairman and chief executive officer Carmelo J. Santoro named Cooper, 39, to the new posts in May, promoting him from senior vice president and general manager of the Microperipheral Products Division. Cooper earned the job, Santoro says, because "he did an outstanding job growing the business through one of the industry's deepest recessions." The numbers are indeed good: for the fiscal year ended Sept. 30, 1985, Cooper's division grew from 35% of company sales to 61%, or to total revenues of about $33 million.

In managing the division, Cooper had profit and loss responsibilities for the company's key product line, controller and read/write amplifier chips for Winchester disk drives.

Santoro had been filling the slots of chairman and president since 1983, when he joined Silicon Systems, itself established in 1972. But the pickup in company growth late last year, spurred by demand for drive products along with the takeoff of the new K212 modems, was too much even for that energetic executive to handle. "Carm recognized the two jobs were killing him," notes a company insider, so he chose Cooper to take over the daily details.

In Cooper, the hard-driving Santoro found an equally intense semiconductor veteran who has been in the business since earning his BSEE from the University of California at Santa Barbara in 1968. Before coming to Silicon Systems, Cooper was responsible for wafer fab at Intel Corp., Santa Clara, Calif.

**CLOSE RELATIONS.** As a manufacturer of application-specific integrated circuits that address sizable niche markets, Silicon Systems must place its greatest emphasis on offering the best possible service to its major corporate accounts, says Cooper. The reason is that the customized nature of ASICs demands a close relationship between supplier and customer on a continuous basis, from the design stage through final equipment delivery.

Quality control is especially important, because ASIC fab runs are small, notes Cooper, and defective components are not easily replaced—not to mention costly and damaging to a vendor-client relationship. The company therefore has been pushing a "big quality-control program that has had dramatic results in recent weeks," he says. "We've broken through the 100-parts-per-million level."

Many of the parts are analog, which are typically more difficult to build than digital commodity-type chips. But what makes the feat particularly noteworthy, he believes, is that the parts-per-million rate was "several thousands just 18 months ago."

The only new tasks confronting Cooper, who retains his old office at the Tustin headquarters because growth has put space at a premium, is involvement in the company's overall financial picture. Business continues to improve, giving the company a good shot at breaking $100 million sales by 1987. In-

## PEOPLE ON THE MOVE

**JACK B. HARROD JR.**

☐ Texas Instruments Inc. has named Jack B. Harrod Jr. senior vice president and general manager of the Avionics Systems business entity. He had been serving as vice president and manager of the company's Radar Systems Division.

**GEORGE J. POPOVICH**

☐ Only two months after joining Inmos Corp. in Colorado Springs, George J. Popovich, 36, has become vice president of North American sales and marketing. He replaces A. C. D'Augustine, 41, who leaves his post after six years with Inmos to become vice president of marketing at gate-array manufacturer Applied Micro Circuits Corp., San Diego. Popovich joined Inmos as vice president of sales in April after a brief period at Lattice Semiconductor and eight years with Intel Corp., where he most recently served as marketing manager for the memory products division. Popovich started his career in the chip industry at Texas Instruments Inc. in 1974 after receiving a BSEE from the University of Nebraska.

**JAMES J. RENIER**

☐ Honeywell Inc.'s vice chairman, James J. Renier, has been elected president and chief operating officer of the Minneapolis computer maker. He will report to Edson Spencer, chairman and chief executive officer, who will shift his focus to long-range planning. Renier joined Honeywell as a senior research scientist and holds a BS in chemistry from the College of St. Thomas in Minneapolis and a doctorate in physical chemistry from Iowa State University.

**HARRY A. CAUNTER**

☐ Gould Inc. has named executive vice president Harry A. Caunter acting head of the Defense Systems Business Section in Rolling Meadows, Ill. Most recently executive vice president for operations services, he has just served a term on the Management Review Committee as part of Gould's program to rotate senior executives through the committee, its top policy-review body. Caunter joined Clevite Corp. in 1957, before it merged with Gould in 1969. He has a BBA degree from Case Western Reserve University.

**WALTER C. STALTMAN**

☐ Moving up at Texas Instruments is Walter C. Staltman, named a Defense Systems & Electronics Group vice president and manager of the Radar Systems Division. He previously had been manager of business development and radar strategy for the Avionics Systems entity.

dustry analysts predict that it will reach the $70 million level in 1986.

But Silicon Systems executives still have fresh in their minds the recessionary troubles and a quarter ending Dec. 28, 1985, that resulted in a loss of $2.4 million. They have no intention of letting the company just drift along. Hence Cooper's emphasis on establishing a profit culture. Silicon Systems is investing a hefty 13% of its sales in research and development and watching costs closely. "We are positioned nicely for shareholders to reap the harvest of these investments," predicts the new president. *–Larry Waller*

# KULICKE PICKS UP WHERE DAD LEFT OFF

**HORSHAM, PA.**

Back when C. Scott Kulicke was an engineering student at Lafayette College in Easton, Pa., just about the last thing he wanted to do was run his father's business, Kulicke & Soffa Industries Inc., a maker of semiconductor assembly equipment. "I didn't know what my plans were," he recalls, "but I knew they didn't involve K&S." Soon circumstances dictated otherwise.

Today, the 36-year-old Kulicke is chairman and chief executive officer of the company his father, Frederick Jr., started with Albert Soffa more than 40 years ago. And he is also recognized as an industry leader: late last month, he was elected president of the Semiconductor Equipment and Materials Institute, an international trade association for manufacturers of chip-making gear. For someone who never planned to join the family business, Kulicke has come far.

Kulicke had expected his older brother Frederick III to follow their father's lead. But in 1969, Frederick, then 26, was killed in Vietnam, radically changing the future—at least as young Scott perceived it. He dropped out of school, he says, spending a year at Kulicke & Soffa as a design engineer before deciding that wasn't what he wanted to do.


**KULICKE:** A reluctant heir to the family business now has become an industry leader.

**BACK AND FORTH.** Changing his plans again, he enrolled at the University of Pennsylvania's Wharton School of Business, and in 1972 graduated with a degree in economics. He rejoined Kulicke & Soffa, quit in a fit of what he terms "rampant immaturity," and then, after a short stint as a motorcycle mechanic, went back to the company again and zipped off to Hong Kong to learn the business.

At the age of 23, Scott became manager of Far East operations, an important post for a company that ships 75% of its products to that part of the world. "The best way to learn about your products is to see how they're used by the customers," Kulicke says, admiring his father's wisdom in sending him so far away so fast. "Even today, when we want to bring a new manager or supervisor up to speed quickly, we send him to the Far East."

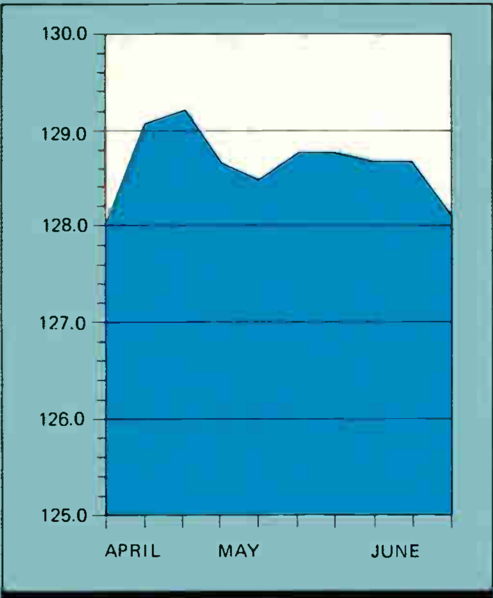
**TURNING POINT.** Two years later, Kulicke headed a product-development team that produced the company's first automated wire bonder. The model 1412 tripled productivity by putting the process under the control of a microprocessor—and spelled the way for Scott to take over the company.

"I became general manager in 1978 because [the model 1412] became our dominant product," Kulicke says, adding that "automatic wire bonders are still our dominant product." Two years after that, Kulicke took over as company president and in 1984 assumed the chairmanship. During that period, from 1978 to 1980, Kulicke & Soffa grew from about $17 million in sales to about $50 million, and in the next five years sales really rocketed to reach almost $125 million in 1985.

But then the market collapsed. Sales for the current fiscal year (which ends Sept. 30) won't top $70 million. Kulicke had to eliminate 900 jobs, cutting his staff to just 1,200 people while doing his best to maintain "all our key design projects." Now as he tries to get the company back on track, Kulicke sees consolidation of U.S. competitors and the threat of increased competition from Japan as the key factors facing the company as it tries to grow past the $100 million mark again.

"You've got to go straight at the competition," Kulicke says. "You figure out what your strengths are, and you optimize them. Then you determine what your weaknesses are, and you sit down and fix them. That's the only way to compete." *–Tobias Naegele*

## ELECTRONICS INDEX





| | | |
|---|---|---|
| THIS WEEK | = | 128.1 |
| LAST WEEK | = | 128.7 |
| YEAR AGO | = | 127.4 |
| 1982 | = | 100.0 |

The *Electronics* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

## U. S. GENERAL ECONOMIC INDICATORS

| | April 1986 | March 1986 | April 1985 |
|---|---|---|---|
| Index of leading economic indicators | 179.2 | 176.6 | 166.7 |
| Budgeted outlays of the federal government ($ billions) | 81.510 | 79.700 | 83.214 |
| Budgeted outlays of the Department of Defense ($ billions) | 22.842 | 24.002 | 20.239 |
| Operating rate of all industries (% capacity) | 77.3 | 77.1 | 79.0 |
| Industrial-production index | 125.1 | 124.9 | 124.1 |
| Total housing starts (annual rate in thousands) | 2,009 | 1,930 | 1,851 |

## U. S. ELECTRONICS INDUSTRY SHIPMENTS

| Shipments ($ billions) | April 1986 | March 1986 | April 1985 |
|---|---|---|---|
| Communications equipment | 5.043 | 5.477 | 4.751 |
| Radio and TV receiving equipment | 1.014 | 1.043 | 0.941 |
| Electronic and electrical instruments | 4.697 | 4.591 | 4.699 |
| Components | 3.284 | 3.432 | 3.193 |

An 8% plunge in communications equipment sales pushed down overall shipments of electronics goods in April by 3.5%, to $14.04 billion. The drop brought electronics shipments for the first four months to $56.7 billion, just 1.7% more than a year ago. Reasons for the sluggish growth include a slowdown in U. S. companies' capital spending and the continued onslaught of imports.

Companies are being very conservative with capital outlays. The previous month's McGraw-Hill survey found that, excluding oil drilling, companies planned to raise spending on new plant and equipment in the U. S. just 2% in 1986. Communication-services companies in the survey reported even weaker capital spending plans. Reflecting the soft market, manufacturers of communication equipment projected that they would cut capital outlays by 3% this year.

April shipments also declined for radio and TV equipment as well as for electronic components. The only sector that managed an increase was instruments—up 2.3%. That rise, however, was not enough to offset the lackluster performance in other sectors, and the *Electronics* index fell 0.5%.

The evidence is in, and it's incontrovertible. When it comes to light, Anritsu runs second to the sun.

True, Anritsu's little laser diodes *are* powerful enough to raise more than a few eyebrows.

And Anritsu optical attenuators can cut *almost* any light source down to size.

And Anritsu optical power meters can take anything a *normal* fiber optic system can dish out.

But none of them can hold a candle to the sun, with its $900 \times 10^{23}$-or-so calories every second and 10-billion-year MTBF.

Still, if you take a closer look, you'll see a bright side to this story.

For instance, let's talk technology: does the sun have anything like Anritsu's laser-accurate outside diameter measuring system for optical fiber production?

In sophistication, Anritsu also has a clear edge. With optical time domain reflectometers and optical spectrum analyzers that give a clear, accurate picture of an entire fiber optics network.

And in terms of visibility, the Anritsu name has become almost an industry standard. Thanks to a dazzling range of measuring

instruments and light sources for all facets of fiber optic communications.

What about versatility? Simply no competition: Anritsu has more than 11,000 products and systems, and these extend to areas far beyond light. To rugged radio and telecommunications equipment. To public telephones, computers and data processing equipment. To measuring instruments for communications. The list goes on and on.

The sun is still safely #1 for now.

But we're on the move.

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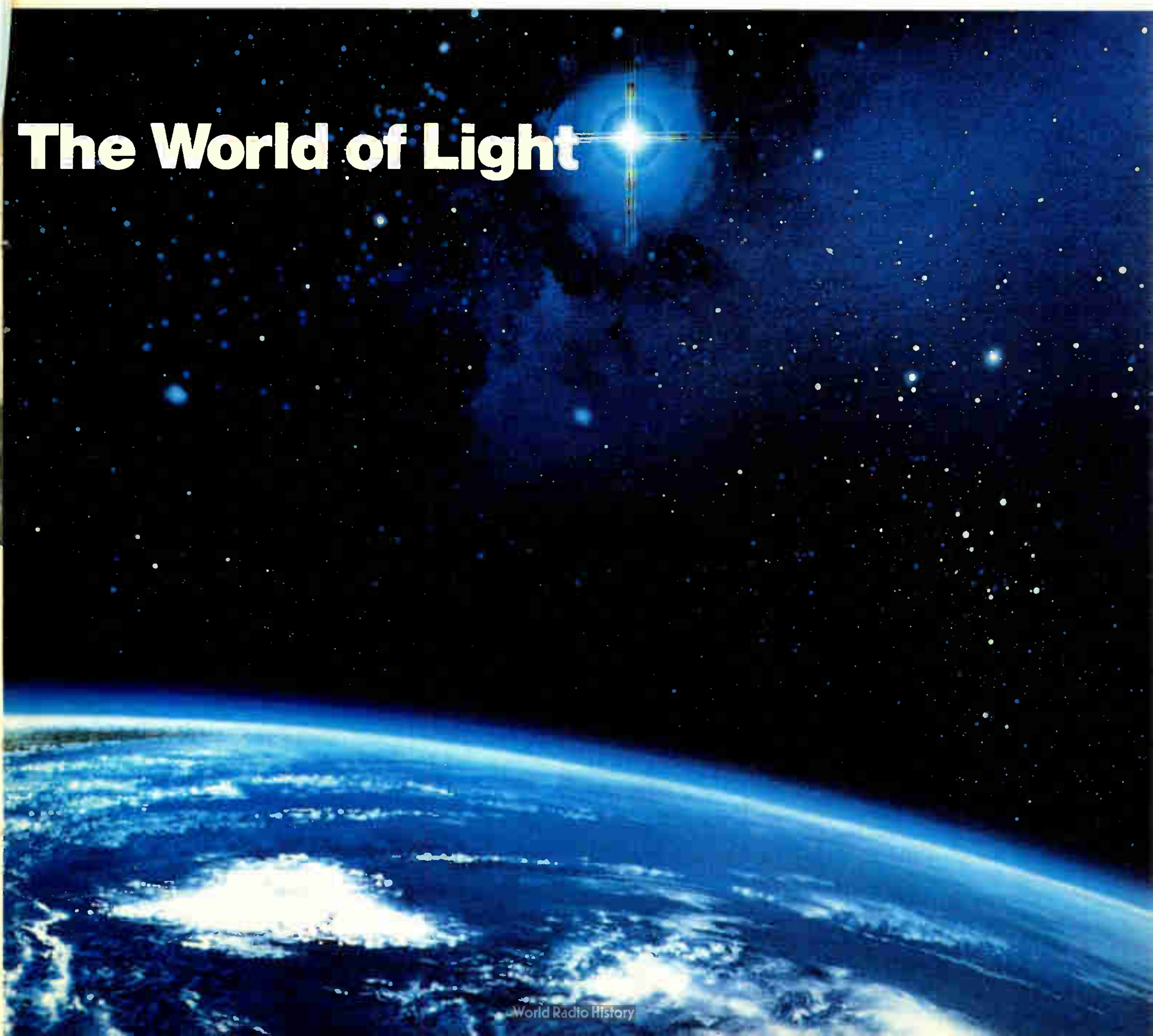
***As of October 1, 1985, Anritsu Electric Co., Ltd. became Anritsu Corporation.***



# NEW PRODUCTS

# LOW-COST LAN CARD SERVES BOTH IBM STANDARDS

## AT $395 PER NODE, K-NET SERVES EITHER TOKEN-RING OR PC NETWORK

At $395 per connection, K-Net is an inexpensive local-area-network card that's priced much lower than the typical $800 per node of competing networks. The LAN is also versatile: it is equipped to serve two personal-computer networking standards, IBM Corp.'s PC Network and its Token-Ring Network.

The K-Net network supports up to 255 personal computers and transfers data at 1 Mb/s. That rate is less than that of the 2-Mb/s PC Network standard and the 4-Mb/s standard for the Token-Ring Network. K-Net allows the user to run programs compatible with PC Network and Token-Ring Network software without modification because it fully simulates the IBM Netbios interface.

"K-Net allows users to integrate multiuser solutions, such as Multilink Advanced or PC-Slave/16, without modification," says Kimtron Corp. president John Kim. In addition, any multiuser application software written for use under PC-DOS 3.1 will work with K-Net.

**NO FILE SERVER.** K-Net does not require a file server. Any peripheral attached to one personal computer in the network—such as hard-disk and tape-backup subsystems, printers and plotters, and modems—can be shared by all other network users. The network also gives the user access to files on other personal computers. To prevent unauthorized access, a security feature has been included that checks a user's password before giving access to a network resource.

In addition, K-Net allows users to send files to a shared printer at the same time. Instead of hanging up the requesting computer when the printer is busy, K-Net will store the print file in a disk buffer, then print it when the peripheral becomes available.

When using K-Net, a manager can view other users' screens to monitor their activities and can broadcast a screen to all network nodes. Any network node can broadcast a one-line message to all other nodes.

With inexpensive twisted-pair wiring or standard telephone line with an RJ-11 modular jack, setting up a K-Net LAN is as easy as installing a phone. The network can be up to 4,000 ft long.

The network card fits into an IBM PC's short slot. Kimtron used very large-scale integration to pack all the features on the short card. "System reliability has increased because we have reduced the number of components," says Robert David, director of marketing. K-Net is available now.

Kimtron is also unveiling three diskless work stations that serve as low-cost alternatives to adding computers to LANs. The 4.7-MHz 8088-based KW-1 is priced at $995 and the KW-2, which uses a 8-MHz 8088-2, is $1,295. The KW-3 has a 80286 and is $1,995. *–Steve Zollo*

Kimtron Corp., 1705 Junction Ct., Building 160, San Jose, Calif. 95112.
Phone (408) 436-6550 [Circle 340]

# WINCHESTER DRIVES OFFER CHOICE OF INTERFACES

With its largest and fastest 5¼-in. Winchester drive family yet, Micropolis is giving customers a choice of the two most popular interfaces. The 10 new drives in the 1500 Series, which top at 382-megabyte capacities, offer as embedded features either the Small Computer System Interface or the Enhanced Small Device Interface. All the drives have average seek times of 18 ms.

**PRICE LEADER.** Micropolis is aggressively pricing its 382-megabyte drives at $5 per megabyte.

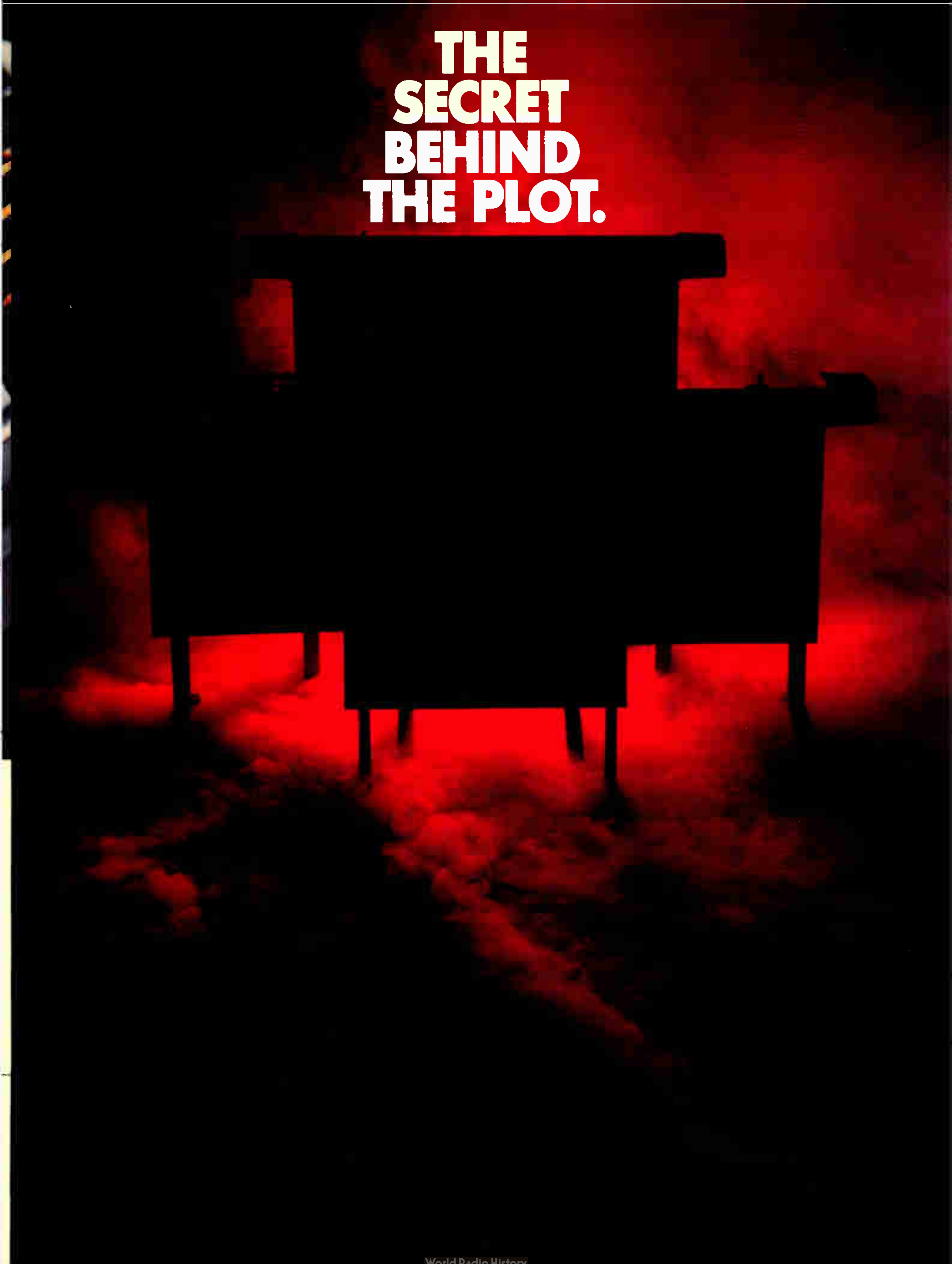
The company expects to have the units in production during the second half, says Chester Baffa, senior vice president of marketing and sales. "The extremely fast access time makes this product an excellent choice to replace larger and more costly drives." The price of the 382-megabyte version is about $1,900 for original-equipment manufacturers, in medium volume. This price amounts to about $5 per megabyte, Baffa says.

The Micropolis announcement comes on the heels of two other companies unveiling Winchester disk drives with embedded controllers. Just last week, Maxtor Corp., San Jose, Calif., began delivering a 5¼-in. 380-megabyte drive with an embedded SCSI controller for $3,400 [*Electronics*, June 9, 1986, p. 13]. Maxtor says that by next year, its drives will be in the same $5/megabyte price range. And two weeks ago, Miniscribe, of Longmont, Colo., announced a lower-capacity 170-megabyte drive with integral ESDI controller for $1,300 [*Electronics*, June 2, 1986, p. 56].

Micropolis is offering five drives in each interface, all boasting unformatted capacities ranging from 280 to 328 megabytes. The ESDI interface has a 10-

## NCC ROUNDUP

*Hot Las Vegas weather but a cold economy will greet the exhibitors and show goers at this year's National Computer Conference, opening this week in the famous gambling town. Despite the continuing recession, 400 exhibitors are betting that they can attract 70,000 visitors with their latest goods, which are covered in these three pages.*


THE SECRET BEHIND THE PLOT.

Mb/s transfer rate. Both hard and soft sectoring options are provided, permitting full compability with all ESDI controllers and applications. In the hard-sectoring option, users can select a sector size from eight standards or create a custom size by means of the Set Unformatted Bytes per Sector command.

The ESDI interface transfers data in the nonreturn-to-zero form, with data separation being performed on-board the drive. This simplifies controller design, says the company. Micropolis boosted the ESDI drives' usable disk space by taking the extra step of synchronizing data to the servo phase-locked-loop, eliminating the need to accommodate speed tolerance in the data format. ESDI also provides future growth opportunities using higher data transfer rates of 15 to 20 Mb/s as technology advances permit.

The SCSI drives have onboard controllers that provide a 1.25-Mb/s transfer rate between buffer and host. A proprietary implementation called the Micropolis High Performance Module provides the maximum possible data throughput when compared with other SCSI controllers, the company claims. Among other features, the 16-K-byte, dual-ported buffer with full parity eliminates the need for sector interleaving.

In the SCSI series, logical block addresses are automatically converted to physical locations for device independence. Data is buffered to allow for flexible transfer rates, in-line defect management with optional automatic bad-block reassignment, and data errors are automatically retried, corrected, or optionally deallocated. The intelligent SCSI offers features that provide for industry standard compatibility.

In the past, reliability has plagued small high-capacity drives. Baffa says the specification has been increased to 30,000 h mean time before failure. "This is a further step in reliability improvement, and an upgrading from 20,000 hours based on in-house test data and measured performance from approximately 200,000 drives," he says.

Shipments of the ESDI version are scheduled to begin in the late third quarter, with production volumes in the fourth quarter; the SCSI model will follow by one quarter. *–Ellie Aguilar*

Micropolis Corp., 21123 Nordhoff St., Chatsworth, Calif. 91311.
Phone (818) 709-3300 [Circle 343]

# A LOW-COST SWITCH BOWS FOR TOKEN-RING NETS

Bridge Communications has adapted the LanSwitch/1, its mass Ethernet local-area-network switch, for token-ring networks, at a price equal to that of the Ethernet version.

In March, Bridge combined an Ethernet controller with low-cost PBX termination technology to produce a communications server that would connect up to 64 Ethernet ports for $250 per node, which Bridge claims is an industry low [*Electronics*, March 17, 1986, p. 65]. Now Bridge will introduce a new communications server, the CS/1-TR, in which the Ethernet controller will be replaced by a controller for the IBM Corp. token ring built around the TMS 380 token-ring chip set developed by Texas Instruments Inc. for IBM.

The CS/1-TR server is the first in a family of token-ring products that Bridge has planned. Still to come are an Ethernet/ token-ring gateway, a token-ring network-management control server, and communications software for personal-computer commmunication on the token ring.

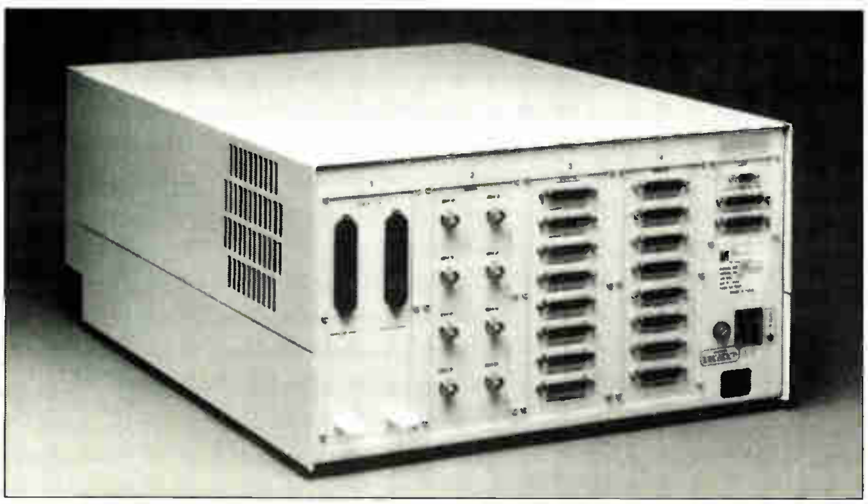
The CS/1-TR can connect as many as 64 token rings, each with 260 nodes, for a total of 16,640 users in a single system. Bridge president William Carrico says the server is designed to complement the IBM token-ring products, "with the added advantage of multivendor access and interconnection across the network."

IBM Personal Computers, asynchronous and IBM 3270 terminals, printers, modems, and ASCII and IBM hosts will be able to communicate across the net, Carrico says. When the development of the International Organization for Standardization's high-level protocols is complete, Bridge's server will use Xerox Corp. XNS software. Later versions will also support the Defense Department's Transmission Control Protocol/Internet Protocol.

Bridge is also offering separately the controller board it designed for the server. Called the TRC/M (for Multibus), the controller sells for $2,000 and can be shipped 30 days after ordering.

In announcing the server, Bridge also revealed that it has agreed to sign a license for the token-ring technology patented by Olaf Soderblum, and will pay a royalty on each system sold. Nevertheless, the token-ring server will be priced the same as the LanSwitch/1—$16,000 for a 64-port configuration. The server will be available 60 days after receipt of order.

Bridge Communications Inc., 2081 Stierlin Rd., Mountain View, Calif. 94043.
Phone (415) 969-4400 [Circle 341]



**TOKEN TOO.** Bridge is applying its PBX network technology to the Token-Ring Network.

# SYSTEM DIAGNOSES T-1 DATACOM LINES

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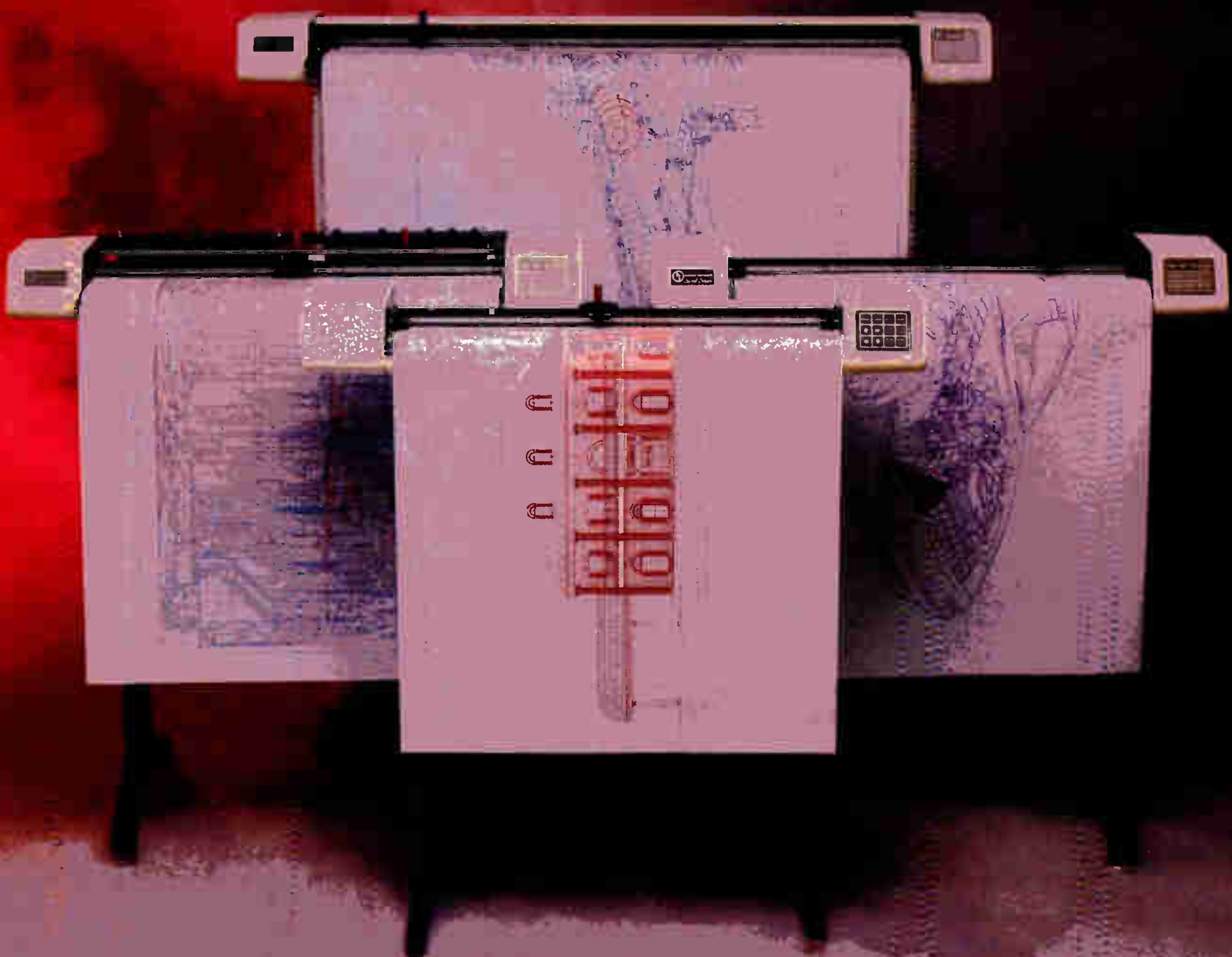

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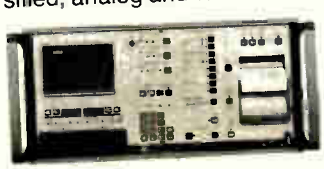

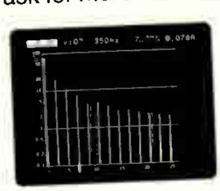

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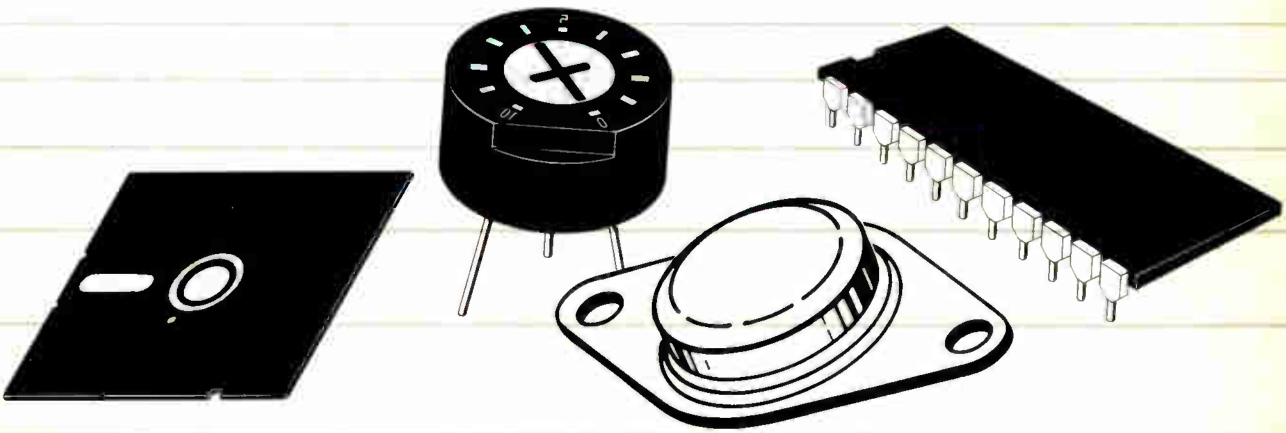

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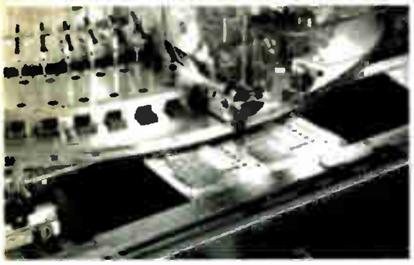

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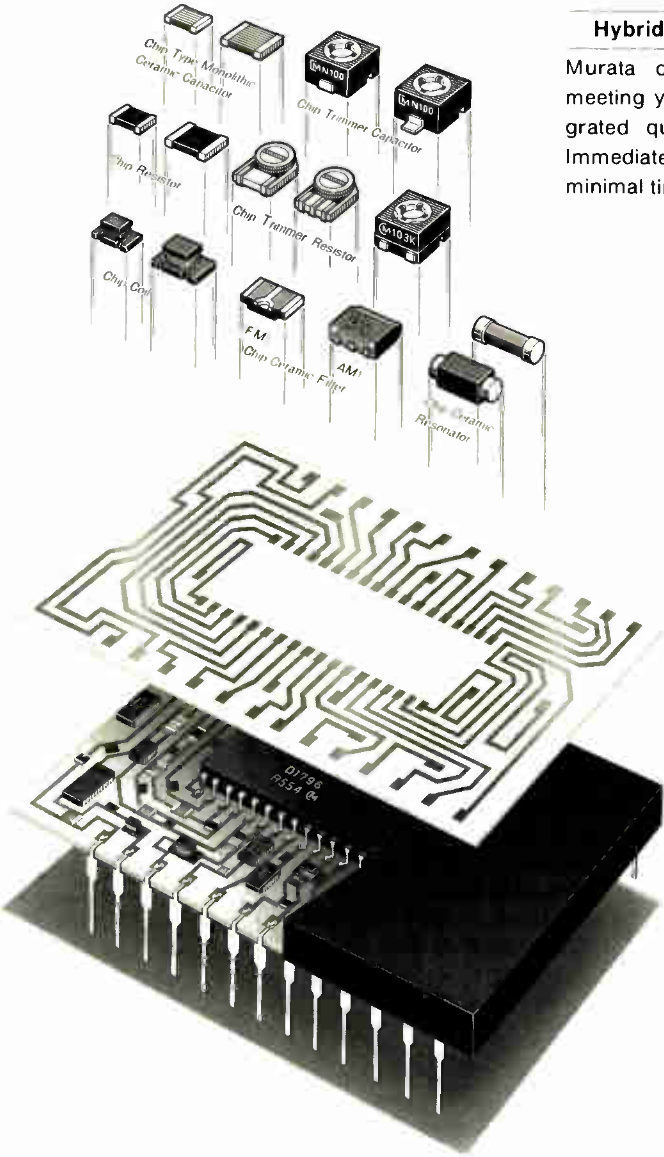


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- Estimates
- Development Plan
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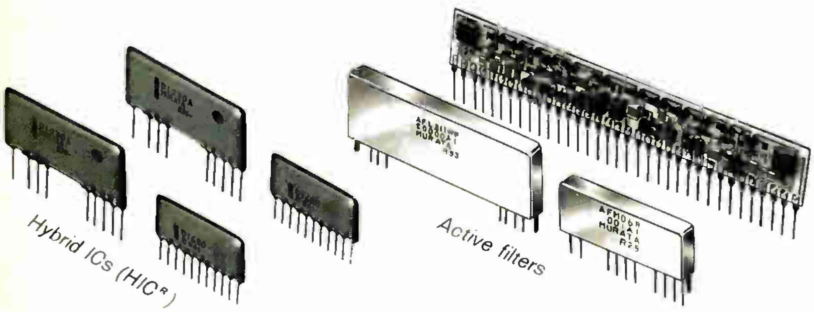
- Product Design
- Testing Sample Product
- Sample Evaluation
- Drawings Submitted for Approval
- Placing of Order/ Mass-production




**HYBRID IC (HIC®)**

(For further information, contact:

muRata

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# Anytime, Anywhere

## FUJITSU PLASMA DISPLAYS: clear from any distance

Fujitsu plasma displays feature a bright and clear display with thin, flat panels. The display is flicker-free and does not tire your eyes. It can be viewed from any direction. High contrast affords good visibility even in bright light. Naturally, you can expect a long service life, since the design is very reliable. The optimum display panel can be selected according to your requirements: dot matrix, characters and numerals, or special patterns. Fujitsu plasma displays are available in small- or large-size panels.

● Factory line display ● FA-equipment status display ● Taxi allocation display ● Bus destination and fare display ● Cash register display ● Petrol pump display ● Share price display ● Time display

**Numeric units (with drive circuits)**

| Model | Character height (mm) | Digits | Brightness (Cd/m²) | Exterior dimensions W × H × D (mm) |
|---|---|---|---|---|
| FPN020DRUD | 20 | 4 | 170 | 138 × 54 × 45 |
| FPN030DRUD | 30 | | | 172 × 54 × 45 |
| FPN040DRUD | 40 | | | 208 × 73 × 45 |
| FPN060DRUD | 60 | | | 304 × 125 × 55 |
| FPN060ARUD | | 1 | | 76 × 125 × 70 |
| FPN080ARUD | 80 | | | 94 × 151 × 50 |
| FPN120ARUD | 120 | | | 124 × 175 × 50 |
| FPR096ARUB | 96 | 1 | | 94 × 161 × 55 |

**Graphics unit (with drive circuits)**

| Model | Display area | | Number of display dots | | Brightness (Cd/m²) |
|---|---|---|---|---|---|
| | Height (mm) | Width (mm) | Vertical | Horizontal | |
| FPS0363SB | 38 | 323 | 16 | 135 | 170 |

**FUJITSU MIKROELEKTRONIK GmbH:**
Arabella Center 9. OG./A, Lyoner Straße 44-48 D-6000 Frankfurt 71, F.R. Germany Phone: 069-66320 Telex: 0411 963
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Furukawa Sogo Bldg., 6-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100, Japan Phone: National (03) 216-3211
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FUJITSU

**EASY TASK.** With its 2.048-Mb/s data rate, T-Scope easily captures and records all events on T-1 communications lines.

replay on another T-Scope or the Autoscope. The T-Scope is targeted at field-service organizations, large corporate data centers, and common carriers.

T-Scope consists of a base unit that records and replays data plus optional gear that enhances the unit's operation. The base unit displays data and interface information on its internal CRT. It also provides an easy-to-use operating system. The base unit, which looks similar to a portable personal computer, consists of the host processor, a CRT, a 20-megabyte Winchester disk drive for storing the data from communications lines, a floppy-disk drive, and two 50-pin bus connectors.

In the on-line run mode, the base unit provides a run-time screen that graphically depicts the status of the storage media. The status screens include an image of the disk filling as well as an indication of leadstate activity. Up to eight leadstates with data and clocks can be recorded.

Because the base unit records unframed data, a display mode is available to view the captured data and provides great flexibility in the presentation of the unframed data. The user loads a buffer of data from disk and displays the data in one of three selectable formats: hexadecimal, octal, or binary. Softkeys are used to shift data bit-by-bit on the screen. Support for code sets such as ASCII and EBCDIC will be added in the future.

The first optional module is the Trap and Framing Logic. This module makes it possible to frame serial data into recognizable codes and provides trapping on user-defined events. Up to eight traps can be set to start or stop recording or simply to mark the occurrence of an event. An event can be either a send-data or receive-data string of up to eight characters, with bit and byte "don't care" settings. An event can also be triggered by leadstate settings. The T-Scope can be controlled remotely, performing all functions at an unattended site. Available now, it is priced starting at $8,500. *–Steve Zollo*

Telenex Corp. Marketing Department, 502 Pleasant Valley Ave., Moorestown, N. J. 08057. Phone (609) 234-7900 [Circle 345]

# SYSTEM TEAMS 68020 AND MULTIBUS

Building computers around the Multibus has a distinct advantage for systems integrators. Peripherals and add-on cards to customize the computers are available from more than 200 manufacturers. Megadata is making use of that advantage with two multiuser Multibus-based 68010-based microcomputers that run under Unisoft's version of AT&T Bell Laboratories' Unix System 5.2. Come September, new versions will be available that will be built around the 68020 microprocessor and the 68881 floating-point coprocessor. They will increase performance fivefold.

Both the 8300 series model 4 and the desktop entry-level model 6 are built around the Motorola 68010 microprocessor and support from 2 to 16 users.

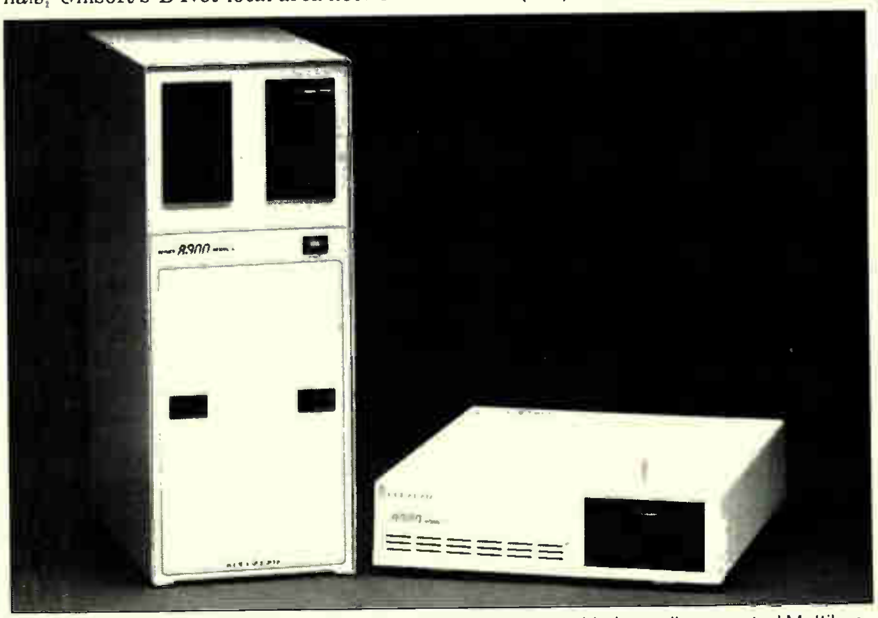
The basic model 4 system contains only two pc boards, with seven card slots available for adding I/O capacity, peripherals, magnetic storage, and additional memory. In its standard configuration, the computer has 1 megabyte of RAM, expandable to 16 megabytes. Also standard is a 26-megabyte Winchester disk drive and a 1-megabyte floppy-disk drive. Options include 40- and 140-megabyte Winchesters, a 45-megabyte streaming-tape drive, and a 9-track tape drive for exchanging data with mainframe computers.

The model 6 holds up to 6 megabytes of RAM and provides two additional card slots. It comes with a 26-megabyte 5¼-in. Winchester disk drive and a 1-megabyte floppy-disk drive. A 40-megabyte Winchester and a 45-megabyte streaming tape drive are optional.

Available software includes Cobol, Fortran 77, Pascal, Basic, and Ada languages. Communications options include Systems Network Architecture/Synchronous Data Link Control, which allows the computers to emulate the IBM Corp. 3274, 3276, 3278, and 3287 terminals; Unisoft's B-Net local-area-networking software; and Locus Computing Corp.'s PC Interface, which lets the computers act as file servers for IBM Personal Computers on a network.

The model 4 ranges in price from $8,235 to $12,985, and the model 6 is priced from $6,345 to $8,825. Both are available now. *–Steve Zollo*

Megadata Corp., 35 Orville Drive, Bohemia, N. Y. 11716.
Phone (516) 589-6800 [Circle 344]



**DYNAMIC TEAM.** Megadata teams the fast 68020 processor with the well-supported Multibus.

# IMAGE-PROCESSING MODULE WORKS LIKE A VMEBUS CPU

## DATACUBE BOARD IS BASED ON DSP CHIP FROM ANALOG DEVICES

Datacube has taken a powerful new digital signal-processing chip and come up with an image-processing module that functions like a VMEbus CPU board. Euclid is easily programmed to perform 8 million instructions/s. But because it operates like a standard CPU, the device should also find applications in such areas as speech analysis and seismic plotting with more than one dimension.

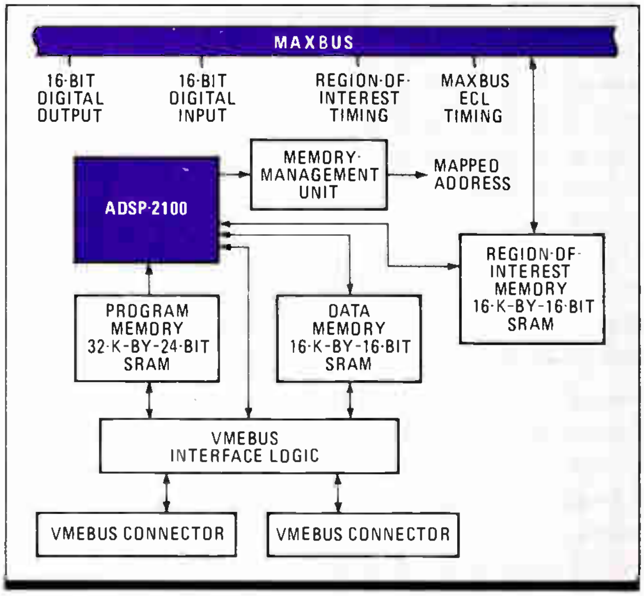
The board is the first commercial product to use Analog Devices Inc.'s ADSP 2100 chip [*Electronics*, Feb. 24, 1986, p. 89]. "We've surrounded the 2100 with the right tools so people can use it like a [Motorola] 68000 board" or other conventional microprocessor, says Shep Siegel, senior engineer at Datacube. "The ADSP-2100 lives on the Euclid like a 68000 or other conventional microprocessor," he says.

The board aims to fill the gap between specialized hardware, such as products designed for convolutions, and more flexible but slower software for fast Fourier transforms and the like. It can work alone or with the company's other MaxVideo image-processing modules [*Electronics*, Jan. 6, 1986, p. 89], and it rapidly implements signal-processing algorithms written in C and in the chip's assembly language.

**NO CONTENTION.** The VMEbus board is a von Neumann processor optimized for DSP applications, and the VMEbus interface is both a master and a slave. On board, Euclid has a writable 32-K-word static program memory store. Also standard is a dual-ported data memory for zero-overhead data transfer, which eliminates contention between local access by the ADSP-2100 and off-card VMEbus masters. This means a direct-memory-access controller or a CPU can load Euclid's data memory while the board is processing previously loaded data.

Standard software includes an ANSI Standard C compiler with in-line assembly facility and a library of ADSP-2100-optimized image-processing and numerical routines, which can be called from C or assembly-language programs.

Euclid has two address generators to double effective fetching speed, useful for functions such as FFTs that require both data and coefficients. The core processing of a typical two-dimensional FFT on a 256-by-256-bit image can be completed in 802 ms, says Siegel. Including all the data transfers over the VMEbus and a log-magnitude display increases processing time to 2.4 s. If executed along the Maxbus, adds Siegel, the entire operation can still be performed in less than 1 s.




**FAST HELPER.** As a coprocessing board, Euclid can perform convolutions and fast Fourier transforms at 8 million instructions/s.

A dynamic word-sizing feature, implemented in hardware, automatically sizes the byte into the word, circumventing the DSP chip's fixed word size. Because DSPs have limited address space, Datacube included a hardware memory-mapping unit with no additional wait states. By employing its 16-page memory-mapping scheme with programmable page values, Euclid users can address multiple 4-gigabyte address spaces.

A semaphore-passing facility is also provided to imbue the DSP board with CPU characteristics. This facility allows multiple processors to share common memory without contention and works much like the Motorola 68000 test-and-set instruction. It is implemented through an indivisible read-modify-write construction.

If used with other Maxvideo products for imaging applications, Euclid can transmit 16-bit data over the MaxVideo bus at a 10-MHz video rate. The data can be acquired from or sent to a 16-K-word RAM called region-of-interest memory. The region-of-interest interface can be used to transfer data at data rates of 20 megabytes/s without using the VMEbus.

The Euclid board will be available in the third quarter and will sell for $5,000 each. *–Craig D. Rose*

Datacube Inc., 4 Dearborn Rd., Peabody, Mass. 01960, (617) 535-6644 [Circle reader service number 338]

# DIGITAL TECHNOLOGY COMES TO CURVE TRACERS

The same digital technology that has modernized oscilloscopes is now helping to update curve tracers, the basic tool of the semiconductor industry. The Sony-Tektronix 370 curve tracer incorporates bubble memory, IEEE-488 programmability, and fancy cursors to give users the advantages of automation for faster testing, storing, and analyzing device-characteristic curves with greater reliability and less training than required for conventional tracers.

The 60-kHz digital storage curve tracer measures and displays characteristic curves on two- to four-terminal devices, including diodes, transistors, thyristors, FETs, and optoelectronic components. The 370 digitizes and displays waveforms on a 7-in. CRT. Alphanumeric readouts include vertical and horizontal scale factors, voltage/current step and offset amplitude, auxiliary voltage, and cursor coordinates.

Curve tracers have remained virtually

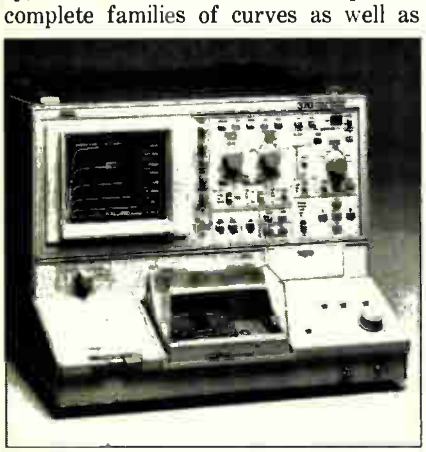
unchanged from when Tektronix pioneered them in 1968; indeed, the company's next most recent model, the 577, was introduced back in 1974. And with all its digital features, the 370 sells for just $15,000, compared with the 577's price of $13,000.

Tektronix has no competition in curve tracers, but its units do compete with other instrument types—for example, parametric analyzers from Hewlett-Packard Co. But although parametric analyzers are often compared with curve tracers, they are less sophisticated, Tektronix says, and don't offer all of the latter's features.

Parametric testers handle only wafers—they cannot test packaged components. Also, parametric testers are limited to low-power devices, whereas curve tracers handle medium-power devices.

The 370 can do a wide range of measurements, using grounded-emitter or grounded-base configurations. It has selectable ac or dc collector supply voltage ranging up to 2,000 V peak. This high voltage, coupled with a current sensitivity of 100 pA/division, allows extended breakdown-voltage measurements. For example, the instrument can test the new high-voltage power MOS FETs beginning to hit the market.

Thanks to the internal bubble memory, the user can save and recall up to 16 complete families of curves as well as



**GOING DIGITAL.** Tektronix has added a host of digital features to its new curve tracer.

16 front-panel setups. Tektronix' older tracer had to be set up manually each time a different part was going to be tested. Stored setups are recalled quickly on command or with the push of a button, both saving time and eliminating human error.

Another benefit the bubble memory brings is a comparison feature. The compare mode simultaneously displays real-time curves with those stored in memory, permitting comparison of the device under test with reference curves.

In a sequence mode, the 370 can semiautomatically step through up to 16 complete tests without requiring a controller. And devices can also be cycled through tests automatically under program control.

An instrument controller can program the 370 through its IEEE-488 interface. The controller can also get measurement results from the instrument for processing and analysis. The tracer can be hooked up to a plotter, enabling operators to make hard copies of characteristic curves—including alphanumeric data—displayed on the CRT.

**CURSORS APLENTY.** The 370 has a variety of cursors. Dot and crosshair cursors can be positioned on the screen to make precise voltage and current measurements. The dot cursor only follows the path of the waveform, providing a reading at any point. The crosshair cursor can be placed anywhere to provide a measurement.

A square box—called a window cursor—can be used to set maximum and minimum values for visual reference checks in go/no-go testing. If the part's measured value is within the box, the part passes; if the value is outside the box, the part fails.

When put in the envelope mode, the 370 displays the minimum and maximum excursions of the curves over time, such as thermal drift of the device under test. The curve tracer also features an averaging mode that improves resolution and measurement accuracy by reducing the effects of random noise. The curve tracer is available two weeks after ordering. *–Steve Zollo*

Tektronix Inc., P. O. Box 500, Beaverton, Ore. 97077.
Phone (503) 644-0161 [Circle 339]

## HP CALCULATOR HAS BUILT-IN EQUATIONS

Hewlett-Packard's Business Consultant calculator can solve built-in or user-defined equations without programming.

Users of the company's earlier calculators had to program the devices in the RPN language, which stands for Reverse Polish Notation.

The Business Consultant features a simplified user interface, algebraic data entry, and built-in programs for finance, general business, statistics, summing and number lists, mathematics, and time and appointments. In addition, specialized equations can be created and solved with the company's formula solver feature, which uses the calculator's menus and soft keys to solve user-created equations. Then users can solve for any unknown variable in the equations by using the numeric keys to type in the known values.

The Business Consultant has a four-line-by-23-character screen that displays messages and user prompts. The calculator, which will sell for $175, will be available in July.

Hewlett-Packard Co., Inquiries Manager, 1000 N. E. Circle Blvd., Corvallis, Ore. 97330 [Circle 372]

## TI CALCULATOR MAKES USE OF WINDOWS

The TI-95 Procalc programmable calculator features windows and menu prompts. It has five user-definable windows for easy prompting, a typewriter-like keyboard, a cartridge port for adding nonvolatile memory or application cartridges, and a peripheral port to connect a cassette recorder and printer.

The definable keys and windows let users choose and execute the 200-plus functions. Users can also program using the windowing feature and function keys to create virtually unlimited sets of functions. The TI-95 comes with 36-K bytes of ROM and 8-K bytes of RAM and runs under TI's Algebraic Operation System. Calculations can be made in decimal, hexadecimal, or octal number bases.

The TI-95 has a multiline, 31-character display. To be available in the fourth quarter, the TI-95 will sell for $200.

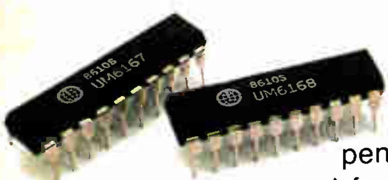
Texas Instruments Inc., Consumer Marketing, P. O. Box 53, Lubbock, Texas 79408 [Circle 373]

## INDUSTRIAL COMPUTER USES IBM PC ADD-ONS

The X-Rated computer features an air-to-air heat exchanger with two air loops driven by 4-in. fans that move air at the rate of 65 ft$^3$/min. Designed for harsh industrial environments, the X-Rated computer includes a 12-slot passive backplane that accepts all IBM Corp. Personal Computer/XT-compatible add-on cards. The CPU is also on a plug-in card. Up to three half-height hard-disk,

# Score A Winning Touchdown with UMC


With backing from UNITED MICROELECTRONICS CORPORATION, one of our customers scored a winning touchdown with a voice control IC last year. He netted a profit of 2.5 million dollars on just one product. This is one of the many examples of how UMC helps its customers score financial goals.




UMC scored its first touchdown by becoming profitable 6 months after it went into operation and has been making a profit and registering phenomenal sales growth annually since then. Last year, 4 quarters of penalties left most companies sitting on the bench and several others were ejected from the game. UMC, however, still romped to a sales growth rate of 24.4%, which was the fourth best in the world and outscored 92% of the IC industry.

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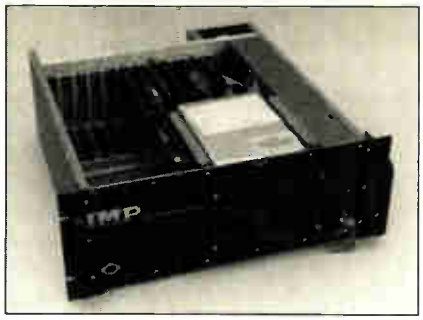
## COMPUTERS



floppy-disk, or tape-storage units can be mounted internally and are accessible through the front panel.

Both 3½- and 5¼-in. disks fit the configuration. Front-panel LED status indicators monitor the internal power-supply voltages. The ruggedized aluminum chassis is assembled with screws for access to all parts of the computer and fits either a chassis or a rack-mounted configuration.

The X-Rated computer is available from stock and sold by component. A complete chassis with power supply, fans, backplane, and card holders costs $2,050 each to original-equipment manufacturers.

Electro Design Inc., 690 Rancheros Dr., San Marcos, Calif. 92069.
Phone (619) 471-0680 [Circle 356]

## 68020-BASED FAMILIES JOIN COMPUTER LINE

Motorola Computer Systems, formerly Four-Phase Systems Inc., has added two 68020-based families to its line of computers. The System 8000, which targets users of office information systems, is built around a 16.6-MHz 68020 microprocessor in a VMEbus architecture. It runs under AT&T Co.'s Unix System V operating system. The Vision/32, also a VMEbus system, is targeted at on-line transaction processing. The products are the first examples of how Four-Phase has been vertically integrated into the Motorola structure—applying Motorola semiconductors and boards in computer systems.

The System 8000 family consists of two models. The model 200 supports up to eight users and the model 400 can handle up to 32. Available next month, the model 400 will sell for $22,335; when available in September, the model 200 will start at $15,690.

The Unix-based Vision/32 machine is compatible with Four-Phase's series 4000 and 5000, which use the Vision applications development tool. The Vision/32 supports eight users and will be available in September for $17,195.

Motorola Computer Systems Inc., 10700 N. De Anza Blvd., Cupertino, Calif. 95014.
Phone (408) 864-4122 [Circle 358]


### Advertising Sales Staff

**Atlanta, Ga. 30319:** Joseph Milroy
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[404] 252-0626
**Boston, Mass. 02116:**
M. E. "Casey" McKibben, Jr.
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# ELECTRONICS WEEK

## MAIL-SORTING SHOOTOUT DELAYED

Competition to provide the next generation of mail-sorting equipment has been suspended for at least two months while U. S. Postal Service officials review the agency's procurement practices. The inquiry follows a senior official's guilty plea to charges of receiving illegal payments that prosecutors say were aimed at swinging orders to Recognition Equipment Inc. The company denies any wrongdoing and says it is not a target of the current grand jury investigation. This month, Recognition Equipment and another Dallas-area producer of optical-character-recognition equipment, ElectroCom Automation Inc., shipped equipment to Phoenix for competitive tests. At stake is more than $320 million in sales to the Postal Service [*Electronics*, April 28, 1986, p. 19].

## 4-BIT PROCESSOR BUILT WITH GaAs

A gallium arsenide 4-bit microprocessor kicks off an ambitious new line in the III-V materials group that McDonnell Douglas Astronautics Co. is designing at its Microelectronics Center, Huntington Beach, Calif. The company calls the MD2901 chip, which uses the Advanced Micro Devices 2901 bit-slice architecture, the first GaAs microprocessor that has proved successful in tests. Produced on the center's pilot GaAs line, it draws 135 mW, one tenth of what silicon requires, but the speed has not yet reached the goal of 100 million operations/s. McDonnell Douglas says development of a 32-bit processor is under way.

## NEW FRENCH FIRM TO MAKE IR ARRAYS

A new company has been set up in Paris to consolidate France's development and manufacture of advanced infrared detectors needed for weapons and space systems [*Electronics*, June 9, 1986, p. 40]. The company, called Sofradir, is 40% owned by Thomson CSF, 40% by Société Anonyme des Télécommunications, and 20% by Commissariat à l'Energie Atomique, the French atomic-energy agency.

## AMDAHL TOPS R&D SPENDERS

Electronics producers figure prominently among the top spenders for research and development in the U. S. in 1985. According to a survey by *Inside R&D*, a weekly publication, for the fourth year in a row Amdahl Corp. led all the rest in R&D dollars spent per employee, at $19,500, and in R&D spending as a percentage of sales, at 15.6%. The average per-employee figure was $5,440, and the average percentage was 5.5%.

## ERICSSON GETS TOE IN THE U. S. DOOR

In an important boost for the campaign by LM Ericsson AB to penetrate the U. S. market for public telecommunications equipment [*Electronics*, April 21, 1986, p. 57], Mountain Bell has signed a letter of intent to conduct a trial of the Swedish company's AXE digital switching system. Ericsson Inc., the American subsidiary based in Richardson, Texas, says a contract for the trial should be signed by midyear.

## TANDY SPINS OFF FOREIGN OUTLETS

Electronics retailer Tandy Corp. is spinning off its 2,100 international outlets in an effort to concentrate more on U. S. markets. The Fort Worth, Texas, company intends to create separate publicly held companies to take over its outlets in Australia, Belgium, Canada, England, France, the Netherlands, and West Germany. Tandy Electronics Ltd. will handle all international outlets except those in Australia, which will be placed under Tandy Australia Ltd. Both companies will be two principal subsidiaries of a new firm called Intertan Inc., according to the plan tentatively approved last week by Tandy, which owns and operates the Radio Shack retail chain.

## WIDCOM FILES CHAPTER 11

Widcom Inc. has filed for Chapter 11 bankruptcy protection. The Campbell, Calif., company developed an advanced codec that makes possible full-motion video transmission at 56 kb/s, but it has been unable to develop what it thought would be an expanding market for teleconferencing. It has also been embroiled in a lawsuit over technology rights with Compression Laboratories Inc., which, like Widcom, was founded by Robert Widergren. He resigned from Widcom last March.

## ARETE THE OEM IN ARMY DEAL

The Army's $250 million contract to the Sperry Corp. for Unix-based multiuser superminicomputers has resulted in a $100 million order to Arete Corp. of San Jose, Calif., Sperry's original-equipment manufacturer. Deliveries of the Arete 1100 and 1200 series computers will begin in August and continue over a three-year period. Sperry will supply peripherals and applications software, and maintain the systems.

## COMPAQ EXPANDS HEADQUARTERS

In a move that the company says will keep the focal point of future expansion in northwest Houston, Compaq Computer Corp. has more than doubled its land holdings and begun increasing its headquarters complex in Houston. Last week, Compaq announced it has purchased 94 acres of land next to its present 55-acre site. The first phase of construction is expected to be completed in a year and a half, adding to offices and manufacturing area.

## XIDEX, WESTERN SIGN OEM DEAL

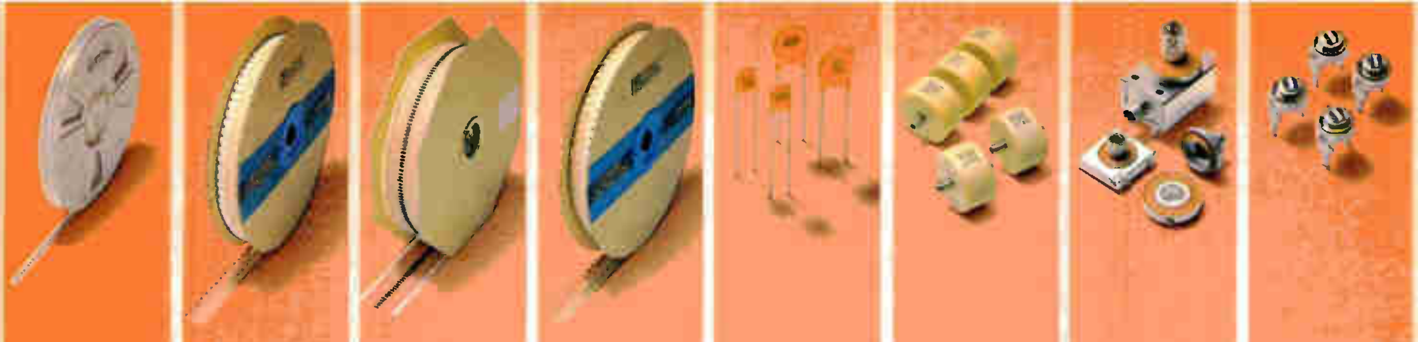
Western Digital Corp. of Irvine, Calif., will manufacture a line of peripheral storage products for Xidex Corp. of Mountain View, Calif., under an agreement valued at $20 million over the next year. Xidex, which will market the products worldwide through its distribution network, itself produces flexible and rigid media. Shipments are to start in late June.

## AUSSIES PLAN FIBER LINK TO N. AMERICA

A billion-dollar fiber-optic network, billed as the largest project of its kind to date, will link Australia, New Zealand, and North America. It will be built by the Overseas Telecommunications Commission, Australia's international telecommunications authority, and the New Zealand Post Office. The first phase will connect Australia and New Zealand by 1991, with additional branches planned by the middle of the next decade.

## EXPERT SYSTEMS: $400 MILLION IN '86

The infant expert systems industry is now established, with North American users this year spending more than $400 million in that area. That's the conclusion of a report published by Ovum Inc., Redwood City, Calif., which forecasts a North American market valued at $1.9 billion by 1992. The authors of the report say their conclusions are based on a survey of 1,000 projects.



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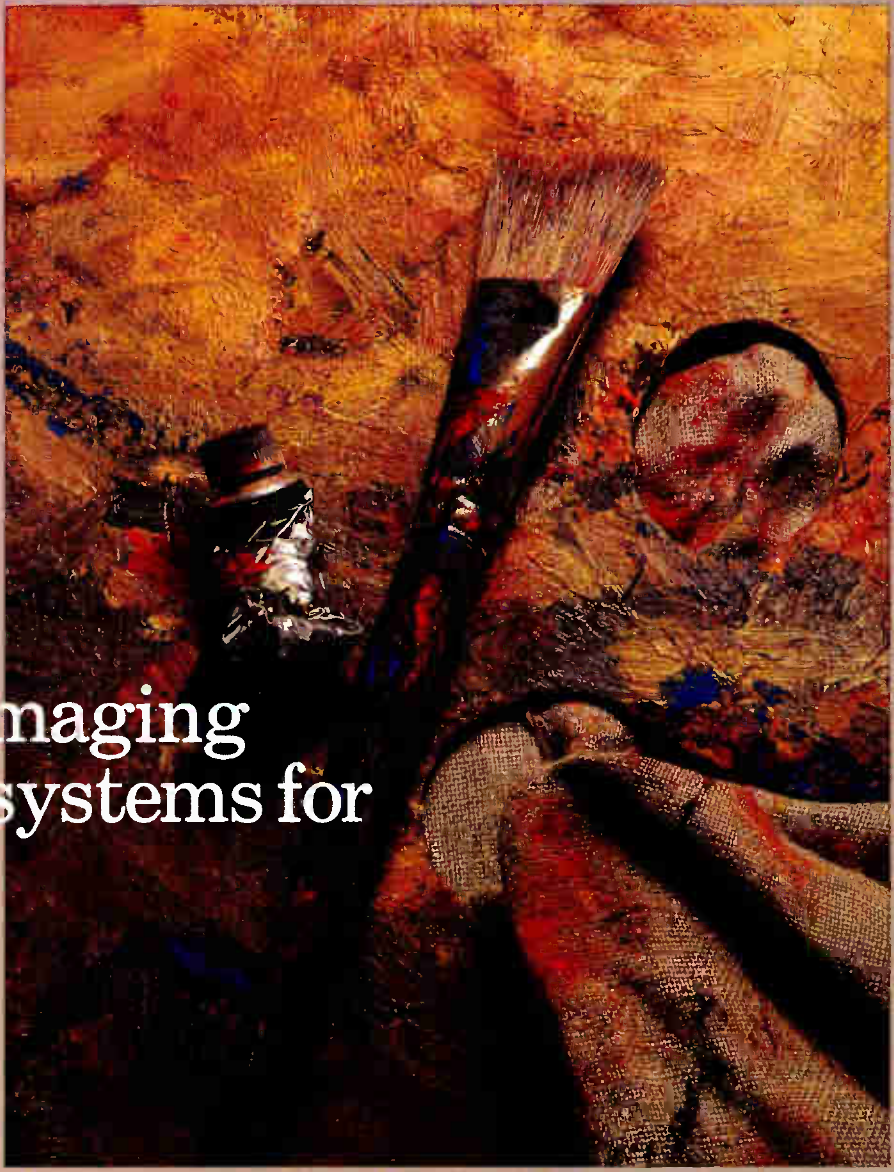

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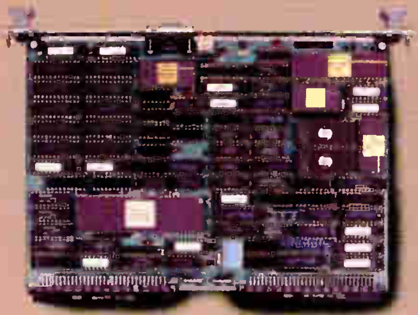

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