BREAKING THE LINEAR BOTTLENECK

SURPRISE! THESE ANALOG CHIPS KEEP UP WITH SPEEDY DIGITAL SYSTEMS/61

- CRYSTAL COMES UP WITH THE FIRST 12-BIT FLASH CONVERTER IC/67
- ANALOG DEVICES' ASICs GRAB DISK DATA AT TWICE THE SPEED/75
- MAXIM'S PROGRAMMABLE FILTER OUTPERFORMS THE FIELD/85
PG-1281 virtually redefines "high performance". With this new Matrox color display processor at the heart of an IBM PC AT, 386 PC, or compatible, a true professional workstation is born. Enhanced by four custom gate arrays, the PG-1281 is the fastest TMS34010-based board in the world today... and you have all the power of high-priced workstations at a fraction of the price!

- 1280 x 1024 resolution
- Full 64-bit bandwidth
- 65,000 vectors/second
- 100 million bits/second BITBLT
- Up to 1.5Mb on-board RAM
- Downloadable user code for easy application development
- Optimized drivers for major CAD packages
- Compatibility with all current graphics standards: Windows, X Windows, CGA, VDI, PGA, and more...
- Optional high-speed 3D coprocessor and EGA/VGA add-on modules.

If you need the best graphics performance available today, you need the PG-1281. For more details call us – fast!

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Circle 900 on reader service card

Have you been looking for the convenience of the ST Connector, HP quality and affordable pricing? Look no more. The DC to 50 Mbaud performance, uniquely efficient optics and 4 km range of Hewlett-Packard's fiber optic transmitters and receivers have already made them a designer's favorite. Now they are available for use with the popular spring-loaded, quick-twist ST Connectors at extremely competitive prices: as low as $12.50 in quantities of 1,000.*

HP's ST transmitters and companion ST receivers are completely specified with 62.5/125, 100/140 and 50/125 μm fiber sizes. For transmitters, coupling repeatability is an exceptional 0.2 dB and MTBF @ 40°C exceeds 4,000,000 hours. No mounting hardware is required. Units can be auto-inserted and wave-soldered.

Fire-you-up sale: 90 days only!
Save 80% off the regular evaluation kit price! For the next 90 days order the complete HFBR-0410 kit**, for just $10.00. (One to a customer, please!) Make checks payable to Hewlett-Packard Company and send with this coupon and your business card to Monte Smith, Hewlett-Packard Components Group, 370 West Trimble Road, Mail Stop 91-1G, San Jose, CA 95131.

I'd prefer an SMA connector evaluation kit for $10 instead.

**Kit includes an HFBR-1412 Transmitter, HFBR-2412 5 megabaud TTL receiver, and 3 metres of AT&T's 62.5/125 μm fiber optic cable with plastic ST ferrules.

For more information, call the Hewlett-Packard sales office listed in your telephone directory white pages and ask for the Components Department. To order, contact your nearest HP distributor. In the U.S., Almac Electronics, Hail-Mark, Hamilton/Avnet, or Schweber. In Canada: Hamilton/Avnet or Zentronics Ltd.

*ST** is a registered trademark of AT&T for Lightguide Cable Connectors. #U.S. list price.
MATTERA: Keeping track of the critical design basics.

As the business of designing electronics gets more sophisticated, technical managers and engineers struggling to stay abreast of the latest technology often find that they are not keeping up with the latest developments in the basic tools of their work, the components that make up the systems. To help close that gap, we are launching in the next issue our new monthly Technology Series.

The editor of the series will be Lucinda Materia, who is one of the most highly respected editors in the electronics trade press. She will be returning to the Electronics family—she was our Components Editor back in 1975—after serving as editor-in-chief and publisher of Electronic Design. Lucinda’s years as an industry observer have enabled her to build a network of solid contacts and sources from coast to coast and overseas.

The emphasis in our Technology Series will be on fundamentals. It will cover each of three key areas—analog and power, components and interconnections, and test and measurement—four times a year.

Fundamental technologies, like components, and instruments are the ones that the senior designers and technical managers must deal with most often,” Lucinda says. “Yet surprisingly, finding information about these important subjects is frequently difficult. So our special sections will be tuned to their principal technical information needs in these critical areas.

The topics to be treated have been carefully selected, and range from data converters to function generators, operational amplifiers to digital multi-meters, and surface-mount passives to oscilloscopes. “The reason we are focusing on these topics,” says Lucinda, “is that they are so critical to the everyday aspects of a design project. When an engineer undertakes a design, the particular power supplies or interconnections that he is going to use are generally the last things in his mind. Instead, he is occupied trying to select the microprocessor, or the graphics processor, or the operating system—and the coverage of these areas in Electronics is already top-notch. So we’re going to put on the table exactly what he needs to make the basic decisions.”

We recognize that the technical managers and engineers who read Electronics have special information needs when it comes to traditional technology areas. The series will provide technical interpretation, perspective, and assessments that can move them faster to their goal—speeding up time-to-market with the right product.

“The articles will be different from the typical how-to-design article found in other industry publications,” notes Lucinda. “They will be geared for the Electronics reader, the high-level technical manager. Thus, they will deal with technical issues, examine trends, and unravel complex technology topics.”

Lucinda adds, “Since we announced the series, we have been getting a very positive reception. In speaking to company officials, I find a lot of enthusiasm. Many of them have been calling me with ideas for articles.”

PUBLISHER'S LETTER

Harry Almond

Mattera: Keeping track of the critical design basics.
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Narrow your horizons.

Put your hard disk controller on a single chip.

Twenty chips and a board is too much hardware for a hard disk controller. Any engineer would agree. So we focused our attention on turning all that into a single chip: the Am9590 Hard Disk Controller.

The Am9590 can control up to 4 drives allowing for any mix of hard and floppy drives. It supports ESDI, ST506/412 or standard double density floppy disk interfaces. Use the Am9590 with its companion chip the Am9582 Disk Data Separator to design your current ST506 system and you've got an easy upgrade to ESDI system performance for the next generation. Or you could always start that next generation now with the Am9590 as a stand alone.

On-chip DMA with data mapping.

We gave the Am9590 on-chip DMA with data mapping (which will come in handy when you're working with UNIX). Then we added dual on-board sector buffers to allow for Zero Sector Interleave. This simple way of organizing sectors means that access time is bounded by drive capabilities—not controller limitations. And it leaves the CPU free to do the things it does best.

On-board EDC.

The Am9590 even has on-board EDC. Select an error detection code (CRC-CCITT) or one of two error correction codes (Single or Double Burst Reed-Solomon). Or if you prefer, the Am9590 provides handshake interface to your own external ECC circuitry. All this adds up to maximum data integrity.

And it's easy to use. A comprehensive high level command set (with command chaining) allows for independent operation without constant CPU intervention. You can even shorten your design cycle with an evaluation board, development software and a BIOS driver.

If all this sounds interesting, get in touch with us for more information. Once you've used the Am9590 Hard Disk Controller, you'll understand why the narrower view can be very broadening.
Keep a close eye on Apple Computer International: it's already beginning to look like the company that its U.S. parent aims to be in the 1990s

I'm going to let you in on another little secret. It's about Apple Computer. I know, I know. You already know all there is to know about the legendary personal computer maker. First it was founder Steve Jobs who stared out at you from all those magazine covers; recently it's been John Sculley, the former "sugared water" salesman who molded an out-of-control entrepreneurial company into a more professional organization. So much has been written about Apple, you say, that there can't be any secrets left. But there are. Fortune magazine may have published six long pages on the PC maker last month, but it didn't print word one about Apple outside the U.S. And that's the real secret: Apple Computer International is the tail wagging the corporate dog.

Keep a close eye on Apple International: it's already beginning to look like the company that its U.S. parent aims to be in the 1990s. It's moving into business markets at a very rapid clip, faster than its domestic parent. It's interested in making acquisitions: system-house integrators for the multi-vendor environment, for example. It has its own dedicated flexible manufacturing, a world-class plant in Cork, Ireland, that builds 27 products on one line. Apple is also growing faster overseas than it is in the U.S. "There has been an acceleration of our growth," says Michael H. Spindler, International president and resident genius behind Apple's overseas success. "Two years ago, we accounted for 20% of Apple's business; now we're 30% of the corporation," he declares. In those two years, overseas profits doubled because International was faster in switching over to the Macintosh.

In 1981, International did only $98 million. But since then, it has shot up at a 40% compound annual rate, to $743 million in fiscal 1987. Says Spindler: "We think we can grow 35% annually over the next few years, hitting $1 billion long before this decade is over." Some experts expect him to account for more than one-third of Apple revenues by 1990, growth that would make Apple more successful overseas than any U.S. computer maker but IBM. To keep up this momentum, International has just moved into phase two in Europe: "Our goal is to make us into a European company, so that we look and feel like a European enterprise," Mike says. This means an operation as self-contained as possible, sourcing almost entirely locally. And it will do its own R&D, with software and communications efforts located in Paris.

ROBERT W. HENKEL

Electronics / December 17, 1987
Amplifier Arsenal

50KHz—2000MHz, Low Noise 100mW output Gain Controlled from $69.95

Our ZFL-2000 miniature wideband amplifier hit a bulls-eye when we introduced it last year. Now we’ve added more models to offer you a competitive edge in the continuing battle for systems improvement.

The ZFL-2000, flat from 10 to 2000MHz, delivers +17dBm output and is priced at only $219.

Need more output? Our ZFL-1000H, flat from 10 to 1000MHz, delivers +20dBm output.

Is low noise a critical factor? Our ZFL-500LN and 1000LN boast a 2.9dB NF.

Variable gain important? Our ZFL-1000G, flat from 10 to 1000MHz, delivers +3dBm output with 30dB gain control while maintaining constant input/output impedance.

Searching for a high-quality, low-cost amplifier? Our ZFL-500 flat from 50KHz to 500MHz, delivers +10dBm output for the unbelievable low price of only $69.95. Need to go higher in frequency? Consider the ZFL-750, from 0.2 to 750MHz, for only $74.95. Or the $79.95 ZFL-1000, spanning 0.1 to 1000 MHz.

One week delivery... one year guarantee.

SPECIFICATIONS

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<th>MODEL</th>
<th>FREQUENCY (MHz)</th>
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* 30dB gain control **+15dBm below 1000MHz

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C101 REV.C

Electronics / December 17, 1987

World Radio History

Circle 9 on reader service card
AGCS family now expanded to 11 devices — see box at right for details.
Finally, graphics to match your imagination...now more than ever.

Imagine a graphics architecture so powerful, you can achieve 16K-by-16K resolution. So effective, you can add virtually unlimited planes of color without degrading performance. So flexible, you can integrate it into an existing design or use it to build an entire range of new systems.

That’s the Advanced Graphics Chip Set from National Semiconductor.

By using a multiple-chip, modular approach, the Advanced Graphics Chip Set avoids the design compromises and limitations of single-chip solutions.

That gives you two unprecedented benefits: performance and flexibility.

Which means you can design exactly the type of system you need with exactly the level of performance your application demands.

For example, you can integrate part of the chip set with an existing general-purpose microprocessor for a low-end display.

Or you can utilize the chip set’s full capabilities for a high-end, high-performance, high-resolution CAE/CAD workstation or laser printer — with virtually unlimited planes of color. Yet with the same high-speed performance as a black-and-white application.

In fact, you can design an entire range of graphics systems without having to “reinvent the wheel” each time, by using the same hardware building blocks and the same central software in each of the systems.

THE MULTIPLE-CHIP SECRET

The secret to all this flexibility and performance is our unique multiple-chip, modular approach. Rather than trying to squeeze all the important graphics functions onto a single chip — which would require some significant design and performance compromises — we’ve partitioned appropriate functions onto individual building-block ICs. This allows us to optimize the design of each chip, and allows you to optimize your own design for your particular application.

GRAPHICS WITHOUT LIMITS

What matters most about the Advanced Graphics Chip Set, of course, is what it does for you. And that answer is clear when you consider its high performance, its modular approach, its open architecture, and its programmability: It gives you graphics without limits. It gives you true design freedom. It gives you the opportunity, for the first time, to design a graphics system “custom fit” to your exact specifications.

So what are you waiting for? If you’re tired of those limited single-chip solutions bogging down your designs, take a look at the Advanced Graphics Chip Set. And learn how you can design a graphics system to match your needs...as well as your imagination.

For more information and availabilities, just contact your local National Semiconductor Sales Engineer or write:
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Advanced Graphics
P.O. Box 58090
Santa Clara, CA 95052-8090
This blazing 64K SRAM, with 12ns address access time, is twice as fast as any non-Performance 64K. It joins our family of 64K architectures—all with 6 transistor storage cells to optimize for performance, margins, temperature range, and supply tolerances.

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<td>P4C164</td>
<td>8K x 8</td>
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*Also available: Common I/O with output enable and separate I/O.

For optimal packing density, our standard 64K SRAMs are delivered in the popular 0.3" package widths, in either hermetic or plastic.

But that's not all. While others are still trying to catch up to the pace set by our 0.8 micron channel lengths and 2.75 micron metal pitch, we have pushed the frontiers of technology out even further. Now Performance's PACE Technology™ features 0.7 micron effective channel lengths, and 2.25 micron metal pitch. (As we've said before, metal pitch is the design rule that separates the men from the boys in VLSI technology.)

All of our chips are made here in our Sunnyvale facility for six-inch wafers, which has now attained Class 1 status.

Memory technology with the highest speed and greatest density gives you faster systems at a lower cost. So don't be left behind. Call the company that is ready to deliver the performance your system needs.

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Telex: 6502715784
FAX: 408-734-0258

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Circle 19 on reader service card

I want a faster system! Please send me detailed information on your SRAMs.

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COMPANY ________________________
ADDRESS _________________________
CITY/ST/ZIP _____________________
PHONE __________________________

Electronics
12/17/87
While biCMOS processes have attracted a stronger following, many designers worry that submicron geometries could restrict biCMOS performance because they would limit the drive capabilities of the on-chip devices. That’s not so, however, according to a group of Hewlett-Packard Co. researchers who described work on an experimental 0.5-μm process at the International Electron Devices Meeting in Washington last week. Testing the process in various ring oscillators, the Palo Alto researchers achieved delay times of 406 ps—two-thirds that of a pure 0.5-μm circuit. What’s more, the process yielded relatively high-performance bipolar devices with cutoff frequencies of 7.5 GHz at 1.5 mA. HP was not alone in singing the praises of sub-micron biCMOS. A group from Texas Instruments Inc. unveiled details of its 0.8-μm process, calling it the “next generation of very high-performance, low-power logic and memory products.” The TI group showed details of a 16-Kbit ECL/CMOS static random-access memory, with a six-transistor cell of only 118 μm². That kind of density could yield a 256-Kbit SRAM of 90,000 mils², which could fit in a 400-mil package and boast an access speed of just 7 ns.

AT&T DEVELOPS A BETTER WAY TO PROBE VLSI CHIPS

Probing, characterizing, and timing VLSI circuits has always been daunting, but now a researcher at AT&T Co.’s Bell Laboratories has found a way to do the job quickly and nondestructively. Janis Valdmanis’s technique can resolve timing signals down to 0.3 ps—100 times better than conventional electronic measurement systems. The entirely external technique can be used on any kind of material including silicon, gallium arsenide, ceramics, or hybrid circuits, and requires no specially designed test circuit on the chip itself. The probe used is a pyramid-shaped crystal of lithium tantalate attached to a quartz rod. Sampling and triggering pulses from two laser beams are focused into the tip, which can be placed close to any point on the chip using an X-Y-Z table for accuracy. Local electric fields at any node affect the birefringence of the crystal, and the effect on the intensity of the pulses can be measured.

U.S. CHIP BUSINESS IS FORECAST TO GROW 17 TO 20% IN 1988...

Most semiconductor experts are cautious about the prospects for 1988 but one notable exception is Charles Clough, president of Wyle Laboratories, a leading chip distributor. He’s predicting strong 17% to 20% growth for the U.S. industry. Clough’s upbeat view is based on the lean inventories of his customers, he says. “They are buying for consumption, not to stockpile,” he explains. “If anything, inventories are lower than a year ago.” Other developments in addition to healthy inventories point to a “year of good, digestible growth,” he adds. These factors include continuing strong demand for Intel Corp.’s 80386 microprocessor and the growing role of integrated-circuit technology in automobiles.

...AND NEW PRODUCT-CYCLES MAY FEND OFF ANY COMPUTER RECESSION

Outstanding performances by the leading computer makers will help fend off an industry-wide recession in 1988, say computer analysts at Sanford C. Bernstein & Co., a New York investment, research, and management firm. The firm predicts earnings growth between 25% and 50% for Compaq, Hewlett Packard, IBM, and Sun Microsystems, all of which are in the early or middle stages of new product cycles. Strong 15% to 25% growth is also expected from Digital Equipment, Control Data, Cray, Honeywell-Bull, and Wang Laboratories. The company says that growth in the computer industry is more closely tied to product cycles than to overall capital spending, the indicator of industry health that is watched most closely.
TIRED OF THE SAME OLD CHIP?

It's the same old story. Static RAM suppliers come out with new claims based on, what else, speed. And with everybody touting speed, they all start looking alike. Until you look at reliability.

That's where INMOS breaks the mold.

At INMOS we've developed SRAMs that give you high performance without compromising reliability.

We've achieved that reliability with innovations like using layered refractory metals to reduce electromigration and eliminate stress voiding, interlevel shorts and to reduce contaminants.

At the transistor level we use lightly doped drains to inhibit hot electron effects, yielding transistors that will last more than a century.

So if you're tired of the same old line about the same old stuff, call INMOS. Our 25ns, 64K SRAMs will make you look at chips in a whole new way.
DECEMBER 17, 1987

PRODUCTS NEWSLETTER

GRAPHICS BOARD KIT IS COMPATIBLE WITH IBM's VGA STANDARD

Add-on board makers itching to field a graphics card 100% compatible with IBM Corp.'s Video Graphics Adapter standard can get a two-to-four-month jump on the competition and save $40,000 to $80,000 in development costs with Award Software Inc.'s AVGA Manufacturer's Kit. The kit includes everything from schematics, a netlist, and prototype boards, right down to FCC registration. Award, a Los Gatos, Calif.-based leader in Basic-input/output-system software, developed the kit with Cirrus Logic Inc., an integrated-circuit maker in Milpitas, Calif. Not surprisingly, the kit specifies Award's VGA BIOS and Cirrus's VGA chip set. Production boards will offer 640-by-480-pixel resolution, 16 colors, and will be compatible with all other IBM graphics standards. The $5,000 kit will be available in mid-January. Samples of Award's VGA BIOS chips cost $15; Cirrus's VGA chip set costs $45.

PEREX'S 150-MBYTE STREAMER CUTS TAPE BACKUP TIME IN HALF

System integrators can cut tape-backup time for their computer products in half with a 150-Mbyte, dual-speed streaming drive from Perex Ltd. Designed for 1/4-in., Small-Computer-Systems-Interface-compatible systems, the Peristream 150 in its 90 in./s mode loads data at 10 Mbytes/min, compared to 5 Mbytes/min for the competition. It gets its performance primarily by running the tape faster than the standard 72 in./s. Control problems are solved by a design with a complex application-specific integrated circuit chip at its heart. The drive also offers a 72-in./s mode and an electrical tape-loading system similar to those used in VCRs, instead of the mechanical systems of other makers, says the Reading, UK, company. Shinwa Corp., Tokyo, developed the loader and will market the system in Japan. U.S. sales will be handled through Naichimen Corp., Los Angeles. Available now, the Peristream will cost original-equipment manufacturers between $500 and $600.

TI CHIP MATCHES IDT's FIFO ON SPEED AND USES LESS POWER

Look for Texas Instruments Inc. to provide International Device Technology Inc. with some strong competition in the fast first-in, first-out memory business with a 1-µm CMOS product that is just as fast but offers an active-mode power rating of 440 mW—20% lower than IDT's IDT7202. TI's 1K-by-9-bit SN74ACT7202 is miserly on power mostly because of the Dallas company's highly efficient EPIC 1-µm CMOS, twin-well, silicon-gate technology. Pin-compatible with the IDT7202, the new FIFO offers similar maximum access speeds of 35 and 50 ns. In standby mode, it beats the Santa Clara, Calif., competition by 47%—44 mW compared to 83 mW—and in an ultra low power-down mode it dissipates 3 mW instead of 28 mW for the IDT7202. Available now in 1,000-piece lots, the FIFO costs $31.25 each for the 35-ns grade and $22.50 for the 50-ns parts housed in plastic dual in-line packages.

INTEL OFFERS ADA LANGUAGE TOOLS FOR THE 80386

Military applications developers using the Ada programming language with Intel Corp.'s 80386 microprocessor can now go one-stop shopping with the Ada-386 Cross-Compilation Package from Intel's Development Tools Operation, Hillsboro, Ore. The package includes chips, board products, and software tools needed to develop embedded real-time 386 applications on a Digital Equipment Corp. VAX terminal. Tools include a VAX/VMS compiler, symbolic debugger, a global optimizer, and an Ada runtime system for various hardware environments. The boards are compatible with Multibus I and II and have 1 Mbyte of dynamic random-access memory. Price varies with the VAX host; a MicroVAX version sells for $36,000 and will be ready in the first quarter.
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<FEATURES>

- FVC-1000 indicates the intensity of interfering electro-magnetic wave approximately according to each frequency band classified based on the FCC, CISPR, VDE standards.
- No necessity for a shielding room or RF anechoic chamber.
Motorola Inc. has ended the suspense. The big semiconductor maker, pushed by its customers and moving to counter threatening new alliances formed by feisty young silicon merchants, has finally decided to enter the emerging market for 32-bit microprocessors based on reduced-instruction-set architecture. And the other big U.S. 32-bit chip makers, National Semiconductor Corp. and Intel Corp., are taking their own routes.

The industry has been abuzz for more than a year with rumors about a Motorola RISC project, called the 78000, but the company would not discuss it. Meanwhile, Sun Microsystems signed up Fujitsu, Cypress Semiconductor, and Bipolar Integrated Technology to build its Sparc architecture [Electronics, Aug. 6, 1987, p. 126]. Then, last month, another trio—LSI Logic, Integrated Device Technology, and Performance Semiconductor—enlisted to back the RISC chip set of work station-maker MIPS Computer Systems. That did it: the multiranged attack on its complex-instruction-set 68000 processors as well as growing customer approval of RISC forced Motorola to go public.

Motorola officials emphasize that though they have been working on RISC for several years, they are unconvinced that the technology will replace CISC. While Sun and MIPS claim higher performance and lower cost for RISC, the Motorola counterclaim is that CISC can match or outperform RISC, and that it can cost less because of higher sales volume. However, the officials acknowledge that RISC can cut design time and serve customers that are enthusiastic about the architecture.

Competitors and some market analysts say what Motorola faces in RISC is spelled r-i-s-k because of incompatibility with the 68020, the new 68030, and the planned 68040. Motorola managers strongly disagree, saying they can set separate standards. They also argue that CISC-based processors will continue to dominate the 32-bit markets, though Motorola officials hint that the future 68040 will have more RISC-like features mixed in with its CISC-based design.

Motorola’s RISC project is separate from its 68000 work, says Murray A. Goldman, senior vice president and general manager of the Microprocessor Products Group in Austin. Goldman says Motorola is spending at a rate of $10 million to $20 million per year on the work. The chip will be in CMOS, operate under Unix, and is expected to be ready early in the year, though Goldman won’t confirm that.

In the MIPS alliance, the three chip houses will apply their fast CMOS technology to the R2000 central-processing unit and R2010 floating-point accelerator, starting out at common speeds of 12.5 and 16.7 MHz. Around mid-1988, IDT, LSI Logic, and Performance Semiconductor will start revving up their own CMOS processes in an all-out race to provide the fastest and lowest-cost parts. The three are also planning to design and produce peripherals independently.

IDT, which is considering a future biCMOS MIPS design, is planning a line of peripherals for the RISC architecture likely to include a graphics coprocessor and digital signal filter. The first will appear in the second half of 1988.

LSI Logic was attracted to the MIPS design by its small size, which makes it easier to include in a semicustom design library, says Rob Walker, vice president and chief engineering officer. After the initial 1.5-µm core, LSI Logic plans a 1.2-µm CMOS design to offer performance of 25 million instructions per second. In 1989, a submicron CMOS process will be used to push performance to 40 mips.

Performance, already selling 16-bit 1750A processors to the military, will use the MIPS design to expand those offerings and enter the 32-bit commercial business. It is also planning peripheral chips, starting with a set of high-speed write buffers.

MIPS will participate in the design of future generations of the core chip set and act as judge on conformance to its software base, says Robert C. Miller, MIPS’s chairman and chief executive officer. Miller also says MIPS might not be finished signing up chip-producing sources yet—the company is also interested in emitter-coupled logic and even gallium arsenide.

GOOD YEAR. The MIPS and Motorola developments serve as a fitting finale to a big year for RISC. The technology built up steam through 1987, partly led by engineering work-station houses seeking more power than they can get from commodity microprocessors, and partly fueled by general discontent over sole-source supplies of 32-bit chips from Motorola and Intel, Santa Clara, Calif.

In addition to the MIPS and Sun teams, the RISC scorecard now lists Advanced Micro Devices Inc., with its AM29000 Streamlined Instruction Processor [Electronics, March 19, 1987, p. 61], as well as Intergraph Corp. Intergraph acquired rights to the first- and second-generation Clipper [Electronics, Nov. 12, 1987, p. 85] from Fairchild Semiconductor Corp.

The MIPS camp is aiming for 1,000 design wins during the next three years, and estimates that the RISC segment of the 32-bit microprocessor business could reach $430 million of a total world market that hits $1.177 billion (see figure). However, at market researchers Dataquest Inc., analyst Alice Leeper estimates the RISC portion to be about half that. “We feel the largest part of the market is in established applications,”
she says, but adds that more RISC announcements can be expected.

Such as one from National Semiconductor Corp. The Santa Clara, Calif., company will announce early next year that it is working on a RISC-oriented next generation of its CISC-based 32-bit 32532. President Charles E. Sporck adds that no RISC processor will be introduced unless it is compatible with the existing 32000 microprocessor line. Intel, also rumored to have a RISC chip in design for embedded control applications, is also considering RISC-like operations for its future 80486.

“We will use RISC technology on the 486 to do RISC-level instructions in single-clock cycles, but the bigger application is in embedded control. I'm not ready to announce any products, however,” says Dave House, senior vice president and general manager of Intel's Microcomputer Group in Santa Clara.

—J. Robert Lineback

CONSUMER

DIGITAL AUDIO TAPE GETS CLOSER IN U.S.

DEARBORN, MICH.

There are growing signs that consumer digital audio tape may finally be able to establish a beachhead in the U.S., despite the political controversy that has so far blocked the entry of the new technology here.

Ford Motor Co. is the latest to join those vowing to test the waters next year. With hardware supplied by Sony Corp., the automaker announced plans this month to offer DAT players as an option for the Lincoln Continental in limited markets beginning in June.

What's more, at least three consumer audio vendors say they'll announce 1988 U.S. price and delivery schedules for DAT hardware at next month's Winter Consumer Electronics Show in Las Vegas after one of them, Marantz Co. of Chatsworth, Calif., said last summer that its introduction would come in October. Likewise, at least one independent record producer plans to announce immediate U.S. availability of prerecorded music on DAT, with others contemplating similar moves.

COPYRIGHT DISPUTE. DAT backers are hoping that these initiatives and possibly others will help break the logjam. At least a dozen manufacturers showed DAT prototypes at last January's show [Electronics, Jan. 22, 1987, p. 30]. But the dispute with the record industry over software copyright issues has so far prevented big-name suppliers from marketing consumer DAT home hardware here.

For its part, the Recording Industry Association of America, which represents major record producers, is continuing to push for federal legislation that would mandate the use of a circuit in all DAT recorder/players to prevent the copying of prerecorded materials containing a special code. The record industry is concerned about lost revenues because DAT can produce high-quality digital copies of records, analog tapes, and perhaps compact disks. Until the issue is resolved, the major record labels have said they will boycott DAT, while major hardware makers sit on the fence. But DAT hardware is being sold in Japan, and is also entering the European market despite similar copyright disputes.

Progress on the U.S. legislative front could come in late January or February. That's when the National Bureau of Standards is expected to deliver results of a test of the proposed DAT copy-protection controversy, Ford plans to offer a player in 1986.

DAT DRIVE. As manufacturers await word on the DAT software-copy protection controversy, Ford plans to offer a player in 1986.

THE IEEE

IEEE'S NEW VOTE RULES WEAKEN 'THIRD PARTIES'

NEW YORK

Petition candidates are effectively being closed out of the Institute of Electrical and Electronics Engineers elections. The IEEE is switching next fall to a new process, approval plurality voting, that effectively prevents "third-party" candidates from winning an election when two or more other candidates split the establishment vote. Under the new rules, members can vote for as many candidates as they choose.

Jack Nagel, an associate professor of political science at the University of Pennsylvania and a leading proponent of approval voting, puts it succinctly: "Approval voting helps prevent a splintering of the majority."

IEEE executives say the new method is an answer to their prayers after three years of trying to improve the organization's electoral process. Approval plur-
The IEEE, with 280,000 members, is the biggest organization to back it so far. That's exactly why the institute's most outspoken critic, Irwin Feerst, who has lost five races for IEEE president as a petition candidate, says the change is unfair. The move was taken solely to keep "the academics and corporate executives" in charge and himself out of contention, Feerst charges. "I am the target of this change," he says. "They're trying to keep the dissidents down."

Henry L. Bachman, the current IEEE president, says that is not the case. "In elections where we have multiple candidates running for a single seat, we've generally had an even split," he says. For example, the 1975 IEEE election pitted Feerst against the IEEE's board of directors' candidate, Joe Dillard, in a two-man race; Feerst drew 37.6% of the vote—respectable, but still far short of Dillard's 61.5% share. But 11 years later, Feerst went up against two board-nominated candidates, Russell Drew and Merlin Smith, and almost won, even though he captured only 34.3% of the votes. Feerst came within half a percentage point of beating Drew, the winner. Feerst almost succeeded because the so-called mainstream voters had been forced to choose between two candidates. Together, Drew and Smith garnered 64.8% of the vote. Anticipating another Feerst candidacy, the IEEE board nominated only Emerson Pugh in 1987. But this time Feerst held off, pushing instead for a constitutional amendment requiring the board to nominate a minimum of two candidates. His aim was to wait a year and try to split the vote again.

FELL SHORT. The amendment was approved by a majority—but not the two-thirds majority it needed to pass. And although the board promised in November to name at least two nominees in the future, it now has acted to foil Feerst's strategy by switching over to approval voting. Now, since mainstream voters no longer must choose between two acceptable candidates, they can vote for each. Such a scenario would make it difficult for Feerst to mount a strong challenge.

Tobias Naegle

INTEGRATED CIRCUITS

SMART POWER GOES OFF-THE-SHELF

LOS ANGELES

Power integrated circuits, until now mostly custom chips for a few major automotive customers, are becoming standard products. The big-name suppliers, Motorola Inc. and Siemens AG, are pitching their first off-the-shelf power ICs to industrial-equipment makers. And several competitors, including a division of General Electric Co. looking to stage a comeback, are polishing their own standards for introduction in early 1988.

The strategy, to develop high-volume momentum to drive down prices, foreshadows the emergence of power ICs as an important business. The chips are attractive because they combine logic circuitry and a power-switching element—at least several amps worth of power and upwards of 25 V—in the same monolithic device. A sensing function is also required. Their compactness and performance permits power ICs to replace entire boards of discrete components in interfacing microprocessors to all types of equipment.

DAUNTING TASK. The chips are complex, however, and low yields make them more than three times as expensive as discrete solutions. In addition, providing what is expected of standard parts has proved daunting. For example, isolating the power from logic economically and protecting chips from real-world conditions such as overvoltage surges and extreme temperatures have been difficult. Also, the most sophisticated chips need up to 15 mask levels, compared to fewer than half that for logic ICs.

"It is a lot tougher than people expected, including us," says Donald Neill, marketing manager for General Electric Co.'s Integrated Power Systems Department. GE bid for leadership in the power IC industry several years ago but recently has kept a low profile. Its power IC facility in Research Triangle Park, N.C., has spent seven years and some $100 million to date. The company, though, considers power ICs "only at the early development stage, where customers are still trying to figure out the payoff," Neill says.

Despite the new-product activity, knowledgeable industry observers say it will take until 1990 or 1991—when the first car models using them extensively will appear—for power ICs to become major factors. Observers also expect better computer-aided-design tools by then, which will make possible application-specific power ICs and provide a boost in other markets.

In fact, the move to standard power ICs helps power ASICs, in the view of Motorola's Daniel Artusi. 'The standard products then become cells which can be used from our expanded smartpower library,' says Artusi, director of marketing, power, and transistors for Motorola's Discrete Products Group in Phoenix.

Motorola and Siemens appear to have a step up on the rest of the field with their chips, called high-side switches, designed for auto use. The Motorola Smartpower MPC 1510 and Siemens Smart Sipmos BTS 412A operate at up to 35 V with a 12-A rating and are intended, under microprocessor control, to switch solenoids and other inductive loads between the power source and the ground. This suits them for myriad industrial tasks, including robotics and program control.

Other power IC makers are not far behind with products in sample quantities and volume production promised shortly. GE, in particular, is preparing to unveil expanded lines. They include power-conversion devices in the GS/600 family with ratings up to 500 V and smart input/output modules with increased functionality in the GS/200 group. "You'll see us recognized as the leader again," GE's Neill predicts.

Siliconix Inc. in Santa Clara, Calif., intends to carve out a niche in battery-powered equipment such as intelligent telephones. The company is adding to its SB100 Smartpower family, which provides dc-to-dc power conversion. Ixys Corp. of San Jose, Calif., is addressing the auto market, where a manufacturing partner is funding a program aimed at producing millions of devices. In the meantime, the privately held company has a line of modules planned for smart input/output in the GS/800 series.
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**SANTA CLARA, CALIF.**

In about the time it takes to grab a cup of coffee, fast new compiler software for CMOS erasable programmable logic devices can convert design descriptions into finished EPLD programming patterns. That reduction—down to minutes from a half hour—promises not only to keep engineers productive during the iterative process of system design, but also to slim down development operations for competitive equipment markets.

The software is from Altera Corp., a Santa Clara, Calif., producer of EPLDs. The company is incorporating the speedy intelligence-laden compiler into the new version 5.0 of its A+Plus design processor software. It becomes available this month for IBM Corp. PC ATs and compatibles. At the same time, Altera is joining a handful of competitors in unveiling faster EPLDs. The one-two punch of fast-turnaround development software and quick CMOS chips is intended to deepen penetration of semicustom markets now served by mask-programmed gate arrays and bipolar PLDs by Altera's EPLDs.

For the development software (see figure), Altera engineers didn't touch the flattener and macromuncher portion of the design processor, which substitutes logic descriptions for TTL symbols and then trims unused logic. But they sped up the expander section which scans for errors, and rewrote the logic minimizer portion to include knowledge-based, general-consensus algorithms that take a specific engineering tack in reducing the size of product tables. Programmers also embedded heuristic strategies into the compiler's design fitter, which now employs artificial-intelligence-like algorithms to quickly determine if a particular approach to putting logic in an EPLD chip will be successful.

Smart fitter programs are becoming necessary in EPLD programming because of the growing densities of the CMOS parts, says Clive McCarthy, vice president of software development. “It is becoming the kind of computing task that cannot be solved strictly by brute force,” says McCarthy, referring to approaches that try all combinations of logic placement before giving up on a design that might not fit.

Altera managers believe the speedup of the A+Plus software has pushed compilation times to their maximum acceptable point. “A designer can now very quickly do 10 or a dozen designs within a day, iterating a system design through changes,” says David A. Laws, marketing vice president. The 5.0 version of the A+Plus design processor,

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**KEY IMPROVEMENTS.** Altera has sped up the expander, rewritten the logic minimizer, and added AI-like algorithms to the design fitter portions of its EPLD design processor.

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Interfacing between processor and main memory gets tougher as speeds increase. But TI has the SN74ALS6301 DRAM timing controller. It can handle any DRAM up to 1 Mbit and incorporates only the essential func-

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Edited by Lucinda Mattera, Former Editor-in-Chief of Electronic Design.

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Technical managers and senior engineers have special information needs when it comes to traditional technology areas. Beyond product announcements and design applications, they require technical interpretation, perspective, and assessments that can help them achieve their ultimate goal—speeding up time-to-market with the right product. Towards that end, Electronics magazine expands its technical coverage of fundamental technologies in 1988 with a new Technology Series beginning in January.

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with a compiler that is 10 to 20 times faster than the previous release, sells for $1,750.

On the device front, faster chips are coming not only from Altera but also from Intel, Lattice, and Cypress. Altera says its additions to the EP600 and 900 series, designated the 610 and the 910, are more than 40% faster than present parts. Laws says that the speed of the two newcomers will enable them to muscle into the territory of high-power-dissipating bipolar parts, which cannot be reprogrammed like the ultraviolet-light-erasable CMOS devices. The 610, which has more than 600 equivalent gates, improves propagation delay to 25 ns from 45 ns; the 910, with more than 1,000 gates, will clip along at 30 ns versus 45 ns. The 610 and 910 have price tags of $12 and $21.50 in 100-piece lots, respectively.

Intel Corp., Santa Clara, Calif., now offers parts equal to Altera's slower ones and is aiming for 25 ns at 35.7 MHz with its new 1-mic 5AC312 EPLD [Electronics, Sept. 17, 1987, p. 65]. Lattice Semiconductor Corp. in Beaverton, Ore., has 15-ns parts now among its electrically erasable PLDs, which it calls generic array logic, or GAL. But with a submicron CMOS process next year, it plans to ship 12-ns EEPLDs in the first half and 10-ns parts in the last half, says Paul Kollar, vice president of sales and marketing. "We may soon beat the TTL boys to the 24-pin level."

Cypress Semiconductor Corp. in San Jose, Calif., is fitting its entire EPLD product line for a new 0.8-μm drawn-gate, double-level metal CMOS process. It will wring 15 and 12 ns out of 25-ns parts starting in the second quarter. "This will allow us to replace all but the 10-ns bipolar parts, which are still not in volume production. We expect to be able to select some 10-ns parts and have a high yield at 12 ns," says Al Graf, the company's PLD product marketing manager.

Robert Lineback
CBL is to bipolar what CMOS is to MOS: both are complementary circuits, with CBL using pnp and npn transistors, and MOS relying on p-channel and n-channel transistors.

To get to the 800 ps-50 μW level, the IBM team uses conventional 2.2-μm technology and a 200-MHz switching transistor. But computer calculations show that the circuit—described at the International Electron Device Meeting earlier this month in Washington—can reach 300 ps and less than 10 μW if 1.2-μm features and a 1.5-GHz pnp are used instead. A circuit boasting such speed but using so little power would set records for bipolar design, says IBM Fellow Siegfried Wiedmann, head of a VLSI design team at Böblingen. A fast pnp transistor is a prerequisite for high-speed switching.

But even those values are not the limit, says Wiedmann. CBLs using 1-μm technologies, trench isolation, and other novel process techniques as well as pnp transistors higher in the gigahertz range should top 100 ps, he says.

Up to now, designers around the world have hardly explored bipolar complementary-transistor logic. The reason: the current-controlled bipolar transistor, in contrast to the voltage-controlled MOS-type, is ill-suited for complementary logic applications. After switching, current continues to flow, which causes fairly high static power dissipation.

The solution would seem to be CMOS-like bipolar complementary-transistor logic in which bipolar transistors replace MOS types. But it is difficult to implement such logic with bipolar structures, even with advanced processing techniques. What’s more, the relatively large saturation time constants of presently investigated transistor structures severely limits the speed. These shortcomings eventually led Wiedmann, who was also one of the developers of integrated-injection logic, to the charge-controlled logic device. The challenge during the three years of CBL development work, Wiedmann says, was finding a way to feed a large controlled charge into the base of a transistor without generating the large continuous currents that conventional bipolar transistors require. By keeping such currents as low as possible, the standby power could be considerably reduced.

The basic CBL circuit consists of three diodes and a pnp/npn transistor pair at the output (see figure). It thus looks like a diode-transistor logic gate; indeed, the logic functions and static signals are similar to those in DTL.

Storing the charge are two input diodes. This minority carrier charge is rapidly transferred between these diodes and the third, the level-shift diode, during each switching transition. The oppositely biased input diodes have a large time constant and can store a large charge, which is typically 0.1 pC, so during the switching period the input diodes act as a low series resistance. So just as with CMOS devices,
When you're out in the trenches fighting it out with ordinary microprocessors, running out of muscle is all too easy. That's why you should look to the new T800 Transputer from INMOS.

The T800 is the fastest 32-bit, single chip, floating-point microprocessor available today. A quick glance at its statistics will show why nothing else is in its league...

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Other team members include the pin compatible T414 Transputer, offering lower cost, 10 MIPS performance and 0.75M Whetstones. Lined-up to provide all the I/O processing you need, the T212 16-bit Transputer is the ideal high performance controller and the M212 Disk Processor combines disk controller hardware and a Transputer on a single chip, supporting both Winchester and floppy disks. And the C004 Link Switch makes the design of software reconfigurable multiprocessor systems as easy as kicking an extra point.

If this all sounds like your kind of game, put the ball in play by contacting your local INMOS sales office today. And get ready to score.
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Electronics

MILITARY

COMING: EMBEDDED TRAINING SYSTEMS

WASHINGTON

Embedded training systems for the military were little more than an idea until recent advances in microprocessors and memory technology. The Department of Defense now thinks the time is ripe for integrating training functions directly into weapons, aircraft, or ship systems, and it has started developing a set of guidelines to speed things along. However, the big stumbling block still is deciding when and how integration should be done.

Traditionally, weapons and training systems have been designed and built by different contractors, under separate contracts and with little interaction. But the growing complexity of modern weapons systems and the high cost of dedicated trainers spurred interest in alternatives. Advocates say the embedded approach saves money, provides better hands-on training, and permits users to practice and refresh skills without having to leave the weapons unit.

The Army took the lead last spring by mandating that embedded training must be evaluated as the first training option. But there is still some flexibility, says Dorothy Finley, a team leader at the Army Research Institute, and the director of a four-year effort to define the concept. "You don't have to have embedded training," Finley says, "but if you don't, you better have a pretty good reason for it."

One obvious reason is whether it's worth the trouble; not all weapons and vehicles may need embedded training. Other considerations include the effect a training system might have on the life-span and cost of its host system. Key to the success of any implementation is an early decision, says J. Thomas Roth, staff scientist at Applied Science Associates. "The initial decision has to be made in the concept stages of a program."

"Embedded training must be viewed as only a component of your training system. It is not going to do all things for you," Finley says. "If you don't always remember that, you can end up with a large current flows only during that period.

In their standby mode, the input diodes constitute a high resistance. That limits the current and therefore the power dissipation to levels that are virtually negligible. The dynamic power, on the other hand, is lower than that of CMOS because CBL uses smaller voltage swings.

— John Gosch

World Radio History

Electronics/December 17, 1987
Matrox Offers Low-Cost Way To VMEbus Image Processing.

A Canadian company has beefed up its graphics board set without adding much fat to its price, by combining real-time image processing with hardware-generated graphics. The MVP-VME from Matrox Electronic Systems Ltd. provides an easy way for VMEbus systems designers to include both image processing and high-end graphics capabilities in their designs. The two-board set, however, costs $6,000, just one half to one quarter of the price of competing systems.

The MVP-VME is the Dorval, Quebec, firm's second image-processing and graphics-combination board product. The first brought real-time image processing and graphics to the IBM PC AT...

Excerpted from an exclusive article in the May 14, 1987 issue.

Electronics / December 17, 1987
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Embedded training may save money and permit better hands-on practice

similar to designing a stand-alone system," Roth says. "But there's a much stronger need for interaction between the systems designer and the training developer."

For example, aircraft have tight space and weight limitations. That means training-system designers cannot add much in the way of computer hardware and must implement their systems in software that will run on the computers in the host equipment. That's where recent improvements in microprocessors and memory technology come in handy to support the additional software.

"Most of it can be done in software. That's the saving grace of it," says Henry C. Okraski, deputy technical director at the Naval Training Systems Center in Orlando, Fla. The center is the focal point for most of the DOD's training-system needs.

Okraski says the center is overseeing development of two embedded training systems "that look very promising." He expects one, which involves the SPA-256 radar, to be installed in 5,000 Navy systems. He also acknowledges that "we are making some inputs" for the SS-N-21 submarine. Code-named the Sea Wolf, the SS-N-21 is planned as the next generation of attack-class submarine.

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Submarines are ideally suited to embedded training technology, Okraski says. They spend up to six months or more between ports, so the crew can test the systems whenever they have time, to make sure they stay sharp.

"Embedded training has a tremendous payoff in areas where there are perishable skills," he says. —Tobias Naegele

Electronics/ December 17, 1987
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“Where we design to your applications.”
A FIRST: MATSUSHITA AND TOSHIBA TO EXPORT U.S-MADE APPLIANCES TO JAPAN

Next year, two Japanese electronics manufacturers will start importing finished consumer products they build in the U.S. for sale in Japan—marking the first time Japanese electric-appliance makers have ever made such a decision. The recent steep rise in the value of the yen, which is making American-built products cheaper in Japan, spurred Toshiba Corp., Tokyo, and Matsushita Electric Industrial Co., Osaka, to make the move. Toshiba will start importing low-end microwave ovens manufactured at Toshiba America's Lebanon, Tenn., plant next March. The company is also considering importing color TVs made in the Lebanon plant, which is putting out 500,000 microwave ovens and 800,000 color TVs a year. Matsushita will import large-screen color TVs made by Matsushita Industrial Co., Franklin Park, Ill., starting in the middle of next year. The Illinois factory builds 1 million color TVs a year.

SIEMENS SETS JOINT VENTURE WITH CHINESE TO BUILD ITS DIGITAL SWITCH

The Chinese have been having a tough time getting the kinds of technology-transfer agreements they prefer over simple hardware imports, but one such agreement has been reached with Siemens AG. Siemens and the Chinese government will set up a joint venture to manufacture the Munich-based company's digital telephone-exchange system, EWSD, and to start microelectronics production in China. Siemens will also work with the Beijing Technological Exchange Center, construction of which is scheduled to begin next spring, by training some 500 Chinese engineers a year at the center. The deal was reached through negotiations between Siemens's chief executive officer Karlheinz Kaske and prime minister Li Peng and general secretary of the communist party Zhao Ziyang.

NIKON TO MARKET HALF-MICRON STEPPER...

The first Japanese stepper manufacturer to start marketing an excimer-laser photolithographic system for fabrication of chips with feature sizes below 0.5 μm will be Nihon Kogaku K.K. (Nikon). The NSR-1505EX stepper can be used initially for development of 16-Mbit dynamic random-access memories, and will be suitable for mass production later on, the Tokyo company says. The resolution of better than 0.5 μm is made possible by a krypton fluoride excimer-laser light source operating at a 258-nm wavelength. The NSR-1505EX provides 5:1 reduction of the reticle pattern for lithography of an area measuring up to 15 by 15 mm per shot. The $2.3 million stepper will be available 10 to 12 months after receipt of order, and Nikon will start accepting orders from Japanese customers in January. Matsushita Electric Industrial Co., Osaka, and Canon Inc., Tokyo, are expected to announce competing products soon.

...AS IT AND CANON PLAN TO BUILD 30% MORE STEPPERS NEXT YEAR

Stepper production is accelerating in Japan. Two leading stepper manufacturers, Nippon Kogaku K.K. (Nikon), Tokyo, and Canon Inc., Tokyo, will increase production of stepper photolithography systems to meet the rapidly increasing worldwide demand for semiconductor production capacity, they say. Nikon, which exports around 30% of its steppers, has just revised upwards its shipment estimates for steppers for fiscal 1987, which will end on March 31, 1988, by 30% to 260 units, and the company expects to sell more than 300 units in fiscal 1988. Canon says that the annual shipments of its steppers will top the 100-unit mark for the first time by December 31. Canon also says it will boost its production rate to 20 units a month from the current 15 units by next spring.
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And bipolar PROM can't match our standby power-down features for lowest system power requirements.
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For highest performance, lowest power 64K PROM devices, you have little choice but Cypress Semiconductor. We give you the fastest low power parts in the industry. And we give you plenty of options:


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Widely accepted in military applications, diagnostic PROM is now gaining in popularity for commercial applications.

Two new innovations should accelerate that acceptance: Our CY7C268 and our CY7C269.

Both function in the normal pipeline mode, with high performance.

Or, when selected, the Diagnostic Register can be loaded with the data on the bus, or the data in the Pipeline Register. Conversely, the system can load the contents of the Diagnostic Register into the Pipeline Register.

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QuickPro: PROM and PLD programming and diagnostics right now, right from your PC-compatible.

QuickPro is fast becoming an essential complement to the PROM programmer in the development lab.

QuickPro is fast becoming an essential complement to the PROM programmer in the development lab.

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2. You have an easy, screen and menu oriented system that gives you lots of options, and saves you lots of time.

3. You can program any Cypress Semiconductor programmable part, on PC-compatibles.

4. As you can see, you can quickly display the contents of any device, to speed debugging.

5. Using the JEDEC standard, (PC-DOS binary for PROM) QuickPro is compatible with the output of all the popular PLD programming tools, including CUPL™, ABEL™ and PALASM™.

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Two new hybrid ICs are small enough to mount transversely in proximity detectors having coils 20 mm in diameter or larger, and therefore dramatically cut the length of these detectors. The OM390 and OM391 measure just 14 by 14 by 1.7 mm and produce a proximity detection operating distance of between 2 and 5 mm, depending on the coil.

The OM390 and OM391 are for such application areas as positioning of machine tools, limit switches, component detection during assembly, and detection of coins in slot machines. By allowing manufacturers to use a shorter tube, the devices open up the possibility of new application areas where space is a critical factor and in addition reduce manufacturing costs.

Each circuit consists of a voltage regulator, an oscillator, a rectifier stage, a Schmitt trigger, and an output stage. They have protection circuits against short-circuit and overload, voltage transients, and reverse-polarity connection. When actuated, the circuit passes an output current up to 250 mA through the load (such as the coil of an electromagnetic relay, an LED, or a photocoupler); two extra terminals connect to an optional indicator LED.

The thin-film circuits fit in M18 hollow-stud assemblies (when they are mounted longitudinally) or M30 (for transverse mounting). They accept a supply voltage between +10 and +30 V (OM390) or —10 and —30 V (OM391), and consume typically 0.4 W from a 24 V supply.

Image intensifier offers third-generation features at a second-generation price

With a price tag of US$ 4500, the Philips XX1610 ‘second-generation super’ proximity-focused image intensifier offers third-generation night vision performance at a second-generation price. The new device suits night-viewing systems for military and security surveillance applications.

The new image intensifier has a sensitivity and signal-to-noise ratio double those of currently available second-generation types and works right down to starlit or clouded moon conditions, still producing an illuminance of 10⁻³ lux. In addition, it has an operational lifetime three times that of other second-generation intensifiers. It operates with the objective lenses and other accessories of second- and third-generation image intensifiers.

Minimum sensitivity is 500 µA/lm, compared with the 240 µA/lm of other second-generation devices. Although third-generation intensifiers have a higher sensitivity of 1000 µA/lm, they cost more than twice as much as the XX1610, and will anyway not be generally available until 1990. Furthermore the XX1610 has a signal-to-noise ratio of 15.5 which matches that of third-generation types.

Light entering the intensifier is collected through a clear-glass anti-veiling glare input window, onto an S20R red-extended photocathode. The electrons generated by this photocathode are multiplied by a micro-channel plate which incorporates a proprietary treatment that gives a long 3500 hour operational life — again matching third-generation intensifiers.

Compact Disc decoding circuits halve IC parts count, use less power, extend temperature range

We are unveiling a pair of third generation Compact Disc ICs for high-performance low-cost systems that forms a complete stereo CD decoding system — instead of the four ICs previously required — with very few other components. Particularly attractive to portable equipment, the CMOS SAA7310 and SAA7320 have a much lower power consumption — typically 475 mW combined — than second generation NMOS ICs, and allow the whole decoding system to be run from a single +5 V supply. The devices also operate over a wider temperature range of —40 to +85 °C which is of great importance in automobile applications.

The SAA7310 decoder incorporates all the functions available on the well-known SAA7210, such as demodulation, error correction and basic interpolation. In addition there are extra functions: a special mode for non-digital audio applications — for example CDROM and CD Interactive — prevents data from being interpolated (and thus corrupted), a strong requirement for such applications; and improved playability for applications where mechanical shock is likely to occur, such as portable players and in-car systems.

The SAA7310 and SAA7320 are both available in a 44-pin quad flat-pack. In addition, the SAA7310 is also available in a 40-pin DIL which can be used as a replacement for the SAA7210.
NMB TO MAKE 1-MBIT MEMORIES FOR TI
Texas Instruments Inc., in full production of 1-Mbit memories in Japan and ramping up output in Dallas, is turning to an outside supplier for help in meeting demand. NMB Semiconductor Co., Chiba, will manufacture 1-Mbit TV frame memory and 1-Mbit dynamic random-access memory for TI. The products will be marketed in both Japan and the U.S. under TI's brand name. NMB will initially supply 50,000 frame memory chips and 100,000 DRAMs a month. The monthly production rate for the 1-Mbit DRAM is expected to be increased up to 1 million units by next March.

U.S.-SINGAPORE CHIP MAKER FORMED
The government-owned Singapore Technology Corp. is teaming up with two U.S. companies, Sierra Semiconductor Corp. of San Jose, Calif., and National Semiconductor Corp. of Santa Clara, Calif., to build a state-of-the-art $40 million plant for making customized computer chips. The joint venture, called Chartered Semiconductor Pte Ltd., will start producing 5,000 six-inch wafers per month in early 1989. That will double over the course of five years. Sierra and National Semiconductor are committed to buying more than 50% of the company's total production. The rest will be sold in the Asia-Pacific region.

KDD LOSES ITS TELECOM MONOPOLY
Two Japanese international telecommunication planning firms are going to give Tokyo's Kokusai Denshin Denwa Co. some competition for the Japanese international telecommunications market. The two Tokyo firms, International Digital Communications Inc. and International Telecom Japan Inc. have received permission from the Ministry of Posts and Telecommunications to enter the market, despite MPT's fears of excessive supply [Electronics, Feb. 19, 1987, p. 46]. However, MPT will not initially permit IDT and its partner to fully utilize their planned 11,000-channel cable. The two firms will be allowed at first to use only the equivalent of 1,250 circuits.

NEC EXPANDS DRAM FACILITY
NEC Corp. will expand manufacturing lines for 1-Mbit dynamic random-access memories at its manufacturing subsidiary, NEC Yamaguchi Ltd. In reaction to the current worldwide 1-Mbit DRAM deficit, NEC Yamaguchi will start building the new production lines next spring with an investment of 14 billion yen and expects to complete them by the end of 1988. The new lines will double the subsidiary's current manufacturing capacity of about 6 million chips including memories and microprocessors. NEC says that the new lines will also be used to fabricate 4-Mbit DRAMs, which are slated for sampling in mid-1988.

U.S. BUYS ISRAELI SIMULATORS
Israel's Elbit Computers Ltd. of Haifa has signed an agreement with the U.S. army to supply simulators for its conduct of fire-control training programs for tank crews. The first stage involves the sale of 16 simulators for $12.5 million. The project is a joint program between Elbit and its American subsidiary, Infineometrics. Elbit officials say that the contract eventually could be increased to $100 million worth of simulators.

CHINA IMPORTS TO GROW SHARPLY
China's fast-growing electronics industry, targeted to grow 16% yearly to a level of $17.4 billion by 1990, could turn out to be a major export customer for producers of components in Japan, other Asian countries, and the U.S. Components imports by Chinese equipment makers totaled $740 million in 1985 and could jump to $1 billion by the end of the decade, reports the Chicago consultants A.T. Kearney Inc. Japan is the dominant supplier, but Kearney suggests U.S. firms stand a good chance to break into the market with large-and ultra-large-scale integrated circuits.

AT&T TO SELL CHIPS IN JAPAN
AT&T International (Japan) Ltd., Tokyo, says that AT&T will market semiconductors in Japan starting in January 1988. An AT&T Japan spokesman says that its parent firm will initially sell MOS integrated circuits for integrated services digital networks, linear ICs, and digital signal processors through several leading Japanese semiconductor trade firms, including Tokyo's Tomen Electronics Corp. and Marubeni Hytech Co. AT&T Japan will cooperate with these trade firms in sales promotion. AT&T will also set up a design center in Tokyo next fall for marketing its application-specific ICs including 1-μm full custom and standard cell ICs.

PHILIPS INVESTS IN CHINA CRT PLANT
Philips signed an agreement with officials of China's Jiangsu province last month providing for a joint venture for making color TV tubes and deflection units. The partners in the $180 million venture will be the Chinese picture-tube maker Huadong and a Hong Kong investment firm, which will have 45% and 25% shares in the venture, respectively. The Dutch firm, which is supplying its flat-and-square tube technology, will own the remaining 30%. The Jiangsu plant will have an annual capacity of 1.6 million tubes.

... AND OPENS A CRT PLANT IN UK
Philips has started production of high-resolution color monitor tubes in Durham, England. The Dutch firm says the plant is Europe's largest manufacturing facility for such tubes—and one of the world's most advanced. Production at the $27 million plant will concentrate initially on 90-degree, 14-inch tubes, with a goal of about a quarter of a million units a year by the end of 1988. Philips sees the market for color monitor tubes growing some 25% a year—from six million in 1986 to 13 million by 1990.

GERMANS TO BOOST COMMUNICATIONS
West Germany's $12.7 billion investment package designed to support the economy—something the U.S. has long urged the Bonn government to do—provides for a $900 million increase in spending by the Bundespost, the country's telecommunications agency. That raises the agency's investments next year from $11.2 billion to $12.1 billion, the bulk of them for communications hardware.

SEL CHURNS OUT MONOMODE FIBERS
With an eye towards Europe's optical fiber-based broadband integrated services digital networks of the 1990's, West Germany's Standard Elektrik Lorenz AG, a member of France's Alcatel Group, has started production of monomode optical fibers in a new factory. Initial production, which began last month at the $24 million, 1,000 square-meter plant in Stuttgart, West Germany, will be 50,000 kilometers of fiber a year, but its annual capacity may be raised to 120,000 km by 1990.
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Circle 167 on reader service card
The continuing debate over whether CISC or RISC technology is the answer to boosting computer performance levels tends to focus on machine speed, often ignoring an equally important issue: architectural compatibility. Computer manufacturer's with 68000-based CISC architectures considering a move to RISC technology for their high-end product offering need to recognize the enormous costs they face. Current systems software must be adapted and supported on different architectures. Two different operating systems as well as diagnostics have to be ported and supported. Compilers for high level languages need to be developed. And these are just a few of the obstacles.

The EDGE 2000 Series VME board set recently introduced by Edge Computer proves that a 68000-compatible CISC system can operate with RISC-like efficiency. But performance is only one side of the coin. Value and the ability to leverage your investment in existing 68000-based software are equally important. By driving costs to approximately $1K per MIPS in OEM quantities, while maintaining 68000-compatibility, Edge makes CISC a more attractive option than other implementations of CISC or RISC. 68000-based manufacturers can stay with CISC and forego a sizeable portion of software porting costs, as well as the on-going expense of supporting and maintaining two different architectures.

In the industry's continuing quest for improved machine performance, Edge has set the pace by achieving faster clock speeds and reducing cycles per instruction. At 1.4 cycles per instruction, the EDGE 2000's AIT (Average Instruction Time) is already lower than most products on the market today.

Nonetheless, the CISC/RISC debate will continue. But for 68000-based manufacturers faced with the need to expand their product lines and bring high-performance 68000-compatible products to market economically and on time, the EDGE 2000 is a clear winner.

Edge Computer now offers SYMETRIX, a concurrent operating system environment, on its line of high performance computer systems. SYMETRIX provides an architecture that allows multiple standard operating systems to operate at the same time on the same system. The first implementation of SYMETRIX integrates the solutions and applications oriented environment of the PICK* Open Architecture with the programming and systems environment of UNIX V2.

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The action in linear is exploding; firms ready monolithic solutions for analog filtering, analog-to-digital conversion, disk-drive read/write, and fiber-optic communications

by Lawrence Curran
Companies in North America requiring strategic alliances in Europe, and the important market in West Germany, can find partners among the twelve thousand production firms based in the state of Baden-Wuerttemberg.

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General Instrument Microelectronics

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The first 12-bit, monolithic flash converter is now in prototype production at Crystal Semiconductor Corp. The sampling analog-to-digital converter is not only more accurate and faster than any other monolithic ADC chip, it's also the equal in performance of 12-bit hybrid circuits, which not only cost more than chips but also consume more power.

To get higher throughput, resolution, and accuracy all on one chip, the Austin, Texas, company went to a moderate-speed architecture called two-step (see fig. 1), which freed up enough area on the chip to add the analog/digital circuitry needed to get the higher speed and the self-calibration for accuracy over time and temperature ranges. As a result, Crystal's converter achieves 1.5-MHz throughput, about 10 to 12 times faster than competing 12-bit monolithic chips, even those fabricated with high-speed BiCMOS, says John R. Croteau, Crystal's manager for high-resolution data-acquisition products. Hybrid circuits, already behind monolithics in price and power consumption, take another step backward because the Crystal ADC's typical conversion time of 1.0 μs (2.5 μs maximum), and 1.5-MHz throughput rivals their performance.

Crystal's CMOS CSZ5412 integrates entire analog subsystems, including a background reference, a proprietary reference generator circuit, and auto-zeroing techniques. It also features a digital self-calibration scheme built around an on-board microcontroller. Setting an on-board control register location allows the device to calibrate itself every 300 to 400 μs. With all this done on-chip, accuracy is designed into the CSZ5412 rather than being factory-calibrated, Croteau says.

Achieving 12-bit accuracy was pulled off by Crystal's engineers without any sacrifice in throughput or conversion speed (see story, p. 70). To obtain 1.5 MHz throughput, the CSZ5412 uses

1. **12-BIT.** Using a 3-μm linear CMOS process, Crystal designers have built a 12-bit monolithic ADC with a typical conversion time of 1 μs.
second sample/hold holds it valid at point B during the second flash. Crystal engineers say that the first S/H allows the second to release after the first flash conversion; its acquisition period is thereby pipelined with the second flash. The first S/H will then acquire the analog input signal and ensure that the voltage at point A is valid to 12-bit accuracy before the end of the second flash. Another convert command can be issued before the decoder has settled, leading to the pipelined cycles.

To achieve 12-bit accuracy, the CSZ5412 piles digital calibration on top of its analog techniques. Upon power up, the CSZ5412 resets and is initially calibrated. Anytime afterward, hardware or software can initiate calibration, ensuring accuracy over operating life or temperature conditions.

The combination of analog and digital calibration techniques employed by Crystal engineers teams up to achieve better than 0.02% total harmonic distortion. On the digital side, Crystal designers incorporated a correcting micro-controller that ensures no missing codes and better than 68-dB signal-to-noise distortion. Offset and full-scale errors are similarly calibrated to within ±½ LSB.

In the CSZ5412, background calibration is an ongoing process that fine tunes the device’s offset and gain transparently to the user. Obtained by setting an on-board control register location, the feature allows the circuit to calibrate itself every 300 to 400 µs, depending on the converter’s other activity. This provides the ADC’s guaranteed accuracy, Croteau says. During every background calibration cycle, the converter compares its positive and negative full-scale code transitions with its positive and negative voltage reference signals. If the error exceeds ±¼ LSB, the device adjusts its transfer function accordingly, he says.

In the first flash conversion, the 64 reference levels define the end points of 64 segments that are the chip’s transfer function. Ideally, references are evenly spaced, to achieve a perfectly linear transfer function. Any errors in the references cause nonlinearity and distortion. To prevent that, the reference generator circuit constantly adjusts the converter’s linearity, ensuring accuracy throughout its operating life. A reference generator consists of an integrator and 64 sample/hold amplifiers (see fig. 3).

In operation, the integrator generates a ramp starting at zero scale, VREF, and ending at full scale, +VREF. The sample-and-hold amplifiers sequentially sample the integrator’s output, resulting in 64 evenly spaced reference voltages. This “walking reference” continually ripples through the sample-and-holds, updating the references.

In addition, the CSZ5412 maintains excellent differential linearity at its segment boundaries. Inaccurate decisions by the comparators in the 6-bit flash can lead to missing codes. Therefore, all comparators are auto-zeroed to avoid errors traceable to offsets or low-frequency noise. An integral part of the comparator, the auto-zero technique involves storing the comparator’s offset on a capacitor: in effect, subtracting it during the comparison. The auto-zeroing improves rejection of low-frequency phenomena such as 60-Hz or 50-Hz line noise.

In the two-step scheme, it is possible for offset errors to occur as a result of threshold voltage mismatches in transistors or other factors. To compensate for these errors, the CSZ5412 adjusts the starting point of the walking reference. Each time the integrator finishes its ascent, it returns to its starting point, VREF. Before the ramp begins, a digitally-variable capacitor array (multiplying DAC2) adjusts the starting point to zero scale. The magnitude of adjustment is determined during the converter’s calibration cycle. During calibration, the CSZ5412 switches VREF into its analog input. An on-chip microcontroller then uses MDAC2 to servo the walking reference’s starting point to the output of the sample/hold (S/H), thus compensating for all offsets.

The resulting setting of MDAC2 is stored on-chip in static random-access memory and is subsequently used each time the integrator returns to zero scale. The CSZ5412 similarly adjusts its full-scale setting. The ramp rate in the integrator determines the spread between reference levels and therefore the CSZ5412’s analog input range. The CSZ5412 calibrates full scale by trimming the capacitor in the integrator and thus the ramp rate. After it adjusts offset during calibration, the CSZ5412 switches +VREF into its analog input. It then adjusts the final reference value to precisely equal the output of sample/hold (S/H), which includes all full-scale errors.

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MIXED-SIGNAL ASICs GRAB DISK DATA TWICE AS FAST

Analog Devices Inc. is easing a major bottleneck in disk-drive performance with a pair of application-specific integrated circuits that recover data from disk heads at greater than 50 Mbits/s—double the throughput of competing designs. The new chips also recover data at error rates as good as discrete active components and small-scale ICs, which are now the bread and butter of readback electronics. The AD890 precision wideband channel processing element and the AD891 rigid-disk data-channel qualifier work in concert to produce low-jitter, accurately positioned digital pulses corresponding to recorded flux transitions on the disk platter (see fig. 1).

A 4-GHz bipolar process using thin-film resistors and sophisticated mixed-signal capabilities, both new strokes in designing a data-recovery circuit, enhance performance of the 890/891 chips. The Norwood, Mass., company also provides flexibility for disk-drive design through user-defined passive filters. By choosing filter components, disk-drive manufacturers can use the 890/891 chips to produce variable performance levels and match those levels to required data transfer rates. The discrete approach is less flexible by comparison and needs considerable space. It also requires tweaking or trimming of components even at the lower 25-MHz rate.

The upshot of Analog Devices' accomplishment is faster product development—a key factor in the supercompetitive disk-drive market. The 890/891 chips are optimized for hard-disk drives but have also generated serious inquiries from developers of fiber optic data links and optical disk drives, which have similar signal processing requirements, says Phil Carrier, Analog Devices product marketing manager. Volume shipments of the 890/891 chips have begun to a major disk drive manufacturer for its next-generation of drives, to be introduced in 1988. The chips cost $7.50 each in quantities of 10,000 and packaged in a plastic leaded chip carrier.

The 890/891 chips foreshadow a family of tailored-performance ASICs from Analog Devices (see story, p. 79). Already developed is a single-IC version of the pair, although this device has reduced performance because of the coupling between mostly analog front-end circuitry and digital output. Also in the works are ICs implementing other disk drive electronics—all with greater flexibility and performance in specific application areas. Included are a 50-Mbit/s, ECL, third-order phase-locked loop device with a 200-MHz voltage-controlled oscillator and fast acquisition times; low-speed TTL versions of the disk-drive ICs; and ICs with embedded read-channel PLLs and encoding/decoding logic and data separators. Versions of these components optimized for optical applications, such as CD ROMs and WORM drives, are also planned.

In data-recovery circuits, the read-signal channel presents design challenges because of a difficult electrical and mechanical environment: low and continuously varying signal levels from the head; severe noise corrupting the already weak signal; mechanical tolerances affecting rotational accuracy; and temperature variations eroding re-
peatable performance. Working in this difficult environment, other approaches had revealed drawbacks, leading Analog Devices to believe there was room for improvement.

Discrete active components and small-scale ICs—available from National Semiconductor Corp. in Santa Clara, Calif., and Silicon Systems Inc. in Tustin, Calif.—cannot exceed bit rates of 15 to 25 MHz without considerable design effort and cost. This occurs because small component variations produce unacceptable phase differences, timing skew, propagation-delay mismatches, and other subtle effects. If the stored bits are not recovered accurately and with precise timing, drive performance will be impaired regardless of the data encoding scheme. In contrast, if the stored bits are recovered error-free, then digital ICs are capable of performing—even at high throughput rates—the subsequent functions of data separation, clock regeneration, and data decoding.

A FLASHY PROCESS

The technology behind the Analog Devices' readback IC pair is a 4-GHz bipolar process called Flash, featuring double-level metallization and laser-trimmed thin-film resistors (see fig. 2). Although the Flash process is not unique to Analog Devices, its combination with thin-film resistors is a first. The thin-film resistors are key: They provide temperature-stable performance and are highly predictable, which allows the precise design of gain and exponentiation function blocks. Control comes through stable and predictable currents in the bias circuits and the ability to compensate for temperature variations in gain and offset. The internal logic is constructed with reduced-swing emitter-coupled logic, with typical propagation delays remaining below 600 ps per gate; outputs are standard ECL levels. The primary benefit of this scheme is a high-speed process that is factory—not user—trimmed.

The 890/891's operation is enhanced by their sophisticated mixed-signal capabilities, a new stroke in designing a data-recovery circuit (see fig. 3). On a disk, binary signals are recorded as flux reversals. These occur at intervals that depend on the particular data encoding scheme, creating the need for low jitter and stable phase response in the recovery circuit. The read head senses the flux changes and generates a weak signal, which is then amplified by a preamp located as close as possible to the head. This signal then goes to the AD890 variable gain amplifier, the crucial performance element over the wide dynamic range of the head signal.

The VGA provides a continuously variable gain of over 30 dB; its output is precisely the level required for optimal operation of the subsequent circuitry. The control signal for the VGA comes from the automatic-gain-control circuit, which must constantly adjust the VGA's gain. The control circuit completes a feedback loop which uses the signal level (the signal from the head) to maintain the desired output level.

The read-head signal, as delivered by the VGA, goes through several filter and buffer stages, and is then used for two functions: driving the control circuit and continuing through the signal processing chain so the actual binary data can be extracted. The AGC circuit's precision full-wave rectifier produces an output proportional to the average value of the input signal—the output of the VGA. In turn, this steady-state output is used to develop an exponentially proportional signal to set the VGA gain.

The exponential factor ensures that the overall loop gain and response will not vary with AGC setting. The attack and decay rates of the AGC gain must be matched to the application: too slow would result in insufficient response time while too fast would cause instability and gain pumping. Gain pumping is an undesirable effect in which the actual gain changes do not conform with the intended changes.

At this point, the amplified signal is not yet ready for decoding into 1s and 0s. Additional filtering and equalization are required to shape the signal amplitude and phase spectra to compensate for distortion, phase shifts, and nonlinearities in the writing and reading processes. These undesirable effects stem from head-coil inductance, mechanical-arm resonances, and other subtle causes.

The filter design is difficult and must be undertaken by the drive manufacturer based on the disk technology's characteristics and the head design. Filtering represents value added by the manufacturer, and here passive RLC components yield the best repeatability, stabil-
ity, and cost characteristics. For filtering purposes, present digital signal processor ICs cannot handle 50-MHz data rates and the low signal levels would require expensive conditioning and ADCs.

The filters also differentiate the signal to locate its peaks. Both the normal and differentiated versions pass to the AD891 threshold comparators. The threshold level is set to qualify valid pulses while ignoring noise. The comparator outputs go to a flip-flop and then to a one-shot, which produces data-output pulses of precise width. It is critical that the one-shot have highly stable outputs—even slight drift or jitter can be interpreted as incorrect data-bit timing, leading to problems in the disk controller’s timing recovery circuitry.

In addition to filtering options, the readback ICs also offer flexibility in other areas. One feature allows the automatic gain control to be turned on or off by digital control lines and another sets a programmable gain amplifier by external voltage levels. Also, input clamping can be switched in to prevent disk write signals from overloading the input, which would erode transition times in the read mode. Filtering and equalization are designed to occur in stages for optimizing the signal.

Overall, the readback ICs live up to stringent design goals. Specifications for the 890/891 functional blocks guarantee data bit recovery at up to 50 Mbit/s, though the ICs have achieved up to 70-Mbit/s rates. The AGC bandwidth is 100 MHz and its control voltage response is linear to within ±0.25 dB over a ±26 dB range (and nearly as good to over 40 dB). The VGA’s equivalent noise figure is only 5 nV-Hz.

In addition, the threshold comparators show less than 3-ns propagation delay and are matched to better than 300 ps. Finally, the timing error contributed by the AD891 from offset, gain, and drift is guaranteed to be less than 1 ns. This is in lieu of the more common “typical” specification, with its usual wide spread in actual values, which often forces the circuit designer to incorporate compensating trims.

Development of the IC pair took nine months from initial planning to functional first silicon. A proprietary circuit simulator, called ADICE (Analog Devices’ Spice-like Simulator), running on a VAX 8800 was used for the bulk of the 890/891 design. In addition, a CALMA-based automated layout and device checking package was used in the design process for the final layout.

The 890/891 are the result of a convergence of several influences within Analog Devices: the identification of markets where existing technology may be inadequate; the search for high-volume market niches; process technology that allows high-speed, highly-predictable designs; and a careful understanding of disk-drive manufacturer’s design needs.

In addition, developing a subsystem for a specific application area was a shift from Analog Devices’ traditional approach of providing high-performance, building-block components such as op amps, ADCs and DACs, or DSP chips—parts that could serve in almost any electronic circuit design. Ray Stata, Analog Devices’ president and chairman of the board, says “The new ASICs should lead to the development of an entirely new generation of high-speed analog signal-processing ICs—products that should dominate this kind of specific application in the 1990’s.”

For more information, circle 481 on the reader service card.

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**The new ASICs should speed development of a new generation of high-speed products that should dominate this kind of specific application during the 1990s.**

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3. **DATA RECOVERY.** Sophisticated mixed-signal functions are needed to achieve error-free data recovery at high rates. The AD890’s variable gain amplifier provides output at precisely the level required for optimal operation of circuitry.
The times, they are a changing, and nobody knows that better than Ray Stata, president and chairman of Analog Devices Inc. Specifically, the military and industrial markets that have long been Analog's mainstays are changing, with growth slowing and customer spending declining. So, over the next five years, Stata plans to emphasize new markets, and he's determined not to miss out on any opportunity to sell his products, especially where no one else is trying. And while he's at it, he wants to improve quality all across the board, from cutting design time to eliminating late deliveries.

Known as the quintessential purveyor of data-acquisition devices, the Norwood, Mass., company, doesn't want to be regarded that narrowly any more. "Our business is better characterized as real-world signal or information processing, rather than acquisition, because our products do more than acquire data," says Stata. While most of its revenue will still come from data-acquisition devices, especially in the industrial and military markets, the company wants to strengthen its position in other areas as well.

Analog has targeted two markets on which it pins its expansion hopes: high-performance computer and peripheral applications, where it is already a player, and portions of the consumer hardware market dominated by Japanese companies. Both markets have substantial growth projections and high-performance needs, characteristics that, in the past, allowed Analog to rise to the fore in the analog integrated-circuit market. The AD890/891 mixed-signal data-recovery ICs that Analog is planning for the high-performance disk-drive arena (see page 76) constitute Analog's first foray into the world of application-specific ICs and look to be the harbinger of things to come.

A clue to the shift in market focus may be found in company financial data. Analog Devices had fiscal 1987 revenues of $370.4 million, up 11% from last year's $334 million. And while growth goals in recent five-year plans at Analog have been in the 25% per year range (see graph), Stata says "We'll probably tell stockholders growth slows at Analog Devices

GROWTH SLOWS AT ANALOG DEVICES

1973-1977
1978-1982
1983-1987

*THE RATIO OF SALES IN EACH YEAR OF THE FIVE-YEAR PERIOD TO SALES IN THE FIRST YEAR OF THE PERIOD.

and expect more like 20% in the near term." That's primarily because of the slowed military and industrial market growth.

One analyst sees Analog's push for more computer and selected consumer device business as a sensible result of a dimming of prospects in the military market. Some 30% of Analog's worldwide revenues come from military system customers, "but slower military sales growth coupled with tougher pricing could prevail through the next administration," says Michael Kubiak, a semiconductor analyst at Kidder, Peabody & Co. in San Francisco.

Stata isn't divulging any details of the financial goals of the five-year plan for 1988-1992, which the company has been working on for over a year, but outlines of the plan plus the efforts of internal task forces and some insight from analysts provide clues about the company's future. Indications are that high-performance computer and peripheral applications will account for 30% of revenues in two or three years, up from 20% today; that the company is going after performance-oriented Japanese-dominate analog sockets in consumer hardware; and that there's a bottom-up push to improve product quality and to shorten the time required to design and deliver products.

While these goals can be accomplished, no one says it's going to be easy. Because the company is giving itself five years to get the changes in place and to establish its market share, Kubiak is optimistic, but wary. "Analogue has a good shot at achieving those goals," he says. But he notes that some of the consumer applications Analog may be targeting are also attracting Motorola Inc. and Texas Instruments Inc. Analog has succeeded in the analog business by avoiding competition with such giants. "Historically, they've done a good job of getting into markets that aren't served by the billion-dollar companies," Kubiak says. "Now that's changing. These are highly competitive, high-volume markets, and Analog still has to prove that it can handle that kind of competition."

On the other hand, he notes that Analog faces only limited competition in its traditional business. "The fragmented nature of the analog market protects them from any one competitor across all the company's product lines. Only Burr-Brown Corp. competes with Analog in both analog IC and assembled products, and Japanese competition is limited," says Kubiak.

One advantage for Analog is that the computers and peripherals markets are not dominated by any of the power-hitters. Andrew Rappaport, president of the Technology Research Group, a Boston consulting and market research organization, points out that lin-
Network management system (NMS)
The NMS efficiently monitors/controls switching and transmission networks. For easy trouble-shooting, it offers expert system technology which guides users to the source of system problems.

Digital switching system: NEAX61
The core of the demonstration was the NEAX61. It displayed integrated broadband and narrowband switching capability, as well as 1.5Mbps high-speed packet switching.

1.12Gbps FOTS
The 1.12Gbps Fiber Optic Transmission System (FOTS) demonstrated its ability to combine 16,128 voice channels into a single-mode fiber.

AT THE R&D ZONE
NEC's intensive R&D efforts, ranging from components to total systems, gave visitors a glimpse of many futuristic visions come true.

4Gbps FOTS
This ultra high-speed system utilizes 1.55μm DFB LDs and InGaAs APDs and transmits over 30km without repeaters.

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MAXIM'S PROGRAMMABLE FILTER OUTPERFORMS THE FIELD

For the first time, a filter IC combines full programmability and high performance

by Bernard C. Cole

A new family of microprocessor-programmable switched-capacitor active filters boasts a combination that has eluded filter designers till now: a wide range of programmable features and superior performance. The MAX260 filter series from Maxim Integrated Products Inc. can be reconfigured by a microprocessor to serve as any of a wide variety of lowpass, bandpass, allpass, and notch filters—and there's no need for external components. Under direct microprocessor control are the center frequency, the Q value, the order of the filter, the resolution, and the type.

The performance of the MAX260 series (see fig. 1) should open new applications for programmable filters. The MAX260 features a maximum center frequency of about 75 to 100 kHz, a four to five times improvement over competitive devices, and a Q value range of 90, also a four to five times improvement, says David Fullagar, vice president of research and development for the Sunnyvale, Calif., company. Moreover, he says, the center frequency can be programmed to any of 64 values over its range, while the Q can be programmed to take on any of 128 values over its full range.

Systems designers are searching for satisfactory programmable filters because they find the task of analog filter design bewildering. That's not surprising, given the number of variables and choices going into the shaping of a needed circuit response. After the question of exact shape comes one of filter type, then parameters, and then the choice of implementation—passive or active. Both active and passive filters, once designed in, are pretty well fixed. And with the conventional, nonprogrammable filter, changing the filter characteristics would require a change in components, something digital designers are not prone to do.

Recent attempts to build microprocessor-programmable switched-capacitor filters have met with mixed results. On the one hand, a number of active-filter-based designs have emerged that combine reasonably high performance and microprocessor programmability but only by keeping tight constraints on applications. Such a filter, for instance, may be confined to a job in data communications, telecommunications, or instrumentation. On the other hand, some general-purpose switched-capacitor filter designs can be reconfigured under microprocessor control, but only at substantial performance costs compared to traditional switched-capacitor filters. In exchange for this programmability as to type and order, such designs have kept center frequency to no more than 20 kHz, Q values to 20 or so, and clock frequency to no more than 300 kHz.

Another advantage of the MAX260 family is that it can be programmed as a second-, fourth-, or eighth-order filter. Competitive devices cannot directly implement a second- or fourth-order filter; they require the addition of an allpass filter to bring the order from the eighth to the sixth, fourth, or second. Competitive microprocessor-controlled universal filters operate at clock frequencies that go nowhere near the MAX series rate of 2 MHz.

Also, because of a proprietary self-biasing scheme, noise specifications of the MAX series are one-fourth to one-third that of competitive programmable devices. In a fourth-order Chebyshev-
New PC/AT-Based Image Processing Breakthrough.

Inside:
- Datacube Boosts International Service
- High Speed DSP Processor Module Receives Kudos
- MaxVideo Family Continues To Grow
- New Look For Frame Stores

Small But Powerful
MaxVision AT-1 is a small box which can go anywhere, but its stylish design makes a neat fit on top of your PC/AT and right under your CRT. Inside the box is a powerful real-time ALU processor, a multiplier unit, three image frame buffers, and input/output processing path lookup tables. Its pixel control feature means users can choose regions of interest within an on-screen image, and process only pixels inside that region's borders. But the real power of MaxVision's ImageWare is that its software lets you use it fully without having to get involved with any hardware details.

MaxVision AT-1 is Datacube's new, powerful plug-in image processing solution for the IBM PC/AT and its clones.

The MaxVision AT-1 has achieved immediate acclaim as a superior development-level image processing system for OEMs, system integrators, consultants and users designing vision and image processing systems for government, defense, security, industrial automation, medical imaging, university R&D, and educational applications.

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The MaxVision AT-1 software has three layers. A window/mouse/user interface allows a quick interaction with the image processing system. All the capabilities of the system are available as mouse selectable items. Besides the user interface, there are two additional layers to MaxVision's software. A command line interpreter enables more experienced programmers to bypass the mouse-driven menus by entering C-language formatted or natural language commands via the keyboard. Finally, all MaxVision's image processing functions and primitives are stored as C-callable functions... allowing programmers to customize, for example, their own image processing software.

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MaxVision is truly easy to run. Simply plug it into any IBM PC/AT, turn on the power, slip in the distribution floppy, and start processing images. MaxVision takes its commands from a pointer device like a mouse, or from the keyboard. All you do is point to the appropriate section of the user friendly menu and the corresponding action takes place. No need to learn how to program a complicated image processor... you can spend your time doing image processing.

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Easy to use, MaxVision takes commands from a mouse or keyboard. No complicated programming is required. Just plug it in and start your image processing using its user-friendly menu. And even though it's simpler to use than you would expect, it is designed to run a wide variety of powerful image processing routines.

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EXECUTIVE OUTLOOK: CRASH ISN’T CHANGING PLANS — YET

Steady as she goes, but keep your eyes peeled!“ is the watchword for captains of the worldwide electronics industry. The stock market crash has them checking and rechecking the horizon, but they still see no solid shape that calls for a course correction.

So on they go with plans they had already made for new products and technology development. Not one interviewed for Electronics’ annual survey of industry executives on the outlook for the coming year would admit to having shelved any work in progress or trimmed back production plans as a result of the stock-market debacle or recent changes in monetary exchange rates. Technical innovation, for now, marches on, while contingency plans are drawn up.

Overseas managers have a special set of problems to face during the coming year. The falling value of the dollar puts major pressure on many European electronics companies (p. 93). The rising yen also plagues the Japanese, wiping out profits and forcing them to relocate production overseas (p. 97).

In the wake of the October crash in stock markets around the world, all the executives surveyed are alert for any sign of an economic downturn. So far, most of them don’t see one coming. But virtually everyone says it’s too early to tell—that it will take time for the real impact of the crash to be felt.

“No one claims they’ve seen any impact yet,” says Alfred J. Stein, chief executive officer of VLSI Technology Inc. in San Jose, Calif. “I think that is a very good sign. However, by the same token, I would not expect to have seen anything yet. I think it will be six months to a year before we know what kind of impact it will have.”

Stein himself is wary: “Personally, I cannot help but believe we are going to see some slowdown.” And a number of other executives agree with him. Most are not sure exactly what they are worried about, but they can’t imagine the crash would have no repercussions. At least two—James A. Bixby, president of Brooktree Corp. in San Diego and Joe Henson, president and chief executive officer at Prime Computer Inc., in Natick, Mass.—used nearly identical words to express their views: You can’t yank a trillion dollars out of the economy in a week and not see some effect.

But the effect to date seems to be caution, not action. Expectations are being scaled back and plans are being laid for trimming expenditures—if a downturn comes. “I think you have to be very careful about assumptions, and my guess is people will be more careful than they would have been otherwise,” says Dean Morton, chief operating officer of Hewlett-Packard Co., Palo Alto, Calif. Meanwhile, nobody wants to make the mistake of overreacting, thereby choking off growth that would otherwise have occurred.

While exercising a certain amount of caution, a number of executives are also expressing a degree of optimism, the reasons for which vary. One reason, ironically, is the slump endured by...
the electronics industry in 1985 and 1986. It left a lot of companies in excellent shape to weather any downturn that might occur. "We went through two terrible years while the economy was doing pretty well," says Gordon E. Moore, chairman and chief executive officer of Intel Corp. in Santa Clara, Calif. "I think we all got ourselves better positioned for pretty tough times. We shrunk our own employment from a peak of over 26,000 to about 18,000. We haven't enjoyed the good times long enough to build that back up again." Walden Rhines, senior vice president of Texas Instruments Inc.'s Semiconductor Group in Dallas, echoes Moore's point. "The depth of our recessions tend to be proportional to the height of our euphoria," Rhines says. "We've only had a modest upturn in 1986-87."

And that lack of euphoria could help offset any ill effects from the stock market crash. VLSI Technology's Stein, for one, thinks times have changed since 1983 and 1984, when the boom got out of hand and book-to-bill ratios ran as high as 1.5 and 2. "That has not happened in this cycle," he says. "It went up nicely, to the 1.2 to 1.3 range, and now it has dropped back down to around 1. It is a nice, strong, steady buildup. This market crash adds to the caution against overbuilding, overcapacity, or false bookings."

The aftershocks of the U.S. market crash are, of course, reverberating overseas. However, overseas markets tended not to slide as fast or as far, and the effects are likely to be gentler. In West Germany, for example, economists are revising downward their projection of gross national product growth, from the 2% forecast before the crash to about 1.5%.

That decline is not big enough to ignite panic. Siemens AG, for example, is delaying expansion or cutting back capacity in some rather low-tech sectors, but it will not allow high-tech fields to suffer, says Alexander Grossmann, a vice president at the Munich company. Similarly, Klaus Bombhardt, managing director at Heilbronn-based Telefunken electronic GmbH, says, "We have not changed our plans to further develop our facilities, and we are counting on another business increase in 1988." And Lubo Micic, managing director of ITT Semiconductors Group in Freiburg, says, "We will not alter our investment plans, nor will we delay the development of new products." In France, Jacques Bouyer, president and general manager of RTC-Compelec SA, also says no projects or programs have been shelved.

The Tokyo stock exchange slid in sympathy with the U.S. markets, but it didn't drop as far, and it rebounded sooner. "This particular crash was centered in the U.S. and the direct impact in Japan was small," says Hiroshi Asano, executive vice president of Hitachi Ltd. in Tokyo. "But the indirect impact—the increase in the value of the yen—hurts badly." It crimps considerably the export-oriented industry of the Japanese.

Some American executives think that the stock market crash may end up helping the U.S. economy in other ways as well—notably by spurring some much-needed action on the federal deficit. "Now our friends in Washington are saying they're going to reduce the deficit in 1988 and 1989," says J. Tracy O'Rourke, president and chief executive officer of Allen-Bradley Co. in Milwaukee. And while the dollar is cheaper and the balance of trade therefore better, O'Rourke says, "miraculously, somehow, inflation does not seem to be responding... Profits are up. Liquidity is up. Money is relatively cheap, and there's lot's of it."

"I think if the crash did nothing more than to get that damn Congress and Administration together to do something constructive, it's going to be almost worth it," says John Krehbiel, chairman of Molex Inc. in Lisle, Ill.

A number of U.S. executives, however, think the electronics industry has some built-in strengths that will keep it prosperous no matter what the government does. Several point out that the computer industry—the major market for components—is starting a strong new product cycle. "There has been a change from the low-end machines—the 8088-based machine—to the 286-based machines," says Intel's Moore. "The 386-based machines are coming out at the high end and the first real 32-bit software is becoming available." All of which means that the new product cycle is working against the possibility of an economic slump. "I personally believe the product cycle will dominate," Moore says.

**The declining dollar is sharing** attention on the economic scene with the stock market crash. What the weaker dollar means to electronics industry executives depends on where they do business. Those who manufacture in the U.S. and sell...
THE DECLINING DOLLAR: BAD NEWS FOR SOME EUROPEANS, BUT NOT ALL

The steep, steady decline of the value of the U.S. dollar against West European currencies is hurting some European electronics businesses, but not all of them. It all depends on where their markets and production facilities are.

From March 1985 till October of this year, the value of the U.S. dollar tumbled 41.4% against the average of West European currencies. This has, in effect, made American goods—and goods from countries whose currency is tied to the dollar—less expensive on European markets and, conversely, European wares correspondingly more expensive in U.S. markets.

"The difference between the franc and the dollar has more of an effect on our outlook than the stock market crash," says Guy Dumas, president of Matra Harris, the chip-making subsidiary of Matra SA in France. "We have not found a solution."

West Germany’s electronics industry, however, is not suffering heavily from the dollar’s drop because only 7% or so of this sector’s exports finds its way to the U.S.—far less than Japan’s exports to America. "And should the dollar weaken even more, the effect on the electronics industry will not be all that dramatic," says Alexander Grossmann, a vice president at Siemens AG, Munich. Siemens itself, he says, is not suffering all that much from the dollar’s decline, because Sie-
Unlike recent International Solid State Circuits Conferences, the 1988 edition of the world’s most prestigious semiconductor event will feature hot developments in all major chip areas. Last February, the ISSCC was heavy in memory circuits, both in terms of numbers of papers and in their significance. The 31st edition, set for Feb. 17 to 19 in San Francisco, is balanced with significant developments in semicustom logic, processors, and analog devices, as well as in all types of memories—random-access, read-only, and nonvolatile.

Memory is still a major player. Among the highlights are two speedy 60-ns dynamic RAMs, one a 16-mbit design from Matsushita and the other a 4-mbit design from Siemens; and two biCMOS 256-Kbit static RAMs from Hitachi and Fairchild that feature access times of 8 and 12 ns, respectively. There also will be a novel nonvolatile ferroelectric static RAM from Ramtron.

In logic, Actel will introduce a user-configurable gate-array technology based on a new antifuse technology that boosts density. Microprocessor fans can cheer for Texas Instruments’ gallium arsenide 32-bit central-processing unit with a reduced-instruction-set architecture technology, and a 40-MHz 32-bit CMOS design from General Electric. On the analog side, there’s an automatic place-and-route system for mixed analog and digital circuits from IBM and a number of advanced data-conversion circuits from Analog Devices, AT&T Bell Laboratories, Hitachi, NEC, and Philips.

As always, the big story in DRAMs and SRAMs will focus on density and speed. Garnering a lot of attention will be a 60-ns 16-mbit DRAM from Matsushita Semiconductor Research Center, Osaka, Japan. Built with an aggressive 0.5-µm CMOS process, it incorporates a high-capacitance trench structure that surrounds the active devices. The result is a cell that’s only 3.3 µm². There’s also a 60-ns 4-mbit DRAM, hot-electron-resistant, from Siemens AG, Munich, West Germany. Its designers believe the memory will scale well to 16 Mbits without sacrificing 5-V operation. This part uses dual-gate FET peripheral circuits, which promise a hundredfold improvement in device lifetime over single-gate designs. Fabricated with a conservative 0.9-µm CMOS process, its trenched-capacitor-based cell measures only 10.58 µm².

Two biCMOS 256-Kbit SRAMs will be eye-openers. From Hitachi Ltd.’s Device Development Laboratory in Tokyo comes one laid out as 256-K-by-1 bit, which smokes along at 8 ns. Its 66.3 µm² cells are made with a 1-µm double-poly-silicon, double-metal process; power dissipation is 400 mW at 50 MHz. Only slightly slower is the 12-ns design from Fairchild Semiconductor Corp. of Puyallup, Wash., now a part of National Semiconductor Corp. Also a 256-K-by-1 bit array, it has

They include: a user-configurable gate-array, a 32-bit GaAs RISC chip, a 40-MHz 32-bit processor, advanced data converters, an 8-ns biCMOS 256-K SRAM, a ferroelectric SRAM.

by Bernard C. Cole

ISSCC: DAY 1 IS DOMINATED BY DIGITAL

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96.5-μm² cells and dissipates about 750 mW.

Although traditional EPROM and EEPROM designs will also push the speed and density barriers, standing out will be a novel 256-by-1-bit ferroelectric shadow RAM integrated onto the same chip with peripheral circuitry fabricated using standard CMOS technology. The device is significantly faster than EEPROMs—production devices will sport 100-ns read-erase-write cycles [Electronics, March 5, 1987, p. 32]. According to the researchers from Ramtron Corp., Colorado Springs, Colo., the nonvolatile RAM uses a single 5-V supply and can be reprogrammed as many times as the most durable EEPROMs, in excess of 10⁸ cycles, over the full military temperature range of -55°C to +125°C.

In semicustom logic, check out a CMOS electrically configurable gate array from Actel Corp. of Sunnyvale, Calif. It employs an antifuse architecture for programming both horizontal and vertical elements. That’s a departure from traditional CMOS programmable logic devices, which use a stored charge to program a cell, or bipolar PLDs, which use a fusible link. The result is significantly increased density. Prototypes made with 2-μm CMOS technology feature 295 configurable modules with eight input/output pins each, 55 user-definable pins, and 112-K programming elements in a 260-by-360-mil die.

In a more traditional vein will be super-high-speed logic devices from Cypress Semiconductor Corp., San Jose, Calif., and Lattice Semiconductor Corp., Beaverton, Ore. Cypress offers a 66-input-term and 258-product-term ultraviolet-based programmable logic array. It is made with an 0.8-μm double-metal CMOS process and features an unprecedented 50-MHz throughput, dissipating only 440 mW. Lattice also describes an electrically erasable device: a 9-ns, 450-mW PLD fabricated with a 1.0-μm CMOS process that features a 20-ns programming time.

Heading the processor list will be a 32-bit GaAs RISC microprocessor from Texas Instruments Inc., Dallas. Containing a 16-by-32-bit register, 32-bit arithmetic logic unit, and a six-stage pipeline, the circuit is fabricated with integrated injection logic and a 1.5-μm heterojunction GaAs bipolar process.

Then there’s General Electric Co.’s 32-bit entry from its Syracuse, N.Y., operation. The 40-MHz CPU is fast: 25-ns access time. It gets its horsepower through the use of a four-cycle instruction pipeline, a seven-cycle load-operation pipeline, and a 320-byte instruction cache RAM.

The glare of so many digital offerings won’t overshadow the analog developments. One from IBM’s General Products Division, Rochester, N.Y., will address the chore of creating mixed analog and digital circuits with computer-aided design. Using device-level automatic place-and-route methodology, IBM researchers claim up to 75% chip utilization.

At the circuit level, interest will be high for data-conversion offerings that use advanced algorithmic, pipelined, and flash designs. Analog Devices Inc., Wilmington, Mass., will describe a 14-bit, 10-μm analog-to-digital converter, and Hitachi Ltd., Tokyo, will lay out details of an 8-bit 20-MHz half-flash ADC as well as a 10-bit 20-MHz ADC with an internal sample and hold. And from Philips Research Laboratories in Eindhoven, the Netherlands, comes a 15-bit, two-stage, digital-to-analog converter.
Fluke’s Board Tester Can Cover All The Bases.

Some digital testers star in the development lab, others shine in production testing, and a few are best at troubleshooting in the field. But the 9100 series of microprocessor board testers from the John Fluke Manufacturing Co. aims to do a job in all three test roles. The Everett, Wash., company is grooming the compact emulative testers for design debugging in the lab, as well as for functional testing and fault isolation in the factory and field.

One of Fluke’s goals for the 9100 series is ease of use. The software simplifies and speeds other test-writing chores so that the typical troubleshooting program can be developed in only 20% of the time it usually takes...
HIGH SPEED STATIC RAMS.

From bit-wide to byte-wide, from 25ns to 70ns, Toshiba is the power — and the speed — in static RAMs.

When you think fast, think Toshiba. We have the organizations and the speeds to meet your requirements. In the popular 4K x 4, we offer a 25ns version in the standard 20 pin type and in a 22 pin version with an output enable function of 15ns. The output enable helps eliminate bus contention while increasing speed.

We were first with 2K x 8 devices which are ideally suited for cache memory applications. We now have a 25ns version in addition to our 35ns offering. Both are now available in plastic DIPs.

For high speed bit-wide applications, we are in full production of two versions of our CMOS 64K x 1 SRAMs. One with access times to 35ns, and one with the lowest standby power in the industry at only 100μA. Both plastic DIP and plastic SOJ packaging are available.

A new product introduction is the 16K x 4 CMOS static RAM with access time of 25ns. Standard 22 pin plastic DIP and SOJ versions are available, as well as a 24 pin plastic DIP and SOJ version with output enable access time of 15ns.

For byte-wide applications we have an 8K x 8 device with access times to 35ns. Packaging is 28 pin 300 MIL plastic DIP. For applications where parity is required, we have an 8K x 9 with speeds to 35ns. This device is also in a 300 MIL plastic DIP.

So when you’re thinking fast, think Toshiba. The power in high speed SRAMs.

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**FAMILY TYPE: HIGH SPEED MOS STATIC RAMS**

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<thead>
<tr>
<th>PART</th>
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NOTE: DIP = PLASTIC CDIP = CERDIP SB DIP = SIDE BRAZED CERAMIC SOJ = SMALL OUTLINE J LEAD PACKAGE
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Circle 108 on reader service card
In the drive to develop technology that can fabricate integrated circuits with submicron design rules, the image repeater has generally been overlooked. But now American Semiconductor Equipment Technologies Inc. has built a repeater that can handle submicron design rules, giving photolithographic fabrication techniques an important edge in their battle with newer electron-beam methods.

Repeaters, the precision tools used in making photomasks, function similarly to steppers—they project the pattern of a computer-generated design for an IC onto a section of the mask material, then move and project the pattern onto another portion. Besides reproducing the resolution of the design itself, they must be able to move and stop with a high degree of accuracy. ASET's 600 series (see fig. 1) of repeaters can handle resolution as low as 0.8 µm. Its positional resolution—the precision with which the repeater can move to a given position—is 0.1 µm, a 50% improvement over the 0.2 µm that is standard both with competing repeaters and with e-beam equipment. Along with increased precision, the new repeaters provide significantly expanded stage travel, of 13 by 13 in., which can produce a mask pattern of this size. By contrast, present systems typically travel only 6 by 6 in., or 6 by 9 in. at best.

ASET, a Woodland Hills, Calif., company that builds photolithographic fabrication equipment (see p. 115), achieved the improvements by drawing on technology borrowed from steppers. The 600 series includes an entirely new camera and employs high-numerical-aperture Zeiss lenses. The company also totally redesigned the mechanical staging that moves repeaters and the laser interferometer system that monitors this movement. The result is a system that can handle resolution down to 0.9 µm over an entire 14-mm-by-14-mm image field, and 0.8 µm over 11 mm by 11 mm.

The new design is a direct response by ASET to what its customers want. In 1986, the company surveyed its users about improvements they would like to see in their repeaters. Some 95% of them listed submicron capability as the most important thing ASET could provide.

 Besides its finer resolution, the 600 series maintains the key advantage of photolithography over e-beam techniques: faster throughput. For typical circuit densities on six-inch wafers, the repeater can make a mask, or reticle, in about five minutes or less, says Chris Van Peski, ASET's vice president for advanced projects. An e-beam system takes several hours. To aid throughput, a reticle changer under program control handles up to four reticles, and can exchange and align each within six seconds. Present image repeaters require 15 to 20 seconds, he says.

All things considered, ASET is convinced the new repeater will have a marked impact when shipments start next month. "From the very strong interest, we expect the 600 series will take a large part of the repeater market, and compete with e-beam for maskmaking," Van Peski says. The new ASET repeater costs $830,000 to $870,000, depending on options.

The only brand-new part of the 600 is the camera which Van Peski says "has features unheard of in an image repeater, but necessary to meet the tight tolerances demanded by the..."
Among the camera-control features is a separate microprocessor control for two key tasks: reducing distortion in the camera reduction ratio and directing its vertical positioning.

Among the new features is the apparatus for controlling focus to tolerances of 0.2 μm, measured by an air gauge at the bottom of the assembly and four pneumatic bridges that sense the distance above the surface (see fig. 2). Outputs of the bridges drive four silicon differential pressure sensors. The sensors' output is used by a microprocessor to control the vertical position, or focus, of the camera.

The 600 is the first repeater to employ a voice coil driver, which provides force without friction, to move the camera. A separate control system governs the camera reduction ratio, compensating for distortion and any changes in the index of refraction of the air as a function of pressure changes. The control loop senses barometric pressure, and also accepts input commands, and adjusts the vertical position and attitude of the object plane. Position of the reticle is sensed by three linear transducers, which provide feedback.

Pneumatic actuators, chosen because they operate without heat dissipation, allow the camera to move extremely small distances with high accuracy—as little as 0.1 mm with resolution of 1 μm. On the other hand, the repeater can also cover greater distances altogether. Its expanded stage travel will accommodate the six-inch wafers that are becoming the standard size in new semiconductor fabrication plants.

For the laser interferometer system, whose position monitoring task is the basis for repeater precision, ASET assembles for the first time on the 600 series many features appearing on other lithography gear. Among other things, it employs a standard dual frequency interferometer from Hewlett-Packard Co., along with specially designed differential interferometers that measure the stage position relative to a reference mirror mounted directly onto the lens housing. If the camera moves laterally, the laser system commands the stage to move a like amount.

"This is important to compensate for any camera motion," Van Peski says. The system is calibrated to provide position resolution of 1/32 wavelength, or just under 0.02 μm.

Closely linked with the laser system, the mechanical staging redesign is supported by a base 20 in. high, 62 in. long, and 30 in. wide that is fashioned from a block of granite. Because the motion during movement is determined by the flatness of the top and bottom of the block, the base is machined flat to 1 μm. The stage itself is supported by air bearings at all points of relative motion, so no friction or wear occurs. Both the x-stage and y-stage are anchored by the granite block, rather than the y-stage serving as a base for the x-stage, as in much other equipment.

In addition to finer resolution and greater precision in operation, the 600 series incorporates a number of other new features. One is grid matching, the capability of changing its internal grid system to match a grid data base from another repeater. ASET added this feature because in more than half of their business, independent maskmakers must match a mask set previously produced. To use it, the maskmaker needs only to measure the mask and transmit the data to the 600.

The 600 is operated through a CRT with job-oriented display screens. The computer is a Hewlett-Packard 9000 series 200 with 1 Mbyte of main memory. Extensive diagnostic software aids troubleshooting and repair of the system.\[For more information, circle 483 on the reader service card.\]
On October 5th, Fluke and Philips joined forces in a global alliance for test and measurement equipment. That means Fluke now sells and services Philips products in North America. With the same customer-driven support that Fluke has delivered for over 40 years. Call us. Because now there's a competitive alternative to HP and Tek. And that's a turn for the better. For you. Phone 1-800-426-0361 Ext. 77.
HOW GREG REYES TURNED AROUND TRE

Greg Reyes, president of American Semiconductor Equipment Technologies Inc., formerly TRE Semiconductor, uses a simple approach with any U.S. company that happens to be in the market for photolithography equipment for integrated-circuit fabrication. He says that all other things being equal, the customer ought to buy from an American company. An American company such as his, for example. He takes issue with anyone who calls the “Buy American” line an appeal to jingoistic nationalism. “It’s not really flag-waving, or even a strategy,” he protests.

As Reyes sees it, ASET's approach to selling to U.S. customers rests on a hard-headed recognition of the realities that govern how such big-ticket equipment as wafer steppers and image repeaters are bought. Even the most patriotic U.S. customer cannot be expected to lay out a million dollars or so solely because a product was made in California rather than Tokyo. The key word is “solely.” Reyes argues that when the quality of the equipment built in the U.S. matches that of equipment built in Japan and the price is competitive, why not keep the money at home? As he puts it: “Why buy Japanese? I'll give you a machine as good as theirs.”

ASET has done well with this pitch as an attention-getter, but it's not betting its future on pure flag-waving. The company has also put together a deft marketing strategy that seeks to avoid head to head confrontation with much larger U.S. competitors GCA Corp. and Perkin-Elmer Corp. Instead of going after the big merchant-market semiconductor companies, ASET focuses on selling to captive operations and selective niches, including gallium arsenide production and mask making. The company plays on the “special relationships” captives demand from suppliers, which are extra service, close coordination in applications, and prompt delivery of equipment. ASET counts Honeywell Inc. as its best customer, along with many other companies that are not in the merchant market but which nevertheless make a lot of ICs.

With this approach, the company has racked up improving sales since Reyes, a semiconductor-industry veteran, led a small group that bought it in March of 1986. Sales are now hitting an annual level of $20 million, and ASET is starting to show a profit.

Getting to that level took a lot of work. ASET had fallen on hard times during the chip recession of 1982-1985. Turning it around required nothing less than a “reinvitalization,” in Reyes' words. At the heart of the changes was an infusion of experienced management to fill key positions. Reyes has held top posts over a 20-year career at major chip firms, and also headed Eaton Corp.’s Semiconductor Equipment Group.

Reyes says the crux of the problem at TRE Semiconductor was that owners had little knowledge of the semiconductor industry at several promising niches. TRE Semiconductor was a subsidiary of TRE Corp., a conglomerate into everything from defense technology to cement. As a result, the semiconductor subsidiary lost its way and started losing money—$25 million in all.

Reyes saw that TRE Semiconductor could be a bargain at the right price: “Despite the losses, it still possessed strong technology.” The company also had a long-standing reputation in the field. It was founded in 1961 as the Microform Division of Electro-Mask Corp., the first independent maskmaker in the semiconductor business. And because of the red ink, Reyes says, TRE was a “very motivated seller.”

The members of his group put together a deal with TRE that got them a $20 million company for $5 million in cash. Once in charge, the new owners moved quickly. Top priority became a state-of-the-art wafer stepper that was already in the works. With further refinement, it became ASET's 900 series, now selling at a steady clip. It features five models, one of which—the I-line ASET stepper, with 365-nm lenses at the deep ultraviolet wavelength—is a banner product, pivotal in submicron applications. ASET is the major supplier to U.S. GaAs chip makers, who use it for 0.5-μm applications, and has shipped six systems against a growing backlog.

Although the future of steppers is downgraded in some quarters as a mature business, Reyes and ASET believe otherwise. He cites consultant projections of about 20% growth through the early 1990s, and is planning accordingly. Production of machines, now at two a month, can be boosted to five, which would increase volume past $50 million annually. A next-generation stepper is scheduled for unveiling in two years.

ASET is also looking beyond the semiconductor industry at several other promising niches. The company has an edge in these niches—ASET's mechanical staging equipment is somewhat larger than competing gear, so it can accommodate the manufacture of bigger products than wafers. Liquid-crystal displays and fine-line printed-circuit boards are potential applications, and Reyes says ASET has shipped machines to major companies in both fields. -L. W.
"I think differently than most people"

"I mean, to me, problems aren't a pain... they're opportunities.

...so when Tom told me he'd have to automate and go to more compact electrical transformers or go bankrupt...well, I was ready.

...meanwhile, I'm sitting in Chicago and it's 4:00 pm...he tells me he needs me tomorrow...I tell him we're on for breakfast...went home, threw some things together...forgot my toothbrush...and caught the last flight out... got in just in time for bacon and eggs.

We worked 12, sometimes 14 hour days at the molder's...just to fine tune the component dimensions...but we got those bobbins molded...went from 40 to 300 coil forms per hour...and Tom got the transformers he needed.

Like I said, no problem."

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NEC TAKES AN EARLY LEAD IN IMPROVED-DEFINITION TV

Motion-adaptive techniques and 60-Hz noninterlaced screen scanning are among the features aimed at solving distortion problems that plague today's televisions

by Charles L. Cohen

First out of the gate in the race to implement improved-definition television is NEC Corp. This month the Tokyo company is starting to market its IDTV chip set, and its subsidiary, NEC Home Electronics Ltd., is launching sales of an IDTV receiver.

Like other implementations that are sure to follow from Hitachi, JVC, Matsushita, Sanyo, Sharp, and Toshiba, the chips from NEC use digital image storage and signal processing to wring the best possible picture from the TV signals broadcast in Japan and the U.S. Motion-adaptive techniques and 60-Hz noninterlaced screen scanning are among the picture-enhancing features.

IDTV is the first step along Japan's chosen route to high-definition TV, due in the mid 1990s [Electronics, Oct. 15, 1987, p. 113]. It aims to cure many of the picture-distortion problems found in today's TV sets, and to improve image resolution. Planned for some time, IDTV had to wait until the price of semiconductor memory came down enough to make it feasible in the consumer market.

Thanks to its large complement of memory, a TV set built with NEC's chip set is able to perform signal processing along the time axis, a claim current digital TVs cannot make; they only perform signal processing along the vertical and horizontal axes of the image. Some of the system's nearly 7 Mbits of memory are used in a circuit that detects motion in the image and then maps out where in the image the motion is. More of the memory is used to separate the signal's luminance and chrominance components—known as the Y and C signals—and to perform the interpolation required for noninterlaced scanning. Both the Y-C separation and interpolation are motion-adaptive, relying on the motion-detection circuit to select the appropriate technique for a given area of the picture. All three processes—motion detection, Y-C separation, and interpolation—use data from more than one image field at a time.

NEC's chip set [Electronics, Oct. 1, 1987, p. 25] includes 7 image-field memories, 11 scan-line memories, and a handful of data converters. In addition, there are six special-purpose chips that detect motion in the image, separate the Y and C signals, perform signal processing, demodulate the color signal, perform interpolation, and generate clock signals.

In today's TV sets, color-signal components crossing over into the luminance signal reduce resolution and generate what is known as dot crawl at outlines within the image. Also, high-frequency Y-signal components that spill into the C signal produce spurious coloration, commonly called cross-color. Better Y-C separation is the answer to both dot crawl and cross-color. Oblique resolution—resolution along a line 45° from the horizontal—in current TVs is also not as good as it could be because of limitations in their Y-C separation circuits. And the interlaced scanning used in today's sets causes line flicker and reduces vertical resolution; both are addressed by moving to noninterlaced scanning.

IDTV tackles these problems with generous digital memory and digital signal processing. So much memory is used, in fact, that IDTV sets would be priced out of sight were it not for the current levels of memory density. They'll start out expensive, even so: NEC is setting the price tag at $2,500 in Japan for its first 27-in. model.

But such sets can improve the picture in ways that current digital TVs cannot. Digital motion-adaptive techniques dramatically improve Y-C separation and the interpolation process that makes noninterlaced...
scanning possible. In signal-processing terms, an IDTV set differs from a conventional TV in that it operates not just in a two-dimensional frequency domain, but in a three-dimensional one, says Shigeo Niitsu, supervisor of the Systems Engineering Department of NEC's Semiconductor Application Engineering Division. In addition to the horizontal and vertical frequency spaces used by conventional-TV signal processing, IDTV uses the time axis during processing. In other words, signal processing in an IDTV set involves more than one picture frame at a time.

Detection of motion within the transmitted image involves comparing one frame with the next to see what has changed. Motion detection is important to an IDTV set because it allows the Y-C separation and interpolation circuits to switch from one technique to another for areas of the picture, depending on whether the areas include motion.

For the areas of the picture where there is no motion, Y-C separation and line interpolation are achieved by in-field adjacent-line techniques. Interpolation of lines by this technique is used in some present large-screen TVs—primarily projection types—to provide increased scanning-line density. It is adequate for picture areas with motion because of the limits of the human brain: some image distortion is caused, but fine details within moving objects cannot be discerned by the viewer.

On the other hand, for some types of still pictures, adjacent-line interpolation can cause very visible picture degradation. IDTV sets, by using interfield interpolation in nonmoving parts of the picture, eliminate this degradation.

Motion-adaptive logic in the IDTV set switches from conventional line-comb filters and the use of adjacent-line interpolation—in image areas with motion—to interframe techniques for separation and interfield techniques for interpolation where no motion is detected. The motion-detection circuitry maps out the areas of the image that have motion on one of the system's seven field-buffer chips. Of the 4 bits it stores for each picture element, 2 bits are used for Y-C separation and 2 bits for line interpolation of the Y signal. This makes possible a stepwise change between in-field and interfield processing (for line interpolation) and between in-field and frame-level processing (for Y-C separation). Conventional digital TVs use line-comb filters to do Y-C separation, and NEC's IDTV system uses them too, in areas where motion is present. But it takes advantage of the way the NTSC signal was designed to vastly improve Y-C separation in nonmoving parts of the picture.

Like other digital TV systems, IDTV operates at a sampling frequency of four times the 3.58-MHz chrominance subcarrier, or 14.32 MHz, with a resolution of 8 bits. In a standard signal, the Y signal's components are at even multiples and the C signal's components at odd multiples of half the line frequency. The result is that C-signal components reverse in phase for each successive frame, while Y-signal phase remains the same. Because of digital frame storage, this situation can be exploited to obtain excellent Y-C separation of still portions of the picture. For both luminance and chrominance, the desired signal can be obtained and the undesired one canceled simply by digitally adding or subtracting signal values from successive frames.

Thus the IDTV set's Y-C separation circuit (see fig. 1) behaves as a line comb filter—and uses scan-line memories to do its job—in areas of the picture where there is motion. The interframe portion of this circuit is called a frame comb filter, and relies on four field-buffer chips.

**SIGNAL CONVERSION**

Access to data from the previous field is also crucial to the interpolation subsystem (see fig. 2) that converts a signal for 30-Hz interlaced scanning into a 60-Hz noninterlaced-scan signal, improving vertical resolution and eliminating interline flicker. This process involves writing twice as much image data on the screen per unit of time; that extra data is generated through interpolation.

In current TVs, 30 frames are displayed every second, and each frame consists of two interlaced 262.5-line fields. Each field scans every other line of the full frame. The viewer's eye and brain integrate the successive fields appearing on the screen, but the vertical resolution apparent to the viewer is only about 60% or 70% of the total number of lines appearing on the screen.

In the IDTV receiver, the incoming signal provides information for every other line on the screen every 1/60th of a second, and the chip set adds the missing lines so that an entire noninterlaced frame is written to the screen in that period, with no missing lines. Thanks to field-buffer storage, these missing lines of the Y signal are simply picked up from the previous field in a process called interfield line interpolation.

Interfield line interpolation doesn't work, how-

![2. INTERPOLATION](image-url)
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UPDATE: SMART-CARD CHIP RESPONSE IS UNEXPECTED

The response to Catalyst Semiconductor Inc.'s single-chip microcontroller for smart-card applications [Electronics, Dec. 18, 1986, p. 59] was surprising to president B. K. Marya. He wasn't taken aback by the hundreds of firms that wanted prototypes from the Santa Clara, Calif., company earlier this year. What he hadn't expected was the range of applications that designers had in mind.

"One of the most unusual uses is a debit coin to be used to eliminate pilferage from vending machines," he says. The debit coin, which works like a debit card, would make it unnecessary to store large amounts of change in vending machines.

Among other potential uses for the CAT61C580 are cards for terminal access, data security, product warranty, health status, telephone access and debit, and identification for passport applications. Right now, Marya says, seven customers are sampling the CAT61C580, with production planned for the first half of 1988.

In development, he says, is a second-generation, smart-card-oriented, 8-bit chip with 4 Kbytes of electrically erasable programmable read-only memory and twice the 3 Kbytes of ROM on the current chip. Also planned is a version with 64 Kbytes of EPROM and 16 Kbytes of ROM.

The CAT61C580 measures 4.5 mils by 5 mils by only 200 µm thick, making it small enough to meet the size requirements set by the International Organization for Standardization for smart-card applications. But it has 2 kbytes of on-chip EEPROM, which is about four times the density of any other ISO-compliant smart-card chip now available that uses the 2-µm CMOS design rules. About 30% smaller than competing devices, the chip, which is jointly designed and fabricated by Catalyst and Oki Electric Co., Tokyo, also contains 128 bytes of RAM besides the 3 kbytes of ROM.

During the fiscal year that ended in March 1987, Catalyst had sales of $4.5 million, mostly from a family of stand-alone EPROMs and EEPROMs. By the end of the current fiscal year, Marya estimates, company income will hit $9 million—and almost 40% of that will be due to sales of smart-card chips.

Bernard C. Cole

UPDATE: CAECO'S CUSTOM IC LAYOUT TOOL IS IMPROVED

When Caeco Inc. introduced its R-Cells VLSI Design System last year [Electronics, Dec. 18, 1986, p. 80], the software package was hailed as a promising development in the battle for automated layout of full-custom VLSI circuits. But even the company acknowledged that a future extension of the system was needed to allow for alteration of entire sections of a layout.

The company produced that extension about six months later. Called Automated Logic Synthesis, Caeco says it could be the solution to the bugaboo that has plagued vendors in the computer-aided engineering tool industry since that field was founded in the early 1980s—how to duplicate the silicon-efficient designs of handmade chips in the automated layout of complex VLSI chips. "Now, for the first time," says John Clairborne, executive vice president at the Santa Clara, Calif., company, "the layout designer can achieve automatic layout with hand-packed densities."

The new process, which was unveiled at the Design Automation Conference in June, improves the R-Cells in two ways. It ties the front-end schematic capture to the back-end polygonalayout function. And it provides automatic schematic back-annotation in the process. With the improvements, a designer can partition a section of the original schematic into a set of R-Cells. The automatic place and route tool then lays out the cells with as much attention to optimum placement as if a designer had laid out the cells by hand.

The innovations significantly increase a layout designer's efficiency. Clairborne says that a good layout designer could average around 10 transistors a day working by hand. "With our automatic layout product, the designer's productivity is increased tenfold."

Both the original R-Cells and the newer Automatic Logic Synthesis have been well received by Caeco's customers, the company says. Among them are Siemens AG, which will use the software tools in its own full-custom design system. Caeco has a contract to deliver more than 70 of its systems to the West German company in the coming year.

Jonah McLeod
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DARPA SHIFTS GEARS IN SMART WEAPONS PROGRAM...

The Defense Department’s quest to develop an autonomous aircraft with attack, surveillance, and survival capabilities is moving along—but the word is that plans are changing in favor of sensor technology. Phase two of the smart-weapons project is underway but neither the Defense Advanced Research Projects Agency, which is funding the program, nor any of the four principal contractors—Texas Instruments, GM/Hughes Electronics, Martin Marietta, and Northrop—is revealing much of anything. What is becoming clear, however, is that original plans for the 30-month second phase called for a heavy concentration on software development and the use of existing sensor technology. That’s changed, says a source close to the project. “More emphasis is now going to be placed on sensors,” he says. “If you don’t have sophisticated sensors to get raw information on your targets, you’re not going to have anything worth processing on your computers.” Darpa is playing its hand close to the vest on this one, says another source, adding that further disclosures aren’t expected until February.

...AS LORAL STUDIES AUTOMATED TARGET DETECTION

Loral Corp. is working on the kind of advanced detection technology that could eventually help future weapons automatically seek out and destroy enemy targets. For now, however, the Loral system is being designed for manned aircraft; it will aid in navigation and be capable of detecting even camouflaged targets. Current automatic-detection systems do not fare well in situations where target densities are low; false alarms are frequent. So Loral is looking at ways to improve resolution, classify target types, and filter false targets by quickly analyzing radar data. With funding from the Defense Advanced Research Projects Agency, Loral’s Defense Systems Division, in Litchfield, Ariz., is developing a millimeter-wave radar system that will operate in the 33.6-GHz frequency range and be capable of collecting ultra-high-resolution, fully polarimetric data. The airborne system will include both instant display and recording capability on high-density tape, which can later be processed on the ground for more detailed analysis.

HUGHES PUTS TOGETHER THE BIGGEST IR SENSOR ARRAY EVER

An airborne infrared sensor array with 38,400 individual detectors soon to be completed by GMHE/Hughes Aircraft Co. may be the most complex electro-optic array ever built. The array is part of a larger sensor subsystem that plays a key part in the Airborne Optical Adjunct Program, a component of the Defense Department’s Strategic Defense Initiative. That effort is trying to demonstrate whether airborne optical sensors can detect and track incoming intercontinental ballistic missiles. The first array has 15 modules, each with four sensor chip assemblies holding 640 IR detectors. It is designed to accommodate up to 44 modules. Data gathered by the detectors is processed first in an analog computer that runs 400 million analog-to-digital conversions/s, and then in a digital processor running at 15 billion operations/s.

FAA TAPS APOLLO FOR AIR TRAFFIC MANAGEMENT SYSTEM

Apollo Computer Inc. will supply work stations to the Department of Transportation for a new Air Traffic Management System that can display, on a single screen, every in-flight aircraft monitored by the Federal Aviation Administration. The DOT is buying 50 work stations for its Transportation System Center in Cambridge, Mass., ranging from Series 3000 personal work stations to high-resolution DN590 turbo three-dimensional-graphics systems. It will be linked with a similar FAA system in Washington to alert air traffic controllers to developing congestion.
SOLID STATE POWER CONTROLLER DEBUTS

Miniature Solid State Power Controllers Feature Short Circuit Protection & Status Feedback

Teledyne Solid State has announced plans to expand their existing solid state relay product line with the addition of SSR remote power controllers featuring true status feedback capability. The first of these new products is the M85C-2AS. This 2 amp unit is housed in a 14-pin hermetic DIP and is provided with integrated short circuit and current overload protection. It also features optical isolation, TTL interface and a discrete true status function to indicate that the output section is on and conducting current. This status feedback data can be utilized by the system in real-time operation or used to provide built-in test diagnostics for system maintenance.

10 Amp Controller Has Short Circuit Protection

Teledyne Solid State introduces the M33C, a high power military DC solid state relay power controller which provides short circuit protection whether switching into a dead short or shorting the unit while under load. In either case, the M33C senses the short circuit condition and initiates shutdown in less than five microseconds. The unit will block the short circuit condition until the short is removed and the unit reset by cycling the input control.

The M33C will also sense current overload conditions and prevent damage from thermal run-away due to excessive load current or ambient operating temperatures. Its integrated short circuit/current overload protection feature not only provides self-protection for the unit, but also allows the M33C to act as a remote circuit-breaker, preventing secondary system failures and providing extensive system benefits, including reduced maintenance and reduced life-cycle costs.

35 Amp Version of Popular 652 Power Solid State Relays Now Available

Teledyne Solid State Series 652 military AC solid state relays now offer a 35 amp version, as well as the popular MIL QPL 25 amp model. The new 35 amp unit provides all the features which have made the 652 a best-seller. These include optical isolation, zero voltage turn-on, logic compatible input current levels, and resistance to shock and vibration at military levels.

TO-5 Relay 25 Years Old–Still Growing

Developed by Teledyne in 1962, the Teledyne TO-5 electromechanical relay has become the industry standard as a versatile, miniature switching device for loads from dry circuit, and low level signals to 1 amp. During its 25 years of development, Teledyne has evolved it into a broad family of relays which include general purpose, sensitive, and magnetic latching types.

For More Information


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The world now has two new benchmarks from the leader in high-performance personal computing. The new 20-MHz COMPAQ DESKPRO 386/20 and the 20-lb., 20-MHz COMPAQ PORTABLE 386 deliver system performance that can rival minicomputers. Plus they introduce advanced capabilities without sacrificing compatibility with the software and hardware you already own.

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For more information worldwide, contact one of the Gates Regional Sales Offices listed below.
Vitesse Semiconductor Corp.'s new 1 Kbit static random-access memory is about twice as fast as the competition. It did it by surrounding gallium arsenide core cells with ECL-compatible input/output circuits to deliver 3-ns access times without having to redesign systems around an exotic technology.

The new 256-by-4-bit VS12G422E RAMs will tackle high-end ECL head-on in applications such as cache memories for supercomputers and minisupercomputers, display memory for graphics systems, and data memory for digital-signal processing.

And since the part offers the radiation hardness and wide temperature range typical of GaAs, it will also offer the military market speeds as yet unavailable. The VX12G422E comes in a 24-pin dual in-line package pin-compatible with industry standard 100422 RAMs.

STANDARD POWER. The Camarillo, Calif., company's very simple planar process—much like an n-MOS process—makes it possible to have GaAs cores with TTL or ECL I/O that use the same power sources as standard parts. The technology goes hand-in-hand with a commercialization strategy for its enhancement/deletion mode GaAs process that calls for fielding the most generic parts first [Electronics, Sept. 17, p. 48].

"Designers do not have to deal with an exotic technology because parts like the new 1-Kbit SRAM can replace existing RAMs to dramatically speed up systems," says president Lou Tomasetta. "We are directing these chips to customers who want to play down the fact that they are working in GaAs. "We would rather the customers think we have a proprietary advantage in GaAs technology—gives Maxim Integrated Products' 12-bit analog-to-digital converter the cost advantage of a mature technology. The design also opens the door to an industry-leading ADC."

The RAM's characterization will be complete by January with shipments set for the same month. Samples were available to selected customers in November.

The GaAs RAM's 4 to 5-ns speed over the -55°C to +125°C military range is relatively flat, especially when compared with ECL and CMOS RAMs, which tend to run only half as fast as their commercial spec when pushed into the military range. Memory chips faster than 10 ns for military applications have not existed until now.

Vitesse managed to develop the device in one month by leveraging design efforts on other parts, specifically by using the same core GaAs memory cells developed for the TTL-compatible RAM introduced in September. Designers also leveraged the ECL logic part from the previously designed parts compatible with Advanced Micro Devices Inc.'s 2001 family.

Considering the device's specifications and GaAs technology, price has been kept in check. This is largely because yields rival those of earlier parts—the very first wafers exceeded 25% yield. Vitesse quickly doubled its yield on the earlier TTL RAMs to over 50% and expects to repeat that with the ECL RAM since the basic cell design is the same. The price of the VS12G422E in 5,000 piece lots will be $70, with single units costing $190.

The new part has a lucrative market to exploit. Dataquest Inc. pegs the 1987 market for ECL RAMs in the U.S. at $156 million and projects the 1988 market to be $175 million. Most sales are in the commercial computer market because high speed ECL RAMs do not maintain their high speed across the military temperature range. The computer segment is expected to grow to $500 million by 1990, but Vitesse thinks the RAM's military applications will expand the total market for very high speed RAMs to much more than $500 million in 1990.

MAXIM TAKES ON ANALOG WITH FASTER 12-BIT ADC

A novel circuit design that allows Zener diodes to be buried in standard CMOS—instead of using complex biCMOS technology—gives Maxim Integrated Products' 12-bit analog-to-digital converter the cost advantage of a mature technology. The design also opens the door to an almost two-fold edge in speed compared to an industry-leading ADC.

The CMOS Max162 targets the market now dominated by the AD7572 from Analog Devices Inc., Norwood, Mass., and uses the same successive approximation process to achieve 12-bit resolution and linearity. But the 162 boasts a maximum conversion time of 3 μs running with a 4-MHz clock. The AD7572's best is 5 μs, says Brian Gillings, director of strategic planning and applications at Maxim's headquarters in Sunnyvale, Calif.

Maxim created a new Zener-diode design for a buried voltage reference. The advantages of fabricating in a mature MOS process instead of the emerging bi-MOS technologies accrue largely because biMOS has "as many as three to five more mask steps compared with standard CMOS," says Gillings. Buried Zeners
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boast lower drift and noise than do other common voltage reference devices.

Besides being easier to make, Maxim's design yields faster speeds for such applications as digital signal processing, high-performance industrial control, data acquisition, and electromechanical systems.

The Max162 includes a 12-bit digital-to-analog converter, successive approximation registers, 12-bit latch, multiplexer, clock oscillator, control logic, three-state output drivers, and on-board voltage reference.

**FRIENDLY.** The part works with most popular microprocessors. For example, it will run with an operating voltage of +5 and -15 volts, like the AD7572, but it also works with the -12V supplies common to analog systems that include microprocessors. Unlike other ADCs, it runs on a 4-MHz systems clock commonly found in many microprocessor-based systems.

The 24-pin part, which has a microprocessor interface, requires only external decoupling capacitors for power supplies and reference voltages. The 162's high speed—90-ns data-access time and 75-ns bus-release time—eliminates wait states. It dissipates 215 mW.

Available in production quantities in December, the 162 has three temperature grades with guaranteed maximum integral nonlinearity of ± 1 least significant bit, and ± 1/2 LSB over a temperature coefficient to 25 ppm/°C maximum.

XICOR UPS EEPROM DENSITY FOURFOLD

Xicor Inc.'s 16-Kbit CMOS serial electrically erasable, programmable read-only memory boosts the capacity of the company's low-cost nonvolatile memory offerings fourfold. But it retains pin-compatibility with lower density parts, so that designers can pack more memory into their systems without the costs associated with an extensive redesign.

Organized as eight pages of 256-by-8-bits, the 96-by-147 mil X24C16 is two-thirds the size of byte-wide EEPROMs. It is housed in an 8-pin dual-in-line package, compared with 24-pin DIPs for byte-wide 16-kbit parts.

The X24C16 uses a two-wire serial interface and software protocol for read and write operations. The serial protocol, which supports bidirectional data transfers, performs a 16-byte-page write in 5 ms.

The 2-µm EEPROM is targeted at a range of low-cost telecommunications, consumer, and battery-powered equipment, and works with 100-kHz microprocessors and controllers. The Milpitas, Calif. firm guarantees data retention for more than 100 years.

Typical active power dissipation of the X24C16 is 2 mA and standby current of 60 µA. A low-power version of the X24C16 for battery-powered systems will operate on 3 to 6 V instead of the 5-V, ± 10% supply for the standard part. Targeted applications include serial communications with modems, data retention features in telephone sets, battery-operated computers, consumer systems such as video and audio products, automotive control, and smart cards requiring space-saving serial ports.

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*For more information of complete product line see advertisement in the latest Electronics Buyers Guide

*Advertisers in Electronics International

† Advertisers in Electronics domestic edition
MANAGER.  
ADVANCED PROCESSOR TECHNIQUES

Develop New Computer Architectures

GE-Government Electronic Systems Division is a recognized leader in the field of computer technology, known for its contributions to VLSI, military computer architectures and DARPA programs. This exceptional professional challenge involves the development of advanced processor architectures for military applications--as well as the design of custom ICs to achieve their implementation. Responsibilities will extend to the coordination of development activities at various company locations and representing the company at appropriate engineering centers.

Qualifications include an MS or Ph.D. in Engineering, with demonstrated abilities in parallel processor computer systems and integrated circuit development. Also necessary is knowledge of VHIC, AVLIS; military computer architectures and DARPA programs are desirable.

The position carries a highly competitive salary and benefits package. Syracuse is notable for its low cost of living and is situated in beautiful lake country, with many cultural and recreational attractions.

For prompt response, please forward your resume, in confidence, to:

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U.S. Citizenship Required

Minorities, females, handicapped and Vietnam Era Veterans encouraged to apply.

No agencies please.

Micro Crystal high quality miniature quartz crystals for surface mounting are tailored to advanced microelectronics requirements.

- Mountable by vapor phase or infrared solder refow, or wave soldering at 260°C for 20 sec.
- Available in 16 mm tape, double pitch, on standard 7" reel (up to 1k pieces per reel).
- Frequency range from 10 kHz to 4 MHz and 8 MHz to 24 MHz.

For more information, contact Micro Crystal, Div. of ETA Industries, Inc., 35 East 21st St., New York, NY 10010. Circle 151 on reader service card.
If the card below has already been used, you may obtain the needed information by writing directly to the manufacturer, or by sending your name and address, plus the Reader Service card number and issue date, to Electronics Reader Service Management Dept., P.O. Box 504, Dalton, MA 01227.
dc to 3GHz

- less than 1dB insertion loss over entire passband
- greater than 40dB stopband rejection
- 5 section, 30dB per octave roll-off
- VSWR less than 1.7 (typ)
- over 100 models, immediate delivery
- meets MIL-STD-202
- rugged hermetically sealed package (0.4 x 0.8 x 0.4 in.)
- BNC, Type N, SMA available

**LOW PASS**

<table>
<thead>
<tr>
<th>Model</th>
<th>LP-10.7</th>
<th>LP-21.4</th>
<th>LP-30</th>
<th>LP-50</th>
<th>LP-70</th>
<th>LP-100</th>
<th>LP-150</th>
<th>LP-200</th>
<th>LP-300</th>
<th>LP-450</th>
<th>LP-550</th>
<th>LP-600</th>
<th>LP-750</th>
<th>LP-850</th>
<th>LP-1000</th>
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<tbody>
<tr>
<td>Min. Pass Band (MHz)</td>
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<td>22</td>
<td>32</td>
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<td>60</td>
<td>98</td>
<td>140</td>
<td>190</td>
<td>270</td>
<td>400</td>
<td>520</td>
<td>580</td>
<td>700</td>
<td>780</td>
<td>900</td>
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<tr>
<td>Max, 20dB Stop Frequency (MHz)</td>
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<td>32</td>
<td>47</td>
<td>70</td>
<td>90</td>
<td>147</td>
<td>210</td>
<td>290</td>
<td>410</td>
<td>580</td>
<td>750</td>
<td>840</td>
<td>1000</td>
<td>1100</td>
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Prices (ea.): P $9.95 (6-49), B $24.95 (1-49), N $27.95 (1-49), S $26.95 (1-49)

**HIGH PASS**

<table>
<thead>
<tr>
<th>Model</th>
<th>HP-50</th>
<th>HP-100</th>
<th>HP-150</th>
<th>HP-200</th>
<th>HP-250</th>
<th>HP-300</th>
<th>HP-400</th>
<th>HP-500</th>
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<th>HP-700</th>
<th>HP-800</th>
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<td>500</td>
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<td>460</td>
<td>520</td>
<td>570</td>
<td>660</td>
<td>720</td>
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</table>

Prices (ea.): P $12.95 (6-49), B $27.95 (1-49), N $30.95 (1-49), S $29.95 (1-49)

*Prefix P for pins, B for BNC, N for Type N, S for SMA example: PLP-10.7

Circle 901 on reader service card

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**Finding new ways...**

**Setting higher standards**