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Electronics®

HDTV: CAN THE U.S. GET ITS ACT TOGETHER?

NEXT-GENERATION TELEVISION

PAGE 70

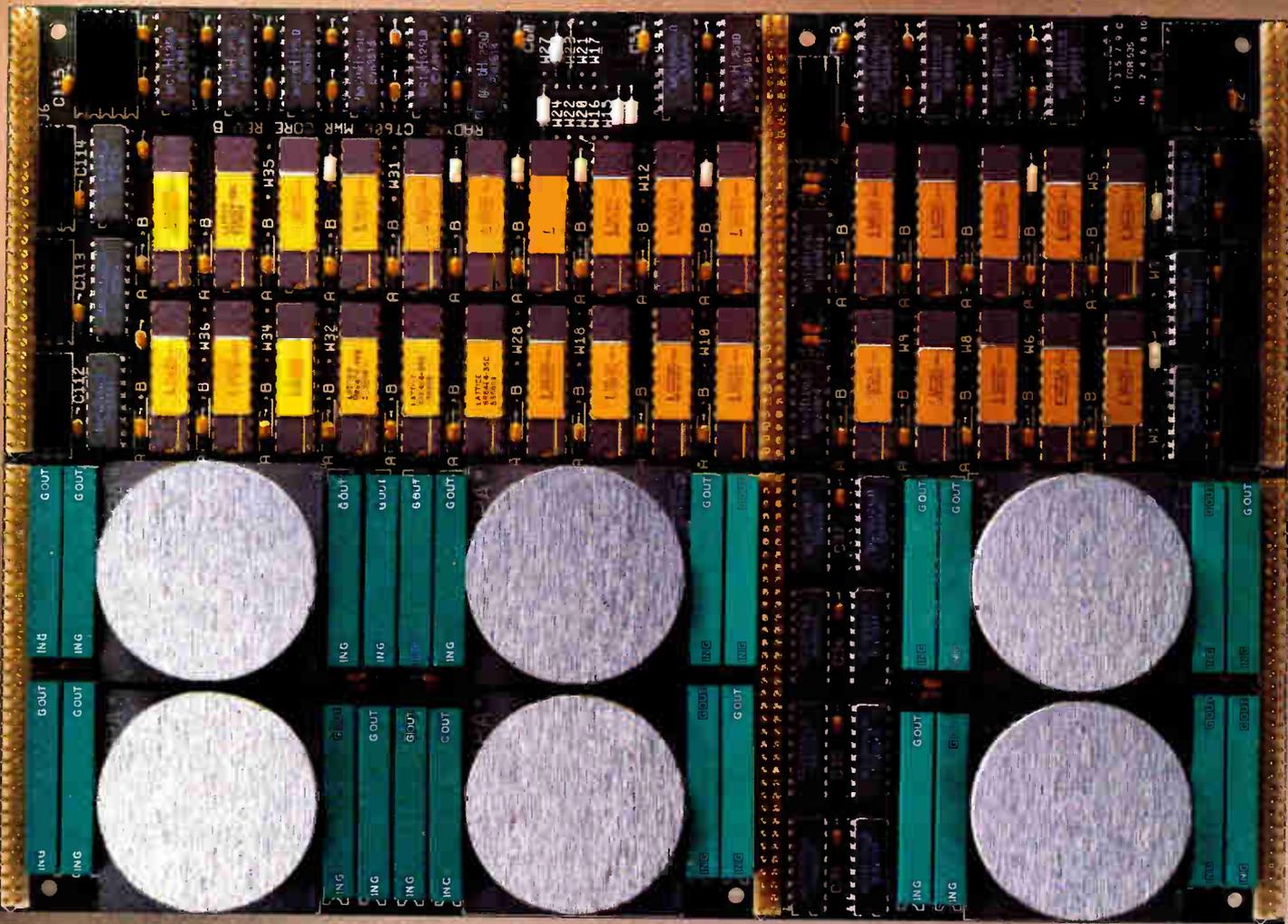


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**FACTIONS IN INDUSTRY
PULL MANY DIFFERENT WAYS
EVEN AS AGREEMENT GROWS ON THE
CRITICAL IMPORTANCE OF HDTV TECHNOLOGY**

***** 3-DIGIT 672

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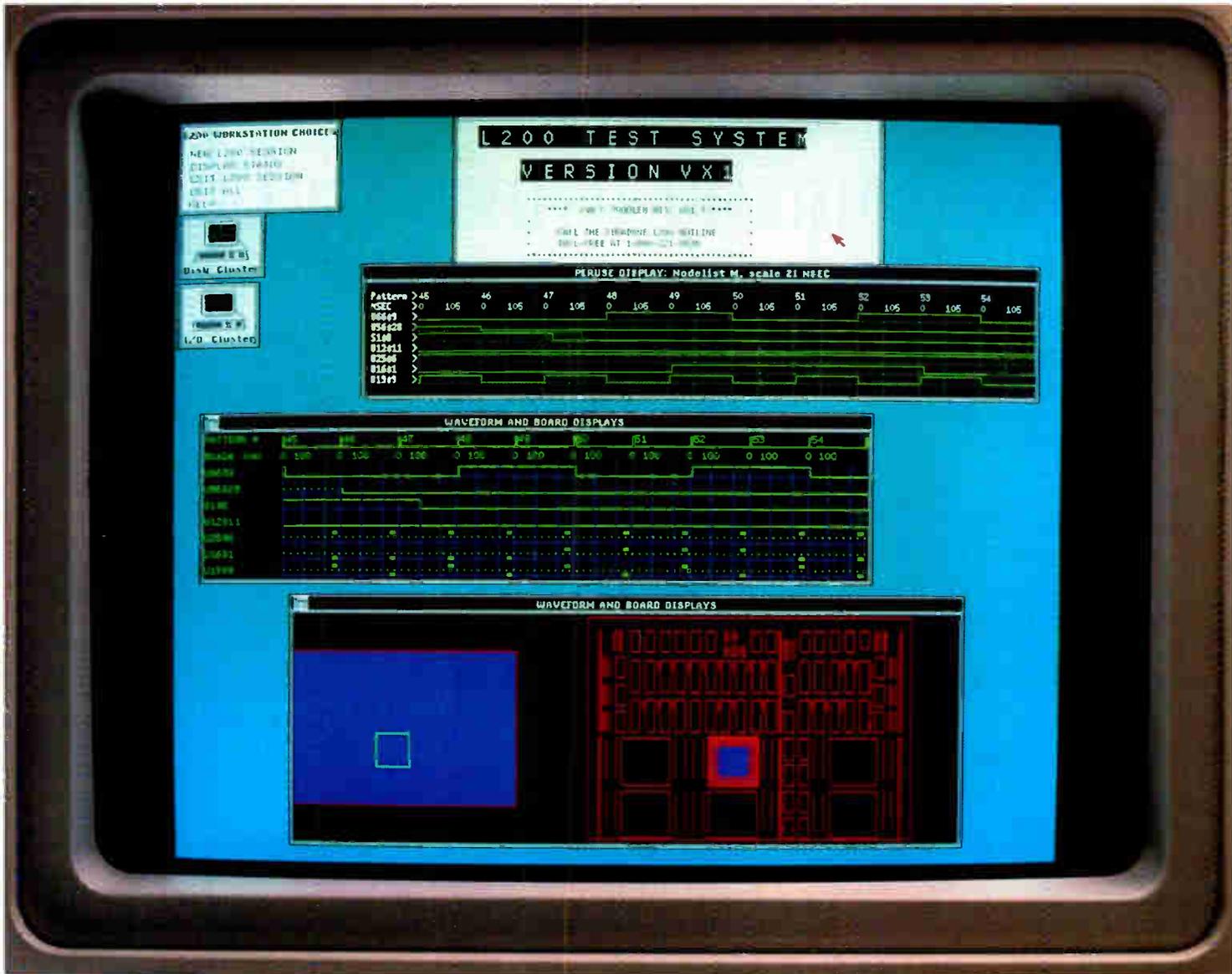
Start with the most advanced hardware for analog and digital testing. An L200 fires functional test patterns at 40 MHz rates. At up to 1152 test channels. Top speed is 80 MHz. That's 4 to 8 times faster than any competitor can deliver.

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Telecommunications Industry Update

A REPORT FROM THE NETHERLANDS FOREIGN INVESTMENT AGENCY

In 1989, the Netherlands will be one of the first European countries to substantially open up its telecommunications equipment and services market—a response to deregulation and market conditions, globalization, and telematics progress. The Dutch telecommunications equipment market is projected to reach nearly \$800 million by 1990, while the European-wide market for equipment and services could exceed \$50 billion.

Holland has ensured that its infrastructure—including PTT Nederland which will become a private company January 1 without regulatory responsibilities—will be able to handle not only today's basic speech, text and data exchanges, but tomorrow's needs for fast total digitalization, mobile and other new value-added services.

Here are some examples of Dutch developments in advanced telecommunications services that will be available to consumers, industry and governments.

✂ **ISDN Picture Phone**—Since 1983, the Dutch have been helping to define the operational standards, compatible with both CCITT and CEPT, for a worldwide small band ISDN videophone terminal. This international effort is being coordinated by the PTT Dr. Neher Laboratories and foresees low-priced picture phones for office and home use in 1992. High-quality mov-



ing pictures accompanied by high-quality voice are transmitted over a 64kbit/second network. The bit rate is achieved by data compression techniques that eliminate redundant information using a hybrid method combining DPCM- and transform-coding. Encryption will ensure privacy. To enhance a possible videophone service, high quality videotext images can be transmitted with the same equipment.

✂ **Teleports**—Designed jointly by Rotterdam's municipal authorities and its business community, the teleport uses the International Transport Information System (INTIS) for the electronic exchange of standardized messages between shippers and suppliers of all modes of transportation. Shippers and freight forwarders already access the network to send shipping instructions to deep-sea carriers and liner agents. They, in turn, communicate electronically with container terminals. Both PCs and mainframes, equipped with a 3780 emulator and a V22bis modem, can access the

network. Access by X.25 protocol will be available soon. Amsterdam is also developing a teleport.

✂ **Transportation Databases**—A standard IBM SNA system with videotext is providing more than 1,500 subscribers throughout Europe with cost savings and real-time information about space availability, type of cargo handled, destinations, departure and arrival times for trucks, trains, ships and airplanes throughout Holland. Called Transpotel, this Dutch database service has expanded through franchising to the United Kingdom, Switzerland, Belgium, Austria, France, Germany and Scandinavia, and soon will extend to Italy and Denmark.

In addition, Holland is a major manufacturing location not only for N.V. Philips's data communications products, but also for Alcatel, N.V., which builds and markets its System 12 for small and medium-sized firms; for Swedish multinational L.M. Ericsson, which manufactures telephones for the Dutch PTT and other telecommunications equipment; for West German multinational Siemens, which produces data communications products; and for the AT&T/ Philips joint venture, which is building a new generation PBX.

Further, three technology universities—at Delft, Twente and Eindhoven—and more than 100 technical institutes along with the Netherlands Organization for Applied Scientific Research (TNO) and major software houses assist companies, regardless of location, with research and development from defining systems needs to designing networks to building prototypes or writing code.

Netherlands Foreign Investment Agency

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BENNY AND THE NETS

By the time America turns on HDTV, will we find anything more than a new format for old jokes?

Some weeks ago, when we were talking about putting a cover on this issue based on our high-definition TV package (p. 70), I had an idea for a visual that—and this is almost certainly a good thing—I discarded immediately prior to initial verbalization. It has stayed with me, however, and now I just have to tell somebody. If you really want to get across what HDTV is going to mean, you see, here's what you do: you merely take a TV screen shot of the consummate British middlebrow comic, Benny Hill, holding his hands out in front of him about 24 inches apart. His eyes bug out. His tongue tries to escape out of one side of his mouth, then the other. He clenches his teeth to get control of it, then begins to repeat, ad infinitum: "It's big! It's big! It's . . . BIG!"

How big—apologies to Ed McMahon—is it? William Schreiber, who heads the MIT Media Lab's Advanced Television Research Program, believes public acceptance could make HDTV the "largest consumer of [both] memory chips and microprocessors." That means bigger than the computer industry. That means bigger than industrial electronics. What's more, the ultimate effect of the worldwide market for HDTV as a technology driver for everything from advanced semiconductors to high-resolution displays can only be projected at this point in terms of incalculable significance. Some visionaries see an inevitable merger of the home-entertainment center with the home computer, creating the 21st century equivalent of the home altar.

What will be a massive ripple effect is already in motion. Read how North American Philips is using an enhanced multiplexed analog-component technology scheme to "stitch together" an NTSC-sized picture with image-widening side panels (p. 78). Read why Zenith believes its process for directly printing color phosphors onto a faceplate will carry cathode-ray-tube technology well into the HDTV revolution no matter what flat-panel developments ensue (p. 79).

Despite all these encouraging signs, we are handing you plenty of downside in the picture. The U. S. has advanced to nowhere near adopting an HDTV standard, and isn't likely to advance in the near future. There are not even rumors of any kind of coherent policy among the industry factions who stand to lose the most—or everything—from lack of one. It's particularly discouraging because no matter who builds the new TV sets we will all eventually buy, or where they are assembled, until the U. S. gets its act together nothing is going to move very far or very fast.

And notice how, at a time when TV technology is approaching a major threshold, the combined product of the U. S. broadcast networks is playing to an increasingly indifferent audience—indifferent to the point of serious commercial impact. One hopes HDTV is not born into a world that couldn't care less. Personally, I can't wait to see Benny Hill reruns on that big screen.

ROBIN NELSON

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A united state.

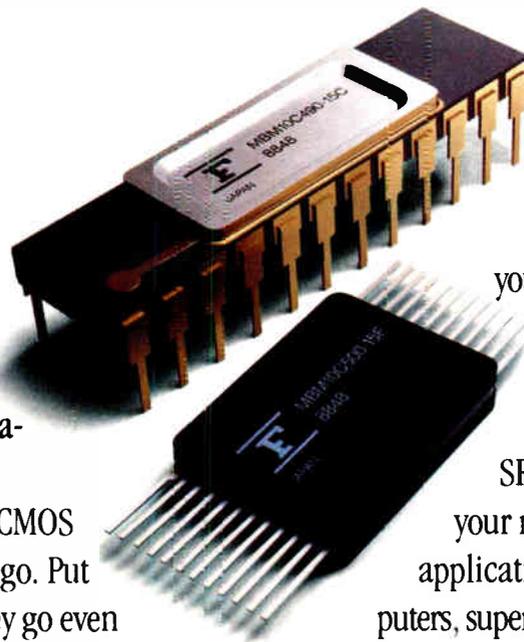
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LETTER FROM RESEARCH TRIANGLE PARK

RESEARCH TRIANGLE PARK, AT 30, REACHES MATURITY

RALEIGH, N. C.

Flying into Raleigh-Durham International Airport, one gets the idea that this central North Carolina community remains a rural haven. The landscape's dominant feature is a seemingly endless grove of lodge-pole pines, and development seems modest at best. But hidden in the piney woods, in the hollow between these two small Southern cities, may well be the most successful planned industrial center in the U. S.

This is Research Triangle Park. Planned 30 years ago by the state as an advanced-research community that could draw and expand on the strengths of the area's three major universities, it has led a remarkable renaissance in the region. Together, the 6,700-acre park and three universities—North Carolina State in Raleigh, the University of North Carolina at Chapel Hill, and Duke University in Durham—have attracted major corporations with a highly educated work force, world-class research support, and one of the nation's lowest unemployment rates.

What's more, unlike such high-tech centers as Silicon Valley or Boston's Route 128 corridor, which harbor computer and electronics companies to the virtual exclusion of anything else, Research Triangle Park prides itself on its diversity. Computer companies sit across the road from mammoth chemical concerns, while U. S. government laboratories, such as those belonging to the Environmental Protection Agency and the Department of Health and Human Services,

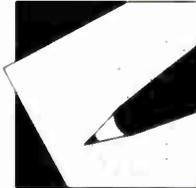
are neighbors to producers of fiber-optic cable.

The result is unparalleled economic stability, effectively insulating the community from the kinds of cyclical, domino-effect layoffs that are common in Silicon Valley. A slump in, say,

the personal-computer industry would hardly ruffle a feather here. "It's extremely important that the park is multidisciplinary," says Robert G. Hirsch, director of the DuPont Co. Electronics Technologies Laboratory, a relative late-comer that arrived in 1985. "When the electronics industry was down in the dumps two years ago, the unemployment rate 'rocketed' to somewhere below 3%." And it hasn't risen since. In fact, says Hirsch, the industrial mix was a prime reason DuPont decided to locate its newest facility—a multidisciplinary electronics lab—in the triangle.

But diversification has also served to give RTP something of a staid image: a place through which corporate giants like IBM, Northern Telecom, and DuPont rotate their managers every few years. Strict limitations on land development—companies can build on no more than 15% of any plot of land in the park's northern sector, and on up to 30% in the southern tier—were designed to attract the deep-pocketed corporate elite. The result: the many small and midsize companies that have sprung up in other high-tech hubs never materialized, and, says one Durham investor, "the triangle area got a bad rap in the investment community."

But times are changing, says Dennis



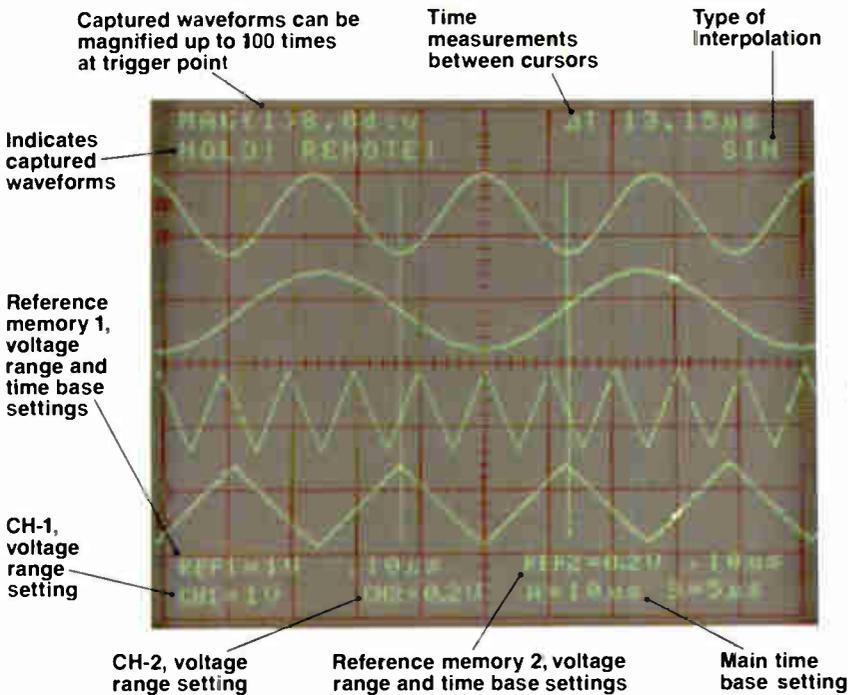
WHO'S WHO IN THE PARK

Company	First year in park	Work force
IBM Corp.	1966	10,000
Northern Telecom Inc.		
Integrated Network Systems Group	1980	7,500
Research Triangle Institute	1959	1,400
BNR Ltd. (Bell-Northern Research)	1987	700
Mitsubishi Semiconductor *	1983	380
General Electric Co.		
Microelectronics Center	1985	350
Data General Corp.		
RTP Laboratory	1977	300
Sumitomo Electric Industries	1983	300
Dupont Co.		
Electronics Division	1985	230
Microelectronics Center of North Carolina	1980	150
GTE Corp.		
Government Systems	1983	75

* LOCATED NEAR PARK

SOURCES: RESEARCH TRIANGLE FOUNDATION, ELECTRONICS

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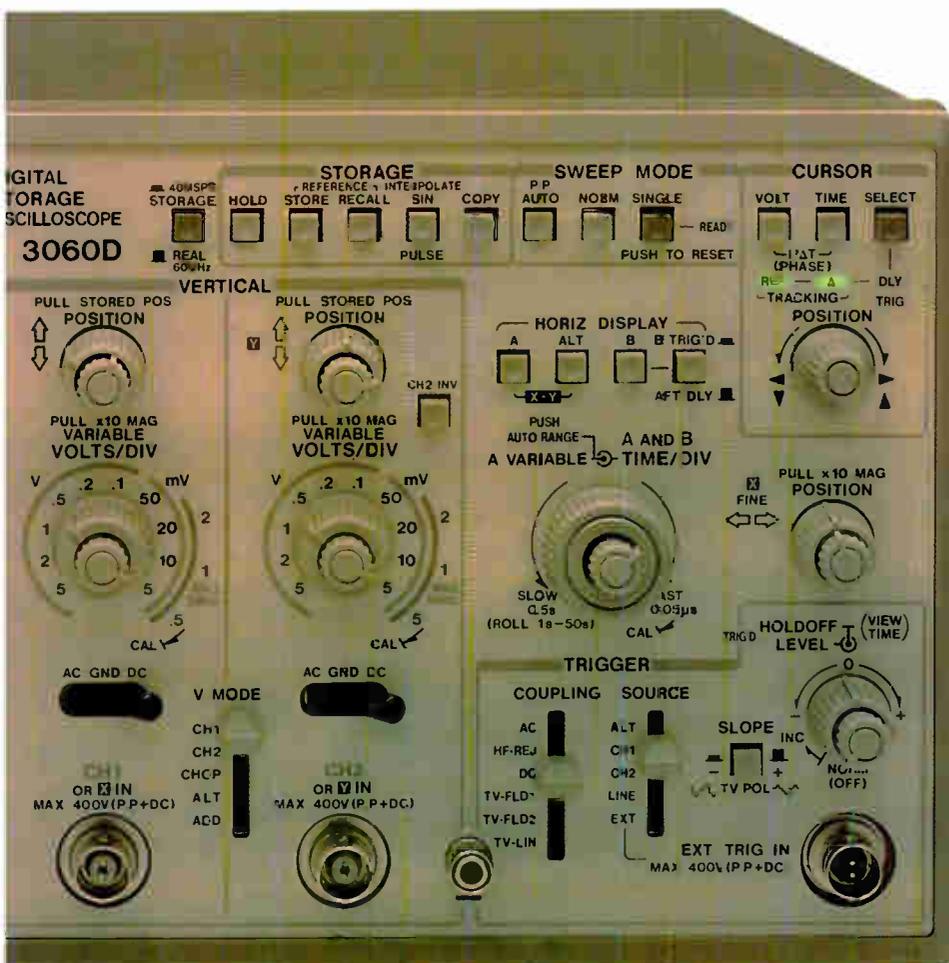
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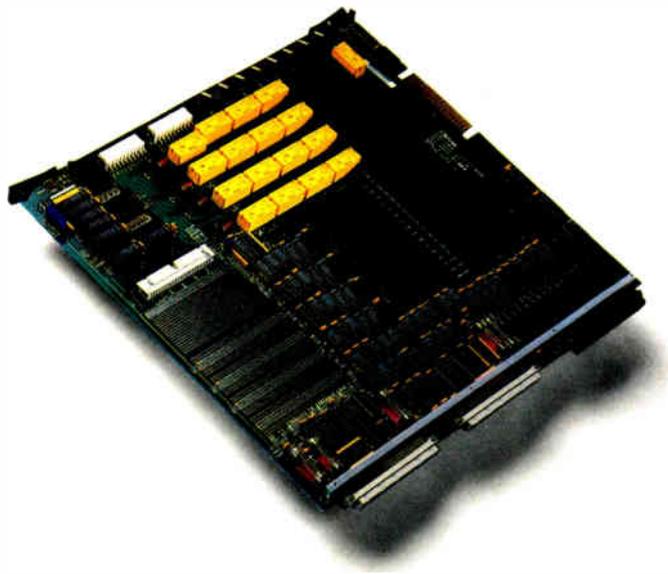


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The 8000 is the only combinational tester with 2,048 fully-hybrid, non-multiplexed test points. Each node has a driver/receiver behind it; each can be used for either functional or in-circuit testing. All of which helps reduce the





cost of programming and implementing engineering changes.

The 8000's digital test subsystem truly warrants the term "high performance," with 10 MHz pattern rate, 8Kx4 RAM per node, programmable slew rates and 10ns programmable edge placement.

The menu-based, mouse-driven interface simplifies programming, with multiple windowing capability,

integrated logic analyzer and graphic quality analysis tools.

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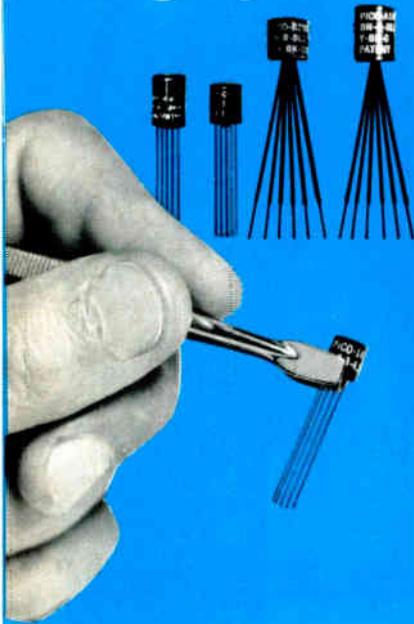


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Daugherty, a general partner in Intersouth Partners, an RTP-based venture-capital company. He says all the ingredients for "soup," his euphemism for a strong entrepreneurial environment, have come together in the last few years. Today, there are at least 30 venture-capital companies from all over the country investing in RTP-area companies, he says, and there is a core of more than 40 high-technology venture-backed companies getting started somewhere in the triangle. Last year the Raleigh Chamber of Commerce and N. C. State combined to set up a new incubator facility called Bitech, for Business Innovation and Technology Center, which will help entrepreneurs draw up business plans, find financing, and get state and federal grants.

That's a marked difference from just a few years ago. Daugherty says he had to struggle to raise Intersouth's first venture fund in 1984. He spent more than a year trying to gather \$10 million and finally gave up at the \$6.5 million mark. "Raising money then for ventures in North Carolina was nearly impossible," he says. Last year, however, he raised \$20 million in less than 12 months—and he did it in the wake of the stock-market crash. Why the change? "We've eliminated a lot of the unknowns," he says.

In the meantime, though, entrepreneurs seeking money for their dreams found themselves moving out to Silicon Valley and north to Boston, where costs were greater, but money was available. Daugherty says several potential local businesses were swept away by outside investors, who insisted that the new companies be set up closer to the bank.

"We got a lot of interest from West Coast firms—more than from the East Coast," says C. Eric Hunter, the 29-year-old president of specialty-chip-maker Cree Research Inc. "One firm, in fact, was very interested—but they wanted us to move out to Santa Clara." Just one year old, Cree is concentrating on converting silicon carbide, an advanced semiconductor material, from a high-temperature curiosity at an N. C. State lab into a commercially viable technology for applications in space, aircraft engines, and other hostile environments. The school has granted Cree exclusive licenses to its patents on the technology and has a financial stake in the company.

But this is still not Silicon Valley. "There's a maturity level there that we're only now starting to reach here," says F. Thomas Wooten, vice president for electronics and systems research at the Research Triangle Institute. The institute, a contract-research facility established with the rest of the park in 1959, reflects

the park's tenants in its technological diversity, with projects in chemistry, pharmacology, and the biological sciences in addition to advanced software, semiconductor, and systems work.

SELLING POINT. Although it was established as an additional lure to attract outside companies to the area, the institute is not limited to working for area firms alone. It derives much of its revenue from government contracts. But like the universities and the nearby Microelectronics Center of North Carolina, a state-supported research consortium, it is one of the park's selling points.

Area executives extoll the virtues of having such world-class research facilities so close at hand. DuPont's Hirsch, for example, says his people regularly use equipment at MCNC that they would not have access to elsewhere. And Richard B. Fair, the center's vice president for design research and technology, says the facility

was a major reason Northern Telecom Ltd. chose to locate its \$50 million, 700-person BNR laboratory here in 1987.

MCNC, too, in many ways reflects the park's diversity, with member

companies such as DuPont, IBM Corp., and Aircor (a maker of gases used in semiconductor processing) representing only a portion of its broad membership. It is a research facility with a \$30 million annual budget that has so far managed to escape the wide notice of the press—and, Fair notes, of Silicon Valley chip makers. With a world-class clean room capable of handling submicron devices, the center produced the working parts of its Massively Parallel Processor, a 1.1-million-transistor chip featuring 128 eight-bit processors with 1 Kbit of memory each.

Now MCNC is expanding its charter and entering the world of supercomputing and high-speed networking. With \$16 million in state funding, the center is building a supercomputer center featuring a Cray Research Inc. Y-MP supercomputer that will be "the most powerful machine in the Southeast," Fair says. It's also setting up a state-wide computer network joining all of the state's colleges and universities with high-speed microwave links. Initial connections will permit 8-Mbit/s communications, but Fair says the system will eventually be able to support speeds up to 45 Mbits/s. As with MCNC's other activities, member companies are also expected to use the facility.

Fair, who doubles as a professor at Duke, says he's seen traffic increase and other things change in his few years in North Carolina. He remains profoundly impressed with the state's progressive attitude toward technology and investment. "Just look," he says, "what they've built in the piney woods."
—Tobias Naeye

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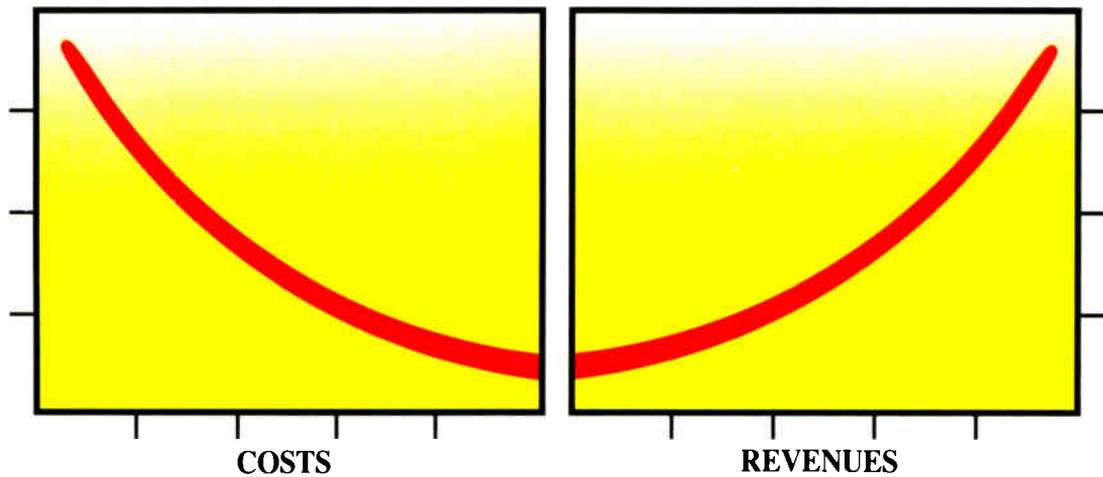


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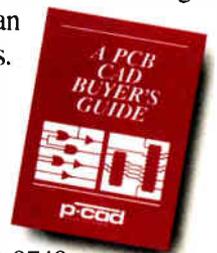
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Circle 39

ELECTRONICS NEWSLETTER

DATA GENERAL FIRES THE FIRST VOLLEY IN ITS RISC CAMPAIGN . . .

The first Data General Corp. systems based on reduced-instruction-set computing are hitting the market—four work stations and a server, all built around Motorola Inc.'s 88000 CMOS microprocessor. The RISC-based platforms run the Unix operating system, marking the Westboro, Mass., computer maker's first departure from its proprietary MV/Eclipse family. The initial RISC units run DG/UX, Data General's variation of Unix, which incorporates a new kernel designed to support symmetric multiprocessing. The firm says the entry-level unit, a diskless model with a 20-in. monochrome display and 4 Mbytes of memory, is priced "well below \$10,000," which positions it against low-end, mostly PC-based work stations. But look for more sophisticated versions to start showing up as Data General moves against its arch-rival, Digital Equipment Corp., into the work-station market. Data General's advantage is that it can price aggressively because it has no installed base to protect. □

. . . BUT SANYO/ICON BEATS IT TO MARKET WITH AN 88000-BASED SYSTEM

Data General barely lost the race to send the first commercial computer using the Motorola Inc. 88000 RISC chip to market—Sanyo/Icon International Inc. got there first. The Orem, Utah, company unveiled its Model 8000 late last month, a week before Data General's announcement. The three-processor Sanyo/Icon system boasts a single-central-processor speed of about 15 million instructions/s and a double-precision whetstone rating of 6.75 million. Prices start at \$155,000. The most likely competitors include DEC's midrange VAX units, plus Pyramid and Sequent computers. □

IEEE JOINS THE CALL FOR GOVERNMENT-BACKED CONSORTIA

Adding its voice to the American Electronics Association and other industry groups, a study group assembled by the Institute of Electrical and Electronics Engineers is calling for not just one, but several government-aided research and manufacturing consortia. These public/private joint ventures would address both research and development and full-scale manufacturing in two "crucial" areas: dynamic random-access memories and high-resolution systems. "You simply can't do R&D and then stop," says Alan McAdams, associate professor of managerial economics at Cornell University's Johnson Graduate School of Management and the chairman of the study group. "You've got to integrate manufacturing." He says that Sematech, a consortium working to produce advanced manufacturing know-how for the semiconductor industry, is "in no way a solution to the U. S. semiconductor manufacturing problem," but merely a "highly desirable first step." He thinks the government should quickly put in place economic incentives that will attract domestic firms back into the commodity-chip business, or risk losing its stake in supercomputing and other leading-edge technologies. □

HEAD SHRINKING ISN'T THE ONLY WAY TO MAKE A DISK DRIVE SMALLER

One way to make smaller disk drives is to shrink the head. Imprimis Technology Inc., a Minneapolis disk-drive maker, has come up with another: reduce the size of the sliders for the head mechanism, rather than the magnetic element itself. The sliders in the company's 70 Series thin-film head assemblies are about two-thirds smaller than those in today's thin-film-head drives. That means they'll help deliver faster access times and higher drive densities, thanks to lower restrictions on head flying height and less stacking space for multiple heads and disks. Imprimis has been providing samples of the new head assemblies to drive makers since late last year. Some 100,000 units should be produced in 1989 starting around midyear. □

ELECTRONICS NEWSLETTER

STANDARDS ARE COMING THAT WILL MAKE PICKING MACHINE-VISION SYSTEMS EASIER

Choosing the right machine-vision system for jobs like printed-circuit-board inspection is about to get easier. The Automated Vision Association plans to offer by midyear a relatively inexpensive software package and a set of "multipoint targets" needed for the first in a series of vision-performance-test standards developed by the Ann Arbor, Mich., trade group. The American National Standards Institute approved the initial test document late last year. It provides a standard way for users and vendors to evaluate a vision system's accuracy and speed in locating and measuring circles, squares, or other markings on a two-dimensional target. Test-control software to run on an IBM Corp. personal computer, as well as standard eight-point targets, should both be available by June. A document covering one-dimensional vision performance tests could be ready by the end of the year, says Leonard H. Bieman, chairman of the association's standards subcommittee. Proposed standards defining a comprehensive methodology for acceptance testing of machine-vision systems could go to ANSI early next year, he adds. □

BREAKER, BREAKER—TRUCKERS CAN TEN-FOUR BY SATELLITE, GOOD BUDDY

Truckers will soon have a new communications tool at their fingertips, one that's far more sophisticated than a Citizen's Band radio. Tiny satellite antennas 6 in. in diameter, mounted atop trucks, let trucking companies track, locate, and communicate with their drivers, without ever making them stop their rigs to get to a pay phone. The system comes from Geostar, a Washington satellite-communications company that has offered one-way communications between truckers and their dispatchers for over a year. The new system, called Satellite System 2C, lets truckers both send data to and get it from their dispatcher's office. So far, truckers can send messages in data form only—they type in emergency messages or send preset responses using a keypad. But Geostar is working on a system with voice recognition, which would allow drivers to send messages by speech. Trucking companies can use the system to keep better track of their trucks and trailers, Geostar executives say, at a cost of only a nickel for each transmission. The system is also attracting the interest of the Defense Department—it could keep track of hazardous waste and other sensitive materials as they're transported across the country. □

MAKERS OF COLLISION-AVOIDANCE SYSTEMS HUSTLE TO SIGN UP AIRLINES

Competition is heating up in the market for aircraft-collision-avoidance equipment after a mid-January ruling by the Federal Aviation Administration. The ruling requires that all commercial aircraft flying in U. S. airspace and capable of carrying more than 30 passengers be equipped with TCAS II (Traffic Alert and Collision Avoidance) systems by the end of 1991. Depending on whose numbers are used, that amounts to 3,500 to 6,000 jetliners which must be outfitted within the next three years. TCAS II suppliers are scrambling to nail down contracts with the big airlines, leading to frantic discounting and deal-making for the systems, which usually carry a single-unit price ranging from \$90,000 to \$130,000. In the lead so far is Bendix King Air Transport Avionics, a Fort Lauderdale, Fla., division of Allied Signal Aerospace Co. As of mid-February, Bendix had announced TCAS II contracts from American, Piedmont, and Southwest airlines, for a total of about 1,200 planes. Honeywell Inc.'s Air Transport Systems Division in Phoenix has also signed up three carriers—Alaska, Northwest, and Qantas airlines—for a total of about 580 planes. By contrast, the third major player in the TCAS II market—Rockwell International's Collins Air Transport Division in Cedar Rapids, Iowa—had yet to announce a production order by mid-February. □



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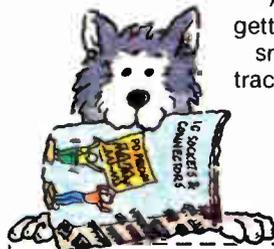
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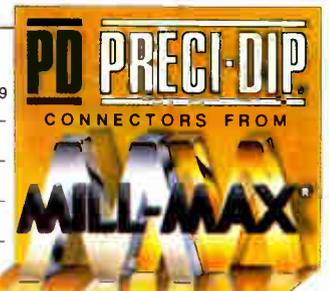
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PRODUCTS TO WATCH

TI'S 1-MBIT EPROM DELIVERS 20-NS STATISTICAL ACCESS TIMES

Forget high-speed cache memories and wait states as the only solutions to the problem of microprocessors outrunning the memories that store their code. The 20-ns average access time of Texas Instruments Inc.'s 1-Mbit erasable programmable read-only memory is fast enough to handle the job, and TI's BurstMode EPROM does it with clever circuitry—not new technology. Key elements include a standard 1-Mbit, 1.4- μ m CMOS array and a 256-bit line buffer that acts as an on-chip cache, loading sequential data from the 1-Mbit array before the microprocessor needs it. Hit rates—the probability that the right data is stored in the line buffer—are about 90%. Other circuitry handles recoveries after misses, which means a 70-ns access time. Unveiled at last month's International Solid State Circuits Conference in New York, the Burst-Mode EPROM will be available by the end of 1989. □

ENCORE'S SUPERMINIS PUSH THE COST OF PROCESSING DOWN TO \$3,500 PER MIPS

The Multimax 500 family of Unix-based parallel-processing superminicomputers from Encore Computer Corp. of Marlborough, Mass., represents one of the first applications of National Semiconductor Corp.'s 30-MHz NS 32532 central-processing unit. Encore's symmetric multiprocessors incorporate a CPU board that features two 532s, each of which executes 8.5 million instructions/s or 17 mips per board. As many as 10 boards can be linked—at less than \$3,500 per mips—to apply 170 mips to both technical and commercial applications, ranging from software development and simulation to database management and on-line transaction processing. Available in July, a minimal 17-mips Multimax 510 system will sell for \$159,000. A similarly priced Digital Equipment Corp. VAX 6300 delivers about 5 mips. Besides the VAX line, Encore says the Multimax 500 family will also compete favorably with Prime Computer's 6550 and Data General Corp.'s MV/40000 lines. □

STAC IMPLEMENTS ITS 2:1 DATA-COMPRESSION ALGORITHM IN HARDWARE

Makers of disk and tape drives who use data compression to effectively double the capacity of their memory products can now offer high performance as well with STAC's single-chip processor. The 9703 implements the company's 2:1 data-compression algorithm and gives at least a thirtyfold boost in the data-transfer rate, compared to software implementations. It gobbles up incoming data at 500 Kbytes/s and puts its compressed output on tape or disk at 250 Kbytes/s. Simulations by the Pasadena, Calif., company show the hardware implementation running more than 30 times faster than an Intel Corp. 80386 processor running the software package. Available next quarter, the chip, intended for QIC-type tape drives, will sell for about \$50. □

NEC'S V80 DELIVERS 17-MIPS PEAK PERFORMANCE

Running at 33 MHz, NEC Corp.'s top-of-the-line V80 32-bit CISC microprocessor delivers a peak performance of 16.5 million instructions/s—2.5 times the performance of NEC's V70 and five times the 16-bit V60. In benchmark tests using the Gibson mix, the V80 delivers 13.1 mips. The chip, which also comes in a 25-MHz version, gets its speed from a seven-stage pipeline architecture and by integrating 1 Kbyte of cache memory for instructions and 1 Kbyte for data. Other architectural features include branch prediction and virtual memory management. Address- and data-bus error detection are provided for nonstop multiprocessor designs. Fabricated in 0.8- μ m two-aluminum-layer technology, the 930,000-transistor circuit fits on a 14.49-by-15.47-mm chip. Sample prices are about \$960 for the 25-MHz version and about \$1,200 for the 33-MHz chip; look for a 45-MHz, 22.5-mips version in 1990. □

PRODUCTS TO WATCH

TOSHIBA'S 4-MBIT EPROM BOASTS 150-ns ACCESS TIMES

Toshiba Ltd.'s 4-Mbit erasable programmable read-only memory sports a fast access time of 150 ns. This comes thanks to polycide-processing technology and an architecture that splits the memory core into four sections to reduce the length of the bit lines each sense amplifier drives. The polycide processing used in the 0.8- μ m fine-pattern technology reduces resistance to about one-tenth that of polysilicon lines, which drops the resistance-capacitance time constant. The short gate length and thin gate oxide deliver a 0.05-ns write-pulse width, enabling the entire 4 Mbits to be written in 60 s. Configured as 512 K by 8 bits, the devices are fabricated with n-MOS memory cells and CMOS peripheral circuits on a 5.62-by-15.30-mm chip. Operating current is 50 mA and standby current is 100 μ A. The TC574000D-150, with an access time of 150 ns, and the TC574000D-200, with an access time of 200 ns, are available on a sample basis. Volume production will begin in May.

FORCE'S VMEBUS COMPUTER MAKES MULTIPROCESSING-SYSTEM DESIGN EASIER

Comprehensive message-passing capabilities offered by Force Computers Inc.'s CPU-23 single-board computer lets original-equipment manufacturers sidestep box-level or custom-design solutions when they build midrange 32-bit VMEbus multiprocessing systems. Aimed at process control, robotics, and other industrial applications, the CPU-23 integrates a Motorola Inc. 68020 microprocessor, a 68882 floating-point coprocessor, a 32-bit direct-memory-access controller, and up to 4 Mbytes of memory. It gets its multiprocessing capability from an application-specific integrated circuit that implements a message-passing architecture for up to 20 central processing units. The Campbell, Calif., company expects the unit to help OEMs considerably reduce time-to-market for their system designs. Available now in 12.5-, 16.7-, and 25-MHz versions, the computer's base price is \$4,990.

THIS 17-MIPS WORK STATION MARRIES MOTOROLA'S 88000 AND INTEL'S 80386

A 17-million-instructions/s Unix work station from Opus Systems Inc. and Everex Systems Inc. promises to raise circuit-design, robotics, and multi-user applications to a new power level. It also lets MS-DOS and Unix applications run simultaneously. The Personal Mainframe Series 8000 achieves its performance by harnessing Motorola Inc.'s 88000 reduced-instruction-set microprocessor to an input/output subsystem based on Intel Corp.'s 80386. The strategic alliance marries the Unix coprocessor-system technologies developed by Opus of Cupertino, Calif., to the personal-computer expertise of Everex of Fremont, Calif. Motorola's binary compatibility standard makes the work station software-compatible with other 88000-based products. Unveiled at the Uniform trade show in San Francisco last month, the work station will be available in the second quarter with prices starting at \$9,995.

COMPAQ ADD-OHS TURN ITS PCs INTO CAD/CAM WORK STATIONS

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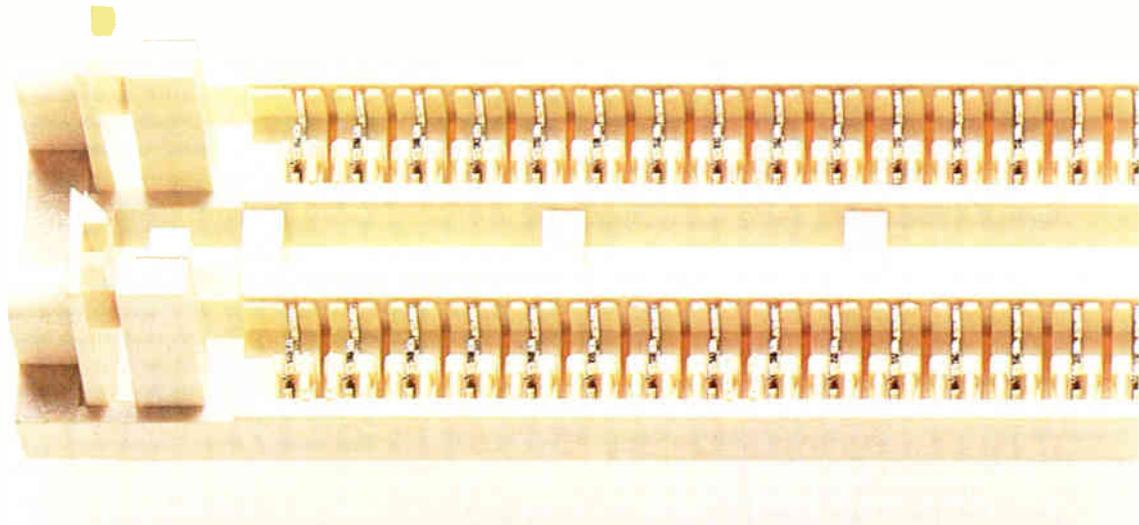
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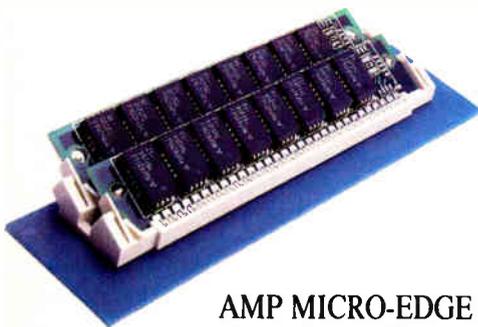


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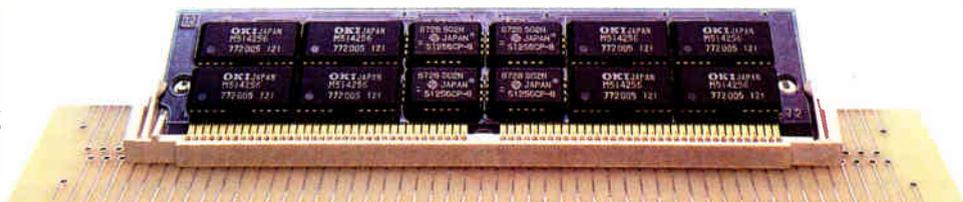
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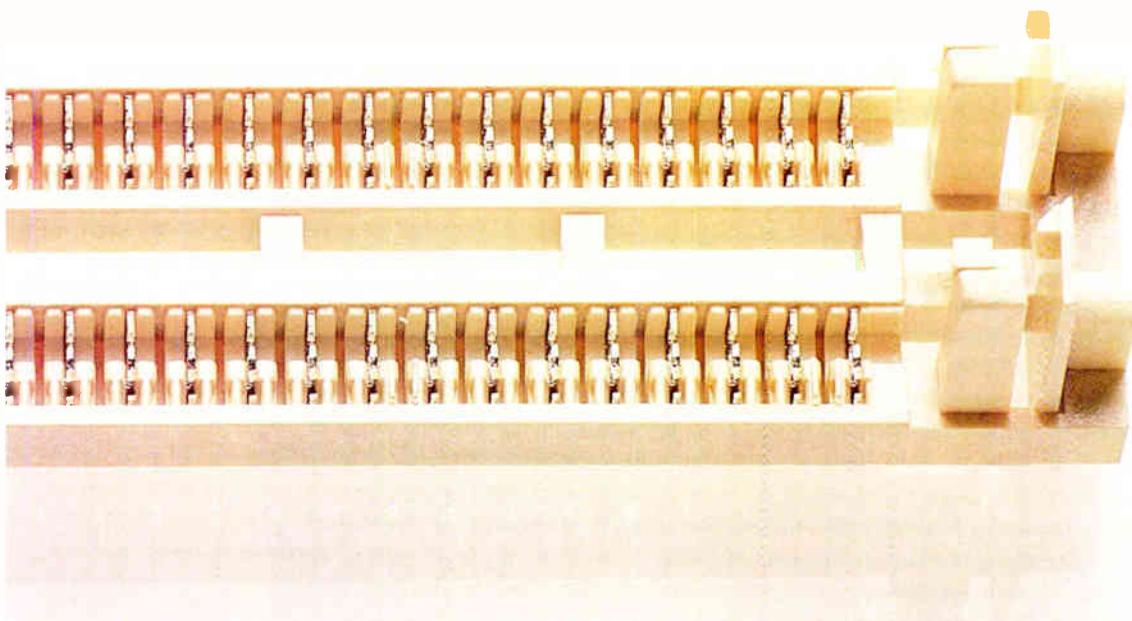
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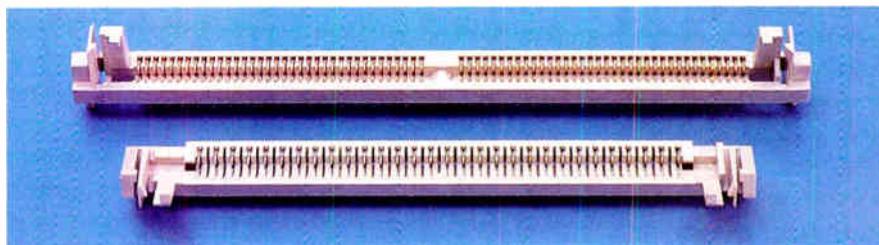
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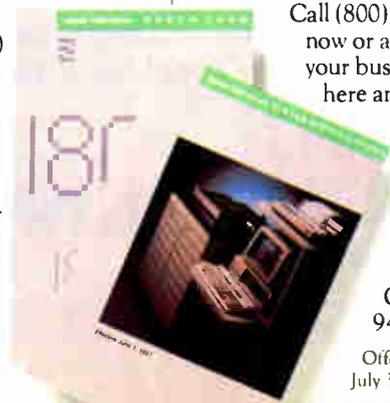
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Electronics

INTEL'S ISSCC BOMBSHELL: A SUPERCOMPUTER ON A CHIP

The 80860 may revolutionize the way work stations are built

SAN JOSE, CALIF.

Intel Corp. has dropped a bomb on the work-station market: a reduced-instruction-set-computer chip that is no less than the silicon equivalent of a Cray 1 supercomputer. It could mean that designers laboring on the next generation of RISC work stations based on Sparc, MIPS, Clipper, or 88000 central-processing units are going to have to start over.

The reason: Intel's chip, the 80860, does right now what the others had hoped to do by year's end. It integrates integer processor, 64-bit floating-point unit, data and instruction caches, and memory-management unit on one chip. It then adds a powerful three-dimensional graphics processor to boot.

The 80860, up to now known as the N10, sets a new benchmark in supercomputer applications. Running at a 40-MHz clock speed, the chip delivers 33 million VAX instructions/s running the Stanford test suites, 10 million floating-point operations/s on the Linpack benchmark, 90,000 Dhrystones, and 500,000 4-by-4 vector transforms/s performing a graphics operation. In addition, it has been designed for multiprocessor operation, so the company has multiprocessor Unix development under way to support it. If all that weren't enough, Intel will start selling the 80860 before the year is up for \$750 in 1,000-unit lots—a supercomputer on a chip at an affordable price.

The chip's commercial debut is bound to light a fire under developers of RISC-based systems, because the 80860 will permit them to build supercomputer work stations that will sell for less than \$10,000. To help this effort along, Intel is providing a compiler in addition to starting the Unix development. Meanwhile, original-equipment manufacturers—IBM Corp. is probably among them—are already designing systems with the chip. Computer makers find the 80860 appealing because its individual processors—integer, floating-point, memory-management and cache, and graphics—can all compute simultaneously.

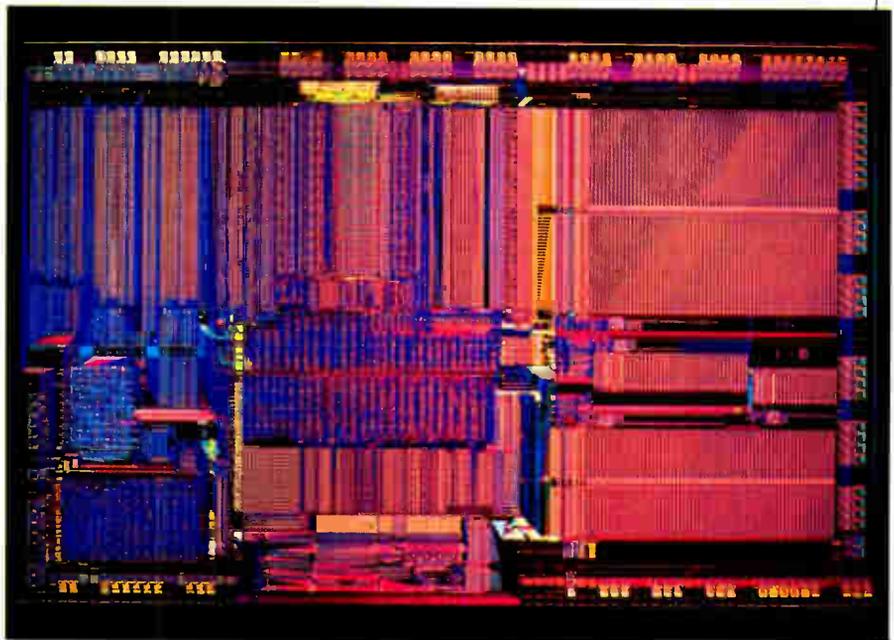
On the marketing side, shipments of RISC microprocessors in work stations have so far been far from breathtaking compared with those of complex-instruc-

tion-set chips such as Intel's 80386. Alice Leeper, senior analyst at Dataquest Inc., a market-research firm in San Jose, Calif., predicts that 600,000 RISC processors will sell this year, with the total growing to 6 million units in 1992. By contrast, she says, 8.3 million CISC processors will ship in 1989, growing to 26.3 million in 1992.

What is needed to narrow the gap is a high-performance, low-cost RISC chip that will spur work-station unit ship-

those making Sparc CPUs have been making do with multiple-chip solutions using 32-bit-wide architectures. Work-station vendors using other chips will also be at a cost and size disadvantage compared with those using the 80860. "With this chip, a designer can build a Cray 1 supercomputer in a small-footprint desktop system for under \$10,000," says Rash.

Rash cites the example of work-station manufacturers already offering diskless



Intel's blockbuster 80860 is likely to goose the work-station market, because it will permit system houses to build \$10,000 supercomputer desktop machines.

ments, and that can be used in embedded-control applications. That's the 80860.

"With the floating-point and graphics capability, the chip is ideal for high-end 3-d graphics work stations," says Bill Rash, advanced 32-bit microprocessor-marketing manager at Intel in San Jose. "It's also ideal for high-end engineering work stations performing simulations for solids and fluids as well as electrical-circuits modeling, and board and chip layout."

In either case, the chip threatens to leave work-station marketplace competitors in the dust. Semiconductor vendors such as Intergraph, MIPS, Motorola, and

machines for less than \$10,000 complete with high-resolution color graphics, a 1,000-by-1,000-pixel color monitor, and 8 Mbytes of random-access memory. "It's possible to build such a system with the 80860, which provides the graphics capability as well as the high-performance vector- and scalar-computing capability, and offer the system at the same price," he says.

The CPU cost with the 80860 will be considerably less than with the other RISC alternatives. A comparison made by Michael Slater, editor and publisher of the industry newsletter *Microprocessor*

Report, puts the single-unit cost of a minimum system using the Motorola Inc. three-chip 88000 RISC implementation at \$1,732 with a 32-Kbyte cache. The Cypress Semiconductor Corp. implementation with six chips and a 64-Kbyte cache costs \$2,500 in multiple quantities. And the MIPS Computer Systems Inc. implementation comes in at about \$1,515 in multiple quantities, with 128 Kbytes of cache.

However, the 80860 does have one disadvantage: a smaller cache than any of the others, though it does come with the integral graphics-processing capability that the others do not offer.

While the cost of the chip makes a persuasive argument for designers to switch from other RISC chips, Slater does not believe other RISC suppliers are going to be too worried yet. "The saving grace for all of them is that they have their own next-generation processors in the works," he says, "and they all have been out there establishing relationships with software developers, starting to build a binary base of software, and selling the user community on adopting a new binary standard."

Intel has recognized the importance of providing software for the 80860. In introducing the chip in late February, the com-

pany announced a complete set of development tools including C and Fortran compilers and Fortran vectorizers. Intel also has an early prototype of a multiprocessing version of Unix on the 80860, now being upgraded to System V, Release 4.0.

"We were concerned about the number

work stations, not to chips. And in recent months, major work-station vendors have already chosen the chip they will use in their next-generation product.

Digital Equipment Corp. is using the MIPS chip, Motorola has signed up a number of major OEMs for the 88000, and an impressive number of companies are building equipment around the Sparc architecture. So far no one has said it has enlisted the biggest OEM of all, IBM. But given Intel's close relationship with Big Blue on the 80386, which is used in IBM's Personal System/2, it's a safe bet that the giant computer maker has had a peek at the new chip—and IBM certainly can use it. Its workstation strategy with the IBM PC RT has been uninspiring at best, and the company is certainly looking to become a greater force.

Toward that end, IBM has licensed a set of tools from Next Inc. of Palo Alto, Calif. Coincidentally, the applications tool kit that Next developed is for a multiprocessor Unix operating system much like the one being developed by Intel and an independent group of companies for the 80860 chip.

But editor Slater thinks IBM has other plans for the 80860. "I think IBM is committed to the RT architecture and I would be surprised to see it change the



Yu tuned the design to the chip process.



Kohn's team used supercomputer methods.

of designers willing to recompile applications to take advantage of the capability of the 80860," says Rash. "But the level of performance improvement the chip offers, in some cases a 50-times boost in floating-point capability, motivates software developers to recompile." However, software developers port software to

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CPU in its RISC-based computer away from its own proprietary architecture," he says. "I could see IBM building a high-performance graphics subsystem using the [80860] as a graphics accelerator. That way IBM retains the main CPU but gets much higher graphics performance at the same time."

Slater believes that Intel's original intent was to bundle the upcoming 80486 with the 80860. "If the [80860] is used as only a graphics accelerator, it is easier to incorporate into a system," he points out. "A graphics kernel can be written for it and then applications software can take advantage of its performance without making the investment in applications-software development that would otherwise be required."

The chip comes with a RISC integer CPU, single- and double-precision pipelined vector floating-point processors (a separate adder and multiplier), 3-d graphics, 4-Kbyte instruction and 8-Kbyte data caches, and paged memory-management unit. It uses a 64-bit data and instruction bus to execute more operations per second. With such a wide data path, the computer can load a 32-bit integer and 32-bit floating-point instruction, which execute concurrently in a single clock cycle.

Moreover, because the unit has separate multiplier and adder, a multiply-and-accumulate operation can occur in a sin-

gle clock cycle as well.

At one company that has seen the 80860, Stellar Computer Inc. of Newton, Mass., vice president Michael Sporer says the idea of fetching a 32-bit integer instruction and a 32-bit floating-point instruction at once "is a fundamentally good idea. We implement that in our machine and I see more and more people doing it."

It's a safe bet that IBM is one of the OEMs that has had a peek at the 80860

In addition, the graphics processor can operate on bytes of data, a powerful feature for handling color. In one instruction cycle, the unit can individually process the values to drive the red, green, and blue guns of a color monitor and still have a byte operation to spare. But raw processing power is useless unless processors can rapidly acquire data to feed these units.

The 80860 has a system of buses that could not be implemented easily on a printed-circuit board with discrete processor chips. "A 64-bit bus feeds instructions to both integer and floating-point processors," explains Intel's Rash. It transfers

320 Mbytes/s of data. Another bus running between the data cache and the floating-point unit is 128 bits wide and can move 640 Mbytes/s. The external bus to the DRAMs is 64 bits wide and can transfer data at 160 Mbytes/s. "Altogether about a gigabyte of data can flow around the chip at any one time," he says.

While the chip uses a split instruction and data bus internally, externally it uses a standard 64-bit-wide bus for connecting to standard DRAMs. The bus transfers a data item every other clock, but with interleaved banks of DRAMs, all three banks can access data at once.

In addition to wide buses, the chip comes with architectural features to improve performance of its various processors. Leslie Kohn, chief architect, says his team applied some of the techniques that were developed for supercomputers to handle large data structures that did not completely fit inside the cache. Large data structures require many random accesses to memory. In a system with three banks of memory, for example, a structure could span all three.

"We have special instructions for performing pipeline accesses of large data structures, called pipelined floating-point load, in which the data is brought directly into the floating-point hardware without going through the on-chip cache," Kohn explains. The pipeline floating-point load

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instruction of a large data structure implies a one-time use of the data coming into the floating-point unit; so it is not desirable to flush the cache and load it with information that will only have to be flushed afterward anyway. This feature—preventing a cache flush and loading data directly from RAM at full speed by overlapping memory accesses from the three banks of memory—provides a factor-of-three speed increase.

Three-dimensional graphics capability was added after the initial chip-architecture definition. "We found that once we had developed the hardware to feed the floating-point unit sufficiently to keep it busy," says Kohn, "we could add another unit that required only 3% more silicon

area, and could piggyback onto existing hardware to give us about a 10-times performance improvement in 3-d graphics."

Just how did Intel come up with this impressive chip? "In a design as complex as the 80860, there are a number of intricate relationships between circuit design, architecture, and the manufacturing process," says Albert Yu, vice president and general manager of the component technology and development group. "What we have that others do not is a design that is tuned to the semiconductor process, and we believe we are ahead in 1- μ m CMOS process technology."

Also, other companies building RISC processors have either had to contract out some of the design or the fabrication

PROCESSORS REV UP AT THE ISSCC

Designers of microprocessors are like builders of drag-racing cars: they squeeze every ounce of power possible out of their finely tuned engines. And at this year's International Solid State Circuits Conference in New York, Intel Corp. of Santa Clara, Calif., took the checkered flag. Intel's vehicle was the 80860, a 40-MHz chip that packs more processing power per square micron than anything in its class this year (see p. 25).

But others were in the race with chips that, although not as loaded as the 80860, posted some impressive compute times as well. Among them was Hewlett-Packard Co.'s entry. The Palo Alto, Calif., firm offered a 32-bit VLSI central-processing unit rated at 30 million instructions/s that proves there's still life left in n-MOS. And Digital

Equipment Corp. of Marlboro, Mass., showed off two reduced-instruction-set computing machines, one monster that can peak at 50 mips and another that can run 20 mips sustained.

Outside the ISSCC, Cypress Semiconductor Corp. has rolled out its Sparc-compatible RISC engine, redesigned by Roger Ross. Ross's redesign cut the chip count from nine to six. In addition, the San Jose, Calif., company intends to introduce this year a complete chip set able to run at 40 MHz, says Dane Elliot, director of applications engineering. It also hopes to have a 50-MHz part by next January that offers 36 mips of integer performance. A floating-point unit running at 50 MHz should give about 9 million floating-point operations/s of double-precision floating-point computational power. Finally, Cypress has a cache-controller/memory-management chip that is the first to bring multiprocessing to the Sparc architecture.

Then there are the complex-instruction-

set CPUs, which promise to pack the magical million transistors under their lids, but will be slower rolling off the assembly line than expected. Michael Slater, who publishes the newsletter *Microprocessor Report*, says that Motorola Inc.'s 68040 and Intel's 80486 will be million-transistor chips, and that both will be out this year.

Slater says that the 68040 from Motorola will house a floating-point engine as well as a the memory-management unit. It will sport more pipelining, too, to boost performance by cutting the average number of clocks per instruction. Intel engineers, meanwhile, are making the same

moves on their 80486.

Slater thinks that Intel will announce the 80846 in April; Intel confirms this. Motorola, however, will hold off until later in the year when it has a few cir-

cuits off the assembly line.

Nor were gleaming engines from Japan in short supply at the ISSCC, though they were aimed at floating-point rather than integer crunching.

A 64-bit chip from Matsushita Electric Industrial Co. of Osaka gets some of its extra horsepower by doubling the word size. The number cruncher can run a 64-bit floating-point add, subtract, and multiply operation every 50 ns and a divide operation every 350 ns. That converts to 20 megaflops of peak performance. Measuring 14.4 by 13.5 mm, the chip crams 440,000 transistors under its lid.

A 32-bit machine, this one from Mitsubishi Electric Corp. of Hyogo, achieves an astonishing 40 megaflops of peak performance. The key lies in the use of an elastic pipeline structure, which minimizes the effects of clock skew on pipeline performance. Fabricated using a 1.3- μ m double-metal CMOS process, the chip holds a relatively modest 85,000 transistors in 13.3 by 12.6 mm.

—Jonah McLeod

Though Intel's 80860 is the winner, others also have pedal to the metal

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of their chips. By contrast, Intel does it all, and the 80860 was the result of a long-range view. To predict future-generation microprocessors, says Yu, one has only to look at developments in large-computer architectures. Then, as process technology allows greater integration, simply implement mainframe architectural features in silicon.

As Kohn and project manager Sai-Wai Fu began designing the chip in 1986, the Cray architecture was well known, but no one imagined it could be implemented on a chip. "With Intel's next-generation process technology, we recognized that we could build a million-transistor chip," says Kohn. "Without being constrained to be compatible with an existing chip architecture, we felt we could achieve significant improvements."

"Intel is good at taking risks when they think it is the right thing to do," Yu says. "When Les and Fu came up with the idea of the chip, it was not all that difficult to embark on the project." But it is one thing to propose an idea and another to produce chips three years later. "It takes a certain amount of faith and vision to believe that you can build a chip with 1 million transistors and that you're going to get good yields on it," Kohn says. "We had that and we were able to do it."

—Jonah McLeod, with additional reporting by Lawrence Curran

SEMICONDUCTORS

ISSCC CHIPS HERALD SWEEPING CHANGES IN SYSTEM DESIGN

SAN JOSE, CALIF.

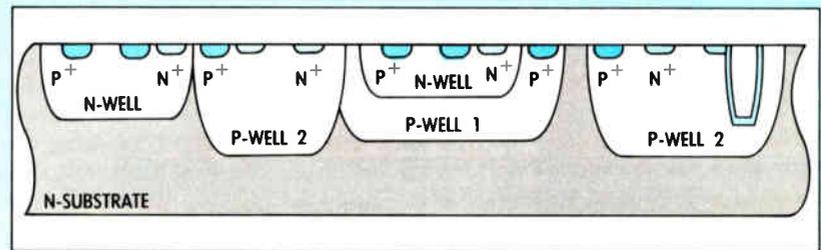
If last month's International Solid State Circuits Conference in New York can be said to have had a theme, it might be "Rethink Your Options, System Designers."

Across the board—in processors, dynamic and static random-access memories, nonvolatile memory, logic, and gate arrays—new circuit developments and combinations unveiled at the ISSCC prom-

ise to open possibilities for drastic changes in how systems are implemented. Not only are processor designers looking to 64-bit-wide architectures to boost system speed while facilitating the use of lower-cost main memory, but the density and speed of the memory devices that are emerging will show the way to system configurations never possible before.

Take DRAMs, for instance. Scarcely

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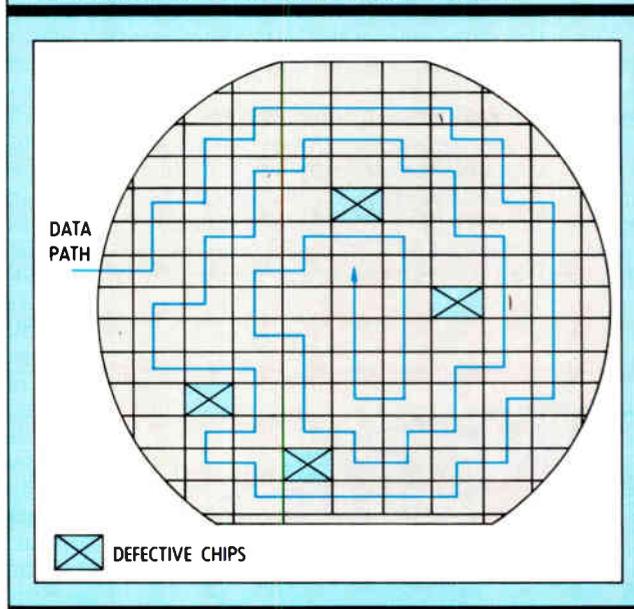
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have samples of 4-Mbit models begun appearing than designers are ramping up for the next generation of 16-Mbit designs. Three Japanese companies—Mitsubishi, NEC, and Toshiba—are aggressively looking to slice off this territory as their own.

The Mitsubishi Electric Corp. design is especially interesting. As if using traditional methodologies of 60-ns access time and 120-ns cycle time weren't enough, the Itami-based company's device also incorporates an on-chip multipurpose register that slashes access time for a limited number of bits to 15 ns. For its part, NEC Corp. of Sagami uses a proprietary latched sensing scheme to push access time on its chip down to just 55 ns.

And pushing row access time even lower, to 45 ns, the design from Toshiba Corp. of Kawasaki uses a combination of process improvements and circuit enhancements. The starting point is a CMOS process with three p-wells and a trench-type capacitor cell. The internal array is broken up into 64 subarrays, each 256 Kbits in size, reducing word-line delays as much as 2 ns

FUJITSU'S SPIRAL DATA PATH



Fujitsu's 200-Mbit wafer-scale serial memory is built around a core of operative and partially defective DRAMs.

They create four to five times the memory that can be crammed into a standard personal computer available on eight to 16 DRAMs or SRAMs with today's commodity parts. Assuming that future generations of the MS-DOS and OS/2 operating systems can be modified to handle it, the same number of sockets now available for a PC would be able to incorporate up to 16 Mbytes of DRAM, the limit in 32-bit central processing units for directly accessible memory.

From the system point of view, a harbinger of things to come in memory design is a 200-Mbit wafer-scale single-ported serial memory from Fujitsu Ltd. of Tokyo. The device was developed in cooperation with engineers from Anamartic Ltd. of Cambridge, England. Made with a standard 1.3- μ m CMOS process, the wafer contains a DRAM core of 1-Mbit dice in

per subarray. Users can also selectively activate eight of the 64 subarrays when operating power needs to be reduced.

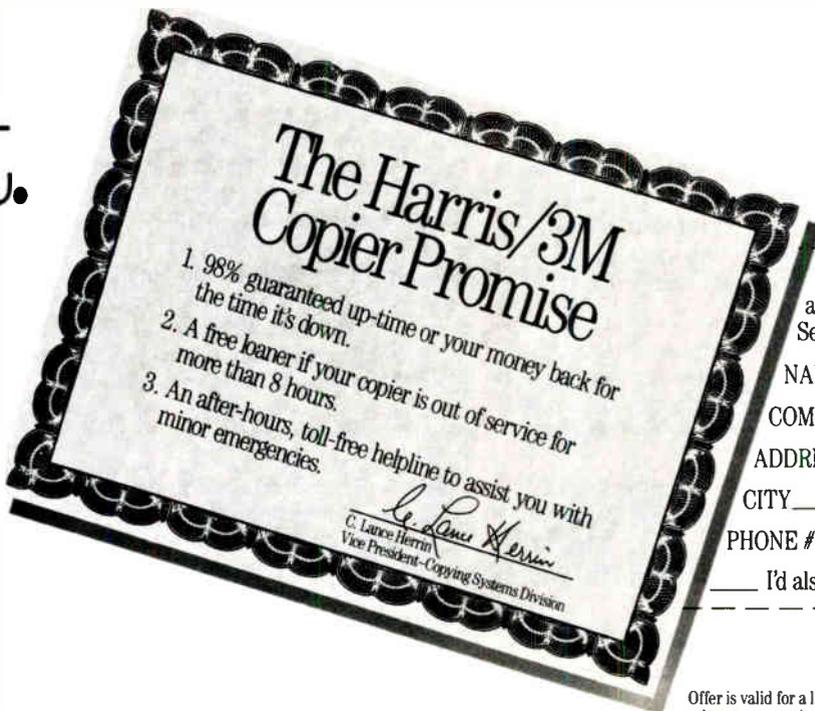
The design options with these parts, which store the equivalent of 2 Mbytes of memory on a single chip, are enormous.

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controller chip transmits commands to each configuration-logic module to set up serial links between the chips, creating a single contiguous-spiral data path. The transfer rate on the device is a respectable 20 Mbits/s, with a 52-ms refresh interval.

The conference also brought news for SRAM users. Developments at the ISSCC indicate that system designers will have to rethink the role of those chips in the traditional memory hierarchy in computer systems. Traditionally, in many high-

performance work stations, minicomputers, and superminicomputers, main memory was basically DRAM-based, while first-level cache was CMOS SRAM, and second-level cache was usually very small bipolar SRAMs.

But with the introduction at the ISSCC of very high-density SRAMs that are also very fast, this hierarchy may have to be juggled. For example, from Sony Corp. of Tokyo comes a 4-Mbit SRAM capable of an astounding 25-ns access time, equiva-

lent in speed to present 256-Kbit CMOS SRAMs. Sony engineers used a 0.5- μ m CMOS process and a dynamic-bit-line loading scheme in combination with address-transition detection.

No less impressive is the 1-Mbit SRAM with which Hitachi Ltd. of Tokyo has been able to push access times down to 9 ns, better than that of the 256-Kbit bipolar-CMOS SRAMs now in production. The Hitachi chip is made with a 0.5- μ m triple-polysilicon double-metal stacked CMOS cell. A three-stage p-channel MOS cross-coupled sense amplifier used in combination with an optimized internal-supply voltage scheme gets the speed. A high-speed redundancy scheme that doesn't carry the usual access-time penalty is a bonus. In it, a spare word is constantly activated when the same word in the regular array is selected.

IBM ENTRY. Also on the SRAM front, engineers at IBM Corp.'s General Technology Division in Essex Junction, Vt., have come up with a 128-Kbit all-CMOS SRAM that is compatible with emitter-coupled logic and boasts a 6.5-ns access time and a 5-ns cycle time. This performance matches the best speeds of 4-to-16-Kbit bipolar and biCMOS ECL SRAMs. The key to the IBM development is a highly pipelined internal architecture in which the chip is partitioned into thirty-two 4-Kbit subarrays, organized into four quadrants with each configured as 128 word lines by 32 bit lines.

Two 1-Mbit flash EEPROMs from Intel Corp. of Santa Clara, Calif., and Seeq Technology Inc. of San Jose are impressive for the speed with which they are moving to higher densities. The parts come no more than a year or so after the two firms introduced their initial 64-Kbit and 128-Kbit designs. In the minds of many in the industry, these devices, which combine the hot-electron write of the EPROM with the cold-electron erase structure of the EEPROM, could displace their EPROM and EEPROM cousins in many applications (see p. 70).

But all the EPROM-EEPROM and SRAM-DRAM developments highlighted at the ISSCC could fade into the background if a nonvolatile dark horse from Krysalis Microelectronics Inc. of Santa Clara proves out. A year ago, the firm said it had built a 512-bit nonvolatile SRAM using a proprietary ferroelectric material and standard CMOS processing [*Electronics*, Feb. 18, 1988, p. 95]. Now it has jumped ahead four memory generations to 16-Kbits, with a proprietary bit-parallel architecture.

The design is impressive for melding full SRAM-DRAM read-write operation with nonvolatility. In addition, its higher dielectric constant offers a way for designers to get the megabit densities of present silicon-based DRAMs, which require sophisticated stacking and trenching technologies.

-Bernard C. Cole



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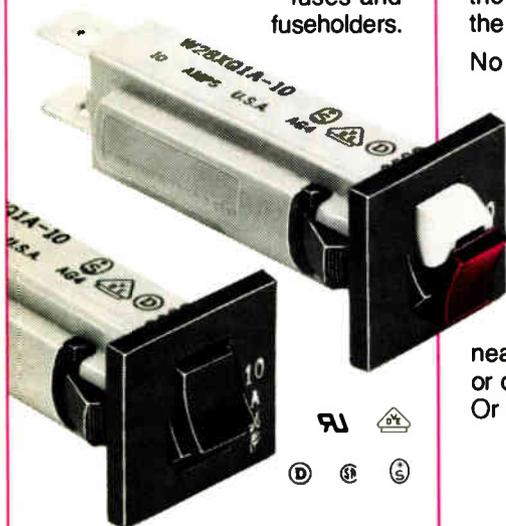
Replace fuseholders and slow-blow glass cartridge fuses in your design with W28 circuit breakers. Get the convenience of breakers at a cost that's competitive with fuses and fuseholders.

Attractive W28 breakers fit in about the same space as a panel-mount fuseholder. They can be prewired and snapped-in from the front. Integral mounting clips hold the W28 securely in place without the use of additional retainers.

No time-consuming searching for fuses. Protection against improper fuse rating substitution. And reduced fuse inventory requirements. All add up to increased value for your product.

Find out more. In the U.S., for the phone number of a nearby P&B sales representative or distributor, call 1-800-255-2550. Or write:

Potter & Brumfield Inc.
200 S. Richland Creek Dr.
Princeton, IN 47671-0001.
FAX: 812-386-2335.



Potter & Brumfield A Siemens Company

Circle 200

THE LAMBDA ATE SERIES

NEW COMPUTER PROGRAMMABLE POWER SYSTEMS.

Now in 3 different versions.

- 
- Fully complies to MATE requirements for your power supply control.
 - Control up to 31 independent power supplies per system.
 - Unique terminal supervisory control and display system monitors voltage, current and operation status.
 - Programmable voltage and current windows.



LAMBDA ELECTRONICS

DIVISION of **Veco** INSTRUMENTS INC.

THE LAMBDA ATE SERIES:

FOR INDUSTRIAL,
MILITARY OR SIMPLE GPIB
PROGRAMMING APPLICATIONS



Lambda Electronics has been the market leader in programmable DC power supplies for the ATE industry since its inception—providing a wide choice of products suitable for industrial and MIL-STD-810C applications up to 500 A. Now, Lambda offers the widest selection of IEEE-488 compatible power systems for all types of ATE applications...whether it's low cost industrial burn-in, or sophisticated functional test systems. Even military solutions that meet the rigorous requirements of MATE, can be configured to meet the exact requirements of ground benign applications. And Lambda can

design your system with optimal load protection.

Lambda offers three different and distinct approaches to meet the needs of the IEEE-488 ATE marketplace. All systems are designed using Lambda standard off-the-shelf modules in both narrow range (slot) and wide range (zero up) outputs, providing a cost efficient method of tailoring a system to your specific requirements...without engineering charges.

Lambda can provide outputs up to 500 A and 120 VDC using standard off-the-shelf power supplies, and further extends the range by using modified

custom supplies. All Lambda ATE systems are available for fast delivery and are backed with Lambda's published guarantees. This ensures each system will meet or exceed all published specifications for the full guarantee period. The three systems which are included in the ATE series are as follows:

1. Low Cost Computer Programmable Power System
2. Functional Talk-Listen Intelligent Power System
3. MATEPLUS™ Talk-Listen Power Systems (Mate Compatible)

LAMBDA ATE SERIES

1. LOW COST COMPUTER PROGRAMMABLE POWER SYSTEM.

An economical off-the-shelf answer for any application requiring multiple output

voltage and current programmability controlled over the IEEE-488 Bus. This system

is described in greater detail in Lambda's 1989 Power Supply Catalog.

2. FUNCTIONAL TALK-LISTEN INTELLIGENT POWER SYSTEM.

Ideal for ATE applications requiring ultimate load protection. This system reduces the time and cost associated with in-house software development of essential features required in the ATE environment. There are two basic modes of operation for the Functional Talk-Listen System—over the IEEE-488 Bus and via the unique RS-232 dedicated lines available with every standard system. These dedicated lines can be used in conjunction with IEEE-488 Programmable operation providing visual indication of power supply ratings, programmed values, actual measured outputs, and operational status or they can become the primary method of controlling the system. For operators with limited programming experience and a budget which does allow

for a fully configured ATE system, a simplified system centered around an RS-232 port is ideal.

This is how the system operates: Each specific output can be independently set by typing "Set Volt" for voltage or "Set Curl" for current limit of that particular output. Next "Safety Windows" which ensure the outputs (V + I) stay within a "Safe Operating Band" are set. The Functional Talk-Listen System does the rest. If any power supply goes out of tolerance of the windows, the monitor notifies you with a message. If an overvoltage or current limit condition exists the system will automatically shut down either the defective power supply or all the power supplies in the system. As an option, load isolation relays may be in-

corporated to automatically disconnect the power supplies from the load upon overvoltage or current limit conditions, or by simply typing "Open" on the terminal for that particular power supply load isolation relay to be selected.

This system is the simplest way to achieve an ATE environment without extensive programming and commissioning delays. And, should the application require upgrading to IEEE-488 operation, this system is fully compliant. The RS-232 port will aid in Stepwise Software Development and ease of system set-up providing all of the load protection features during operation in the manual mode.

TRIPLE OUTPUT

MODEL	DC OUTPUTS	DIMENSIONS (inches)	PRICE
A) MY*23341	(3) 0-7.5 VDC @ 500A	20 ³ / ₄ × 19 × 21 (4 Racks)	\$13,995
B) MY*23342	(2) 0-7 VDC @ 3.4A (1) 0-32 VDC @ 1.5A	5 ³ / ₁₆ × 19 × 21	\$5,156

QUAD OUTPUT

MODEL	DC OUTPUTS	DIMENSIONS (inches)	PRICE
C) MY*23343	(2) 0-18 VDC @ 1.8A (2) 0-32 VDC @ 1.1A	5 ³ / ₁₆ × 19 × 21	\$6,081
D) MY*23344	(2) 0-7 VDC @ 6.5A (1) 0-18 VDC @ 3.2A (1) 0-32 VDC @ 2.1A	5 ³ / ₁₆ × 19 × 21	\$6,581

FIVE OUTPUT

MODEL	DC OUTPUTS	DIMENSIONS (inches)	PRICE
E) MY*23345	(2) 0-7 VDC @ 3.4A (2) 0-18 VDC @ 1.8A (1) 0-32 VDC @ 1.1A	5 ³ / ₁₆ × 19 × 21	\$7,082
F) MY*23346	(2) 0-7 VDC @ 4.8A (1) 0-18 VDC @ 2.3A (2) 0-32 VDC @ 1.5A	10 ⁶ / ₁₆ × 19 × 21 (2 Racks)	\$7,570

SIX OUTPUT

MODEL	DC OUTPUTS	DIMENSIONS (inches)	PRICE
G) MY*23347	(5) 0-7 V @ 6.6A (1) 0-18 V @ 3.2A	10 ⁶ / ₁₆ × 19 × 21 (2 Racks)	\$9,030
H) MY*23348	(3) 0-7 V @ 3.4A (1) 0-18 V @ 1.8A (2) 0-32 V @ 1.1 A	10 ⁶ / ₁₆ × 19 × 21 (2 Racks)	\$8,280

3 - For MATEPLUS™ pricing information, consult factory.

FUNCTIONAL TALK-LISTEN INTELLIGENT POWER SYSTEMS

SYSTEM DESCRIPTION

Lambda's Functional Talk-Listen Power Supply System provides the communication link between an end user's controller (computer) and Lambda standard off-the-shelf power supplies.

The modular design of the system and broad selection of Lambda power supplies gives an engineer maximum versatility in tailoring a system to his specific needs. System elements include:

- Lambda Standard Power Supplies—Wide range and narrow range (slot) supplies.
- Lambda Standard Rack Adapter for mounting and packaging equipment.
- Interface Card—Accepts CIL commands over the IEEE-488 bus. (One per system.)
- Programming Cards—One per power supply.
- VT-100 (or compatible) Hardware hookup lines.
- Multiple Designed-in Software Features—User accessible.

The Lambda Talk-Listen Power System includes all the interconnection wiring and comes completely assembled, tested, and carries Lambda's 5-year guarantee.

SYSTEM FEATURES

Lambda's Functional Talk-Listen System provides:

- Two-way communication (talker/listener).
- Programming of functions in English mnemonic language.
- Confidence test (internal self-test).
- Programming of voltage and current limit.
- Performance monitoring.
- Bus independent fault mitigation.
- Programmable and/or tracking overvoltage protection.
- Monitoring of output voltage and/or load current over the IEEE-488 bus.
- System Syntax verifications.

More importantly, this system provides the test engineer with more diagnostic and sensory capability than any other off-the-shelf, programmable power supply system available in the marketplace today.

The Lambda system is capable of controlling the output voltage and current limit of up to 31 power supplies per system. The unique part of the system is its ability to monitor the operating conditions centered on or related to programmed values of voltage and current limit. This monitoring capability is twofold. The first being the actual output parameters (V + I) of each power supply in the system. The second is a passive fault monitoring scheme which is based on user definable safety windows that provide the test engineer with fault notification when these minimum or maximum values are exceeded. These values are setpoints which are independent of the overvoltage (VLTL) or programmed current limit (CURL) value of the power supply. The attainment of an overvoltage fault (VLTL) or a sustained current limit will both result in system disconnect and shutdown (RST) without any action initiated by the controller. See Table 1 for additional features and specifications of the Lambda Functional Talk-Listen System.

FUNCTIONAL TALK-LISTEN SYSTEM SPECIFICATIONS

Number of Power Supplies Programmed Per System
31.

Power Supplies

Lambda wide range supplies and narrow range (slot) supplies.

Zero-Up Wide Range Power Supplies

LD Series (wide range models)
LQ Series, LT Series, new LLS and LMS Series

Narrow Range (Slot) Power Supplies

LR Series

Output Voltage Range

Up to 120VDC.

Output Current Range

Up to 500A.

VOLTAGE REGULATION MODE

Line Regulation/Load Regulation

Individual power supply specifications apply.*

Ripple and Noise

RMS—Individual power supply specifications apply. (Plus 2mV for linear power supplies.)

Peak-to-Peak—Individual power supply specifications apply. (Plus 6mV for linear power supplies.)

Programming Accuracy

0.1% of full scale.

Programming Resolution

0.025% of full scale.

Temperature Coefficient

TC of individual power supply plus 0.01%/°C.

Overshoot

0.25 Volt maximum at turn-on, turn-off, or recovery from short circuit (without load isolation relay option).

Programming Voltage

Numerical or scientific notation, four digits in volts.

Programming Time

Voltage programming 50 milliseconds typical.

Voltmeter Accuracy

0.7% of full scale.

CURRENT REGULATION MODE

Line Regulation/Load Regulation

Individual power supply specifications apply. (Wide range supplies only.)

Ammeter Accuracy

1.7% of full scale + 20mA.

Programming Accuracy

2.0% of full scale.

Resolution

1.0% of full scale.

AC Input

105 to 132VAC, 50/60Hz.

187 to 242VAC, 50/60Hz or 205 to 265VAC available as an option.

Operating Temperature Range

0°C to 60°C.

Storage Temperature Range

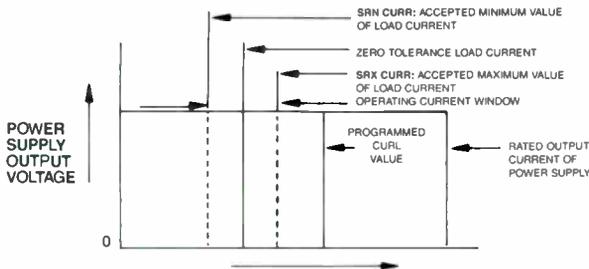
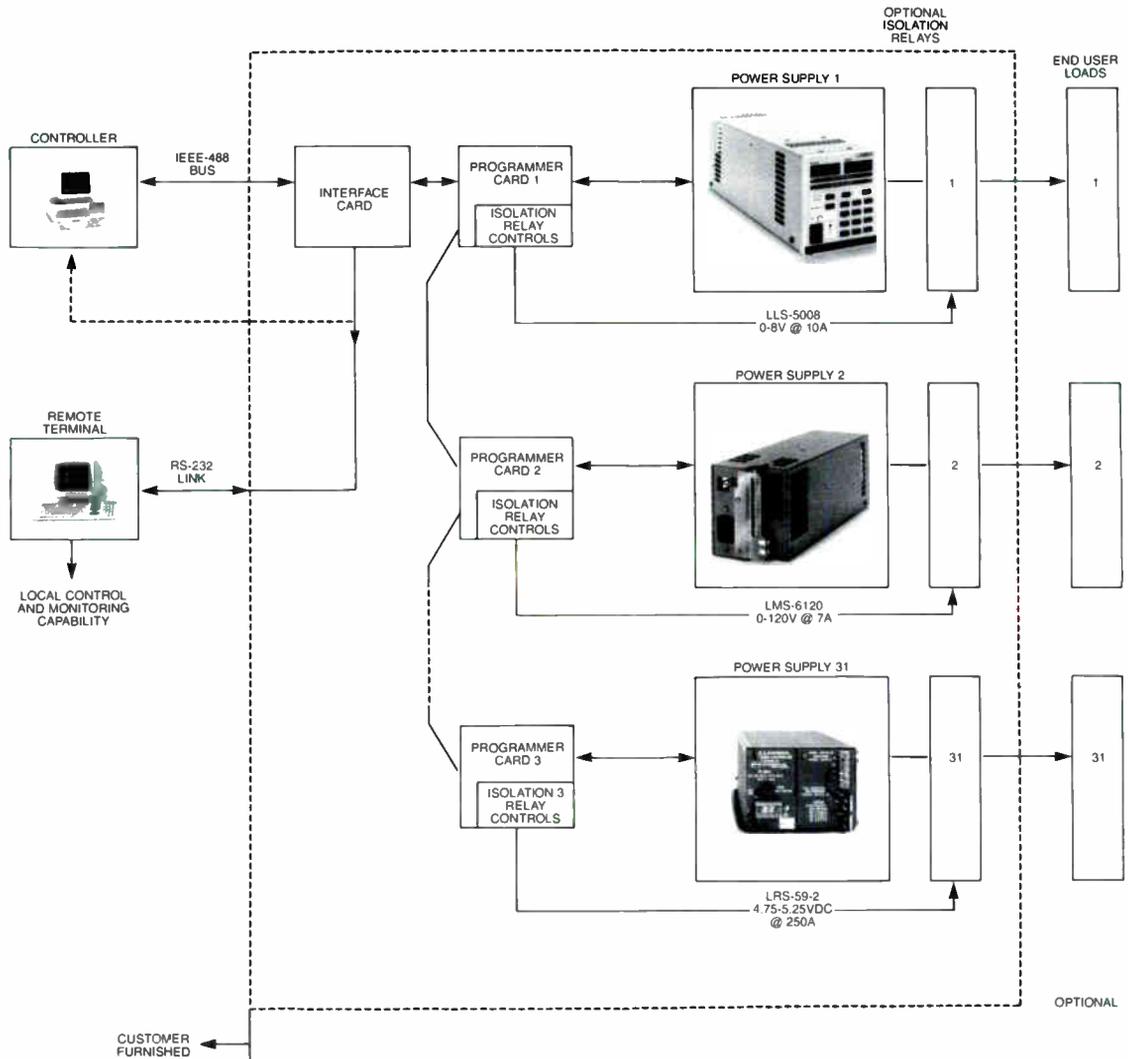
-25°C to +85°C.

Power-On Status

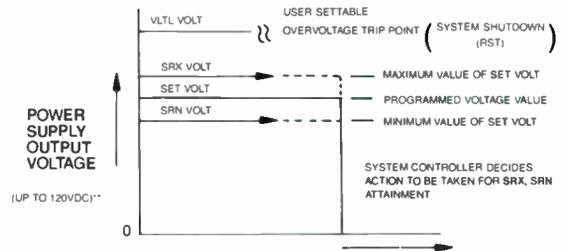
All outputs set to zero volts, zero current.

FUNCTIONAL TALK-LISTEN INTELLIGENT POWER SYSTEM

SYSTEM BLOCK DIAGRAM



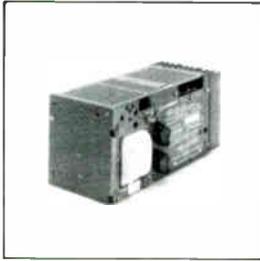
Graphical Definitions of SRX CURR, SRN CURR, SET CURL and Rated Current.



Graphical Definitions of VLTL, SRX VOLT, SRN VOLT, SET VOLT.

MATEPLUS™ PROGRAMMABLE POWER SYSTEMS

COMPATIBLE POWER SUPPLIES



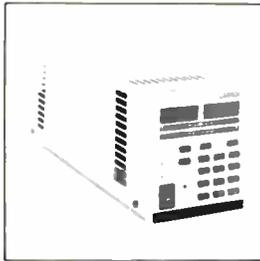
LD SERIES (WIDE RANGE MODELS)
UP TO 9.5 AMPS



LMS SERIES
UP TO 100 AMPS



LR SERIES
UP TO 250 AMPS



LLS SERIES
UP TO 100 AMPS

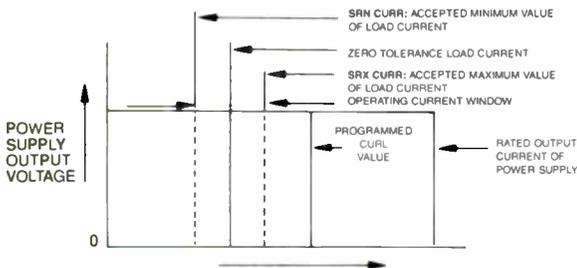


LQ SERIES
UP TO 14 AMPS

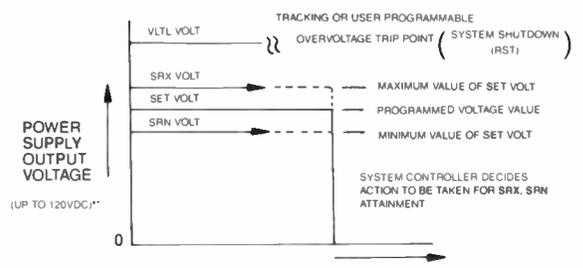


LT SERIES
UP TO 500 AMPS

OPERATIONAL LOAD FAULT CONDITIONS

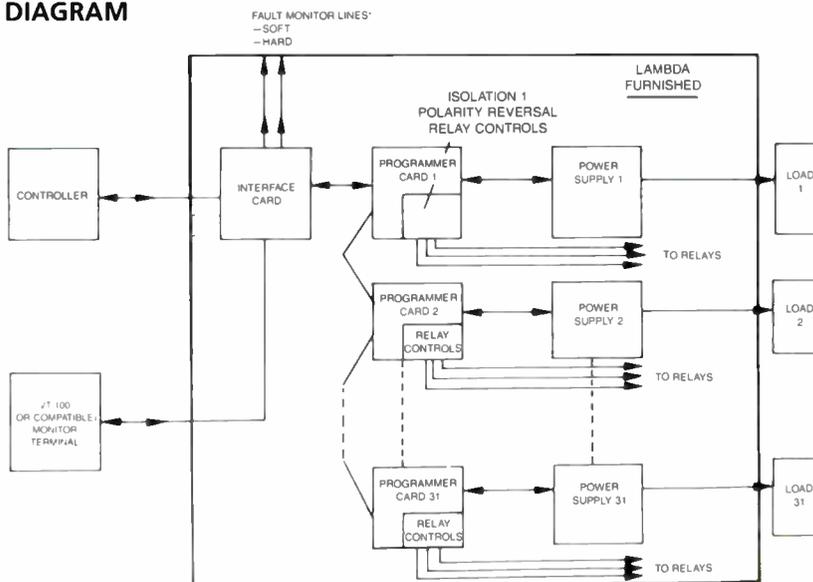


POWER SUPPLY OUTPUT CURRENT
(Graphical Definitions of SRX, SRN CURR, SET CURL
and Power Supply Rated Current.)



POWER SUPPLY OUTPUT CURRENT
(Graphical Definitions of VLTL, SRX, SET SRN VOLT.)

MATEPLUS BLOCK DIAGRAM



MATEPLUS™ PROGRAMMABLE POWER SYSTEMS

PROGRAMMING FORMAT

COMMAND MNEMONICS	DESCRIPTION
FNC DCS: CH nn	FNC—Function DCS—DC Source :CH nn Power Supply #
SET VOLT nn · nn	SET VOLT— Programmed Output Voltage Value (Volts)
SET CURL nn · nn	SET CURL—Programmed Current Limit Value (Amps)
RST, CLS, OPN	RST—Reset to Zero Volts, Zero I Limit CLS—Relay Close OPN—Relay Open
CNF, STA	CNF—Confidence Check (Internal Self-Test) STA—Status Report Requested
SRX	Set maximum window value
SRN	Set minimum window value

MATEPLUS™ RESPONDS TO FOLLOWING IEEE-488 COMMANDS:

COMMAND MNEMONICS	DESCRIPTION
ATN	Attention
DCL	Device Clear
IFC	Interface Clear
MLA	My Listen Address
MTA	My Talk Address
REN	Remote Enable
UNL	Unlisten
UNT	Untalk
GTL	Go To Local
DAB	Data Byte
FTH	Fetch Output Load Values (V + I)

Table 2 — COMPARING LAMBDA'S MATEPLUS™ SYSTEM WITH STANDARD MATE REQUIREMENTS

LAMBDA MATEPLUS™ SYSTEM FEATURES	MATEPLUS™	STANDARD SYSTEM REQUIREMENTS
• Two-way communication (Talker-Listener)	+	/
• Voltage and current readback over the bus via FTH command	+	
• Programmable overvoltage protection	+	
• Programming of functions in standard MATE (English) mnemonic language	+	/
• Confidence test (internal self-test)	+	/
• Full voltage and current limit programmability	+	/
• Performance monitoring	+	/
• Local/remote operation for ease of system set-up and maintenance	+	
• Initialization of all power supplies in system, providing signature identification under software control	+	
• User defined overvoltage tracking (VLTL). System reset (RST) occurs upon attainment of that value	+	
• SRX VOLT, SRN VOLT: These two programmed voltage limits allow the user a safe acceptable window of voltage output	+	
• SRX CURR, SRN CURR: These two programmed current values allow the user a safe acceptable window of current output	+	
• Polarity reversal of each power supply under program control (option)	+	
• Constant current operation under program control (wide range supplies only)	+	
• Load isolation relay commands automatically activating upon load faulting or under command of host computer (option)	+	
• VT terminal (or equivalent) display system providing the following visual information:	+	
1) Channel Number (1–31 power supplies)		
2) Rated output of each power supply (V + I)		
3) Programmed values of:		
a) Voltage		b) Current limit
4) Actual measured values of:		
a) Output voltage		b) Load current
5) Status for each channel consisting of:		
a) Pending initialization		d) Faulted
b) Operational		e) Communication error
c) Window limit exceeded		
6) Replaces the function required by multiple voltmeters and ammeters		
• Dedicated bus independent hard and soft failure lines	+	
• Programmable and/or overvoltage tracking. System reset (RST) occurs upon attainment of that value	+	
• Monitoring of output voltage or load current over the IEEE-488 bus	+	

THE LAMBDA ATE SERIES

COMPUTER PROGRAMMABLE POWER SYSTEMS.



TO ORDER CALL YOUR LOCAL LAMBDA SALES ENGINEER.

Open 8:00 AM to 7:30 PM (East Coast Time).

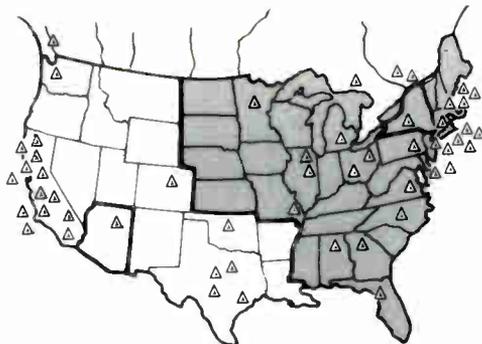
To contact the direct-factory Lambda Sales Engineer responsible for your account and located in your area, or to contact Customer Service for price, delivery or placing purchase orders, call as follows:

**IN EASTERN
UNITED STATES**
(Shaded area)

1-800-LAMBDA-4
(or call 516-694-4200)

**IN WESTERN
UNITED STATES**

1-800-LAMBDA-5
(or call 516-694-4200)



ADDRESS ALL CUSTOMER
CORRESPONDENCE TO:
LAMBDA ELECTRONICS
515 BROAD HOLLOW ROAD
MELVILLE, NY 11747
TWX: 510-224-6484
FAX: 516-293-0519

Canada

Lambda Electronics
4125 Cousens St.,
St. Laurent
Quebec H4S 1V6

1-800-361-2578
FAX: 514-337-1235

In Metropolitan Montreal
514-337-0311

France, Orsay

Lambda Electronique
Tel: 6012-1487

Japan, Tokyo

NEMIC-Lambda K.K.
Tel: 03-447 4411

England,

High Wycombe, Bucks:

Lambda Electronics
Tel: 36386/7/8

Germany, Achern

Lambda Electronics GmbH
Tel: 07841/5031

Israel, Tel Aviv

IsLAMBDA ELECTRONICS,
Tel: (03) 493941-2

Singapore

NEMIC-Lambda(S) PTE LTD
Tel: 251-7211

Korea, Seoul

Veeco-Korea K.K.
Tel: 02-556-1171/2

 **LAMBDA
ELECTRONICS**

DIVISION of  INSTRUMENTS INC.

WINDS OF CHANGE BUFFET DISTRIBUTORS

LOS ANGELES

The death in December of Anthony R. "Tony" Hamilton, chairman of Avnet Inc., could in coming months have more significance than the passing of a major industry figure usually does, mostly because of its timing.

More than three decades ago, Hamilton, who was respected even by competitors because of his upbeat outlook and accomplishments, single-handedly invented electronic-parts distribution as practiced today. Moreover, his brand of management—featuring heavy emphasis on salesmanship—built the flagship of distribution, Hamilton/Avnet Electronics. With some \$1.4 billion in sales, the Culver City, Calif., company has set the pace for a business that topped \$8 billion in the U. S. last year.

Distributors have been beset by many troubles in recent years, even during the chip boom of 1986-88. Today, their disappointing financial results reflect how tough things have gotten. So Hamilton's death, coming at a point when many executives and analysts believe that some fundamental changes have to take place, could hasten those changes.

DOMINO EFFECT. Even Hamilton's own company is not immune, industry observers say. They now single out as weaknesses the once-acknowledged strengths of Hamilton/Avnet, notably its nationwide scope and so-called "broad," or multiple-product, lines. Any basic changes at the firm will produce a domino effect for other companies, which must deal with Hamilton/Avnet because of its size and influence. It's still the largest U. S. distributor, followed by Arrow Electronics Inc., Melville, N. Y., and Lex/Schweber Electronics Inc., Westbury, N. Y.

For the time being, while Hamilton/Avnet management assesses where it stands, the official stance is only "growing concern for the bottom line," in the words of Edward Kaniger, senior executive vice president. Kaniger is running operations and reports to Leon Machiz, the former Avnet president who has taken over Tony Hamilton's corporate role. Both executives have vast experience and respect in the business, but outsiders note that "the company has Tony's stamp on it from top to bottom."

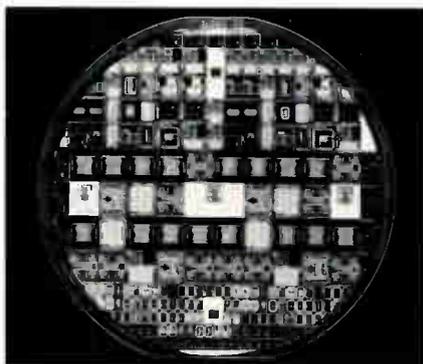
But it seems clear that "there will be some changes, because the mantle of leadership has passed to a different person," says financial analyst Clarke Walser of the Chicago Corp., Chicago. Others in the industry are less diplomatic; they say flatly that Hamilton/Avnet must change to keep up with competitors. Walser points out that Hamilton/Avnet

"for many years took advantage of its size," using it for buying clout with suppliers, which often translates into a price edge for customers. But events of the past business cycle, and disruptions in the semiconductor business itself, have made these largely a thing of the past. One ef-

fect is that smaller rivals have successfully chipped away at Hamilton/Avnet's markets, which are served by 53 franchised locations.

The bedrock issue confronting distributors today—and especially Hamilton/Avnet, which some believe has grown too

MOSIS



MOSIS Multiproject CMOS Silicon Wafer

Reduce the Risk of VLSI Design Prototypes as low as \$400!

Lowest Cost

Since 1981 MOSIS has been providing a prototyping service to IC designers by merging designs onto multiproject wafer runs. In the last two years, more than 3,200 prototype designs from commercial firms, universities and government agencies have been fabricated through MOSIS on over 100 fabrication runs.

Pay as low as \$400 and get enough parts to verify your design, instead of paying \$40,000 or more for a run and getting more parts than you need. Use the prototyping runs to develop your own libraries. With MOSIS' cost-sharing, you can't afford not to try out your ideas on silicon!

Highest Quality

Photomasks are purchased to zero-defect density specifications. Parametric test structures on the wafers are measured to ensure compliance with vendor process specifications. Standardized yield monitors measure defect density.

Wide-Ranging Technologies

MOSIS supports several different technologies and fabricators. Among them are:

- CMOS double-level metal at 3.0, 1.6 and 1.2 microns from Hewlett-Packard
- CMOS double-level metal at 2.0 microns from VLSI Technology
- CMOS double-level metal with second poly option at 2.0 microns from Orbit for analog designs

Projects can be designed with design rules from either MOSIS, the wafer fabricator or the DoD. MOSIS also distributes a library of DoD-developed standard cells (3.0, 2.0, and 1.2 microns) to designers interested in semi-custom design.

Diversified Design Tools

MOSIS Fabrication runs support:

- Fabricator's Tool Sets
- Berkeley Tool Set
- DoD Standard Cell Libraries (3.0, 2.0, and 1.2 microns)
- GENESIL Designs and Silicon Compiler Systems



MOSIS

For more information, contact Christine Tomovich or Sam Delatorre at (213) 822-1511.

The MOSIS Service, 4676 Admiralty Way, Marina del Rey, California 90292-6695

large to continue to dominate the fast-moving business—"is finding some way to differentiate themselves from their competition," says Walser. Merely selling standard commodity parts in small lots, the original basis for this field, can no longer support profitable growth.

Hence the pell-mell scramble of recent years as most companies dash into one or more new venues, such as computer and peripheral sales, semicustom chips, "kitting" parts together for assembly, and just-in-time delivery. Hamilton/Avnet is involved in all these activities. And its rivals believe that no matter how the distribution giant changes, it will remain a formidable factor.

Further complicating matters, the business remains oversaturated, with too many distribution outlets (some 1,500 or more) serving an industry that could get by very nicely with half that amount. "There are just too many mouths to be fed," says Walser.

Finally, to meet their own market-share needs, chip-firm suppliers typically award product franchises to too many distribution outlets in most geographic areas, further feeding the kind of dog-eat-dog competition that now prevails.

If these did not present enough challenges, the alternating boom-bust nature of components, which has always chal-

lenged and hampered the business, has been especially problematic of late. Most distributors haven't been able to regain the financial ground lost in the 1985 down cycle, which is apparent in results compiled by Walser. The most glaring weakness, and the one that most disturbs Wall Street about the publicly traded companies, shows up in profit margins, which are stagnant at levels well below those achieved in the past.

Still, distributors tend to be the most optimistic breed in the industry, and their upbeat outlook is still apparent in the

With their outlets proliferating, companies have a look-alike problem

face of the setbacks. The trouble is, distribution executives can't agree on the best ways to fix the problems.

For example, take the subject of nationwide operations, along the Hamilton/Avnet lines. Because selling parts in low volume is recognized as essentially a local-service business, the best setup should be a national firm that can buy in quantity, offer the financial stability of size, and concentrate through its franchise locations on building local ties. In practice, however, "returns from these economies of scale are all on paper," says John Geraghty, an analyst at New York's First Boston Corp. "They have not been realized for several years."

The main drawback in practice is that while expansion into new areas often gets the targeted sales gains, the operating costs rise even faster. With each sales office maintaining its own inventory, computer, and sales-support personnel, incremental sales gains are often more than offset by the cost of doing all the extra business.

Some regional distributors have established beachheads when an opportunity pops up. Among them is Semispecialists of America Inc., which started expanding last year and now has seven offices served by two warehouses. Semispecialists intends "to become a national distributor with a regional focus," says Robert Ball, senior vice president of the Melville, N. Y., company.

Manufacturers and customers are "looking for [distribution companies] with focus rather than a shotgun approach," he says. Semispecialists will try to keep its regional personality by limiting expansion to 17 carefully selected regional markets.

"We think it is cost-prohibitive to be everywhere," says Ball. "There's a move back to having two or three major distribution centers—one on the East Coast, one on the West Coast, and an option for

putting one in Dallas." Computerized inventory control and overnight delivery services make the consolidation of warehouse space possible, he says.

Another regional distributor that has now expanded is El Segundo, Calif.-based Wyle Laboratories Inc., which has moved into the East with distribution centers in Boston and Atlanta. But company president Charles M. Clough sees the problem less in terms of geography than in terms of each firm concentrating on what it does best.

The trend in recent years is plain to Clough: "It is running sharply toward specialization, because the broad-line outfits are not doing as well as they should." The reason is simple, he says. "No one, not even Hamilton/Avnet, has the resources to do it all." Wyle has been the industry leader in offering semicustom devices through its design centers, and also is among the front-runners in component kitting and computer-system sales.

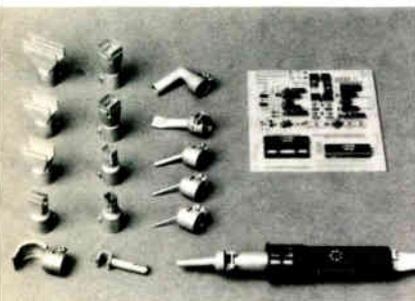
Clough's approach seems validated by the success of one of the two most profitable distributors, Anthem Electronics Inc., San Jose, Calif. In the key financial measurement of return on equity, Anthem is running at about 17%. The other profitability leader, according to a report by the Wall Street firm Donaldson, Lufkin & Jenrette Inc., is Marshall Industries, El Monte, Calif., with a similar return on investment.

JUST A FEW. Anthem achieves its financial marks by "focusing on a few activities, sophisticated chips, and computer subsystems," says its president, Peyton L. Gannaway. The firm, grossing about \$280 million, has far fewer suppliers than similar-sized competitors, with only 15 lines accounting for upward of 95% of sales. Adds Gannaway, "We'd rather be outstanding in a few lines than mediocre in many." Semispecialists, which is privately held and does not report profits, is following a similar strategy by giving its regional vice presidents considerable autonomy over which lines will be carried in their regions. It reported gross sales of \$160 million in 1988, which places it 12th among electronics distributors.

"We see two tiers of distributors emerging," says Semispecialists' Ball. "One will be the commodity type and the other will deal in more sophisticated technologies, such as ASICs and programmable logic devices." Although the business may stratify into two tiers, Ball does not rule out both being served by a single distributor with different strategies for each tier. "I don't think you'll see the commodity approach of carrying every line when it comes to ASICs," he says.

Instead, distributors will have partnerships with one or two manufacturers, he says. Although ASICs and programmable devices will be an important business, Semispecialists expects the market for com-

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Circle 205

modity chips to flourish as well, because of ASICs' price premium in the form of nonrecurring engineering costs. "If you're only going to build a few machines," says Ball, "there's just no reason to jump into ASICs."

Although Wyle, Anthem, and several others continue to find success by narrowing their focus, there are still some holdouts doing well with broad lines. Gordon S. Marshall, of Marshall Electronics in El Monte, sees little reason to go charging off into new things. In his view, the troubles stem from the fact that many distributors simply "do a terrible job." Poor business practices such as allowing runaway costs explain much of the disarray, he says. Then, too, "there are too many of us [distributors]." Marshall credits his firm's success to "working at being the low-cost producer," and rivals agree that he runs the most efficient operation in the business. The tough-minded Marshall also is the only national firm to handle major Japanese lines, which make up about 25% of its \$500 million-plus sales.

LOOKING EAST. Other distributors have their eye on how that market—as well as the distribution strategy for Korean components—will develop. The market presence of Japanese and Korean chip makers "is most clearly felt in memories and particularly dynamic random-access memories," says Ball. Like other distributors, Semispecialists tends to put the onus of selling foreign parts on the U. S. chip makers by saying that if the domestic semiconductor houses "choose to create a void, we're considering going somewhere else." Chips from Far East sources seem likely to become "increasingly a factor as time goes on," says Ball, "but I don't think they will be ubiquitous."

Along with questions about the course of events at behemoth Hamilton/Avnet, many industry executives worry that a recession will force unwanted changes on everybody, just as the chip downturn did in 1985. At that time, several firms disappeared, including one of the top 10, Kierulff, which was acquired by Arrow. If bad times do come in the next year, companies with big debt loads, such as Arrow and Hall-Mark Electronics Corp., Dallas, could be most vulnerable, says the Chicago Corp.'s Walser. In fact, Hall-Mark was the subject of a \$220 million leveraged buyout last year.

Marshall, who has seen chip cycles come and chip cycles go, is certain a recession is on the way. But he sees any resulting downsizing of distribution paradoxically serving to improve the business later. That's especially true for firms such as his that have strong finances, he says, and can weather the storm. "That's not gloom and doom," he says, "but realism." —Larry Waller, with additional reporting by Jack Shandle

SIGNAL PROCESSING

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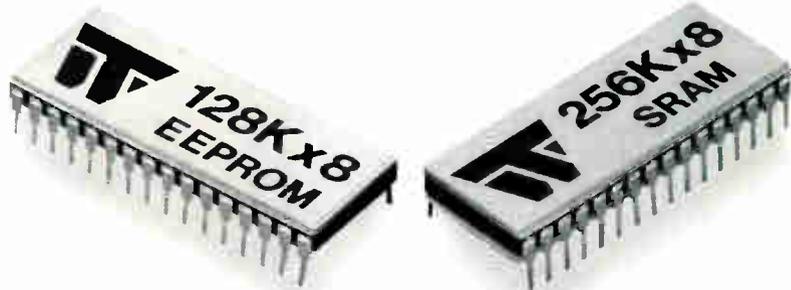
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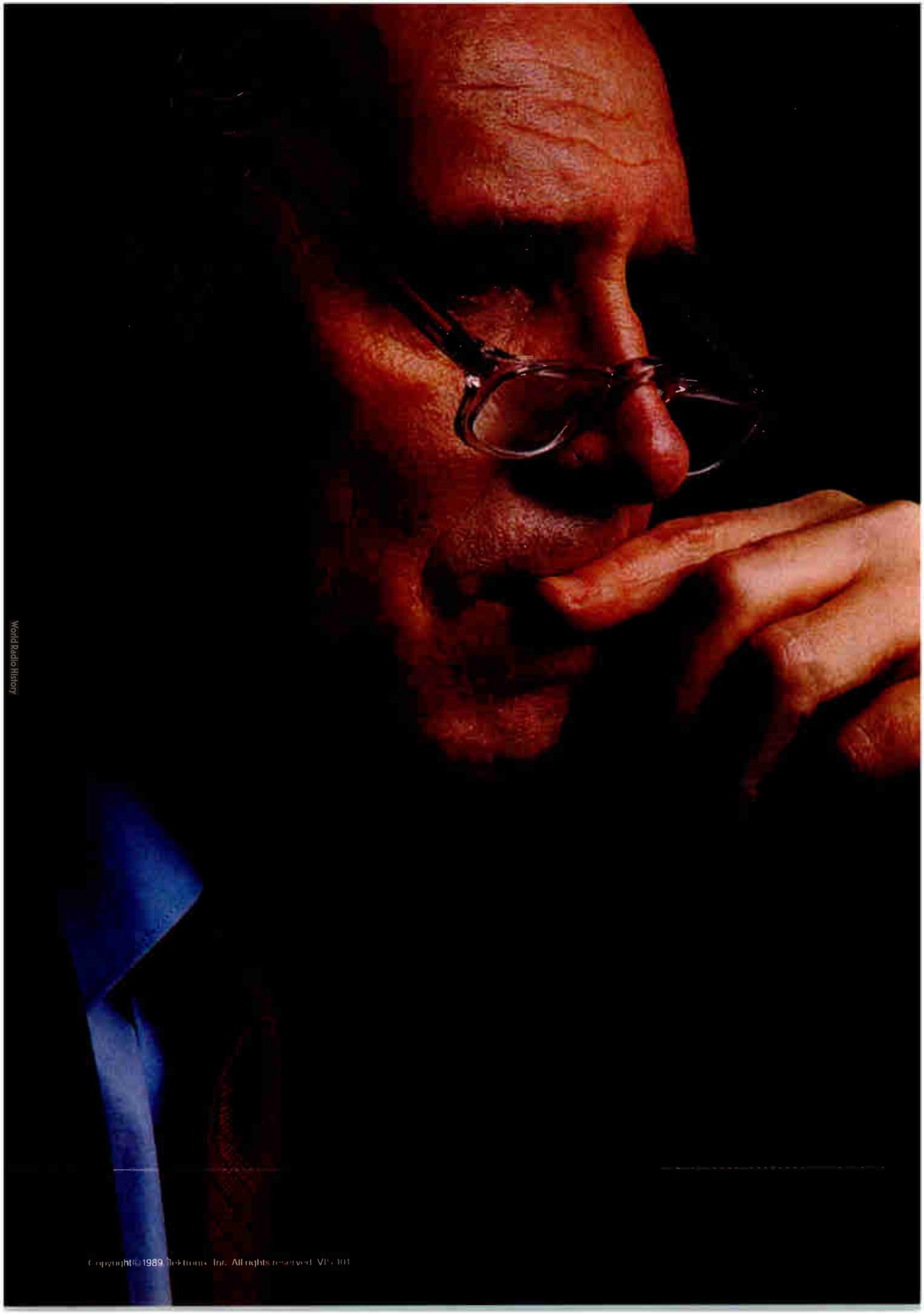
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Circle 4

depends on Advanced Micro Devices Inc.'s 29325C floating-point chips, which can be used as either adders or multipliers, as its base processors. But the SSP delivers more than raw computing power. Positioned in the high-end market to compete with supercomputers and array processors, the SSP does away with the computing overhead of Fortran programming—which is required by supercomputers—by letting applications developers “write” assembly code graphically. More than 35 microcoded primitives—among them fast Fourier transforms, vector and matrix arithmetic operations, trigonometric functions, filter functions, and even the Hough transform—turn the trick.

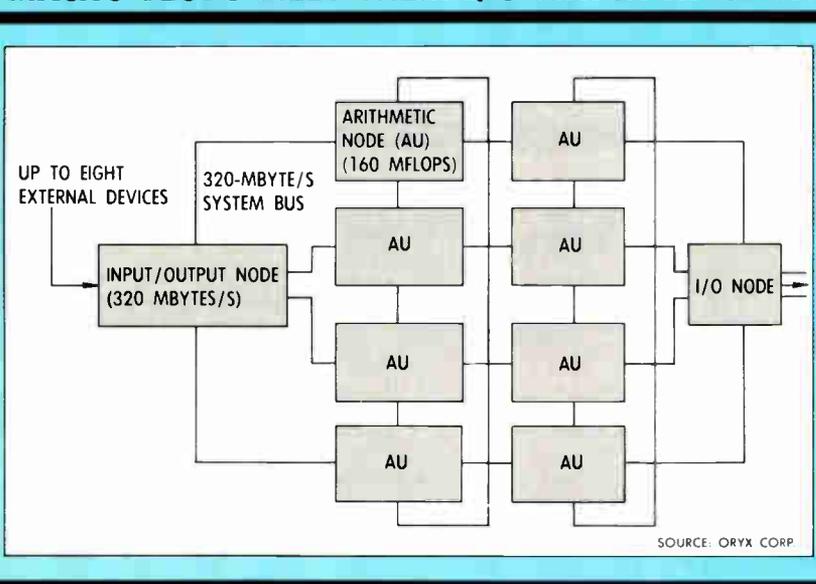
“In the past, developers have been using Crays programmed in Fortran or hardwiring application-specific compute devices for this kind of signal and image processing,” says Harold Messias, Oryx’s vice president of marketing. Because it is a high-level language, Fortran has a ravenous appetite for millions of floating-point operations per second. “If you’re paying for 100 megaflops and you’re programming in straight Fortran,” he says, “you’re lucky to get 20 megaflops of actual Linpack performance, depending on the application.” Hardwiring eliminates Fortran overhead, but at the expense of adding tedium.

NOW TESTING. Funded initially by a \$3.5 million stake from Eastman Kodak Co. in Rochester, N. Y., in 1985, Oryx got another \$7.4 million last year from an investment team that includes Kodak, Grumman Ventures, Allied Signal, and six venture capitalists. Its first product, a 60-megaflops machine, went to Grumman Aerospace Corp. in Bethpage, N. Y., last month for benchmark testing such military applications as surveillance, intelligence, and electronic warfare. Oryx will announce pricing later this month.

Since it has targeted real-time markets such as imaging from radar and sonar signals, electronic warfare, and military intelligence, Oryx armed the SSP with a formidable input/output bandwidth—320 Mbytes/s—which is well matched to its computing power. “The issue isn’t throwing a lot of chips in a box,” says Messias. “It’s getting the information into the chips so they can do something with it. But I/O is expensive. It’s where you really have to have a lot of wires.”

Oryx bases its SSP on a crossbar-switch architecture that connects processing elements and parallel memories. The crossbar switch realigns the eight processing elements in a node with any of eight parallel-memory-element buses. Each processing element can access any memory element on any 100-ns clock cycle, and any memory element can broadcast to any or all processing elements on any clock cycle. A node controller running under a real-time operating system

MACHO-FLOPS MEET THEIR I/O MATCH AT ORYX



Oryx optimizes the use of the SSP’s gigaflops-level signal-processing power with I/O nodes that handle 320 Mbytes/s and compute at 80 megaflops.

oversees all this, scheduling and dispatching up to 50,000 tasks—fast Fourier transforms, for example—per second.

Using 32-bit floating-point arithmetic, the SSP can attain near-one-gigaflops performance with six nodes, each contributing 60 megaflops of performance. The six-processing-node configuration is serviced by a 320-Mbyte/s I/O node, which interfaces with up to eight external devices and up to four processing nodes. Memory for the system has options from 16 to 512 Mbytes. If 60 megaflops is too much horsepower, the processing nodes can be scaled down to 20 megaflops, but Messias says, “We’re not really selling into that market.” Top-gun performance is a blazing 10 gigaflops.

The SSP was designed from the start to be rugged enough for military use. “It’s not a laboratory machine,” Messias says. “We can do image processing that allows the military to make tactical decisions in real time.” The SSP can handle image enhancement, edge enhancement, and contrast enhancement using the various transforms in its library of microcode primitives. Its high I/O bandwidth lets it handle the sonar, radar, or signal-intelligence input from the real world.

One possible application, for example, is the Autonomous Land Vehicle being developed by the Defense Advanced Research Project Agency. The ALV is essentially an unmanned tank; it drives itself. In this application, rapid calculations of the Hough edge-enhancement transform play a key role in keeping the ALV on course. “We’re not going to see unmanned tanks any time in the near future,” Messias says, “but there may be spin-offs from the development program.”

—Jack Shandle

FINANCING

HIGH-TECH FIRMS FINDING NEW MONEY SOURCES

LOS ANGELES

In the short term, the lingering slump in the prices of high-technology stocks mostly hurts the people who own them. But for the longer run, the sorry record of these once-glamorous equities can do more than just bruise some bank accounts. The effects of the crash of Oct. 19, 1987, already are so well marked that the customary way of financing growing high-tech businesses may well be changed forever. “You have to be fast on your feet—and innovative—to get things financed these days,” says Jon W. Bayless, a partner at Sevin Rosen Management Co. in Dallas.

Driving the change is the failure of new stock issues—or initial public offerings, in Wall Street parlance—to perform their traditional function. Since the early 1960s, IPOs have served as the keystone for startup companies to finance their next phase of growth and for their investors to recoup the original stake—with a profit—by selling stock.

When low prices dry up the market for IPOs—and also the secondary stock offerings that often are used as the next financing phase—companies that need capital have to seek it elsewhere.

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Circle 12

World Radio History

technologies. The result is a spate of alliances involving heavy hitters—for example, Silicon Graphics Computer Systems with Control Data Corp., and Sun Microsystems Inc. with AT&T Co. However, deals involving smaller companies are more common: TRW Inc. investing in AES Corp., a Peabody, Mass., defense-electronics firm; or Hewlett-Packard Co. buying 15% of a new superconductor-device firm, Conductus of Palo Alto, Calif.

Another tactic is the good old-fashioned

loan, though not usually from a bank. Loans come either directly from financial institutions in private placement deals, or from venture capitalists. In fact, the same institutions that will shun an IPO find direct investment attractive as so-called mezzanine financing. That approach previously covered only a short-term second round of investment in startups but now is seen as a longer-term vehicle.

The venture firms are playing so great a role in financing that they could be mov-

ing toward full-fledged investment banking of the type practiced by Wall Street outfits, says Bayless. In one new trend, venture companies handle arrangements for both sides, putting institutions that buy into a venture firm's own funds in touch with startups in its stable of clients. So Sevin Rosen brought in New York's Gibraltar Fund for a sizable stake in Proteon Inc., a Westborough, Mass., local-area-network startup. All this leaves fast-growing privately owned companies frustrated. Brooktree Corp. of San Diego, for one, has seen its IPO plans stymied. "It's just gruesome, that's what it is," says James Bixby, president.

There is no single source that keeps score on IPOs, but the authoritative *Technologic Computer Letter* tracks them more closely than anyone. Editor Richard Shaffer could count only 18 high-tech new issues for 1988, with most taking place during the first half. The total is down some 50% from 1987, he says, which also was a slow year. IPOs raised about \$450 million last year, which was probably far under the total venture money socked into the field.

And the future doesn't look much brighter because of the resistance to IPOs from institutional money managers, the influential stock pickers who handle billions for banks, pension funds, and mutual funds. The managers are a significant cadre, accounting for upwards of three quarters of all stock activity.

JOB THREAT. With all the values abounding in visible, proven high-tech listed firms, "it's tough for an investment banker pushing a new issue to walk in [to a money manager] and say, 'Have I got a hot company here for you,'" says Pierre R. Lamond, a principal at Sequoia Capital in Menlo Park, Calif. As Brooktree's Bixby notes, money managers are on the spot too. "One admitted to me that if he picked one more high-tech loser for his fund, it would cost him his job."

As to whether the recent Wall Street rally will have a positive effect on the IPO outlook, financial analyst Adam F. Cunney has a blunt response. "Absolutely not," says the San Francisco-based analyst, who follows semiconductors for New York's Kidder Peabody & Co. He points out that only a few high-tech companies fared well while smaller firms continue to lag badly. Nothing will change for the better in the face of "continued financial-community skepticism about the high-tech companies' ability to generate a profitable return with a slowdown or recession looming," he says.

Still, the market could confound the pessimists. Gary Smaby, analyst for Needham & Co. in Minneapolis, agrees that prospects are none too bright right now. "But in 1986, I would have said exactly the same thing. And then we had that spurt in 1987 technology stocks. It's very unpredictable," he says.

—Larry Waller

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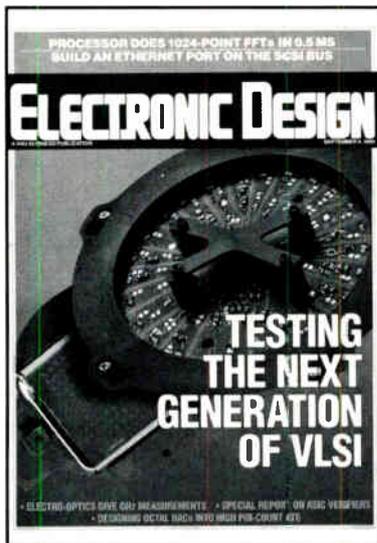
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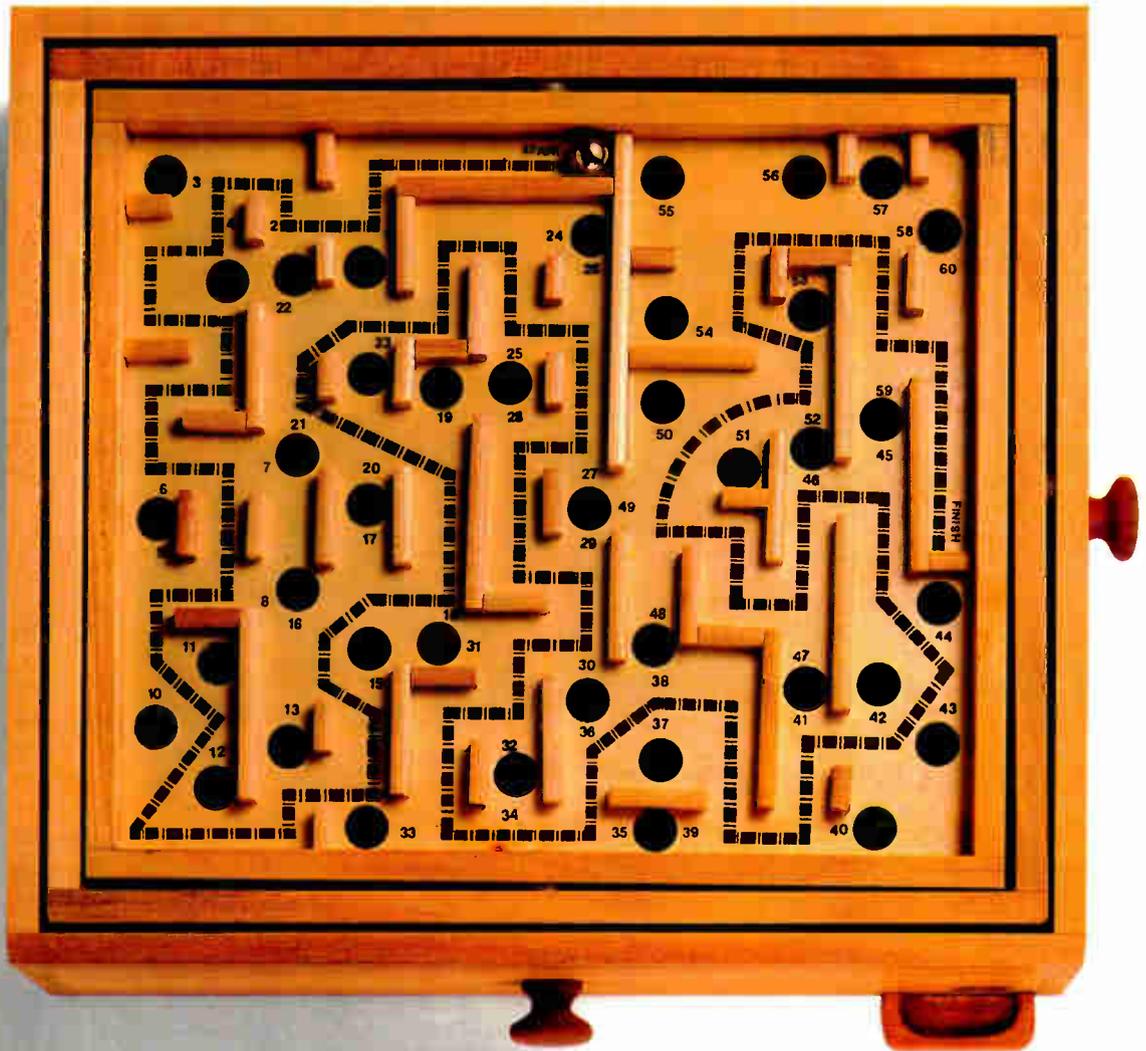
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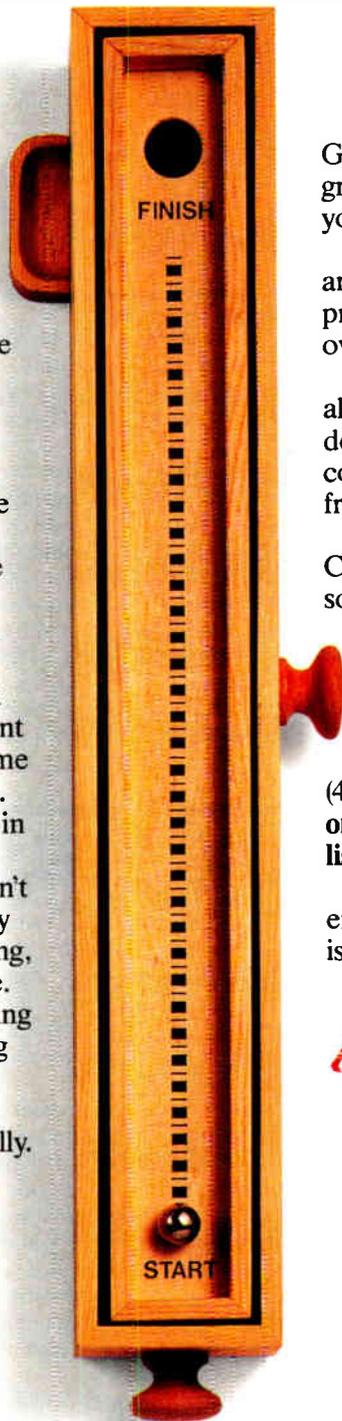
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Leadership by Design

Circle 50

MOTOROLA TAKES ITS SHOW, IMAGINOLOGY, ON THE ROAD

PHOENIX, ARIZ.

Of all the big U. S. semiconductor houses, Motorola Inc. may be the one least likely to launch a glitzy new marketing gambit. The company's image is conservative, verging on stodgy.

Nonetheless, Motorola has come up with just such a gambit—a traveling trade show, featuring its products and the hardware that uses them. What's more, the show is drawing enthusiastic crowds and rave reviews.

Called Imaginology, the show was put together by Motorola's Phoenix-based Semiconductor Products Sector, solely for itself and its customers. Over the past year, it's played in seven locations, drawing larger and larger crowds. Most importantly, from Motorola's point of view, those crowds have included some 15,000 design engineers—the people any chip company knocks itself out to reach.

What's drawing the crowds is an event that features solid technical seminars on Motorola products, hardware that incorporates the latest Motorola chips, and voluminous application tips on how to use them. All of this is presented in a state-of-the-art show—Motorola went to top outside consultants to find out how to put together a slick production, with top-flight graphics, lighting, and sound.

Evidently, the effort was worth making—it would have been hard to get those

15,000 design engineers into the Motorola booth at most industry trade shows. But besides working as a direct-marketing tool, Imaginology could have wider, more long-lasting benefits, says Adam F. Cuhney, a financial analyst based in the San Francisco office of Kidder, Peabody & Co. He sees the show providing "recognition value" among customers and potential customers as to the level of service

Throwing a party earns Motorola the customer's undivided attention

Motorola provides. This is particularly important for Motorola, Cuhney thinks, because intensive service and customer support will be the hallmark of the 1990s, and Motorola has suffered from being "looked at as an old-style organization of the 1970s," he says. Also, Imaginology offers Motorola a way to show off its product lines, which are the broadest anywhere. And the company gains an edge by throwing a party—the audience's attention is undiverted by any competitors.

The audience, of course, gets a lot from the show too—the technical seminars, the product demonstrations, the applications tips. But the real secret of the show's suc-

cess in attracting people seems to be very simple: Imaginology comes to them, rather than making them come to it. That was the thinking when Motorola came up with the idea, says Robert C. Field, director of the chip sector's advertising and promotion department, who is the show's godfather. Two years ago, Motorola, like most semiconductor houses, was dissatisfied with existing shows. It dropped out of some, including Wescon. "We had a brainstorming session, on 'how do we reach those engineers?'" says Field. "We go to their home area, that's how."

Though the idea is working well, Field says the show's format is continually being tinkered with, "We learn as we go along," he says. More and more Motorola chip customers are joining up. Some 112 came to a show in Detroit last October, compared with less than 30 at the first show in January 1988 in Irvine, Calif. In Detroit, the company gave 31 seminars, dedicated entirely to automotive electronics, up from 12 seminars in Irvine.

Motorola will not say exactly how much the show is costing, but Field acknowledges that \$1 million is a reasonably accurate estimate of total expenses, not including travel costs and the time of the people involved. But this is not inordinate compared with the costs of major industry shows: participating in the biggest of them could set the company back \$500,000, sources say. In any case, Motorola management is backing Imaginology.

So Motorola will keep Imaginology on the road. At least three dates are scheduled for this year and into 1990. The main challenge now, Field says, is "topping last year."
—Larry Waller

CONSUMER

THE POCKET DIARY GOES ELECTRONIC

TOKYO

Electronic organizers are selling like hot rice cakes in Japan, where business people who didn't realize until recently that they needed another executive toy are now spending up to several thousand yen apiece on the things. At least one Japanese manufacturer is encouraged enough by their reception to start exporting the gadgets, but how well they'll go over among Americans is the subject of brisk debate in the U. S. consumer-electronics community.

An executive organizer looks like a pretentious pocket calculator, and in fact the two companies driving the market are Sharp Corp. of Osaka, and Casio Corp. of Tokyo, the leading manufacturers of calculators in Japan. People use them as they would a desk calendar or pocket diary, to keep track of appointments and expenses and so on, punching the information in on a keypad instead of writing it

down. The organizer stores the data in memory; the user punches a few more keys to display it. The availability of inexpensive memories with extremely large capacity, operating at low power, and of low-cost display drivers, makes them practical to produce.

At their most extravagant, organizers can include all the functions found in so-called "personal-productivity software" for a personal computer. In Japan, this includes most of the functionality of a word processor, including character generators for a kanji character font and programs to convert phonetic keyboard input to kanji. Many include a communications link to exchange data with a similar unit or a printer.

Sharp is modifying its export models to provide raised keys on the keypad, rather than the film keys used in Japan. On both domestic and export models, it offers plug-in cards to add functions. About 70%

of Sharp's organizer sales in Japan are units that take the plug-in cards, says Akira Nakanishi, a manager in Sharp's information systems group.

Simpler organizers are available from another manufacturer, Seiko Instruments Inc. of Tokyo, as well as from Sharp and Casio. These are single-purpose units about the size of a credit card, says Shinji Morisaki, the general manager of Seiko's Portable Products Department. They do one main chore—keep schedules or store telephone numbers—and usually work as four-function calculators, too. Users can also buy a kind of loose-leaf notebook, like the inserts for storing floppy disks in computer manuals, that hold three of the units. The keys can be operated through the transparent pockets, so a binder turns the single-purpose units into a somewhat cumbersome multifunction organizer.

If the Japanese have their way, the or-

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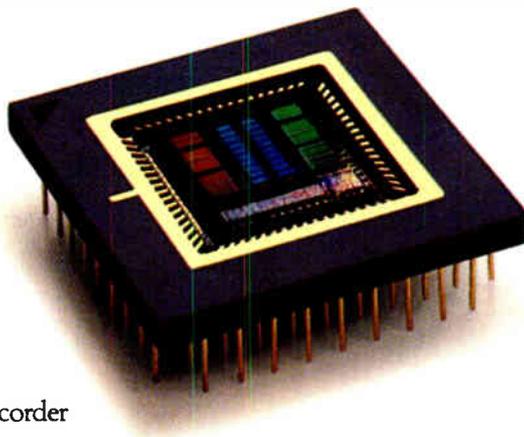
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VLSI TECHNOLOGY, INC.

Circle 13

ganizers will soon invade the U. S. Advance troops have already landed, in the form of Sharp's Wizard, a multifunction organizer introduced last October. It weighs 8 oz. and sells for \$300, says Steven Salas, national sales manager for Sharp's U. S. subsidiary, Sharp Electronics Corp. in Mahwah, N. J. The \$300 list price gets you the base unit with 32 Kbits of read-only memory, enough to handle a telephone directory, a memo pad, scheduling functions, a built-in world clock, a

calculator, and some other functions. Plug-in cards to add more functions are for sale at retail prices ranging from \$100 to \$130. Three are available so far: a time-management card, a dictionary/thesaurus card, and an eight-language translator card. More are in the works.

Sharp thinks the big selling point for Wizard will be software to let it communicate with an IBM Corp. PC, which is due in February. Software to hook up with the Apple Computer Inc. Macintosh will

follow. "On one end of the scale, you could call the Wizard a high-class electronic organizer, which it is," Salas says. "But on the other end of the scale, you could call it a PC interface. The reason I'm excited is we're not competing against faster and better—like the original PC, then the XT, the AT, and the 386. Instead, we're competing for portability and lightness. So we're not talking about megahertz speed here. We're talking about portability."

Other, more objective observers question whether U. S. business people are all that eager for portable information. One of them is Robert Gerson, editorial director for *TWICE*, a New York consumer-electronics trade publication. He points out that electronic organizers came around in the 1970s and flopped. The new organizers are smaller and easier to operate, but Gerson still doubts people are willing to take the time to punch in all the phone numbers and appointment dates that make the organizer useful as something other than a paperweight with a display screen and keypad. The Wizard is "a wonderful gadget," Gerson says. "But here again, you still have to put all that information in. When you talk about the Wizard, it is something for engineers. I don't know who else is going to use one."

Sharp is promoting the Wizard as a device for salesmen and other business types who are on the road a lot, not engineers. Gerson wonders whether a large company will be willing to pay \$300 each to give, say, 1,000 salespeople a trinket that essentially is nothing more than a Filofax with batteries. He thinks it more likely the Japanese makers will run afoul of the East-West culture clash. "They have discovered time after time that it is not like the Japanese market," he says. "We're very gadget-oriented, but not this kind of gadget."
—Charles L. Cohen
and Wesley R. Iversen



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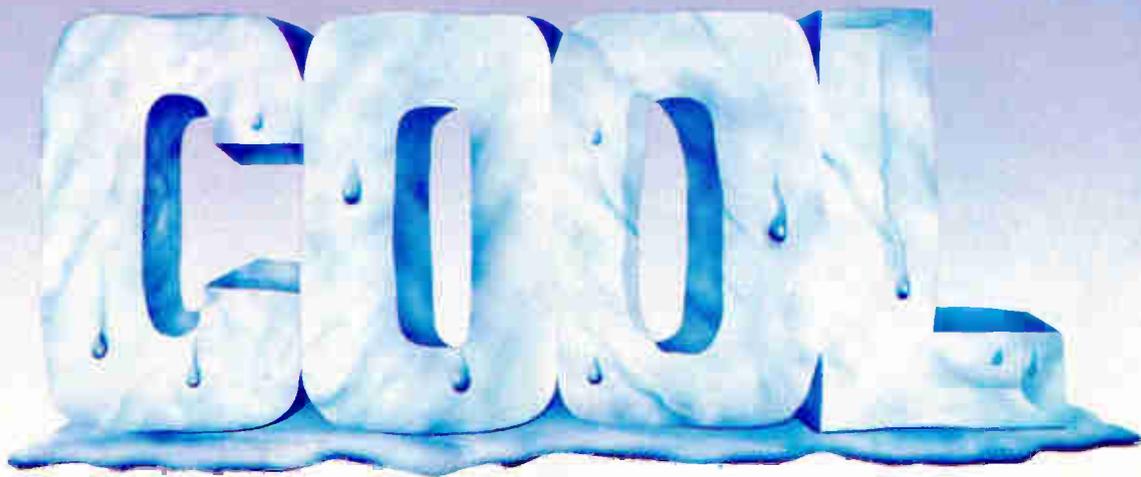
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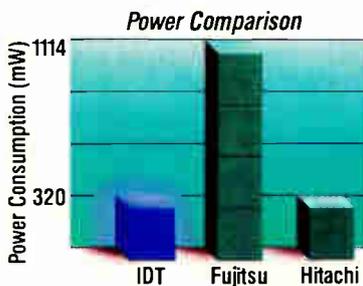
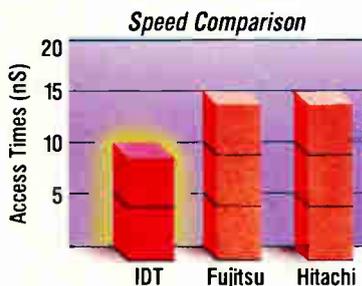
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WASHINGTON INSIDER

SDIO KEEPS CHIPPING AWAY AT DIAMONDS IN THE ROUGH

The Strategic Defense Initiative Organization thinks diamonds could be a satellite's best friend. Their naturally high band gap means diamond computer chips can withstand much higher temperatures than silicon or gallium arsenide—700°C compared with about 125°C. They can also tolerate far more radiation and operate at higher power and frequency, which makes them highly attractive for use in the satellites that would make up a Star Wars system. Cooling systems—now 65% of the average satellite's weight—could be made some nine times smaller and the cost of a launch slashed to a tenth of what it is now, says Dwight Duston, director of SDIO's Innovative Science and Technology office. SDIO accordingly is pumping more than \$4 million a year into work on diamond-based chips. Its research shows that diamond circuits can be designed and built, but a major hurdle remains: growing diamond wafers. "Diamond has a hard lattice constant to match," Duston says—the 700°C-to-800°C temperatures being used to grow thin diamond films are too hot for the most suitable substrate materials, such as lithium fluoride, to survive. The Research Triangle Institute in North Carolina is scrambling to develop a copper-nickel alloy that could stand such temperatures; elsewhere, work is focusing on a low-temperature processing technique that would allow the use of lithium fluoride. If any of these pan out, Duston says, diamond chips could eventually be price-competitive with silicon—making them practical for commercial as well as military applications. □

SILICON CARBIDE DEBUTS AS AN APPROACH TO RAD-HARD CIRCUITRY

While SDIO officials are trying to make diamond wafers, a small company in Durham, N. C., next month will begin selling a family of diodes that exhibits many of diamond's properties. Cree Research Inc.'s high-power, high-frequency diodes use silicon carbide, which like diamond is a refractory material that can operate at very high temperatures—around 350°C—and in very harsh environments. The diodes also are inherently hardened against radiation. More important, SiC can easily support oxide layers, so unlike gallium arsenide it can be used to create MOS FETs—a basic building block in silicon chips. Working on a number of development contracts with SDIO, the Air Force, NASA, and the Navy, Cree plans to move up from diodes and eventually produce small- and medium-scale integrated circuits. □

THE PENTAGON GETS CLOSER TO GENERIC CHIP SPECIFICATIONS

The Defense Department hopes to establish by summer a final version of a new "generic" specification that will radically alter the way the military buys integrated circuits. The spec, Mil-I-38535, aims to eliminate the costly and time-consuming practice of qualifying each chip individually by letting the Pentagon certify processes and manufacturing lines instead. Any part produced on a certified line would be fully qualified for military use. That should cut the time it takes to turn new technology into working chips on the DOD's Qualified Parts List. In the process it will make it easier for the military to use application-specific ICs. The new system will also relax requirements for government audits and end-of-the-line testing, allowing chip makers to take much more responsibility for their products. Not that making the new Qualified Manufacturers List will be a piece of cake—it's going to take extensive investment in quality and process controls, from design through wafer fabrication, assembly, and test. The Defense Electronics Supply Center in Dayton, Ohio, has already done a week-long preliminary QML audit at AT&T Microelectronics, and is also working with other interested vendors, including GE/Harris, IBM, Intel, LSI Logic, National Semiconductor, Texas Instruments, and VLSI Technology. □

WASHINGTON INSIDER

IF THE 101st CONGRESS FREES THE BABY BELLS...

Ever since a federal court decision split them off from AT&T Co., the seven regional Bell Operating Companies have been pressing for more freedom, and their wish may be granted soon. The House of Representatives is irked by the fact that the author of that decision, U. S. District Court Judge Harold Greene, still controls communication law and policy as far as AT&T and the operating companies are concerned. It may move this year to repeal restrictions that keep the RBOCs out of manufacturing and selling advanced information services. Last year, the House passed a resolution calling for a major communications bill in 1989. House insiders now say keeping to that schedule is unlikely, but they insist that a bill will be passed in the House by 1990. The Senate, by contrast, appears less impelled to get involved with the issue. "The Senate Commerce Committee believes Judge Greene is acting reasonably," says Thomas Cohen, the committee's senior legal counsel. "No intervention is necessary at the moment." But officials at the Justice Department are hinting that they believe the current restrictions "are against technology" and have "delayed progress in the information age," so the Senate could be forced into action, too. □

... WILL IT ALSO LET THEM GET INTO THE CABLE-TV BUSINESS?

Congress may let the regional Bell Operating Companies build equipment and sell services in the next year or two, but it's not likely to settle another, related issue any time soon: whether telephone companies can operate cable-TV systems. "The telephone companies are all looking for new opportunities, and high on their list is cable," says Howard Anderson, managing director at the Yankee Group, a Boston investment firm. "They have learned that they have only one asset, their core network." Right now, the Cable Television Act of 1984 forbids them to use that network to deliver cable TV in their home territory. Congress could repeal the act, but that would only clear the way for independent telephone companies. The regional Bell companies would still be locked out by the ban on offering information services established by the court decision breaking up AT&T Co. And even lifting that ban won't settle the issue, says Walter B. McCormick Jr., majority chief counsel for the Senate Commerce Committee. The real question is not whether the phone companies are allowed to deliver TV signals—he says that's inevitable—but whether they should be limited to the role of distributor or allowed to offer their own programming. □

TRW PULLS AHEAD WITH THE FIRST PROTOTYPE MIMIC CHIPS

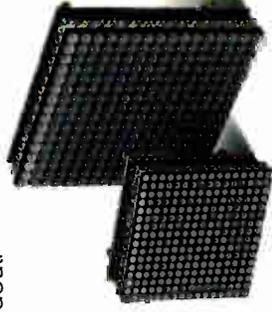
TRW Inc. is taking an early lead in the Microwave/Millimeter Wave Integrated Circuits Program. The company became the first of four Mimic contractors to weigh in with working chips when it delivered its first prototypes in February, but what puts the TRW parts in a class by themselves is the advanced technology TRW is using—a proprietary heterojunction bipolar transistor technology unique among the four contractors. The chips, which include a logarithmic intermediate-frequency amplifier, a switched attenuator, and an amplifier/divider, operate at up to 6 GHz. TRW's 3- μ m minimum feature sizes are comparatively large—and therefore less of a dimensional design challenge than those of its competitors—says Mimic program director Eliot Cohen. But, he says, "that's what is most appropriate" for the target systems the chips were designed for: data handling in the IF range between the high-frequency sensors that acquire data and the low-frequency digital electronics that process it. The new device makes possible packaged modules that consume only 20% of the power and take up only 5% of the space of current bipolar-based hybrid amplifiers. □



Toshiba LED Module Achieves Delicate Display with 16-Gradient Control.

The forms and functions of information and its handling are diversifying with great speed. Toshiba, a world leader in the opto-electronics field, has developed a 16 x 16 LED dot matrix module that opens new possibilities in information display. By combining these modules, a display equivalent to that of a TV can be realized. By use of Toshiba's outstanding two-color LED together with its unique gate array for driving, 16-gradient control is achieved in this new product. Compact design makes the module lightweight and optimally thin. Unique heat radiation design greatly improves the dispersion of heat from the module, and connections are simple, ensuring freedom from maintenance. In applications ranging from simple messages to visual displays such as message boards, entertainment and projector use, Toshiba's LED module is a standout.

CHARACTERISTICS	DETAIL					
Type Name	TLMM501B2	TLGM501B2	TLSM501B2	TLMM502A1	TLGM502A1	TLSM502A1
Color Display*	Red, Green, Amber	Green	Red	Red, Green, Amber	Green	Red
Dot Size		ø5mm			ø3mm	
Dot Pitch		6mm			4mm	
Weight (Typ.)	170g	165g	165g	95g	85g	85g



*Amber color is made by a mixture of red and green.

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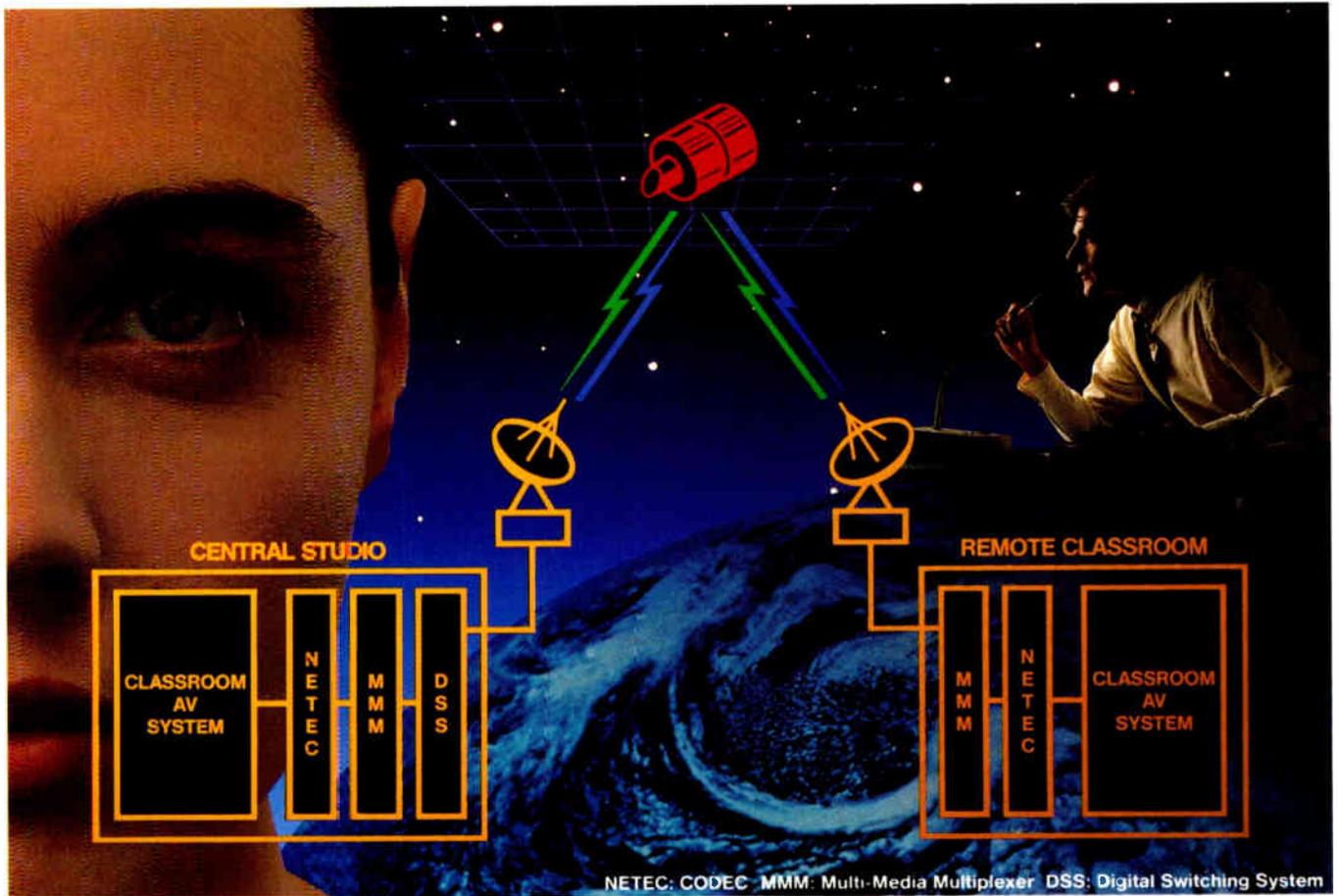
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Circle 17

NEC NEWSCOPE



TELE-EDUCATION VIA SATELLITE NETWORK: INTERACTIVE VIDEO AND AUDIO.

NEC is operating one of the world's most advanced satellite-based tele-education systems. Called NESPAC (NEC Satellite Pedagogical Network for Advanced Creative Education), the system links a central studio at the NEC Technical College near Tokyo with three other classrooms in remote locations across Japan.

The most prominent feature of NESPAC is interactive video and

audio communication between lecturer and students. The system can simultaneously transmit and receive two channels of color motion video signals, as well as one channel of audio and data signals from an electronic writing board.

For economical use of the satellite circuit, a NETEC series video codec digitizes and compresses video and audio signals to 1.544Mbps. It also scrambles the signals to ensure

information privacy. An AEC-700 echo canceller efficiently suppresses the echoes caused by satellite communication.

The NESPAC system offers a panorama of C&C technology. From the camera to the satellite transponder, from the earth station equipment to the 100-inch video projector, virtually all elements of the system are NEC products.

NEC is a leader in long-distance education systems using communications media including public telephone networks, terrestrial microwave systems, CATV fiber optic cables and satellites.

NUMBER 141

FDDI FIBER OPTIC TRANSCEIVER.

The American National Standard Institute (ANSI) is now compiling the standard for high-speed LANs. Called the Fiber Distributed Data Interface (FDDI), the new standard features a data rate of 125Mbps, 100km network coverage and up to 500 nodes.

NEC's NEOLINK-1312 is designed to meet or exceed FDDI-PMD requirements. The new 125Mbps fiber optic transceiver incorporates a 1.3 μ m LED, PIN-PD and two LSIs. These are the same components used in our 200Mbps datalinks (NEOLINK-2012). Over 60,000 pairs of the 200Mbps link have been shipped since 1985 without a single field failure.

The new NEOLINK-1312 features a transceiver configuration designed for easier mating with an MIC duplex connector. The design eliminates the need to painstakingly align separate transmitter and receiver units on a printed wiring board. Crosstalk and noise problems are also solved with our circuit and isolation expertise.

The NEOLINK-1312 offers an average output power of -16 dBm; average receiving power between -34.5 and -13.0 dBm. It operates on either a single +5V or -5.2 V power supply.



NEW SOLID-STATE TV TRANSMITTERS: UP TO 40KW IN UHF.

Solid-state TV transmitters are fast replacing tube types because they are more reliable, economical and easier to maintain.

The all solid-state transmitters of NEC's new PCU-900 series incorporate the latest semiconductor and RF circuit technologies. We offer five models for UHF broadcasting: 5/10/20/30 and 40kW.

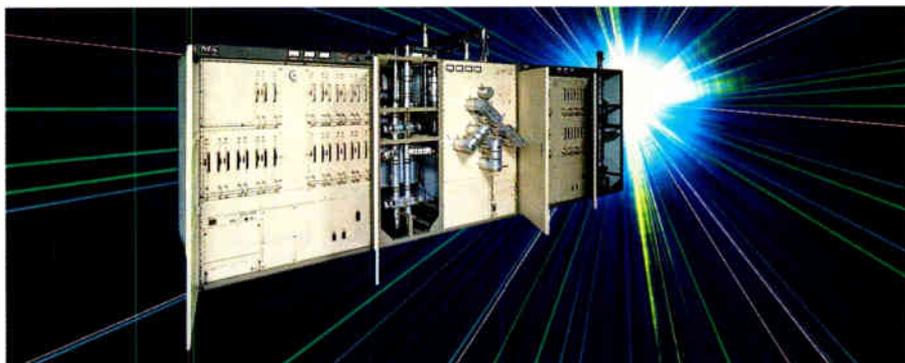
All models use 800W PA modules

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Since the transmitters operate on 28V DC power, they provide greater safety and require less maintenance. Power transistors are efficiently cooled by our "Jet Air Cooling" system.

NEC also supplies a series of fully solid-state transmitters for VHF broadcasting. Our PCN-1400 series has five models: 5/10/15/20 and 30kW.



VAST LIBRARY SYSTEM FOR CHINA.

NEC is supplying a large-scale information system to the National Library of China (NLC) in Beijing. With over 14 million volumes in its collection, the NLC is one of the world's largest libraries.

The library system for the People's Republic of China consists of two mainframes for database management and 270 personal computers for terminal applications. The system will handle 56 languages and allow retrieval of millions of books in each language

by category and author listing.

The NLC and NEC are jointly developing Chinese-language software for the system. The software will meet China's new national standard of 32,000 characters. The library system will be in full-scale operation in mid-1991.

Since the NLC is one of China's academic centers, it will use the system in the future as the core of a network linking thousands of libraries around the country.

NEC

Signetics 68070
Moto dives into RISC chip pool

NEW YORK—Motorola finally takes its plunge into the RISC pool today as it announces its long-awaited 68070 chip set. More...

chip from a semiconductor manufacturer to find a place in the computer and workstation world. Major system companies are pushing the RISC theme with own architectures, shutting the door on standard products...

Intel unveils long-awaited 386 coprocessor control chip

Intel Corp. of Santa Clara unveiled on Thursday its long-anticipated 'P-9' computer chip, which will create less expensive personal computer systems that run more sophisticated software.

Introduction of the new 80386SX chip, which analysts say eventually will supplant Intel's widely used 80286 chip as the "brain" of certain IBM PC and compatible computers, essentially is a marketing move that allows computer makers to offer lower-cost alternatives in their high-powered 80386-based product line.

For example, prices of coprocessors—like the IBM 80286—range from \$4,500. Systems based like the IBM Model 4 chip—start at about \$10,000. The 80386SX will run all the software of the 80286—although more slowly. The new chip also will run 80286 software, Intel said. While analysts said they expect...

Advanced Micro Devices positions its 29K for the embedded micro market

AMD, with its new 29000 microprocessor, probably the most recent addition to its embedded microprocessor line...

386

Although National Semiconductor's NS32532 microprocessor has a dedicated math coprocessor (the NS32380), its 1-MFLOPS floating-point calculation speed is deemed too slow for many tasks. To meet speed demands, National came up with the NS32580, a dedicated coprocessor-control chip that ties Weitek's WTL3164 fast floating-point data path in the 32-bit NS32532 microprocessor. The combination yields a peak floating-point performance of 15 MFLOPS for single- and double-precision tasks.

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PACIFIC RIM TRENDS

FUJITSU AND HITACHI PLUG AWAY AT JOSEPHSON-JUNCTION WORK

It is unlikely that those odd ducks of the semiconductor barnyard, Josephson junction processors, will be the basis of a complete superconductive system any time soon. Moreover, the difference in temperature and the long leads between the liquid-helium environment and semiconductor processors create a time delay that makes JJs difficult to use where data must be exchanged with semiconductor circuits. However, none of this would be a problem in applications such as code conversion in multigigabit/s communications circuits. The JJ could also be used as a form of front- or back-end processor for another computer. For those reasons, development work continues, and researchers at Fujitsu Ltd. and Hitachi Ltd. are reporting progress. Those at Fujitsu have built a JJ processor with a 4-bit microprocessor core logically equivalent to the Advanced Micro Devices Inc. 2901, a 4-bit-by-4-bit multiplier, a 12-bit accumulator, an 8-Kbit program read-only memory, and a sequencer. The chip has 24,000 Josephson junctions fabricated in 1.5- μm -diameter niobium aluminum-oxide niobium technology. Fujitsu says it will take three to five years to develop a prototype. At last month's International Solid State Circuits Conference in New York, Hitachi reported on a JJ processor, but with a lower level of integration and a lower speed. It uses technology similar to Fujitsu's but has 2.5- μm features. □

THE JAPANESE BUILD A SMALLER SYNCHROTRON FOR X-RAY LITHOGRAPHY

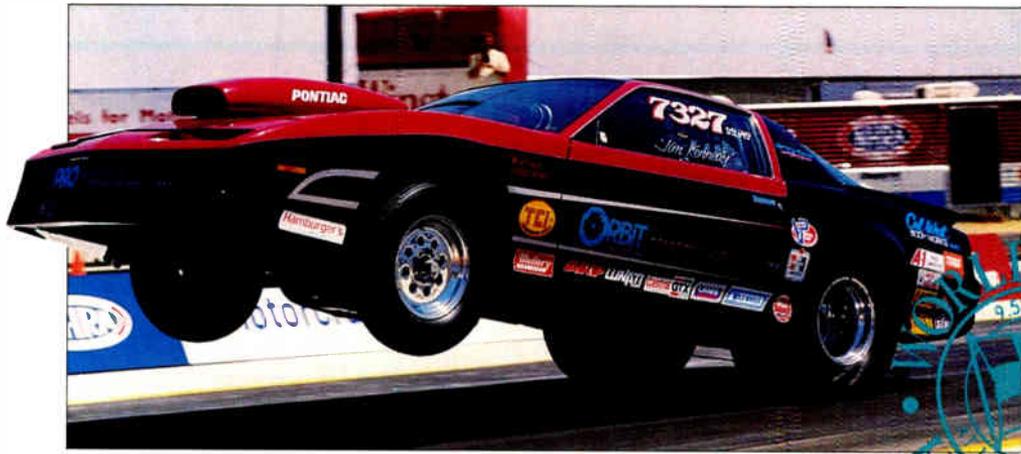
Japanese researchers now have a working synchrotron storage ring with superconducting magnets that's almost small enough to be used on a fabrication line for ultralarge-scale integrated circuits. The new storage ring provides the 7 Å unit-peak soft X-rays needed for lithography to fabricate devices with 0.2- μm or smaller design rules. The racetrack-shaped ring is at a Nippon Telegraph & Telephone Corp. office in Atsugi. At just 2.5 by 8 m, it accelerates electrons to the required 600 million electron volts, and the associated linear accelerator that injects electrons into the ring is only 1.7 m long. The normal-temperature-magnet ring the facility has used until now measures 15 by 15 m. □

SONY CHALLENGES SVHS WITH BETTER RESOLUTION IN 8-mm VCRs

Smaller is getting sharper in video-cassette recorders. Sony Corp. next month will start sales in Japan of a "high-band" 8-mm camcorder and video deck that offer the high horizontal resolution of more than 400 TV lines despite the small tape size. Resolution is comparable to the increasingly popular SVHS format (developed by Victor) and to studio equipment. The high-band format was adopted by 10 companies in March 1988. For high-band use, Sony will sell precision cassettes with two new types of tape, both of which record the TV signal in a semiperpendicular mode with a minimum wavelength of 0.49 μm . Evaporated-metal tape, said to be the first for video use, has a signal-to-noise ratio 5 dB higher than former tapes. □

NTT DATA AND NISSAN TO START SMART-CARD COMPANY

NTT Data Communications Corp. aims to ramp up the Japanese smart-card market in cooperation with giant auto manufacturer Nissan Motor Co. Ltd. of Tokyo. NTT Data, also in Tokyo, is the company recently spun out from Nippon Telegraph & Telephone Corp.; with Nissan it will establish a company in Tokyo in May to make the cards. The joint venture, whose name has not been chosen, will be capitalized at about \$4 million—90% from Nissan and the rest from NTT Data. Its aim is to market a card developed by NTT Data that will target the owners of Nissan's vehicles. □



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EUROPEAN OBSERVER

WEST GERMANY STARTS HOOKING UP ISDN ON A LARGE SCALE

Without much fanfare, West Germany's communications authority, the Bundespost, is introducing integrated services digital networks on a large scale. During the past few weeks, partial networks have started operating in Düsseldorf, Frankfurt, Hamburg, Hanover, Munich, Nuremberg, Stuttgart, and West Berlin. The Bundespost figures it will be offering ISDN service nationwide by 1993. In the meantime, the West German communications industry is bracing itself to handle the rising demand for terminal equipment that ISDN will create. The Bundespost is prepared to give up its monopoly on subscriber terminals by the middle of 1990, which will open the door to inexpensive hardware from the Far East and will spark fierce rivalry in the marketplace. To meet the competition, small West German equipment makers who now enjoy a secure market with one powerful customer, the Bundespost, are forming co-operatives to work on development and marketing strategies and to buy components in bulk. □

EUROPEAN PROJECT COMES UP WITH A BREAKTHROUGH TV SCREEN

Finland's Lohja Corp. is ready to produce a monochrome flat-screen TV with a 12-in. electroluminescent screen. The event marks an important milestone in the European Community's RACE program, for Research and Development in Advanced Communication Technologies in Europe. The screen, including the electronic circuitry behind it, is only 54 mm thick. That means it can be used to make radically different TV sets—models that can be hung on a wall, for example. The screen is the largest developed so far using EL technology, claims Jorma Antson, marketing manager for flat screens at Lohja's Finlux division. The monochrome prototype runs off a 12-V dc power supply and consumes only 20 W. Images are built up from sizes of 200 by 384 pixels, each pixel measuring 0.6 by 0.6 mm. The project's goal is a color version of the set, with commercial products available by the second half of the 1990s. Besides Lohja, the RACE participants include France's Matra Communications, the Italian-French combine SGS-Thomson Microelectronics, and the University of Ghent in Belgium. □

TEXAS INSTRUMENTS BUILDS A WAFER PLANT TO HANDLE PAN-EUROPEAN CHIP DEMAND

Texas Instruments Inc. is getting ready for increased chip demand when Europe 92, the tariff-free, unified European market, opens up. TI is building a wafer-production plant in Avezzano, 60 miles east of Rome, at a cost of \$250 million. The plant should begin operating by the end of next year and working at full capacity by the middle of 1991. It will employ more than 500 people, who will turn out MOS integrated circuits, including dynamic random-access memories. Production will begin with 4-Mbit DRAMs; advanced MOS logic ICs will eventually follow. □

PROJECT AIMS FOR A 1-GIPS OBJECT-ORIENTED COMPUTER

Work is starting on a pan-European project called Tropics, for transparent object-oriented parallel-computing system, a machine intended to run more than a billion instructions per second. The project is scheduled to take five calendar years and about 700 man-years to complete, with the first phase taking some 210 man-years to produce a prototype. The finished Tropics will be made of hundreds of processors operating in parallel and is intended as a server on local-area networks handling complex office applications. Philips International NV of the Netherlands heads the project. Participating firms include France's Thomson-CSF, Italy's Olivetti, West Germany's Nixdorf, and a number of universities and research institutes. □



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Design Turn: 14 weeks.



Photos: David Samoff Research Center

U.S. GROPPES FOR

Where there's a will, there's a way, the old adage goes. But one of the hottest questions of the day is whether the U. S. can find either the will—or the way—to pull off a seeming miracle in high-definition television. Having all but ceded the consumer electronics business to the Japanese and other foreign producers more than a decade ago, the U. S. electronics industry now says it's time to get back into the game.

The point of attack: HDTV. "We'd like to see some of our companies return to the [consumer] fray, to see some of our personal-computer companies or some of our new companies get into it and compete on a fair basis, coupled with fair-trade practices," says J. Richard Iverson, president of the American Electronics Association, which is leading the HDTV assault. A strong U. S. presence in HDTV development and manufacturing will be crucial to future U. S. competitiveness up and down the whole electronics "food chain," the AEA contends, from key segments such as personal computers right down to base semiconductor technology.

It won't be easy. The U. S. faces well-entrenched foreign competition that already controls about 87% of the U. S. TV market and is well ahead in HDTV development. Only in the past year or so have American interests launched a frantic ef-

fort to get an HDTV game plan in place. Most agree that some form of government participation will be essential for success. But so far, the debate has produced little beyond evidence of widespread disagreement among a multitude of competing domestic and foreign interests, each pushing its own view of how HDTV should be developed and deployed.

"What we lack is a coherent national strategy," says Rep. George Brown Jr. (D-Calif.), senior majority member on the House Science, Space, and Technology Committee. Some, in fact, question whether divergent U. S. interests can muster the cooperation necessary to put a single HDTV plan together and then carry it off successfully. Others doubt that even the best-laid plan would be enough. "We're trying to make up for a 15-year hiatus in consumer electronics, and it's likely to be an impossible task," says an executive at one U. S. chip house.

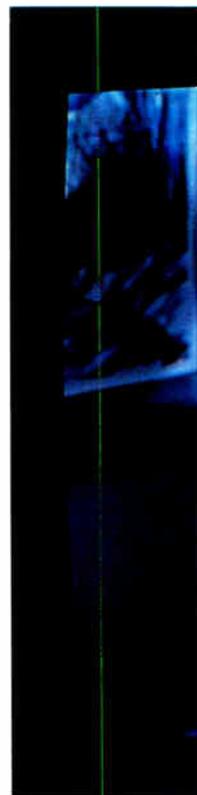
Still, many feel the U. S. must make the effort. As the third generation in consumer television, HDTV promises revolutionary changes in home entertainment rivaling those produced by the advent of monochrome TV in 1939 and color in 1954. Directly at stake economically is what could become a \$20 billion to \$40 billion worldwide market in HDTV receivers by the year 2010. But for U. S. chip and computer makers, the issue involves much more.

by Wesley R. Iverson

Because HDTV receivers and video-cassette recorders will gobble up vast amounts of digital memory and logic circuitry, many believe HDTV will drive technology in advanced semiconductors, high-resolution displays, and other technologies. And ripple effects will be felt across virtually every segment of the worldwide electronics industry.

"We're not talking small potatoes here," says William Schreiber, director of the Advanced Television Research Program at the Massachusetts Institute of Technology's Media Laboratory. "If HDTV really develops and proves to be popular with the public, it will be the largest consumer of memory chips and the largest consumer of microprocessors—bigger than the computer industry and bigger than industrial electronics."

The AEA goes further. In a nutshell, the Santa Clara, Calif.-based trade group believes that if the U. S. cedes HDTV-receiver production to Japan and others, it risks becoming a second-rate technology player. Advanced digital circuitry for HDTV will find its way into computers, telecommunications, and other markets. If HDTV development and production oc-



U. S. electronics interests are scrambling for position in what could be a make-or-break effort. 'HDTV is more than just another TV set,' the AEA warns

UNITY ON HDTV



cur offshore, U. S. chip makers will find themselves in an increasingly weak position to sell into overseas markets or into products built in the U. S. by foreign manufacturers, the reasoning goes.

What's more, high-resolution flat-panel and cathode-ray-tube display technology developed for HDTV will find applications in defense, medical imaging, and computers, among other segments. As sophisticated HDTV products gain more and more processing power, they will begin to compete with PCs and work stations, some experts believe. And if the Japanese

have a dominant HDTV position, they will leverage the volume to take PC market share from the U. S., the AEA warns.

According to a working document issued by an AEA task force late last year, if the U. S. settles for controlling less than 10% of worldwide HDTV production, it stands to lose half of its current world-market share in semiconductors and PCs. To merely maintain its current share in both of these key segments and others, the U. S. needs to capture half or more of the HDTV manufacturing base, the AEA contends. In short, "HDTV is more than

just another TV set," says Iverson.

Not all, of course, subscribe to the AEA line. "There's almost an HDTV hysteria today," says Larry French, a corporate vice president at North American Philips Corp., the New York-based arm of Philips International NV of the Netherlands. "It's becoming a symbol of what's wrong with the U. S. and [with] U. S. competitiveness." And the Electronic Industries Association—a Washington trade group with membership that includes foreign-owned consumer manufacturers—challenges many of the AEA's conclusions. The focus should not be on who owns the HDTV manufacturing, the EIA says, but rather on assuring the maximum number of U. S. jobs in HDTV production, research, and development.

But the AEA view is one that many in industry and government seem increasingly to be rallying around. Even the Pentagon is getting into the act. The Defense Advanced Research Project Agency is planning later this year to award \$30 million in HDTV development funding aimed at display and video-processor technology. Bids on that effort were due Feb. 27.

The House of Representatives, meanwhile, is holding hearings on HDTV competitiveness, with an eye toward finding what's needed to foster a U. S. technology thrust. The idea of a consortium similar to the \$100 million Sematech chip effort is being floated around. And now a special Commerce Department advisory committee has come out with a preliminary report stating that "lack of significant U. S. participation [in HDTV] would exacerbate the already dwindling U. S. industrial base in consumer electronics and adversely affect U. S. semiconductor, computer, and related industries."

In any effort to gain a major stake in the HDTV business, the U. S. is starting

out way back in the pack. The big Japanese and European consumer-electronics makers already own most of the TV manufacturing plants in the U. S. and have well-oiled marketing and distribution systems in place. Zenith Electronics Corp. of Glenview, Ill., is the last remaining domestically owned TV manufacturer, and its consumer operations have been under heavy financial pressure.

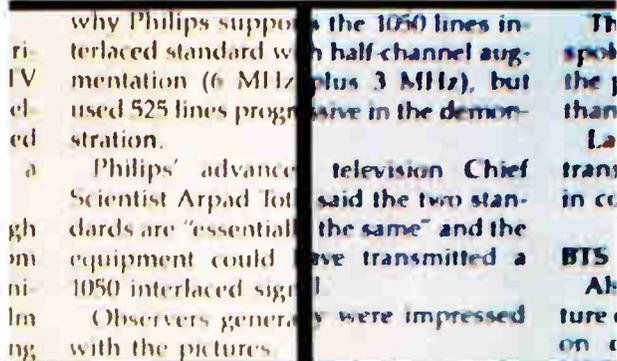
What's more, both Japan and Europe have a big lead over the U. S. in HDTV technology. The Japanese have spent around \$700

million on HDTV over the past two decades and will begin direct-broadcast-satellite HDTV transmissions to their home market next year. They will use the MUSE (for Multiple Sub-Nyquist Encoding) system developed by Japan's public broadcasting system, NHK.

The Europeans likewise have banded together in an organized effort and are spending \$200 million to \$250 million a year on HDTV in the pan-European Eureka project. Satellite broadcasts of a wide-screen 625-line version of the Multiplex Analog Component (MAC) format are expected to begin in 1992, with full-service European high-definition MAC broadcasts following in 1997.

The U. S., by contrast, has not even selected a transmission standard yet.

The Federal Communications Commission narrowed the field somewhat last fall, declaring that any broadcast-transmission scheme chosen must be compatible with the current 6-MHz National Television System Committee (NTSC) standard, while also fitting within the current frequency-spectrum space allotted to VHF/UHF NTSC broadcasts. That



Improved sharpness shows when a standard NTSC image is compared to one from North American Philips' HDS-NA system.

knocked out several systems, most notably Japan's MUSE, which requires an 8.1-MHz channel. But it still leaves the FCC with about 20 HDTV transmission schemes to choose from, submitted by both foreign and domestic concerns.

The FCC hopes to choose a U. S. standard within two to three years (see story, below). And as the commission narrows down the list of formats under consideration, the selection process is likely to be a high-profile issue. It has implications for a variety of heavyweight interest groups, including the broadcast, cable-TV, telephone, satellite, and fiber-optics industries, among others.

Indeed, the battle over when and how HDTV is delivered to American homes could have a significant impact on the nation's information-delivery infrastructure, says Jeffrey Hart, professor of political science at Indiana University and a visiting researcher at the Berkeley Roundtable on the International Economy, a research arm of the University of California at Berkeley. Because of its high-bandwidth advantages, fiber is increasingly seen as the logical solution.

will ultimately be developed for the different delivery media. And that prospect has led MIT's Schreiber to propose that HDTV receivers be built using an open, bus-structured architecture that could be easily adapted to a range of transmission formats, without requiring set-top converter boxes. Instead, the consumer would plug hardware cards directly into the HDTV receiver's common bus, much as PC users plug in expansion cards today. Such an "open-architecture receiver" could be readily expanded to connect a wide range of other units, including VCRs, optical disks, computers, video games, and electronic still cameras, Schreiber says.

NOT OPEN. But the concept has gone over like a lead balloon at the EIA. "There is already such a low degree of profitability in TV sets today," says Thomas Friel, vice president of the EIA's consumer electronics group, and TV makers are not interested in opening the HDTV set up to third-party hardware and software developers. Besides, he adds, an open architecture would be too confusing for consumers.

For its part, the EIA has proposed a

WHEN WILL WE SEE HDTV? DON'T HOLD YOUR BREATH

One day there will be a single U. S. standard for high-definition television, and the marketplace will be able to move forward with hardware and programming for the consumer. The only question is: when?

The Federal Communications Commission, which will have the final say on a broadcast standard, originally sought to settle the issue by 1990. It's now likely, however, that a standard won't be chosen until late 1991 or 1992. The initial optimism with which those backing HDTV formats promised short-term delivery of hardware prototypes has since given way to caution: the stakes are too high to risk compromising a system's chances by rushing it to test.

Even the Advanced Television Test Center, a private entity formed last year by a number of broadcast organizations

to test the 20 proposed formats on the FCC's behalf, has been delayed. The Alexandria, Va., facility will act as the eyes and ears of the FCC, testing proposed systems and helping to recommend which

The FCC wanted a standard by 1990; now it's 1991 or later

should become the standard. Early plans called for the center to start testing prototype hardware late last year or early this year, but now it appears the facility won't even be set up until autumn.

"There's no point in setting up a testing facility until you've got something to test," says Ben Crutchfield, program offi-

cer at the center. The center's staff is now busy trying to develop and publish the test procedures so the proponents will know what to expect. "It's moving about as quickly as it can," Crutchfield says.

"The original time was unrealistic scheduling," says William Hassinger, assistant chief for engineering of the FCC's Mass Media Bureau. "Everyone is finding out just how much there is to be done. A lot of the proponents, as they approached the big test, decided they wanted to be darn sure they were ready. There's too much at stake."

Once the center begins work late this year, the process will be slow, and unless a fair number of proponents drop out, it could take well over a year to complete the task. Only then can an FCC subcommittee analyze the results and make a recommendation to the FCC itself, and in-

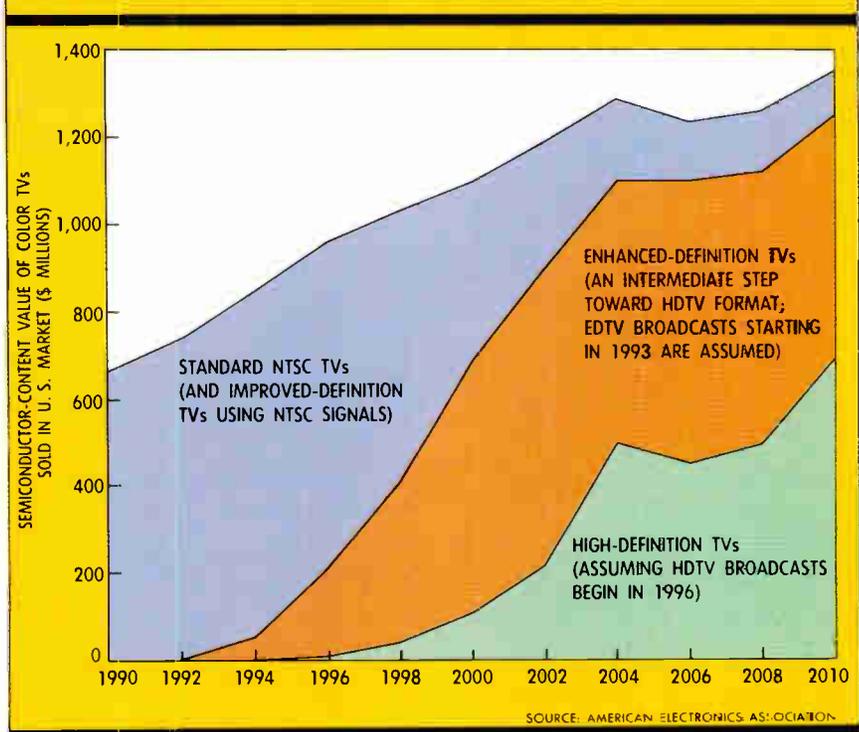
standard "multiport" receiver with two inputs—one UHF/VHF for NTSC signals, the other a baseband port for HDTV. The baseband port could handle multiple standards for various media as long as those standards shared a "friendliness," or commonality, in certain baseband characteristics, such as frame rates, field rates, and aspect ratio.

This intense interest in multiple media stems from HDTV's potential to revolutionize home entertainment. HDTV receivers will display twice the horizontal and vertical resolution of today's NTSC sets, with 10 times the color-information detail, producing a picture quality equivalent to that of 35-mm movie film. It will deliver a cinema-like wide-screen picture, with an aspect ratio of 16:9 or 5:3, compared with the 4:3 NTSC standard. Multichannel wideband audio will round out the package, delivering crystal-clear stereo hi-fi sound, equivalent to that of a compact disk.

All this comes at a price: HDTV receivers will sell initially for \$2,500 to \$4,000 at retail. And there is always the chance that U.S. consumers won't take to the technology in sufficient numbers to drive volume pricing and create a mass market.

But based on an assumed \$2,500 retail starting price, the EIA is predicting rapid penetration, with 10% of U.S. households owning one HDTV set four years after introduction. That would be a higher acceptance rate than for either color TV or VCRs. The EIA projects that Americans will buy 13 million HDTV receivers in the year 2003, 92% of which will be manufactured in the U.S., employing 232,000 workers and contributing \$23 billion to the gross national product. The AEA is more conservative. It projects U.S. sales at 4.9 million units in 2003, producing a \$2.8 billion market. The numbers climb to 11 million units

A HUGE CHIP MARKET FOR HDTV



and \$6.6 billion by the year 2010.

Because no single U.S. firm would be likely to take on the high risk and expense of HDTV development and manufacturing on its own, most in the AEA camp agree that government involvement is a requirement. But what form that might take is still anyone's guess.

It might include new types of industry and government-industry consortiums. And it might include any combination of federal loan guarantees, tax breaks, relaxation of antitrust laws, new trade regulations, or stricter enforcement of the

antidumping laws already on the books.

Not surprisingly, U.S. executives of foreign-based firms are playing down the need for a big federal spending program. "HDTV is really just a small part of a much larger problem," says French of Philips. Japanese companies dominate consumer electronics not because of technological superiority, he says, but because U.S. companies chose not to compete in an arena of low profit margins. "I see no reason to expect that this will remain anything but a competitive business with small profit margins. To see HDTV

siders say those two steps alone could easily take another year or more.

"It could still happen in 1991," says Robert Hopkins, chairman of the FCC subcommittee and executive director of the Advanced Television Systems Committee, an industry group. "It's all going to depend on how long the testing takes and how many systems are built."

Of the proposals vying for attention, experts say some will not be built, some will not work, and others may ultimately be ruled out because they do not offer compatibility with current NTSC TVs. The rest will be judged on moving- and still-picture quality, the robustness of their transmission signals, cost, and other factors that Hopkins says have yet to be determined.

Many in the electronics industry have worried aloud that a delay will allow the

Japanese and Europeans to get an early lead—or even to force a de facto standard on the U.S. Others disagree. If anything, they say, a delay may strengthen any fledgling consortium's effort to establish itself before consumer demand reaches a fever pitch.

As for the specter of other media launching independent drives into HDTV, that's not likely to happen any time soon, says the FCC's Hassinger. "Cable is playing it very cautiously. They carry broadcast programming, and consequently one has to make sure everything fits. They don't want to have to carry different kinds of signals, and there is a question as to whether one could carry different kinds of signals and still have an operating system," he says.

Further, cable-TV operators, though tempted, will not push ahead of their

broadcast counterparts, on whom they depend for programming. They are afraid that if they guess wrong, their investment in an incompatible HDTV system would wash away in an instant. As for satellite alternatives, as long as the FCC can set a standard in the next two to three years, most experts don't think there's anything to worry about.

But "if broadcasters have to mess around for another five years, some other media, such as satellites, could come along with a system that is not broadcast-compatible," says James E. Carnes, vice president for consumer electronics and information sciences at the David Sarnoff Research Center in Princeton, N. J. The center, with assistance from NBC and Thomson Consumer Electronics Inc., is one of the proponents hoping to set the standard (see p. 76). —Tobias Naegle

as a panacea for the U. S. trade problem is unfounded," he says.

That mirrors the EIA stance. The group believes that the U. S. could have ample participation in HDTV manufacturing and R&D through foreign-owned companies that build TVs in America. According to EIA figures, there are 35 TV and TV-component factories in the U. S., 32 of which are foreign-owned. France's Thomson Consumer Electronics Inc. (RCA and GE brand names) and the Dutch giant Philips (Magnavox, Sylvania, Philco, and Philips), in particular, do extensive R&D in this country.

Given the way things stand, EIA president Peter McCloskey is more than skeptical of AEA goals. "It is the right time for companies who are considering it to get back into the [consumer-electronics] business," he allows. "But I think there's also got to be some reality to it. Today, the largest single Japanese company in the U. S. market is Sony at 6.5%." For a new U. S. entry to reach the AEA's 50% penetration goal "would be rather startling," he says.

But John F. Mitchell, vice chairman of Motorola Inc. in Schaumburg, Ill., for one, believes that the rebirth of mass-

market consumer manufacturing is possible here. A 50% HDTV market share "would be accomplished very easily if the U. S. government got behind an effort to change some regulations and enforce others," Mitchell says. What's needed, in particular, is a pledge from the government to enforce antidumping laws on HDTV, he adds.

Motorola is one of 16 U. S. firms participating in an AEA-sponsored "partnership." Formed in January, it will study ways of ensuring major U. S. HDTV participation [*Electronics*, February 1989, p. 65]. The effort could lead to the formation of a government-funded industry consortium aimed at HDTV product development—or even manufacturing, if appropriate anti-trust exemptions could be obtained.

The membership list is impressive. Besides Motorola, it includes Apple, Digital Equipment, Harris, Hewlett-Packard, IBM, Tektronix, and Texas Instruments, among others. Each kicked in about \$5,000 for the study effort. Zenith is supporting the work in principal, but is not contributing any funding.

Significantly, the AEA did not invite participation by foreign-owned firms. And at Thomson Consumer Electronics in

Indianapolis, vice president D. Joseph Donahue says he is concerned.

"One of the little things I worry about is that if the U. S. does the wrong thing, it will discourage all the people who have R&D here now," he says. "Say there is a consortium formed, or there's a Darpa contract, or just a contract. If you exclude Philips and Thomson, you give them great encouragement to do more with European or Japanese semiconductor houses. One of your goals is to save the U. S. semiconductor industry—and that's the way you're going to do it?"

CAN'T WAIT. If the issue does come to federal funding, Donahue says he'd favor a small, one-by-one contracting approach with innovative U. S. laboratories over a Sematech-style consortium. "If we had to wait to form a Sematech [for HDTV], we'd all be out of business" by the time it got started, he says.

But unless things change, an HDTV version of Sematech may not be a concern. Despite House interest, a consortium is an unlikely proposition, says one Senate aide familiar with the issue. "The Sematech people had their act together. But the TV industry, or the electronics industry, hasn't come together," the aide says. A unified front—an entire industry speaking as one—is key, says the aide, and that looks virtually impossible, given the divergent opinions of the AEA, the EIA, and other competing interests.

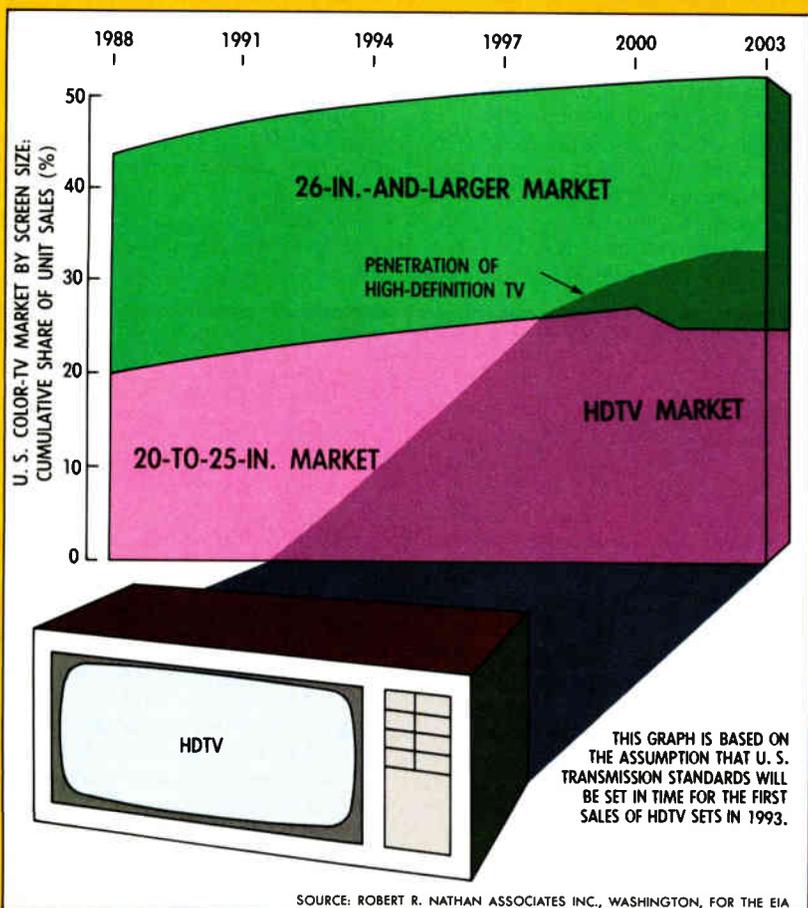
But some sense a shift in the political winds. "Initially, the AEA was saying it had to be U. S. firms only," says Hart of the Berkeley Roundtable. "But the AEA is now beginning to move toward the possibility of foreign participation." Hart has seen the issue from both sides: he helped the EIA prepare Congressional testimony and he served as a member of the AEA Task Force on Advanced TV.

"What I've seen recently is a lot of desire on everybody's part to make sure that the different organizations don't cancel each other out," he says. "They all see it as an opportunity to get some interesting policies out of the government. But they also see a possibility of getting some stupid policies. What they're trying to do at this point is get their act together across the organizations."

Until the AEA-commissioned study is completed, most in the AEA camp decline to speculate on any next step. But there are all kinds of ideas floating around. "Maybe the consortium ought to buy back RCA from Thomson," muses a high-ranking executive at one U. S. firm. "The consortium concept would have difficulty if it were only built around Zenith, with just 13% of the TV market. Combined with RCA, though, they'd have a base to shoot for a 50% share in HDTV."

Whichever direction the development efforts take, it's clear that an increasing number of heavyweight computer and

HDTV WILL PENETRATE THE BIG-SET MARKET



semiconductor houses are taking a serious interest. Digital Equipment Corp., for example, is doing "a tremendous amount of HDTV-related R&D, in both hardware and software, encompassing video displays, semiconductors, and private and public networks as transmission media," says Bruce Holbein, DEC's manager for government relations in Maynard, Mass. And in Berkeley Heights, N. J., Daniel Lankford, vice president of market development for AT&T Microelectronics, says, "We fully intend to be in the business of providing HDTV chip sets and subsystems. We are beginning to do some work now to define what those chip sets might be."

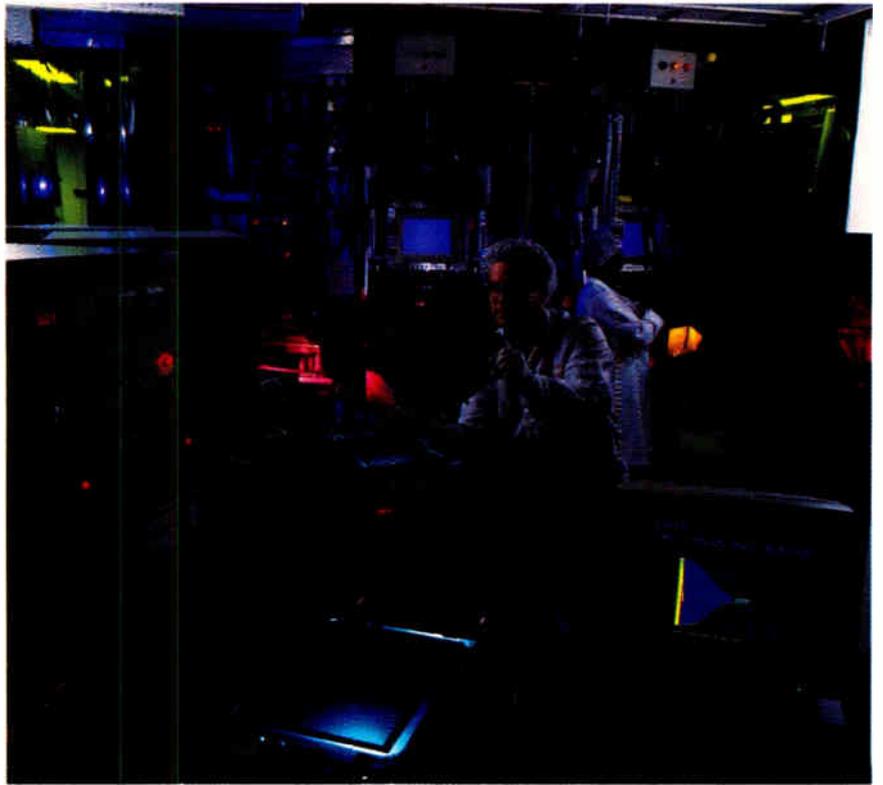
Another reason for the interest is that as HDTV dawns, consumer television sets are suddenly starting to look a lot more like computers. Some Japanese HDTV receivers already include up to 40 custom integrated circuits, and the typical Japanese TV in the 1990s may contain 1 or 2 Mbytes of video random-access memory.

Future HDTV sets will be able to connect to 100 Mbytes of data storage as well as to printers, facsimile machines, telephones, and a variety of other gear. And they will be two-way interactive, permitting delivery of a variety of services via wide-bandwidth cable or fiber.

"What we're seeing is a coming together of TV and computer technology, and at some point the distance between HDTV and midrange computing really blurs," says Barry Whalen, a vice president at Microelectronics and Computer Technology Corp., the Austin, Texas, research consortium. "That's why we're interested, and that's why Darpa's interested." Whalen "absolutely" sees HDTV as competing against PCs and work stations, and having a big impact on the way computing is sold 10 to 30 years from now.

And computer makers can't afford to overlook the threat, he says. "Every time a technology has changed the way people buy computing, a different set of companies came to the fore." The consortium, in fact, is talking to members about starting a research program next year to focus on what Whalen calls "HDTV in the large." The group would explore ways in which very large HDTV flat-panel displays might one day be used as a kind of "artificial reality"—as a "synthetic window" in the home, for example, or in cockpitlike simulators that consumers might use as a substitute for travel. The concept might also tie into HDTV's built-in processing power and rely on artificial-intelligence techniques for a variety of user-assisted information-gathering and entertainment functions, Whalen says.

Apple Computer Inc., for one, has seen the vision. The Cupertino, Calif., firm recently produced a videotape of how a fictional system it calls the Knowledge Navigator might one day be used in tying computers and HDTV video and graphics



'What we're seeing is a coming together of computer and TV technology—the line between them blurs'

together. In the video, a professor interacts with a notebook-sized computer and a large flat-panel HDTV to prepare a lecture in a matter of minutes. The HDTV display is used to show charts, graphics, and maps generated by the computer on demand, and as a videophone when the professor makes calls to other researchers around the world.

"The tremendous interplay between HDTV and computers is already obvious," says James Groell, vice president for special projects at PCO Inc., a Chatsworth, Calif., optoelectronics firm. Some work stations already have near-HDTV quality, and there is no reason to believe it will not be demanded by computer displays of all types when HDTV broadcasting starts in the 1990s, Groell says.

Indeed, the technology will lead to much lower-cost high-resolution screens than those found on today's high-end graphics work stations, say executives at Hewlett-Packard Laboratories in Palo Alto, Calif. HDTV technologies such as displays, memory, and signal-processing chips will drive developments in computers, test equipment and other industrial

markets, and military gear, HP says.

Despite the HDTV interest at many big firms, some companies are still holding back. Chip maker Intel Corp. of Santa Clara, Calif., for example, says it has no interest in the business. Likewise Compaq Computer Corp. in Houston. "We're in the mainstream, high-end market," says a Compaq spokesman. "Until any of that [HDTV technology] becomes something where there's higher, broader market demand, the chances are you won't see it from this company."

For those who do hope to participate, most agree on one thing. As Motorola's Mitchell puts it: "The most important question of the day is, 'Which standard?'" Until the FCC decides, the design of HDTV chips and receivers for the U. S. market can't begin in earnest. And in the best-case scenario, U. S. HDTV broadcasting can't begin until 1993.

But some see that time lag as propitious. "The U. S. does have some advantages. This will be our standard. We can set it when we want," says AT&T's Lankford. And by giving the now fractious factions more time to close ranks, it could result in a more measured U. S. plan in any forthcoming manufacturing venture, many believe. "The U. S. has the laboratories for research, the displays, the chips, and the assembly capability," says Groell at PCO. "Technology is not the problem. It's having the will to do it."

Additional reporting by Lawrence Curran, Jonah McLeod, Tobias Naegele, Jack Shandle, and Larry Waller

ACTV TAKES A TWO-STEP PATH TO HIGHER DEFINITION

Amid all the hoopla surrounding HDTV, it's easy to lose sight of one fact: there are already more than 140 million TVs in U. S. homes, and the Federal Communications Commission wants to make sure they won't be made obsolete overnight. So any new TV standard will have to be compatible with existing NTSC signals and hardware. And that, say scientists at the David Sarnoff Research Center, is what Advanced Compatible Television is all about.

ACTV is not, in fact, a full high-definition system, but rather a two-step approach to putting HDTVs into America's living rooms by the turn of the century. ACTV 1 offers enhanced definition—480 lines versus the 350-line resolution of conventional pictures—and a wider screen with an aspect ratio of either 16:9 or 5:3, as opposed to today's boxlike 4:3. The system is fully NTSC-compatible and the signal fits within a single NTSC channel. The second stage, ACTV 2, will build on the initial system by transmitting additional detail once more spectrum becomes available.

The brainchild of the same Princeton, N. J., lab which, as RCA Laboratories, pioneered TV in the 1930s and color TV in the following decades, ACTV is being billed as the thinking-man's choice for a U. S. standard. The idea is to give viewers a near-HDTV-quality picture in the 1990s, while industry tries to develop afford-

able, large-screen displays and government wrestles with the regulatory problems of reallocating spectrum.

"Even if you could deliver full HDTV to the home tomorrow, most people just wouldn't be able to see it," says James E. Carnes, Sarnoff's vice president for consumer electronics and information sciences. "The kinds of displays people can afford to buy for the next five to 10 years are either not bright enough for normal use or are not high-definition-capable."

But that doesn't mean broadcasters can afford to wait. A delay could open the door for some serious competition from either satellite broadcasting or some other source, he says. "Broadcasters have to do something in 1991 or '92. If they've got to wait until 1996, it'll be too late," says Carnes.

To produce broadcast images that can be displayed on both conventional sets and the wider ACTV 1 displays, Sarnoff scientists had to break their signal down into four components, each serving a special purpose and each squeezed as tightly as possible so they could fit into the available 6-MHz channel bandwidth.

They include an NTSC signal, time-ex-

panded to prevent distortion in NTSC receivers, which forms the central portion of the ACTV image; the high frequencies for the left and right NTSC-encoded side panels (which make the picture wider); a signal containing extra horizontal luma detail that is ignored in NTSC systems but sharpens vertical lines and edges shown in the ACTV image; and a vertical-temporal luma "helper" signal that assists the ACTV receiver in maintaining extra sharpness. In addition, the main NTSC signal component includes the time-compressed low-frequency portions of the left and right side panels to produce the wider image.

Next, the combined signal must be encoded to look and act just like a standard NTSC signal if it is to be broadcast or

transmitted by a cable-TV system. Without NTSC encoding, the signal can disrupt transmission signals from adjacent channels or be disrupted by them. "That's the price of being

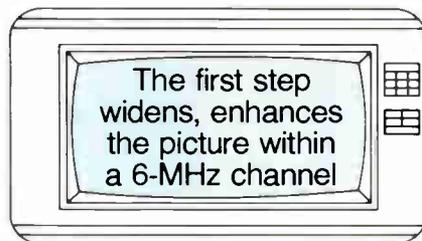
compatible," says Jack Fuhrer, Sarnoff's director of advanced TV research.

To reassemble the four components for transmission, the three supplemental signals must be physically or perceptually hidden in the main signal. Components 2 and 3—the side-panel high frequencies and the extra horizontal luma details—are hidden through compression, so that they are displayed on NTSC sets as complementary color flicker that is imperceptible to the human eye. Component 4, the helper signal, is electrically removed by TV sets with synchronous rf detectors—standard NTSC equipment.

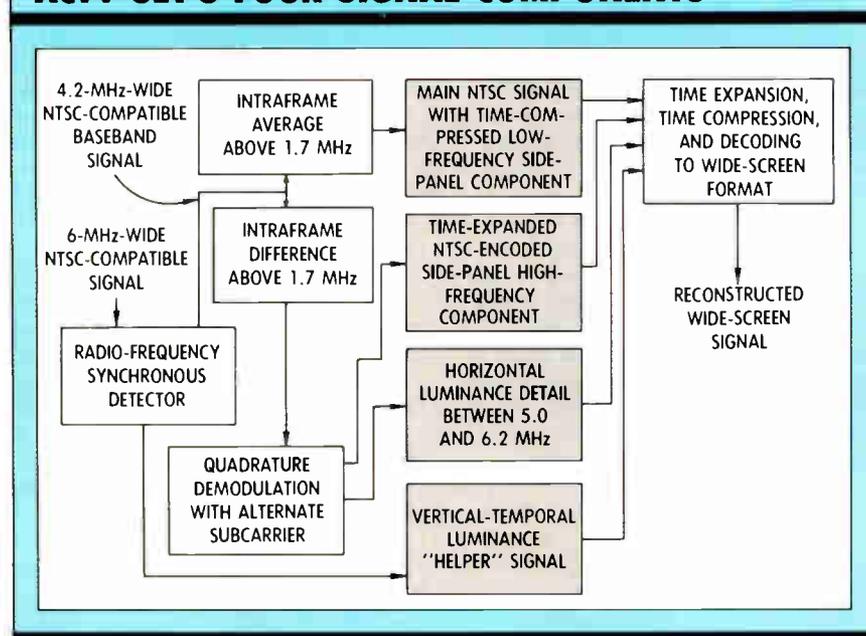
The next hurdle lay in the fact that the signal must go through yet another metamorphosis in order to be recovered as a high-definition signal and displayed as a quality picture on an ACTV receiver. For this task, Sarnoff engineers developed a novel digital filtering technique, called "intraframe averaging." It can separate a modulated signal from a baseband signal without vertical temporal crosstalk.

To avoid a visible seam where the side panels are joined to the central NTSC-compatible image, there is some overlap between what is carried by the central and side-panel components. The receiver then compares the overlap, mixes the results, and produces a "feathered seam." Once that's done, the extended horizontal luma detail is matrixed into the rest of the signal, producing the final image.

The lab is now debugging the hardware and will have demonstration material available by May, Fuhrer says. But it will be November or December before a ruggedized version can make the trip to the FCC's test center. —Tobias Naegele



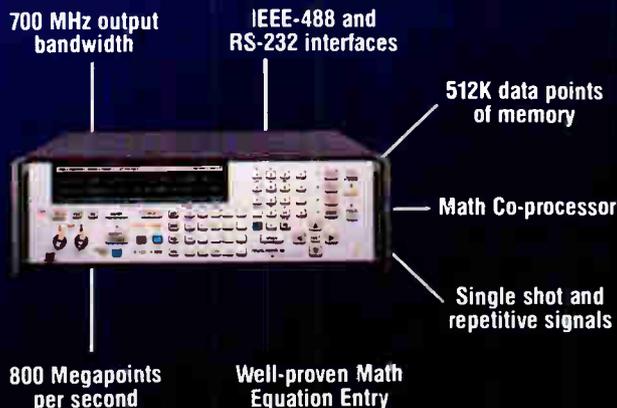
ACTV SET'S FOUR SIGNAL COMPONENTS



The Sarnoff proposal isn't for full high-definition TV, but an enhanced-definition version that relies on breaking a signal into four components that fit within an NTSC channel.

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PHILIPS' SCHEME PACKS PIXELS WITH TIME MULTIPLEXING

Sending HDTV pictures over the stingy U. S. frequency-spectrum allocations for both terrestrial and satellite-TV broadcasting is like packing 10 pounds of pixels into a five-pound bag, and North American Philips Corp. thinks it has an excellent way of doing just that.

Its HDTV technology integrates satellite, terrestrial broadcast, and cable TV into a comprehensive system that features a signal format easily convertible among media. Fully compatible with NTSC signals, it achieves a one-step conversion to HDTV by cleverly interleaving a variety of techniques, including time-division multiplexing, signal sampling, and analog-to-digital conversion.

Conceived and developed at Philips' Briarcliff Manor, N. Y., laboratories, the High-Definition System for North America, or HDS-NA, will deliver wide-screen, NTSC-compatible pictures free of motion artifacts, says C. A. A. J. Greebe, director of electronics systems research. Besides eliminating motion artifacts, which create a jittery picture, another HDS-NA strong point is its pan-and-scan capability, in which the field of NTSC pictures can be selected from any segment of the larger HDTV picture.

Two problems haunt HDTV designs: transmitting the additional information needed to create an HDTV picture, which is wider and has double the resolution of NTSC pictures, over the existing 6-MHz/channel terrestrial broadcast standard; and fitting the information into the satellite system's 9-MHz broadband limit.

HDS-NA accomplishes this in the satellite system by using time-division multiplexing and by sampling the high-resolution signal. Terrestrial-bandwidth problems are addressed by using 3-MHz aug-

mentation channels transmitted in the guard bands between 6-MHz channels.

In the satellite system, Philips has enhanced conventional multiplex-analog-component technology, which separates a single 64- μ s TV scan line into three time intervals. For an NTSC signal, sending a scan line in 64 μ s can be easily accomplished, says Greebe, but the same process for the increased data in an HDTV line would require many more times the



bandwidth than is currently allocated.

Instead of handling each scan line independently, Philips processes the information in groups with four scan lines each, which it calls "Superlines." A 128- μ s "Superline" has five time-multiplexed intervals: normal NTSC luminance data; high-resolution horizontal luminance data; color data; low-resolution vertical-luminance data; and the digital-control and sound data. Sampling proceeds by transmitting the first scan line at NTSC resolution. The third scan line is then transmitted at high resolution—1.5 times NTSC. Information in the second and fourth lines is processed pixel by pixel and transmitted only if it shows a change from line 3.

The HDS-NA terrestrial broadcast system treats an HDTV picture as a normal-size NTSC screen plus two panels, one on either side of the NTSC picture. Information for the NTSC-sized part of the screen is transmitted in the normal 6-MHz NTSC

channel, and side panels are transmitted in a 3-MHz augmentation channel within the 6-MHz guard band adjacent to the NTSC channel.

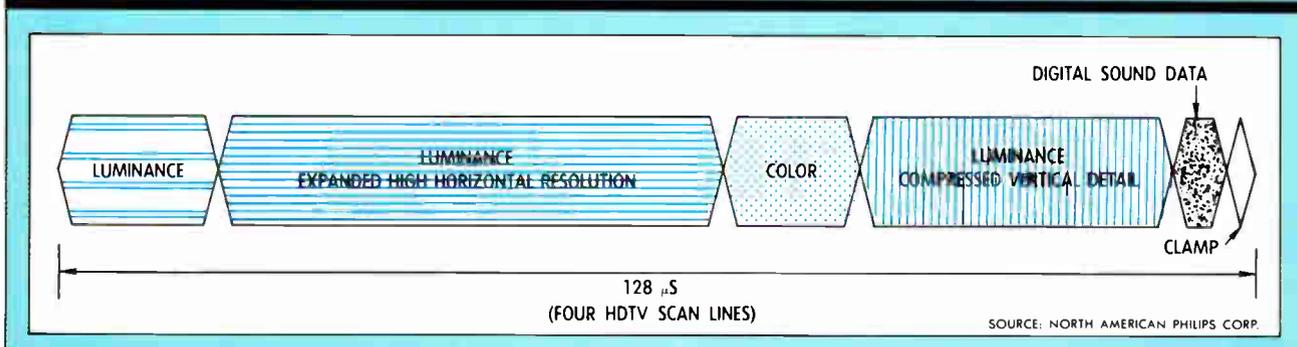
Interference with signals in adjacent cities is avoided by digitizing the information in the augmentation channel. This does not harm signal integrity, says Greebe, because a digital signal is either a 1 or a 0 and does not require the high signal-to-noise ratio of an analog signal to achieve equivalent sensitivity. Digital modulation allows a power level of the augmentation signal 15 to 20 dB below the power needed for analog modulation. Image-statistics techniques compress the digital data to meet bandwidth limits.

The biggest technical challenge for Philips, says Greebe, was in developing techniques to "stitch together" the NTSC-sized picture and the panels. Color matching is accomplished by having a microcomputer in the receiver calculate the differences in the two signals—such variables as delays caused by echoes, noise level, and nonlinear distortions—and compensate for them. To position the panels and NTSC-sized picture on the HDTV screen without a visible demarcation line, Philips first overlaps the segments slightly and then converges the components. The HDS-NA system also introduces random jitter into the boundary, says Greebe. Since the demarcation line moves incrementally to the left or right with each new frame, the human eye does not have time to perceive it.

An important advantage of Philips' screen-plus-panels approach is its pan-and-scan capability. The NTSC viewer wants to see the most interesting part of the action in the wider HDTV screen, says Greebe, which means the field of view for the NTSC screen must be capable of moving within the HDTV field. Since all the panel information comes over the same 3-MHz augmentation channel, he says, it is a simple matter to designate how much goes to the right—and how much to the left—of the NTSC screen.

—Jack Shandle

PHILIPS' SUPERLINE CONDENSES HDTV



Instead of handling each scan line separately, Philips processes the information in groups of four scan lines each. Each resulting "Superline" has five time-multiplexed intervals: normal NTSC luminance data; high-resolution horizontal luminance data; color data; low-resolution vertical-luminance data; and the digital control and sound data.

CAN CRTs HOLD THEIR OWN IN THE HDTV ERA?

The bigger the display, the better the next generation of high-definition TV receivers will look. And the arrival of HDTV is likely to spark the development of high-quality, large-area flat-panel displays, because cathode-ray tubes of the size appropriate for HDTV require very deep cabinets. But Zenith Electronics Corp. is placing its bets on mainstream CRT technology, which it believes will hold sway well into the HDTV revolution.

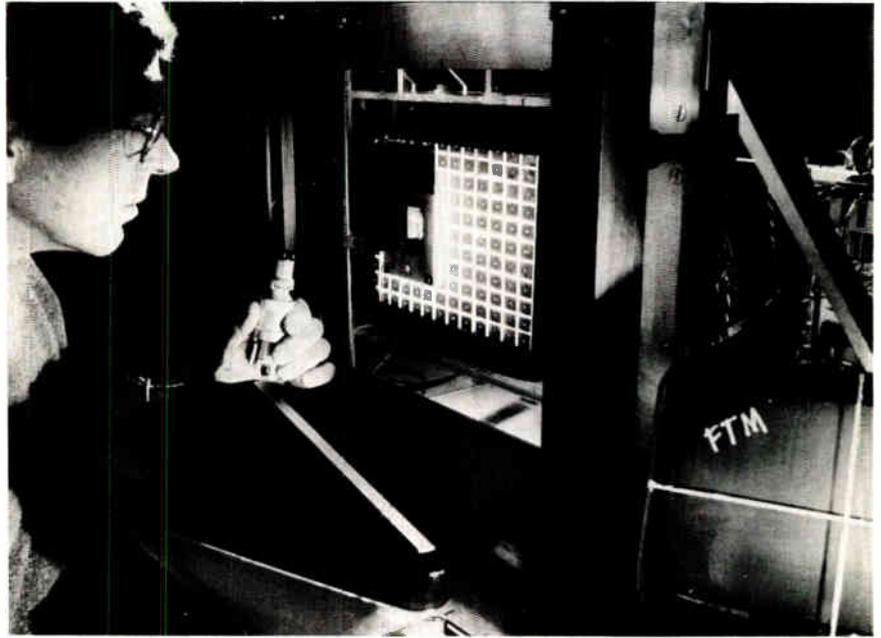
"I've been in the business for 20 years, and the flat panel is always five years away," says Martin L. Lerner, vice president of engineering at Zenith's CRT Division in Melrose Park, Ill. "The flat panels have yet to become cost-competitive."

Zenith is instead working on a new low-cost way to manufacture its patented flat-tension-mask, or FTM, picture tubes. If the idea pans out, it could help drive down high-volume CRT production costs in the big-screen era, Zenith says. And it could play a role in any drive to bolster U. S. HDTV manufacturing competitiveness. What remains to be seen now is whether the company can attract outside funding to try out the idea. It has already appealed to the Defense Advanced Research Project Agency, and hopes to nab a share of the \$30 million the Pentagon has earmarked for HDTV. Zenith also has an entry in the HDTV standard-selection sweepstakes, with its Spectrum Compatible HDTV System one of 20 proposed to the Federal Communications Commission [*Electronics*, November 1988, p. 191].

The Zenith FTM manufacturing scheme relies on an unconventional approach to tube making based on direct printing of color phosphors onto the screen faceplate, instead of the conventional photolithography. The scheme uses high-precision, interchangeable shadow masks that can simply be added to the tube at the end of the production line. Today's methods, by contrast, require the shadow mask to serve as the negative for the faceplate phosphors during photolithography; both the mask and the faceplate must then remain registered for the rest of the production process.

Printing the phosphors directly on the faceplate could be done at low cost using a small machine having very high output, thus eliminating the slow and costly four-step photolithography process, Lerner says. Another advantage is that handling requirements for assemblies moving through the factory would be simplified, since shadow masks could be placed in a clean area until needed.

"We think this could be the nucleus of a very large business" in high-volume, low-cost HDTV tubes, says Zenith chairman and president Jerry Pearlman at the



Zenith's FTM picture tubes could be made in large sizes for HDTV with an unconventional approach based on printing the color phosphors directly onto the faceplate.

firm's Glenview, Ill., headquarters. The problem is that Zenith, the sole remaining U. S. TV manufacturer, does not have the \$70 million to \$75 million that Pearlman says it needs to bring FTM manufacturing to high-volume production.

Zenith currently makes a 14-in. version



of the FTM using more conventional production techniques. That unit is manufactured for a high-resolution computer monitor. But Zenith has been fishing for funding to develop the technology to produce the big screens for consumer picture tubes. Last year it submitted an unsolicited proposal to Darpa, well before the Pentagon unveiled plans in late December to spend as much as \$30 million on HDTV research. Last month, Zenith was reworking its proposal to meet Darpa's requirements for a formal submission. The firm is sure to face competition, but, says Lerner, "we think we're going to win."

Among other things, he is counting on the appeal of FTM technology, which features a perfectly flat, reflection-free faceplate for superior CRT performance. Com-

pared with conventional displays, the FTM tube provides up to 80% higher brightness, or up to 70% better contrast ratios, at equivalent resolution, Zenith says. While conventional displays rely on a convex glass faceplate and a correspondingly curved shadow mask that is suspended within the tube on springs, the FTM mask is stretched and bonded directly to the faceplate under tension.

As in conventional tubes, the FTM shadow mask is effectively a thin metal sheet containing hundreds of thousands of perforations that help direct beams from the tube's electron gun to the screen faceplate. Here they excite red, blue, and green phosphors to create the video image. But the FTM mask is only one quarter the thickness of conventional curved masks. And since it is stretched tight, it is not subject to movement or expansion due to heating. The result is an inherently more rugged and accurate CRT, Zenith says.

The flatness of the FTM design, in fact, is key to the low-cost manufacturing, because direct printing of faceplate phosphors and using interchangeable masks would be unthinkable with curved masks. "Because this thing is flat, it can be done, though it's not easy," Lerner says. "But it's impossible to do on a curved surface. The tolerances don't allow it." Lerner declines to estimate the savings this might produce. "But enough [manufacturing] steps go away" so that "a very good savings" results. —Wesley R. Iversen

HOW THE U. S. IS LEADING THE WAY IN STRATEGIC NONVOLATILE TECHNOLOGY

The technology impacts a broad range of products, and U. S. companies are at the forefront

by Bernard C. Cole

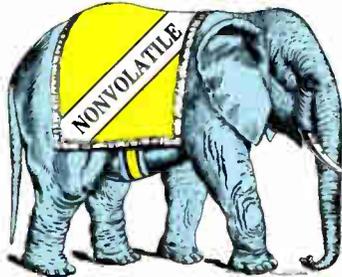
It's a pretty good bet that expertise in dynamic random-access memories alone won't be enough to determine technological and market leadership in the semiconductor industry in the 1990s. Instead, nonvolatile technology is elbowing its way into the running as the critical strategic area of the coming decade.

"The DRAM represents a significant portion of the market in terms of units and sales, but it is still just a memory device," points out Richard Pashley, the general manager of flash-memory operations at Intel Corp. in Folsom, Calif. "But nonvolatile technology is becoming important because it crosses all technology and product areas. It's becoming a memory technology that will soon surpass static RAMs and DRAMs in density, and it will become critically important in logic, microprocessors, standard cells, and even analog circuits."

U. S. manufacturers in particular are grimly determined that what happened in DRAMs and almost happened in ultraviolet-erasable programmable read-only memories in the early 1980s, when Japanese competition more or less wiped out the U. S. chip makers, will not happen again. Not only are they pushing hard to establish density and speed leadership in EPROMs and EEPROMs, they are investing heavily in new nonvolatile technologies. Among these newcomers are antifuse PROMs, ferroelectric RAMs, and flash-nonvolatile memories, which combine the read and write features of EPROMs and EEPROMs.

Although the 1986 semiconductor trade agreement between the U. S. and Japan did little to retrieve the U. S. position in DRAMs, it did allow American semiconductor companies to come back to a position of unrivaled dominance in nonvolatile memory, says Michael Villott, vice president and general manager of the flash-memory division of Seeq Technology Inc. in San Jose, Calif.

"I think we learned our lesson, and in general U. S. companies are doing everything they can to keep their lead, not only in memory but in logic as well," says Paul



Lubeck, marketing manager for electrically erasable memory at National Semiconductor Corp. in Santa Clara, Calif. "If we lose our lead in nonvolatile technology, we lose out across the board, not just in memory."

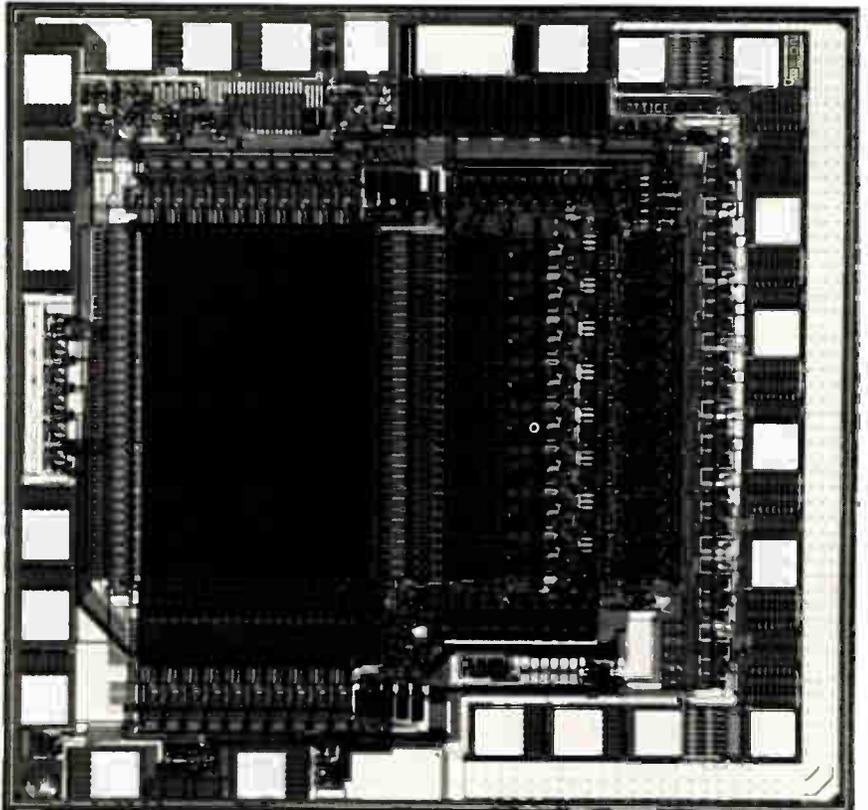
Despite the break offered to the U. S. by the trade agreement, the Japanese still pose a formidable threat. They're continuing to press for higher-density EPROMs, EEPROMs, and flash memories. And in programmable logic, the effort is almost as intense, even though Japanese vendors have not established any significant beachhead.

To make sure that the price of participation is prohibitively high, Advanced Micro Devices Inc. of Sunnyvale, Calif., through its subsidiary Monolithic Memory Inc., plans to challenge in court any

newcomers it suspects of violating the AMD-MMI patents on programmable-array-logic architecture. AMD and numerous other U. S. players are also moving upward in density and speed, developing new programmable-gate-array architectures and application-specific programmable-logic-device designs.

In addition, nonvolatile technology is being put together in new ways, opening up new applications. Chip makers are combining EEPROM on the same die with EPROM, SRAM, analog functions, or standard cells. Vendors are also pushing EPROM- and EEPROM-based microcontrollers to new speed and density.

Finally, there is emerging a new nonvolatile-memory technology, ferroelectric RAMs, which by the mid-1990s will transform not only the semiconductor but also the rotating-memory market. Such devices give systems designers what they have always wanted—the speed of an SRAM or DRAM plus the nonvolatility of



Lattice Semiconductor's Ultramos III process pushes propagation-delay times for its array-logic family down as low as 10 ns in a 300-gate device.

magnetics—along with the use of higher dielectric-valued materials compatible with CMOS processing. These may make it possible to build megabit SRAMs and DRAMs without the expensive fabrication facilities and complex processing required by conventional techniques.

The jury is still out on which of these technologies will come to dominate the market. All the analysts can do is guess. The EPROM market worldwide will grow from about \$1.93 billion this year to about \$2.45 billion in 1992, says Mary Olsen, industry analyst at Dataquest Inc. in San Jose. And the market leaders in terms of both units and dollar volume are U. S. manufacturers, she says—AMD, Intel, and Texas Instruments, followed by Fujitsu, Hitachi, Mitsubishi, National, NEC and SGS Thomson.

LEADER OF THE PACK. In the move toward higher densities and higher speeds, says Olsen, it is fairly certain that U. S. firms will retain their lead. The same holds true in EEPROMs, a segment Dataquest says will grow from \$436 million in 1989 to about \$707 million in 1992: here the major players are the U. S. manufacturers Seeq and Xicor at the high-density end. Other U. S. firms—including Atmel, Catalyst, Exar/Exel, General Instrument, International CMOS Technology, National, and SGS Thomson—are competing on a level playing field with Japanese heavyweights such as Fujitsu, Hitachi, Mitsubishi, and NEC.

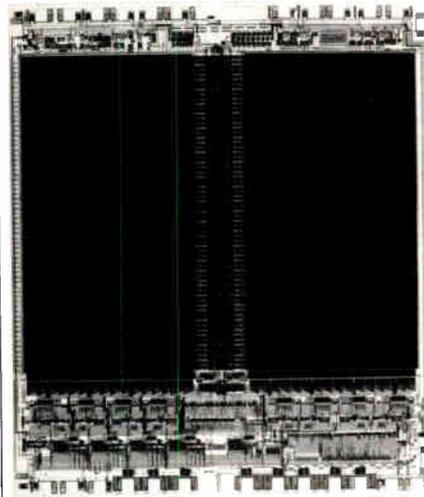
One big question, says Olsen, is the impact of the new EPROM/EEPROM-based nonvolatile flash memory, which in most implementations combines the hot-electron write feature of EPROMs with the cold-electron floating-gate capability of EEPROMs. One major vendor, Seeq, expects that the technology will grow from virtually no market in 1987 to about 37% of the EPROM market in 1990, and to about 62% by 1992.

The initial applications will be as a replacement for such devices in embedded-control applications, says Sanjeev Dua, marketing manager for flash memory at National. But by the mid-1990s, he believes that most of the market for flash will be in totally new applications, such as SRAM and bubble-memory replacement and as solid-state alternatives to disk drives. By 1992, the cost of flash memory relative to EPROMs will drop to no more than twofold, versus the present 400%-to-500% differential. Relative to EEPROMs, says Niles Kynett, project manager for flash memory at Intel, it will drop from about 60% to about 20%.

In programmable logic, which Dataquest expects to grow from about \$275 million in 1989 to about \$700 million in 1992, virtually all of the major players remain U. S. manufacturers. The much smaller, but faster-growing CMOS portion, which presently constitutes 30% of

the total market, is expected to grow to about 45% by 1992, up from only a 16% share in 1987. Even here the major players remain U. S.-owned. They include Cypress (28%), Altera (20%), Lattice (13%), Intel (11%), and AMD/MMI (8%). Noticeably absent is any major Japanese presence except for Fujitsu and Ricoh, and one lone Korean firm, Samsung.

A key element in CMOS PLDs and programmable gate arrays gaining market share is their ability to more than match conventional gate arrays in density and cost per bit, on the one hand, and the speed of bipolar small-scale-integration



Intel is ready with a 1-Mbit flash EEPROM featuring 90-ns read-access times.

and medium-scale-integration standard logic and PLDs, on the other. At the high-density end, for example, AMD, a second source for the SRAM-based Xilinx logic-cell arrays, has just introduced a new generation of circuits that use a 0.8- μ m CMOS process to achieve a gate toggle rate of 100 MHz.

At Altera Corp. in Santa Clara, a 0.8- μ m CMOS process is being used to achieve gate densities as high as 6,000 equivalent gates in its multiple-array-matrix family. The parts also have propagation delays of no more than 30 ns, allowing their use in systems with clock speeds of up to 50 MHz.

Intel has developed a new addition to its microcomputer programmable-logic circuits that combines a 1.0- μ m CMOS process and circuit innovations to achieve a 6-ns delay time in a proprietary PLD with 16 inputs and eight latched outputs, equal to the best that TTL PLDs of comparable size are able to achieve. A key circuit innovation is a distributed TTL translator that is integrated into a symmetrical latch that turns off output drivers much more quickly. At 100 MHz, active power is only 125 mW, at least 25% lower than bipolar implementations.

In electrically erasable PLDs, vendors are similarly pushing for as much speed

as possible. In its family of generic array-logic devices, Lattice Semiconductor Corp., of Hillsboro, Ore., is continuing to push the performance further down into the bipolar arena. With its latest 0.8- μ m CMOS process, Ultramos III, it has driven propagation delay times down to as low as 10 to 12 ns in its 300-gate-equivalent GAL20V8, and to about 15 ns in its 500-gate-equivalent GAL22V10. In its 700-gate GAL6001 generic programmable-logic arrays, the company expects Ultramos III to achieve propagation delays of 20 to 25 ns.

Going for both speed and gate-array-like densities in EEPROMs, International CMOS Technology Inc. of San Jose is applying both process and architectural improvements to a new family of devices that allow densities as high as 3,000 equivalent gates and gate delays as low as 25 ns (see p. 86).

There is still a considerable market for medium- to low-speed EPROMs in the 150- to 200-ns range for low-end 4-, 8-, and 16-bit microcontroller applications as one-time programmable replacements for mask-programmable ROMs. But the fastest-growing portion of the market is the one serving the needs of the new generation of 20- to 30-MHz complex- and reduced-instruction-set microprocessors.

To store large amounts of application microcode, protocol-conversion data, or type fonts in such applications now requires a designer to choose among high-speed SRAM, with its lack of nonvolatility, or battery backup. Traditionally, such applications have been served by bipolar PROMs. However, because of power-consumption requirements, they are limited to densities below 128 Kbits.

Except for niche applications requiring speeds below 10 ns, most bipolar sockets for devices up to 128 Kbits are rapidly being replaced by lower-power CMOS alternatives. CMOS EPROMs are starting to replace bipolar devices at the 16-, 64-, 128-, and 256-Kbit levels for applications requiring access times of 25 to 45 ns; the CMOS parts run at similar speeds but use half to a quarter the power.

The speed battle will no doubt expand to the higher densities. Companies such as AMD, Intel, and WaferScale are now producing 1-Mbit designs in the 90-ns range. On the way from WaferScale Integration Inc. in Fremont, Calif., are 1-Mbit EPROMs, based on a proprietary staggered-contact architecture and using a 1.25- μ m CMOS process capable of speeds ranging from 60 to 90 ns. Also in the works is a 4-Mbit design that builds on the earlier technology by using a staggered-gate scheme to achieve die areas that are no larger than competitive devices in development at Intel, NEC, and Toshiba, but at 90 to 100 ns are 50% faster (see p. 84).

WaferScale Integration is also plan-

ning a whole family of flash-memory devices based on its split-gate, staggered-cell EPROM technology. Requiring a 5-V supply for programming and erasure, the flash cell uses the company's split gate for programming and erasure and a separate select gate for reading. The company is able to do this without sacrificing density or speed, says Boaz Eitan, director of device technology memory design, by taking advantage of the smaller cell size and higher speed of the split-gate structure. Initial product plans include coming to market by midyear with a 55-ns, 256-Kbit flash EEPROM, followed by a 90-ns, 1-Mbit version by the fourth quarter. Both require a separate 5-V program/erase voltage.

However, it is Texas Instruments Inc. in Dallas that is going for the speed record in high-density EPROMs. TI is applying a concept that has become common in microprocessors—the burst mode—in which read-access times are reduced to only 20 ns. The burst-mode EPROM depends on a statistical approach to performance enhancement, says Pradeep Shah, advanced nonvolatile-memory product manager at TI.

SPECIAL LINE BUFFER. Based on the fact that microprocessor code typically exhibits a high degree of both linearity and locality, the TI burst-mode EPROM incorporates a special 32-byte line buffer as well as control logic to take advantage of this. Accesses to memory are assumed to be local if they remain within the current address range of the line-buffer contents and are then accessed within 20 ns. When the data requested is not local, the line buffer is reloaded with the appropriate data from the main array within 70 ns.

In terms of density, flash memories are setting records for the rate at which they're gaining ground. This month—less than two years after it introduced a 128-Kbit n-MOS flash EEPROM—Seeq will introduce not one, but two 1-Mbit flash memories (see p. 85). One is aimed at EPROM sockets and another toward traditional EEPROM applications.

Not far behind is Intel. Last year the company entered the flash-EEPROM arena with 64- and 256-Kbit devices. And last month at the International Solid State Circuits Conference in New York, Intel engineers described a 1-Mbit flash EEPROM with a 90-ns read-access time, a 900-ms erase time, and a 10- μ s/byte program time. The device also boasts an endurance performance greater than 100,000 cycles.

Also announced at the ISSCC

was a 256-Kbit flash EEPROM, coming from TI. The device differs from the Intel and Seeq products by using only 5 V compared with their 12 V. The TI part uses the same contactless-array technology as TI's EPROMs, but with an additional module added for flash devices. Samples should be available later this year, says TI's Shah, and 1-Mbit versions should arrive in 1990.

With all of the focus on flash devices, full-featured EEPROMs using the cold-electron effect for both write and erasure

Flash memories are setting records for the big gains they're making in density

of the floating gate are not being ignored. Interestingly, except for Xicor Inc. of San Jose, which has announced plans to begin production of a 1-Mbit EEPROM later this year, most of the effort has been on the part of Japanese players.

At the ISSCC, for example, researchers from Mitsubishi Electric Corp., Itami, described a 1-Mbit EEPROM fabricated using a 1- μ m, triple-polysilicon CMOS process and capable of 120-ns access times. The device can be reorganized as either a 128-K-by-8-bit or a 64-K-by-8-bit device. At the same meeting, researchers from Toshiba Corp., Kawasaki, described an experimental 4-Mbit EEPROM with a 1.6- μ s read time and a 4-ms page-programming time. The Toshiba part achieves its density two ways—by arranging eight cells in

a series and having them share two select transistors.

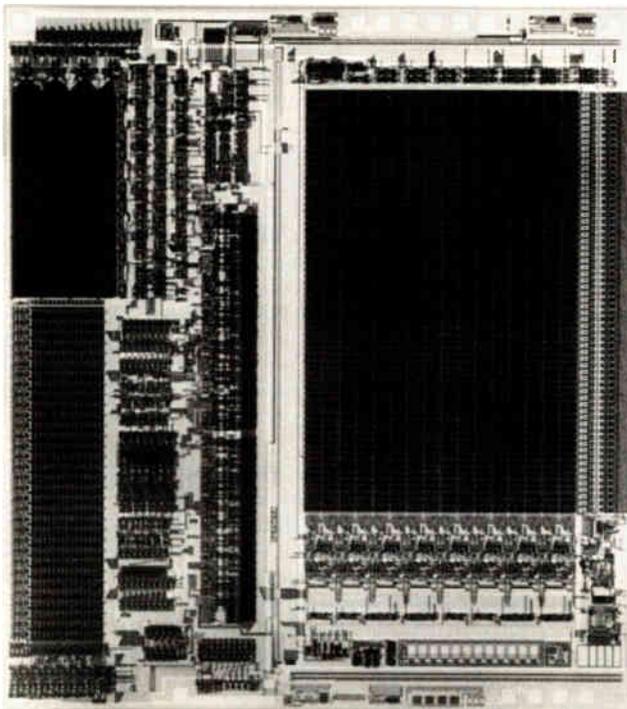
One product that's benefiting considerably from the increasing speed and density of stand-alone EPROMs and EEPROMs is the single-chip microcontroller. At the 4- and 8-bit level, the use of one-time programmable EPROMs instead of mask-programmable ROMs for storage of program memory on chip has allowed Japanese manufacturers to drive down costs while quickly producing devices with application-specific code. In the U. S., the move has been toward increasing the flexibility of microcontrollers by increasing the density and speed of the on-board nonvolatile memory and also by combining various types of circuits on the same device.

Setting new records, Catalyst Semiconductor Corp. of Santa Clara is now entering production with the CAT62C780, which combines 64 Kbits of EEPROM—twice what is commercially available—on the same chip as an 8-bit central-processing unit, 192 bytes of SRAM, and 6 Kbytes of ROM. TI, on the other hand, has developed a family of configurable 8-bit microcontrollers, the TMS370 family, that incorporates 32 Kbits of EEPROM for program memory and another 256 bytes for use as data memory.

Taking another tack, WaferScale Integration has leveraged its expertise in high-performance EPROM technology and come up with the PAC1000, a 20-MHz, 50-ns, user-configurable, 16-bit microcontroller with 64-Kbytes of on-chip EPROM targeted at high-end embedded-control applications.

The newest twist in EEPROM applications will be the emergence this year of a variety of analog circuits that incorporate EEPROM for storage of calibration code. The EEPROMs are an alternative to laser trimming, on the one hand, and CMOS-based switched-capacitor arrays that are self-calibrated by means of some sort of on-chip digital sequencer or controller, on the other. Investigating such alternatives are companies as diverse as Atmel, Exar, National Semiconductor, and Sierra.

First out of the block in any significant way with a family of standard analog functions incorporating EEPROM is Sierra Semiconductor Corp. of San Jose, which will soon offer samples of a family of programmable analog interface devices, the SC22324. This universal EEPROM-based, user-programmable device is a second-order, switched-capacitor, dual-biquad filter. Other EEPROM-based analog interface devices will include a



Catalyst Semiconductor's microcontroller holds 64 Kbits of EEPROM—twice that of competing parts.

programmable gain equalizer and a programmable loop-back controller.

In the longer term, U. S. companies are hard at work on radically new nonvolatile technologies. Antifuse technologies, such as the competing versions being developed by Actel Corp. and Integrated Circuit Corp., are one. Ferroelectric memories, under development at Krysalis Corp. and Ramtron Corp., are another.

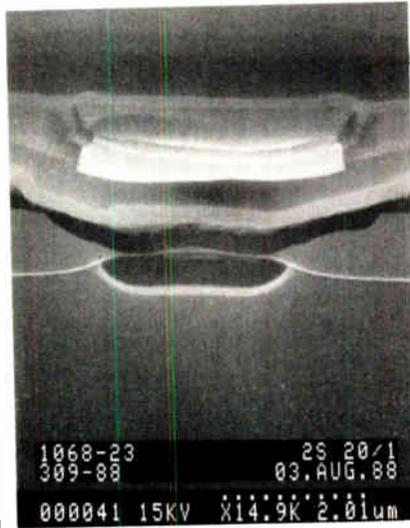
Where existing fusible-link bipolar devices are programmed by blowing links, antifuse devices are programmed by establishing interconnections. The two antifuse companies are taking different routes to commercializing their technology. Actel of Sunnyvale, Calif., has chosen to develop a family of user-configurable, one-time-programmable gate arrays, which in the initial implementation will allow densities up to 6,000 gates. ICC, by contrast, is using high-speed nonvolatile memories as the initial route to commercialization (see p. 87).

Despite competing technologies and product strategies, however, both companies agree on one thing: the long-term potential of antifuse technology. Not only is the antifuse extremely scalable and compatible with existing high-density VLSI CMOS processes, but the number of contacts for an equivalently sized chip is twice that of a gate array, says John McCollum, the manager of technology development at Actel.

The scalability of the antifuse devices opens up a wide range of possibilities beyond gate arrays and nonvolatile memory, says Bruce Roesner, president of ICC in San Diego. Antifuse technology will also be important in cell-based custom and semicustom designs, where antifuse-based PLAs could be used to implement random logic and antifuse-based ROMs and PROMs on the same chip for program storage. Incorporated into microprocessors, he says, antifuse-based ROM microcode can be changed either by field programming or by changing the last mask to alter the microcode. "In RISC-based designs, for example, it should be possible to incorporate more RISC instructions in the form of table-lookup or PLA implementations," Roesner says.

Another coming technology, ferroelectric memory, will have a fundamental impact on two levels, says Howard Bogert, executive vice president of Dataquest. One is as a nonvolatile memory with write/programming speed equivalent to that of SRAMs, he says. The other is by taking advantage of their higher dielectric constant to eliminate the need for advanced trenching techniques now required in high-density DRAMs. "With the cost of building a DRAM production line approaching half a billion dollars, something in the way of a revolution is needed," he says. "Ferroelectric RAM technology could be it."

Ramtron Corp. of Colorado Springs, Colo., has already formed alliances with several companies to commercialize its process. Among them are ITT Microelectronics, NMB Semiconductor, and TRW. In the first phase of its ITT agreement, Ramtron transferred its existing 3.0- μm ferroelectric technology to ITT. In phase two, which has already begun, the ferroelectric technology is being moved to ITT's existing 1.5- μm CMOS process, with plans for a linear shrink, which will take the process to 1.2- μm . For the 1.5- and 1.2- μm technology, the ferroelectric technique will still be an additive process. In this approach, the size of the ferroelectric cell will be 1.5 by 1.5 or 1.2 by 1.2 μm . That will be sufficient to build devices of up to 256-Kbit density, according to Rich-



Actel uses antifuse technology in one-time-programmable gate arrays.

ard Horton, Ramtron's president.

In phase 3, Ramtron and ITT will codevelop an entirely new 0.8- μm process. In this process, the ferroelectric technology will no longer be additive, but will be merged with the CMOS double-level-metal process to produce a 0.8-by-0.8- μm ferroelectric cell, with the necessary density for building ferroelectric RAMs up to 4-Mbit densities, Horton says.

In terms of upcoming products, Horton says the firm intends to attack three separate markets with what he calls low-density, medium-density, and high-density product families.

The low-density family, to be built in the 1.5- and 1.2- μm technologies, will include five parts, at densities of 256 bits, 512 bits, 1 Kbit, 2 Kbits, and 4 Kbits. These parts will be announced and provided in sample form during the second half of this year. They will be aimed at applications now served by nonvolatile RAMs and small EEPROMs, including radio-frequency identification tags, smart cards, electronic odometers, and utility meters. The medium-density family will

consist of three parts, at 16, 64, and 256 Kbits, with the same pinouts as current EEPROM devices. The high-density family will use the 0.8- μm technology and will consist of two products: a 1-Mbit part and a 4-Mbit part.

Horton, naturally, believes that ferroelectric technology holds the potential to shake up memory markets. But he is quick to note that, in the near term, "we are not targeting mass- or broad-scale displacement of DRAMs or disk memory on a cost-per-bit basis."

RUGGED. Rather, Ramtron will aim initially for areas where very rugged nonvolatile memories are required, in which size, weight, and reliability are the critical parameters. For example, the high-density 1- and 4-Mbit parts will sell for up to twice the price of DRAMs on a per-bit basis when they go into production in 1992 or 1993. "And our forecast says they will converge on DRAMs in price per bit by the mid-1990s," Horton says.

Krysalis Corp. of Santa Clara is planning a family of nonvolatile latches and registers that will be 74-TTL-series-compatible, says vice president of technology William Miller. The first one, due for sampling in September, is the 74CF374, which will be an octal-D flip-flop. The part will have the same pinout as a TTL part, but it will be capable of holding the output states in a nonvolatile shadow memory.

Krysalis is also looking at a market for parts that could be a direct replacement for battery-backed nonvolatile SRAMs and EEPROM-based nonvolatile RAMs. Instead of SRAM shadowed by EEPROM, the Krysalis devices will write directly to a ferroelectric cell. These parts, which may be in production by early next year, will be able to do the same job that nonvolatile RAMs do but at lower power, lower price, and with better features, according to Miller.

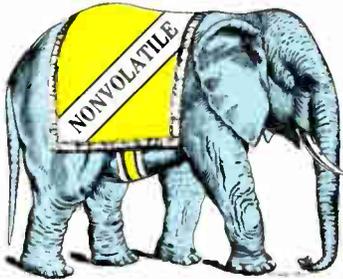
"Once we get down the learning curve in this technology," Miller says, "it certainly has the potential of providing an economical, high-density, nonvolatile random-access memory. The simplicity of having the ability to use a single memory type and having all your memory in your nonvolatile system brings you back to the architectures that people were using in the 1960s, when they were using magnetic core." The difference, he says, is that "we'll have the capability and economics of solid-state memory."

How fast will that happen? At this point, no one can say, but Miller points out that after MOS memory became widely available some time in the late 1960s, it pretty well wiped out core memory in less than 10 years. "Revolutions in this industry can take place fairly quickly," he says. "Ten years from now, most people probably won't be able to remember when most of the memory in a system wasn't ferroelectric." □

A 'DISADVANTAGE' LEADS TO A FAST 4-MBIT EPROM

By making an advantage out of what a lot of companies would consider a serious drawback, WaferScale Integration Inc. has come up with a 4-Mbit erasable programmable read-only memory in a die size the same as or smaller than memories one fourth its density—and with access times as fast or faster. Moreover, the Fremont, Calif., company fabricated the CMOS EPROM with the same tried-and-tested process that it used in its earlier 256-Kbit and 1-Mbit designs.

Actually, WaferScale more or less had to use the same process—unlike most other EPROM companies, it doesn't have its own fabrication facilities, relying instead on outside foundries. That could be a serious disadvantage, but WaferScale turns it into a boon. "We do not have the luxury of playing around with the process every time we want to improve the speed, increase the density, or reduce the



die size," says Boaz Eitan, director of device technology and memory design. "Instead, working within very precise limits, we must rely on circuit and architecture improvements to get the speed and density enhancements we want."

By making those kinds of improvements, WaferScale could use its 1.2- μm process to build the new EPROM and still achieve a 90- to 120-ns read-access time—as fast as any 1-Mbit EPROM available and twice as fast as any of the 4-Mbit EPROMs now being offered as samples. The average cell size is only 9.5 μm^2 and the die area only 241 mil². Competitive 4-Mbit EPROMs available as samples from such companies as Intel, NEC, and Toshiba require much tighter 0.8- to 1- μm design rules to achieve die sizes ranging from 375 to 385 mil².

WaferScale's initial parts, specified at 100 to 120 ns, will be available in sample

quantities by midyear, with faster parts—90 ns—arriving before the end of the year.

WaferScale expects the new part will find eager users among the manufacturers of high-performance 32-bit processors, in both reduced- and complex-instruction-set systems, says Dale Prull, director of marketing communications.

"Currently, systems designers have had to make a choice when considering memory for program or code storage: low-density, sub-256-Kbit, sub-100-ns EPROMs with no wait states, or 1-Mbit designs with access times anywhere from 100 to 150 ns," he says. "Alternatively, if both speed and density were required, designers had to sacrifice nonvolatility and use static random-access memories in combination with some form of nonvolatile memory."

STAGGERING. The improvements that WaferScale made to boost performance, says Syed Ali, manager of memory design, were largely circuit-design enhancements to the company's proprietary split-gate architecture [*Electronics*, July 9, 1987, p. 65]. The enhancements include a staggered-contact architecture that reduces the number of contacts in an array by almost 25 times, and a staggered-cell design that further improves packing density by alternating the floating gates and reducing bit-line area.

In addition, some tinkering with the process resulted in a fieldless array that allows devices to be moved closer together while at the same time increasing the effective channel width. Although the bit-line capacitance of this design is much higher due to the longer continuous n+ bit lines, says Eitan, this disadvantage is offset by the fact that the EPROM cell is capable of generating read currents of about 140 to 160 μA at 5 V, about twice what is possible with current EPROMs.

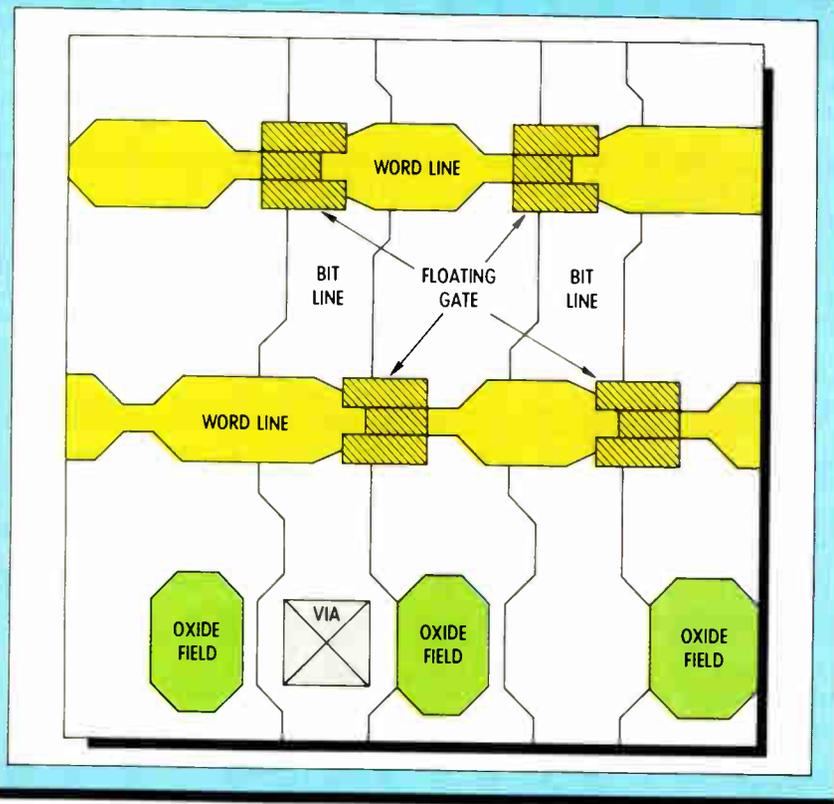
To improve the speed of the device, designers can employ a number of techniques. Chief among them are a differential-balanced amplifier design employing address-transition detection, along with a dual-function column multiplexer and decoder scheme.

The improvements give WaferScale a decided advantage, Eitan says. At most of the companies making EPROMs, circuit designers are running into a brick wall as they try to improve density and speed through scaling. The industry-standard ground-array architecture, with one contact every two cells, limits the scalability of the cell.

WaferScale, by contrast, has eliminated this limitation with its proprietary staggered virtual-ground-array architecture combining staggered contacts and staggered cells. In effect, says Ali, the architecture allows significant reductions in both cell and array size without pushing the lithography.

—Bernard C. Cole

STAGGERED GATES GIVE GREATER DENSITY



WaferScale's staggered-contact, staggered-gate architecture enables it to make a 4-Mbit EPROM with its old 1.2- μm process technology and still achieve 90-ns access times.

SEEQ PUSHES FLASH MEMORY TO 1 MEGABIT

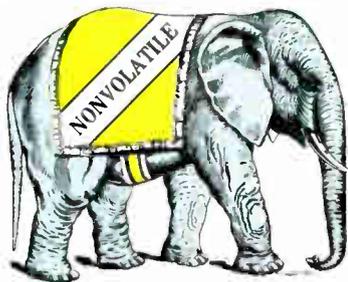
On the fast track toward higher densities, Seeq Technology Inc. is coming to market with not one, but two 1-Mbit nonvolatile flash-memory products. The devices are built using a 1.5- μm n-well CMOS version of the n-channel MOS process the San Jose, Calif., company used to make its first flash device in mid-1986—but the products represent an eightfold increase in density.

The new parts are both 128K-by-8-bit devices, compared with their 16-K-by-8-bit predecessors [*Electronics*, Aug. 21, 1986, p. 53]. The 48F010 targets applications using electrically erasable programmable read-only memory; the 27F010, EPROM applications. The increase in density they both achieve outstrips the growth rate of both full-featured EEPROMs and ultraviolet-erasable PROMs, says Mike Villott, marketing manager for the company's electrically erasable memory division. More than that, he says, it outdoes the growth rate of any other memory technology as well. He predicts that flash memory devices will track the density of EPROMs and eventually bypass them by the mid-1990s.

What makes the fast track to high density possible is the fact that flash nonvolatile memory draws on the features of two other well-characterized and mature nonvolatile technologies. Seeq and the others working with the technology, such as Intel, National Semiconductor, and Toshiba, combine the hot-electron-injection-based write mechanism of EPROMs with the electrical erasure by cold-electron-tunneling used in conventional full-featured EEPROMs.

What makes Seeq's approach different in its 1-Mbit devices is the company's one-and-a-half transistor design. It combines the EPROM transistor and a read-select transistor into a single 5.6-by-4.4- μm cell. As flash devices, either the entire array or extensive subsections are erased simultaneously. By contrast, most full-featured EEPROMs have two transistors and can be erased and reprogrammed byte by byte.

A number of companies have devel-



oped their own single-transistor designs. But Seeq modifies the basic EPROM cell so that the polysilicon gate controlling the channel between it and the floating gate extends beyond the edge of the floating gate. This creates a phantom select

transistor (at the rightmost end of the gate structure in the photo, where it overlaps the diffusion), thus eliminating the need for a separate external transistor.

This solves a problem created by other approaches to flash-memory design, Vil-

lott says. In most designs, the cell's floating gate is, in the erased state, depleted of electrons, and it therefore behaves like a depletion-mode transistor. That makes the device overshoot or undershoot its threshold limits, so that an unaddressed cell in the erased state leaks current. This leakage causes false data reads or failure to program.

In the Seeq approach, both the drain and source sides of the cell are self-aligned. The section of the channel under the influence of the phantom control gate forms an n-channel select transistor. This

transistor operates in the enhancement mode. Linked to the floating gate in series, the enhancement-mode transistor cancels out the effect of the depletion-mode transistor, preventing leakage. Programming in the one-and-a-half-transistor cell is similar to that in an EPROM, using hot-electron injection in the channel between the control gate and the floating gate. During programming, the phantom select transistor is on only in the addressed cell. The phantoms in all unaddressed cells are off.

Erase uses Fowler-Nordheim cold-electron tunneling from the gate to drain diffusion. During the process the control gate is grounded and the drain raised to high voltage.

The two devices differ in operating range and programming flexibility. The EEPROM version can be erased and programmed over a temperature range of 0 to 70°C; it offers endurance up to 1,000 program and erase cycles. The EPROM can be erased and reprogrammed only at room temperature; endurance is 100 cycles.

Both parts are available in the same Jedec-standard, byte-wide, 32-lead pinout. And both feature a bulk-erase time of less than 5 s for the entire array. Typical read-cycle time is 200 to 300 ns. A sector-erase capability allows individual erasure and reprogramming of 128 sectors of 1 Kbyte apiece. Sector-erase time is 500 ms, while write-cycle time is 100 to 150 $\mu\text{s}/\text{byte}$. An externally generated 12-V signal does the programming; an internally generated 12-V signal erases.

In flash-erase mode, the external signal powers internal pumps that supply the drain current of the cells to be erased. During the erase, the floating gate becomes less negatively charged through Fowler-Nordheim tunneling. The gate of the cell remains grounded.

Programming is similar to programming an EPROM. At powerup, a special circuit protects the memory against false write and erase. A 10-MHz oscillator drives a three-loop sequence of 30 shift-register generators, which provide the waveforms needed for programming and flash operations.

Available this month, the 48F010 flash EEPROM in plastic dual-in-line packages is priced at \$92, in quantities of 100. The 27F010 flash EPROM is priced at \$78.75 in similar quantities. —Bernard C. Cole



In Seeq's design, a control gate overlapping the floating gate creates a phantom select transistor, so no external transistor is needed.

lott says. In most designs, the cell's floating gate is, in the erased state, depleted of electrons, and it therefore behaves like a depletion-mode transistor. That makes the device overshoot or undershoot its threshold limits, so that an unaddressed cell in the erased state leaks current. This leakage causes false data reads or failure to program.

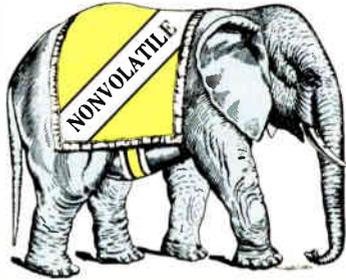
In the Seeq approach, both the drain and source sides of the cell are self-aligned. The section of the channel under the influence of the phantom control gate forms an n-channel select transistor. This

ICT'S ARCHITECTURE BOOSTS PGA SPEEDS AND DENSITIES

A family of electrically erasable programmable gate arrays from International CMOS Technology Inc. breaks some new ground in speed and density. The San Jose, Calif., company uses a state-of-the-art 1.0- μm CMOS process and its own distributed logic-array matrix architecture in the new array family. It calls the devices PEELs, for programmable electrically erasable logic arrays.

The series includes four devices with equivalent gate densities of 1,200 to 3,000 gates. Those are two to four times the densities of currently available electrically erasable programmable logic devices. Clock rates range up to 50 MHz. Device propagation delays are from 23 to 25 ns, performance equal to bipolar TTL devices with 300 to 600 gates.

ICT is combining the reprogrammability of electrically erasable parts with the performance of small PLDs and the flexibility and density of PGAs, says Robin Jigour, director of marketing. Generally, programmable logic devices, with their sum-of-products logic architecture, can perform functions requiring many inputs and product terms and still maintain the short delay times typical of single-level architectures. PGAs, on the other hand, support only a limited number of inputs per cell. That makes it necessary to use



multiple levels of cells for complex logic functions and results in longer propagation delays. The result is that wide-path logic functions, including binary counters, state machines, adders, or any sum-of-product logic function with more than four or five inputs, will usually perform better if implemented in a PLD.

PGAs are usually better for multilevel applications and implementation of input/output-buried logic. These are logic functions that do not limit the use of pins for input, output, or both, unlike most PLDs. Also unlike PLDs, PGAs create their own logic functions within each cell based on a limited number of cell inputs. The cells are then programmed for interconnection to create even more complex logic functions.

ICT could get that combination of speed, flexibility, and density by using a matrix architecture that turns the conventional PGA approach on its ear, Jigour says. A programmable-logic matrix interconnects and controls specialized array building blocks like I/O cells, logic-control cells, and global cells.

Rather than using the cells in the array as the programmable elements and the interconnect as the control, the architecture uses the cells for control and the interconnections for actual programming

of the various logic functions.

The array is made up of multiple buses of input lines (the input bus) and product terms and sum terms (the AND and OR buses, respectively). One output from each logic-control cell can be connected to any I/O cell, with the other connected to the internal input bus. The inputs to each logic-control cell actually sum terms from the OR bus. In this approach, Rigour says, the AND buses can provide anywhere from 80 to 240 product terms for sum-term usage, depending on the number of I/O and logic-control cells.

The first devices in the family to be offered are the 1,200-gate PA7024, with 20 I/O cells and 20 logic-control cells; and the 1,700-gate PA7040, with 36 I/O cells and 24 cells for logic control. Available as samples this month, the parts will sell for \$15 to \$18 each in quantities of 1,000 to 10,000. The 1,500-gate PA7028 and the 3,000-gate PA7068 will be introduced later this year.

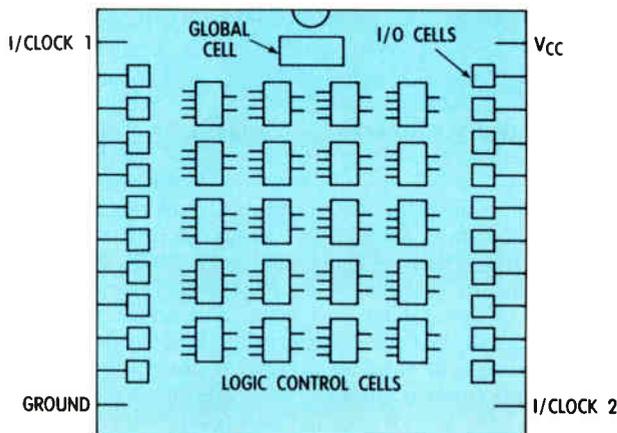
MANY SUMS. In the first two devices, each logic-control cell has four primary inputs and two primary outputs. The two outputs of each logic-control cell are designed to function independently of one another. This makes it possible for the two devices to have 40 and 48 sum-of-product functions, respectively, available for internal and external use. By comparison, the industry-standard PLD, the 22V10 from Advanced Micro Devices Inc., has 10 such functions. One of the two logic-control-cell outputs can be routed to any I/O cell and its associated I/O pin. The other is buried for use within the logic-array matrix, up to 20 levels for the 7024 and 24 for the 7040.

What the combination of electrical erasability and the new architecture gives to the typical PLD user, Jigour says, is an embarrassment of riches. "Compare it to a PLD where the maximum number of configurations that can be achieved is about 12," he says. "The PEEL architecture allows up to 4,000."

To make choosing the best of these possible configurations as simple as possible, ICT has developed a design-entry tool, the Arrays architectural editor. Also available are the standard software-design tools for logic compilation, schematic capture and conversion, and Boolean entry and conversion.

With the Arrays tool, various architectural elements are examined and controlled using a mouse. Among the elements are initializing a design, defining pin names, moving cell configurations, selecting cell interconnections, and modifying the basic cells. Even Boolean entry has been simplified, according to Jigour, with the desired sum selected by the mouse. The architectural editor will be supported on MS-DOS-compatible systems, he says, with CGA, EGA, and VGA graphics support. —Bernard C. Cole

PUTTING THE CELLS IN CONTROL

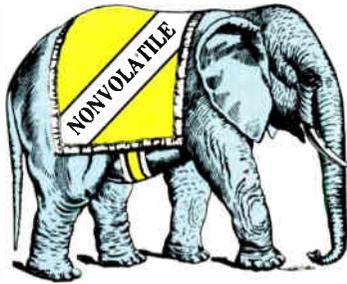


The PEEL family of programmable logic arrays combines I/O, logic-control, and a global cell in a new architecture that allows up to 4,000 configurations.

TECHNOLOGY TO WATCH

ICC TAKES THE ANTIFUSE ONE STEP FURTHER

Before the end of the year, a new player in the user-programmable logic and memory market will be arriving on the scene with a highly promising technology. Instant Circuit Corp. of San Diego, Calif., has developed an innovative antifuse-based technique that is compatible with all types of processes: CMOS, bipolar, and gallium arsenide. Company founder Bruce Roesner believes the approach will pave the way for a new generation of speedy, high-density VLSI-level memories, logic chips, and gate arrays.



as an insulator. As a result, he says, the diode and interconnect structures are less affected by radiation than are active semiconductor transistor and diode structures. Roesner says test devices have remained operational even when subjected to as much as

5 Mrads, full dosage. One indicator of the performance improvements possible with the ICC approach is the first product the company is developing, an 8-K-by-8-bit, two-level-metal CMOS field-programmable ROM. The device, to be introduced before the end of the year, is fabricated using conservative 2.0- μ m design rules and has a target access time of 35 ns. That's comparable in

The technique is compatible with all IC processes: CMOS, bipolar, and GaAs

In embracing the antifuse concept, the ICC parts are kin to the programmable gate arrays from Actel Corp. of Sunnyvale, Calif. [*Electronics*, Feb. 18, 1988, p. 75]. An antifuse approach means implementing functions by establishing interconnections at predetermined locations. By contrast, the current crop of bipolar fuse-based technologies, including programmable read-only memories and logic devices, gets programmability by blowing connections between gates to configure a function.

But, says Roesner, ICC's antifuse technology, for which at least half a dozen patents have been issued, differs radically from Actel's. Actel relies on a proprietary dielectric placed between an n^+ diffusion and polysilicon layer in any CMOS, biCMOS, or bipolar process. ICC, on the other hand, builds its antifuse structure atop a preexisting substrate and subsequent layers of logic and/or memory. Except for specific contact points, these two layers are separated by an oxide layer in an architecture much like that used in silicon-on-oxide insulator techniques.

ENHANCES SPEED. That's why ICC's programming methodology can be applied to all forms of ICs, Roesner says. A programming voltage compatible with today's memory chips (5 to 20 V) can be selected by controlling the thickness of the deposited programming layer. For example, he says, 10 V applied for less than 20 ns across the instant-circuit element results in a permanent connection with a resistance of only a few ohms. Thanks to the low capacitance of the instant-circuit memory bits and diodes, speed is enhanced no matter which semiconductor technology is used for the base circuitry. "This is especially true as the memory or logic array size gets larger," he says.

When programmed, the memory element is essentially a diode in series with a short circuit. When unprogrammed, it acts

speed to similar EPROM-based devices fabricated with 1.2- to 1.5- μ m design rules. The programming rate is 30 ns/byte. Active power dissipation is 140 mW and standby power is 110 μ W. Roesner says initial devices will closely approximate the performance specs of existing parts, even though the technology allows parts that are even faster.

In these one-time programmable PROMs, the logic for address-decode and other peripheral support logic is built on a standard substrate using existing CMOS

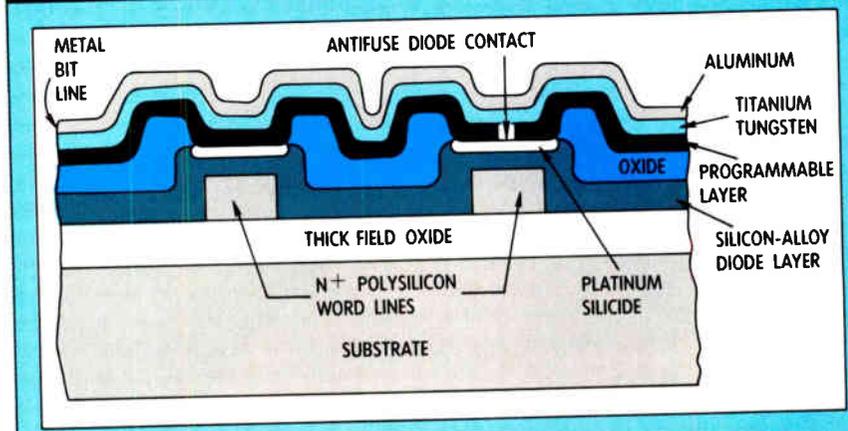
technology. The same holds for an array of field-effect-transistor elements. Onto this substrate is placed an insulating oxide layer, upon which the programmable antifuse structure is built. In a ROM, this involves selective deposition of a platinum-silicide layer over each transistor element, followed by another oxide isolation layer, which is masked out above the transistor elements. Then the antifuse programming layer is deposited, followed by barrier metal, such as titanium tungsten. At the end comes a conductive aluminum layer.

The result is a cross-hatched array of polysilicon and multilayered-metal lines. Information in a particular cell is programmed by cutting through the proprietary programming layer, forming a selectable contact in the form of a Schottky diode at the crossing of the two above each FET element. Then, depending on whether positive or negative logic is used, the presence of a contact indicates either a logical 1 or a logical 0; the absence of a contact indicates the opposite.

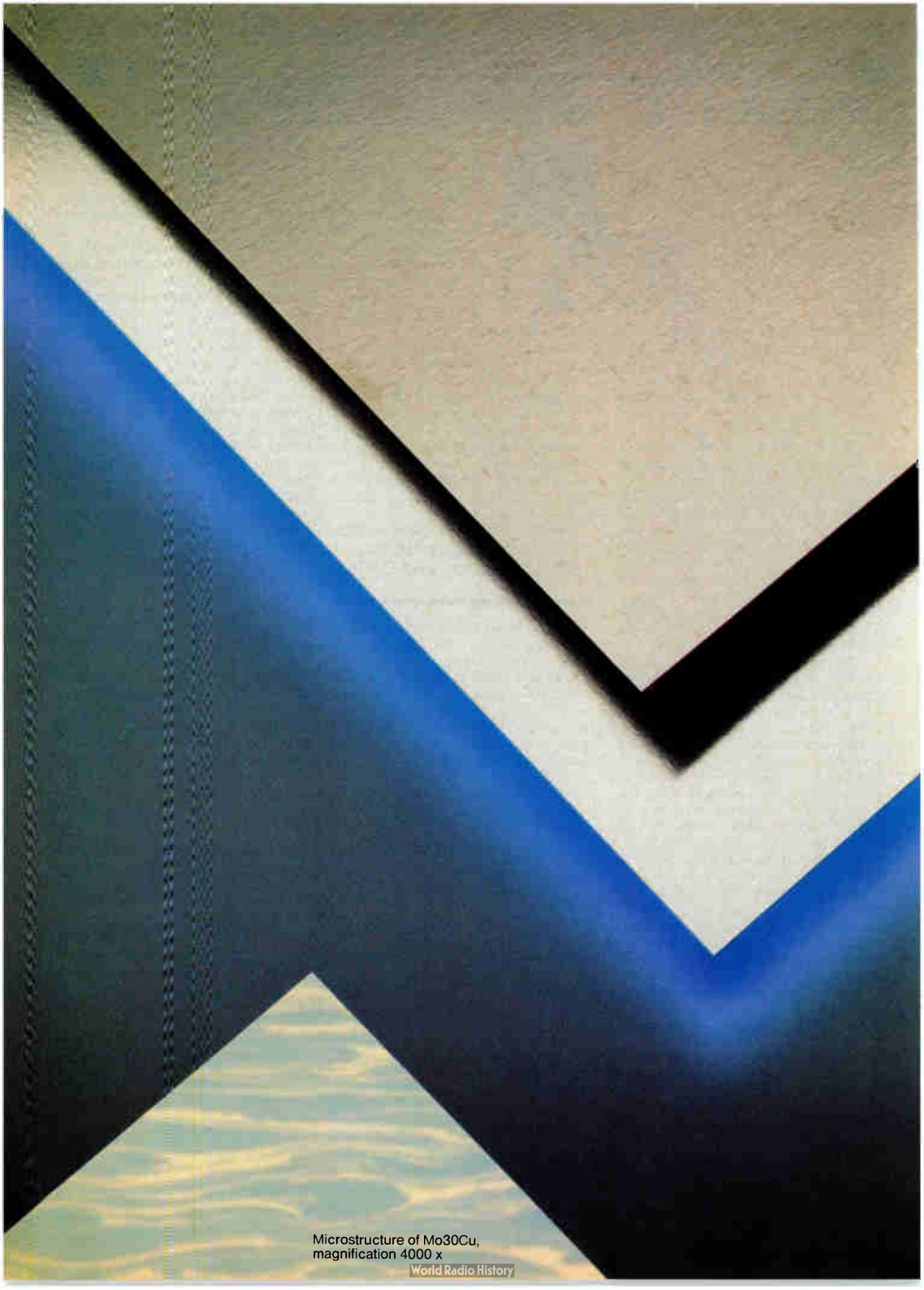
Each polysilicon line consists of n^- material in direct contact with the n^+ layer. In the multilayer metal lines, the aluminum reduces the lines' resistance and the barrier metal prevents the aluminum from diffusing through the polysilicon lines. The junction between the programming material, the barrier metal, and the n^- FET element forms the Schottky diode. Tests have shown the diodes to have a turn-on voltage less than $\frac{1}{2}$ V, a leakage current of only 15 nA, and a reverse voltage breakdown of 10 V. To implement such a structure to form a programmable logic device requires only a minor modification of the top layer of interconnect lines.

-Bernard C. Cole

HOW ICC BUILDS ITS ANTIFUSE STRUCTURE



Instant Circuit Corp. builds its antifuse structure atop a preexisting substrate and layers of logic and/or memory with an oxide layer in between, in a scheme reminiscent of silicon-on-oxide.



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PC SOFTWARE: PUZZLING OVER TODAY'S MENU

*Incompatible operating systems,
graphical user interfaces, and
networking systems make perplexing
decisions for users and vendors*

Once upon a time, life was simple for personal computer buyers and vendors: as a matter of course, you picked an IBM Corp. PC or compatible and ran the DOS operating system.

But the simple life is no more. In just two years' time, the PC world has been thrown topsy-turvy by a shift from a single industry standard—the original PC—to multiple choices. In hardware, there are two major factions: IBM-compatible and Apple Computer Inc.'s Macintosh. In software, operating systems and user interfaces have sprouted up in both camps like mushrooms after a rain.

"It's such a mess!" says Michael Slater, editor and publisher of *The Microprocessor Report*, an industry newsletter. "There are conflicting operating environments, conflicting operating systems, and conflicting application interfaces."

In fact, more elements are in a state of flux than at any other time in the short history of the PC, and nowhere are the stakes higher than in software. Faced with today's difficult choices, buyers are taking longer to make major purchasing decisions, leaving software vendors wondering how to proceed. "The most vulnerable [group] in this mess is the software developers," says Slater. "Do they write for DOS, X Windows, OS/2, and the Mac-

intosh? Or must they select a subset, and if so, which one?"

These questions are echoed by those facing buyers, whose challenge is to pick the PC configuration that is best-suited and most cost-effective for a particular function or set of functions. This can be a mind-boggling exercise. For example, should you move to OS/2, the operating system for IBM's Personal System/2, or will DOS suffice? If DOS will do, what version? If OS/2 is required, which edition? Do the users want DOS 4.1 with its menu-driver-shell user interface—or should they stay with the familiar command-oriented editions of DOS 3? To further complicate matters, AT&T Co.'s Unix operating system will be giving OS/2 a run for its money in the new PC world of multitasking and networked systems.

UNTIL THEN. One day these hassles may vanish. When user interfaces all behave alike—such as the close match between OS/2's Presentation Manager and the Open Software Foundation's OSF/Motif—and the major operating systems all have the mainline applications implemented, users may not have to think about what operating system is running it all. But until then they face some tough decisions.

All this hubbub is bound to cause some perturbation in the market. While buyers

might initially rejoice at the dazzling array of products to choose from, they soon come up against some sobering reality: there's a price to pay for the advanced systems. The new, sophisticated software—especially the plethora of multitasking and multiuser environments now available for machines based on the 80386 and 286, or a Macintosh alternative—demand much more expensive hardware than the old. This is one reason why industry watchers peg the PC segment as growing just 8% this year, down from a 15% growth rate in 1987 and 10% in 1988 [*Electronics*, January 1988, p. 59].

"The industry and software are transforming and will continue to do so for a while," says Gary Stimac, vice president of systems engineering at Compaq Computer Corp. in Houston. "Some of the trends in the industry have not reached their end point. For example, an operating system for the 386 that can run both OS/2 and DOS applications simultaneously is the right answer." Currently, if a user runs OS/2 he has to give up DOS, and vice versa. "The current OS/2 is a compromise solution," says Stimac.

There are also advantages and disadvantages in the new wave of graphical user interfaces, according to Stimac. "As the trend of moving from character interfaces to graphical user interfaces continues, corporations have to decide not if,

by Tom Manuel



Photo: William Costello

Which is the best upgrade path from DOS? What will it cost? When is the time?

but when, to change over," he says. "But is it a smooth transition to graphical user interfaces? to departmental computing? to local-area networks? No."

Naturally enough, the software houses believe that any transitional pains are just part of the process. "There are different products to meet different user needs," says Mark Mackaman, OS/2 product marketing manager at Microsoft Corp. in Redmond, Wash. "Users should identify their needs, then find out what applications satisfy these needs. The applications will dictate the operating system, which will dictate the hardware platform required." It will take some hard work to sort all this out, he says, but the result will be more productive computing.

One of the more beguiling possibilities

raised by the turmoil in PC software is the chance it offers for Unix to break into the mainstream. Currently there's a flurry of activity to provide PC applications in Unix and to make available mixed environments where Unix and DOS applications both run. Unix is available in several flavors now for the more powerful high-end machines built with the 80386 processor. It offers a multitasking, multi-user environment that makes full use of the architecture's 32-bit capabilities, well beyond what OS/2 can do. Soon there will be a couple more versions of Unix that could drive both 386 and future 486-based machines—AT&T and Sun Microsystems Inc.'s merged Unix System V.4 and the Open Software Foundation's OSF/1.

While some observers see Unix over-

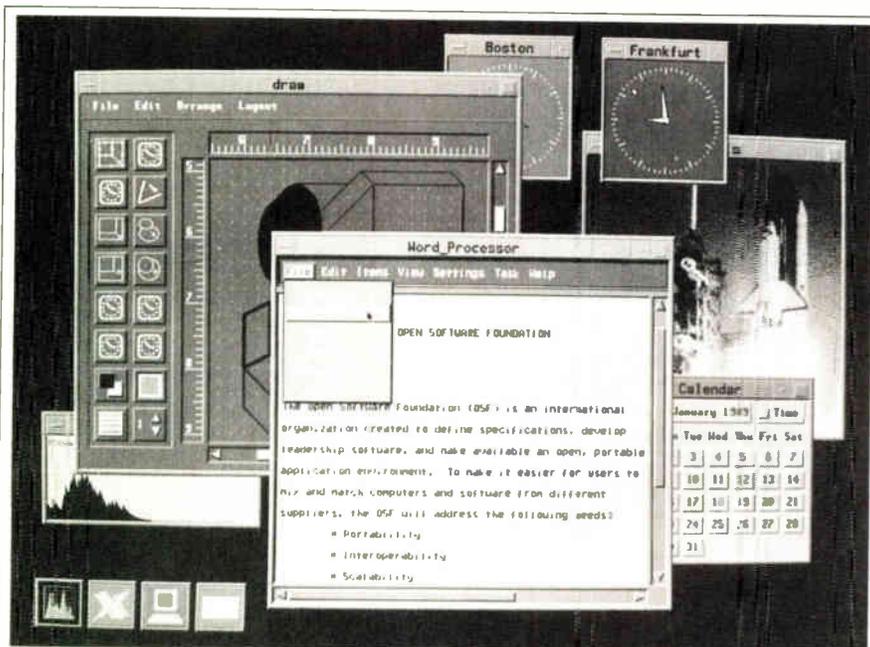
taking OS/2 in the high-performance segment of the industry, others believe it will remain enmeshed in the niche market areas it now serves. "Unix tends to be sold in niche marketplaces and as a platform for building vertical applications," says Microsoft's Mackaman. About 65% of the Xenix applications sold (Microsoft's earlier version of Unix) have been used in this way, he says. "I see Unix systems [in the future] as a server in the OS/2 and LAN Manager environment," says Mackaman. The LAN Manager is a networking program developed by Microsoft and 3Com Corp. of Santa Clara, Calif., that ties PCs running DOS and OS/2 in the same network. Microsoft is offering a variation, called LMX, for Unix; it brings computers running Unix into the same networks with OS/2 and DOS machines.

JUST ONE. LMX is just one of many developments that are giving Unix a better chance at penetrating the PC world. Sun last year introduced its 386i computer running the Sun OS version of Unix. The machine, which falls in the high-end-PC price range, boasts a graphical user interface called Sun View, built-in networking capability, and the ability to simultaneously run MS-DOS applications: multiple DOS applications can run in Sun View windows at the same time that Unix applications are running in other windows. To accomplish this, Sun uses the VP/ix product from Phoenix Technologies Ltd., Norwood, Mass., which implements the DOS windows and largely performs the DOS-Unix integration.

Besides allowing the applications to transfer data among themselves, the Sun system also supports interprocess communications between Unix and DOS. This is done through a product called PCNFS, a PC extension to Sun's Network File System, which the Mountain View, Calif., company released last December.

"Someone on a DOS machine today who is stretching the limitations of DOS has two choices in a step to the future: he could move up to Unix or OS/2," says Will Poole, senior software product marketing manager at Sun's East Coast division in Billerica, Mass. A Unix machine is a viable choice for breaking free of DOS's limits, he says, because it delivers a large address space, a graphical user interface, a good software-development environment, and a bunch of technical applications. These goodies come at no loss of investment in DOS applications and training when a DOS-under-Unix product is also used.

It's not surprising, then, that more and



The new OSF/Motif, from the Open Software Foundation, gives Unix systems a graphical user interface with a look and feel like Microsoft Corp.'s Presentation Manager for OS/2.

more DOS-under-Unix packages are coming to market. For example, emulators of the 286 instruction set for other processors are available from both Phoenix Technologies and Insignia Solutions while Hunter Systems offers the XDOS emulator for Motorola Inc. 68020 and 68030 processors, which power the Macintosh [*Electronics*, March 31, 1988, p. 80]. DOS emulators for the Sparc reduced-instruction-set processor architecture and the Digital Equipment Corp. VAX architecture are under development.

"These DOS-under-Unix products can provide the best of both worlds," says *The Microprocessor Report's* Slater. "Multiple OS applications can be executed concurrently in a fully protected windowing environment, which is something that OS/2 will not be able to provide until a 386-specific version is available."

AN ALTERNATIVE. Of course, another way to run DOS applications with Unix is to port them to run in a native mode directly under Unix. A Santa Monica, Calif., startup, Segue Software Inc., is set to do just that. Its first product will be a Unix version of the Norton Utilities, to debut by the end of the third quarter. "When most of the important [PC] industry-standard applications are available in Unix too, users will not be concerned whether their machine runs Unix or what," says Peter G. Weiner, founder and CEO of Segue. "All the native-Unix versions of popular DOS applications are going to come out eventually, but we want to make it a moot issue and get things rolling now."

On another front, some firms are exploring ways to run multiple DOS applications on 386 PCs without running Unix or waiting for a 386 version of OS/2. Among the multitasking software-control pro-

grams for 386-based machines are Microsoft Windows/386; VM/386 from Intelligent Graphics; 386-to-the-Max by Qualitas; Desqview/QEMM-386 from Quarterdeck Office Systems; and The Software Link's PC-MOS/386. Another approach to multitasking on 386-based PCs is the Concurrent DOS line of multiuser operating systems from Digital Research Inc. in Monterey, Calif.

The issues and choices are no less complex outside the realm of Unix. In hardware there are different processor architectures—Intel 286 or 386, Macintoshes with Motorola 68020 and 68030 CPUs, and on the horizon some of the emerging RISC processors may be cheap enough for high-end PCs and certainly for network-server applications. And there's a seemingly bottomless basket of software goodies: operating systems, user interfaces, graphics, networking systems, and application programs. How do prospective buyers, application-software vendors, and system vendors sort it all out?

Each of these groups faces a unique set of challenges. Buyers must be certain they will get the best possible system for their needs for the lowest possible cost. When choosing an operating system, they must consider whether or not they need a windowing interface and networking.

As in most systems-integration issues, a close analysis of the application-software needs is paramount. Deciding when the expensive spread is cost-justifiable can be very tricky. Users who want to run just one application most of the time—a spreadsheet or word processor, for example—may not require operating software that offers anything more than single-tasking DOS. But suppose a user decides to run several programs on a reg-

ular basis, especially a graphics program or CAD package, but does not necessarily need to run them concurrently. Then DOS with a windows package and mouse interface, and a windowed version of the applications, would probably enhance productivity without adding too much cost.

If a user needs to run several tasks at once, including one or more background communication jobs, and will be shifting among them, then a concurrent multitasking system is in order. The expense to upgrade both the hardware and software will probably pay off in increased productivity, provided that a productivity-enhancing mix of applications is available to take advantage of the operating-software environment. In addition, a graphical user interface could be considered a must in this case, because with several tasks running at once, the best way to keep track of what's going on is through a dynamic windowing system.

When organizations move into work-group computing, then they require a network complete with servers, work stations, and very sophisticated software. The server computers work best if they are running a multiuser operating system such as Unix. Network-managing software, such as LAN Manager or Novell Inc.'s Netware, will probably be required. Each work station will be running an advanced multitasking (and possibly multiuser) operating system, such as OS/

FACING THE PC OPERATING

Features	MS-DOS
Users per system	One
Recommended minimum configuration	8088 processor, 640-Kbyte memory, 2 floppy-disk drives
Maximum user memory	640 Kbytes (8 Mbytes extended)
Memory management	Physical static, segmented
System security	None
Execution modes	Real
Execution granularity	Program
Interprocess communications	None
Device input/output	Simple, often polled
Networking	PC Net, MS Net, PC NFS, Novell, others

2 Extended Edition or Unix, and a graphical user-interface system.

To justify and fully exploit work-group computing systems, new applications that effectively use the richness of the operating environment must be available. But currently, such applications are few and far between. Still, companies can start now to buy and install the hardware, networks, and operating software for work-group computing and be ready when the applications arrive. The cost will be considerably higher than running a bunch of stand-alone PCs, but the eventual payoff appears certain. The most computer-savvy organizations can start to build some of their own applications for this new environment and then add off-the-shelf packages as they emerge.

On the other hand, the independent software vendors' task is to bet on which mix of operating systems and user interfaces will survive—and thrive. Then they must decide how to offer their applications for as many of the popular platforms as possible. System vendors offering only hardware have the easiest decision—just make sure that their hardware can run all the major operating-software environments.

The blossoming of PC networks as a productivity tool in large corporations has generated its own rubric: work-group computing. PC networks, central servers for files, communications, printers, data bases, and access to corporate data on

Work-group computing justifies the added cost of OS/2 or Unix

mainframes and minicomputers are emerging as the tools of this segment. "During the last six years of personal computer evolution from the 8086 to the 20-MHz 386, most users were after personal productivity [enhancement]," says Compaq Computer's Stimac. "But as we move into the 1990s, we see PC software evolving to work-group productivity."

Networking demands using the newer operating software technologies to handle sophisticated data-base applications on groups of desktop work stations. "It certainly seems clear that it's a strong trend," says David Liddle, chairman and founder of Metaphor Computer Systems Inc. of Mountain View. "A few years ago, networking was thought of as exotic; not now, when most desktop computers in the Fortune 500 [companies] come in ready for networking and get connected right away," he says.

Metaphor has been supplying its distributed-network computing system, called the Metaphor Data Interpretation System, to a growing number of Fortune 500 company customers since 1985 on its proprietary work stations and servers. Last year it completed an agreement with IBM for porting the DIS software to the IBM PS/2 under OS/2 Extended edition and opening the door for other technology transfers between the two companies.

Distributed data-base computing will spur new growth in the PC segment when it gets rolling at top speed. "There is a big rise in the number of companies thinking about and starting to implement a whole new suite of applications with more value" than the traditional single-user PC applications like spreadsheets and word processing, says Liddle. "All of these require access to lots of data from a wide range of sources."

Whatever combination of hardware, operating system, user interfaces, and networking users select for the new world of distributed applications, it will not come cheaply. The PC or work-station platforms required to run the newest applications will initially be three to five times as costly as the typical single-user stand-alone personal computer in use today—an AT-type DOS machine or the original Macintosh, for example. And on top of the work-station costs, networking and servers must be added.

To run multitasking operating systems, networking, and data-base managers requires processors like the Intel 386 or forthcoming 486, the Motorola 68030 or future 68040, or even some of the new

RISC processors. Memory capacity of several megabytes and up to 10 Mbytes or more is also needed, since graphical user interfaces, such as the Presentation Manager, soak up several megabytes of main memory to run efficiently. The applications that will take advantage of these systems will require plenty of disk storage, either on the work stations or at data servers. This level of hardware and software can easily run from \$10,000 to \$25,000 per user at today's prices.

Each of the advanced operating systems has available one or more graphics-oriented user-interface environments designed to run with it. They are all slightly different. OS/2 users have the Presentation Manager, and DOS users can choose from a couple of versions of Microsoft Windows and other packages, such as the Digital Research GEM system. And there are a number of user environments for Unix. Besides Sun View, AT&T and Sun are building a user interface called Open Look to go with their new merged Unix, System V.4. Then there's the Open Software Foundation's OSF/Motif, a user interface made up of several pieces of other interfaces, with the behavior and look of the Presentation Manager.

"As you look at the different operating environments moving through the PC market, there is one common thread—most users want windows," says Compaq's Stimac. The various graphics-oriented user interfaces and operating systems are all designed to make personal computing more effective, more efficient, and easier to do. But a price must be paid for this. First, a much more expensive computer configuration is required, and second, while easy to use, the new system may be rather complex to set up and support. Either an information-system staff or manager may be needed.

ABANDON DOS. Meanwhile, one of the most important choices facing PC users is whether to abandon DOS for new technology—OS/2 or Unix and a graphical user interface—and if so, when. Of course, there is little need to make this wrenching and costly shift if DOS is still doing the job. Users have a huge investment in equipment, applications, and training—more than \$100 billion—in the original industry-standard IBM PC. For companies making the changeover, much of this massive investment will have to be written off.

Still, a lot of today's installed equipment base is probably about ready to be replaced anyway, and this presents an opportunity for users who will be buying high-power hardware to take advantage of the newer software. But for other users, the feeling might be, "if it ain't broke, don't fix it." Much can be said for this approach. For many, DOS is going to be around for a long time—another five years at least. □

-SYSTEM CHOICE

OS/2	Unix
One	Many (depending on system performance)
80286 processor, 6-to-8-Mbyte memory, 20-Mbyte hard disk	68020 or 80386, 4-to-8-Mbyte memory, 40-to-80-Mbyte disk
16 Mbytes per process	3 Gbytes per process
Virtual, demand-segment swapped	Virtual, demand-paged
Protected-mode operation at operating-system level	User passwords, group-level permission (Orange Book Class C1 level)
16-bit protected	16- and 32-bit protected
Thread within process	Process
Shared memory, message queues, semaphores, pipes	Shared memory, message queues, semaphores, pipes
Interrupt-driven	Interrupt-driven
LAN Manager	TCP/IP, NFS, RFS

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BROADBAND STANDARD CASTS A WIDE NET, AND HAS NOW REACHED CRITICAL MASS

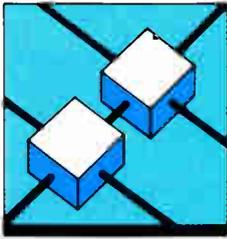
With technical problems solved and products available, broadband Ethernet is taking off

by Jack Shandle

Broadband networking has long been hobbled by a lack of standards, high installation costs, and a reputation for being an arcane technology because of its analog radio-frequency signaling. But now it's breaking free of those constraints and stands poised to stake out a bigger share of the local-area-networking market.

The standards problem was settled in 1986 with the adoption of the IEEE 10BROAD36 standard for running IEEE 802.3 Ethernet on broadband nets. Almost immediately, one vendor—Chipcom Corp. of Waltham, Mass.—plunged into the market with broadband-Ethernet products. But it wasn't until the last quarter of 1988 that competition arrived to pique the interest of system integrators and original-equipment manufacturers, who like to have more than one vendor supplying goods.

Now three companies market broad-



band-Ethernet lines that include basic connection and signaling devices along with bridges to baseband LANs. And one firm—Lanex Corp. of Beltsville, Md.—is offering a new bridging product that will connect broadband to telecommunications-based wide-area networks. The product initially will work with AT&T Co.'s T1 lines and the CCITT V.35 standard, says Joe Greaney, vice president of engineering. Bridges to IEEE 802.5 token-ring LANs and the Fiber Distributed Data Interface (FDDI) are next, he says.

Finally, the bugaboo of high initial installation cost will be dispelled by a cabling system that is now completing beta-site testing. The new system, from two Pennsylvania companies, cuts costs drastically and offers virtually "plug-and-play" installation.

Just as crucial to broadband's future as these developments, however, is the

growth of local-area networking itself. Ironically, broadband's big selling points—multichannel capability and the ability to link large geographic areas—have been greatly enhanced by the proliferation of baseband LANs. More and more corporations are finding themselves with isolated baseband networks scattered around one or more large buildings, says Maureen Lawrence, Chipcom's vice president of marketing. Broadband Ethernet lets them link these LANs with an IEEE standard protocol.

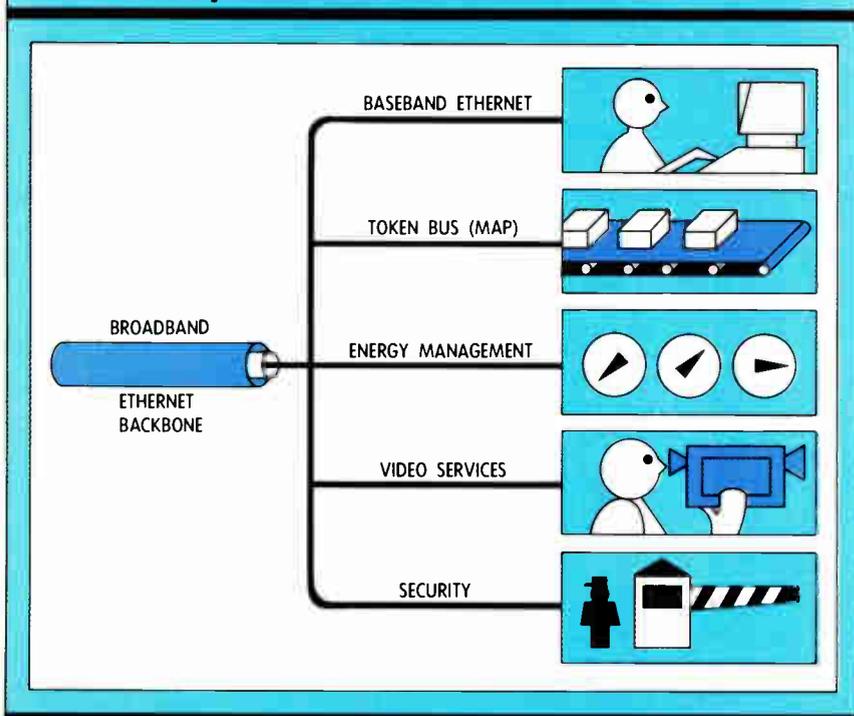
Broadband's distance advantage is significant: the 10BROAD36 standard specifies a maximum distance of 3,600 meters between the two most remote nodes. By contrast, standard "thick-cable" Ethernet is 500 m; "thin-cable" Ethernet is 180 m; and an upcoming version running on telephone twisted-pair wiring is 100 m. If that advantage weren't enough, Chipcom's Marathon Bridge product extends broadband's maximum run to 26 miles.

Making the broadband option even more attractive is the multichannel capability. Unlike popular baseband LANs, which carry only data, it transports data, voice, video, and virtually any other communications service on the same cable.

GROWING MARKET. All these benefits have created a broadband-Ethernet market that analysts now place at about \$65 million, says Gail Daniels, Workgroup and LAN marketing manager for Digital Equipment Corp. in Littleton, Mass. However, she adds, the allure of fiber-optic technology may nip at the heels of broadband's growth. Not surprisingly, broadband vendors paint a rosier picture. Both Chipcom and Lanex say that the overall broadband category—which includes proprietary networks as well as broadband Ethernet—will make up 8% to 10% of the total LAN-equipment market in 1990. That's about \$250 million, assuming a total market of \$2.5 billion, says Chipcom's Lawrence, who pegs broadband-Ethernet's share at about 50% of that total.

Of course, no one is saying that broadband Ethernet can beat baseband LANs in terms of cost per node. A baseband Ethernet transceiver built into an add-on board for a personal computer, for example, costs \$350. A single-port broadband transceiver—which must be a modem because of broadband's rf signaling—costs

ONE CABLE, MANY SERVICES



Broadband networks make more sense than conventional baseband LANs for companies with multiple communications services that require CATV cabling.

\$2,500. Even the attempts of the broadband vendors to bolster their competitive position by offering multipoint modems falls short. Chipcom's eight-port modem, for example, costs about \$5,000, Lawrence says. That brings the cost per connection down to \$625—still \$275 more than the baseband competition.

So with the vast majority of LAN connections remaining baseband, broadband's niche lies in tying them together and providing multiple-channel networking to customers who want it. Not surprisingly, these benefits are becoming increasingly complementary as corporations become more communications-oriented. If a customer is going to install a backbone to link LANs, the argument goes, why not one that carries video, voice, and data instead of just data?

Until now, the answer might still have been "thanks, but no thanks." That's because broadband nets were expensive to install and needed an rf expert to maintain. But the new cabling system from Broadband Networks Inc. of State College, Pa., and AMP Corp. of Harrisburg, Pa., offers a remedy. The LAN-Line Broadband Star Wiring System can replace the custom-built broadband net with a less costly design that's close to being plug-and-play. "We put a lot of the system engineering into the hardware, so you don't have to know anything about rf to maintain it," says Steve Davidson, Broadband Networks' vice president of marketing.

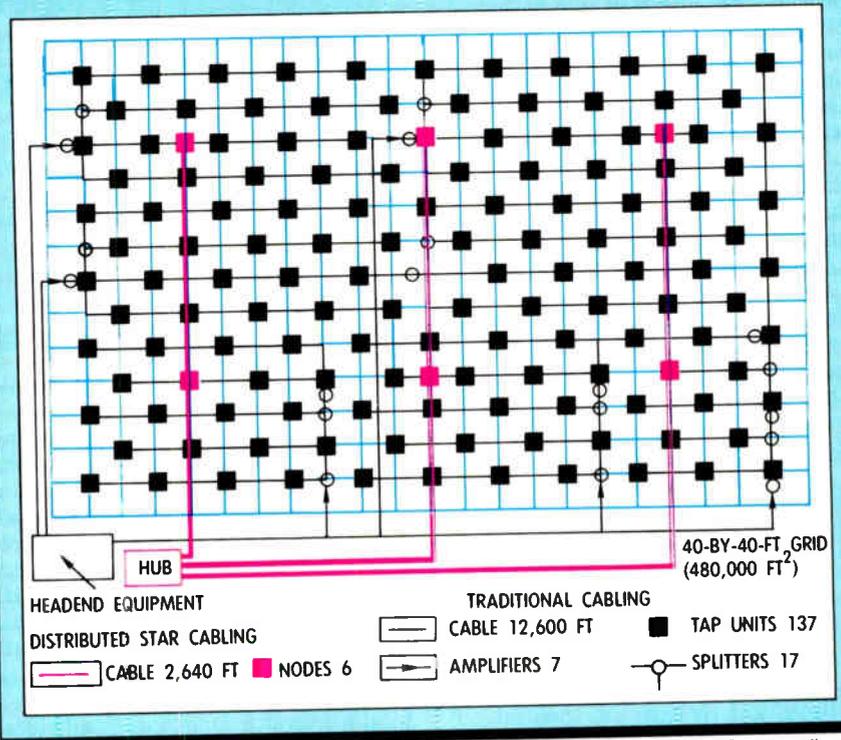
Since the product solves most network-wide rf-engineering problems, engineering costs are greatly reduced—so much so that a complete wiring job costs 40% to 60% less than installing the alternative, a branching-tree network, he says. "You don't have to put up \$1 million to totally cable a 2-million-square-foot building any more; you can start by spending as little as \$10,000 and expand as the need arises."

EASY TO RUN. Once installed, the network is a breeze to run. For starters, it replaces the normal aluminum-shielded CATV cable with inexpensive RG-11 cabling. More important, it uses a distributed-star topology instead of the branching-tree topology of conventional broadband networks.

"With a CATV system, you had 16 adjustments to make periodically," Davidson says. "We need just one." With the old topology, customers had two unattractive options forced upon them by the fact that rf signal integrity is sensitive to overall network loading. They could design a small network knowing that a complete redesign would be required when it came time to expand. Or they could invest a big chunk of money to install a cabling grid that would allow for expansion but initially would be underutilized, probably for years.

The distributed-star topology sidesteps these problems because each "service

A WAY TO SAVE ON CABLING COSTS



A new cabling system developed by Broadband Networks Inc. and AMP Corp. radically reduces CATV cabling costs and allows broadband networks to grow incrementally.

node"—the point from which user connections radiate—can be engineered to be electrically independent of the rest of the network, says Davidson. This means network designers can add new service nodes using only some additional cable,

Unlike baseband nets, broadband carries data, voice, and video on one cable

which has predictable losses, plus an equalizing, or line-balancing, module to compensate for those losses.

Distributed by AMP, the system's distributed-star topology is set up so that each node in the star serves a specific, well-defined area. By contrast, most installations now are based on a nodeless linear signal path, as in the branching-tree scheme. Each service node, located in a wiring closet, can support up to 127 user connections over direct wiring. The service nodes connect directly to a hub, which can support up to 150 nodes. The system conforms to IEEE 802.7 standard specifications for a broadband coaxial-cable system, and it delivers all the services of a CATV wiring system, says Davidson.

Depending on the success of the LAN-Line Distributed Star Wiring System, market estimates for broadband networks could be thrown into a cocked hat.

But other market forces and technologies—especially fiber optics—will also have an impact on the long-term growth rate. "Broadband is an effective and mature technology," says Daniels of DEC, "but our market research also indicates that customers are expressing a lot of interest in fiber-optic backbones." That technology will be hampered by a lack of networking standards, she says. On the other hand, "very often customers will set standards based on their own requirements." FDDI, for example, is on its way to becoming a de facto industry standard, and network vendors have widely adopted 62.5- μ m fiber-optic cable as the cabling system of choice.

Lanex's Greaney estimates a higher overall 1990 broadband market than does Chipcom's Lawrence: it will hit \$350 million, he predicts, a figure representing about 18% of a total LAN-equipment market of \$2 billion. Broadband Ethernet should nab a 13% share of the \$214 million LAN-bridge market by that time, he says.

Both Lawrence and Greaney believe the broadband market could be even larger if its benefits become better known. Besides its other attributes, broadband Ethernet matches baseband in giving users access to high-level protocols such as Transmission Control Protocol/Internet Protocol (TCP/IP), DECnet, IBM Corp.'s Netware, and OSI protocols.

Immunity to electrical noise is another big advantage in environments littered

with electric motors and similar equipment. Electrical noise affects baseband transmissions because the frequency spectrum it produces can interfere with baseband's Manchester-encoded waveforms. But broadband LANs operate at 30 MHz and up—well above the frequencies that manufacturers use for Ethernet.

MULTIPLE CHANNELS. Unlike baseband LANs, which send digital data over a single channel, broadband LANs transmit analog data over multiple channels at radio frequencies. Data originating in a baseband LAN must be converted to analog form by a modem to enter the broadband backbone. Frequency-division multiplexing is used to establish the channels, typically a half dozen in a band that is 300-to-400-MHz wide. Chipcom, for example, begins its recommended frequency allocation at about 5 MHz and runs up to 300 MHz.

Along with Ethernet, the most common choices of communication services on broadband networks include Manufacturing Automation Protocol/Technical Office Protocol (MAP/TOP) networks, PC networks, point-to-point low-speed modems operating at 9,600 Kbit/s, fire alarm systems, standard TV broadcast signals, and video teleconferencing.

Broadband channels are specified in 6-MHz increments, which is the bandwidth of a single TV channel. Like its baseband counterpart, broadband Ethernet transfers data at 10 Mbits/s and implements a collision-sense multiple-access/collision-detection protocol. The 10BROAD36 standard specifies 100% collision detection—something not all proprietary Ethernet-like broadband networks offer. A collision occurs when two stations on the network try to transmit simultaneously.

Baseband nets detect collisions by monitoring the dc content of the signal—a voltage drop indicates a collision and the messages are retransmitted after a pause. Since the rf signals of broadband nets are alternating current, however, there is no dc component to monitor. Instead, broadband checks on three possible events that would indicate a collision had occurred: an error in the transmitting-station's address; the possibility that the Ethernet controller is trying to transmit while it is receiving; and whether a specific part of the data packet—the unscrambled mode delimiter—is received when expected.

Over the past six months, vendors specializing in selling broadband-Ethernet products to OEMs and system integrators have rolled out an impressive assortment of new gear. Most important are two types of products: modems, which play the same role as transceivers in baseband networks; and bridges that attach baseband networks to the broadband cable.

Three companies now offer Ethernet modems compatible with the IEEE 10BROAD36 standard. Besides Chipcom

HOW BROADBAND ALLOCATES SERVICE

Application	Data rate	Bandwidth
Map token bus	10 Mbits/s	12 MHz
Ethernet	10 Mbits/s	12 MHz
PC network	2.5 Mbits/s	6 MHz
Point-to-point data transfer	9600 bits/s	50 KHz
Fire alarm system	38.4 Kbits/s	300 KHz
Television		6 MHz
Video teleconference		12 MHz

and Lanex, the third player is Fairchild Data Systems of Scottsdale, Ariz.

The company with the widest offering is also the granddaddy of the field: Chipcom, which introduced its Ethermodem family in 1986. Its Ethermodem III series lets users upgrade existing units by replacing frequency modules rather than buying all-new modems. Ethermodem III addresses the bandwidth-allocation issue, since it lets users choose the standard 18-MHz bandwidth or a 12-MHz bandwidth for maximum utilization of the network's total bandwidth. One-, two-, and eight-

ports connect the broadband network to any 802.3 baseband net, whether of thick or thin coaxial cable, twisted-pair, or fiber. Besides making the connection, it performs normal bridging functions. "It filters and forwards data between the subnetwork and the backbone," says Lawrence. "Data that does not have to go out on the backbone to reach its destination is isolated in the subnetwork."

Bridging is a strategic market for Lanex, says Greaney. Its LAN Express REM 8023 Remote Bridge fills the wide-area-network interconnection market for linking broadband Ethernet to telecommunications protocols such as T1 and CCITT V.35. The REM 8023 boasts a 4-Mbit/s data-transfer rate and supports network management and the spanning-tree algorithm commonly used therein. Lanex also has products that bridge broadband-Ethernet LANs to its own proprietary broadband network and to other broadband Ethernets.

Lanex will add a baseband-to-broadband-Ethernet bridge in the second quarter of this year, says Greaney, and intends to address other popular network protocols later in 1989. One upcoming product will bridge IEEE 802.5 token-ring baseband nets and broadband Ethernet. Next in line is a bridge between broadband Ethernet and FDDI networks.

Chipcom has taken a different tack in addressing fiber with ORnet, an implementation of Ethernet on fiber that offers 10-Mbit/s transmission, 100% collision detection, and interconnection with Ethernet devices within a network 2.5 miles in diameter. Looking ahead, Chipcom has provided a migration path to 100-Mbit/s FDDI by specifying the same fiber-optic cabling system as FDDI—namely, cables measuring 62.5- μ m in diameter.

Chipcom offers a solution to still another problem: networks that are so large that they exceed the 3,600-meter diameter specified for broadband distance. The Marathon Bridge, says Lawrence, uses the IEEE 802.4 token-bus specification developed for MAP/TOP networks to extend the total distance between the two most distant nodes to 26 miles. □

One new product extends broadband's 3,600-meter range to 26 miles

port modems are available, as are products for single- or dual-cable networks. Of particular interest is the new Ethermodem III PC. It allows an IBM PC AT or Personal System/2 to connect directly to broadband-backbone cable.

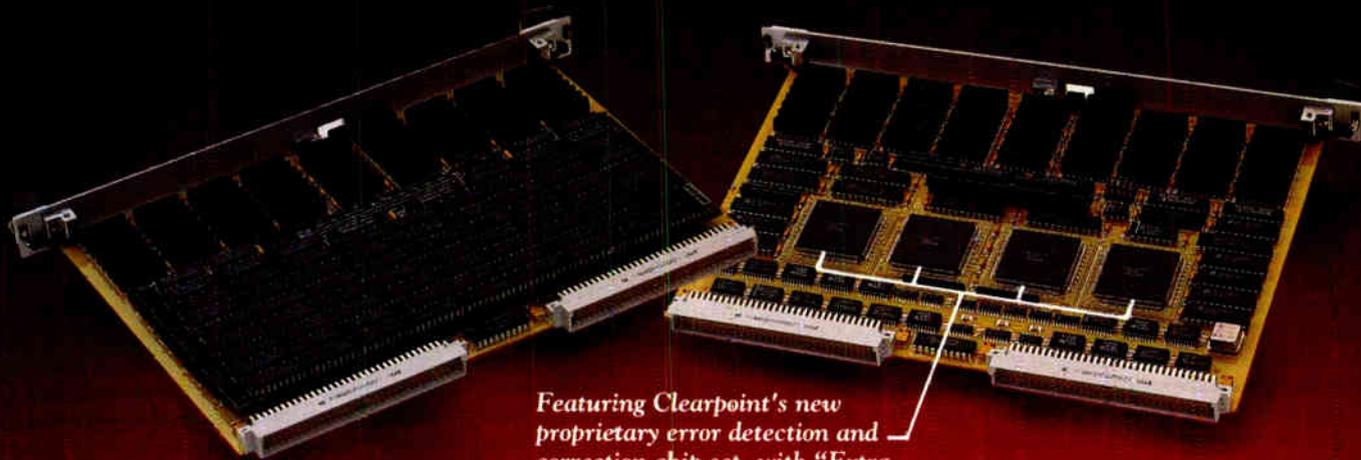
Also arriving late last year were Lanex's LAN Express TRN8023 modem and Fairchild's TOP M8023 modem. Both connect PCs, host computers, and terminal servers to the broadband network. The LAN Express comes in one-, two-, or eight-port models, runs on single- or dual-cable networks, and operates over an 18-MHz bandwidth. Fairchild's M8023 TOP-link modem is also a one-, two-, or eight-port device that operates on dual- or single-cable networks.

All three vendors offer modems that operate in the bandwidths specified by 10BROAD36, so customers who are just building a broadband net are assured of vendor interoperability. But for those who set up their nets before the standard was adopted—and may have allocated a service for that part of the spectrum—the three also offer optional bands.

To interconnect network LANs with a broadband backbone, Chipcom and Lanex both have a line of bridging products. Chipcom's Ethermodem III Bridge con-

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FUZZY LOGIC: IT'S COMPREHENSIBLE, IT'S PRACTICAL—AND IT'S COMMERCIAL

It simplifies tough problems and boosts the performance of real-time control systems

by Larry Waller

Proponents of fuzzy-logic technology concede they have problems getting people to listen. The term "fuzzy," pinned on the group of concepts when they were developed back in 1965, proved too colorful a moniker to shake. The trouble is, putting "fuzzy" and "logic" together creates a mental conflict, which is especially acute for potential users who cut their programming teeth on classical Boolean logic's clear-cut precision.

Despite the semantic hurdle, however, fuzzy logic shows all the signs of breaking out of the near-cult status it has gained since its sudden appearance as an esoteric mathematical concept. Although developed at a U. S. university, practical fuzzy-logic applications are being spearheaded by the Japanese. With fuzzy logic used for real-time control of a Japanese subway system, it's clear that the technology is not a blue-sky dream: it can be both practical and reliable. It offers major advantages in real-world commercial applications, particularly in expert systems, where it makes tough problems much simpler to solve and radically improves system performance.

The Japanese are developing fuzzy logic with a will, both at the software level and in chips designed to execute fuzzy-logic algorithms. At the same time, a U. S. startup has developed a fuzzy-logic microprocessor for a body of customers who, again, are almost all Japanese.

The appeal of this form of logic stems from its ability to provide a straightforward, systematic framework for using approximate reasoning to solve complex programming problems. This form of reasoning enables programmers to deal easily with the kinds of imprecise quantifiers—like most, many, few, nearly zero, infrequently, about 100, and so on—that typically abound in human thinking about real-world situations. The fuzzy-logic approach gives the programmer a simple, graphic way to represent the meaning of these linguistic terms that is both mathematically rigorous and makes "tuning" the representation of those terms an integral part of the debugging process.

Fuzzy logic wraps up in a single system the standard-logic approach and probability theory, so a system takes into account different levels of uncertainty in, for example, expert-system production-

rule evaluations. For practical work, it offers an entree to artificial intelligence developments—in contrast to the recognized complexity and disappointing results of conventional approaches in AI.

In Japan, fuzzy-logic hardware and software for industrial-control jobs are up and running in myriad tasks. Some 60 companies there, including the biggest names in industry, are reaping the first results of having plowed substantial research and development resources into the field during this decade.

By any standard, Japanese involvement can be described as mushrooming, says Lotfi A. Zadeh, who conceived the principles of fuzzy logic nearly a quarter century ago. A professor of electrical engineering and computer sciences at the

Most of the action is in Japan, but a U. S. startup now has a fuzzy-logic processor

University of California at Berkeley, his subsequent development of fuzzy logic, along with encouragement and consultation through the years, has earned him guru status among researchers.

The reason for the stepped-up pace is simple to fathom, he says, since the inherent nature of fuzzy logic so neatly fits the needs of this AI application. "Where human expertise is important [as in developing AI]," he says, "it is easier to express things in imprecise terms, the way people explain things verbally." Backers note that the less-complex programs are considerably smaller than equivalents done in conventional logic, up to an order of magnitude smaller in some cases.

FUZZY MOTORMAN. From its first use in 1980 in cement kilns in Sweden, one of the lowest-tech industrial-control tasks, fuzzy-logic hardware now has scored with one of the most demanding. A unit built by Hitachi Ltd., Tokyo, runs subway operations in Sendai, Japan, 200 miles north of Tokyo. It regulates train speed more precisely than the best human motorman and serves as a showcase for fuzzy-logic gear.

Similar hardware is going into elevator controls, and there are numerous units already controlling various automated pro-

duction sequences across the industrial spectrum. Scarcely a month goes by without additional experimental hardware appearing. A system for parallel-parking automobiles without driver help, for example, impresses Zadeh because no other AI approach has been able to solve this tough problem.

Not quite all of the action centers in Japan: the U. S. startup Togai InfraLogic Inc. in Irvine, Calif., is the only firm founded just to capitalize on fuzzy logic. Since its formation last August, the company has designed a commercial processor and is implementing it in silicon for its largely Japanese client base. Togai has also introduced the first fuzzy compiler, for its proprietary Fuzzy-C language.

Masaki Togai, the firm's chief executive officer, has devoted his career to fuzzy logic since doing his doctoral work on the subject a decade ago at Duke University in Durham, N. C. Later, at AT&T Bell Laboratories in Murray Hill, N. J., he and fellow researcher Hiroyuki Watanabe designed and built the first experimental fuzzy-logic processing chip.

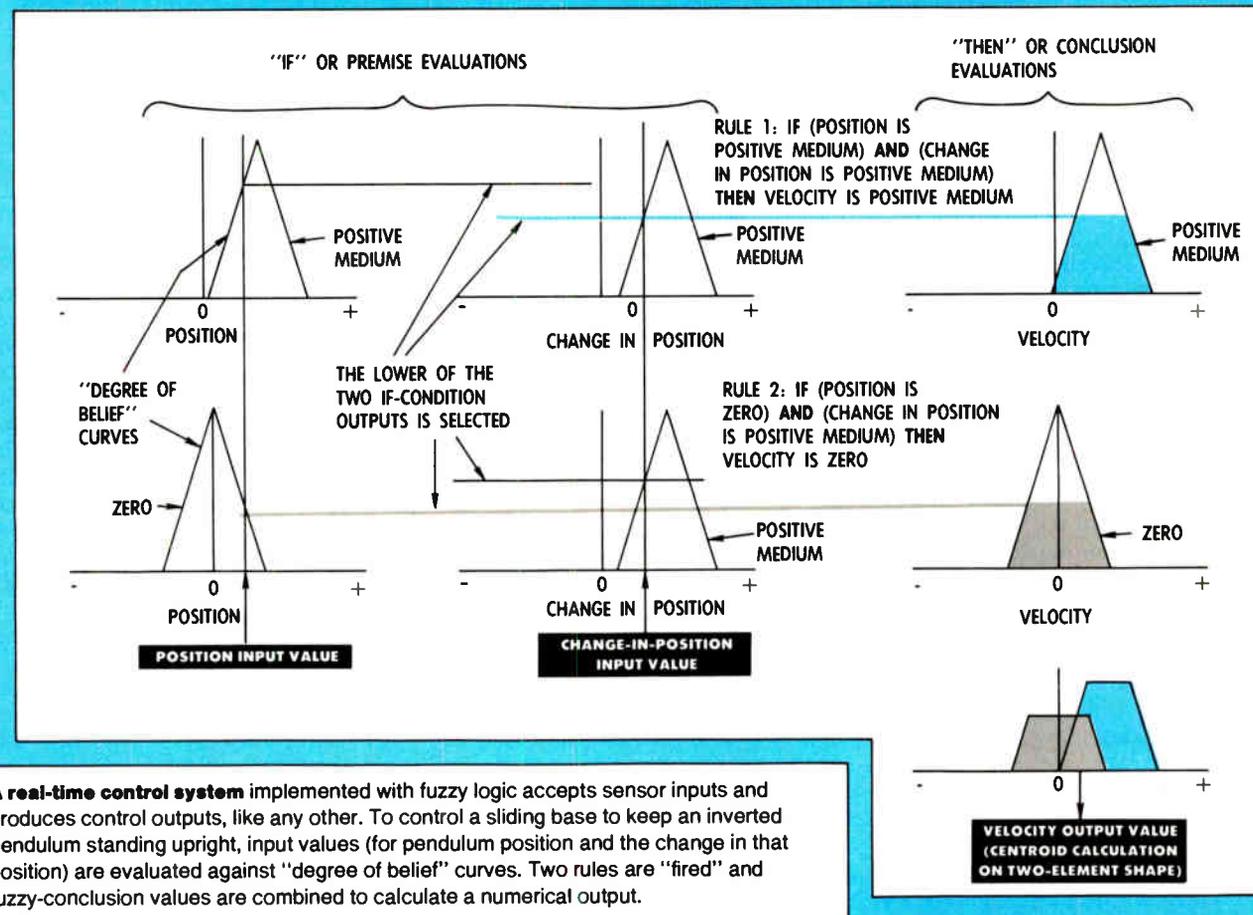
Togai InfraLogic is putting finishing touches on the final design of its microprocessor and will make samples available by summer for about \$90 initially. The FC110 Digital Fuzzy Processor is intended as an embedded-system central-computing element. Optimized fuzzy-logic instructions give the chip the power to run the key inferencing operations some 20 times faster than an equivalent compiled program running on a 80386-based system, the company says.

In tests, a simulated FC110 running at 10 MHz executes about 28.6 thousand fuzzy-logic inferences per second (Kflips), compared with 2.3 Kflips for a 20-MHz 80386. The device resembles an 8-bit reduced-instruction-set computer architecturally, but its instruction set and addressing modes are designed for a fuzzy-knowledge base stored on a separate read-only memory and expressed in Fuzzy-C.

The Togai compiler supplies a graphics interface and tools for writing knowledge-based production rules. The programs can run on a general-purpose microcomputer, and soon on the FC110.

The plan from the beginning "was to have all the development tools ready be-

HOW FUZZY LOGIC DEALS WITH UNCERTAINTY



A real-time control system implemented with fuzzy logic accepts sensor inputs and produces control outputs, like any other. To control a sliding base to keep an inverted pendulum standing upright, input values (for pendulum position and the change in that position) are evaluated against "degree of belief" curves. Two rules are "fired" and fuzzy-conclusion values are combined to calculate a numerical output.

fore the chip," Togai says. But "we face a massive education task in teaching users an entirely new system." What makes it so different from conventional programming, of course, is that "there are no absolutes." The Togai compiler is the tool designed for developing expert systems that typically use a lot of imprecise information. Togai training material shows an experienced programmer how to describe in fuzzy-logic terms the "vague approximations embodied in [human] language," says Togai.

A BLACK ART. Handling the "membership functions" or "degree-of-belief curves," which are key descriptive elements that must be determined for any production rules in the knowledge base, for example, can be "somewhat of a black art," says Carl Perkins, vice president for business development at Togai. New terms must be learned, too, such as "defuzzification," which is a means offered by the compiler for generating a "crisp" data output—an actual numerical value—when needed. One way of defuzzifying is the centroid method, which produces the output by a center-of-gravity averaging technique. Another defuzzifies by picking an average of a centroid and other values.

The company has a training program on a floppy disk for personal computers.

It illustrates fuzzy-logic principles through an example: controlling an inverted pendulum. The fuzzy controller uses sensor inputs for pendulum position and movement, evaluating those inputs with production rules to produce a control output for moving the base the pendulum stands on. By sliding the base back and forth, the controller balances the inverted pendulum, like a vertical rod balanced on the palm of a hand (see diagram).

The input values are evaluated as points on degree-of-belief curves. The curves have been arranged to approximate the meaning of linguistic expressions like "the position of the pendulum is zero." The expression indicates that the pendulum is at the zero-position angle, corresponding to the straight up, or balanced, position. Another expression, "the position is positive medium," means the pendulum is slightly to one side of the upright position.

Different points on one curve indicate the degree of belief, or the probability level, that the position is zero: belief is at its maximum exactly at zero, but belief tapers off gradually, rather than abruptly, as values diverge from the zero point. Simple triangular curves are often sufficient, says Perkins, but smoothing them

out into bell-shaped curves can sometimes improve system accuracy.

Potential users may balk at the notion that some odd shape representing combinations of a very few "belief values" about where the pendulum is and how much it has moved can be used to perform this tricky real-time balancing act. But when they've gone through the demonstration, two things stand out: it's easy to set up, and it works very well as a solution to a complex problem.

Togai estimates that 10% of expert-system implementations will incorporate fuzzy logic in the near future. Consumer and business equipment have the most potential. "As soon as a fuzzy processor is built into an appliance or office-automation device, competing manufacturers will be forced to follow suit to maintain market share," he says. Some U. S. companies have projects looking at fuzzy logic, though at a pace well behind Japan.

The bedrock advantage comes from simplicity and the fact that when working with classical logic, "precision is expensive." One reason the Japanese lead the fuzzy-logic pack is that "they have found they don't need high accuracy in many applications and there's a significant payoff [from fuzzy logic]," Zadeh says. □

THE MOVEMENT TO VXIBUS IS GATHERING STEAM QUICKLY

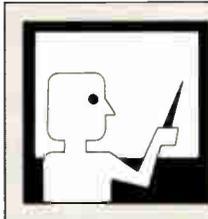
Designers and users alike benefit from the standard for modular instruments

by Samuel Weber

A little more than a year and a half ago, five major instrument makers formed a consortium to promote the VXIbus, a modular-instrument standard based on the VMEbus and open to all manufacturers. Now the standard is making ripples in the instrumentation industry, and the ripples seem certain to swell into waves over the next 10 years.

Started by Colorado Data Systems, Hewlett-Packard, Racal-Dana Instruments, Tektronix, and Wavetek in July 1987, the consortium now numbers 10 member companies. Seventy-eight instrument makers have signed up to support the standard. And VXIbus-compatible products are starting to make their way to market.

The appeal of the VXIbus is the new power and flexibility the standard could ultimately provide for system designers



EXECUTIVE BRIEFING is a monthly feature of Electronics that provides managers with a concise review of developments in fields that are making frequent headlines.

and users alike. It governs the use of modular instruments, or instruments on cards. Such tools can lower the cost, size, and weight of automated test systems, a fact that has for some time made them attractive to designers and users. But more importantly, modular instruments using the VXIbus can also provide performance beyond that of rack-and-stack standard instruments governed by an older standard, IEEE 488, also known as the General-Purpose Interface Bus. They can also outperform instruments on cards in per-

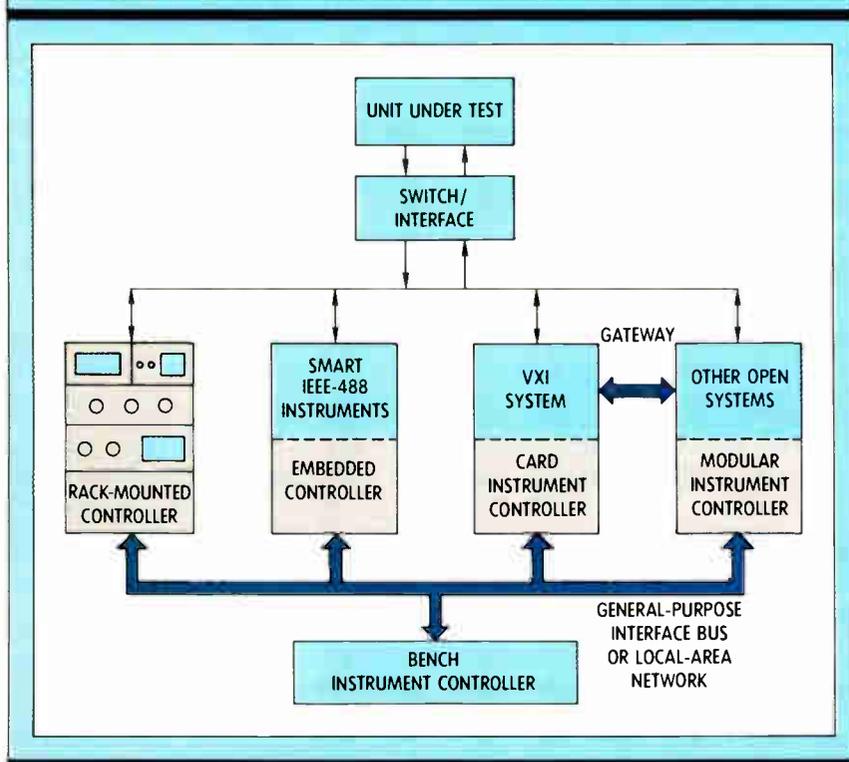
sonal-computer-based systems.

The concept of modular instrumentation is not new. Instrument houses such as Colorado Data Systems, HP, and National Instruments have been offering for several years product lines that operate under the control of proprietary controllers or personal computers linked by industry-standard interfaces such as RS-232 or IEEE 488. Cards have proliferated, along with the software designers need to put together systems by plugging cards into the IBM Corp. PC AT or XT bus, the Personal System/2 via Micro Channel, or the Apple Computer Inc. Macintosh II via NuBus. But the card makers must provide functions that can operate in all four environments. And with a General Purpose Interface Bus link, the system can never be faster than GPIB allows—less than 1 Mbit/s.

VXIbus is open and nonproprietary, so it allows a wide range of instruments, interfaces, and computers from different manufacturers to be plugged into the same chassis and to function compatibly. And it retains the ability to connect with GPIB, PC, or other types of controllers. At the same time, VXI overcomes some of the major limitations of GPIB, mainly slow data transfer and the need for precise timing coordination among the various instruments in a system. It achieves this by placing all of a system's instruments within a common frame and plugging them into a common high-speed bus. That means a system designer can mix and match functions from a multiplicity of vendors, giving him a wider spectrum to choose from to meet the requirements of his application. And designers get all the performance advantages permitted by the tight coupling of a variety of instrumentation functions through the high-performance VMEbus.

FAST RAMP. Despite its advantages, the speed with which the standard is catching on has surprised a lot of people. The reasons aren't hard to figure out, says Allen Hollister, chairman of the VXIbus consortium and program manager for VXI at Wavetek Corp. in San Diego. "From a technical point of view, it's a giant leap forward over the standard GPIB rack-and-stack instruments," he says. "From a market point of view, there has been a much greater response than I expected.

TYING TOGETHER MULTIPLE INSTRUMENTS



With VXI, a measurement system can combine rack-and-stack instruments, GPIB-controlled instruments, and now modular instruments in one environment.

Having 78 manufacturers out there building to the standard at this point in time is tremendous, considering the short time it's been out."

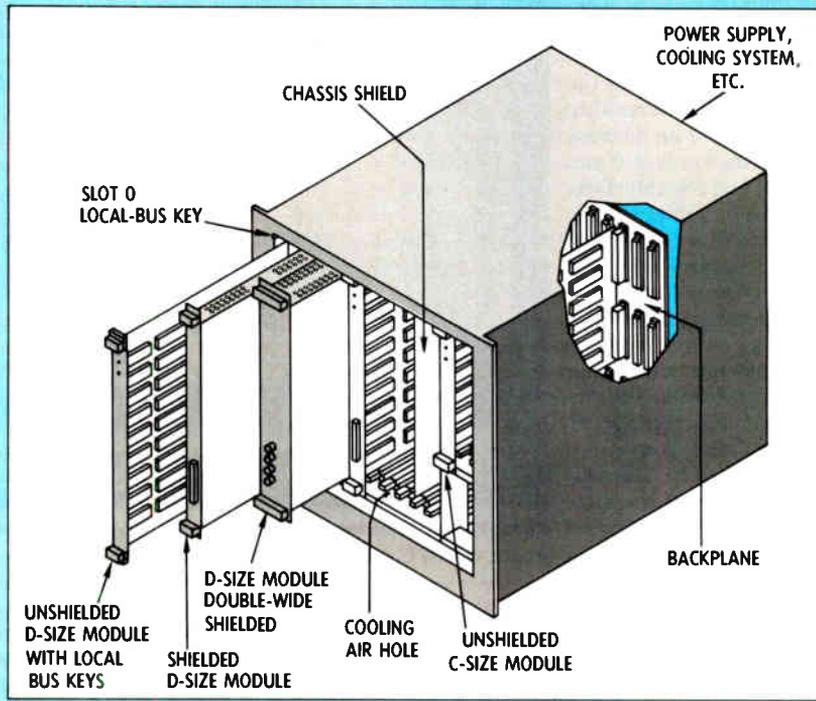
One reason is that competitive and technological pressures won't let instrument makers or users ignore VXI. "Anybody who has been involved with the GPIB in the past in any way, whether they're an instrument manufacturer or a GPIB user, is interested, because it will directly affect their applications," says Ron Wolfe, strategic marketing manager for National Instruments Corp. in Austin, Texas. "Today's marketplace is kind of like what you see when sharks get into a feeding frenzy. If you just get it started, it will fuel itself, because everybody's so scared of getting behind their competitors that they can't afford not to learn about it right away."

Galen W. Wampler, an industry analyst and president of Prime Data Corp. in San Jose, Calif., agrees with that prediction. He estimates that within 10 years, 20% of what will then be a \$10 billion test-instrumentation market will be dedicated to VXI-compatible products. He says that 40% of this market will be what he terms "computer-dependent" by the year 2000, and half of that will belong to VXI. "It will be a strong growth factor for the instrument industry," he says, "particularly for high-performance instruments now in the \$1,000-to-\$3,000 range, and more complex measurement systems up to \$20,000." Another observer—Malcom Levy, the marketing manager of Racal-Dana in Irvine, Calif.—reckons that VXI will constitute one third of the automatic test equipment market within five years.

MATE SUPPORT. A major factor in launching VXI was its adoption last July by the U. S. Air Force as the instrument-on-card standard for its Modular Automatic Test Equipment, or MATE, program. The Air Force got involved in 1985, when it asked the MATE User's Group for recommendations on standardizing instruments on cards. The request came as part of a general push by the military to cut the size and weight of test equipment and reduce the number of different kinds and sizes of boxes it was using. The Army and Navy formed similar programs, but eventually elected to go with their own, less commercially oriented, standards. The Air Force, though, wanted to use as much commercial equipment as possible, leading it to the VXIbus.

Early in 1987, technical discussions and exchanges among instrument manufacturers began, aimed at developing commercial and military modular-instrumentation standards based on the VMEbus. A proposal to establish an IEEE working group was submitted to the IEEE Standards Board, which approved the formation of the P1155 working group. The five-member consortium submitted ver-

MANY INSTRUMENTS, ONE FRAME



Putting all instruments in a common mainframe, like this D-size model, and plugging them into a high-speed bus helps to overcome GPIB limitations.

sion 1.1 of the VXIbus specification to the working group in October of 1987 and, after verification of interoperability of early products, followed it with version 1.2. Recently, IEEE P1155 adopted version 1.2 as a base document for consideration as an IEEE commercial standard. Official

Competitive pressure leaves users and vendors no room to ignore VXI

adoption is virtually assured. Thus, the VXIbus standard stands beside the GPIB standard as one of the watershed developments in shaping the future direction of test instrumentation.

The VXIbus specifies three addressing techniques that can be used in an IEEE-488-to-VXIbus interface. These are designated IEEE 488 primary addressing, IEEE 488 secondary addressing, and embedded addressing protocols.

With primary addressing, each VXI instrument appears to the host controller as a separate IEEE 488 instrument with its own address, command, response, status code, and state storage. The interface must recognize each of the VXIbus devices through its IEEE 488 address and interact with each for reads, writes, serial polls, and so on. This results in a considerable overhead of lost time between trans-

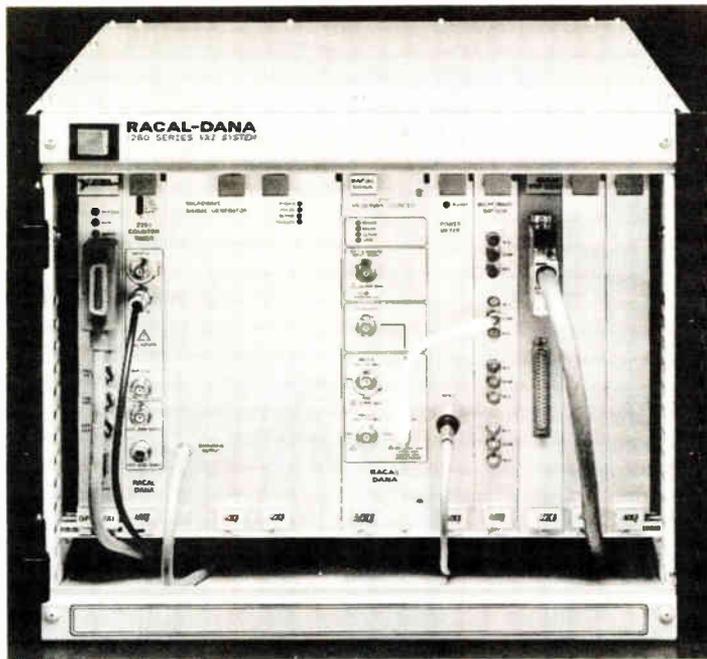
actions. The advantage is that software packages, tools, or drivers designed to work with IEEE 488 instruments will work with their VXI equivalents with only an address change required. One disadvantage is that there are only 31 primary addresses available, so conflict could arise in a multiframe system.

Secondary addressing is the method most commonly used, because it maps GPIB onto VXI in a straightforward manner. It is similar to primary addressing, but with it a single primary address designates the entire VXIbus system, using IEEE 488 secondary addresses to route 488 communications to or from VXIbus instruments in the mainframe. With this method, the 488 primary address locates the particular 488-VXI interface, then, via the secondary address, locates the specific VXI instrument within the system.

The third method, embedded addressing, can be used to link VXI systems to non-GPIB controllers. Here, a single unique address is assigned to the VXIbus system. A header is attached to each message identifying its destination device.

Which approach is best to use is a subject of some debate among the VXI consortium. Tektronix Inc. believes the embedded addressing system offers a number of advantages for what it calls the "superinstrument" concept the company favors. "What we're doing is using the idea of a single-primary, single-secondary address, so that the collection of VXI in-

struments looks like a single superinstrument," says Dave Haworth, VXI program manager at the Tektronix Measurement Systems Division in Vancouver, Wash. "Instead of using the 488 hardware addressing codes, you have an address header in the command you send to it, and this interface, called slot 0, will appropriately route that to 488.2 instruments sitting in the VXI frame," he says. "Basically, instead of tying it to a specific interface—depending on the 488 interface addressing scheme—you can pull the interface out and put in a local-area network. You could send the embedded addressing information in the message from the LAN to the controller, or it can be in a computer bus-structure extension."



Racal-Dana's mainframe for rf and microwave instruments holds modules from a variety of other instrument vendors.

The result is "software control of embedded addressing, and you don't tie yourself to the conventions of GPIB."

However, Hewlett-Packard Co. favors the first approach, the single-primary, multiple-secondary addressing. The Palo Alto, Calif., company wants to preserve the relationship between VXI and HPIB, its version of IEEE 488. Not only is it simpler to use, the company argues, but it permits expanding the number of addressable devices in a GPIB-controlled system to more than 900. HP believes that when used in an IEEE 488 system, embedded addressing produces serious performance degradation. It requires the interface module in the VXIbus chassis to store, check, parse, and match each string before relaying the command to the appropriate module. The company concedes that for RS-232 or other serial links to VXIbus systems, embedded addressing is required.

National Instruments also feels that embedded addressing is very difficult to

use, pointing out that at present there is no agreement as to how to do it in some standard way. An IEEE committee, P1174, has been formed to come up with one. "We're using secondary addressing, because it's real specific about GPIB," says National's Ron Wolfe. "But the minute you say you're not using GPIB, you're using a serial port like RS-232, which doesn't have any addressing scheme, or Ethernet, say, then secondary addressing doesn't make any sense."

Because embedded addressing lets the system designer use logic addressing instead of the hardware addressing specified by VXI, Wolfe points out, you can have processors on cards, or actual instrument modules, or a subroutine in a library on some processor module. "You can literally have thousands of instruments or functions in your system that can be addressed and used in one consistent manner, and you don't care if it's hardware or software," he says. "Embedded addressing also lets you get many

layers below the secondary-layer-only [level] permitted by secondary addressing. If you have a commander/servant configuration that's four layers deep, with secondary addressing there's no way to get down to the bottom," he says. "With embedded addressing, the header can be used to route messages down to all the layers. Where it gets hard is if you get down to the fourth or fifth layer, and it wants to interrupt: how does it get back to you? That hasn't been addressed as yet. That's one of the specific problems the committee is addressing."

Whether VXIbus instruments can cut it in the rf and microwave realm is another point of contention in the consortium. Hewlett-Pack-

ard contends that VXI specifications are not capable of handling the electromagnetic-interference shielding requirements of this range of equipment. It has developed its own open-standard architecture for rf- and microwave-level equipment, called the Modular Measurement System.

But Malcolm Levy, at Racal-Dana, believes that VXI is perfectly acceptable for rf instruments. "The major problem is that instruments being as close as they are, can we get the rf performance in a VXI instrument? We believe the answer is yes." Helping to prove his point, Racal-Dana showed the company's first rf and microwave VXI instruments at ATE West, held in Anaheim, Calif., in January.

So far, only a limited number of VXI-compatible products of any kind are available, but the number is growing and their dearth has not seemed to discourage potential users. "I thought there would be a few years' delay, but people started calling up wanting to get products almost immediately when VXI was announced,"

BUILDING AN INSTRUMENT STANDARD AROUND THE VMEbus

The VXIbus takes its name from "VMEbus Extensions for Instrumentation." As the name implies, it uses the VMEbus standard (IEEE 1014) as a base and supplements it with features appropriate for instrumentation systems, without changing the basic VME specification.

A VXI-based system consists of a mainframe chassis and backplane connections for mounting plug-in modules, or cards. The system may consist of up to 256 devices, including one or more VXIbus subsystems. A VXIbus subsystem consists of a central timing module, referred to as slot 0, with up to 12 additional instrument

modules. These 13 modules will fill a standard 19-in. cabinet, mounted vertically on 1.2-in. centers. Users can interconnect multiple VXI chassis with the help of bus extenders.

The VXIbus uses the standard Euro-card A and B module sizes specified by VMEbus, but adds two larger sizes, C and D, all of which are spaced on 1.2-in. centers. The A board has a single 96-pin connector known as P1, while the B and C boards have an additional connector, P2. P2 adds a 10-MHz emitter-coupled-logic clock, ECL and analog supply voltages, ECL and TTL trigger lines, an analog

summing bus, a module-identification line, and a daisy-chain 12-bit structure known as the local bus. This local bus can be largely defined by the module manufacturer. The largest module, the D-size board, is aimed at higher-performance instrumentation. It adds a third connector, designated P3, which not only provides the same resources as P2, but adds a 100-MHz clock and synchronization signal and additional power-voltage lines, six additional parallel ECL trigger lines, and a two-line, so-called STAR bus to provide bidirectional communication between each instrument module and slot 0. —S. W.

says Larry Desjardin, research and development section manager at HP's Loveland Instrument Division. "We announced our E1400A mainframe in August of last year, although we were shipping it earlier—in March—to some customers. That was before there were any instruments available. You wonder, if there are no instruments, why would they want cages? Well, we found that people were using them to develop their own custom modules for some unusual functionality they needed."

That kind of interest is still a little unusual, says Lou Klahn, marketing manager for Colorado Data Systems Inc., Inglewood, Colo., a company that helped pioneer the instrument-on-a-card concept. "There's been a big rush toward developing product and a lot of interest on the part of the customer," Klahn says. "I don't think that a lot of customers have put forth their hard-earned dollars yet, but I think that's primarily a budget-cycle problem as opposed to anything to do with the technology or the standard itself."

One possible reason for the deliberate pace with which products are being introduced is the fact that some sophistication is required of both designers and users of VXIbus instrument systems. Designers already familiar with VMEbus standards will not have a lot of difficulty with the VXI extensions. However, those who were used to putting rack-and-stack systems together via IEEE 488 will miss the knobs and displays that enabled them to set up and adjust the equipment.

VIRTUAL KNOBS. But more products are starting to appear. In fact, the lack of knobs and displays is itself giving rise to a whole class of products: software tools that produce virtual instrument displays on a PC screen. They include National Instruments' LabWindows, an MS-DOS-based tool that permits program creation and operation through a library of instrument control functions. LabView, a similar package for the Macintosh, is also available from National. Wavetek's Wavetest and HP's newly introduced Interactive Test Generator are equivalent tools. Although designed initially for the PC-based instrument-on-a-card market, they can easily be adapted to VXI through a GPIB interface such as National Instruments' GPIB-VXI or Colorado Data Systems' 73A-151. In fact, at the ATE West show in January, National showed a version of LabWindows designed to work directly with VXI systems, although it is not yet a product.

VXI-system-development tools and mainframes are also becoming available from several companies, among them Colorado Data Systems, Hewlett-Packard, and Tektronix. For those ATE system designers who want an optimum match between the high performance of

THE AIR FORCE AND NASA MOVE ON VXI

Air Force support is a big factor in the development of VXIbus. One of the first major military contracts based on the standard is a deal worth \$72 million for the Corsair Avionics System Tester. CAST is automatic test gear for testing the bombing and navigation systems of the A-7 aircraft. Allied Signal Test Systems' Teterboro, N. J., division expects to complete a prototype in May and deliver production units next January.

"VXI allows us to use standard, available, off-the-shelf instruments," says Lawrence Gioielli, engineering manager for the A-7 at Allied Signal. "So the real saving isn't just up front—it's in the life-cycle costs. If you had a group of unique instruments, the Air Force would have a

hard time supporting the system in the future. With VXI, you can add devices when you want. If I design my own bus, it's a whole new system for the Air Force to learn and support."

Another major use of VXI will be in a Hewlett-Packard Co. automatic test system for Rockwell International as part of the space-shuttle program. The system is actually being designed and built by Tasco Electronic Services Inc. of Anaheim, Calif. It will include several commercial modules, says Carmy Yellin, a Tasco senior system engineer. But its core is a Tasco-designed programmable serial word generator, recorder, and analyzer built to VXI standards. Tasco plans to offer the unit as a product. —S. W.

the VXIbus and the breadth of software afforded by direct PC control, Radix Microsystems' EPC-2, and the 73A-160 VXIbus-compatible personal computers will be welcome. They are 80386 and 80286-based PC ATs, respectively, which are designed to plug into VXI C-sized mainframes. They not only provide IEEE 488 interfaces, but can also act as complete VXI resource managers. "If you have a PC embedded in a VXI environment, you

Using VXIbus demands sophistication, but software is making it easier

end up with a very high-performance system, because you're not using the slow GPIB interface to communicate and transfer data back and forth," says Glen Myers, president of the Beaverton, Ore., company. "Also, the PC world has a tremendous amount of software available that will be useful in a VXI environment. To us it makes sense to put the PC in the mainframe and have the PC have direct access to the instrument at the full bandwidth of the bus, to be able to drive the TTL and ECL trigger lines from the VXI backplanes directly." Tektronix, which owns 40% of Radix, showed its own D-sized version of the EPC-2, designated the 5530, at ATE West.

National introduced one popular interface product early in the game. Its GPIB-VXI board performs transparent conversion of IEEE 488 signals and protocols so that an IEEE 488 controller can control VXIbus instruments alongside IEEE 488 instruments.

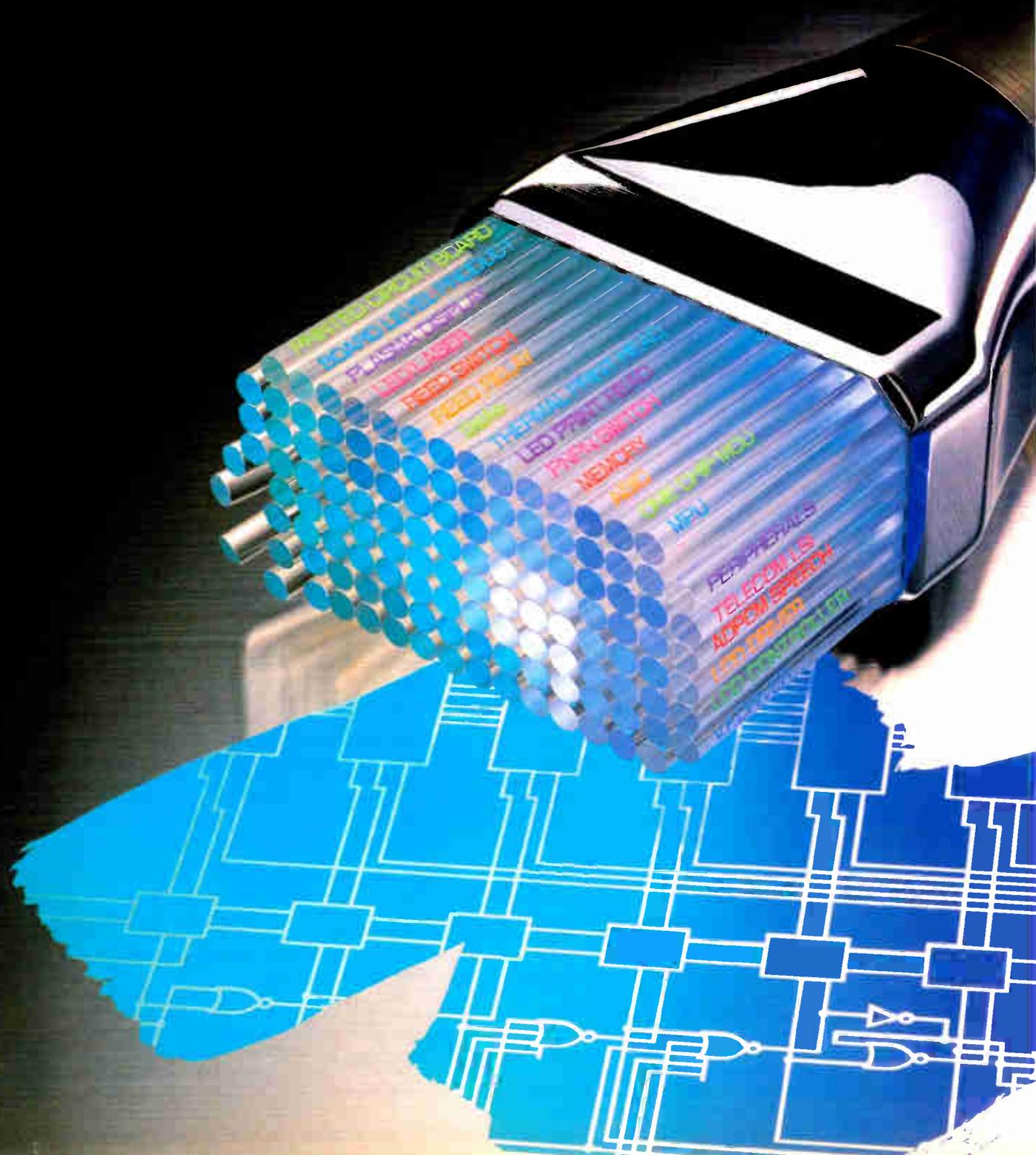
Even after VXI-compatible products start appearing in larger numbers, nobody expects that VXI is going to replace GPIB any time soon. Neither will the VXI products eliminate monolithic bench in-

struments. "IEEE 488 go away? I don't think so," says Radix Microsystems' Myers. "I think there will be a short-term tendency for anyone who has an idea for the world's best next instrument to do it both for 488 and VXI, and then there'll be some point when people won't consider 488 any more."

Others, like Colorado Data Systems' Klahn, point out that some types of instruments—spectrum analyzers, for example—do not lend themselves to modularity. And Bo Ray, vice president of marketing for Rapid Systems Inc., a manufacturer of instruments on cards for PCs, says, "VXI is a great standard, and will be very important. But a majority of instrumentation situations call for a single instrument. The cost of PCs is coming down and the power is going up, and a lot of software is available. So we see a continuing market for PC-instrument cards in a cost-conscious environment."

Not everyone is so sanguine about the future of monolithic benchtop instruments or non-VXI PC-based instruments. "I think in the long term, the days of the instrument panel with control buttons and little displays are over," says Richard Faubert, vice president of product development at GenRad Inc. in Concord, Mass. "VXI with instruments on a card and some kind of PC with windows is the way to go." GenRad sees VXI as a useful adjunct to the automated test equipment business, but without a major impact on ATE itself.

"We have a development effort to get ourselves ready to be able to provide custom options—it isn't that we will have a fixed set of instrumentation available," Faubert says. "It will be used by the custom-products operation where that group can add instrumentation, particularly analog, at customers' requests. We're trying to get up to speed to be able to select and integrate VXI boxes into the mainline system." □



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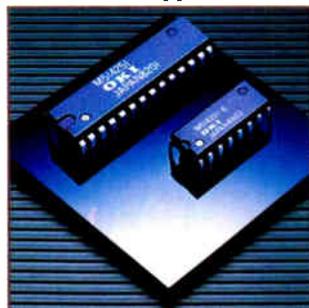
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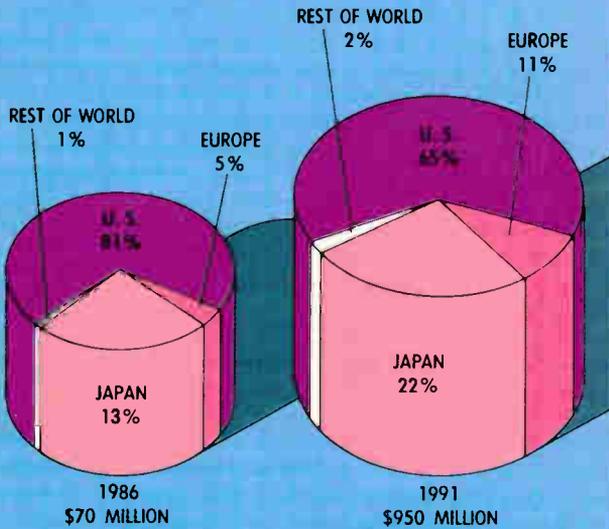
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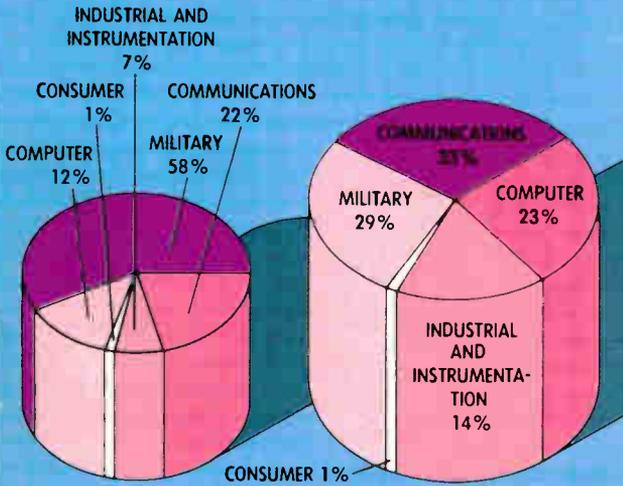
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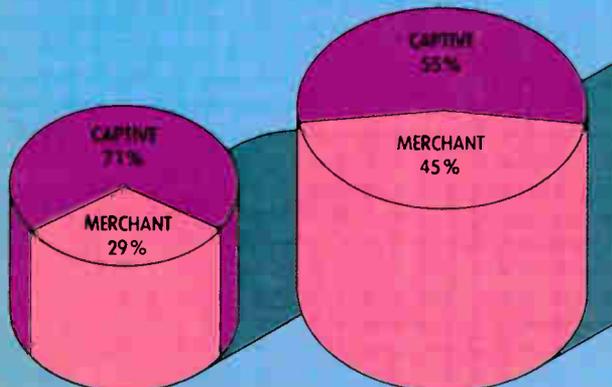
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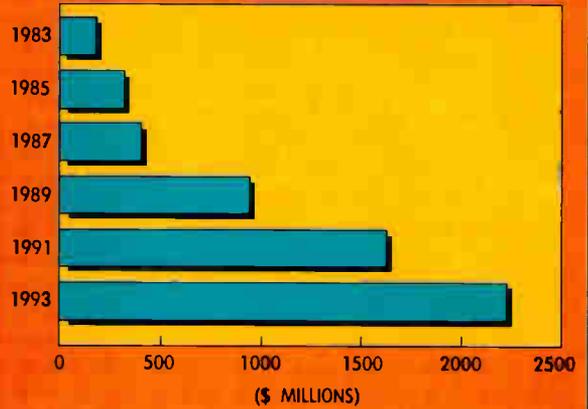


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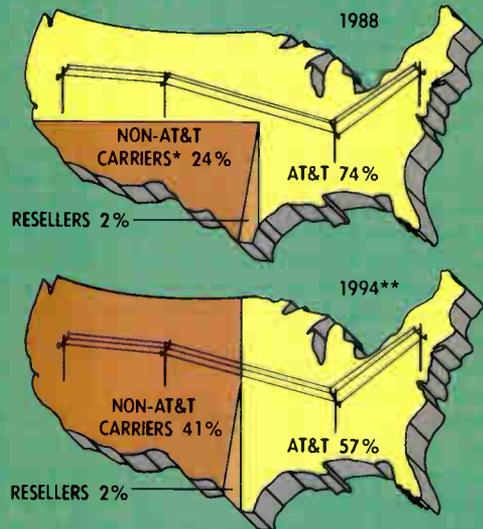
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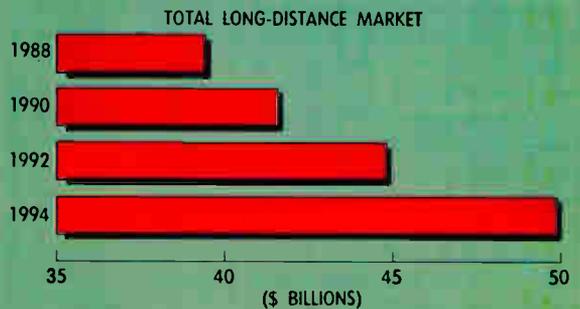
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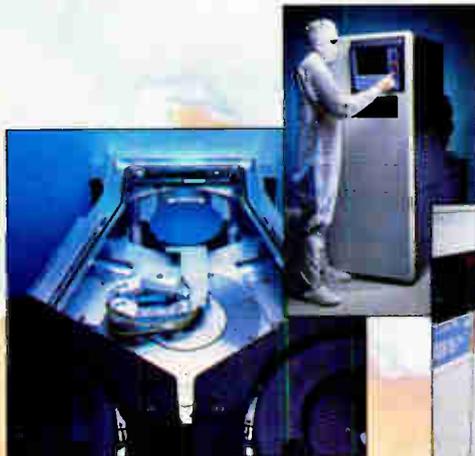
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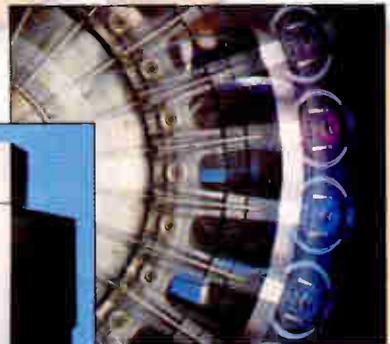
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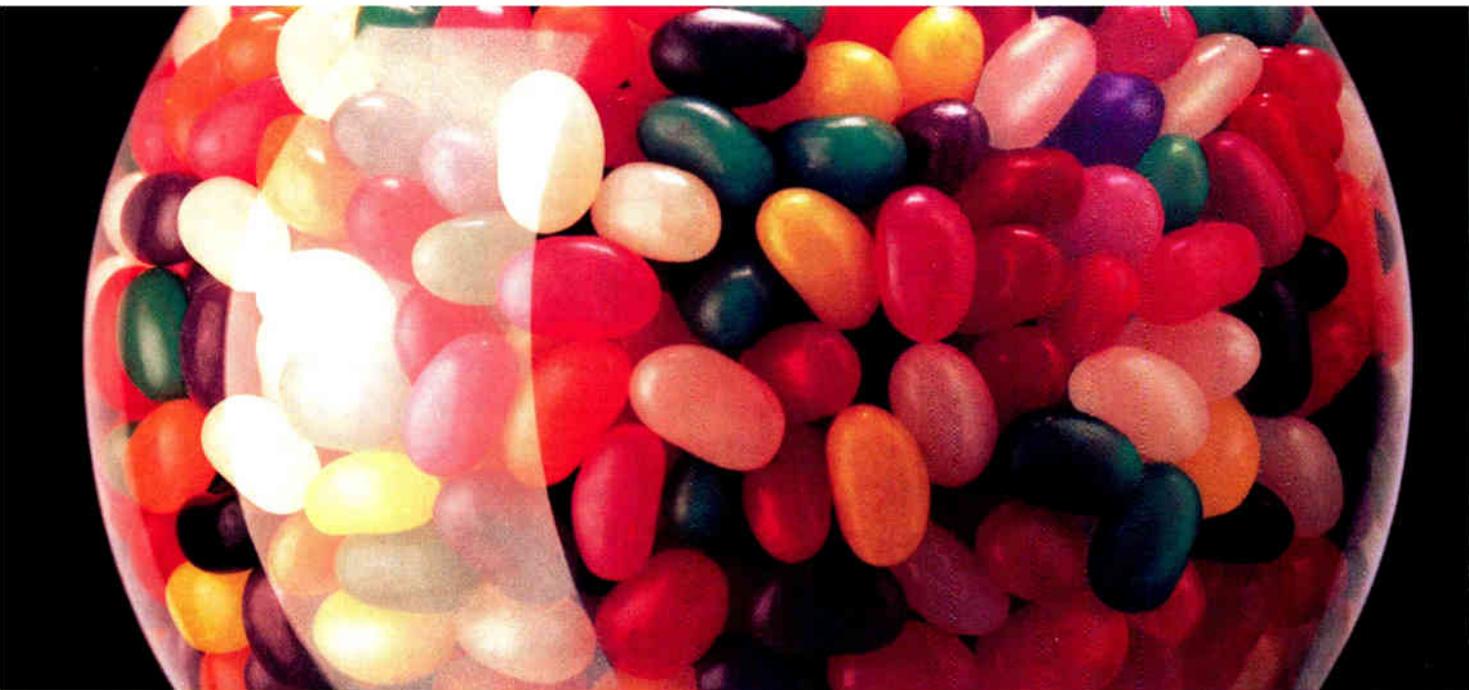
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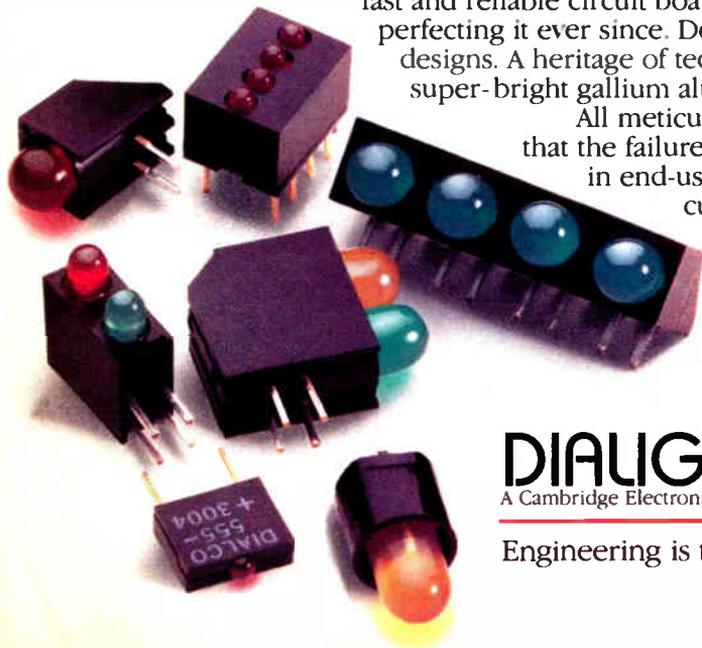
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A FIVE-YEAR PLAN THAT REALLY WORKS

At Analog Devices, detailed agendas spark growth

Five-year plans are helpful corporate strategic-planning tools, but it's doubtful that many of them are as detailed, involve as many people, or are as public as those that guide Analog Devices Inc. They force Analog to analyze what kind of company it is and should be, and they also force a consensus commitment among senior managers. The current version, covering 1988-1992, is the fourth. It embodies ideas from 150 people on 16 committees and task forces and was almost two years in the making.

Something else about the plans: they seem to help stimulate growth at Analog. Since the company wrote the first one in 1972, revenue growth has averaged about 25% a year—from \$15.6 million that year to \$439 million for fiscal 1989, which ended last Oct. 31.

Not all the plans have met all the goals of the Norwood, Mass., manufacturer of analog and digital signal-processing products—primarily integrated circuits. The most painful and glaring failure was the anemic growth performance of the company in 1985 and 1986, says Ray Stata, chairman and president.

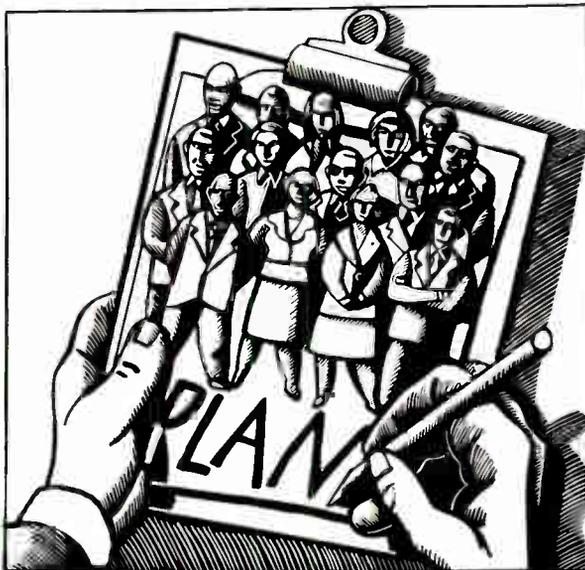
With the plan calling for revenue growth of 27% and 12% in those years, the actual increases were just 3% and 4%. Stata attributes the low growth to "an unusually violent boom-bust cycle of semiconductor production and inventory accumulation."

As the driving force behind the five-year-plan concept, Stata says that he has been pivotal in formulating and executing the schemes. However, his input has diminished over time as he has deliberately involved more senior planners. "But the CEO has an important role in setting expectations for the planning process," Stata says. "Equally important, when the plan is finished, the CEO has a unique responsibility to communicate the plan," both inside and outside the company.

There are 11 major objectives in the

current program. A key one is revenue growth of 20% per year and return on capital of 15%, both figures outpacing the industry average. Achieving the revenue-growth goal would make Analog Devices a \$900 million corporation in 1992.

Some of the plan's other objectives



aren't as easily measured but are no less important, Stata says. Those include meeting employee expectations for employment security and personal growth; achieving excellence in low-cost, high-volume manufacturing; and achieving continuous organizational learning and improvement.

The foundation for the plan was laid almost two years before it was finished, with formation of a strategic planning committee. The early meetings were essentially brainstorming sessions among top management to determine corporate objectives "and identify the significant things we had to change as a company—the imperatives for change," Stata says.

The strategic planning committee spun off task forces, which were charged with addressing, among other issues, human resources, quality improvement, and diversification. The task forces in their turn have evolved into several standing bodies, including

by Lawrence Curran

groups on business planning, human resources, and information systems, plus a quality-improvement steering committee. They meet at least once a quarter to monitor progress.

The "imperatives for change" that grew out of the current plan included recognition that the company needs to penetrate new markets without losing its leadership in those it dominates; become both a product innovator and low-cost producer; and improve in customer performance ratings.

Becoming a low-cost manufacturer involves a fundamental change and directly affects the firm's ability to crack new markets, company executives say.

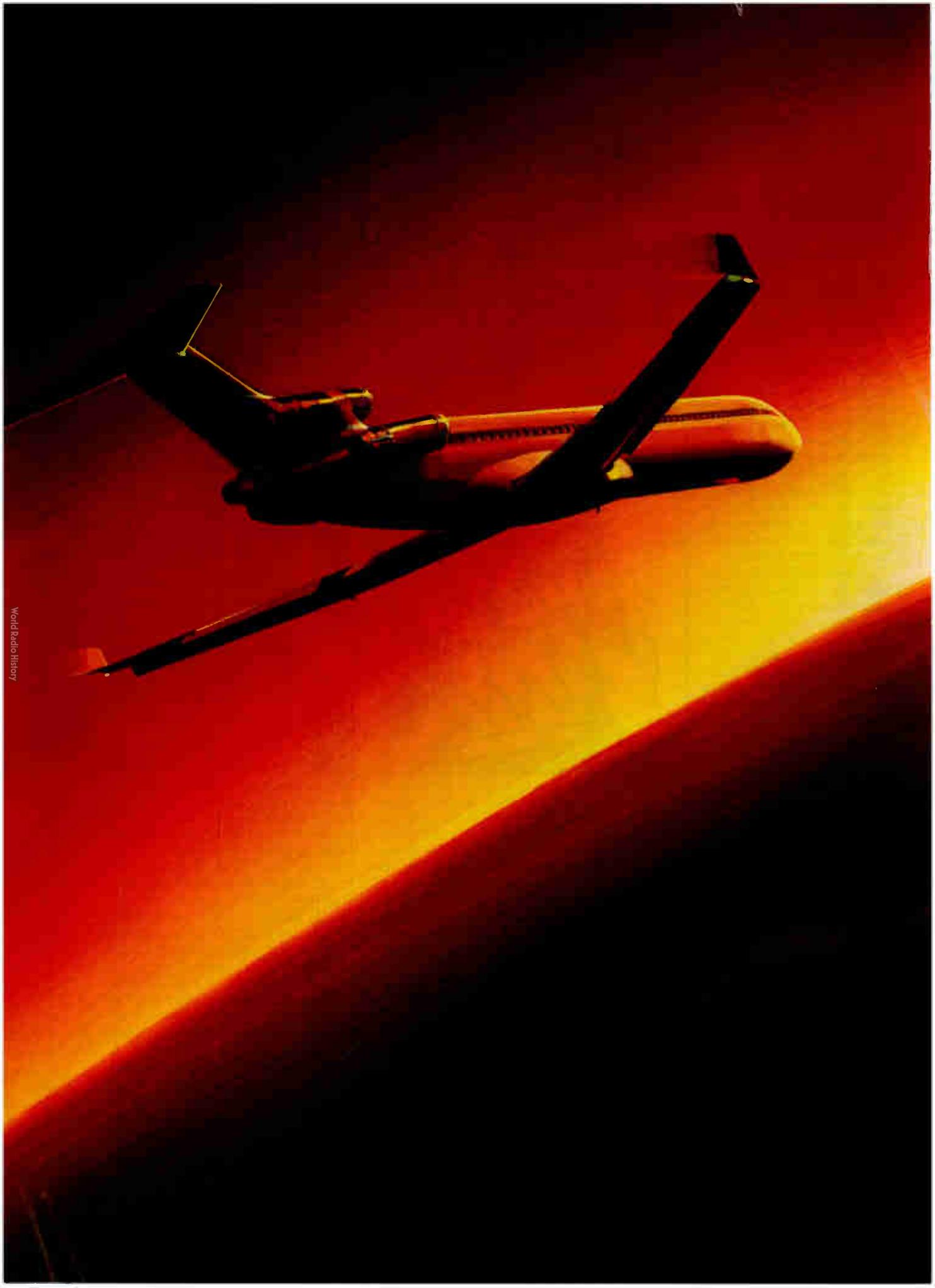
Historically, Analog's proprietary-products business has involved high-performance, relatively high-priced linear and mixed-signal ICs produced in much lower volumes than are digital circuits like dynamic random-access memories. Consequently, the firm had assigned relatively low priority to economical high-volume manufacturing.

But that's changing as the company moves to provide components that are used in consumer audio and video equipment as well as in disk drives, all of which must be produced in high volume at competitive prices.

Another of the plan's objectives resulted in the formation of a quality-improvement program. That goal grew out of the company's recognition that although Analog Devices may be the market-share leader in a number of product categories, "we didn't stand out in the minds of our customers as leaders in quality and service," Stata says.

The quality push was actually launched before the current plan was written. But Analog has seen fit to make quality improvement one of the plan's 11 objectives: to achieve leadership in vendor ratings as measured by on-time delivery, low rejection rates, and overall responsiveness to customers' wishes.

Finally, while some may wonder how the five-year plans affect Analog's competitive position, Stata points out that the amount of market, technology, and product analysis that goes into the plans can't help but make the company a stronger competitor. He reasons that if the plans are sound "and we meet our objectives, we'll be addressing the competitive issues as well." □



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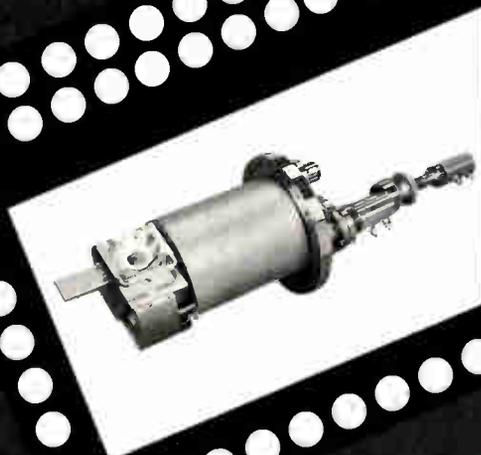
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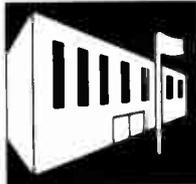
COMPANIES TO WATCH

THE QUIET MONEY MAKER SPINS OFF STARTUPS ITS OWN WAY

Burr-Brown's inside ventures get into the black in a hurry

TUCSON, ARIZ.

Burr-Brown Corp. always did march to a different drummer. In part that's because the components maker has been doing business since 1956 far out of the geographic mainstream, down the road from Phoenix and nearly 1,000 miles away from Silicon Valley, and partly because the firm's products aim at uncrowded niches. One result of the path blazing is near-anonymity: despite an enviable record, Burr-Brown is one of the least-known chip-based firms.



has gone about its work quietly, with no complaints about Japanese trade barriers or nationalistic buying practices. It has done nothing unusual—it divines customer needs early, works closely with them, and delivers quality products on time—but it has done them well. A major reason, says president and chief executive officer James J. Burns, is that "it's always a Japanese national [from Burr-Brown] sitting across from those Japanese customers."

Not content to rest on those laurels, Burr-Brown is turning to another approach to spur growth from new businesses. Using so-called intrapreneurship, it involves helping employees with new ideas to spin off companies that will exploit them. The point is to keep those em-

ployees from leaving to do their own thing. If they stay, the parent company can share the fruits of their ingenuity.

The technique has been tried elsewhere with varying degrees of success; characteristically, Burr-Brown is doing it with a twist. It launched successful spin-offs—in personal-computer expansion boards, specialty power supplies, and modems and multiplexers—between 1983 and 1986. Now a fourth, in communication networks, is being prepared for launching.

One difference from other companies' inside spin-offs, which usually take a while to show profits, is that all three of Burr-Brown's went into the black about 18 months after startup. Although their total sales volume is still only about \$11 million, the signs are pointing to a rapid climb, says Burns.

The main problem with intrapreneurial

The company has parlayed its specialty in linear-conversion devices and the data-acquisition equipment that uses them into sparkling annualized growth rates. For much of the decade they've exceeded 20%. Burr-Brown even sailed relatively unscathed through the downdraft that drove most chip firms deeply into the red in 1984-85. And now with its basic stand established, it is adding a new arrow to its quiver. As is typical with the firm, it is taking a basic tactic—spin-offs—and giving it a twist.

Not that the company appears to need anything new. Net income in 1988 was \$11.5 million on nearly \$177 million in revenue, both records. "They've built a good, solid company," says Raj Rajaratnam, financial analyst at New York's Needham & Co. He says, and other analysts who track the firm agree, that "Burr-Brown usually does things its own way."

Rajaratnam is most impressed with Burr-Brown's success in international markets. He points to Japan, where it has more than a third of its sales. "It's done the best job there of any U. S. chip company," he says. Pacing the company's Japanese action is a digital-to-analog chip for compact-disk players, accounting on its own for some \$25 million or 75% of its market. In the wings, awaiting the predicted takeoff of digital audio tape, is an analog-to-digital unit, the PCM78, that could be as successful as its CD mate.

Moreover, the company's customer roster of the largest Japanese consumer-electronics houses makes it even more unusual among U. S. chip-based firms. Since it started selling in Japan in 1975, it



Checking the latest product of Intelligent Instrumentation Inc., a Burr-Brown venture, are Jim Burns, left, president of Burr-Brown, and Gene Tobey, president of the new venture.

spin-offs, say management experts familiar with the technique, is getting the right mix of independence and attention from the parent. Spinning the venture off too far from the support of the mother ship can sink it without a trace. On the other hand, holding on too tightly risks smothering it "in the bear hug of corporate bureaucracy," says Gene E. Tobey, who started Burr-Brown's unsuccessful attempt at growth through internal development, a department to start new businesses. It closed in 1982. He now heads the successful PC-board spin-off.

From the start, the major organizing point was "to give them freedom to act," Burns says, recognizing from the outset that without granting latitude "to make their own mistakes," nothing lasting could be accomplished. However, to avoid letting any mistakes become terminal, such corporate services as finance, marketing, and technology are there for the asking. But these were to be used only when executives of the spin-offs needed them, and not specified as part of the deal. Most other startups begin with many such controls, but Burns thinks that only a flexible agreement will work. His other maxim is a long-range timetable. "Don't be in a hurry," he says; forcing growth before building a solid base courts trouble.

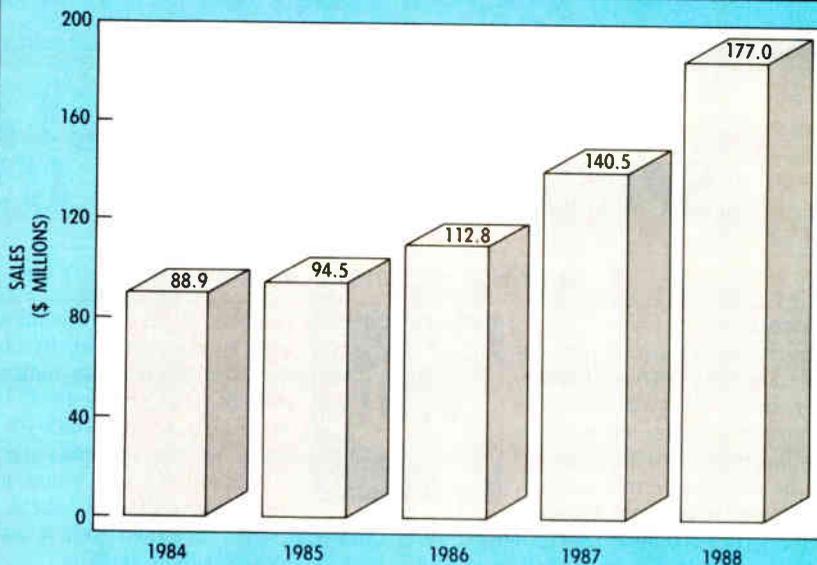
The stab at internal growth failed because "they were never on their own, and the bureaucracy imposed itself," Burns says. Tobey confirms that heavy corporate participation in decision making and some other things shackled the launching of products into risky new segments, where the highest potential lay. "We never really found what clicked, except for pushing what we already had," he recalls.

So when Burns offered the chance to try his hand again in 1983, Tobey jumped at it. The new venture, aimed at what was then a nascent market in PC expansion boards for data acquisition, is Intelligence Instrumentation Inc. Its PCI20000 line offers a broad choice of PC instruments.

MONEY RAN OUT. Though the company is now in the pink, Tobey admits to making the typical error of many startups—spending the initial stake too quickly, overestimating sales, and thus running out of capital early on. "It was some of the pain of a real startup, but good old Burr-Brown wouldn't let us sink," he says. When he called, the corporate cavalry arrived in the form of help in arranging a bank credit line and installing good financial controls. Tobey found too that Burr-Brown's worldwide marketing organization is a big advantage with customers. Burr-Brown holds 79% of each unit, with the remaining ownership in the hands of employees, as additional incentives.

The second venture was Analog Micro-

BURR-BROWN CLIMBS QUIETLY



SOURCE: COMPANY REPORTS

systems Inc., making specialty power supplies. The third, Dataforth Corp., manufactures modems and multiplexers for short-haul industrial communications of less than 6,000 ft. The presidents of the units, Larry McDonald and Lee Payne, respectively, were previously Burr-Brown engineering managers. The fourth unit now being planned is in communication networks.

Burns says the ventures are about where he expects them to be. He sees

their big growth coming during 1990, after an anticipated business slowdown this year.

Starting the spin-offs has become a glamour job to Burr-Brown executives, and even to the official supervising them, W. Grafton Burger, vice president for corporate development. Burns confesses that he has an ulterior motive in whipping up this interest in spin-offs. "They're a good way to train general managers," he says.

-Larry Waller

XYLOGICS DIVERSIFIES, BUT WITH DISCIPLINE

BURLINGTON, MASS.

It's been an up-and-down ride over the last dozen years for Xylogics Inc. The company has probably got the largest share of the market it's in—computer peripheral controller boards—but the going has been tough. It grew fast in infancy, but sagged badly after losing sight of its primary business. Now under more disciplined management, Xylogics is coming on strong again.

At the moment the firm is diversifying, but this time with a sober step into communications controllers. It is not about to take a quantum leap like the one it took into computer systems six years ago—a step that almost deep-sixed the company.

Founded in 1977 to provide controllers—primarily for Digital Equipment Corp. disk and tape drives—Xylogics quickly became the market-share leader. The company's revenue had grown to \$10 million by 1982 and it was profitable in its first four years. Then came changes.

Xylogics branched into DEC-compatible subsystems and systems, selling to both original-equipment manufacturers and end users. "We built a product but didn't have the marketing and field-service resources to support it," says Chappell "Chap" Cory III, senior vice president for marketing operations and corporate development. "It was a good product technically, but nobody had done a business plan." By 1983, Xylogics had lost its leadership in DEC peripheral controllers and its market identity, and it was losing money on declining revenues. The net loss for that year was \$2.9 million on revenue of \$8.6 million.

That crisis led to a series of events that saved Xylogics from "hemorrhaging badly," says Bruce Bergman, chief executive officer and chairman. Then-president Wayne Griffiths resigned and was replaced by interim CEO Tom Gnuse of Prime Capital Management, Stamford, Conn., a Xylogics investor. He laid off

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At the same time, the transition management team of treasurer and senior vice president for finance Vincent Salvi, Gnuse, and Cory shed the system and subsystem business to refocus the company on OEM board-level controllers. This time the focus had a Multibus flavor, because research indicated a substantial market opportunity in that segment.

Finally, Bergman was recruited from his post as general manager of IBM-compatible controller and subsystem operations at Control Data Corp. of Minneapolis, and became president and CEO in July of 1983. He says he joined Xylogics armed with a well-defined business plan that included adding peripheral controllers for Multibus-based systems.

GOOD FIT. "I was an ideal fit for Xylogics," Bergman says. "IBM Corp. was shipping the 3380 disk drive; we were facing a revenue dip because CDC didn't have a 3380." In search of alternate business, Bergman developed plans covering various products, including peripheral controllers for Multibus-based systems. But CDC didn't implement any of those plans, so Bergman "hit the ground running at Xylogics with a plan on day one," he says.

Coincidentally, Xylogics had cracked the Multibus realm earlier in 1983 when its 440 Multibus controller was picked by Sun Microsystems Inc., Mountain View, Calif., for use in a work station.

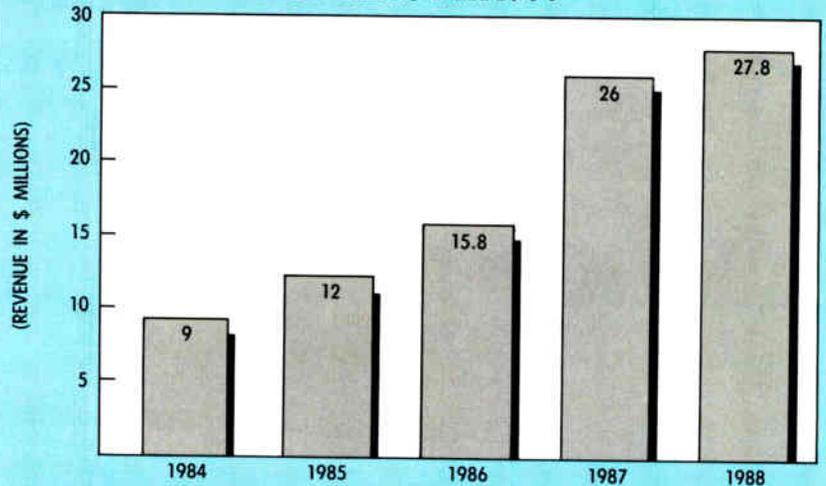
Bergman and Salvi soon secured \$2.25 million in new equity from investors. The company began investing in new products and technology that have helped expand product breadth and improve performance. Those include additional Multibus products, controllers that are compatible with Control Data's Storage Module Drive interface, plus an important effort to design application-specific chips to boost controller performance.

The new team and market focus led to a turnaround in October 1984. Although the company lost money that year, it returned to profitability that month. By its initial public offering in March of 1987, Xylogics attracted \$10.7 million.

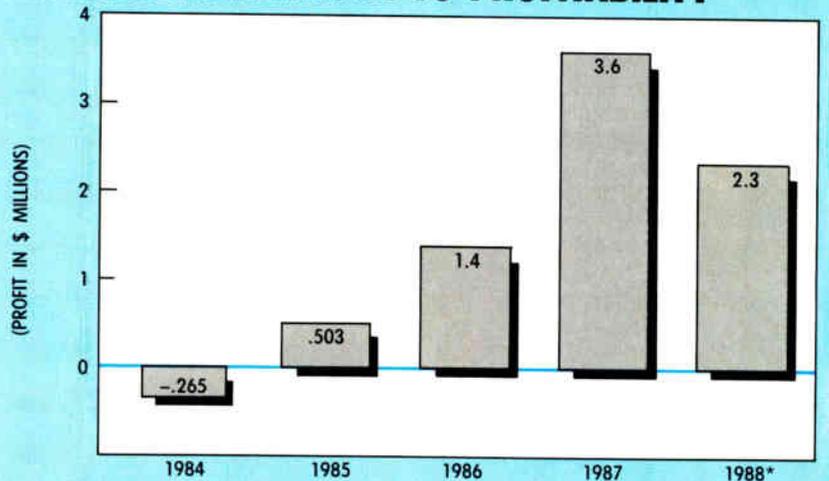
Peter Savage, the president and chief operating officer who was named in late January, is an extension of the new management. He had been vice president for engineering. Bergman credits Savage with developing Xylogics' architecture for the SV series of controllers for high-performance disk drives. It uses the IPI-2 Intelligent Peripheral Interface standard introduced last fall [*Electronics*, November 1988, p. 23].

John Berylson, recently a partner with Cowen & Co., an investment banking firm in Boston, says Bergman and Salvi complement each other nicely. Cowen helped underwrite Xylogics' initial public offering. "Bruce is good at strategic plan-

XYLOGICS' TALE OF RECOVERY...



... INCLUDES A RETURN TO PROFITABILITY



*NOTE: DIP REFLECTS R&D INVESTMENT OF \$4.7 MILLION, OR 17%

SOURCE: ELECTRONICS

In 1983, the new CEO hit the ground running with a Multibus plan

ning; Vin is good at projecting the numbers and assessing the risks" of those plans, Berylson says.

But detailed planning of the company's most important new direction—communications controllers—falls mostly to Cory, who has been with Xylogics almost since its inception. He says the company is wary about going off in too many directions in light of its near-fatal experience.

The product line now includes a broad range of Multibus offerings, high-performance SMD controllers, Enhanced Small-Disk-Interface controllers, and newer 32-bit controllers for VMEbus systems, as well as communications controllers. The latter thrust began with the 780, which Xylogics claims is the first communications controller using a 32-bit data path.

It supports 16 full-duplex asynchronous ports at 9,600 bits/s.

Analyst Berylson sees little risk in the communications-controller business for Xylogics: "This should be an almost riskless product extension, not a new business. The risk will be in making it profitable." Perhaps the biggest challenge facing Xylogics, says Berylson, is growing as fast as it must. "It needs a bigger critical mass, and there will be a lot of pressure on it to grow fast—by acquisition or otherwise," he says. Xylogics acquired a terminal-server product line last December from Encore Computer Corp. of Marlboro, Mass.—its first acquisition.

Bergman's goals for the company include having it recognized as a leader in both peripheral and communications controllers and having revenue of \$100 million "in the early 1990s." That kind of growth and recognition can come through "aggressive research and development investment, and by acquisition of product lines, technologies, or entire companies," he says. —Lawrence Curran

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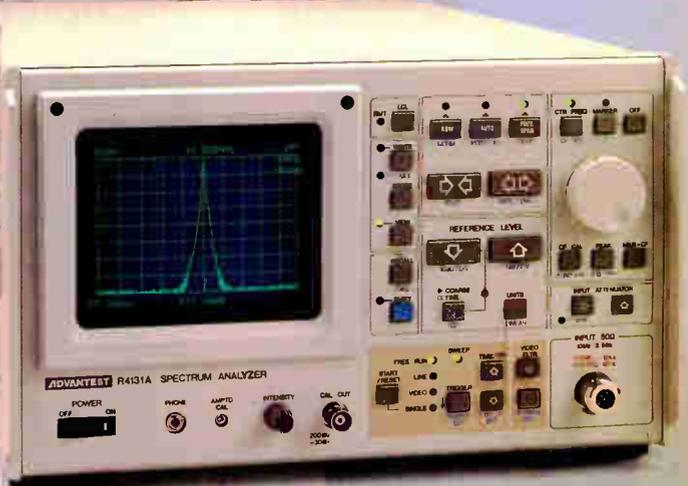
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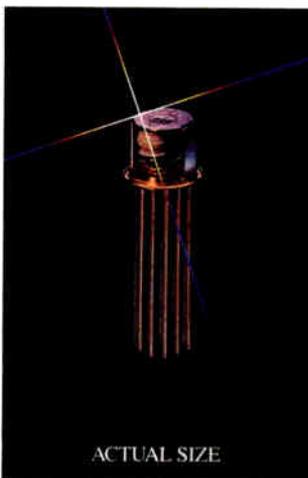
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PEOPLE TO WATCH

HOW MIKE BENNETT PLANS TO GUIDE INTERLAN'S SKYROCKETING GROWTH

He wants to leverage the company's in-house talent to expand into software

BOXBOROUGH, MASS.

When Michael Bennett joined Interlan Inc. early last year as vice president for operations, he felt as if he were hitching a ride on a rocket. That's understandable: the company's fortunes were zooming. Revenue had grown at more than 40% annually for several years.

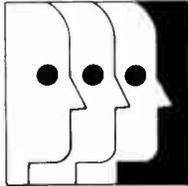
The rocket is still climbing, but now Bennett, the new president and chief executive officer, is steering and he's intent on breaking through the \$50 million barrier and soaring on to \$100 million in annual revenue.

Bennett, 37, was recruited by his predecessor and friend, Michael Barker. It had been Barker's intention for some time to leave the company after turning the business around. That done, he brought Bennett aboard in January 1988. The plan from the start was for Bennett to take over at Interlan, a supplier of local-area-network products that integrate computer systems shared by departmental work groups.

Barker's task was the result of a slowdown that afflicted Interlan a few years after the company was founded, in 1981. At first Interlan had taken off fast, but within four years growth had slowed seriously enough for the company to start casting about for a corporate parent. It found one in Micom Systems Inc., a Simi Valley, Calif., provider of local-area- and wide-area-network products. Micom acquired Interlan early in 1985.

PRIVATE AGAIN. But Bennett says the marriage was never a happy one, largely because it stifled the entrepreneurial spirit that had pervaded the original, independent Interlan. Part of his current aim is to nourish that spirit, which was revived when Interlan was bought last September by Odyssey Partners, a New York-based investment firm that returned it to its privately held status.

Before coming to Interlan, Bennett, a fourth-generation Texan with traces of his native accent still peppering his speech, was a general manager at Tandy Corp. in Fort Worth, Texas. In addition, he has 12 years of general- and manufacturing-management experience at Digital Equipment Corp., acquired in various



DEC facilities in New England, Phoenix, Scotland, and West Germany.

For some of those years Barker and Bennett worked together at DEC. They discovered their skills and temperaments were different but complementary. "Mike is a fantastic guy," Bennett says. "But he's a one-man show, and his view at Interlan was short-term. He's a turnaround guy and he had a short-term contract. His focus here was on what deal we can do this week with what original-equipment manufacturer. That's what the company needed."

Now that Interlan is back on its feet, the company needs someone who, in contrast to Barker, takes a long-term view. That's Bennett's forte. "My style is to



Bennett: 'My style is to create a company people feel they can grow with.'

create a company people feel they can grow with," he says. "I want to pay attention to the company environment and make it a good place to work. I'm not a one-man show."

He says his approach encourages people to rise into the ranks of management, "because they can regard Interlan as their company, not Mike Barker's company. I want to make Interlan more than a quick stop in a career progression."

LINING UP. To assist in that aim, Bennett recently organized Interlan's widely varied products—there are 500 to 600 of them—into three lines: hardware-platform, network-management, and software products, each of which is headed by a product-line director. The three directors have gross-margin goals to meet, plus responsibility for deploying engineering resources to meet product time-tables and developing the following year's financial plan.

On the financial front, Interlan had \$32 million in revenue when it went private in fiscal 1988. The company will complete its fiscal year 1989 on March 31 at about \$55 million, well above the revenue goal of \$44 million. Bennett expects growth rates of between 30% and 35% in the next two or three years, which would easily bring the company through the \$100 million plateau in 1992.

During that period, Bennett would like to see Interlan's image evolve. Currently, it's best known as a provider of low-end networking-hardware boards. He thinks it can build on that. "We have some exceptional talent on the software side of the house," he says, "and we're beginning to develop a more specific approach to leveraging software sales."

Toward that end, Interlan recently introduced a software product that provides a link between Novell Inc.'s NetWare LAN and a personal-computer-based file server running OS/2 LAN Manager software from Microsoft Corp. It's called Interlan LAN Server and it enables transparent interoperability between a NetWare client and the LAN Manager server.

"This is software only," Bennett says, "and we'll absolutely continue to develop this kind of product."—Lawrence Curran

DR. BOGOCH PRESCRIBES A COMPUTE-SERVER SOLUTION

NEW YORK

A compute server for Macintoshes. What a novel idea.

But, then, Sam Bogoch is a novel guy. For one thing, he located his company, Human Devices Inc., not in Silicon Valley or on Boston's Route 128, but in New York's Greenwich Village. For another, he's a nonpracticing physician, a graduate of Harvard University and Columbia University Medical School. More to the point, he has launched his first product, Chorus ComputeServer, with a creative vision for delivering parallel-processing technology to microcomputer users.

According to Bogoch's vision, the platform would be built from the ground up to be a compute server. It would run at up to 32 million floating-point operations/s using a parallel architecture based on Inmos Corp.'s Transputers. It would aim at Apple Computer Inc.'s Macintosh because the Mac's interface encourages "people to do things they wouldn't try to do on a work station with a complicated interface." And he believes that applications developers will support the system because it is easy to use.

Bogoch sees business and technical microcomputing systems consisting of a user's front end and a compute-server back end. While the front-end/back-end terminology is not new, Bogoch has applied a more rigorous definition to the idea. "Without a coherent user interface, we don't consider a machine to be a front end," he says. That leaves out IBM Corp.'s Personal System/2, Sun Microsystems Inc.'s machines, and the other computers that people assume have the business and technical market tied up. "Apple is the only premier front end on the market right now," he says.

NOT YET. As he sees it, Sun and AT&T Co. really haven't established Open Look, a consistent user interface for Unix environments. IBM will eventually have Presentation Manager widely distributed and resident on many desktops—but it's not there yet. Steve Jobs has got Next-Step, and the Open Software Foundation will have its Motif software running sooner or later. "All those front-end environments would complement our back end," says Bogoch, "but in fact the only one with an installed base is the Mac."

The applications in Bogoch's microcomputing world view are, by necessity, compute-intensive programs that handle such applications as fully interactive finite-element modeling, photorealistic graphics, and financial modeling based on Monte Carlo simulations, which are used by stock analysts. "Because the Mac's inter-



Bogoch wants to bring parallel processing to the Macintosh masses.

face is so easy to use, programmers aspire to create applications with much more functionality than they would on a machine with a complicated interface."

With that kind of orientation, it is not surprising that the Apple Venture Capital Group in Cupertino, Calif., wants to learn more about Chorus and Bogoch. A unit of Apple Computer, the venture-capital group "picks third-party companies whose success would be good for Apple and gives them enough money so they don't have to worry about real venture capitalists," says Bogoch. Interest is strong enough to prompt a first meeting, and Bogoch is hoping for more.

In the meantime, the corporate strategy at Human Devices is to spin off the off-the-shelf Chorus hardware from the parent company. Human Devices was founded as a hardware consulting company specializing in one-of-a-kind portable devices and neural networks. One such design was a real-time controller for a wafer-fabrication plant. The consulting business has doubled in sales every year. "My interest has focused fairly sharply on Chorus," says Bogoch, "and our vice president, Tom Schultz, will take on most of the responsibility for Human Devices."

'Without a coherent user interface, we don't consider a machine to be a front end'

With such a technological heritage, it stands to reason that Chorus deserves a break-the-mold marketing scheme, and Bogoch has complied. Unlike the typical marketing strategy for a new hardware platform, he says, "We don't pay applications developers to port their programs to the hardware. We have them do it on speculation because they think the platform is promising." So far, about 20 have signed up and the Chorus ComputeServer will begin shipping this month.

"We're providing a back-end applications platform, not raw technology where the end user has to find a way to use it," says Bogoch. While the underlying technology is exotic, it is virtually transparent to both users and programmers.

LINDA APPEAL. For applications developers, the programming environment Linda is a prime attraction in the Chorus ComputeServer. Linda makes the task of porting an application program over to a parallel architecture almost as easy as calling a subroutine.

Developed at Yale University and marketed by Scientific Computing Associates, New Haven, Conn., Linda works best if the conventional program in C was written with parallel processing in mind, says Bogoch. "It's going to put a real dent in Occam and other screwball programming languages" that developers once had to deal with to effect parallel processing on Transputer-based hardware, he says. Similarly, neither user nor applications developer need worry much about the networking aspects of Chorus. Besides C, Linda supports Pascal and Fortran development environments.

"Linda does all the message-passing and data arbitration," he says. "We support Appletalk now and we'll have an Ethernet option, but it will all be transparent to the programmer." Eventually, he says, "Chorus will talk to any network that's available."

The company has shipped test systems to Macintosh software developers, universities, and major corporations. Commercial applications being adapted for parallel processing using Chorus include the 3DWorks and RenderWorks animation packages from MacroMind; Crystal Ball, a forecasting and simulation package from Market Engineering; Dimensions RayTracer, a 3-d modeling and ray-tracing program from Visual Information; Inertia, a structural computer-aided-design package from MCAE; and HyperBrain, a neural-network program from Neuronics.

In fact, it was neural nets that got Bogoch the Dr. before his name. After Harvard, he attended medical school at Columbia with neural nets in mind—and to avoid writing a dissertation. "But what I learned most about was people," he says. Maybe that's what accounts for his novel outlook.

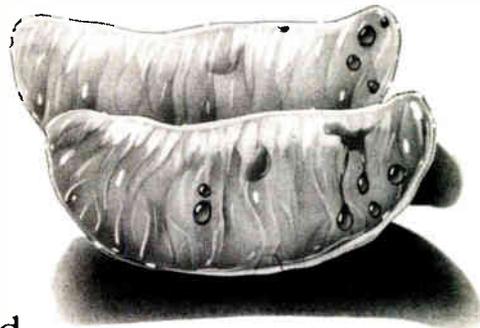
—Jack Shandle

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fish and types of sausages smoked by traditional methods should be eaten in moderation.

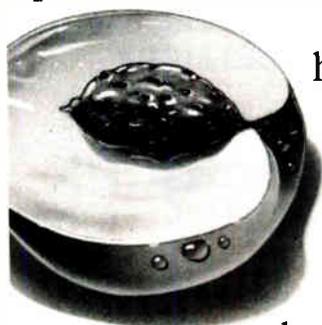
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TV OR NOT TV? THAT'S BRANNON'S QUESTION

PRINCETON, N. J.

No less than other electronics industry executives, Intel Corp.'s Bob Brannon ponders the future. What sets his vision apart is that it includes more than just the traditional next generations of hardware—the personal computers, compact-disk read-only memories, and video random-access memories. For Brannon, a big part of the picture includes that ubiquitous American species, the couch potato.

Brannon sees the future as being largely shaped by a marriage of the personal computer and the TV set—a vision that's at the front of the industry's collective mind as it grapples with high-definition TV (see p. 70). Brannon's interest comes as no surprise; after all, he's the general manager of Intel's Digital Video Interactive operation in Princeton.

But Brannon takes the scenario one step further by pondering the fundamental nature of that match as it first reaches the market: will it be a TV in a PC, or a PC in a TV? To Brannon's mind, the answer has implications for international trade balances and technology leadership.

"Both the market push and the technology push will make it easier to put a TV into a personal computer," he says. That's pushing in the right direction for Intel, which holds a dominant position in PC chips, and for the U. S. in general, which is still the wellspring of PC software, hardware, and architectures.

If the goal is to market a TV with a PC inside, the product is stuck with a price point of \$500 to \$1,000—a tall price/performance order for "full, deep interactivity," says Brannon. But the personal-computer market is "much less price sensitive," with machines selling for \$1,000 to \$5,000 and beyond.

For those who object that TV's strongest appeal is the passivity it offers—witness the proud-to-be-a-couch-potato syndrome—Brannon presents what he calls the Future/Interactive. "PC people are not couch potatoes," he says. What's more, "the 18-year-olds of today were the first generation to grow up with the Atari-games box, and the current 10-year-olds are growing up with a much more advanced version of that. As time goes on, the demand for interactive toys and tools will grow."

A GOOD FIT. The theory fits nicely into Intel's Digital Video Interactive game plan as outlined by David House, general manager of the Microcomputer Components Group, last October: training applications followed by the educational market and finally, the consumer market over the next five years [*Electronics*, November 1988, p. 32]. Using a proprietary chip set, a secret compression algorithm, and a CD-ROM drive, the technology offers full-motion video along with extensive editing capabilities.

Interactive TV will have no small effect on the prospects for the future of the U. S. consumer-electronics industry. Should the market defy Brannon's logic and follow the PC-in-a-TV scenario, Japan would have the edge because of its production-technique and technology leads. Besides TV technology, Japan also has the upper hand in video RAMs, which will be the memories of choice for either approach. Only Micron Technology Inc. in Boise, Idaho, manufactures video RAMs in the U. S., Brannon points out.

As the scenarios unfold, Brannon is having as much fun as any industry observer watching the behind-the-scenes race for dominance in PCs. "How to build

the next generation of PCs and what they're going to be built out of is what will separate the leaders," he says. "There's a tremendous set of decisions to be made. All the present PC leaders have a race on their hands."

Decisions include the extent to which mixed media and full, deep interactivity will be built into succeeding generations. Other open questions involve the human interface, graphics, and voice recognition. Apple, Commodore, Compaq, and IBM are among those struggling with these questions in the U. S., he says, as are Fujitsu, NEC, and Sanyo in Japan and Amstrad, Olivetti, and Bull HN (formerly Honeywell-Bull) in Europe.

"I believe they will all invest in DVI," says Brannon, "but that doesn't mean they won't invest in other alternatives." So Intel is not standing still—or limiting its options. Research continues on all fronts, including the compression/decompression algorithms. Algorithm development at other laboratories, including the Media Lab at the Massachusetts Institute of Technology, can be used in DVI hardware, for example, because the algorithms are stored in microcode.

It's been less than a year since Intel tapped Brannon's shoulder for the DVI job. He had been general manager for European Systems Operations before coming to Princeton. Previous positions at Intel and Hewlett-Packard Co. gave him a background in boards, software—he negotiated Intel's Xenix agreement with Microsoft Corp.—development systems, and components.

"They wanted someone who had done a startup," he says, "somebody who could parachute in, hire people, negotiate—and go through the pain." —Jack Shandle

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READER'S REPORT

A crack in the crystal ball

To the editor: I look forward each year to the annual *Electronics* World Market Forecast edition. It always provides a valuable service by presenting a diverse set of statistics, covering all facets of our industry in a consistent and easily digestible format.

But in this year's version, I was extremely disappointed to see a quotation where comments I had made relating to past performance in one sector of the market in 1988 were erroneously attributed to some future prospects for an entirely different sector of the market in 1989 [*Electronics*, January 1989, p. 98].

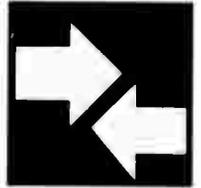
During preparation for this edition, I was asked why the very high-speed bipolar fuse-programmable sector of the programmable-logic-device market had slowed in the latter half of 1988. I attributed this to a softening in demand from the personal-computer makers.

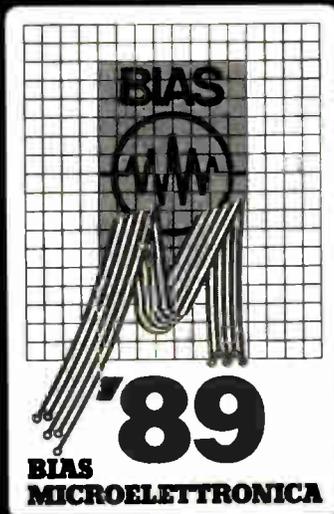
My expectations, then, and now, were for continued strong growth for CMOS-based reprogrammable logic in 1989 and beyond. This is entirely consistent with the forecast I made in the fall. Recent forecasts by independent market-research organizations, such as Dataquest in San Jose, Calif., and Integrated Circuit Engineering and InStat, both of Scottsdale, Ariz., support a growth-rate forecast of 100% or more in the same period for which you forecast only a 9% increase.

CMOS-based PLDs serve an extremely broad range of customers, with balanced representation across computer, industrial, military, and telecommunication sectors of the domestic and international markets. Therefore, they are far less likely to be affected by the fortunes of the PC business than bipolar devices, which depended heavily on this sector for their growth in 1988.

Propelled by declining prices, enhanced performance, and low cost, easy-to-use PC-based computer-aided-engineering tools—particularly CMOS erasable PLDs—are rapidly replacing the standard CMOS and TTL families for most general-purpose logic applications. This fact is an important contributor to the declining sales you predict for CMOS (5%), low-power Schottky (6%), and standard TTL (-25%) logic later in the same article. In fact, the Technology Research Group Inc. of Boston claims that CMOS PLDs will replace 80% to 90% of today's small- and medium-scale integration by the time the mid-1990s arrive.

David A. Laws
Altera Corp.
Santa Clara, Calif.





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TRACKING JAPAN'S ELECTRONICS INDUSTRY

THE STRUCTURE OF THE JAPANESE ELECTRONICS INDUSTRY

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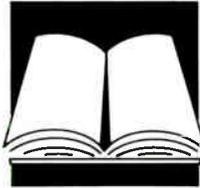
The increasing value of the yen and the lack of growth in the formerly dominant consumer electronics sectors is forcing changes in the Japanese electronics industry. Japanese manufacturers are pushing their low-value-added products offshore and concentrating on making high-value-added products at home. Imported products ranging from low-end consumer gear from newly emerging countries to minicomputers and work stations from the U. S. have become more competitive in Japan.

Meanwhile, other Japanese industries—those that are in worse straits because they don't benefit from the constant stream of new products that keeps the electronics industry vibrant—are pushing their way into the business. Steel manufacturers are now in the semiconductor business, and chemical and detergent firms are making optical and magnetic disks.

This book, by the Dodwell & Co. market-research group, attempts to track and analyze such changes through late 1988. It also presents a statistical snapshot of the industry at that time, along with tables charting its growth from 1983 or 1984 to 1987.

The book starts off with an overview of the industry and a description of the effect during the past few years of the appreciation of the yen. Short sections survey the communications sector, including new domestic and overseas common carriers and value-added networks; foreign companies' activities in Japan; Japanese steel manufacturers entering the electronics industry; capital investment; and research-and-development investment. Then comes a 40-page analysis of Japanese products with production value exceeding 100 billion yen; products with very high growth rates; and new products expected to become significant.

A large part of the book consists of profiles of Japan's nine electronics firms worth a trillion yen; the 36 worth 100 billion yen; and 330 smaller firms, in decreasing amount of detail. For the largest companies there is a great amount of data, including news of recent activities, lists of subsidiaries, affiliates, foreign associates, and research labs with products involved. (IBM Japan Ltd. just made it over the trillion-yen line in fiscal 1987, but it's relegated to the second tier in this



book and so gets shorter shrift than the nine Japanese giants.) Tables compare the nine behemoths with each other and with 13 foreign companies.

In one sense, of course, much of the information in this book was out of date before it was published. But it does capture the state of the industry at a certain point, as its title promises. And it should be a useful starting place for anyone who needs to know about Japanese electronics, because it indicates what kind of information is readily available and the sources for it. Some parts, such as the convenient English list of industry associations, should change very slowly.

Although the book is published by an English trading firm, the language appears to have been written in a Japanese-dialect version of American English. Key words seem to be used in their dictionary form rather than according to the mean-

A strong yen and sagging consumer business are forcing some changes

ing dictated by the structure of the sentence in which they are used. Even more disturbing are mechanical translations, like the one that turned "central processing unit" into "main equipment unit." Most of the text flows smoothly, though, and a reasonably intelligent reader should not be inconvenienced.

Also somewhat disturbing is the unquestioning acceptance of product categories used by the Ministry of International Trade and Industry and the Electronics Association of Japan. As a result, all those products that are not strictly consumer goods or components are considered to be industrial.

The index gives single-page rather than multiple-page references. Firms are listed under their English names; the Japanese name is included in parentheses if it's significantly different. Cross-referencing is provided for some but not all names—anyone who knows only the Japanese name of a company could get lost looking for it. There's no subject index, so a reader who wants to find particular topics has to look through the table of contents.

—Charles L. Cohen

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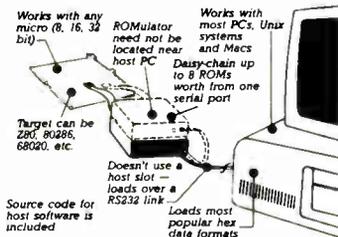
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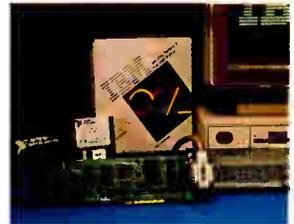
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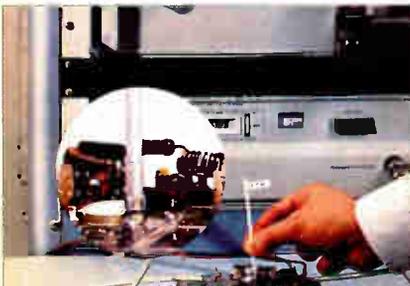
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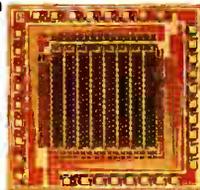
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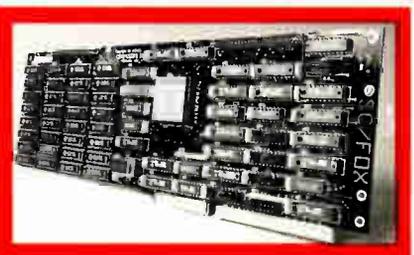
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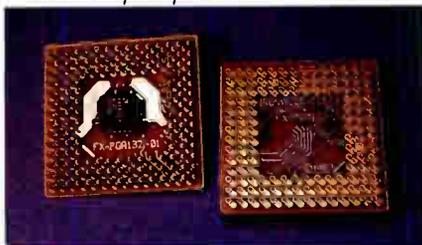
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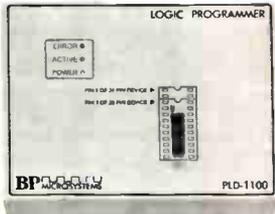
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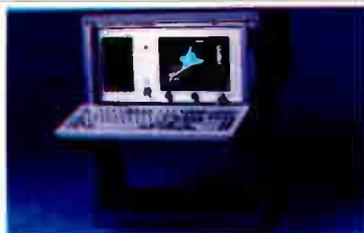


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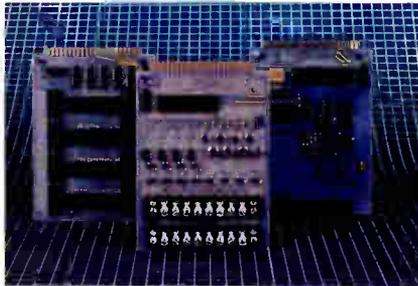


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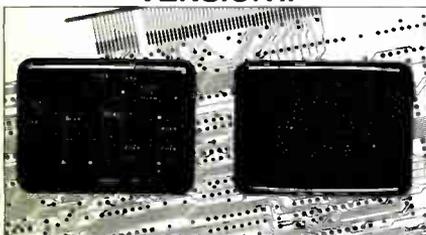
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UPDATE: THE SERIES 10000 POWERS APOLLO'S RECOVERY

A lot of murky water has gone under the bridge at Apollo Computer Inc. lately. In the year since the company introduced its Series 10000 "desktop supercomputer" [*Electronics*, March 3, 1988, p. 69], the company that pioneered the technical work station lost its president, weathered consecutive profitless quarters, and probably slipped in market share. The fourth-quarter results form the only bright spot in this otherwise bleak landscape. They show Apollo's reduced-instruction-set supercomputer coming on strong in a surge that brings a sense that the company is on its feet and making its way back from 1988's setbacks.

Volume shipments of the Series 10000 were a big contributor to the fourth-quarter turnaround. Revenue for the quarter was a record-breaking \$184 million, up from \$162.9 million for the same quarter in 1987. Net income for the period was \$3.1 million. Although that is far below the \$10 million reported in the same quarter last year, it nevertheless is a return to profitability.

Even before Apollo added a robust three-dimensional graphics subsystem to the Series 10000 last month, the Chelmsford, Mass., company had shipped an estimated 250 units of the RISC machine to customers. That figure comes from Vicki Brown, senior analyst for work stations at International Data Corp., the Framingham, Mass., market-research firm. "That's good when you consider they started shipping last October," Brown says.

Brown also points out that the system has given Apollo a formidable tool in its competition with Sun Microsystems Inc., the Mountain View, Calif., market-share leader in work stations. She says the Series 10000 "is getting good margins and is performing well, especially against the Sun 4/260." She also says Apollo hopes this product will be crucial in its recovery. "I think it will be. It has a multiprocessor capability, which Sun doesn't have," she says.

Nevertheless, Apollo lost momentum last year when revenue and profits slipped because sales of existing systems were slowing. "Momentum, once lost, is difficult to get back," says Brown. She adds that when 1988 numbers are tallied, they'll probably show Apollo out of second-place standing and in a tie for third with Hewlett-Packard Co. in work-station market share. That puts it behind Digital Equipment Corp. and Sun.

From the beginning it was the company's intention to

stagger the introduction of the Series 10000. First Apollo put out the server, then followed up with the 3-D graphics subsystem in a version called the Series 10000VS, for visualization system. Although the RISC-based drawing engine's debut was planned for last fall, it didn't show up until this year because of delays on the part of a supplier.

Thirteen CMOS arrays of 22,000 gates each make up the VS drawing engine, says Paul Bemis, Apollo's marketing manager for high-end systems. The five gate arrays in the engine, made for Apollo by Integrated CMOS Systems Inc., Sunnyvale, Calif., use a 1.5- μ m dual-metal CMOS process. They operate at 36 MHz and have an emitter-coupled-logic output section to accommodate the display of high-bandwidth raster data. The Series 10000 can have as many as four central-processing units. Each CPU can perform 1.5 million graphic transforms/s because each is directly linked to the drawing engine over the machine's 64-bit-wide, 150-Mbyte/s X-bus.

This tight coupling enables simultaneous and intensive number crunching along with graphics rendering. That makes the VS especially suitable for interactive visualization in applications such as computational fluid dynamics, molecular modeling, and electronic design.

"The graphics subsystem is designed to render images as fast as the CPUs can generate the required data," Bemis points out. That contrasts with the slower, more conventional approach of using long rigid-geometry pipelines. In the Apollo system, each 64-bit CPU has two floating-point processors and an integer processor working in parallel

for fast throughput. The CPU-linked RISC drawing engine handles pixel-drawing tasks that are common to all graphics applications. Importantly, Bemis says, the display enhances the processing and rendering power. It's a high-resolution, 1,280-by-1,024-pixel, 70-Hz, noninterlaced, flicker-free monitor. The VS comes with either 40 or 80 planes of frame-buffer memory. The 40-plane version sells for \$94,900—that's \$25,000 more than the basic server. An 80-plane system is priced at \$104,900. Additional processors cost about \$20,000 each.

Bemis maintains that by introducing the server-only version first, "we learned that there was a tremendous pent-up demand for a graphics resource like the VS on a network, but not at each seat. The VS is an engineering work-group resource, with perhaps one VS-equipped system for 15 seats."

With another processor, that works out to \$10,000 to \$15,000 per seat. That's about the same as an earlier VAX from DEC, he says, though the VS performs considerably better than its predecessors.

—Lawrence Curran

SPECIAL REPORT

TECHNOLOGY TO WATCH



SURPRISE! APOLLO UNVEILS A 'DESKTOP' SUPERCOMPUTER

Journal has been talking a great deal about the imminent arrival of a new class of supercomputer. It's not the supercomputer as a desk, or the supercomputer as a rack-mounted system, or the supercomputer as a mainframe. It's the supercomputer as a desktop. Apollo Computer Inc. has just unveiled its new Series 10000 "desktop supercomputer" in a surprise unveiling at the headquarters of a major user.

The new Series 10000 from the Chelmsford, Mass. company is built around a reduced-instruction-set architecture that the company calls Prime. For parallel re-architected-instruction supercomputing. Among other things, the Prime design makes the 10000 the first RISC system to hit an execution rate of more than one instruction per cycle, according to Terry Condon, marketing manager for high-performance systems, who says the 10000 executes 1.2 to 1.3 instructions per cycle. The RISC system currently available from computer vendors to Sun Microsystems, MIPS Computer Systems, and Sun Microsystems, stores for one cycle per instruction but do not meet the Apollo system.

The 10000 has also packed some other firsts. It's the first work station with a user RISC system architecture including memory processing and floating-point unit, and system buses. It's the first work station to use a new cache technology which provides a built-in system for tearing down VLSI arrays. Finally Condon claims his new machine meets a benchmark in an LSI logic benchmark performance: \$10,000 per megabyte, compared with about \$100,000 per megabyte for conventional supercomputers.

The 10000 is also one of the new first single-chip supercomputers, the other is Apollo Computer Corp.'s Prime. The Prime design apparently will use the new cache technology to deliver production models in May. Apollo expects to ship two versions of the 10000. One is a server system without a display, which will sell for just over \$70,000. The other is a desktop workstation offering 1.5-MHz 68000-processor-based graphics, priced just under \$90,000. However, the 10000's three-dimensional graphics subsystem will not be available until the first month of design work on the subsystem started after the CPU design, so the workstation will ship a 2-D graphics subsystem.

The work station also, though, represents a major rebranding by Apollo to its new RISC architecture. Apollo reports that the Prime architecture will soon

be used in three future generations of its hardware over the next five to 10 years, with performance increasing every two years or so as successive generations of microprocessor technology are incorporated into it. In the 10000, Prime is implemented in CMOS gate arrays, with custom semiconductor logic as floating-point processors. The system also delivers the impressive LSI logic performance of 1.2 instructions per CPU, or it executes in single precision.

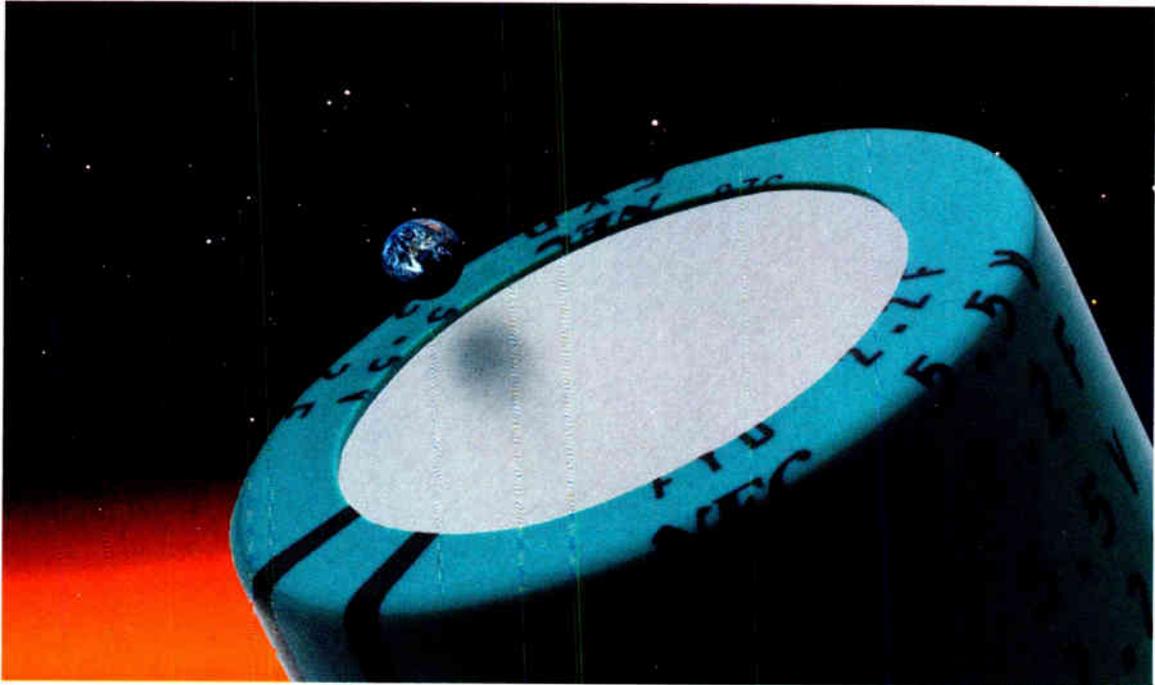
Prime is based on what Apollo calls "redundant-structure" RISC. As in other RISC systems, Prime implements the instruction set in hardware, with hard-wired instructions and delayed branching. Where Prime differs is in delivering single-cycle execution. Typically all instructions are executed in one machine cycle. One important reason Prime can execute an instruction



The Apollo Series 10000 supercomputer workstation offers a RISC architecture called Prime. Its hardware array and cache are

The RISC system also gives the company a weapon in its battle with Sun

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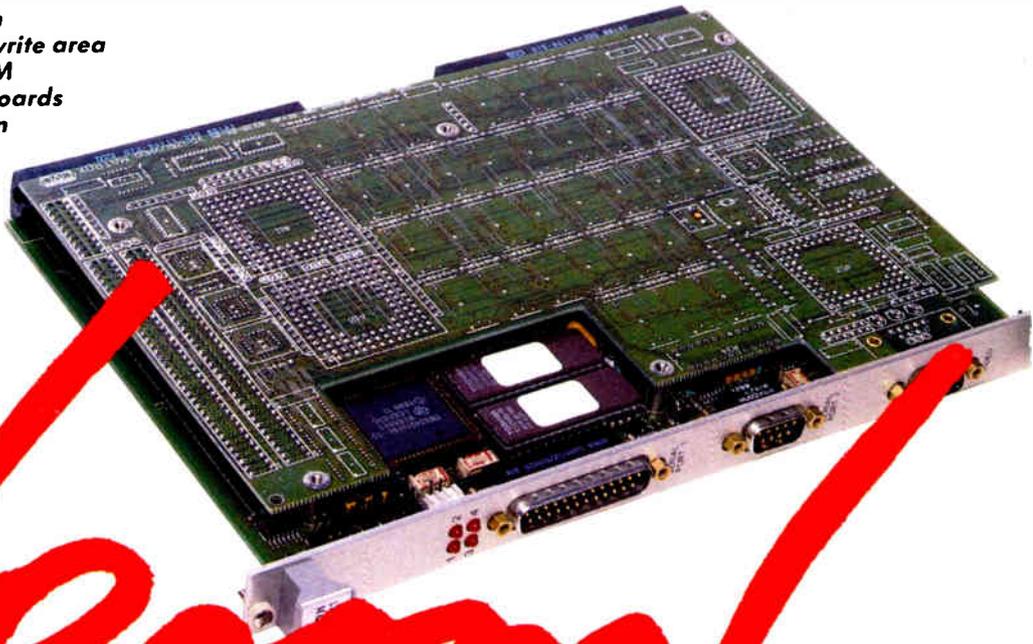
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