CIRCUITS FOR ELECTRONICS ENGINEERS

Edited by Samuel Weber
Executive Editor,
Electronics

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M. L. WILLIAMS

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table of contents

Preface

Since 1964, the Designer's Casebook section of *Electronics* magazine has been consistently one of the best read sections of the magazine. The reasons for this are not hard to find. First, engineers are always looking for ways to relieve the drudgery that is part of design. If they can save time and effort by incorporating or adapting ideas from others, they will do so with alacrity. Second, the standards of *Electronics* have always been high. Published Casebook ideas are selected for innovation, usefulness, and accuracy.

This volume is a compilation of 346 useful circuits that have appeared in Designer's Casebook over the last four years. They were designed by engineering readers of *Electronics* from all over the world and represent approaches to achieving oft-required electronic functions in a variety of ways. There are 51 such functions arranged alphabetically, and the circuits have been conveniently grouped within them for fast access.

This is not intended as a hobbyist book. While some are relatively simple, most of the circuits in this volume have been designed by engineers for the achievement of engineering objectives. They are presented on the same principle that has made Designer's Casebook so popular for so many years: namely, that re-inventing the wheel is wasteful of engineering time.

To the hundreds of inventive engineers who have contributed their innovative ideas to Designer's Casebook, and to the thousands of loyal *Electronics* readers who have responded enthusiastically to them, this book is gratefully dedicated.

1. Amplifiers

Single preamplifier/isolator drives lf and vlf receivers

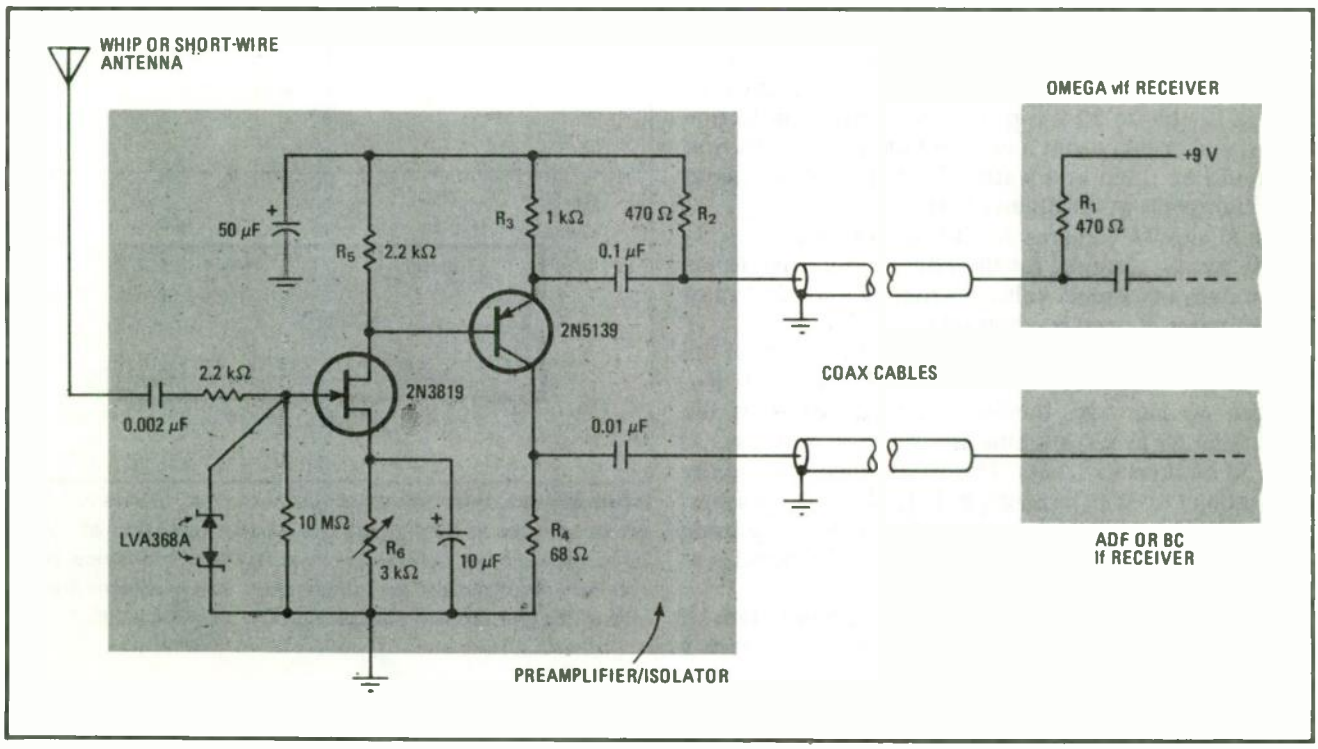
by R.W. Burhans
Ohio University, Athens, Ohio

Some rf front-end circuitry proposed for Omega receivers [*Electronics*, Sept. 5, 1974, p. 98] has now been used in several flight tests of simplified vlf navigation for general aviation. The results showed that the first-stage MOSFET occasionally burned out in the presence of very close lightning discharges, and that a common antenna, such as the automatic direction finder sense whip, should be used for both the Omega navigation receiver and the ADF receiver.

Corrections for both problems are made in the circuit of Fig. 1. The MOSFET has been replaced by a low-cost junction FET that provides a gain of 2 or 3 and adequate low-noise performance over the frequency range from 5 to 1,500 kHz. An expensive wideband line-isolating transformer used in the original preamplifier has been eliminated by using a simple resistor divider string (R_1, R_2) to carry power to the preamplifier and signal output to the Omega receiver over a single cable. A small resistor in the collector lead of the 2N5139 output emitter-follower provides a unity-gain buffer output for driving an ADF or broadcast-band receiver from the preamplifier at a low impedance level through a separate cable. Isolation between the vlf receiver (10–100 kHz and the ADF/broadcast-band receiver (200–1,500 kHz) is completely satisfactory.

The 2N3819 JFET is much less likely than a MOSFET to burn out with static charges, and the back-to-back zener diodes give gross protection from high-level short-duration burst interference. The atmospheric 5–1,500-kHz noise level is usually a limiting factor in high-output-impedance preamplifiers of this sort, so an ultra-low-noise MOSFET is not required.

Adjustment of source-bias resistor R_6 centers the operating point for equal positive and negative peak clipping on large signals. The circuit can handle input signal levels up to 0.1 volt rms before round-off distortion of the output waveform begins. For unity gain at the lf terminal, the ratio of R_4/R_3 is approximately B × A, where B is the current gain of the 2N5139 stage and A is



Dual-purpose front end. Preamplifier/isolator circuit, fed by a single antenna, drives a vlf navigation receiver and an lf broadcast-band or automatic-direction-finder receiver. The two receivers are connected to the preamp by separate coaxial cables that can be as long as 100 feet. Circuit is designed for small general-aviation aircraft, so size, weight, and cost are minimized and ruggedness is emphasized.

the gain of the 2N3819 stage. A gain of 2 or 3 at the vlf output is desirable to drive the additional filters and limiting amplifiers in the Omega receiver.

This isolating preamplifier can also be used in ground-station monitors with a single wire antenna driving two receivers, such as a WWVB 60-kHz time reference plus 100-kHz Loran C, or an Omega plus Loran C, and so forth. One of the receivers must supply power to the preamplifier, as shown in the figure. The upper frequency is limited to 1,500 kHz by the low-cost JFETs; somewhat higher-frequency performance might be achieved with JFETs such as the 2N4416. □

Unity-gain stage is 50-ohm driver

by William A. Palm
Control Data Corp., Minneapolis, Minn.

A recurring problem for the circuit designer is the connection of his op amp, his oscillator, or his test instrument to the low-impedance outside world. The simple buffer-driver shown here provides unity-gain class A operation, high input impedance, and 50-ohm output impedance over a wide frequency range. It also provides blast-out (short-circuit) protection and can be built with a single IC.

Because the base-to-emitter voltages of transistors Q_1 and Q_2 cancel each other, the dc voltage between input and output is near zero. With 2N2222 and 2N2907 transistors, actual offset voltage will run from 0 to 50 millivolts. This offset can be balanced out by adjustment of resistor R_5.

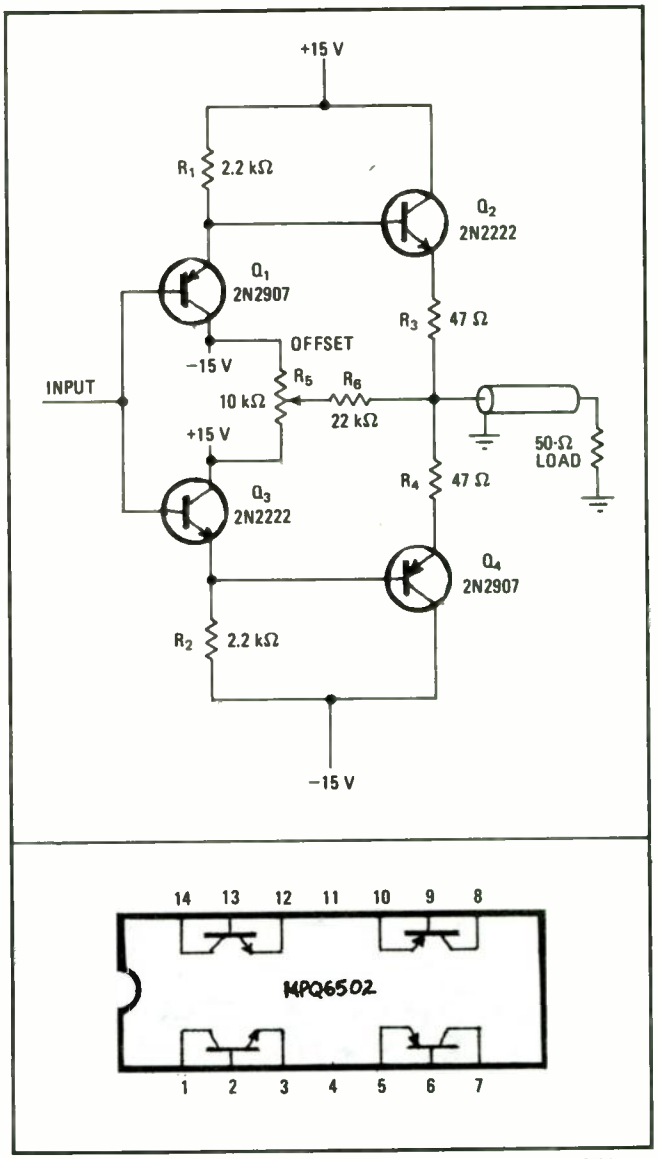
With ±15-V supplies and the resistor values shown, this driver will deliver 10 V peak to peak, undistorted, into a 50-ohm load. Without the external load, the output will double to 20 V p-p. For total circuit protection against a shorted output and dc inputs, resistors R_3 and R_4 should be rated at 4 watts. The circuit draws about 17 milliamperes in the quiescent state.

Actual supply voltages are not critical. Resistors R_1 and R_2 can be changed for the appropriate drive to accommodate any supply voltages from ±5 V to ±20 V. For ±5-V supplies, R_1 and R_2 should be 680 ohms.

The input impedance of the circuit is a function of the gains of the transistors used. For transistors with h_{FE} between 50 and 100, the input impedance is in the range from 50 to 100 kilohms at 1 kHz and decreases to 25 to 50 kilohms at 1 MHz. This impedance is normally high enough to offer imperceptible loading on op amps. Even a 2-kilohm potentiometer, used as an amplitude adjuster, sees only a 4% loading from low frequencies to 1 MHz.

For the circuit shown, the driver has a bandwidth of about 10 MHz when the source has an impedance of 1 kilohm. With a source impedance of 50 ohms, the frequency response is greater than 10 MHz.

A convenient means of packaging this circuit is the MPQ6502 complementary quad shown in the inset. The MPQ6502 has two 2N2222 (npn) and two 2N2907 (pnp) transistors in the handy 14-pin dual-in-line package. □



Driver delivers. Unity-gain driver has zero offset, delivers 20 V p-p into an open circuit, or 10 V p-p into a 50-ohm load. Useful as output for op amps and test instruments, it has high input impedance, good frequency response, and low current drain. Supply voltages are not critical. The four transistors are packaged in an MPQ6502 IC.

Eliminating offset error in sense amplifiers

by Dan Chin
Cambridge Memories, Newton, Mass.

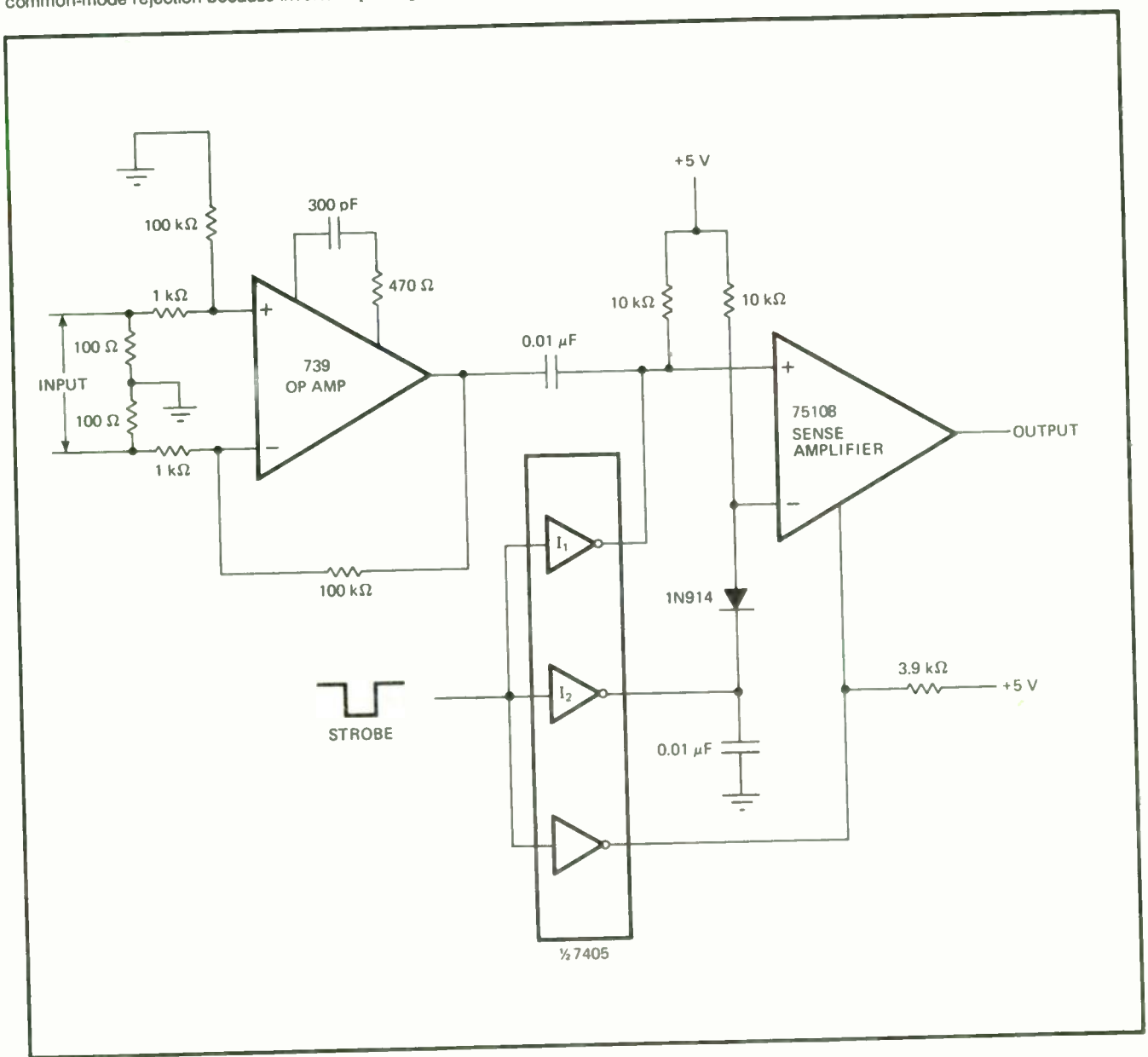
A sense amplifier for a memory must detect a pulse signal during a gated time interval. But a significant error occurs at the amplifier's output when its input offset voltage is large in comparison with the voltage amplitude of the pulse signal.

If the offset voltage is removed by ac coupling, however, the pulse's baseline could shift when the readout data pattern changes. But if, in addition to being ac-coupled, the pulse is held to ground except during the time interval of interest, a reference voltage can be developed and the pulse compared to it.

The dc-restored sense amplifier in the figure makes use of this technique. The input operational amplifier performs as a basic linear amplifier, providing a signal gain of 100. The amplifier's output is ac-coupled to the sense amplifier for detection.

Dc restoration is accomplished by the open-collector inverters connected to the inputs of the sense amplifier. Two of the inverters, I_1 and I_2, assure that any offset voltage is applied equally to both inputs of the detector, permitting offset error to be eliminated by the detector's common-mode rejection. The diode in series with the detector's negative input sets the threshold level halfway between the pulse baseline and the minimum expected peak voltage. □

Sensing pulses, barring offset errors. Data is ac-coupled from the operational amplifier to the sense amplifier to get rid of offset-voltage error. The dc signal level is then restored by open-collector inverter gates. Any additional offset error is eliminated by the sense amplifier's common-mode rejection because inverters I_1 and I_2, at each of the sense amplifier's inputs, introduce equal offsets.



Dc restorer for video use offers ultra-stability

by Roland J. Turner
AEL Communications Corp., Lansdale, Pa.

A sample-and-hold technique, along with strong degenerative feedback, permits an active dc restorer to operate with very high stability over a wide temperature range. Restoration stability can be maintained to within 30 microvolts, even in the presence of a dc offset voltage as large as 100 millivolts.

The circuit is useful in radar applications, where it is often essential to peak-detect or integrate video signals relative to a stable dc reference. This is especially true if the video sensor contains diodes that have a temperature-dependent offset voltage.

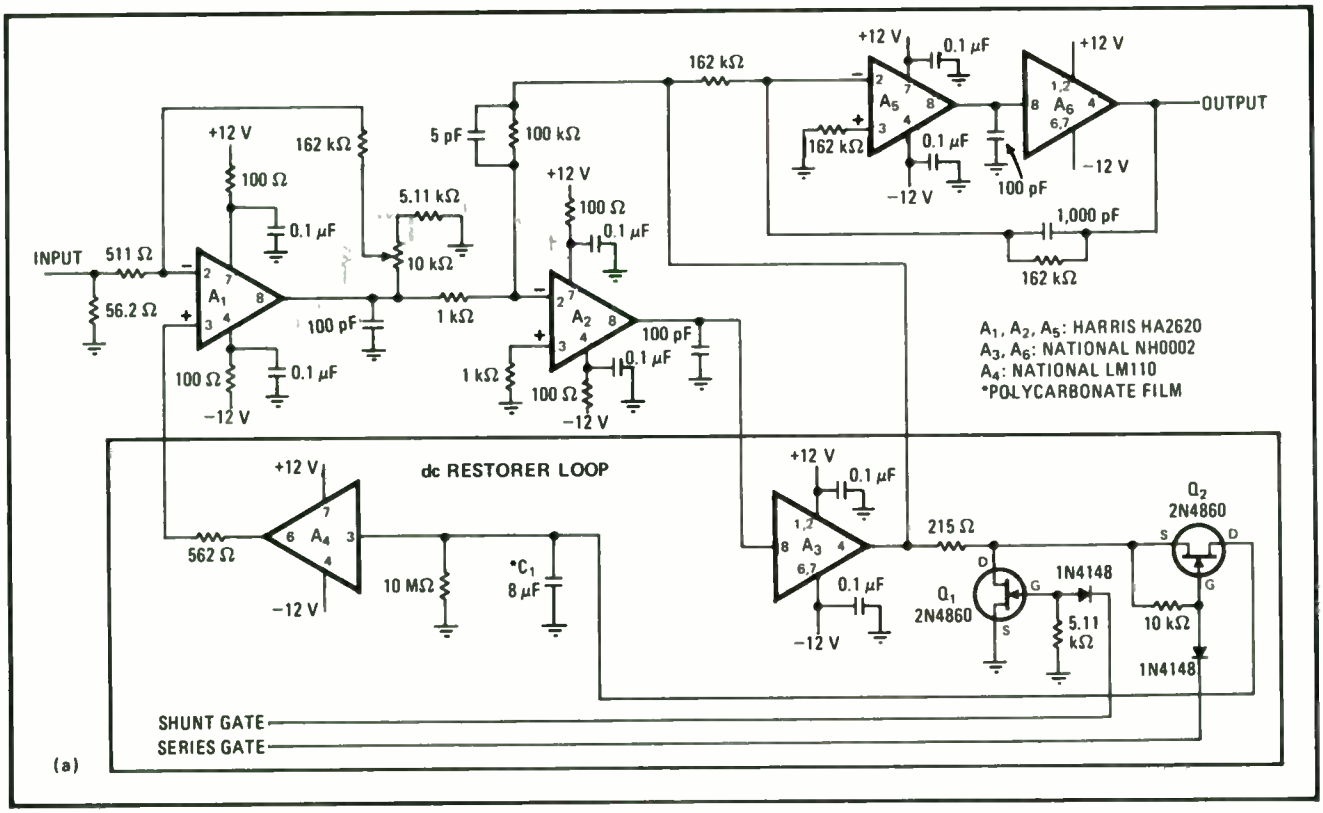
The dc restoration must be performed without any temperature-induced offset voltage, since dc coupling must be preserved in the video processing (peak detection or integration) following dc restoration. Accurate signal detection, then, heavily depends on providing a stabilized dc restoration level. The video output signals must be independent of any thermal variations that may occur in the video detector and dc restorer.

Conventionally, a dc restorer operates at relatively high signal levels and requires considerable video gain prior to dc restoration. Moreover, a dc restorer generally employs a temperature-compensated zener diode, and two matched diodes to keep the dc restored level relatively constant over a wide temperature range. But even with the best matched diodes and the most stable temperature-compensated zener, the dc restored level cannot be made more stable than ±10 mV over a 100°C temperature range. With the dc restorer shown here, however, stabilities of 30 μV can be established at extremely low video levels.

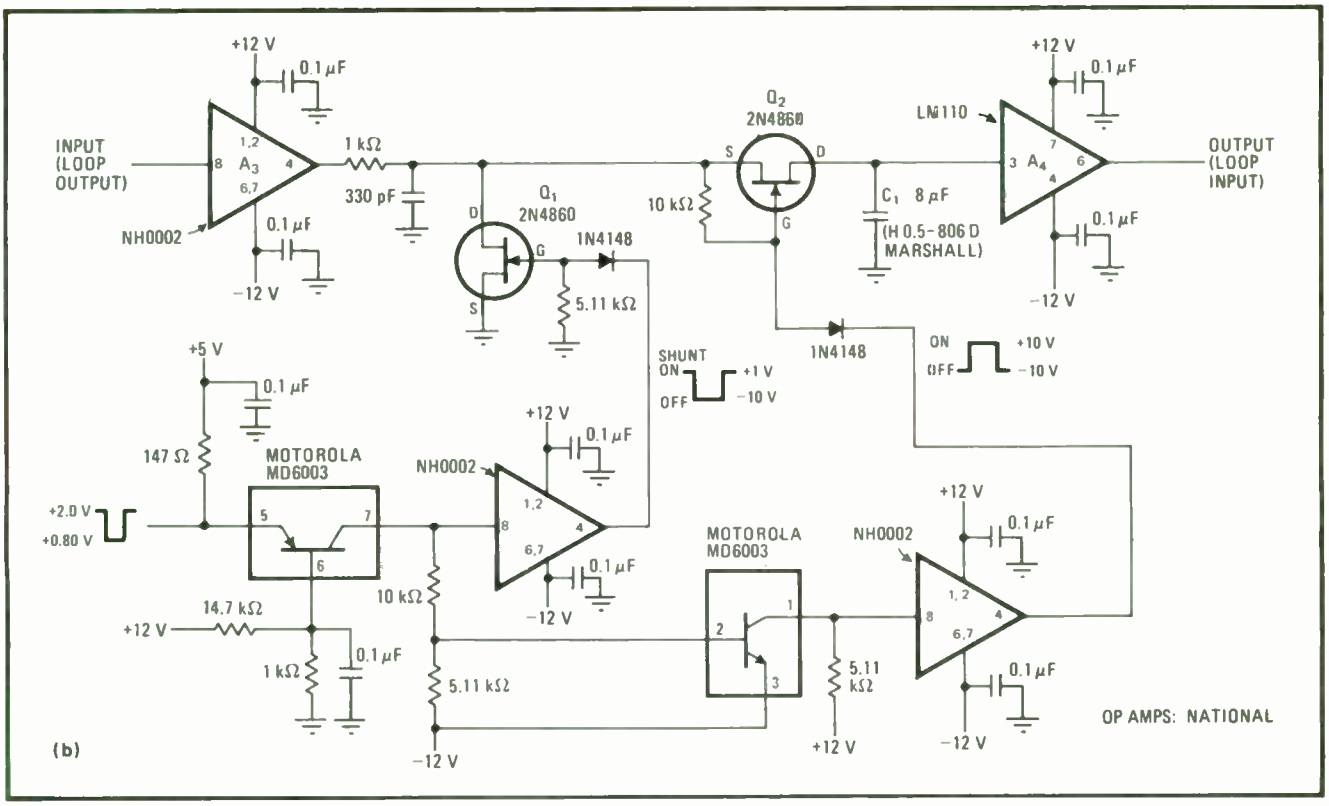
A complete video amplifier employing this improved dc restoration technique is drawn in (a). In this circuit's sample-and-hold scheme, the dc output of a dc-coupled amplifier is sampled over a 50-microsecond gating interval. It should be noted that dc coupling must be maintained from the input (sensor) through to the output integrator or peak detector. As a result, dc signal changes longer than the sensor's thermal time constant, which is typically less than 10 milliseconds, can be recognized as a valid signal/target by the peak detector or integrator.

The full schematic of the dc-restorer section of the video amplifier is given in (b). During the dc-restoration interval, the FET shunt gate, Q_1, is open, while the FET series gate, Q_2, is closed. During the gating interval, sampling capacitor C_1, which is a highly temperature-stable polycarbonate-film capacitor, charges to the average noise level present at the output of amplifier A.

When the sampling gate is closed, the circuit's sampling process activates a degenerative-feedback loop that forces the average signal value at A_3's output to approach the signal-noise level. In effect, the dc level at the noninverting terminal of input amplifier A_1 is forced to match the dc level at A_1's inverting terminal to



Emphasizing stability. Dc restoration loop of video amplifier (a) allows the amplifier to match dc input levels to within 30 microvolts, in spite of widely varying temperatures. The sample-and-hold circuitry of the dc restorer loop is shown in (b). During the gating interval, which is 50 microseconds long, FET shunt gate Q_1 is off, FET series gate Q_2 is on, and capacitor C_1 (a temperature-stable unit) charges.



within 30 μV. During the signal processing interval, when shunt FET gate Q_1 is on and series FET gate Q_2 is off, the voltage across capacitor C_1 establishes an ultrastable dc-restored level at the positive input to amplifier A_1 as a reference for detecting whatever video signals may be present at the negative input of A_1.

To realize a high degree of dc-restoration stability within the gating aperture, it is essential to select op amps for amplifiers A_1 and A_2 that have fast slew rates. This is why Harris' type HA2620 op amp, which has a gain-bandwidth product of greater than 30 megahertz, is used for both A_1 and A_2. Amplifier A_4 is a high-stability buffer that serves as a high-input-impedance load for the sampling capacitor, C_1.

This active dc restorer can reduce a 100-mV dc offset at the sensor to an equivalent dc offset of less than 30 μV. And because of the low leakage of the sampling gate, the stored charge on capacitor C_1 is not disturbed during the hold interval, even if a 10-V signal is present at the gate input.

The forward gains (80 decibels) of amplifiers A_1, A_2, and A_3 contribute to the degenerative-feedback loop during the dc restoration interval, forcing A_1's positive input to follow the dc offset present at A_1's negative (sensor) input. The circuit's integrating stage containing amplifiers A_5 and A_6 must be placed outside the dc-restoration loop, since the fast slew rate of the forward-control loop must be preserved during the dc restoration interval.

For the circuit to operate properly, the input-signal condition must be known during the dc-restoration interval. In radar systems, this time occurs between pulse transmission and signal reception; for television signals, this time occurs during the sync tip transmission. □

CATV transistors function as low-distortion vhf preamplifiers

by Paolo Antoniazzi
Società Generale Semiconduttori, Milan, Italy

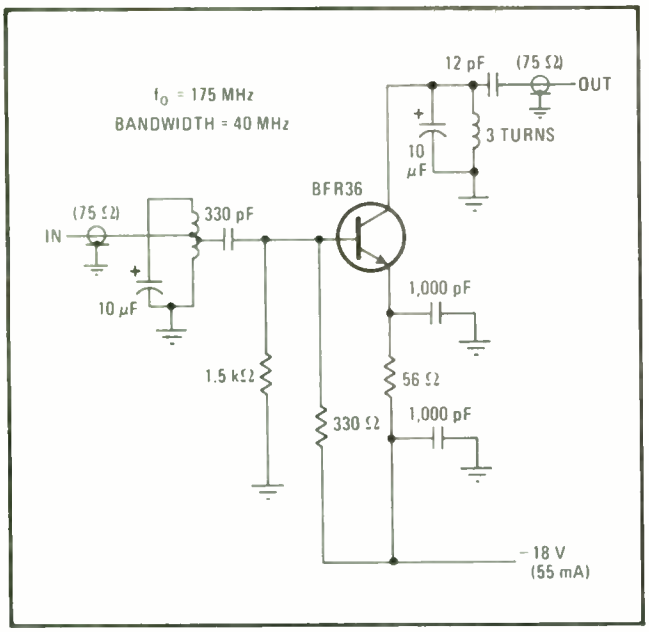
A standard cable-TV transistor makes an excellent vhf preamplifier, minimizing signal distortion over a wide dynamic range. Generally, FETs or MOSFETs are used rather than bipolar transistors because of the cross-modulation distortion created by the nonlinear behavior of the bipolar's base-emitter junction. CATV transistors, however, operate at currents of 20 to 80 milliamperes, so that their intrinsic emitter resistance is kept small and the effects of input-junction nonlinearities are eliminated.

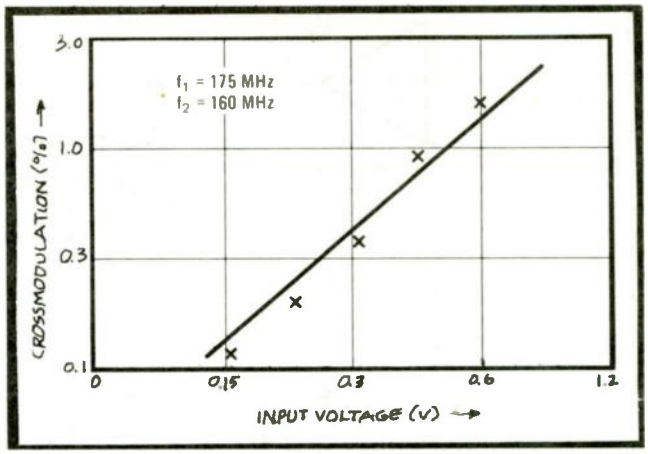
The single-stage antenna preamplifier shown is intended for mobile fm communications applications and is particularly suitable for use with double-balanced Schottky-diode mixers. It obtains 13 decibels of gain at 175 megahertz from a medium-power CATV transistor.

The circuit can handle 0.5-volt inputs with less than 1% cross-modulation, as indicated by the performance plot. Noise figure depends on how large the operating current is. But even for a transistor collector current of

50 mA, the noise figure is typically 5 dB or less.

The transistor used here is designed principally for line-amplifier applications. Its crossover frequency is 1.5 gigahertz, its operating current can range from 20 to 150 mA, and its feedback capacitance is typically 1.7 picofarads at a bias voltage of 15 v. □





Linear performer. Bipolar CATV transistor is heart of vhf antenna preamplifier that can process 0.5-volt inputs with under 1% cross-modulation. The nonlinearities that are normally associated with a bipolar transistor's base-emitter junction and that cause signal distortion are practically eliminated in the CATV transistor because of its high operating current. Circuit gain is 13 dB at 175 MHz.

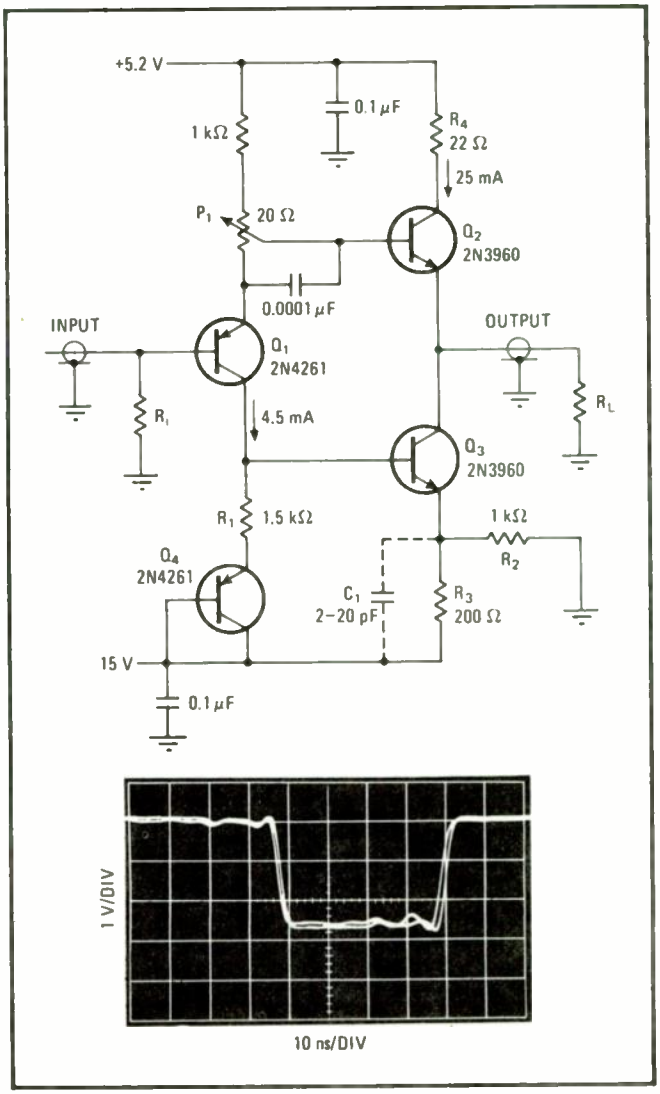
High-speed voltage-follower has only 1-nanosecond delay

by O.A. Horna
COMSAT Laboratories, Clarksburg, Md.

When a voltage-follower is needed for isolation and/or impedance transformation in fast analog circuits, a simple emitter-follower can be made to give better performance than an integrated operational amplifier. A dual complementary emitter-follower overcomes the disadvantages of the conventional emitter-follower—its input-to-output offset voltage and its relatively low voltage gain. Propagation delay for this complementary circuit is less than 1 nanosecond.

The first emitter-follower, pnp transistor Q_1, drives a second emitter-follower, npn transistor Q_2, so that the offset (emitter-base) voltages of these transistors are opposite in polarity. The dc voltage difference between input and output terminals is therefore very small and can be adjusted to almost zero with potentiometer P_1. Transistors Q_1 and Q_2 should make good thermal contact with each other to compensate for the temperature dependence of their emitter-base voltages.

Output transistor Q_2 is loaded by a variable current source, npn transistor Q_3, the base of which is connected to the collector of transistor Q_1. For a given bias current



Fast emitter-follower. Back-to-back emitter-followers, transistors Q_1 and Q_2, are complements, causing their opposite-polarity offset voltages practically to cancel. (Potentiometer P_1 permits fine offset zero adjustment.) Transistor Q_3 is a variable-load current source, while transistor Q_4 is wired as a diode for Q_3's temperature compensating. Scope display shows superimposed input and output signals.

(25 milliamperes here), transistor Q_2 can then deliver nearly twice as much current to the load as would be possible with a constant-current source. The last transistor, Q_4, is connected as a diode to temperature-compensate transistor Q_3's emitter-base voltage.

When the input voltage goes positive, the emitters of transistors Q_1 and Q_2 also become positive. The current through transistor Q_1 decreases, dropping the voltage across resistor R_1 as well as the current through transistor Q_3. The opposite action occurs for a negative input.

The voltage gain of transistors Q_1 and Q_3 can be made greater than unity (between 1.1 and 1.2) by adjusting the resistance ratio of resistor R_2 to resistor R_3. This compensates for the voltage gain of transistors Q_1 and Q_2, which is less than unity (between 0.9 and 0.95). With an unloaded output, the circuit's total stable voltage gain ranges from 0.985 to 0.995, and the output resistance is less than 1 ohm. (The output is protected against short circuits by resistor R_4.)

The scope trace shows the circuit's input and output voltages superimposed on each other. With a load resistor of 50 ohms and an output voltage of ±2.5 volts, the circuit's propagation delay is less than 1 nanosecond, and the rise and fall times are smaller than 2 ns without overshoot. The maximum voltage swing is ±4 V, the bandwidth is approximately 200 megahertz, and the slew rate is over 2 kilovolts per microsecond.

When the load resistance is less than 200 ohms, the circuit's transient response and the bandwidth can be substantially improved by adding a speed-up capacitor, C_1. However, under a no-load condition, when the load resistance is 500 ohms or more, this capacitor can cause the circuit to oscillate.

All four discrete transistors can be replaced by a single quad package, Motorola's MHQ6001, which contains two pairs of pnp and npn transistors. Since these transistors have a gain-bandwidth product of only 400 MHz, as opposed to 1 gigahertz for the discretes, the circuit's propagation delay and rise and fall times will be three to four times longer.

For the bias currents given in the figure, the dc source resistance, R_i, must be less than 2 kilohms. The circuit's input resistance is greater than 50 kilohms for load resistances of 50 ohms or more. □

Getting power and gain out of the 741-type op amp

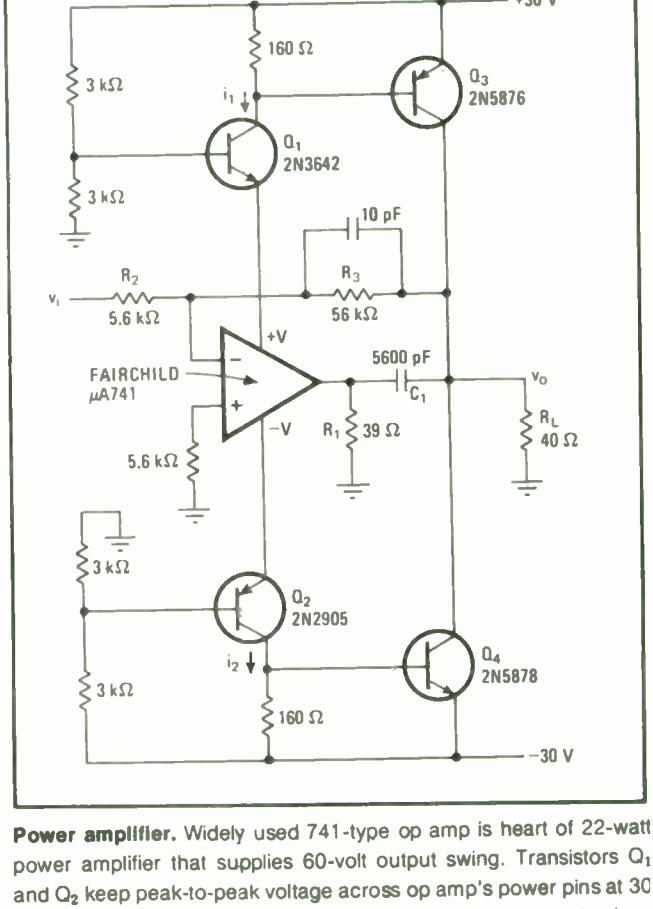
by Pedro P. Garza, Jr.
General Electric Co., Apollo and Ground Systems, Houston, Texas

The popular 741-type operational amplifier can be used as the basis for a high-voltage power amplifier that is capable of delivering 22 watts of peak power at an output voltage swing of 60 volts. Voltage gain for the amplifier is 10, and its frequency response is flat from dc to 30 kilohertz.

Most integrated-circuit op amps are not designed to accept more than 36 V across their power pins. Here, therefore, transistors Q_1 and Q_2 protect the 741-type op amp by maintaining a 30-V differential across the device's power pins. The base of transistor Q_1 is biased at 15 V by the voltage divider network formed by the 3-kilohm resistors, while Q_1's emitter is at 15 V minus its base-emitter voltage drop. The biasing arrangement for transistor Q_2 is similar.

Since a 39-ohm resistance (resistor R_1) is connected to the op amp's push-pull output, substantial currents will be drawn by the device. Currents i_1 and i_2, which appear at the collectors of Q_1 and Q_2, are used to generate the base drive voltage for the power-output stage, made up of transistors Q_3 and Q_4. The power-output stage has a wider frequency response than the 741-type op amp. The negative feedback path through capacitor C_1 provides a frequency roll-off characteristic similar to that of the op amp, thus assuring unconditional stability.

The resistance ratio of resistor R_3 to resistor R_2 determines the amplifier's voltage gain. If the op amp's input-offset voltage is nulled out and resistors having tolerances of ±0.25% are used for R_2 and R_3, the power amplifier's linearity error will be within 0.4% over the output voltage range of +29.8 V to −29.8 V.



Power amplifier. Widely used 741-type op amp is heart of 22-watt power amplifier that supplies 60-volt output swing. Transistors Q_1 and Q_2 keep peak-to-peak voltage across op amp's power pins at 30 V so that device's 38-V rating is not exceeded. Using low-value load resistor (R_1) at op-amp output produces currents (i_1 and i_2) large enough to drive output power stage of transistors Q_3 and Q_4.

Output voltage swings of more than 60 V are possible if transistors with higher collector-base breakdown-voltage ratings are used along with higher power supply voltages. □

High-gain triple Darlington has low saturation voltage

by Eric Burwen
G&S Systems Inc., Burlington, Mass.

A triple Darlington amplifier can be useful in situations that require a minimum of base drive, such as high-efficiency switching regulators or buffer amplifiers with high input impedance. Combining very high current gain and a saturation voltage equal to that of the two-transistor Darlington, this circuit was originally conceived for use in high radiation environments, where the β parameter of a transistor can readily degrade to 5 or even less.

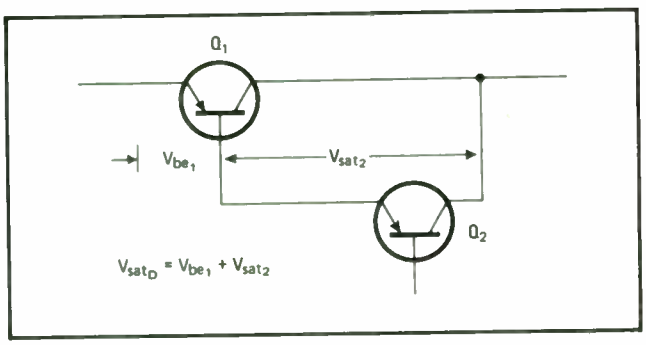
In the conventional Darlington amplifier (Fig. 1), the total saturation voltage is the sum of the base-to-emitter voltage of Q_1 and the saturation voltage of Q_2 alone. Although no transistor or circuit attains the ideal 0-volt saturation voltage, that of the Darlington amplifier is suitably low. But if three transistors of like polarity were cascaded (Fig. 2), the V_{sat} of the resulting amplifier would be nearly double that of the conventional two-transistor circuit.

On the other hand, a triple Darlington made of complementary transistors (Fig. 3) has the same saturation voltage as that of the double Darlington. This is true whenever the saturation voltage of Q_3 taken alone is less than or equal to the combination of:

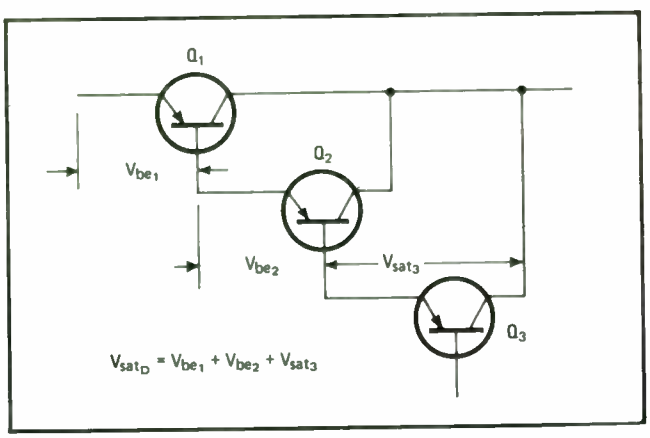
$$V_{be1} + V_{sat2} - V_{be2}$$

Because the current gain of the triple Darlington is large, the currents in Q_1 and Q_2 are large, so that these three voltages do in fact add up to a level larger than V_{sat3} alone. (When Q_3 is in the circuit, of course, its saturation voltage is exactly equal to the combination, by Kirchhoff's law.)

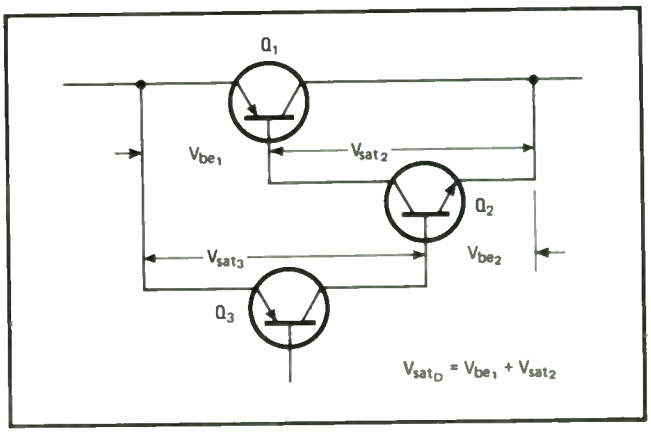
In an experimental version of the triple Darlington (Fig. 4), a current of 8 microamperes controls a load of 2 amperes—a gain of 250,000. The saturation voltage at 2 A is 1.2 volts, the sum of V_{be1} = 0.9 V and V_{sat2} = 0.3 V. Transition times are t_{on} = 200 nanoseconds and t_{off} = 500 ns; storage time is 1 microsecond. □



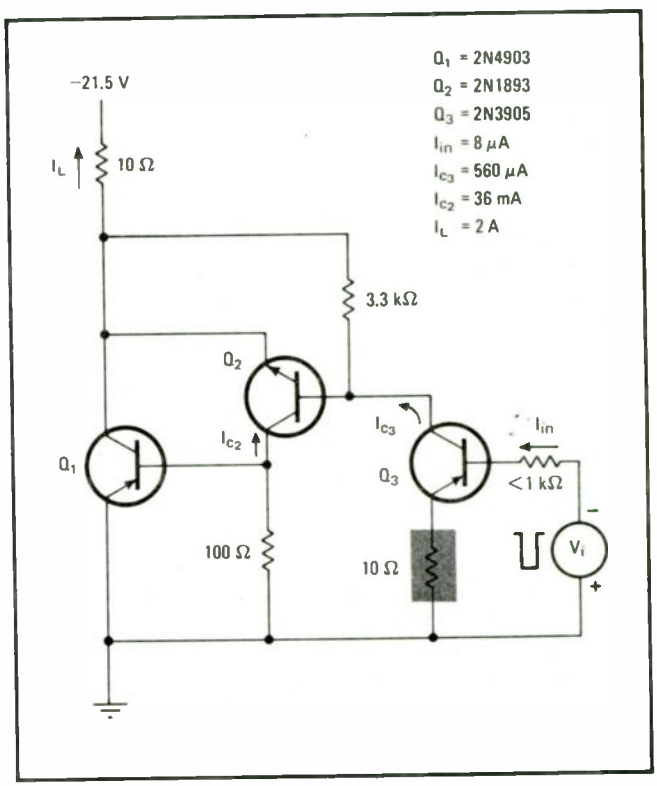
1. Conventional. Two-transistor Darlington amplifier has high current gain, compensating for degraded β, and low saturation voltage.



2. Unsatisfactory. Simply cascading three similar transistors gives a saturation voltage that is much too high.



3. Triple Darlington. Making the circuit out of two pnp and one npn transistors gives high gain without boosting saturation voltage.



4. Switching-time test circuit. Gain is 250,000 in this circuit. The 10-ohm resistor (color) is required to limit the current in Q_3; otherwise, when that transistor saturates, its large current will pass through the base of Q_2 and reduce the β.

Transducer preamplifier conserves quiescent power

by Robert F. Downs
Ocean & Atmospheric Science Inc., Santa Ana, Calif.

A low-voltage micropower preamplifier holds power dissipation to approximately 13 microwatts because of the low bias current of its two-transistor impedance converter output stage. The preamplifier, which is intended for use with a capacitive transducer, operates at a quiescent current of 10 microamperes with a supply voltage of only 1.35 volts.

The gate of field-effect transistor Q_1 is essentially biased at 0 V through resistor R_1. Negative feedback, provided by resistor R_2, maintains Q_1's gate-to-source voltage at approximately -0.4 V, forcing its drain current to less than 4μA. Resistor R_2, therefore, contributes significantly to Q_1's bias stability.

Preamplifier input impedance depends on both R_1 and the voltage gain of the field-effect transistor stage. Actual FET intrinsic input impedance can be ignored since it is orders of magnitude larger than R_1.

If e_i denotes input signal voltage, the voltage across R_1 can be expressed as $e_i(1+K_v)$, where K_v is the stage's voltage gain. Since current through R_1 is increased by a factor of $1 + K_v$, the apparent input impedance is $R_1/(1+K_v)$.

On a small-signal basis, then, the preamplifier's input stage is equivalent to a common-source configuration, while the bias arrangement is that of a source-follower. For the over-all circuit, the dc input impedance is around 1.5 megohms, while the ac input impedance is about 300 kilohms.

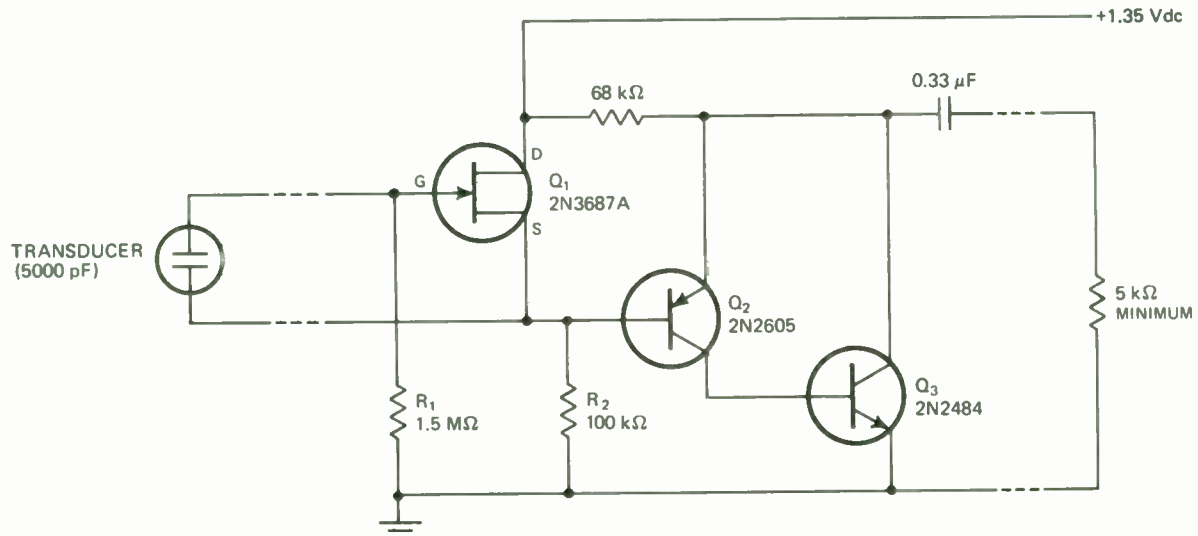
The FET selected for this circuit should have a low pinch-off voltage (V_P) and a low drain current (I_{DDS}) when the gate-source junction is shorted. For the device used, V_P is about 0.1 V and I_{DSS} approximately 100 μA. Because a FET's transconductance (g_m) depends on drain current, Q_1's g_m is only around 50 micromhos.

Since the FET's output conductance is negligible, its output impedance, like that of a common-source stage, essentially equals R_2. Because this is a high resistance value, two bipolar transistors, Q_2 and Q_3, are used as an impedance converter.

This converter stage operates like a pnp emitter-follower, providing very high values of current gain and input impedance. Moreover, it realizes greater bias voltage compatibility between the FET and bipolar stages than a conventional Darlington pair could. Converter bias current is about 6 μA, input impedance exceeds 2 megohms, and output impedance is about 4 kilohms.

For the preamplifier, equivalent input broadband noise is relatively low, about 33 μV from 140 hertz to 20 kilohertz. And voltage gain is nominally 5 (14 decibels). □

Power pincher. Preamplifier for capacitive transducer input dissipates only 13 microwatts and operates from 1.35-volt supply. Bias current of impedance converter, composed of bipolar transistors Q_2 and Q_3, is only 6 microamperes, keeping total circuit current drain to only 10 μA. FET input stage has source-follower bias arrangement but provides voltage gain of common-source configuration.



Two ICs make low-cost video-distribution amp

by M. J. Salvati
Sony Corp. of America, Long Island City, N.Y.

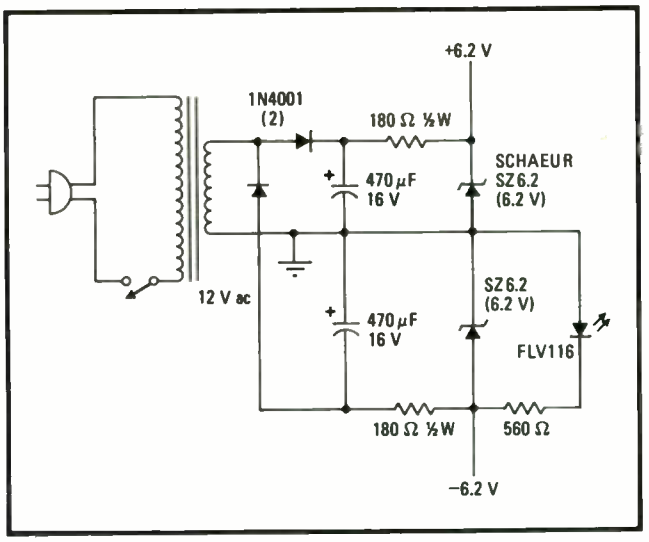
For less than $25 in parts, a video distribution amplifier can be constructed with all the features of commercial models selling for over $300. The circuit shown in Fig. 1 takes the 1-volt peak-to-peak output of a standard video signal generator or TV camera and provides four or more independent outputs that each deliver 1-v pk-pk video into 75-ohm loads. Two input connectors are mounted in parallel because the 50-kilohm impedance is high enough to permit "loop-through" connection, in which a second distribution amplifier is paralleled with the first by means of the second connector. If not used for loop-through, the second connector should be terminated with 75 ohms. The frequency response of the unit is flat from dc to 4 megahertz.

The video distribution amplifier circuit in Fig. 1 uses a National LM318 high-speed operational amplifier and a National LH0002CN current driver in a feedback loop. The resulting output impedance is so low that the output approximates a zero-impedance voltage source, so loads connected to the output resistors have no effect on each other. The 75-ohm output resistors provide the proper drive-source impedance for coaxial cable, short-circuit protection for the LH0002CN, and increased isolation between loads.

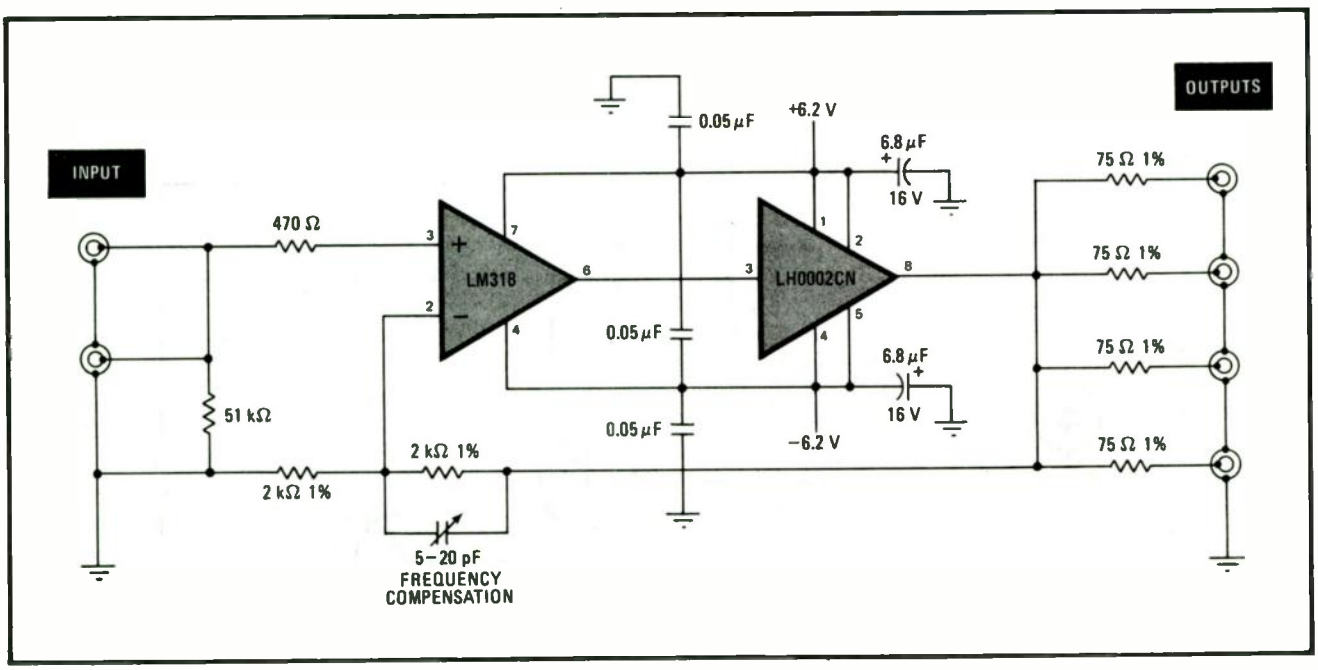
The only adjustment required is the frequency-response compensation capacitor. This trimmer is set to provide the same output amplitude with a 1-MHz sine-wave input as is obtained with a 10-kilohertz sine wave input.

The 6.8-microfarad bypass capacitors should be tantalum electrolytics and should be installed close to the LH0002CN pins. The 0.05-μF bypass capacitors should be disk ceramics installed as close to the LM318 pins as possible. The 75-ohm and 2-kilohm precision resistors must be noninductive types, such as metal film or carbon film.

The outstanding feature of this design is the low cost of the ICs implementing it. Although the slewing ability



2. Power supply. Compact supply uses zener-diode regulation to provide ±6.2 volts required for video distribution amplifier. This power supply and the amplifier shown in Fig. 1 are capable of driving more outputs than the four shown.



1. Video distribution amplifier. Signal from TV camera or video signal generator is amplified to provide 1 v peak-to-peak at each of four outputs matched to 75-ohm loads. Second input connector can be used for "loop-through" connection of a second distribution amplifier or for a terminating resistor. Frequency-compensation adjustment balances stray capacitances, providing flat response from dc to 4 MHz.

of the LM318 is insufficient to handle reliably a 2-V pk-pk output swing at 4 MHz, the amplitude of the highest-frequency component (color burst) in a standard composite video signal is only a small percentage of the overall amplitude, so the LM318 can easily handle a standard video signal.

The power supply recommended for use with this amplifier is shown in Fig. 2. Fig. 3 shows the complete video distribution amplifier and power supply unit packaged in a metal box. □

3. All packed up and ready to go. Amplifier-and-power-supply unit for 4-way distribution of video signals is packaged in metal box. Parts cost for complete assembly is less than $25.

2. Analog-digital converters

Adding automatic zeroing to analog-to-digital converter

by Tom Birchell
Advanced Electronic Controls, Fremont, Calif.

Automatic zeroing can easily be added to a counting-type analog-to-digital converter by using up/down decade counters and a digital-to-analog converter to generate an error-correction signal. The automatic zero function can be especially useful in a-d applications involving strain gages or other sensors where mechanical considerations can cause minute-to-minute changes in the effective zero point.

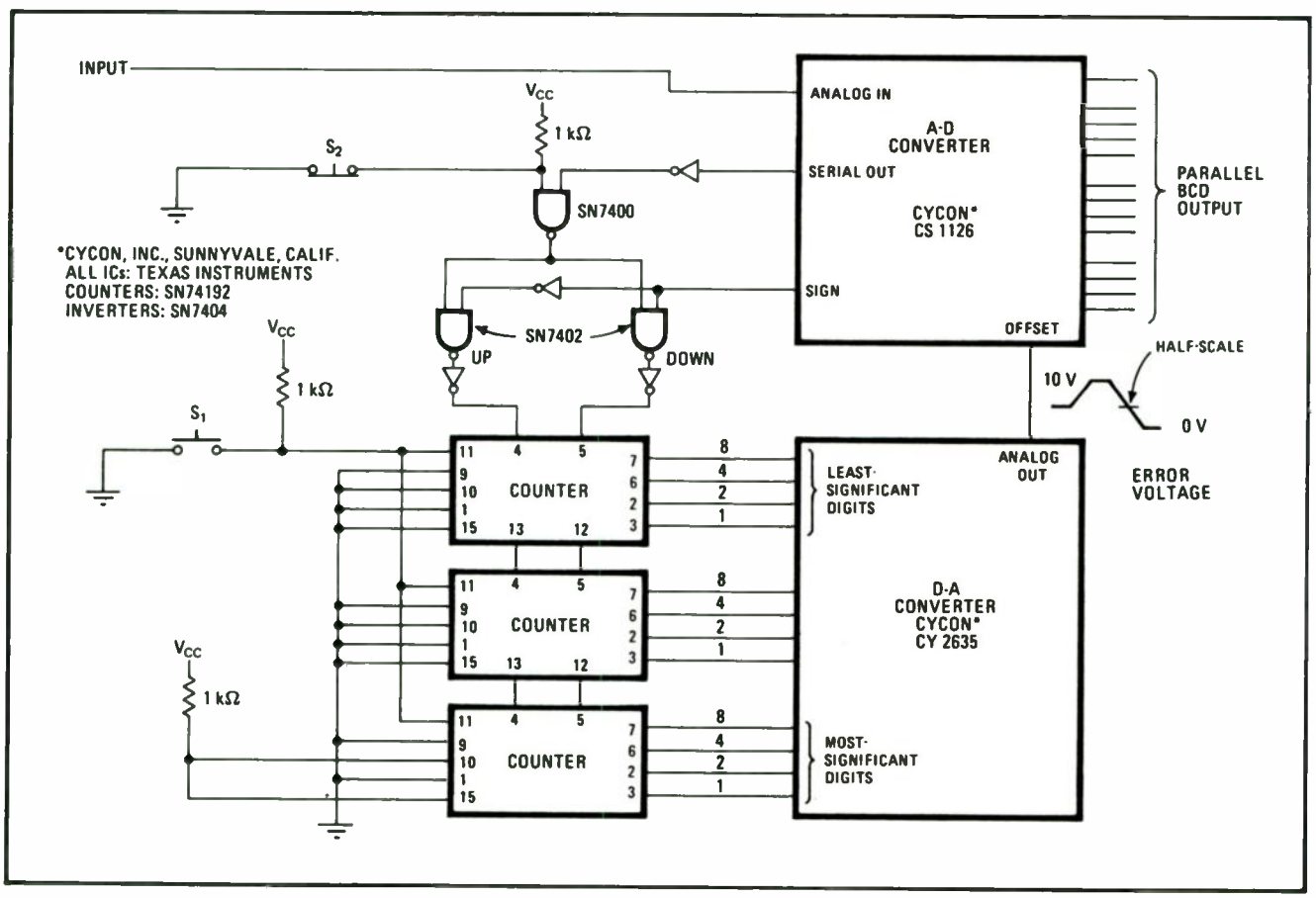
Normally, a zero-setting potentiometer must be adjusted constantly, but with the closed logic servo loop shown, it is only necessary to depress a pushbutton switch to produce the activating logic signal. Essentially, the circuit employs the pulse train occurring at the serial output of the counting-type a-d converter to generate an error voltage. This error voltage is then fed back to the offset-adjustment input of the a-d converter to correct this device's zero setting.

Switch S_1 (which is optional) loads the four-bit synchronous decade counters with a starting number for calibration purposes. Here, the half-scale point of the d-a converter's output is chosen as the calibration number to obtain a symmetrical correction range. If the expected offset variations will occur predominately in one direction, the calibration number should be selected to optimize the correction range.

Once the decade counters are preloaded, switch S_2 initiates the correction cycle. When switch S_2 is depressed, the pulses from the serial output of the a-d converter drive the decade counters either up or down, depending on the error polarity, which is determined by the sign bit. The output voltage of the d-a converter changes accordingly, adjusting the offset input of the a-d converter until no more pulses are produced at this device's serial output. The circuit is now adjusted to the true digital zero point.

For this circuit, the nominal adjustment range is ±7% of the full range of the a-d converter. □

Eliminating offset error. Closed servo loop containing decade counters and digital-to-analog converter automatically zeroes the offset voltage of analog-to-digital converter. Pulse train from the a-d converter's serial output is used to generate the error voltage. Depending on the sign bit, the counters are driven up or down, adjusting the d-a converter's output and, therefore, the offset input of the a-d converter.



Logic system checks out analog-to-digital converter

by Charles J. Huber
Westinghouse Electric Corp., Systems Development Div., Baltimore, Md.

Testing the conversion accuracy of an analog-to-digital converter need not be a laborious and time-consuming task. The test configuration shown can reduce the job to a go/no-go operation without undue expense (approximately $36 for integrated circuits plus the cost of a digital-to-analog converter).

This test system produces a 12-bit digital ramp that is converted (by the d-a converter) to a 4,096-step analog ramp. The analog ramp is applied to the a-d converter under test, and the resulting output from the 10-bit a-d converter is compared to the 10 most significant bits of the 12-bit digital ramp.

An input clock is applied simultaneously to a one-shot delay network and to a ripple-through counter consisting of three four-bit binary counters. The delayed clock becomes the input for six four-bit buffer latches. These accept and delay all 12 of the bit outputs from the counter to remove glitches from the digital ramp. The delayed clock now acts as the basic time reference.

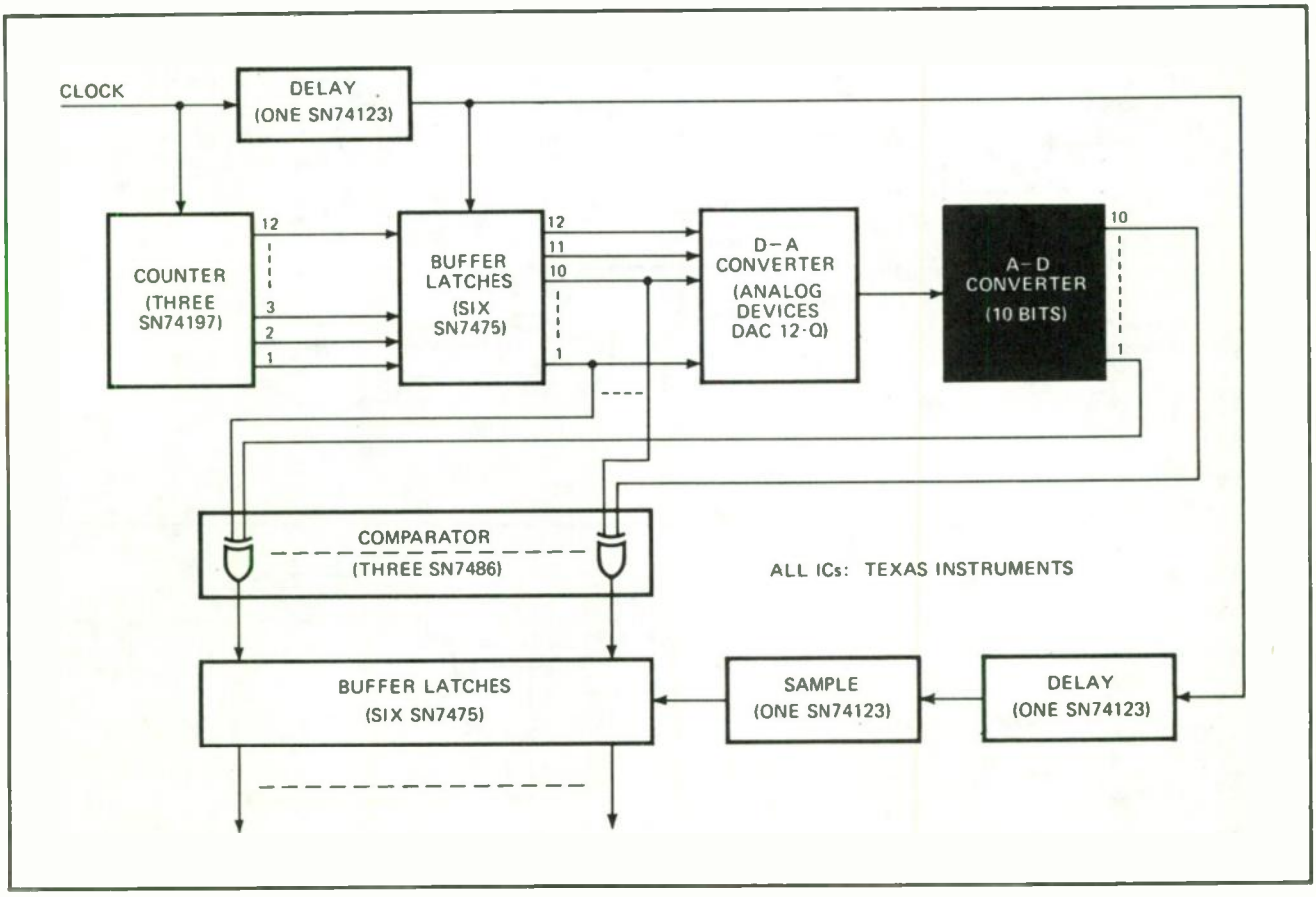
The 10 most significant bits from the latches drive both a d-a converter and a comparator formed by three quad exclusive-OR gates. These gates compare the bits of the digital ramp to the output bits of the a-d converter, on an individual basis. The analog output of the d-a converter corresponds to the input digital code within ±⅛ the least significant bit.

The delayed clock pulse also passes through another one-shot delay network before reaching a sample circuit, which strobes a second set of buffer latches. For zero error at the buffer outputs, the minimum strobe delay equals the a-d conversion time. An interpolating voltage applied to the d-a permits continuous voltage control of the a-d output over the ⅛-bit range.

The test system can accurately determine conversion times of 2 microseconds for successive-approximation and variable-reference a-d converters. Additionally, the nature and position of other conversion errors can be determined by relating displayed error pulses to the digital ramp. For example, small areas of the ramp can be investigated by making constants of the 10 most significant bits of the digital input and using the eleventh and twelfth bits as variable controls.

More system flexibility can be obtained by using an up/down counter to eliminate the d-a converter's slew time when the count changes from 111 . . . 1 to 000 . . . 0. Replacing the counter with a pseudo-random generator allows testing for all input changes. □

Verifying converter accuracy. A-d converter test system generates 12-bit digital ramp with ripple-through binary counter. Buffer latches smooth out any ramp glitches. D-a converter then develops analog input for a-d converter using only 10 most significant ramp bits. Exclusive-OR gates compare a-d output with ramp. Errors pass to another buffer for comparison with appropriately delayed clock.



Height-to-width converter digitizes analog samples

by Roland J. Turner
RCA Corp., Missile and Surface Radar division, Moorestown, N.J.

By controlling the charge on a storage capacitor, a temperature-stabilized height-to-width converter can produce a gray code output from an analog input sample. The converter uses a differential diode-transistor arrangement to operate over a temperature range of −55°C to +65°C, and its conversion error is less than 0.15 microsecond for a full-scale output pulse width of 3.25 μs.

During the first half of the input sample, a clear pulse removes all charge from storage capacitor C_1. During the second half, a charge proportional to the sampled analog signal is placed on this same capacitor through transistors Q_1 and Q_2.

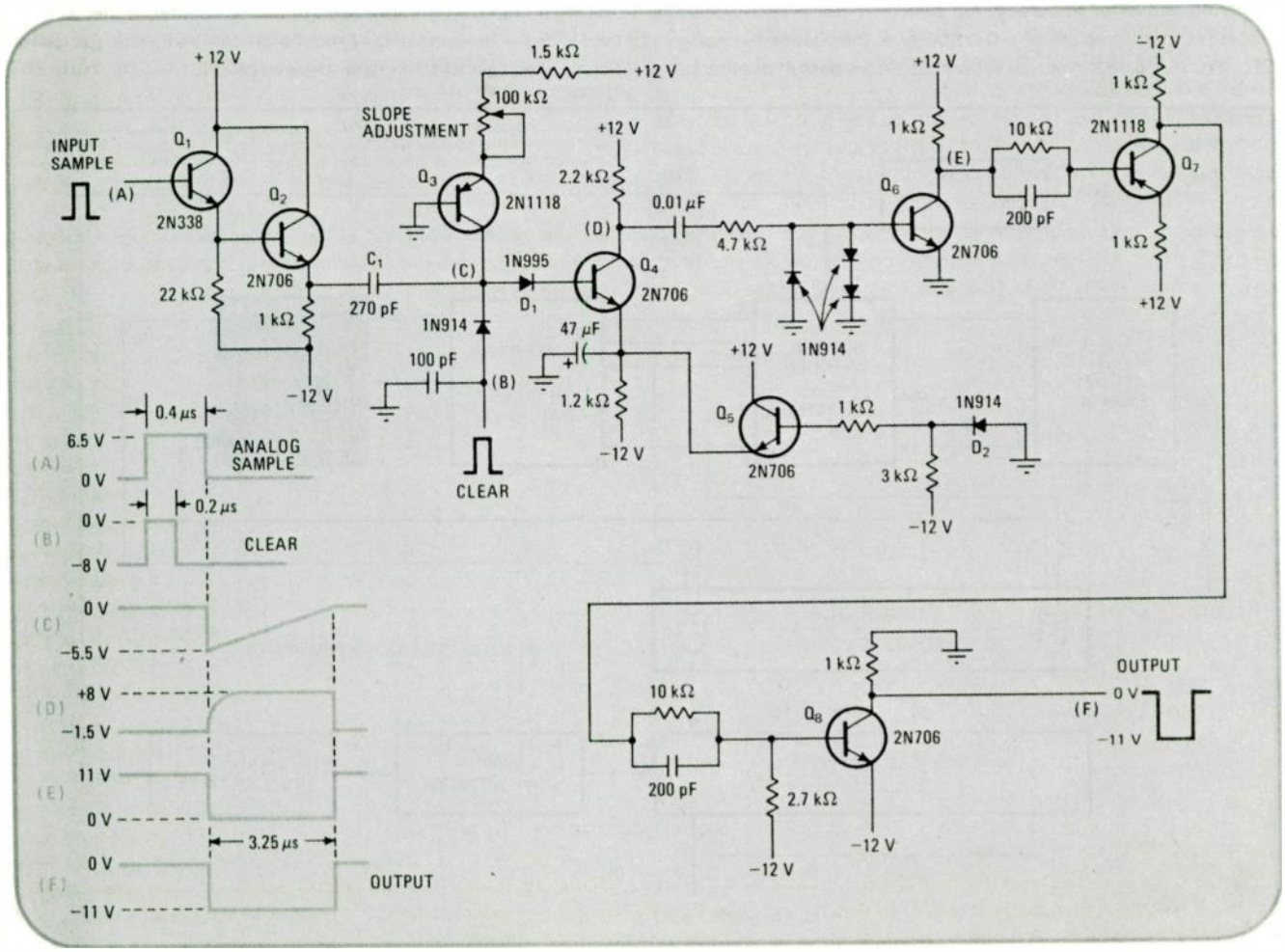
Current source Q_3 keeps diode D_1 forward-biased and transistor Q_4 fully on during the sample time. On the trailing edge of the analog sample, D_1 becomes reverse-biased by a voltage level equal to the amplitude of the analog sample before its termination. Transistor Q_4 is then cut off, and for a period of time that is proportional to the stored analog sample amplitude, a current source formed by Q_3 and the slope-control potentiomteter linearly discharges capacitor C_1.

During the time that Q_4 is off, the converter generates a pulse that has a width proportional to the amplitude of the analog sample. When the stored charge goes to zero, diode D_1 and transistor Q_4 are again turned on by the current source. After Q_4 conducts, a new sample may be processed. Transistors Q_6, Q_7, and Q_8 act as pulse shapers to yield the desired output.

Diodes D_1 and D_2 and transistors Q_4 and Q_5 are connected in a differential configuration to keep Q_4's conduction interval independent of temperature variations. The voltage drops of D_1 and D_2 and the base-emitter voltage drops of Q_4 and Q_5 track each other as temperature varies.

The converter in the diagram is designed to operate with a peak-to-peak video input level of 6.5 volts. Maximum output pulse width is determined by the slope adjustment, which is set to provide a pulse width of 3.25 μs for a an input video level of 6.5 v. The waveforms shown represent the maximum level of the gray code. □

Compensating for temperature. Differential hook-up of transistors Q_4 and Q_5 and diodes D_1 and D_2 maintains temperature stability of height-to-width converter. Amplitude of analog input sample is converted to gray code output. Second half of input sample charges capacitor C_1, then linear current ramp through transistor Q_3 discharges C_1. During discharge time, D_1 and Q_4 are off, and output pulse is produced.



Current source and 555 timer make linear v-to-f converter

by Andrew McClellan
Case Western Reserve University, Cleveland, Ohio

In many situations it is desirable to linearly control the output frequency of a 555 timer circuit by adjusting a potentiometer or an input voltage. In the conventional astable configuration of the 555, the timing capacitor discharges and charges through one or two timing resistors. Thus the frequency is inversely related to changes in the timing components, and is also inversely related to changes in the control voltage.

However, inexpensive and accurate linear voltage-to-frequency conversion can be obtained from the 555 astable multivibrator circuit in Fig. 1. A voltage-dependent current I linearly charges the timing capacitor C so that output frequency increases linearly with the input control voltage V_{in}. During the charging phase of the cycle the capacitor voltage is given by:

$$V_C = V_{CC}/3 + It/C$$

Charging continues until V_C reaches $2V_{CC}/3$, making charging time t_c equal to $V_{CC}C/3I$.

At this point the capacitor rapidly discharges back to $V_{CC}/3$ through the ON resistance R_{CE} of the discharge transistor in the timer (pin 7). The discharge time, t_d, is approximately equal to $0.69R_{CE}C$.

The circuit is designed to make t_c much greater than t_d, so the period T of the multivibrator is very nearly equal to t_c and the frequency f becomes:

$$f = 3I/V_{CC}C$$

The 741 operational amplifier and transistor Q_3 form a voltage-dependent current source such that:

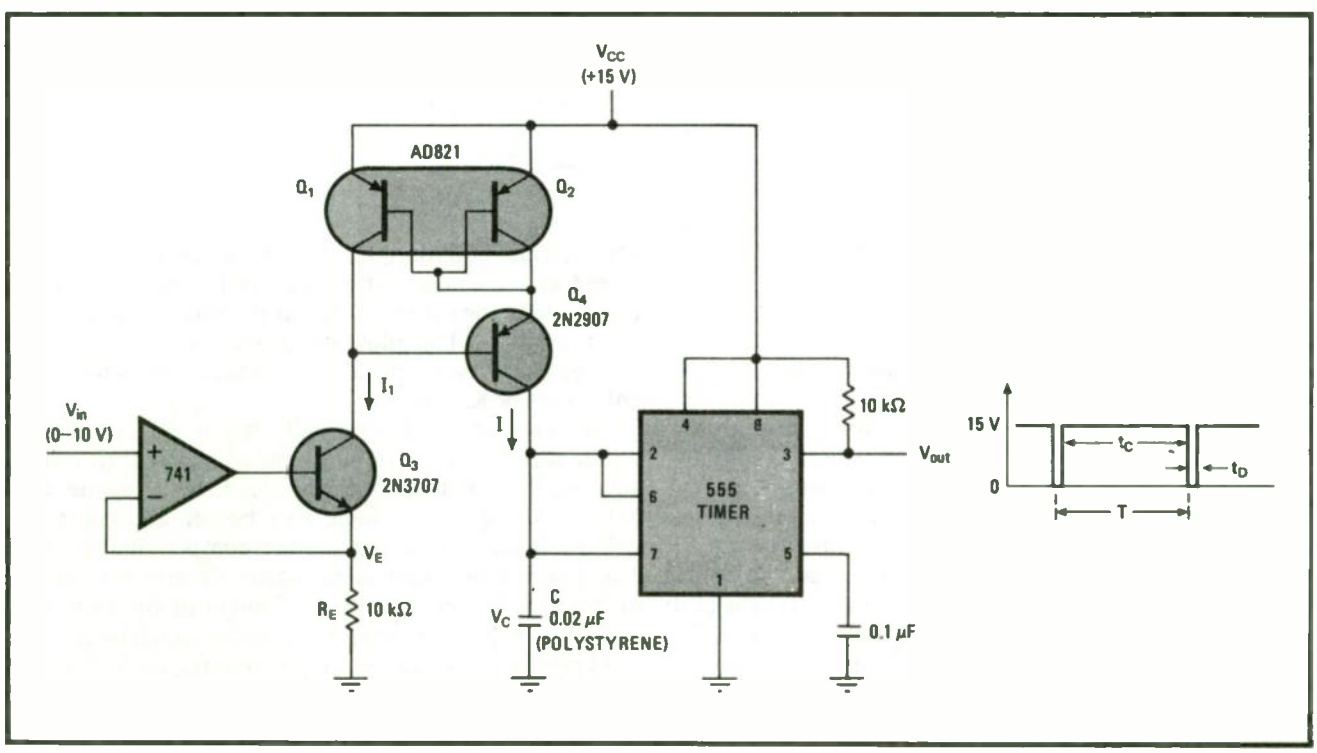
$$I_1 = (V_E/R_E)[\beta_3/(\beta_3+1)] = V_{in}/R_E \text{ (approx.)}$$

where β_3 is the forward current transfer ratio of Q_3. The op amp greatly reduces any drift due to change of V_{BE} in Q_3.

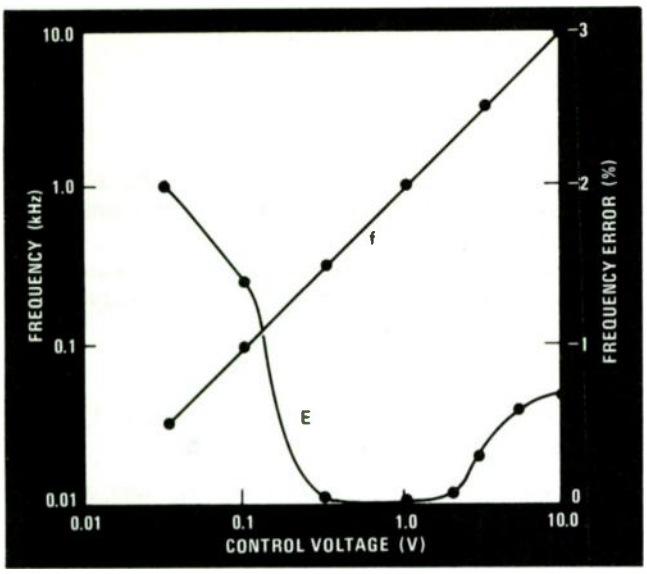
To allow the input voltage V_{in} to be referenced to ground, the capacitor is actually charged by current I from the current mirror formed by Q_1, Q_2, and Q_4 that makes I equal to I_1. The transistor Q_4 functions in a modified cascode configuration to increase the output impedance of the current source and increase the tracking of I_1 and I. Substituting V_{in}/R_E for I in the frequency equation gives:

$$f = 3V_{in}/R_ECV_{CC}$$

For a maximum input control voltage of 10 volts and the parameters used, the charging current can be easily varied over a range from 10 microamperes to 1 milliampere, and the output frequency in hertz is given by:



1. Linear voltage tuning. Inexpensive linear voltage-to-frequency converter uses an op-amp-driven transistor current source and a current mirror to charge the timing capacitor in a 555 astable multivabrator circuit from control voltage V_{in}.



2. Straight and accurate. Graphs show the experimental frequency-versus-voltage relationship, and the percentage departure from linearity, obtained with the circuit in Fig. 1.

$$f = 10^3 V_{in}$$

The experimentally obtained frequency and accuracy are shown in Fig. 2. At high frequencies (10 kilohertz) the non-zero discharge time (t_d) becomes significant and tends to make the frequency less than the predicted value. At low frequencies (100 hertz) the decreased transistor betas and the bias currents of the comparators (pins 2 and 6) decrease the voltage-to-current conversion factor and tend to also make the frequency less than the predicted value. This latter error may be compensated for to some degree by adjusting the offset of the 741 so that $V_E = V_{in} + 1.5$ mV. This has the effect of increasing the conversion factor at low input voltages without seriously affecting the accuracy at larger input voltages. Here this technique reduces the error in the 100-Hz region to less than ±0.4%.

For higher-frequency operation (1–100 kHz), it's better to reduce capacitor C to 0.002 microfarad, rather than decrease R_E; otherwise the ratio of t_d to t_c would become too large, and errors would result at the high end of the frequency range. □

Analog-to-digital converter produces logarithmic output

by Ronald Ferrie
Communications & Controls Co., Pittsburgh, Pa.

When the logarithm of a signal voltage must be converted to a digital number, a log converter is normally used in conjunction with an analog-to-digital converter. But the circuitry involved becomes much simpler if the a-d converter is made to perform the log conversion itself. The resulting digital log converter has a two-decade dynamic range that can be set over a wide range of voltage levels.

In the circuit, a START pulse sets flip-flop FF_1 and resets the counter to zero. This action closes switch S_1 and opens switch S_2. (Field-effect transistors are used for these switches.) The unknown input voltage is now applied to the integrator, charging capacitor C through R_1.

The reference voltage for the comparator is initially set at zero. As the output voltage from the integrator passes through zero, gate G_1 is enabled so that pulses from the oscillator enter the counter at frequency f_o.

When the counter is filled (N pulses accumulated), the next pulse causes the counter to return to zero and to generate a carry-out pulse that resets flip-flop FF_1. This opens switch S_1, disconnecting the input voltage from the integrator, and closes switch S_2, causing capacitor C to discharge through resistor R_2. Also, the comparator reference voltage becomes E_R.

The integrator's output voltage decays until it reaches the comparator reference of E_R. This decay period is:

$$t_x = R_2C \ln(E_{o(pk)}/E_R) = R_2C \ln(E_iN/R_1Cf_oE_R)$$

At time t_x, the comparator output goes to zero, inhibiting gate G_1 and terminating the count. During the decay period, pulses still enter the counter at frequency f_o and accumulate for a count of:

$$N_x = f_o t_x = f_o R_2C \ln(E_iN/R_1Cf_oE_R)$$

Since time t_x began with the counter set to zero, this equation represents the total count stored at the end of the decay period. The expression can be rewritten as:

$$N_x = K_0 \ln(E_i/K_1) - \alpha$$

where:

$$K_0 = f_oR_2C$$

$$K_1 = R_1Cf_oE_R/N$$

$$\alpha = K_0 \ln(K_1)$$

The second equation for N_x shows that the number stored in the counter at the end of the cycle is proportional to the logarithm of the input voltage minus a constant term, α. The plot of output count versus input voltage shows two typical performance curves for different values of K_0 and α.

The log converter nominally has a two-decade dynamic range, which can be extended to about three decades easily and to about 3.5 decades with some difficulty. This dynamic range can be set at almost any voltage level, depending on the components selected. The low-voltage limit is primarily determined by the drift and offset voltage of the integrator op amp. And resistor voltage ratings limit the high-voltage level.

Typically, a two-decade log converter built this way, and having an α value of zero, will accept inputs of 1 to 100 volts, producing an output pulse count of 0 to 460. For such a converter, N = 1,000, f_o = 50 kilohertz, R_1 = 100 kilohms, and C = 2 microfarads. □

Comparators and resistors form clockless a-d converter

by Adrian H. Kitai
Hamilton, Ont., Canada

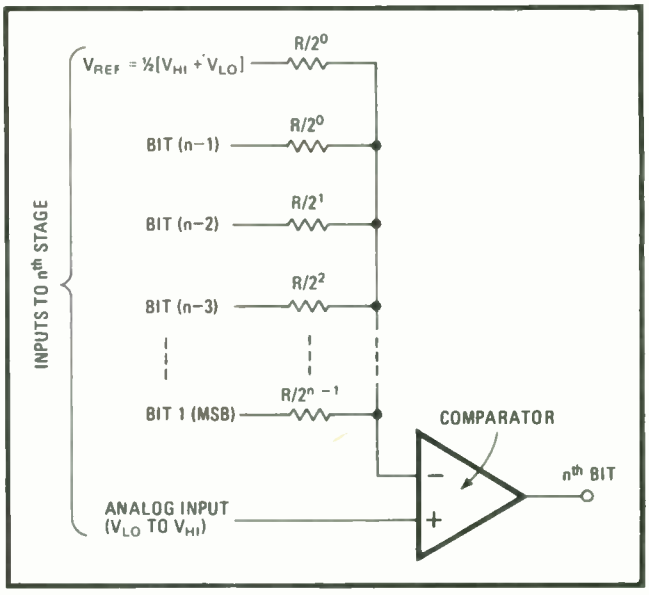
A successive-approximation analog-to-digital converter can be built out of comparators and resistors only. Conversion speed is determined by the settling time of the comparators, and no clock is needed.

The concept is illustrated in Fig. 1, which shows the n^{th} stage of a converter. The analog input voltage is compared with a voltage, the value of which is determined by the outputs of all previous stages, as well as by V_{ref}. A resistor is connected to weight each of the previous comparator outputs, and an additional resistor is connected to V_{ref}, which must be midway between the HI and LO levels of the comparator's output voltage. The n^{th} comparator needs n resistors, except for the first stage which needs none.

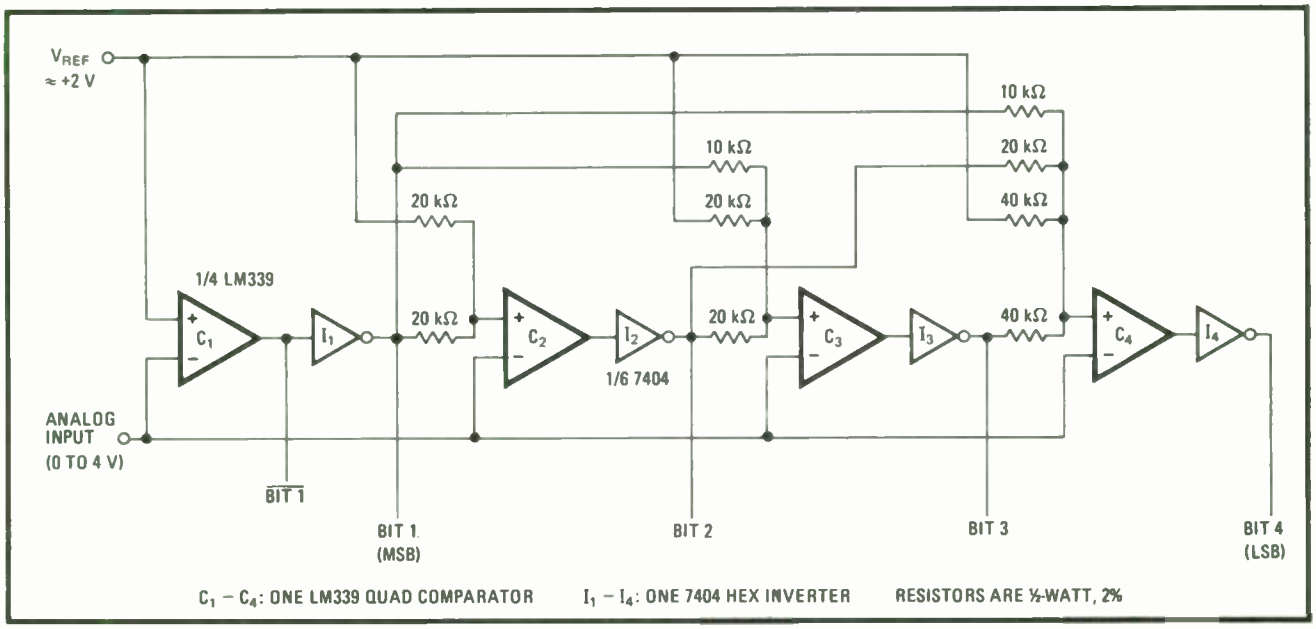
Since, however, the open-collector outputs of the comparators do not deliver voltages of sufficient precision, they are in practice followed by inverters that clamp the voltages. To compensate for this inversion of the comparator output, the input connections to the comparators are the reverse of those shown in Fig. 1; i.e., the analog input signal is connected to the inverting inputs instead of to the noninverting inputs.

Figure 2 shows a practical 4-bit circuit that uses only two inexpensive integrated circuits. This circuit is useful for applications such as driving a display of 16 light-emitting diodes. Comparator C_1 has its positive input tied to V_{ref}. When an analog input lying between ground and $2V_{ref}$ (near +4 volts) is applied to the negative input, the output of inverter I_1 is the first bit. This output is used to establish the switching level for C_2, which is either ½ V_{ref} or ³⁄₂ V_{ref} depending on whether I_1's output is LO or HI. In the same way, the remaining comparators provide bits 3 and 4.

To understand the circuit's operation, assume, for simplicity, that the LO and HI output levels of the transistor-transistor-logic inverters are 0 v and +4 v respectively. Then each of the 16 quantized intervals is 0.25 v wide. Also V_{ref} is set at +2 v. If, for example, 3.4 v (a value within interval 13) is applied to the analog



1. Nth stage. In n^{th} stage of successive-approximation a-d converter, an analog input voltage that lies between V_{LO} and V_{HI} is compared with a voltage determined by an average of the reference voltage and weighted values of the more significant bits. Reference voltage V_{ref} is fixed at the midpoint of the analog input range.



2. No clock. Comparator C_1 compares the analog input voltage with V_{ref}. This defines bit 1 and is averaged with V_{ref} to set the switching level for C_2. Bit 2 is averaged with both V_{ref} and a weighted value of bit 1, to set the switching level for C_3. Bit 4 is obtained similarly. Each output can drive one TTL load. LM339 comparators can sense input voltages down to ground potential, so only a +5-volt supply is needed.

input, bit 1 goes HI (+4 V), and the input to the noninverting terminal of C_2 is therefore the average of 4 V and 2 V, or 3 V. This sets bit 2 HI. When the weighted levels at bit 1, bit 2, and V_{ref} are now combined, the positive C_3 input voltage is 3.5 V. Bit 3 is therefore set LO and is summed along with V_{ref} and bits 1 and 2 to set the plus input of C_4 at 3.25 V; thus bit 4 is set HI. The output of the circuit is therefore 1101, or decimal 13.

The quad LM3339 comparator operates from a single +5-V supply and has a settling time of 1.3 microseconds per bit. The totem-pole outputs of the TTL inverters supply the resistor networks with well-clamped voltage levels. In addition, the complement of every bit is available from the LM339 open-collector outputs. □

Comparator IC forms 10-bit a-d converter

by James M. Williams
Massachusetts Institute of Technology, Cambridge, Mass.

This analog-to-digital converter uses an integrated-circuit comparator to provide an accurate 10-bit representation of an analog signal in 1 millisecond or in 100 microseconds, depending on the clock rate. The circuit, which costs only $13 to build, is accurate over the temperature range from 15°C to 35°C.

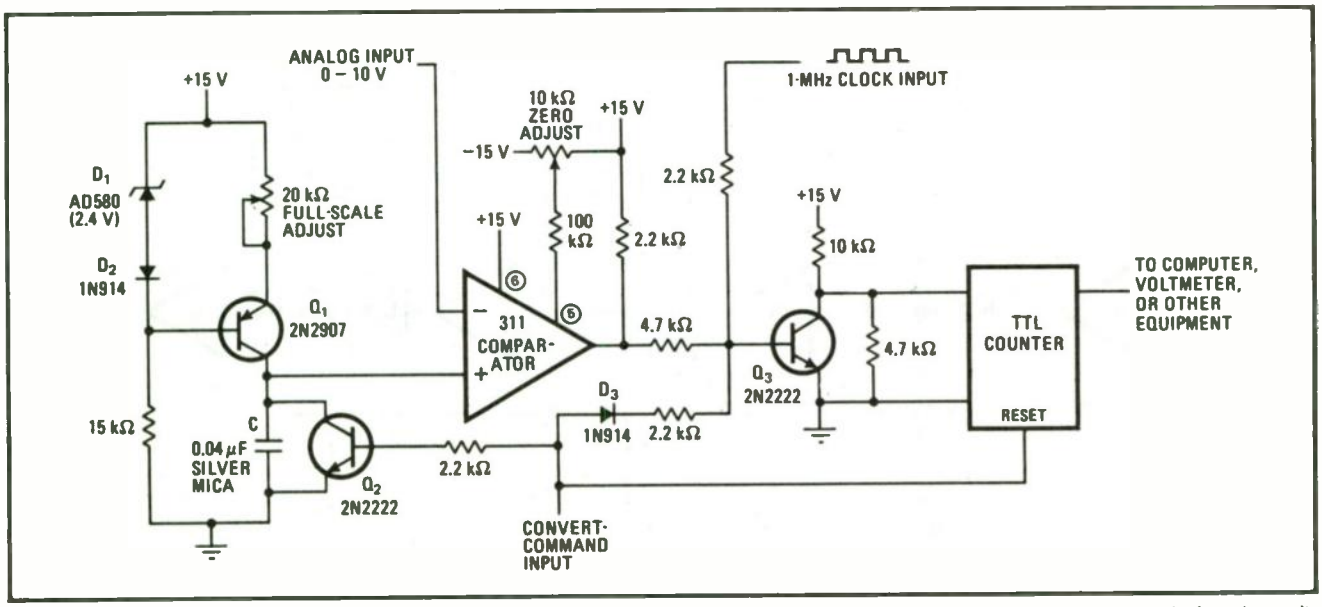
In addition to low cost, advantages include low parts count, low power drain, immunity from power-supply fluctuations, and capability to transmit data over two wires. Disadvantages include the necessity for a stable clock (although one clock can serve many converters), and dependence upon a capacitor for stability. The circuit may be sensitive to noise, but a small RC filter can be used for noise suppression.

Operation over extended temperature ranges is not recommended. If such use is necessary, however, capacitor C (Fig. 1) should consist of a 0.03 silver-mica capacitor in parallel with a 0.01 polystyrene capacitor.

The digital output from this converter is the number of clock pulses counted during the time required for the capacitor to charge up to the level of the analog voltage. As the circuit diagram in Fig. 1 shows, the analog input can be any voltage from 0 to 10 V. This voltage and the voltage across the capacitor are compared in the IC. As long as the analog voltage is greater than capacitor voltage V_C, the comparator allows a counter to count clock pulses. But when V_C reaches the level of the analog voltage, the counting is stopped. The total number of pulses counted is a measure of the analog input. The charging rate of the capacitor is set so the pulse count is proportional to the voltage; e.g., 1,000 pulses corresponds to 10 V.

The detailed operation of the a-d converter in Fig. 1 is straightforward. Transistor Q_1, diodes D_1 and D_2, and the resistors constitute a constant-current source for charging capacitor C. The 2.4-V zener D_1 stabilizes the source against power-supply variations, and the voltage drop across D_2 matches the emitter-to-base voltage in Q_1, despite any temperature changes.

The type 311 IC compares the input voltage to the capacitor voltage V_C and controls transistor Q_3. The input voltage is applied to the inverting (−) input of the comparator, and V_C is applied to the noninverting (+) terminal. At quiescence, V_C is about 12 V, so the 311 output is high. This high signal keeps Q_3 on, so that the data line into the counter is grounded and no clock pulses are counted.



1. A-d converter. Integrated-circuit comparator permits counting of clock pulses only while capacitor is charging up to level of analog voltage. With 1-MHz clock shown, conversion of 10-volt analog voltage to 10 bits (1,000 counts) takes 1 millisecond. If clock rate is 10 MHz, and C is 0.004 μF, conversion is accomplished in 100 microseconds.

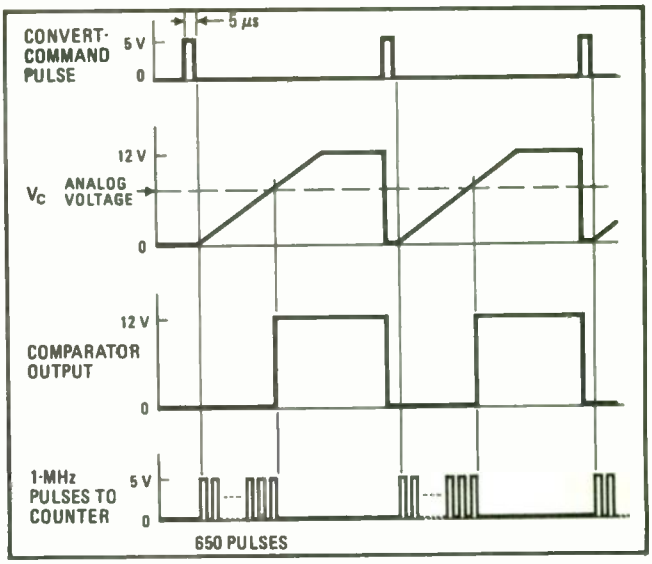
When a convert-command pulse is applied, transistor Q_2 turns on and discharges C, so that the 311 output goes to zero. Diode D_3 and the 2.2-kilohm resistor keep Q_3 on, however, so that no pulses can be counted during the convert command. On the falling edge of the command pulse, Q_1 begins to charge C linearly, and D_3 ceases to hold Q_3 on.

Now, because the output of the comparator is low, the clock pulses can turn Q_3 on and off, so that clock-frequency pulses are delivered to the counter. The combination of the 10-kilohm resistor and the 4.7-kilohm resistor makes the level of these pulses compatible with transistor-transistor logic (TTL) in the counter circuit.

When V_C charges up to the level of the input voltage, the 311 output goes high again, which turns on Q_3 and grounds the data line so that no more pulses are counted. Fig. 2 shows the timing diagram for the converter operation.

To calibrate the counter, a 10-v signal is applied at the input, and the 20-kilohm potentiometer is adjusted so that 1,000 pulses appear at the counter for each conversion command. Then a 0.01-v signal is applied, and the 10-kilohm pot is adjusted so that 1 pulse is counted for each conversion. The unorthodox voltage-offset adjustment for the comparator corrects for incomplete discharge of C; the minimum voltage across C is V_{CE}(sat) of Q_2.

The circuit in Fig. 1 can convert 10 bits (i.e., count 1,000 pulses) in 1 ms. For conversion in 100 μs, the clock frequency must be 10 megahertz, and C must be 0.004 microfarad. Conversion commands can then be given at rates up to 10 kilohertz. □



2. Timing diagram. For an analog voltage of 6.5 V as in this example, 650 pulses are counted while capacitor charges up to turn off comparator output. Convert commands can be given at any rate up to 1 kHz for circuit as shown in Fig. 1.

Coding a-d converters for sign and magnitude

by William D. Miller
Hybrid Systems Corp., Burlington, Mass.

Successive-approximation analog-to-digital converters that provide a sign/magnitude type of output coding are not only hard to come by, they also tend to be costly. In a sign/magnitude-coded output, the output bit values are identical for either positive or negative inputs of the same magnitude, and an extra bit (a sign bit) is used to distinguish between the two input polarities. A fairly simple circuit can be used to develop sign/magnitude output coding for either a unipolar converter or a bipolar converter having an offset-binary-coded output.

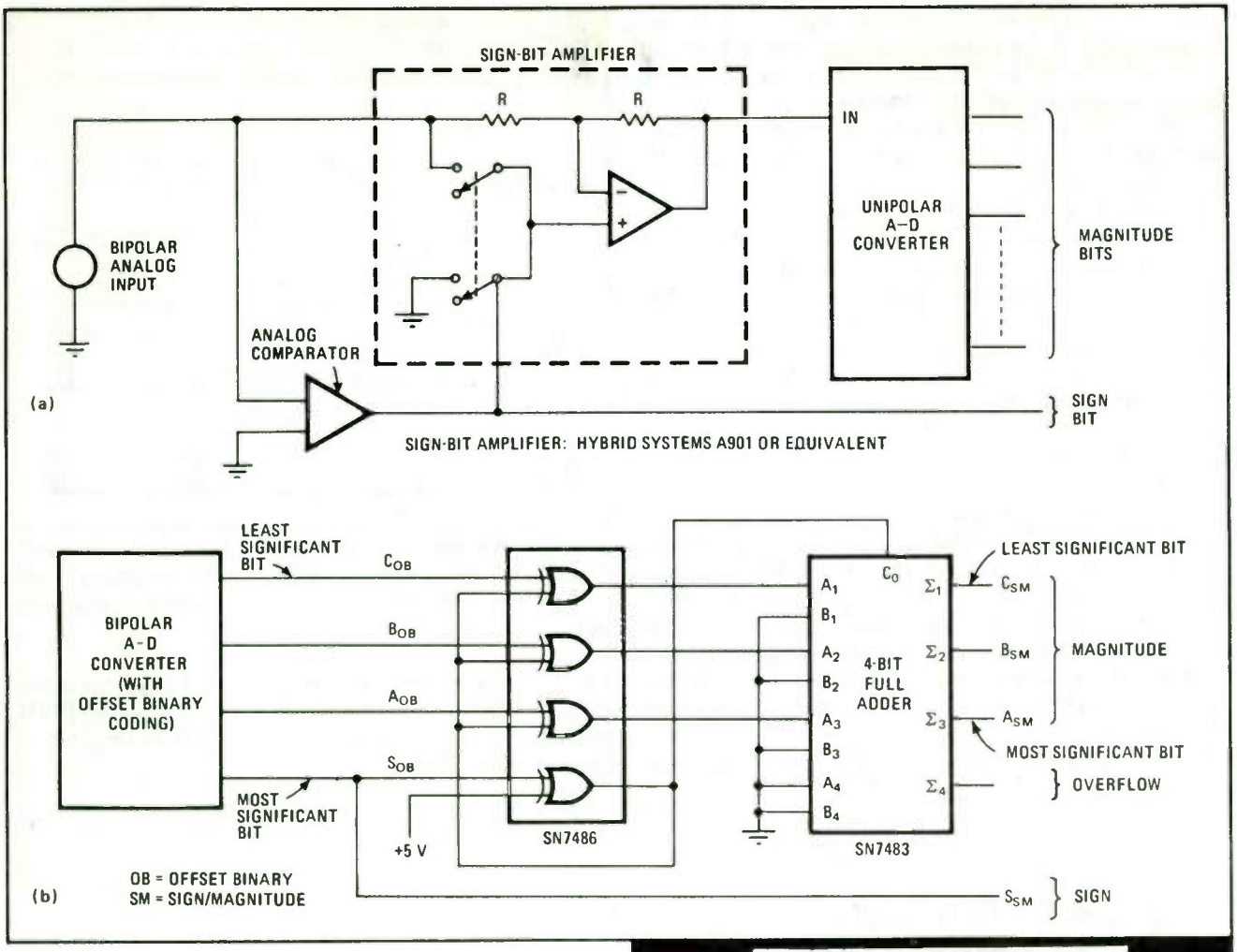
For the unipolar converter, an analog circuit (a) consisting of a sign-bit amplifier (or an equivalent absolute-value network) and an analog comparator is placed at the input end of the converter. The circuit maintains the unipolar input to the converter to preserve the magnitude information, while the sign information is generated on a separate line.

Besides accommodating any unipolar code, this approach provides the zero-plus and zero-minus codes that occur within ±½ least significant bit of the true zero input. Parts cost for the circuit, however, is rather high—in the range of $30.

A more economical digital approach (b) can be used if the a-d converter is one of the readily available bipolar types having an offset-binary-coded output. Exclusive-OR gates and full adders are the logic elements needed to convert from the offset binary code to the sign/magnitude code. With this technique, parts cost is only $5 or so for a 12-bit converter.

The figure shows a representative four-bit system. The table compares the offset binary and sign/magnitude codes for the 16 corresponding digital output words. For words 1 through 8, each bit in each code is identical. For words 9 through 16, one code is the two's complement of the other code. For clarity, the most significant bit of each code is assumed to be the same for the same word.

For words 9 through 16, the exclusive-OR gates translate the offset-binary-coded output bits from the converter to a one's complement code. These gates also develop the carry-in bit for the four-bit adder. Three of the adder's output sums provide the sign/magnitude data in the desired two's complement code. The adder's



CODE CONVERSION

	FROM OFFSET BINARY				TO SIGN/MAGNITUDE			
WORD	S_{OB}	A_{OB}	B_{OB}	C_{OB}	S_{SM}	A_{SM}	B_{SM}	C_{SM}
1	1	1	1	1	1	1	1	1
2	1	1	1	0	1	1	1	0
3	1	1	0	1	1	1	0	1
4	1	1	0	0	1	1	0	0
5	1	0	1	1	1	0	1	1
6	1	0	1	0	1	0	1	0
7	1	0	0	1	1	0	0	1
8	1	0	0	0	1	0	0	0
9	0	1	1	1	0	0	0	1
10	0	1	1	0	0	0	1	0
11	0	1	0	1	0	0	1	1
12	0	1	0	0	0	1	0	0
13	0	0	1	1	0	1	0	1
14	0	0	1	0	0	1	1	0
15	0	0	0	1	0	1	1	1
16	0	0	0	0	← OVERFLOW AT Σ_4 →			
	SIGN	MAGNITUDE			SIGN	MAGNITUDE		

Simple conversion. Analog circuit of (a) enables a unipolar a-d converter to accept bipolar inputs and produce a sign/magnitude-coded output. A sign-bit amplifier or an equivalent absolute-value network performs the polarity selection. The digital circuit of (b) translates the offset-binary-coded output of a bipolar a-d converter to a sign/magnitude-coded output. A four-bit system is shown here.

fourth output sum acts as an overflow bit to indicate when the input count exceeds the adder's capacity.

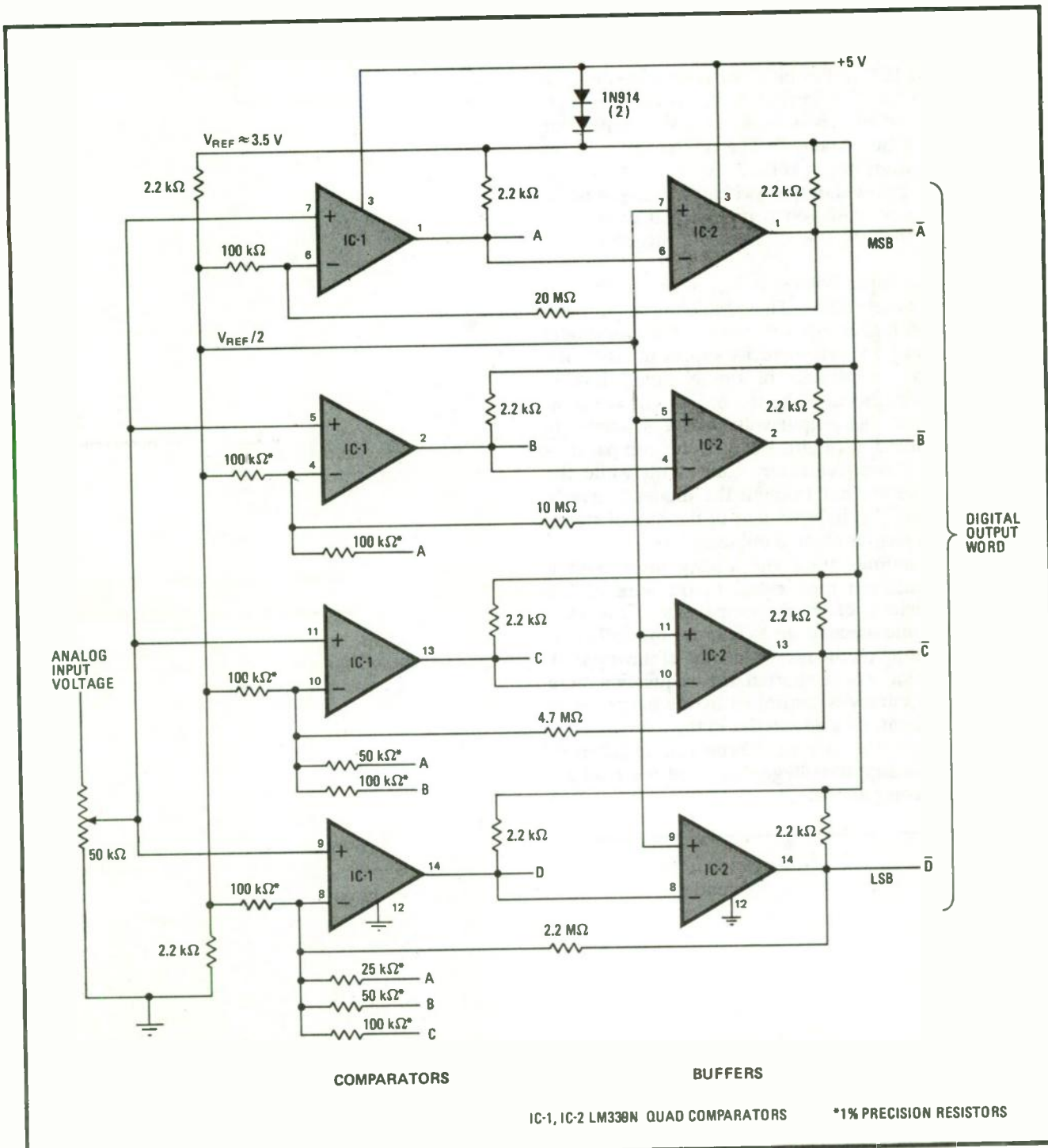
Circuit (b) produces a single nonpolarized output word of 1000 when the analog input is within ±½ least significant bit. Therefore, this circuit is suitable for applications requiring mirror symmetry between corresponding nonzero positive and negative words but not ultrafine resolution about zero. □

Four-bit a-d converter needs no clock

by Craig J. Hartley
Baylor College of Medicine, Houston, Texas

Many analog circuits utilize digitally controlled solid-state switches or multiplexers to adjust filter roll-off, amplifier gain, and the like; and in many such cases the adjustable parameter is itself a function of some analog voltage. As it happens, the 3-bit or 4-bit analog-to-digital converter required in such applications can be built from only three parts—a 5-volt supply and two quad comparators.

Other a-d converter designs generally include a coun-



Four-bit a-d converter. This conversion circuit uses negative feedback to match the digital output word to the analog input voltage one bit at a time. It distinguishes 16 voltage levels between 0 and 3.5 V. This converter does not require a clock, a d-a converter, or digital signals for operation, which makes it convenient for driving a digitally controlled switch in a system where all other elements are analog.

ter, a clock, a d-a converter, a comparator, and other associated digital circuitry. In the design described here, however, the elements of one quad are used as comparators, while the elements in the other quad serve as buffers. The four outputs can drive TTL loads directly.

In operation the state of each output bit is determined in sequence, starting with the most significant bit. The reference voltage for each bit is determined by a resistor network at the inverting input of each comparator. The resistors are connected in a 1, ½, ¼ . . . sequence to ½ V_{ref} and the outputs of each of the more significant bits. The reference voltage for bit A (MSB) is always ½ V_{ref}. For bit B the reference voltage is ¼ V_{ref} if bit A (MSB) is low, or ¾ V_{ref} if bit A is high. The reference for bit C is ⅛, ⅜, ⅝, or ⅞ V_{ref}, depending on the states of bits A and B. The reference for bit D, the least significant bit, is 1/16, 3/16, . . . 15/16 V_{ref}. To eliminate unwanted output switching on input noise, hysteresis of about 0.02 volt is provided at each reference input by the 20-, 10-, 4.7-, and 2.2-megohm feedback resistors.

The full-scale input voltage is V_{ref}, which in this circuit is approximately 3.5 V. (The 50-kilohm potentiometer scales down higher input voltages.) The two diodes set V_{ref} at about 1.5 V below the 5-V supply to satisfy the maximum input conditions of the National LM339 comparators and also to make the output voltage compatible with TTL. The output voltage is approximately 0.14 V (low) or 3.5 V (high). Because the comparator-buffer pairs are complementary (one is off while the other is on), the current through the diodes is nearly constant, making V_{ref} independent of the output states. Total supply current is about 8 milliamperes.

The digital outputs track the analog input with a worst-case acquisition time equal to the sum of the propagation delays of each comparator. This sum ranges from 1 microsecond up to 5 μs for the 339 comparator, depending on the rate of change of the input. A faster comparator would shorten the acquisition time significantly. Accuracy is controlled by the matching of the resistors indicated by an asterisk in the figure.

Compatibility with other logic forms can be achieved by adjusting the supply voltage, V_{ref}, and the load resistors on each comparator. □

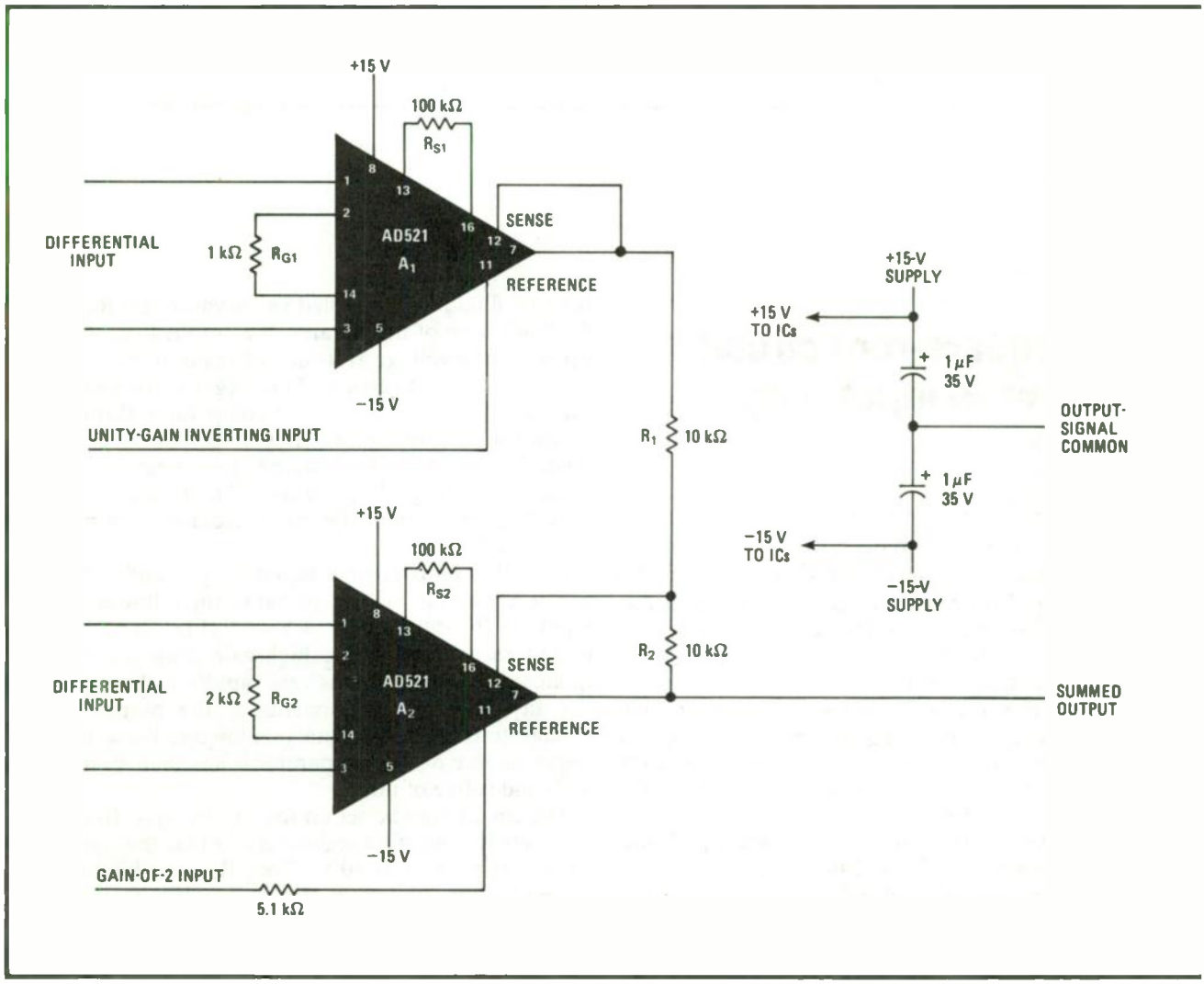
3. Analog signal processing

Two instrument ICs sum six inputs

by A. Paul Brokaw
Analog Devices Semiconductor, Wilmington, Mass.

Connecting two IC instrumentation amplifiers (in-amps) as shown produces an amplifier that will sum six input signals. The six inputs may be independent signals that can be added or subtracted to produce a single output. Alternatively, some of the inputs may be paired in the usual fashion, as shown, to yield two floating differential inputs, leaving the remaining two inputs available for independent use. This latter arrangement sums two input signals that lack a common reference or ground, and the two remaining inputs allow the addition of single-ended signals that are referred to the output signal ground.

One example of the use of this technique is to find the difference between the output signals from two independent bridge circuits, then multiply this difference by



Six-pack. Two instrumentation-amplifier (in-amp) ICs can sum six input signals. The six inputs may be either independent signals or pairs o inputs that lack a common reference or ground and form a differential input as shown. The remaining inputs allow the addition of single-ended signals that are referred to the output-signal common. This technique surpasses conventional operational-amplifier summing that uses virtual-ground current-summing; the op-amp adders work only with single-ended inputs and therefore cannot sum independent signals.

a gain of 100, subtract a fixed offset voltage, and provide an adjustable zero offset. The output of the summing amplifier can then be used to drive a strip-chart recorder.

This technique surpasses conventional op-amp summing amplifiers that use virtual-ground current-summing techniques. Op-amp summing amplifiers present a relatively low input impedance to input signals, and moreover, they work only with single-ended inputs and therefore will not sum independent signals.

The output reference terminals of these in-amps can be used as true signal inputs. The output of amplifier A_1 will thus follow signals applied to this high-impedance point. This output represents the sum of the amplified differential input signal and the reference input signal. Since the ratio of resistor R_{S1} to R_{G1} is 100 to 1, the differential input to A_1 is amplified by a gain of approximately 100.

The output sense terminal of amplifier A_2 is used as a separate high-impedance input in an inverting configuration. This terminal closes amplifier A_2's feedback loop. Resistors R_1 and R_2 convert amplifier A_2 into a unity-gain inverter for the output signal from A_1. These resistors also double the gain of A_2 for signals from its differential and reference input. The ratio of A_2's resistors R_{S2} and R_{G2} is 50 to 1, both to compensate for this gain and to balance the contribution from the two differential inputs to the output signal.

The resulting output consists of A_2's differential input amplified by a gain of 100, from which A_1's differential input amplified by 100 is subtracted, A_2's reference input is doubled and added, and A_1's reference input is subtracted.

The gains of the two differential input channels may be modified by changing the value of resistors R_{G1} and R_{G2} to vary the R_S/R_G ratios. The gains of the two reference terminals may also be modified by changing the ratio of the sense feedback resistors (R_1 and R_2). However, this change may reduce the input signal range. The two gains cannot be changed independently.

If a seventh input is desired, the sense feedback loop of amplifier A_1 should be opened and a pair of resistors added. These resistors will provide an extra input, like R_1 and R_2, with a noninverting (actually twice-inverted) gain to the output. Unlike the other six inputs, however, this seventh one will have a relatively low input impedance and will present a variable load that depends upon the upper reference input voltage. □

Analog square-root circuit handles wide input range

by W.V. Dromgoole
Christchurch, New Zealand

A square-root circuit is frequently needed for linearizing the output from transducers that have a square-law response. It also finds many applications in analog computations. The design described here produces a square root with accuracy within 1% for input voltages in the range from 0 to + 100 volts.

As shown in Fig. 1, the circuit has three operational-amplifier stages: a squarer using op amp A_1, a comparator using op amp A_2, and a voltage follower using op amp A_3. It operates by comparing the scaled input voltage to the square of the voltage that is fed back from the output of the circuit. When the two are equal, the output voltage must be the root of the input.

The positive input voltage at point X is applied to the noninverting terminal of the comparator through resistor R_9. The comparator's output goes positive and charges the capacitor C, the capacitor voltage is buffered by the voltage follower and applied to the inverting input of the squarer by means of the scaling resistor R_3.

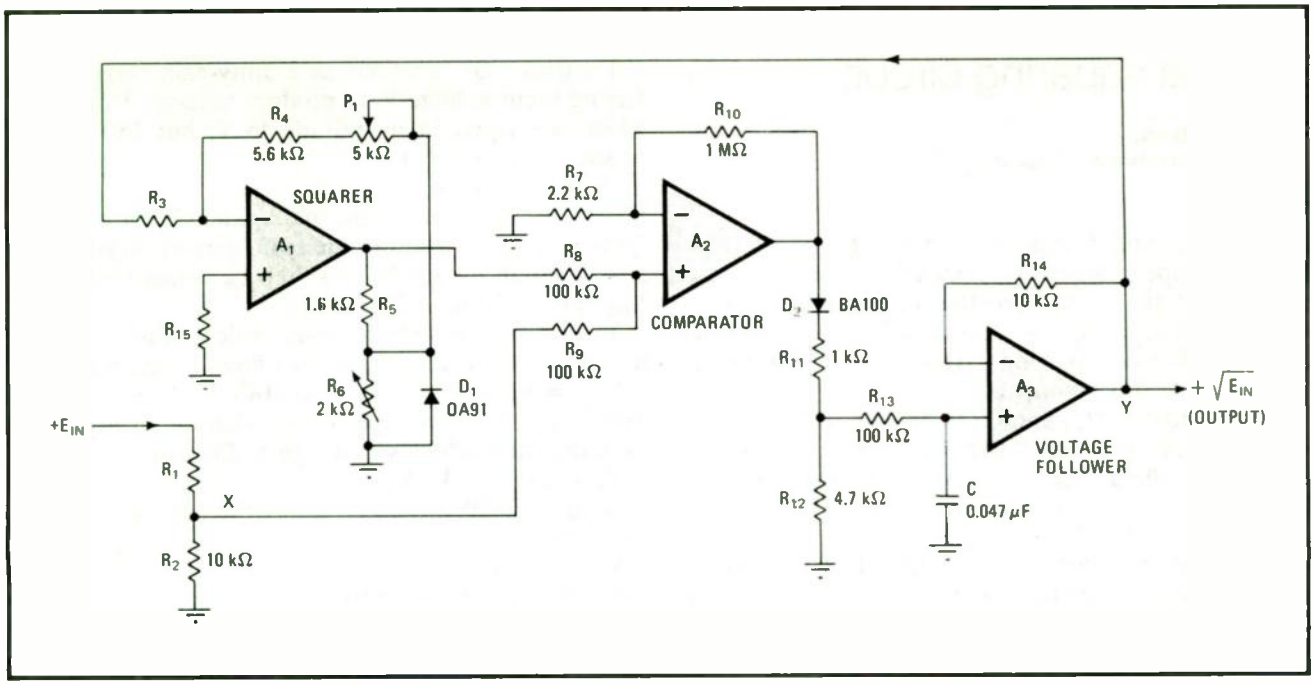
Because of the approximate square-law characteristics of diode D_1 (modified in curvature by R_6) in the feedback loop of the squarer, the output from A_1 is the square of the voltage at its inverting input; it is negative because of the inversion. This negative output drives the noninverting input of the comparator through R_8. When the magnitude of this voltage equals that from point X, the comparator output goes negative, and C discharges through R_{13} and R_{12}. (The function of diode D_2 is to prevent the comparator from putting negative charge on C.)

Thus the comparator automatically modifies the voltage on C to maintain the output of the follower and the input to the squarer at $+V_{IN}^{1/2}$ (Fig. 2). It is connected as a noninverting high-gain amplifier that responds to voltage changes very rapidly without producing any sawtooth components at the output. Swept voltage tests made with an oscilloscope show that the response time of the comparator is less than 10 milliseconds and is free of jitter.

The circuit may be set up for any $V_{IN(MAX)}$ from 10 to 100 volts by adjusting resistor R_1 so that the maximum voltage at point X is 10 v. Since R_2 is 10 kilohms, the value of R_1 in kilohms is ($V_{IN(MAX)}$ - 10). The value of R_3 in the squarer circuit is made 10 $V_{IN(MAX)}^{1/2}$ kilohms.

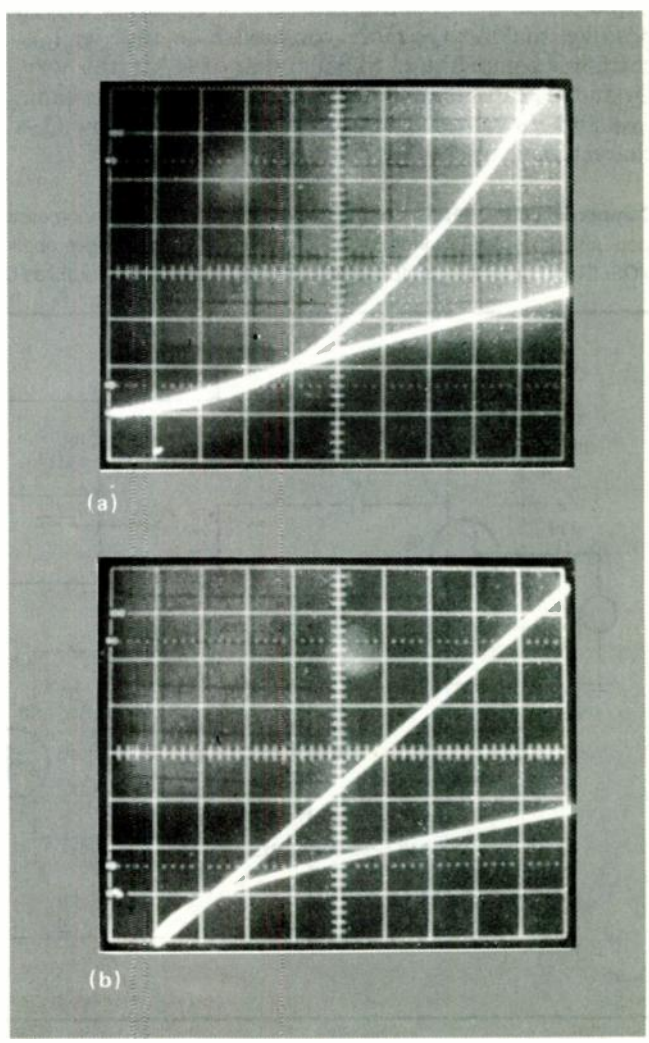
Typical values are:

$V_{IN(MAX)}$ (volts)	R_1 (kΩ)	R_3 (kΩ)
10	0	31.6
50	40	71
100	90	100



1. Getting to the root. Output from three-op-amp circuit is square root of input. Comparator A_2 balances input with square of output to produce the root. Accuracy within 1% is achieved through good square-law characteristic of diode D_1 in feedback loop of squarer A_1, plus adjustment of scaling and tracking controls P_1 and R_6. Voltage follower A_3 buffers voltage across capacitor.

2. Two views of operation. In (a) the upper trace is a square-law input, and the lower trace is the linear output from the circuit of Fig. 1. In (b) the upper trace is a linear input, and the lower trace is the square-root output. Crossovers in photos occur at input of 1 volt.



Potentiometer P_1 is adjusted to make the voltage at point Y exactly equal to $V_{IN(MAX)}^{1/2}$. Finally, resistor R_6 is trimmed to provide the best square-root tracking, P_1 being readjusted as R_6 is varied.

To minimize offset error, resistor R_{15} should be equal to the resistance of the combination of R_3 in parallel with R_4 and P_1. Since $(R_4 + P_1)$ is much smaller than R_3 on any range, however, R_{15} may be made 6.8 kΩ as a good compromise. Diode D_1 should be chosen to have a resistance of about 160 Ω for an applied voltage of 0.8 V. The type 741 op amps use a ±15-V power supply, decoupled with 0.1-microfarad ceramic capacitors at the voltage-input points. □

Quasi-matched MOSFETs form filterless squaring circuit

by W.V. Subbarao
North Dakota State University, Fargo, N.D.

By compensating inexpensive dual-gate MOSFETs so that they appear matched, a squaring and frequency-doubling circuit can be made to function reliably over a broad frequency range without the aid of a filter. Conventional filterless squaring circuits require costly high-quality matched components.

Biasing MOSFETs Q_1 and Q_2 to operate in their depletion region causes MOSFET behavior to resemble that of the junction field-effect transistor. The drain current (I_D) of either Q_1 or Q_2 is given by:

$$I_D = I_{DSS}(1 - V_{GS}/V_P)^2$$

where I_{DSS} is the drain current with both gates shorted to the source terminal, V_{GS} is the voltage between shorted gates and the source terminal, and V_P is the pinchoff voltage (the V_{GS} value when $I_D = 0$).

Since Q_1 and Q_2 are not matched, they may, however have about the same V_P value (approximately -1.5 volts) but exhibit different I_{DSS} values. If Q_2's I_{DSS} current is lower than that of Q_1, say 3 milliamperes as compared to 4 mA, the control gate (G_2) of Q_2 can be driven positive, making Q_2 more conductive so that its I_{DSS} current is compensated to equal that of Q_1. In this way, Q_1 and Q_2 can be made to look matched with the same I_{DSS} and V_P values. The transfer curves show how Q_2's characteristic tracks Q_1's characteristic.

Transistor Q_3 functions as a unity-gain stage, transferring input voltage V_i to produce voltages V_1 and V_2, which are equal in magnitude to V_i but 180° out of phase with each other:

$$V_1 = -V_2 = V_i$$

Effectively, the input to the main gate (G_1) of transistor Q_1 is V_i, and the input to the main gate of transistor Q_2 is $-V_i$. Input voltage V_i can then be considered as the V_{GS} voltage for both Q_1 and Q_2.

The MOSFET transfer characteristic can now be used to solve for the drain current that flows in resistor R_D:

$$I_{D1,2} = I_{D1} + I_{D2} = 2I_{DSS} + 2I_{DSS}(V_i/V_P)^2$$

The output signal voltage contribution can be separated from the output dc offset voltage of $2R_DI_{DSS}$:

$$V_o = 2R_DI_{DSS}(V_i/V_P)^2$$

Letting $K = 2R_DI_{DSS}/V_P^2$ allows the output voltage to be written as:

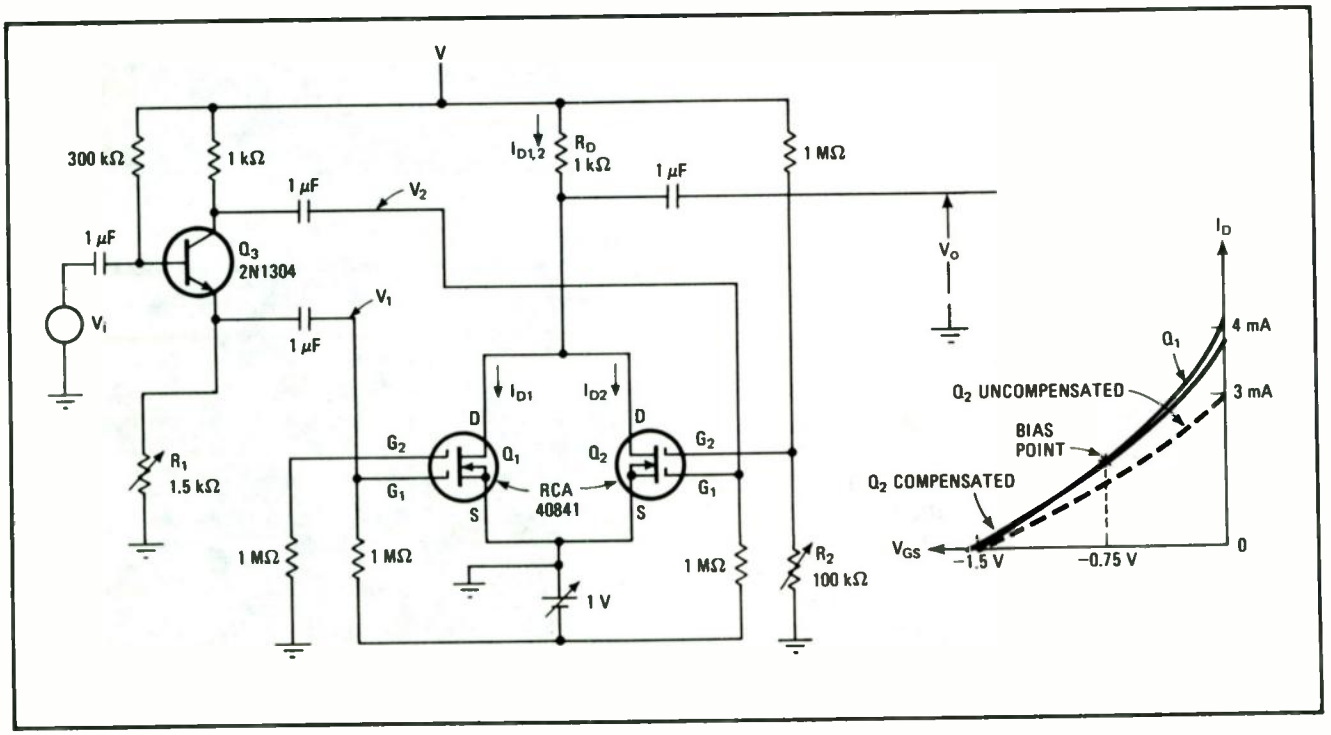
$$V_o = KV_i^2,$$

which is a squaring function.

The value of resistor R_D is held to 1 kilohm to prevent the dc offset current of $2I_{DSS}$ from saturating the MOSFETs when the circuit is operating. Also, peak output voltage swing is restricted to about 1 volt to keep from driving the MOSFETs away from their optimum midpoint bias condition.

For a sinusoidal input, V_o is also a sinusoid at double the input frequency and with a voltage gain of approximately 3.5. Resistors R_1 and R_2 are adjustable so that the Q_1-Q_2 match can be preserved for changing input signal conditions. This permits the circuit to operate from 200 hertz to 1 megahertz without any distortion. □

Compensated MOSFETs double frequency. Filterless squaring circuit works from 200 hertz to 1 megahertz. MOSFETs Q_1 and Q_2 are operated in their depletion mode, causing them to square voltages applied to their main gates (G_1). Adjusting control gate (G_2) voltage forces MOSFETs to simulate a matched pair. Unity-gain transistor Q_3 drives Q_1 and Q_2 with equal voltages of opposite polarity ($V_1 = -V_2 = V_i$).



Timer IC paces analog divider

by Kamil Kraus
Pizen, Czechoslovakia

The quotient of two analog voltages, V_x/V_y, is required in many control and computation applications. This ratio can be produced by a circuit that consists of a voltage-to-frequency converter and an amplitude modulator, as shown in the accompanying diagram.

In the V-to-f converter, input voltage V_y drives a field-effect transistor through an operational amplifier. The FET operates as voltage-controlled resistor to determine the frequency of a 555-timer astable multivibrator. The resistance of the FET is given by:

$$R = V_p^2/[(1+R_1/R_2)I_sV_y - I_sV_p]$$

where V_p is the FET threshold and I_s is the drain current when V_y is zero.

In this mode of operation, the capacitor C charges and discharges between ⅓ and ⅔ of V_{CC}. Thus the output voltage of the timer varies from 5 to 10 volts if the supply is 15 v. The charge and discharge times and therefore the frequency are independent of the supply voltage.

Input voltage V_x is applied to the inverting input of op amp A_2, which acts as the amplitude modulator. When the output from the timer (pin 3 of the 555) goes high, transistor Q turns on and grounds the noninverting input of A_2, so that the output from A_2 is $-V_x$. When the timer output is low, transistor Q is off and the output from A_2 is $+V_x$.

The output from A_2 is therefore $-V_x$ during the charging time of the timer:

$$t_c = 0.693(R+R_B)C$$

and is $+V_x$ during the discharge time of the timer:

$$t_d = 0.693R_BC$$

The average value of the output voltage from A_2 over the period of the timer is given by:

$$\overline{V}_{out} = V_x(t_d - t_c)/(t_c+t_d)$$

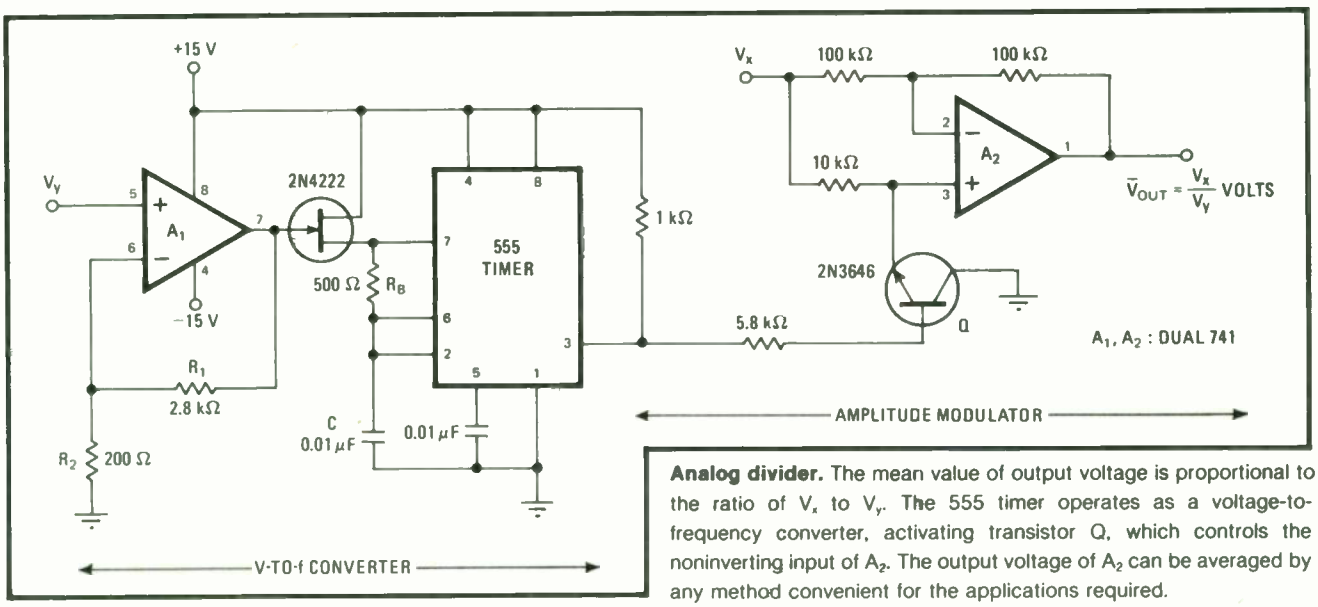
Substitution of the expressions for the charge and discharge times, and use of the relation for R, yield:

$$\overline{V}_{out} = -V_pV_x/(1+R_1/R_2)V_y$$

if R_B is made equal to $V_p/2I_s$. For the 2N4222 FET, V_p is 15 volts and I_s is 15 mA, so R_B is 500 Ω. The value of C is 0.01 microfarad, as recommended by the 555 manufacturer. If the value of R_1 is $14R_2$ as shown, the average output voltage, in volts, is:

$$\overline{V}_{out} = -V_x/V_y$$

Thus the mean value of the output voltage from A_2 is numerically equal to the ratio of input voltages V_x and V_y. These voltages can have any values in the range from 0 to +10 v; the average of the output can be realized with an RC across the output circuit, or read on a damped voltmeter, or whatever the application requires. □



Analog divider. The mean value of output voltage is proportional to the ratio of V_x to V_y. The 555 timer operates as a voltage-to-frequency converter, activating transistor Q, which controls the noninverting input of A_2. The output voltage of A_2 can be averaged by any method convenient for the applications required.

4. Audio circuits

Shift register with feedback generates white noise

by Marc Damashek
Clarke School for the Deaf, Northampton, Mass.

A shift register with linear feedback generates a pseudo-random sequence of pulses that can be used without digital-to-analog conversion or audio processing as extremely high-quality audio white noise. The output from the register, fed directly to an audio amplifier, produces a power spectrum that is flat to within ±1 decibel over the entire audio range.

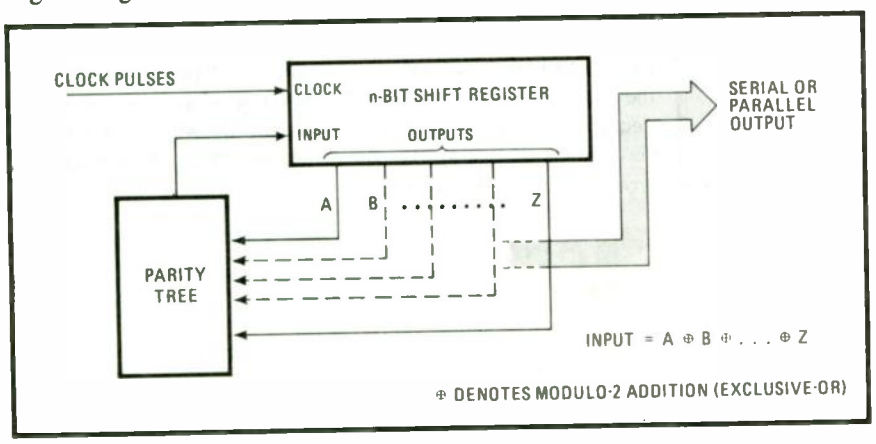
The operating principles of a linear-feedback shift register (LFSR) are illustrated in Fig. 1. The input to the first stage of an n-bit register is determined at each clock pulse by the exclusive-OR (parity) function of some output taps of the register. Choosing these taps is the crucial step in constructing a LFSR that performs as required.

For an n-bit shift register, taps can be chosen so that the register cycles through $2^n - 1$ different states before repeating any previous state. All possible n-bit words are generated except the word containing only 0s [*Electronics*, Nov. 27, 1975, p. 104]. In addition, with the use of only two taps, some shift-register lengths can produce these maximal-length sequences. A partial list of such registers is given in the table, which is excerpted from "Shift Register Sequences," by S. Golomb (Holden-Day Inc., San Francisco, 1967). As the table shows, even shift registers that are only moderately long can produce astronomically long sequences.

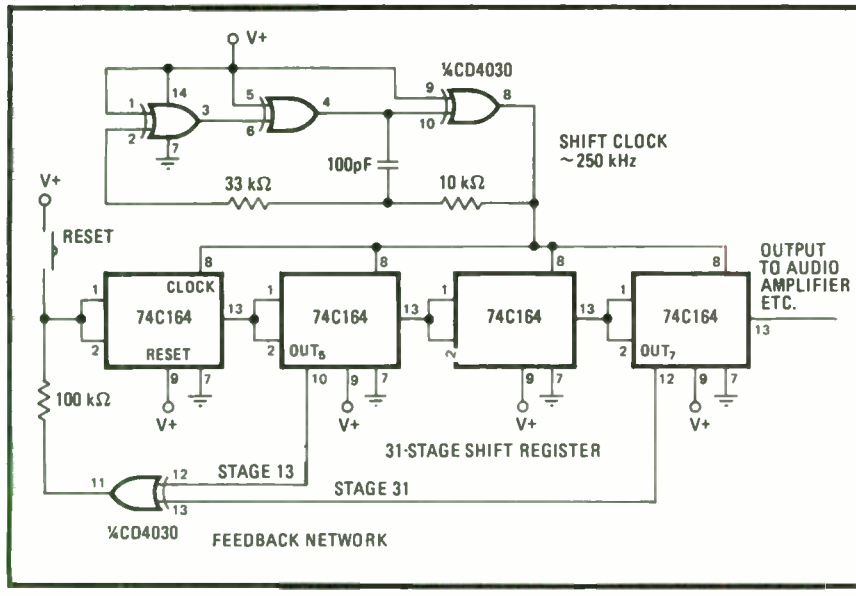
An appropriate clock and a sufficiently long register generate a flat power spectrum of audio white noise, using the digital bit stream itself as the noise source. Fig-

MAXIMUM-LENGTH LINEAR-FEEDBACK SHIFT REGISTERS THAT REQUIRE ONLY TWO FEEDBACK TAPS

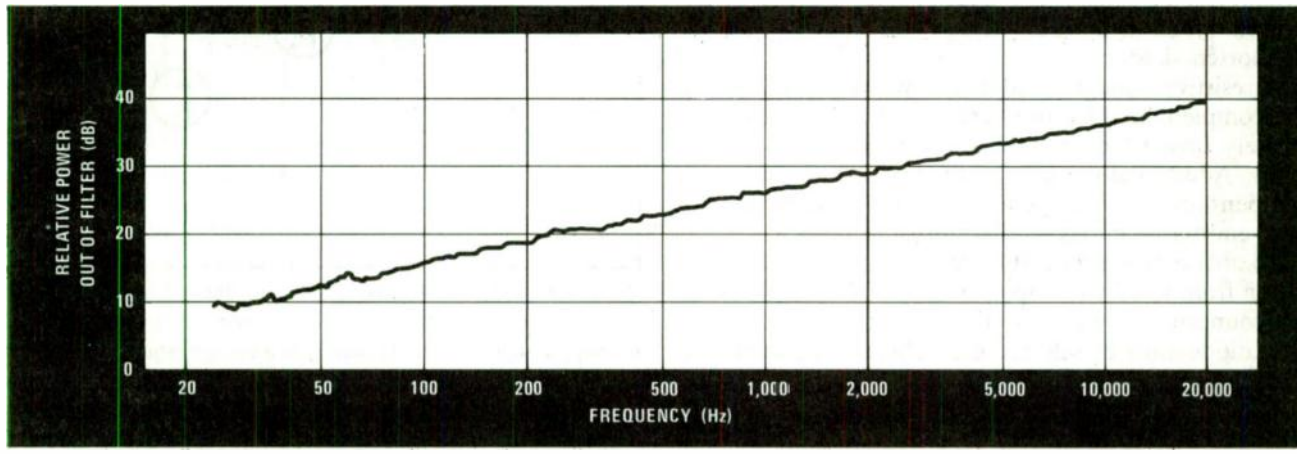
7	1, 7 or 3, 7	127	0.51 ms
9	4, 9	511	2.0 ms
10	3, 10	1,023	4.1 ms
11	2, 11	2,047	8.2 ms
15	1, 15 or 4, 15 or 7, 15	32,767	131 ms
17	3, 17 or 5, 17 or 6, 17	131,071	0.52 s
18	7, 18	262,143	1.0 s
20	3, 20	1,048,575	4.2 s
21	2, 21	2,097,151	8.4 s
22	1, 22	4,194,303	17 s
23	5, 23 or 9, 23	8,388,607	34 s
25	3, 25 or 7, 25	33,554,431	2.2 m
28	3, 28 or 9, 28 or 13, 28	268,435,455	18 m
29	2, 29	536,870,911	36 m
31	3, 31 or 6, 31 or 7, 31 or 13, 31	2,147,483,647	2.4 h
33	13, 33	8,589,934,591	9.5 h
35	2, 35	34,359,738,367	1.6 d
36	11, 36	68,719,476,735	3.2 d
39	4, 39 or 8, 39 or 14, 39	5.5×10^{11}	25 d
41	3, 41 or 20, 41	2.2×10^{12}	102 d



1. Pseudorandom pulses . . . In this linear-feedback shift register, some of the output ports are connected back to the input through an exclusive-OR circuit. Depending upon which output taps are fed back, a non-repeating sequence of any length up to $2^n - 1$ binary words can be generated.



2. . . . generate noise . . . This 31-stage linear-feedback shift register is arranged to produce a maximum-length pseudorandom bit sequence by connection of stages 13 and 31 back to input. Output bit stream, which can be taken from any port, constitutes a white-noise source.



3. . . . like this. The output power spectrum of the circuit in Fig. 2, measured directly at the output of stage 31, slopes upward because filter bandwidth is proportional to frequency. The slope of 3 dB/octave indicates white noise. Reference level (0 dB) was chosen arbitrarily.

ure 2 shows a 31-stage LFSR, with taps at stages 13 and 31 and a shift clock running at 250 kilohertz.

Any shift register that provides access to the required feedback bits will serve. For instance, two CD4006s might have been used instead of the 74C164s. With only three ICs, these shift registers can give access to bits 13 and 31. For a white-noise generator in audio applications, the component values are noncritical. The reset button ensures that at least a single 1 is initially in the shift register, but the manual button can be replaced by a more elaborate initialization circuit if desirable.

The audio-power spectrum from the circuit in Fig. 2, measured directly at the output of stage 31, is shown in Fig. 3. A series of ⅓-octave filters measures the spectrum. The curve is inclined upward at a rate of 3 decibels per octave, matching the increasing bandwidth of the filters. The deviation from a straight line inclined 3 dB/octave is less than 1 dB over the frequency interval from 25 Hz to 20 kHz. The largest deviation occurs at the power-line frequency of 60 Hz. The table shows that the string produced by this register is longer than 2 billion bits and, at a 250-kHz clock rate, will take more than two hours to repeat.

The LFSR pulse sequences are also used for error-correcting codes, spread-spectrum techniques [*Electronics*, May 29, 1975, p. 127], and other random-selection processes. In a maximum-length LFSR n bits long, the bit string produced is statistically identical to $2^n - 1$ flips of an ideal coin (one with precisely equal probabilities of landing heads or tails). Thus, for example, a 17-stage LFSR can generate the equivalent of 131,071 coin-flips. Any stage of the register may provide the output, since every bit is eventually shifted the entire length of the register.

Such a device could be useful for producing uncorrelated stimuli in a psychophysical experiment, because it could easily determine which of two possible stimuli to present to a test subject. It can do so with an undiscernible, yet repeatable, pattern so that a second test subject could be given the same sequence of stimuli. If the bit string from the 31-stage register in Fig. 2 were used for test stimuli with an average interval between stimuli of 5 seconds, it would not repeat for 340 years. □

One-transistor regulator minimizes amplifier distortion

by Dale Hileman
Sphygmetrics Inc., Woodland Hills, Calif.

In a complementary-transistor power-amplifier stage, crossover distortion is usually difficult to control because the extremely critical bias point of the stage is hard to maintain. But when a single bipolar transistor is connected as a voltage regulator, the bias point can be controlled easily through a potentiometer that allows the biasing conditions to be set exactly.

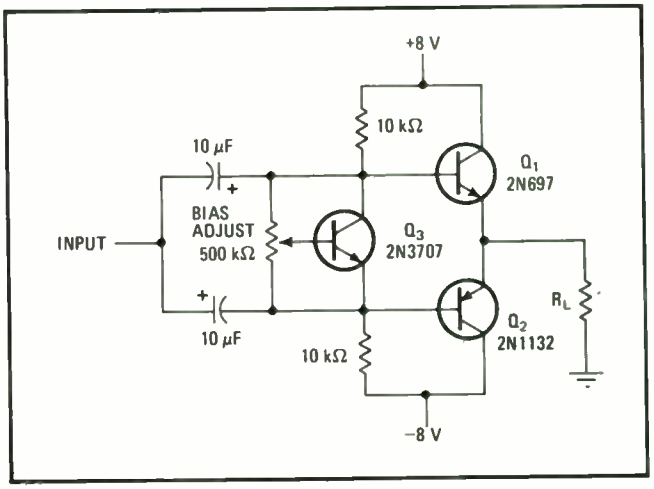
If the base bias current is too small, the stage exhibits severe crossover distortion. On the other hand, too much bias causes a needlessly high collector current; the transistors can be damaged, or their lifetimes considerably shortened. If the stage is powered by batteries (for example, in portable equipment), battery life will be shortened, too.

A resistive voltage divider is sometimes used to bias the complementary transistors, but this scheme can be entirely unsatisfactory unless the bias source is regulated. Additionally, such a divider does not provide compensation for the effects of temperature on the base-emitter junctions of the transistors.

To obtain better regulation and temperature compensation from the divider approach, a diode (or two) is often connected between the bases of the two transistors. This diode must be selected carefully, since it must produce the exact voltage drop needed. What's more, if this voltage drop changes as the equipment ages, the biasing will suffer accordingly.

The circuit shown in the diagram overcomes these problems. It employs a bipolar transistor as a simple voltage regulator and has a potentiometer that sets the stage's bias point precisely. Transistors Q_1 and Q_2 serve as the complementary power amplifier, with transistor Q_3 acting as the bias regulator.

The input to the stage is applied through the two coupling capacitors, and the collector-emitter voltage of transistor Q_3 is set by the potentiometer. The setup provides the optimum base bias for transistors Q_1 and Q_2. If the circuit's operating temperature varies, transistor Q_3 automatically adjusts the bias voltage to compensate transistors Q_1 and Q_2. □



Crossover-distortion regulator. Complementary transistors Q_1 and Q_2 form a power amplifier stage in which the bias point is controlled closely through transistor Q_3 acting as a voltage regulator. The bias-adjusting potentiometer permits exact setting of the stage's bias point so that crossover distortion is held to a minimum. The transistor regulator also automatically compensates for varying temperature.

C-MOS sums up tones for electronic organ

by Robert Woody
Hercules Inc., Radford, Va.

An electronic organ that produces a wide variety of voices, either singly or in combination, can be built with relatively simple circuitry if complementary-MOS logic circuits and linear diode gates are used. The organ, which requires only one gate for each frequency, adds tones to derive the harmonic content of each voice. Sound reproduction varies smoothly, too, so that there are no unpleasing key clicks.

The circuit shown generates the eight frequencies of note A. Adjacent frequencies of the same note have 2:1 ratios and are separated by an octave. Similar circuit arrangements generate frequencies for notes B through G and five sharps, for a total of 12 notes. These 12 notes, each having eight frequencies, comprise the 96 frequencies in the organ. Individual frequencies are spaced

at 6% intervals, from 32.7 to 7,902 hertz.

The eight square-wave outputs of the Hartley oscillator and the binary divider have precise frequencies, but are not musical because square waves contain only the fundamental frequency and odd (not even) harmonics. Furthermore, if these square-wave frequencies are turned on and off directly by key switches, the sounds begin and end too abruptly to be musically pleasing, and key clicks will be heard.

A diode gating circuit, like the one consisting of diode D_1, resistor R_1, and capacitor C_1, is used to convert each square wave to a sawtooth. This supplies the even harmonics and helps to turn the tones on and off gradually without clicks.

The square wave alternates between the supply voltage and ground. While the square wave is at ground, D_1 is forward-biased by current flowing through R_1, and the gate output is also at ground. When the square wave goes to the supply voltage level, D_1 is back-biased so that current through R_1 charges C_1, causing the gate output to have a rising slope. The capacitor discharges quickly through the diode when the square wave returns to ground, and the cycle repeats.

Resistor R_2 and capacitor C_2 slow the application of current to resistor R_1, permitting the gate to turn on and off gradually without clicks. Since C_1 charges for half the cycle of square-wave frequency f, time constant R_1C_1 is half the period of f, or:

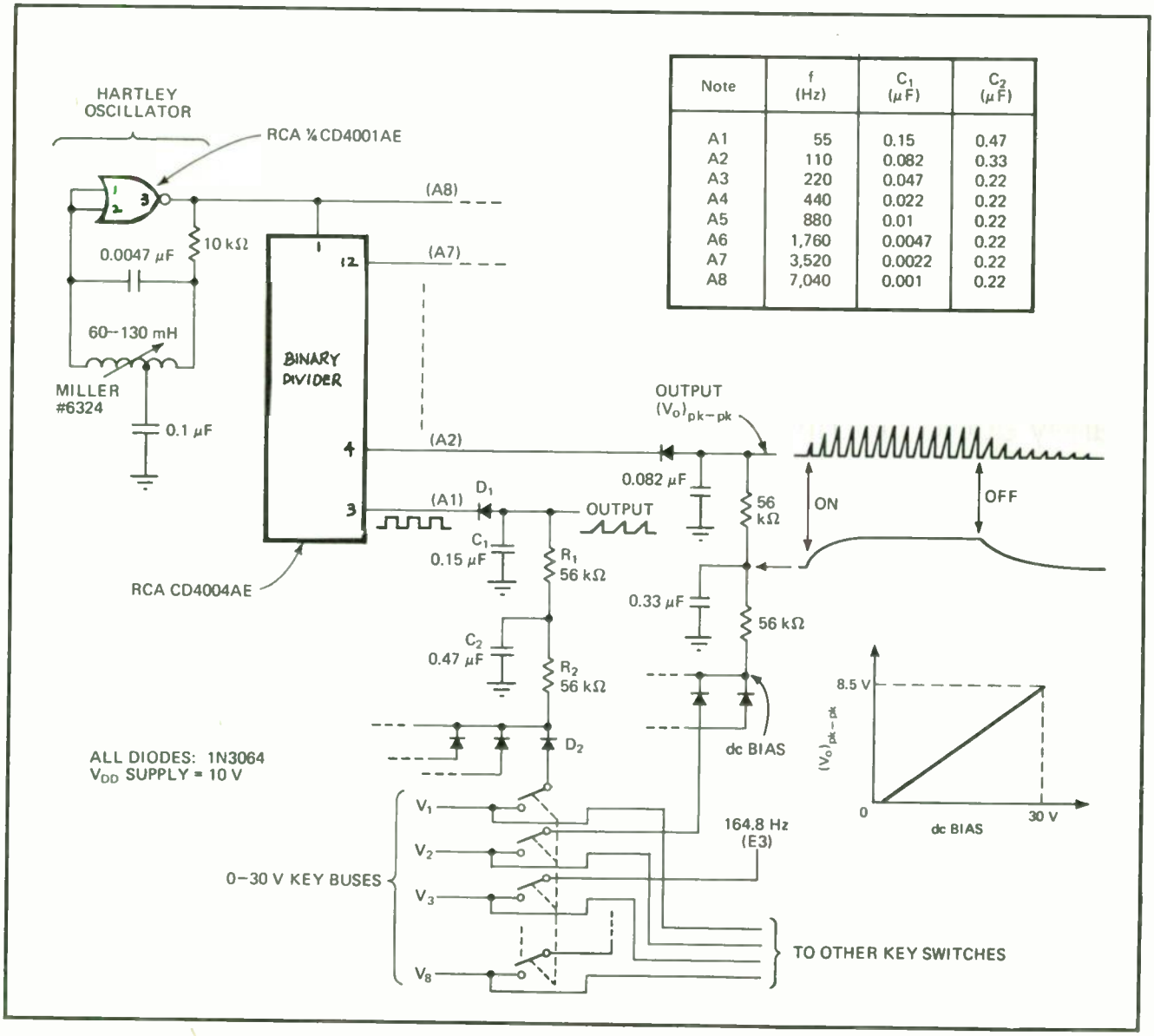
$$C_1 = \tfrac{1}{2}fR_1$$

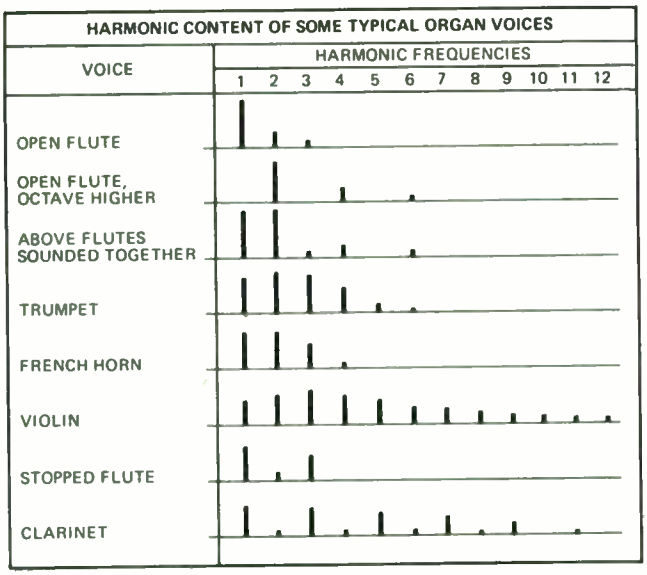
Values for capacitor C_2 are selected to approximate the switching times of organ pipes. Since the output of each gate is linearly proportional to its dc biasing voltage, the tone amplitude needed can be metered out precisely.

To sum tones to create the desired organ voices, which comprise several harmonically related tones, each gate output must be filtered to reduce its harmonics

C-MOS makes organ music. Complementary-MOS ICs add tones to produce eight frequencies that make up note A. Each of the remaining six notes, B through G, plus five sharps, requires its own Hartley oscillator and binary divider network to generate all 96 organ frequencies. Diode gate at each divider output converts that square wave to a sawtooth to get the necessary even harmonics.

Note	f (Hz)	C_1 (μF)	C_2 (μF)
A1	55	0.15	0.47
A2	110	0.082	0.33
A3	220	0.047	0.22
A4	440	0.022	0.22
A5	880	0.01	0.22
A6	1,760	0.0047	0.22
A7	3,520	0.0022	0.22
A8	7,040	0.001	0.22





down to the simplest voice produced in the organ, namely the flute. Since the eight frequencies of a note are multiples or submultiples of each other, they can be handled by one low-pass filter. This means that only 12 low-pass filters are needed for all 96 frequencies.

The diodes between the gates and the key switches—diode D_2, for instance—allow a given tone to be sounded by a number of different key switches. All of the key switches indicated are operated by the key for note A1. The voltages (V_1, V_2, V_3, . . .) on the key buses determine the amplitude at which the tones are sounded (V_1 controls the fundamental frequency tone, V_2 the second harmonic, V_3 the third, . . .). The key bus voltages set the harmonic content and, therefore, the voice of all the keys on the keyboard.

To conserve circuitry, the third harmonic, note A3, borrows a tone from the gate (not shown) used for note E3. The resulting 0.2-Hz frequency error cannot be heard. □

Handy audio amplifier minimizes power drain

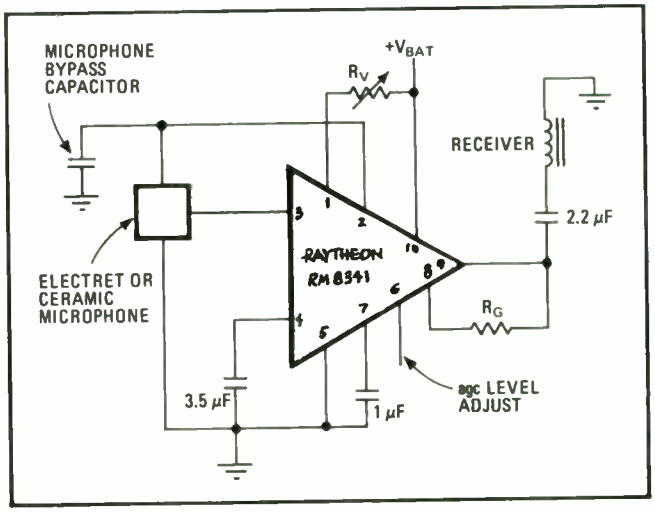
by Fred Riffle
Raytheon Semiconductor Div., Mountain View, Calif.

Primarily intended for use in hearing aids, a low-power-drain, high-gain monolithic audio amplifier includes a number of design features that make it suitable for a variety of other applications, like tape-recorder preamplifiers and wireless microphones. The device even has a controlled operating-power range, enabling it to be used for moderate-level acoustical power gain applications.

As shown by the basic circuit hookup of Fig. 1, amplifier gain can be adjusted with a standard volume control, while maximum gain is determined by a single external resistor. Automatic gain control, which typically covers a 30-decibel gain range, can be added by outboarding just one capacitor. And the amplifier's input is directly compatible with either a ceramic or an electret microphone.

The unit, Raytheon's model RM8341, runs from a single silver-oxide or mercury battery cell at a nominal power drain of 100 milliwatts. It can operate over a supply-voltage range of 1.1 to 1.7 volts. In single-unit quantities, the amplifier sells for less than $8.

Additionally, the space needed by the amplifier and



1. Complete amplifier. IC audio amplifier can operate from a single battery over a wide voltage range. Automatic gain control is implemented by the capacitor at pin 7; maximum gain is determined by resistor R_G. A standard volume control, R_V, can be used.

its supporting network is kept to a minimum, because the RM8341 requires low-value capacitors for frequency compensation. Output distortion is held to 1% nominal, and output linearity is also quite good. The unit provides a single-ended class AB output and can deliver 150 microwatts to a 1-kilohm load.

Figure 2 shows the circuitry of the IC amplifier. Essentially, there are four stages: three in the signal path, and a fourth in the internal dc feedback path.

Stage A_1 (transistors Q_1 and Q_2) and stage A_2 (transistors Q_3 and Q_4) are differential gain networks, which have a composite gain that is proportional to the product of currents I_1 and I_2. The first stage, A_1, is designed to allow the dc level of the input to vary from 0.2 to 0.8 V without affecting output voltage amplitude. Transistors Q_5 and Q_6 are level shifters that provide the proper bias currents for transistors Q_3 and Q_4 of stage A_2.

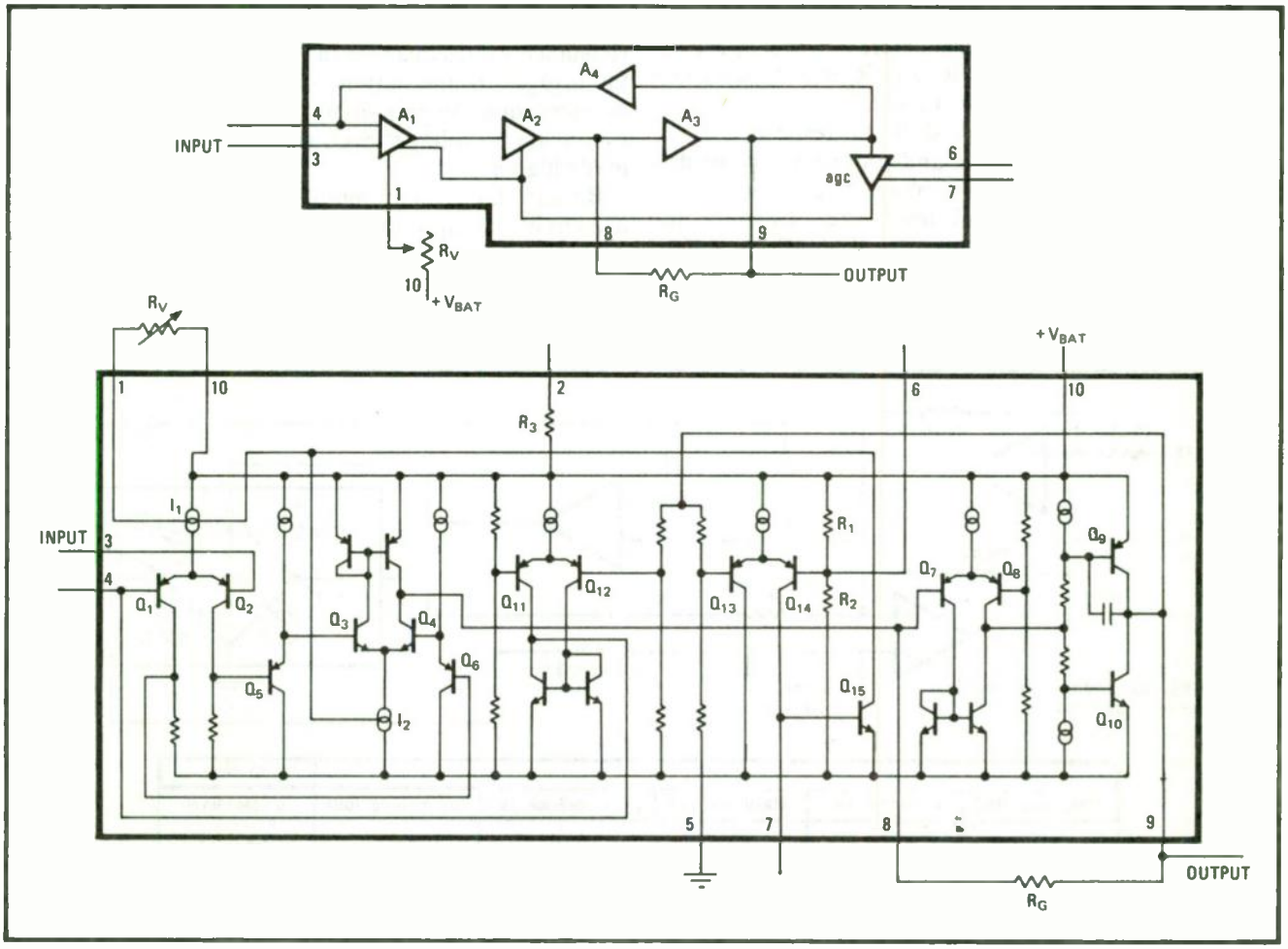
The two current sources, I_1 and I_2, vary simultaneously with the value of volume control R_V but change only slightly with variations in supply voltage. In this way, the gain loss can be held to less than 2 dB when battery voltage drops from 1.6 to 1.2 V.

The power output stage, A_3, consists of transistors Q_7, Q_8, Q_9, and Q_{10}. This stage provides the current demanded at the output of stage A_2 by external gain resistor R_G. Stage A_3, therefore, is a current-to-voltage converter whose gain is proportional to the value of resistor R_G; this resistor, of course, determines what the amplifier gain is at full volume.

The last stage, A_4, is made up of transistors Q_{11} and Q_{12}. Stage A_4 establishes a dc level at the base of transistor Q_2 that fixes the dc level at the output of stage A_3 at half the battery voltage. This arrangement allows the amplifier to handle large ac signals without clipping them. Stage A_4 also determines the amplifier's low-frequency rolloff response.

When the automatic gain control is activated, transistor Q_{13} turns off and transistor Q_{14} turns on, so that the external capacitor from pin 7 to ground begins to charge. This turns on transistor Q_{15} and its rising collector current decreases the magnitude of current sources I_1 and I_2 and, therefore, the over-all gain.

Both gain stages, A_1 and A_2, are employed in the agc loop to obtain more gain compression without distortion. The level to which the agc limits the output can be varied by an external resistor from pin 6 to ground. Internal resistors R_1 and R_2 set the agc level to some nominal value. If agc is not wanted, pin 7 is grounded. Resistor R_3 is for microphone supply-line rejection. □



2. Chip layout. The amplifier consists of four stages, plus a loop for automatic gain control. The gain of stage A_1 (transistors Q_1 and Q_2) and stage A_2 (transistors Q_3 and Q_4) is determined by volume control R_V. Stage A_3 (transistors Q_7 through Q_{10}) is the power output network, while stage A_4 (transistors Q_{11} and Q_{12}) adjusts A_3's dc output level and prevents the ac signal from being clipped.

Audio amplitude leveler minimizes signal distortion

by Edward E. Pearson
Burr-Brown Research Corp., Tucson, Ariz.

An ac current-controlled bridge in the feedback loop of an operational amplifier can provide very close control of signal amplitude, while contributing negligible distortion at or near a predetermined optimum input signal level. The resulting circuit is well suited for amplitude leveling in test oscillators, communications equipment, and telemetry systems. It can be built for around $4 and offers extremely close amplitude control over the entire audio spectrum.

Unlike conventional circuits that apply increasing amounts of feedback along the entire span of input voltage range, this amplitude leveler applies zero feedback (and, therefore, zero distortion) at an optimum input level and produces positive or negative feedback above and below this level. The differential output from a bridge is used to get the desired feedback.

The bridge, which is outlined in color, employs two devices, T_1 and T_2, whose resistance varies with current. Such components as incandescent lamps, thermistors, or even active devices can be used. Here, T_1 and T_2 are incandescent lamps. Resistors R_1 and R_2 are chosen to be within the resistance range of T_1 and T_2.

A specific voltage, V, will shift the resistance of T_1 and T_2, balancing the bridge and producing a zero differential output ($e_1 - e_2$). As voltage V is varied above and below the zero output level, the bridge is unbalanced in opposite directions and develops differential outputs of opposite phase.

Letting $R_1 = R_2 = R$ and $T_1 = T_2, = T$, voltage e_1 can be expressed as:

$$e_1 = TV/(T+R)$$

and voltage e_2 is:

$$e_2 = RV/(T+R)$$

so that the differential voltage becomes:

$$e_1 - e_2 = (T-R)V/(T+R)$$

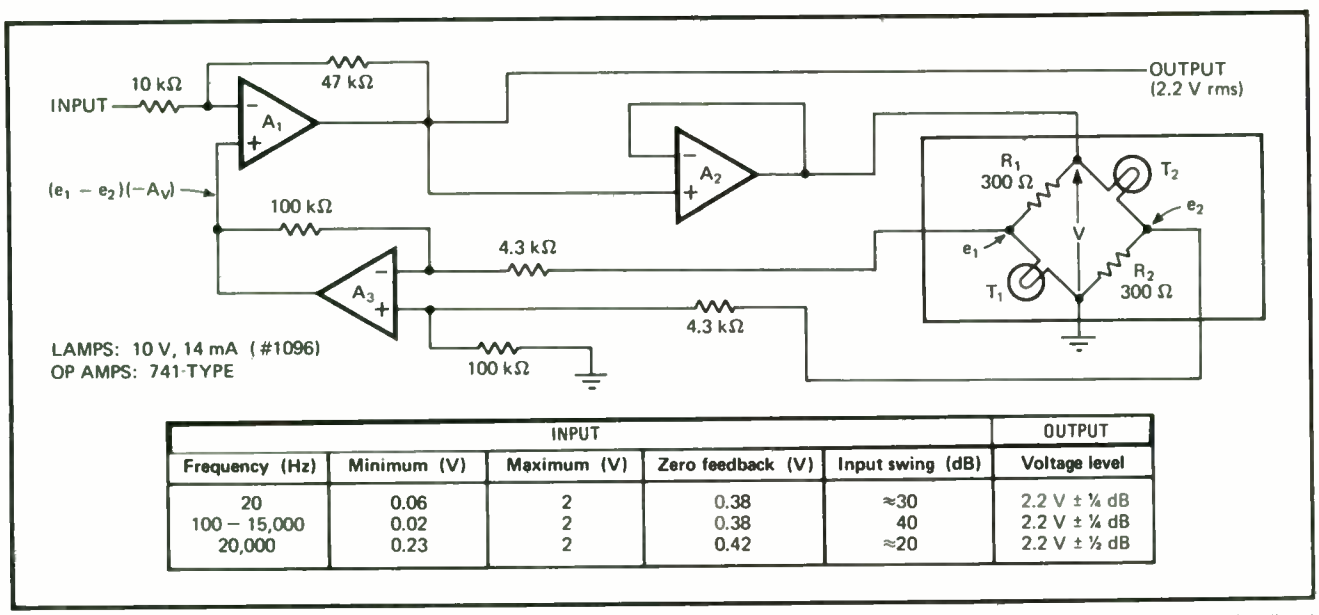
When T is greater than R, $e_1 - e_2$ is more than zero; when $T = R$, $e_1 - e_2 = 0$; and when T is less than R, $e_1 - e_2$ is smaller than zero.

Depending on the input signal level present at amplifier A_1, the network formed by the bridge and amplifiers A_2 and A_3 produces positive, negative, or zero feedback. For the component values indicated, an input voltage of approximately 0.4 volt is just sufficient to drive the bridge to a balanced condition (zero feedback).

At this input level, the components in the feedback network cannot contribute to distortion in the output. If the input voltage varies from the optimum 0.4-v level, the inputs to amplifier A_3 will become unbalanced, and an amplified differential voltage (from the bridge) will produce gain compensation at amplifier. A_1. The table indicates the range and degree of amplitude control obtained.

The circuit's output voltage can be made higher by increasing the value of resistors R_1 and R_2; the higher resistance values increase the voltage needed to balance the bridge. Or, the output voltage can be made smaller by increasing the gain of amplifier A_2. To lower the optimum input voltage level, the gain of amplifier A_1 is made higher.

Because increasing amounts of positive feedback are present at the input to amplifier A_1, the circuit becomes unstable at very low or zero input levels. The table shows the minimum permissible input levels; the circuit must be modified to accommodate input signal drop-outs. □



INPUT					OUTPUT
Frequency (Hz)	Minimum (V)	Maximum (V)	Zero feedback (V)	Input swing (dB)	Voltage level
20	0.06	2	0.38	≈30	2.2 V ± ¼ dB
100 – 15,000	0.02	2	0.38	40	2.2 V ± ¼ dB
20,000	0.23	2	0.42	≈20	2.2 V ± ½ dB

Leveling audio signals. Rather than increasing feedback with increasing input voltage, audio amplitude leveler operates at zero feedback for an optimum input voltage. Current-controlled bridge in feedback loop of amplifier A_1 develops the differential voltage needed to keep the output level steady. The incandescent lamps act as current-variable resistors that balance the bridge when input voltage is 0.4 volt.

Synchronous noise blanker cleans up audio signals

by M.J. Salvati
Sony Corp. of America, Long Island City, N.Y.

Fluorescent lights, gas rectifiers, neon lamps, SCRs, and triacs all produce a substantial rf signal that often radiates through their power-line connections and interferes with nearby communications receivers. This type of radio interference desensitizes the receiver and makes the recovered audio signal very difficult to understand.

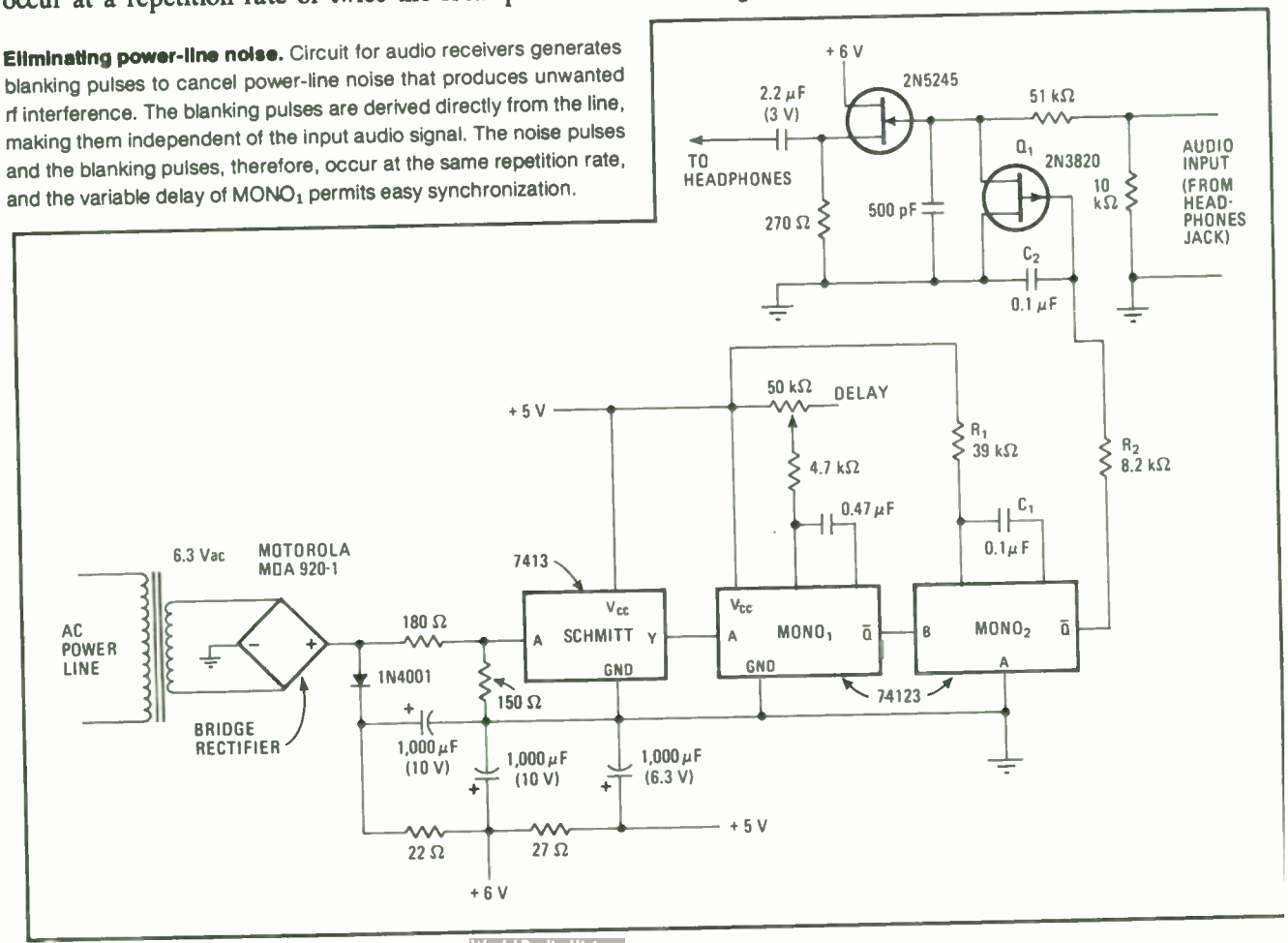
The circuit shown here significantly improves the audio intelligibility of a receiver by eliminating the noise pulses generated by a single dominant nearby noise source. The noise pulses are removed from the audio signal with only slight distortion. Moreover, since this noise-blanking circuit is not internally connected to the receiver, it can be moved from one receiver to another as needed.

The noise pulses produced by power-line radiation occur at a repetition rate of twice the local power-line frequency. Since the noise-blanking circuit is driven by the same power utility as the noise source, the output signal from the bridge-rectifier section of the noise blanker will have the same rate as the noise pulses.

The source of the blanking pulses, therefore, is independent of the input audio signal. The blanking pulses cause the FET gate (transistor Q_1) to conduct to silence the receiver. Since the blanking pulses are not derived from the input signal, their timing does not depend on the shape and rise time of the noise pulses, nor is it affected by the modulation characteristics of the desired signal.

The output from the bridge rectifier is shaped by a Schmitt trigger that drives a dual monostable multivibrator. The first monostable ($MONO_1$) delays the blanking pulse, which is produced by the second monostable ($MONO_2$), relative to the rectifier's output. The delay is variable so that the blanking pulse can be positioned to coincide with the noise pulse.

The width of the blanking pulse is determined by resistor R_1 and capacitor C_1. The fast rise time of the blanking pulse (from $MONO_2$) is slowed down by the low-pass filter formed by resistor R_2 and capacitor C_2, thereby minimizing the distortion of the recovered audio signal □



Eliminating power-line noise. Circuit for audio receivers generates blanking pulses to cancel power-line noise that produces unwanted rf interference. The blanking pulses are derived directly from the line, making them independent of the input audio signal. The noise pulses and the blanking pulses, therefore, occur at the same repetition rate, and the variable delay of $MONO_1$ permits easy synchronization.

Microphone preamp gets power through signal cable

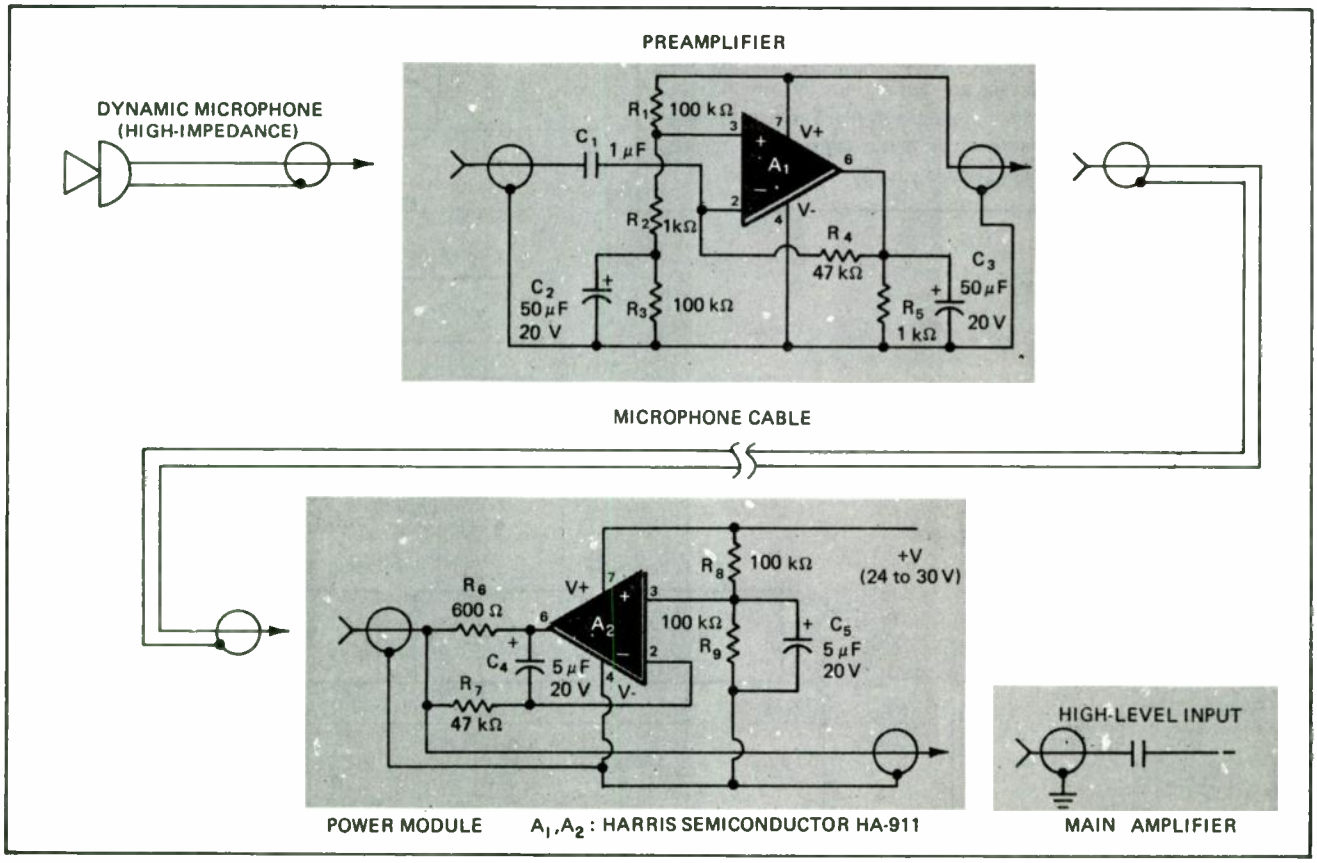
by Don Jones
Harris Semiconductor, Melbourne, Fla.

When a high-impedance microphone is at the end of more than 20 or 30 feet of cable, a preamplifier powered by batteries is often placed at the microphone to prevent high-frequency loss and to enhance the signal-to-noise ratio. But a preamp can be made much more compact if instead of using batteries it is powered remotely over the shielded or twisted-pair audio cable.

The hookup shown here is an unconventional application of an operational amplifier, but the performance will please any broadcaster or audio enthusiast. Performance is definitely high fidelity. Frequency response is better than ±1 decibel from 20 hertz to 20 kilohertz, and equivalent input noise is about 3 microvolts rms over this band.

The diagram shows the circuit arrangement. In the quiescent state, the output terminal (pin 6) of operational amplifier A_1 is biased by R_1, R_2, and R_3 to about half the power supply voltage, with negative feedback through R_4. However, the audio-output signal is not taken from pin 6; instead, the audio output comes from pin 7, the V+ terminal of the op amp. This output signal is inverted with respect to the normal amplifier output, so even though the audio-input signal from the microphone is fed into the inverting op-amp input terminal, the amplifier is actually noninverting. The gain (about 100) is determined by the ratio of R_1 and R_2, which form the feedback network from the V+ (audio-output) pin. The HA-911 op amp is used because its noise level (8 nV/Hz$^{1/2}$, 0.35 pA/Hz$^{1/2}$) and gain-bandwidth product (8 MHz) are many times better than those of general-purpose op amps.

In the power module, op amp A_2 supplies about 12 V dc at 7 milliamperes through a 600-ohm termination to the cable; the dc power for the module can probably be obtained from the main amplifier. Instead of using the power module, the power for the preamp could be supplied to the cable through a passive choke in series with a dc supply, but 150 henrys would be required to obtain the same noise isolation from the dc line. □



Two-way cable. Microphone cable carries power up to preamplifier and carries amplified signal down to main amplifier. Preamp, mounted at high-impedance microphone before long cable to preserve fidelity and suppress noise, is light and compact because its power is supplied through the cable, eliminating batteries. Although op amps are used in unconventional arrangements, performance is excellent.

FETs remove transients from audio squelch circuit

by Glen Coers
Texas Instruments Components Group, Dallas, Texas

Using field-effect transistors instead of bipolar transistors for an audio squelch circuit eliminates switching transients without sacrificing switching time. Moreover, because there are no transients, the circuit's frequency response can be as low as desired.

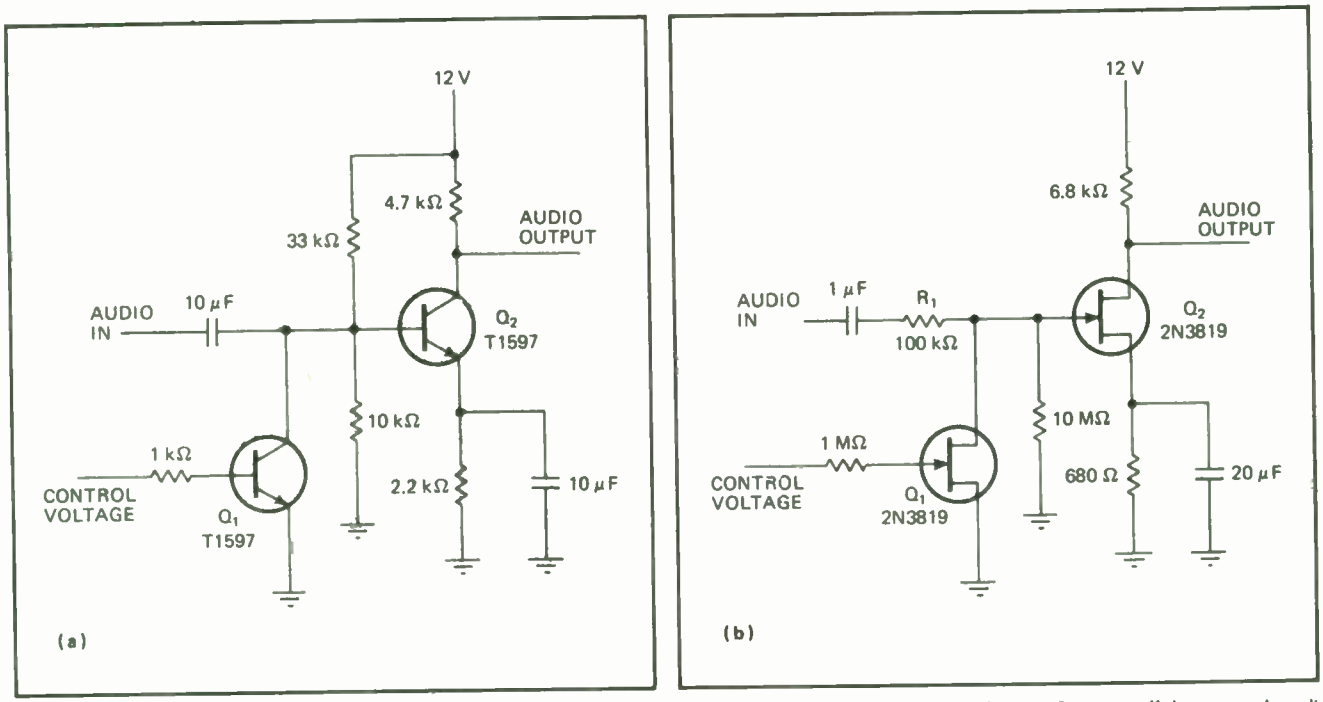
In a typical audio squelch circuit (a), bipolar transistor Q_1 acts as the control device for bipolar transistor Q_2, which serves as the amplifier. When Q_1 turns off Q_2, the base voltage of Q_2 switches from a dc level (in this case, 2.8 volts) to ground, causing a large transient output voltage spike to be generated.

The problem can be minimized by slowing the switching speed of Q_1 or raising the low end of the amplifier's frequency response. However, this method is not practical in applications requiring a broad frequency response, such as high-fidelity audio equipment.

Building the circuit with FETs (b) provides a better solution. Again, transistor Q_1 is the control, while transistor Q_2 is the amplifier. Only ac voltage is present at the gate of Q_2; its dc level is at ground potential so that there is no transient generated when Q_2 is switched off.

When Q_1's gate is at zero volts, the device itself conducts, bypassing the audio signal to ground. Transistor Q_1 and resistor R_1 form a voltage divider that attenuates the signal by about 60 decibels. The "on" resistance of the FET is approximately 100 ohms.

To pass the audio input, a negative voltage must be applied to Q_1's gate to turn the device off. The audio signal at the gate of Q_2 can then reach the output devoid of any switching transients. □



FETs replace bipolars. In bipolar-transistor audio squelch circuit (a), large output transient is generated when Q_2 turns off, because dc voltage at Q_2's base is grounded. Substituting FET circuit (b) eliminates transients without limiting switching speed. Control FET Q_1 turns off for negative gate voltage, allowing amplifier Q_2 to pass audio signal to output. Only ac voltage is present at Q_2's gate.

5. Automatic gain control

Agc rf threshold detector provides fast slewing

by Roland J. Turner
American Electronics Communications Corp., Lansdale, Pa.

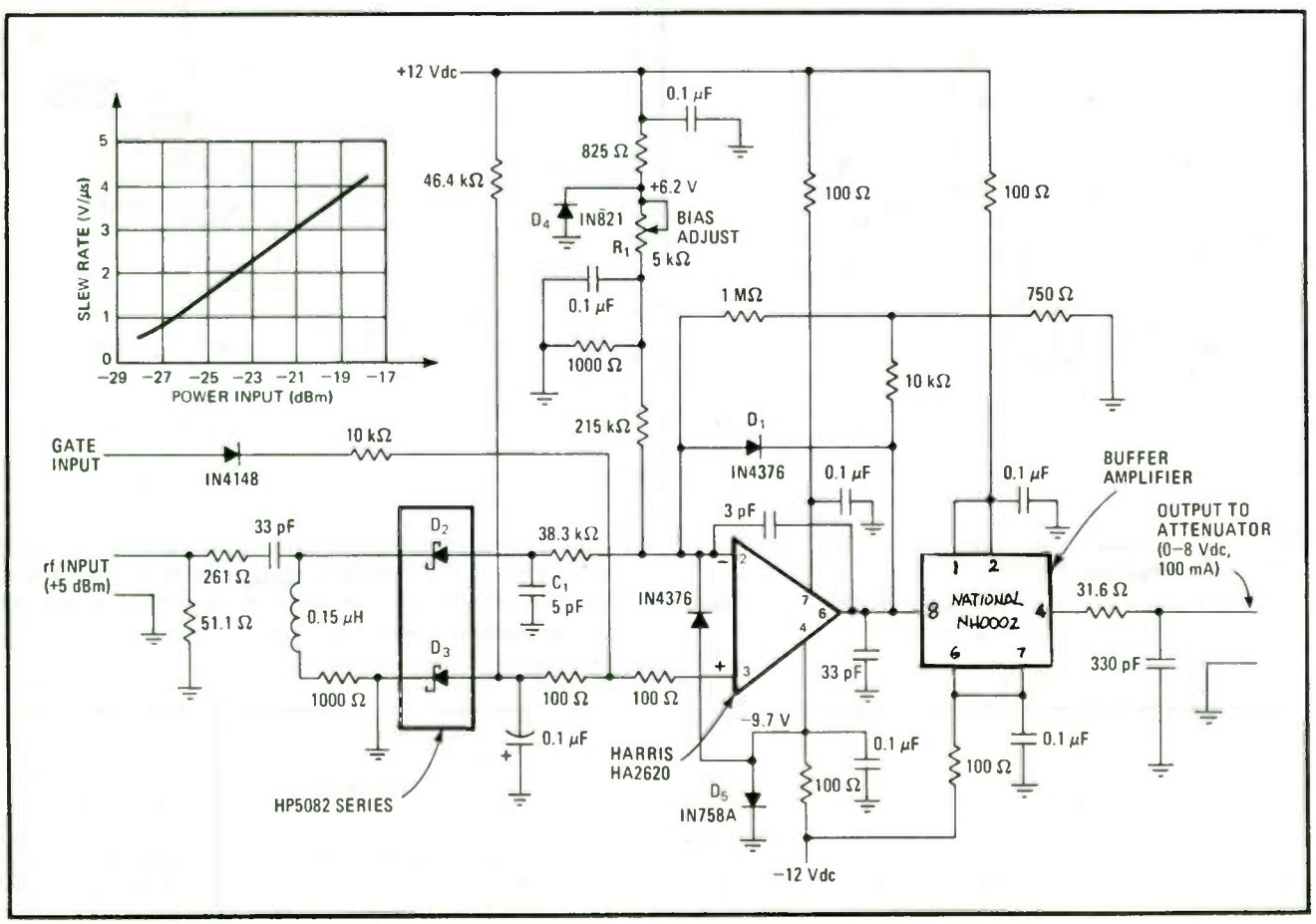
In both radar and communication systems, an automatic-gain-control loop is commonly employed to keep signal level constant for enhanced signal detection. As systems become more adaptive, the agc loop must be more sophisticated, frequently forcing simple circuits to perform multiple functions.

Meeting this demand is an rf threshold detector for the agc loop in an rf receiver. The detector can process signals of 1 megahertz to 1 gigahertz with a slew rate of several volts a microsecond. It also permits delayed agc operation and can perform over a wide range of temperature and supply-voltage variations.

Furthermore, below the detection threshold, the signal can be processed linearly in the rf section of the receiver. Above the detection threshold, the output of the rf section is rapidly leveled so that such detrimental effects as limiting and hangup cannot occur in subsequent i-f stages. This fast action prevents the receiver from being desensitized at high signal levels and permits low-level targets to be detected even in the proximity of heavy clutter.

With the threshold power level (typically 0 to 5 dBm) applied at the detector's rf input, the input voltages of the operational amplifier are equalized so that there is no output voltage. For signal levels below the threshold, the op amp's inverting input swings positive, relative to the noninverting input, and the op-amp output is

Closing the loop. Threshold detector for agc loop in rf receiver can handle broadband signals with frequencies of 1 megahertz to 1 gigahertz at slew rates as fast as 1 volt/microsecond. Dual Schottky diodes and high-slew-rate op amp account for circuit's speed. Temperature compensation, from 0°C to 60°C, is provided by diodes D_2 and D_3, while diodes D_4 and D_5 compensate for supply variations of ±6%.



clamped by diode D_1 near the quiescent bias voltage set by potentiometer R_1. This clamp prevents the output of the op amp from swinging to the negative supply voltage and enhances the recovery time of the detector at its threshold level.

As soon as the rf input develops 3 millivolts of rectified bias voltage across capacitor C_1, the detector's output goes positive to 1 V, thereby activating the agc loop in which it is installed. Only the differential offset voltage between the dual Schottky diodes, D_2 and D_3, is impressed across the op amp's differential input. The op amp provides 50 decibels of gain, while Schottky diode D_3 provides automatic temperature stabilization for the detector. Diodes D_4 and D_5 are temperature-stabilized reference diodes that desensitize the detector to power supply variations.

The rf section of the receiver is gated by switching the voltage at the detector's gate input from its normal −10-V bias level to 10 V. This overrides any signal condition, forcing the detector's output to go to 8 Vdc and forcing the associated attenuator in the agc loop to its maximum attentuation state.

For power levels above the detection threshold, the detector produces 4.2 V at its output per decibel of input power over the operating temperature range of 0°C to 60°C. Less than 0.5 dB of loop dynamic range is consumed by the static offset voltage of the transfer function over the same temperature range.

Moreover, the transfer function remains constant and unaffected by ±6% variations in the supply voltages. Less than 0.3 dB of loop dynamic range is consumed by static offsets in the transfer function for the same supply variations. For signals greater than 2 dB above threshold, the detector slew rate exceeds 1 V/μs. □

Touch Tone receiver front end provides agc and filtering

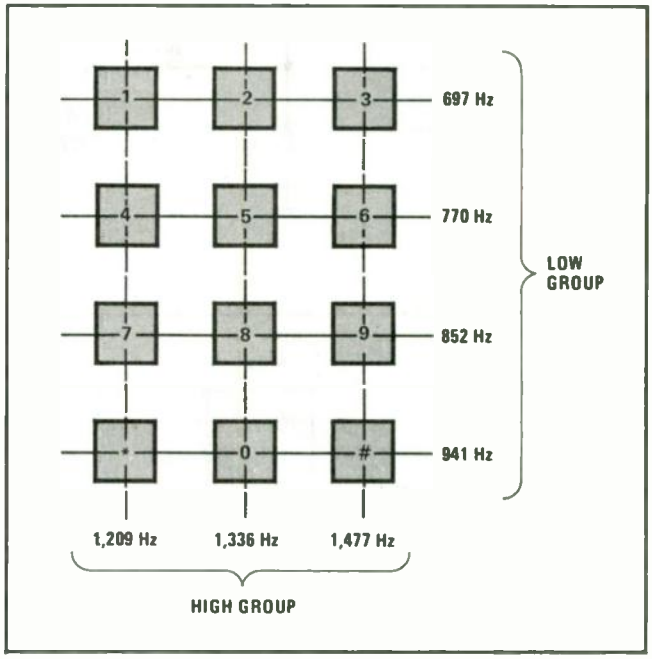
by Jack D. Dennon
Computerphone System, Renton, Wash.

Signals from Touch Tone phone buttons can initiate remotely controlled operations such as turning on a front-door light or entering a sales order in a computer. Such control functions utilize the two-frequency signal that is generated on the phone line when one of the Touch Tone buttons is pushed. As indicated in Fig. 1, one frequency is from the low group (LG), and the other is from the high group (HG). A receiver that measures the two frequencies can respond to a specific button.

Touch Tone receiver circuits can be built inexpensively with either phase-locked-loop tone decoders such as the Signetics 567, or decoders based on active filters using operational amplifiers. For optimum performance from either type of decoder, the receiver should have a front end that consists of an amplifier to provide automatic gain control and high-pass and low-pass filters to separate HG frequencies from LG frequencies.

The simple Touch Tone receiver front end shown in Fig. 2 performs these functions, using only a Norton-type LM3900 quad op-amp and a single complementary-MOS 74C04 hex inverter. The circuit, which uses inexpensive components that are widely available, operates from a single supply voltage of 4 to 15 volts.

The incoming two-tone signal can be taken directly from a line-isolation transformer. It divides across a potentiometer that is set to provide the indicated voltage levels and then is amplified in the automatic-gain-control amplifier and the C-MOS fixed-gain amplifier. Analog operation of the C-MOS digital IC is obtained by biasing the inverting amplifiers to the center of their



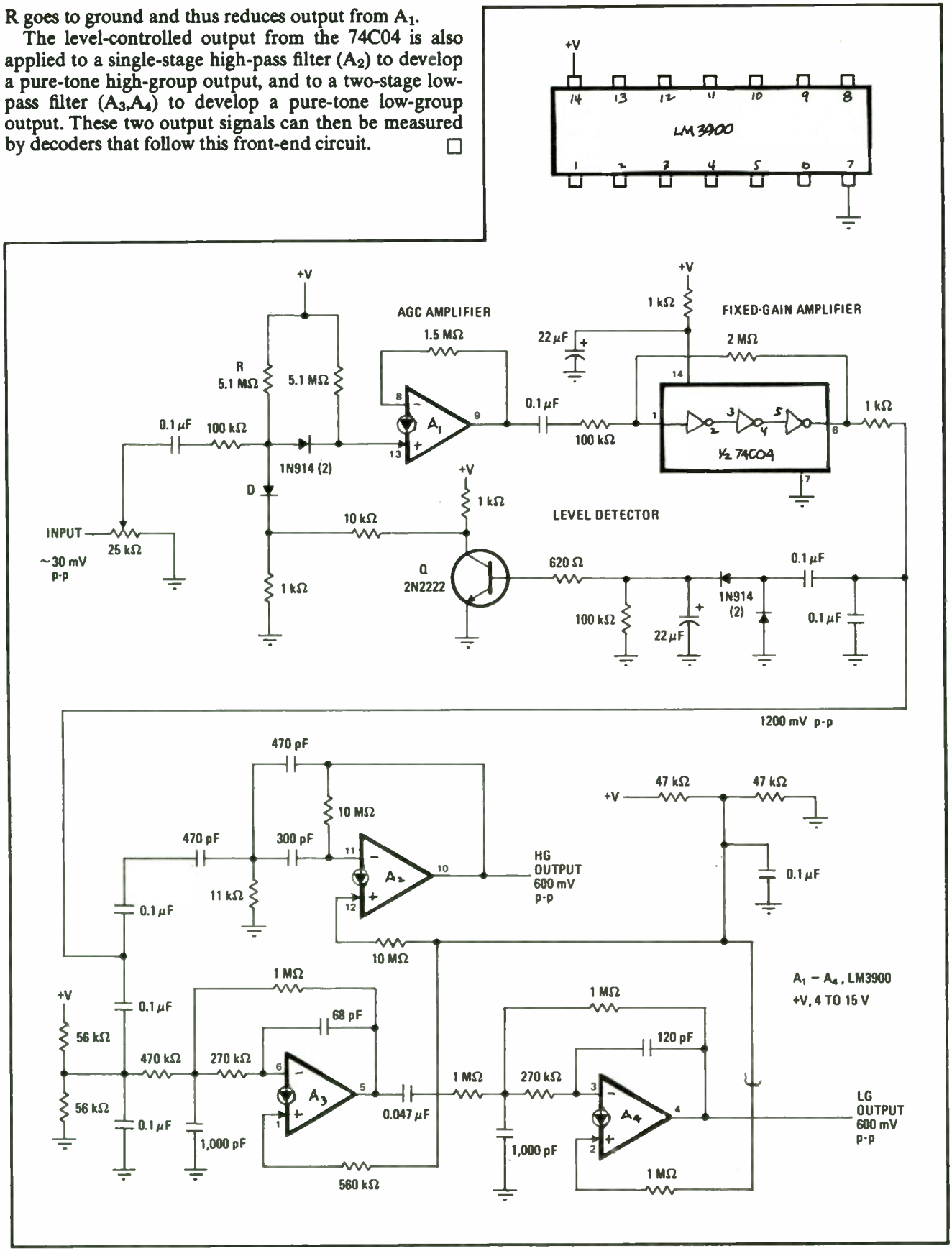
1. Coding. Each button on a Touch Tone phone is identified by the pair of frequencies that is generated when the button is pushed. Four low-group frequencies correspond to the four rows of buttons, and three high-group frequencies correspond to the three columns. To determine which button was touched, the two frequencies are separated in the receiver front end described here and measured in the decoders that follow the front end.

linear range; the gain is fixed at 2 MΩ/100 kΩ, or 20.

The agc signal that is taken from the output of the 74C04 fixed-gain amplifier is rectified and smoothed to drive transistor Q. The transistor controls the output from the agc amplifier by controlling the bias on diode D. A weak signal into Q back-biases D so that current flowing from the supply through the resistor R is forced into A_1 and produces a large output; a strong signal into Q leaves D forward-biased, so that the current through

R goes to ground and thus reduces output from A_1.

The level-controlled output from the 74C04 is also applied to a single-stage high-pass filter (A_2) to develop a pure-tone high-group output, and to a two-stage low-pass filter (A_3,A_4) to develop a pure-tone low-group output. These two output signals can then be measured by decoders that follow this front-end circuit. □



2. Front-end circuit. The two-frequency signal coming in from a Touch Tone phone is boosted or attenuated to a convenient level in agc amplifier, and then is separated into a low-group output and a high-group output by low-pass and high-pass filters. Only two inexpensive and widely available ICs are required to implement these functions. Many operations can be controlled remotely by the Touch Tone push buttons.

Varistor voltage divider improves receiver agc

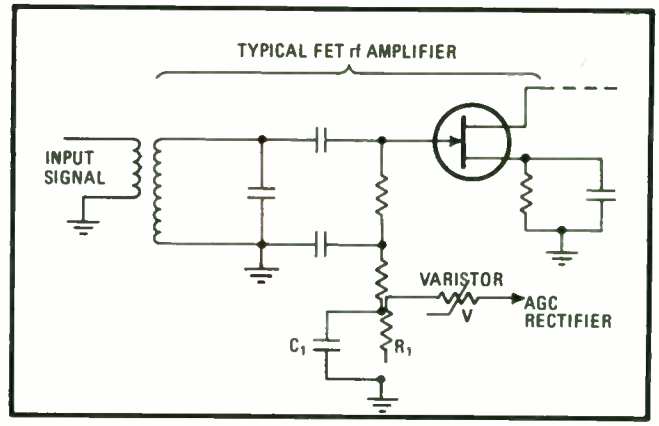
by M.J. Salvati
Sony Corp. of America, Long Island City, N.Y.

Adding a varistor to the automatic gain-control circuitry in a communications receiver is a simple way to improve output-signal leveling. The varistor and a fixed resistor make up a variable voltage divider that is placed between the rf amplifier and the agc rectifier.

This arrangement improves the effectiveness of the agc circuitry because the percentage of the agc voltage applied to the controlled rf-amplifier stage varies in the same direction as the input-signal level. Furthermore, at low signal levels, this percentage is very small, allowing the amplifier to operate at maximum gain for the best noise-figure performance. The varistor agc, therefore, provides the benefits of delayed agc (or manually switching off the agc) without the abrupt discontinuity in control characteristic of the latter technique.

When the agc voltage is at its highest level (for a strong signal), the varistor's resistance is low, causing most of the agc voltage to appear across resistor R_1. This provides maximum gain reduction. When the agc voltage is at its lowest level (for a weak signal), the varistor's resistance is high and only a small agc voltage appears across the resistor, producing very little gain reduction.

The resistance values of the varistor and the resistor are selected so that the varistor is about half the value of the resistor when the agc voltage is at its maximum level (for the largest expected input signal). This selection will provide the best receiver output-signal leveling for inputs ranging from 1 to 1,000 millivolts and the best receiver noise figure (because of nearly complete agc turnoff) for inputs below 10 microvolts.



Varistor agc. Variable voltage divider formed by a varistor and a fixed resistor gives the advantages of delayed automatic gain control without any abrupt discontinuities. The varistor resistance becomes low for strong signals and high for weak signals, thereby varying the agc voltage applied to the controlled rf-amplifier stage. The scheme enhances receiver sensitivity and improves output-signal leveling.

The resistance values actually chosen for the varistor and resistor will depend on the signal levels available at the agc rectifier. In general, resistor R_1 will be about 2 megohms for vacuum-tube receivers and about 100 kilohms for semiconductor receivers. Since the time constant of the agc filter formed by the varistor, the resistor, and capacitor C_1 changes with signal level, the value of the capacitor should be chosen for adequate filtering of modulation variations when the varistor resistance is half the value of the resistor.

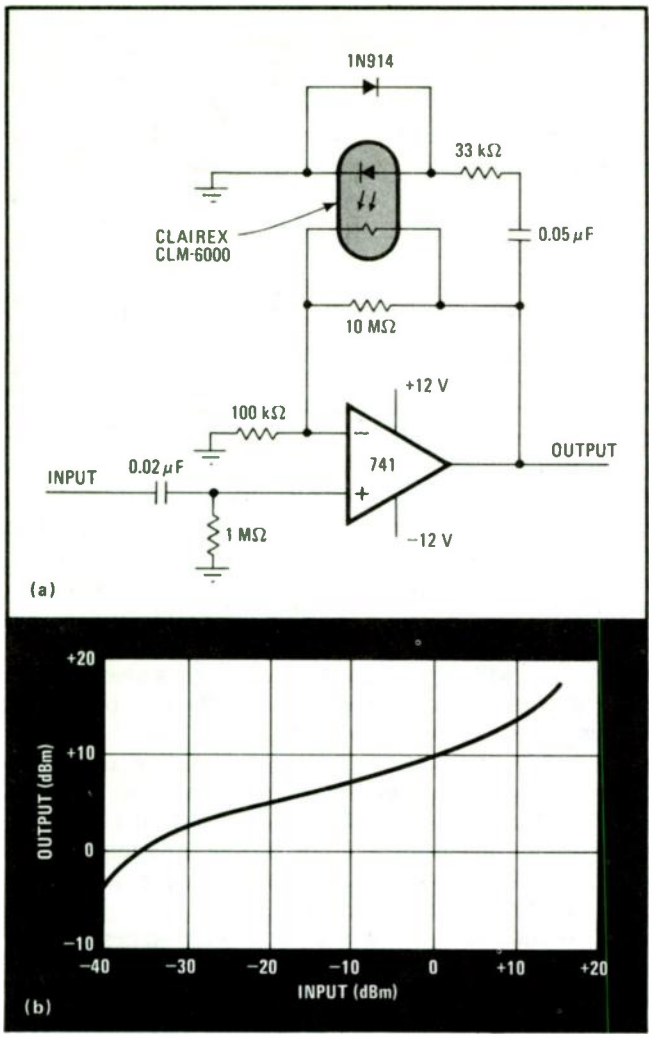
When included in all the controlled stages (along with the rf amplifier stage) of a semiconductor receiver, varistor agc can improve receiver sensitivity by 3 decibels, halve the decibel change in receiver output for a given change in input level, and increase the receiver's absolute output level by 8 to 12 dB. □

Photocoupler provides agc for audio communications

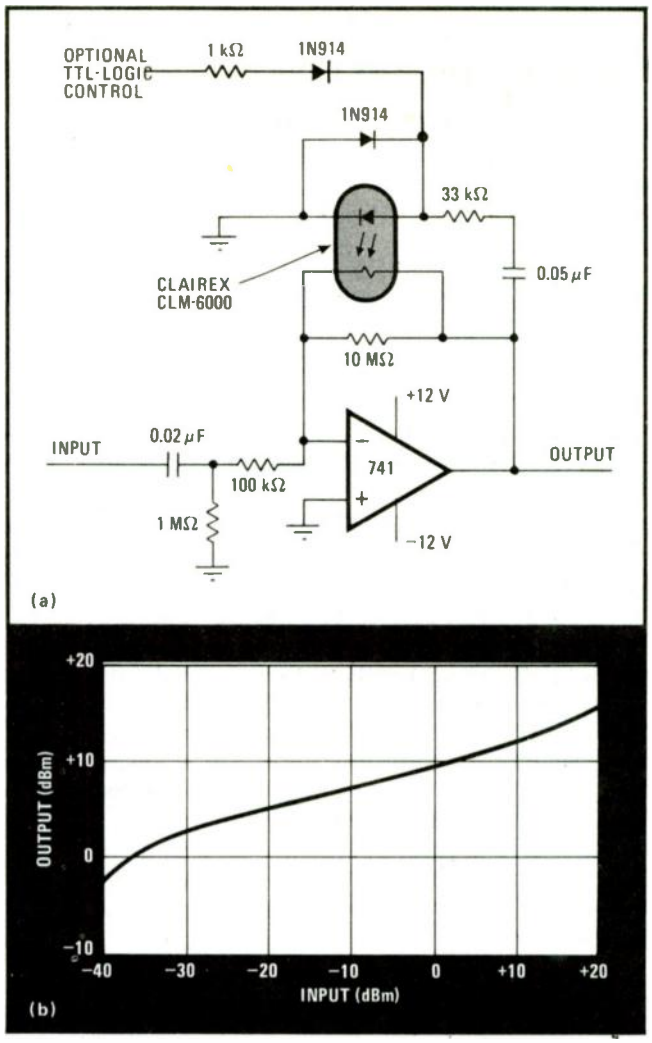
by Richard K. Dickey
California Polytechnic State University, San Luis Obispo, Calif.

In all communications systems that have speech input, some form of automatic gain control is desirable to maintain the optimum signal level despite wide variations in the amplitude of the input level. To eliminate fluctuations caused by varying transmission efficiency, agc is also desirable at the receiving terminal.

A good agc system should introduce no amplitude or frequency distortion and should have a fast attack and a



1. Agc amplifier. Photoresistor in optical coupler provides feedback path for operational amplifier circuit in (a); output signal drives LED to reduce photoresistance and thus reduce gain. Transfer characteristics are shown in (b); 0 dBm is taken as 0.775 volt rms. The lower limitation on agc is shown by the curved portion of the characteristic at low input levels. Gain approaches unity at high input levels.



2. Wider range. Inverting connection of op amp (a) provides greater agc; transfer characteristics (b) show that 50-dB variation of input signal produces only 12.6-dB variation at output. The input impedance is less than for noninverting connection used in Fig. 1, and a constant low driving impedance is required. Optional portion of circuit shown in color allows a TTL signal to turn off output.

moderately slow decay. The circuit of Fig. 1(a), which has all these features, can reduce an input variation in excess of 50 decibels to an output variation of only 16 dB. This circuit uses a 741 operational amplifier connected in the noninverting mode. The gain of this configuration is $1 + R_F/10^5$, where R_F is the feedback resistance (in ohms). The feedback resistor is the photoresistor of a CLM-6000 optical coupler.

Unlike the more common phototransistor couplers, the CLM-6000 has a photoconductive cell; op-amp output voltage in excess of the forward drop of the coupler's light-emitting diode (about 1.4 V) decreases the photocell resistance. Therefore the 741 operates as a linear amplifier with a gain that is controlled by its own output. The characteristics of the photoresistor include a quick drop in resistance when illuminated and a slow recovery of resistance after darkness begins. The compression characteristics of the agc amplifier are shown in Fig. 1(b).

The 1N914 diode that shunts the LED completes the circuit for the negative phase of the ac signals, so that the 0.05-μF capacitor can discharge. The 10-megohm shunt across the photoresistor is necessary to prevent loss of dc feedback and consequent output saturation in the absence of signal. If output saturation were allowed to occur, the system would lock up, and no ac signal could appear at the output.

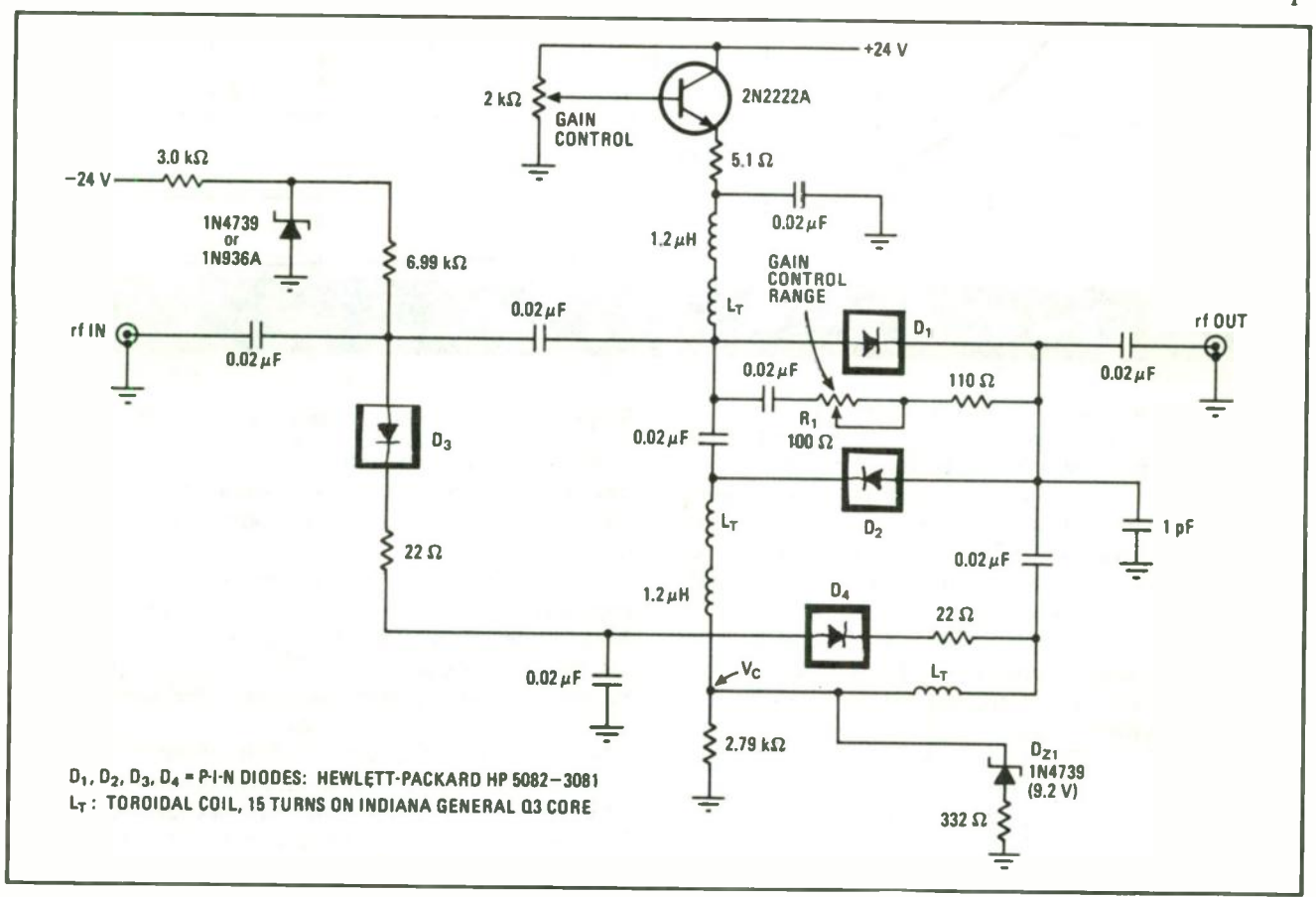
For a wider dynamic range, the inverting-mode operational amplifier circuit of Fig. 2(a) can be used; the input impedance is finite (100 kilohms), and a constant low driving impedance is required. For large input signals, the gain of this circuit goes below 1, so the circuit becomes an attenuator.

An additional feature of this configuration is that the output may be effectively switched off by a transistor-transistor-logic signal applied to the LED as shown. When the TTL signal is high, the LED emits so much light that the photoresistor conducts strongly and forces the gain to zero. When the TTL signal is low (less than 0.8 V), the circuit operates normally. □

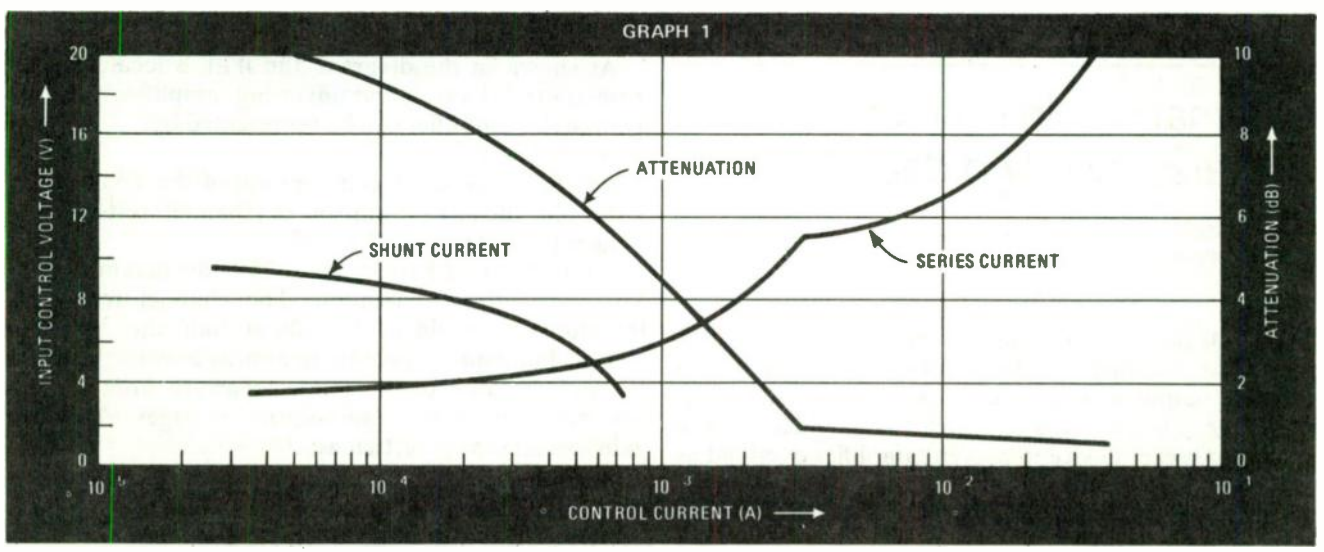
Broadband p-i-n attenuator has wide input dynamic range

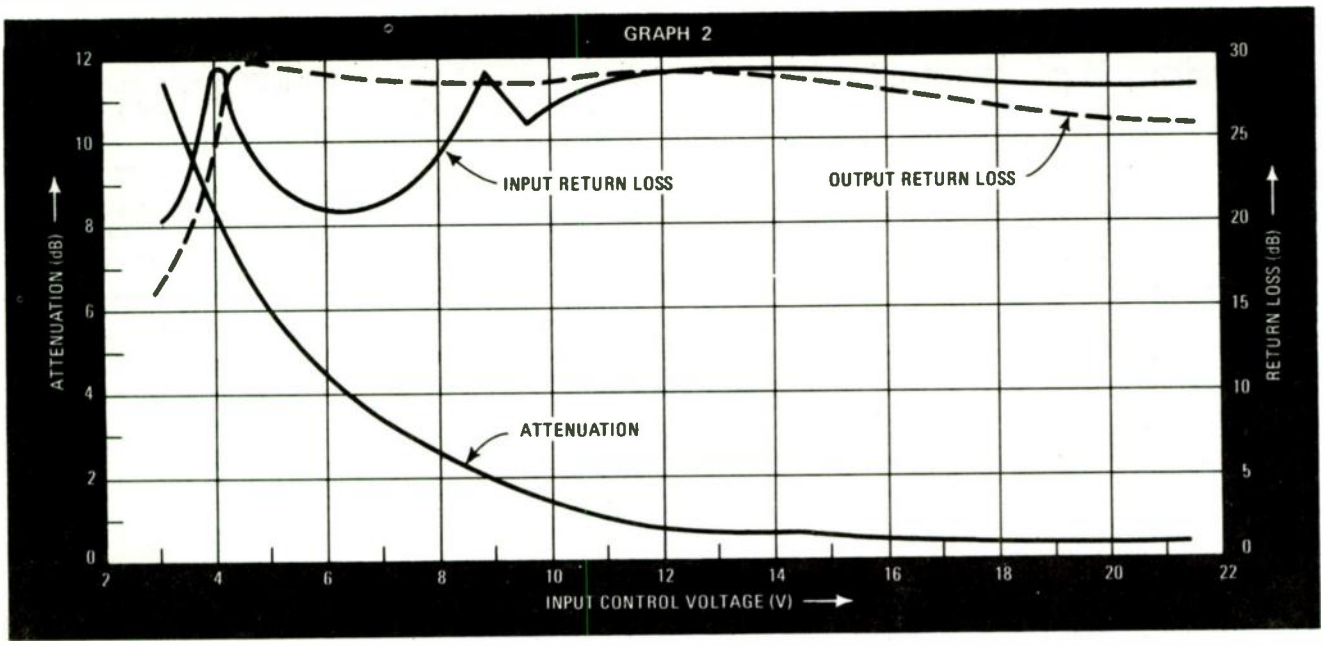
by Roland J. Turner
American Electronic Labs, Colmar, Pa.

A low-loss broadband attenuator that is built with p-i-n diodes offers an exceptionally flat response over a wide input dynamic range. The circuit, which employs the p-i-n diodes in a π configuration, is useful for automatic-gain-control applications over the frequency range of 50 to 300 megahertz. Its response remains flat to within ±0.10 decibel over the full 11-dB input control range. Insertion loss is less than 0.50 dB, and the input/output return loss exceeds 20 dB over the entire op-



High performer. This rf attenuator provides exceptional response flatness over a wide input dynamic range from 50 to 300 megahertz. High-quality p-i-n diodes connected in a π configuration minimize the circuit's intermodulation distortion. Diodes D_1 and D_2 form the series arm of the π network, while diodes D_3 and D_4 form the shunt arm. Graphs 1 and 2 show the attenuator's primary characteristics.





erating frequency range and gain-control range.

A π configuration, as opposed to a bridged-T network, is used here because of its superior performance. The π attenuator requires less current-drive shaping, and it reduces the effect of parasitic inductances on input/output return losses, since stabilizing resistors can be used in its shunt arm. The bridged-T attenuator, on the other hand, requires low resistance values in its shunt arm so that stabilizing resistors cannot be used. Therefore, the input return loss and response flatness of the bridged-T attenuator are seriously affected by reactive current at high attenuation levels.

The high-performance π attenuator shown in the figure uses p-i-n diodes that exhibit very low intermodulation distortion across the circuit's full operating band. P-i-n diodes D_1 and D_2 form the series arm of the π-configuration attenuator—they are connected in parallel for signal transfer and in series for the control bias.

When low attenuator loss is desired (for control voltages of more than 10 V), zener diode D_{Z1} conducts and forces the series control bias current to exceed 35 milliamperes. For an attenuation level of greater than 1.5 dB, D_{Z1} is nonconducting, and the series control current in diodes D_1 and D_2 is less than 5 mA. Series resistor R_1 is used to set the gain control range between 8 and 13 dB.

The attenuator's control circuit is quite simple. The control bias voltage, V_C, which governs the turn-on of shunt diodes D_3 and D_4, is determined by the amount of series control current that flows. Consequently, when the series control current decreases, the shunt control current automatically increases.

Graph 1 shows the series and shunt control currents, as well as the attenuation level, produced at various input control voltages. The gain-control characteristic and the input/output return loss generated by this current profile are plotted in Graph 2.

The operating frequency range of the attenuator is limited by the p-i-n diodes used. With the ones called for here, the attenuator should provide similar performance characteristics down to 5 MHz. □

Automatic gain control operates over two decades

by Carl Marco
Martin Marietta Corp., Orlando, Fla.

A voltage-controlled junction-field-effect transistor permits an automatic-gain-control circuit to maintain a constant output voltage over a two-decade input-voltage range. The resulting agc circuit is intended for use in a radar seeker device to prevent amplifier overload as the target gets closer. Inputs can range from 40 millivolts to 4.1 volts peak-to-peak, but the output remains a nominal 0.2 V pk-pk.

As shown in the diagram, the JFET is located in the gain-control loop of noninverting amplifier A_1. The gain of this amplifier can be represented by:

$$A_V = 1 + R_F/R_I$$

where R_I is the series combination of the 1-kilohm resistor plus the FET's drain-source (channel) resistance:

$$r_{ds} \approx r_{ds(on)}/(1 - V_{GS}/V_{GS(off)})$$

For the FET used here, $r_{ds(on)}$ is 25 ohms maximum and $V_{GS(off)}$ is −10 V maximum. The channel resistance, therefore, stays linear for about half the range of $V_{GS(off)}$, but tends to become nonlinear at voltages above $\frac{1}{2}V_{GS(off)}$ because of the FET's departure from square-law behavior at high gate-source voltages. Amplifier gain can then be rewritten as:

$$A_V = 1 + (110\ k\Omega)/[(1\ k\Omega) + (0.025\ k\Omega)/(1 - |V_{GS}|/10)]$$

$$A_V = 1 + 110/[1 + 0.025/(1 - |V_{GS}|/10)]$$

The voltage divider formed by resistors R_1 and R_2 attenuates (by around 20:1) input signal amplitude to prevent distortion at the output. Since the inverting input of amplifier A_1 tries to track its noninverting input, the positive input is the one that determines the FET's drain-source voltage. This channel voltage must be kept small to force the FET to remain in its triode region of operation. A shift in the FET's operating region would introduce large amounts of distortion.

Amplifier A_2 is connected as a half-wave rectifier. When A_1's output swings positive, diode D_1 conducts, shunting A_2's feedback resistor (R_3) and bringing the junction of this resistor and diode D_2 to zero. When A_1's output goes negative, diode D_2 conducts so that amplifier A_2 has a gain of −1 and a positive output.

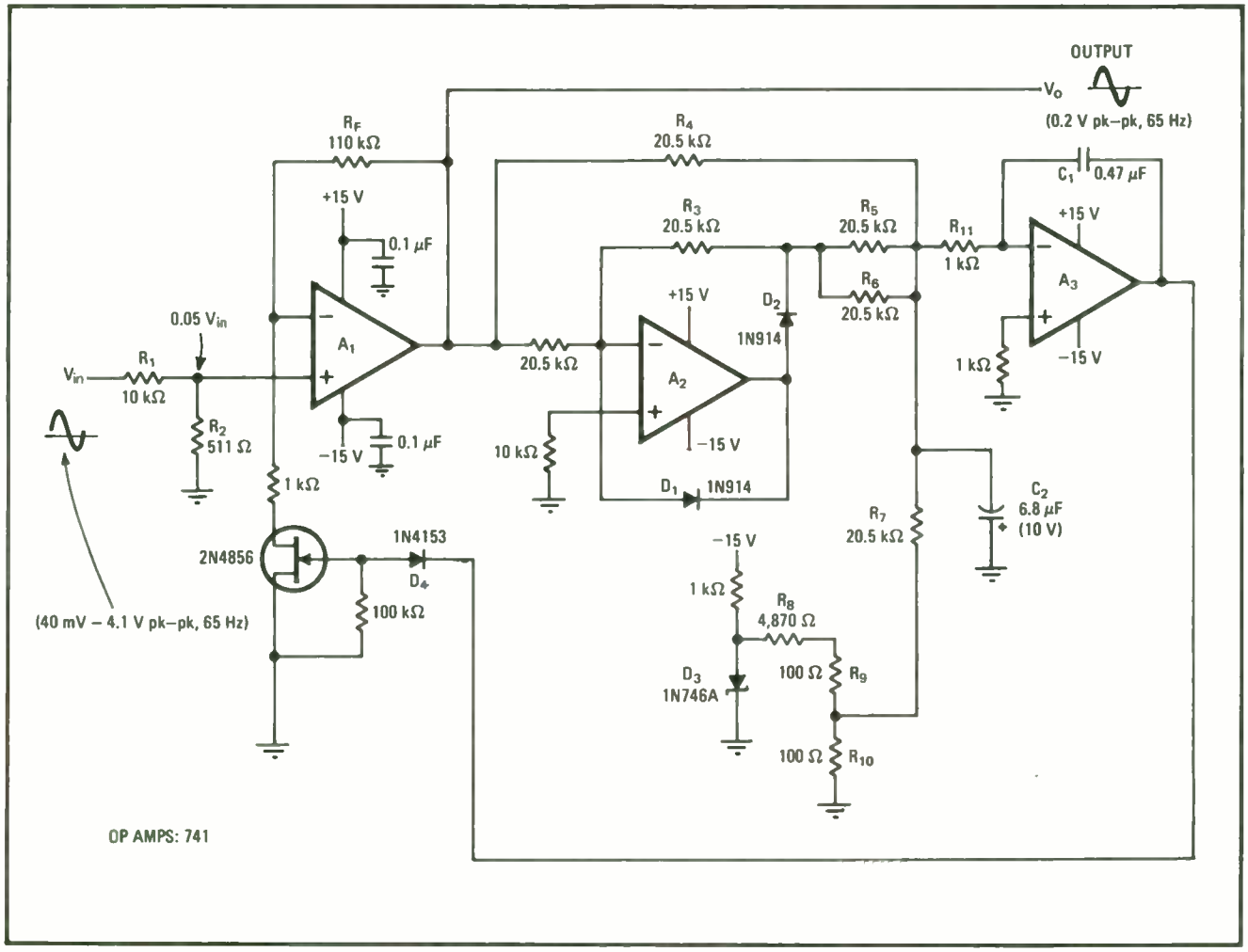
Resistors R_4, R_5, and R_6 provide full-wave rectification for A_1's output signal. Since the resulting rectified signal is supplied from a high-impedance source (and not buffered as is usually done), it is a current drive signal that can feed amplifier A_3 directly. When the circuit is balanced, the current through resistor R_7 is equal in magnitude but opposite in polarity to the full-wave rectified current.

The voltage divider, composed of zener diode D_3 and precision resistors R_8, R_9, and R_{10}, determines the signal level applied to amplifier A_3. This amplifier performs as a comparator/integrator, supplying the very large dc gain needed for the circuit's closed-loop feedback. Capacitor C_1 prevents A_1's output from oscillating, while resistor R_{11} allows filter capacitor C_2 to be added without creating a "virtual" ground at A_3's input.

Capacitor C_2 prevents ac ripple from modulating the FET's gate voltage and producing distortion. Its value is chosen by trading off circuit-response time against the amount of filtering. Only a small change in A_3's input current causes the circuit to adjust itself, producing whatever agc voltage is required to maintain an output of 0.2 V peak-to-peak.

When input-signal amplitude increases, the drive current to amplifier A_3 also increases, causing A_3's output to go more negative. This raises the FET's channel resistance and decreases A_1's gain, thereby maintaining the output level at 0.2 V pk-pk. An input voltage of 4.1 V pk-pk or higher cuts off the FET, making the voltage gain of A_1 equal to unity. Amplifier A_1 then tracks the input, attenuating it by a factor of 20. At an input level

FET in the driver's seat. Automatic-gain-control circuit employs voltage-controlled JFET as the variable control element. The FET's channel resistance determines gain of amplifier A_1, in response to error voltage produced by comparator A_3. Amplifier A_2 and the surrounding diode/resistor network perform as full-wave rectifier. The output is maintained at 0.2 volt for inputs from 40 millivolts to 4.1 V.



of 4.1 V, output distortion is only 1.1%.

For an input below 40 millivolts, the drive current to A_3 becomes negative so that A_3 provides a positive output, back-biasing diode D_4 and bringing the FET's gate-source voltage to zero. The gain of amplifier A_1 is then at its maximum value (1 + 110/1.025 = 107), permitting the circuit to track the low-level input and producing an output of 5.35 V_{in}.

The circuit's output-voltage level can be increased to 0.4 V pk-pk, for an input voltage range of 80 mV to 8.2 V pk-pk, by changing the voltage division at the comparator input—resistor R_7 is connected between resistors R_8 and R_9, rather than between resistors R_9 and R_{10}. However, this change increases output distortion to 4.4% at the 8.2-V input level. □

Automatic gain control quells amplifier thump

by Paul Brokaw
Analog Devices Inc., Semiconductor Division, Wilmington, Mass.

If an audio amplifier with automatic gain control makes a thumping noise when the input signal level changes quickly, the cause may be unwanted feedthrough of the gain control signal to the amplifier output. A simple solution is the addition of a resistor to prevent variations in the control voltage from being fed through to the output.

In the "thumpless" agc circuit of (a), transistors Q_1 and Q_2 form a differential amplifier that has a gain determined by the emitter current of the pair, I_E. This emitter current varies the transconductance and therefore the gain of transistors Q_1 and Q_2. But if gain changes too quickly, a thump may be heard. Inserting resistor R_1 in the emitter-current control circuit eliminates the thump.

Emitter current I_E is made nearly equal to the current (I_2) flowing through resistor R_2 by using identical same-substrate transistors for Q_3 and Q_4. When the base-emitter voltages of these two devices are equal, their collector currents (I_E and I_2) are also equal.

Since the base and collector of transistor Q_4 are shorted together, this device's base-emitter voltage will rise until its collector current becomes equal to $(1 - 2/\beta)I_2$, where β is the common-emitter current transfer ratio. Since transistor Q_3 is identical to transistor Q_4, Q_3's collector current will also rise to the same value. If current transfer ratio β is large and the reverse voltage feedback ratio of the transistor is small, Q_3's collector current (I_E) will nearly equal resistor current I_2. The value of current I_2 is:

$$I_2 = (E_{control} - V_{B4})/R_2$$

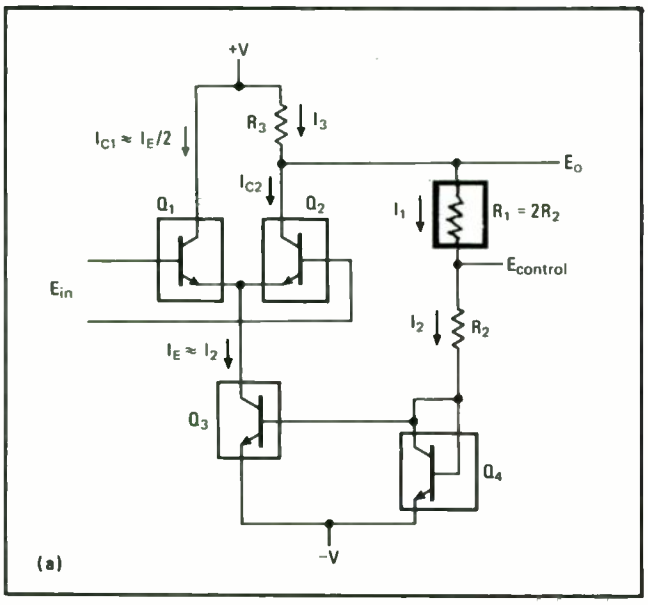
where V_{B4} is the voltage at the base of transistor Q_4.

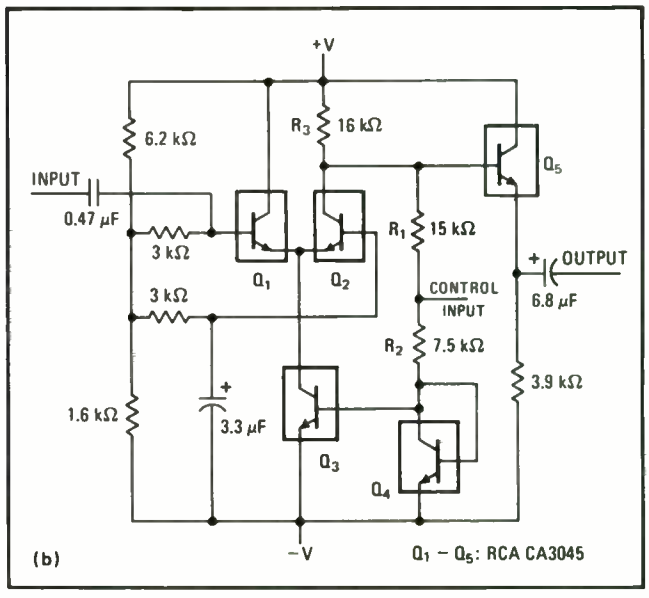
Because the collector currents of transistors Q_3 and Q_4 are approximately equal, the transconductance of the differential pair (transistors Q_1 and Q_2) will vary in direct proportion to the control voltage. If Q_1 and Q_2 are identical, emitter current I_E will divide equally between them. Each transistor will have a collector current of $\alpha I_E/2$, where α is the common-base current gain.

If α is approximately equal to 1 and I_E is approximately equal to I_2, the collector currents of transistors Q_1 and Q_2 become:

$$I_{C1} = I_{C2} \approx I_2/2$$
$$I_{C1} = I_{C2} \approx (E_{control} - V_{B4})/2R_2$$

where I_{C1} is the collector current of transistor Q_1 and I_{C2} the collector current of transistor Q_2. The current (I_3) through resistor R_3 is due to both resistor current I_1 and





Improved agc. Automatic-gain-control circuit (a) for audio amplifier applications eliminates unwanted thumping that may be heard when the input-signal level changes abruptly. Resistor R_1 prevents sudden variations in the control voltage from reaching the output as an audible thumping. An audio amplifier using this agc scheme is shown in (b); amplifier gain is 30 for a control voltage of 15 volts.

collector current I_{C2}. Current I_1, which flows through resistor R_1, is given by:

$$I_1 = (E_o - E_{control})/R_1$$

Resistor current I_3 is the sum of collector current I_{C2} and resistor current I_1:

$$I_3 = I_{C2} + I_1$$

$$I_3 = \frac{E_o}{R_1} - \frac{V_{B4}}{2R_2} + \left(\frac{1}{2R_2} - \frac{1}{R_1}\right)E_{control}$$

If $R_1 = 2R_2$, the last term in this equation drops out, making current I_3 independent of the control voltage, except for a small contribution caused by the dependence of V_{B4} on $E_{control}$. Since the output voltage is proportional to resistor current I_3, and not to the control voltage, variations in the control voltage will not be fed through to the output.

To implement a complete audio amplifier (b) with agc requires only a single monolithic array of five matched transistors. Two transistor pairs are used as indicated in (a), while the fifth remaining transistor is used as an output signal buffer.

The base current error introduced by transistor Q_4 can be reduced by making resistor R_2 slightly less than what the half-value approximation calls for. If resistors R_1 and R_2 are made variable, the performance of the circuit can be optimized by adjusting them for minimum feedthrough. For the component values indicated, the amplifier's voltage gain is about 30 when the control voltage is 15 volts. Circuit gain is directly proportional to the control voltage minus V_{B4}. (Voltage V_{B4} can be approximated as 0.55 v.)

Naturally, amplifier performance is limited by component tolerances. With components having 5% tolerances, the feedthrough signal can typically be suppressed by 20 to 30 decibels. Tighter tolerances will, of course, improve feedthrough suppression, but at some point, the various approximations made (like neglecting the transistor base current error) will limit performance. For a large control voltage, amplifier gain becomes inversely proportional to absolute temperature. At room temperature, this variation in amplifier gain amounts to about 0.03 dB/°C, which is not objectionable for most automatic-gain-control applications. □

6. Automotive circuits

Precision auto tachometer squelches point bounce

by James B. Young
Canadian General Electric Ltd., Peterborough, Ont., Canada

A tachometer circuit for automobiles with capacitive-discharge ignition systems suppresses point bounce while measuring motor rpm accurately to within 1%. The circuit, which has an operating temperature range of -20°F to 150°F, can also be used as a temperature-compensated ratemeter or to eliminate relay-contact bounce.

Many automobile tachometers do not work properly with a capacitive-discharge ignition because this type of system employs the breaker points only for triggering an SCR. The voltage waveform across the breaker points, therefore, consists of a series of 14-volt pulses, rather than the 200-v spikes that exist in the usual kettering ignition system.

The tachometer circuit shown is composed of three sections: a relaxation oscillator at the input for point bounce suppression, a monostable multivibrator for pulse generation, and a buffer for driving a meter.

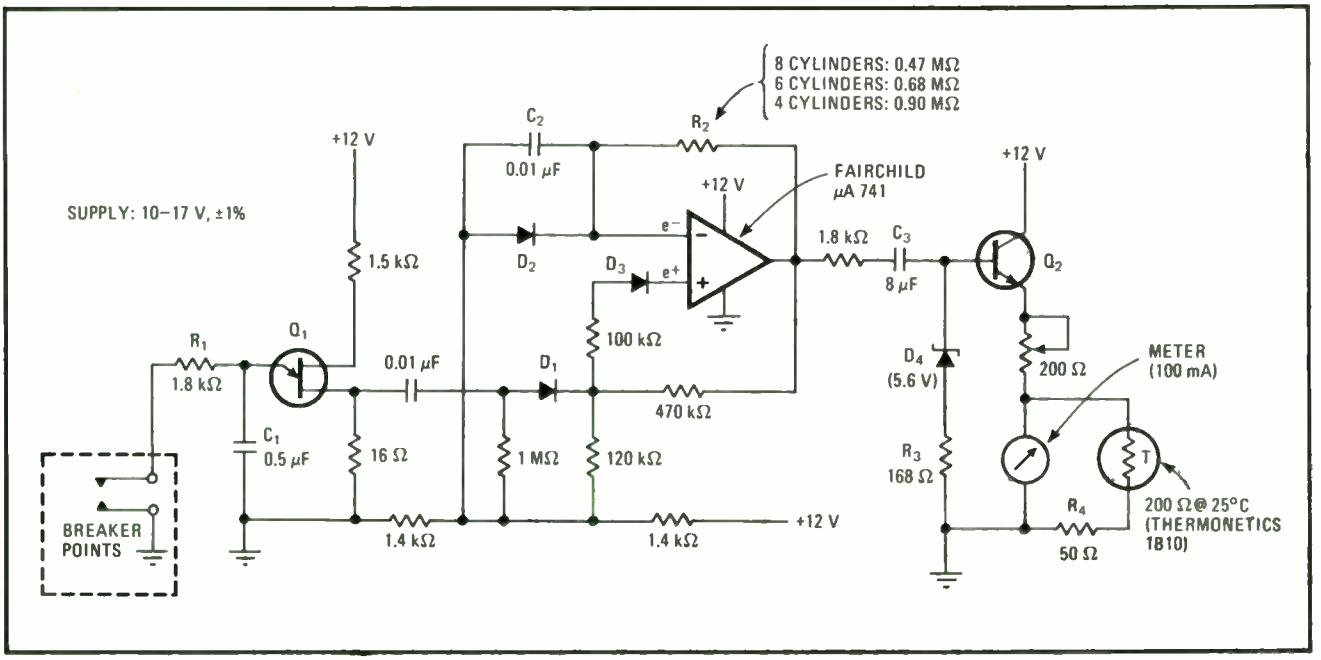
Unijunction transistor Q_1 is operated with an emitter current that is larger than its valley current so that it will not turn off after triggering. When the points open, capacitor C_1 charges through resistor R_1 until Q_1 fires (in 0.5 to 0.7 millisecond) and triggers the monostable. The current through R_1 keeps Q_1 on and prevents C_1 from charging until the points close. If the points bounce upon closure, they will not be open long enough to allow C_1 to charge and fire Q_1 again.

For every point opening, the monostable produces a pulse having a fixed width and amplitude. Normally, the output stage of the operational amplifier produces a negative saturation voltage. But when a positive trigger from the relaxation oscillator is applied through diode D_1, the op-amp's output switches to a positive saturation voltage, causing capacitor C_2 to charge positively through resistor R_2. Capacitor C_2 stores the charge until e^- is greater than e^+, and the op amp switches back to its stable state.

Diode D_2 clamps the voltage across C_2 to about -0.6 v, while diode D_3 provides temperature compensation for changes in D_2's junction-voltage drop. Both of these diodes should be kept in thermal contact with each other. Since the op amp is left floating so that it can be operated from a car's single supply voltage, it has a small positive output voltage when in its untriggered state, making capacitor C_3 necessary to decouple the meter.

Zener diode D_4 and resistor R_3 regulate the output against supply voltage variations, and the thermistor compensates for temperature variations in the base-emitter voltage of transitor Q_2. If a meter with a full-scale current rating of less than 5 milliamperes is used, the thermistor, as well as transistor Q_2 and resistor R_4, can be omitted. □

Measuring rpm. Intended primarily for automobiles with capacitive-discharge ignitions, tachometer circuit accurate within 1% is immune to breaker-point contact bounce. When points open, capacitor C_1 charges until unijunction transistor Q_1 fires and triggers one-shot formed by op amp. Point bounce is suppressed because C_1 takes 0.7 millisecond to charge before Q_1 can fire. Circuit can operate from -20°F to 150°F.



Sure-fire ignition system safely limits engine rpm

by L.G. Smeins
Ball Brothers Research Corp., Boulder, Colo.

For a capacitive-discharge automobile ignition system to work properly, the SCR in the circuit must receive an accurate and stable triggering signal. The circuit shown not only produces a reliable SCR trigger, but also filters point-bounce, limits rpm, and buffers the point opening.

The trigger pulses for the SCR are generated by a conventional unijunction-transistor trigger circuit that contains a UJT having a high intrinsic standoff ratio (η). The values of resistors R_1 and R_2 are chosen to make $R_2/(R_1+R_2)$ less than η.

When the points close, the bipolar transistor turns off and the base-2 voltage (V_{B2}) of the UJT becomes approximately $12R_{BB}/(R_{BB}+1\ k\Omega)$, provided that resistor R_1 is much greater than 1 kilohm. (R_{BB} is the interbase resistance of the UJT.) Capacitor C_1 charges to a voltage that is slightly less than ηV_{B2}.

When the points open, the bipolar transistor saturates, pulling V_{B2} to about 6 V and raising the capacitor's voltage to more than ηV_{B2}. The UJT now goes into avalanche, producing a voltage pulse across resistor R_3 that fires the SCR. The charging rate of capacitor C_1 lim its the SCR's firing repetition rate, thereby providin point-bounce filtering and rpm-limiting.

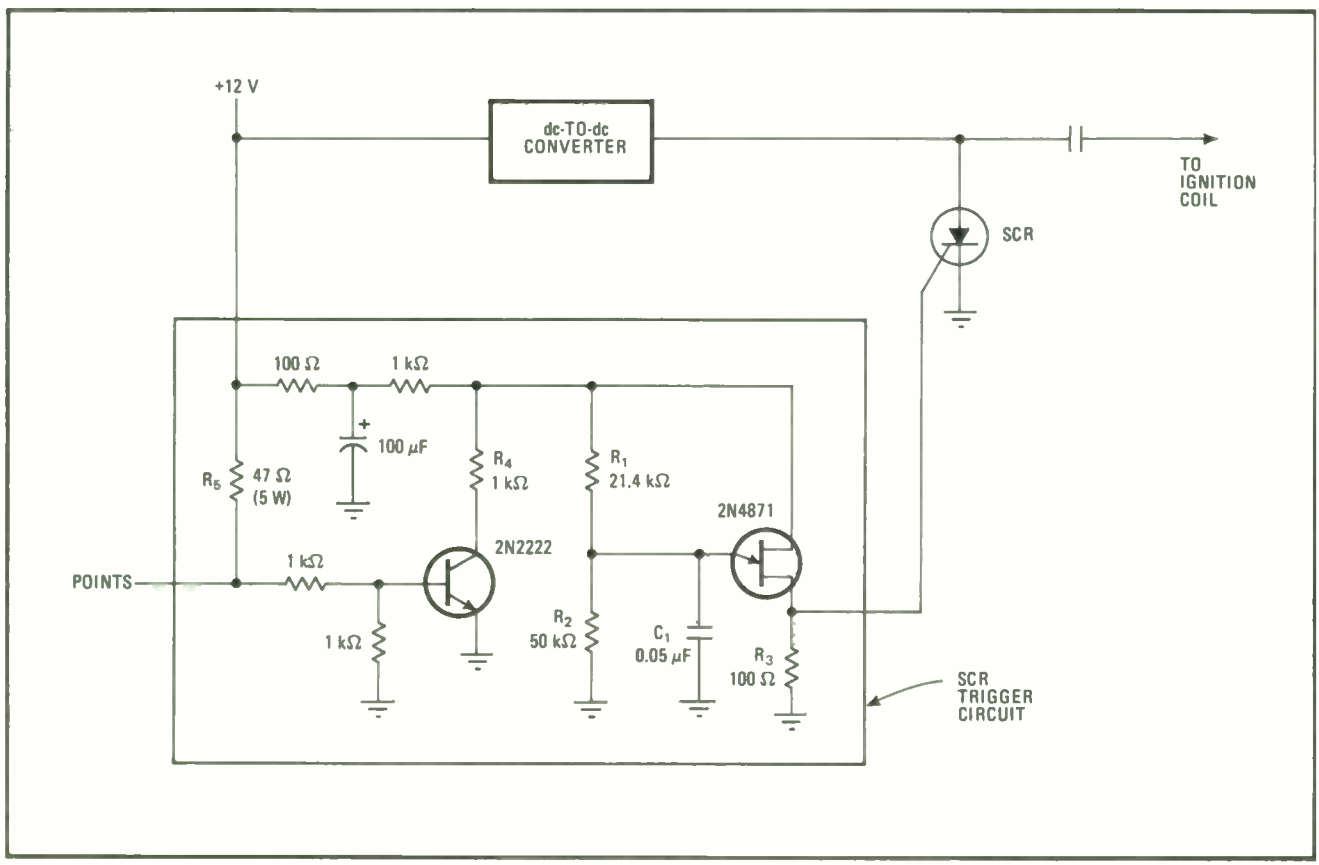
Suppose that an rpm limit of 6,000 is to be imposed on an eight-cylinder engine. For a type-2N4871 UJT $\eta = 0.75$ and $R_{BB} = 6$ kilohms. Resistor R_1 can be se equal to 21.4 kilohms, and resistor R_2 to 50 kilohms, s that $R_2/(R_1+R_2) = 0.7$, which is less than η. The firin voltage for the UJT is 4.55 V, and capacitor C_1 mus charge to this voltage 6,000 times per minute.

Two different charging rates occur because the targe capacitor's voltage changes when the points close. If th point gap is adjusted properly, the ratio of the close period to the open period is ⅔ to ⅓. Since the total pe riod is 2.5 milliseconds, the points remain open fo 0.833 ms and closed for 1.67 ms. The value required fo capacitor C_1 can be found by computing capacitor volt age at the end of each of these periods. In this case, value of 0.05 microfarad has been chosen for C_1.

The exact rpm setting needed for limiting can be ob tained by adjusting the value of resistor R_4 slightly When the limiting speed is reached, the ignition fire every other plug, in this way avoiding the severe tran sient loads associated with circuits that shut down com pletely to limit rpm.

Although the circuit shown here is for a point-drive system, it can be adapted easily for a magnetic or op tical pickup by removing resistor R_5 and driving th bipolar transistor with a logic-level signal. □

Improving gas mileage. Efficient automobile combustion is provided by this capacitive-discharge electronic ignition, which features reliable SCR-triggering. The charging rate of capacitor C_1, because it determines how often the SCR is fired, provides rpm-limiting and point-bounce filtering. When the limiting speed is reached, only every other plug is fired to avoid the transient loading caused by a complete shutdown.



Ice warning indicator monitors road conditions

by Steven E. Summer
Hauppauge, N.Y.

For more than 10 years, Rover automobiles have had a built-in indicator that warns their drivers of possibly icy roads. With the availability of the versatile and economical integrated quad op amp, this same safety feature can now be installed quite easily in any make of automobile.

The ice warning indicator shown monitors ambient air temperature to alert the driver to the conditions under which ice will start forming on the roads—that is, when air temperature is between 32°F and 36°F in wet weather. The device is rugged and provides good noise rejection.

The circuit produces a variable duty cycle to control the flash rate of a light-emitting diode. At 36°F, low-duty-cycle light flashes are generated, and as the temperature drops towards 32°F, the LED indicator remains on continuously. The flashes occur about once a second.

A thermistor with a nominal resistance of 15 kilohms at 25°C acts as the temperature-sensing probe. It is mounted in a baffled enclosure that is exposed to ambient air. The baffle prevents erroneous readings due to air movement.

The circuit's three amplifiers are part of the same chip as the quad op amp. Since circuit action depends on current ratios, circuit operation is insensitive to variations in battery voltage, making zener regulation unnecessary.

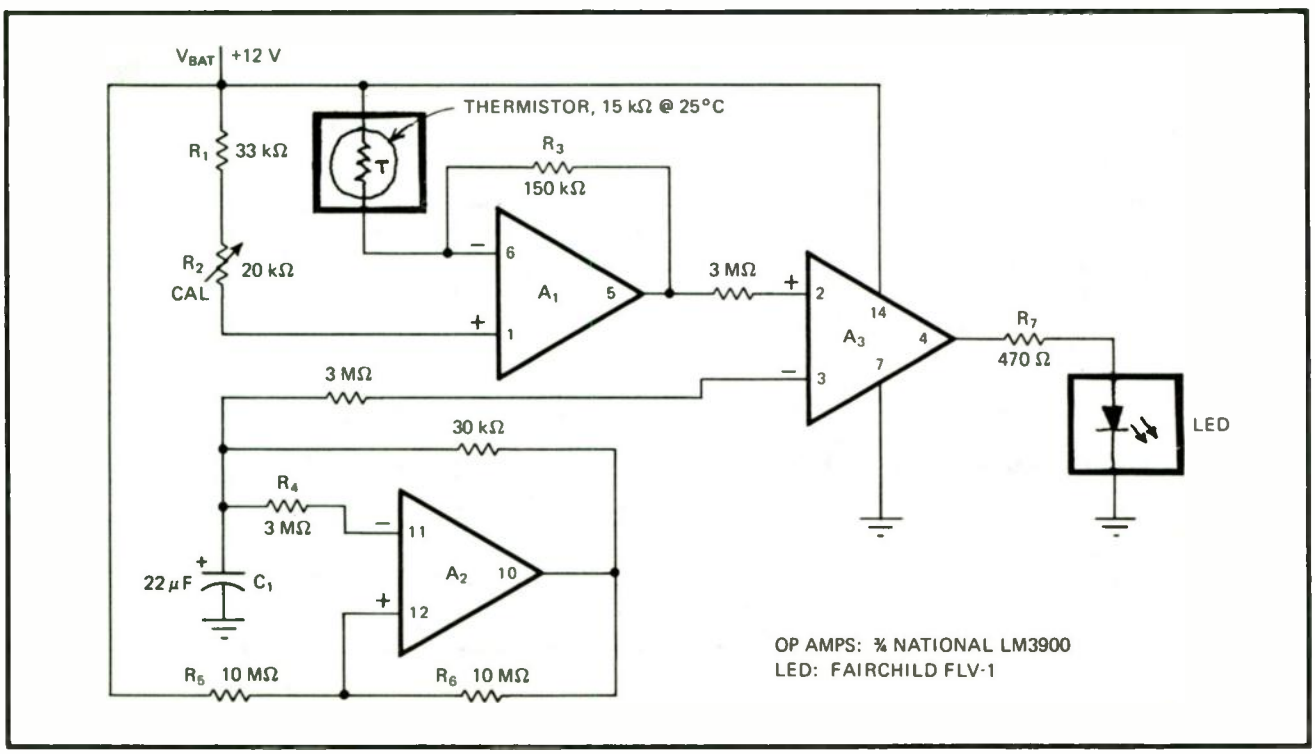
Amplifier A_1 compares the resistance of the thermistor to the series combination of resistors R_1 and R_2. Feedback resistor R_3 sets the correct slope of A_1's output-voltage response to temperature. At 32°F, A_1's output is $0.6V_{BAT}$; at 36°F, it's $0.3V_{BAT}$.

Amplifier A_2 is connected as a free-running multivibrator having a repetition rate of approximately one pulse per second. Three resistors—R_4, R_5, and R_6—set the upper and lower voltage limits for capacitor C_1 at $0.6V_{BAT}$ and $0.3V_{BAT}$, respectively.

The outputs of amplifiers A_1 and A_2 are compared by amplifier A_3. When the multivibrator (A_2) output is lower than A_1's output, A_3's output goes positive, lighting the LED. Resistor R_7 limits LED current to around 25 milliamperes.

Resistor R_2, which calibrates the circuit, is adjusted by placing the thermistor probe in an ice slurry and setting R_2 so that the LED is always on. Other operating points can be obtained by changing the values of resistors R_1, R_2, and R_3. □

Driving aid. Ice warning indicator, which puts the flexibility and economy of the quad op amp to work, uses a thermistor probe to sense air temperature. At 36°F, the LED indicator flashes once per second. This flash rate increases as temperature approaches 32°F until the LED remains on continuously. A varying-duty-cycle output determines the flash rate. Amplifier A_2 is wired as a free-running multivibrator.



IC boosts starting energy for solid-state ignition

by Charles R. Carter
McMaster University, Hamilton, Ont., Canada

Even in very cold weather, starting need not be a problem in a car with a conventional solid-state ignition system. The addition of a single monolithic integrated circuit and a few discrete devices will keep spark timing accurate and guarantee that six to 10 times more energy than usual reaches the spark plugs.

The circuit is interposed between the ignition points and the solid-state ignition (Fig. 1). Every time the points produce a pulse, the dual monolithic multivibrator IC turns it into a train of pulses by driving a transistor on and off repeatedly. As a result, each spark plug gets many chances to fire with each opening of the points, instead of just one.

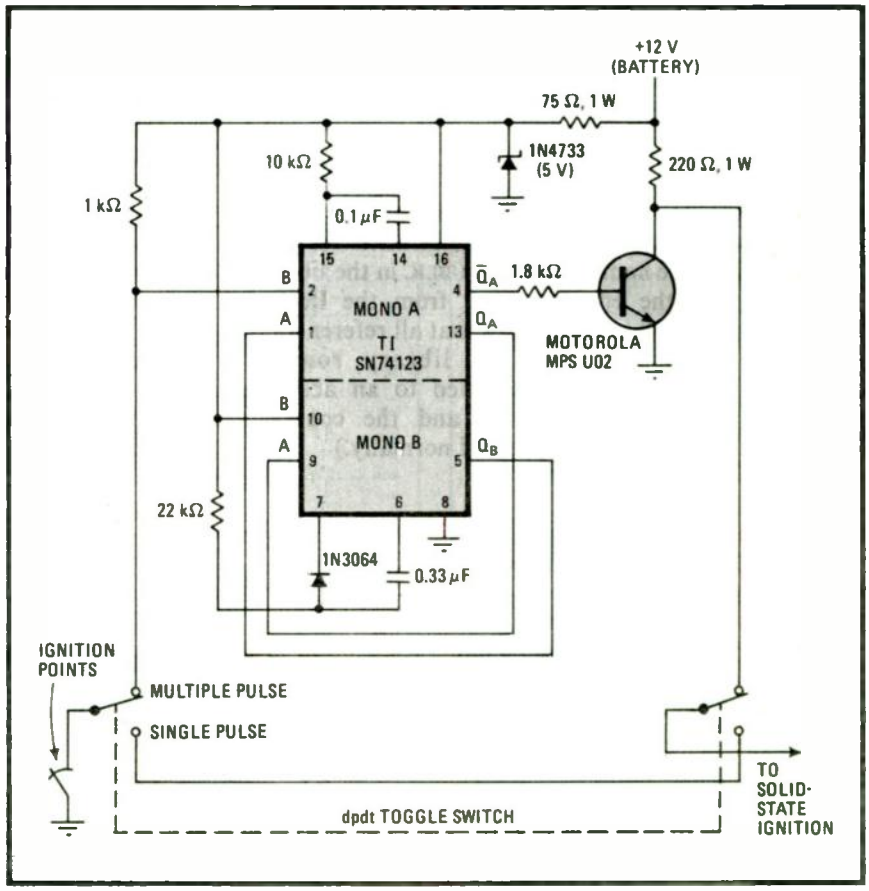
A Texas Instruments SN74123 multivibrator is shown in the figure, but for operation at very low temperatures (to −55°C) the SN54123 package can be used in exactly the same way. When the points open, a rising edge at the B input to mono A occurs, making Q_A go high and $\overline{Q}_A$ go low for 500 microseconds. The falling edge of the Q_A output, applied to the A input of mono B, turns on a Q_B pulse 7 milliseconds long.

The Q_B output from mono B is connected to the A input of mono A. If the B input from the points remains high (in other words, the points remain open), mono A is triggered from Q_B, causing a second pulse of 500 μs to occur 7.5 ms after the first pulse. This second pulse again triggers mono B. This process is repeated over and over, thereby producing a train of pulses. When the points close, mono A is inhibited, and the pulse train is terminated.

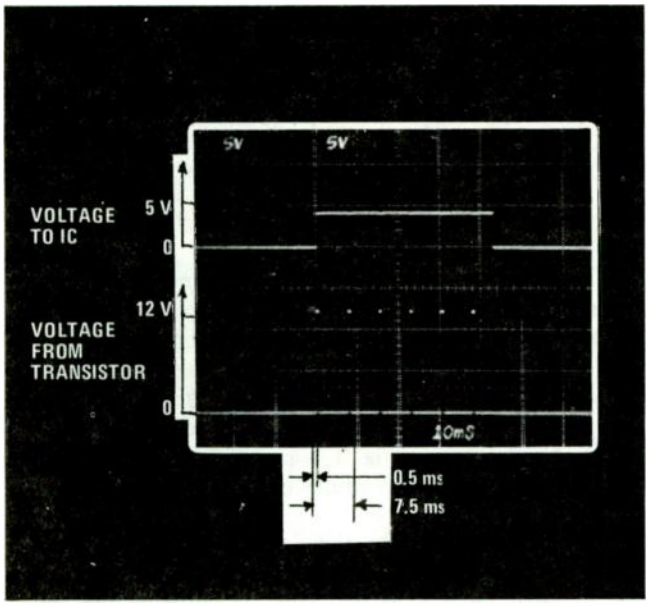
The pulse train from the $\overline{Q}_A$ output of mono A is applied to the base of the transistor, which then acts in an identical fashion to the points, insofar as the solid-state ignition is concerned. Thus, when the points open as shown in Fig. 2, a train of pulses is applied to the solid-state ignition, rather than just one pulse as would be the case in normal operation, causing the spark plug to fire many times.

The interpulse spacing provided by mono B is not critical. A lower boundary is determined only by the maximum rate at which the solid-state ignition operates. This is typically 2.5 to 3 ms.

The upper boundary is related to the desired number



1. Extra sparks for better starts. When the toggle switch is set for the multiple-pulse starting mode, the multivibrator IC and transistor send a series of pulses to the ignition every time the points open. After starting, the switch is simply flipped for normal triggering to the solid-state ignition. The zener diode provides 5-V regulation for the IC down to a battery voltage of about 7 V.



2. Pulses to ignition. Upper trace shows voltage waveform at B input of mono A due to points opening. Lower trace shows the resulting train of pulses, which triggers the solid-state ignition six times. The train of pulses is terminated when the points close.

of pulses that are produced while the points are open. For a V-8 engine with a cranking speed of one revolution per second and a dwell angle of 30°, the 7.5-ms interpulse spacing produces about 10 pulses spaced at 3° intervals while the points are open. Slower cranking speed provides more pulses with a smaller interval in degrees between pulses.

This technique was tested several times in January 1976 on a 1967 Mustang equipped with a solid-state ignition that refused to start in −10°F temperatures and high humidity. After several attempts to start the car had failed, the multiple-pulse circuit was switched in by using the toggle switch. The engine then started almost immediately. For normal driving, the toggle switch is returned to the single-pulse position. □

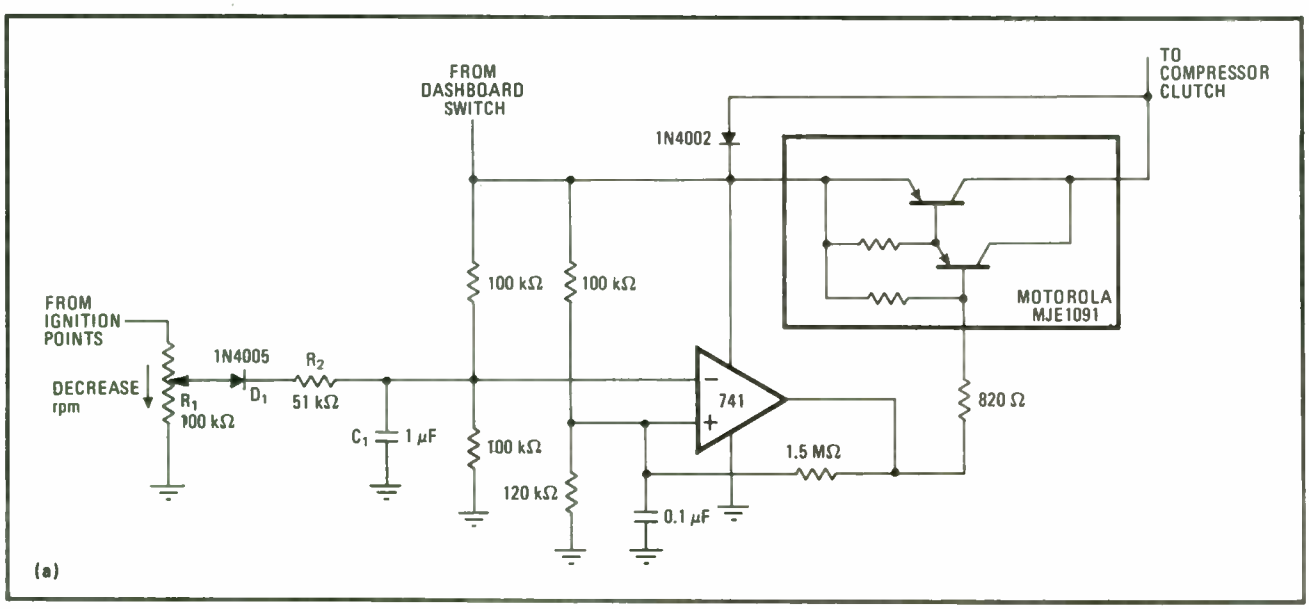
Electronic switch controls automobile air conditioner

by L.G. Smeins
Ball Brothers Research Corp., Boulder, Colo.

Stalling and overheating often plague an air-conditioned automobile in which the refrigerator compressor continues to run while the engine idles. The solution to the problem is simple—turn the compressor off when the engine is idling, and turn it on again when the car picks up speed.

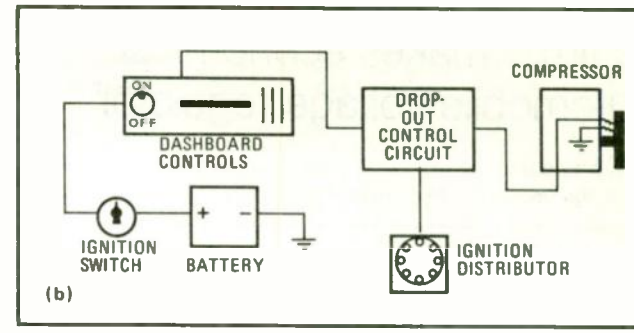
The control circuit shown in (a) does this by monitoring the engine's rpm and electrically disengaging the compressor clutch for as long as the engine is idling. The circuit works well for the electromagnetic compressor clutch found in most cars.

Compressor drop-out and pull-in are controlled by an operational amplifier that is connected as a Schmitt trigger and that drives a series bipolar switch. When engine rpm falls below the drop-out voltage level, which is determined by potentiometer R_1, power is removed from the magnetic clutch. Hysteresis in the Schmitt trig-



ger prevents the clutch from engaging again until the engine rpm is approximately double the drop-out rpm. The simple charge-pump pulse-rate network, consisting of diode D_1, resistor R_2, and capacitor C_1, performs the rpm sensing.

After the circuit is installed as suggested in (b), the drop-out point should be adjusted for optimum performance. To do this, first start the engine and let it idle with the air conditioner turned on. If the compressor clutch is not engaged, turn potentiometer R_1 (in the direction for decreasing rpm) until the clutch engages. Now turn this same potentiometer (in the direction of increasing rpm) until the compressor clutch just disengages. At this potentiometer setting, the compressor should turn on when engine rpm increases to approximately 1,700 and should turn off when the engine drops back to an idle. □



Keeping cool. Control circuit (a) monitors engine rpm and turns of air conditioner when engine drops to idle, preventing stalling or overheating. The operational amplifier is connected as a Schmitt trigger whose hysteresis provides the voltage differential needed between compressor turn-on and turn-off. A bipolar switch drives the compressor's clutch. The circuit can be installed easily (b).

Tail-biting one-shot keeps car-door light on

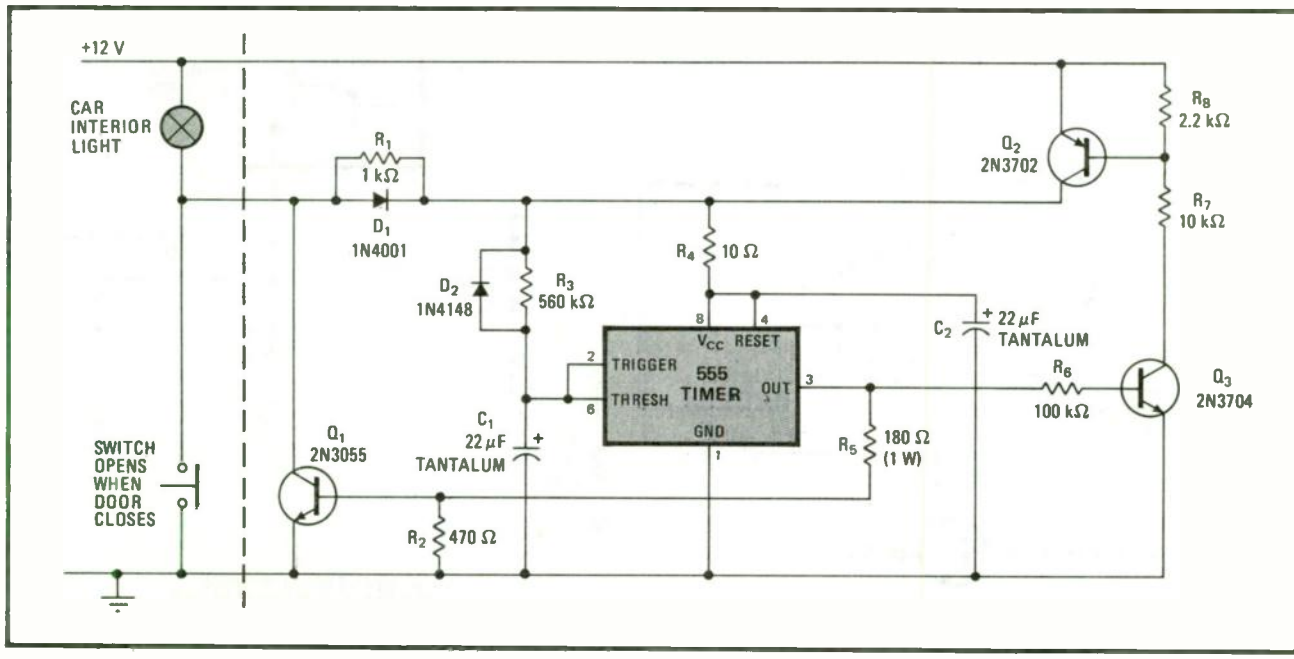
by B. D. Redmile
Salisbury, Rhodesia

A one-shot multivibrator that drives the same line it is sensing is useful for such applications as burglar alarms and switch-action delays because it can be fitted at any point in the circuit. Full reliability of the original circuit is retained, since connection of the one-shot across it does not break it. In the arrangement shown in the schematic, a 555 timer keeps the interior light of a car turned on for 10 seconds after the car doors are closed.

In the idle condition (door closed, light off), the 12-volt line charges capacitor C_1 and supplies power to the 555. The current drain is only about 10 milliamperes, so the light does not go on. The threshold terminal of the 555 is held high by R_3, so its output is low and all the rest of the circuit is off. When a door is opened, the light goes on in the usual way and the power to the one-shot is removed. Capacitor C_1 then discharges rapidly through D_2 and R_1.

When the door is closed and the lamp starts to turn off, power flows to the 555. With C_1 discharged, the threshold terminal is at low voltage, so the output goes high. This turns on transistors Q_1, Q_2, and Q_3. Q_2 maintains power to the 555 while Q_1 furnishes a path for current to flow to keep the light on. After a delay set by C_1 charging through R_3, the 555 output goes low, restoring the circuit to its idle state.

The combination of C_2 and R_4 prevents transients on the battery supply from damaging the 555 or prematurely terminating the one-shot high output pulse. □



Holds the light. When car door closes, output current pulse from 555 timer turns on transistor Q_1 to keep interior light on for about 10 seconds. This type of one-shot arrangement, driving the line that is sensed, can be added at any point in the circuit. It is useful in alarm systems, process controls, automatic machinery, safety circuits, and convenience circuits such as this one.

IC timer makes economical automobile voltage regulator

by T.J. Fusar
Powell-Mac Electronics, Madison, Wis.

A 555-type IC timer, in combination with a power Darlington transistor pair, can provide low-cost automotive voltage regulation. Such a regulator can even make it easier to start a car in cold weather.

As the diagram shows, the circuit requires very few parts. The value of resistor R_1 is chosen to prevent the timer's quiescent current, when the timer is off (output, pin 3, low), from turning on the Darlington pair.

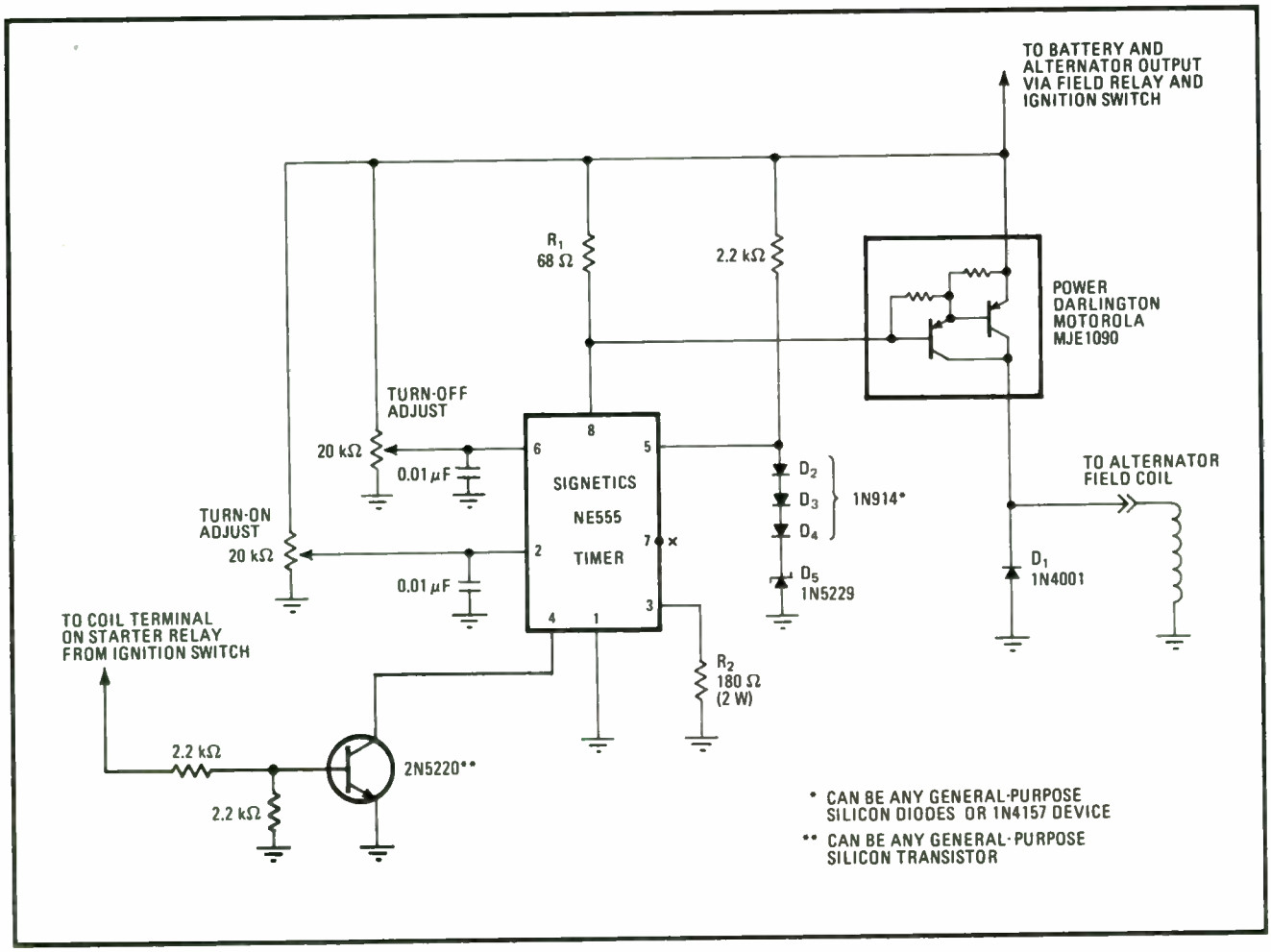
If battery voltage becomes too low, the timer turns on, driving its output high and drawing a current of about 60 milliamperes through resistor R_2. This causes a sufficient biasing voltage to be developed across resistor R_1 and the Darlington turns on, supplying the energizing current to the field coil of the car's alternator. Diode D_1 suppresses the reverse voltage of the field coil when the Darlington pair is turned off.

The regulator's low-voltage turn-on point is fixed by setting the voltage at the timer's trigger input (pin 2) to approximately half the reference voltage existing at its control-voltage input (pin 5). The high-voltage turn-off point is set by making the voltage at the timer's threshold input (pin 6) equal to the reference voltage at pin 5. At 77°F, the turn-on voltage is typically 14.4 volts, and the turn-off voltage is typically 14.9 v. These voltage levels, of course, should be set to match the charging requirement of a given car's specific battery-alternator combination.

The value of the reference voltage is established by the diode string, D_2 through D_5; here, it is approximately 5.9 v. The output voltage has a negative temperature coefficient of -11 millivolts/°F.

A transistor and a couple of resistors can be added to the circuit for better cold-weather starting. These parts are drawn in color in the figure. During starting, the transistor holds the timer in its off state, lightening the load on the car's cranking motor. (And to prevent radio interference, a 10-microfarad capacitor can be connected from the Darlington emitter to ground.) □

Regulating car voltage cheaply. Monolithic 555-type timer is the heart of this simple automobile voltage regulator. When the timer is off so that its output (pin 3) is low, the power Darlington transistor pair is also off. If battery voltage becomes too low (less than 14.4 volts in this case), the timer turns on and the Darlington pair conducts. The parts drawn in color permit easier starting in cold weather.



Automobile ignition system is rugged and reliable

by J.P. Thomas
Litton Industries, Litton Systems (Canada) Ltd., Rexdale, Ont., Canada

Capacitive-discharge ignition systems permit engine performance to be maintained over an extended period by reducing automotive component degradation due to mechanical wear. With a capacitive-discharge system, ignition voltages are high, allowing sparkplug gap spacing to vary considerably without affecting engine performance. But ignition point current is kept low so that point erosion is significantly reduced.

The failure of a capacitive-discharge ignition system can usually be attributed to erratic triggering of the silicon-controlled rectifier, the heart of the circuit. Erratic triggering can generally be traced to either poor design of the trigger circuit or improper elimination of point bounce.

In contrast, here is a capacitive-discharge ignition system that provides reliable SCR triggering over a broad range of operating conditions and offers an engine overspeed cutout as an additional feature. The system can operate over the temperature range of −70°F to +150°F and over the supply-voltage range of 7 to 20 volts.

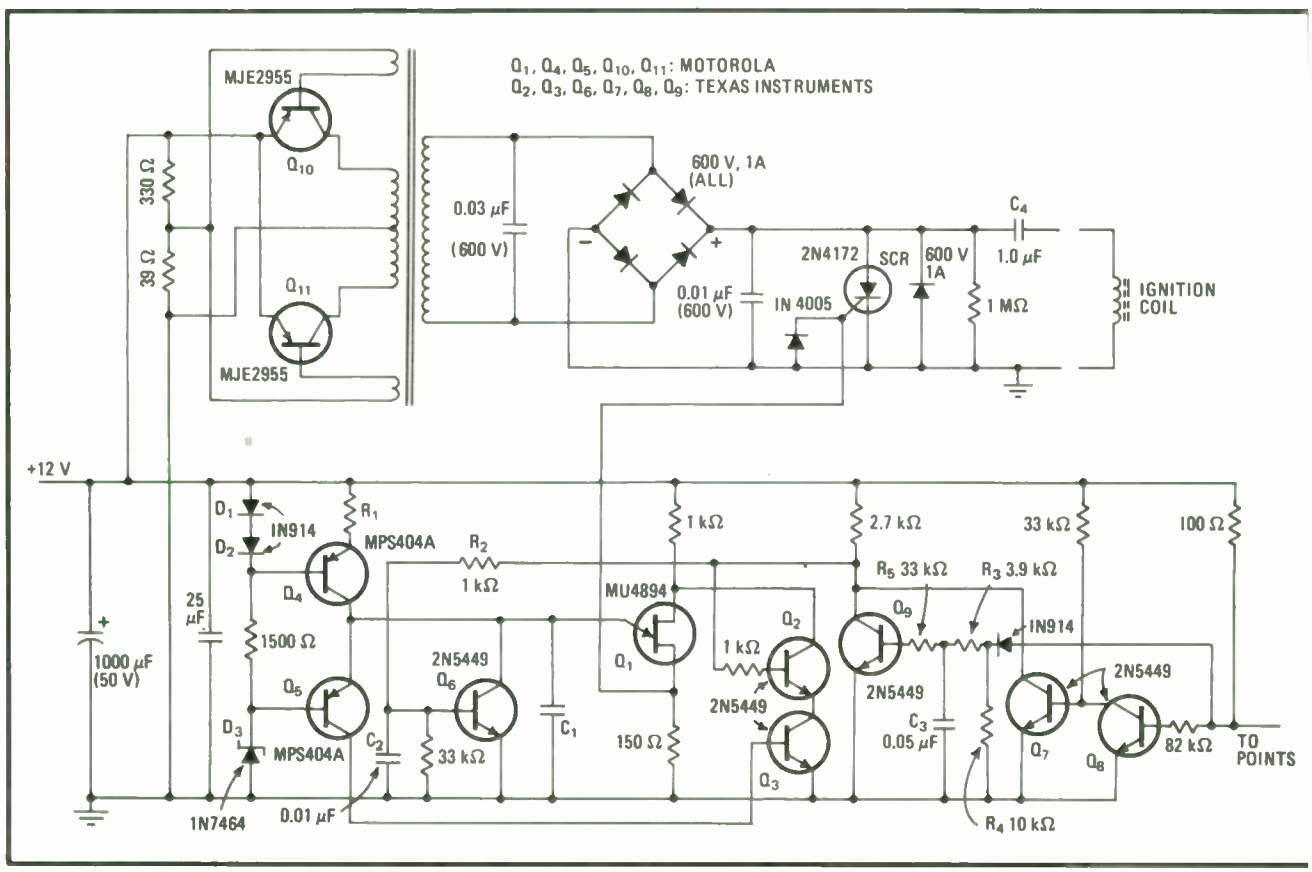
Unijunction transistor Q_1 generates trigger pulses for the SCR by discharging capacitor C_1 when transistors Q_2 and Q_3 are both saturated. Engine overspeed protection is provided by transistors Q_3, Q_4, and Q_5, diodes D_1, D_2, and D_3, and a speed limit set by the values of resistor R_1 and capacitor C_1. Transistor Q_4 and its associated components act as a current source that charges capacitor C_1 at a predictable constant rate when the points close. Transistor Q_6 discharges C_1 when the points open.

Unless capacitor C_1 is charged to a voltage that equals D_3's zener voltage plus Q_3's base-emitter voltage, transistor Q_3 remains off so that the SCR trigger pulses are inhibited. If the time between successive point openings is less than C_1's charging time, the ignition system is inhibited, thereby providing overspeed protection. The circuit's cutoff point is precise so that there is no erratic behavior at the edge of the protection speed and the possibility of engine damage due to transient mechanical loads is eliminated.

When the ignition points open, transistor Q_3 is in saturation, and transistor Q_2 will go into saturation as transistor Q_7 turns off and transistor Q_8 saturates. After the time elapse (about 5 microseconds), determined by the time constant of capacitor C_2 and resistor R_2, transistor Q_6 is driven into saturation, removing any charge remaining on capacitor C_1.

At some time during this sequence, the voltage across

Sure firing. Automobile capacitive-discharge ignition system performs reliably at 7 to 20 volts from −70 F to +150°F, in addition to providing engine overspeed protection. Unijunction transistor Q_1 generates trigger pulses for the SCR by discharging capacitor C_1. When points close C_1 is charged; when points open, C_1 is discharged. The discharge capacitor, C_4, accumulates about 375 V for high spark energy.



C_1 falls below the level required to keep transistor Q_5 on, forcing this device, as well as transistor Q_3, to turn off. After the time (around 20 μs) established by capacitor C_3 and resistor R_3 has passed, transistor Q_9 saturates, causing transistor Q_6 to turn off and removing the base drive from transistor Q_2.

When the points close, transistor Q_7 saturates, and transistor Q_8 turns off, maintaining transistor Q_2 in its off state. Capacitor C_3 begins to discharge through resistors R_3, R_4, and R_5 and Q_9's base-emitter junction. The time constant of this network is long enough to keep transistor Q_9 saturated during a point-bounce cycle, but short enough to discharge capacitor C_3 completely during a normal point-dwell cycle.

Transistors Q_{10} and Q_{11}, the transformer, and the bridge rectifier form a dc-to-dc inverter that charges the 1-microfarad discharge capacitor, C_4, to about 375 V. This voltage level provides a spark energy that is an order of magnitude larger than what is available from a standard ignition system. A conventional ignition coil is used as a pulse transformer to raise the discharge voltage to about 40 kilovolts, which is approximately four times greater than the voltage provided by conventional ignitions.

For a four-stroke engine, the value of resistor R_1 can be initially chosen as:

$$R_1 = 18/NMC_1$$

where N is the number of cylinders, M is the maximum engine rpm, and C_1 is expressed in farads. For a two-stroke engine, the initial estimate for R_1 is:

$$R_1 = 9/NMC_1$$

The value of capacitor C_1 is somewhat arbitrary, but it should be at least 0.1 μF and not more than 0.5 μF. After choosing C_1, the value of R_1 must be adjusted to give the precise speed limit desired. □

Tri-level indicator monitors automobile's electrical system

by S. K. Wong
Torrance, California

The battery voltage of a car in operation indicates a great deal about the condition of the alternator, the voltage regulator, and the battery itself. Expensive sports cars are routinely equipped with gages to monitor voltage. Sedans may be optionally equipped with these voltmeters, but a good gage usually costs more than $30, and its size may make it difficult to install on the instrument panel.

Fortunately, exact voltage readings are not necessary to indicate the condition of the electrical system, even if a precise value could be read while the car is running. An instrument that shows three levels of voltage can give enough information to indicate that (1) a major component of the electrical system is faulty; (2) the battery voltage is fairly low, and the electrical system

should be checked; or (3) the battery voltage is adequate for efficient functioning of the system.

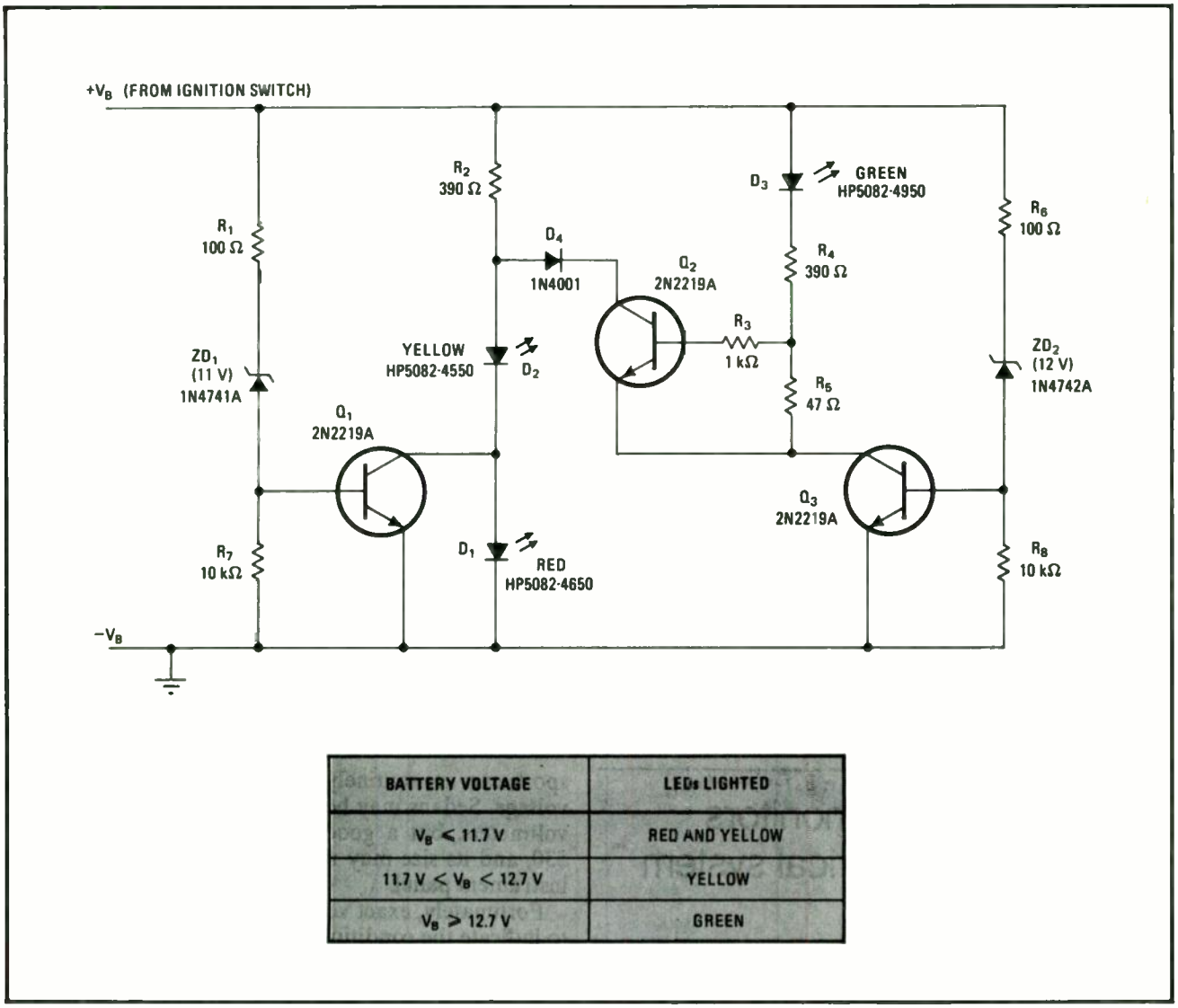
A solid-state tri-level voltage indicator that uses light-emitting diodes to show three voltage ranges can be built for $5 to $10, depending on the quality of the parts used, and it is a bargain for the purpose it serves. The circuit shown in the diagram uses, in addition to the three LEDs of different colors, three npn switching transistors, two zener diodes, one blocking diode, and a handful of 0.5-watt resistors. The red and yellow combination indicates a battery voltage of less than 11.7 V, yellow shows 11.7 to 12.7 V, and the green light shows that the battery voltage is 12.7 V or more.

If the battery voltage is below 11.7 V, all of the transistors are turned off. Diode D_4 blocks the current path through green LED D_3, the base and collector of Q_2, D_2, and D_1, so that current flows only through R_2, D_2, and D_1. The red and yellow LEDs light up to indicate that the battery, voltage regulator, alternator, or any combination of the three, is bad.

If the voltage is between 11.7 and 12.7 V, transistors Q_2 and Q_3 are still turned off, but zener ZD_1 conducts and lets Q_1 turn on to shunt out the red LED. Thus only the yellow LED lights up, warning the driver of a fairly low battery voltage. Unless this low-voltage situation improves after a few miles of driving, the electrical system of the car should be inspected for faults or high contact resistances.

If the battery voltage quickly reaches 12.7 V or more after the car is started, Q_3 also turns on. Current through Q_3 lights the green LED and also turns on Q_2 to shunt out the yellow LED. The resulting green light assures the driver of a functioning electrical power system in his car.

The user may choose zener diodes with somewhat different breakdown voltages if he wants to shift the three indication levels to fit his own requirements. □



BATTERY VOLTAGE	LEDs LIGHTED
$V_B < 11.7$ V	RED AND YELLOW
11.7 V $< V_B <$ 12.7 V	YELLOW
$V_B > 12.7$ V	GREEN

Battery-voltage indicator. Colored LEDs indicate three ranges of battery voltage in car. A weak battery turns on red and yellow, a stronger battery breaks down 11-V zener to light only yellow, and a strong battery turns on green as both zeners conduct. Resistors R_7 and R_8 provide high-temperature stability. This unit can warn of need for corrective maintenance of car's electrical system.

7. Bridge circuits

Feedback linearizes resistance bridge

by Robert D. Guyton
Mississippi State University, State College, Miss.

With the addition of a feedback circuit, the output voltage of a standard resistance bridge can be made to vary linearly for a change in bridge resistance. The feedback circuit provides good sensitivity for a wide range of bridge resistance variations, while maintaining the full-scale linearity of the bridge output voltage to within 0.1%. Furthermore, either an ac or a dc voltage may be used to excite the bridge.

The output voltage of the standard bridge remains zero as long as its four resistance arms are equal to each other, with a resistance value of R ohms. One arm of the bridge is variable from this resistance null:

$$R_x = R + \Delta R$$

where ΔR represents the change in bridge resistance. For the standard bridge:

$$V_o' = V_1(\Delta R)/(2R+\Delta R)$$

This is not a linear relationship, since ΔR appears in the denominator. The standard bridge, therefore, is usually limited to those applications that involve only small values of ΔR.

The feedback circuit shown in the figure alters the bridge excitation voltage so that the relationship between the output voltage and ΔR becomes linear:

$$V_o = (1+2R_f/R)V(\Delta R)/2R$$

Feedback resistor R_f determines the circuit's sensitivity to the change in bridge resistance. Bridge excitation voltage can be written as:

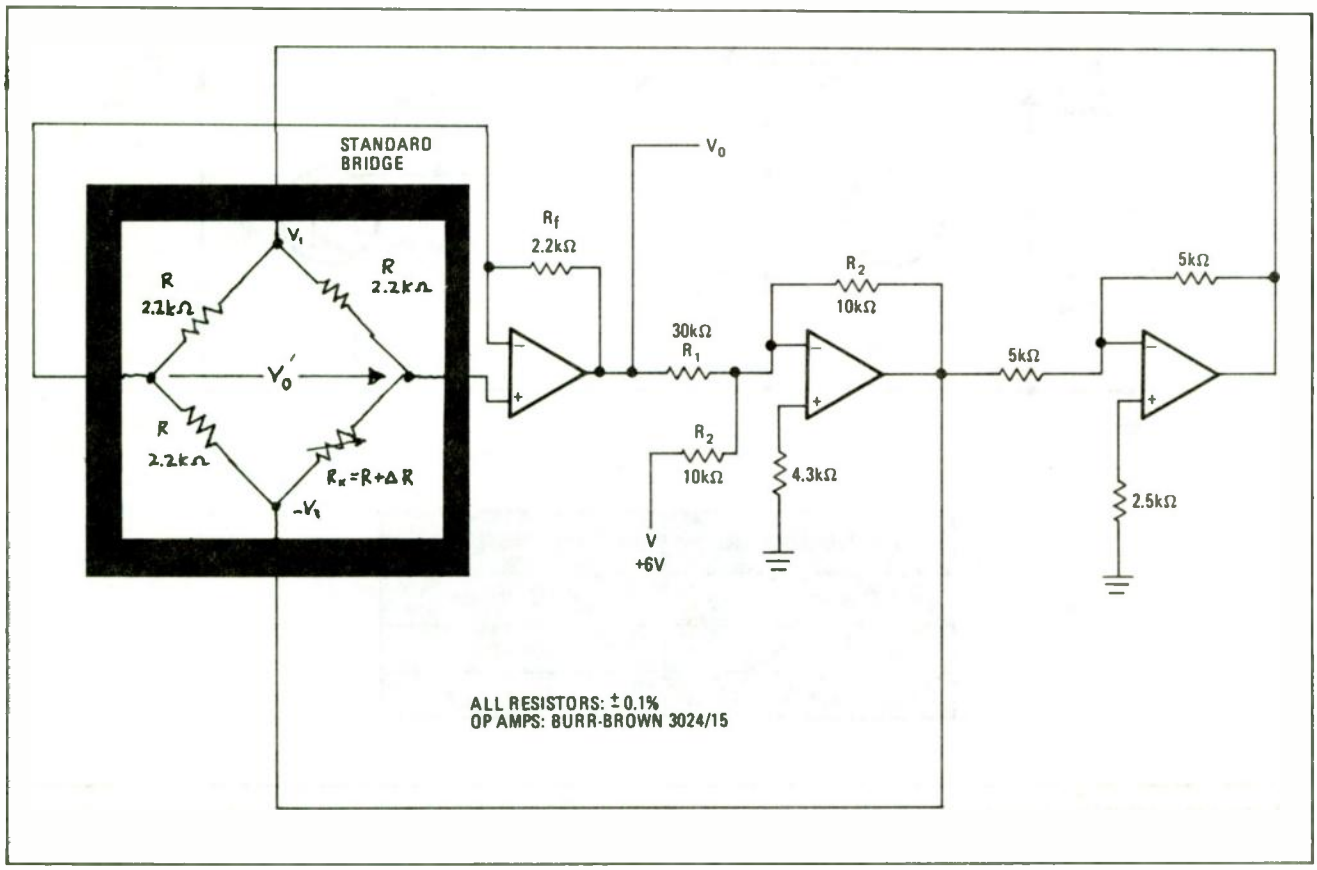
$$V_1 = V + RV_o/(R+2R_f)$$

when:

$$R_1 = R_2(R+2R_f)/R$$

Resistance R_x can vary from 0 to 2R. □

Linearized resistance bridge. Adding feedback circuit to standard resistance bridge allows output voltage V_o to be linearly related to variations in bridge resistor R_x. Changes in bridge resistance produce output voltage that is linear to within 0.1%. Circuit sensitivity is set by value of feedback resistor R_f. Amplifiers control bridge excitation voltage V_1, which can be due to either ac or dc source.



Winking LED notes null for IC-timer resistance bridge

by James A. Blackburn
Wilfrid Laurier University, Waterloo, Ont., Canada

A resistance bridge that makes use of the popular 555-type IC timer operates without requiring the usual combination of a meter and an amplifier. Moreover, the circuit's sensitivity does not depend on the unknown resistance. And since a light-emitting diode is used for visual indication, there's no need to worry about shock-isolation for a meter movement. Two possible applications for the bridge are as a thermometer (where the unknown could be a thermistor) or as a photometer (where the unknown could be a photoresistor).

The color block in the diagram shows where unknown resistor R_X is inserted in the bridge. When the resistance of the dual potentiometer is increased, the brightness of the LED also steadily increases. Then, at a particular setting of the potentiometer (R_{POT}), the LED's brightness is suddenly halved. The ratio of R_{POT}:R_X at which this winking occurs is determined solely by the properties of the two IC timers.

The first timer ($TIMER_1$) operates in its astable mode and, therefore, is free-running. Its output (signal A) is low for a period of $T_1 = 0.693R_XC$ seconds and high for a period of $T_2 = 0.693(R_X + R_{POT})C$ seconds. The output from $TIMER_1$ is differentiated and then used to trigger the second timer ($TIMER_2$), which is operating in its monostable mode.

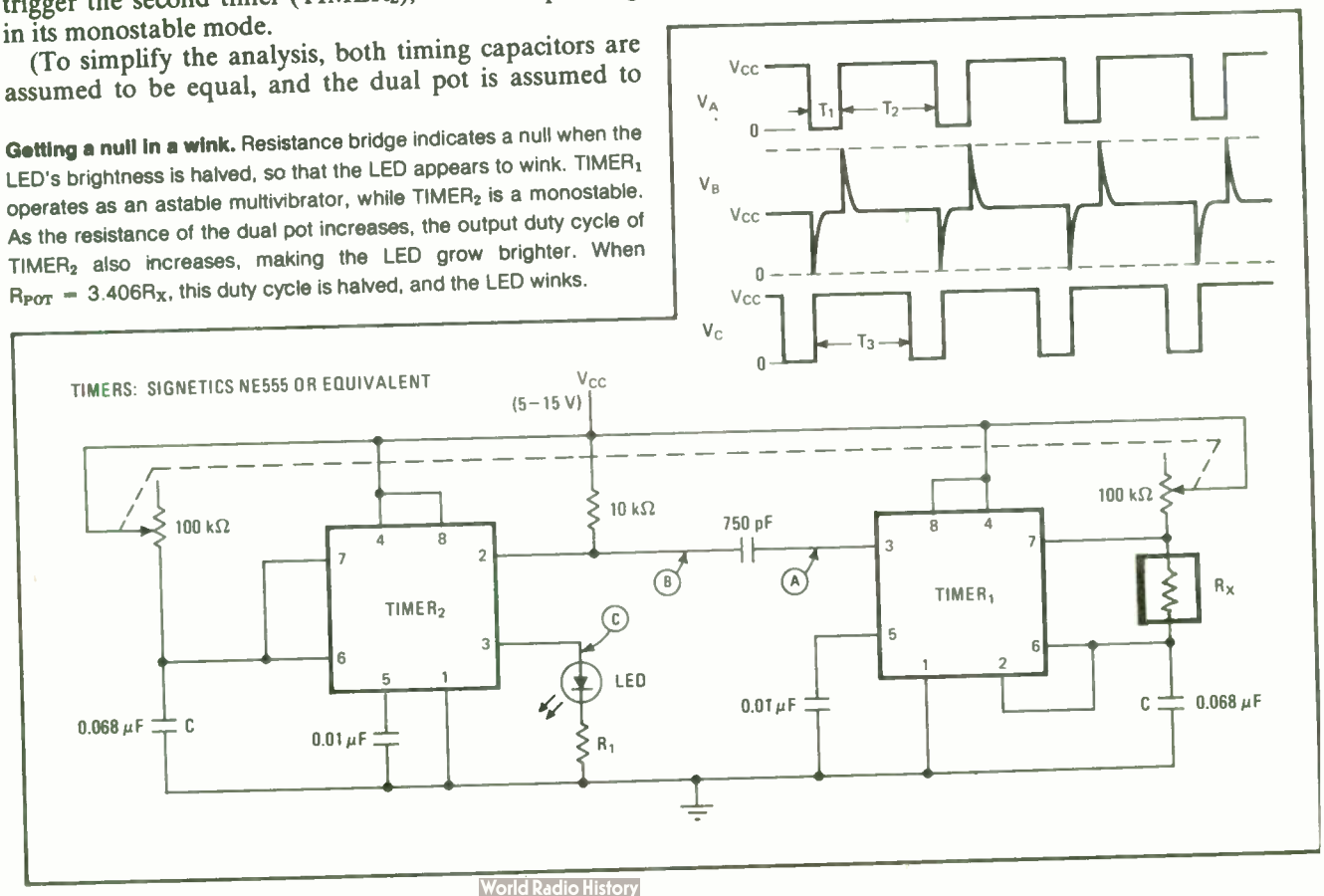
(To simplify the analysis, both timing capacitors are assumed to be equal, and the dual pot is assumed to track without error. In addition, the triggering spikes are considered to be of negligible width compared to period T_1.)

As R_{POT} is increased, the periods of signals A and B become longer, and the on-time of $TIMER_2$ ($T_3 = 1.1R_{POT}C$) starts to increase at a slightly faster rate. This means that the duty cycle of signal C is getting larger, and the LED will appear to grow brighter.

A closer look at the waveforms reveals that when period T_3 is just slightly less that $T_1 + T_2$, the duty cycle of signal C is nearly 100%. But when T_3 is slightly greater than $T_1 + T_2$, the duty cycle of the signal C drops to 50% and, at the same time, the frequency of this signal decreases to half the frequency of signal A. This happens because $TIMER_2$ locks out trigger pulses while its output is still high and, therefore, ignores all alternate negative-going spikes.

Further increases in R_{POT} cause the duty cycle of signal C to rise again slowly from 50% to a limiting value of 79.4%. The abrupt transition from 100% to 50% occurs when $R_{POT} = 3.406R_X$, making the calibration of this resistance bridge intrinsically linear. Circuit performance is limited by the desired upper and lower operating frequencies and the width of the triggering pulses.

For the component values shown, the circuit can operate over a fairly wide range of unknown resistance values—from 1 kilohm to 100 kilohms. The value selected for the LED's current-limiting resistor, R_1, depends on the supply voltage used. □



Getting a null in a wink. Resistance bridge indicates a null when the LED's brightness is halved, so that the LED appears to wink. $TIMER_1$ operates as an astable multivibrator, while $TIMER_2$ is a monostable. As the resistance of the dual pot increases, the output duty cycle of $TIMER_2$ also increases, making the LED grow brighter. When $R_{POT} = 3.406R_X$, this duty cycle is halved, and the LED winks.

Circular voltage divider needs fewer resistors

by Dale Hileman
Physiometrics Inc., Malibu, Calif.

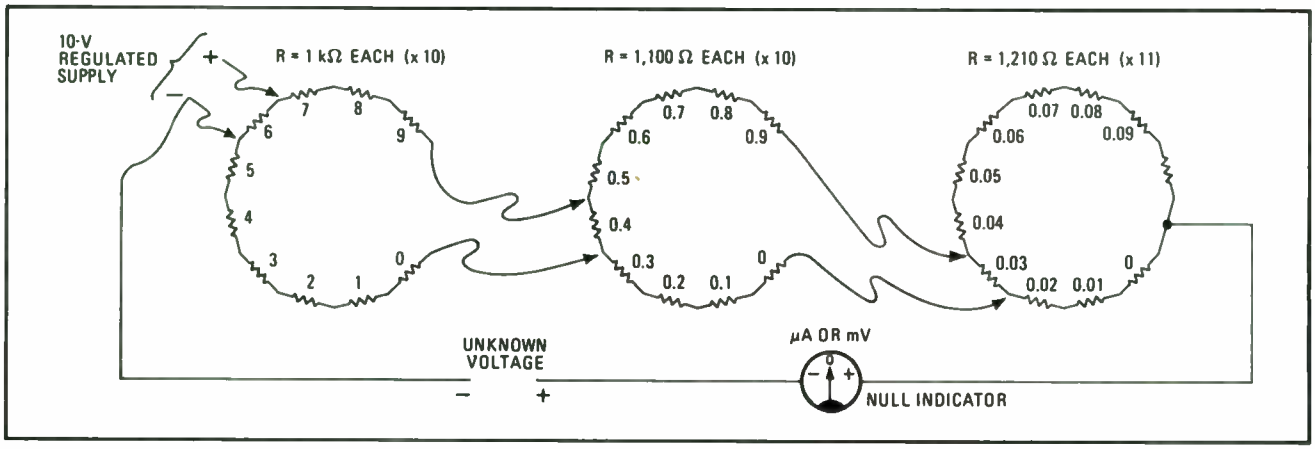
A bridge that provides precision dc voltages from 0 to 10 volts, in steps of 0.01 V, can be easily and economically realized with a "circular" voltage divider. In this uncomplicated divider arrangement, the point from which the output is taken remains fixed, while the voltage source is moved from one point to another.

In a conventional voltage-divider setup, the fixed voltage is applied across the entire network, and the output voltage is taken from a selectable tap. This approach, however, may involve complex switching and usually requires a large number of resistors, which is undesirable because precision resistors are expensive.

As shown in the diagram, a total of only 31 resistors is needed to provide a settability to within 0.01 V. Each ring has 10 resistors, except the last, which contains 11. The value of the resistors in a given ring must be 1.1 times the value of the resistors in the preceding ring. The bridge in the illustration is set up to produce an output of 6.43 V.

The tighter the tolerance of the resistors, of course, the more accurate the output voltage can be. And the more sensitive the null indicator is, the more closely the bridge output can be read. As lower-value resistors are used, the bridge output impedance becomes lower.

The principal limitation of this arrangement is the allowable power dissipation of the resistor in the first ring across which the full supply voltage is applied. □



Dial a voltage. Circular resistor arrangement trims resistor count without sacrificing precision. The output voltage of this bridge can be set from 0 to 10 volts, to within 0.01 V. All resistors in the same ring have the same value, which is 1.1 times larger than the value of the resistors in the preceding ring. Resistors in the first ring must be able to withstand the full supply voltage. Just 31 resistors are used here.

8. Clock circuits

Micropower comparators generate 2-phase clock

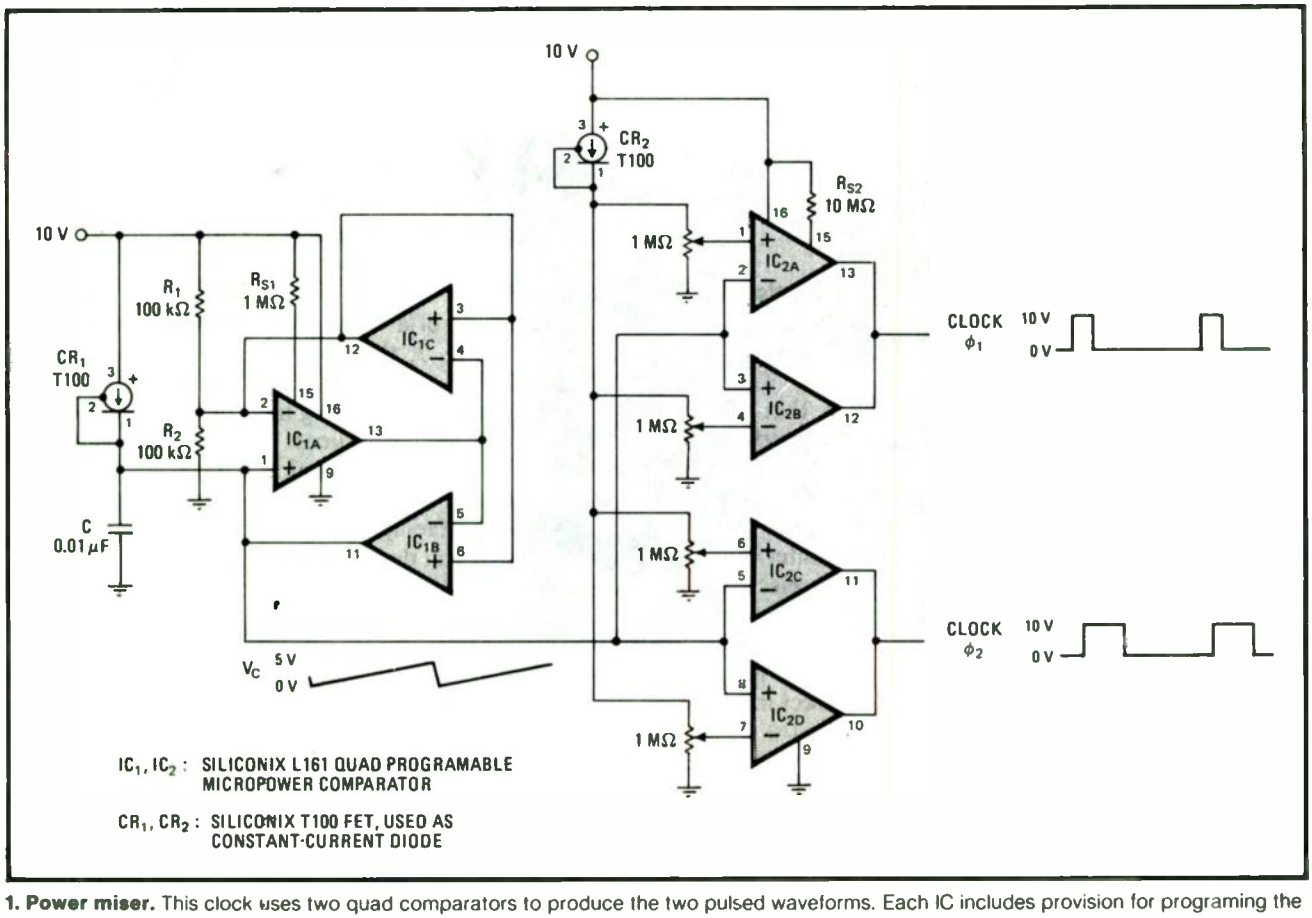
by Norman G. Wheelock
Siliconix Inc., Santa Clara, Calif.

A versatile two-phase clock generator that uses two L161 quad micropower comparators provides signal outputs with variable phase and variable pulse widths. The entire circuit draws only 300 microamperes from a 10-volt supply. The 3-milliwatt power consumption allows the circuit to be used in a broad variety of applications such as time-delay generators, logic sequencers, hand-held signal injectors, and other systems where a multiphase clock is required.

The waveforms in Fig. 2 illustrate circuit operation. As a ramp generated by the first L161 increases in amplitude, the outputs of two window comparators, which are formed by the second L161, rise and fall. A rise occurs when the lower limit of the window comparator is crossed, and the fall comes when the upper limit is reached. The upper and lower limits of the window comparators are variable throughout the full voltage range of the ramp. Variations in the upper and lower limits of the window comparators allow for change in pulse widths and relative phase of the signal outputs.

The actual circuit diagramed in Fig. 1 is composed of two sections: a ramp generator, formed by three of the four comparators on IC_1, and two window comparators, formed by IC_2. The operating speed and power consumption of the comparators are set by the value of the resistor R_s between the power supply and pin 15 of the integrated circuit; each comparator draws 5 V_{sup}/R_s, and a bias circuit draws V_{sup}/R_s, so the total current is 21 V_{sup}/R_s. The 210 μA drawn by IC_1 provides moderately fast operation of the comparators in that IC, and the 21 μA set for IC_2 limits its comparators to slow switching.

The ramp-generation circuit is controlled by the charging of C by a constant-current diode, CR_1. When the charge on C reaches the voltage of pin 2 of IC_{1A}, IC_{1B} is turned on, and C is quickly discharged. IC_{1C} is also



1. Power miser. This clock uses two quad comparators to produce the two pulsed waveforms. Each IC includes provision for programing the current drawn by the comparators, and thus controls their speed. Clock frequency is 100 Hz to 100 kHz.

turned on at the discharge point, grounding the reference pin. This action provides a form of positive feedback such that IC_{1B} is prevented from being turned off as the charge on C falls below the reference level at pin 2.

The time T during which the ramp charges is:

$$T = CV_{ref}/I$$

where I is the current provided by CR_1 (30–48 microamperes), V_{ref} is the reference voltage on the inverting input of IC_{1A} (5.0 v), and C is the value of the capacitor charged through CR_1.

Because the comparator used to generate the ramp has its supply current programed to provide moderate switching speeds necessary for quick discharge of C, the discharge time is negligible. Therefore, the rate, f, at which the ramp cycles is effectively:

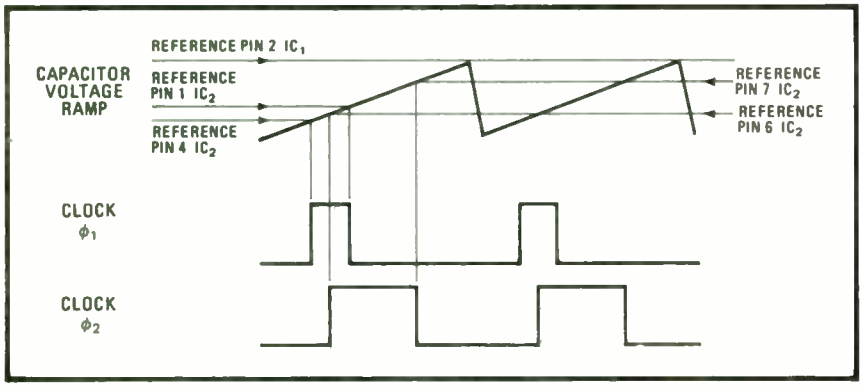
$$f = I/CV_{ref}$$

This frequency is set by choosing the value of C, and it can be trimmed by adjusting V_{ref}, if necessary.

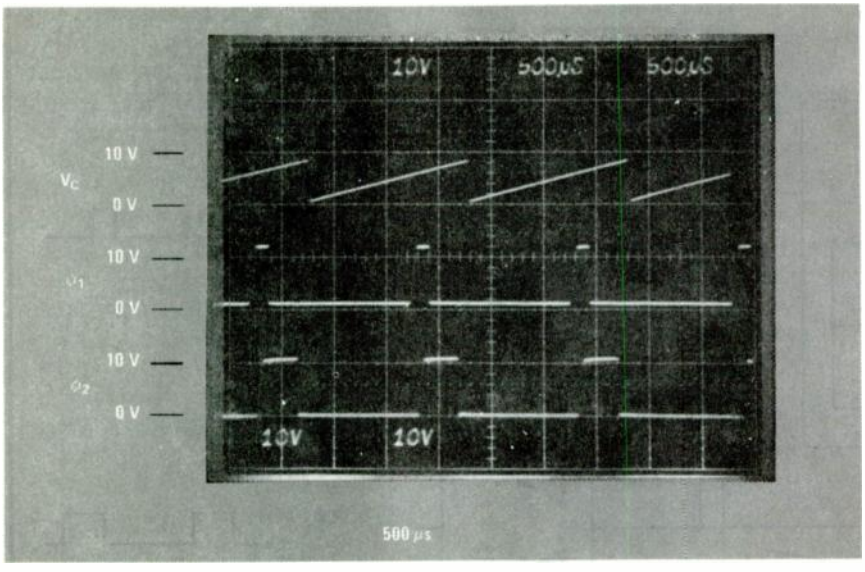
The remaining portion of the circuit is composed of two classic window comparators. Upper and lower limit references are provided by a second current-reference diode (CR_2) and several potentiometers. The comparators in the circuit are programed for slow switching to prevent signal output during the discharge period of C.

Most of the current to the circuit is drawn by IC_1 (210 μA). IC_2 consumes 21 μA and the current-reference diodes a total of 60 μA. The remaining current flows through the resistor network that provides reference voltage for IC_{1A}. The total current delivered to the circuit (341 μA) is a factor of 100 smaller than that required by nonprogramable comparators.

The T100 field-effect transistors that are used as constant-current diodes also contribute to circuit economy, passing less than an eighth of the currrent of conventional constant-current diodes. They have a temperature coefficient of only about 82 nA/°C. □



2. Go in and out the windows. Two clock signals, with independently variable widths and variable relative phase, are generated by setting the reference levels of two window comparators driven by a voltage ramp. A biphase clock finds application in various logic systems.



3. Picture this. Scope photo shows linear voltage ramp across capacitor, plus output pulse trains of the two clock signals, from circuit of Fig. 1. Calculated frequency, for 35-μA charging current and 5-V ramp height, is 70 kHz; waveforms indicate about 67 kHz. Note complete absence of unwanted glitches in clocks' waveforms during capacitor discharge.

Multiphase clock produces nonoverlapping pulses

by Glen Coers
Texas Instruments, Components Group, Dallas, Texas

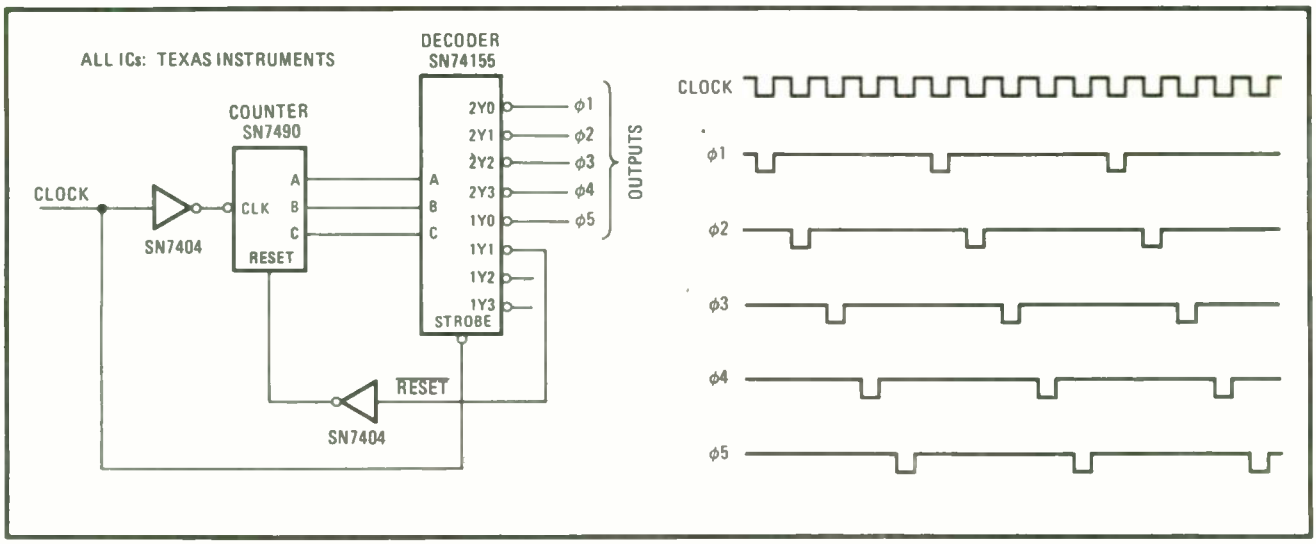
A multiphase clock pulse generator can be put together from a few IC packages by taking advantage of the versatility of an MSI TTL decoder/demultiplexer. The clock generator can be programed to produce from two to seven differently phased clock-pulse trains, and none of the pulse edges will overlap. Furthermore, the time between the pulses of the various clock phases is the same as the width of a single pulse. This means that each individual clock phase is well-defined, and there is no pulse-edge ambiguity, as with other clock-generating techniques.

An MSI decade counter is used with the MSI decoder/demultiplexer, which is connected as a three-line-to-eight-line decoder. Only three of the outputs of the decade counter are needed.

The number of clock phases is determined by the decoder output that is selected to reset the counter to zero. The counter's reset line is simply connected to the decoder's output line that is next in the sequence. As shown in the figure, a five-phase clock is produced by wiring the counter-reset line to the sixth decoder's output line.

The inverter at the input of the counter assures that the decoder is disabled when the count is changing and enabled after the data has stabilized. This eliminates the transients that can appear on the decoder's output lines when the counter is changing states. □

Programable clock. Two MSI devices—a decade counter and a three-line-to-eight-line decoder—can be wired as a simple multiphase clock generator. The circuit can produce from two to seven clock phases without any overlapping pulse edges. The number of clock phases is determined by connecting the counter's reset line to the decoder output line that is next in sequence. A five-phase clock is shown here.



Oscillator drives digital clock when ac power fails

by Robert C. Moore
Applied Physics Laboratory, Johns Hopkins University, Silver Spring, Md.

Including an oscillator in the design of a digital clock can keep the clock going during an interruption of the ac power. When ac power is present, the clock is driven by 60-hertz pulses that are generated from the 15.36-kilohertz oscillator and synchronized by the ac line. If the ac power is interrupted, a standby battery keeps the oscillator running to drive the clock. When ac power returns, the circuit automatically resynchronizes to the line frequency, giving excellent long-term stability.

The circuit that drives the clock chip uses two complementary-MOS integrated circuits—a 74C04 hex inverter and a 14520 dual hexadecimal counter (Fig. 1). Two of the inverters from the 74C04 are connected to form a

Schmitt trigger pulse-shaping amplifier with 4.5-volt hysteresis.

The Schmitt trigger drives another inverter, connected as a 40-μs one-shot to generate a 60-Hz master reset pulse that is synchronous with the ac line. The remaining three inverters in the 74C04 are used as a 15.36-kHz oscillator to drive the 14520 dual hexadecimal counter. The 14520 divides the 15.36 kHz by 256 to obtain 60 Hz for driving the 5314 clock chip. This counter should overflow 60 times a second.

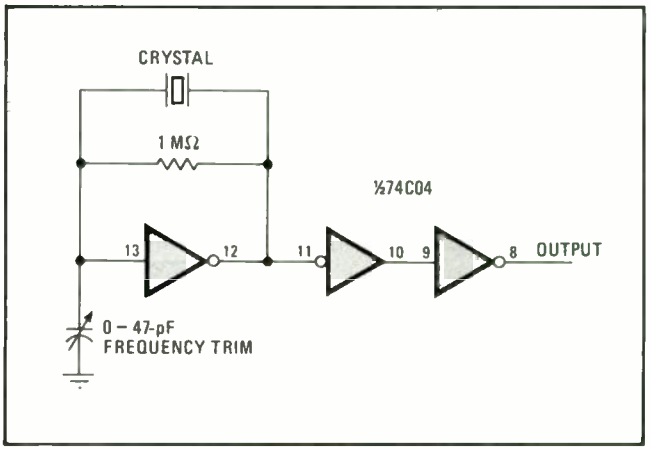
To ensure that the 14520 overflow is synchronous with the 60-Hz line, the counter is reset to zero once each cycle of the line. If ac-line power is interrupted, the counter simply runs free at its rate of nearly 60 Hz until line power is restored. When power is restored, the reset pulses again synchronize the counter to the ac line. All circuit operation is completely automatic and free from transients.

The dc output from the rectifier bridge supplies power to the C-MOS ICs, the clock chip, and the display device (not shown in Fig. 1). The dc current also trickle-charges the standby battery. During an ac interruption, however, the battery does not deliver power to the display circuit. To limit battery drain, the opposing 1N4001 diode prevents current from flowing to the display; therefore the display is dark while the ac power is off.

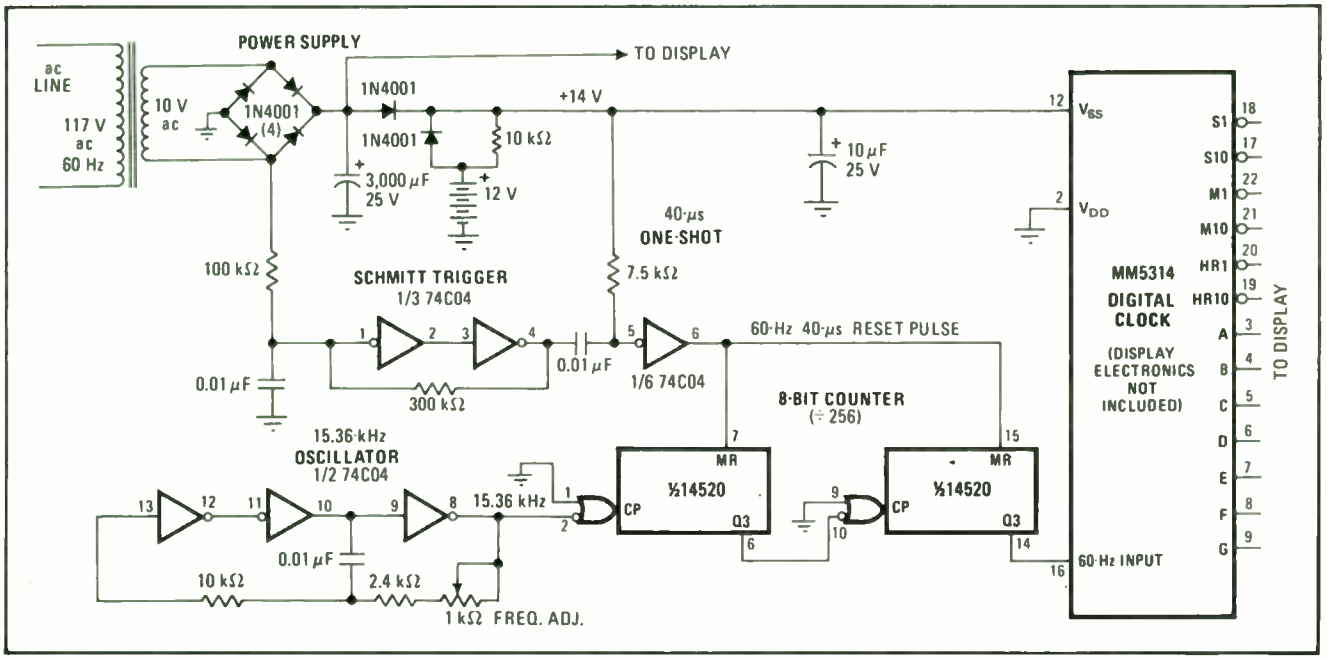
A frequency-trimming potentiometer is included in the oscillator circuit. This 10-turn pot can be adjusted by a screwdriver while the oscillator output or counter output is being checked on a frequency meter, or it can be merely touched up if the clock is gaining or losing time in the course of a few days.

To improve short-term frequency stability during power outages, a crystal-controlled 15.36-kHz oscillator should be substituted for the RC circuit shown in Fig. 1. The number of bits in the counter may be increased if a higher crystal frequency is desirable.

Figure 2 gives details of the crystal-controlled oscillator design. The crystal frequency must be an integral multiple of 15.36 kHz, and the oscillator circuit of Fig. 2 must be followed by a divide-by-N counter, where N is the crystal frequency divided by 15.36 kHz. For example, if a 4017 divide-by-10 counter were to be used, the crystal frequency would be 153.6 kHz. Similarly, if the counter were a 4024 (divide by 128), the crystal frequency would be 1.96608 MHz. The master reset pin of the counter should be connected to the reset pulse. □



2. Better time. Crystal-controlled oscillator provides better frequency stability during power outages than the RC oscillator shown in Fig. 1. Frequency must be a multiple of 15.36 kHz, and oscillator must be followed by appropriate divider/counter to provide 15.36 kHz into the 14520 8-bit counter that drives the clock chip.



1. Good time in blackout. Two C-MOS circuits enable digital clock to continue accurate time-keeping during interruptions of ac power. In normal operation, 60-Hz output of divide-by-256 counter is phase-locked to ac line. Counter output runs free at its rate of nearly 60 Hz during power interruption, drawing power from rechargeable standby battery. Display is not powered during battery operation.

TTL interface circuit synchronizes computer clock

by Jim Crapuchettes
Stanford University Medical Center, Stanford, Calif.

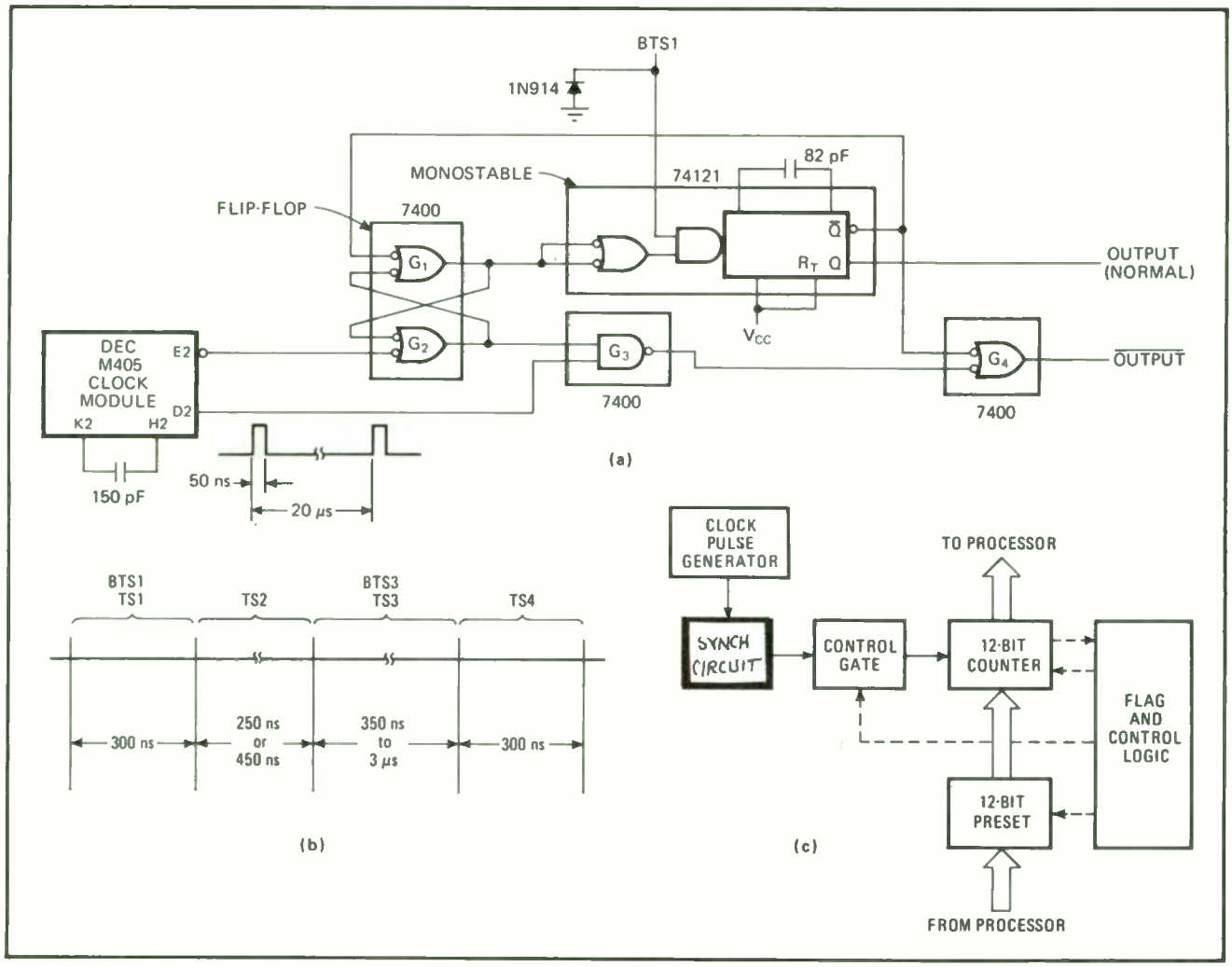
A clock-synchronization circuit for computer interfacing allows the counter of a continuously running real-time clock to be read by the computer when the counter is not changing. The circuit requires only two TTL IC packages. The normal approach is to use complicated circuits requiring a latch or flip-flop for each bit of the clock counter.

There are only two restrictions on the two-IC clock-synchronization circuit: the computer processor must have time states available for the circuit, and the longest cycle time for the processor must be shorter than the period between two successive pulses from the system's clock-pulse generator.

Essentially, this simple circuit (a) forces the clock into synchronization with the processor, rather than trying to synchronize the processor with the clock. This is done by letting the contents of the clock counter be changed only during that portion of the processor cycle in which the counter cannot possibly be read by the processor.

This particular synchronization circuit is designed for the PDP-8/E minicomputer with an external I/O bus option, which is made by Digital Equipment Corp. of Maynard, Mass. The circuit can also work directly from DEC's Omnibus bus design, and it can be applied directly to DEC's PDP-8/I, PDP-8/L, and PDP-12 minicomputers.

The processor cycle, which is drawn in (b), is split into four time states, TS1 through TS4. Two of these time states, TS1 and TS3, are brought out from the processor



Reading out data. Synchronization circuit (a) forces real-time counter clock to be in step with computer processor so that data is read only when the counter is not changing. The delay, time state TS2, in the processor's timing cycle (b) between counter changes (TS1) and the execution of I/O instructions (TS3) is used. Block diagram (c) of real-time clock indicates where sync circuit goes.

on the I/O bus as buffered time states, BTS1 and BTS3. All I/O instructions are actually executed during TS3, and there is a minimum delay of 250 nanoseconds between TS1 and TS3. Therefore, as long as the contents of the clock counter changes only during TS1 and all carries across the counter are finished in less than 250 ns, the counter changes and the computer readouts cannot overlap. The diagram (c) of the system's real-time clock shows the circuit's location.

A pulse from the clock-pulse generator sets the R-S flip-flop formed by gates G_1 and G_2. The next occurrence of time state TS1 (it may be occurring when the flip-flop is set) will trigger the monostable multivibrator. (The 74121 is used here because it produces a fixed-length pulse or none at all, contains part of the necessary gating, and has complementary outputs.) The diode, which is between the monostable and ground, prevents undershoot from the BTS1 line of the I/O bus.

The $\bar{Q}$pulse output from the monostable resets the flip-flop. To be sure that the flip-flop will always be reset, the duration of this $\bar{Q}$pulse must be longer than the duration of the pulse from the clock pulse generator. Since this clock pulse is 50 ns, an 82-picofarad capacitor is added to stretch the monostable pulse to about 100 ns.

The flip-flop has no provision for initialization to the reset state, but it will be set correctly within one cycle of the processor. Initialization is necessary only if the clock control gating is between the clock-pulse generator and the synchronization circuit.

Gates G_3 and G_4 are needed if the clock must continue to run even when the processor is in the halt (pause) state and if the processor does not halt in the time state used for clock counting. In the case of the PDP-8/E, the processor halts in TS1, so these gates are not needed.

When used, they cause the pulses from the clock generator to be gated directly to the circuit's output if the flip-flop is set. As soon as the processor returns to the run state, the flip-flop releases the pulse it has been holding, triggering the monostable and allowing the normal sequence to continue.

The correct number of pulses, therefore, always passes through the circuit, whether the processor is running or not. The only difference will be a long pulse period when the processor is halted and a short pulse period when it continues.

It should be noted that the same synchronization technique could be used with a computer that has only one time state brought out to peripherals. The trailing edge of that time state could be used to trigger a monostable whose output pulse would perform the same function as the BTS1 pulse of this circuit. □

Quad NAND gate package yields two-frequency clock

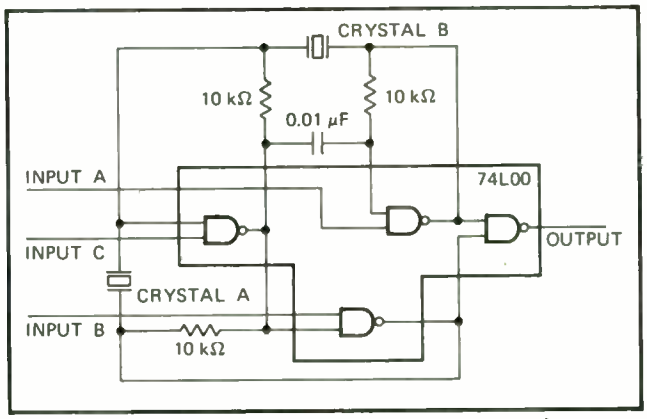
by Howard L. Nurse
Applied Technology Division, Itek Corp., Palo Alto, Calif.

Crystal-controlled clock oscillators generally require three logic gates to produce a single output frequency. This means that the fourth gate in the common quad-type gate package is not used. But, with just a couple of extra parts, that fourth gate can be put to work.

The two-frequency crystal clock in the diagram takes maximum advantage of a quad TTL NAND gate package with a minimum of external components. And this economical circuit can be remotely programed by grounding one of its three input lines.

With input A grounded, the circuit oscillates at the frequency of crystal A. With input B grounded, it oscillates at the frequency of crystal B. If input C is grounded, the circuit is inhibited.

The TTL-compatible output of this two-channel clock is a 40% square wave when either input A or input B is grounded. With the low-power TTL NAND-gate package used here, operating frequencies in excess of several megahertz can be achieved. □



Two for the price of one. Dual-frequency crystal-clock oscillator utilizes all four gates in a quad package, whereas conventional single-frequency oscillators make use of only three. This inexpensive circuit can be remotely programed by grounding input A to operate at the frequency of crystal A or by grounding input B to oscillate at crystal B's frequency. Grounding input C inhibits the circuit.

Generating overlapped clock phases for CCD array

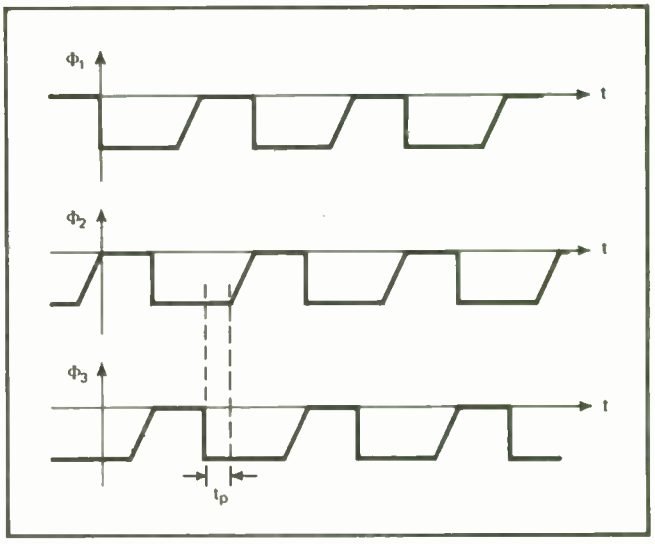
by Hans-Jörg Pfleiderer and K. Knauer,
Siemens AG, Munich, Germany

Arrays of three-phase charge-coupled devices require overlapped clock pulses (Fig. 1) for satisfactory operation. To generate these overlapped pulses, Fairchild Semiconductor, which produces the arrays commercially, suggests a rather complicated logic circuit in a report that it circulates.

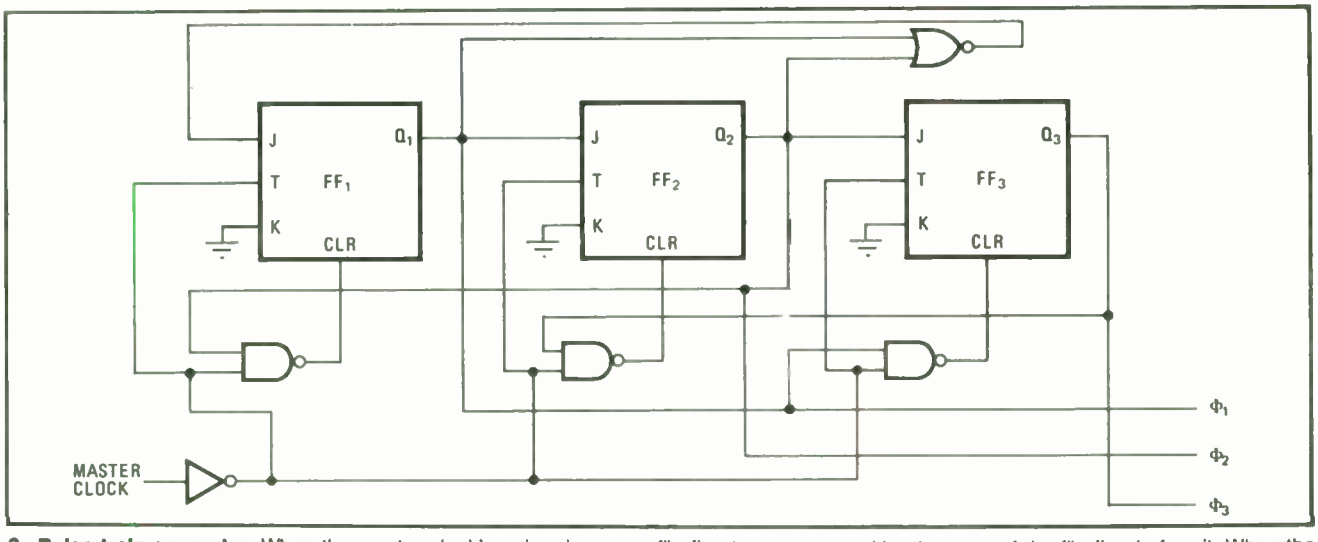
But a less complicated circuit (Fig. 2) can also generate the train of overlapped pulses, as shown in the timing chart (Fig. 3). When the master clock pulse goes high, J-K flip-flop FF_1 turns on only if the outputs Q_1 and Q_2 are both low. With FF_1 on, Q_1 rises, opening the gate so that the rise of the next master clock pulse turns on FF_2, without affecting FF_1. However, with Q_2 up, the fall of the master clock's pulse clears FF_1 via the CLR input of FF_1.

This approach—setting the output of each flip-flop high with the J input, provided the preceding flip-flop is already on, and setting it low with the clear input when the following flip-flop is on—is used for each of the three flip-flops. The width of the overlap is approximately equal to the width of the master clock's pulse, and the frequency of each waveform is one third that of the master clock's pulse. The circuit is self-correcting and also self-starting.

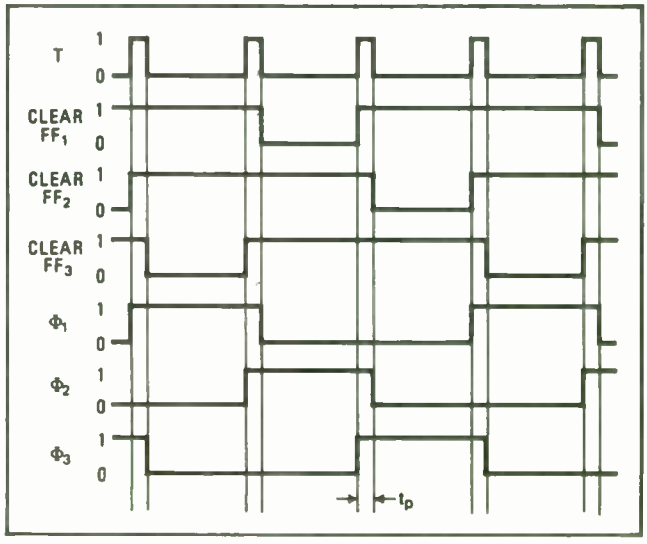
The same idea can also be used in driving the phase voltages for a two-phase CCD. □



1. Overlap. Arrays of three-phase charge-coupled devices require overlapping pulse trains for proper operation. The logic to produce these trains does not have to be complicated—it need not involve more than three flip-flops and a few gates.



2. Pulse-train generator. When the master clock's pulse rises, one flip-flop turns on, gated by the state of the flip-flop before it. When the pulse falls, the preceding flip-flop turns off, this time gated by the state of the following flip-flop.



3. Pulse timing. As the three flip-flops turn on and off (second, third, and fourth traces from top), their outputs overlap by the width of the clock pulse, minus circuit delays. The frequency of each waveform is one third that of the master clock's pulse.

9. Comparators

Phase comparator for servo loops

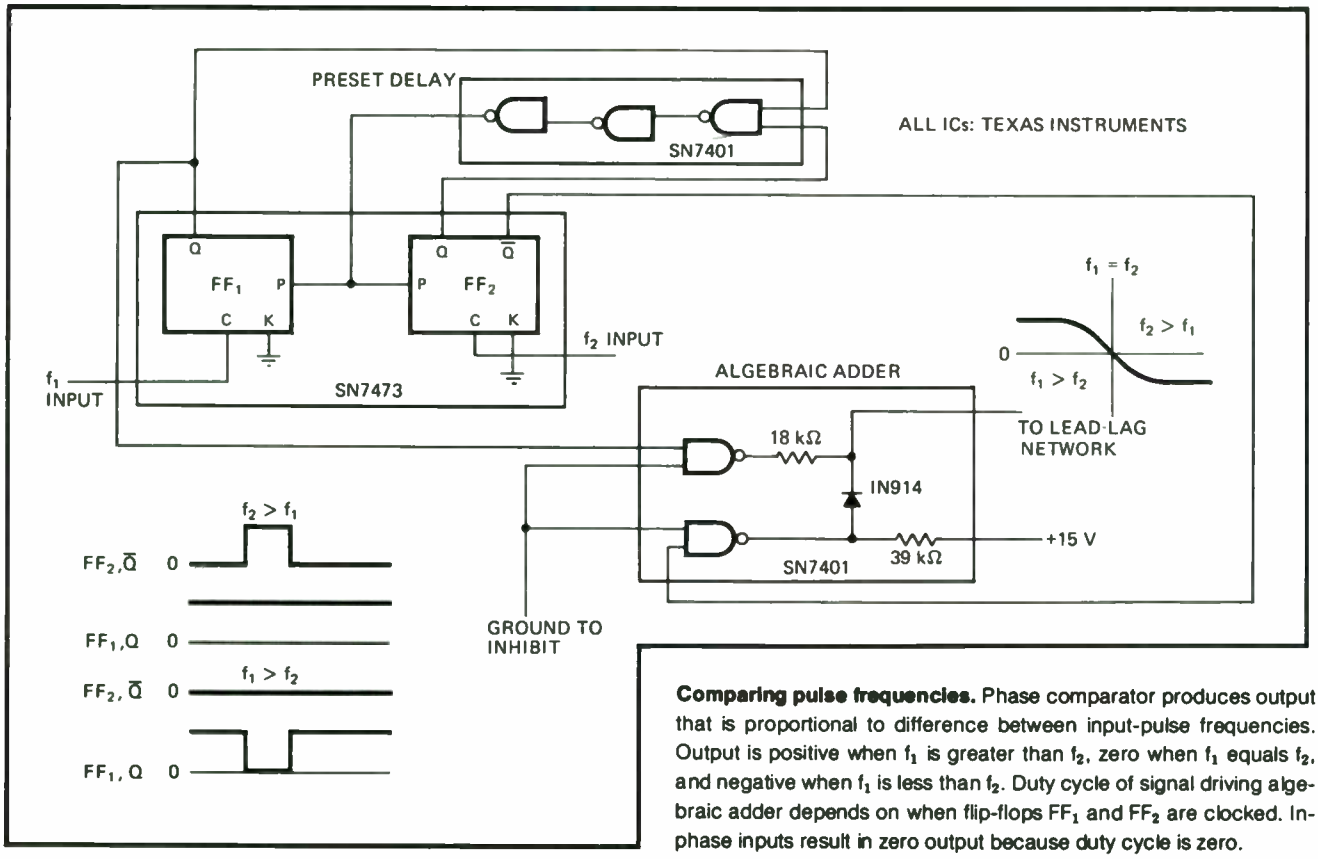
by Francis E. Adams
San Bernadino Microwave Society, Corona, Calif.

An easy-to-build phase comparator offers a number of advantages for use with dc servo motors and in voltage-controlled-oscillator loops. The output of the comparator is zero for inputs that are in phase, and, unlike the output of discriminators, it remains real, even for extreme differences in the two input-pulse frequencies. Moreover, the circuit, which is composed of low-cost, readily available ICs, can operate at a frequency that is limited only by the type of devices employed.

Both J-K flip-flops, FF_1 and FF_2, are preset so that their Q outputs are at logic 1. After an input pulse at frequency f_1 clocks FF_1 and causes its Q output to become logic 0, and an input pulse at frequency f_2 clocks FF_2 and produces a logic 0 at its Q output, the preset delay containing three NAND gates resets the flip-flops. The propagation delay time of these NAND gates assures that both flip-flops are preset.

The time lapse between FF_1 being clocked and FF_2 being clocked determines the duty cycle of the pulse train seen by the algebraic adder. As input pulse frequencies f_1 and f_2 approach each other, this duty cycle becomes smaller. When the two inputs are in phase ($f_1 = f_2$), the duty cycle is zero, except for a narrow contribution due to the preset time of the NAND gates, which is usually less than 1 microsecond.

If f_1 is greater than f_2, there is a positive output current that is proportional to the phase error. If f_2 is greater than f_1, then there is a negative output current, which is also proportional to the phase error. For $f_1 = f_2$, the output current is zero. □



Comparing pulse frequencies. Phase comparator produces output that is proportional to difference between input-pulse frequencies. Output is positive when f_1 is greater than f_2, zero when f_1 equals f_2, and negative when f_1 is less than f_2. Duty cycle of signal driving algebraic adder depends on when flip-flops FF_1 and FF_2 are clocked. In-phase inputs result in zero output because duty cycle is zero.

TTL gates speed up pulse-height analysis

by Joseph Laughter
University of Tennessee Medical Units, Memphis, Tenn.

Being used mainly for analyzing nuclear energy, determining white-noise amplitude, or counting blood cells, pulse-height analyzers require high-speed performance. They are complicated to design with discrete transistors. But with transistor-transistor logic and integrated comparators, fast operation can be realized at a fraction of the usual cost.

Positive dc voltage E_L is the lower limit for a pulse passing from input to output, and positive dc voltage E_U is its upper limit. At the instant the input pulse rises above E_L, lower-level comparator A_1 switches to zero, triggering monostable multivibrator OS_1. The output of OS_1 returns to zero after about 300 nanoseconds and triggers monostable OS_2, sending a 60-ns pulse to the anti-conic gate. The anti-conic gate inverts the pulse and triggers the output pulse shaper (monostable OS_3).

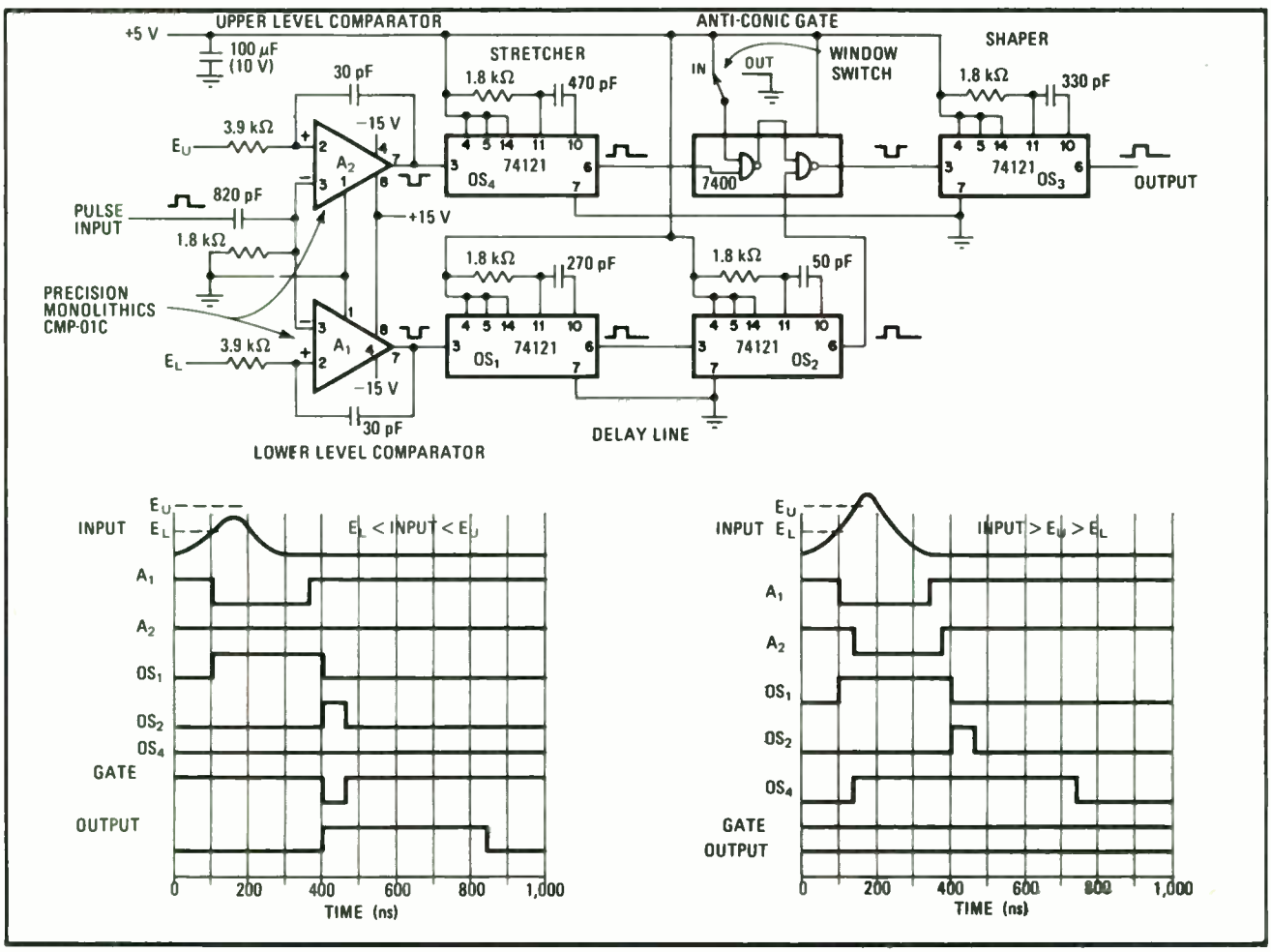
When input pulse height is greater than E_U, comparator A_1 is fired first, and then upper-level comparator A_2 is fired. Once A_2 switches on, the pulse stretcher (monostable OS_4) produces a positive pulse that turns off the anti-conic gate for 600 ns. Therefore, when the pulse from monostable OS_2 appears several nanoseconds later, it is blocked by the anti-conic gate and there is no output. Throwing the window switch to its "out" position disables the anti-conic gate, allowing a pulse to reach the output each time the input pulse exceeds the lower-level limit voltage.

This pulse-height analyzer can accept positive pulses having a maximum rise time of 250 ns and a maximum repetition rate of 500,000 pulses per second. The repetition rate can be increased by using lower-value timing capacitors for delay line OS_1, output pulse shaper OS_3, and pulse stretcher OS_4. However, input rise time requirements become more stringent.

The type CMP-01C comparators can be replaced by the more popular type 710 comparators if the supply voltage is changed from ±15 volts to +12 and −6 v. Although the type 710 is considerably cheaper, it does not perform as well in critical applications.

Timing curves show output wave forms for several important points in the circuit. □

Examining pulse height. Comparators A_1 and A_2 set lower (E_L) and upper (E_U) voltage limits. When pulse height exceeds E_L, one-shots OS_1 and OS_2 slow down pulse from A_1 and transmit it to anti-conic gate, which fires output pulse shaper OS_3. When input exceeds E_U, A_1 and A_2 switch, causing pulse stretcher OS_4 to turn off gate so that pulse from OS_2 cannot reach output. Window switch at "out" disables gate.



One-shot/flip-flop pairs detect frequency bands

by Edward E. Pearson
Opelousas, La.

A retriggerable monostable multivibrator and a type D flip-flop can form a simple reliable frequency comparator that senses if an input frequency is greater than or less than a predetermined reference. Connecting additional comparators in parallel, together with AND logic, permits the detection of input frequencies that fall within selected bands.

Both the one-shot and the flip-flop are wired for positive edge triggering. Each input pulse causes the monostable's output to go high for the period of its preset timing interval. The flip-flop is triggered simultaneously, but its output is determined by the state of its D input at the time of trigger threshold.

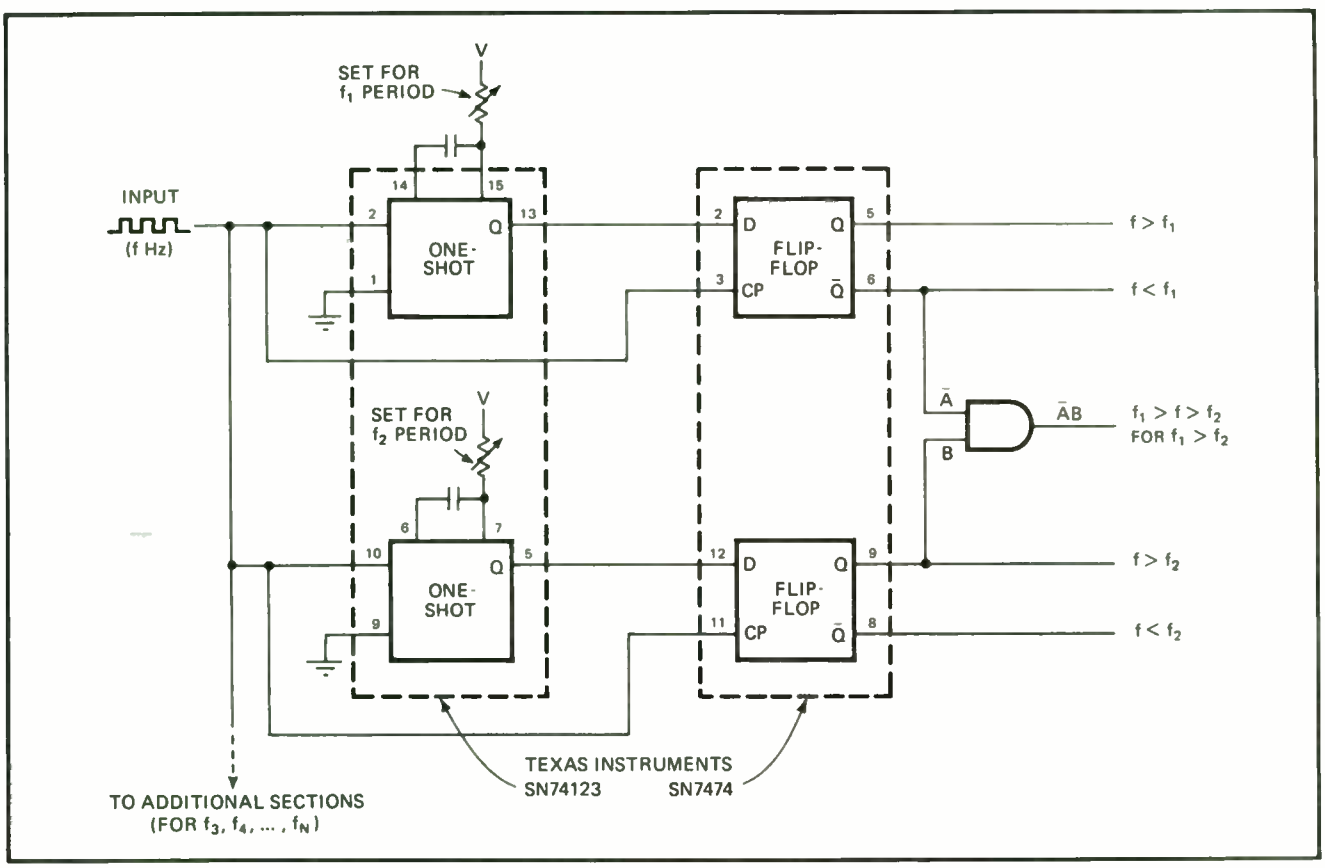
If the period of the input frequency is shorter than the preset timing of the monostable, a constant high level will be present at the D input, forcing the flip-flop's Q output to remain high. If the input frequency period becomes greater than that of the monostable, the D input will go low prior to the next incoming trigger. The flip-flop's Q output then goes low and remains low until the input period becomes shorter than that of the monostable.

To determine whether an input frequency (f) falls between two known frequencies, f_1 and f_2, two one-shot/flip-flop combinations are required, as shown. The top pair of devices detects an input greater or less than f_1, while the bottom pair detects an input greater or less than f_2. The AND gate provides a high output when the input frequency lies inside the preset band (less than f_1 or greater than f_2, if f_1 is greater than f_2). This detection scheme can be expanded to include any desired number of segments within the operating passband.

The frequency band detector also has an inherent memory function that could be particularly useful in control applications. When the input signal terminates, for example, with a tone burst, no trigger is available to the flip-flops, and all outputs remain static until the input signal returns.

Although the detector responds only to the period of the input signal and does not require the input to maintain a specific duty cycle, input pulses must have a rapid rise time. All trigger thresholds must be reached within an interval that is appreciably less than the monostable's propagation delay time. Circuit speed is limited only by the setup and hold performance of the components being used. □

Sensing frequency. Retriggerable one-shot and flip-flop compare frequency of input to preset reference frequency. To form frequency-band detector, two frequency comparators and AND gate are needed. Depending on period of input pulse train, each one-shot output is high or low. Each flip-flop triggers to level seen by its D input prior to trigger threshold. AND gate output goes high when f falls between f_1 and f_2.



Simple logic circuits compare binary numbers

by Edward J. Murray
Inter-Computer Electronics Inc., Lansdale, Pa.

In real-time data acquisition applications, determining the relative magnitude of two binary numbers with hardware, rather than software, now requires only three logic modules if data is being transferred serially. Previously, rather complex circuitry was needed.

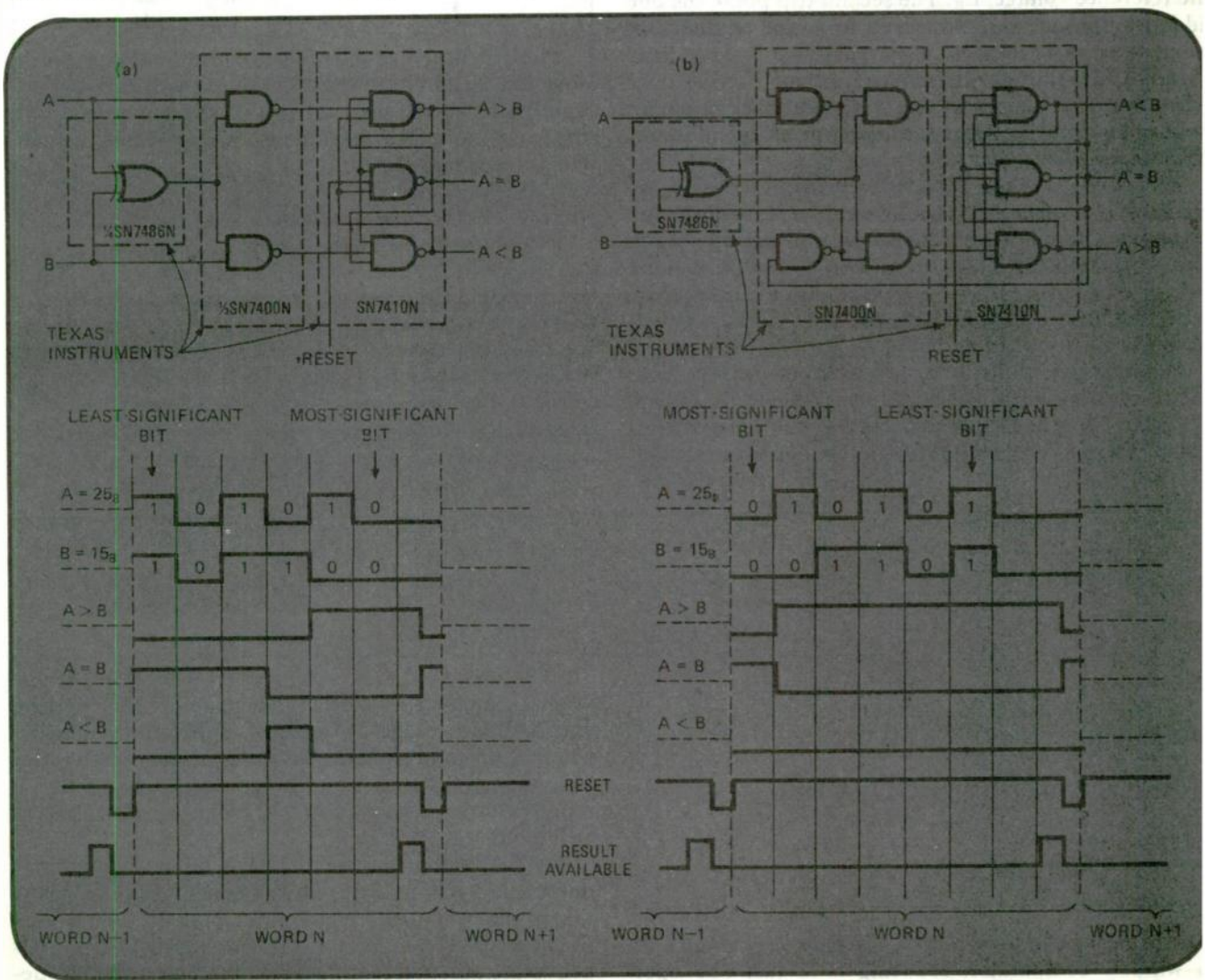
Only the most-significant difference between two coincident serial data streams defines their relative magnitude. If the least-significant bit is transmitted first, the last difference between coincident word bits determines which is the largest word. When the most-significant bit is the first transmitted, the first difference establishes relative magnitude, and all other differences can be ignored.

Six logic gates (a) can compare two words when the least-significant bit is the initial input. Eight logic gates (b) are needed when the most-significant bit arrives first. The heart of both schemes is a three-state latch that provides three comparisons for input words A and B: A is greater than B, A equals B, and A is less than B.

The timing diagrams in (a) and (b) illustrate circuit operation when input A is octal number 25 (binary 010101) and input B is octal number 15 (binary 001101). Signals A and B are not limited to a fixed number of bits per word. Any variable word size can be used if the results are interrogated after the word has been transmitted and a reset pulse precedes the word being interrogated.

This type of binary comparator is useful in preliminary data sorting and number ranging prior to software processing for multi-channel data acquisition. In the timing diagram, the "result available" waveform indicates the best interrogation periods.

Checking number size. To find relative magnitude of serial words A and B, only most-significant differences between coincident data bits must be considered. Transmitting least-significant bit first (a) requires six gates for comparison. Two additional gates are needed (b) if most-significant bit is transmitted first. In timing diagrams, octal 25 (binary 010101) is compared to octal 15 (binary 001101).



Varying comparator hysteresis without shifting initial trip point

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz.

An operational amplifier is a convenient device for analog comparator applications that require two different trip points. The addition of a positive-feed-back network will introduce a precise variable hysteresis into the usual comparator switching action.[1] Such feedback develops two comparator trip points centered about the initial trip point or reference point.

In some control applications, one trip point must be maintained at the reference level, while the other trip point is adjusted to develop the hysteresis. This type of comparator action is achieved with the modified feedback circuit shown in the figure.

Signal diode D_1 interrupts only one polarity of the positive feedback supplied through resistor R_2. Hysteresis, then, is developed for only one comparator state, and one trip point remains at the original level set by the reference voltage, E_R. The second trip point, the one added by hysteresis, is removed from the original trip point by:

$$\Delta V = R_1(V_Z - E_R)/(R_1 + R_2)$$

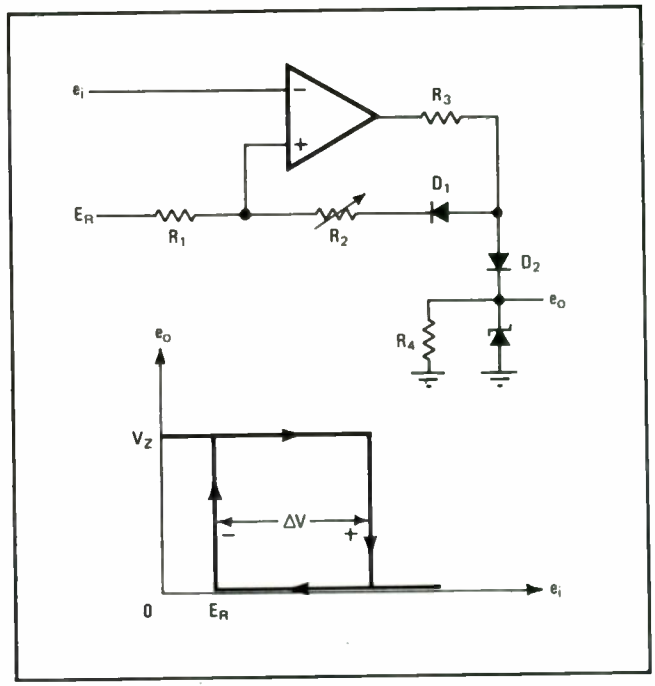
where V_Z, the zener voltage, is greater than reference voltage E_R. Varying resistor R_2 will adjust the hysteresis without disturbing the trip point at E_R.

The circuit's other performance characteristics are similar to the common op-amp comparator circuit. The accuracy of both trip points is determined by the op amp's input offset voltage, input bias current, and finite gain. Resistor R_3 limits the current drain through the zener diode, and resistor R_4 provides a discharge path for the capacitance of diode D_2.

The output signal can be taken either directly from the op-amp output or from the zener diode, as shown. With the latter hookup, the output signal voltage alternates between zero and zener voltage V_Z, which might be desirable for interfacing with digital logic circuits. It should be noted, however, this output cannot sink current in the 0-volt state.

Switching speed is determined by the op amp's slewing-rate limit for high-level input-drive signals. When the input drive is a low-level signal, the output rate of change is limited by the gain available to multiply the input signal's rate of change. Both the slew-rate limiting and the gain limiting of switching time are eased if phase compensation is removed from the op amp. □

REFERENCE:
1. G. Tobey, J. Graeme, and L. Huelsman, "Operational Amplifiers: Design and Applications," McGraw-Hill, 1971.



Controllable hysteresis. Positive feedback circuit for analog op-amp comparator does not shift the initial reference trip point while introducing hysteresis in the second trip point. The voltage difference, ΔV, between the trip points can be adjusted by varying resistor R_2. When the output voltage is taken from the zener diode, as shown, it switches between zero and V_Z, the zener voltage.

Window comparator needs only one op amp

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz.

Diode gating can considerably simplify the circuitry for a window comparator, reducing it to just one operational amplifier, a single voltage reference element, and a diode bridge. A window comparator indicates whether or not a signal is within a given voltage range for applications such as go/no-go testing. Normally, it requires two op amps and two voltage references, as well as an AND gate.

A signal within the comparator's defined range produces a low output state, while a signal above or below that range produces a high output state. In the conventional window comparator, one op amp detects signals above the acceptable range, and the other op amp de-

tects signals below the range,[1] by comparing the signal against separate voltage references. To provide a single comparator output, the signals from the op amps are combined by an AND gate.

For applications where moderate accuracy, say 1%, is acceptable, the circuit shown here can be used. Since only one op amp is required, there is no longer any need for a gate to combine the outputs from two op amps. Also, the same reference element, a zener diode, now serves to define both the upper and lower voltage limits. Because of this common reference element, the upper and lower limits will be well-matched about zero. For limits not centered about zero, the center of the range can be shifted by connecting bias resistors from the power-supply voltages to the appropriate amplifier input.

Through diode gating, the input signal is directed to the proper amplifier input. Input signals above the positive limit forward-bias diode D_1, pulling the zener voltage upward so that diode D_2 is also forward-biased. A positive voltage is now applied to the noninverting input of the amplifier, causing this device's output to swing to its positive state. The upper range limit, therefore, is the zener voltage plus two forward diode drops ($V_Z + 2V_F$).

A positive output swing is also produced by negative input signals that exceed $-V_Z - 2V_F$. These negative signals will forward-bias diodes D_3 and D_4 so that a negative signal appears at the amplifier's inverting input. Signals within the range defined by the positive and negative voltage limits are not passed by the diode bridge to the amplifier, and the amplifier's output is negative because of the bias voltage from resistor R_1.

The accuracy of this comparator is controlled by the diode voltages at low input frequencies and by the amplifier's gain-bandwidth limit at high input frequencies. Since both the zener and diode voltages are subject to tolerance and temperature variations, the range limits can be in error by several percent. To reduce the temperature sensitivity of the range limits, resistors R_2 and R_3 bias the zener so that its thermal voltage variation approximately cancels those of two junction diodes. (The dc voltage shift introduced by resistor R_1 adds to the amplifier's offset voltage error, making this offset error comparatively small.)

At high input frequencies, the comparator error is dominated by the gain-bandwidth-limited output swing of the amplifier from its positive state to its negative state. This transition occurs when the input signal is disconnected from the amplifier by the diode bridge, leaving only the small voltage developed by resistor R_1 at the amplifier's noninverting input. The limited input drive voltage to the amplifier results in a slow output fall time.

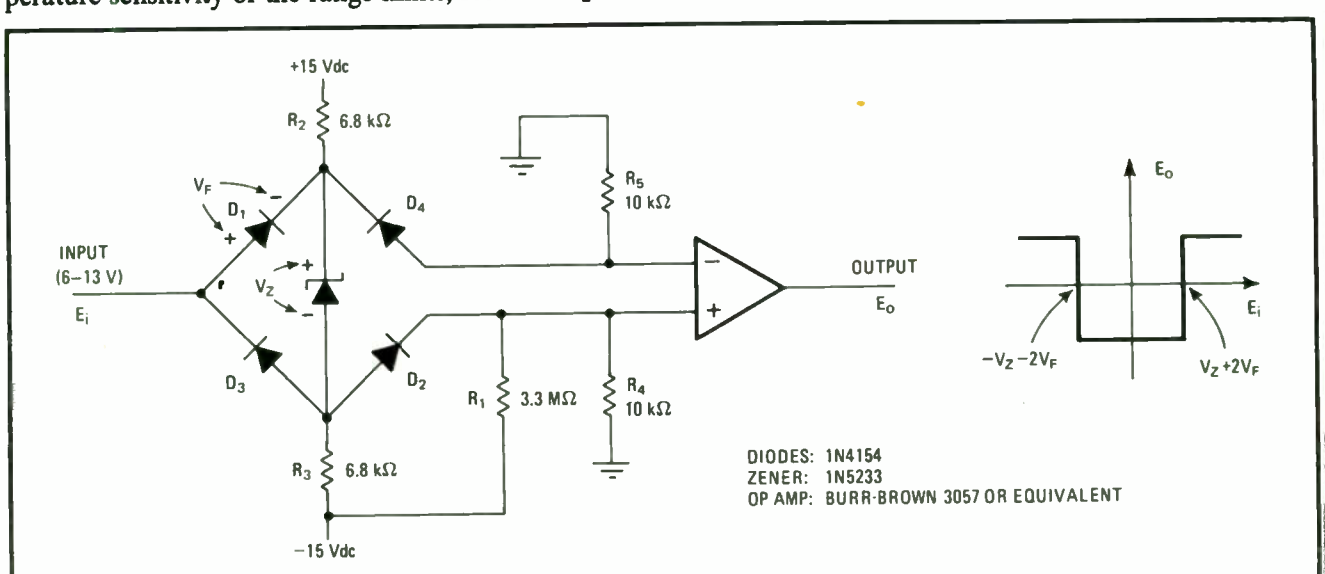
If a compensated op amp is being used in the circuit, its gain-bandwidth product can be improved by removing the device's phase compensation. Or, an uncompensated op amp can be used instead, as is done here. With the uncompensated op amp shown, the window comparator will have a bandwidth of 2 kilohertz and an ac error of only 1%.

There are a couple of other response limitations that should be considered. They are the amplifier's overload recovery delay and the discharging time of the diode capacitances. In order to switch, the amplifier must first recover from its saturated condition—this introduces a time delay. Fortunately, removing the phase compensation from most op amps shortens their overload recovery time.

Another switching delay can be produced by the capacitance discharging time of diodes D_2 and D_4 through resistors R_4 and R_5, respectively. This factor, along with the input resistance, is determined by one of these resistors shunted by either resistor R_2 or R_3. □

REFERENCE

1. "Applications of Operational Amplifiers—Third-Generation Techniques," J. Graeme, McGraw-Hill Inc., 1973.



Saving an op amp. Window comparator for moderate-accuracy applications can be built with only one op amp. The zener diode and the diode bridge determine the circuit's voltage limits, directing positive and negative signals to the appropriate amplifier input. The circuit's output is low for signals within the defined range. D_1 and D_2 conduct for positive signals, while D_3 and D_4 conduct for negative signals.

Single op amp compares bipolar voltage magnitudes

by F.N. Trofimenkoff and R.E. Smallwood
University of Calgary, Alta., Canada

The operational-amplifier bridge circuit shown in Fig. 1 is a window comparator for bipolar signals. It indicates when the magnitude of the input signal exceeds a preset value. Selection of resistor values sets positive and negative trigger levels independently, so that the trip levels for the two polarities need not be the same.

To analyze the circuit, first ignore the output clamping diode. The input diodes isolate one of the two signal paths, depending on the polarity of e_i. For e_i positive:

$$e_o = -(e_i - e_d)(R_2/R_1) - e_r(R_2/R_3)$$

where e_d is the voltage drop across the diode when it conducts. For e_i negative:

$$e_o = (e_i + e_d)\frac{[1+(R_2/R_3)+(R_2/R_6)]}{[1+(R_4/R_5)]} - e_r(R_2/R_3)$$

The switch-over points are defined by setting $e_o = 0$ in each of these expressions. For e_i positive:

$$(e_i - e_d) = e_r(R_1/R_3) \qquad (1)$$

and for e_i negative:

$$(e_i + e_d) = \frac{-e_r[1+(R_4/R_5)]}{[1+(R_3/R_2)+(R_3/R_6)]} \qquad (2)$$

If the positive and negative trip levels must have the same magnitude, then the coefficients of e_r in equations (1) and (2) are equal. The equality reduces to:

$$[1+(R_3/R_2)+(R_3/R_6)] = [1+(R_4/R_5)](R_3/R_1) \qquad (3)$$

If the switching levels are different, equations (1) and (2) must be used to determine the resistor ratios. But regardless of the levels, R_2 is very large and may even be infinite—that is, the circuit may have an open-loop configuration—to provide the maximum gain and thereby produce a sharp transition between the output states at the switch-over points.

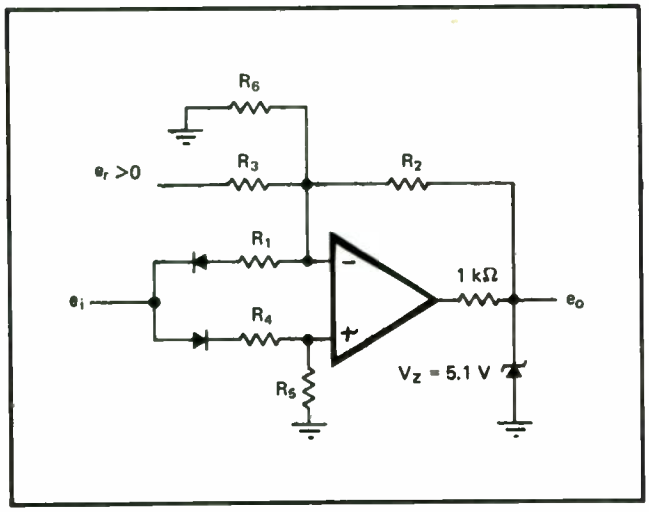
The circuit may be simplified if, for example, the reference voltage is greater than the desired switch-over point. In that case, $R_4 = 0$. If it is less, then R_6 is omitted from the circuit. For symmetrical switching, making $R_4 + R_5$ approximately the same as R_1 equalizes the diode currents, thus more nearly matching the diode forward voltage drops.

If now the output clamp is taken into account, it keeps the lower level of the output from going more than very slightly negative, as shown in Fig. 2. The complement of this transfer function is obtained by changing the polarities of the input diodes and the reference voltage.

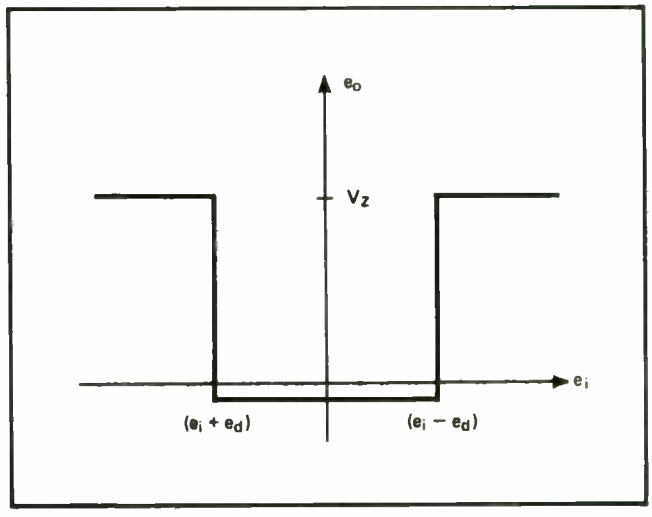
As a design example, suppose ±10.0-volt switch-over points are required, and $e_r = 15$ V. Assume $e_d = 0.5$ V, and use 11 kilohms for R_1 and an open circuit for R_2. Equations (1) and (3) show that $R_3 = 17.4$ kilohms, $R_4 = 0$, $R_5 = 11$ kilohms, and $R_6 = 29.9$ kilohms. Building the circuit with these component values results in measured switch-over points of −10.12 and +10.15 V. The actual switching is completed during a change in the input of less than a millivolt, because the amplifier gain is high and the open-loop configuration is used.

This simple circuit has some disadvantages. Among these are the forward voltage drops of the input diodes, which are significant. Consequently, the circuit cannot be operated near $e_i = 0$. These voltage drops can be minimized with germanium or hot-carrier diodes.

Another disadvantage is that the switch-over points are temperature-sensitive, because the diode forward drops have a temperature coefficient. Finally, the speed of the circuit depends on the type of operational amplifier and on the clamping scheme. Using a comparator in place of the operational amplifier permits somewhat faster switching. □



1. Comparator. Amplifier output is low when the input is between two levels set by choice of resistances, and high when outside these levels. The two trigger levels are independent.



2. Transfer function. Output clamp keeps low level only a fraction of a volt below ground. The complementary function is obtainable by inverting the two input diodes and the reference voltage.

Logic circuit selects most intense signal

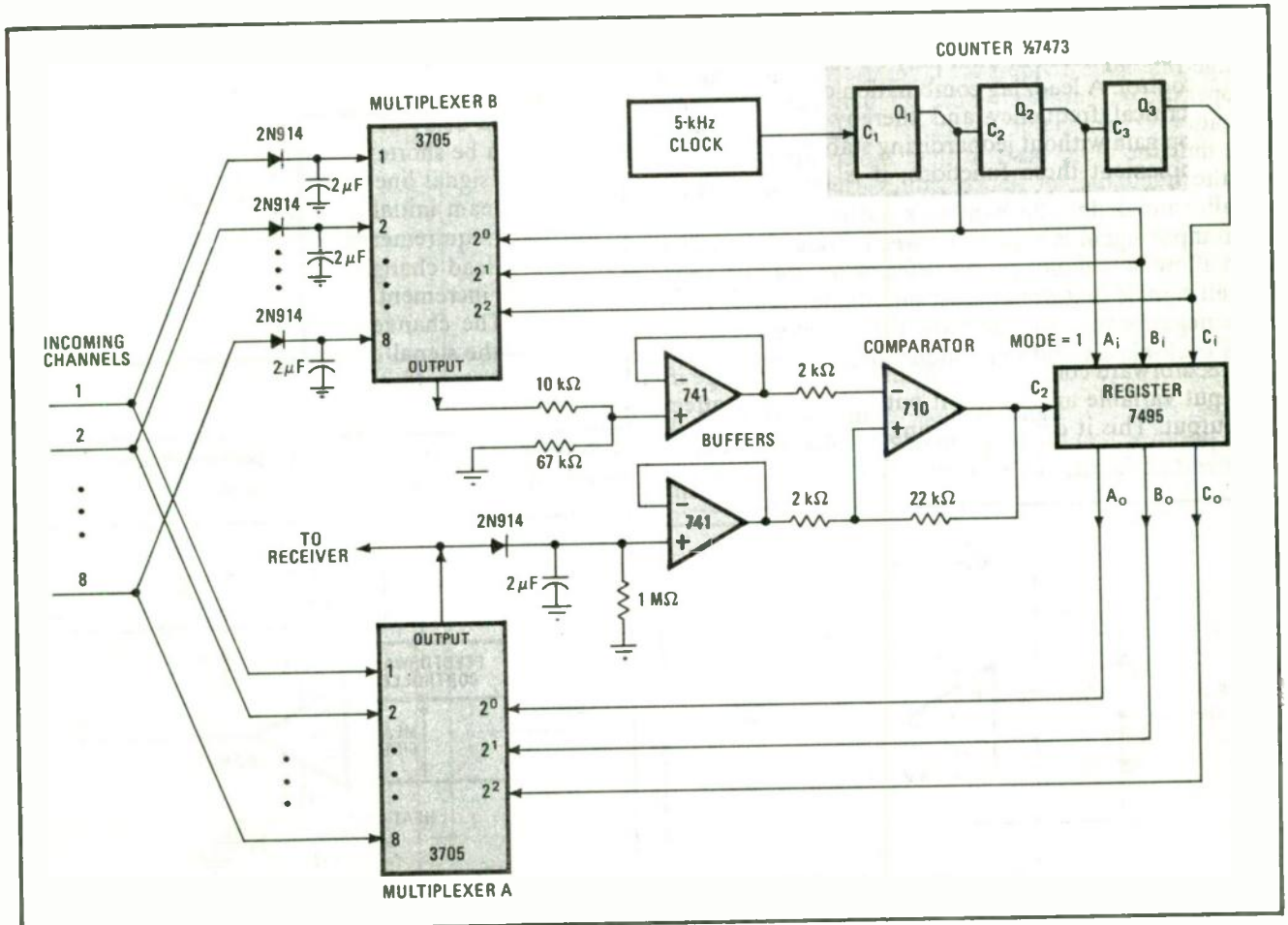
by P. V. H. M. L. Narasimham
Indian Institute of Technology, Kanpur, India

In police wireless communications where each patrol car has its own frequency, messages from the cars are received at police headquarters via satellite receiver stations to avoid blind angles, obstacles, and dead zones. An operator at headquarters could select the best signal from these stations by manually sampling the various outputs from the HQ receiver and comparing their volumes. This method is unsatisfactory because of delays in switching and subjective evaluation of signals. Therefore, an automatic maximum-strength-signal selector is needed to select the strongest of incoming signals and connect it to the headquarters receiver. Whenever the signal level from any unselected relaying station becomes higher, the headquarters receiver must promptly select that signal.

The circuit shown uses a pair of analog multiplexers to automatically connect the headquarters receiver to the strongest signal. The incoming signals from eight satellite stations, band-limited to the range from 300 to 3,000 Hz, are amplitude-limited to ±5 volts peak to peak. These signals go to multiplexer A and also go through eight level-detectors to multiplexer B. The channel-selector inputs to multiplexer B are driven by a 3-bit counter that counts 5-kHz clock pulses. Thus, the signal levels of the eight incoming channels appear, one after another, at the output of B. These levels are compared with the level-detected output from multiplexer A by a 710 comparator. The output from the comparator controls the operation of a 7495 register.

The channel-selector inputs to A come from a register that contains the code for the channel with the highest signal level, as explained below. The output from B is attenuated about 10% by the resistive voltage divider, to give the output from A an advantage in the comparator. The comparator's output is high as long as the most intense signal is selected by A.

If propagation conditions change so that the signal level on some unselected channel, say U, exceeds the level on the selected channel, then when multiplexer B is switched to channel U the output of B is higher than the output of A. Therefore the comparator's output goes low. On this trailing edge, the contents of the counter are clocked into the register so that A also selects chan-



Goes with strength. Most intense signal coming from relaying stations is connected to central receiver through multiplexer A. If signal from A is not the strongest, comparator goes low when counter clocks multiplexer B to the stronger signal. Register then changes input code to A so that the stronger signal is connected to receiver. System allows police cars (each with own frequency) to contact HQ via satellite stations.

nel U. Because of the 10% advantage given to A, the comparator's output then becomes high again. Thus the most intense signal is selected by A and connected to the receiver; all of this takes place within a fraction of a clock period.

The inputs of the comparator are buffered through the type 741 voltage followers to avoid loading on the level detectors and thus preserve the accuracy of comparison. The level detectors are simple diode peak detectors with 2-microfarad capacitors. Their performance is satisfactory, but they may be replaced by better level-detectors if necessary. □

Modified window comparator compensates for temperature

By C. E. Musser
General Electric Co., Binghamton, N.Y.

A window comparator circuit, which detects signal voltages at two different levels by comparing them to fixed references, can be modified to compensate for temperature variations that otherwise can affect the trip points that define the window.

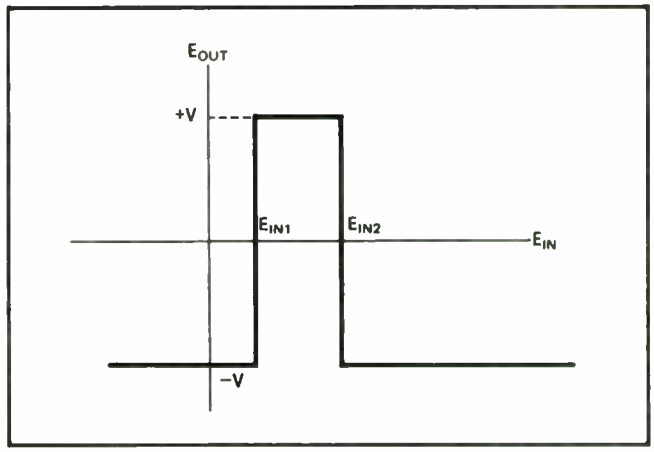
In the circuit's simplest configuration (Fig. 1), two voltage-reference dividers are connected to the inputs of an operational amplifier. Both dividers have the same excitation polarity, but the non-inverting input reference must be more positive than the inverting. Choosing the fractional resistance values establishes this inequality and defines the window's width.

An input signal is applied between diodes D_1 and D_2 from a low-impedance source, such as another op amp. For all signals that are at least one diode voltage drop more negative than the inverting input reference, diode D_2 is back-biased and not conducting, and the op amp is in negative saturation.

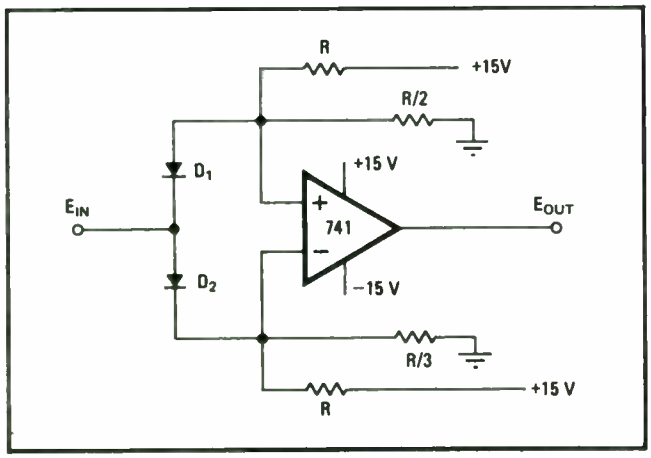
When the input signal is more than one diode drop more positive than the junction of the voltage divider at the inverting input, diode D_1 turns off and D_2 turns on. When the non-inverting op amp input becomes slightly more positive than the inverting input, the amplifier switches to positive saturation. In Fig. 2 this level is called E_{in1}.

A still larger positive excursion of the signal, to E_{in2} in Fig. 2, pulls the inverting input above the non-inverting one, making the op amp switch back again to negative saturation.

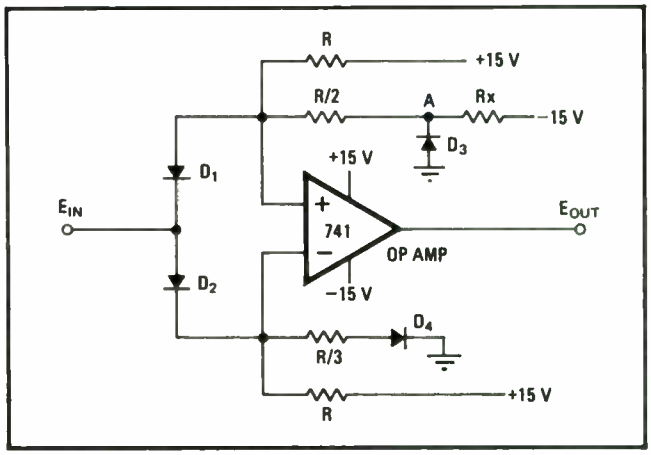
The two voltage references can be made negative by reversing the polarity of the excitation voltages and the input diodes. Doing this also reverses output polarity—it effectively turns Fig. 2 upside down. The reference volt-



2. Switching points. Op amp output is positive whenever input lies between E_{in1} and E_{in2}, negative for other levels.



1. Plain window. Operational amplifier, otherwise in positive saturation, is in negative saturation whenever input signal is more than 0.6 volt below negative reference or above positive reference.



3. Modified window. Because temperature changes can vary diode characteristics and change trip points, extra diodes in dividers vary in the same way and minimize the extent of the change.

ages for this circuit are

$$E_{in1} = V[(R/3)/(R+R/3)] - V_d = (V/4) - V_d$$
$$E_{in2} = V[(R/2)/(R+R/2)] + V_d = (V/3) + V_d$$

where V_d is the diode voltage drop.

Temperature changes cause diode variation that affect the trip points. Additional diodes in the dividers (Fig. 3) vary in the same way as the input diodes, and thus partially compensate for such changes. The resistor R_x should be chosen so that point A is slightly negative, just enough to bias the diode into continuous conduction. For the modified circuit the reference voltages are

$$E_{in1} = \eta[(V - V_d)(R/3)/(R + R/3)] + V_d\theta - V_d$$
$$= (V - V_d)/4$$
$$E_{in2} = \eta[(V + V_d)(R/2)/(R + R/2)] - V_d\theta + V_d$$
$$= (V + V_d)/3$$

Both of these circuit versions have been tested at room temperature using ±1% metal-film resistors, 1N4148 diodes, and 741 op amps. Assuming V_d to be 0.6 volts, the measured trip points agreed well with the calculated values. □

10. Control circuits

Complementary lighting control uses few parts

by Mark E. Anglin
Novar Electronics Corp., Barberton, Ohio

A very useful tool for stage lighting, light shows, or even home movies is a complementary lighting-control unit that will fade out one lamp while simultaneously increasing the light output of another. The usual design for such a control unit is rather complicated, relying on dual potentiometers, two fader circuits, and two of everything else. But the circuit in the diagram can perform this function with a minimum of parts, and the two loads track each other accurately without adjustments.

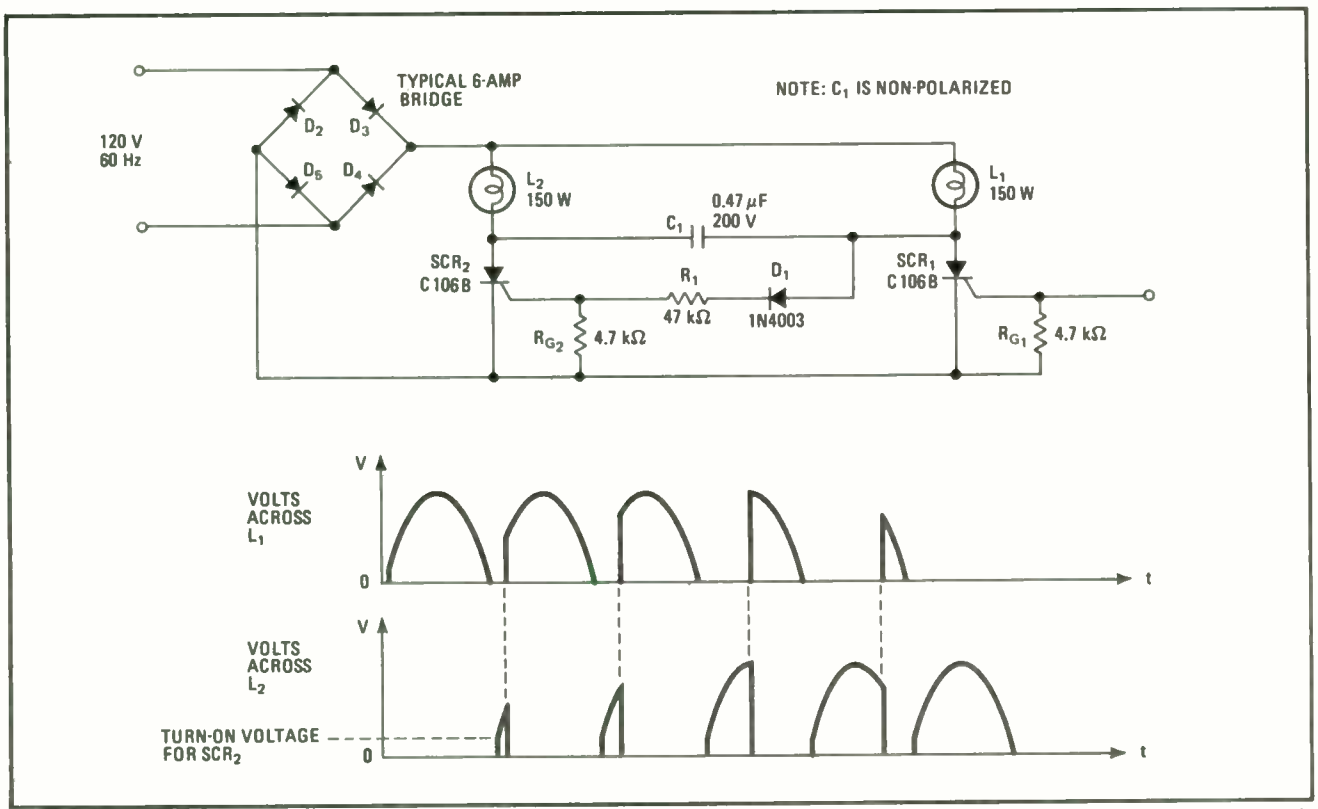
The gate of SCR_1, a silicon-controlled rectifier, is driven from a standard phase-control circuit, based, for example, on a unijunction transistor or a diac. It controls the brightness of lamp L_1 directly. Whenever SCR_1 is not on, a small current flows hrough L_1, D_1 and R_1, permitting SCR_2 to fire. When SCR_1 turns on, current flow ceases through D_1 and R_1; the energy stored in C_1 produces a negative spike that turns SCR_2 off.

In this circuit, the peak current through the diode bridge never exceeds the peak current through either SCR, because the two SCRs can never be conducting at the same time. This is an advantage over the conventional circuit, in which each SCR would be fired at a 45° phase angle to produce half brilliance from the lamps. This represents the worst case of simultaneous conduction and draws a peak current from the bridge that is twice the magnitude of the current of a single 150-watt lamp.

If this control circuit is to be used with lamps rated at more than 150 watts, the value of C_1 should be increased. The value of C_1, in microfarads, equals or exceeds:

$$(1.5\ t_{off}I)/E$$

where t_{off} is the turn-off time of the SCR in microseconds, I is the maximum load current, and E is the voltage at this maximum load current. □



Parts miser. Complementary lighting control fades one lamp out while bringing up the other one, with fewer parts than conventional controls use. Waveforms are segments of successive half-cycles of a full-rectified sine wave as control signal varies.

Precision triac trigger has wide dynamic range

by Ronald Sans
Tampa, Fla.

Standard triac triggering circuits do not generally provide an input dynamic range that is broad enough for precise driving of ac loads. But if the ac line is made to synchronize a voltage comparator to a zero-voltage switch, a triac trigger can be built to handle input signals over a 50-decibel dynamic range at frequencies of 10 hertz to 10 kilohertz. The circuit is useful whenever the triggering parameters of a triac must be controlled precisely, as for the currently popular light-box type of music display.

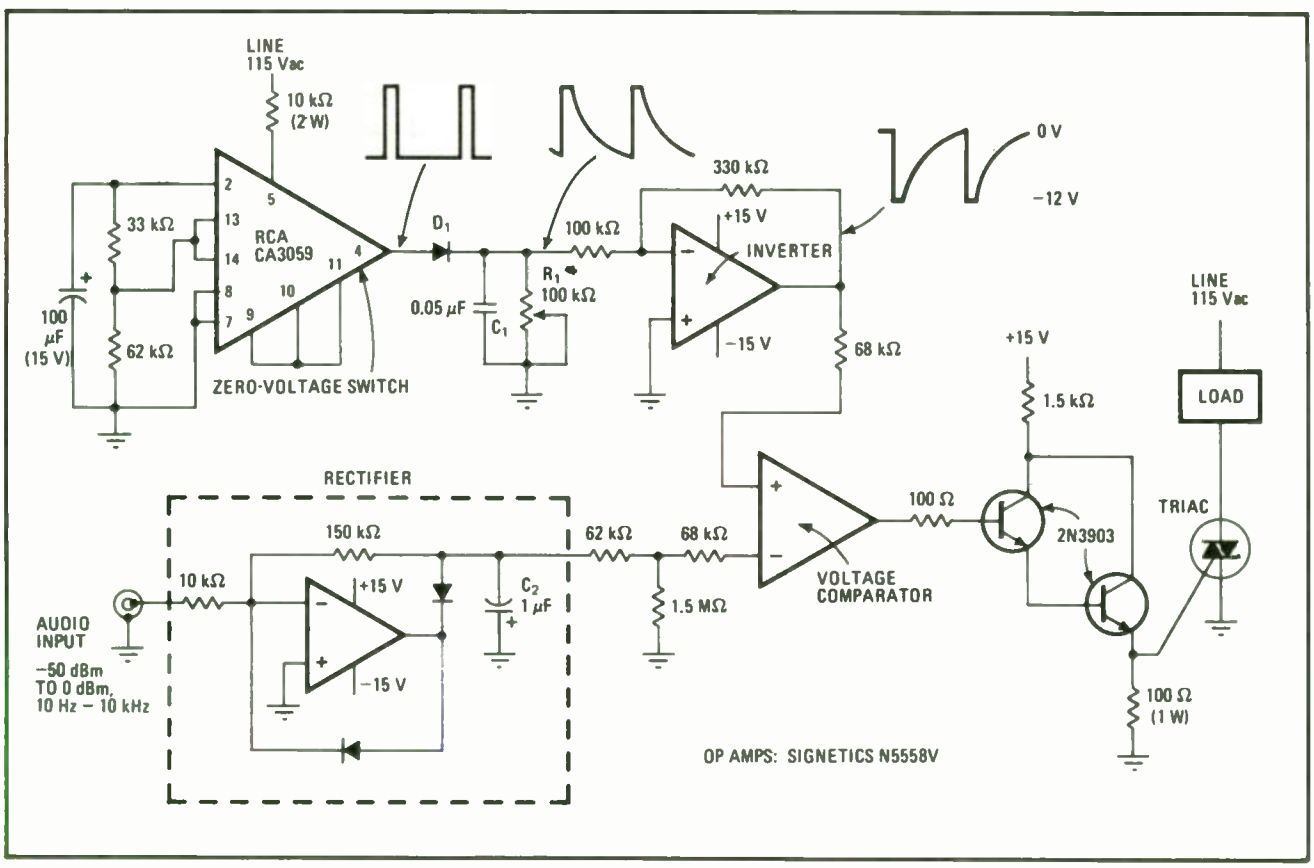
The zero-voltage switch produces a 100-microsecond pulse that begins 50 μs before the line voltage reaches zero. Every 8.3 milliseconds, therefore, an output pulse from the zero-voltage switch passes through diode D_1 to resistor R_1 and capacitor C_1. The leading edge of this pulse charges capacitor C_1, while the trailing edge discharges C_1 through resistor R_1. The dynamic range of the circuit is determined by the setting of resistor R_1. (When R_1 is set to about 47 kilohms, the dynamic range is approximately 30 dBm.)

Input signals of less than -30 dBm (0 dBm for a 600-ohm reference) turn off the triac; signals equal to -30 dBm just turn on the triac; and signals of 0 dBm or higher produce a full-power output. Since the circuit's output is based on the exponential discharge of capacitor C_1, the output power of the circuit varies logarithmically and depends on the values chosen for resistor R_1 and capacitor C_1.

The input signal is applied to the full-wave rectifier, which is capable of accepting signals of less than -50 dBm. The rectifier produces a negative voltage that is filtered by capacitor C_2 and then fed to the inverting input of the voltage comparator. Capacitor C_2 determines how much delay or damping there is; the higher the input frequency, the smaller the capacitor can be.

A conventional Darlington amplifier is used as the output trigger. A higher frequency response can be obtained by using high-frequency operational amplifiers instead. □

Driver for ac loads. Triac triggering circuit operates over wide dynamic range, providing precision control for an ac load like a music display. Audio input power levels can range from -50 to 0 dBm. The setting of resistor R_1 determines the circuit's dynamic range, while the value of capacitor C_2 determines the circuit's damping factor. The circuit is synchronized to the ac line.



Sampling regulator controls motor speed

by Philip Dempster
Este Instruments, Inc., Richmond, Calif.

A permanent-magnet dc motor can serve as its own tachometer for speed control, allowing considerable cost savings to be realized over an expensive motor-tachometer unit. Sampling is employed in the motor-speed regulator shown to eliminate the errors and uncertainties introduced by the motor's armature and brush resistances. Motor speed can vary over a 20:1 range.

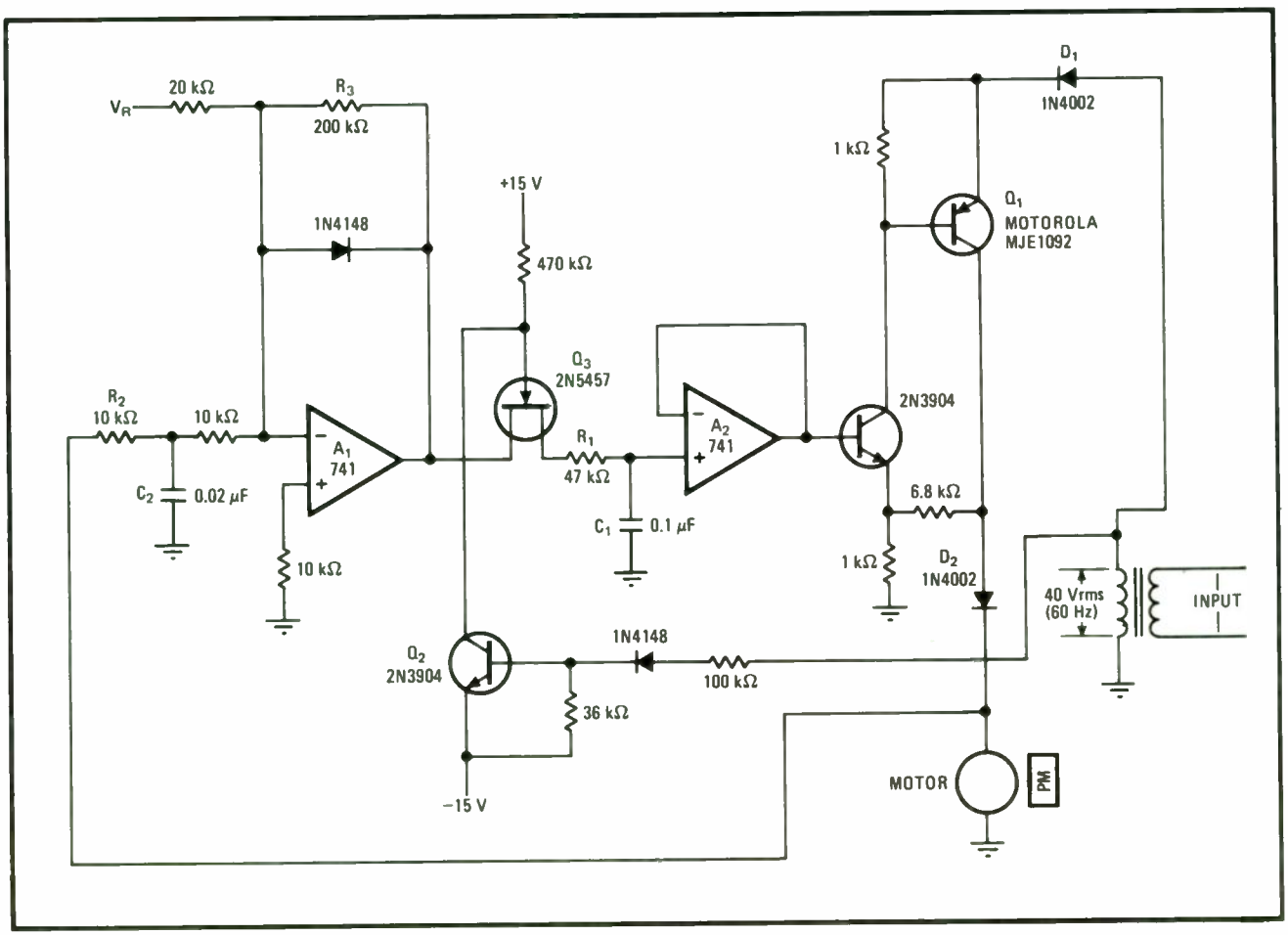
During positive half cycles of the input, the transformer's secondary voltage drives transistor Q_1 through diode D_1. During negative half cycles of the input, this drive power is removed, and the motor's back emf is compared to reference voltage V_R. Any resulting error signal is applied to the inverting input of amplifier A_1.

For a portion of each negative half cycle, transistor Q_2 is switched off by the transformer's secondary voltage, causing field-effect transistor Q_3 to conduct. The amplified error signal at the output of A_1 can then be transferred to capacitor C_1, where it is stored until the following sampling period. During the next positive half cycle of the input, this stored error signal is amplified again (by amplifier A_2) and then applied to the motor to correct any speed error that may exist.

Diode D_2 decouples the motor from the drive circuitry during each sampling period to prevent errors from being introduced in the sampled voltage. Two RC filters—one formed by resistor R_1 and capacitor C_1, and the other by resistor R_2 and capacitor C_2—are intended to reduce brush transients. The R_1C_1 filter has the longer time constant of the two and is located after FET Q_3 to avoid degrading the recovery time of amplifier A.

Resistor R_3 controls the gain in the feedback loop. Its value should be chosen to provide the highest possible gain while preserving good loop stability. □

Motor-speed control. Sampling regulator circuit permits motor speed to be varied over 20:1 range. For portion of negative half cycle of the input, the motor's drive power is removed so that the motor's back emf can be compared to reference voltage V_R. Any resulting error is stored across capacitor C_1 until the next positive half cycle of the input. The error voltage is then applied to the motor for speed correction.



Dc motor control circuit cancels armature resistance

by Leland N. Van Allen
Ideas Inc., Beltsville, Md.

An ideal permanent-magnet dc motor (or one with a separately excited field) rotates at a speed that is determined solely by applied voltage and is independent of motor load. This is the speed at which the back-emf generated in the rotating armature just equals the applied voltage. Since an ideal motor has no armature resistance, the current drawn can rise to any value necessary to support the load.

But practical motors do have an armature resistance, which degrades their speed regulation with increasing load. This problem can be solved by placing a negative resistance that is exactly equal to the armature resistance in series with the armature.

With the motor-control circuit in the diagram, motor rpm is linearly related to input control voltage, no matter the size of motor load. A high-power operational amplifier is used to drive the motor, and positive current feedback is used to create the necessary negative resistance.

A current-proportional signal is obtained by inserting a small sampling resistor, R_S, at the return side of the motor. This signal, which is applied to the noninverting input of the op amp, causes the voltage that drives the motor to be just enough higher than what should be needed by an ideal motor to satisfy the armature and sampling resistances. The over-all effect is the same as driving an equivalent ideal direct-current motor from a firm voltage source.

The circuit's supply voltages should be about 3 volts higher than the maximum voltage to be applied to the motor, but less than ±22 V, unless a different op amp is used. After a reasonable value is chosen for input resistor R_{IN}, say 10 kilohms, feedback resistor R_F can be determined from:

$$R_F = R_{IN}(\text{rpm})/kE_{IN}$$

where k is the motor "tachometer" constant, expressed in units of rpm per volt. The value of this constant can be found experimentally by driving the motor at a known speed and measuring its open-circuit voltage.

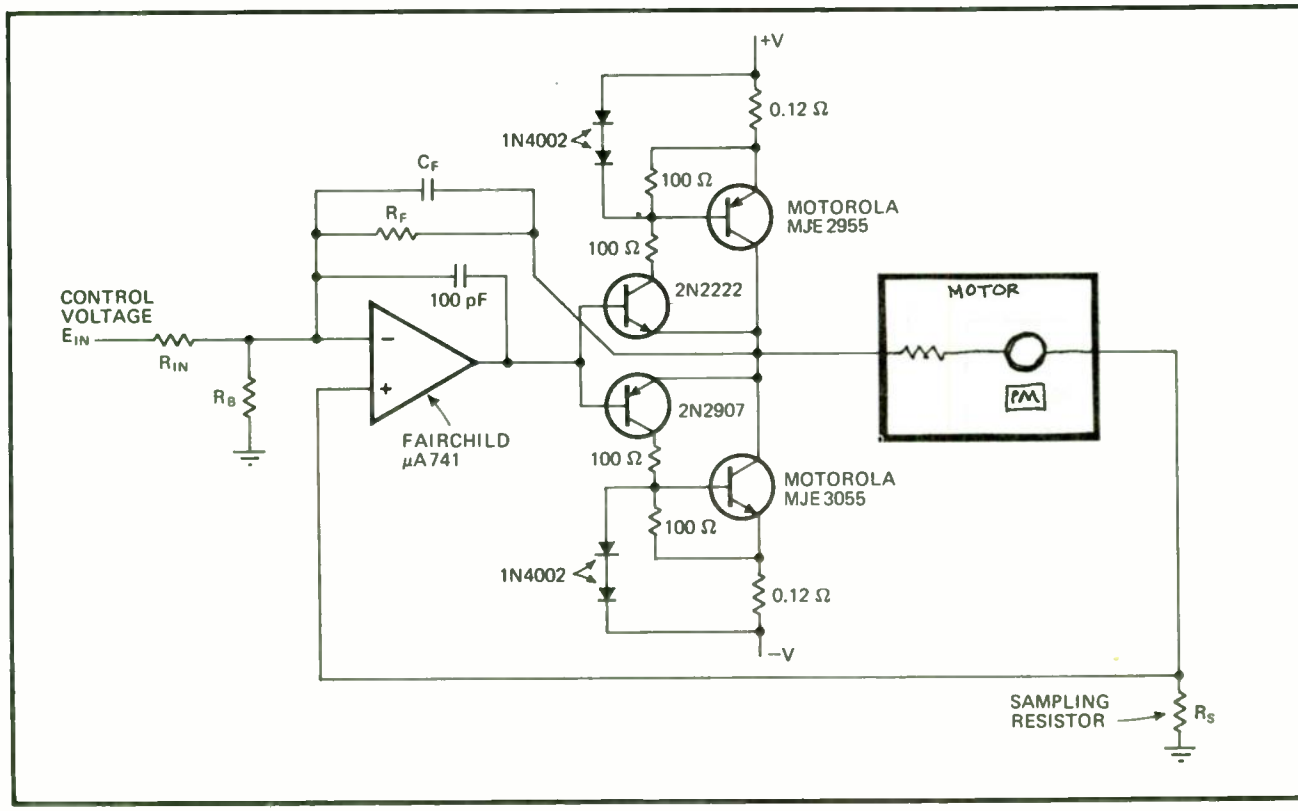
Next, a reasonable value must be selected for the current-sampling resistor, R_S. To minimize power waste, resistor R_S should be considerably smaller than the armature resistance, R_A—for example, $R_A/10$ is a good choice. The value of resistor R_B can then be computed:

$$R_B = R_{IN}R_FR_S/(R_AR_{IN} - R_SR_F)$$

Resistor R_B determines the size of the negative resistance that appears at the output of the op amp. Its value does not affect the motor's rpm-per-volt response.

Capacitor C_F, which is determined experimentally to find the best choice of values, should be as large as possible, but not so large that the motor responds sluggishly. An R_FC_F time constant of 50 milliseconds should serve for most applications. □

Making motor response linear. Permanent-magnet dc motor rotates at rate that is linearly proportional to input control voltage, no matte what the load is. This positive-feedback circuit generates a negative resistance that is equal to the motor's armature resistance, allowing the motor's rpm-per-volt response to be independent of the load. A sampling resistor is used to get current feedback.



Stepper drive circuit boosts motor torque

by E. Wolf
Redactron Corp., Hauppauge, N.Y.

The output power of a stepping motor can be boosted when it's stepping, while the dissipated power during its dwell (holding) intervals is minimized, by effectively doubling the supply voltage of the motor-drive circuit with capacitor charge. The boosted drive circuit shown is intended for four-phase 28-volt motors.

During the dwell intervals, the drive circuit supplies the pair of motor coils that were energized during the previous clockwise step. Transistor Q_1 is on, but conducts only leakage current because transistors Q_2 and Q_3 are off. This permits capacitor C_1 to charge to the supply voltage of 24 V. (Transistors Q_1 and Q_2 form a complementary Darlington transistor pair.)

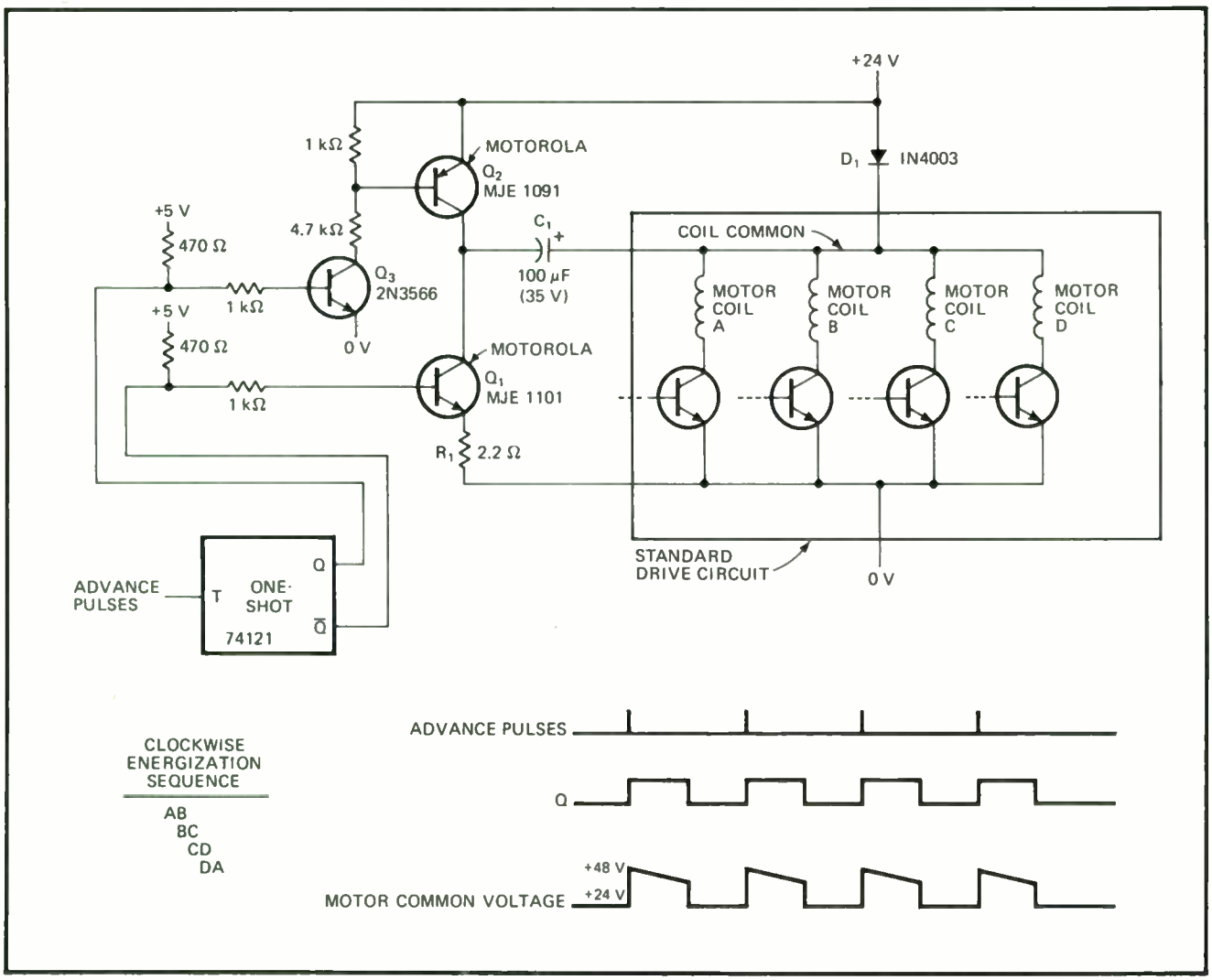
The motor's advance sequence is dictated by a pulse stream that increments the motor's winding-sequence counter and also triggers the monostable multivibrator at the input of the drive circuit. When the $\bar{Q}$ output of this one-shot goes low, its Q output goes high, turning off transistor Q_1 and turning on transistors Q_2 and Q_3.

Since diode D_1 is reverse-biased, the potential at Q_2's collector rises to about 24 V, and the capacitor is restricted to a discharge path through the motor windings. Therefore, the voltage available for the coil common lead is nearly two times the supply voltage—or approximately 48 V. With this boosted voltage, motor-winding current rises rapidly to enhance available torque.

Once the current buildup time is over, the one-shot completes its timing cycle, turning off transistors Q_2 and Q_3, while turning on transistor Q_1, which is current-limited by resistor R_1. Capacitor C_1 recharges to the supply-voltage level. This cycle repeats for every stepping pulse.

The timing of the one-shot is not critical. A reasonable timing period would be half of the shortest period between advance pulses. □

Stepping up torque. Drive circuit for stepping motor boosts available stepping power without increasing supply voltage. During motor dwell time, capacitor C_1 charges to 24-volt supply level. When advance pulse triggers one-shot, transistor Q_1 turns off while transistors Q_2 and Q_3 turn on. Coil common voltage then builds to twice the supply level because Q_2's collector voltage rises by 24 V.



Logic circuit converts synchronous motor to stepper

by Michael D. Doering
Food and Drug Administration, Bureau of Radiological Health, Rockville, Md.

A simple circuit that is compatible with transistor-transistor-logic circuits can convert a two-coil synchronous motor to a synchronous stepping motor. Since circuits that perform this conversion are not available commercially, the designer is usually forced to use relays or come up with his own stepper control circuit.

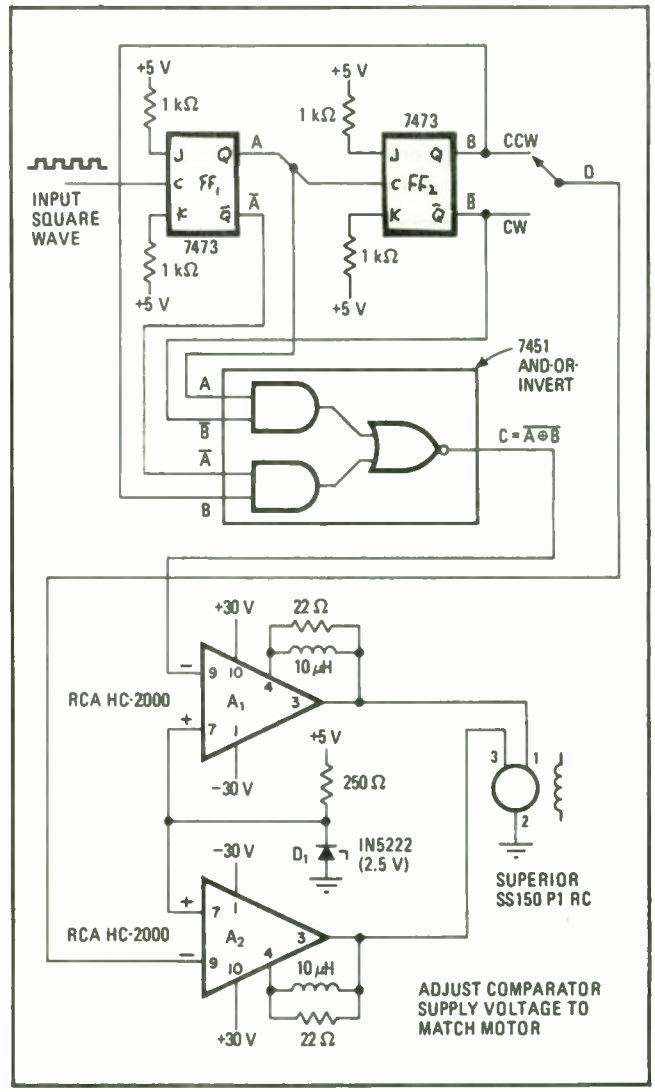
The problem of conversion generally arises when a variable-speed synchronous motor is needed that is capable of delivering up to 1,800 inch-ounces of torque, or when a variable-speed adaptor is required for a motor that is already installed. The converter, therefore, must be a high-current, high-voltage, variable-frequency circuit that can drive a two-phase 115-volt ac motor.

A variable-frequency square wave, which can be supplied by TTL integrated circuits, drives the converter and establishes motor stepping speed. Motor-speed accuracy depends on how accurate the input square-wave frequency is. The size of the step and the maximum stepping speed are determined by the motor used.

Flip-flops FF_1 and FF_2 are connected as a repeating two-bit counter, which has its output decoded by an AND-OR-INVERT circuit. This arrangement provides the four states, which are noted as A, B, C, and D in the diagram, needed to make the motor step properly.

The position of the switch at the output of FF_2 determines the direction of rotation. As can be seen from the figure, the D state simply represents the switch-selected B or $\bar{B}$ states.

Output states C and D are fed to the inverting inputs of high-power comparators A_1 and A_2, respectively. The voltage levels of these two states are then compared to the reference voltage established by the 5-V supply and zener diode D_1. Each comparator drives a separate motor coil and can develop a 75-V 100-watt output. □



Stepping a synchronous motor. Logic circuit plus high-power comparators step two-phase synchronous motor in clockwise or counterclockwise direction. Frequency of input square wave determines motor stepping speed. Two-bit counter formed by flip-flop pair and AND-OR-INVERT circuit produce four logic outputs (A, B, C, and D) that control motor. Each comparator output supplies one motor coil.

Controlling ac loads with C-MOS bilateral switches

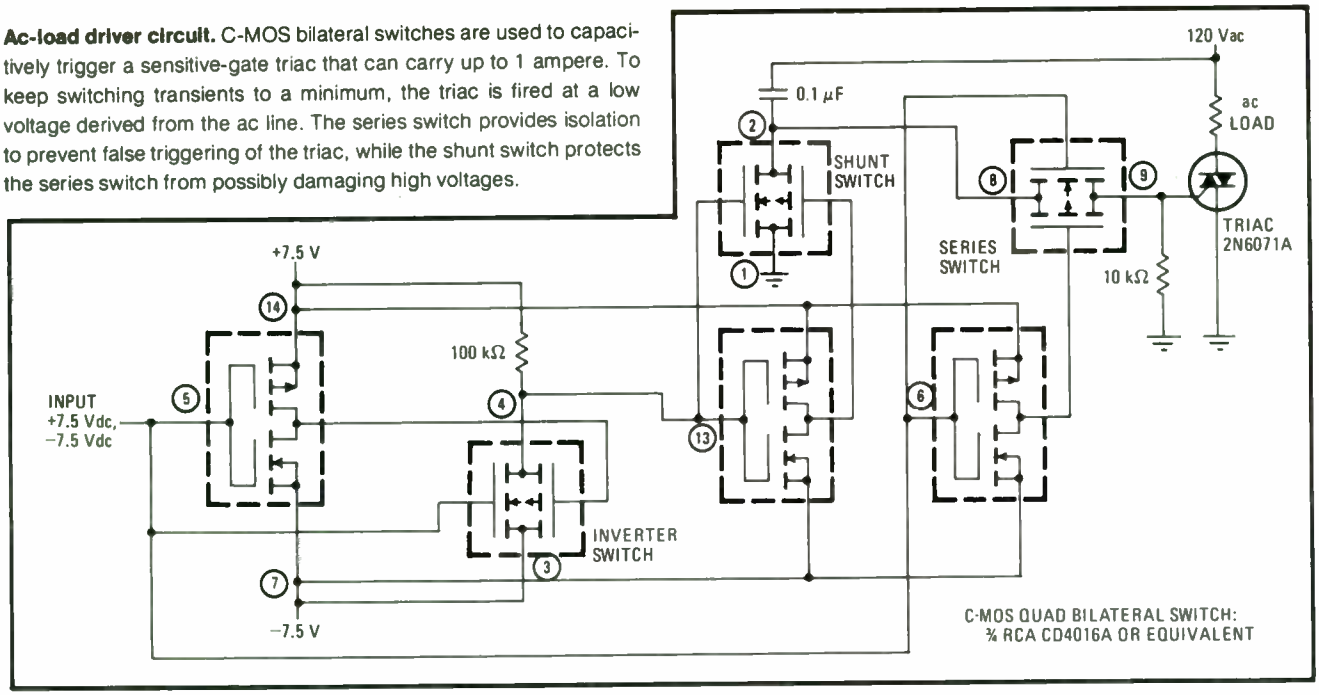
by Arthur Johnson
Darlington, Md.

Power to an ac load can be efficiently controlled by an integrated complementary-MOS quad bilateral switch and a capacitively triggered sensitive-gate triac. The necessary gate-triggering current comes, not from the low-voltage C-MOS power supply, but from the ac line.

Capacitor-triggering is best for firing the triac because it produces the maximum current (at 90° phase shift) when the ac voltage crosses the zero-voltage level. Therefore, the fullest possible use is made of gate-triggering current. Also, the triac is switched into conduction at a low voltage to reduce switching transients, and maximum power is delivered to the load.

The driver circuit for ac loads is drawn in the dia

Ac-load driver circuit. C-MOS bilateral switches are used to capacitively trigger a sensitive-gate triac that can carry up to 1 ampere. To keep switching transients to a minimum, the triac is fired at a low voltage derived from the ac line. The series switch provides isolation to prevent false triggering of the triac, while the shunt switch protects the series switch from possibly damaging high voltages.



gram. Because the on-resistance of each C-MOS bilateral switch is several hundred ohms, circuit voltages could falsely trigger the triac. The triac gate therefore needs to be isolated by the series switch, which, in turn, needs to be protected in its nonconducting state by the shunt switch from possibly damaging high voltages.

Two power-supply voltages, +7.5 volts and −7.5 v, are needed to control both positive and negative ac voltage excursions. This may prove to be a minor inconvenience. But since the necessary gate-triggering current does not have to come from these supplies, they may be simple half-wave-rectified high-resistance sources.

The sensitive-gate triac used here has a maximum current-carrying capacity of 1 ampere. If a larger load must be handled, a triac with higher ratings can be controlled by the smaller triac. In this way, a large load can be controlled without wasting a large amount of energy.

The capacitor value is chosen to provide the required triac-triggering current of 5 milliamperes maximum:

$$C = (5\ mA)/2\pi f E_{max}$$

where f is the ac frequency and e_{max} is the zero-to-peak ac voltage level. □

11. Counters

Counter inverts period to measure low frequency

by Matthew L. Fichtenbaum
General Radio Co., Concord, Mass.

Measuring the frequency of a low-frequency signal directly is a slow process, since enough signal cycles must be counted to give the needed resolution. Measuring the signal's period instead can give the needed information in only one period, but computation or circuitry to convert period to frequency is necessary. The circuit described here finds the reciprocal of the measured period by means of standard binary and binary-coded-decimal counters.

The concept underlying the technique is illustrated in Fig. 1. Four counters are required. Counter A measures the period of the unknown signal by counting the number of clock pulses, N, during a cycle. The number N programs counter B, which is a programable divide-by-N unit. Counter C creates a burst with a fixed number of pulses K.

This burst is applied to counter B, which computes a number K/N, thus taking the reciprocal of the period, N, and producing a number of pulses proportional to the unknown signal frequency. Finally, counter D accumulates these pulses to display the frequency.

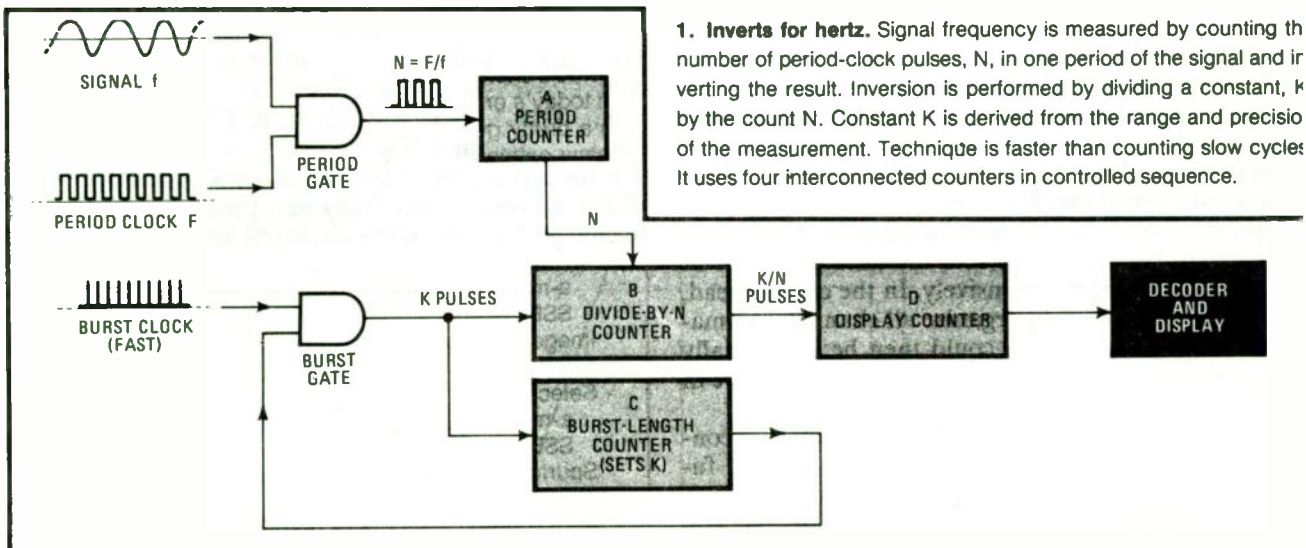
The application determines the clock frequency and the counter lengths.

1. Clock frequency is defined by the highest frequency to be measured, and the resolution with which it must be measured. For example, if 1 kilohertz must be measured to 1% accuracy, 100 clock pulses must occur in 1 millisecond (one signal period). This defines a clock frequency of 100 kHz.
2. The lowest frequency to be measured has the longest period, which defines the lengths of counters A and B. In this example, a low-frequency limit of 10 hertz would require a counter capable of counting 0.1 second (period of 10 Hz) × 100 kHz, or 10^4 clock pulses. Fourteen bits would suffice.
3. The size of counter C depends on the length of the pulse burst. The period of a 10-Hz signal results in a count of 10^4 in counter A. If K/N is to be 10, then K, the number of pulses in the burst, must be 10^5. A 17-bit counter is required. The actual frequency of the burst does not enter into the end result; to speed calculation, the burst frequency should be as high as is convenient.
4. Finally, counter D must count to the highest frequency measured, 1,000. This requires 10 bits, or 3 BCD decades if the frequency is to be displayed.

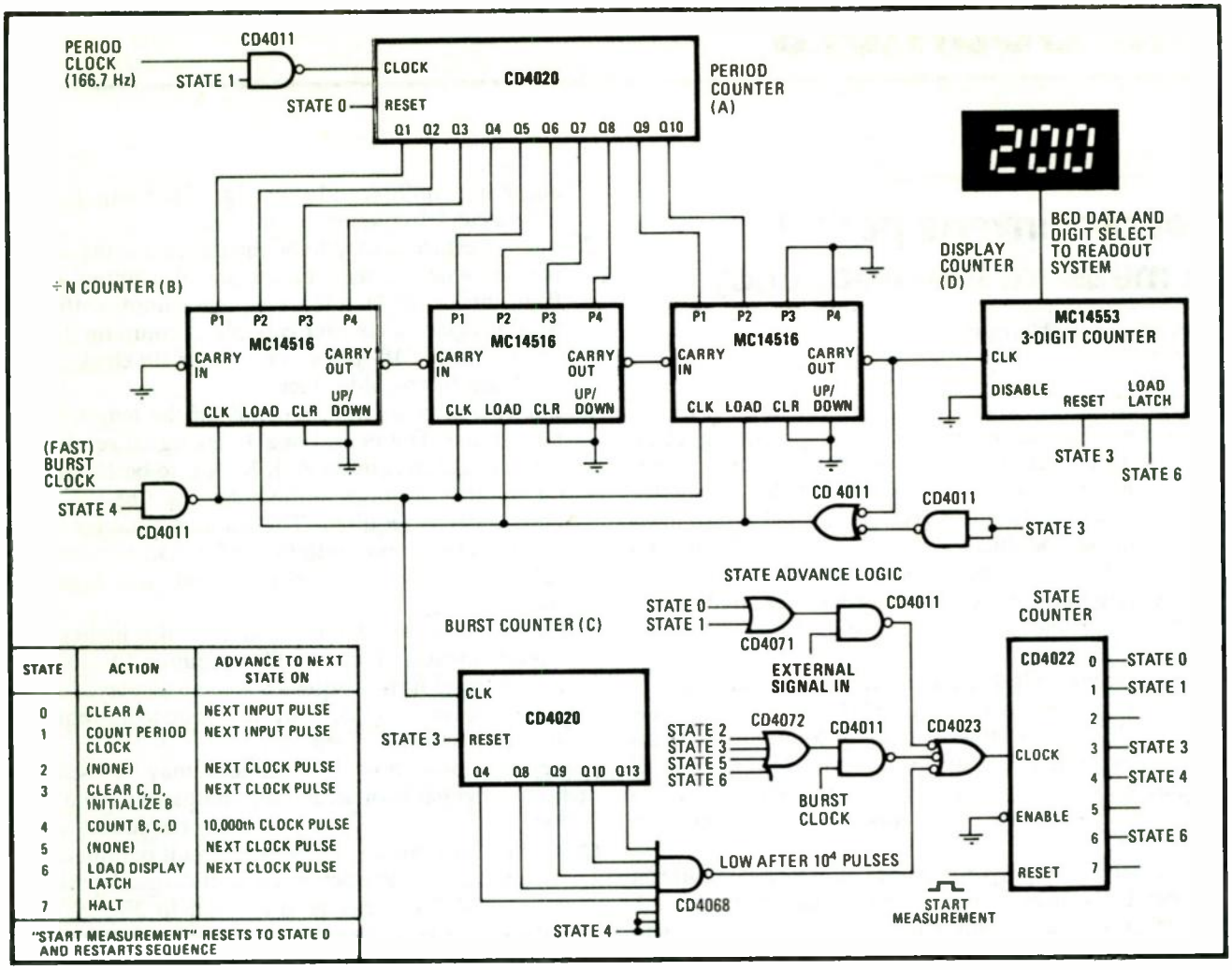
Control logic, to implement the sequencing required, must of course be provided.

Figure 2 shows how the technique may be used in a tachometer capable of measuring shaft speed from 10 to 200 revolutions per minute, with 2% resolution at 200 rpm. The four steps above give the circuit parameters.

1. At 200 revolutions per minute, the signal period is 0.3 second. To measure the speed to 2%, 50 clock pulses must be counted in this time, so the clock frequency must be 166.7 Hz.
2. At 10 rpm, the signal period is 6 seconds. Counting clock pulses for this time results in 6 × 166.7 = 1,000 counts, so counters A and B are each 10 bits.
3. The pulse burst must give a quotient of 10 with 1,000 counts, so it must be 10,000 counts long. Therefore K is 10^4, and counter C thus requires 14 bits.
4. Counter D, the display register, must count up to th



1. Inverts for hertz. Signal frequency is measured by counting the number of period-clock pulses, N, in one period of the signal and inverting the result. Inversion is performed by dividing a constant, K, by the count N. Constant K is derived from the range and precision of the measurement. Technique is faster than counting slow cycles. It uses four interconnected counters in controlled sequence.



STATE	ACTION	ADVANCE TO NEXT STATE ON
0	CLEAR A	NEXT INPUT PULSE
1	COUNT PERIOD CLOCK	NEXT INPUT PULSE
2	(NONE)	NEXT CLOCK PULSE
3	CLEAR C, D, INITIALIZE B	NEXT CLOCK PULSE
4	COUNT B, C, D	10,000th CLOCK PULSE
5	(NONE)	NEXT CLOCK PULSE
6	LOAD DISPLAY LATCH	NEXT CLOCK PULSE
7	HALT	

"START MEASUREMENT" RESETS TO STATE 0 AND RESTARTS SEQUENCE

2. Measuring frequency. Implementation of arrangement in Fig. 1 uses C-MOS devices. A fifth counter, the CD4022 divide-by-8, sequences the steps of the procedure, as shown in the table. This measurement system is fast because it counts clock pulses for only one period of the signal frequency, instead of counting many cycles of signal. Precision of measurement is high because clock rate is high.

maximum of 200. Three BCD decades will suffice. For the low frequencies involved, complementary-MOS devices are adequate. The control logic consists of a CD4022 divide-by-8 counter with individually decoded outputs. Each output corresponds to a step in the control sequence as follows:

- Clear period counter A.
- On next signal transition, start counting clock pulses in counter A.
- On next signal transition, stop counting A.
- Clear counters C and D.
- Enable counters B, C, D to compute frequency.
- After 10,000 pulses, stop counting.
- Load output latch to update BCD display.

A network of gates selects the proper signals to advance the sequencer from state to state.

For easier implementation, the length of the pulse burst may be chosen to be an exact power of 2. This simplifies the logic around counter C.

The final display is equal to K/FT, where K is the length of the burst, F is the period-clock frequency, and T is the signal period. Scaling either K or F changes the displayed result accordingly and provides an easy way to change the units of the displayed answer. □

Up/down synchronous counter takes just four MSI packages

by Richard J. Bouchard
Sanders Associates Inc., Nashua, N.H.

An 8-bit synchronous up/down counter with programmable increment-decrement values and a look-ahead overflow-underflow line can be implemented with only four medium-scale integrated circuits. An up/down control line allows the counter to increment either up or down on each clock input pulse by any number from 1 to 7. This type of counter is used in such applications as differential analyzers and X-Y deflection circuits for random-plot cathode-ray-tube displays.

The counter contains an 8-bit latch that is driven by two 4-bit adders. The output of these adders is the sum of the existing latch (counter) output, plus or minus the existing value of the 3-bit increment-decrement control signal. Therefore, at any given time, the input to the latch represents the next counter state, which is synchronously entered into the latch upon receipt of a clock input pulse.

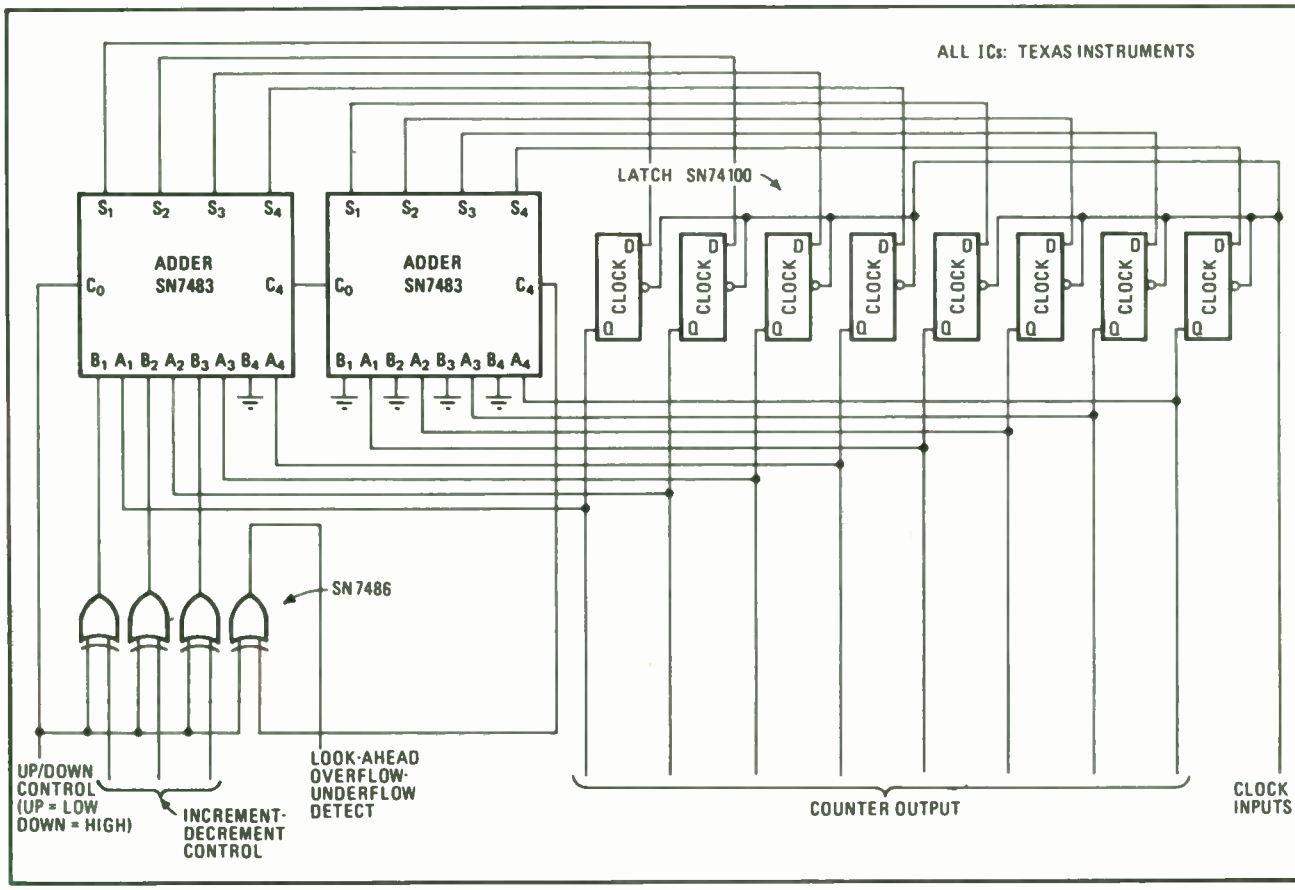
In the count-up mode, the three-bit increment-decrement value is added directly to the existing counter output to provide the next-count input for the latch. In the count-down mode, however, the inputs to the (left) adder from the output lines of the quad exclusive-OR gate represent the 1's complement of the 3-bit increment-decrement value.

The carry input of the least-significant adder stage is activated simultaneously via the count-down control line, and the 2's complement of the existing decrement value is added to the counter output. For the count-down mode, then, the input to the 8-bit latch is less than the existing counter output by the value of the 3-bit increment-decrement control.

One of the stages of the quad exclusive-OR gate is used to generate a positive output signal whenever the next count to be entered into the latch will cause either an overflow or underflow in the counter output. This is accomplished by simply gating the up/down control line with the carry output of the last adder stage. In a vector display, the look-ahead overflow-underflow signal can be used to inhibit the clock input so that vector wrap-around does not occur.

The range of programable increment-decrement values may be readily extended from the 1-to-7 one shown here to a 1-to-127 one by adding a second quad exclusive-OR element. □

Space-saving counter. Four MSI circuits make up complete 8-bit synchronous up/down counter that includes look-ahead overflow-under flow detection. Output count can be dynamically varied by 3-bit increment-decrement control. For count-up, the value of this signal is added to the existing counter output; for count-down, it is subtracted. The latch input always represents the next counter state.



C-MOS counting circuit accumulates 2^{70} pulses

by Robert M. Owens and Kenneth J. Hintz
Naval Weapons Laboratory, Dahlgren, Va.

An easy-to-build counting circuit satisfies today's increasing need to monitor events or quantities over long periods of time. The circuit, which consists of only five ICs, can count to 2^{70}—that's greater than a sextillion (1×10^{21})! It can be used in any situation where a large number of events must be counted.

Primarily, however, the circuit is intended to provide the integral of temperature over a 30-day period by counting the total cycles of a linear temperature-dependent oscillator. It employs complementary-MOS ICs to reduce power consumption to approximately 4.5 milliwatts for a supply voltage of 9 volts. This allows the circuit to be left unattended in the field for periods of longer than 30 days.

At first, the 64-stage static shift register is reset so that its $\bar{Q}$ and the Q output of flip-flop FF_1 are high. The DATA input of FF_1 is high until a sync ("add one") pulse is generated by the $\bar{Q}$ output of flip-flop FF_2 and the divide-by-64 binary counter, at its Q_6 output.

As the sync pulse goes high, FF_1's DATA input goes low. On the next clock pulse, then, FF_1's Q output goes low, inverting the next bit in the shift register. Since the shift register's $\bar{Q}$ output is high, FF_1's DATA input returns to its high state after the sync pulse occurs, and the rest of the bits in the shift register are recirculated unchanged. At its Q output, the shift register now contains the serial information, 100 . . . 000.

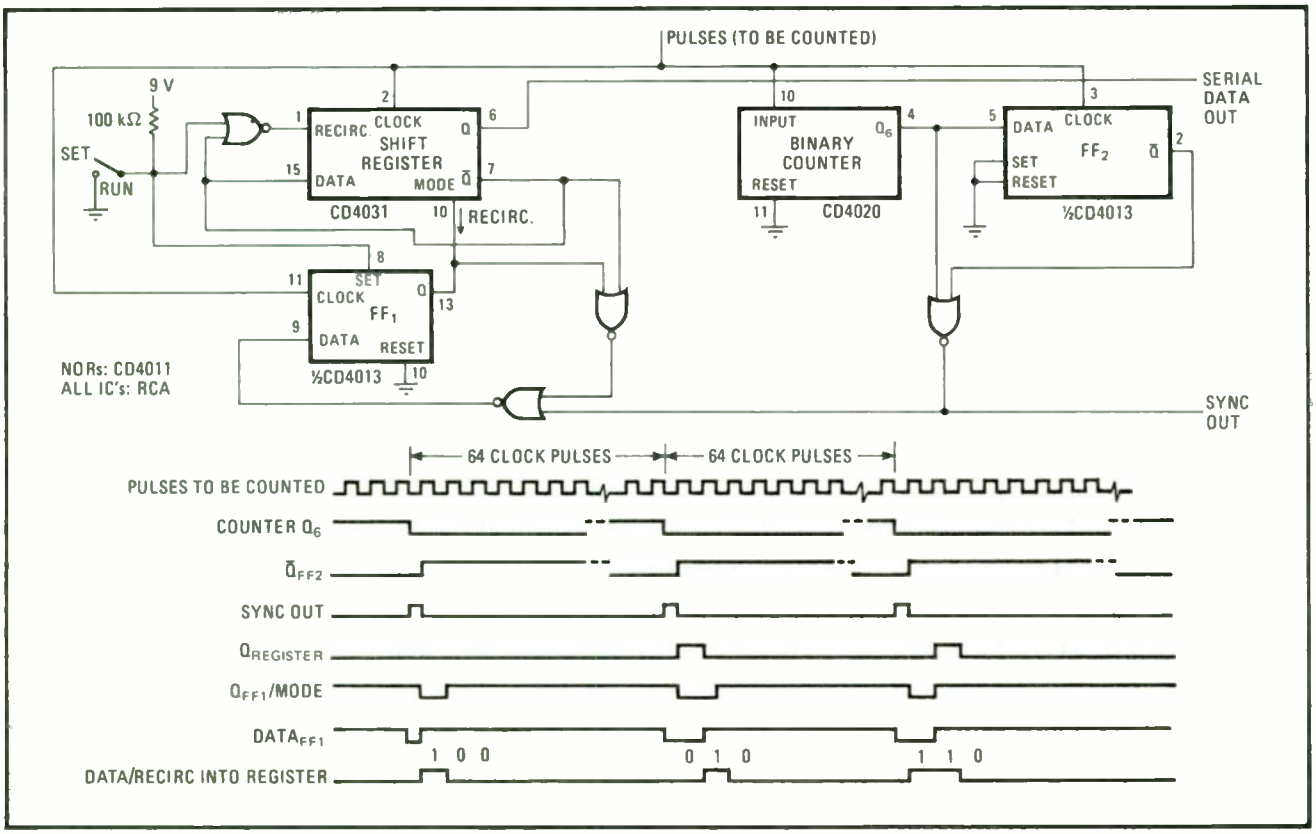
On the next sync pulse, the first register bit is again inverted, but since the register's Q output is low, as is FF_1's Q output, then FF_1's DATA input is held low, effectively implementing a "carry one." This "carry one" causes the second register bit to be inverted too. However, because the second bit goes from low to high ($\bar{Q}$ output of the register goes high), FF_1's DATA input goes high, causing FF_1's Q output to go high so that the rest of the bits are recirculated unchanged.

The shift register now contains 010 . . . 000. The next sync pulse starts the inversion process again, incrementing the register by one, and resulting in an output of 110 . . . 000.

Essentially, the circuit provides a divide-by-n function, where n is the number of stages in the shift register. Since the register can store n bits of information, the circuit has an effective total count capability of $2^n + n$. The total count can be varied by adjusting the register length and by selecting the tap on the binary counter that provides one sync pulse for every register cycle.

For this circuit, the total count is 2^{70}—a count that would require 37.4 million years to achieve if the circuit is clocked at a rate of 1 megahertz. The circuit's resolution for this period would be ±64 counts. □

A real old-timer. Low-power counting circuit can keep track of more than a sextillion input pulses—a count that would take over 37 million years to attain at a clock rate of 1 megahertz. The circuit, which is made up of five C-MOS ICs, actually counts to 2^{70}. It "slows" (for counting purposes) the incoming pulse train by combining a divide-by-64 binary counter with a 64-stage static shift register.



High-power counter drives 20-watt loads

by Christopher Strangio
Villanova University, Villanova, Pa.

A high-current ring counter, which sequentially drives a series of resistive loads, develops an output power level of 20 watts at 2 to 5 amperes. A four-stage version of the circuit is shown here, but the design may be extended to an unlimited number of stages. Typically, this type of counter can be used as a low-voltage lamp driver.

There is one silicon controlled rectifier in each stage. When any one of these SCRs conducts, the stage associated with that SCR will also be in its conduction mode, and the load driven by that stage will be energized.

Initially, all the stages are nonconducting. A SET pulse must be applied to the gate terminal of any one of the SCRs (SCR_1 is used for this circuit) to enable the counter. Conduction can then be passed from the first stage to the succeeding stages by successive trigger pulses. Circuit operation is the same for each stage.

Assume that SCR_2 is in its conduction mode. Prior to triggering, capacitor C_2 is charged to the supply voltage measured from point A to point B, since SCR_2 is conducting, and its anode terminal is at ground level.

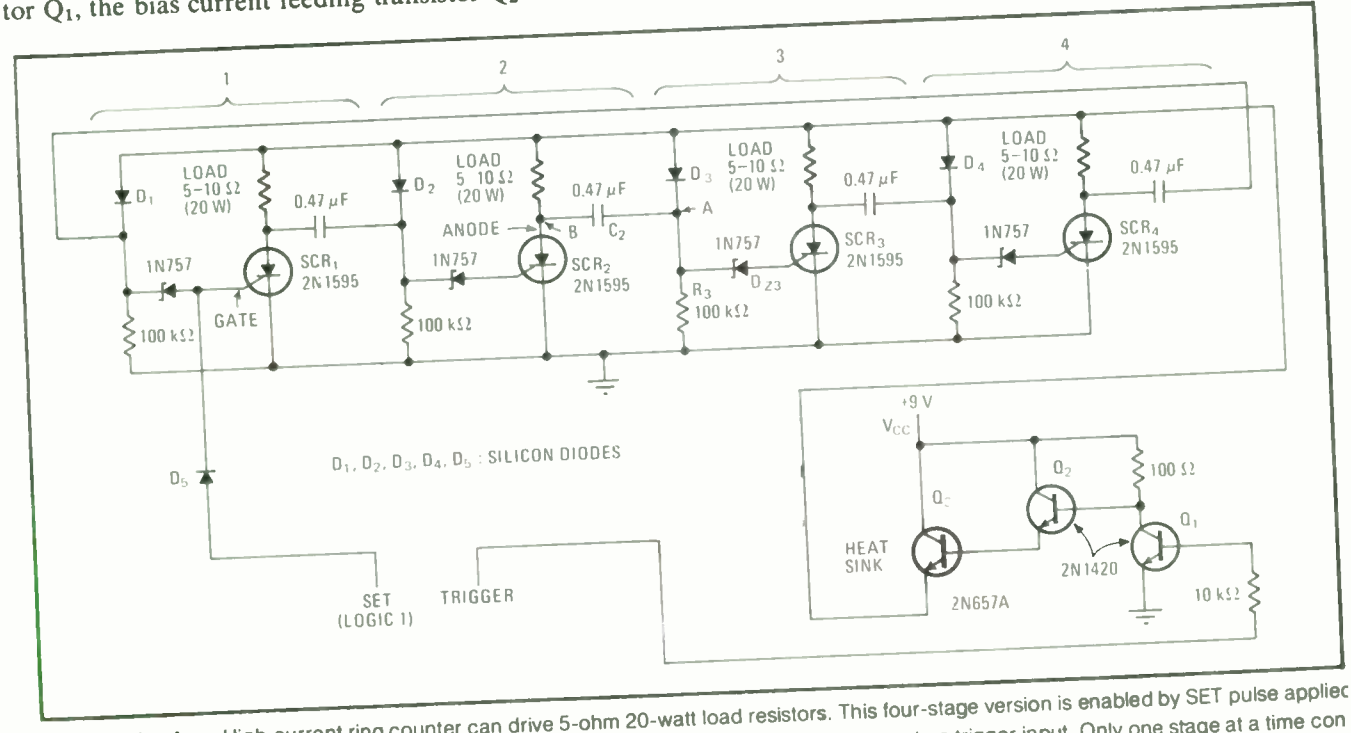
When a trigger pulse is applied to the base of transistor Q_1, the bias current feeding transistor Q_2 is shunted to ground. Drive transistor Q_3 then turns off, the SCR power source is blocked, and any SCR that was conducting will switch off. During this power-off interval, capacitor C_2 retains its charge because all possible discharge paths are blocked. The capacitor in each stage, therefore, serves as a memory that indicates what SCR was previously conducting.

When the trigger pulse terminates, a bias current again flows to transistor Q_2, and power is returned to the SCRs. The anode of SCR_2 now rises to the supply voltage, along with the voltage across capacitor C_2. Because the capacitor is still holding its charge, capacitor voltage increases to the supply voltage at point B, and to twice the supply voltage at point A.

Zener diode D_{Z3}, which is connected to the gate terminal of SCR_3, has a reverse breakdown voltage that is about 20% greater than the supply voltage. Therefore, as point A rises to twice the supply voltage, zener D_{Z3} will conduct, providing a gate trigger for SCR_3 and turning this device on.

Resistor R_3 drops the voltage at point A from the zener breakdown voltage, which is the SCR's gate-current cutoff point, to the supply voltage. Since R_3's resistance is considerably larger than the equivalent SCR gate resistance, resistor R_3 does not disturb the discharging of capacitor C_2 during triggering.

The trigger input pulse should have a minimum width of 200 microseconds, a maximum frequency of 1 kilohertz, and an amplitude of 6 to 9 volts. When SCRs with low firing points are used, put a resistor between each SCR gate and ground to inhibit noise. □



Sequential pulser. High-current ring counter can drive 5-ohm 20-watt load resistors. This four-stage version is enabled by SET pulse applied to gate terminal of SCR_1. Each stage operates identically, producing a drive pulse in response to a trigger input. Only one stage at a time conducts. During triggering, the capacitor in the previously conducting stage retains its charge equal to the supply level.

Transistor array converts to fast-switching thyristors

by H.S. Kothari
Central Electronics Engineering Research Institute, Pilani, India

An ordinary monolithic transistor array can be wired to perform as multiple four-layer silicon-controlled switches by making use of the terminal to the array's substrate. For example, a seven-transistor array having common emitters can be used to implement a seven-stage ring counter.

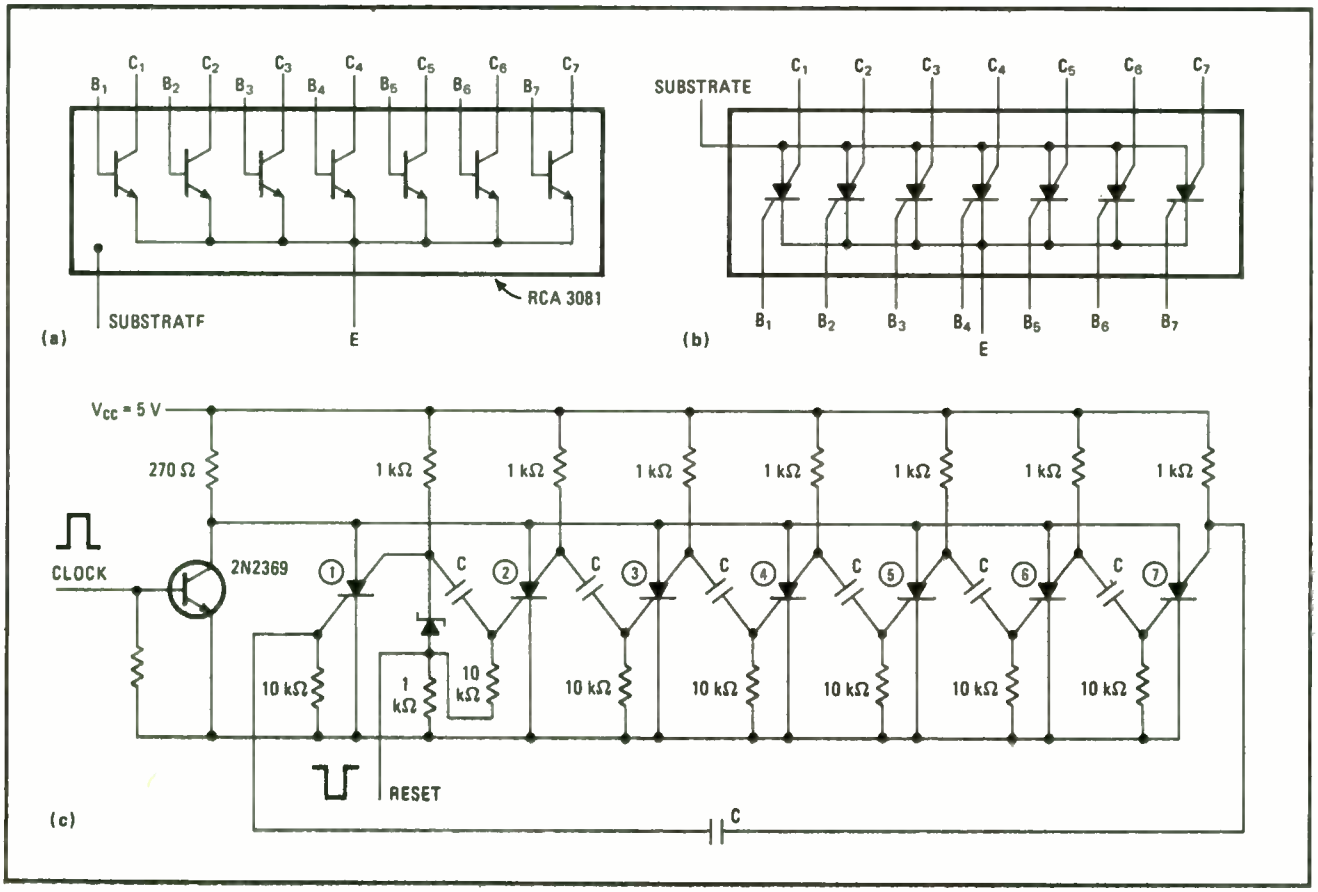
As shown in (a), the npn transistor array has a separate connection to its p-type substrate. The array is easily wired as shown in (b), with the substrate being employed as a common anode to form pnpn structures that can be regarded as silicon-controlled switches. And since the geometry of each transistor is very small, switching times can be on the order of a few nanoseconds.

The schematic of the ring counter is drawn in (c). The first stage is turned on by the trailing edge of the reset pulse. Now, when a clock pulse is applied to the input transistor, the voltage at this transistor's collector drops, and the other counter stages are turned off. In this way, a trigger pulse is transferred from the first stage to the second stage. The next clock pulse causes a trigger pulse to go from the second to the third stage. This process continues and repeats when the seventh counter stage triggers on the first counter stage.

The hold-on current for any stage can be between 50 microamperes and 1 milliampere. The negative voltage amplitude of the reset pulse should be large enough to lower the voltage of the anode gate of the first stage so that this stage is sure to fire. The anode-gate voltage, therefore, is made negative with respect to the anode voltage.

The length of the triggering delay is determined by the capacitance value selected. Voltage amplitudes can be made as large as the collector-emitter breakdown limit of each transistor by increasing the supply voltage, as well as the zener voltage, to some suitable maximum level. □

Wiring transistors as thyristors. Integrated seven-transistor array (a) can be wired as silicon-controlled switches by making use of their common substrate connection. The transistors can then be operated as four-layer devices (b) that have switching times on the order of a few nanoseconds. One application for the pnpn switch array is illustrated in (c)—a seven-stage ring counter.



Potentiometer and timer control up/down counter

by Frank Gergek
Weston, Ont., Canada

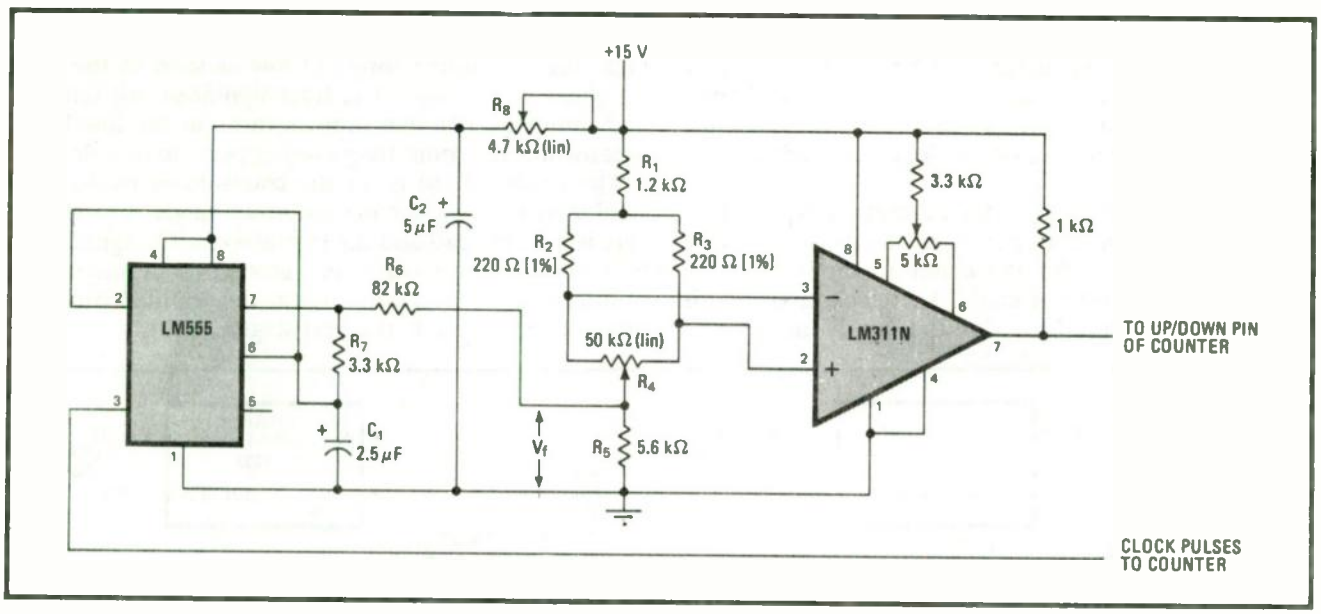
A single potentiometer in an astable multivibrator circuit can replace the clocks and push buttons necessary for setting an up/down counter. It provides a variable clock frequency and the correct logic states.

The same circuit (Fig. 1) can be used in such varied applications as manually adjusting a tool through a stepping motor, rolling a script up and down on a video terminal, and in video games.

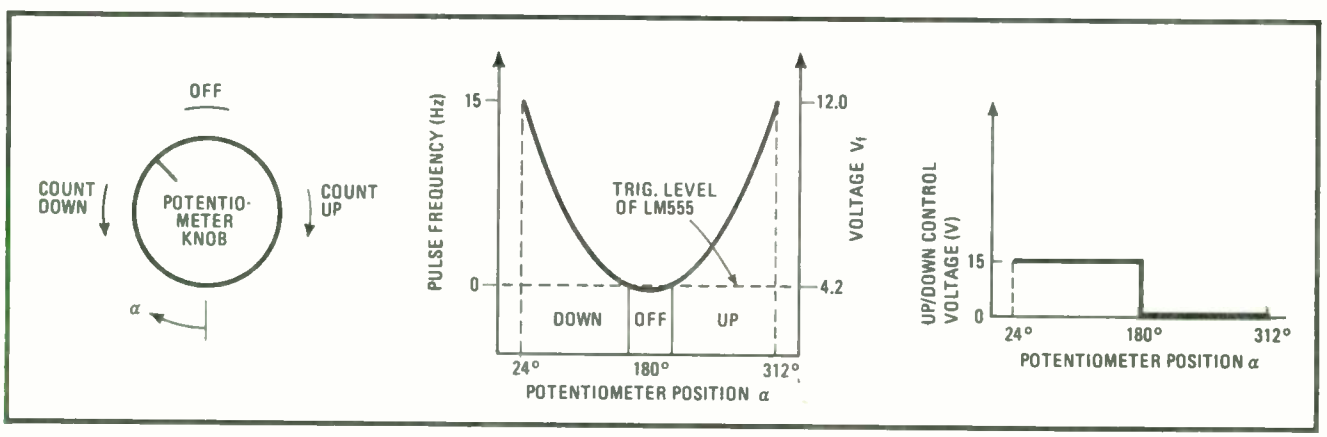
With a three-decade up/down counter that has display but no direct preset capability, a clock feeds pulses into the counter input. To reach the number 615, say, 615 pulses are needed. Two clocks speed up the process: a fast one for rough setting, then a slow one for fine setting. There is a push button for each clock. If the setting is to be reached from both lower and higher numbers, two more push buttons are necessary.

A potentiometer and a 555 timer simplify setting. The pot lets clock pulses be applied quickly for fast setting, then more slowly as the counter gets close to the desired setting. It also holds one pin of the counter at a high or low logic state, depending on whether the counter is to go up (low logic) or down (high logic).

The clock frequency is changed with potentiometer R_4. When R_4 is at its midpoint, the 555 is below threshold for triggering, so the clock rate is zero. When



1. Up or down. Circuit for setting an up/down counter has two outputs. Output from multivibrator delivers clock pulses; clock frequency increases exponentially from zero as potentiometer is turned away from middle position. Output from comparator is either high or low so that counter counts either down or up; output is high counterclockwise from off position of potentiometer, and low clockwise from it.



2. Slow or fast. The LM 555 timer IC operates as a voltage-controlled oscillator, with frequency of clock-output pulses controlled by voltage V_f. The relationship of V_f to the position of the wiper of R_4 is parabolic, even though R_4 is linear.

the potentiometer is turned clockwise or counterclockwise, the 555 generates pulses at a frequency that increases exponentially (Fig. 2). For the component values shown, the maximum frequency is 15 hertz.

Resistors R_2 and R_3 sense whether the potentiometer is clockwise or counterclockwise from its midpoint off position. They cause the comparator to produce either a high or low logic state. The comparator output is high when R_4 is counterclockwise from off, and low for clockwise rotation. This output, also shown in Fig. 2, tells the counter whether to count down or up.

The circuit is adjusted initially by setting R_4 to its midpoint, and then setting R_8 so that the 555 is just below its threshold of oscillation. □

External gate doubles counter speed

by Jeffrey Mattox
United States Air Force, L.G. Hanscom Field, Bedford, Mass.

The counting rate of a standard synchronous up/down binary or decade counter can be doubled without altering the clock frequency. A single external gate does the trick for the count-up or the count-down mode.

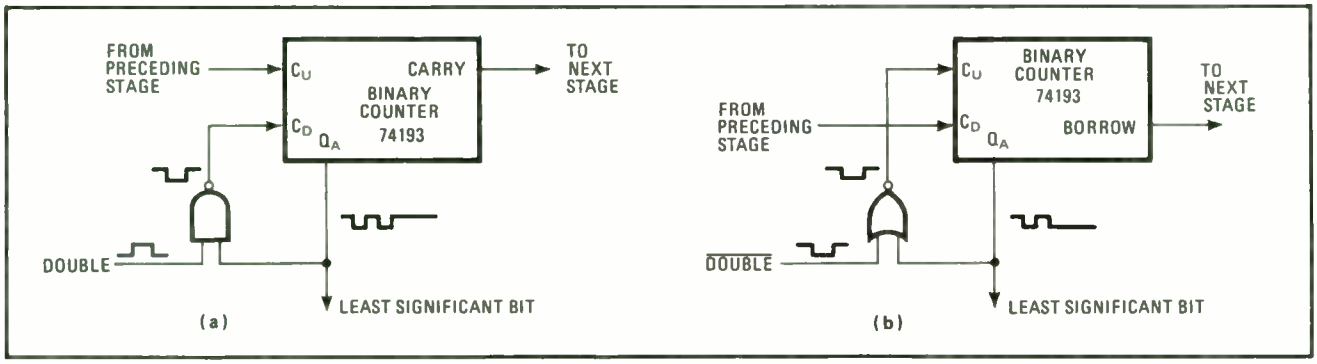
The ability to double the counting rate is useful for applications where a counter must be advanced at twice the normal rate, as in racing the digits to set a digital-clock stage. The extra gate can also be used to halve the counting rate, depending on the logic level of the controlling signal.

Both the decade counter (for example, a type 74192) and the binary counter (for example, a type 74193) have two clock lines—one for the count-up mode, and the other for the count-down mode. The clock input that is not being used is usually tied to the supply line. For either type of counter, there is a counting flip-flop for each output bit.

By sensing the counter's least significant output bit and lowering the alternate-clock input at the proper time, the least significant bit is kept static, and the second counter flip-flop receives all the primary clock pulses. In addition, the state of the least significant bit locks out the alternate-clock input from the other counting flip-flops. For an up-counter, the least significant bit must be high; for a down-counter, it must be low.

The circuit of (a) shows a type 74193 binary counter connected for the count-up mode. The alternate-clock input, in this case the count-down input (C_D), is controlled by a NAND gate. When the DOUBLE input goes high, the C_D input is brought low as soon as the least significant bit is high. The least significant bit remains high until the DOUBLE input returns to the low level. Meanwhile, the count frequency appears to double.

The circuit of (b) is for the count-down mode. It is similar to the one for the count-up mode, but an OR gate is used instead and the DOUBLE control signal must be inverted. The CARRY and BORROW outputs of the counter operate normally so that the doubled counting rate may be carried to the next stage. □



Twice as fast. External gate can double or halve the counting rate of either a decade or binary up/down counter, depending on the logic level of the control signal. The actual clock frequency remains the same. Here, the operating speed of a binary counter is doubled for both the count-up mode (a) and the count-down mode (b). The counter's unused alternate-clock input goes to the controlling logic signal.

Ring counter eliminates false gating signals

by Glen Hamilton
Dickson, Tenn.

A ring counter that performs reliably at speeds up to 7 megahertz can be designed to prevent counting errors caused by false gating signals. Besides being able to clock in either direction (up or down), the counter can be reset from any ring output without losing a clock pulse. Only five dual in-line integrated-circuit packages are needed—a binary counter, a quad latch, a quad NAND gate, and two BCD-to-decimal decoders.

When the input clock pulse rises to logic 1, the binary counter is incremented up or down, depending on the position of switch S_1. The unused clock input to the binary counter must be held continuously at logic 1. For most applications, switch S_1 can be eliminated because only one clock direction is required. To switch between the two clock inputs, two gates must be added so that

the unused connection is always held at logic 1.

With the transition of the input clock pulse from logic 1 to logic 0, the binary counter outputs are loaded into the latches. The next clock pulse enables the NAND gates, allowing the $\bar{Q}$ signals from the latches to pass to the decoders, which then select the appropriate ring output to be enabled. Each succeeding clock pulse sequentially steps and enables the decoder outputs.

The number of stages in the ring is determined by the ring output at which switch S_2 is placed to implement the reset function. When the ring output tapped by switch S_2 is enabled, the binary counter is set to the number appearing at its preset input lines. These preset inputs can be either hardwired or made selectable.

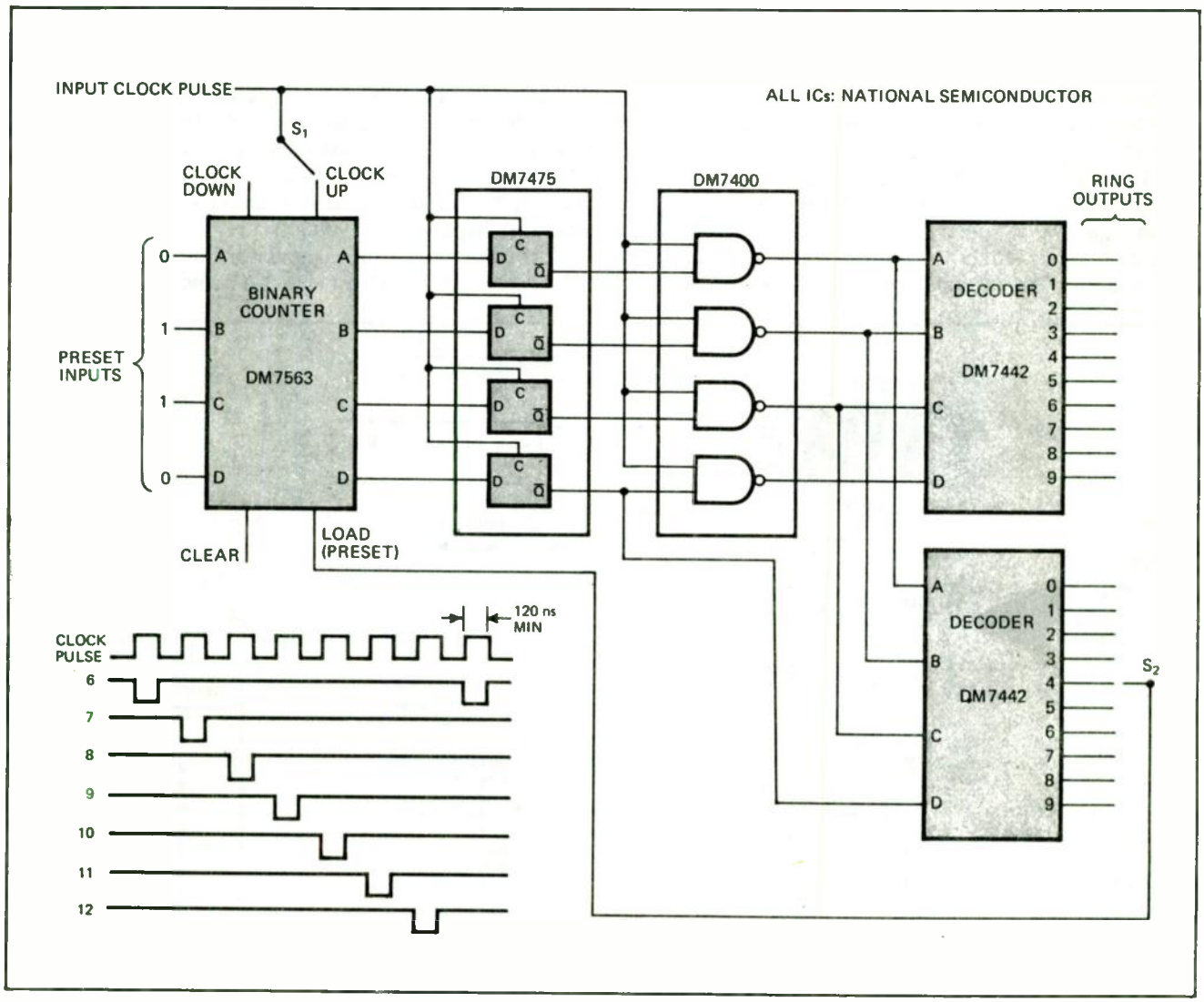
For the wiring connections shown, the binary counter has the binary number six continuously held at its preset inputs, and the ring counter's reset function is placed at the fourth output line of the second decoder. This hookup resets the binary counter to six each time the twelfth ring output is enabled, causing the ring counter to step sequentially from six to 12 and then repeat, as indicated by the waveforms in the timing diagram.

All ring outputs are disabled (in the logic 1 state) when the input clock pulse is logic 0. During this time, the ring outputs are inhibited by the NAND gates to prevent false gating due to transients. Also, all ring outputs are always 180° out of phase with the input clock pulse, and a transition from logic 1 to logic 0 is required to reset the ring counter. This means that the ring counter will be reset only when the ring output selected by switch S_2 is enabled (in the logic 0 state).

The circuit can also be used as a frequency divider that has its output pulse frequency determined by the width of the input clock pulse. Any integral divisor, from 2 to 15, can easily be selected by switch S_2. The divided frequency may be taken from any of the ring outputs.

The binary counter is provided with CARRY TO and BORROW FROM pins, permitting counters to be cascaded for generating more than 15 outputs. With two binary counters, up to 256 outputs can be produced, as long as an appropriate number of decoders is used. □

Sure-clocking ring counter. Input clock pulses sequentially step data through binary counter to latches (flip-flops) to NAND gates to BCD-to-decimal decoders. Switch S_1 permits clocking up or down, while switch S_2 selects number of stages in ring. S_2 also carries reset signal that sets binary counter to its preset input number. Counting proceeds only for clock transition from logic 0 to logic 1.



Low-speed counter uses low-priced calculator chip

by Dennis J. Flora
Stevens Institute of Technology, Hoboken, N. J.

A totalizing counter that runs at less than 40 hertz makes novel use of an inexpensive calculator IC, one of several now available. The IC in the illustrated counter is the MM 5736, a six-digit calculator chip that can directly drive the segments of small common-cathode light-emitting-diode displays. Because of this capability, the single IC replaces many discrete counter and decoder ICs; only a few extra logic chips are required.

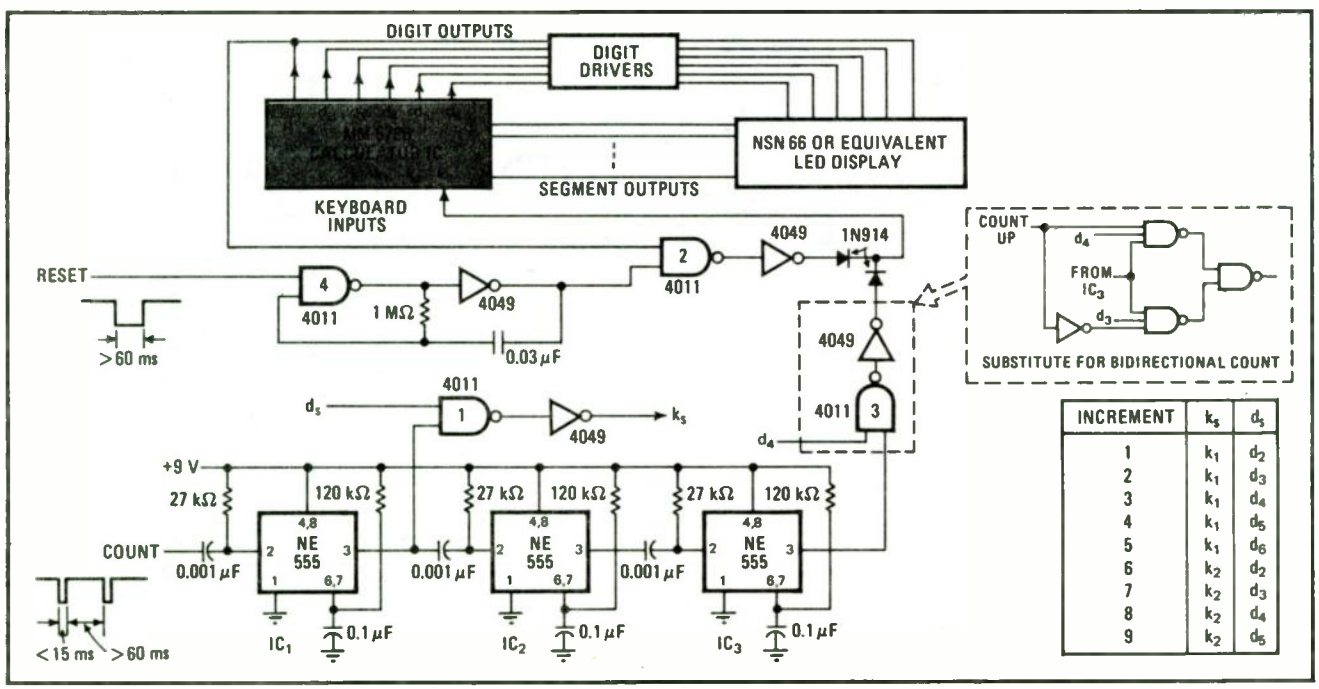
The MM 5736 has seven segment outputs, six digit outputs, and three keyboard inputs. In normal usage, the segment outputs drive the individual segments of all digits in a conventional display. The digit outputs drive the digits of the display, scanning rapidly from one to the next in synchronism with the segment outputs so that individual numerals are illuminated. These digit outputs also scan the keyboard. If any key is depressed, a connection is made from one digit output to one of the three keyboard inputs, uniquely identifying that key. The logic circuits in the chip respond to that input to display a digit or to begin an arithmetic operation.

The logic that is added in lieu of a keyboard includes three 555 timers, four two-input NAND gates, four inverters, and a few discrete components. The calculator chip and this logic together count events as signaled by an external count pulse, incrementing the display by 1, 2, or any integer up to 9.

The negative-going leading edge of each count pulse triggers a 555 timer connected as a monostable multivibrator, generating a pulse about 15 milliseconds long. This is long enough for the six digit outputs of the chip to complete many full scans, connecting what looks to the calculator like a key depression to one of the keyboard inputs. (In normal operation, a key depression is usually much longer than 15 ms because of human reaction time, and the corresponding digit entry is made in the calculator chip many times.) The "key" in this case is a hard-wired connection from one of the digit outputs to a NAND gate-inverter combination, and another is a hard-wired connection from the inverter to one of the keyboard inputs, in accordance with the table. By this means, the counting increment is entered into the calculator.

The end of the 15-ms pulse triggers a second timer that forces a delay during which the calculator can become stable after receiving the "key depression." (In normal operation, this delay is created as the user moves a finger from one key to another.) At the end of this delay, the third timer is triggered to produce a pulse that gates the digit output d_4 into the keyboard input k_3 to enter what the calculator sees as an instruction to add. Thus, for every incoming count pulse, the calculator chip adds the wired-in increment to the previous total and displays the result.

Normally, to clear this calculator, the clear button on the keyboard is pressed twice. To provide time to clear



Calculator counter. Logic blocks take the place of a keyboard to provide appropriate signals for the single-chip calculator, MM 5736, to serve as a simple counter. It costs less than the collection of discrete devices that otherwise would be required.

the counter, the reset pulse must be held low for at least 60 ms. During that time, an astable multivibrator assembled from another NAND gate, an inverter, a resistor, and a capacitor, provides at least two connections of digit output d_1 to keyboard input k_3. Since this is the same input used by the "add" pseudo-instruction, two diodes create the equivalent of an OR gate in front of k_3.

The counter can be expanded to count either up or down by removing the inverter following NAND gate 3 and inserting, before the gate, two three-input NANDs, as shown in the inset of the diagram. This connects either d_4 to k_3 to count up, as in the main diagram, or d_3 to k_3 to count down, controlled by a single additional logic input that specifies the direction of counting. This input has to be inverted to provide the proper level at both the three-input gates; the removed inverter can be used for this function.

The whole counter can be built for $15 to $20, an economical substitute for the six discrete counters and six decoder/drivers that would otherwise be required. □

12. Current sources

Controlled current source is versatile and precise

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz.

A precision voltage-controlled current source can be made by placing a pair of complementary field-effect transistors in the feedback loop of an operational amplifier. The resulting circuit will have a differential input, as well as a bipolar output current that can be used to drive either grounded or floating loads. From signals of up to ±10 volts, the circuit develops a ±10-milliampere output, accurate to within ±0.01%.

Signal voltages are usually derived from control voltages, but sometimes it is better to derive signal currents from the control voltages for either testing or driving certain loads. For example, a voltage-controlled current source can provide a simple programmable bias current for transistor testing.[1] Or it can be used for resistance measurement, since contact resistance will not affect the test signal supplied by a current source. A current output is also needed for process-control instrumentation or for driving a meter or a dc torque motor.

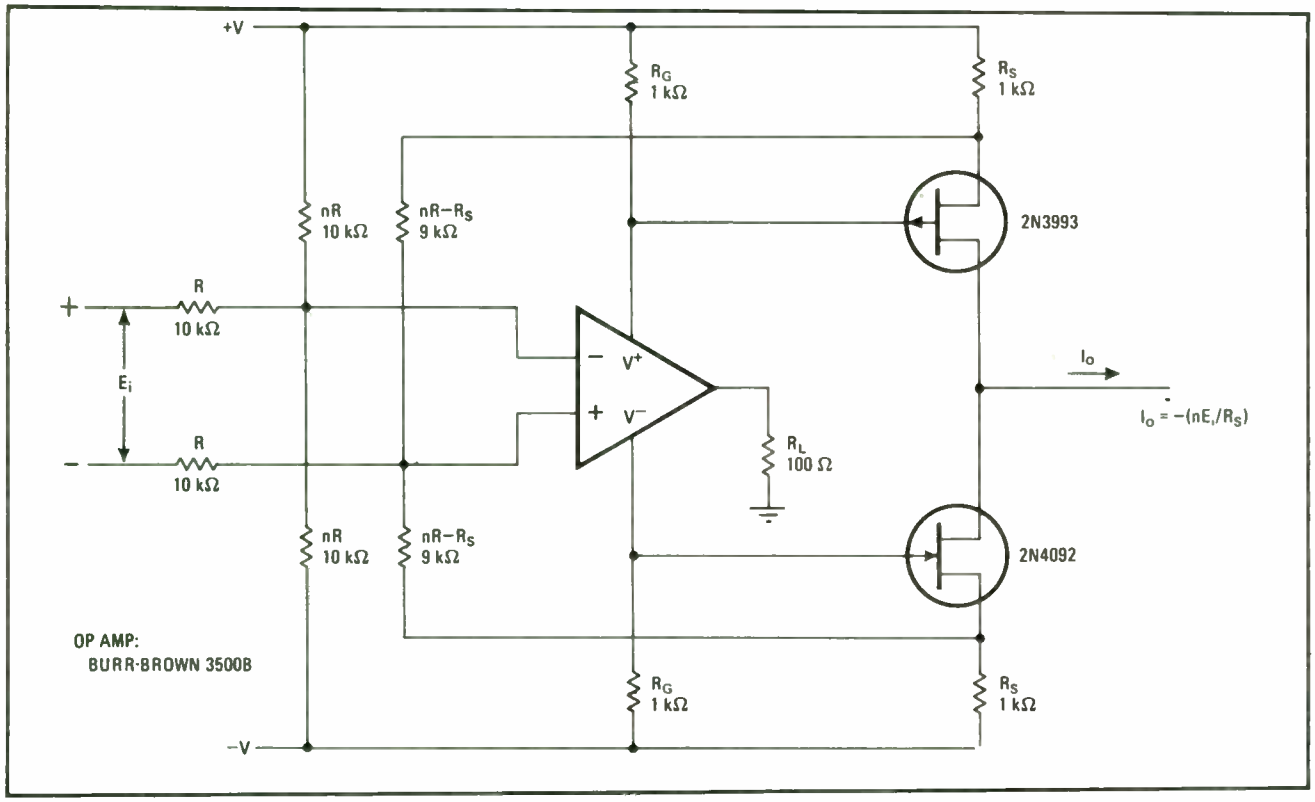
These varying applications may involve unipolar or bipolar output currents, single-ended or differential inputs, grounded or floating loads or sources, and varying degrees of accuracy. The circuit shown in the diagram can satisfy all of these requirements, and it is simpler than many previous not-as-versatile current sources.[1,2]

The circuit here consists of opposing FET current sources that are controlled by high-gain feedback around an op amp. The difference in FET currents produces the output current, and this difference current is controlled by summing the feedback, at the amplifier input, from the current-sensing source resistors (R_S). At feedback equilibrium, the sum of the two feedback signals is directly related to the differential input signal. The circuit's output current is given by:

$$I_o = -nE_i/R_S$$

where n represents the desired resistance-ratio factor.

Differential inputs and high power-supply rejection are provided by an attenuator network at the inverting amplifier input; it matches the feedback network con-



Current drive. Voltage-controlled current source can accept a single-ended or differential input, supply a unipolar or bipolar output, and handle a grounded or floating load or source. The difference current developed by the complementary FETs is sensed by resistors R_S and fed back to the amplifier input, where it is summed with the input signal voltage. Both FET gates are driven from the op-amp supply terminals.

nected to the other amplifier input. This is analogous to the matched input and feedback networks connected to an op amp to form the common difference amplifier.[2]

To simplify biasing and improve large-signal bandwidth, the gates of both FETs are driven from the op-amp supply terminals, rather than from the op-amp output terminal. Quiescent biasing for the FETs is obtained from the quiescent current drains of the op amp, and no level-shifting bias must be set up from the amplifer to the FETs.

Large-signal bandwidth is also improved by the reduced output swing required from the amplifier. Only a 1-volt swing is needed across amplifier load resistor R_L to obtain the rated output current, which is drawn through the supply terminals for maximum drive to the FETs.

Additionally, the lower amplifier output swing is not as greatly bandwidth-limited by the amplifier slewing-rate limit, as it is in other designs. Optimum bandwidth is achieved by making resistor R_L small enough to limit output swing without excessively lowering amplifier gain. Large-signal bandwidth is then limited by the amplifier's maximum common-mode swing rate.

The circuit's output current is controlled by the input voltage to within the accuracies of the resistors selected and within the gain-bandwidth and power-supply-rejection limitations of the op amp used. Most accuracy limitations caused by the FETs are overcome by the feedback, except for the small contributions from gate-drain leakage currents.

Output current is limited to the I_{DSS} level of the FETs but can be boosted by using the transconductance multiplying technique sometimes employed for common FET controlled current sources.[1] Output impedance is multiplied, through the feedback, from that of the FETs to the practical limit imposed by stray and parasitic effects—it is around 10^{12} ohms shunted by 10 picofarads.

By virtue of the circuit's differential inputs, common-mode signals are eliminated by a common-mode rejection that is adjustable to over 90 decibels. The primary common-mode-rejection limitations are the accuracies of the resistor ratios and the resistor matches, except for the noncritical match between the FET gate resistors (R_G).

The common-mode rejection can be adjusted by trimming the input resistors. Prior to this adjustment, any desired nulling of dc offset voltage should be performed by trimming the resistors denoted as nR. □

REFERENCES

1 J. Graeme, "Applications of Operational Amplifiers—Third Generation Techniques," McGraw-Hill, New York, 1973.

2. G. Tobey, J. Graeme, and L. Huelsman, "Operational Amplifiers—Design and Applications," McGraw-Hill, New York, 1971.

Bilateral current source is digitally programable

by Andrew Olesin

Soltek, Montrose, Colo.

Engineers use adjustable current sources for measuring device characteristics such as transistor beta or diode-breakdown voltage. To automate the procedure, a digitally controlled current source that can be programed for currents of ±1 nanoampere to ±1 milliampere can be made from two operational amplifiers and a multiplexer. The digital inputs can be directly driven by transistor-transistor logic or complementary-MOS, and the polarity of the input voltage determines whether the circuit is a current source or a current sink.

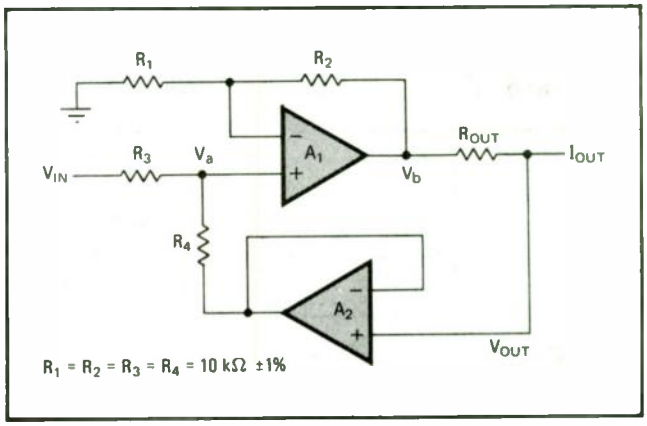
The basic bilateral current source is shown in Fig. 1. Operational amplifier A_2 is a high-input-impedance voltage follower that drives the node where voltages V_{IN} and V_{OUT} are summed. The node voltages are

$$V_a = (V_{OUT} + V_{IN})/2$$
$$V_b = V_a[1 + (R_2/R_1)] = 2\,V_a = V_{OUT} + V_{IN}$$

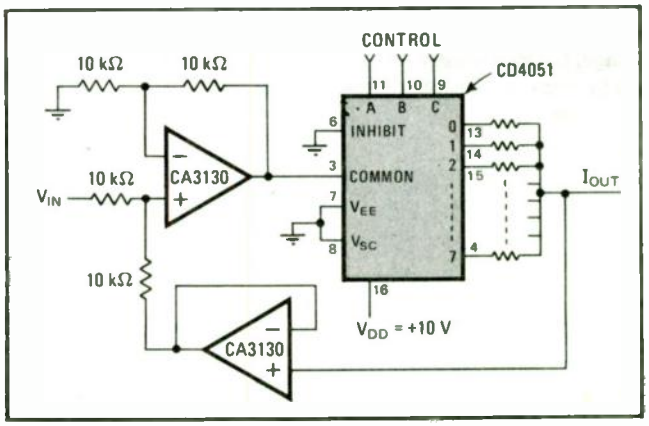
This last equation shows that the voltage across resistor R_{OUT} equals V_{IN}; therefore, because A_2 has a high input impedance,

$$I_{OUT} = V_{IN}/R_{OUT}$$

Maximum output current is limited by the current available from op amp A_1 at its maximum output voltage



1. Current source. Basic circuit provides output current of V_{IN}/R_{OUT}. Direction of current is given by sign of V_{IN}. Resistance R_{OUT} can be made digitally adjustable, as shown in Fig. 2.



2. Programable. C-MOS multiplexer connects various resistors into circuit to serve as R_{OUT}. Thus current is adjusted by digital control.

age. The minimum current is governed by the input current of A_2, which should be less than 1% of the minimum current from the source.

Although the circuit will function well with any general-purpose operational amplifier, the CA3130 C-MOS/bipolar op amp is especially suited for this application because of its field-effect-transistor input, full voltage output swing, and low cost.

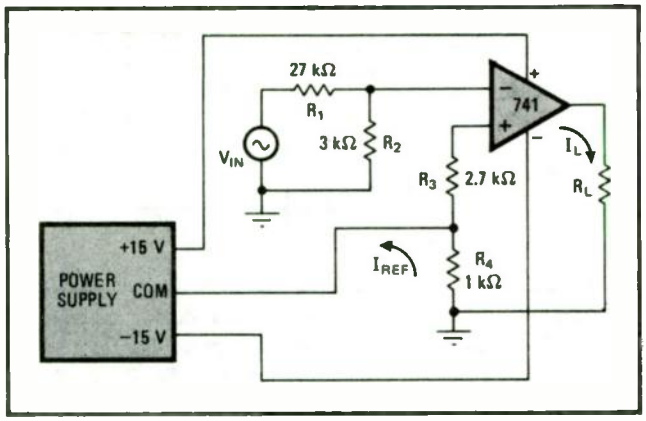
Programable current ranges are obtained by inserting one or more CD4051 C-MOS analog multiplexers in series with resistors of selected values, as shown in Fig. 2. The CD4051 multiplexer has internal level-shift circuitry to accommodate different logic families.

For the higher current ranges (R_{OUT} less than 10 kilohms), it may be necessary to take the on resistance of the switches into account by adjusting the combined resistance of the switch and resistor to yield accurate currents. If V_{IN} is less than ±0.5 V, the op-amp input-offset voltages should be nulled. □

Controllable current source eliminates matched resistors

by James A. Stanko
State Univesity of New York, Stony Brook, N.Y.

A bipolar constant-current source that has a grounded voltage source and a grounded load is usually limited in accuracy and internal impedance by the degree of matching of two or more resistors. For the circuit below, however, no matched resistors are required; linearity and internal impedance are determined solely by the operational amplifier gain, offset, and power supply rejection ratio. This circuit takes advantage of the fact that the op amp's power supply can usually be floated.



Uncritical. Load current produced by this circuit depends on input voltage, not load resistance. Circuit does not require matched resistors for accurate control of current, but power supply must float.

To understand the operation of the circuit, remember that no current to speak of flows into the input terminals of the op amp under feedback conditions, and no voltage difference exists across the terminals. Thus, the op amp drives the common terminal of the power supply to the voltage level established at the inverting input. This voltage appears across the reference resistor R_4. It is set to a suitably low value by input attenuator R_1 and R_2 to avoid thermally induced errors caused by power dissipated in the reference resistor. The values of R_1 and R_2 are chosen to provide a convenient scale factor. The reference current thus established is exactly equal to the current flowing in the load, and therefore the load current is

$$I_L = -I_{ref} = -\frac{V_{in}}{R_4}\frac{R_2}{R_1 + R_2}$$

The value of load current does not depend upon the value of load resistance and can be controlled by the value of V_{in}.

The minus sign in the expression for load current indicates the degenerative feedback action of the circuit. If I_L increases, the extra voltage drop through R_4 drives the noninverting input of the op amp lower and thus decreases the output.

Resistor R_3 is made equal to the parallel combination of R_1 and R_2 to minimize any error caused by input bias current. For the values shown in the figure, input voltages up to ±10 volts produce current outputs up to ±10 milliamperes.

This circuit has been used for over a year to supply current to electromagnets. In this application it is boosted by an emitter follower for greater output current and more voltage compliance. □

13. Detectors

Simple gating circuit marks both pulse edges

by Ralph Tenny
Texas Instruments, Central Research Laboratories, Dallas, Texas

A bidirectional edge detector can be built from only two integrated-circuit packages—or with only one package if exclusive-OR gates are used. Applications for the circuit include triggering for event counters and frequency doubling for digital data communications.

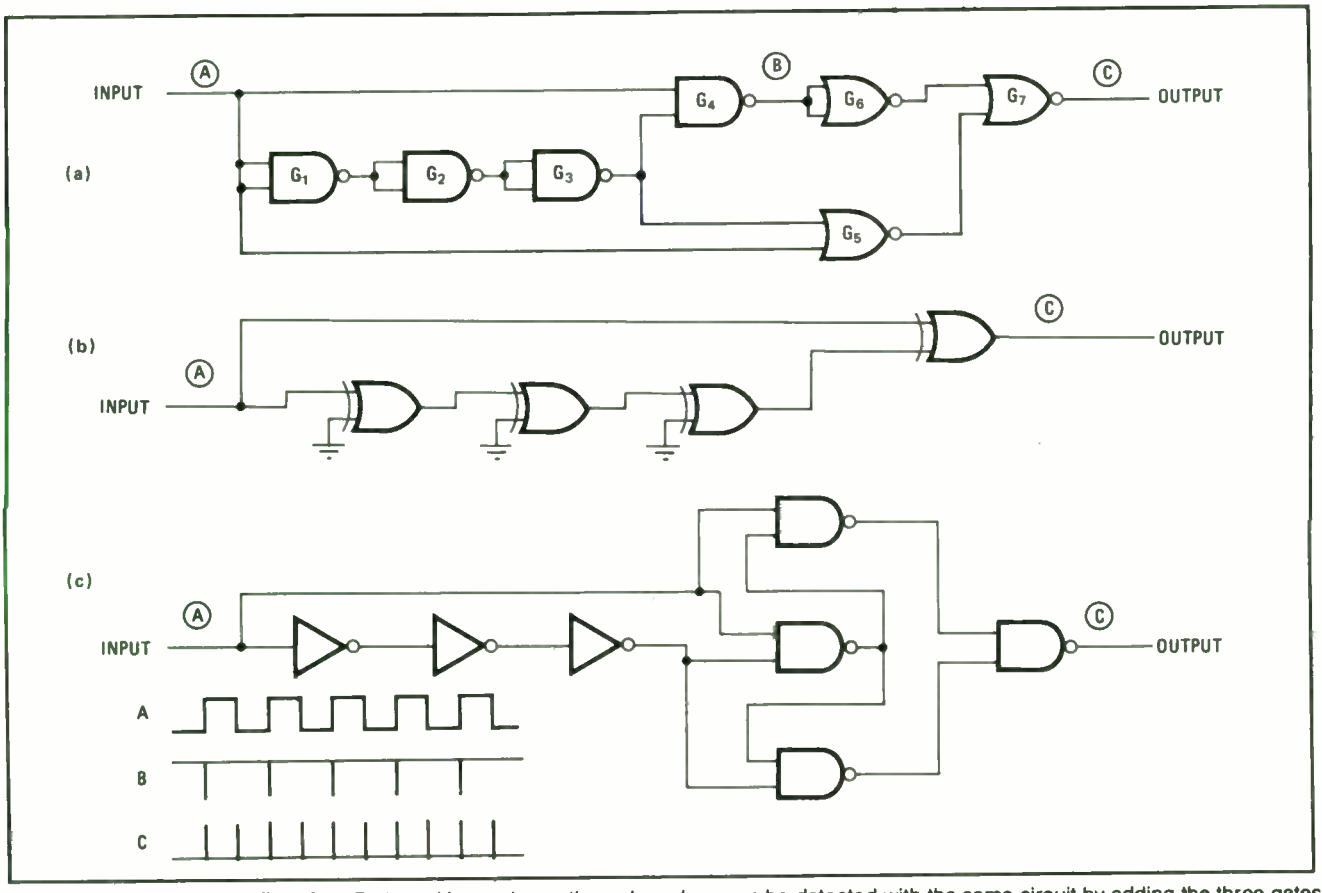
The configuration for the standard edge detector is drawn in black in (a). If NAND gates are used, as indicated here, the circuit responds to positive-going edges. If NOR gates are used, it detects negative-going edges.

When the input signal is low, the output of gate G_4 will be high. And when the input becomes high, G_4's output goes low one gate propagation delay later. Meanwhile, the input signal ripples through gates G_1, G_2, and G_3, causing G_3's output to go low after three gate delays. The output of G_4 then become high again one gate delay later. This means that G_4's output is a negative pulse that is three gate delays wide. The four gates, therefore, mark the positive-going edges of the input.

Adding three NOR gates to this standard circuit, as shown in color in (a), enables the circuit to mark both positive and negative edges. Gate G_5, together with gates G_1, G_2, and G_3, form a negative-edge detector. Gate G_6 simply inverts the output from gate G_4, while gate G_7 simply sums and inverts the detected edges.

The same dual edge detection can be obtained from a single quad exclusive-OR gate package when the gates are connected as indicated in (b). Or, an equivalent circuit can be constructed by hooking up three inverters and four NAND gates, as in (c).

The timing diagram shows the key waveforms for all the circuits. □



Noting each pulse-edge direction. Both positive and negative pulse edges can be detected with the same circuit by adding the three gates drawn in color in (a) to a standard unidirectional edge detector (drawn in black) If exclusive-OR gates are used, as in (b), the bidirectional edge detector requires only one IC package. Inverters and NAND gates, as in (c), can also provide the same circuit function.

Differentiate and count to find frequency error

by Robert C. Rogers
Texas A&M University, College Station, Texas

By counting differential pulse transitions for a known period, a simple error-detection circuit measures the frequency difference between a variable square wave and reference square wave. Usually, frequency error is found by counting both signals for some fixed period and then comparing the resultant values, or by mixing the signals and then counting the beat frequency. The first method often requires a considerable amount of digital logic if high-frequency signals are involved, while the second method is generally limited by the passband of the beat-frequency detector.

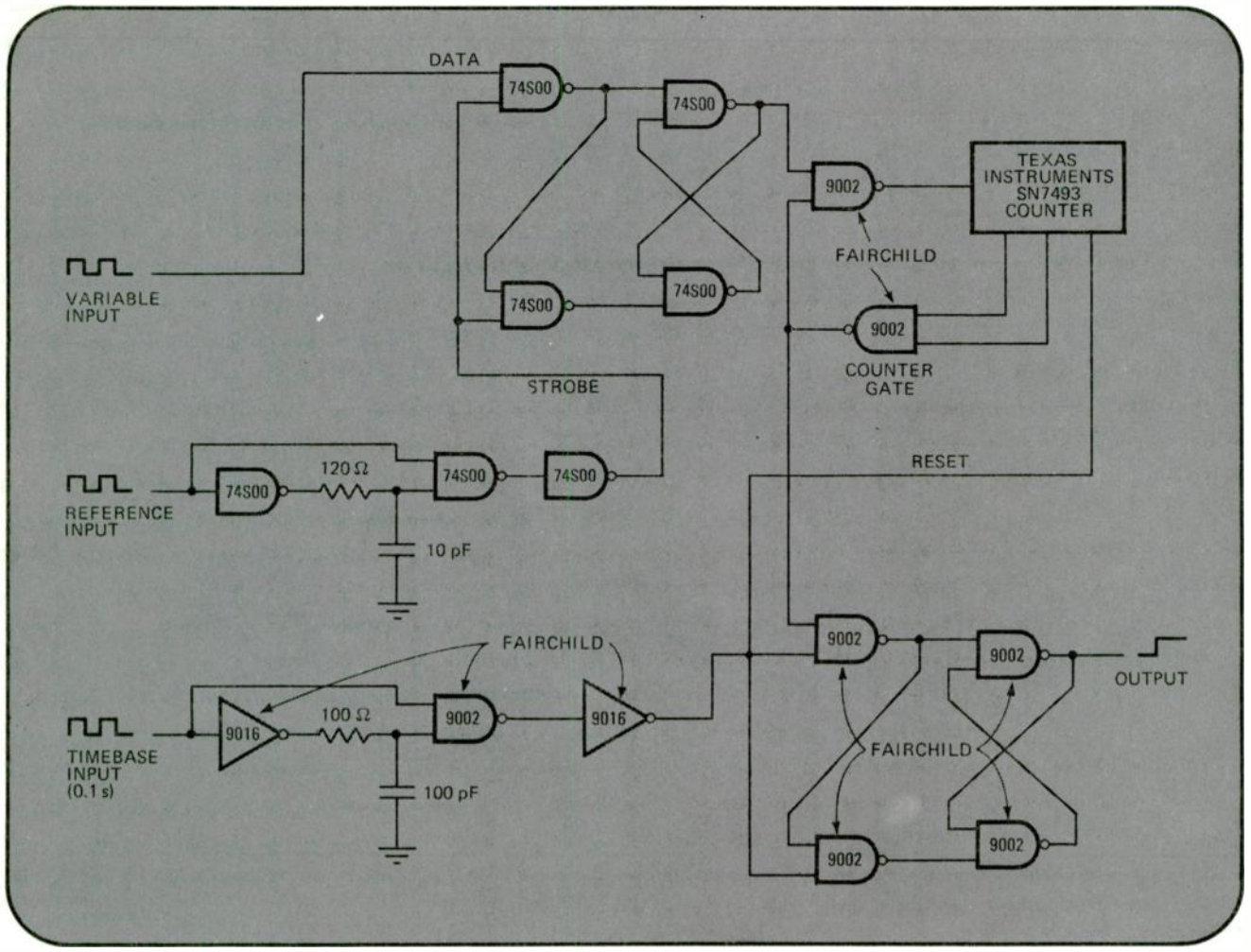
The frequency error detector shown requires input signals that are compatible with logic circuits. (A zero crossover detector could be used initially to prepare the inputs.) The reference square wave is differentiated and applied to the strobe input of a latch, and the variable square wave is applied to the data input of the latch.

How many positive or negative transitions the latch output makes in a given period represents the number of times the variable frequency has gained or lost a full cycle relative to the reference. Counting these transitions for a known period, then, yields the total frequency error during that period. A high-level output indicates that the variable is within the limit.

The time-base input signal sets the latch to a logic 1 if the four-bit counter does not reach a value of 10 in the preceding 0.1-second timing interval. This signal is also used to reset the counter for the next counting period, which begins when the reset pulse returns to zero.

There are two drawbacks that should be remembered. The detector fails if the variable frequency becomes identical to the reference in both frequency and phase, and it becomes ambiguous when the variable frequency is either a higher or lower harmonic of the reference. However, even with these limitations, the detector is useful and reliable over the reference range of 5 to 20 megahertz. Error limit for the circuit shown is ±100 hertz and can be changed by altering the number detected by the counter gate. □

Frequency error detector. Differentiated reference square wave drives latch strobe input; variable square wave feeds latch data input. Counter logs either positive or negative transitions of latch output for specific period to total frequency error between inputs. High circuit output indicates error is within desired limit. Time-base signal sets latch and resets counter. Detector range is 5 to 20 MHz for ±100 Hz.



Frequency discriminator uses one-shot and flip-flop

by Peter Alfke
Fairchild Semiconductor, Mountain View, Calif.

A frequency discriminator that is accurate to within about 3% can be built inexpensively with only two integrated-circuit packages. The circuit, which is intended for industrial-control and communications applications, senses whether an incoming frequency falls within a predetermined band, or if the frequency is lower or higher than the band.

A dual retriggerable monostable and a dual flip-flop are the two IC packages. The positive-going edge of the incoming signal clocks both flip-flops and triggers the first monostable, M_1. When this monostable, which has an "on" time of approximately $0.31R_1C_1$, completes its timing cycle, it triggers the second monostable, M_2, which has an approximate "on" time of $0.31R_2C_2$.

For a low incoming frequency, both monostables have completed their timing cycles before the next positive-going edge of the input occurs. The next edge, then, sets flip-flop FF_1 and resets flip-flop FF_2 (Q_1 and $\bar{Q}_2$ outputs go high), indicating that the incoming frequency is below the design band:

$$f_L = 1/[0.31(R_1C_1 + R_2C_2)]$$

If the input frequency is increased, the next leading edge occurs while the output from monostable M_2 is still high, so that both FF_1 and FF_2 are set (Q_1 and Q_2 outputs go high). This indicates the incoming frequency is within the design band.

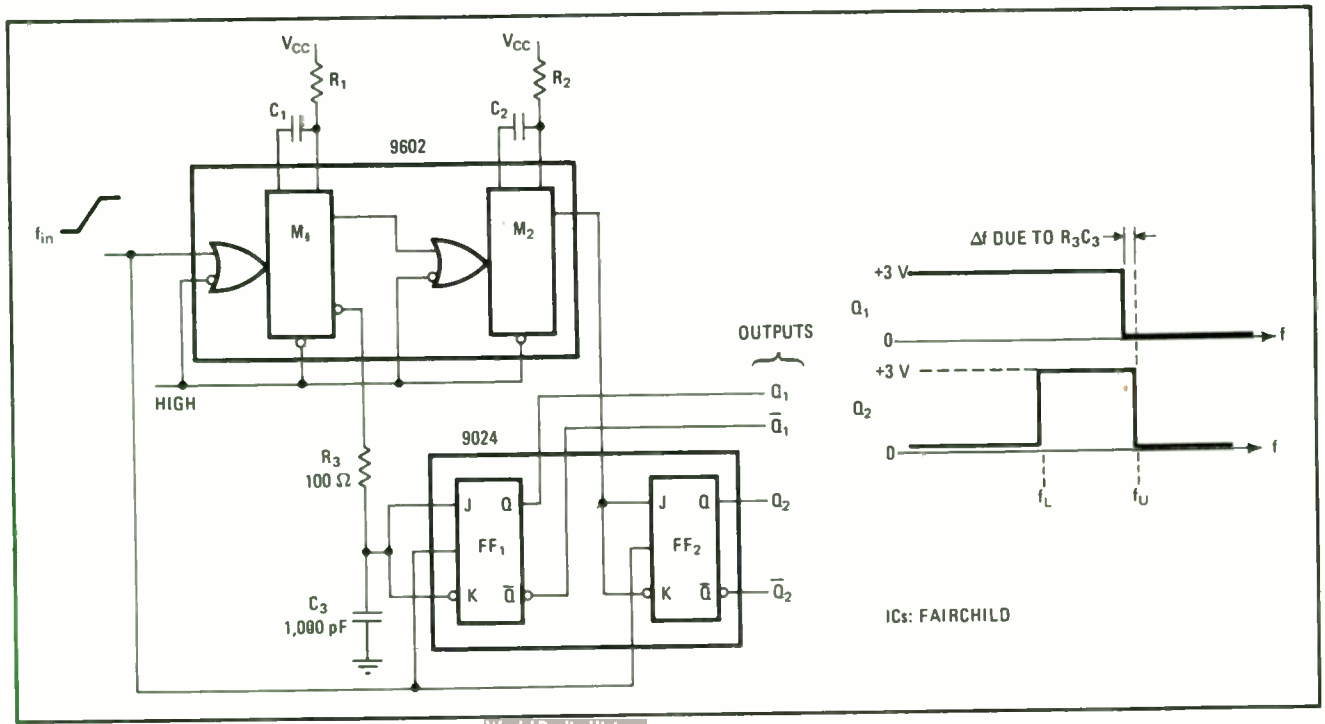
Increasing the input frequency further causes the next leading edge to occur before monostable M_1 has finished its timing cycle, beginning a new period for this retriggerable monostable. The continuing output from M_1 prevents monostable M_2 from triggering so that both flip-flops are reset ($\bar{Q}_1$ and $\bar{Q}_2$ outputs go high). This means that the incoming frequency is higher than the design band:

$$f_U = 1/0.31R_1C_1$$

The time constant (about 100 nanoseconds) established by resistor R_3 and capacitor C_3 makes the setup time of flip-flop FF_1 longer than the trigger delay of monostable M_2. This assures that FF_1 will change state at a frequency that is slightly below, rather than above, upper band limit f_U, thereby avoiding ambiguous output codes around f_U.

The circuit's frequency response is limited to a few megahertz because of the inherent delays of the monostables. Whenever the range of operating frequency permits, type 96L02 monostables should be used because they offer better temperature stability than the type 9602 devices. (The 74121 multivibrator cannot be used here because of its duty-cycle limitations.) □

Monitoring frequency. A couple of retriggerable monostables and flip-flops can be connected as a fairly accurate low-cost frequency discriminator. Lower and upper band limits are determined by the monostables' timing circuits. For in-band inputs, outputs Q_1 and Q_2 are high; for low frequencies, Q_1 and $\bar{Q}_2$ are high; and for high frequencies, $\bar{Q}_1$ and $\bar{Q}_2$ are high. The R_3C_3 delay avoids ambiguity at the upper limit.



Schottky diode pair makes an rf detector stable

by Roland J. Turner
AEL Communications Corp., Lansdale, Pa.

If broadband rf detection is to be efficient at low signal levels, detection thresholds must be stable—a design goal achievable with a pair of matched Schottky diodes. The diode-stabilized circuit shown here, for instance, maintains a detection stability of ±0.06 decibel over a temperature range of −20°C to +90°C for an rf drive level that is a 10th of that of a conventional detector.

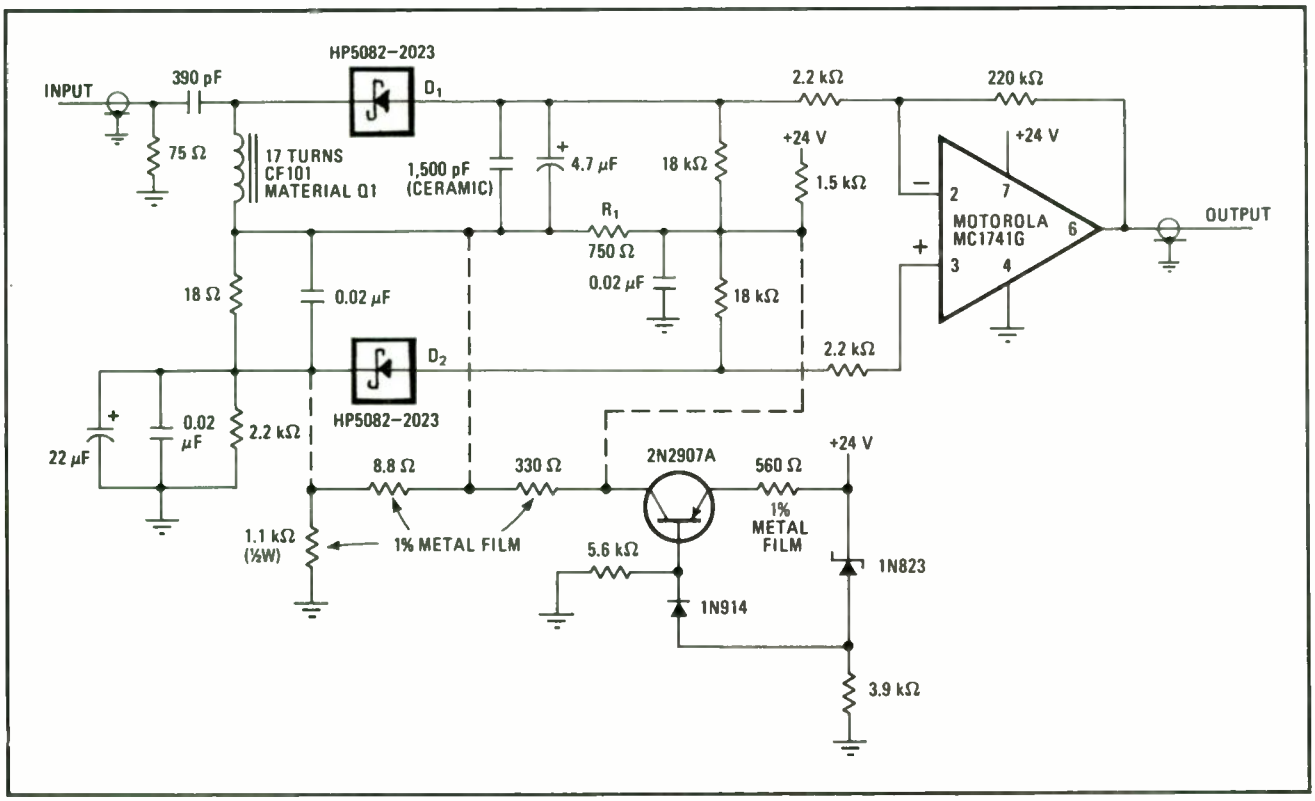
With such a circuit, the amount of rf circuitry required can be much reduced because accurate stabilized detection thresholds can be set for low rf drive levels. Also, the circuit's temperature stability and detection efficiency permit the realization of a sensitive receiver—one that can have a high video gain as well as a low rf gain.

Normally, it is hard to achieve high detection efficiency at a low rf drive level while keeping detection efficiency constant over a wide temperature range. This is because of the nature of the forward blocking voltage of a diode. For example, at room temperature, a silicon diode has a forward voltage of about 500 millivolts and a temperature coefficient of 2 mV/°C, so that the forward voltage will vary considerably—from 370 mV at 90°C to 590 mV at −20°C.

The rf drive level needed to start the detection action must exceed the diode's forward blocking voltage so that load current may flow. However, since the forward voltage changes by 220 mV from −20°C to +90°C, the rf drive level required must vary accordingly to maintain detection action. The inherent detection efficiency, therefore, is low and strongly dependent on temperature, limiting the maximum video gain that may follow the detector.

The rf detector depicted here, though, solves these problems. The two Schottky diodes, D_1 and D_2, are matched to within 5 mV from 0.1 to 0.5 milliampere and are connected in a half-wave rf detector configuration. The dc bias developed across diode D_2 and resistor R_1 serves as an arming bias for the detector diode, D_1, establishing temperature tracking between the two diodes.

The voltage drop across resistor R_1 establishes a reverse offset bias on diode D_1, in this way setting a known rf threshold that the rf drive level must exceed before detection action takes place. And the voltage drop across diode D_2 acts as a temperature-dependent forward arming bias on diode D_1. The level of this arm-



Temperature stabilized. High-efficiency rf detector operates at low input drive levels over a wide temperature range. Matched Schottky diodes (D_1 and D_2) and a fixed rf threshold bias (via resistor R_1) permit the circuit to hold voltage detection stability to ±0.06 dB from −20°C to +90°C for a 55-mV input. Sensitivity to supply-voltage changes can be minimized by adding colored network (and omitting R_1).

ing bias tracks the forward blocking voltage of diode D_1 as the temperature changes.

Because of this temperature-compensating arming bias, it is possible to realize constant detection efficiency over a wide temperature range, in addition to a constant rf threshold detection level. For a constant rf input of 55 mV, the detection voltage developed by the circuit varies only 1.8 mV between -20°C and +90°C. Rf peak voltages as large as 80 mV can be detected quite efficiently.

The operational amplifier at the output of the circuit senses the detection voltage and translates it to a 12-volt level. This output voltage varies only 2.1% from -20°C to +90°C for a constant rf input drive. Here, the op amp's gain is 40 dB, a figure that can be safely increased to 50 dB without adversely affecting the output stability of the circuit.

The circuit's performance will be further enhanced if the detector is made insensitive to variations in supply voltage. This can be done by adding a current source (shown in color in the diagram). The current source keeps the rf threshold voltage constant, despite supply variations of ±0.5 V. In connecting this source, resistor R_1 must be omitted. □

Temperature-stable decoder for modulated pulse widths

by H.R. Beurrier
Bell Telephone Laboratories, Murray Hill, N.J.

Besides offering exceptional temperature stability, a pulse-width-modulation decoder for remote proportional radio control produces a presettable fail-safe analog output when the input control signal is interrupted. The circuit converts a time-modulated pulse input to an analog output.

Transistors Q_1 and Q_2 form a sawtooth generator with a ramp output that starts when the input control signal goes positive and that resets when the input goes negative. The control signal switches Q_2 alternately on and off.

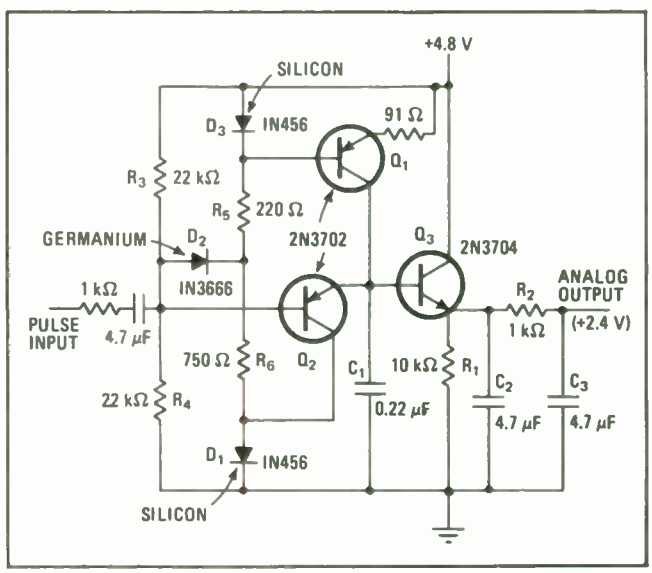
When the base of Q_2 is driven positive by the input, this transistor turns off and capacitor C_1 charges with the constant current supplied by transistor Q_1. (The longer the input pulse duration, the higher C_1's ramp voltage and the resulting output voltage.) When Q_2 is driven negative, it conducts, pulling its emitter voltage in the negative direction and partially discharging capacitor C_1.

Emitter-follower Q_3 acts as a peak-voltage detector that charges capacitor C_2 positively when its base is driven positive by the ramp voltage of capacitor C_1. If the voltage across C_1 is too negative to forward-bias the base-emitter junction of Q_3, capacitor C_2 discharges through resistor R_1. This portion of the circuit, therefore, acts as a diode peak detector with power gain. Resistor R_2 and capacitor C_3 are connected as a simple first-order output filter.

Once the input signal is terminated, the base voltage of transistor Q_2 settles to a level determined by the voltage divider of resistors R_3 and R_4. This voltage level is coupled to the output through transistors Q_2 and Q_3, which are connected as cascaded emitter-followers. The complementary arrangement of Q_2 and Q_3 causes any temperature-induced change in the base-emitter voltage of transistor Q_2 to be cancelled by an equal-in-magnitude, but opposite-in-polarity, change in the base-emitter voltage of transistor Q_3.

The circuit's output voltage is referenced to the lower point of capacitor C_1's charge/discharge cycle. When the input is negative, diode D_1 reverse-biases transistor Q_2's collector so that capacitor C_1 always discharges to the same level. Diode D_2 and resistors R_5 and R_6 clamp the capacitively coupled input control signal so that transistor Q_2's base is driven slightly negative. Diode D_3 simply fixes the base voltage of transistor Q_1.

With the component values shown, the circuit will convert a pulse width of 1.25 ±0.63 milliseconds to an analog output of 2.4 ±0.6 volts dc. The 1-kilohm input resistor simply reduces the loading on the driving source. □



PWM decoder. Circuit detects pulse-width-modulated signals, supplying dc analog output over wide operating temperature range. If input control signal is interrupted, decoder output goes to preset fail-safe level. Transistors Q_1 and Q_2 and capacitor C_1 make up sawtooth generator that drives transistor Q_3, which acts as peak-voltage detector. Q_2 and Q_3 are cascaded complementary emitter-followers.

Video detector stores peak for minutes

by Stephen Hayes
Altadena, Calif.

In slow-scan image processing, a video signal often must hold its peak value for longer than the few seconds provided by diode peak rectifiers. But a rectifier that can retain a peak value of a video signal for up to four minutes can be built from two operational amplifiers and two transistors, avoiding the cost and complexity of digital storage for a sample-and-hold circuit.

In the circuit shown in Fig. 1, the CA3100 op amp compares the input signal (between 0 and 6 volts) to the voltage on a 0.47-microfarad plastic capacitor. The output of the CA3100 is an amplified error signal used to adjust the charge on the storage capacitor.

The storage and output sections are conventional. A MOSFET operational amplifier, the CA3130, with the twin assets of low cost and low input bias current, acts as a unity-gain buffer between the capacitor and the output terminal. The 2.2-kilohm resistor lowers the output impedance from the very high level of the 3130.

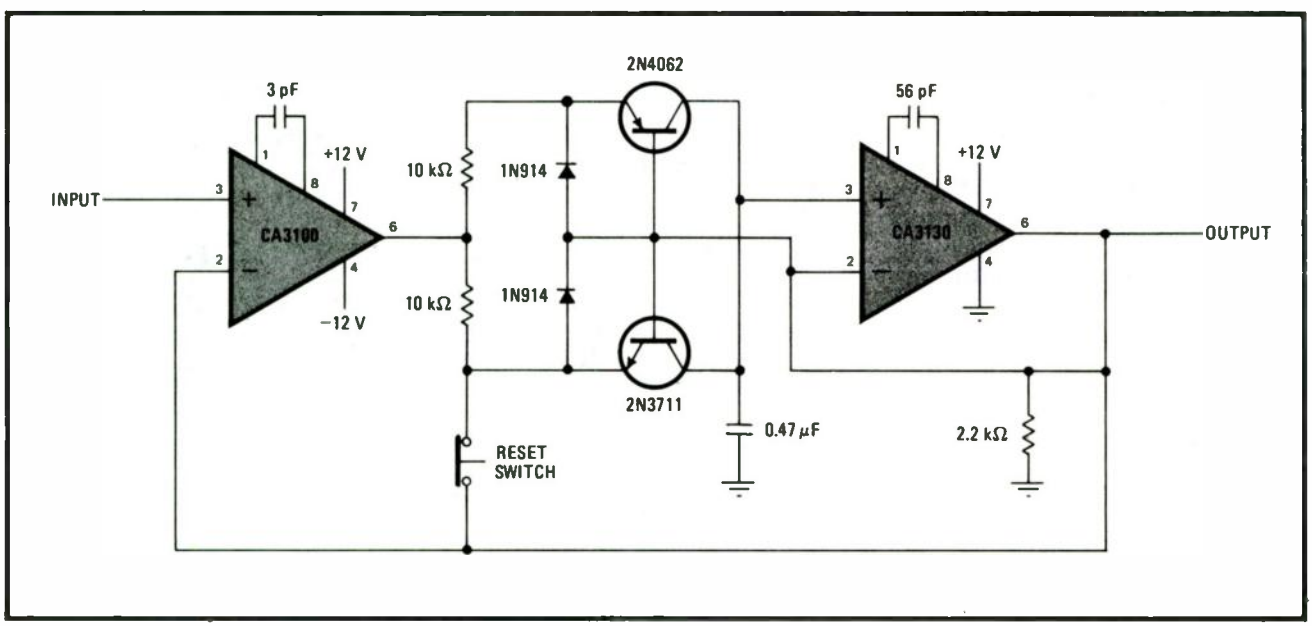
The key feature of the circuit is the unusual method of transferring charge into and out of the capacitor. Normally, a peak rectifier uses a series diode for this purpose. However, the diode has a reverse leakage current that is unpredictable, temperature-dependent, and often on the order of several nanoamperes. To avoid this leakage, the circuit shown uses the base-collector junction of a pnp transistor to transfer charge. The current is injected into the emitter, with the base connected to the output of the buffer amplifier. As a result, the base-collector voltage is close to zero, and collector leakage current is small.

An npn transistor is added to allow the capacitor to be discharged. Normally, this transistor does not conduct because its base-emitter junction is shorted by the switch. Thus, when the switch is closed, the output voltage (which is equal to the voltage across the capacitor) is determined by the most positive level applied to the input terminal. When the switch is open, the output voltage tracks the input signal (Fig. 2).

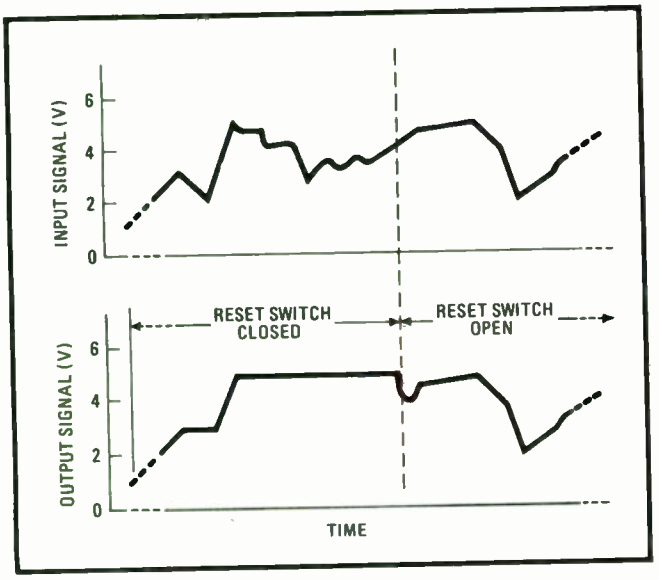
Holding performance of the circuit is quite good. If a 3-V signal is applied and removed, the output decays less than 10 millivolts in 10 minutes. This implies that the total leakage current into the capacitor is less than 10 picoamperes.

A drawback is the low slew rate. The minimum slew rate is set by the 10-kilohm resistors, the 0.47-μF capacitor, and the difference between the maximum output voltage of the CA3100 and the maximum signal voltage. With a 6-V input signal, the slew rate is about 850 V/s.

Several variations on the circuit are possible. The switch could be replaced by an electronically controlled device, such as a relay or a CD4016 complementary-metal-oxide-semiconductor transfer gate. This change



1. Stores maximum level. Peak detector circuit accepts analog input signals of 0 to 6 V in amplitude, provides output level that is maximum value of input. Use of pnp transistor for rectification minimizes charge leakage from capacitor, so peak level can be held for several minutes. Switch and npn transistor allow circuit to be reset. While reset switch is open, output signal follows input signal. If the reset switch is relocated to short the emitter to the base on the pnp transistor, the circuit is a minimum level detector, storing the lowest level of the input signal.



2. Holding the peak. Output from circuit of Fig. 1 is the highest level that has been applied to the input since switch was closed. If switch is opened, output slews down to input level, and then follows input. Circuit was developed for determining dynamic range of low-bandwidth scanning signal from an electron microscope, but is useful for any peak rectifier that requires low decay rate.

would allow electronic control of the reset function.

If the switch is moved to the emitter of the npn transistor, the circuit stores the lowest level of the input signal. If switches are placed in both locations, the circuit can function in four modes: tracking (both switches open), positive peak detector, minimum level detector, and holding (both switches closed).

By using both a positive peak detector and a minimum level detector in a circuit, maximum and minimum voltage levels can be stored for such purposes as setting the gains of variable-gain amplifiers, or storing the levels of transient peaks in a signal. □

LED display shows beat frequency

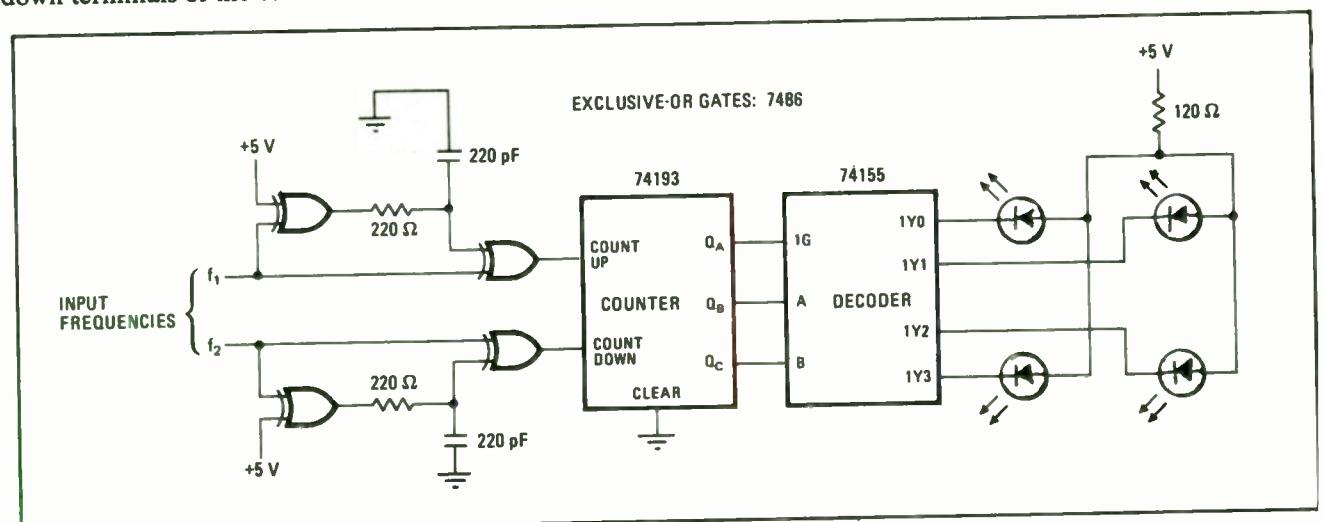
by Sergio Franco
Oberlin College, Oberlin, Ohio

A simple, easy-to-use beat-frequency indicator can be built at a cost of only about $5. The circuit, which employs four light-emitting diodes as its display, can be used in a variety of applications, but is particularly suited to the tuning of musical instruments.

The heart of the circuit is a 4-bit synchronous up/down binary counter. After undergoing proper shaping by exclusive-OR gates, input frequencies f_1 and f_2 are applied, respectively, to the count-up and count-down terminals of the counter. The net count, therefore, will be in either the up or the down direction, depending on whether f_1 is greater than or less than f_2. When f_1 equals f_2, the counter alternates between two consecutive states, producing a net count of zero.

These three input conditions can be easily displayed by means of four LEDs arranged in a circle. (A decoder is used to drive the LEDs from the counter output lines.) Only one LED is on at a time. Therefore, when f_1 is greater than f_2, a dot of light is produced that rotates clockwise; when f_1 is less than f_2, the dot rotates counterclockwise; and when f_1 equals f_2, there is no rotation.

Furthermore, since the exclusive-OR shaping network produces a sharp negative pulse for each transition of the two inputs, the dot of light moves one step for every beat. The rate of apparent rotation of the dot, then, is an exact indication of the beat frequency. □



LEDs show the beat. Economical circuit displays the difference frequency between its two inputs, as well as indicating their relative magnitude. Since only one LED conducts at a time, what is displayed is a dot of light. The dot rotates clockwise when f_1 is greater than f_2 and counterclockwise when f_1 is smaller. The rate of rotation is the beat frequency. When f_1 equals f_2, the dot remains stationary.

Radiation monitor has linear output

by Paul Prazak, *Burr-Brown Research Corp., Tucson, Ariz.*, and Lt. William B. Scott, *Edwards AFB, Calif.*

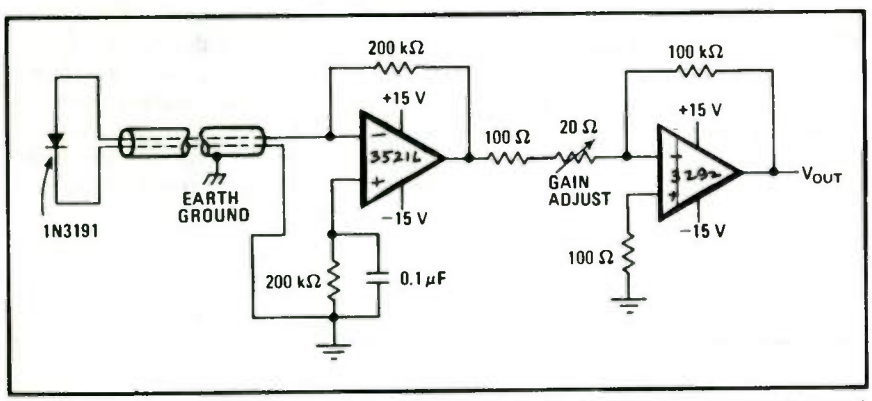
A commercial silicon diode can be used as a direct-reading detector of gamma rays and high-energy X rays in radiotherapy. Besides generating an output that is linearly proportional to the radiation intensity, the diode makes a small enough probe to map the radiation field accurately. The monitoring system of diode plus two operational amplifiers provides an output voltage that varies linearly from 0.1 volt to 10 v as the dose rate varies from 10 rads per minute to 1,000 rads/min.

The 1N3191 or other off-the-shelf diode is operated in a zero-bias short-circuit mode. Irradiation of the diode junction creates electrons and holes that are collected by the depletion gradient, producing a nanoampere current which is proportional to the intensity of the radiation.

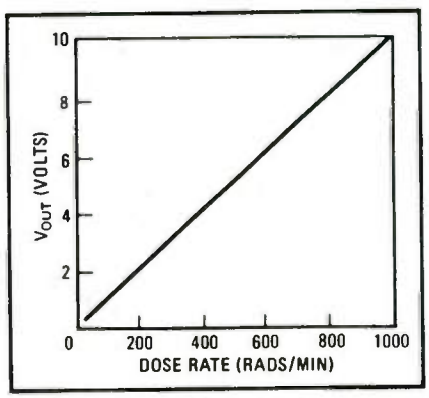
To amplify the small signal from the diode, a 3521L operational amplifier with low bias current (10 picoamperes maximum) and ultra-low offset voltage drift (±1 microvolt/°C maximum) is used. As shown in Fig. 1, the 3521L is connected in a current-to-voltage configuration where the inverting input appears as a virtual ground. This FET-input op amp delivers output voltages of 100 μv to 10 millivolts, which are well above the noise level. The 200-kilohm resistor between ground and the noninverting input serves to balance the amplifier, and the 0.1-microfarad capacitor stabilizes the amplifier by shunting out noise and preventing oscillations resulting from positive feedback.

An additional stage of gain amplifies the signal to the desired level. The offset-voltage drift of this stage must be extremely low because it is amplified along with the signal. Therefore the chopper-stabilized 3292 op amp, which has a maximum offset drift of only ±0.3 μV/°C is used here. The 100-ohm resistor again balances the inputs to the amplifier. The gain of this stage should be around 1,000; it is adjusted by means of the 20-ohm potentiometer so that an output voltage of 0.10 v to 10.00 v corresponds to a dose rate of 10 rads/min to 1,000 rads/min at the detector, as shown in Fig. 2.

The output voltage can be displayed on a 3½-digit panel meter, so that the numerals directly indicate radiation intensity. An alternative is to use an ultralinear voltage-to-frequency converter, an optical coupler, a counter, and a display to completely isolate the radiotherapy patient from the monitoring and recording system. An advantage of this approach is that the integrating input of the voltage/frequency converter would average out any high-frequency noise in the system. □



1. Dosage-rate meter. Commercial diode is detector in this highly accurate radiation monitor. Low-drift FET-input op amp amplifies detector current to usable level, and chopper-stabilized amplifier then provides additional gain while minimizing any error caused by ambient-temperature fluctuations. Gain is adjusted so that output voltage is 1% of incident radiation intensity in rads per minute; therefore voltage can be displayed on 3½-digit DVM for direct reading of dosage rate. Cost of parts for this monitor is about $90.



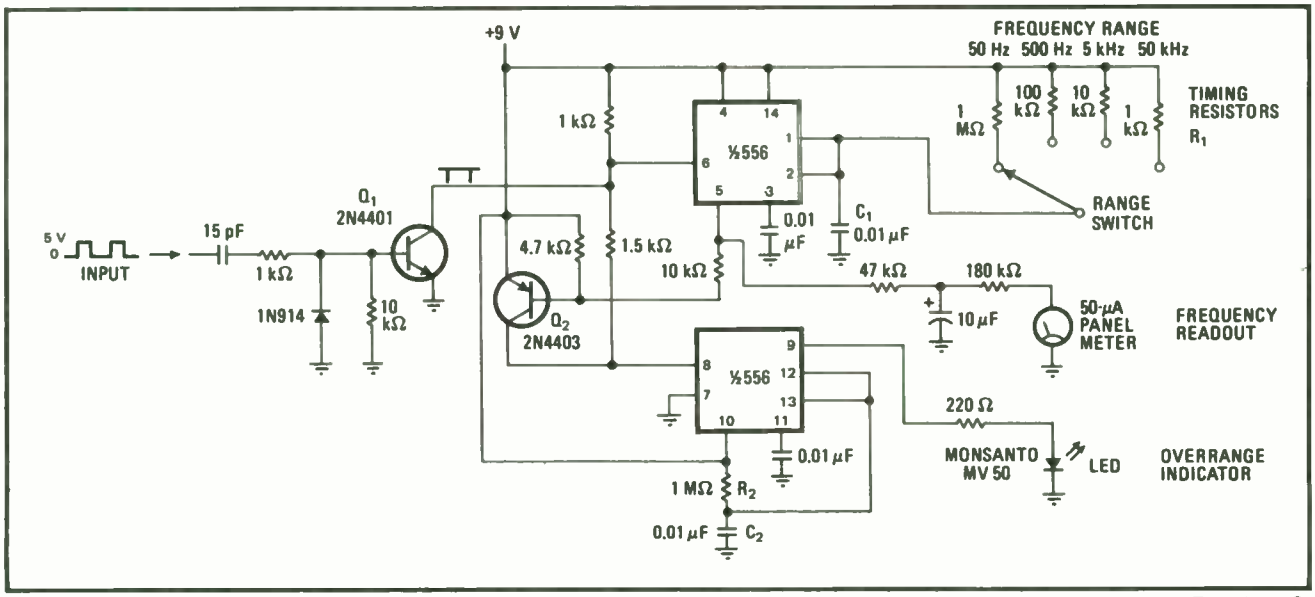
2. Linear response. Output voltage from monitor is linearly proportional to radiation intensity at diode. Over dosage rate range shown, total system error is less than 1%. Small size of diode probe permits accurate mapping of radiation field.

Overrange indicator can enhance frequency meter

by F. E. Hinkle
The Applied Research Laboratories, University of Texas, Austin, Texas

By making use of a 556 integrated circuit, which is composed of two 555 timers in a single package, an overrange indicator can be economically added to an analog frequency meter. A 555 can be used alone as a monostable multivibrator that is triggered by the frequency to be measured. To provide unambiguous measurements, however, the meter described here uses a second timer to flash a warning light whenever the input exceeds the maximum frequency setting. Although the technique of using monostables in analog frequency meters is not new, the use of new circuit developments makes the design economical and easy to implement.

When the range switch on this meter is set to the 50-



Unambiguous. Addition of overrange indicator to analog frequency meter warns when switch is set to wrong frequency range. Transistor Q_2 allows input signal to trigger LED monostable whenever input frequency is greater than meter range. Inexpensive and reliable circuit shown is useful from near dc to well over 20 kHz.

hertz range, any input frequency from near dc to 50 Hz causes a panel meter to read correctly; e.g., a frequency of 42 Hz produces a meter reading of 42 microamperes. However, the meter reading is incorrect when the input frequency exceeds 50 Hz, and therefore a light-emitting-diode overrange indicator flashes. If the range switch is then moved to a setting higher than the frequency, the LED stops flashing and the meter again indicates correctly. For example, a 300-Hz signal would be measured on the 500-Hz range, and the meter would show 30 microamperes.

In the meter diagramed here, the upper portion of the circuit measures the frequency and has the 50-μA panel meter as its readout. The lower portion provides the overrange indication and has the LED as its warning light. These two portions of the circuit are driven by a common input.

The input signal is a rectangular pulse train; the pulses are differentiated to produce the negative spikes that are needed to trigger the timer. For a sine-wave or sawtooth input signal, a Schmitt trigger might be used to generate the negative impulses.

When pin 6 of the frequency-measurement monostable is triggered, pin 5 goes high. It stays high and delivers current for a time equal to $1.1R_1C_1$. This positive output pulse appears once for every cycle of the input frequency (unless the trigger impulse arrives while the output at pin 5 is already high). The current pulses smoothed by the 10-microfarad capacitor, provide an average value that is shown on the microammeter.

At low frequencies, the output pulses are well separated, so the average current is low. At higher frequencies, however, they are closely spaced and approach a duty factor of about 95% at the upper frequency limit set by the range switch. Average current thus increases as the frequency increases. Resistors in the output circuit are chosen so that the average current is 50 μA at the maximum frequency in each range.

If the input frequency exceeds the meter range, a trigger spike arrives while the output is already high. As a result, that input cycle is not counted, so the frequency meter indication is erroneous.

To warn that trigger impulses are arriving while pin 5 is high, pin 5 is also connected to the base of pnp transistor Q_2. When pin 5 is low, Q_2 conducts and holds pin 8 high, thus preventing the warning-indicator monostable from being triggered. But when pin 5 is high, Q_2 is turned off; a negative input spike that reaches pin 8 therefore can trigger an output from pin 9 that flashes the LED. The duration of the flash is $1.1R_2C_2$. □

14. Digital-analog converters

Logic driving gates double as d-a converter switches

by Amos Wilnai
Monolithic Memories Inc., Sunnyvale, Calif.

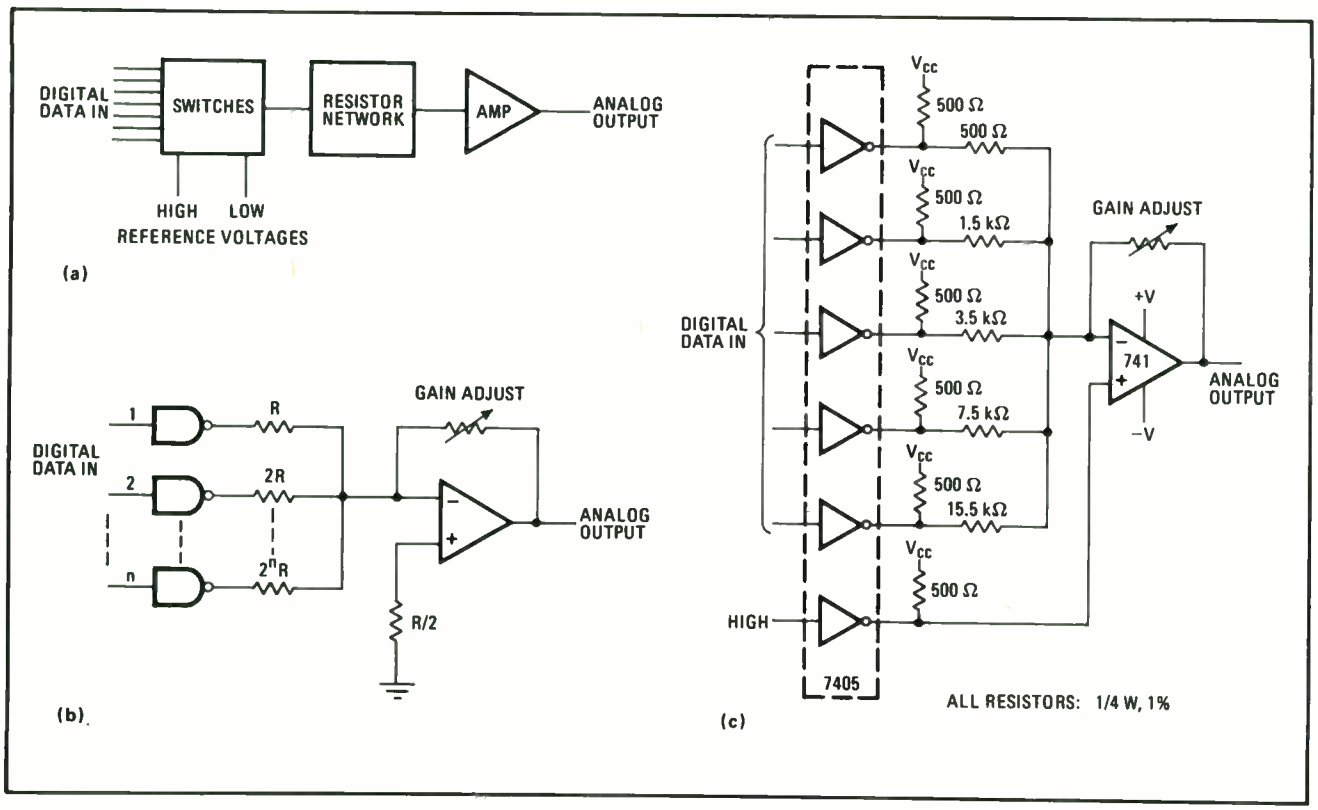
The design of a weighted-resistor digital-to-analog converter can be simplified by using the gate that supplies the digital input data as a switch. This approach permits a high-resolution converter to be built with standard open-collector logic. With 1% resistors, five-bit resolution is possible; tightening the tolerance to 0.1% can provide seven-bit resolution on selected units.

A d-a converter (a) usually contains input switches, a resistor network, and an operational amplifier that provides gain and a low-impedance analog voltage output. The digital input data is generally supplied at standard logic levels—for example, at transistor-transistor-logic levels or diode-transistor-logic levels. Logic gates driving the converter can therefore be used as its input switches (b).

Individually packaged gates, however, limit output word length to about two to three bits because of the marked gate-to-gate variation in logic low and logic high output levels. A TTL high, for instance, is guaranteed to be between 2.4 and 5 volts, while a low lies between 0 and 0.4 V. Output resistance also varies considerably from unit to unit. Excellent voltage-level tracking can, however, be obtained by using gates that share a common substrate if they are operated under the same load conditions. A five-bit converter (c) can be built with an open collector hex inverter performing the input switching function.

When the outputs of the open-collector gates are low, each gate has a load impedance of 500 ohms, and the collector-emitter saturation voltages of the gate output transistors are within millivolts of each other. When the outputs are high, each output transistor is off and the resistor network is referenced to supply voltage V_{CC}.

Longer output word lengths can be realized in the same way by utilizing two hex inverter packages. There may be some variation between packages in the low gate output voltage level, but this can be minimized by selecting the two packages from the same lot (by using the date code on the package). □



Let gates do the switching. Basic digital-to-analog converter (a) requires input switching network to interface digital input data. Using individual logic gates (b) to drive and switch converter limits resolution. However, up to five-bit word lengths can be obtained with open-collector hex inverter (c) as driving and switching network. Because inverters have common substrate, voltage-level tracking is good.

No-ladder d-a converter works from one 5-V supply

by E. Insam
Chelsea College, University of London, London, England

An 8-bit digital-to-analog converter that operates from a single positive 5-volt supply can be built without the usual front-end ladder network. This is done by creating a pseudo-random binary generator that is driven by a free-running multivibrator at a nominal clock frequency of approximately 5 megahertz. The multivibrator also provides the –5-V supply line for the converter's operational amplifier.

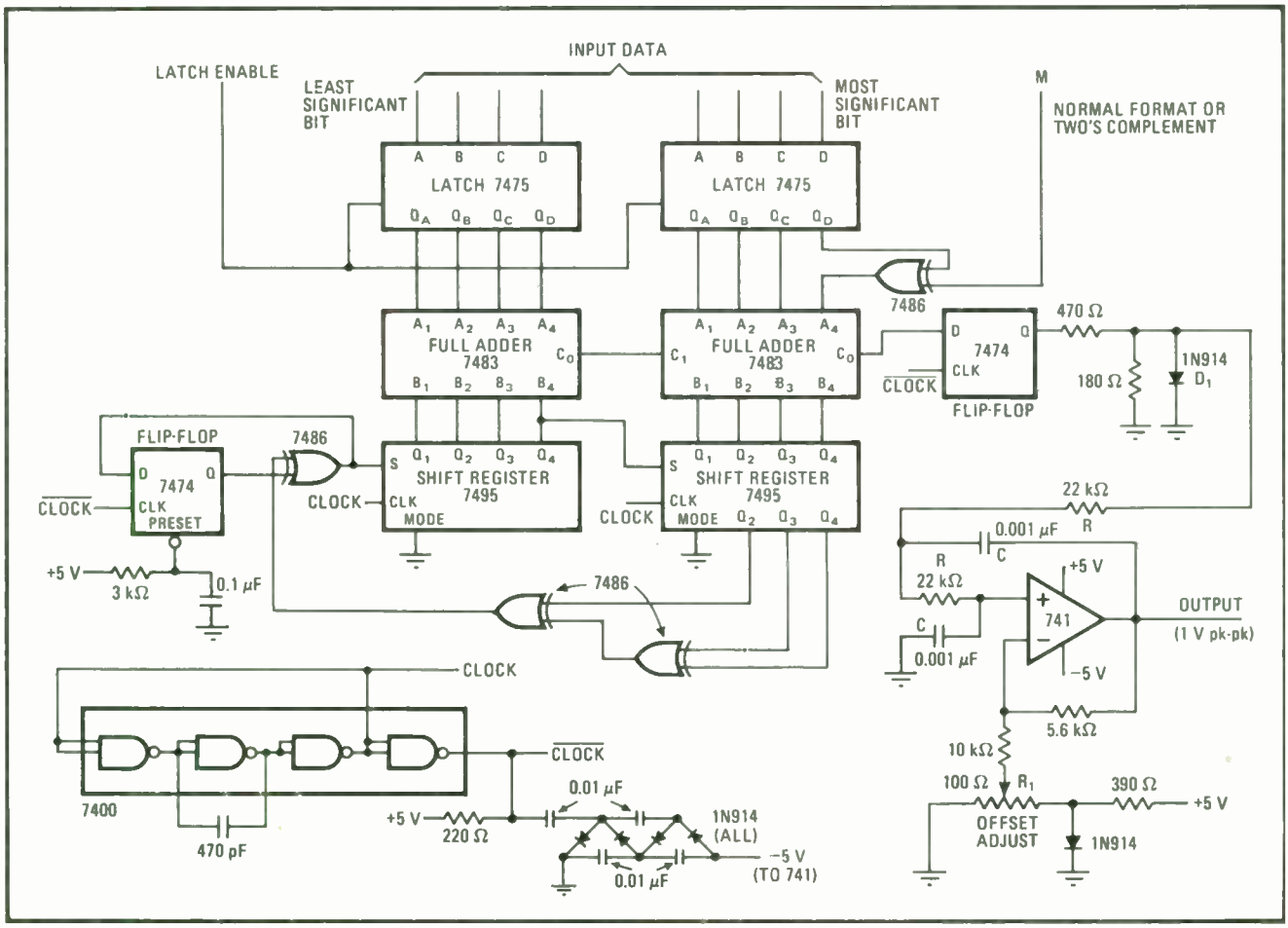
The output from the binary generator is compared (by subtraction) with the 8 input data bits. These can be in either a normal format or a two's-complement format, depending on the control input M. The carry output from the full adders is a pulse train whose mean value is proportional to the input data and is clamped to about 0.6 V by diode D_1.

This pulse train is then fed to an active Butterworth low-pass filter formed by the op amp and its associated components. In the circuit given here, the gain of this stage is set at 1.59 to give the necessary filter-pole positions and to bring the peak-to-peak output amplitude of the converter to 1 V. Potentiometer R_1 controls the dc shift of the analog output.

The quantizing noise consists of harmonic multiples of the clock frequency divided by 255. In this case, the lowest harmonic occurs at around 20 kilohertz, which is beyond audibility. The cutoff frequency ($\omega = 1/RC$) of the Butterworth filter is around 7 kHz. The circuit's gain accuracy, which is not a major concern for audio work, depends only on diode D_1 and the closed-loop gain of the op amp.

The transistor-transistor-logic version of this d-a converter consumes around 300 milliamperes. If low power drain is an important design factor, complementary MOS devices can readily be substituted, reducing the current consumption to around 40 mA. □

From digital to analog. Instead of the conventional ladder network followed by an op amp, this d-a converter employs a pseudo-random binary generator and an active low-pass filter. The generator's outputs and the 8 input data bits are subtracted in the full adders, resulting in a "carry" pulse train that drives the filter. Only one positive 5-volt supply is needed to power the entire circuit.



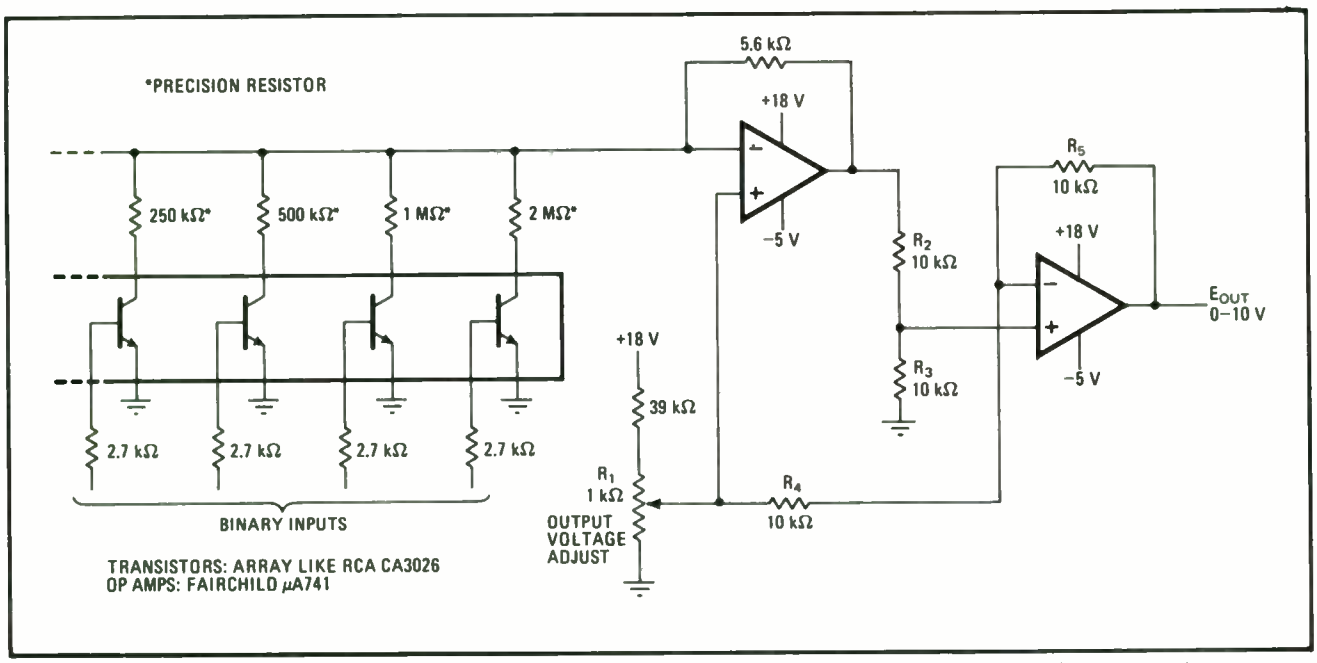
Digital-to-analog converter is built from low-cost parts

by Phillip J. Storey
Jands Pty. Ltd., Marrickville, N.S.W., Australia

An economical but reliable digital-to-analog converter can be made from readily available IC transistor arrays and general-purpose op amps. The converter is intended to interface with decimal or hexadecimal up/down counters, as well as directly addressed memories. It provides a positive-going output voltage that ranges from 0 to 10 volts and that can be used to control audio attenuators or light-dimmer units.

Each input transistor clamps its precision resistor to ground when a binary bit is applied to that input line. Input words can be up to 8 or 12 bits in length. Potentiometer R_1 allows the maximum output voltage to be varied about the nominal 10-V level. Additionally, as long as resistors R_2 through R_5 have at least a 1% tolerance, the output dc offset voltage will be only on the order of millivolts.

The converter works best within the frequency range of 3 hertz to 1 kilohertz, but can operate at clock rates as high as 100 kHz. However, output glitches become evident at the faster clock rate. □



Ready-made DAC. This digital-to-analog converter can almost be put together from a spare-parts box, since it is made up of components that are usually right on hand. Input words can be 8 or 12 bits long, and the positive-going analog output varies from 0 to 10 volts. If 1% resistors are used in the output stage, the output offset voltage is within millivolts of zero without any prior adjustment.

Amplifier adds sign bit to d-a converter output

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz.

In feedback systems, digital-to-analog converters frequently require bipolar outputs to supply both polarities of feedback-correction signals. One means of developing both polarities is to offset the output, but this method sacrifices the convenience of BCD bit-coding.

A better way to control output polarity is to provide sign-bit control to the digital-to-analog converter by connecting the output operational amplifier of the d-a

converter as a gated amplifier. This connection is possible when the op amp has uncommitted feedback to permit coding options. However, the technique can be applied to any current-output d-a converter by using an external op amp.

Shown in the figure is the gated-amplifier connection that provides the sign-bit control. The op-amp output is switched at the circuit output by transistor Q_2 in response to the sign-bit signal. When the sign bit is high, Q_2 is off, so the amplifier does not control output voltage e_o, and operation is that of a current-output d-a converter driving resistive load R_2. The output current from the converter, i_o, divides between the internal resistor R_0 and the path through R_1 and R_2 to ground. The output signal, which is negative, is determined by:

$$e_o = -i_o R_0 R_2/(R_1+R_2+R_0)$$

If the sign bit is low, switch Q_2 is turned on so that the op amp can control e_o. Then the amplifier performs as a current-to-voltage converter, giving an output signal of

$$e_o = i_o R_1$$

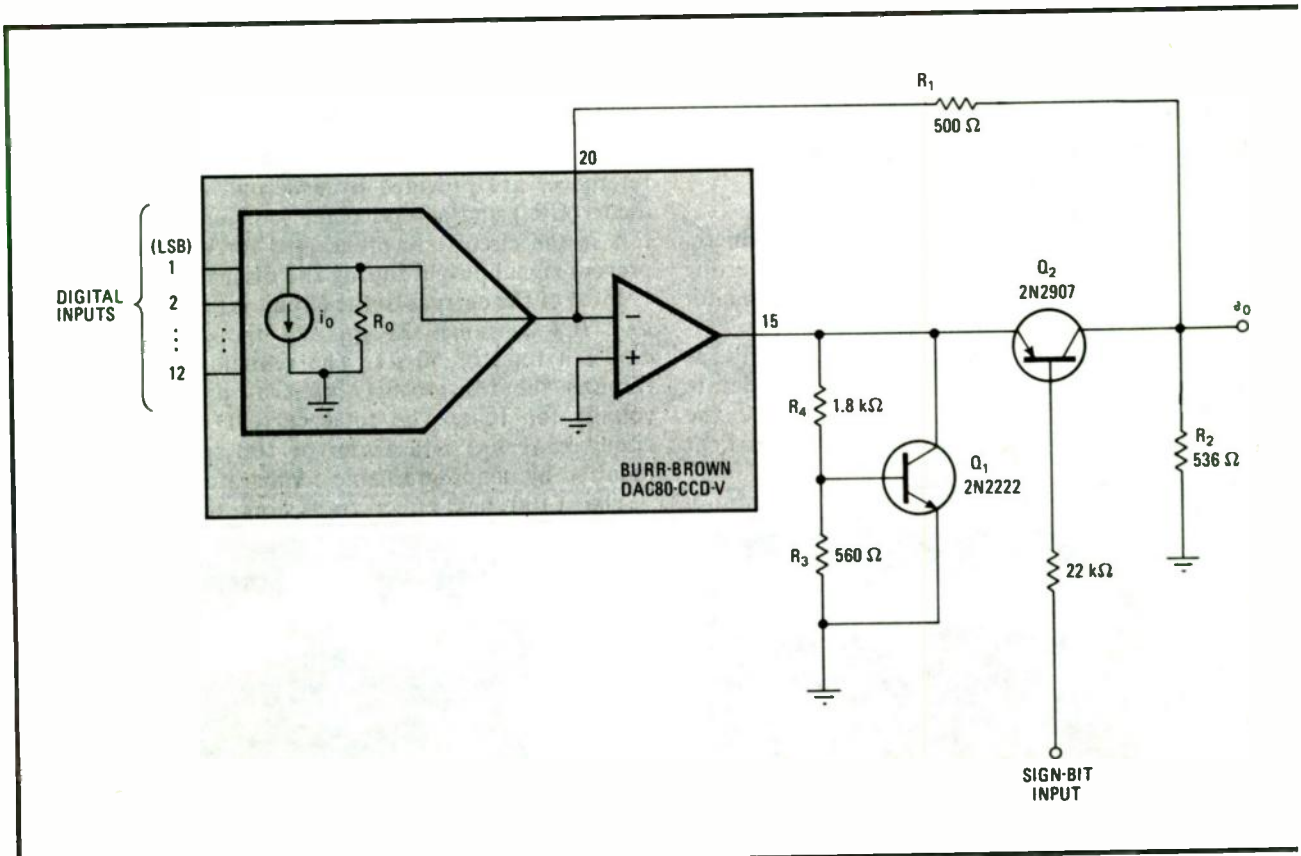
For a symmetrical response, the above opposite-polarity signals are made to have the same magnitude for a given i_o. This requires that

$$R_2 = R_1(R_0+R_1)/(R_0-R_1)$$

The value of R_0 is given on the data sheet for the d-a converter; for the DAC-80, it is 15 kilohms. The values of R_1 and R_2 are chosen so that the full-scale output current from the converter develops about 2 volts across them. The full scale i_o is 2 milliamperes, so $(R_1 + R_2)$ is approximately 2/0.002, or 1 kilohm.

Also connected to the gated amplifier is a clamp formed by transistor Q_1 and resistors R_3 and R_4. This clamp ensures logic-level compatibility for the sign bit. By clamping the positive swing of the op amp, it is possible to turn Q_2 off with the high-state voltage available from command logic. With the values of R_3 and R_4 illustrated, TTL-compatibility is achieved. To clamp the amplifier output, Q_1 performs as a simple shunt regulator by limiting its collector-emitter voltage to a maximum of $(1+R_4/R_3)V_{BE1}$. At that voltage, Q_1 turns on to clamp the amplifier output by forcing it into current limit.

Preservation of conversion accuracy requires three trimming adjustments to the circuit. First, an offset correction signal should be added to the op amp with Q_2 turned on and only the least significant bit on. Then, the positive output gain is adjusted by trimming R_1 with full-scale output—all bits turned on—and Q_2 on. Finally, Q_2 is turned off, and the negative-output gain is set by adjusting R_2. In this circuit mode, the op amp's input is overloaded, so it must maintain high input resistance under overload to avoid shunting the signal current. □



Sign bit sets analog-output polarity. In this circuit, the sign of the output voltage of the digital-to-analog converter is determined by a sig bit applied to Q_2. If the sign bit is low, the output voltage e_o is positive, and if the sign bit is high, e_o is negative. Here the sign bit is added to th d-a conversion by gating the internal output op amp, but an external op amp can be used on any current-output d-a converter.

15. Discriminators

Adjustable discriminator cleans up signal noise

by Dennis D. Barber
University of Houston, Houston, Texas

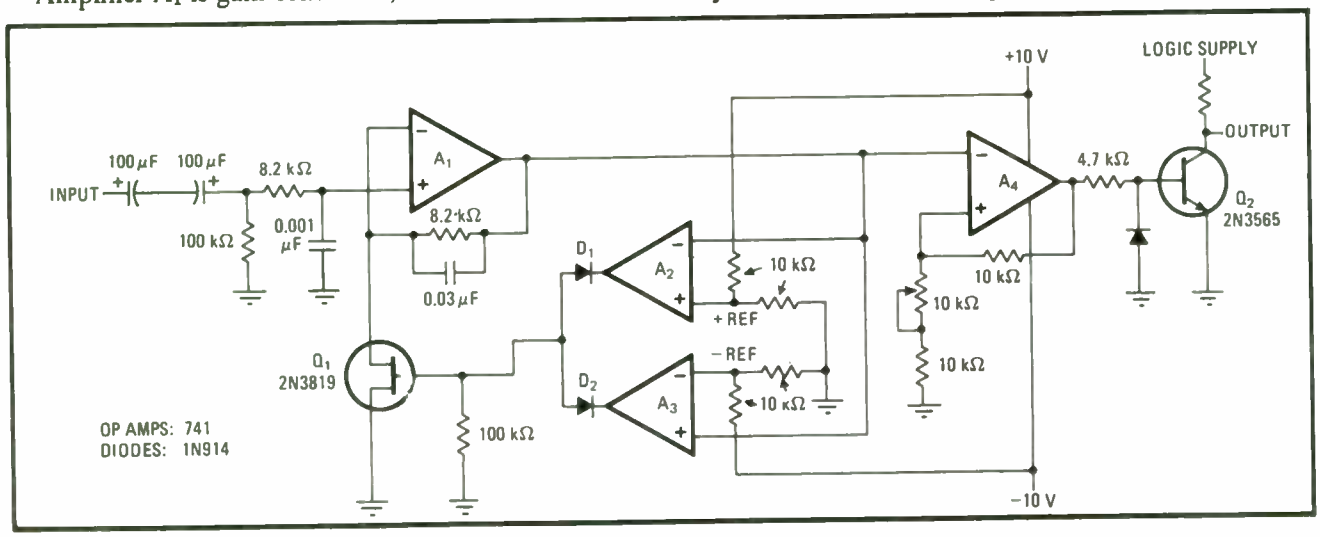
Telemetry signals or other logic signals often pick up a lot of extra noise during transmission. But they can easily be cleaned up at the receiving end by a discriminator circuit having adjustable hysteresis.

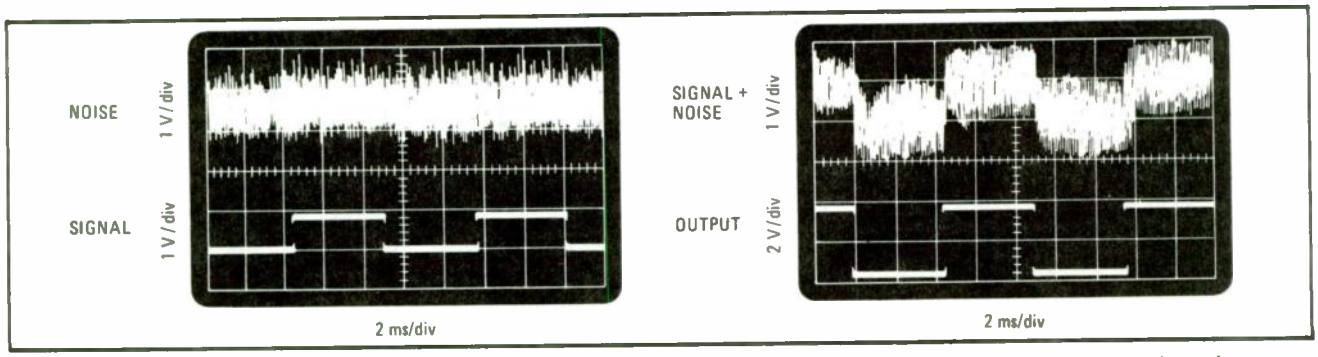
The voltage discriminator shown in the figure can clean up signals containing as much as 70% noise without the need to alter the signal amplitude or dc level. The input to the amplifier that serves as the voltage-discriminator (amplifier A_4) is kept constant at 5 volts peak-to-peak. But the signal to be conditioned, the one at the input to the circuit, does not have to be critically maintained or its level known precisely.

Amplifier A_1 is gain-controlled, with field-effect transistor Q_1 acting as the gain-control element. This FET, which functions as a voltage-variable resistor, is controlled by amplifiers A_2 and A_3. Amplifier A_4 is the voltage-discriminator stage that provides the adjustable hysteresis through its variable regenerative feedback.

Before the capacitively coupled input signal goes positive or negative, the output of amplifier A_1 may be treated as if it were at ground. The gain of amplifier A_1 is then at its maximum since the inputs to amplifiers A_2 and A_3 are below (in absolute magnitude) their respective reference voltages. The output of each amplifier is now positive, and diodes D_1 and D_2 are back-biased, which allows transistor Q_1 to turn fully on.

If the input signal goes positive, the output of A_1 will move towards the positive power-supply level. When it reaches the reference voltage of A_2, the output of A_2 quickly swings negative, turning transistor Q_1 partially off and thus lowering the gain of A_1. The output of A_1 is held at the positive reference voltage until this reference level is greater than the input voltage multiplied by the maximum gain of A_1. At this point, the input voltage is only a few millivolts above ground.





Pulling the data out of the noise. Adjustable-hysteresis voltage discriminator makes significant improvement in signal-to-noise ratios, as can be seen from the scope traces. The level of regenerative feedback of amplifier A_4, the voltage-discriminator stage, is adjusted to provide optimum noise immunity. The gain of amplifier A_1 is controlled by transistor Q_1, which is operated as a voltage-variable resistor.

As the input signal swings from positive to negative, the output of amplifier A_2 goes positive, but the output of amplifier A_3 becomes negative. The gain of amplifier A_1, therefore, is limited until the input signal again returns to very near ground.

In this way, the input voltage to amplifier A_4, the voltage discriminator, is maintained at a constant level. The threshold voltages for A_4 can be set slightly less than the reference voltages of A_2 and A_3, enabling the circuit to provide excellent noise immunity.

The capacitors at the input of the circuit are used to limit the amplitude of high-frequency spikes. The 100-microfarad capacitor values indicated in the diagram function well over a frequency range of 1 cycle per minute to 1,000 cycles per second and over an input amplitude range of 1 to 10 v pk-pk.

Transistor Q_1 can be almost any junction FET. Transistor Q_2 is included to make the output of the circuit compatible with the type of logic being used. Many types of general-purpose op amps should work in the circuit, and even Norton amplifiers like the type-3900 units can probably be used if the appropriate circuit modifications are made.

The oscilloscope photographs show how dramatically this discriminator can clean up signals. One photo shows separate signal and noise voltages, while the other photo shows the total input signal and the resulting output. □

Two-IC pulse discriminator handles wide range of inputs

by Steven E. Holzman
ESL Inc., Sunnyvale, Calif.

Just two IC packages will build a pulse-width discriminator having a pulse window that may be as narrow as tens of nanoseconds or as wide as several seconds. Applications for the circuit include radar, communications, and signal-processing systems.

The lower pulse limit (T_L) is determined by the timing period (T_A) of one-shot OS^A, while the upper pulse limit (T_U) is established by the sum of this timing period and the timing period (T_B) of one-shot OS_B:

$$T_L = T_A$$
$$T_U = T_A + T_B$$

Of course, period T_A for one-shot OS_A and period T_B for one-shot OS_B are set by selecting the proper values (from a data sheet) for resistor R_A and capacitor C_A, and resistor R_B and capacitor C_B, respectively.

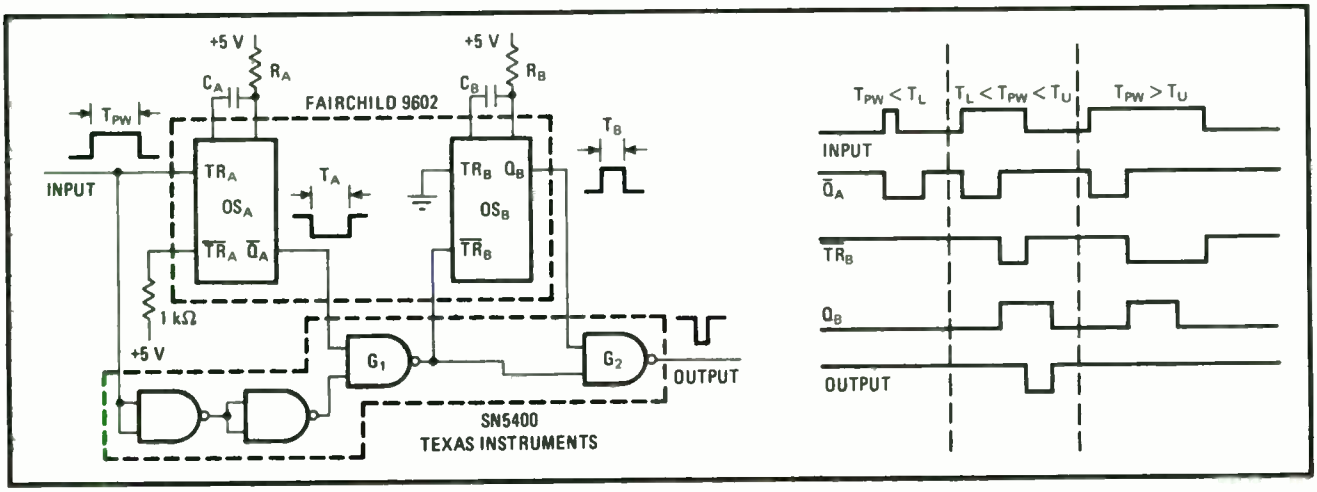
When the input pulse width, T_{PW}, is less than T_A, one-shot OS_A is triggered, but one-shot OS_B is not. The input pulse's leading edge causes the $\overline{Q}_A$ output of OS_A to go low for T_A seconds. However, NAND gate G_1 remains inhibited because the delayed (by two gates) version of the input pulse returns to its low state before the $\overline{Q}_A$ output becomes high again.

If the input pulse is within the circuit's time window, gate G_1 is enabled when $\overline{Q}_A$ returns to its high state, triggering one-shot OS_B so that its Q_B output goes high for T_B seconds. NAND gate G_2 is also enabled, producing an output pulse and indicating that the input pulse width "qualifies."

When the input pulse lasts longer than upper time limit T_U, the Q_B output of one-shot OS_B goes high while gate G_1 is still enabled. This inhibits gate G_2 and prevents an output pulse from being generated.

The two NAND gates between the input and gate G_1 slow up the input pulse so that narrow pulses do not occur at G_1's output before one-shot OS_A can trigger. □

Pulse-width window. This circuit produces an output only when the input pulse width falls within preset time limits. Timing period (T_A) of one-shot OS_A sets the lower limit (T_L), while the timing periods ($T_A + T_B$) of both one-shots set the upper limit (T_U). Qualified pulses trigger both one-shots and enable all the gates. Short pulses do not trigger one-shot OS_B, and long pulses do not enable gate G_2.



Voltage discriminator has 0.1-mV resolution

by Ryszard Bayer
Institute of Nuclear Research, Swierk, Poland

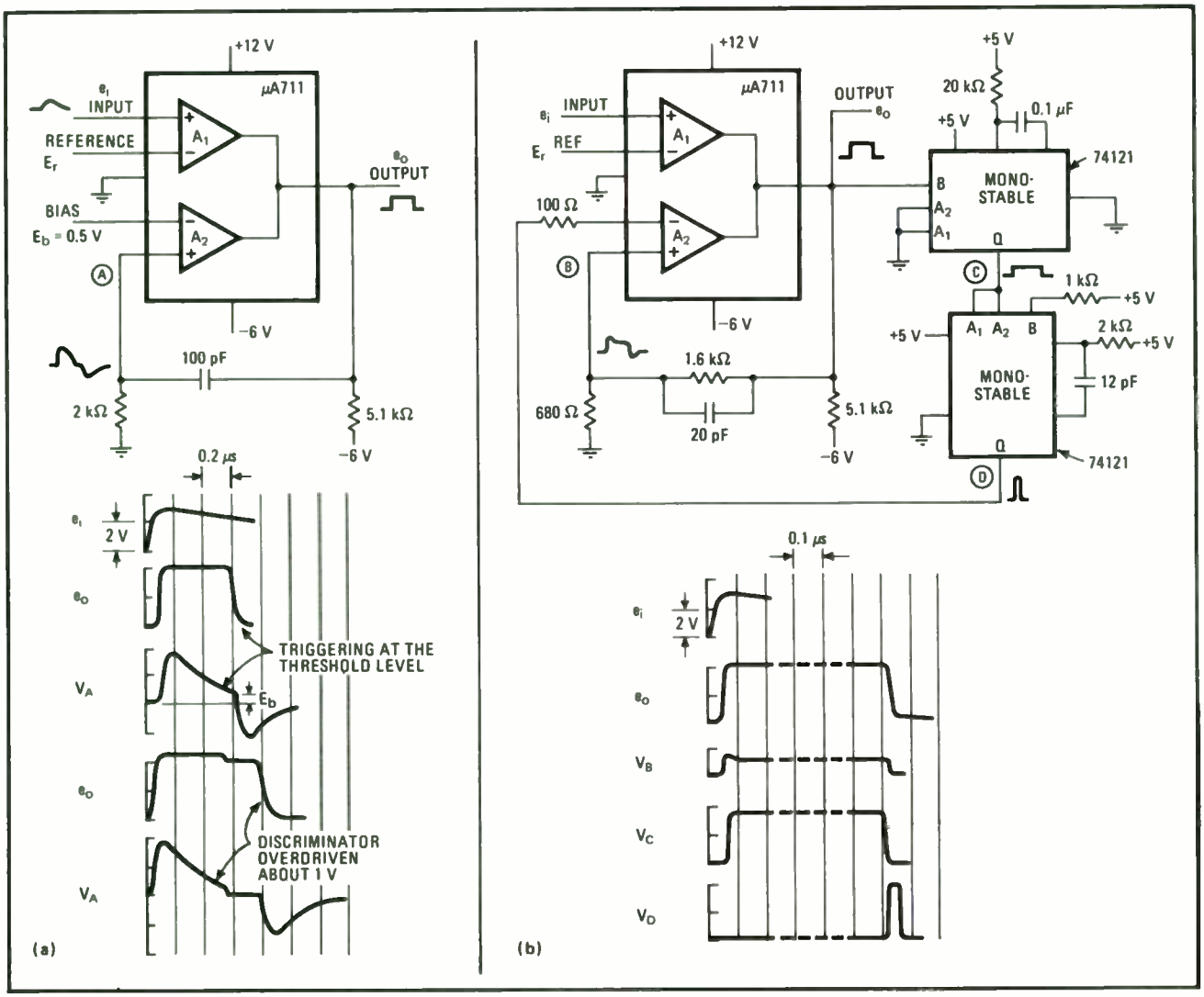
Positive feedback permits a dual IC comparator to perform as a high-resolution voltage discriminator that can detect either positive or negative pulses having amplitudes ranging from a few millivolts to 5 volts. When driven from such low-impedance sources as operational amplifiers, this discriminator has a linearity of better than 0.03% and a voltage resolution of about 0.1 millivolt.

The input signal is compared with the reference voltage by comparator A_1. The signal appearing at the moment of comparison of these two voltages is taken from the common output of both comparators and fed back to the noninverting input of comparator A.

Because of this positive-feedback path, the discriminated signal is amplified considerably, reducing the amplifier's offset voltage and improving voltage resolution. Since the feedback signal is introduced to the noninverting input of comparator A^{ϵ}, both inputs of comparator A_1 can be driven from low-impedance sources for better discriminator accuracy.

With capacitive feedback, as in circuit (a), the discriminator has only one stable state. With dc feedback, as in circuit (b), the discriminator becomes bistable. At the moment the input and reference signals are compared, the bistable discriminator is set to its high level. It can be reset by applying a second pulse to the inverting input of comparator A_2. This second pulse can be applied after the first pulse has been terminated for a time that exceeds the duration of the first pulse minus the discrimination-level threshold. □

Discriminating comparators. Integrated dual comparators can differentiate between input-signal height and the reference-voltage level to within 0.1 millivolt. This high resolution is due to the positive feedback from the output to the noninverting input of comparator A_2. Capacitive feedback (a) produces a unistable discriminator, while dc feedback (b) produces a bistable one that can be reset with a second input pulse.



Buffer keeps noise from triggering thyristor

by L. R. Rice
*Westinghouse Semiconductor Division, Youngwood, Pa.**

Certain shortcomings in passive noise-rejection networks have led to development of an active circuit designed to prevent false triggering of thyristors. Such undesired firing can occur when noise transients cross the thyristor gate conductors, and can produce fluctuations of load power, oscillations in control circuits, and equipment damage. The offending pulses usually arise from reactive-load energization or de-energization, such as the discharge of a capacitor or the switching of a relay.

In the field, passive networks that discriminate against both signal and noise, such as those shown in Fig. 1, are often used, but they are impractical at times and some application problems simply cannot be solved with these techniques. Therefore an active circuit, consisting of a buffer connected between the trigger source and the thyristor gate, is needed.

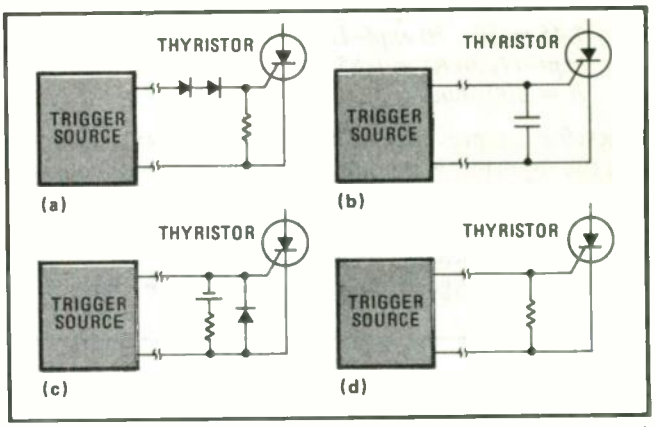
As shown in Fig. 2, this buffer consists of an RC integrating circuit, a comparator, and a pulse generator. An incoming voltage, either signal or noise, charges 0.02-microfarad capacitor C through resistor R. The 2N697 comparator amplifier turns on when the capacitor voltage reaches the threshold value equal to the sum of the voltage drops in diode D_2, the base-to-emitter junction, and zener diode D_3. This threshold voltage is given by

$$V_{TH} = V_{diode} + V_{BE} + V_{zener}$$
$$= (1.0 + 0.45 + 6.0)\ volts$$
$$= 7.45\ volts$$

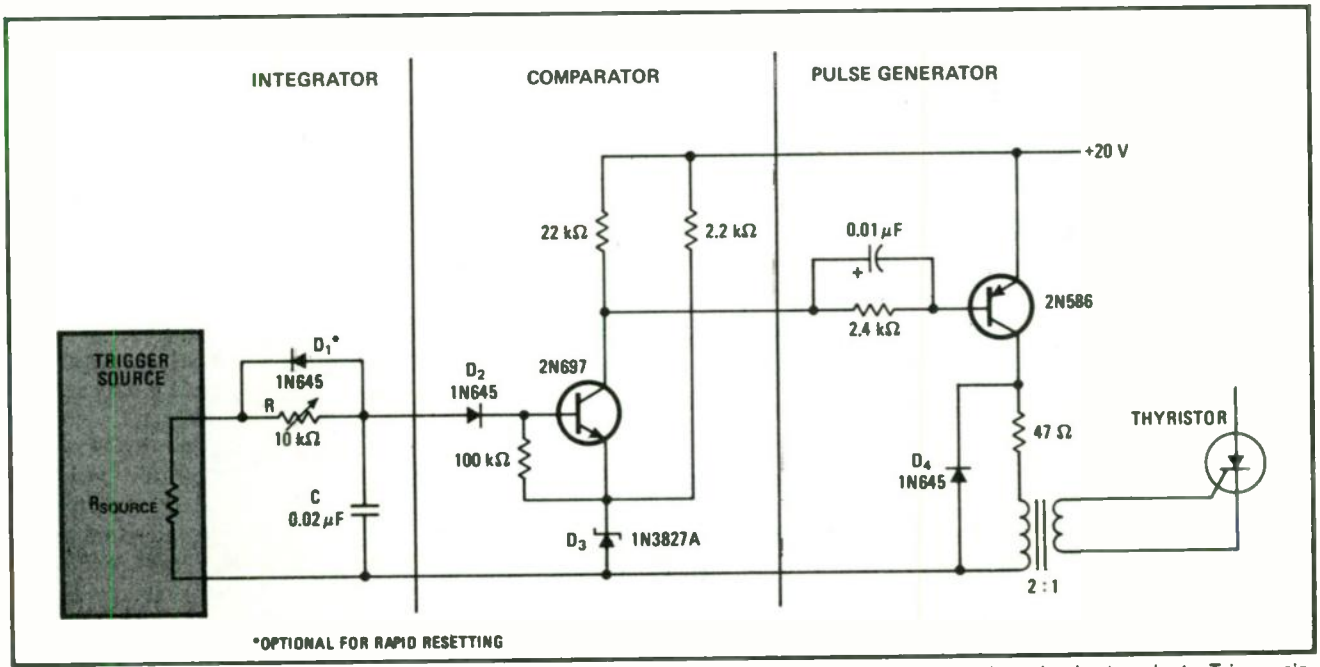
When the capacitor voltage reaches this value and turns on the comparator, the 2N586 pulse generator starts to conduct and fires the thyristor.

Variable resistor R is adjusted so that the time constant RC is large enough to prevent noise pulses from charging C to threshold. For example, if the noise ambience can be represented by a 50-volt pulse of 1-micro-

*Now with White-Westinghouse Corp., Mansfield, Ohio.



1. Quick fixes. Noise in thyristor gate lead is sometimes suppressed by one or another of these means: (a) diodes raise threshold voltage; (b) capacitor shunts high frequencies; (c) saturated diode reverse-biases gate; (d) resistor decreases gate sensitivity.



2. Buffer. Integrator prevents false triggering of thyristor by discriminating between genuine trigger signals and noise transients. Trigger signal must last long enough to charge capacitor C to the threshold voltage of the comparator, which then turns on the pulse generator. Variable resistor R permits adjustment of the charging-time constant so that noise pulses cannot charge C to the comparator's threshold.

second duration, the value of R that would allow C to just reach threshold in 1 μs is found from the charging equation

$$V_C = V_0 - V_0 exp(-t/RC)$$
$$7.45 = 50 - 50\, exp(-1/0.02R)$$
$$exp(-1/0.02R) = 0.85$$
$$R = 300 \text{ ohms}$$

Therefore, to prevent the 50-V/1-μs noise pulse from firing the thyristor, R is made a bit larger than 300 ohms.

After the noise pulse has ended, capacitor C discharges back through R, or through diode D_1 if quicker recovery is required.

A signal voltage from the trigger source charges up the capacitor just as a noise pulse does, but the signal duration is made long enough for the capacitor to reach threshold. If the trigger signal is 12 volts, for example, and R has been set for 300 ohms, then the signal must be applied for at least a time duration t (in microseconds) given by

$$7.45 = 12 - 12\, exp[-t/(300 \times 0.02)]$$

or t = 6 μs. Thus the 12-V trigger signal must last for 6 μs to fire the transistor.

Because this circuit delays the normal firing point to achieve noise rejection, timing in the trigger source may require adjustment if not controlled by feedback from the load. □

16. Display circuits

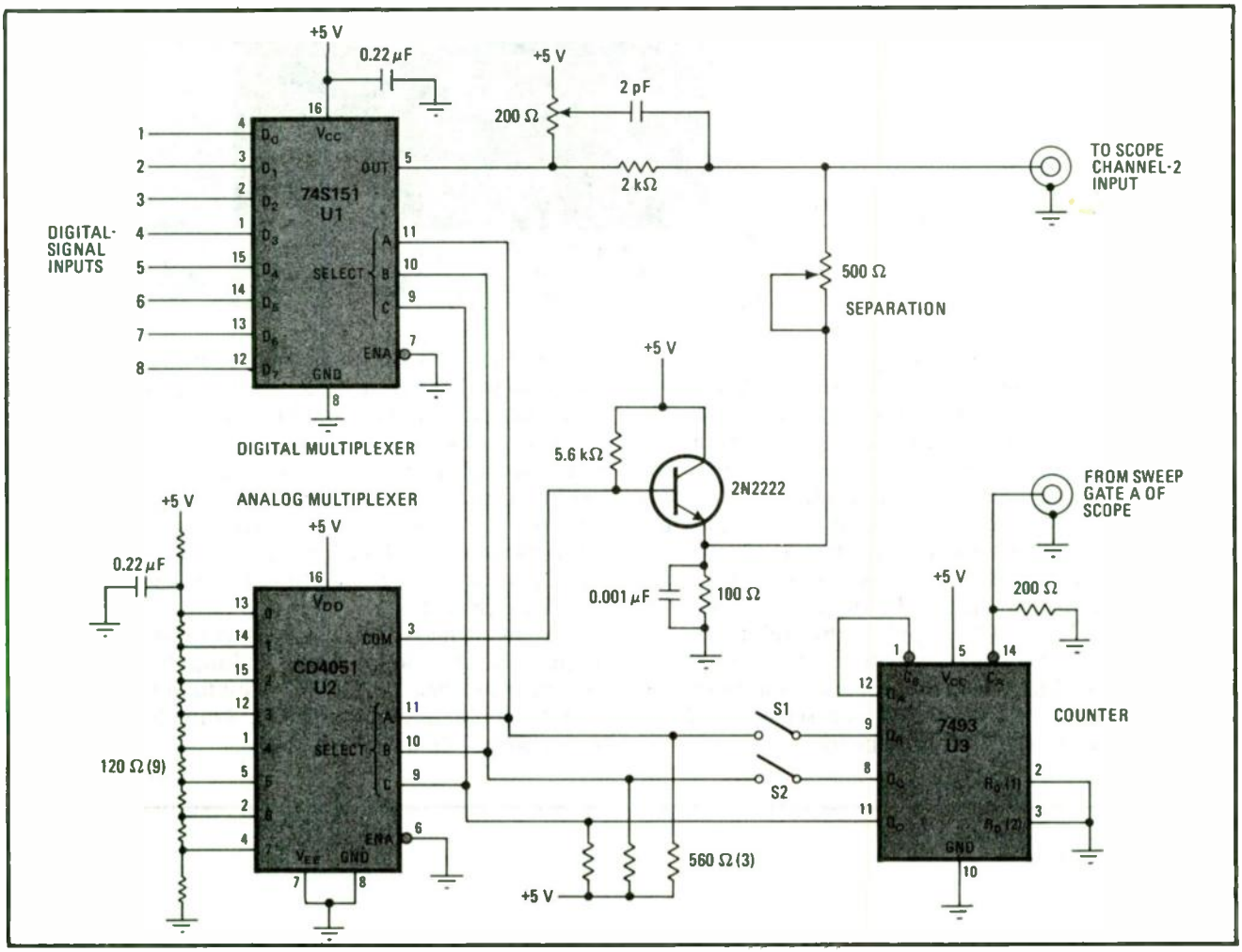
Scope display of eight signals helps debug sequential logic

by Matthew L. Fichtenbaum
General Radio Co., Concord, Mass.

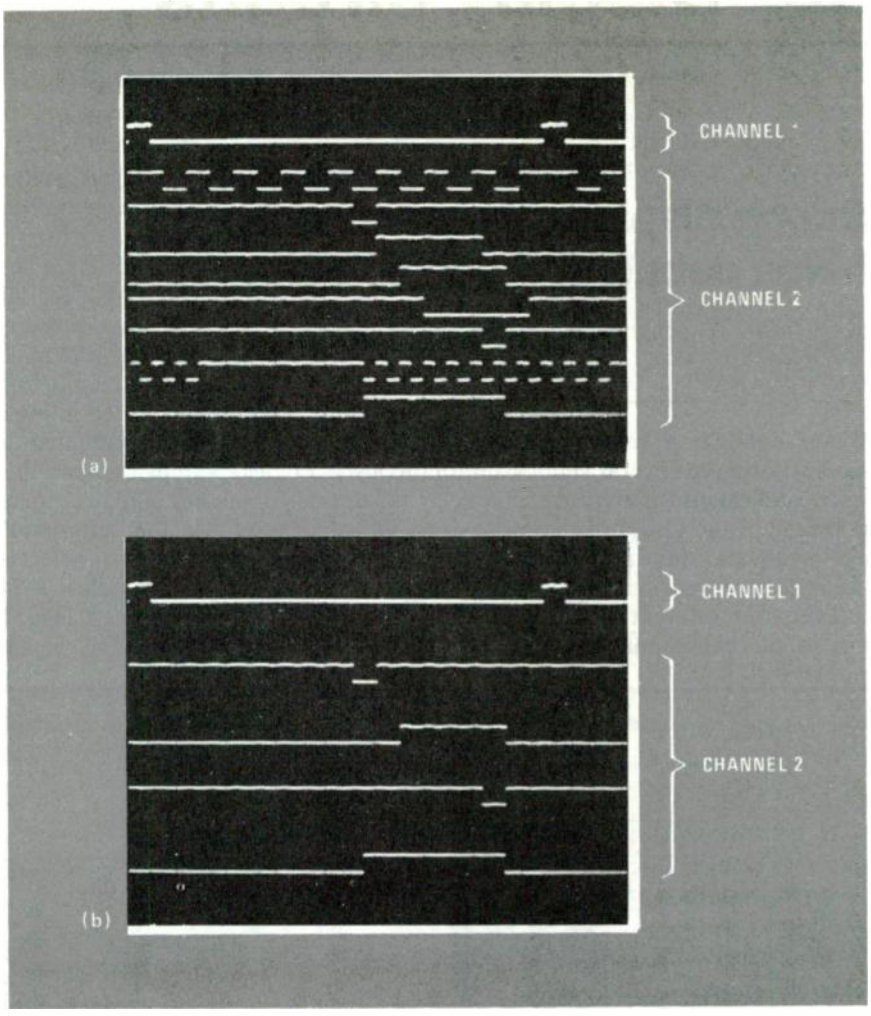
When debugging sequential logic, an engineer may have to observe several signals simultaneously. Logical states and the times that they change are of primary importance in the visual display; the exact values of voltage levels and the duration of rise times and fall times are of lesser importance.

Two, four, or eight digital signals can be displayed on one of the two channels of a Tektronix 454 or similar dual-trace oscilloscope, as demonstrated in the photographs on the next page. The other channel may then be used for triggering or for observation of a ninth signal. The eight signals are treated as logic levels and are gated by a digital multiplexer. Although this procedure does not preserve voltage levels and wave shapes, it does achieve maximum speed with simple circuitry.

The circuit for displaying the signals on the scope is illustrated in Fig. 1. The 7493 divide-by-16 counter (U3) is incremented after each scope sweep. The counter steps through the eight inputs sequentially, and the extra stage compensates for the use of every other sweep in the "alternate" display mode. The counter's highest three bits select an input signal via digital multiplexer U1, which is a 74S151 TTL Schottky type. At the same time, the CD4051 C-MOS analog multiplexer U2 picks a dc voltage off a resistor chain. This voltage is summed



1. Multi-trace adapter. Two, four, or eight digital input signals time-share the channel-2 trace of a dual-trace oscilloscope by means of this circuit. The digital multiplexer selects individual digital inputs in cyclic succession, and the analog multiplexer separates their wave forms vertically; sweep counter drives multiplexers. Switches S_1 and S_2 permit display of only two or four digital wave forms, instead of eight.



2. Signal tracing. Channel 2 of dual-trace scope is multiplexed to display eight different logic wave forms in (a) and four wave forms in (b). The channel-1 trace, used for triggering, appears at top in both photos; it is brighter than the channel-2 traces because of its higher duty ratio. This simultaneous display of several signals is convenient for logic-circuit debugging. High and low states, and the timing of their changes, are indicated accurately even though the multiplexing does not preserve voltage levels and wave shapes. The multi-trace adapter circuit is shown in Fig. 1 on the preceding page.

with the digital signal, providing a different reference level for each trace and thus separating the traces vertically from each other on the screen, as shown in Fig. 1.

The 500-ohm variable resistor adjusts the magnitude of the dc offset, varying the trace separation. The scope's variable vertical-sensitivity control may be used to adjust the over-all display amplitude. The 200-ohm potentiometer is adjusted for best transient response. Both the 500-ohm and 200-ohm pots should be cermet or other noninductive types. The three 560-ohm resistors pull up the levels of the inputs to the multiplexers.

The resistor chain could be replaced by eight potentiometers in parallel, with their wipers connected to the input terminals of the CD4051, for separate adjustments of the vertical positions of the individual traces.

If switch S_1 is open, the scope displays only four traces (digital inputs 1, 3, 5, 7). If both S_1 and S_2 are open, only two inputs (3 and 7) are displayed.

This time-division-multiplexing of channel 2 on the dual-trace scope of course makes the signal wave forms less bright than the channel-1 trace. In Fig. 2(a), the top trace is scanned eight times as often as each of the lower eight traces, and in Fig. 2(b), channel 1 is scanned four times as often as any one of the four offset wave forms that share channel 2.

The circuit may be built in a small box, with appropriate connectors to the scope and inputs. It should be used near the logic circuit under test to minimize signal-lead length and circuit-loading. Only 5 volts of dc power are required. □

Chopping mode improves multiple-trace display

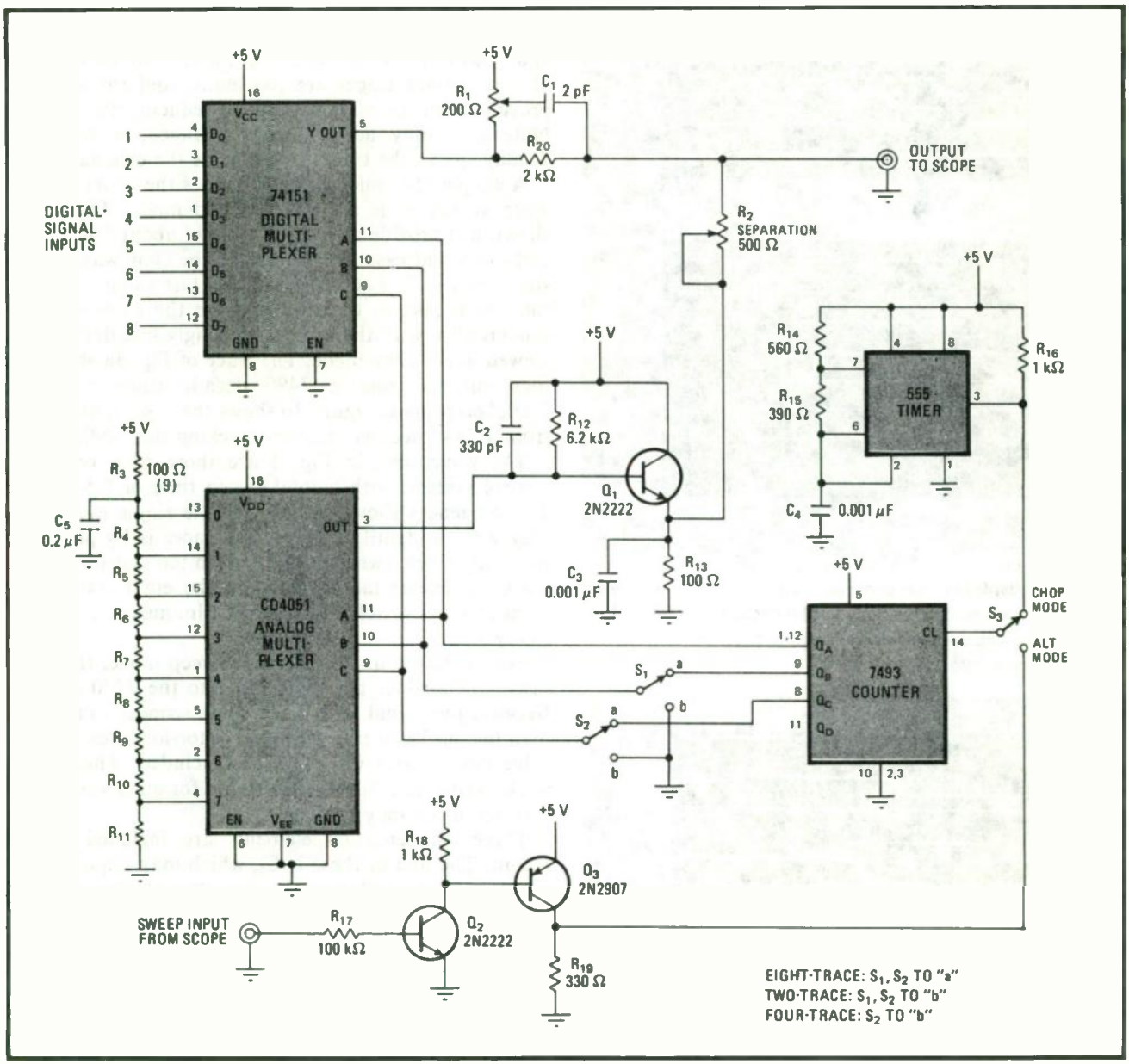
by C. S. Pepper
IRT Corp., San Diego, Calif.

A chopped mode of signal sampling extends the usefulness and versatility of an oscilloscope display that shows several signals simultaneously. The eight-trace oscilloscope switch described in the preceding article, operates in an alternating mode that uses both beams of a dual-beam scope. One beam repeats as usual, and the second steps through a repeating pattern of eight vertical levels. Each level displays one line of digital data; the result is a nine-channel trace-sequential display.

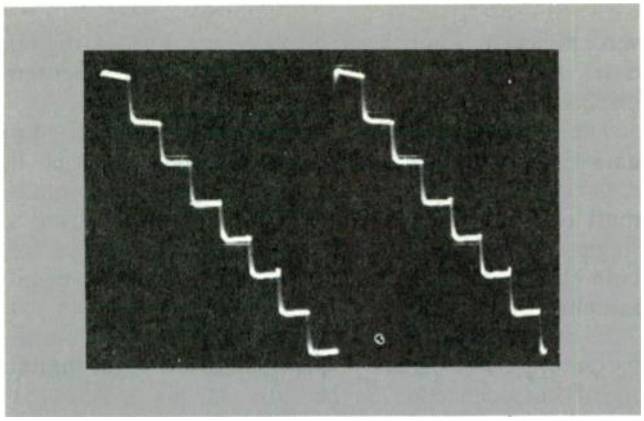
The sequential mode of sampling is satisfactory for data that is repeated at a sufficiently high rate. But, if data repeats slowly or occurs only once, all of the signals must be sampled at high speed and displayed during a single sweep. The circuit shown in Fig. 1 provides for both the chopped and alternate-sweep modes of signal sampling and display.

In this circuit, the 74S151 is an 8-line digital multiplexer. Inputs A, B, and C pick one of the eight digital signals for connection to the output at pin 5. A 74151 may be used if the faster Schottky device is not required.

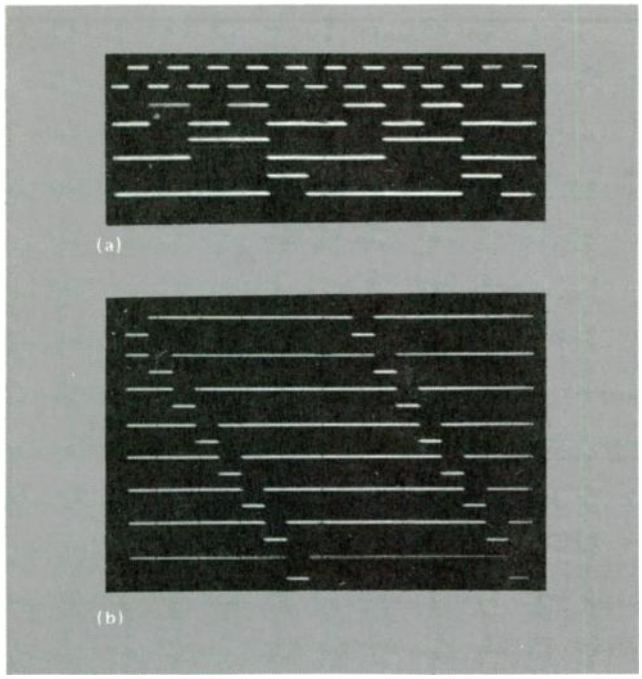
The CD4051 analog multiplexer takes its inputs from



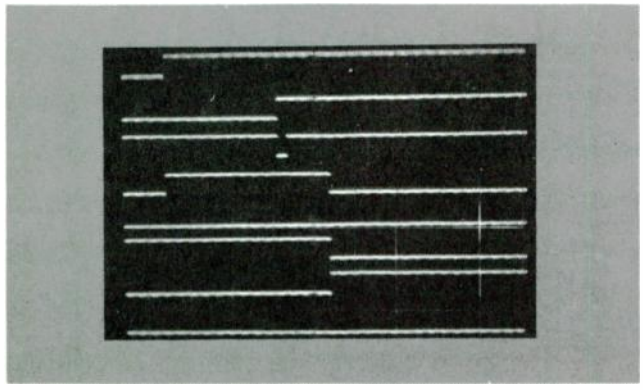
1. Signal traces. Scope displays two, four, or eight digital input signals, timeshared on either a chopped or sequential basis. The digital multiplexer selects individual inputs in cyclic succession, and the analog multiplexer separates their traces vertically. Both multiplexers are driven by a counter that counts pulses from a 555 timer for the chopped mode or sweeps from the scope for the alternate-sweep mode.



2. Fast steps. Staircase waveform positions scope trace in the chopped mode. Each step is 5 microseconds wide.



3. Outputs displayed. the chopped mode produced these waveforms of (a) the four outputs from a 7490 decade counter, and (b) the first eight outputs from a 7442 decimal decoder driven by the 7490. Input pulse rate was 1 kHz.



4. Slow process. Timing diagram of a slow speed controller with total trace length of 0.5 second was photographed by use of chopped mode. Display was triggered from the negative transition of the upper trace.

a resistance-chain divider that establishes a set of eight equally divided voltage levels. These levels appear at the output in the same sequence as the digital signals from the 74S151 because the two multiplexers have common addressing. A 2N2222 transistor, Q_1, provides drive power for the analog output, and the digital and analog signals are summed at the output to the oscilloscope.

Addressing is obtained from the 7493 counter. The circuit utilizes a single channel of the oscilloscope, with external triggering from one of the signals or a related source. The Q_A, Q_B, and Q_C outputs provide fast chopping of the data. If a slower chop signal can be used, dropping back to Q_B, Q_C and Q_D will double the ON time for the same chop frequency.

Switches S_1 and S_2 provide options of eight, four, or two traces. For eight traces, both switches are in position (a), and for a two-trace display, both switches must be in the grounded (b) position. If only switch S_1 is in the (b) position a four-trace pattern, composed of traces 1, 2, 5, and 6, will appear. This can be a useful option because, at times, eight traces are too many, and the switches provide a means of momentarily reducing the clutter. Note that only addressing is changed; a two-trace display spaces the traces the same as the original eight.

A simple 555 timer circuit provides the counter input when switch S_3 is set for the chop mode. The values shown will provide a trace-bit time of about 5 microseconds, or a staircase time of 40 μs. The chop waveform is shown in Fig. 2. Each step is 5 μs—fast enough to cover the line breaks in the traces. Since the chop is not in synchronism with the data, surprisingly fast data can be viewed in the chop mode. The trace of Fig. 3a shows the four outputs from a 7490 decade counter with a 1-kilohertz input. Figure 3b shows the first eight outputs from a 7442 decimal decoder tracking the 7490.

The waveforms in Fig. 4 are those of a very slow control system, with a total sweep time of 0.5 second. The sequences shown are all for one single event. The only way to identify these scope traces is by photography—the single sweep goes by much too fast to begin to track the events taking place on the eight traces. The eight-channel switch and Polaroid film make the photography simple.

For operation in the alternate-sweep mode, the scope sawtooth provides the clock input to the 7490 counter. Because the signal level from some scopes is much too high for the 5-volt transistor-transistor-logic counter, the drive circuit with Q_2 and Q_3 is included. This circuit works well with a 30-V sweep in, but for other voltages, a revision of R_{17} may be needed.

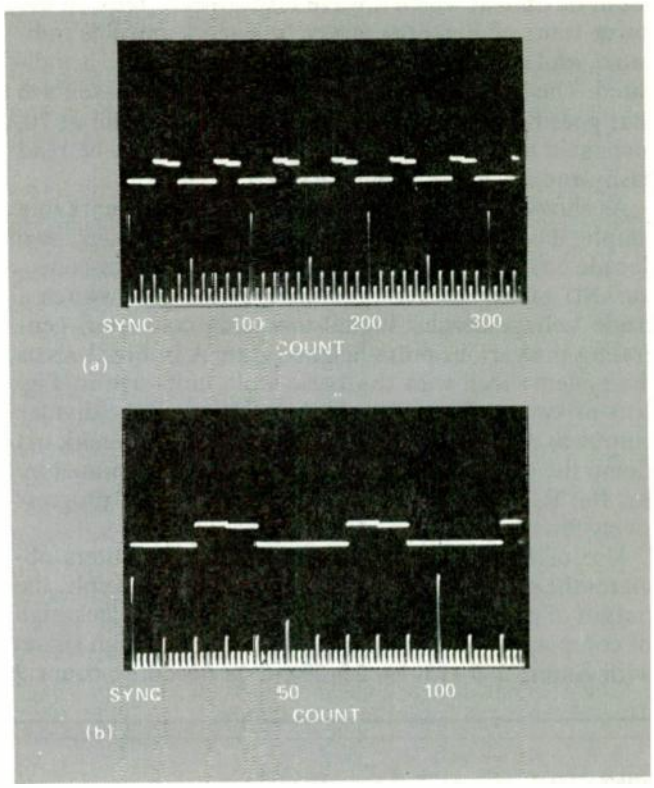
Three compensation elements are included in the circuit. The first of these is C_5, which may require some tweaking to best flatten the top step of the staircase shown in Fig. 2. The second is C_2, which eliminates overshoot at the end of each step. The effect of overshoot is to draw a thick trace; the 330-picofarad value shown may require trimming to produce the narrowest trace and to eliminate ringing. Finally, R_1 and C_1 should be trimmed to produce the narrowest trace. □

Graduated-scale generator calibrates data display

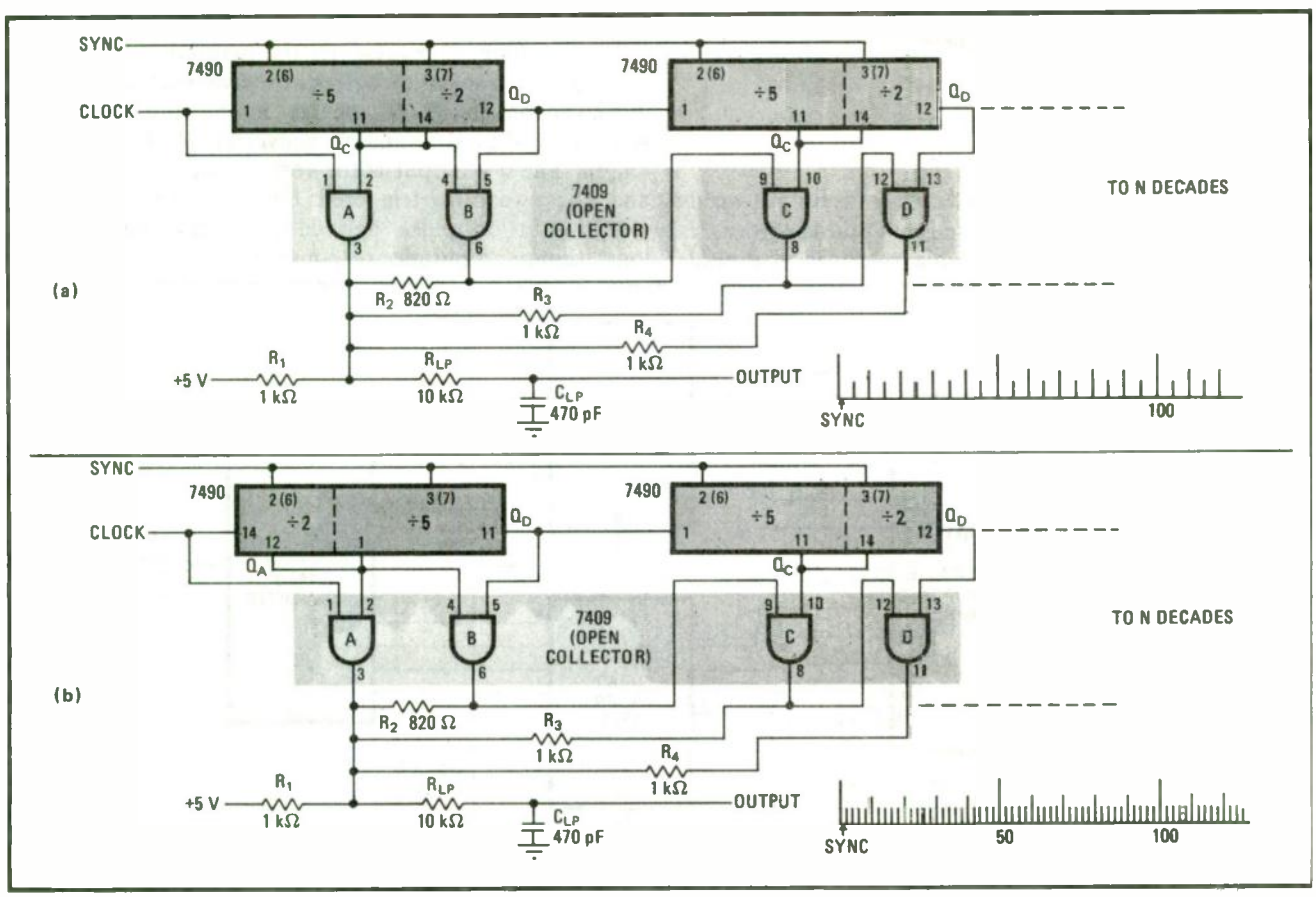
by Ken E. Anderson
IBME, University of Toronto, Canada

Scope and chart displays may require reference signals to indicate timing or counting scales. The circuit shown here is added to the display portion of a real-time digital data correlator at a cost of $3 or $4 to provide a graduated scale below the correlation display on a two-channel scope. Although it lacks the precision of a cursor, the continuous scale offers greater versatility and speed of operation. It also references the display data when stored on hard copy.

The photographs in Fig. 1 show two scales that can be generated to aid the observer in determining the pulse



1. Measurement aids. Graduated scales are generated on dual-trace scope or chart to facilitate probing of displayed data. In lower trace (a), every fifth clock pulse has a spike; in lower trace (b), every second clock has one. From these scales, observer sees that upper trace rises at count 20 and falls at count 40. Circuits for generating scales are shown in Fig. 2.



2. Here's how. Circuits for generating graduated scales of incoming clock pulses use decade counters. Two AND gates per decade switch voltage-divider d-a converter to produce various pulse heights; the AND gates have open collector outputs. Each counter in (a) divides by 5 and then by 2 to provide scale with a basic unit of 5 counts. In (b), first counter divides by 2 and then by 5 to provide a basic unit of 2. Second counter divides by 5 and then 2 to enhance pulses at 50 and 100. Values of R_{LP} and C_{LP} shown here are chosen for use with a 10-kHz clock

count or time at which a wave form rises or falls. In the lower trace of Fig. 1(a), every fifth clock pulse is indicated, and in Fig. 1(b), every second clock pulse is indicated. The upper trace in each photo shows a wave form that goes high at count 20, low at 40, high again at 70, low again at 90, and so forth. These counts can be read easily and accurately from the reference scales.

As shown in Fig. 2, the scale generator is remarkably simple. For two decades of unique graduations, two decade counters (7490) and one package of open-collector AND gates (7409) are required. These gates switch a crude voltage-divider digital-to-analog converter, generating the various pulse heights. Gate A in Fig. 2 ANDs the system clock with the basic scale unit—five in Fig. 2(a) or two in Fig. 2(b)—enabling the voltage-divider output to rise. Low gates B, C, or D (or combinations) clamp the output to appropriate levels as determined by R_1, R_2, R_3, and R_4. As higher-order counters progressively flip high, taller graduations are created.

Use of the 7490's quinary and binary counters obviates the need for extensive decoding. For example, the output of gate A in Fig. 2(a) goes high on the clock high of count 4, (9, 14, 19, etc); gate B ANDs this high signal with counts 5–9 (15–19, 25–29), thus decoding count 9 (19, 29). The cascaded decade circuit decodes counts 49 and 99. For display on a scope, a low-pass filter or integrator consisting of R_{LP} and C_{LP} is added to improve the appearance of the scale by increasing the rise and fall times of the pulses. Relative pulse heights may be altered via resistor ratios of R_1, R_2, R_3, and R_4. However, to ensure adequate noise margin at inputs of gates C and D, R_1 must not be greater than R_3 or R_4.

Synchronization of the scale generator to the scope and system output is accomplished by providing a pulse to reset the counters to zero (pins 2, 3) for graduations on counts 4, 9, 14, 19, etc. or to maximum (pins 6, 7) for graduations on counts 5, 10, 15, 20. . . .

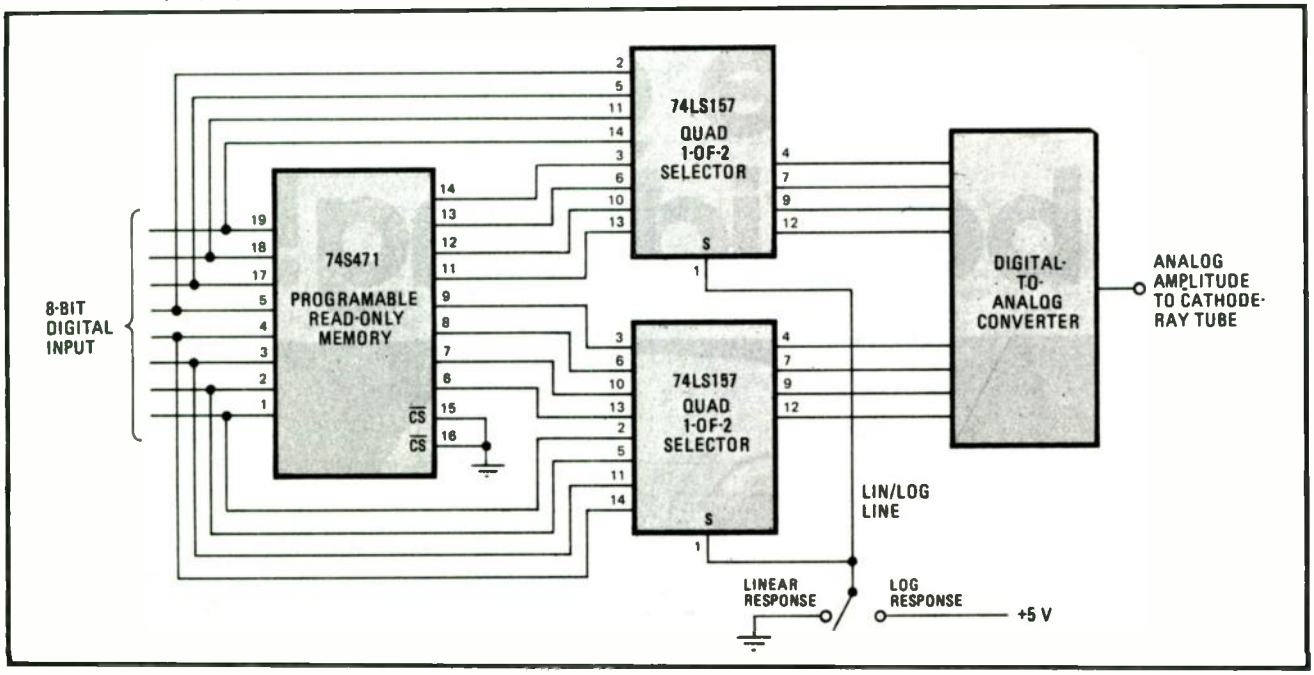
The use of this graduated-scale generator can ensure precise tagging of displayed data even when the scope is being operated in the magnify, delayed-sweep, and uncalibrated-sweep modes. Other applications include generation of a time scale for sweep calibration of scopes (when clocked by a high-precision source) and generation of a clock-pulse scale for troubleshooting cyclic sequences. The latter application is illustrated by the upper traces in the two photographs; this waveform is actually the output of the second bit of the second quinary counter (pin 8 of the second 7490). □

PROM provides linear or logarithmic display

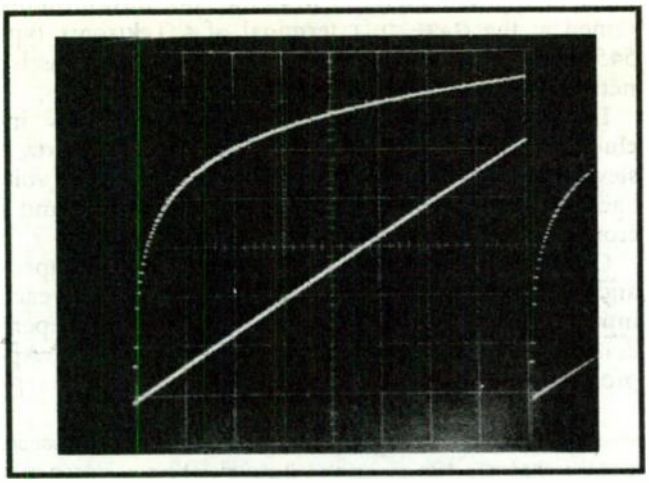
by John Brady
Applied Research Laboratories, University of Texas, Austin, Texas

A read-only memory, programed so that its output words are logarithmically related to the input address words, is useful for displaying a logarithmic response in digital-signal processing. The display has none of the drift and gain error with time that are associated with the use of an analog log amplifier, and, in many cases, is more economical.

In digital-signal processing, the magnitude of a time-varying function or of a frequency-varying function is displayed on an oscilloscope by connecting the digital word to a digital-to-analog converter of the same bit length. The d-a output is the vertical input to the scope, and the sweep is triggered by a suitably repetitive synchronization pulse derived from the signal. If a logarithmic amplitude response is needed, the usual



1. Three ICs select response. The 74LS157 quad two-line-to-one-line data selectors choose either the linear input code or the logarithmically scaled output from the 74S471 PROM and present it to the d-a converter for display on a scope.



2. Log response. The logarithmic PROM output corresponding to a linear digital ramp input is shown in the top trace after conversion. The ramp input is shown in the lower trace. The scope is triggered by the overflow in the 8-bit counter that generates the ramp signal.

approach is to place an analog log amplifier between the d-a output and the cathode-ray-tube input. However, use of a programable read-only memory makes possible the much simpler solution shown in Fig. 1.

In this circuit the 74S451 transistor-transistor-logic PROM converts the linear 8-bit amplitude into a logarithmically scaled output code. The two 74LS157's (quad two-line-to-one-line data selectors) allow selection of the linear input or the logarithmic response. When the LIN/LOG select line is low, input pins 2, 5, 11, and 14 of the 74LS157 are connected to output pins 4, 7, 9, and 12, respectively, so the response is linear. But if the display-select line is high (+5 volts), pins 3, 6, 10, and 13 of the 74LS157 are connected to pins 4, 7, 9, and 12, so that the response is logarithmic. Both linear and log output responses to a digital input ramp are shown in Fig. 2.

The PROM is used in a basic look-up scheme. The linear input number serves as the address to the PROM. The stored code effectively performs the operation 20 log (input address), with the output code linearly scaled in decibels. For an input signal with n bits, the smallest output step is k decibels, where k is given by:

$$k = (20 \log 2)\, n/(2^n - 1)$$
$$= 6.02\, n/(2^n - 1)$$

The general form of the output is then:

$$y = (20 \log m)/k$$
$$= (2^n - 1)\,(20 \log m)/6.02n$$

where y is the output code in dB, and m is the linear input code—i.e., the base-10 representation of the binary input number. If the input is a 8-bit binary signal, then:

$$y = 255\,[20 \log (\text{input address})]/48.1$$

In calculating the stored values of the PROM, fractional output codes are rounded to the nearest whole number. Any resulting error is less than 0.1 dB. An input amplitude of zero, which produces an unrepresentable value in decibels, is assigned an output value of zero.

Although the number of PROM output bits does not need to equal the number of input bits, maintaining the equality allows the linear and log displays to have the same base line and full-scale points. □

Converter for oscilloscope provides four-channel displays

by Grady M. Wood
Harris-Intertype Corp., Melbourne, Fla.

With the help of only two integrated circuits and a handful of passive components, conventional single- or dual-channel oscilloscopes can be economically converted to four-channel displays. The key element is a four-channel programable amplifier, the Harris type HA-2405. This is an operational amplifier with four identical input stages, any one of which may be electronically connected to the output stage by two binary address inputs.

For the scope converter circuit, each amplifier is wired in its unity-gain inverting mode. High-value (2 megohm) feedback resistors provide a high input impedance for each channel. All four non-inverting amplifier inputs go to a variable voltage source formed by a 500-kilohm potentiometer that is between the ±15-volt

power supplies. This arrangement provides an independent centering control for each channel. Any offset voltage resulting from the large feedback resistors is not a problem, since the centering control provides adequate amplifier adjustment range.

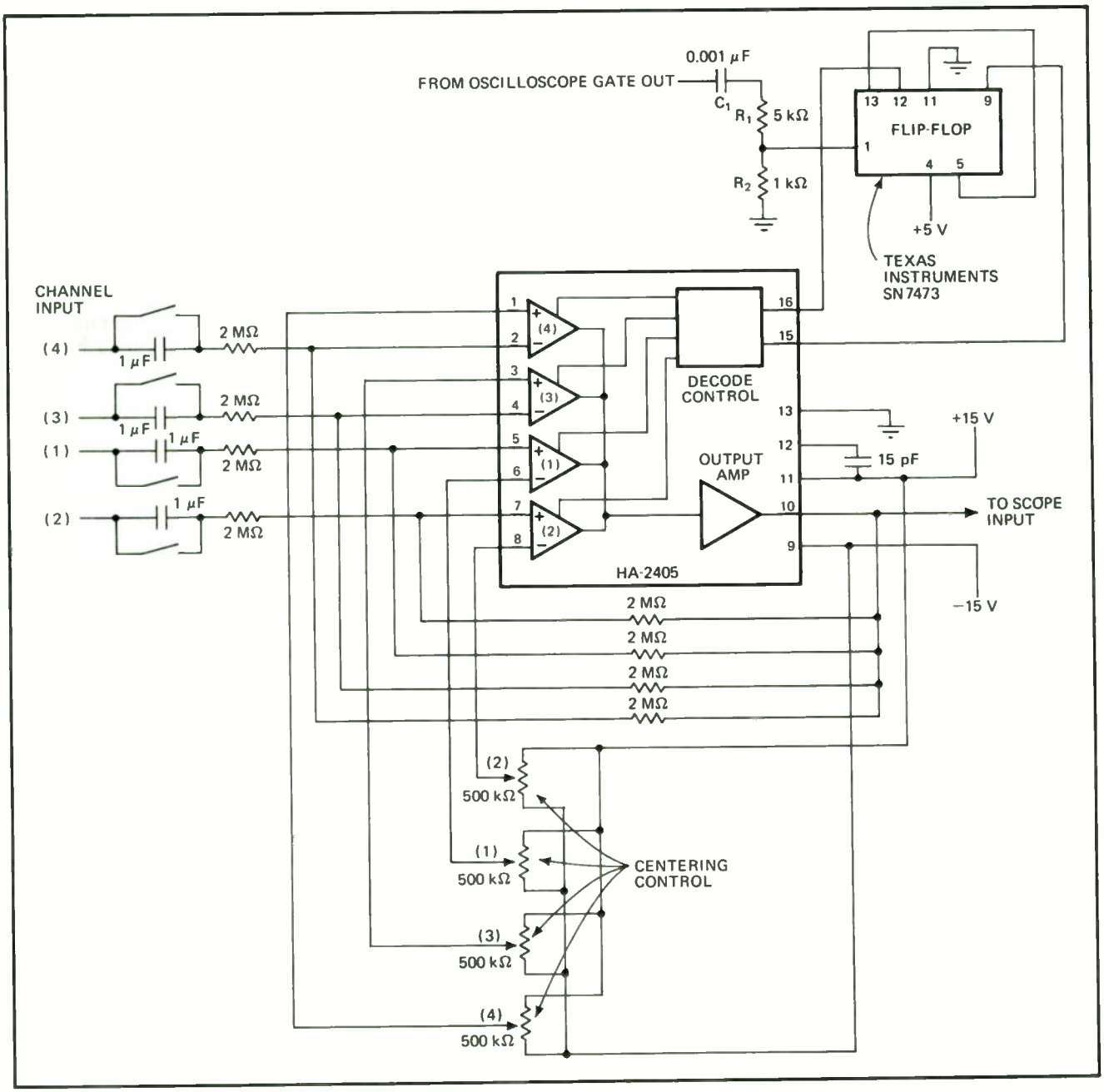
The scope's gate output is divided down by a dual J-K flip-flop to supply binary channel selection signals for the integrated amplifier circuit. This gate signal is synchronized to the scope's sweep, so that there are no timing difficulties. After each trace is completed, the negative-going gate signal selects the next channel. The retrace time allows adequate time for channel selection.

The passive network at the input to the flip-flop—capacitor C_1 and resistors R_1 and R_2—extracts a trigger pulse of approximately 5 V from the 30-V waveform obtained at the GATE OUT terminal of a Tektronix type 545 scope. Other scopes may require a different passive network.

Important circuit performance characteristics include: a gain of 1, a bandwidth of dc to 5 megahertz, a slew rate of 15 V/microsecond, a maximum input voltage of ±10 V, an input impedance of 2 megohms, and a crosstalk figure of 80 decibels.

Circuit voltage range, bandwidth, and input impedance can be increased by adding op amps to buffer each input. Making the gain of each of these buffers independently variable further improves circuit versatility. Approximate parts cost for the entire circuit is $25. □

Scope converter. Monolithic quad operational amplifier provides inexpensive way to increase display capability of standard oscilloscope. Binary inputs drive IC op amp; dual flip-flop divides scope's gate output to obtain channel selection signals. All channels have centering controls for nulling offset voltage. Negative-going scope gate signal selects next channel after each trace. Circuit operates out to 5 MHz.



17. Encoders and decoders

PROM converts binary code to drive 1½-digit display

by V.R. Godbole
North Electric Co., Galion, Ohio

In providing visual readouts for test circuits, inspection equipment, error indicators, and the like, it is often necessary to go from a machine-generated 4-bit binary code to a 1½-digit display of the numbers 0 to 15. This process is usually performed in two steps, but a programable read-only memory can handle it in one.

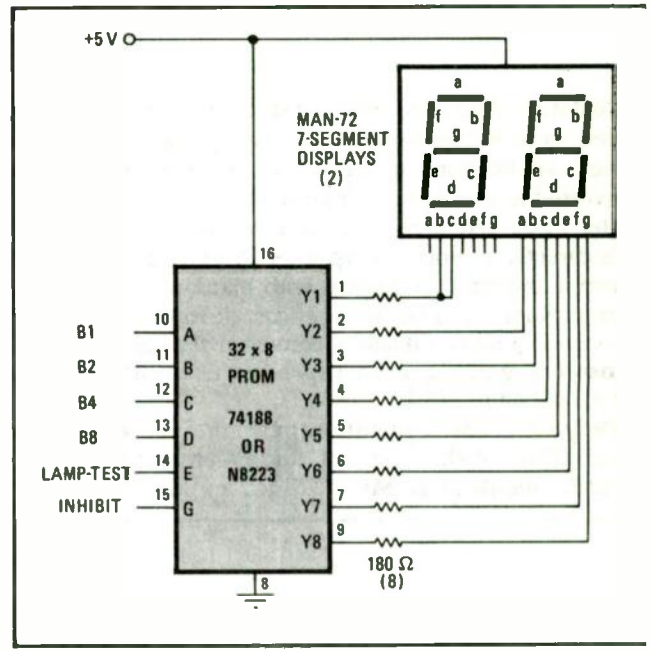
In the usual approach, the first step is to convert the binary code into a BCD code by any one of the several available techniques. The second step is to use standard BCD seven-segment decoder/driver integrated circuits to drive the popular seven-segment visual readouts. The PROM, however, can be programed to accept the binary input signals and generate the proper outputs to drive the display directly.

This use of a PROM has several advantages. Conversion and driving are done in one step, thus providing direct interface to the visual display. Blanking and lamp-test can be included at no extra cost. Space is conserved, and cost is competitive with other approaches.

Binary coding of the numbers from 0 to 15 requires only four binary bits. The most-significant-digit position of the visual decimal display requires only a 1 or else no indication at all; therefore, this digit can be driven by generating only a single output signal that can turn on the segments to show a 1 when required. To drive the seven segments of the least significant digit, seven outputs are needed. Thus the converter/driver must accept four binary inputs and produce eight outputs to drive display segments.

A 32-by-8-bit PROM, type 74188 or N8223, can serve this purpose. The PROM has open-collector outputs with sink capability of 16 milliamperes per output at output voltage of 0.5 volt, enabling it to interface directly with the display segments through suitable resistors. Also, besides performing the necessary conversion, the PROM has additional word capacity that can be used for desirable features such as blanking and lamp-testing at no additional expense. The figure shows the complete circuit diagram for the converter; it requires only the display devices and eight resistors in addition to the memory IC. The truth table lists the instructions required to program the PROM.

Locations 0 through 15 contain the bit patterns that generate segment drives to produce numbers from 0 to 15. Locations 16 through 31 are left unprogramed; therefore when the lamp-test input is taken to a logic 1, one of locations 16 through 31 is addressed. This circuit state causes all outputs to be set at logic 0, turns all segments on, and produces the number 18. When the inhibit input is taken to a logic 1, the PROM outputs are turned off and cause the display to be blanked. □



Here's how. PROM drives seven-segment display to show decimal value of 4-bit input signal. This compact interface is convenient in microprocessor circuits, which often have spare PROM capacity. A 32-by-8-bit PROM can provide the drive signals for numbers 0 through 15 and also accommodate lamp-test and inhibit commands. Applications include test-number indication in small test instruments and display of settings on binary-output touch switches.

TRUTH TABLE AND PROGRAM FOR DRIVING 1½-DIGIT DISPLAY

Inhibit	Lamp test	B8	B4	B2	B1	Display	Program in memory Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8
0	0	0	0	0	0	0	1	0	0	0	0	0	0	1
0	0	0	0	0	1	1	1	1	0	0	1	1	1	1
0	0	0	0	1	0	2	1	0	0	1	0	0	1	0
0	0	0	0	1	1	3	1	0	0	0	0	1	1	0
0	0	0	1	0	0	4	1	1	0	0	1	1	0	0
0	0	0	1	0	1	5	1	0	1	0	0	1	0	0
0	0	0	1	1	0	6	1	1	1	0	0	0	0	0
0	0	0	1	1	1	7	1	0	0	0	1	1	1	1
0	0	1	0	0	0	8	1	0	0	0	0	0	0	0
0	0	1	0	0	1	9	1	0	0	0	1	1	0	0
0	0	1	0	1	0	10	0	0	0	0	0	0	0	1
0	0	1	0	1	1	11	0	1	0	0	1	1	1	1
0	0	1	1	0	0	12	0	0	0	1	0	0	1	0
0	0	1	1	0	1	13	0	0	0	0	0	1	1	0
0	0	1	1	1	0	14	0	1	0	0	1	1	0	0
0	0	1	1	1	1	15	0	0	1	0	0	1	0	0
1	X	X	X	X	X	(OFF)	1	1	1	1	1	1	1	1
0	1	X	X	X	X	18	0	0	0	0	0	0	0	0

1 = HIGH 0 = LOW X = DON'T CARE

Converter changes 7-segment output to decimal or BCD

by Prentice L. Orswell
National Oceanic and Atmospheric Administration, Boulder, Colo.

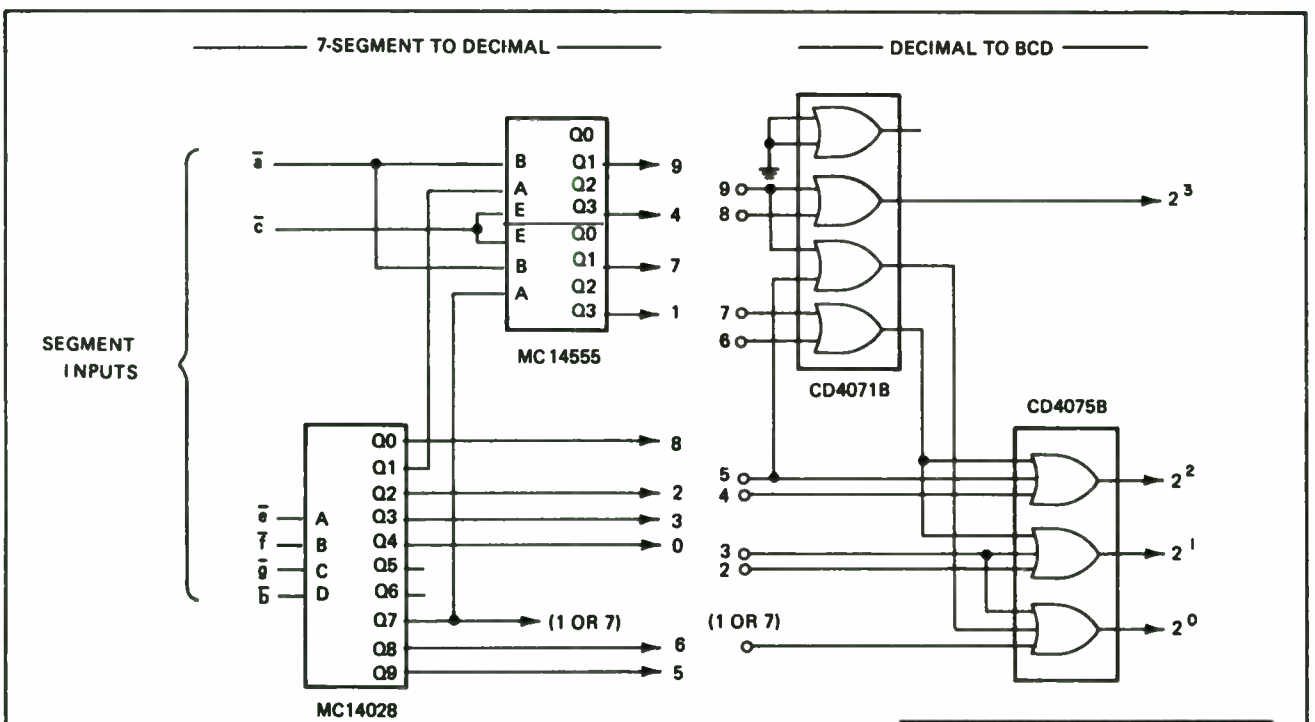
Calculator chips and other LSI circuits with outputs coded to drive seven-segment displays can have more varied applications if the seven-segment outputs are converted to decimal or binary-coded decimal. The converter described here accepts seven-segment MOS signals directly at voltages up to +15 volts and provides decimal and/or BCD outputs with blanking. It uses only four packages, at a component cost of less than $5. (For a seven-segment-to-decimal converter that used discrete transistors, gates, and an expensive demultiplexer, see the article on p. 128.]

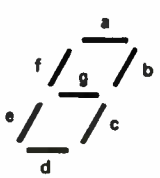
Only six of the segment outputs are required for this circuit. Four of them—b, e, f, and g—are applied to the input terminals of an MC14028 IC; a and c are applied to an MC14555, along with two signals from the MC14028. These two packages have a combined total of 10 output terminals, one of which goes high to represent a numeral (0 through 9) when the complements of the numeral's seven-segment voltages are applied at the input; most LSI circuits provide complementary outputs. The 10 terminals are the decimal outputs. (Another output, corresponding to either 1 or 7, is discussed below.)

If BCD outputs are desired, the decimal outputs are connected to the input terminals of a CD4071B and a CD4075B. These units provide a total of four output terminals, which go high to represent the four BCD bits.

In the seven-segment-to-decimal portion of the circuit, the MC14028 (which is a BCD-to-decimal decoder) uniquely determines six of the decimal outputs. The complements of b, e, f, and g segment voltages for both 1 and 7 decode to output Q7, and digits 4 and 9 both decode to Q1. To separate these in the MC14555 (which is a dual binary-to-1-of-4 decoder), the complement of a is used as an additional input. Full blanking is assured by applying the complement of c at the enable inputs.

Conversion to BCD from the decimal code could be accomplished in several ways. An ideal one-package so-





7-SEG. DIGIT	SEGMENT ā c̄ d̄	SEGMENT b̄ g̃ f̄ e	MC14028 OUTPUT SELECTED
0	000	0100	Q4
1	101	0111	Q7
2	010	0010	Q2
3	000	0011	Q3
4	101	0001	Q1
5	000	1001	Q9
6	000	1000	Q8
7	001	0111	Q7
8	000	0000	Q0
9	000	0001	Q1
BLANK	111	1111	ALL LOW

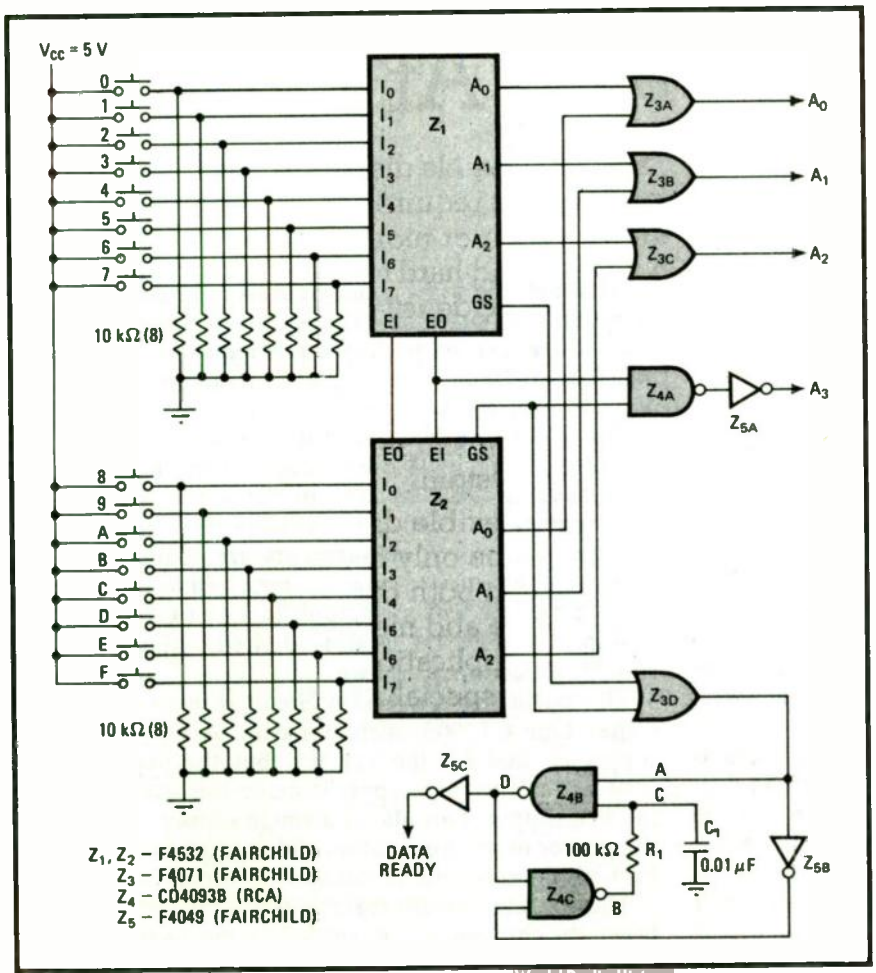
Converter. Complements of seven-segment voltages, fed into inputs of this circuit, produce high level on one of the decimal-output lines and (if the conversion is carried over to the BCD) on one or more of the BCD output lines. Thus for segment voltages that could display a seven-segment 5, inputs for the b and e segments are high, producing a voltage on decimal output line marked 5; and if BCD-to-decimal stage is connected, lines marked 2^0 and 2^3 go high.

lution would be a 10-bit priority encoder, but this circuit is not available in C-MOS, so at least two packages are required to implement the encoder. An 8-bit priority encoder and some gating would work. A more economical approach, using OR gates, is shown in the diagram. Note that one gate is saved for other uses by utilizing the 1-or-7 output. All of the BCD outputs go low with blanking. □

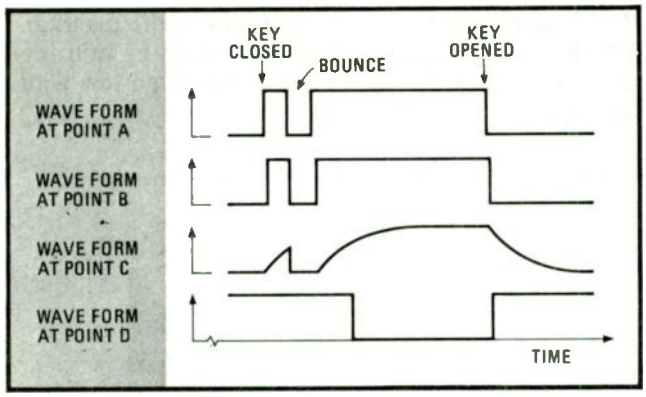
Hexadecimal encoder debounces keyboard

by Ralph Tenny
Texas Instruments Inc., Dallas, Texas

Programs and instructions for microprocessors are commonly written in hexadecimal machine code (0, 1, . . . 9, A, B, . . . F), but must be fed into memory in binary code. In the 16-key encoding keyboard circuit described here, the unique application of two eight-input priority encoders provides the user with key lockout—if he accidentally presses two keys to one encoder simultaneously, only the higher value is encoded, and oper-



1. Encodes and debounces. Pressing any one of the 16 hexadecimal-digit keys produces the corresponding 4-bit binary output through the two priority encoders Z_1 and Z_2. Key debounce is provided by the Schmitt trigger delay latch Z_{4B}/Z_{4C}, as illustrated in Fig. 2. This keyboard is a convenient interface to microprocessors or other binary devices for which instructions may be written in hexadecimal code.



2. Less bounce to the ounce. Wave forms at four points in delay latch illustrate how R_1C_1 delay and Schmitt trigger action prevent key-bounce from generating multiple outputs.

ation of one encoder automatically disables the other.

Another unique feature of the circuit is a delay latch, which debounces the keys. Only when the key contacts have settled down to a steady closed or open position can the microprocessor read the code.

As Fig. 1 shows, the circuit accepts the hexadecimal input over 16 keys and translates it into 4-bit binary outputs for parallel feed to a computer. The priority encoders provide the basic encoding.

The keys are arranged in two groups, 0 through 7 and 8 through F. Each subgroup is encoded in 3-bit binary code; if two keys in the same subgroup are pressed, the code output corresponds to the highest-priority key depressed. Lockout between subgroups is accomplished by cross-coupling the enable-input (EI) and enable-output (EO) pins, so that the output code is decided by which subgroup is accessed first. Encoding for the fourth bit is accomplished by an AND gate between the low-order enable-output and the high-order group-select (GS). The composite output code then consists of the subgroup output bits ORed together for the lower three bits, and the fourth bit output.

The keys are debounced by delay latch Z_{4B}/Z_{4C}. The basic ingredients of the latch are the CD4093B Schmitt trigger elements and an RC delay (R_1 and C_1) in the feedback loop of the latch. The debounce wave forms in Fig. 2 show that a key must stop bouncing before the latch feedback, delayed by a time 0.85 R_1C_1, locks in the key action. Release of a key immediately resets the latch, with the input bypassing the delay loop. It is imperative that a Schmitt trigger be incorporated in the delay latch, but the use of C-MOS holds down the size and cost of the capacitor. The values of C_1 and R_1 are determined by the bounce characteristics of the push-button keys. The 0.01 microfarad and 100 kilohms shown in Fig. 1 will debounce almost any key. □

Providing a decimal output for a calculator chip

by Jack Lambert
Lambert Associates, Lexington, Mass.

Calculator chips, which are becoming readily available, can be used to advantage in applications other than pocket calculators. However, these chips usually have an output that drives a multiplexed seven-segment display. This is not really convenient for performing subsequent operations or even for interfacing with Nixie-type readouts.

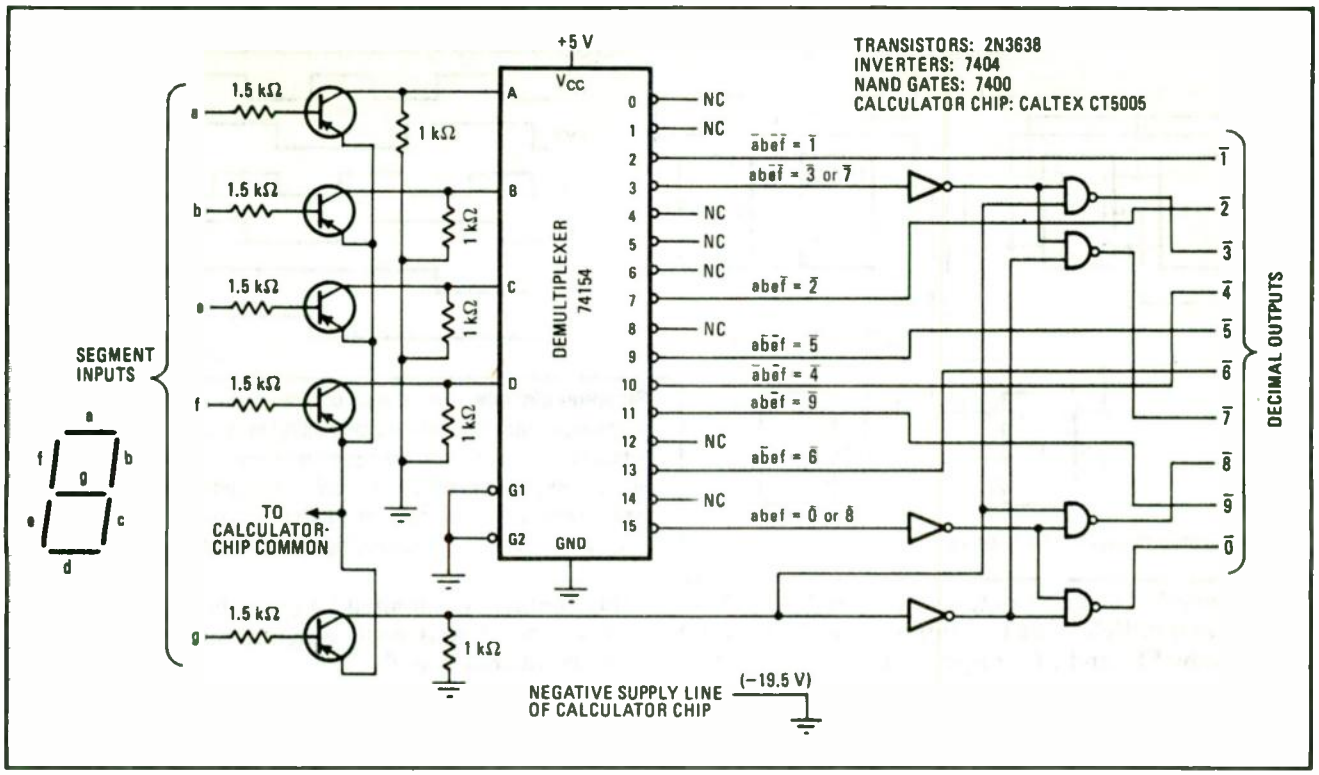
With the circuit shown here, the output of a calculator chip can be converted to the more convenient decimal form. If desired, this decimal output can also be converted, for example, to a binary-coded-decimal form. A calculator chip having a decimal output can be used as an input to another calculator, to operate a large dot-matrix display, to feed a printer, or to drive a digital controller or computer.

Although the conversion circuit is not necessarily the simplest logic scheme, it is easy to set up and to wire. Only three TTL IC packages are required—they are a four-line-to-16-line demultiplexer, a hex inverter, and a quad two-input NAND gate.

The lower-case letters in the diagram correspond to the display segments used to set up the logic for the conversion circuit. Only five of the seven possible segment inputs are needed to develop all of the decimal outputs; the other two segments are redundant. The seven-segment logic inputs are high, while the decimal outputs are low. The gate inputs (G1 and G2) to the demultiplexer may be used if desired, otherwise they should be tied low, as shown.

This particular conversion circuit is intended for the Caltex type CT5005 calculator chip. A separate 5-volt supply is used for the TTL ICs, but the negative line (−19.5 V) of the chip supply is made the ground line of the TTL supply. This allows a single supply, one having the proper dropping resistors and regulation, to be used for both the chip and the conversion circuit.

The discrete transistors serve as a simple interface between the chip and TTL devices. This means that the display outputs of the chip can directly drive the conver-



More applications. Decoder circuit converts the seven-segment-display outputs of a calculator chip to decimal form, greatly increasing the application versatility of the chip. All 10 of the decimal outputs can be derived from only five of the segment inputs. The same power supply is used for both the chip and the decoder's TTL circuitry. The chip's negative supply line acts as ground for the TTL supply.

sion circuit. Of course, a chip other than the type CT5005 device may require other interfacing.

The use of the type 74154 demultiplexer results in a certain amount of redundancy in the circuit's decoding process. However, the demultiplexer does keep the wiring simple, and it also conserves board space without increasing parts cost significantly. The entire circuit costs about $3.50 to build. □

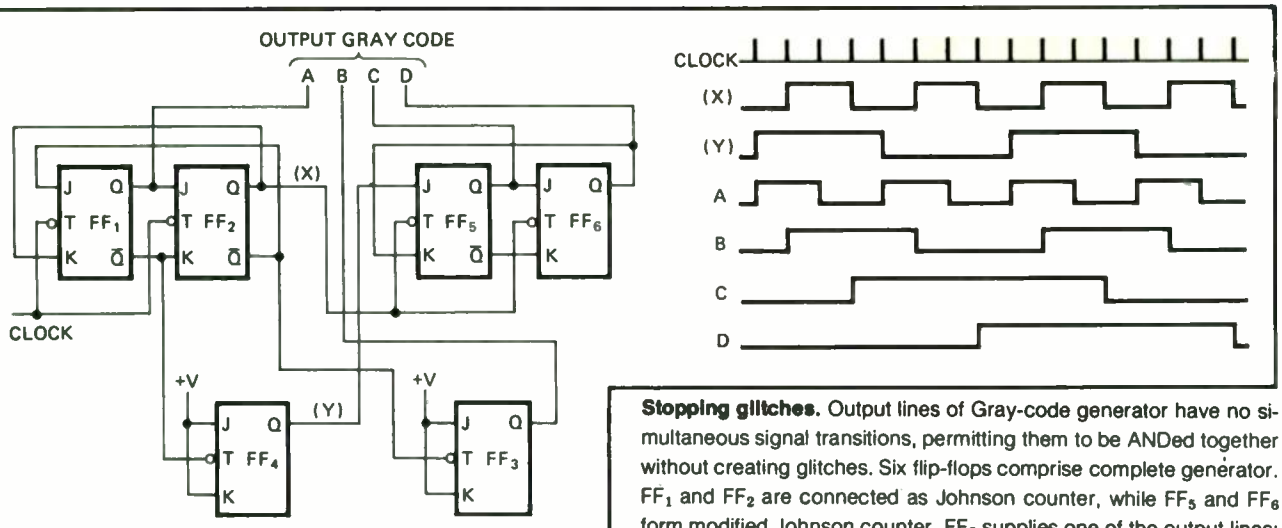
Gray-code generator avoids output glitches

by Carl Moser
Western Electric Co., Winston-Salem, N.C.

When binary signals are ANDed together, undesirable glitches can be generated at a circuit's output if one or more signal transitions are simultaneous. A Gray-code generator can be built with six J-K flip-flops that are arranged so that only one signal transition occurs at any particular time. Therefore, the four output signals forming the Gray code can be ANDed without glitches.

Flip-flops FF_1 and FF_2 are wired as a Johnson counter. The Q output or FF_1, which is 90° out of phase with the Q output of FF_2, provides the A Gray-code output line. Flip-flop FF_3 is toggled by the $\overline{Q}$ output of FF_2, causing it to produce the B Gray-code output line.

The other three flip-flops, FF_4 through FF_6, form a modified Johnson counter. FF_5 and FF_6 are toggled



Stopping glitches. Output lines of Gray-code generator have no simultaneous signal transitions, permitting them to be ANDed together without creating glitches. Six flip-flops comprise complete generator. FF_1 and FF_2 are connected as Johnson counter, while FF_5 and FF_6 form modified Johnson counter. FF_3 supplies one of the output lines; FF_4 is part of simultaneous toggling scheme for FF_5 and FF_6.

simultaneously by the Q outputs (labeled X and Y in the diagram) of FF_2 and FF_4. Output lines C and D are generated by FF_5 and FF_6, respectively.

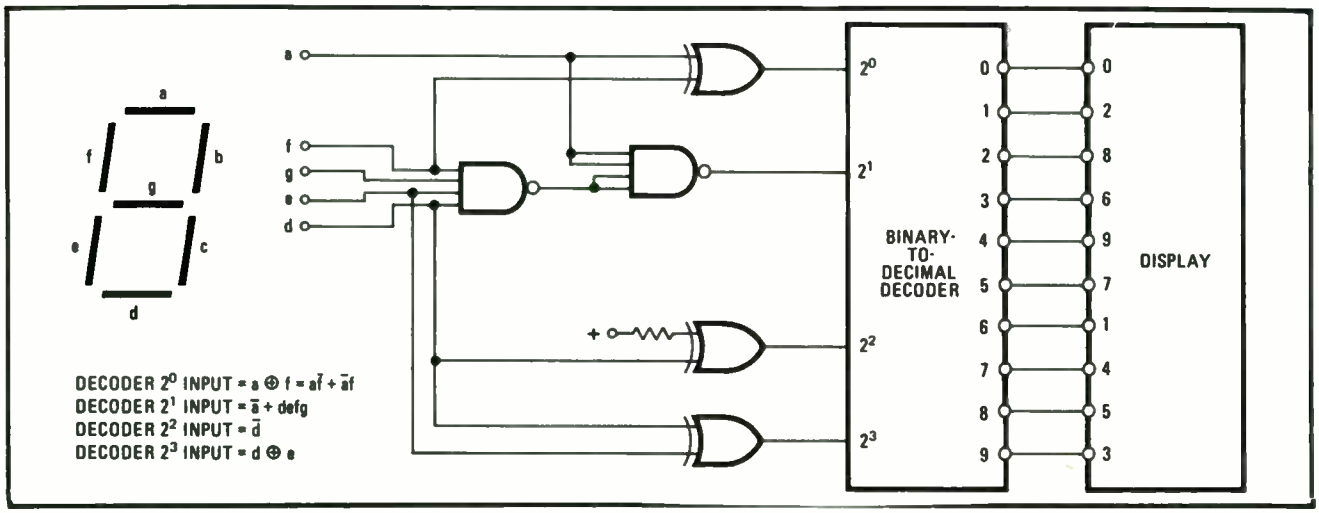
Since the circuit is asynchronous, its maximum operating frequency is limited by the delay of the flip-flops. For correct output code generation, all the flip-flops must be cleared initially. □

IC trio converts 7-segment code to decimal

by James Southway,
McDonnell Douglas Astronautics Co., St. Louis, Mo.

A device that converts a seven-segment display code into decimal code and is less expensive than the demultiplexer described in a previous article [see articles pp. 126 and 128], uses only three integrated circuits. The only other requirement is front-end buffering, and only if its TTL circuitry is to be used with a MOS system. Like the demultiplexer, this device enables a seven-segment display code to directly drive any kind of cold-cathode gas discharge indicator tubes.

The small number of ICs is made possible, in part, by combining the logic of the binary-to-decimal decoder with a few external logic gates, and by cross-wiring the decoder outputs to the display inputs. In other words, output 1 of the decoder drives the display input for 2; output 4 drives the input 9, and so on. (The only uncrossed output is 0, as shown in the diagram.) The decoder is a 74141 or equivalent; the external logic is one dual four-input NAND, 7420, and one quad exclusive-OR, 7486. Another saving is made by using one of the four exclusive-OR gates in the 7486 as an inverter, and one of the two four-input NANDs in the 7420 as a two-input NAND. □



Converter. Seven-segment display code is converted into a 1-out-of-10 code for driving such things as indicator tubes, and uses only three integrated circuits. Decoder, external logic, and cross-wired outputs keep the IC count low.

18. Filters

Digital-to-analog converter controls active filter

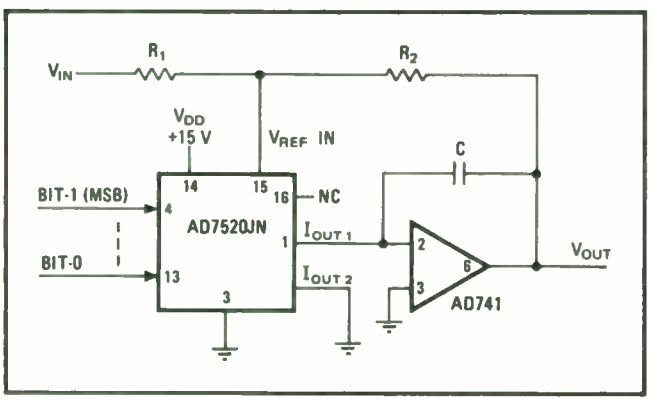
by Jerry Whitmore,
Analog Devices, Santa Clara, Calif.

A monolithic digital-to-analog converter can be the control element of an active filter. Shown in Fig. 1 is a circuit that generates a low-pass, single pole that can be moved over a dynamic frequency range of 2^n:1, where n is the resolution in bits of the d-a converter. If, for example, a converter with 10-bit resolution is used in this circuit, dynamic range is 1,024:1.

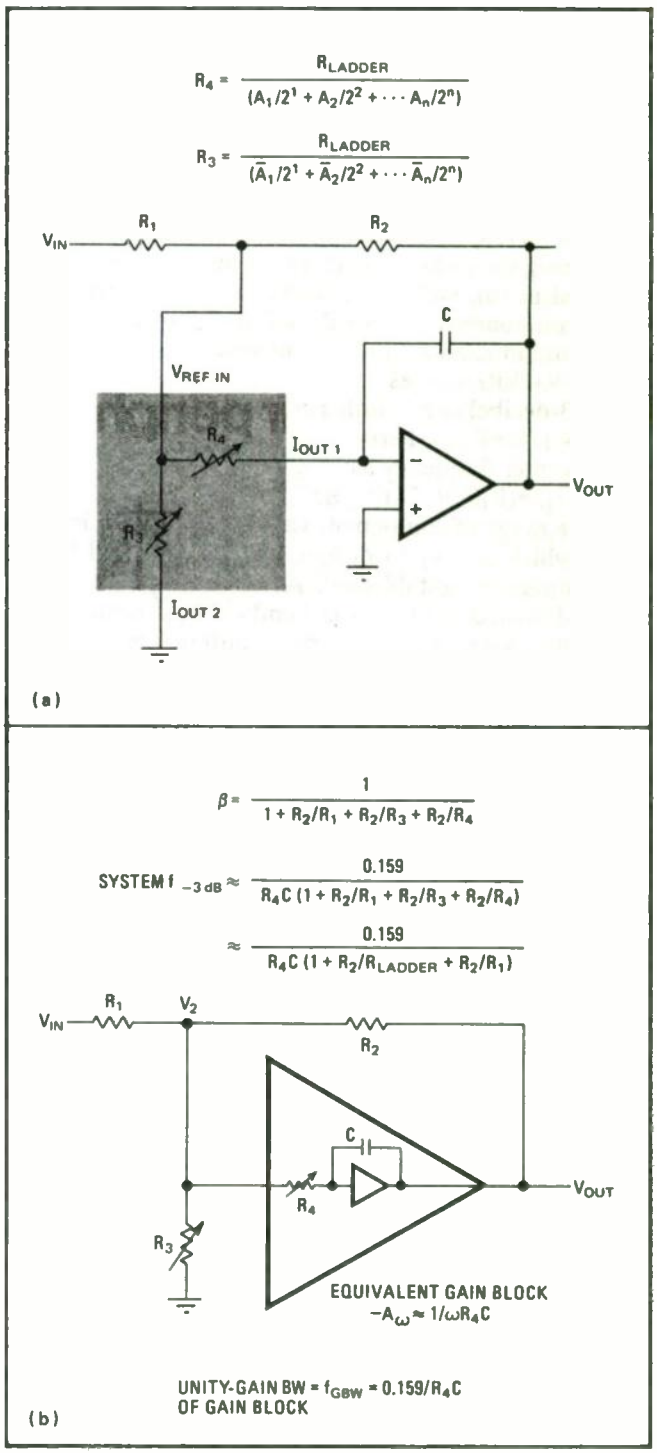
An equivalent simplified version of Fig. 1 is shown in Fig. 2(a), where R_4 and R_3 take on the values shown. R_{ladder} is the characteristic resistance of the R-2R ladder of the d-a converter and the coefficients A assume a value of 1 for an on bit, and zero for an off bit. Note that R_4 in parallel with R_3 equals R_{ladder}.

The circuit, consisting of R_4, C, and the amplifier, can be treated as a gain block as shown in Fig. 2(b). At frequencies above the open-loop corner, the response of the gain block is $A(\omega) = V_{out}/V_2$ or about $1/\omega R_4C$. Its unity gain bandwidth is $F_{GBW} = 0.159/R_4C$.

Frequency response of a closed-loop amplifier is $F_{3dB} = BF_{GBW}$ where B is the amplifier feedback attenuation ratio. Using the unity gain bandwidth of the gain block and the system B results in the filter closed loop frequency response equations shown in Fig. 2(b). □



1. 1,024:1. An active low-pass filter such as this, built around an operational amplifier, passive components, and a 10-bit digital-to-analog converter, has a dynamic-frequency range of 1,024:1.



2. Equivalent circuits. The d-a of (1) can be replaced by the circuit within the dashed lines (a). A further simplification (b) lumps R4, C and the op amp into a gain block.

Active filter has separate band and frequency controls

by John Jenkins
Montgomery, Ala.

The bandwidth and center frequency of an active bandpass filter can be controlled independently by two separate resistors. Moreover, the filter's gain remains at unity over its full tuning range. Filter Q range is 2 to 200, while center frequency is 1 to 10 kilohertz.

The circuit shown in (a) has these properties, but it requires a variable inductor, which is usually difficult to tune, can be large, and cannot provide good temperature stability. The transfer function for this LC filter is:

$$e_o/e_i = (s/R_1C_1)/(s^2 + s/R_1C_1 + 1/LC_1)$$

Replacing the inductor with an active RC network, as illustrated in (b), yields a temperature-stable circuit. If all the components are ideal and $R_2C_2 = R_3C_3$, the equivalent inductance can be expressed as:

$$L_{eq} = R_2C_2R_f \text{ henries}$$

and the 3-decibel bandwidth as:

$$BW = 1/(2\pi R_1C_1) \text{ hertz}$$

and the center frequency as:

$$f_o = 1/[2\pi(R_fC_1R_2C_2)^{1/2}] \text{ Hz}$$

A wide range of component values can be used in the circuit, which is easy to design, once the desired filter specifications are established. As an example, a filter will be designed with a 5-Hz bandwidth, a center frequency of 1 kHz, and a maximum output voltage of 1 volt peak-to-peak. A few important operational amplifier specifications must also be known. Typically, input resistance (R_i) is greater than 40 kilohms, output resistance (R_o) is less than 200 ohms, voltage gain (G_v) is more than 10,000, and output voltage swing (V_{os}) exceeds 20 v pk-pk.

To solve the design equations, let:

$$K_1 = (R_fC_1R_2C_2)^{1/2} = 1/(2\pi f_o) = 1.59 \times 10^{-4}$$
$$K_2 = R_1C_1 = 1/(2\pi BW) = 3.18 \times 10^{-2}$$
$$K_3 = (R_fC_1/R_2C_2)^{1/2} = [(V_{os2}/e_{omax})^2 - 1]^{1/2} = 19.98$$

then the filter's time constants can be computed:

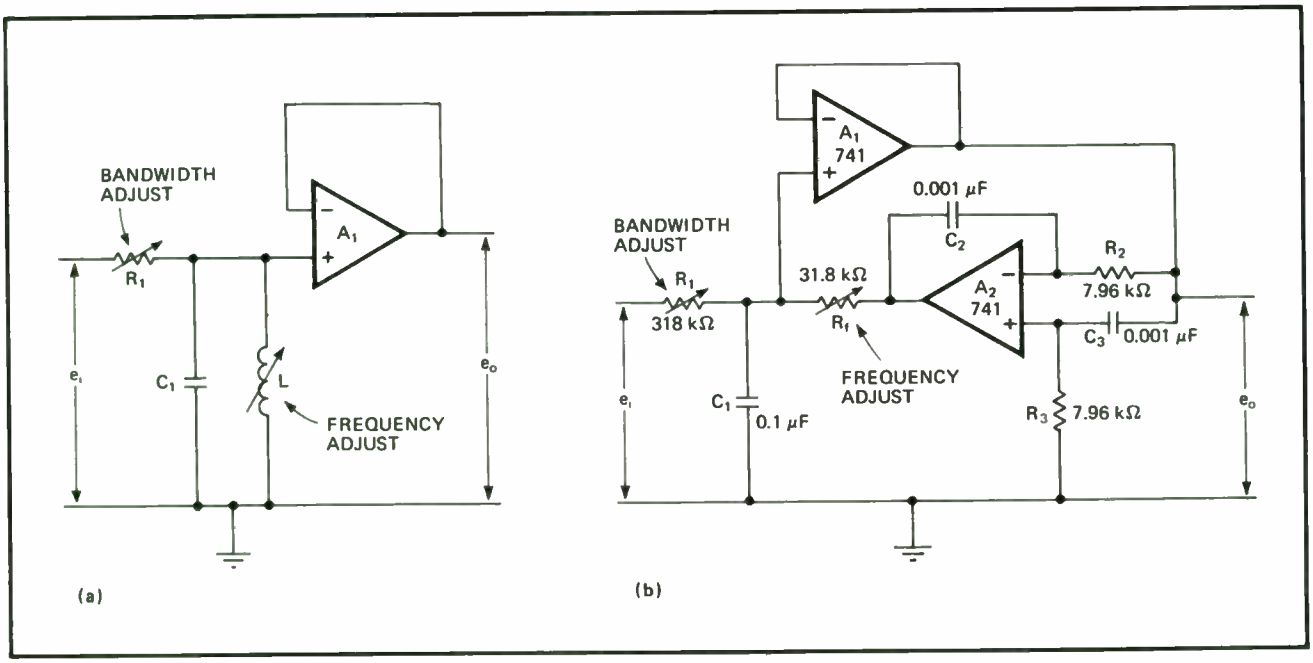
$$R_1C_1 = K_2 = 3.18 \times 10^{-2}$$
$$R_2C_2 = K_1/K_3 = 7.96 \times 10^{-6}$$
$$R_fC_1 = K_1K_3 = 3.18 \times 10^{-3}$$
$$R_f/R_1 = K_1K_3/K_2 = 0.1$$

For most applications, a few simplified guidelines can be followed to choose component values: resistor R_1 should be less than 400 kilohms, resistor R_2 should lie between R_{i2} (about 40 kilohms) and 1 kilohm, the load resistance should be greater than 1 kilohm, and factor $(1 - R_3C_3/R_2C_2)$ should range between 0 and resistance ratio $(R_f/R_1) \times 10^{-2}$.

This last constraint requires that time constant R_2C_2 track R_3C_3 within +0% and -0.1%. Therefore, these resistors and capacitors must have closely matched temperature coefficients and operating temperatures. Metal-film resistors and NPO-type capacitors that are mounted close together can be used. (The R_2C_2 and R_3C_3 time constants can be aligned by first opening the filter's input to obtain maximum Q, then increasing R_3 until oscillation occurs, and then decreasing R_3 until oscillation just stops.)

A set of typical component values is noted in (b). As indicated, resistor R_1 tunes filter bandwidth, while resistor R_f adjusts center frequency. □

Active circuit ousts variable inductor. Bandpass filter (a) offers independent center frequency and bandwidth adjustments. Hard-to-tune variable inductor can be replaced by active circuit (b) that provides an equivalent inductance and better temperature stability. Fully active filter is easy to design and will operate over a broad range of component values. General-purpose amplifiers can be used.



Wien bridge in notch filter gives 60 dB rejection

by Donald DeKold
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A modified phase splitter and Wien bridge network form a notch filter that is capable of providing 60 decibels of signal rejection. The bridge network, which consists of two capacitors and two resistors, makes this high rejection possible and allows the filter to be tuned with ganged capacitors or resistors. The three-capacitor, three-resistor bridge ordinarily used for the twin-T variety of notch filter is not as easy to null because more components must be trimmed, and maximum notch depth is usually about 45 dB.

Because of the wideband frequency response of its modified phase splitter, the filter (a) can operate from subaudio frequencies up to hundreds of kilohertz. For very-low-frequency performance, however, a direct coupling scheme must be worked out.

Unlike a unity-gain phase splitter, the filter's phase splitter has a gain of approximately -2 at its collector. If collector resistance is small with respect to resistor R of the bridge, the ac equivalent circuit of (b) can be drawn. The voltage transfer function of the equivalent circuit is:

$$H(s) = V_o(s)/V_i(s) = (s^2C^2R^2 + 1)/(s^2C^2R^2 + 3sCR + 1)$$

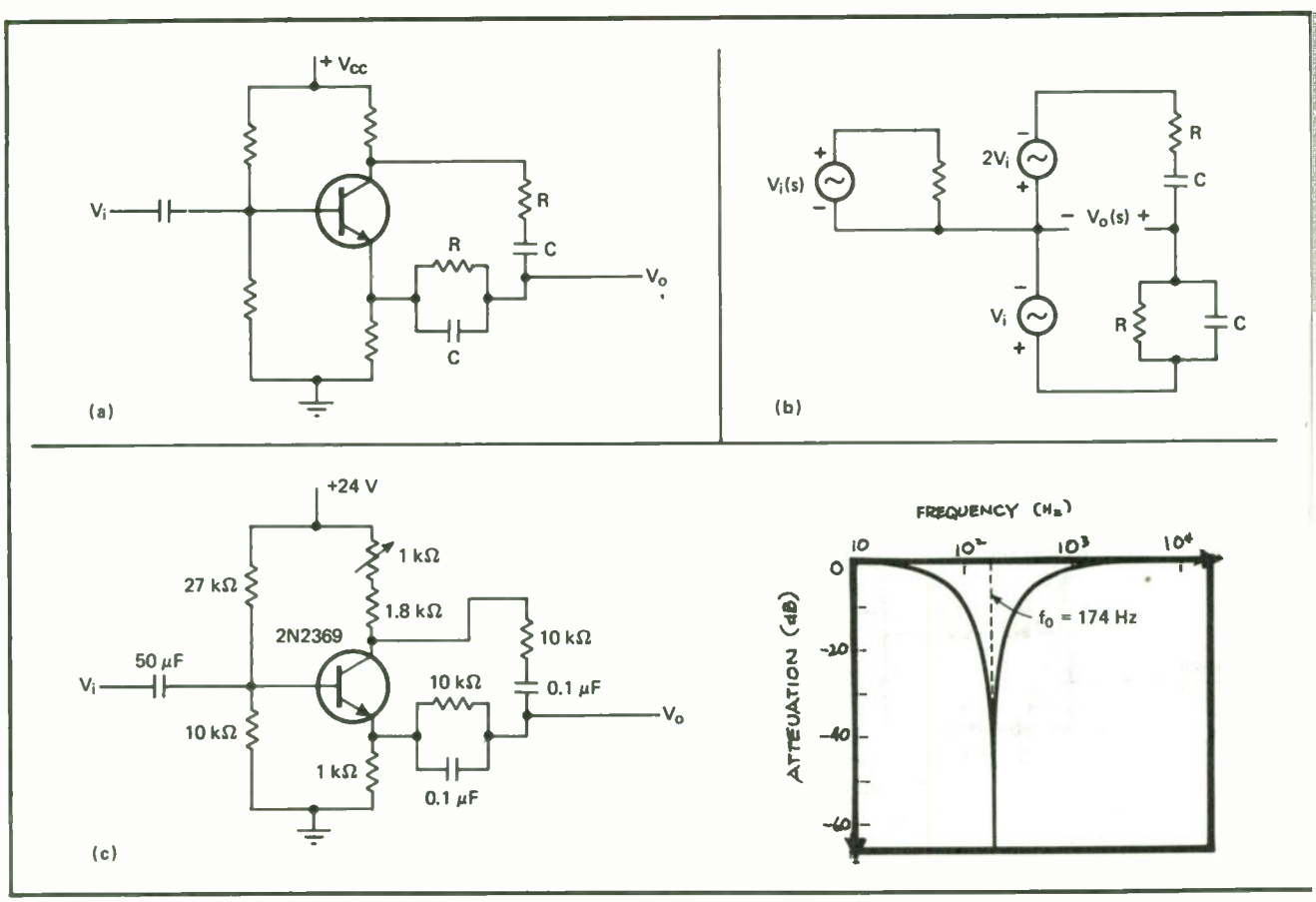
where $s = j\omega$, with ω representing frequency.

This transfer function has a transmission zero at $\omega = 1/RC$, the center frequency of the notch. At frequencies above and below the notch frequency, H(s) approaches unity. Since every R is paired with a C in the expression for H(s), the shape of the transfer characteristic cannot be changed by varying the ratio of R/C. The filter's Q, therefore, is constant for any value of R or C, or at any frequency for which the notch is designed.

A practical implementation of the filter is shown in (c), along with its frequency response. Instead of a single collector resistor, a potentiometer and a series resistor are used so that the filter can be adjusted for maximum signal rejection.

Employing a standard dual ganged variable capacitor for the bridge capacitors allows the notch to be tuned from 8 to 200 kHz. Notch depth may vary because of imperfect tracking of the capacitors, but will never drop below a minimum of 45 dB. Because the filter operates at a high impedance level, it should be shielded to avoid noise pickup at the output node. □

Effective notch. Non-unity-gain phase splitter and four-element Wein bridge make up notch filter (a) capable of suppressing unwanted signals by 60 decibels. Ganged variable components can be used for bridge R or C, allowing notch to be tuned over broad frequency range. Filter transfer function can be found from equivalent circuit (b). Practical filter (c) has adjustable collector resistance.



Voltage-tuned filter varies center frequency linearly

by Vassilios J. Georgiou
University of Massachusetts, Amherst, Mass.

Although a voltage-tunable multiple-feedback active filter generally offers constant gain and constant bandwidth throughout its tuning range, its tuning curve for center frequency versus control voltage is usually highly nonlinear for extended frequencies. This is due to the nonlinearity of the field-effect transistor, which is used as a variable resistor, and because the center frequency varies inversely with the square root of the FET's drain-source resistance. Employing feedback, therefore, to linearize the FET's behavior is not a solution.

Instead, a modified version of the diode function generator can be used to drive the FET's gate terminal. For the voltage-tunable bandpass filter shown, center frequency remains nearly linear for changing control voltage over a center-frequency range of 4.5:1.

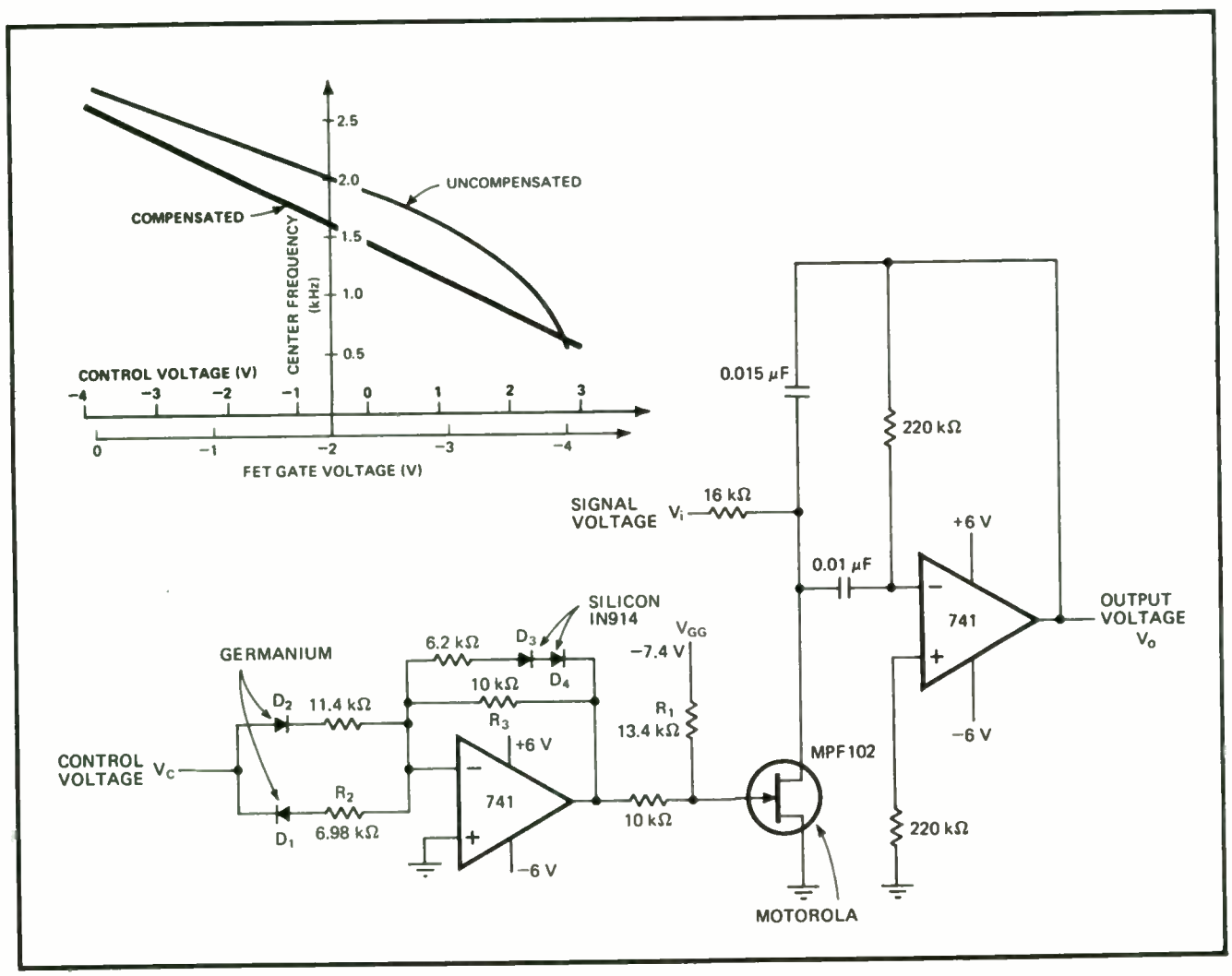
Resistor R_1 and supply voltage V_{GG} bias the FET at −3 volts, thereby setting the filter's first breakpoint for $V_C = 0$ at 1,460 hertz. For negative values of control voltage, only diode D_1 conducts, and the gain of the amplifier is determined by resistors R_2 and R_3.

For positive control voltages, diode D_2 conducts, and amplifier gain is about half the value it is for negative control voltages. As a result, the lower portion (right-hand side) of the filter's tuning curve tilts upward and aligns with the upper portion (left-hand side) to form a linear characteristic.

Diodes D_3 and D_4 define the second filter breakpoint—at $V_C = 2.4$ V—by further reducing amplifier gain and extending linear operation to 570 Hz. Preferably, the germanium diodes, D_1 and D_2, should be gold-doped so that they have a low forward-voltage drop. □

BIBLIOGRAPHY
G. Deboo and R. Hedlund, "Automatically Tuned Filter Uses IC Op Amps," EDN/EEE, Feb. 1, 1972, p. 38.

Straight-line tuning. Modified diode function generator (in color) drives FET variable resistor for voltage-tunable bandpass filter, causing center frequency to vary linearly with control voltage over 4.5:1 frequency range. Gain of function-generator amplifier is reduced for positive control voltages to raise lower section of (uncompensated) tuning curve. Compensated filter remains nearly linear.



Tunable active filter has switchable response

by Philbrook Cushing
La Jolla, Calif.

With a minimum number of components, a positive-feedback active filter that has a continuously tunable cutoff frequency from 20 hertz to 20 kilohertz can be built. Additionally, the inexpensive filter provides switch-selectable low-pass or high-pass responses with either Bessel (RC) or Butterworth (maximally flat) characteristics. The skirt rolloff is 40 decibels per decade.

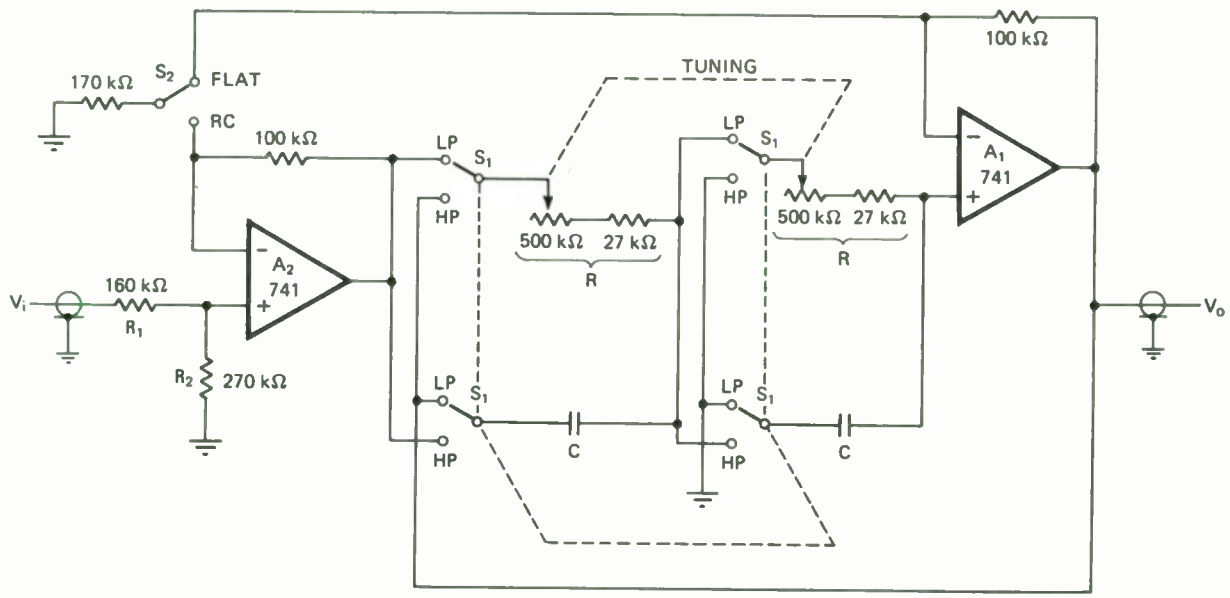
Basically, the filter consists of amplifier A_1, two equal variable resistors (designated as R), and two equal capacitors (designated as C). A four-pole switch, S_1, interchanges the resistors and capacitors to vary filter response between high-pass and low-pass. The filter's cutoff frequency can be written as:

$$\omega_o = 1/RC$$

Another switch, S_2, changes the filter's characteristic. With S_2 at its RC position, the gain of amplifier A_1 is unity, giving the filter a Bessel characteristic. With S_2 at its "flat" position, A_1's gain becomes 1.59, which produces a Butterworth function. The corresponding gains for amplifier A_2 are 1.59 and unity, so that the gain product from A_2's noninverting input to the output is 1.59 for either setting of switch S_2. Resistors R_1 and R_2 reduce over-all gain to unity for easy cascading.

Output offset voltage, as well as its variation with tuning, may be zeroed out by applying conventional nulling methods at amplifier A_1. The slew rate of the type 741 operational amplifier limits the flat portion of the high-pass response to about 40 kilohertz at a 3-volt peak-to-peak signal level. If two filters are cascaded, bandpass and band-reject responses can be added. □

Versatile filter. Positive-feedback active filter can be tuned continuously from 20 hertz to 20 kilohertz. Two switches provide choice of output—either low-pass (LP) or high-pass (HP) response having either Bessel (RC) or Butterworth (flat) characteristic. Switch S_1 interchanges resistors and capacitors that determine cutoff frequency, while switch S_2 changes gain of amplifiers A_1 and A_2.



CUTOFF FREQUENCY	C (μF)
20 Hz – 200 Hz	0.02
200 Hz – 2 kHz	0.002
2 kHz – 20 kHz	0.0002

R: ALLEN-BRADLEY TYPE J, ± 10%
C: POLYSTYRENE, MALLORY TYPE SX, ±5%

Two-IC digital filter varies passband easily

by Andrew M. Volk
University of Wisconsin, Madison, Wis.

Only two integrated circuits—a dual monostable and a three-input NAND gate—are needed to build a digital filter that offers completely adjustable cutoff frequencies as well as excellent frequency stability. The bandpass filter is also independent of the duty cycle of the input waveform. It can be used in a variety of circuits, for instance, in tone-controlled devices or for fm demodulation of digital codes.

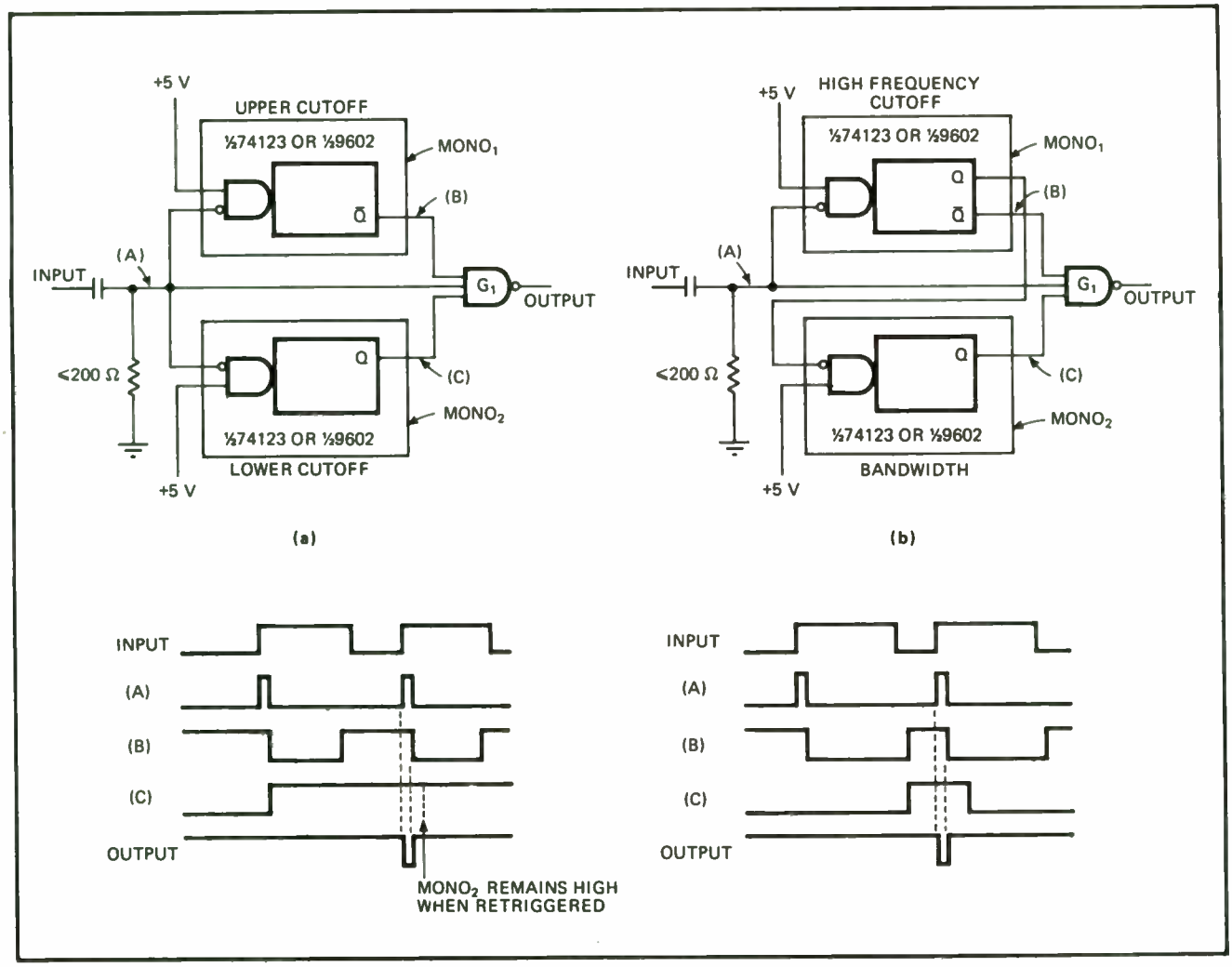
The input RC differentiator makes the filter independent of the duty cycle of the input. In (a), the lower and upper cutoff frequencies of the filter's passband are determined by the retriggerable monostable multivibrators. The output pulse length of the first monostable ($MONO_1$) is set to the period of the highest frequency of interest, while the output pulse length of the second ($MONO_2$) is set for the lowest frequency wanted.

If an input pulse appears after $MONO_1$ times out but while $MONO_2$ is still high, there will be a pulse at the output of gate G_1. When the input frequency exceeds the upper cutoff, $MONO_1$ stays triggered (its $\bar{Q}$ output remains low). When the input frequency is below the lower cutoff, $MONO_2$ times out (its Q output goes low). This prevents input pulses from passing through the output gate.

For the circuit in (b), $MONO_1$ sets the high-frequency cutoff, and $MONO_2$ sets the filter bandwidth. As in circuit (a), the input pulse reaches the output when $MONO_1$ has timed out and $MONO_2$ is high.

To obtain a constant output level when the input frequency is within the filter's passband, a retriggerable monostable that has its pulse length set for $1/f_{min}$ can be placed at the output. The monostable will remain triggered as long as there are output pulses from gate G_1. However, there will be a time lag in the filter's response of $1/f_{in}$ for pickup and $1/f_{min}$ for dropout.

For particularly critical applications or for high-speed operation, the input differentiator, made up of the passive RC network, should be replaced with a regular monostable, like a 74121-type or a 9603-type. □



Digital frequency selection. Bandpass digital filter built with two ICs is easily adjusted for lower and upper passband cutoffs. In (a), output pulse width of retriggerable monostable $MONO_1$ sets high-frequency cutoff, while $MONO_2$'s output pulse width sets low-frequency cutoff. In (b), $MONO_1$ determines upper cutoff frequency and $MONO_2$ determines bandwidth. The RC network differentiates all input waveforms.

Analog filter can be programed digitally

by Leonard M. Smithline
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The frequency response of an analog active filter can be selected digitally, yet with the resolution and accuracy of resistive tuning and the dc stability of capacitive tuning. The filter accepts TTL inputs, permitting it to be controlled directly by a computer and making it ideal for electronically switched systems. Furthermore, this digitally programable filter is cost-competitive with mechanically switched types of filters, especially for high-order filter functions.

A simple first-order low-pass filter is drawn in (a). The corner frequency of this circuit is determined by the proportion (α) of the amplifier output voltage (V) that is applied to the feedback capacitor (C). Since applying a voltage of magnitude αV to capacitor C produces the same feedback current as applying a voltage of magnitude V to capacitor αC, the value of capacitor C is effectively multiplied by α. Therefore, the filter's corner frequency can be written as:

$$\omega_b = 1/\alpha R_f C$$

where R_f is the feedback resistor. The over-all dc gain of the circuit is unaffected by loop gain α.

The effective multiplication of capacitance C by gain α can be used to control the filter's corner frequency, as shown in (b). In this circuit, the filter's corner frequency is determined by logic inputs through a voltage-divider setup. Resistor R_a is the upper leg of the divider, while the resistance of the lower leg is selected by enabling the appropriate TTL inverter buffer. When a logic input turns on one of the buffers, the resistor associated with that buffer is shorted to ground.

Resistor R_b provides the appropriate bias voltage for the buffers. The transistor, which is wired as an emitter-follower, reduces the resistance of the voltage divider that is reflected forward in series with capacitor C. This Thevinin equivalent resistance (R_T) is divided by the current gain (β) of the emitter-follower. For the circuit to operate properly:

$$R_T/\beta \text{ must be much less than } R_i \parallel R_f$$

where R_i is the input resistor. Since the dc levels of both the buffers and the transistor are blocked by the capacitor, there is no need for any bias stabilization circuitry.

If the effects of biasing resistor R_c are neglected, programable gain α can be expressed as:

$$\alpha = 1/[1 + (R_a/R_b) + \Sigma R_a G_i]$$

where G_i represents the conductance of those resistors, R_1 through R_n, whose buffers are enabled. The filter's corner frequency now becomes:

$$\omega_b = \omega_o(K + \Sigma R_a G_i)$$

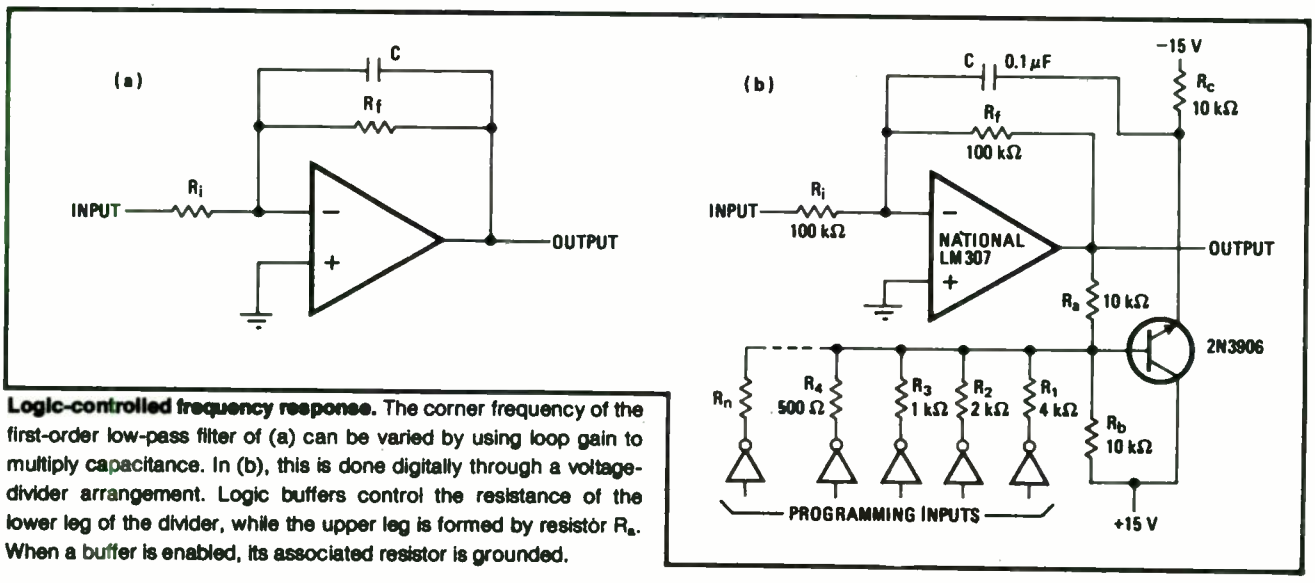
where:

$$\omega_o = 1/R_f C$$
$$K = 1 + (R_a/R_b)$$

The filter's starting frequency—that is, the corner frequency of the filter with none of the logic buffers enabled—is equal to $K\omega_o$. And each increment above this frequency, as each logic buffer is enabled, is equal to $\omega_o R_a G_i$. Since the effects of the enabled buffers are additive, the filter can be programed to accept either standard binary codes or a binary-coded-decimal input. For the component values cited in the figure, ω_o is 100 radians/second, K is 2, the starting frequency is 200 rad/s, and the frequency increment is 250 rad/s.

Moreover, the programing approach that is shown here can be extended to higher-order filters through the use of either the standard biquad or state-variable filter configurations.[1,2] □

REFERENCES
1. A.E. Schultz, "Active Filters Are Moving toward Standardization," Electronic Products, June 18, 1973.
2. G.E. Tobey, J.G. Graeme, L.P. Huelsman, "Operational Amplifiers—Design and Applications," McGraw-Hill Inc., 1971.



Logic-controlled frequency response. The corner frequency of the first-order low-pass filter of (a) can be varied by using loop gain to multiply capacitance. In (b), this is done digitally through a voltage-divider arrangement. Logic buffers control the resistance of the lower leg of the divider, while the upper leg is formed by resistor R_a. When a buffer is enabled, its associated resistor is grounded.

Narrowband digital filter achieves high Qs

by Thomas A. Visel
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A digital filter that is built with conventional logic ICs permits Qs of 2,000 to 10,000 to be readily achieved. Additionally, the filter's bandwidth is entirely independent of its operating frequency. And, as with other active filters, this circuit's upper frequency is primarily limited by the maximum bandwidth of the operational amplifiers used.

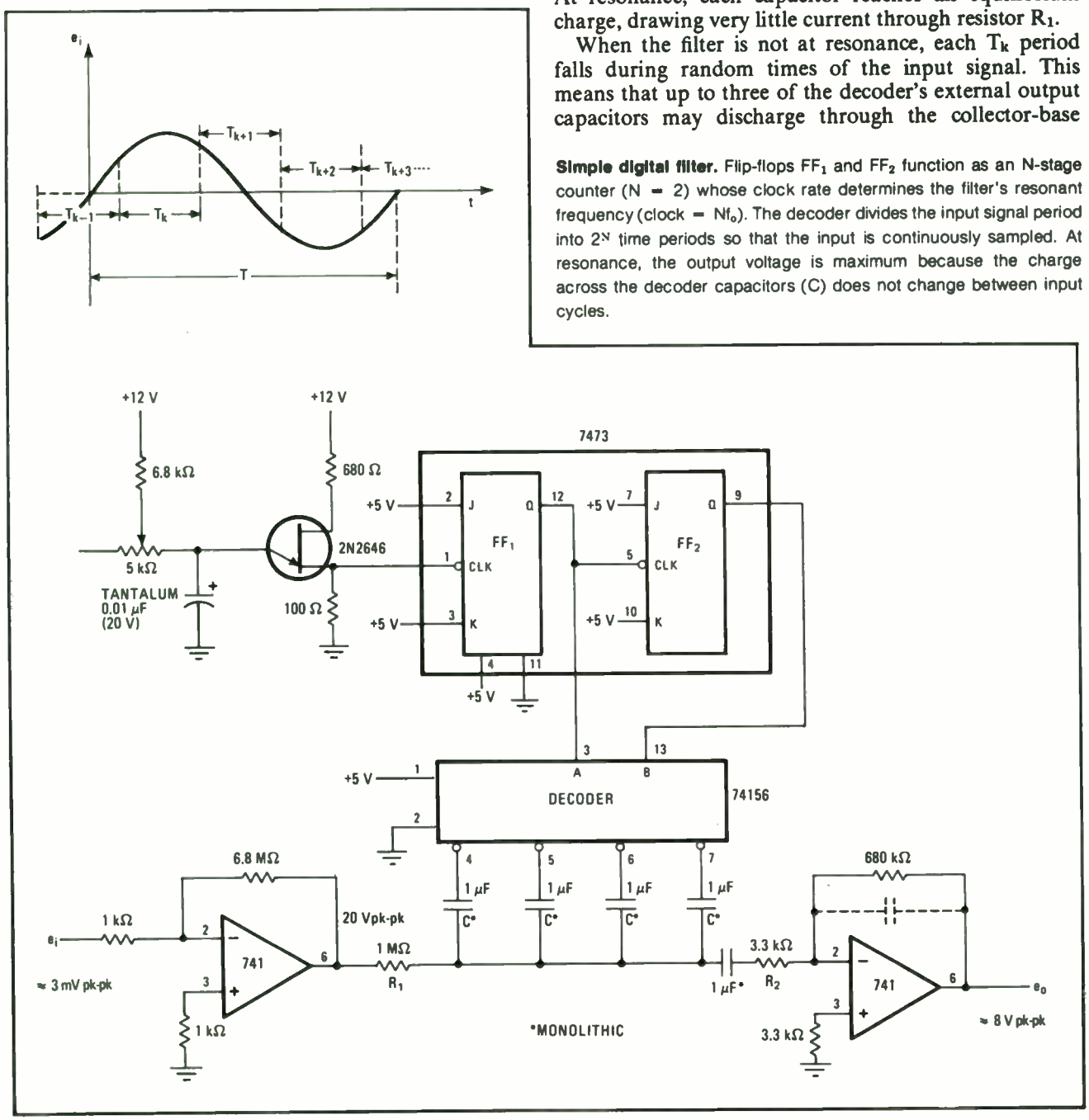
The operating frequency (f_o) is determined by the rate at which flip-flop FF_1 is clocked. Flip-flops FF_1 and FF_2 form an N-stage counter (N = 2 here), and the applied clock rate is Nf_o. The decoder functions as an N-line-to-2^N-line open-collector decoder, dividing the incoming signal into 2^N time periods at resonance. For the circuit shown, when f_o is 1 kilohertz, each of these periods (T_k) is 250 microseconds long.

At resonance, each of the four decoder outputs turns on successively for a quarter period of the incoming signal. This successively charges each of the decoder's output capacitors to:

$$V_C = \int_{T_k}^{T_{k+1}} \frac{Ae_i \exp(-t/R_1C)\,dt}{R_1C}$$

where A is the gain of the input operational amplifier. At resonance, each capacitor reaches an equilibrium charge, drawing very little current through resistor R_1.

When the filter is not at resonance, each T_k period falls during random times of the input signal. This means that up to three of the decoder's external output capacitors may discharge through the collector-base



Simple digital filter. Flip-flops FF_1 and FF_2 function as an N-stage counter (N = 2) whose clock rate determines the filter's resonant frequency (clock = Nf_o). The decoder divides the input signal period into 2^N time periods so that the input is continuously sampled. At resonance, the output voltage is maximum because the charge across the decoder capacitors (C) does not change between input cycles.

junctions of the decoder's internal output transistors, while the selected capacitor charges, or vice versa. A rather large net current will then be drawn through resistor R_1, diminishing the output voltage.

The output waveform, therefore, appears as a sampled version of the input signal. The more counter and decoder stages there are, the more exact will be the output waveform sample. A two-stage counter, like the one used here, is sufficient for such applications as synchronous tone detection in audio spectrum analyzers. Critical filtering applications will require additional stages.

For the components given, the filter's operating frequency is limited to 2.5 megahertz, and its 3-dB bandwidth is 12 hertz set at an f_o of 20 kHz. When resistor R_2 is a large value, the filter's bandwidth is:

$$BW = 1/(4\pi R_1 C)$$

For a 500-Hz step in frequency, the output response envelope is about 8 milliseconds from its 10% to 90% points. □

Tunable notch filter suppresses hum

by Peter Lefferson
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Close-tolerance components are not necessary in a hum filter if its rejection frequency can be adjusted to the frequency of the line-current hum. Such a filter is cheap and easy to build.

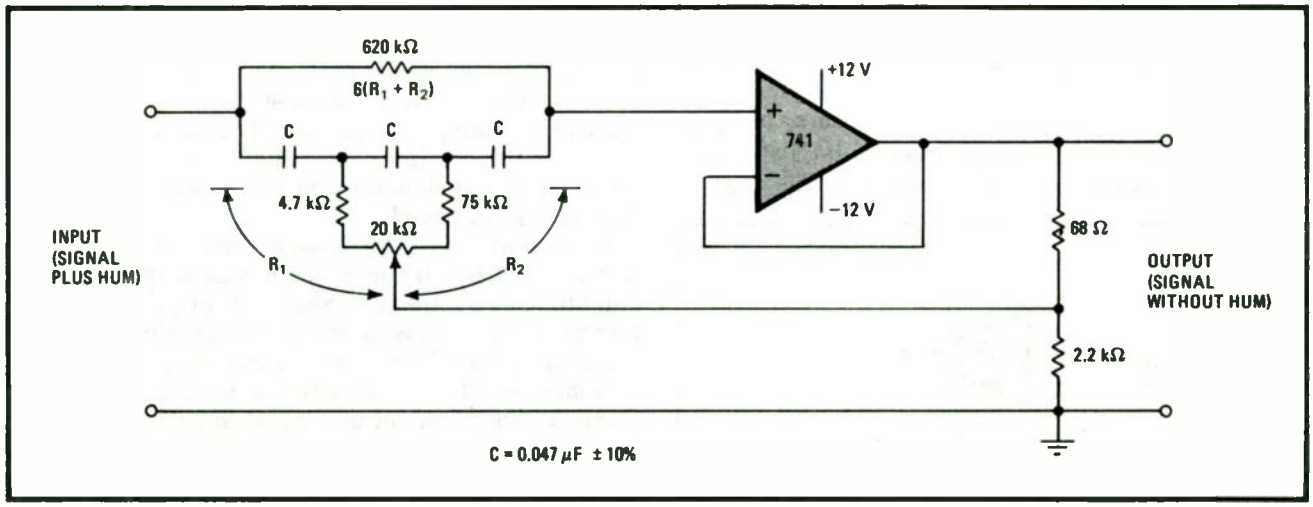
Notch filters are often designed into audio and instrumentation systems to eliminate unwanted signals or pickup such as 60-hertz line-frequency hum. For a given rejection frequency, close-tolerance components are usually required to guarantee repeatable design. An inexpensive, reproducible, narrow-stop-band circuit that can be built with wide-tolerance parts and can be tuned from 50 Hz to 60 Hz with 30-decibel minimum notch depth satisfies most hum-rejection requirements.

The illustrated circuit employs a bridge-differentiator RC network with active feedback. The notch frequency in hertz is given by:

$$f_o = 1/2\pi C(3R_1R_2)^{0.5}$$

where C is the farad value of the capacitors in the circuit; R_1 is the sum of the 4,700-ohm fixed resistor and the left-hand portion of the potentiometer, expressed in ohms, and R_2 is the sum of the right-hand portion of the pot and the fixed 75,000-ohm resistor. Although the operational amplifier can be of almost any sort, the 741 shown is typical. The notch bandwidth is set by the feedback gain of the noninverting amplifier, so replacing the 68-ohm resistor with a lower value narrows the rejection band.

With the given component values, this circuit can be tuned to reject the U. S. 60-Hz or the European 50-Hz power-line frequency. With 10%-tolerance capacitors, the minimum notch depth is 30 dB and the total 3-dB bandwidth is 14 Hz for 50 Hz and 18 Hz for 60-Hz center frequency. The insertion loss outside of the stopband is a negligible fraction of a decibel. □



Tuning a hum. This narrow-stop-band filter can be tuned by the pot to place the notch at any frequency from 45 to 90 Hz. It attenuates power-line hum or other unwanted signals by at least 30 dB. Because the circuit uses wide-tolerance parts, it is inexpensive to build.

Nonlinear low-pass filter rejects impulse signals

by Barrie Gilbert
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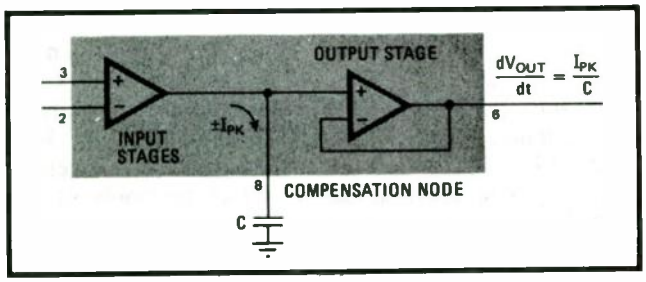
A circuit that rejects impulse signals but passes low-slew-rate signals without attenuation or phase shift can be made by connecting a capacitor to the compensation terminal of an operational amplifier. This nonlinear low-pass filtering is useful in the reduction of noise (particularly impulse noise) and in the control of glide rate between notes in electronic music equipment.

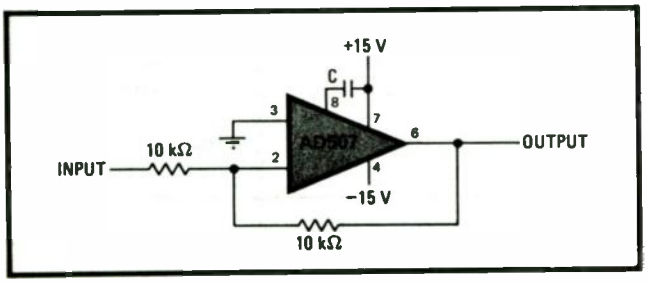
Figure 1 shows the basic configuration required of the op amp. It must have a compensation node into which it drives a stable current, I, during slewing. For optimum performance, this current should have the same magnitude in either slew direction. An external capacitor tied to the node then limits the slew rate to any value below the maximum specified for the particular op amp, because V_{out} is the voltage across the capacitor, and therefore

$$dV_{out}/dt = I/C$$

Not all op amps have the necessary configuration,



1. Nonlinear filter. An operational amplifier that has a compensation terminal with a well-controlled peak current, such as the AD504 or AD507, becomes a nonlinear low-pass filter when a capacitor is connected as shown. Because the slew rate of this circuit is limited, impulse signals and noise are strongly attenuated while low-slew-rate signals are passed without a change of amplitude or phase.



2. How to do it. The actual working circuit for the nonlinear low-pass filter shown here has the performance illustrated by wave forms in Fig. 3. Capacitor C has various values, depending on application.

and of those that do, only a few have a sufficiently well-controlled value for the peak current from the compensation node, I_{pk}. The AD507 is ideally suited to this application, having an I_{pk} that varies little from device to device or with temperature or supply-voltage variations. Its nominal value of ±200 microamperes, which may be either measured or calculated from the compensated slew rate, gives a slew-rate of 1 volt per microsecond for a C of 200 picofarads, and reliable accuracy up to slew-rates of 10 V/μs.

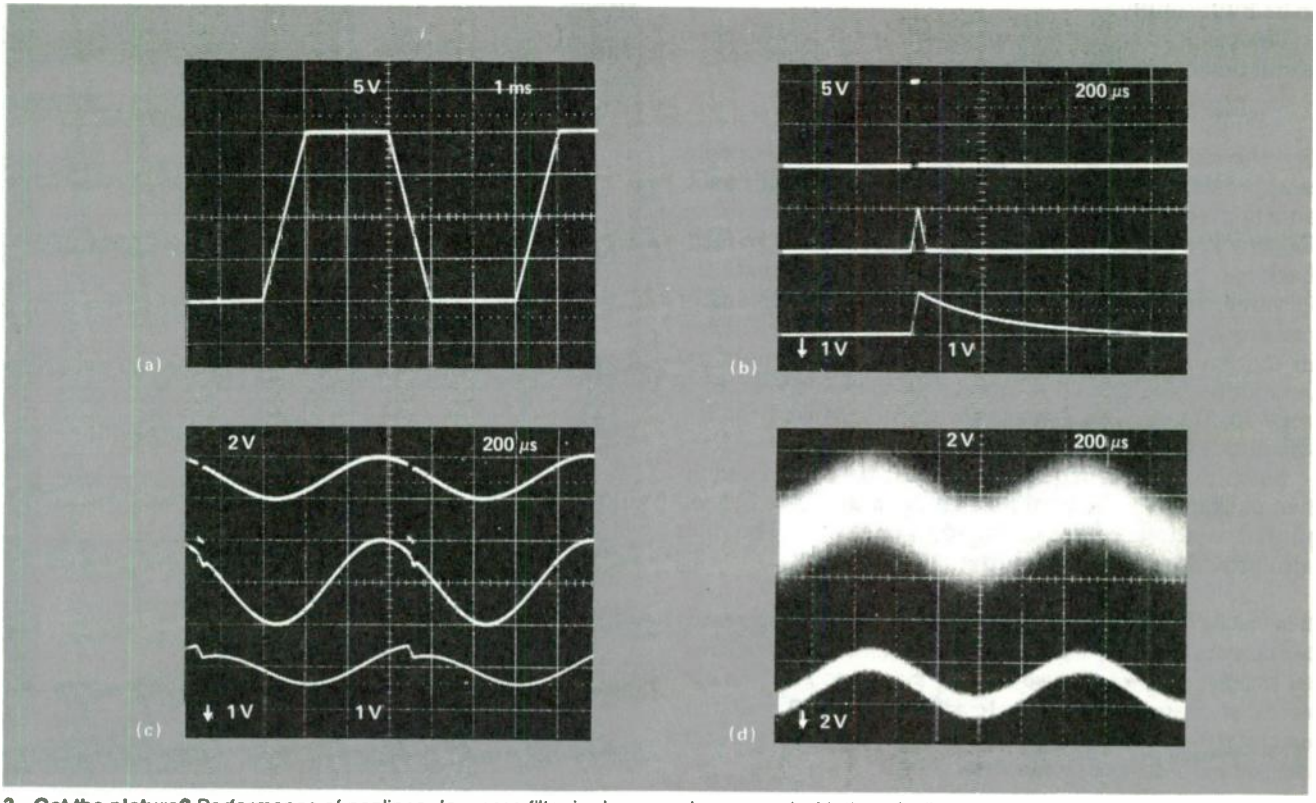
Figure 2 shows a unity-gain inverting amplifier using the AD507; with C = 0.01 microfarad the slew-rate is 0.02 V/μs. The response to a ±10-V square wave, shown in Fig. 3a, demonstrates this slew rate. Notice that C provides adequate loop stabilization, so the capacitor normally connected from pin 6 to pin 8 may be omitted. The small-signal response of this filter is determined by C, but is much higher than the full-power response; for the capacitor shown the figures are 20 kilohertz to −3 decibels (signal level of ±100 mV), and 320 hertz for ±10 V, respectively. Gains other than unity may be achieved simply by altering the ratio R_2/R_1, and the amplifier may be used equally well in the noninverting mode. The slew-rate is unaffected by the absolute value of the resistors, the gain, or the mode.

The usefulness of the filter can be judged by the other wave forms in Fig. 3. In Fig. 3b a 40-μs pulse of 10-V amplitude is shown in the top trace, and the output from the nonlinear filter with C = 0.008 μF is shown in the center trace, which for clarity has been inverted and expanded vertically. The nonlinear op-amp filter has reduced the pulse to a 1-V triangle lasting 80 μs. For comparison, the response of a single-pole linear filter having a time-constant of 400 μs is shown in the lower trace. Although the amplitude has been reduced to 1 V, a tail in the response extends beyond 1 millisecond.

The capacity to reject impulse signals while passing signals of low slew rate with neither attenuation nor phase error is shown more clearly by the wave forms in Fig. 3c. Here the input is a 1-kHz sine wave of 1-V amplitude, on top of which rides a 40-μs pulse of amplitude 3.5 V representing a noise spike. The center trace is the output of the nonlinear filter and shows that the pulse has been almost eliminated while the wave form of the sine wave is preserved.

In contrast, the linear low-pass filter (again a single 400-μs RC network) more than halves the sine-wave amplitude and introduces about 60° of phase lag. Furthermore, the pulse is stretched and actually distorts the wave form, as the lower trace demonstrates.

Nonlinear filters may also be used to reduce the Gaussian noise content of a signal, since it contains occasional high peaks (there is a 0.37% probability that the amplitude exceeds three times the rms value). Fig. 3d illustrates this. Again the input is a 1-kHz sine wave with an amplitude of 1 V, to which has been added 1 V rms of white noise. The output shows an undistorted



3. Get the picture? Performance of nonlinear low-pass filter is shown and compared with that of a linear low-pass (RC) filter. In (a) the input signal is a square wave; with C = 0.01 μF, the circuit slews the output at 20 V/ms. Both (b) and (c) show impulse inputs, response of nonlinear filter with C = 0.008 μF, and response of a linear low-pass (RC) filter. Noise reduction is demonstrated in (d).

sine wave, with only 0.3-v rms noise. Subjectively (if this were an audio signal) the improvement is slight, and more care is needed in selecting the optimum slew rate to effectively reduce white noise.

Unlike in linear filters, no change in response results from cascading stages of equal gain and slew rate. Also, if stages of different gain or slew rate are used, the one having the lowest slew rate is in the driver's seat. A high-pass nonlinear filter can easily be made by subtracting the low-pass signal from the direct input. In fact, the voltage at the summing node of the op amp in Fig. 2 is the high-pass function of the input.

Bandpass filters also can be constructed, by cascading a low-pass section with a high-pass section. When these have the same slew-rate the center frequency of the bandpass filter is inversely proportional to input amplitude. The practical value of the high-pass and bandpass nonlinear filters has not been established. □

State-variable filter uses only two op amps

by Charles Croskey
Pennsylvania State University, University Park, Pa.

One of the more useful circuits for an active filter design—the state-variable active filter—can be somewhat expensive to build because it normally requires three operational amplifiers. Two of these op amps function as integrators, while the third is used as an inverter, since a difference integrator has been rather difficult to make with a normal op amp.

The state-variable filter in the diagram, however, re-

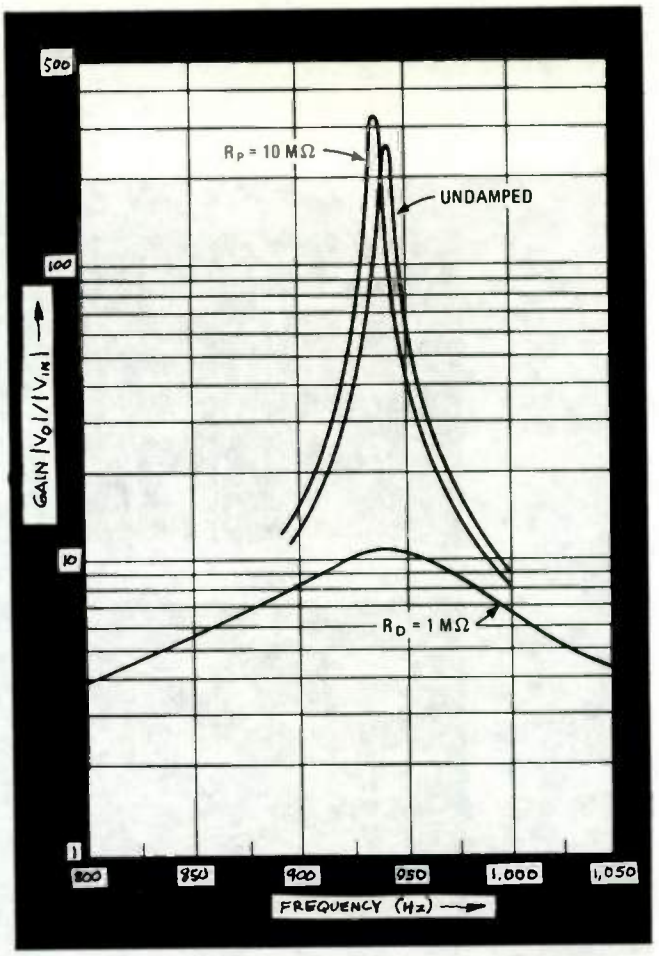
quires only two op amps. The circuit takes advantage of the recently introduced integrated quad amplifiers, such as Motorola's MC3401 and National's LM3900, which respond to a current difference instead of a voltage difference. Such amplifiers permit a difference integrator to be built simply.

The center frequency of the filter's bandpass function is still determined by the usual relationship of:

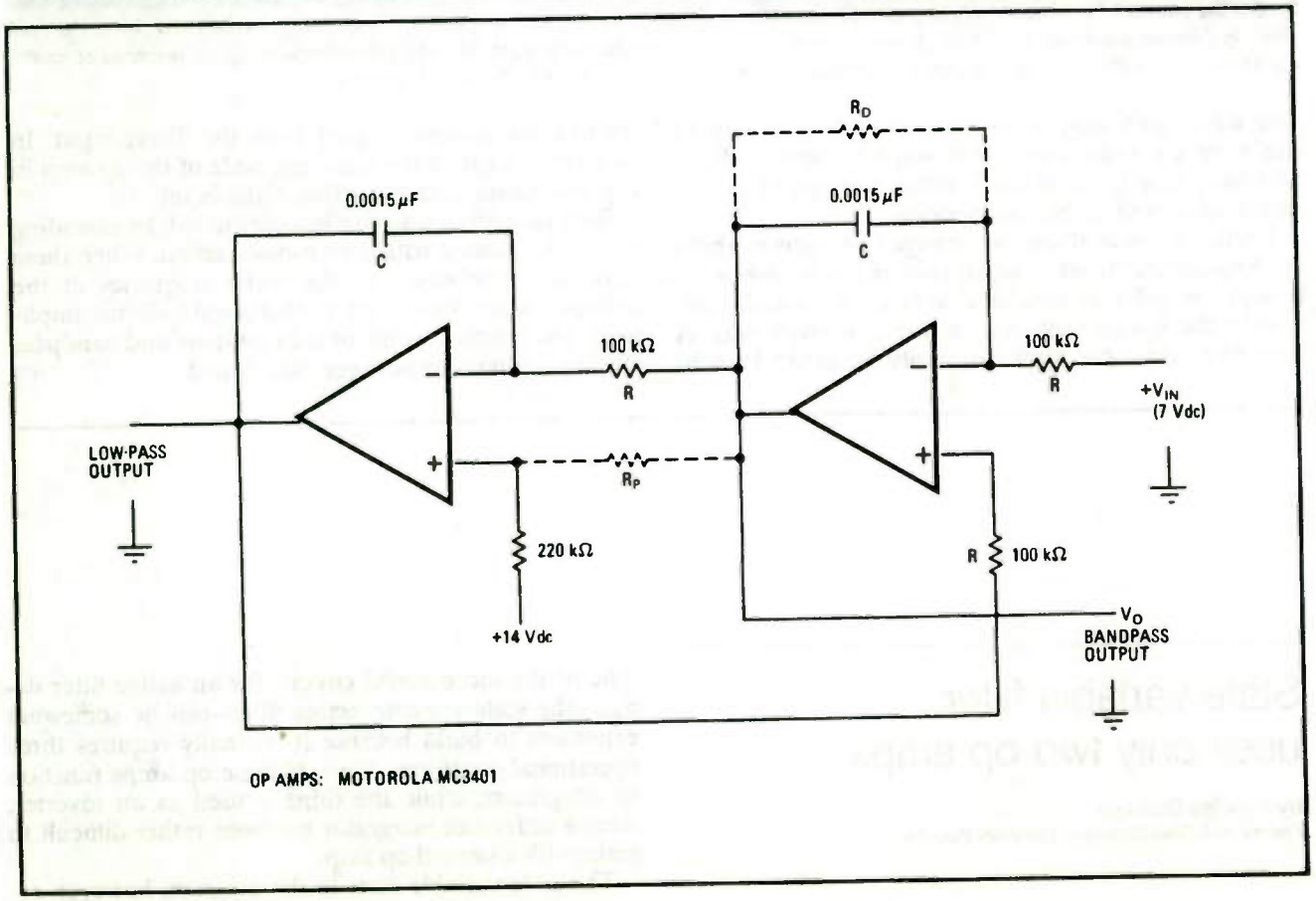
$$\omega_o = 1/RC$$

For the circuit values shown here, the center frequency is approximatley 940 hertz. The filter's damping factor, and therefore its Q value, can be adjusted by resistors R_D and R_P. To increase the Q value, some positive feedback can be added through resistor R_P; to decrease the Q value, resistive damping can be added by means of resistor R_D. As can be seen from the gain curves drawn in the figure, the Q value rises to 260 from a nominal (undamped) value of 248 when a 10-megohm resistor is used for R_P. Or if a 1-megohm resistor is used for R_D, the filter's Q value drops to 9.3.

Since the circuit requires only half of a quad amplifier package, the remaining two op amps can be employed as another filter or for additional gain. The filter also provides a low-pass output. □



Eliminating an op amp. This state-variable active filter employs only two op amps, instead of the three normally required. The usual inverter amplifier can be eliminated because the two op amps are connected as difference integrators. To adjust the filter's Q, resistor R_D or resistor R_P can be added to the circuit. The gain curves show both damped and undamped responses for the filter.



Three-mode network is filter or oscillator

by Michel Baril
University of Quebec, Montreal, Quebec, Canada

A triple-function circuit can be built with standard inexpensive components to operate as a bandpass filter, a notch filter, or a sine-wave oscillator. The operating mode is switch-selectable; the operating frequency range is 1 hertz to 20 kilohertz. Both of the filters can be separately adjusted for Q and center frequency.

The circuit (a) functions as a bandpass filter when switch S_1 is in the FLTR position, switch S_2 is open, and switch S_3 is closed. A notch filter is obtained by keeping S_1 in the FLTR position, closing S_2, and opening S_3. There are three possible oscillator outputs, one at each amplifier output; they are 180° out of phase with each other. For the oscillator mode, switch S_1 is in the OSC position, switch S_2 is open, and switch S_3 is closed.

The basic functional block of circuit (a) is the phase shifter shown in (b). The transfer function for this network is:

$$e_o/e_i = (1 - RCs)/(1 + RCs)$$

where s is the Laplace transform variable. Although there is no attenuation, the output lags the input by an angle that varies from 0 to π as frequency increases from zero to infinity. Cascading two of these blocks yields a phase-shifter whose angle is adjustable from 0 to 2π. Its transfer function is:

$$e_o/e_i = [(1 - RCs)/(1 + RCs)]^2$$

When a voltage divider made up of resistors R_1 and R_2 is placed across the two blocks, as shown in (c), the transfer function is modified to:

$$e_o/e_i = R_1/(R_1 + R_2) + [R_2/(R_1 + R_2)]\,[(1 - RCs)/(1 + RCs)]^2$$

If $R_1 = R_2$, output voltage e_o is a minimum (or equal to zero) when the phase lag is π.

When circuit (c) is used as the feedback element of an operational amplifier, the transfer function becomes that of a bandpass filter:

$$e_o/e_i = (R_1 + R_2)/[R_1 + R_2(1 - RCs)/(1 + RCs)]^2$$

The resulting circuit is the one shown in (a). Amplifiers A_2 and A_3 are the basic phase-shifters in the feedback loop of amplifier A_1. If amplifier A_3 is used as a buffer, the circuit becomes a notch filter.

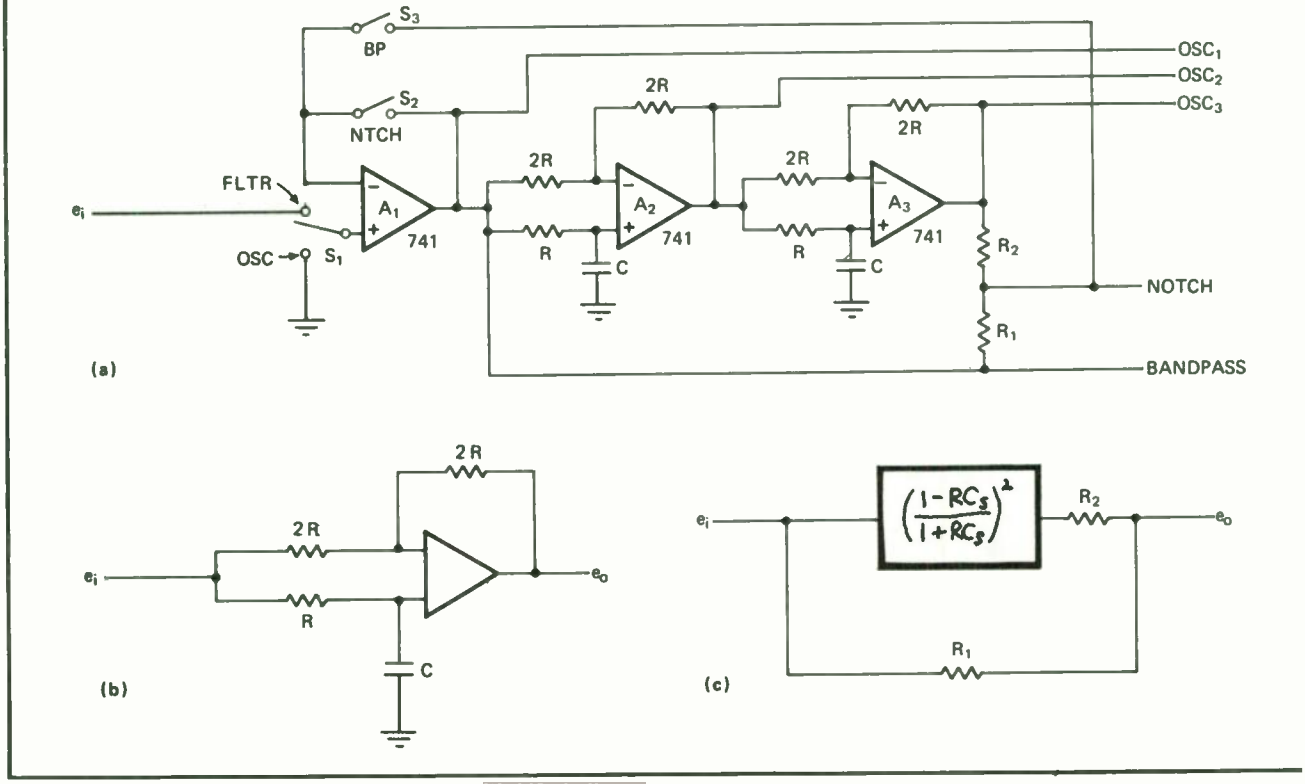
The Q factor of either the bandpass or the notch filter can be adjusted by changing the ratio of R_1:R_2 (theoretically, $Q = \infty$ when $R_1 = R_2$). Filter center frequency (f_o) can be varied by changing the values of resistor R and capacitor C:

$$f_o = 1/(2\pi RC)$$

For the circuit to work as an oscillator, the non-inverting input of amplifier A_1 must be grounded and resistor R_1 set equal to resistor R_2. Again, the operating frequency is set by varying the values of resistor R and capacitor C.

Circuit performance depends principally on the amplifiers, rather than the passive components. It is not

Choice of functions. Circuit (a) has three switch-selectable operating modes—it can be a bandpass filter, a notch filter, or a sine-wave oscillator. The three oscillator outputs differ in phase by 180°. Two of the phase shifters shown in (b) are cascaded and, along with the voltage divider formed by resistors R_1 and R_2, placed in the feedback loop (c) of a third operational amplifier.



necessary for resistor R or capacitor C to be precision components; resistors having tolerances of ±5% will do. And the resistor labeled 2R in the diagram can actually be much larger than 2 × R without impairing the performance of the circuit. However, to get very high filter Q or to use the circuit as an oscillator, voltage-divider resistors R_1 and R_2 must be precision parts, with tolerances as tight as ±1% or ±0.1%. □

19. Frequency dividers

TTL decade counter divides pulse train by any integer

by T. Durgavich and D. Abrams
Abrams Associates, Arlington, Mass.

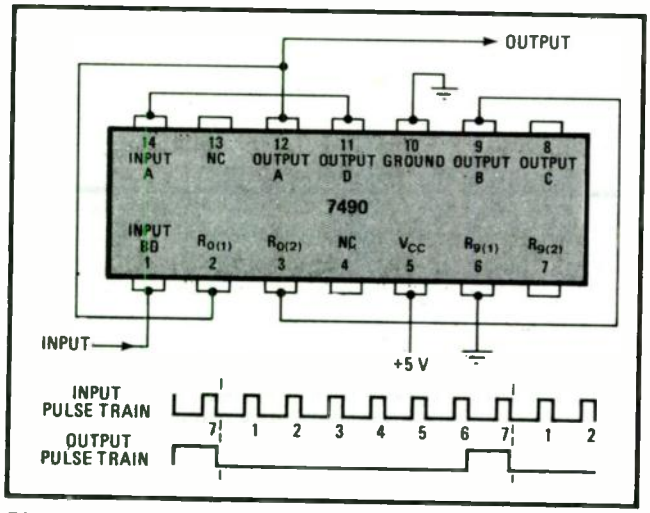
In many applications a pulse train must be divided by a fixed integer. For example, digital clocks often divide the line frequency by 60 to obtain a 1-hertz output, and time-base generators divide a crystal oscillator frequency down to several stable low-frequency outputs. If the integer is 10 or less, just one 7490 TTL decade-counter can handle the division.

Usually frequency division in TTL circuits is accomplished by using binary counters and logic gates. To divide by N—i.e., to get one output pulse for every N input pulses—the logic gates are connected so that the counter is reset when the N^{th} pulse is counted. The most significant bit is used as the output, because it makes the high-to-low clocking transition only once for every N input pulses. If it is necessary to have an output pulse of a specific length, then a monostable may be triggered when the N^{th} pulse is detected.

The disadvantage of this division technique is that, even for divisors less than 10, two ICs are required—a binary counter and a gate. But a pulse train can be divided by any integer between 2 and 10 by use of just one 7490 TTL decade-counter IC, owing partly to its divide-by-2 and divide-by-5 stages and partly to its internal ANDed reset, which lets it reset only when both pin 2 and pin 3 are high.

The counter can be made to reset on any count from 2 to 10 by appropriate connections of the pins. The necessary interconnections for each value of N are shown in the table.

For example, if division by 7 is desired, the 7490 is wired as shown in the figure. The input and output pulse trains for this configuration are also shown. If a larger division is required, it's only necessary to cascade several stages together, provided the divisor has factors that are all less than 10. □



Divide-by-7 circuit. A 7490 TTL decade-counter integrated circuit, when connected as shown here, produces one output pulse for every seven input pulses. Because the divide-by-2 stage follows the divide-by-5 stage, the seventh count is a non-BCD code and can be detected by the internal two-input NAND gate to reset the counter. Other connections permit division by any other integer up to 10.

OPERATION OF 7490 IC AS A DIVIDE-BY-N COUNTER

DIVISOR N	INPUT PIN NO.	OUTPUT PIN NO.	EXTERNAL CONNECTIONS
2	14	12	PIN 2 OR 3 LOW
3	1	8	PIN 8 TO PIN 2 PIN 9 TO PIN 3
4	1	8	PIN 11 TO PINS 2 AND 3
5	1	11	PIN 2 OR 3 LOW
6	14	8	PIN 12 TO PIN 1 PIN 9 TO PIN 2 PIN 8 TO PIN 3
7	1	12	PIN 11 TO PIN 14 PIN 12 TO PIN 2 PIN 9 TO PIN 3
8	14	8	PIN 12 TO PIN 1 PIN 11 TO PINS 2 AND 3
9	14	11	PIN 12 TO PINS 1 AND 2 PIN 11 TO PIN 3
10	14	11	PIN 12 TO PIN 1 PIN 2 OR 3 LOW

Control one-shot divides frequency by up to 30

by Jerome Snaper
Leach Corp., Controls Div., Azusa, Calif.

A three-gate control allows precision frequency divisions of up to 30 merely by changing a resistance. A crystal oscillator acts as the frequency source so that all subharmonics of the reference frequency have crystal stability.

NAND gates G_1 and G_2 and the crystal comprise the oscillator that generates the reference frequency. The one-shot, consisting of NAND gates G_3 and G_4, controls gate G_5, which is synchronized by the oscillator.

After one pulse of the reference frequency passes to the output, the one-shot locks out gate G_5 for a period of time determined by the setting of potentiometer R_t. When the one-shot resets, another single pulse reaches the output, and the cycle repeats.

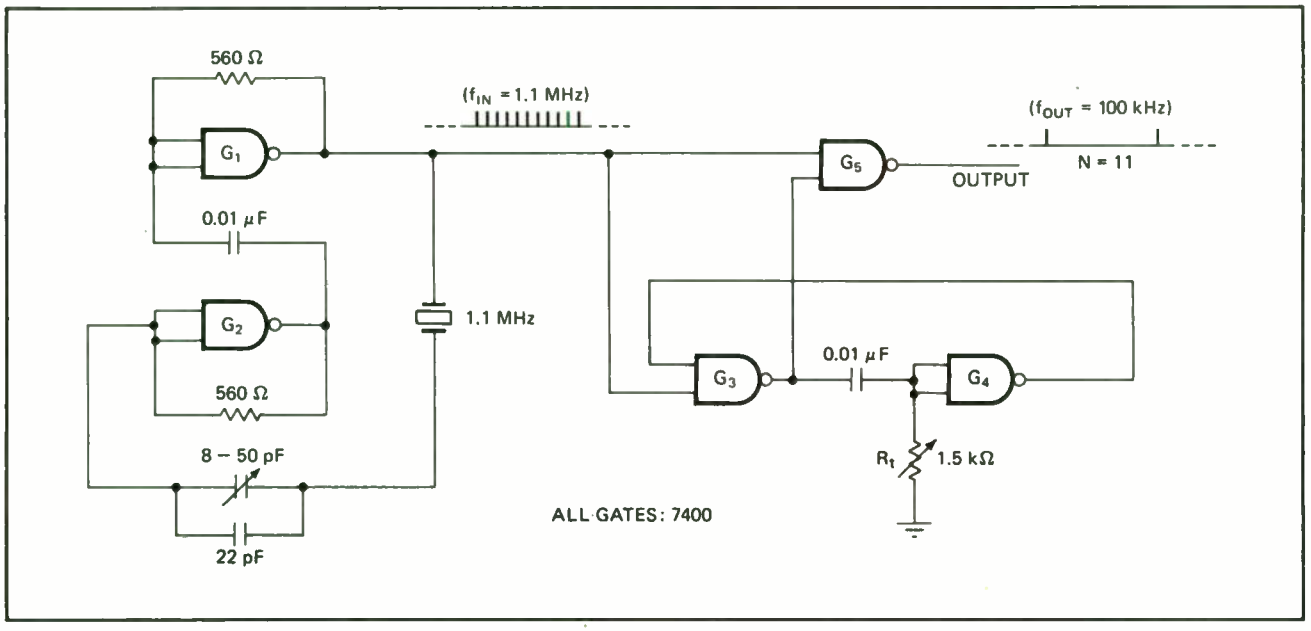
The input frequency, f_{in}, is simply a multiple of the output frequency, f_{out}:

$$f_{in} = Nf_{out}$$

where N is the division factor. N can have any integral value between 2 and 30. The circuit shown divides a 1.1-megahertz reference frequency by 11 to yield an output frequency of 100 kilohertz.

Additional versatility is possible by substituting a field-effect transistor or voltage-variable resistor for the potentiometer. Then, frequency divisions can be electronically swept over a wide range. □

Precision division. Crystal oscillator supplies reference frequency for three-gate divider scheme. NAND gates G_3 and G_4 form one-shot that controls gate G_5. After G_5 passes single reference pulse, one-shot inhibits this gate for period selected by adjustment of potentiometer R_t. When one-shot resets, another reference pulse passes to output. Crystal frequency can be divided by up to 30 without loss of stability.



Binary division produces harmonic frequencies

by Donald DeKold
Santa Fe Junior College, Gainesville, Fla.

Harmonically related frequencies—more specifically, a fundamental frequency and its first nine overtones—can be generated with binary division of a blanked pulse train. The harmonic frequency generator, which consists of a clock pulse generator, a decade counter, and a few NOR gates and flip-flops, produces square-wave outputs at frequencies f_o through $10f_o$.

The clock frequency must be 2^n times faster than the frequency of the highest harmonic of interest (n is the number of flip-flops used for the binary division). Therefore, to produce the highest harmonic, $10f_o$ in this case, the clock output is simply divided down by 2^n. For all harmonics but the fifth, however, the clock signal must be properly gated before it can be divided.

To understand why this is so, consider what happens

with the ninth harmonic. The uppermost NOR gate passes and inverts the first nine clock pulses to reach it. But the arrival of the tenth pulse coincides with the arrival of a high from the decade counter. Since the counter's output stays high for the full duration of the tenth clock pulse, the gate's output remains low, preventing the tenth pulse from propagating. This tenth-pulse rejection occurs every $2^n f_o$ times per second.

Clearly, the gate's output pulse frequency is nine-tenths that of the clock frequency, because one pulse is blanked for every ten delivered. The gate's output waveform may be regarded as the 2^nth overtone of $9f_o$, but one that is badly distorted with respect to phase. The nine pulses making up a full period of this waveform are cumulatively advanced in time from their proper locations as they progress through one complete period of the binaryfflovertone of thefflfundamental.

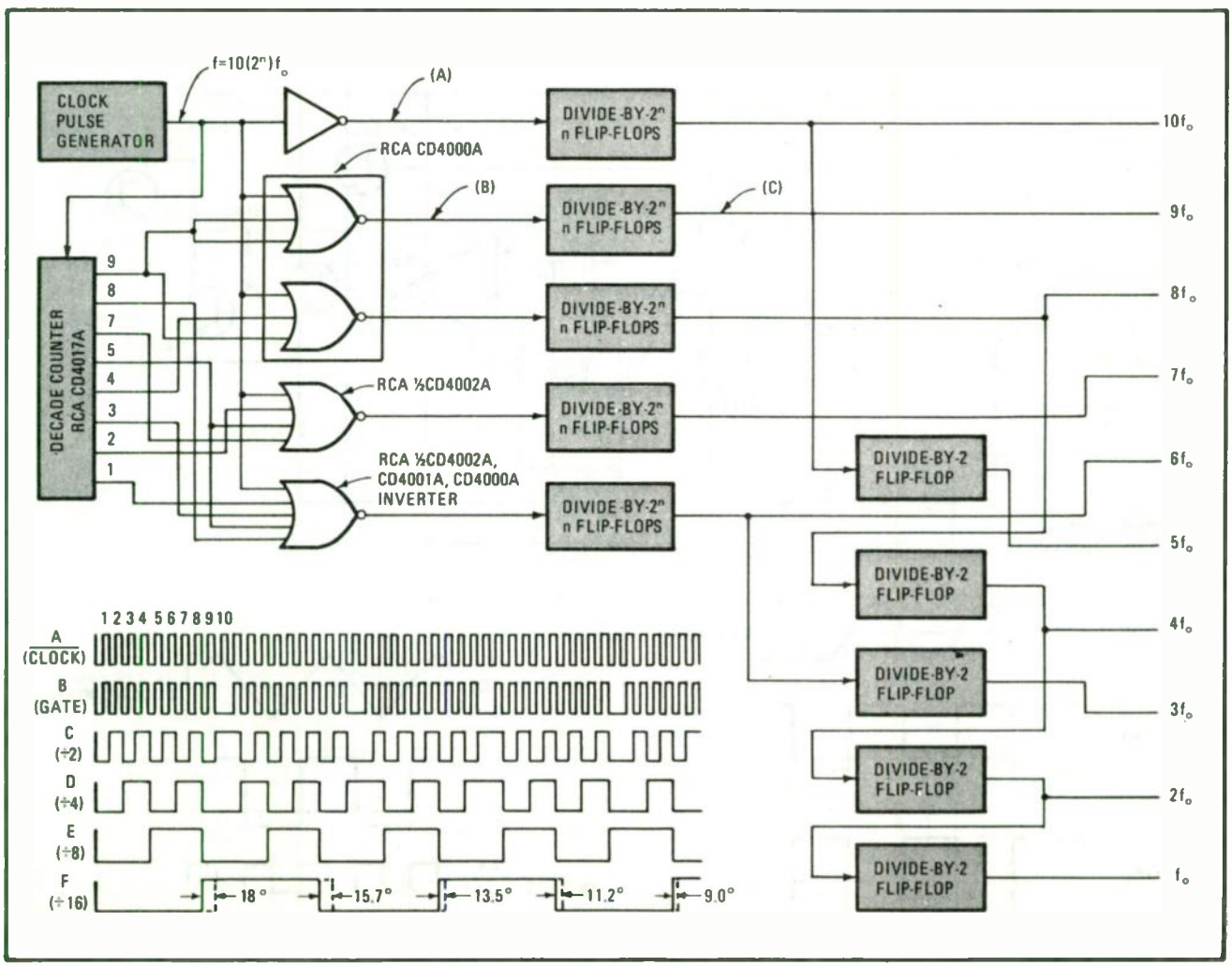
This phase distortion can be almost eliminated by successively dividing the gate output by two with flip-flops, as shown in the timing diagram. Waveforms A through F illustrate how the blanked space can be made smaller by flip-flop divisions of 2, 4, 8, and 16. Although only 2½ cycles of divided-by-16 waveform F are shown, the reduction of phase distortion is still evident.

The proper locations of this waveform's transitions—those that a true square wave of frequency $9(2^{n-4})f_o$ would produce if divided in the same way—are denoted by the colored dashed lines. The leftmost switching edge, which exhibits the largest error, is advanced by 18° from the true edge. At any stage of division, the maximum uncertainty in a transition will always be less than the period of the clock frequency.

Harmonic frequencies $6f_o$, $7f_o$, and $8f_o$ are developed in much the same way as $9f_o$. Two clock pulses must be blanked for $8f_o$, three for $7f_o$, and four for $6f_o$. To generate harmonics $5f_o$, $4f_o$, $3f_o$, $2f_o$, and f_o, binary divisions of harmonics $10f_o$, $8f_o$, and $6f_o$ are performed as indicated.

Complementary-MOS integrated circuits can be used to build this harmonic generator. If RCA's type CD4017A decade counter is chosen, the maximum clock frequency is limited to 5 megahertz. (An unused dual-input NOR gate in RCA's type CD4001A package can be employed as the clock inverter.) □

Harmonic generator. Single clock signal can be used to create fundamental frequency f_o and its first nine harmonics. Clock frequency can be divided directly for tenth and fifth harmonics, but other harmonics must be gated to produce appropriately blanked pulse train. (For instance, one clock pulse out of ten is blanked by top NOR gate for harmonic $9f_o$.) Flip-flops then divide gated outputs.



20. Frequency doublers

Frequency doubler accepts any waveshape

by Donald DeKold
Santa Fe Junior College, Gainesville, Fla.

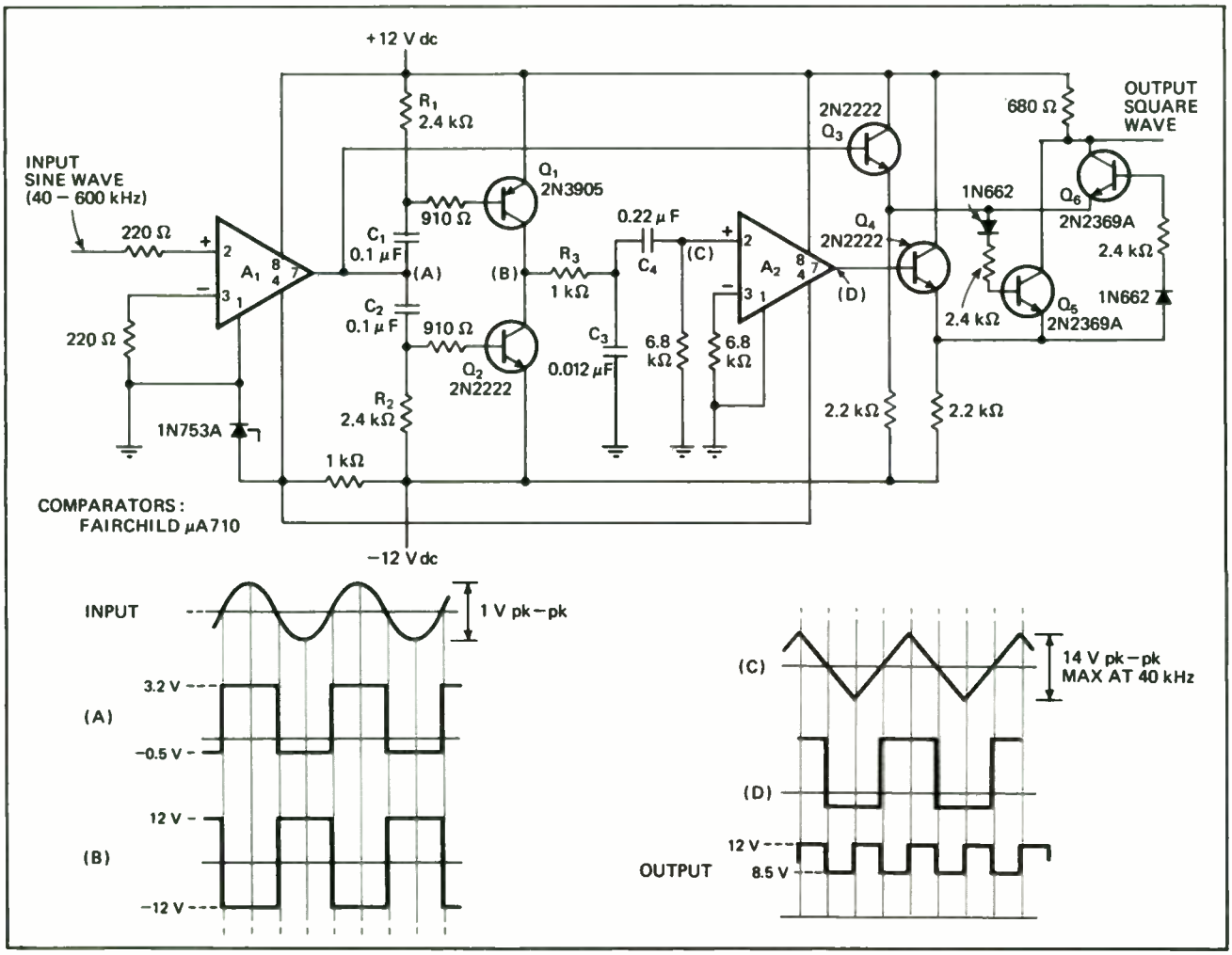
The frequency of nearly any waveform can be doubled by means of quadrature square waves that drive a biconditional logic circuit. Only two restrictions must be imposed on the input to this frequency doubler—the wave form must have a duty cycle of approximately 50% and a peak-to-peak amplitude of at least 0.5 volt.

For the circuit shown, the input is a sine wave that can vary in frequency from 40 to 600 kilohertz. The output is a square wave at twice the input frequency, having a duty cycle of about 38% for the lower-frequency inputs to around 65% for the higher-frequency inputs.

Comparator A_1 operates in its noninverting mode, accepting the input sine wave and producing a square wave at its output. Capacitors C_1 and C_2 couple this square wave to a pair of complementary switches, transistors Q_1 and Q_2. The switches boost the amplitude of the square wave to 24-v pk-pk. Resistors R_1 and R_2 prevent the bases of Q_1 and Q_2 from being clamped to dc voltages that would drive them into cutoff.

Capacitor C_3 is alternately charged and discharged through resistor R_3. When Q_1 is in saturation and Q_2 in cutoff, C_3 exponentially charges towards 12 v dc; with Q_1 cut off and Q_2 saturated, C_3 discharges towards

Frequency times two. Sine-wave input is converted into square wave by comparator A_1. Emitter-followers Q_1 and Q_2 charge and discharge capacitor C_3, producing triangular wave that drives comparator A_2. Resulting square-wave output of A_2 is in quadrature with square-wave output of A_1. Switches Q_5 and Q_6 conduct only when comparator states are different, providing square wave that is twice input frequency.



−12 v dc. When the charging or discharging interval is short compared to the R_3C_3 time constant, the voltage across capacitor C_3 approximates a triangular wave that has its peak value occurring 90° out of phase with the peak amplitude of the input sine wave.

The triangular wave is applied to the noninverting input of comparator A_2 through capacitor C_4. The comparator "squares" the triangular wave about its zero crossings, producing a square wave that is 90° out of phase with the output of the first comparator.

Transistors Q_3 and Q_4 are emitter-followers that act as buffer amplifiers for both comparators and drive a set of nonsaturating switches, transistors Q_5 and Q_6. When comparator states are the same, Q_5 and Q_6 are off; when comparator states differ, Q_5 or Q_6 conducts.

The switching action of transistors Q_5 and Q_6 is equivalent to the biconditional logic function:

$$XY + \overline{X}\,\overline{Y} = 1$$

which has the effect of doubling the frequency of quadrature square waves. A diode and resistor in each transistor's base-emitter loop prevent false switching when both comparators are in the same state, but may have different output levels.

A square wave with a 50% duty cycle can be realized for a nominal input frequency of 120 kHz. At lower frequencies, the duty cycle is smaller because the triangular wave becomes exponentially rounded. At higher frequencies, the duty cycle is larger, since the amplitude of the triangular wave decreases, thereby shortening the duty cycle of the square wave at the output of the second comparator. Also, circuit delays become significant compared to the period of high-frequency inputs.

The frequency doubler can operate below 40 kHz if higher capacitor values are used throughout the circuit. To operate at higher frequencies, faster switching devices must be used, and transistors Q_1 and Q_2 must not be allowed to saturate.

Since the maximum input voltage for the type μA710 comparator is ±7 v, the amplitude of the triangular wave must not exceed 14 v pk-pk. □

Pulse-frequency doubler requires no adjustment

by Thomas McGahee
Don Bosco Technical High School, Boston, Mass.

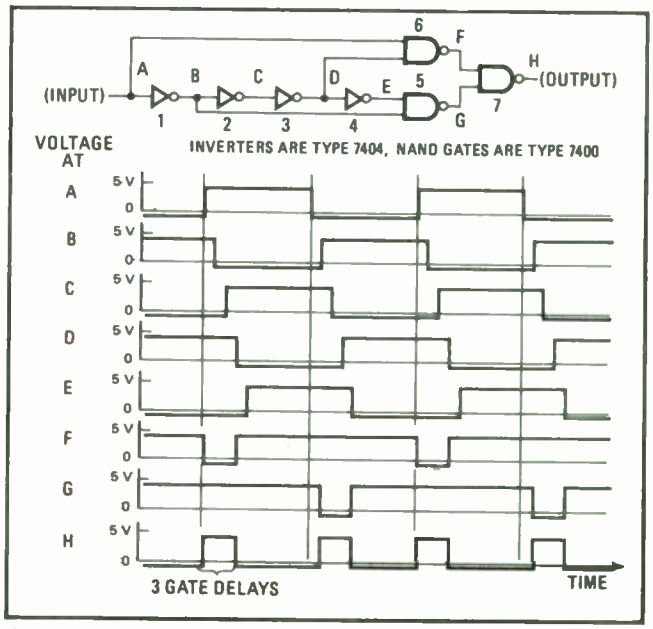
Sometimes a frequency doubler is needed in a digital system, and unfortunately most doubler circuits have to be adjusted for a particular operating frequency. However, this circuit, which has operated successfully in a specially designed divide-by-N counter, requires no adjustment over a range from near dc to 10 megahertz.

When a signal pulse passes through the circuit, each inverter introduces a small delay, typically of 20 nanoseconds, in addition to inverting the pulse. For example, the signal at point D inverts 60 ns after the input signal at point A has inverted; thus, gate 6 continues to have high signals at both of its input terminals for 60 ns after the input at point A changes from low to high. As a result, the output from gate 6 (i.e., point F) will go low for 60 ns after a positive-going transition at the input to the circuit.

Somewhat the same thing occurs at gate 5, except that it develops a 60-ns low output after a negative-going transition at the input. In the circuit diagram, inverters 1, 2, and 3 all serve double duty in producing these 60-ns low pulses at points F and G. This design reduces the number of gates needed.

The pulses from gates 5 and 6 are fed to the terminals of gate 7, which produces a positive pulse 60 ns wide every time either one of its input terminals goes low. Since one terminal goes low on the leading edge of each input pulse at point A, and the other terminal goes low on the trailing edge of each input pulse at A, the frequency of the output pulses at point H is twice the frequency of the input pulses at point A.

The output is in the form of positive pulses that are 60 ns wide. There is a 20-ns difference in the spacing between successive output pulses because the portion of the circuit that comprises the negative-going edge-detector has one more inverter stage than the positive-going edge-detector section does. This slight asymmetry is noticeable only at the highest frequencies. If particularly slow input signals are used, it is a good idea to place a Schmitt trigger just before the input. □



Frequency doubler. Propagation delays through inverters cause NAND gates 5 and 6 to go low for 60 nanoseconds following the rising and falling edges, respectively, of input pulse. Therefore output goes high twice as often as input.

Switched frequency doubler provides multiple outputs

by Michael F. Black
Texas Instruments, Systems Analysis Section, Dallas, Texas

Frequency doublers that operate in the vhf/uhf range typically consist of complicated arrangements of saturated amplifiers, tuned circuits, and harmonic-suppression traps. With these circuits, a constant input impedance is usually difficult to sustain with changing temperature. Also, if the doubler must be switched, it is difficult to maintain circuit simplicity and high isolation ratios.

The switched frequency doubler shown here, however, provides high harmonic rejection, as well as constant input impedance, and it requires a minimum of adjustment. The circuit, which consists of a double-balanced mixer followed by a linear amplifier, accepts a 50-megahertz input of 5 dBm. In addition, it has provision for fast on/off switching and multiple 100-MHz outputs to 50-ohm loads.

The input power is split by the two-way power divider, HY1, and applied to the RF and LO ports of the mixer, M1. The mixer output, of course, is made up of several frequencies: twice the input frequency, the input frequency itself, the difference frequency (between the input and the local oscillator), and harmonics.

The difference frequency, which is dc, is shorted by the rf choke (L_1), and the input-frequency component is attenuated by the LO/i-f and rf/i-f isolation of the mixer. Transistor Q_1 is tuned to the doubled frequency, and the high-Q circuit in its collector loop further attenuates the unwanted frequencies to about 50-dB down. Through inductor L_2, the matching structure of this collector loop provides the only circuit adjustment.

Only three 50-ohm outputs are shown here, but more can be added. For each output, two capacitors (C_1 and C_2) transform the 50-ohm load up to a resistance value that output transistor Q_1 can drive satisfactorily. The reactance of inductor L_2 then tunes out the capacitance to present a high-value real load to Q_1's collector at the doubled frequency.

The value of L_2's reactance is:

$$X_{L2} = (\tfrac{1}{3})(R_P/Q)$$

where R_P is the load resistance that transistor Q_1 sees, and Q is the circuit's figure of merit. The reactances of the transformation capacitors, C_1 and C_2, are also dependent on R_P and Q. They can be expressed as:

$$X_{C1} = [R_P/(1+Q_2)][Q - [(50/R_P)(1+Q^2) - 1]^{1/2}]$$
$$X_{C2} = 50/[(50/R_P)(1+Q^2) - 1]^{1/2}$$

Circuit Q is selected according to the harmonic rejection required. The higher the value of Q is, the higher the harmonic rejection will be, but the more difficult some component values may become to obtain. For the circuit given here:

$$Q = 6$$
$$R_P = 1.5 \text{ kilohms}$$
$$X_{L2} = 83 \text{ ohms at } 100 \text{ MHz} = 0.13 \text{ microhenry}$$
$$X_{C1} = 222 \text{ ohms at } 100 \text{ MHz} = 6 \text{ picofarads}$$

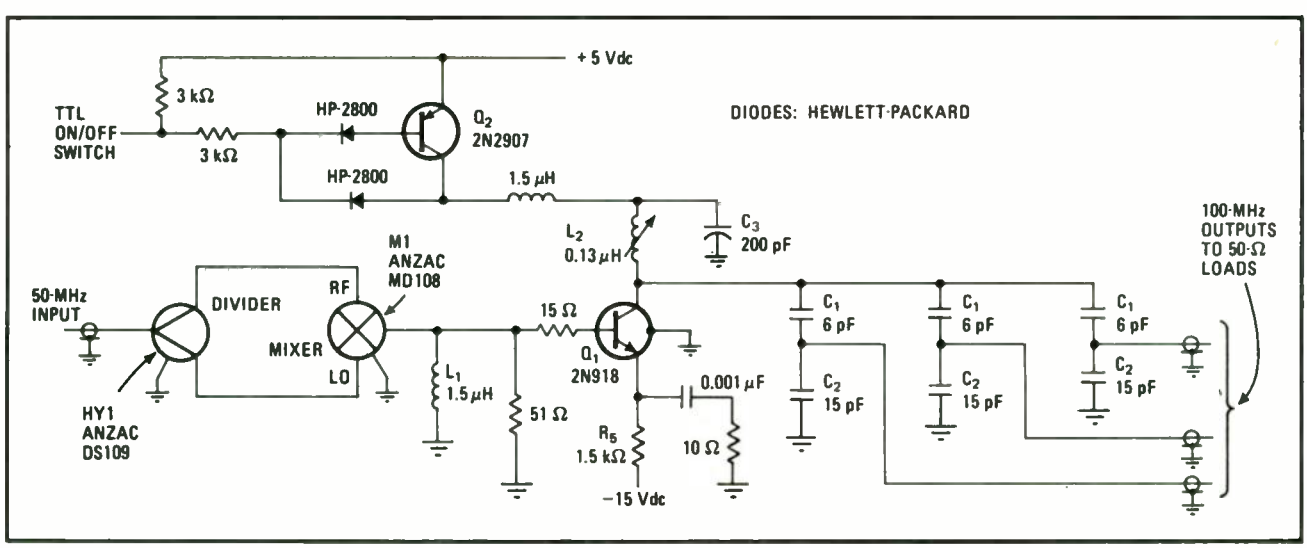
and:

$$X_{C2} = 104 \text{ ohms at } 100 \text{ MHz} = 15 \text{ pF}$$

Each output of the circuit supplies a power level of +3 dBm at a frequency of 100 MHz.

Transistor Q_2 is a nonsaturating switch that is compatible with a TTL open-collector input. Together with its associated circuitry, transistor Q_2 switches transistor Q_1, providing the mutiple gated outputs. Switching times of well under 1 microsecond can be realized when an appropriate value is chosen for capacitor C_3. The circuit's on/off isolation is better than 50 dB. □

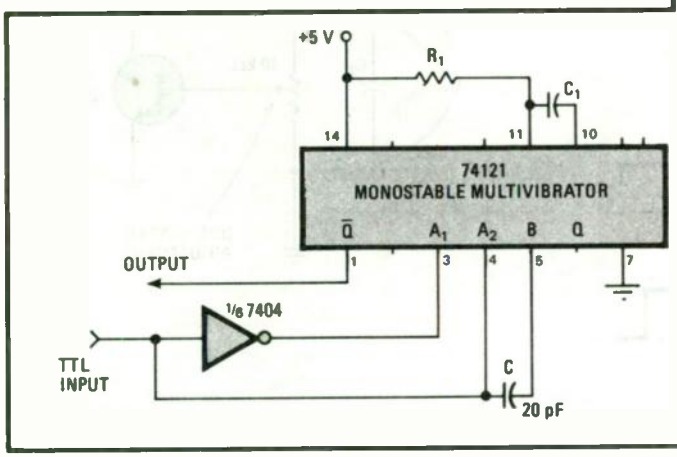
Rf frequency doubler. From a 5-dBm input at 50 megahertz, this switched frequency doubler develops multiple 3-dBm outputs at 100 MHz, seen by output transistor Q_1 so that the circuit can handle 50-ohm loads with relative ease. The doubler's only adjustment, inductor L_2, is used to tune out this added capacitance. Transistor Q_2 is used to switch transistor Q_1.

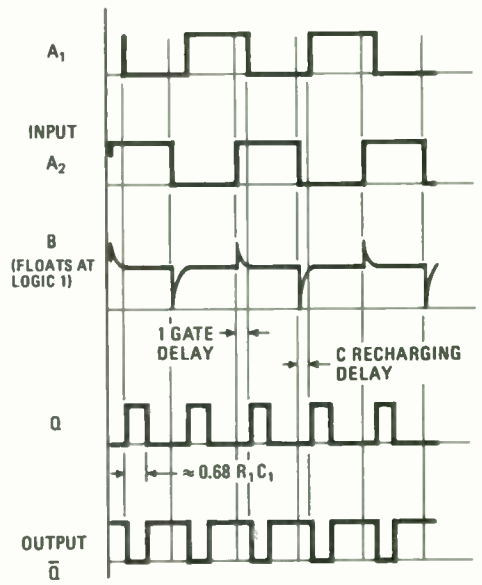


Frequency-doubler produces square-wave output

by Robert L. Taylor
I&F Electronics, Nashville Tenn.

Most digital frequency-doublers use edge-detection techniques to produce two narrow output pulses per input pulse. Although these types of doublers work well, they have the disadvantage of producing highly asymmetrical outputs and usually cannot be cascaded to obtain higher multiplication factors. These problems can be eliminated by use of a monostable frequency-doubler with a modified version of H.P.D. Lanyon's feedback system [see "One-shot with feedback loop maintains constant duty cycle," *Electronics*, July 24, 1975, p. 93].

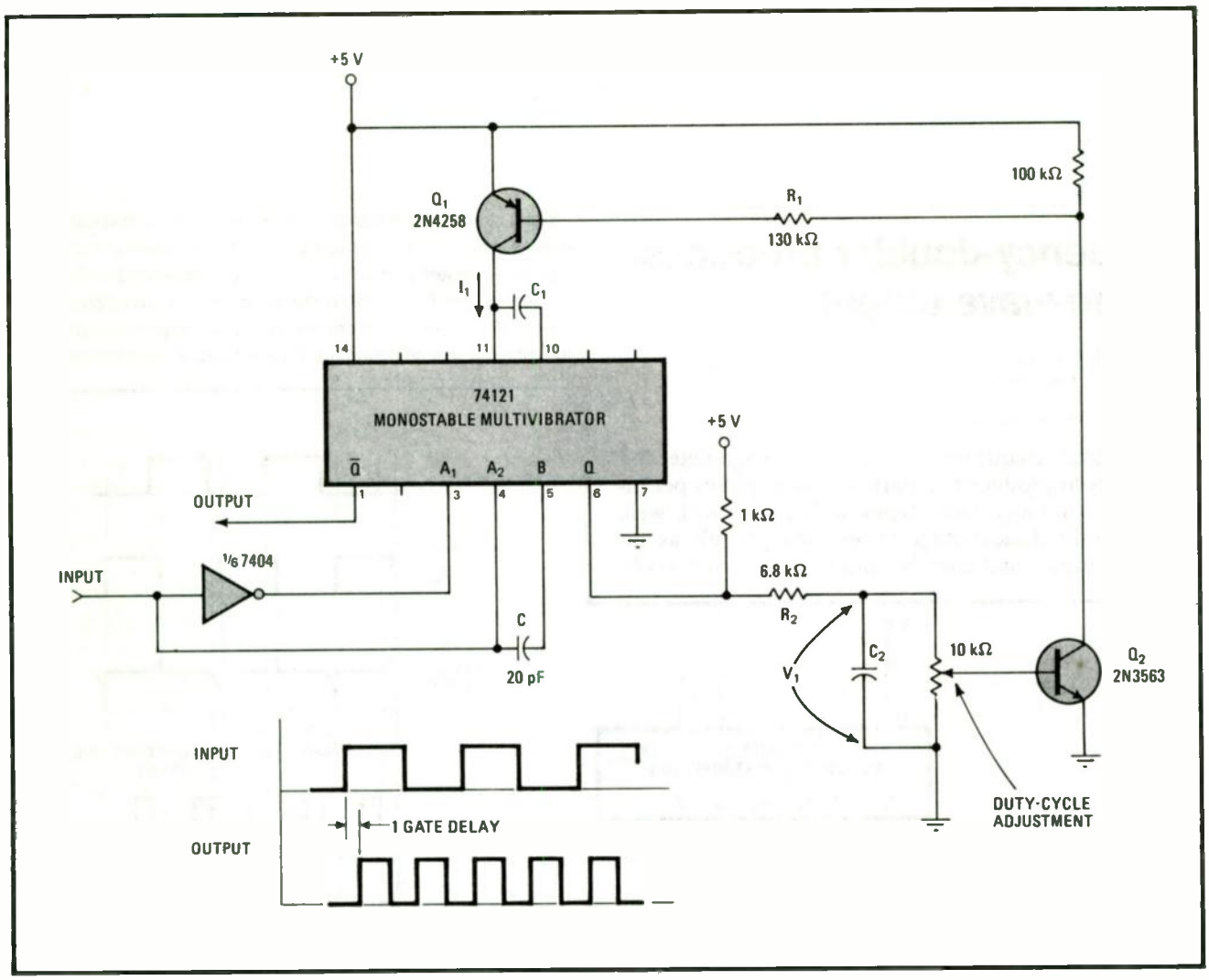




1. Basic frequency-doubler. The monostable multivibrator produces two output pulses for each cycle of input waveform. One output pulse is triggered on falling edge of A_1, and second output pulse is triggered when B goes high after spiking low. If output pulse width is set for 50% duty cycle at one frequency, it is asymmetrical at other frequencies. The time delays are shown disproportionately large.

The basic doubler circuit and its timing diagram are illustrated in Fig. 1. The propagation delay introduced by the inverter allows the 74121 monostable multivibrator to trigger on the rising edge of the input wave, and the 20-picofarad capacitor triggers on the falling edge. Since both edges of the input are detected, the output frequency is twice the input frequency. By selecting the proper R_1C_1 value, a 50% duty cycle could be obtained with the circuit of Fig. 1, but only for one fixed input frequency.

In the improved circuit arrangement shown in Fig. 2, the output pulses from Q are filtered by R_2C_2 to produce a voltage V_1 that is directly proportional to the input frequency. A portion of V_1, tapped off the 10-kilohm potentiometer, is amplified and inverted in transistor Q_2. The amplified voltage is applied through R_1



2. Constant duty cycle. Addition of feedback loop to circuit of Fig. 1 makes duty cycle of output wave independent of input frequency. Triggering of output pulses is the same as in the basic circuit, but the pulse width is automatically adjusted for the duty cycle set by the potentiometer. Here the pot setting gives a square wave at the doubled frequency. Delays of 30 or 40 ns are negligible at frequencies below 1 MHz.

to transistor Q_1, which serves as a controlled current source that feeds the timing circuit of the 74121. The value of R_1 is chosen to limit I_1 to a maximum of 5 milliamperes.

In operation, the 10-kΩ symmetry potentiometer is adjusted for a 50% duty cycle output. If the input frequency increases, V_1 increases proportionally and causes Q_2 to conduct more. This draws more base current from Q_1 and causes its collector current to rise. An increase in I_1 produces a corresponding decrease of output pulse width, tending to lower V_1. The high gain of this negative feedback loop keeps the output duty cycle very near 50% over about a 1,000:1 frequency range. Best results occur when the maximum frequency f_{max} is less than $1/(800\ C_1)$, where C_1 is in farads and f is in hertz. The size of capacitor C_2 is chosen to provide good filtering action for V_1 at the lowest frequency used—that is, C_2 is greater than $1/(1{,}000\ f_{min})$. Other parts values and transistor types are not critical. □

21. Frequency synthesizers

Long/short-period pulses speed synthesizer setting

by Gregory W. M. Yuen
University of Technology, Loughborough, Leicestershire, England

An up/down counter is sometimes used to generate binary digits to tune a phase-locked-loop frequency synthesizer. However, the process is slow—each digital word at the counter's output is set to the desired value by push buttons that increment or decrement the count by one each time the button is pushed.

To speed up the tuning process, the buttons can be held down for a while. In this mode of operation the pulse generator rapidly steps the counter up or down through a succession of states.

The circuit shown below combines both tuning modes. Momentarily pressing a button generates a single pulse that increments or decrements the counter by one, as shown in cycle 1 of the timing diagram.

Keeping the button depressed for more than about half a second steps the counter to change the tuning at a 10-hertz rate; this condition is illustrated in the cycle diagram. Depressing the appropriate button causes the counter to step in the desired direction. As the desired frequency is approached, the button is momentarily pressed to manually step the counter repeatedly until the desired frequency is obtained. Since the method combines the speed of oscillator-derived stepping and the precise tuning of manual stepping, it provides both coarse and fine tuning.

In the circuit diagram, IC_1 is an ITT 74124 universal pulse generator. It consists of two cascaded monostables with feedback to make it operate as an oscillator. When the inhibit-oscillator input is high, this feedback path is active.

In the quiescent state, no button is pressed. Because IC_1's inhibit oscillator input is low, there is no oscillation. Because flip-flop FF_1's $\bar{Q}$ output is low, both transistors are off. When a button is pressed momentarily, it triggers the first monostable in IC_1 to send a pulse to output Q_1. Pulse width T_1 depends on the timing circuit connected to pins 1, 2, and 3. The second monostable is triggered from the trailing edge of Q_1. The Q_2 and $\bar{Q}_2$ outputs from the second monostable, at pins 10 and 9 respectively, have widths T'_2 that depend on the timing circuit connected to pins 11, 12 and 13 (C_2, R_1 and the internal resistance connected to the second monostable—the transistors stay off because FF_1's $\bar{Q}$ output does not change). When cycle 1 is completed, the output pulse from Q_2 has incremented or decremented the counter by one.

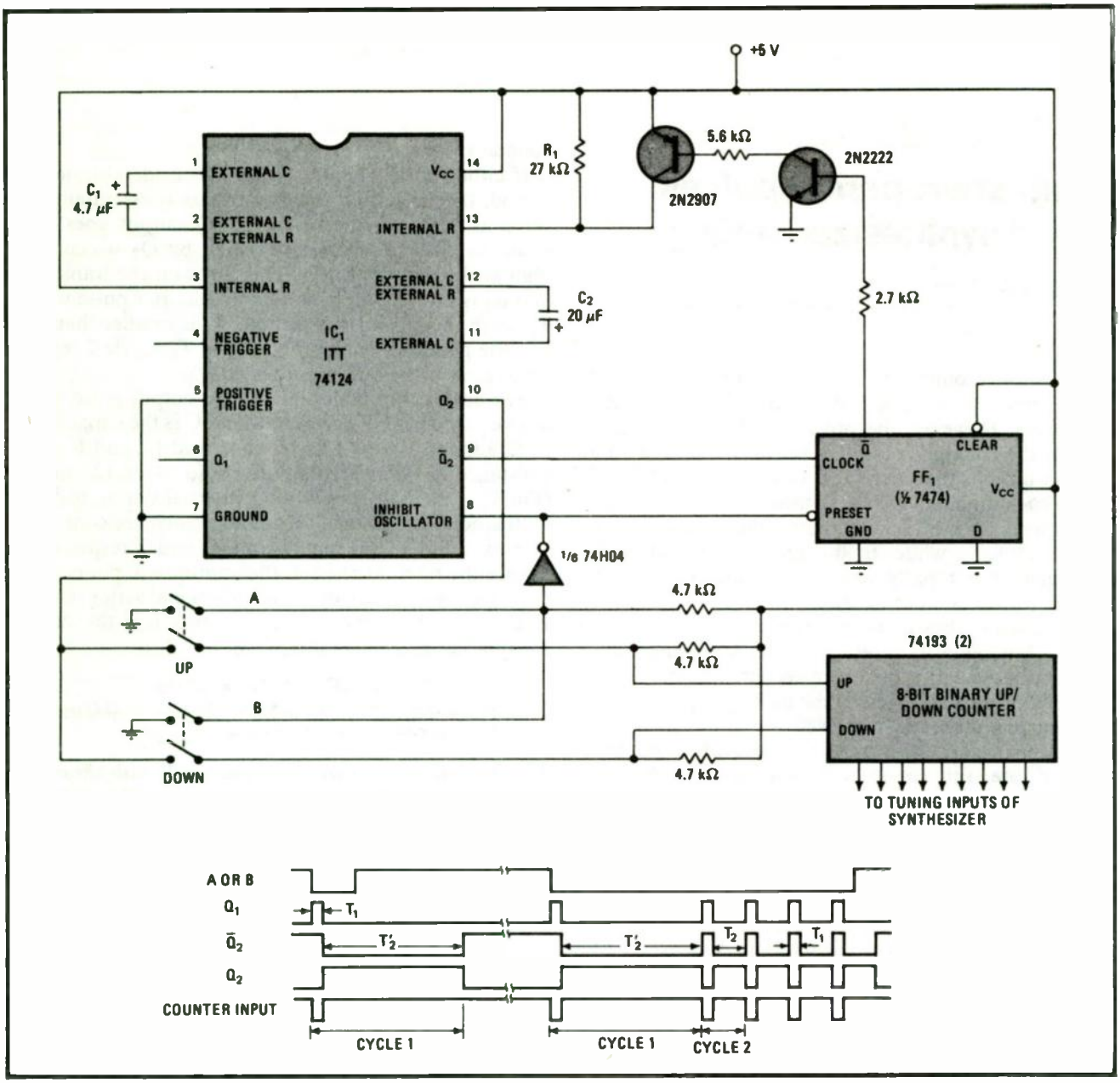
If either button is pressed for a considerably longer period, the initial sequence of events is essentially the same as before. However, FF_1's $\bar{Q}$ output goes high when its clock input is taken high by $\bar{Q}_2$ which goes high at the end of cycle 1. This turns on the transistors and R_1 is shorted out, resulting in a shorter pulse width, T_2, from the second monostable. T_2 is smaller than T'_2, and the period of oscillation is $T_1 + T_2$. Cycle 2 repeats for as long as the button is pressed.

For both monostables in IC_1, the output pulse width is given by 0.695CR seconds, where C is the capacitance in farads across pins 1 and 2 or 11 and 12, and R is the resistance in ohms across pins 2 and 14 or 12 and 14. (Pin 14 is the V_{CC} supply pin.) Internal timing resistors with a nominal value of 7.2 kilohms each are connected at pins 3 and 13 for monostables 1 and 2 respectively. To use the internal resistor, the appropriate pin is taken to V_{CC} either directly or via an additional series resistor. In the latter case, the timing resistance R is the sum of the internal and external resistances. Thus:

$$T_1 = 0.695(4.7\ \mu F)(7.2\ k\Omega) = 24\ ms$$
$$T_2' = 0.695(20\ \mu F)(7.2\ k\Omega + 27\ k\Omega) = 480\ ms$$
$$T_2 = 0.695(20\ \mu F)(7.2\ k\Omega) = 100\ ms$$

The measured pulse widths agreed well with these calculated values. Tantalum capacitors were used for C_1 and C_2.

The up/down counter, consisting of two cascaded 74193s, increments or decrements the output word when the up or down button is pressed. Obviously, the indication of channel or frequency can be derived from the counter's output. If, however, continuous tuning is also provided (by opening the loop at the PLL's voltage-controlled-oscillator tuning-voltage input and connect-



Two buttons set digital tuning word. Digital outputs from up/down counter constitute an 8-bit word that specifies the output frequency of a frequency synthesizer. Speedy access to any of 256 possible words is provided by incrementing or decrementing the counter with pulses. If a button is depressed momentarily, a single pulse is generated; if the button is held down, a fast stream of pulses is generated.

ing this input to a variable-dc voltage source), a frequency counter is used to display the frequency.

If the synthesizer's address word for tuning is in binary-coded decimal, 74192s or other up/down decade counters may be used. Larger tuning-address words can be accommodated by cascading more counters.

A memory (random-access or programable-read-only, depending on whether or not volatility is undesirable) allows arbitrary tuning sequences, including skipping or repeating individual frequencies. If this facility is required, the memory is inserted between the counter and the synthesizer's tuning-address input. □

Thumbwheel switches set synthesizer output frequency

by Jerrold L. Foote
University of Utah College of Medicine, Salt Lake City, Utah

Two binary-coded thumbwheel switches can set the output of a two-decade frequency synthesizer that includes the two switches, a single crystal oscillator, and two decade counters. Synthesizer output accuracy and long-term frequency stability are the same as that of the crystal used as the reference frequency source. Whatever pulse-to-pulse time variation occurs is minimized to an acceptable level by a chain of binary counters.

The synthesis technique involves generating a series of pulses and blank spaces, divided by as many binary counters (N) as needed to yield the desired output frequency (f_o). The frequency-selection circuit consists of thumbwheel switches, S_1 and S_2, two banks of diodes and their corresponding decade counters, and a flip-flop formed by gates G_1 and G_2. More decades of frequency control can be added easily.

The number of oscillator pulses passed by the flip-flop-controlled NOR gate, G_3, is determined by the thumbwheel switch setting (S). Blank spaces occur while the decade counters are counting beyond the switch setting. When these counters reach their maximum count (M), the flip-flop resets, and the oscillator pulses pass through gate G_3 to the binary countdown string. The output frequency is given by:

$$f_o = f_i S/MN$$

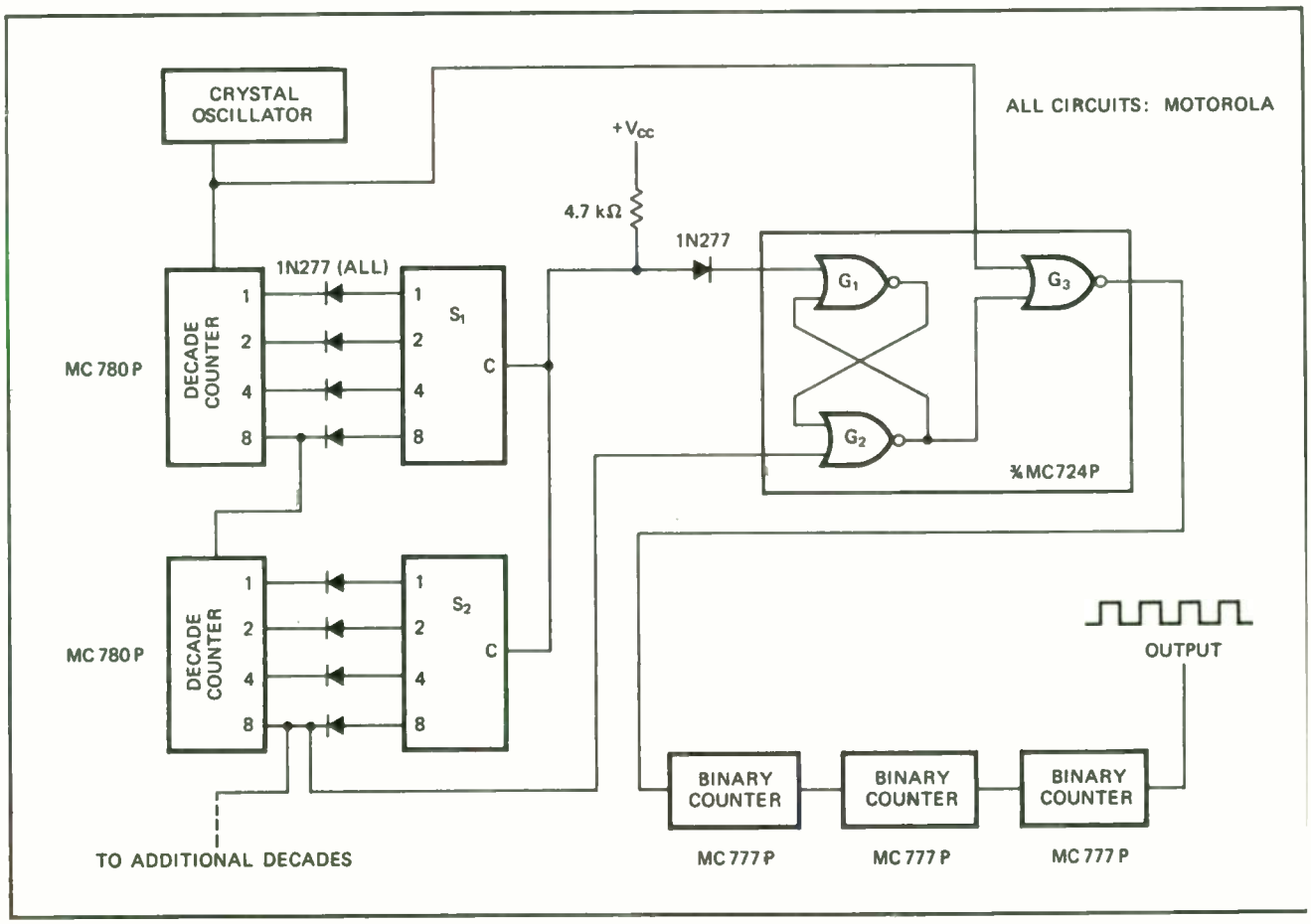
where f_i is the crystal frequency.

The output of gate G_3 is a train of pulses and blank spaces that must be time-averaged to reduce the pulse-to-pulse time variation (ΔT) in the output frequency. This time-averaging is performed by the binary countdown string. The closer the tolerance that must be held on ΔT, the larger is the number of binary counters required. Maximum pulse-to-pulse time variation is:

$$\Delta T = S/f_o N$$

Crystal frequency can be as high as 10 megahertz. □

Dialing frequency. Thumbwheel switches determine number of output decades for frequency synthesizer. Single crystal oscillator serves as frequency source. Decade counters generate pulse train that is divided by binary counter chain to obtain frequency set by switches. When switch-fixed decade count is reached, flip-flop formed by gates G_1 and G_2 resets, enabling gate G_3 so that pulses pass to binary counters.



22. Function generators

Norton quad amplifier can be a low-cost function generator

by P. Vlcek
Orbit Controls Ltd.,
Cheltenham, Gloucester, England

A versatile function generator that minimizes hardware as well as cost can be built with one of the newly introduced Norton quad amplifiers [*Electronics,* Dec. 6, 1973, pp. 116-120]. The price of the complete generator is less than $3, and the entire unit can fit on a circuit board as small as a 1½-inch square.

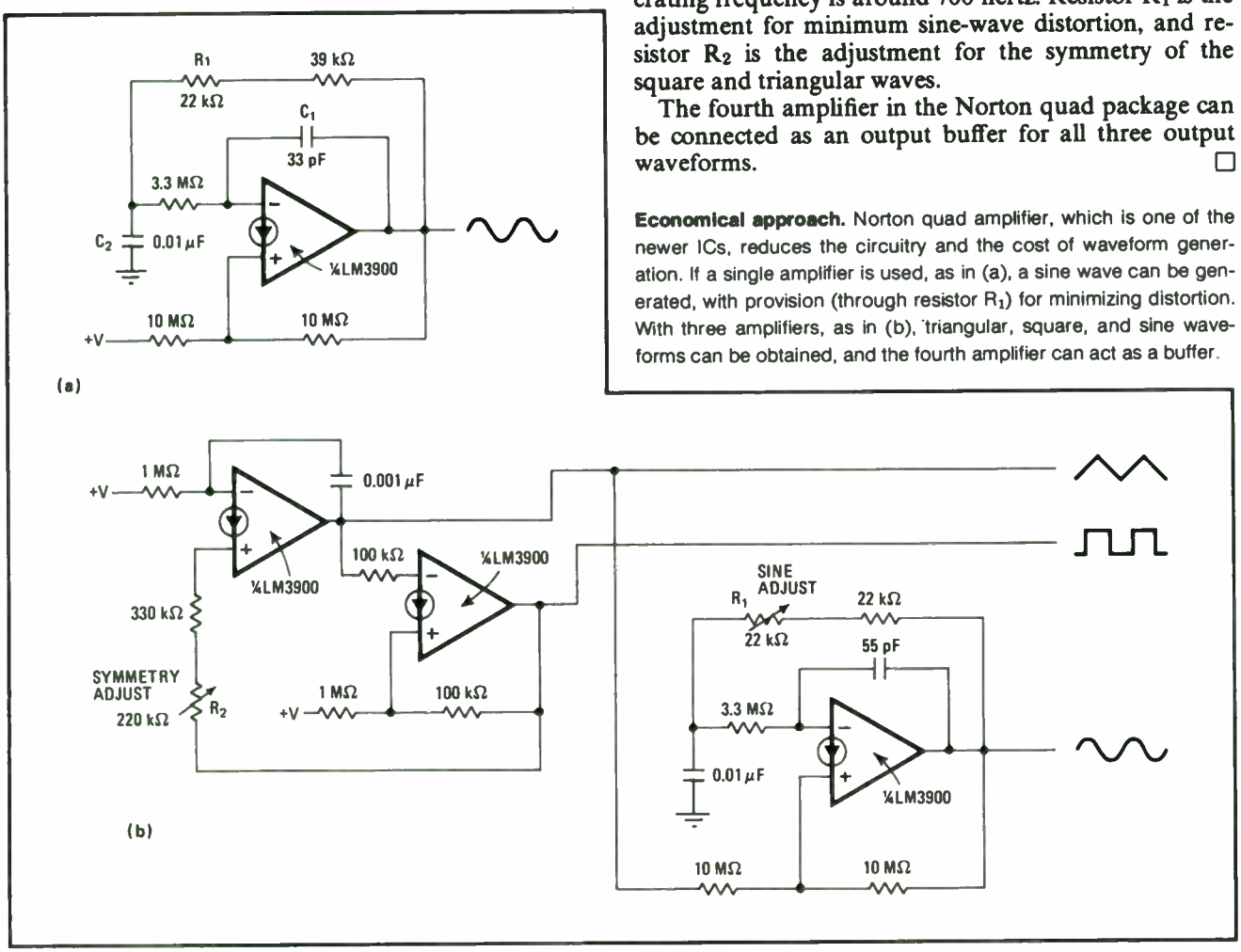
Only a single Norton amplifier is needed to obtain a sine-wave generator (a). When resistor R_1 and capacitor C_1 are omitted from this circuit, the resulting configuration is the standard one for a Norton-amplifier square-wave generator, with the timing current passing through capacitor C_2.

The addition of integrating capacitor C_1 to this square-wave generator produces a resonably accurate sine wave at the output. Resistor R_1, which helps to match the circuit's time constants, can be used to adjust the output sine wave for minimum distortion.

A similar circuit can be used to add a sine-wave output to the conventional hookup for a square-wave/triangular-wave generator built with two Norton amplifiers. As shown in (b), the triangular output acts as the input for the sine-shaper amplifier.

For the component values given here, the circuit's operating frequency is around 700 hertz. Resistor R_1 is the adjustment for minimum sine-wave distortion, and resistor R_2 is the adjustment for the symmetry of the square and triangular waves.

The fourth amplifier in the Norton quad package can be connected as an output buffer for all three output waveforms. □



Economical approach. Norton quad amplifier, which is one of the newer ICs, reduces the circuitry and the cost of waveform generation. If a single amplifier is used, as in (a), a sine wave can be generated, with provision (through resistor R_1) for minimizing distortion. With three amplifiers, as in (b), triangular, square, and sine waveforms can be obtained, and the fourth amplifier can act as a buffer.

Counter and decoder/driver produces staircase voltage

by Donald F. Dekold
Santa Fe Community College, Gainesville, Fla.

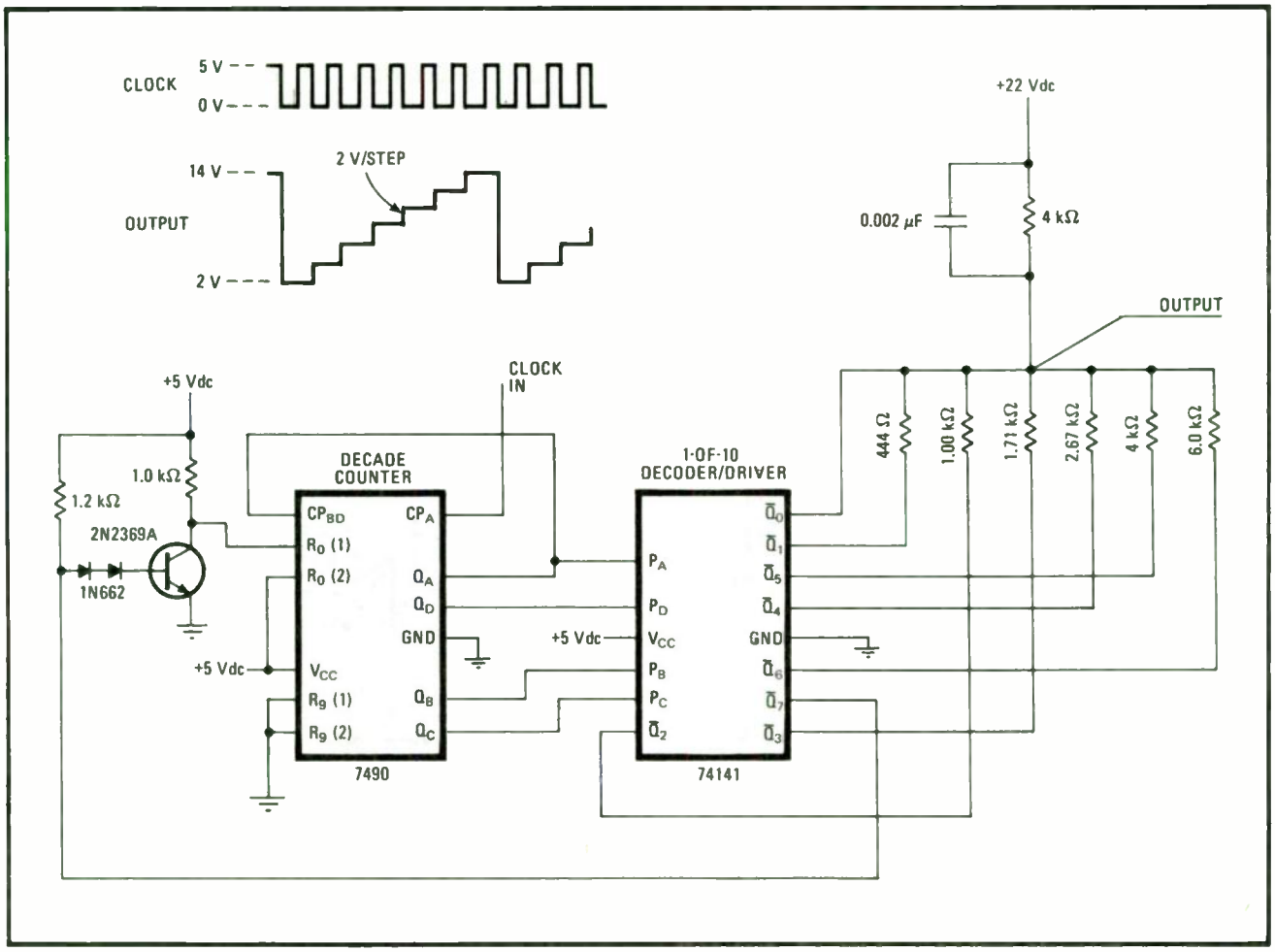
Generating staircase voltage waveforms is easy if some of the newer TTL MSI devices are used. Only two IC packages are needed—a decade counter and a 1-of-10 decoder/driver. Up to 10 distinct staircase voltage steps can .be generated, and the steps can be made quite large, up to 65 volts dc, before exceeding the output breakdown limitations of the decoder/driver. The circuit is useful as a building block in a curve tracer or a low-resolution analog-to-digital converter, and in control applications requiring the sequential stepping of voltages.

Resistive voltage division is employed (only one output of 10 is on at a time), rather than op-amp summing techniques. This allows the steps to be generated at a rather faster rate than would be possible with an op amp, which is hampered by its slew-rate limitations. The step levels need not advance with equal increments (or decrements), but can be programed by selecting the proper resistors in the voltage divider network. However, loading effects must be considered when designing for the output levels wanted.

The circuit in the diagram generates a seven-level staircase output, increasing from 2 to 14 V dc in 2-V increments. The eighth negative clock transition produces a logic low at the corresponding decoder/driver output, $\overline{Q}_7$, which resets the counter to zero via the transistor stage. (Without this reset transistor, the counter would automatically reset to zero at the end of the 10th clock cycle.) On the first count, the generator's output is taken from the decoder/driver's $\overline{Q}_0$ output and is 2 V dc, a typical value for the decoder/driver when it is sinking a 5-milliampere current.

The generator may accept clock frequencies as high as 10 kilohertz, but the transition-time transients that will occur between each output step make the capacitor shown necessary. Although the capacitor provides smoother step transitions, it limits the maximum operating frequency. □

Two-package stepper. Staircase output generated by decade counter and 1-of-10 decoder/driver can have up to 10 voltage steps, each step being as large as 65 volts. The resistor voltage divider network scales the outputs of the decoder/driver to the desired step sizes. Clock frequencies can be as fast as 10 kilohertz. The capacitor smooths the output transients that may occur at the clock transitions.



Synchronous ramp generator maintains output linearity

by D. M. Brockman
Boeing Co., Seattle, Wash.

With complementary-MOS analog switches, a synchronous ramp generator can be built without the need for expensive ladder networks or costly amplifiers. This circuit is intended for use in a multichannel analog-to-digital converter system where digital words must be developed to represent transducer outputs.

When triggered, the circuit generates a linear ramp having time and voltage parameters that are independent of component tolerances, power-supply voltage, and clock rate. The ramp output is synchronous with a binary or binary-coded-decimal counter and always runs from a negative reference voltage at the counter's zero state to a positive reference voltage at the counter's full-scale state. The generator's ramp output can be used as the reference signal for comparator-type analog-to-digital converters.

The ramp is generated by integrator A_1. Switch S_2 is initially closed, and switches S_1 and S_3 are open, clamping A_1's output to $-V_{ref}$. The counter is kept reset by flip-flop FF_1.

When the circuit is triggered, the counter begins to run, S_2 is opened, and S_1 is closed. Integrator A_1 begins to charge linearly at a rate determined by time constant R_1C_1 and the output voltage produced by integrator A_2.

After the counter reaches full scale, switch S_1 opens and stops the ramp, while switch S_3 closes and starts the comparison cycle.

During the comparison cycle, A_1's output is inverted by amplifier A_3 and summed with $+V_{ref}$ by integrator A_2. If the sum is not zero, A_2 charges toward a voltage (and polarity) that will make the sum zero at the next comparison cycle. When the counter reaches full scale for the second time, the comparison cycle is ended, switch S_3 is opened, switch S_2 is closed, and the counter and flip-flop FF_1 are reset.

This generate/compare process is repeated each time the circuit is triggered. And, after a few cycles, the output voltage of integrator A_2 will be just large enough to drive integrator A_1 to $+V_{ref}$ in the time required for the counter to reach full scale.

Inverter A3 is provided with a gain adjustment to compensate for tolerances on integrator A_2's summing resistors and to allow the peak ramp voltage to be set exactly to $+V_{ref}$. Time constant R_1C_1 must be chosen so that integrator A_2 does not saturate. And time constant R_2C_2 must be selected for circuit stability:

$$R_2C_2 = T^2/R_1C_1$$

where T is the ratio of the full-scale count to the clock rate.

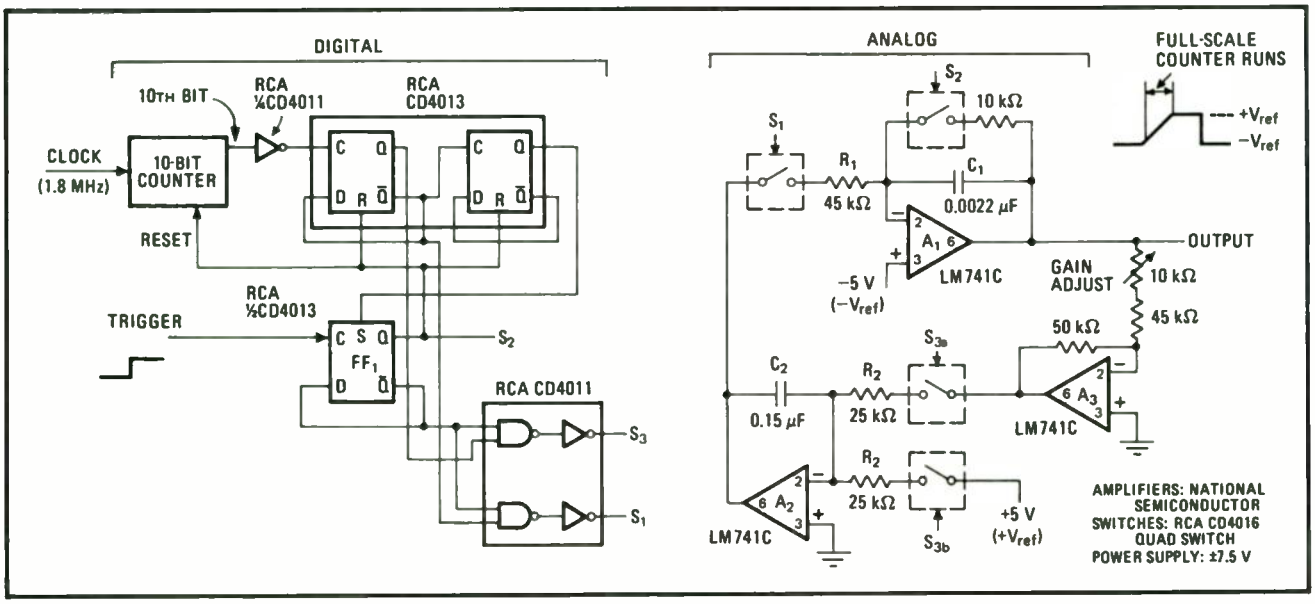
The circuit's stability factor becomes:

$$S.F. = R_1R_2C_1C_2/T^2$$

If the stability factor is equal to one, the circuit will respond to step changes in $+V_{ref}$ without overshoot. If the factor is greater than one, the generator's response will be underdamped.

The component values shown are for a 1.8-megahertz clock rate and a full-scale count of 1,024. □

Automatic compensation. Synchronous ramp generator uses low-cost complementary-MOS analog switches instead of high-priced ladder networks. Closed-loop circuitry automatically corrects ramp slope for small changes in component values, clock rate, or supply voltage. Ramp output climbs from $-V_{ref}$ to $+V_{ref}$ as counter runs from its zero state to its full-scale count. For this circuit, clock rate is 1.8 megahertz.



Triangular-wave generator spans eight decades

by William S. Shaw
University of Texas, Applied Research Laboratories, Austin, Texas.

Because of its nonsaturating design, a triangular-wave generator can cover eight decades of frequency—from 0.01 hertz to 2 megahertz. Lower and upper frequency limits are set by resistance adjustment. Circuit layout is not critical, and complementary circuitry assures output symmetry and amplitude stability, as well as the absence of dc offset. By decreasing output voltage swing and increasing current, the generator's frequency range can be made to span 1 to 20 MHz.

Transistors Q_1 and Q_2 are constant-current sources whose outputs are switched to produce the charging and discharging currents for the output capacitor. Transistor pairs Q_3-Q_4 and Q_5-Q_6 are differential amplifiers that function as comparators; Q_3 and Q_6 conduct whenever Q_4 and Q_5 switch off, and vice versa.

The series string of diodes D_1 and D_2 and resistors R_1, R_2, R_3, and R_4 set comparator voltages V_1 and V_2. Diodes D_1 through D_4 compensate the four-transistor integrated-circuit array so that the generator maintains its frequency stability with changing temperature. Comparator input and output currents are:

$$i_1 = 28.7R_1/(R_1+R_2+R_3+R_4)R_5$$

$$i_2 = R_7 i_1/R_6$$

When Q_4 and Q_5 are on, Q_3 and Q_6 are off, and output capacitor C_1 charges at a constant rate (since i_2 is a constant) until the upper trigger level (V_U) is reached:

$$V_U = V_{E1} + V_{BE1} + V_{D5}$$

where V_{E1} is the voltage at Q_1's emitter, V_{BE1} is Q_1's base-emitter voltage, and V_{D5} is the voltage across diode D_5. Once output voltage equals V_U, transistor Q_1 conducts and Q_2 switches off, turning Q_3 and Q_6 on. Since R_7 is larger than R_6, Q_4 and Q_5 will switch off.

Due to the symmetry of the circuit, capacitor C_1 is discharged by transistor Q_6 at the same constant rate as it was charged and by the same current, i_2. The capacitor discharges to the lower trigger level (V_L):

$$V_L = V_{E2} - V_{BE2} - V_{D6}$$

where V_{E2} is Q_2's emitter voltage, V_{BE2} is Q_2's base-emitter voltage, and V_{D6} is the voltage across diode D_6. When V_L is reached, Q_1 turns off, Q_2 turns on, and V_2 becomes larger than V_4. This switches on Q_4 and Q_5, causing Q_3 and Q_6 to switch off by feedback through capacitor C_2. The cycle can now repeat.

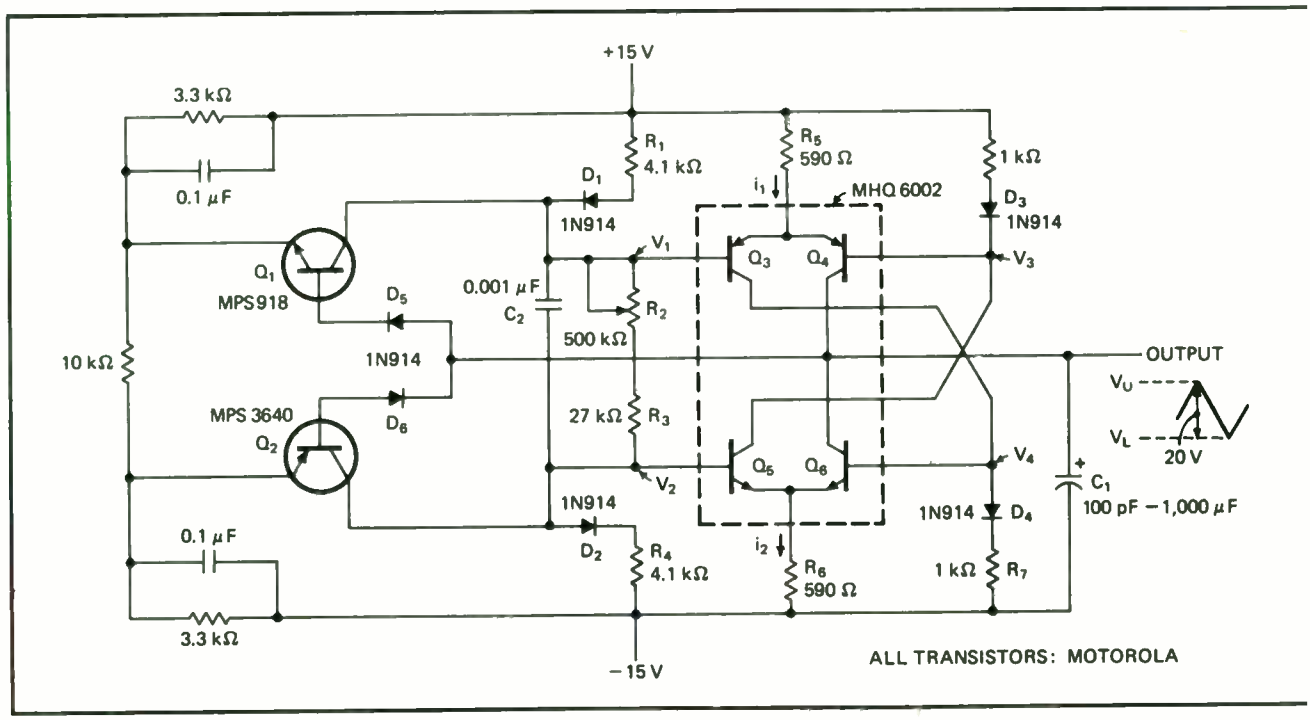
Diodes D_5 and D_6 allow the output to slew above and below the limits imposed by the emitter-base breakdown voltage (about 6 V) of Q_1 and Q_2. The generator will oscillate without latch-up as long as V_{E1} is less than V_1 and V_{E2} is greater than V_2.

For a 20-V peak-to-peak output, the frequency is:

$$f_{out} = 0.0425 i_1/C_1$$

Capacitor C_1 determines nominal output frequency while resistor R_3 sets the lower frequency limit and potentiometer R_2 sets the upper limit in addition to providing a linear frequency span of 20:1. When R_2 = 500 kilohms and C_1 = 1,000 microfarads, f_{out} = 0.01 Hz when R_2 = 0 and C_1 = 100 picofarads, f_{out} = 2 MHz. □

High-frequency triangles. Complementary nonsaturating circuitry permits triangular-wave generator to provide 20-volt output at frequencies as high as 2 megahertz. Output triangle is obtained by charging and discharging C_1. Current from Q_2 charges C_1 until output voltage reaches threshold V_U, then Q_3-Q_4 and Q_5-Q_6 comparators switch, and Q_1 supplies discharge current until threshold V_L is reached.



Staircase generator resists output drift

by Maxwell Strange
NASA, Goddard Space Flight Center, Greenbelt, Md.

Tracking capacitors that mutually cancel temperature drift make a simple analog staircase generator, which is as accurate and stable as expensive circuits that employ precision digital-to-analog converters. Additionally, the strictly analog circuit is easier to adjust for any number of steps and to any step amplitude.

The generator essentially consists of two sections, a one-shot and an integrate-and-hold circuit. The one-shot, which drives the integrate-and-hold circuit, is triggered by an oscillator or system clock that determines the generator's stepping rate. During the high period (T) of the one-shot's output pulse, integrating capacitor C_1 is charged to produce an output voltage step:

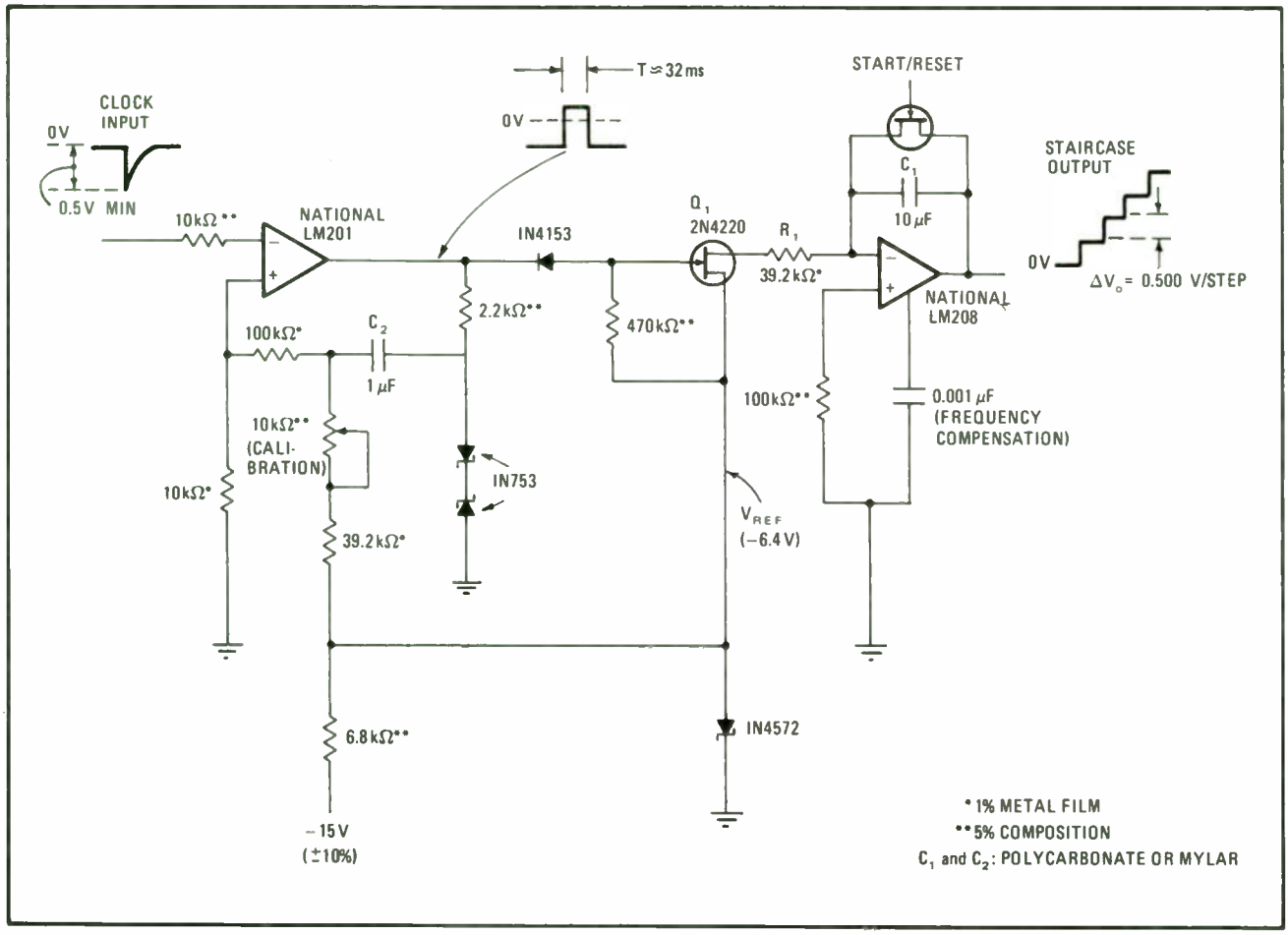
$$\Delta V_o = V_{REF}T/R_1C_1$$

Between one-shot output pulses, transistor Q_1 is off, and the integrator becomes a hold circuit and maintains the output constant.

Capacitors C_1 and C_2 are the two components with the greatest effect on step height stability. If the same type of capacitor is used in both the one-shot and the integrator sections of the circuit, the temperature coefficients of C_1 and C_2 will cancel. Staircase risetime is proportional to capacitor C_2, while integrator slope is proportional to capacitor C_1, so that step height is unaffected by a similar percentage change in both capacitors. The period of the one-shot's output pulse is directly proportional to the ratio of C_2/C_1.

As for the output voltage droop that occurs during the integrator's hold mode, the value of C_1 must be large enough to keep it negligible over the staircase cycle. For the components shown, output droop is only about 1 millivolt in 10 seconds, and step amplitude is stable within ±0.2% from 0°C to 50°C. □

Stepping up. Staircase generator employs one-shot to drive integrate-and-hold circuit. During one-shot period, capacitor C_1 charges and steps up output voltage. When one-shot is off, integrator section holds step height constant. Output voltage droop is kept to 1 millivolt in 10 seconds. Step amplitude drift is held to ±0.2% because temperature coefficients of same-type capacitors C_1 and C_2 cancel.



Generating tone bursts with only two IC timers

by L. W. Herring
LWH Associates, Dallas, Texas

With very few external components, two IC timers can be made to function as a tone-burst generator that is useful for radio and telephone applications. In the circuit shown here, one timer controls the tone burst, and the other generates its frequency.

Normally, a tone-burst generator is built with three timers, two being required for the control function. Although a single timer in its delay mode could provide the initial time period, the second timer is required to generate the burst length and reset the first timer. Alternatively, in the astable mode, a single timer's output duty cycle could be adjusted for the quiet and burst periods, except for one thing—the time to the first burst would be almost twice as long as the time to subsequent bursts because the initial charging period of the timing capacitor is longer than later periods.

Nevertheless, a single timer can in a sense be fooled into providing the control function on its own if an RC network (resistor R_2 and capacitor C_2 in the figure) is added to the timer's ($TIMER_1$) threshold and trigger inputs. Of course, the larger primary timing network (resistor R_1 and capacitor C_1 in the figure) remains connected to the timer's discharge circuit.

$TIMER_1$ is set up as an astable oscillator. But its threshold inputs are kept high by the additional RC network (R_2 and C_2) for longer than it takes the timer's discharge circuit to completely discharge the main RC network (R_1 and C_1). This assures that the output period of $TIMER_1$ remains almost constant, no matter if the burst is the first one or the last one.

The period that $TIMER_1$'s output remains high can be approximated by the standard equation for delay-mode operation:

$$T_{on} = 1.1R_1(C_1+C_2)$$

The burst output time (when the output is low) can be adjusted to the desired value by the R_2C_2 network. This period is approximated by the equation for astable-mode operation:

$$T_{off} = 0.693R_2C_2$$

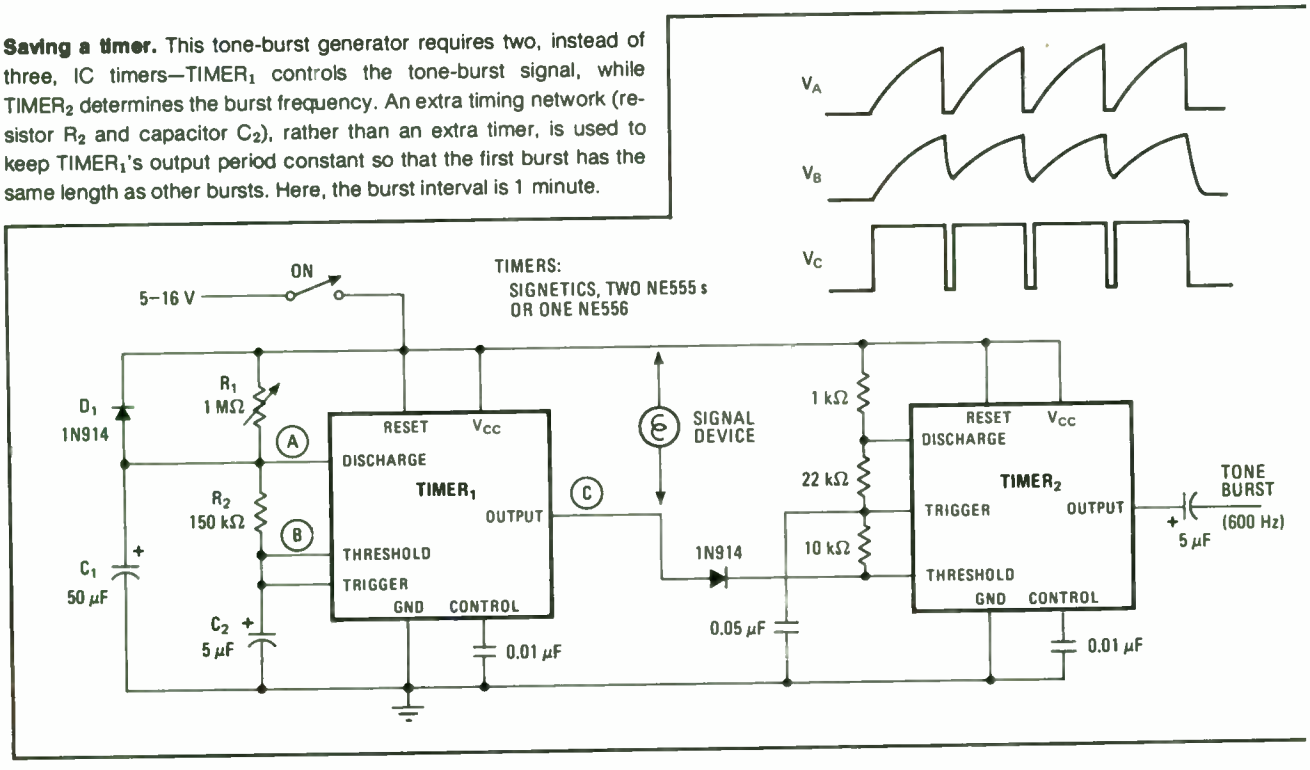
When the added time period (burst length) approaches or exceeds the main time period, the two timing networks interact.

For this circuit, the output of $TIMER_1$ remains high for 1 minute and goes low for a half second. The best way to activate the circuit is to switch the V_{CC} supply lead for the entire circuit. Diode D_1 assures that capacitor C_1 will be discharged after any partial periods.

The control timer ($TIMER_1$) can provide the output for a lamp, bell, buzzer, or other signaling device. (This timer's output must be used to sink the signaling device, which must also be wired to the supply line.) $TIMER_2$ operates as the tone oscillator, determining the frequency of the tone burst. The manner in which $TIMER_2$ is keyed eliminates the need for an intermediate device to invert the output of $TIMER_1$ to operate the reset lead of $TIMER_2$.

This simple tone-burst generator can be used as an audible timing reminder for long-distance telephone calls or for radio repeaters that have 3-minute shutdown timers. The same arrangement can be used to generate sampling pulses for a sample-and-hold circuit or for a serial-to-parallel data converter for Ascii-character detectors. □

Saving a timer. This tone-burst generator requires two, instead of three, IC timers—$TIMER_1$ controls the tone-burst signal, while $TIMER_2$ determines the burst frequency. An extra timing network (resistor R_2 and capacitor C_2), rather than an extra timer, is used to keep $TIMER_1$'s output period constant so that the first burst has the same length as other bursts. Here, the burst interval is 1 minute.



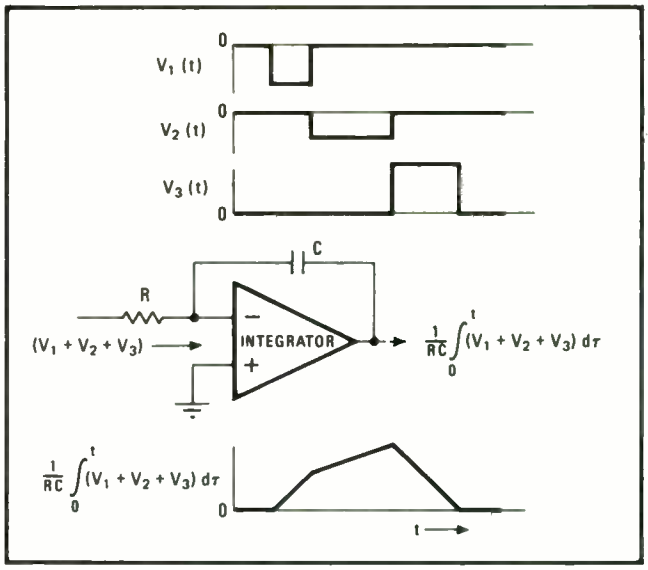
Waveform is synthesized from linear segments

by E. D. Urbanek
Bell Telephone Laboratories, Murray Hill, N.J.

Just as a curve can be approximated by a series of straight lines, so can a waveform be approximated by a succession of voltage ramps. The voltage ramps may be the output of an integrator driven by a succession of rectangular pulses of various amplitudes and durations. Figure 1 shows how the integration of three such pulses produces three sequential ramps to yield a novel wave shape. The amplitude and polarity of each pulse determine the slope and direction of the corresponding ramp, and the width of the pulse determines the length of the ramp. The output voltage function can be made to resemble a curve if enough pulses and ramp segments are used.

A function generator that synthesizes waveforms in this manner is used as a control for automatic-gain-control circuits and for sweep generation. As shown in Fig. 2, it contains type 121 one-shot multivibrators to generate the pulses that are to be integrated, a 741 operational amplifier connected as an inverter to change the polarity of pulses when necessary, and another 741 op amp connected as an integrator. The 2N2481 transistor prevents drift.

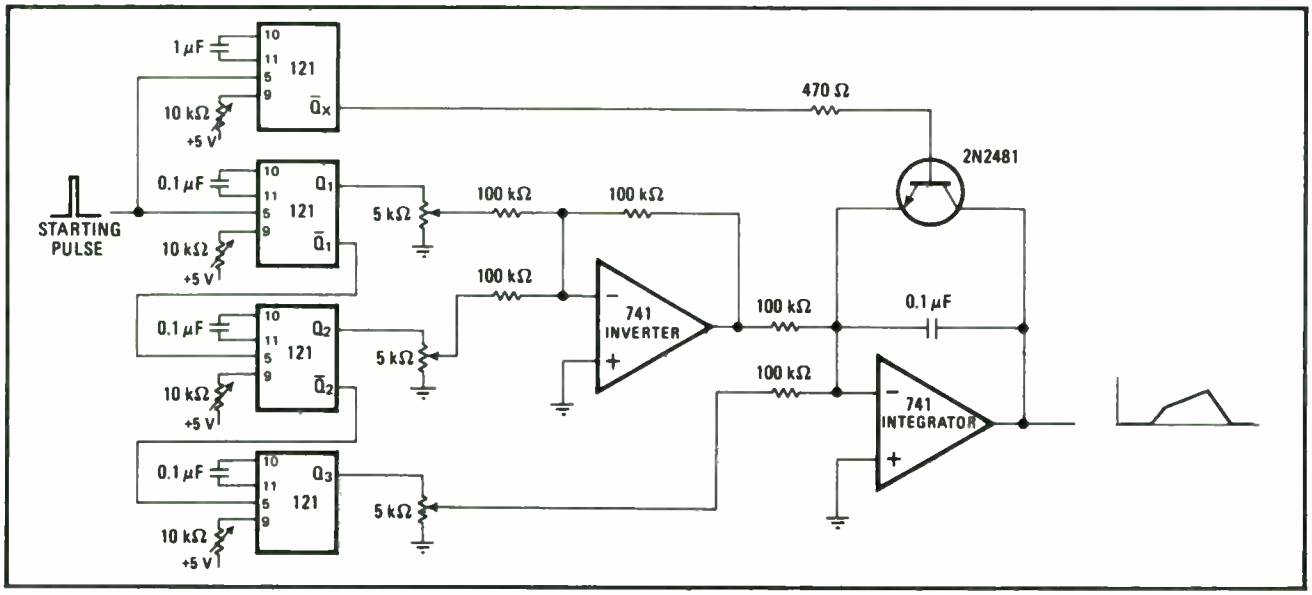
The one-shot units are arranged in a series so that the complementary output ($\bar{Q}$) of the first unit serves as the trigger for the second unit, and so forth. This arrangement produces a sequence of positive pulses. The duration of each pulse is determined by the timing resistor and capacitor of its one-shot, and the amplitude of each pulse is set by the potentiometer at the output of the



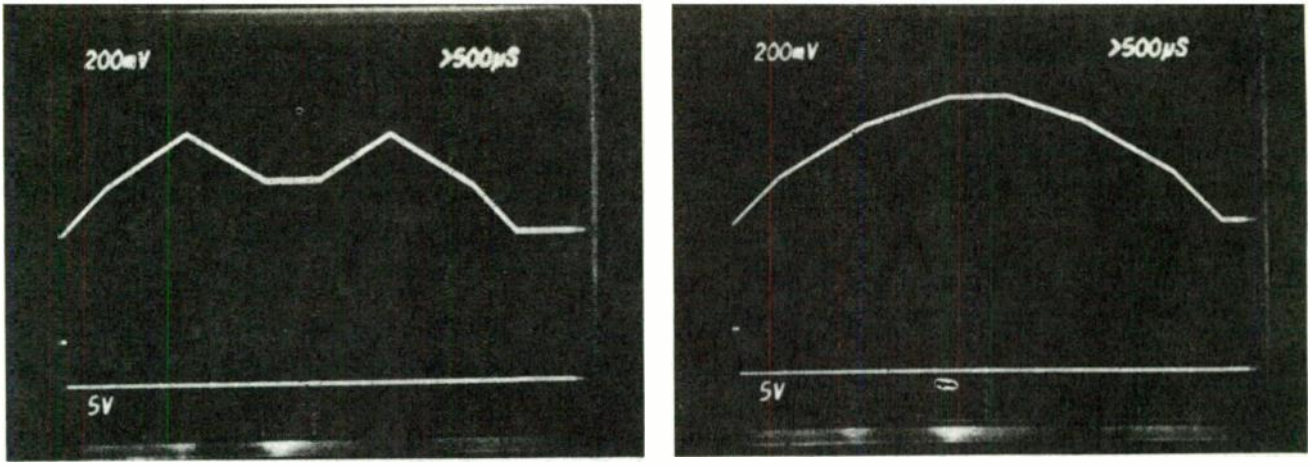
1. Waveform generation. Integration of sequential rectangular pulses produces sequential voltage ramps that make up output waveform. Amplitude, polarity, and duration of pulses determine the slope, direction, and length of the ramps.

one-shot. Each positive pulse can be connected directly to the integrator to produce a ramp with negative slope, or it can be connected through the inverter and thence to the integrator to produce a ramp with positive slope.

An additional one-shot unit and the transistor are used to form an anti-drift control. The complementary output ($\bar{Q}_x$) of this one-shot is used to drive the transistor, which discharges the 0.1-microfarad integrating capacitor. With no input pulse applied, the transistor keeps the capacitor discharged. Holding the integrator output at zero in this way prevents integration of any offset voltages. When an input pulse is applied to start the function generator, ($\bar{Q}_x$) is driven off and the transistor releases the capacitor. The off time of ($\bar{Q}_x$) may be



2. Circuit. Function generator uses one-shot multivibrators to supply series of pulses to op amp connected as integrator. Pulse polarity can be reversed by op amp connected as inverter. Complementary output from each pulse generator triggers next pulse in sequence, producing continuity in wave shape. Pulse widths are set by RC time constant for each one-shot, and pulse amplitudes are set by potentiometers.



3. Waveforms. Scope traces generated by seven-segment function generator. Maximum voltage on these traces is about 0.5 volt, and duration of traces is about 4 milliseconds. Traces could be brought down to zero-voltage level smoothly, by sloping segments, or abruptly, by use of transistor to short-circuit integrating capacitor. Trace on right here shows that just a few segments suffice to approximate a curve.

adjusted to coincide with the total on time of the function generator, or it may be adjusted to terminate the waveform at any point during the on time.

Scope traces of seven-segment waveforms are shown in Fig. 3. The voltage level remains constant (because there is no input pulse to the integrator) between the end of the seventh segment and the retriggering of the start pulse. The maximum voltage on each trace is about 0.5 volt, and the total duration of a trace is about 4 milliseconds.

In applications where a wide range of ramp slope is required, the potentiometer attenuators can be eliminated, and the input resistors on the inverter and integrator can be made variable. This increases inverter gain and allows control of both voltage and time constant of the integrator for adjusting the slopes. □

Link-coupled tank circuit steps up C-MOS drive voltage

by R.W. Mouritsen
National Research Council of Canada, Ottawa, Canada

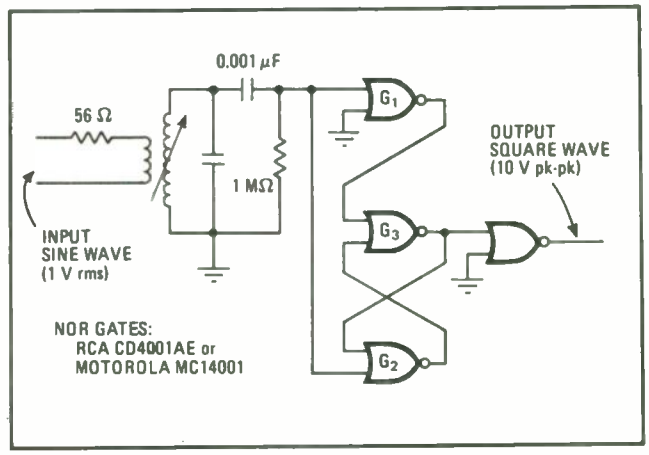
Because of their low power dissipation, low leakage current, and high noise immunity, complementary-MOS devices are a sound design choice for portable or battery-operated equipment—such as counter chains or clocks driven from standard oscillators. However, several volts, typically 5 to 7 volts, are usually required to turn on the C-MOS device, whereas most standard oscillators normally have an output of only about 1 V root-mean-square at 50 ohms.

A simple way around this problem is to use a link-coupled tuned circuit as a voltage step-up transformer. Since the input impedance of the C-MOS device is extremely high, the tank circuit is loaded only by the primary source impedance reflected across the secondary winding. This allows the use of a fairly high-Q coil. The link-to-secondary turns ratio is adjusted to produce, across the tuned circuit, a sine wave with a peak-to-peak amplitude of approximately 90% of the supply voltage, when the driving signal is 1 V rms at 50 ohms.

The squaring circuit shown in the figure is an example of this link-coupling technique. It consists of a C-MOS quad two-input NOR gate package, connected as a forced latch.

With the input at 0 V (logic 0), the outputs of gates G_1 and G_2 are logic 1, while the output of gate G_3 is logic 0. As the input rises (towards logic 1), the outputs of gates G_1 and G_2 go to logic 0 when the C-MOS turn-on threshold voltage is reached. This forces the output of gate G_3 to go to logic 1 and remain there until the input falls below the threshold level. At that time, gate G_1 goes to logic 1, allowing gate G_3 to return to logic 0 and causing gate G_2 to go to logic 1.

When the supply voltage is 12 V and the input signal is 1 V rms at 50 ohms and 1 megahertz, the squaring circuit produces an output that approximates a square



Squaring circuit. Link-coupled tuned circuit provides transformer-like action, stepping up the low-level drive signal supplied by most standard oscillators. This permits complementary-MOS gates, the threshold voltages of which are generally 5 to 7 volts, to be used without adding extra active devices. With this squaring circuit, a 1-V sine wave is converted to a 10-V square wave at megahertz rates.

wave with an amplitude of around 10 V pk-pk and with rise and fall times of about 50 nanoseconds. The tuned circuit used here has a narrow operating band. A wider band may be obtained by employing a small toroid having a bifilar secondary with a link-coupled primary. This will yield about the same output waveform, but operating frequency will range between 500 kilohertz and 3.5 MHz, depending on the ferrite used. □

Square-wave generator stresses frequency stability

by S.F. Aldridge
IBM Corp., General Products Div., San Jose, Calif.

Offering features that are usually found only in more elaborate oscillators, a simplified voltage-controlled square-wave generator produces very symmetrical complementary square-wave outputs that exhibit good frequency stability over a wide operating temperature range. Output frequency repeatability can be held, without adjustment, to within a 5% range, and operating frequencies can exceed 50 megahertz.

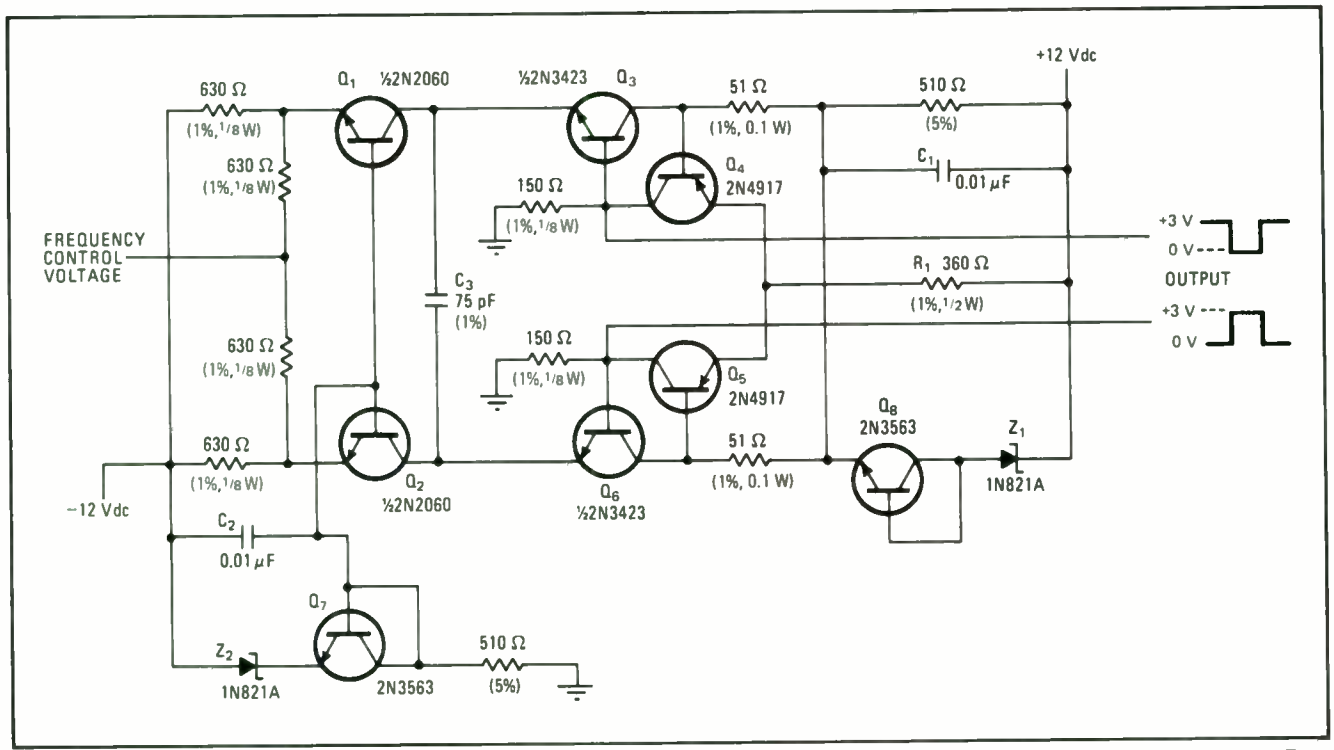
The circuit's noise insensitivity is excellent due to its current-source decoupling (provided by capacitors C_1 and C_2). Moreover, noise generation within the generator is held to a minimum because of the constant-current nature of the circuit.

Power-supply variations as large as 15% produce a negligible shift in output frequency because of the action of the circuit's current sources (transistors Q_1 and Q_2) and the configuration of the circuit's oscillator section. The generator can be considered to provide linear operation throughout the entire range of its input frequency control voltage.

Basically, the oscillator section consists of two Schmitt triggers: one formed by transistors Q_3 and Q_4, and the other formed by transistors Q_5 and Q_6. The triggers share the two current sources (transistors Q_1 and Q_2), as well as resistor R_1 because of capacitor C_3. Transistors Q_4 and Q_5 form a differential switch that allows only one Schmitt trigger to be on at a time.

The charge rate of capacitor C_3 determines the switching frequency of the Schmitt triggers and, therefore, the output frequency, This charge rate can be controlled by varying the voltage on the frequency-control input line, which, in turn, changes the current of transistors Q_1 and Q_2. The output frequency can also be altered by changing the value of capacitor C_3.

Temperature compensation is provided by zener diodes Z_1 and Z_2. Transistor Q_7 compensates the base-emitter junctions of transistors Q_1 and Q_2, while transistor Q_8 compensates transistors Q_3 and Q_6. To achieve the best circuit performance, matched transistors and components having 1% tolerances should be used. □



Simplified design. Square-wave generator supplies complementary outputs whose frequency is determined by an input control voltage. This control voltage determines the current provided by transistors Q_1 and Q_2 to charge capacitor C_3. The charge rate of this capacitor sets the switching frequency of the two Schmitt triggers, which are formed by transistors Q_3 and Q_4 and transistors Q_5 and Q_6.

Digital pulses synthesize audio sine waves

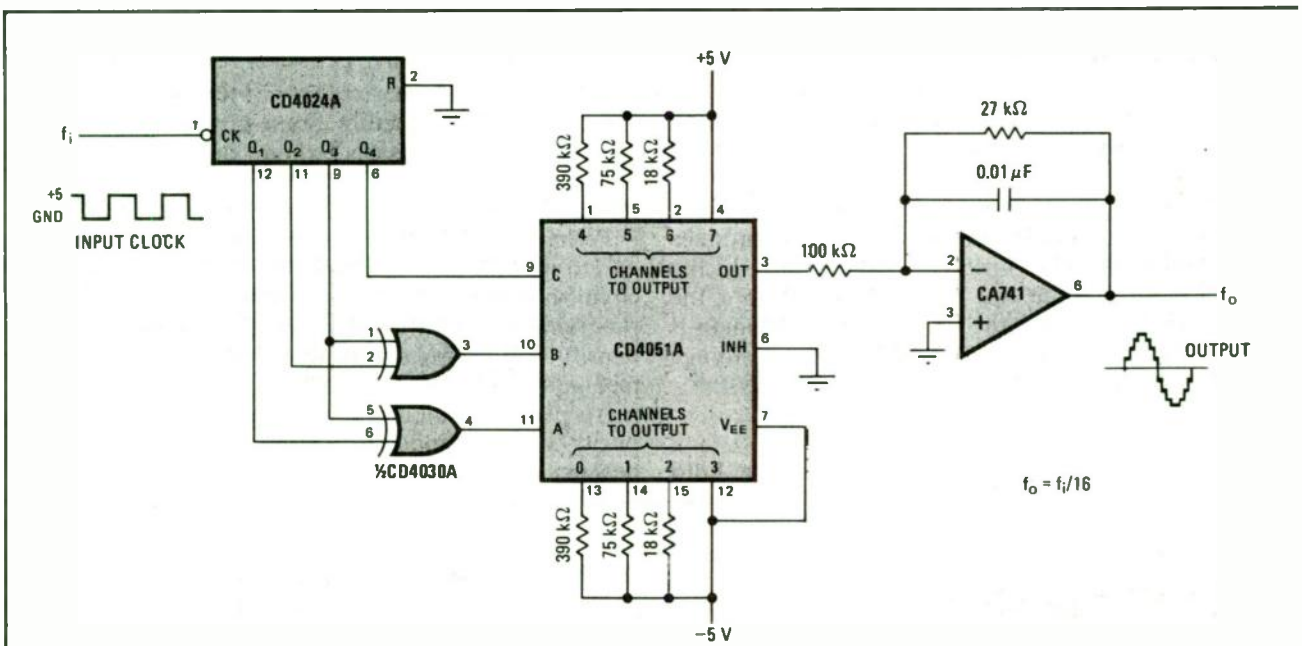
by Patrick L. McGuire
General Dynamics, Pomona, Calif.

Audio tones are often employed for signaling and control in digital systems. To minimize harmonic distortion and channel cross talk, the waveforms of these tones must resemble sine waves as nearly as possible. If the square-wave signal typical of a digital system were used directly, it would have to be thoroughly filtered. Integrated circuits that produce sinusoids from digital inputs, now available commercially, are powerful for their specific functions. However, the technique shown here offers a more general approach to the generation of sine waves or other repetitive waveforms. It requires only a few inexpensive components and dissipates very little power because it is implemented with complementary-MOS circuits.

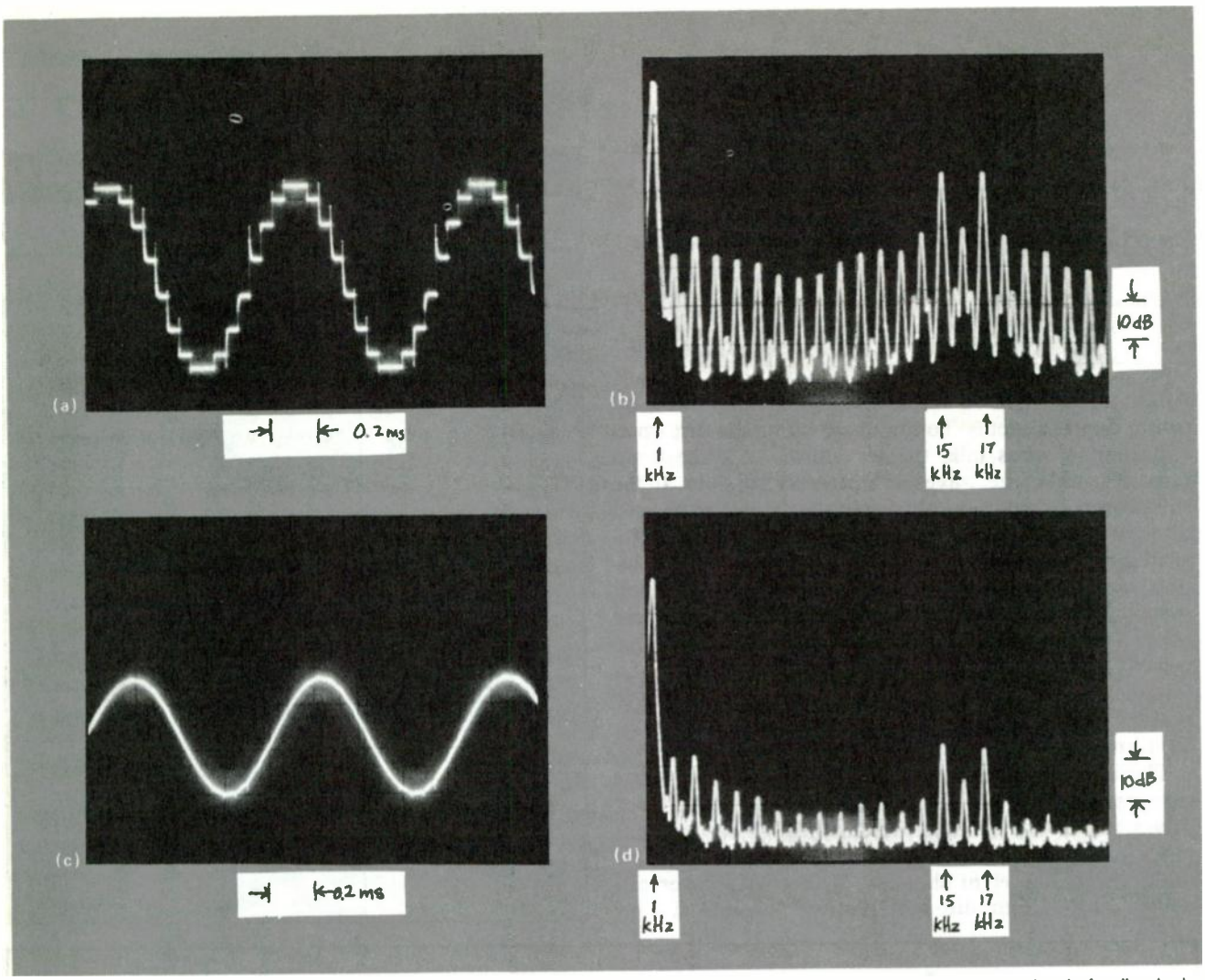
The circuit shown in Fig. 1 generates a 1-kilohertz sine wave from a 16-kHz clock input. The input clock drives a CD4024 counter, which, through some count modification in exclusive-OR gates, drives a CD4051 multiplexer. The eight channels of the multiplexer can deliver any of four different positive currents or four

GENERATING SINE WAVES

Pulse No.	Outputs from CD4024 Q_4	Q_3	Q_2	Q_1	Inputs to CD4051 C	B	A	ON channel of CD4051	Output voltage from 741
⋮		⋮				⋮		⋮	⋮
14	1	1	1	0	1	0	1	5	−0.77
15	1	1	1	1	1	0	0	4	−0.28
0	0	0	0	0	0	0	0	0	0.28
1	0	0	0	1	0	0	1	1	0.77
2	0	0	1	0	0	1	0	2	1.14
3	0	0	1	1	0	1	1	3	1.35
4	0	1	0	0	0	1	1	3	1.35
5	0	1	0	1	0	1	0	2	1.14
6	0	1	1	0	0	0	1	1	0.77
7	0	1	1	1	0	0	0	0	0.28
8	1	0	0	0	1	0	0	4	−0.28
9	1	0	0	1	1	0	1	5	−0.77
10	1	0	1	0	1	1	0	6	−1.14
11	1	0	1	1	1	1	1	7	−1.35
12	1	1	0	0	1	1	1	7	−1.35
13	1	1	0	1	1	1	0	6	−1.14
14	1	1	1	0	1	0	1	5	−0.77
15	1	1	1	1	1	0	0	4	−0.28
0	0	0	0	0	0	0	0	0	0.28
1	0	0	0	1	0	0	1	1	0.77
⋮		⋮				⋮		⋮	⋮



1. Sine-wave generator. The 16-kHz input clock drives a counter that, through X-OR gates, drives a multiplexer. The multiplexer simpl routes currents in amplitudes proprotional to a sampled sine wave into the summing junction of the op amp. The feedback capacitor rolls o the frequency response of the amplifier at about 600 Hz. This technique of waveform generation can also be used for other repetitive waves.



2. Output. Wave shape and spectral composition of output from circuit in Fig. 1 are shown with and without filter capacitor in feedback circuit of output operational amplifier. Without filtering, waveform (a) clearly shows the discrete steps of synthesis, and spectrum (b) contains harmonics at 15 kHz and 17 kHz that are only 25 dB below the fundamental 1-kHz output. With frequency response rolled off at about 600 Hz by addition of filter capacitor to circuit, waveform (c) is smoothed, and all harmonics in spectrum (d) are down by more than 45 dB.

different negative currents to the summing junction of a 741 operational amplifier. The table indicates how the counter and X-OR gates ensure that these currents are delivered in the proper sequence to produce the output waveform shown in Fig. 2. The wave is smoothed by the feedback capacitor in the op-amp circuit.

The photographs in Fig. 2 demonstrate the step-by-step generation of the sine wave and the smoothing effect of the filter capacitor, as well as the harmonic content of the output. Without the filtering, the 15th and 17th harmonics are only 25 decibels weaker than the fundamental output signal, but the capacitor adds a corner at about 600 Hz so that these harmonics are reduced to 45 dB below the signal. □

Timer IC stabilizes sawtooth generator

by Frank N. Cicchiello
Geometric Data Corp., Wayne, Pa.

A temperature-independent audio-frequency sawtooth generator that uses a 555 integrated-circuit time is shown on page 109. Its sawtooth output maintains linearity within 1%, and its output is available from a low-impedance source that is fully buffered from the timing circuitry.

The circuit is superior to the more conventional approach that develops a linear sawtooth by adding a con-

stant-current pump to charge the sawtooth-forming capacitor. Since V_{BE} of the constant-current transistor changes with temperature in a conventional circuit, a corresponding change in its current would cause a variation in frequency of the output sawtooth. No such change occurs in this 555 circuit.

Connecting pin 2 to pin 6 (trigger and threshold inputs respectively) of the 555 causes it to trigger itself and free-run as an astable multivibrator. Consider the circuit action after the IC's internal discharge transistor (pin 7), having dumped the charge on the sawtooth-forming capacitor C_1 via R_3, has become an open circuit and allows C_1 to recharge.

C_1 begins to charge through R_1, R_2, and R_3 toward the supply voltage V_{CC}. For all practical purposes, the change in voltage at the junction of R_2 and R_3 is equal to that at the top side of C_1. This voltage change is applied to the base of a Darlington-type emitter follower, Q_1. Since Q_1 has virtually unity gain, it couples this same change in voltage back to the top side of R_2. As a result, the voltage across R_2 remains essentially constant during C_1's charging cycle and so produces the same effect (linear-ramping) as a constant-current source feeding C_1.

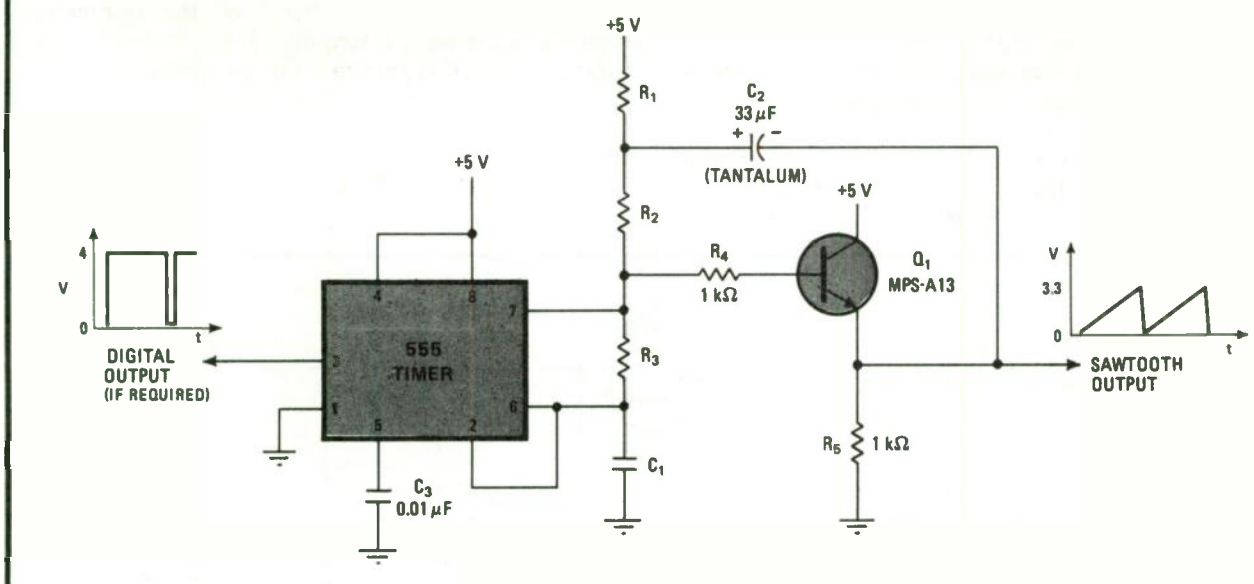
Once the linear sawtooth signal at pin 6 reaches a value of ⅔ V, the IC's internal comparator resets its flip-flops. The reset again activates the discharge transisto (pin 7), causing C_1 to dump through R_3; this actio causes a new trigger wave to be applied to pin 2, thu repeating the circuit operational cycle.

Resistor R_3 is required to slow down the negative-dis charge slope of the sawtooth wave form. Resistor R_4 is parasite suppression resistor for Q_1. C_3 is a bypass ca pacitor on the voltage-control (pin 5) input of the IC which is unused in this circuit.

The component and frequency relationships can b simply stated and easily implemented:

$R_1 = R_2$
R_2 is equal to or greater than 10 R_5
R_3C_1 is equal to or greater than 5×10^{-6} s
R_4 = 1 kilohm
R_5 is equal to or greater than 100 ohms
R_1C_2 is greater than 10 R_2C_1
$f = 1/C_1[0.75(R_1 + R_2) + 0.693\ R_3]$

As in the conventional exponential sawtooth gener ator circuit, the output frequency is independent o variations in supply voltage. Typical performance dat is shown in the table. □



FREQUENCY		R_3	R_1 & R_2	C_1
Computed	Measured			
54.2 kHz	60 kHz	5.1 kΩ	10 kΩ	1,000 pF
665 Hz	667 Hz	510 Ω	100 kΩ	0.01 μF
6.7 Hz	6.9 Hz	51 Ω	1 MΩ	0.1 μF

±5% TOLERANCE ON ALL COMPONENTS

Linear, buffered, and stable. Sawtooth voltage generator, developed for CRT sweep deflection, uses 555 astable multivibrator. Emitter-fol lower arrangement of the transistor maintains charging current to C_1 constant for linear ramps and provides buffered low-impedance output Temperature-induced changes of V_{BE} do not affect frequency. Table shows typical frequency characteristics; supply voltage can be raise for greater output without changing frequency. In addition to the sawtooth wave form, a digital output is also available from 555 as shown this signal may be useful for triggering a scope, for example, but it is not necessary for generating the sawtooth.

Triangular waves from 555 have adjustable symmetry

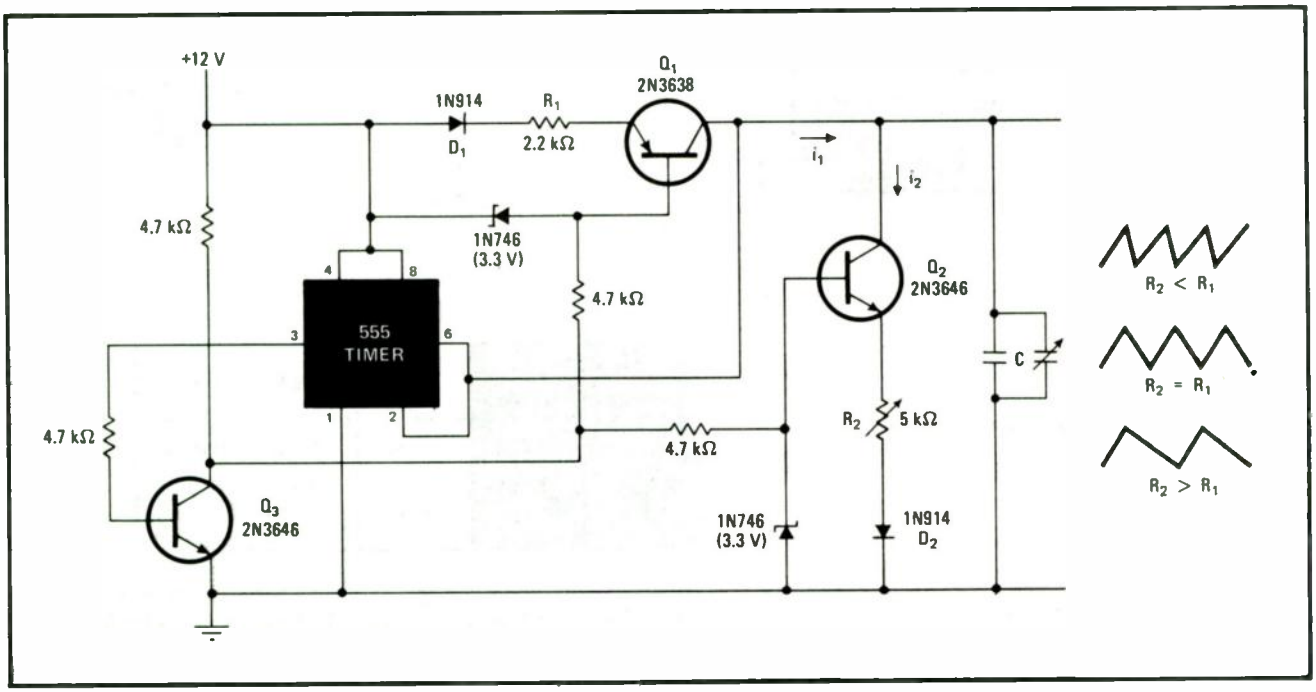
by Devlin M. Gualtieri
University of Pittsburgh, Pittsburgh, Pa.

The fixed-frequency triangular waveform so often required in pulse-duration modulators or sweep generators too often turns out costly to implement. Though operational-amplifier circuits can develop a triangular wave by integration of a square wave, the tips of the triangle become blunt at frequencies above 10 kilohertz unless expensive devices with high slewing rates are used. Also, though single-package voltage-controlled oscillators provide triangular output, they are not cost-effective for fixed-frequency applications, and most have high current drain. However, an inexpensive 555 timer and some transistors can generate triangular waves at frequencies up to about 100 kHz.

The circuit shown generates a triangular waveform by alternately charging and discharging a capacitor. The transistors Q_1 and Q_2 with their zeners act as a switched-current source and a switched-current sink that are activated by Q_3. When Q_3 is on so that its collector is low, the Q_1 current source is switched on, and a current i_1 charges capacitor C. The linear voltage ramp that appears across C corresponds to the charging law $dV/dt = i_1/C$.

Voltage V across the capacitor increases until it reaches a level that is two thirds of the supply voltage, which is the upper trip point of the 555 timer. The voltage at pin 3 of the timer then goes low, turning off Q_3. Since the collector of Q_3 is thus made high, the Q_1 current source is deactivated, and the Q_2 current sink is switched on. The capacitor is discharged by i_2 until the lower trip point of the 555 timer is reached, at one third of the supply voltage. At this point the 555 changes state and the cycle repeats. Thus the output voltage varies from 4 V to 8 V if the supply is 12 V.

Q_1 and Q_2 may be any high-gain pnp and npn transistors, such as 2N3638 and 2N3646. Q_3 may be any npn switching transistor, such as 2N3646. The forward voltage drops of D_1 and D_2 ensure turn-off of Q_1 and Q_2. Resistor R_2 is a symmetry adjustment, controlling the discharge rate of C by varying i_2. For the values shown, the frequency in hertz of the symmetrical triangular wave form is roughly 75/C, where C is in microfarads; thus, C determines the frequency. □



Ups and downs. Triangular waveform is generated across capacitor C by alternately charging and discharging through emitter-follower constant-current sources consisting of transistors Q_1 and Q_2 plus their zener diodes. Current sources are turned on and off by 555 timer.

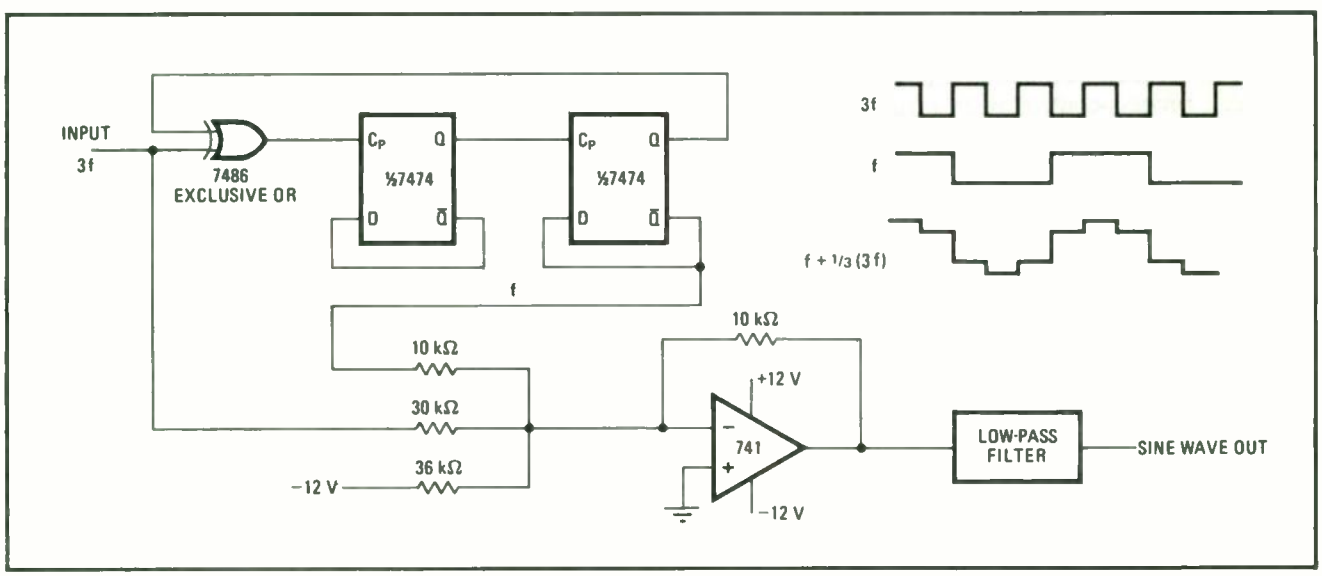
Frequency divider plus op amp approximates sine wave

by John Taylor,
NOAA, Boulder, Colo.

A group of digital and analog integrated circuits can be combined to create an audio tone from a digital pulse train. Ordinarily a single flip-flop can convert pulses into a symmetrical square wave. But for many applications, it is desirable to produce a closer approximation to a sine wave.

This can be done with the circuit shown here. The frequency divider accepts a square wave at a frequency of 3f, and produces a square wave at the required output frequency f. Use of an exclusive-OR gate at the clock input of the first flip-flop results in two advantages over a more conventional divide-by-3 circuit: (1) the output is symmetric, and (2) the input (3f) is 180° out of phase with the third harmonic of the output (f).

This phase relation is such that if f and 3f are summed together in the 741 op amp (with weighting factors of ⅓ and 1 respectively), the third harmonic of square wave f is canceled. This produces a stepped waveform which is a much better approximation to a sine wave at frequency f than a square wave. If a zero average sine value is desired, a dc offset can also be included in the summation. If an approximate sine wave is not good enough, the output of the op amp can be filtered by a simple low-pass filter, since the lowest harmonic to be rejected is five times the fundamental. □



Pulse to audio. An exclusive OR, two-stage frequency divider and op amp are used to sum the third harmonic and fundamental of a square wave, producing a stepped approximation to a sine wave that is easily filtered.

23. Instrument circuits

Voltage-to-current converter for process-control systems

by Harry L. Trietley, Jr.
Taylor Instrument Process Control Div., Sybron Corp., Rochester, N.Y.

To avoid damage to process-control instruments, such as controllers and chart recorders, the maximum value of the signal current that drives these devices must be limited. This signal current, which corresponds to a control signal voltage, can become too large if the control-signal voltage exceeds its normal range or if some other abnormal condition occurs.

Without requiring a series output resistance, the voltage-to-current converter in the diagram limits output current to between 24 and 40 milliamperes, a safe range for much process-control instrumentation. The circuit converts an input signal of 0 to 1 volt to a current of 4 to 20 mA for driving a load of 0 to 1,300 ohms.

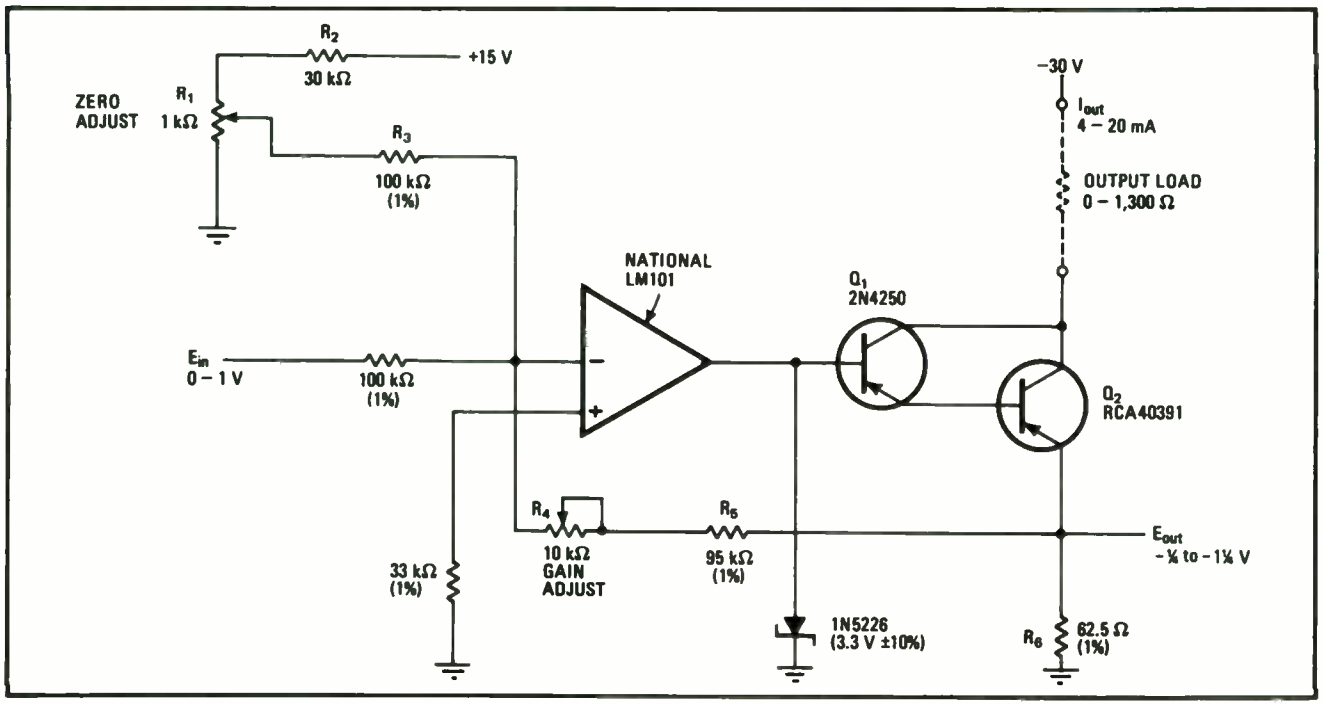
Under normal operating conditions, the zener diode does not conduct. The amplifier and transistors Q_1 and Q_2 perform as an operational amplifier, the output of which is at the emitter of transistor Q_2. With the resistance values shown, the circuit has a gain of 1. Resistors R_1, R_2, and R_3 form an offset zero adjustment, while resistor R_4 provides precision gain adjustment.

The output current, I_{OUT}, equals the sum of the currents in resistors R_5 and R_6, regardless of the size of the output load. Since resistor R_5 is much larger than resistor R_6, the output voltage (E_{OUT}), which ranges from ¼ to 1¼ V, produces a current of 4 to 20 mA.

Integrated op amps, such as the National Semiconductor LM101 used here, are internally limited to output currents of about 25 mA. When the converter's output reaches the zener's voltage, the zener will conduct, grounding the amplifier's output current and clamping the converter's output voltage to a nominal level of 3 V ±10%. The output voltage is actually limited to between 1.5 and 2.5 V because of the base-emitter voltage drops of transistors Q_1 and Q_2. The output current is then limited to a maximum value of between 24 and 40 mA.

If the value of resistor R_6 is lowered to 25 ohms, the output current range becomes 10 to 50 mA, with limiting occurring between 60 and 100 mA. Other outputs, gains, or current limits can also be realized. □

Instrument interface. Circuit converts control signal voltages to signal currents for driving process-control instruments, such as chart recorders. For the components values shown, this converter limits output current to between 24 and 40 milliamperes to protect the instruments from excessive driving currents due to out-of-range control voltages. The zener diode limits output voltage to 1.5–2.5 volts.



Data averager for panel meter operates from meter's clock

by George Mitchell and Richard D. Spencer
University of Illinois, Urbana, Ill.

In many scientific applications, measurements made with a digital voltmeter require time-averaging to reduce the measurement uncertainty of a noisy signal. A simple averaging circuit can be easily added to a digital panel meter for summing independent measurements so that the uncertainty of the data is reduced.

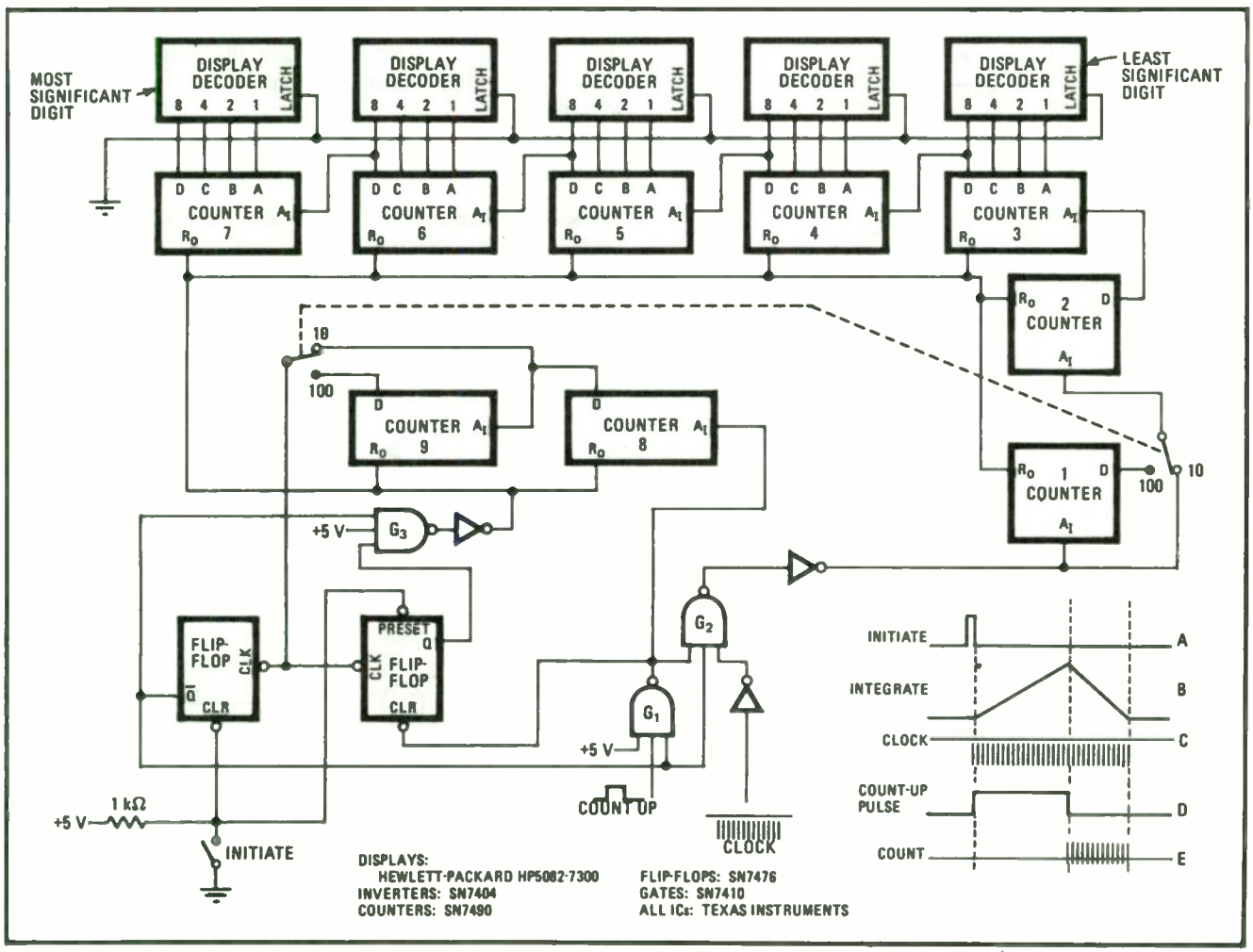
The averaging circuit shown here causes the DPM to sum 10 or 100 measurements (depending on switch position), thereby reducing data uncertainty by a factor of 3.2 or 10, respectively. Although this circuit is intended for an Electro-Numerics' model 305 4½-digit ratio panel meter, it can be readily adapted to any DPM that uses a dual-slope converter.

The circuit, which is activated with an initiate pulse (trace A in the figure), takes advantage of the clock pulse train (trace C) from the DPM's dual-slope converter. The clock train is transmitted during the integration period (trace B) of the analog signal and reference inputs. The count-up pulse (trace D) corresponds to the fixed integration time of the analog signal input.

NAND gates G_1 and G_2 use the count-up pulse to gate the clock output of the DPM's dual-slope converter so that the input to either decade counter 1 or 2 (trace E) is directly proportional to the ratio (in this case) of the analog inputs. As can be seen, counters 1 and 2 are scalers of 10 and 100, respectively, for the gated clock pulse train. Counters 3 through 7 form the decimal accumulator, and counters 8 and 9 are tally registers that inhibit averaging of data past the required number of samples (10 or 100).

The averaging circuitry is synchronized to the DPM's converter cycle by the two flip-flops and three NAND gates. Grounding the initiate line clears the tally registers and scalers, as well as the accumulator, and initiates the accumulation of a new average. The average, or scaled, output is displayed by light-emitting-diode readouts that have their own decoder/drivers. The binary-coded decimal output of the accumulator may also be used to transfer data directly to a printer or computer. □

Averaging out noise. Measurement uncertainty of noisy signals is reduced by time-averaging circuit for digital panel meter. The circuit, which runs from clock of DPM's dual-slope converter, sums 10 to 100 measurements, reducing data uncertainty by 3.2 or 10. Counters 1 and 2 are the scalers, counters 3 through 7 make up the accumulator, and counters 8 and 9 are the tally registers.



Capacitor corrects drift for analog data amplifier

by Charles Walton*
IBM Corp., Systems Development Division, San Jose, Calif.

Inserting a capacitor in the gain control feedback path of an analog data amplifier can provide automatic offset voltage drift correction. The drift voltage is stored on the capacitor and held to ±0.1 microvolt/°C.

The gain of the amplifier circuit (a), which is intended to operate in conjunction with a multiplexer, is selectable. Junction field-effect transistors are used to implement the gain control. Their gate voltage is provided by a resistor network that allows the gate voltage to track the signal voltage so that errors due to gate leakage current are eliminated.

Between multiplexing cycles, transistor Q_1 conducts, grounding the amplifier input, and transistor Q_2 also conducts, making amplifier gain equal to unity. As a result, the amplifier's dc offset voltage occurs at its output, as well as at its positive input and at the top of storage capacitor C. The other side of the capacitor may be grounded. Or, if resistor R_4 is relatively small compared to the sum of the other feedback resistors, R_1 through R_3, as is usually the case, then turning on transistor Q_5 effectively grounds capacitor C. The capacitor behaves as a battery during the ensuing amplifier cycle. Its value is not critical, but should be reasonably large.

To amplify input signal e_{x1}, transistor Q_{x1} is turned on, and one of the feedback ratios (β) is chosen by selecting transistor Q_3, Q_4, or Q_5. The feedback signal ($e_o\beta$) is added to the drift-corrected signal and amplified by the factor, $1/\beta$. For example, if input e_{x1} is zero and transistor Q_4 is selected for the desired gain, both amplifier inputs will be equal to the drift voltage and will be of the same polarity. The amplifier's output will then be essentially zero. In fact, even if the drift voltage is as substantial as 100 millivolts, the amplifier's output will still be kept within a few microvolts of zero by the circuit.

The primary source of drift error is temperature effects at the amplifier's input. Other sources are compo-

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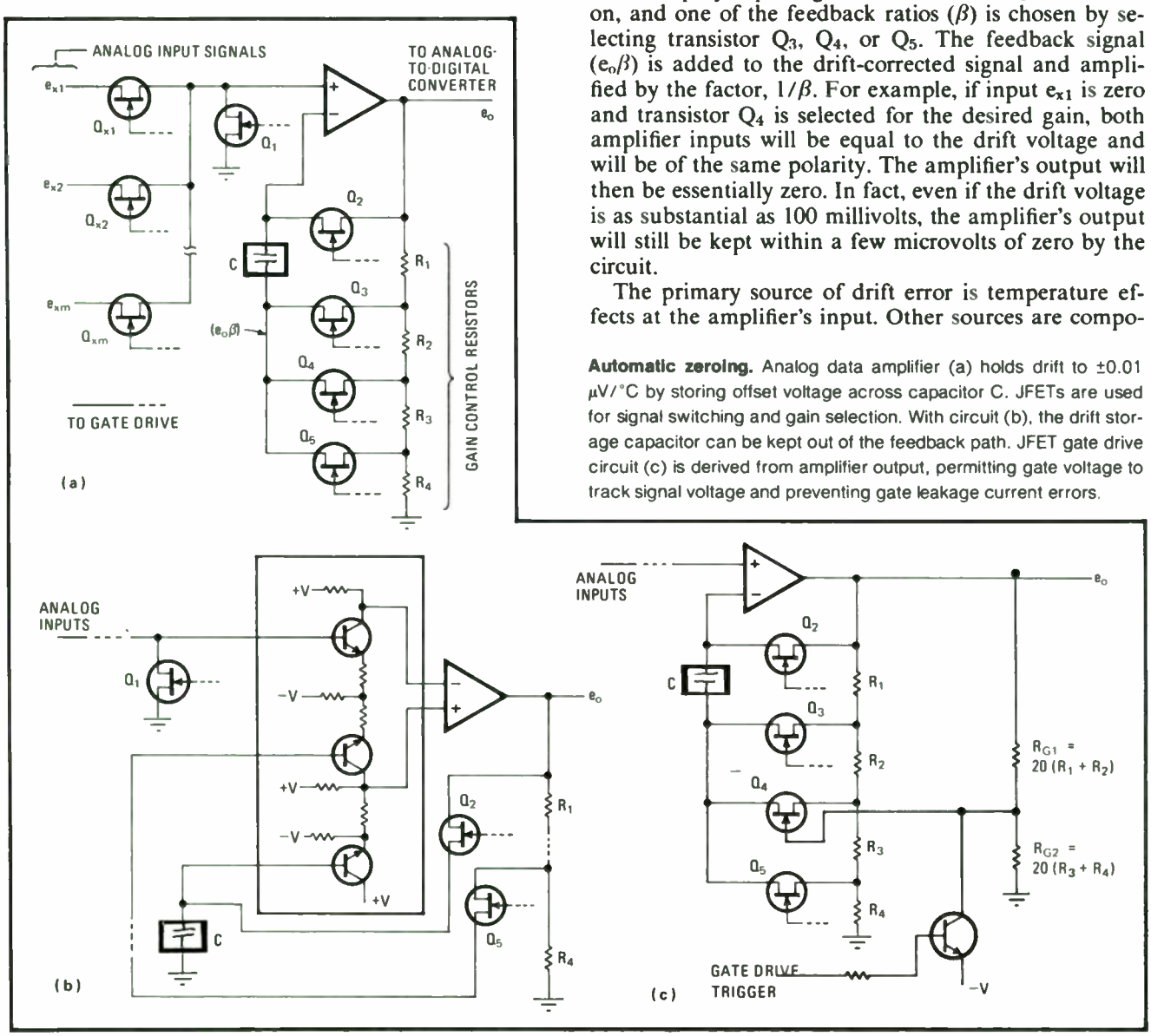


Automatic zeroing. Analog data amplifier (a) holds drift to ±0.01 μV/°C by storing offset voltage across capacitor C. JFETs are used for signal switching and gain selection. With circuit (b), the drift storage capacitor can be kept out of the feedback path. JFET gate drive circuit (c) is derived from amplifier output, permitting gate voltage to track signal voltage and preventing gate leakage current errors.

nent aging, power supply variations, and the offset of subsequent amplifier stages. But all these effects are slow compared to the amplification cycle time (200 microseconds, in this case). Therefore, the data system simply needs to adjust the stored capacitor voltage between amplification cycles or between a group of amplification cycles.

Placing bipolar transistors at the amplifier's input, as shown in (b), permits the correction capacitor to be kept out of the feedback path. (In most applications, this is only a minor advantage.) When transistors Q_1 and Q_2 are on, the amplifier places a voltage on capacitor C so that the next amplification cycle is automatically corrected for drift.

JFETs are used here for gain control, multiplexing, and zeroing, rather than MOSFETs, because they have more predictable control characteristics, need smaller switching voltages, and cost less. Possible errors due to JFET gate leakage currents can be avoided by utilizing the gate drive circuit of (c).

When a JFET is conducting, its gate voltage need only be within about 0.3 volt of its drain and source voltages. If the gate voltage is slightly less than this, there is a small increase (for an n-channel JFET) in the drain-source resistance. If the gate voltage is slightly higher the silicon-diode characteristic of the gate-source junction prevents any error-sized current from flowing.

The gate drive circuit shown meets these JFET gate voltage requirements by employing the amplifier output to drive the gates, thereby allowing the gate voltage to track the input signal. In the figure, the gate voltage for transistor Q_4 is obtained from the voltage divider formed by resistors R_{G1} and R_{G2}. These resistors do not have to have tolerances as tight as those of the feedback resistors (±5%, as against ±0.02%).

The high impedance of the gate drive resistors avoids loading the amplifier output. There is a pair of divider resistors for each value of gain. To turn off a gain control transistor, a bipolar transistor is turned on, holding that JFET's gate voltage sufficiently negative to keep it off for all signals. Junction gate leakage current is typically below 100 nanoamperes, minimizing the possibility of errors.

General-purpose JFETs can be used for the amplifier circuit—ones having a source-drain resistance of 50 to 200 ohms. □

Low-drift ICs form instrumentation amplifier

by K. C. Seino
Fermi National Accelerator Laboratory, Batavia, Ill.

Accurate measurements sometimes require use of high-quality differential amplifiers that have high input impedances at both the inverting and noninverting input terminals, as well as high common-mode rejection ratio at all values of voltage gain. These instrumentation amplifiers are available commercially in both modular and integrated-circuit versions, each of which has its own advantages and disadvantages.

This instrumentation amplifier was built from three low-drift op amps. The circuit, designed for a gain of 10, optimizes performance, cost, and size. Its performance matches that of the best modular instrumentation amplifiers. What's more, the low cost and convenient size are as advantageous as those of integrated instrumentation amplifiers for the desired performance. The entire circuit fits easily on a printed-circuit board in a limited area where it would be difficult to fit a modular amplifier. The cost of the ICs, which are the major components in the circuit, is less than $30.

The characteristics of three modular instrumentation amplifiers are shown in the table. The Burr-Brown 3620 is estimated, by means of a formula in its data sheet, to have a maximum input offset voltage drift of about ±3 microvolts/°C at gain of 10. Over a temperature change of 25°C, the total drift of ±75 μV represents an error of only 0.4% on a 20-mV signal. Balanced against this good performance, however, are a size of 2 by 2 by 0.4 inches and a price of $90.

Integrated-circuit instrumentation amplifiers, which

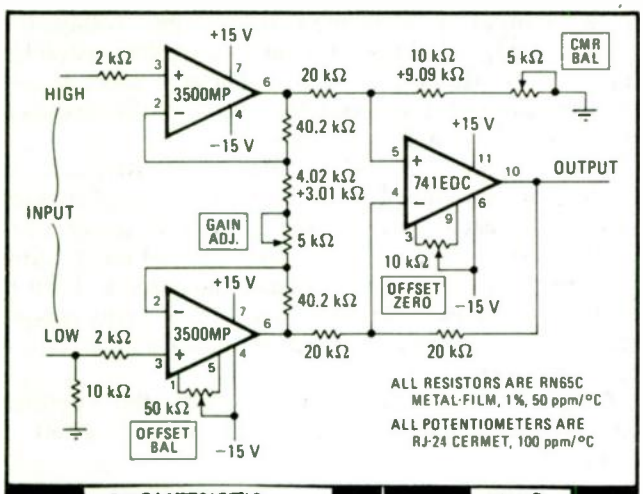
are considerably less expensive than the modular units, are available in metal cases or in 14-pin dual in-line packages. Their input impedances and common-mode rejection are good, as shown in the table. However, at low gain, their offset-voltage drift becomes significant and affects the accuracy when measuring millivolt signals. At a gain of 10, the drift in input-offset voltage of the Burr-Brown 3660K is estimated, by means of the equation in the data sheet, to be ±52 μV/°C. Therefore, a 25°C temperature change causes a voltage change of ±1.3 mV, or a 6.5% error on a 20-mV signal.

To avoid tradeoffs between performance, size, and cost, the possibility of building an instrumentation amplifier from low-drift operational amplifiers was examined. The input voltage was 20 mV, and a 200-mV output was required; therefore, the amplifier was designed for a voltage gain of 10. The circuit was designed around the Burr-Brown 3500MP matched pair and the Fairchild μA741E. As the diagram shows, four potentiometers can be adjusted to achieve optimum performance from this circuit.

The first potentiometer balances voltage offsets at the outputs of the 3500MP units. It is important to adjust the offset at one output to equal the offset at the other, rather than zeroing each one. The second pot is the over-all gain adjustment; it is set to give a voltage gain of 10. The third pot is the common-mode-rejection adjustment. The gain difference between the upper and lower paths for common-mode signals is set so that a maximum rejection can be obtained at the 741E stage.

The last potentiometer zeros the voltage offset at the final output. The gain of 10 was obtained in the matched-pair low-drift stage so that drift in the last stage would have a minimum effect in the over-all thermal behavior of the circuit.

Over a temperature change of 25°C, the input-offset voltage drifts only ±75 μV, which is less than 0.4% error on a 20-μV signal. Common-mode rejection is greater than 94 decibels at room temperature and greater than 70 dB at 50°C. □



CHARACTERISTIC	VALUE
Input-offset voltage:	
Value at 25°C	Adjusted to zero
Max. change with temp. (G = 10)*	± 2.6 μV/°C
Input impedance:	
Differential	10^7 Ω
Common-mode	5×10^9 Ω
Common-mode rejection:	
at ± 10 V dc, 25°C	≥94 dB
at ± 10 V dc, 50°C	≥70 dB
Cost of ICs	$28.40

*G = voltage gain

Instrumentation amplifier. Circuit with three ICs has high input impedances at both inverting and noninverting terminals, good common-mode rejection, and low offset-voltage drift. Gain is 10 and is adjustable. Four potentiometers are set for best performance.

CHARACTERISTICS OF MODULAR AND IC INSTRUMENTATION AMPLIFIERS

CHARACTERISTIC \ UNIT	MODULES			INTEGRATED CIRCUITS	
	Analog Devices 605K	Burr-Brown 3620J	Teledyne-Philbrick 4253-01	Analog Devices 520K	Burr-Brown 3660K
Input-offset voltage:					
Max. value at 25°C	–	± (0.2 + 0.5/G) mV	± 0.5 mV	–	± (1 + 300/G) mV
Max. change with temp. (G = 1)*	± 75 μV/°C	± 12 μV/°C	± 1 μV/°C	± 0.5 mV/°C	± 0.5 mV/°C
Max. change with temp. (G = 1,000)	± 1 μV/°C	± 2 μV/°C	± 2 μV/°C	± 5 μV/°C	± 2.5 μV/°C
Input-bias current:					
Max. value at 25°C	100 nA	± 25 nA	−10 pA	± 40 nA	200 nA
Max. change with temp.	−1 nA/°C	± 0.5 nA/°C	1 pA/°C	± 0.2 nA/°C	−2 nA/°C
Input-offset current:					
Max. value at 25°C	± 100 nA	–	–	± 20 nA	± 20 nA
Max. change with temp.	± 1 nA/°C	–	–	–	± 0.2 nA/°C
Input impedance:					
Differential	10^9 Ω	3×10^8 Ω	10^{13} Ω	2×10^9 Ω	$(2 \times 10^{10}/G)$ Ω
Common-mode	10^9 Ω	10^9 Ω	10^{13} Ω	2×10^9 Ω	2×10^{10} Ω
Common-mode rejection:					
at G = 1	70 dB	–	80 dB	65 dB	70 dB
at G = 10	–	74 dB	80 dB	–	–
at G = 1,000	94 dB	100 dB	120 dB	95 dB	110 dB
Package size (inches)	1.5 x 1.5 x 0.4	2 x 2 x 0.4	2 x 2 x 0.4	14-pin DIL package	TO-100 package

*G ≡ voltage gain

Integrated multiplier simplifies wattmeter design

by Donald DeKold
Santa Fe Community College, Gainesville, Fla.

A broadband wattmeter can be built simply and inexpensively with an IC multiplier as the heart of a power-to-voltage transducer circuit that has an output voltage that is directly proportional to the instantaneous load power. The circuit's frequency response extends from dc to several kilohertz. When the output is applied to a simple meter movement or a digital voltmeter, the circuit makes a complete handy power meter.

The maximum load power that the circuit can handle while retaining its proportional output is 2 kilovolt-amperes; this power may be real or reactive. The maximum load voltage, $e_L(t)$, can be 400 volts, while the maximum load current, $i_L(t)$, can be 5 A. The transducer's output voltage is given by:

$$e_{out} = Ke_L(t)i_L(t)$$

where, for the design being shown here, K = 0.005 V/VA. Output voltage e_{out} can vary from −10 to +10 V, depending on what the instantaneous polarities and magnitudes of the load voltage and load current are.

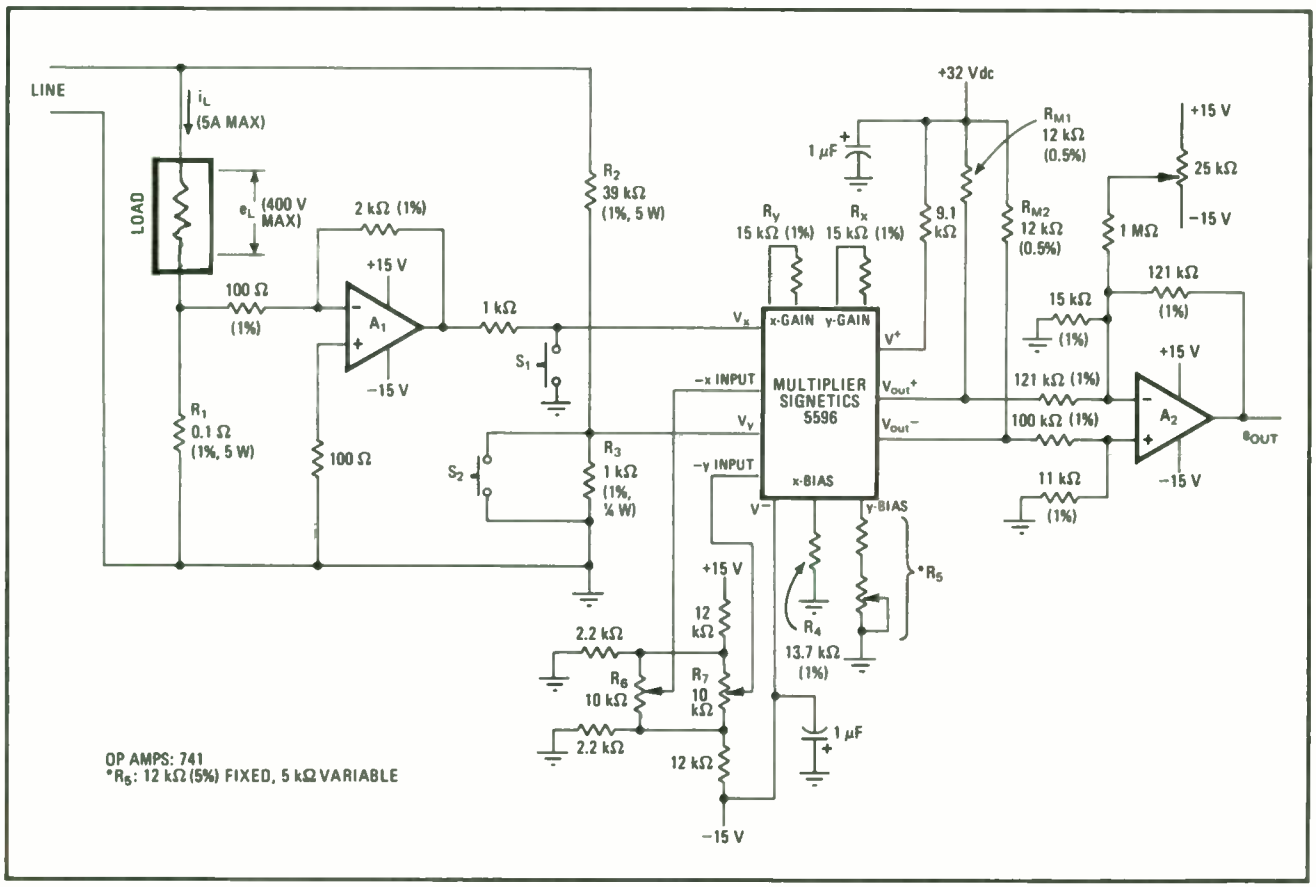
The circuit's voltage and current ranges can be modified easily by simply changing two resistors—resistor R_1 for the current and resistor R_2 for the voltage. Changing the value of these range resistors also alters the value of constant K, thereby producing a wattmeter of whatever range is desired.

Load current is sensed by a current-shunt element, resistor R_1, and is amplified by a factor of −20 as it passes through operational amplifier A_1. The output from this op amp is applied to the V_x input of the multiplier. In this case, input V_x must not exceed ±10 V, restricting load current $i_L(t)$ to a peak value of ±5 A.

Load voltage, which is derived from the voltage divider set up by resistors R_2 and R_3, is applied to the V_y input of the multiplier. This multiplier input is also limited to ±10 V, which holds load voltage to ±400 V.

The output of the multiplier is a differential voltage (from the V_{out}^+ and V_{out}^- terminals) that is proportional to the product of inputs V_x and V_y. This output depends on a number of factors: the magnitude and polarity of inputs V_x and V_y, the values of gain resistors R_x and R_y, the values of multiplier load resistors R_{M1} and R_{M2}, and the bias currents established by resistors R_4 and R_5 and the supply voltages. For the component values shown, the multiplier's output is approximately $V_xV_y/10$. (The proportionality constant may be varied somewhat by trimming resistor R_5.)

Measuring power. IC multiplier produces output that is proportional to the power being dissipated in the load. The circuit is a power-to-voltage transducer that can be used to measure power levels as high as 2 kilovolt-amperes by simply connecting its output to a meter movement or a digital voltmeter. Since all offset voltages are trimmed to zero, fairly accurate measurements can be made over the full output range.



The differential multiplier output is applied to operational amplifier A_2, which acts as a level shifter and develops a single-ended output voltage. The signal gain through this stage is −1. Resistor R_6 permits A_2's offset voltage to be adjusted to within a few millivolts of zero.

In general, when ac power is developed in the load to which the circuit is connected, the load voltage is:

$$e_L(t) = E_{pk} \sin\omega t$$

And the load current becomes:

$$i_L(t) = I_{pk} \sin(\omega t + \phi)$$

so that the power in the load can be expressed as:

$$p(t) = [E_{pk}I_{pk} \cos\phi/2] - [(E_{pk}I_{pk}/2) \cos(2\omega t + \phi)]$$

In this last equation, a sinusoidal time-varying component is present that is twice the frequency of the load current or load voltage and that has an average value of zero. The dc term in the power expression represents the average real power dissipated in the load.

The circuit's output voltage reflects these analytical relationships—it has both a dc component and an ac component of twice the input frequency. When e_{out} is applied to an ordinary average-reading dc meter, the response of the meter is directly proportional to the average real power dissipated in the load.

The transducer circuit is fairly accurate, since the dc offset voltages produced by the multiplier and the level shifter are eliminated. Switches S_1 and S_2 apply a 0-V dc input to the multiplier's V_x and V_y inputs, so that resistors R_6 and R_7 can be used to trim the offset of each of these inputs to zero. (This is most easily accomplished while sensing an ac power signal with an oscilloscope at the output; each voltage input is trimmed for an ac null at the output.)

Precision components, as indicated in the diagram, should be used for best results. It is also essential that the supply voltage be stable since the offset trim voltages are derived from these sources.

Simultaneous readings made with this circuit will deviate nominally from each other by only 1% for the upper 75% of the 2-kVA output range. □

24. Integrators

Two-amplifier integrator extends timing performance

by Nabil R. Bechai
Leigh Controls Ltd., Ottawa, Ont., Canada

A simple integrator normally consists of a single operational amplifier and an RC network for setting up the desired time constant. Although uncomplicated, this approach can be troublesome if either a very small or a very large time constant is needed.

The integrator in the figure, however, makes it easy to obtain either short or long timing periods because the values of the timing components are scaled by a straight resistance ratio. The integrator's output voltage is given by:

$$V_{out} = -\frac{R_1}{RCR_2}\int V_{in}\,dt$$

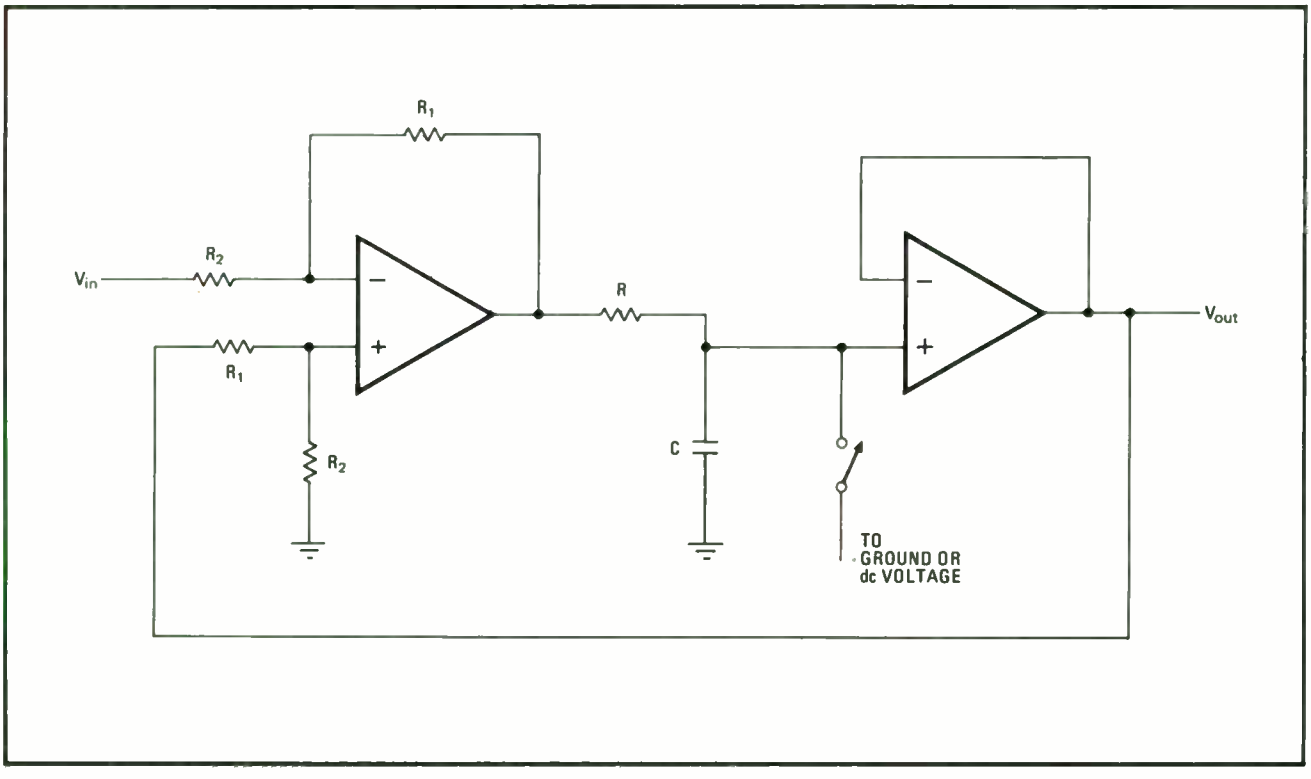
and its time constant becomes $(R_2/R_1)RC$. The circuit provides very good linearity when precision resistors having a tolerance of ±0.1% are used for resistors R_1 and R_2.

Although a second op amp is needed to build the integrator, the circuit offers some additional advantages. For example, it permits initial conditions to be established easily. One of the capacitor's leads goes to ground, and if one end of the switch is connected either to ground or to some dc voltage, the capacitor's initial condition can be set up as either zero or otherwise by simply closing the switch.

Furthermore, when the switch is activated, the integrator's output is not shorted, and the circuit's output op amp operates as a voltage-follower. In a conventional integrator, the initial-condition switch is generally placed across the capacitor, which is in the op amp's feedback loop. With the switch closed, then, the output of a conventional integrator is shorted to the op amp's inverting input.

The integration period of the two-amplifier circuit described here can be as short as 1 nanosecond or as long as 1,000 seconds. The bandwidth of the integrator depends on which op amps are used. For high-frequency operation, National's type LM318 op amp and RCA's type CA3100 op amp are recommended. □

Broad timing range. An extra op amp permits this integrator's time constant to be scaled by resistors R_1 and R_2 so that an exceptionally short or long timing period can be obtained easily. The time constant is $(R_2/R_1)RC$, rather than the usual RC alone. The desired initial condition for the capacitor is established by simply closing the switch, which can go to ground (for zero initial charge) or to some dc voltage.



Inverting transistor boosts integrator's time constant

by Roland J. Turner
General Electric Space Division, King of Prussia, Pa.

Designers of low-frequency analog instrumentation will welcome an integrator that can provide a large time constant with a low-value capacitor. The accompanying circuit does just that. Its integration time constant is the RC product multiplied by the current gain of a superbeta Darlington transistor. Moreover, this circuit has high input impedance, which is an absolute necessity in such applications as an integrator driven by a peak detector. And it offers a third characteristic that is desirable for any integrator—its transient response is critically damped, which prevents integration from being seriously disturbed by noise or transients.

The key feature of this integrator is the inclusion of an inverting transistor in the feedback loop to the input of an operational amplifier. Because the transistor provides inversion, the incoming signal can be applied to the high-impedance noninverting-input terminal of the operational amplifier. The process of inversion, i.e., degenerative feedback through the integrating capacitor, provides critical damping. The value of the capacitor is effectively multiplied by the current-gain factor of the transistor.

The circuit diagram shows that the 741 op amp is connected as an amplifier, with the incoming signal applied through 10-kilohm resistor R to the high-impedance noninverting terminal. To prevent high-frequency oscillations and to limit low-frequency noise, part of the output from the 741 is fed back to the inverting input through a parallel resistor-capacitor combination. The op amp drives a 2N4974 pnp superbeta Darlington transistor. The transistor is biased by the voltage drops across the two zener diodes and across the emitter-to-base junction, which produce a dc base drive of 2 microamperes through the 50-kilohm resistor. The 4.7-kilohm resistor is not critical—it merely limits the current through the 1N573A zener to about 1 milliampere.

Current gain in the transistor, β, is 5,000, so the dc collector current is 10 milliamperes. This current, flowing through the 1-kilohm resistor, centers the voltage level for integrating capacitor C at -7 volts so that the integrator can handle both positive and negative inputs.

When signal e_i is applied at the input to this circuit through resistor R, the output signal of reverse polarity, e_o, is fed back through integrating capacitor C to the noninverting terminal of the op amp. The over-all transfer function of the circuit is

$$A(s) = e_o(s)/e_i(s) = -1/R\beta Cs$$

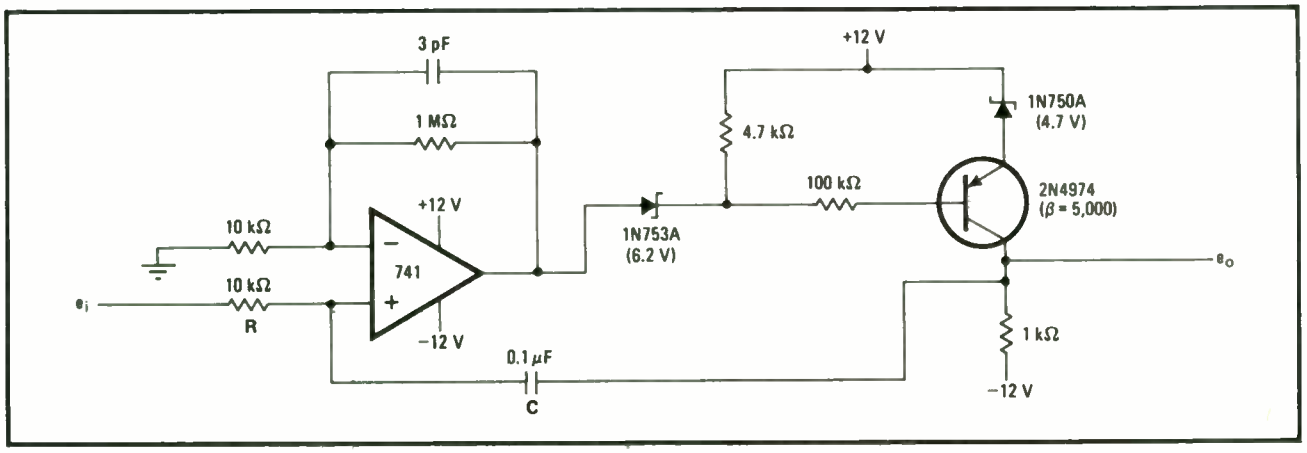
A conventional op-amp integrator using the same R and C would have a transfer function of -1/RCs. Thus, to provide the same transfer function, the integrator that includes a transistor can use a capacitor that is smaller by the factor β. Or, if the capacitor value is held fixed, the transistor provides an integrating time constant that is larger by the factor β.

The circuit shown here has an effective time constant

$$\tau = \beta RC$$
$$= 5{,}000 \times 10{,}000 \text{ ohms} \times 0.1 \times 10^{-6} \text{ F}$$
$$= 5 \text{ seconds}$$

To achieve this time constant, a conventional op-amp integrator would require a 500-microfarad capacitor.

This integrator circuit can function effectively at any frequency that the operational amplifier can handle, and at any signal level that does not saturate the transistor. Any of several operational amplifiers can be used; the 741 was chosen here for its good compensation. Likewise, many transistor types can be used. The 2N4974 was chosen for its availability and high β. □



Integrator. Operational amplifier plus transistor makes integrator with large time constant, despite small size of integrating capacitor C. The circuit shown here has an effective time constant βRC of 5 seconds. Feeding the noninverting input terminal of the operational amplifier gives high input impedance, and degenerative feedback through the transistor provides critically damped transient response.

Miller-effect integrators act as signal separator

by Dale Hileman
Sphygmetrics Inc., Woodland Hills, Calif.

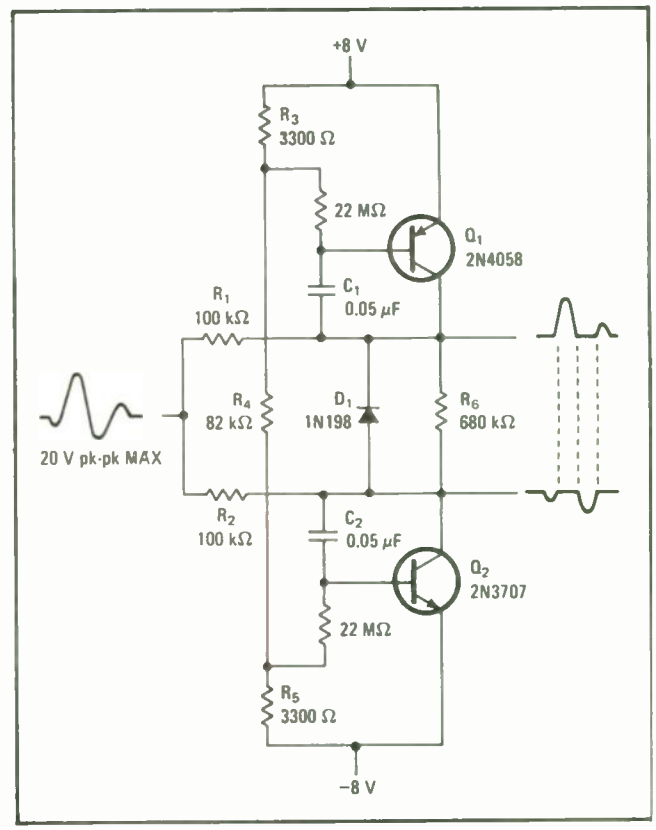
Complementary Miller-effect integrators are better than biased diodes for rectifying a signal and separating it into its positive and negative components. The diodes require enormous integrating capacitors when a dc level in the base line must be retained, and big capacitors commonly have leakage or polarization problems.

In the signal separator shown, each of the Miller-effect integrator stages serves as a half-wave rectifier. Together with two small 0.05-microfarad integrating capacitors, C_1 and C_2, they simulate a large effective capacitance that maintains the dc level of the signal's base-line potential.

Negative-going signal excursions cause transistor Q_1 to conduct, clamping the output to the base-line potential. Positive-going excursions, on the other hand, cut off transistor Q_1 and pass directly to the output. The operation of complementary transistor Q_2, which is the other integrator-rectifier stage, is the same as that of transistor Q_1, but signal polarity is reversed. A high-impedance load should be used to avoid an excessive voltage drop across either resistor R_1 or resistor R_2.

The voltage divider set up by resistors R_3, R_4, and R_5 holds the base voltages of both transistors close to their conduction threshold so that output signal transitions can be maintained near the base-line potential. Resistor R_6 acts as a collector load for both Q_1 and Q_2 to minimize the effect of their collector-emitter leakage current. Diode D_1 is included to minimize the effect of changing ambient temperature on this leakage current.

Signal separation is best at low frequencies, within the audio range and down to about 3 hertz. Even lower operating frequencies can be achieved by increasing the values of capacitors C_1 and C_2, but the rate of base-line integration becomes slower. □



Separating the ups and the downs. Signal separator employs complementary Miller-effect integrators to keep capacitor values low. The circuit permits input dc base-line potential to be retained so that it also is present at the output. Transistor Q_1 prevents negative-going inputs from reaching the output, while transistor Q_2 stops positive-going inputs. The circuit's load impedance should be kept high.

Precision integrator resets as it samples

by Dennis J. Knowlton
University of Wyoming, Laramie, Wyo.

A circuit that continuously samples the integral of an input and resets itself achieves an accuracy of within 0.1%. Other integrators with this tight an accuracy can be expensive and complicated because they do not integrate continuously but rather require some time to sample and reset.

The integrator shown uses two sample-and-hold circuits—while one is sampling, the other is holding the previous integral value. Reset is also continuous—the previous value of the integral is fed back so that the circuit is continuously reset for the full integration time period. In this way, integration precision is determined primarily by hardware and not by technique. Adding an offset adjustment to each of the operational amplifiers permits accuracy to be improved by at least an order of magnitude.

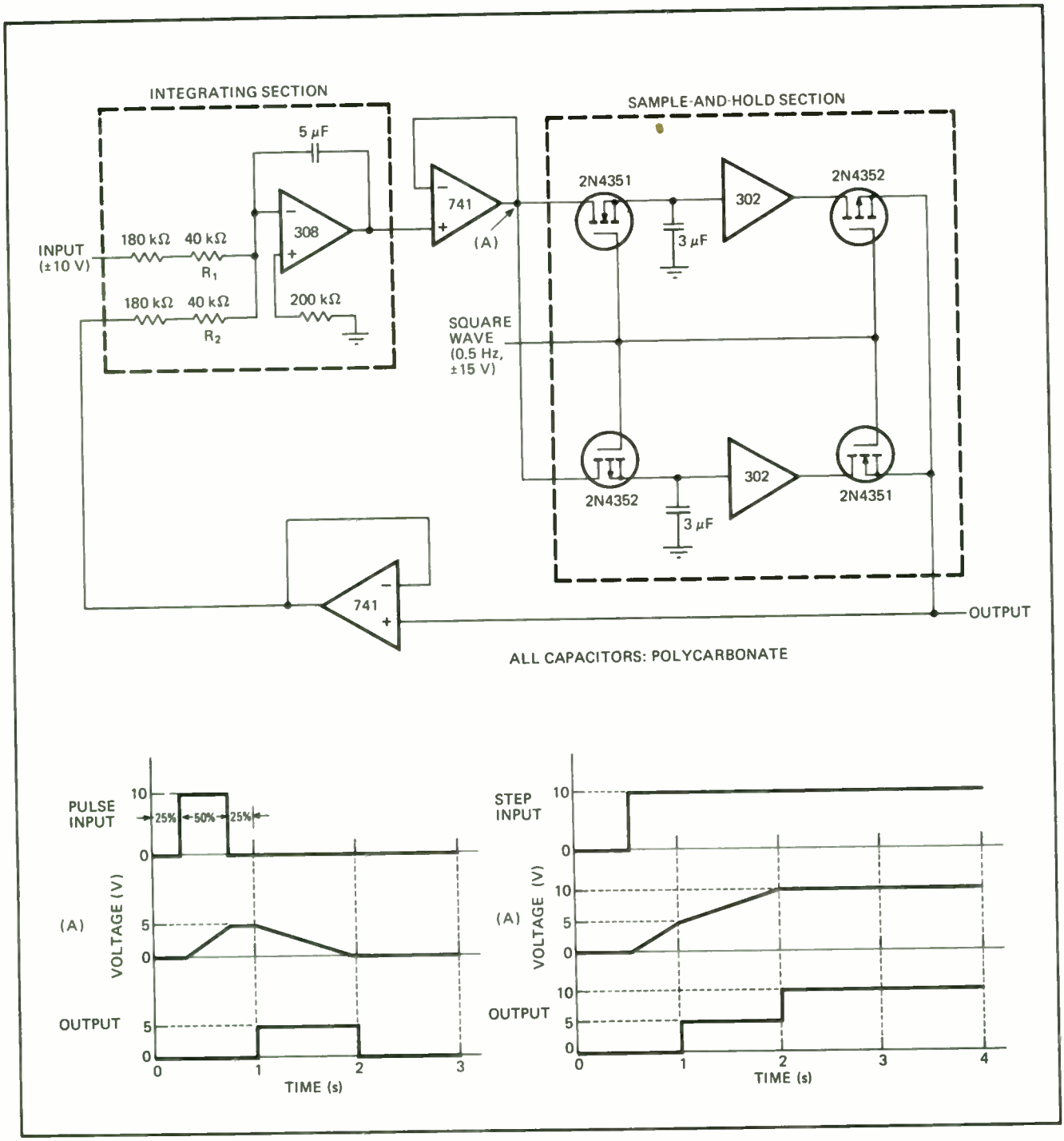
The integrating section is a simple integrator, composed of an op amp having a low input bias current and a feedback capacitor. The sample-and-hold section contains complementary MOSFETs. One portion of this section holds the integral, while the other follows (samples) the output from the integrating section. When the MOSFETs are switched, these roles are interchanged. The

741-type op amps are used in voltage-follower configurations to isolate the integrating section from the sample-and-hold section.

The integrator is a true feedback system. If the integration period is 1 second, the integral formed during a 1-second period is fed back to the input during the following 1-second period to reset the integrator. Meanwhile, new data is being integrated. The output, then, is the sum of the new integrated data, plus the old data that has been integrated back to zero, which simply yields the integral of the new data. Two timing diagrams show the circuit's response to a pulse input and to a step input.

Calibration procedure for the integrator is straightforward. After the feedback circuit is unhooked, resistor R_1 is adjusted to obtain the desired slope from the integrating section (for example, 1 volt out per second per volt in). The feedback circuit is then connected again, and resistor R_2 is adjusted so that there is no overshoot or undershoot to a step input. □

Precision integration. Simple integrator can provide accuracy within 0.1% because it continuously integrates input. Output from integrating section is sampled by one sample-and-hold circuit, while the other holds previous integral and uses it to reset integrator. Complementary MOSFETs do the switching. Sample-hold roles reverse every integration period.



25. Inverters

Single bipolar transistor inverts pulses on command

By Dale Hileman
Sphygmetrics Inc., Woodland Hills, Calif.

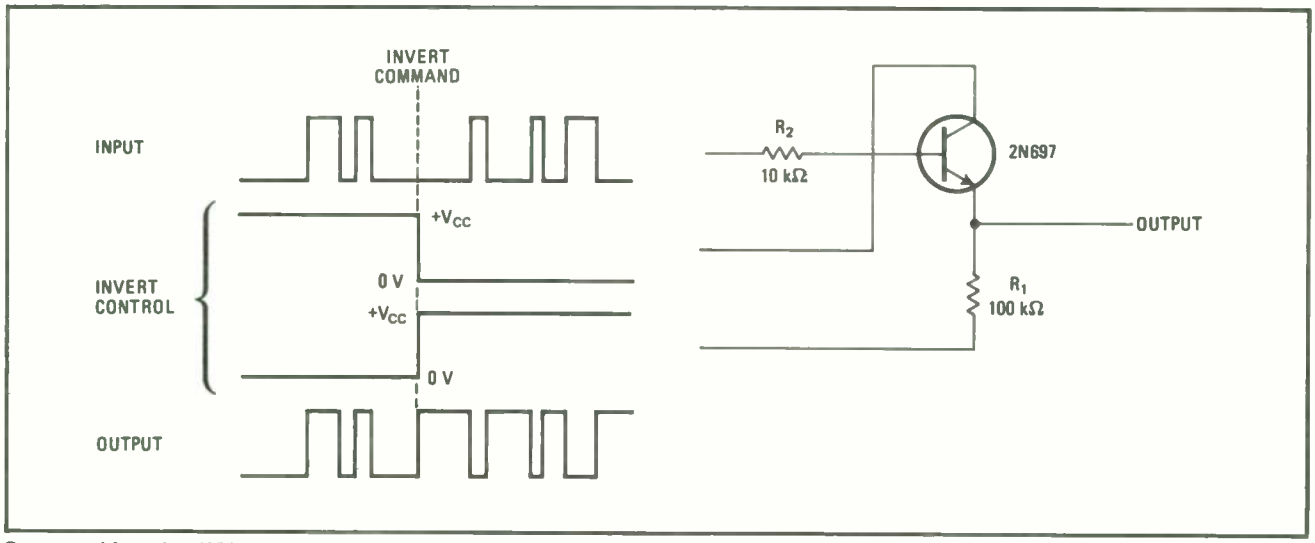
An ordinary bipolar transistor can be made to function as a command inverter—that is, it will pass a pulse signal without modifying the pulse, but it can invert the signal upon command. The command is a simple reversal of the polarity of the supply voltage.

To do this usually requires several gates, involving perhaps dozens of parts and interconnections. The command inverter shown here, however, requires only three parts: a single bipolar transistor and two ordinary resistors.

The key to this circuit's operation is that the role of a transistor's emitter and collector can be interchanged if the supply polarity is reversed. When the polarity of the invert control signal is normal, the transistor operates as an emitter-follower, so that the polarity of the output pulse train is the same as the polarity of the input pulse train.

The invert command reverses the polarity of the supply voltage, making the transistor's collector act as an emitter and its emitter act as a collector. Now the circuit becomes an inverting amplifier, with resistor R_1 serving as the collector load resistor. Under this condition, resistor R_2 simply limits the transistor base current to a safe value.

Any general-purpose npn or pnp bipolar transistor may be used in the circuit, and the precision of neither resistor R_1 nor resistor R_2 is critical. This command inverter will work with virtually any value of supply voltage and any input pulse level that the transistor will tolerate. □



Command inverter. With normal supply polarity, this bipolar transistor operates as an emitter-follower, passing the input pulse train to the output without modifying it. But when the supply polarity is reversed, the transistor's emitter acts as its collector, and the transistor's collector acts as its emitter. Now the polarity of the input pulse train will be inverted at the transistor's output.

Digital command inverts signal

by Craig J. Hartley
Baylor College of Medicine, Houston, Texas

Many digital designs require voltage-controlled signal inversion. The circuit shown here accepts bipolar inputs with amplitudes up to ±7 volts and has a gain of either +1 or −1, depending on the logic level at the control terminal. A TTL-logic level of 1 produces a gain of +1 (no inversion of the input signal), and a logic level of 0 produces a gain of −1 (signal inversion). The circuit uses a 741 operational amplifier and two transistors.

When the control logic is high, both Q_1 and Q_2 are turned off, and the operational amplifier becomes a voltage follower. The input signal E_i is present at both input terminals and at the output terminal of the op amp, so no current flows through resistors R_1, R_2, or R_3. Therefore the gain in this logic-low mode is independent of the values of the resistors and is given by

$$E_o/E_i = +1$$

When the control logic is low, both Q_1 and Q_2 are saturated, so the noninverting terminal of the op amp is grounded and the input signal is applied only to the inverting terminal. Therefore the gain is

$$E_o/E_i = -R_2/R_1$$

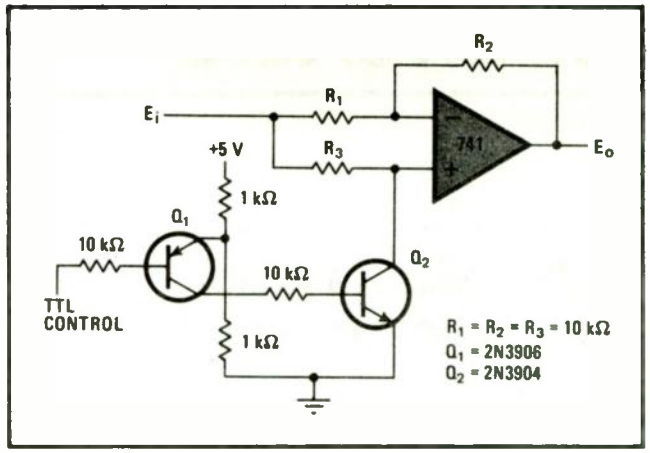
In this circuit R_1 and R_2 are equal, and therefore the gain in this logic-low mode is

$$E_o/E_i = -1$$

In this mode of operation, there is an offset proportional to the saturation voltage of Q_2:

$$V_{offset} = V_{sat}(1 + R_2/R_1) = 0.02\ V$$

Because this circuit is intended to handle bipolar input signals, Q_2 must be driven by a high-impedance source such as Q_1, so that Q_2 is turned off by having its base open-circuited, rather than by having its base grounded. If the base of Q_2 were grounded, negative input signals to the circuit would forward-bias the base-to-collector junction and distort the output signal. With the circuit shown here, the negative input swing is limited by the base-to-emitter breakdown voltage of Q_2 (i.e., 6 to 10 V), while the positive input swing is limited only by the op amp saturation voltage. □



Voltage-controlled inverter. Circuit transmits or inverts input signal, depending on logic level at control terminal. Logic 1 produces a gain of +1 (no inversion), and logic 0 produces gain of −1 (inversion). Maximum signal swing is ±7 volts. Offset is about 0.02 volt.

Transistor array cuts cost of algebraic inversion

by Pavel Ghelfan
M.G. Electronics Ltd., Rehovot, Israel

Monolithic operators for algebraic inversion are convenient, but a reliable algebraic inverter can be built quite simply and at less cost from an integrated five-transistor array and two operational amplifiers. The circuit first converts the input signal to a logarithmic equivalent and then takes the antilog of this.

The output voltage (V_L) of amplifier A_1 is a logarithmic function of the input current (I_{in}) and the current (I_R) that the transistor array sinks at pin 13:

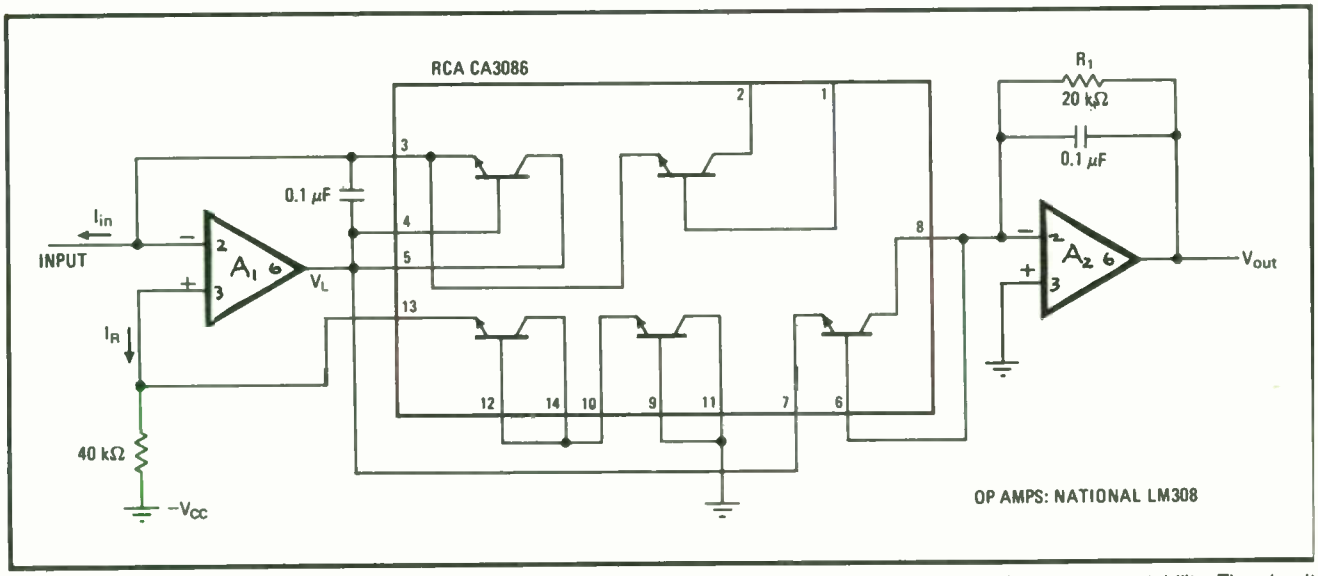
$$V_L = \frac{2kT}{q} ln\left(\frac{I_R}{I_{ES}}\right) - \frac{kT}{q} ln\left(\frac{I_{in}}{I_{ES}}\right) = \frac{kT}{q} ln\left(\frac{I_R^2}{I_{in} I_{ES}}\right)$$

where I_{ES} is the emitter saturation current (with collector shorted to base) of the array's transistors, k is Boltzman's constant, q is the charge of an electron, and T is absolute temperature. The antilogarithmic operation is performed by amplifier A_2. The circuit's output signal can be expressed as:

$$V_{out} = I_{ES} R_1 \exp(qV_L/kT) = I_R^2 R_1 / I_{in}$$

Trimming the value of constant current I_{IR} will adjust the numerator of this equation so that the output voltage of the circuit is brought to the desired value and kept there.

This inversion operator maintains good stability over a 50°C temperature range, as well as over three decades of signal amplitude variation. Its amplitude range can be significantly broadened by using low-bias-current operational amplifiers. □



Taking the reciprocal. Algebraic inverter employs IC transistor array to keep costs low and to provide good temperature stability. The circuit converts the input signal to a logarithmic voltage and then takes the antilogarithm of this voltage to develop the output signal. The output, of course, is indirectly proportional to the input and can be brought to the desired value by adjusting resistor R_1.

26. Limiters

Broadband cutoff limiter is phase-transparent

by Roland J. Turner
RCA Missile & Surface Radar Division, Moorestown, N.J.

When information is transmitted in the phase domain, the video or intermediate-frequency processor in a radar or communications system frequently requires a limiter circuit that does not alter the zero crossings of the input signal.

By using current cutoff limiting, a broadband phase-transparent (zero phase-shift) limiter can be built that maintains input zero crossings within 14 picoseconds, while providing a gain of 20 decibels over its linear range. This limiter, which operates from dc to 30 megahertz, can improve receiver sensitivity, allowing smaller targets to be resolved in a radar system or, in a communications system, reducing level- and frequency-dependent phase noise so that phase-detection thresholds can be lowered.

The limiter circuit uses microwave transistors that have a unity-gain crossover frequency (f_T) of greater than 1 gigahertz. The bandwidths of the transistor stages making up the limiter can then exceed 500 MHz to yield the limiter's over-all wideband performance by using conventional microstrip techniques.

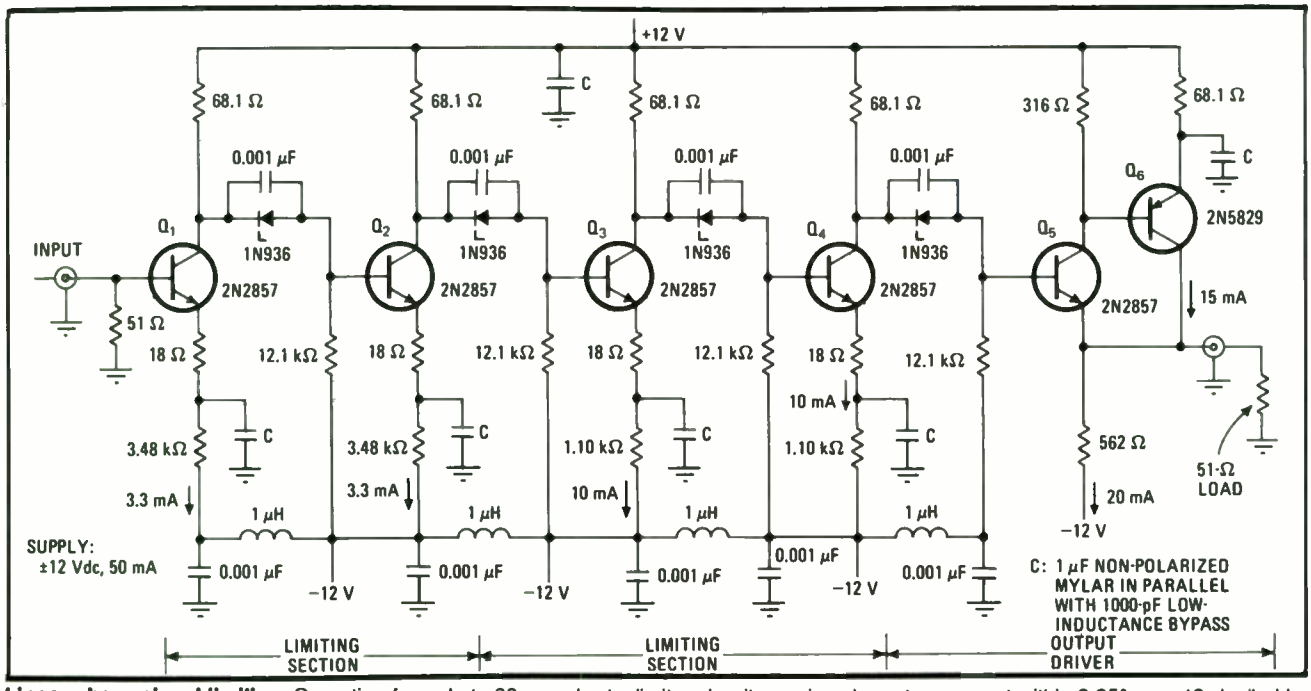
Exceptional signal control is realized by driving the transistors into their cutoff regions to achieve limiting action. Transistor cutoff parameters are more controllable and more clearly defined than transistor saturation parameters. And with cutoff signal limiting, the transistors look like high impedances to low load impedances, thereby achieving fast limiting action with controlled passive elements.

Transistors Q_1 through Q_4 perform the limiting function, while transistors Q_5 and Q_6 operate as a unity-gain output driver. There are two limiting sections, one consisting of Q_1 and Q_2, and the other of Q_3 and Q_4. Two transistor stages, then, form each limiting section.

For one polarity of the input signal, one transistor stage operates as a low-gain broadband amplifier, while the other limits the section's output by performing as a cutoff isolation amplifier. During the opposite polarity of the input signal, the transistor stages reverse roles. Each limiting section supplies a gain of 3.3. The output level of each section is determined by its quiescent operating point.

This limiting scheme provides extremely low carrier output phase shift for the full dynamic range of the input signal. Over a 40-dB input range, from 100 millivolts peak-to-peak to 10 volts pk-pk, the limiter circuit is phase-transparent within 0.25°. For example, the output is 1.2 V pk-pk for a 120-mV input. For frequencies up to 20 MHz, the output impedance of the driver section is less than 5 ohms.

From dc to 20 MHz, the time displacement of adjacent zero crossings of the output waveform are within 14 picoseconds of the period established by the input zero crossings. In the phase domain, this means that the phase of a 20-MHz input will be shifted less than 0.1° at the output, making the limiter phase-transparent for all practical purposes. □



Linear-phase signal limiting. Operating from dc to 30 megahertz, limiter circuit remains phase-transparent within 0.25° over 40-decibel input dynamic range. Each limiting section contains two transistor stages. Depending on input signal polarity, one stage is low-gain broadband amplifier, while the other acts as cutoff isolation amplifier. Optimum usage of transistor cutoff parameters achieves desired limiting action.

Linear signal limiting with feedback multiplier

by R.J. Karwoski
Raytheon Co., Equipment division, Sudbury, Mass

A signal can be linearly compressed or limited over a wide dynamic range by using a four-quadrant analog multiplier as a feedback element. Particularly useful for audio applications, this linear limiting technique does away with the signal distortion that occurs with nonlinear methods. Also, the linear limiter does not require the careful calibration and many trial-and-error adjustments needed for a nonlinear limiter.

The control section of the linear limiter consists of three operational amplifiers and a multiplier. Op amp A_1 is the throughput amplifier with local feedback through resistors R_F, R_1, and R_2. When R_F is shorted, the control circuitry is bypassed, and the circuit becomes a linear voltage-follower:

$$e_o = e_i(1 + R_F/[R_1R_2/(R_1 + R_2)])$$

The fundamental feedback equation for the limiter is based on amplifier A_1:

$$e_o = A_o e_i/(1 + A_o\beta)$$

where gain A_o is determined by A_1's local feedback arrangement of R_F and R_1 in parallel with R_2. Feedback factor β depends on the control section, whose operating function resembles the basic feedback equation. The relationship between multiplier input e_Y and multiplier input e_X becomes:

$$e_Y = e_X/(1 + e_X)$$

For small values of e_X, this equation degenerates to:

$$e_Y = e_X$$

which is a linear function representing a 1:1 compression ratio between e_o and e_i. For large values of e_X, the function becomes asymptotically limiting:

$$e_Y = e_X/e_X = 1$$

Over-all limiter transfer function can be written as:

$$\frac{e_o}{e_i} = \frac{1 + R_F/[R_1R_2/(R_1 + R_2)]}{1 + 410\,R_F(e_i)_{pk}/R_2}$$

Multiplier output $e_Xe_Y/10$ and the product of gains of amplifiers A_2, A_3, and A_4 are represented by the factor $410(e_i)_{pk}$, where $(e_i)_{pk}$ is the peak input signal amplitude. Resistor R_F controls both circuit gain and compression. However, for any single value of e_i, the limiter can be set to provide a gain of unity, regardless of R_F's resistance and how much or how little limiting is needed. Additional over-all gain adjustments are then unnecessary, even if the compression ratio must be changed.

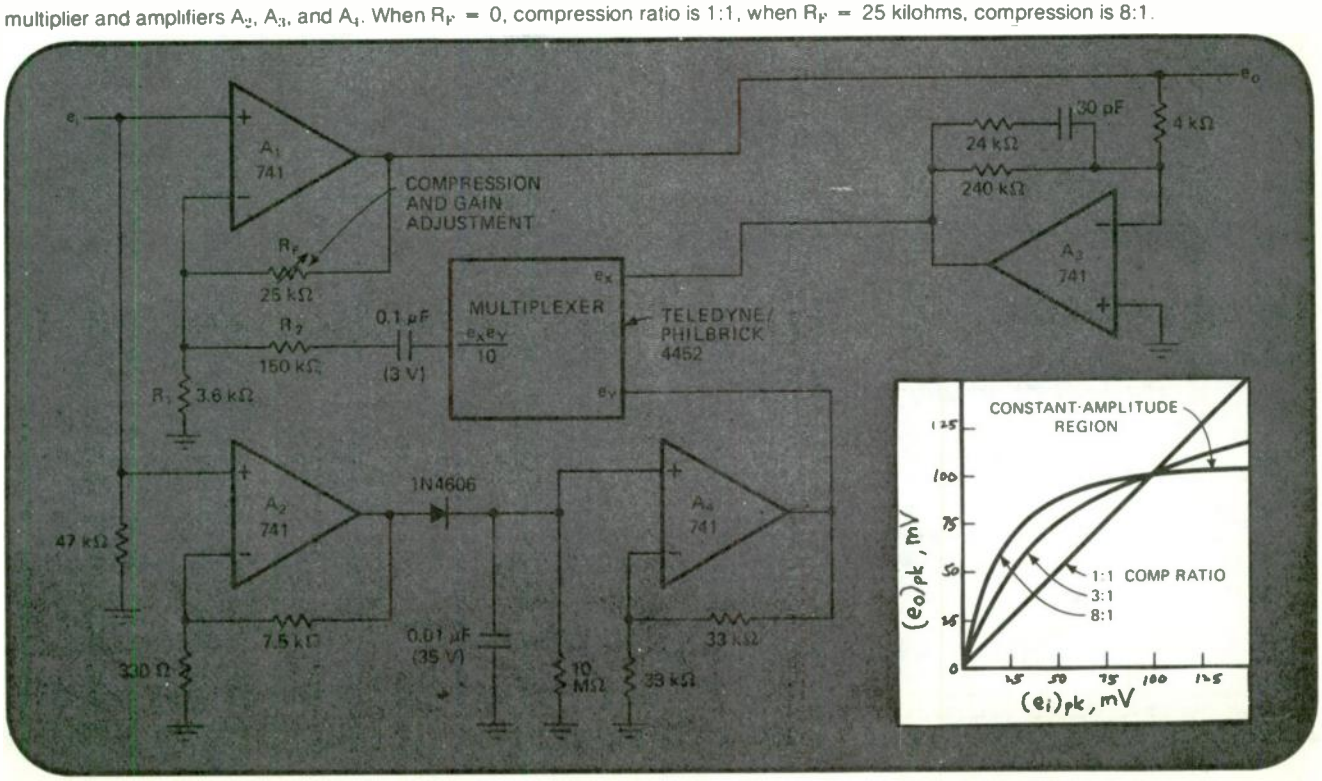
With a 100-millivolt input, the circuit illustrated supplies a 100-mV output, no matter what the setting of R_F. For any value of R_F, resistor R_1 is selected to keep:

$$1 + R_F/[R_1R_2/(R_1 + R_2)] = 1 + 410R_F(100\text{mV})/R_2$$

Circuit compression ratio can be varied by changing the value of R_F, but circuit gain remains unity for $e_i = e_o = 100$ mV.

The performance curves show the limiter's transfer function for three compression ratios with circuit unity-gain point at 100 mV—1:1 (no compression, $R_F = 0$), 8:1 (maximum compression, $R_F = 25$ kilohms), and 3:1 (midrange compression).

Variable linear limiter. Compression ratio can be varied by adjusting resistor R_F without changing circuit gain—limiter's unity-gain point remains $e_i = e_o = 100$ millivolts. Amplifier A_1 is controlled by local feedback through resistors R_F, R_1, and R_2 and by additional feedback from multiplier and amplifiers A_2, A_3, and A_4. When $R_F = 0$, compression ratio is 1:1, when $R_F = 25$ kilohms, compression is 8:1.



27. Logic circuits

Unclocked logic element makes quick decisions

by Leslie K. Torok
University of Toronto, Toronto, Ont., Canada

A new kind of logic element can make logic decisions without requiring a clock for synchronization. Called Jade, this asynchronous decision element can operate at speeds as high as clocked logic blocks, offers easy debugging, and allows sequential logic systems to be mechanized directly from flow charts. Moreover, Jade will operate in clocked as well as unclocked systems.

A control signal, DO, functions much like the clock in synchronous logic, while input signal X represents the logic condition that must be decided and acted upon. The Jade element has two states—a quiescent state when signal DO is logic 0 and a decision state when DO is logic 1. There are four possible outputs: XTRUE (X is true), $\overline{\text{XTRUE}}$ (not XTRUE), XFALSE (X is false), and $\overline{\text{XFALSE}}$ (not XFALSE).

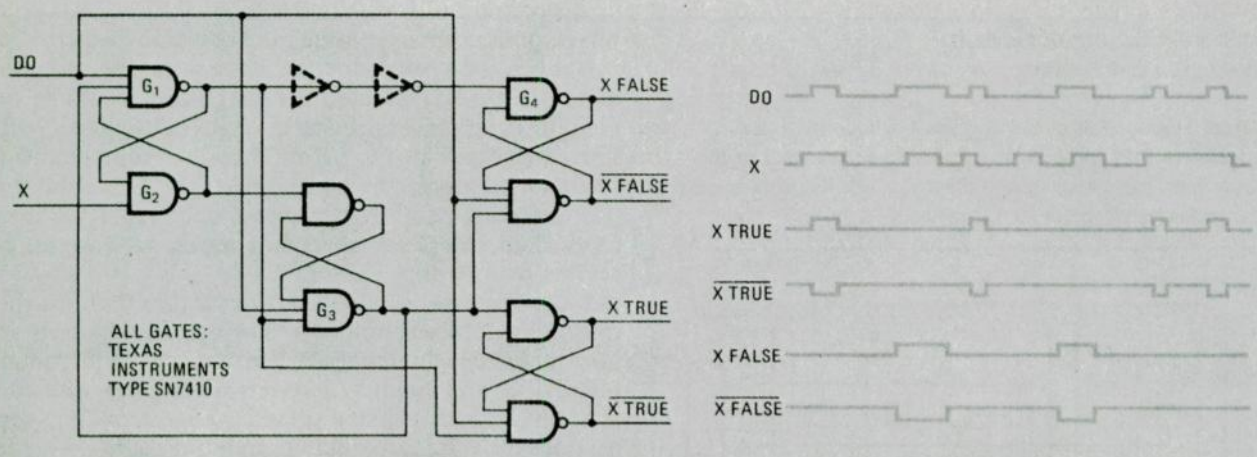
When the Jade is in its quiescent state (DO = 0), XTRUE = XFALSE = 0 and $\overline{\text{XTRUE}}$ = $\overline{\text{XFALSE}}$ = 1. For the decision state (DO = 1), Jade makes an exclusive and singular decision at the rising edge of signal DO — XTRUE = 1 and $\overline{\text{XTRUE}}$ = 0 if X = 1, or XFALSE = 1 and $\overline{\text{XFALSE}}$ = 0 if X = 0. The output decision then activates the appropriate task logic.

As long as DO = 1, further changes in X do not affect the output. Returning DO to logic 0 clears the decision, causing Jade to assume its quiescent state. It should be noted that XTRUE = XFALSE only in the quiescent state. For the decision state, XTRUE = $\overline{\text{XFALSE}}$ and $\overline{\text{XTRUE}}$ = XFALSE, since the outputs are exclusive. Those outputs that are not selected remain quiescent.

As X drops to logic 0 and DO rises, a spike may appear at the output of gate G_1 when the propagation delay of gate G_2 to a logic 1 is less than the propagation delay of gate G_3 to a logic 0. If the spike is wider than the minimum hold time of gate G_4, a double decision is made. To prevent this, two inverters can be placed between G_1 and G_4 to integrate the spike.

Jade can sort decisions at speeds of at least 10 megahertz, with signals X and DO having pulse widths of about 30 nanoseconds. □

Decisions, decisions. Asynchronous decision element named Jade uses control signal DO instead of clock to gate information signal X. When DO is logic 0, circuit is in quiescent state; when DO is logic 1, circuit is in decision state and provides single exclusive output out of four possibilities. Inverters can be added to avoid switching spike that causes erroneous double decision. Truth table shows logic characteristic.



INPUT X	DECISION STATE, DO = 1				QUIESCENT STATE, DO = 0			
	X FALSE	$\overline{\text{X FALSE}}$	X TRUE	$\overline{\text{X TRUE}}$	X FALSE	$\overline{\text{X FALSE}}$	X TRUE	$\overline{\text{X TRUE}}$
0	1	0	0	1	0	1	0	1
1	0	1	1	0	0	1	0	1

Simplifying sum-correction logic for adding two BCD numbers

by Robert D. Guyton
Mississippi State University, Mississippi State, Miss.

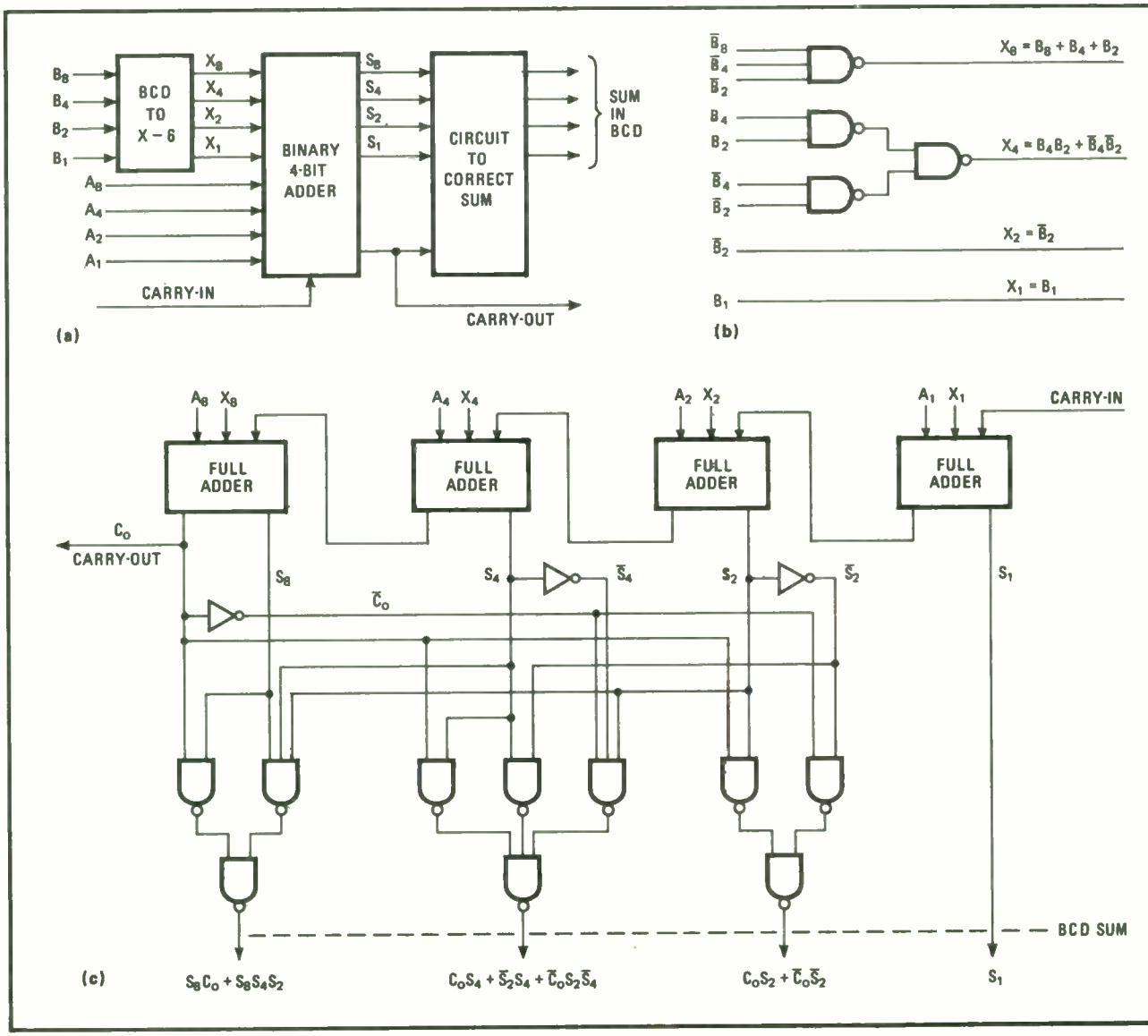
To add two numbers in binary-coded decimal form, much less logic hardware is needed if one of the numbers is converted to the excess-6 binary code before the addition is done. The other number remains unchanged.

The block diagram of (a) outlines the approach. One BCD input is converted to the excess-6 code by a second-level logic circuit, which is drawn in (b). This translated number and the unchanged BCD number are then added by a 4-bit binary adder. The resulting output carry is correct, but the sum must still be corrected—and can be corrected by a simple second-level logic circuit rather than a multilevel type of logic circuit based on half and full adders.

The BCD-to-excess-6 translator circuit needs four NAND gates and three inverter gates. The rest of the over-all addition circuit is shown in (c): the four-bit binary adder requires four full adders, while the sum correction circuitry requires 10 NAND gates and three inverter gates.

The complete excess-6 addition circuit, therefore, consists of 14 NAND gates, six inverter gates, and four full adders. As against an addition circuit based on excess-3 code conversion, that's a savings of six NAND gates, three inverter gates, one full adder, and two half adders. □

Conserving logic hardware. The circuit for adding two binary-coded-decimal numbers can be implemented with fewer devices by changing one of the BCD numbers to the excess-6 code format. When this conversion is done, simple logic gates can be used to perform the necessary sum correction. The figure shows the circuit's block diagram (a), the excess-6 code translator (b), and the complete circuit (c).



Circuit adds BCD numbers faster with less hardware

by Dharma P. Agrawal
Federal Polytechnic Institute of Lausanne, Switzerland

To add two binary-coded decimal numbers, at least four full adders are needed, not to mention the gates and inverters that correct the sums from each adder and generate the decimal carry-out. But this extra logic hardware can be simplified, as has already been shown ["Simplifying sum-correction logic for adding two BCD numbers," by Robert D. Guyton: *Electronics*, May 30, 1974, p. 108], and the new approach proposed here economizes on hardware and improves speed still further.

The circuit in the accompanying diagram uses a neat dodge to reduce the number of logic elements required to add the two BCD numbers $A_8A_4A_2A_1$ and $B_8B_4B_2B_1$. The dodge is to obtain the decimal carry-out, C_0, from the uncorrected sums S_2, S_4, and S_8, and the uncorrected carry C_{16} first, and only then to use C_0 to obtain the corrected sums S_1', S_2', S_4', and S_8'.

The boolean expression for the decimal carry-out can be written as

$$C_0 = C_{16} + S_8S_4 + S_8S_2$$

The circuit schematic shows how to obtain this value for C_0 by using just three NAND gates and one inverter.

The truth table for the corrected sums S_8', S_4', S_2', and S_1' as functions of C_0, S_8, S_4, S_2, and S_1 can be prepared, and their boolean expressions can be obtained as

$$S_8' = \bar{C}_0S_8$$

$$S_4' = S_4S_2 + \bar{C}_0S_4$$

or $$= S_4S_2 + \bar{S}_8S_4$$

$$S_2' = C_0\bar{S}_2 + \bar{C}_0S_2$$

or $$= C_0\bar{S}_2 + \bar{S}_8S_2$$

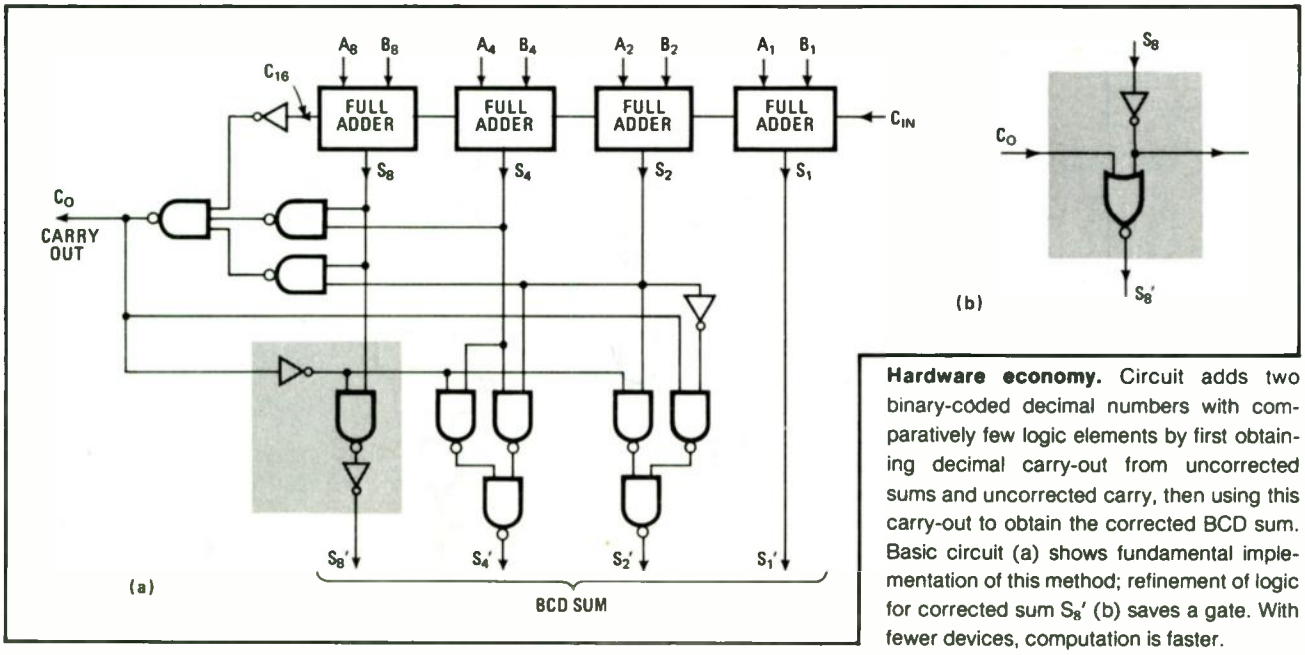
and $$S_1' = S_1$$

The circuit diagram clearly indicates the hardware accomplishment of each of these corrected sums. Note that the portion of (a) that is inside the shaded box can be replaced by the arrangement (b) to produce S_8' with one less gate and implement the alternative expressions for S_4' and S_2'.

The numbers in the accompanying table demonstrate how effectively this BCD adder reduces parts count and time delay, compared with some earlier circuits. □

COMPARISON OF BCD ADDERS

	Excess-3 adder	Guyton's adder	Proposed adder (a) shown here	Proposed adder (a), partially replaced by (b)
Number of full adders	5	4	4	4
Number of half adders	2	–	–	–
Number of 3-input NAND gates	20	4	1	1
Number of 2-input NAND gates		10	9	8
Number of 2-input NOR gates	–	–	–	1
Number of inverters	9	6	4	3
Time delay in terms of number of:				
Full adders	5	4	4	4
Half adders	2	–	–	–
Gates	?	6	5	4



Hardware economy. Circuit adds two binary-coded decimal numbers with comparatively few logic elements by first obtaining decimal carry-out from uncorrected sums and uncorrected carry, then using this carry-out to obtain the corrected BCD sum. Basic circuit (a) shows fundamental implementation of this method; refinement of logic for corrected sum S_8' (b) saves a gate. With fewer devices, computation is faster.

Common-gate, common-base circuits shift voltage levels

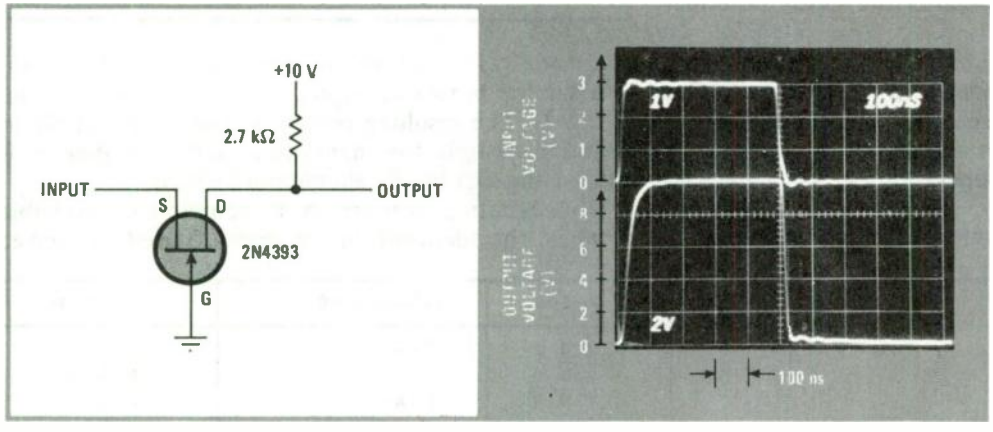
by Peter J. Bunge
Atomic Energy of Canada Ltd., Chalk River, Ontario

The voltage-shifting interface needed between incompatible logic systems can be quite straightforward—just a field-effect transistor in a common-gate circuit or a bipolar transistor in a common-base circuit. Both circuits are fast, uncomplicated, and economical in both parts cost and power drain.

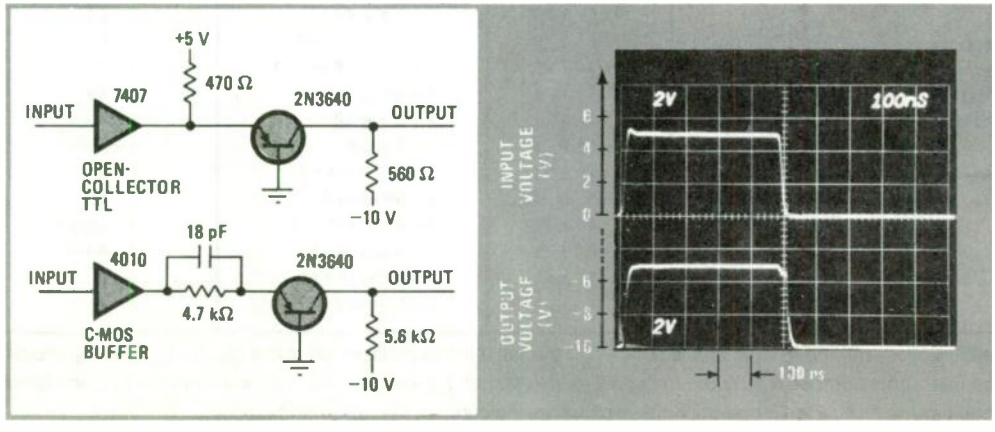
The common-gate FET circuit shown in Fig. 1 can couple the active outputs from any logic family to a voltage level higher than the V_{CC} of the logic—an impossibility with pullup resistor interfacing or complementary-metal-oxide-semiconductor buffer (4009, 4010) interfacing. It uses much less power than open-collector transistor-transistor-logic interfacing, especially when only one signal is involved, and it is much faster than some commercial level shifters (e.g. 100 nanoseconds versus 900 ns for the Solitron CM410AE). For the 2N4393 FET shown, the input range is 3 to 40 volts while the output range is 0 to 40 V (determined by the pinch-off and breakdown voltages of the device.)

The common-gate circuit provides only positive output voltages. A typical application is in interfacing an n-MOS random-access memory, which has 0-V and 3-V output levels, to C-MOS circuitry. Interfacing is necessary in this case because the 3-V level is just at the operating threshold of C-MOS when it is operating from a 5-V supply.

Common-base transistor circuits are used to interface positive voltage levels to negative-referenced logic. Figure 2 shows arrangements for translating 0-V or +5-V TTL or C-MOS levels to −10 V or −5 V. These methods are simple, require little power, and can be used with either active outputs or open-collector outputs, as shown. □



1. Level translator. A field-effect transistor in the common-gate configuration can provide output voltages that are higher than the supply voltage of the driving logic. Here the FET voltage-shifter accepts input levels of 0 or 3 V and delivers outputs of 0 or 10 V. The fast transitions and short delays that are demonstrated in the oscilloscope photo are achieved by minimizing the load capacitance.



2. Signal polarity inversion. Common-base level translator interfaces positive voltages to negative-referenced logic. Circuits here accept levels of 0 or 5 V and deliver outputs of −10 or −5 V. Waveforms shown are for circuit driven by open-collector TTL. Speed is sacrificed to conserve power in the circuit driven by a C-MOS buffer. The 18-pF speed-up capacitor charges input capacitance of transistor.

IC logic units simplify binary number conversion

by Harvey F. Hoffman
Norden Division, United Aircraft Corp., Norwalk, Conn.

A variety of digital arithmetic processing applications require one arithmetic notation to be converted to another. Six of the most widely used conversions can be accomplished easily with a pair of medium-scale integrated circuits called arithmetic logic units. The table lists these six conversions and their associated rules.

The function chart for an arithmetic logic unit is given in Fig. 1. As an example of how to wire the ICs, consider circuit (a) in Fig. 2 for converting an 8-bit number in two's-complement notation to a number in signed-binary notation. The number to be converted is N, and the converted number is P. The eighth bit (N_7, P_7) is the sign bit, and the least significant bit is the first number bit (N_0, P_0).

The function-select inputs are $S_0 = 0$, $S_1 = S_2 = S_3 = 1$, and the mode (M) input controls the sign bit. The arithmetic function (when $M = 0$) that may be performed is A plus (A OR $\overline{B}$) with no carry (C_n) input to the first unit. (A and B are the input numbers.) The logic operation (when $M = 1$) for these same function-select inputs is A OR B, no matter the state of the first unit's carry input.

If number A is set to zero and the carry-in term is set to one, then to arithmetic operation ($M = 0$) is $\overline{B}$ plus 1, which is the binary representation of a negative number in two's-complement notation. With number A again set to zero, the logic operation ($M = 1$) gives an output of B.

Therefore, if the inverse of the sign bit is applied to the mode (M) input, the A inputs are held at zero and the number in two's-complement form is applied to the B inputs. The resulting output is then in signed binary notation. If only the magnitude of the number is required, the sign bit, P_7, should not be used.

This notation conversion is completely reversible. That is, the identical circuit may be used to convert

ARITHMETIC-NOTATION CONVERSION RULES

From signed binary to two's complement:
- If sign bit is negative, complement each number bit and add 1 to result.
- If sign bit is positive, output number equals input number.

From two's complement to signed binary:
- If sign bit is negative, complement each number bit and add 1 to result.
- If sign bit is positive, output number equals input number.

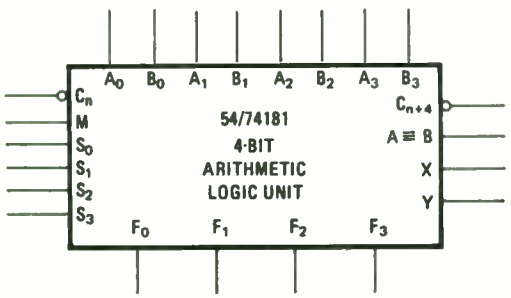
From signed binary to one's complement:
- If sign bit is negative, complement each number bit.
- If sign bit is positive, output number equals input number.

From one's complement to signed binary:
- If sign bit is negative, complement each number bit.
- If sign bit is positive, output number equals input number.

From two's complement to one's complement:
- If sign bit is negative, subtract 1 from number.
- If sign bit is positive, output number equals input number.

From one's complement to two's complement:
- If sign bit is negative, add 1 to number.
- If sign bit is positive, output number equals input number.

Notes:
- The sign bit is the most significant bit.
- A logic 1 in the sign bit location represents a negative number.
- A logic 0 in the sign bit location represents a positive number.

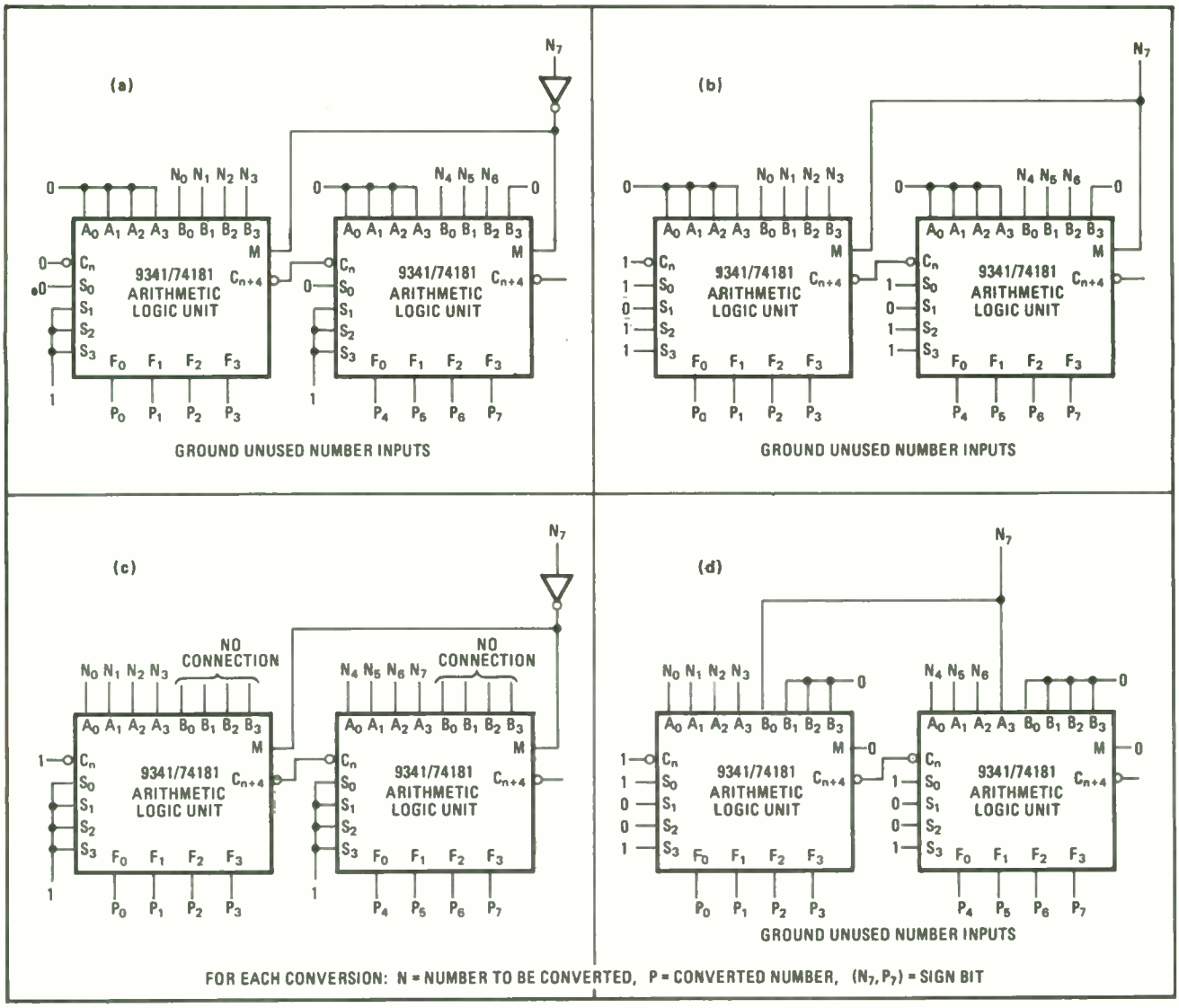


S_0 S_1 S_2 S_3	Arithmetic ($M = 0$, $\overline{C}_n = 1$)	Logic ($M = 1$)
0 0 0 0	F = A	$F = \overline{A}$
1 0 0 0	F = A + B	$F = \overline{A + B}$
0 1 0 0	F = A + $\overline{B}$	$F = \overline{A}B$
1 1 0 0	F = minus 1 (2's comp.)	F = Logic 0
0 0 1 0	F = A plus A$\overline{B}$	$F = \overline{AB}$
1 0 1 0	F = A$\overline{B}$ plus [A + $\overline{B}$]	$F = \overline{B}$
0 1 1 0	F = A minus B minus 1	$F = A \oplus B$
1 1 1 0	F = A$\overline{B}$ minus 1	F = A$\overline{B}$
0 0 0 1	F = A plus A$\overline{B}$	$F = \overline{A} + B$
1 0 0 1	F = A plus B	$F = \overline{A \oplus B}$
0 1 0 1	F = AB plus [A + $\overline{B}$]	F = B
1 1 0 1	F = AB minus 1	F = AB
0 0 1 1	F = A plus A (2 X A)	F = Logic 1
1 0 1 1	F = A plus [A + B]	F = A + $\overline{B}$
0 1 1 1	F = A plus [A + $\overline{B}$]	F = A + B
1 1 1 1	F = A minus 1	F = A

1. Functional capability. The operation of an arithmetic logic unit is outlined in the table for all possible selection (S_0, S_1, S_2, and S_3) inputs. The input numbers are A and B, and the output number is F. When the unit's mode (M) input is low, it produces the arithmetic function given in the middle column. When the mode input is high, a logic operation takes place, as indicated in the right-hand column.

from signed-binary notation to two's-complement notation.

The wiring connections for the four other conversions listed in the table are also shown in the figure. Circuit (b) is for converting from one's-complement notation to signed-binary notation, or vice versa. Circuit (c) is for converting from two's-complement notation to one's-complement notation. And circuit (d) is for converting from one's-complement notation to two's-complement notation. □



2. Number conversion. Two arithmetic logic units can be interconnected to change a number's arithmetic notation. The circuit of (a) converts two's-complement notation to signed-binary notation, or vice versa; circuit (b) converts one's complement to signed binary, or vice versa; circuit (c) converts two's complement to one's complement; and circuit (d) converts one's complement to two's complement.

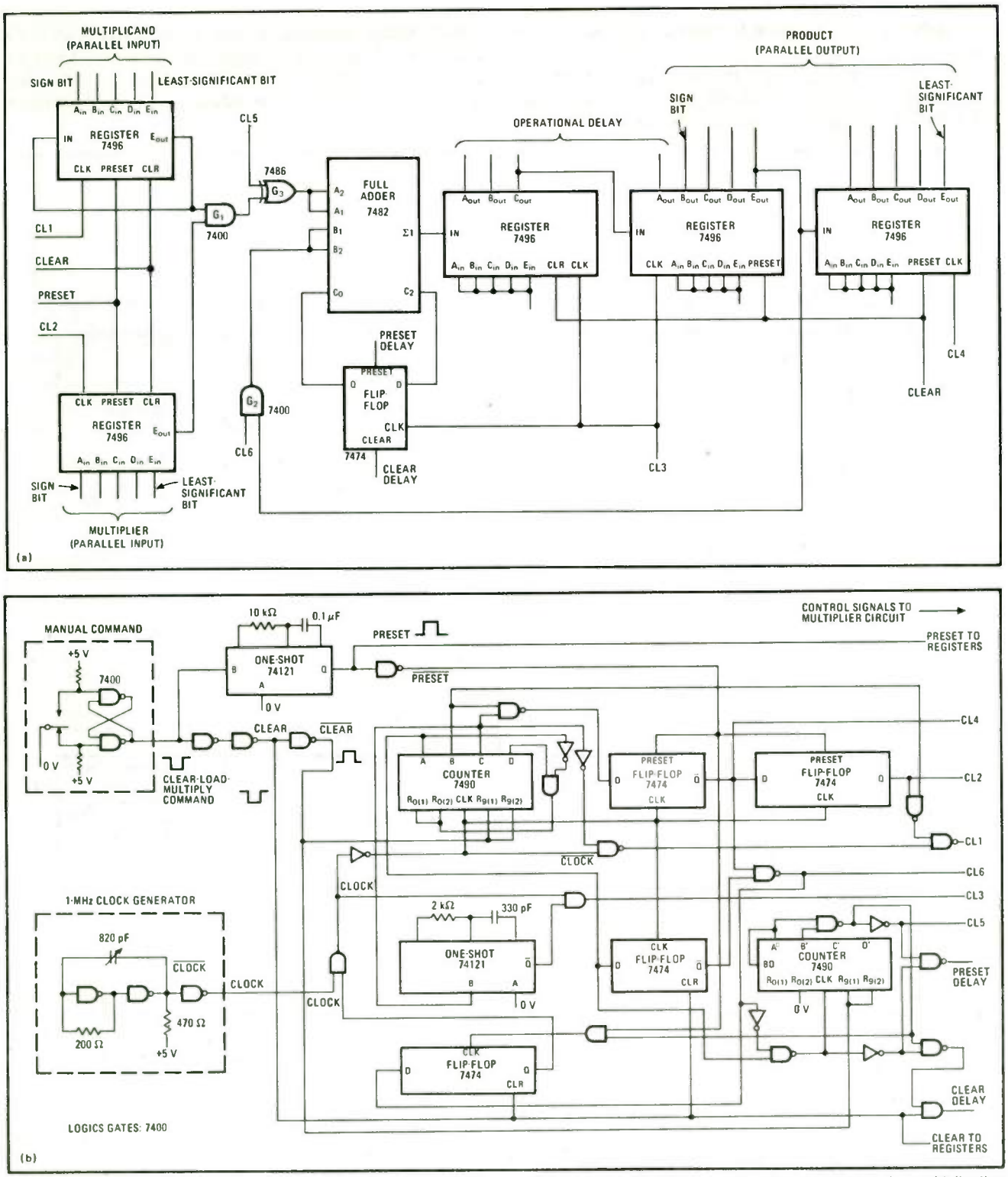
Serial digital multiplier handles two five-bit numbers

by T.K. Tawfig and H.L. Hvims
Allerod, Denmark

Because of the fast operating speeds of today's digital circuits, the serial type of digital multiplier can be regarded as a practical alternative to the parallel or serial/parallel type in many applications. The serial approach can mean a large savings in the number of ICs required to do the job.

The circuit shown is an expandable serial digital multiplier that can accept two 5-bit numbers in two's-complement form. It is useful in such applications as digital filters, signal correlators, and other digital systems that employ two's-complement notation. The multiplier circuitry is shown in (a), while the circuitry used to get the necessary control signals is shown in (b).

The multiplication process is started by a CLEAR-LOAD-MULTIPLY command, which is generated by a manual latch, and stops automatically upon completion. When this start command initiates the control sig-



Serial multiplication. The number of ICs needed to build this digital multiplier is minimized because the circuit performs the multiplication serially. The two 5-bit two's-complement input numbers, however, as well as the output number, are in parallel form. The multiplier circuitry is given in (a), and the control-signal circuitry in (b). The system is easily expanded to accommodate larger numbers.

nals, the two numbers to be multiplied—the multiplicand and the multiplier—are loaded into their respective registers.

Each bit of the multiplicand is gated by each bit of the multiplier through gate G_1. To obtain the final product, the partial sums are added to the partial products. Gate G_2 passes the partial sums, and gate G_3 provides an inversion when the flip-flop delay is preset. This inversion causes the multiplicand to be subtracted when it is gated by the sign bit of the multiplier. An additional shift register provides an OPERATIONAL DELAY for spreading the sign bit. The final product is available in parallel form from the two output registers.

The basic clock frequency for the multiplier circuit is

1 megahertz. Naturally, a faster clock is needed if bigger numbers are to be multiplied. The number of clock pulses required to multiply two n-bit numbers (where n includes the sign bit) is 2n(n–1). Additionally, larger numbers will mean more registers in the multiplier circuitry and more counters in the control-signal circuitry. (Some minor circuit changes must also be made.)

There is a useful rule of thumb to keep in mind to minimize modification when the multiplier is expanded. Choose the factor 2(n–1) to be the nearest larger integer power of 2 and then set the extra bits introduced in the multiplicand and the multiplier to zero. □

Gate threshold difference produces initializing pulse

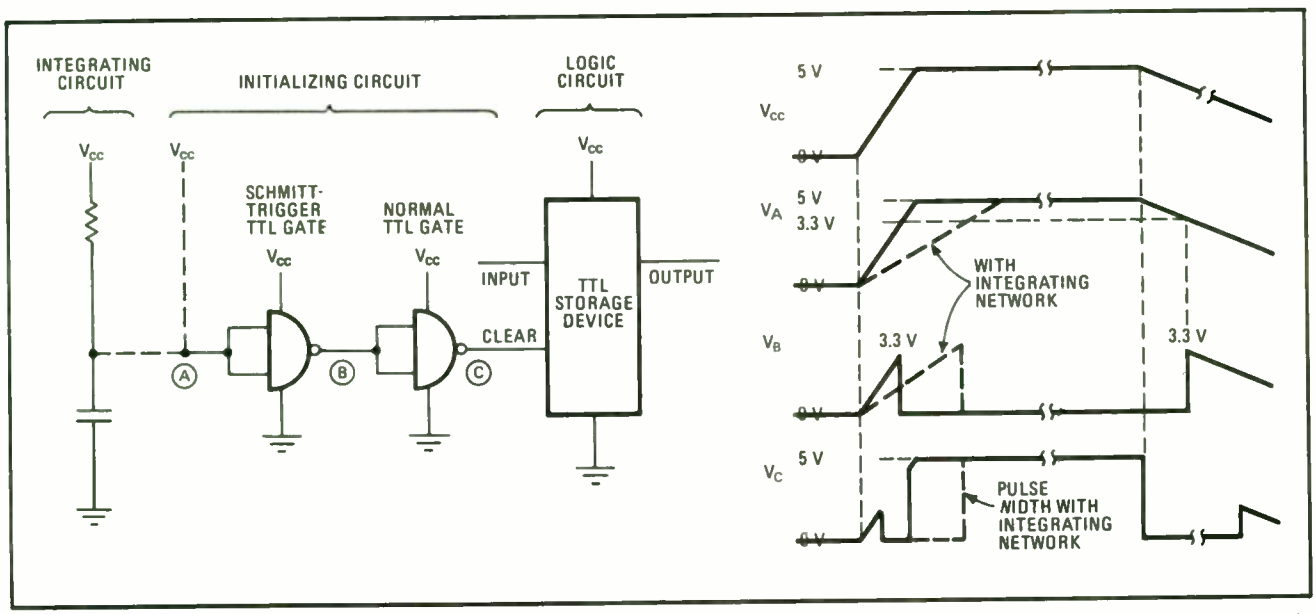
by Jose Souto Martins
GTE Automatic Electric Inc., Northlake, Ill.

Often it is necessary to have a digital circuit assume a predetermined logic state when the supply is turned on. This is not always easy to do, particularly when the digital circuit contains storage devices such as flip-flops and latches. But a simple two-gate circuit, consisting of a standard TTL NAND gate and a Schmitt-trigger TTL NAND gate, can solve this initialization problem without the need of integrating circuits or external reset leads.

The circuit makes use of the difference between operating threshold voltage levels of the two gates to produce an initializing pulse. When the power supply is switched on, the voltage at points A, B, and C rises at the same rate as the applied supply voltage. Neither gate will sink any current until its operating threshold is reached.

Because the operating threshold of the standard gate is lower than that of the Schmitt-trigger gate, the standard gate will respond first. When this gate's threshold is reached, its output goes to logic 0, clearing the storage element. And when the supply voltage reaches the higher operating threshold of the Schmitt trigger, this gate's output goes to logic 0, causing the standard gate to return to its normal operating state so that its output is again logic 1. The circuit, therefore, generates a pulse that can be used to initialize a logic system.

The width of the initializing pulse depends mainly on the power-supply rise time and the voltage difference between the operating thresholds of the two gates. Clearly, if the power-supply rise time is instantaneous, no pulse is generated. This undesirable situation can be avoided by adding an integrating circuit at point A, thereby guaranteeing a minimum width for the initializing pulse. Needless to say, the slower the power-supply rise time, the longer is the initializing pulse. (It should be noted that another pulse is generated when the power supply is turned off.) □



A free pulse. The threshold voltage difference between a regular TTL NAND gate and a Schmitt-trigger TTL NAND gate permits a pulse to be generated for initializing a TTL storage device. As the supply voltage rises, the regular gate changes state twice, producing an output pulse whose duration depends on power-supply rise time. The integrating circuit assures a certain minimum pulse width for the output.

Logic probe with LED display checks ECL circuits

by William Wilke
University of Wisconsin, Madison, Wis.

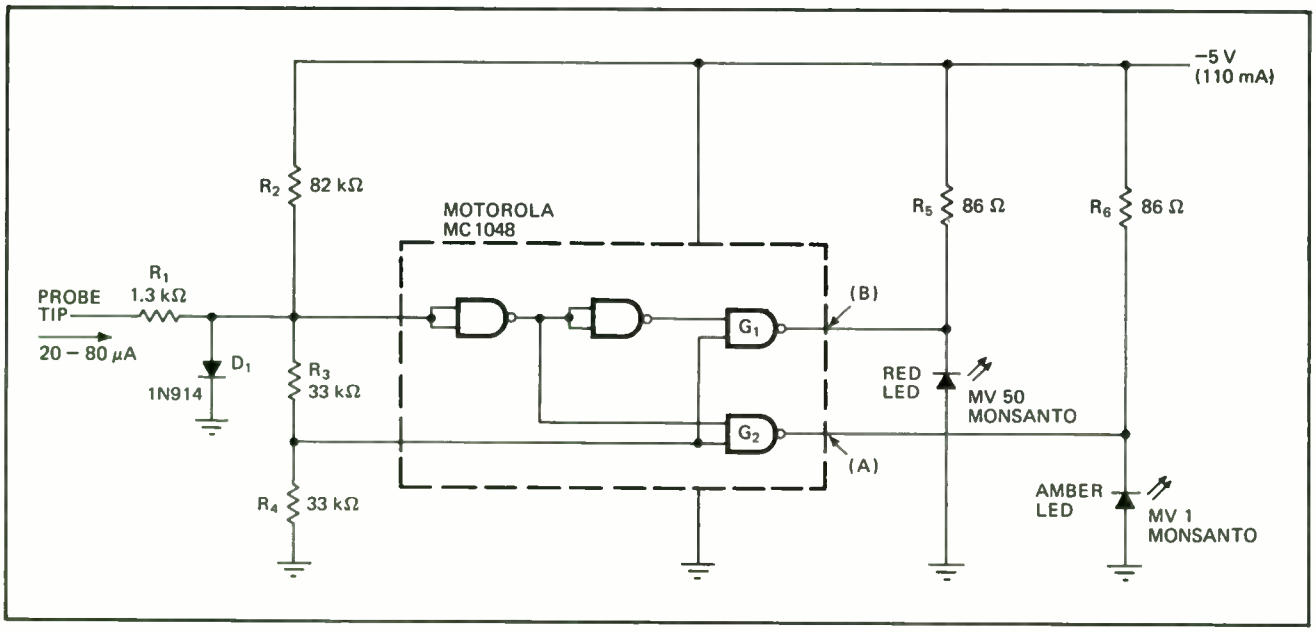
A simple logic probe for testing emitter-coupled-logic circuits identifies three input conditions—a logic high, a logic low, and an open circuit. The probe indicates a logic high (–0.75 volt) by lighting a red light-emitting diode, a logic low (–1.5 V) by lighting an amber LED, and an open-circuit condition by lighting neither. The circuit costs about $4–$5 to build.

Input resistor R_1 and diode D_1 protect the circuit against positive voltages. When an open circuit exists at the probe tip, resistors R_2, R_3, and R_4 hold point A at a logic low so that gates G_1 and G_2 are disabled. Since the LEDs only light for a logic low excitation voltage, both stay off regardless of the voltage level at point B.

When the probe tip is connected to a low or a high logic level, point B is forced to that level (–1.5 or –0.75 V) and point A is forced to a logic high level. Now gates G_1 and G_2 are enabled and, depending on the level at B, either the red or the amber LED lights up.

Resistors R_5 and R_6 allow the quad ECL NAND gate to switch up to 20 milliamperes through the LEDs for a brighter light output. The entire logic probe circuit can be assembled inside an ordinary felt tip pen or other small container. □

ECL logic probe. Red light-emitting diode lights up for logic high input, while amber LED indicates low input. Both LEDs are dark with open circuit at probe tip. When low or high is present at input, gates G_1 and G_2 are enabled, point A goes high, and point B goes to logic level at input, lighting proper LED. For open-circuit input, G_1 and G_2 are disabled and point A is low, keeping both LEDs off.



Simple gating circuit monitors real-time inputs

by David F. Hood
Bell-Northern Research, Ottawa, Canada

In normal operation, the set and reset inputs of the simple flip-flop circuit are not allowed to become active simultaneously, although both can remain at logic 0. But if this elementary rule is violated, a new gating function that can arbitrate real-time inputs is realized.

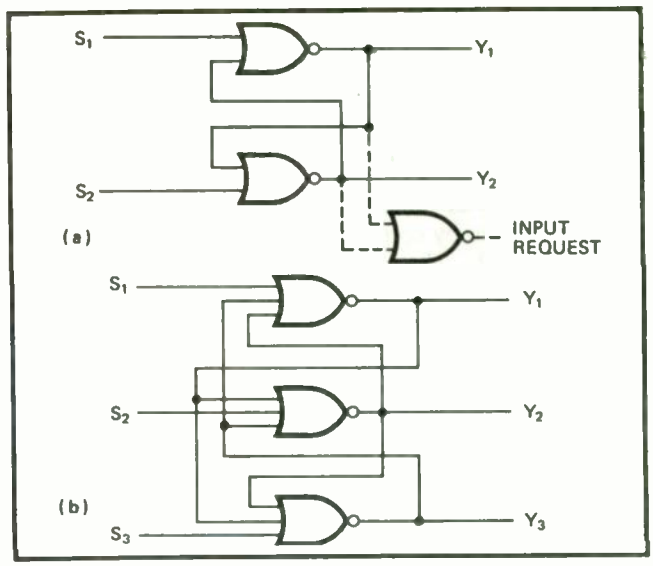
The circuit is particularly useful in signal-processing applications where interrupt requests may arrive asynchronously to be processed by a simple sequencer, rather than by a computing-type device. In such applications, the simplicity of the circuit also makes possible considerable cost savings.

When circuit (a) is used as a flip-flop, its S_1 and S_2 inputs are both low in the quiescent operating state. If the S_1 and S_2 inputs are both high instead, outputs Y_1 and Y_2 are low (in the quiescent mode). Now, when S_1 goes low, Y_1 goes high, and Y_2 does not change. But if S_2 then goes low, neither Y_1 nor Y_2 changes. And since the circuit is symmetrical, if S_2 goes low while S_1 is high, Y_2 will go high and lock out S_1. The signal paths of S_1-Y_1 and S_2-Y_2 may be regarded as inverters with real-time priority arbitration. The addition of a third gate to the circuit provides an INPUT REQUEST lead.

With a third gate, the circuit can also be extended to accept three inputs, as shown in (b). Further extension is done in a similar manner. As with circuit (a), the first

input that goes to logic 0 inhibits all the other inputs, while producing an output itself. Two or more inputs going to logic 0 simultaneously will produce a race condition that, nevertheless, can have only a single victor. One input can be handicapped relative to another by using RC delay networks at the input or output of the handicapped gate.

The same operating description and circuit configurations apply if all the logic levels are inverted, and if NAND gates are substituted for the NOR gates. □



Lock-out gate. Both set and reset (S_1 and S_2) inputs to flip-flop (a) are kept high in quiescent state. When either S_1 or S_2 goes low, its output (Y_1 or Y_2, respectively) will go high, but the other output stays low even if its input goes low. Since only one signal can pass to the output at a time, this gate can arbitrate asynchronous interrupt signals. An additional gate (b) accommodates another input.

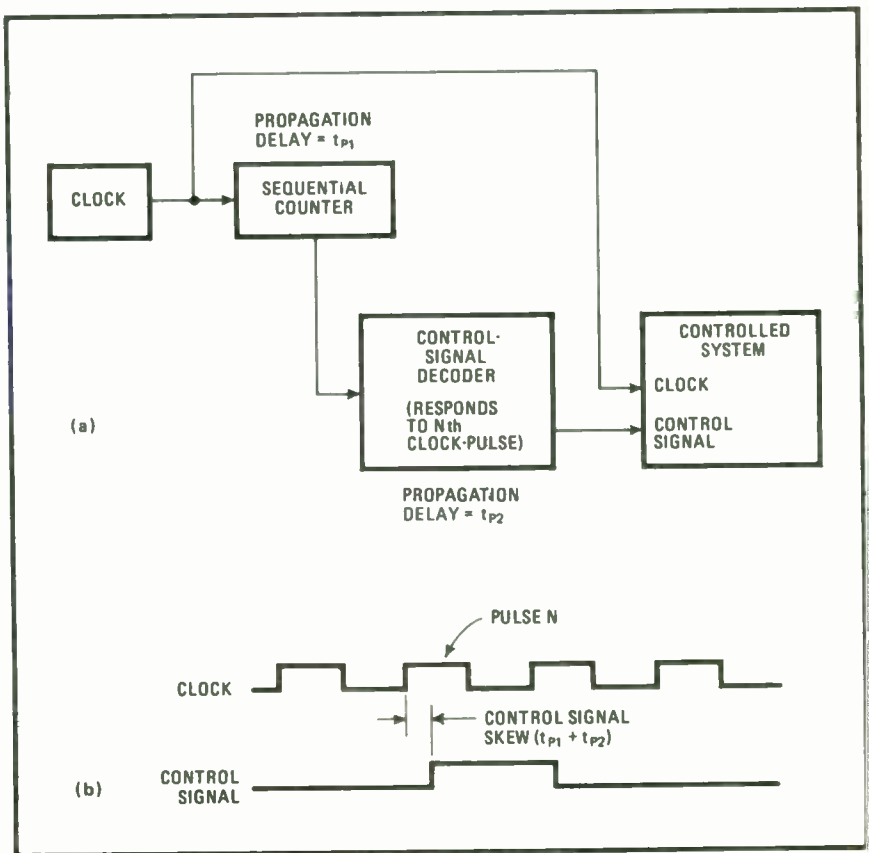
NAND gates and inverter synchronize control signal

by Robert L. White
Applied Research Laboratories, University of Texas, Austin, Texas

In many sequential digital systems that respond to a rising pulse edge, control signals must be synchronized to the clock pulses. These control signals are usually obtained by decoding the desired states of a sequential counter that is driven by the system clock (Fig. 1a). Since the counter and decoder have propagation delays, the decoded control signal is delayed or skewed relative to the system clock, as illustrated in Fig. 1b. But as the clock frequency of the system gets higher, the skew time may become a significant portion of the clock cycle and cause erratic circuit operation.

One example of this problem is encountered with an accumulator operating with a 15-megahertz clock. On the rising edge of every 40th clock pulse, a control signal transfers data from the accumulator to a data regis-

1. Skewed up. In a digital system that requires synchronization of clock and control signal, propagation delays in counter and decoder cause erratic circuit operation. Block diagram (a) shows how control signal is delayed relative to clock pulse, and timing diagram (b) shows waveforms for clock and control signal.



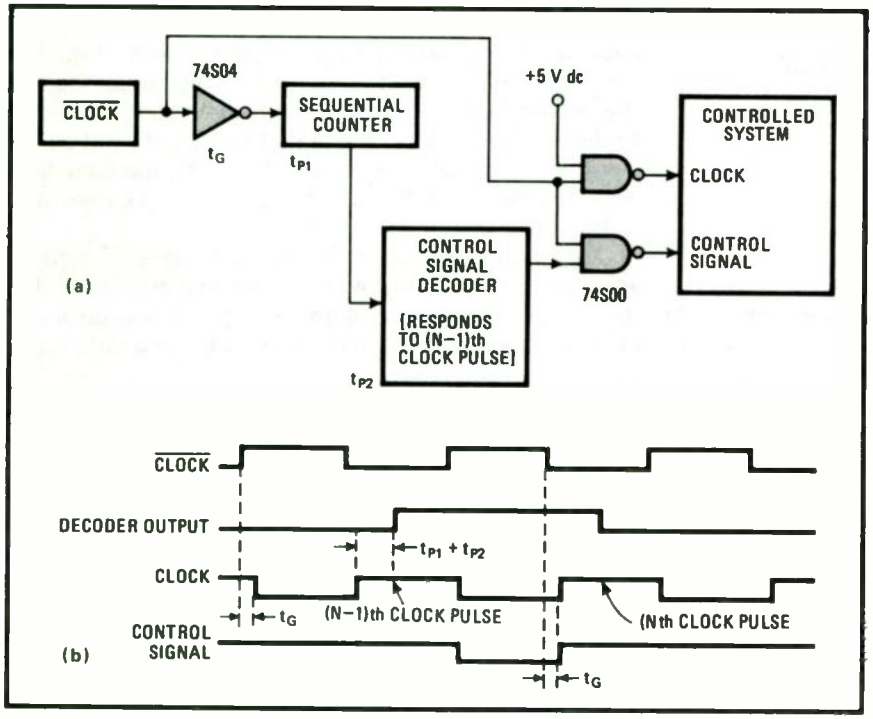
ter. The control-signal skew causes the data to be transferred at some instant between the clock edges, rather than at the edges. Since the accumulator output is changing between clock edges, its value is uncertain at the instant of data transfer, and the system's operation is erratic.

But the skew of the control signal can be reduced to a negligible value by configuring the sequential system as shown in Fig. 2a. The clock of Fig. 1 becomes $\overline{\text{clock}}$, and inverters are added to the $\overline{\text{clock}}$ line. One inverter is shown as a 74S04, but it could be one gate of a 74S00 IC. The other inverter is the top NAND gate in the 74S00. Also, $\overline{\text{clock}}$ drives an input of a NAND gate in the control-signal line. The decoder in Fig. 2 responds one clock-pulse sooner than the one in Fig. 1.

The synchronizing effect of the inverter and NAND gates can be seen in Fig. 2b. Line 3 shows that the control signal waveform is in the high state until the decoder output goes high. This event occurs at the (N – 1)th clock pulse, i.e., one clock period before the rising edge of the control signal.

After the decoder output goes high, the control signal remains high until $\overline{\text{clock}}$ also goes high. After $\overline{\text{clock}}$ goes high, the inputs of the two NAND gates are the same. Therefore, the control-signal and clock waveforms are alike; their falling edges and the subsequent rising edges virtually coincide at the leading edge of the Nth clock pulse. The only skew remaining is the difference between the propagation delays in the two NAND gates. With a 74S00 IC, the difference between the delays in the two NAND gates was less than 1 nanosecond.

The circuit discussed above provides a control signal with a rising edge that is closely synchronized with the rising edge of the clock. Its applications involve the transfer of data in high-speed digital systems. The circuit can be used for any application requiring a precisely timed signal transition that does not occur on every edge of the clock pulse. □



2. Squared away. By adding inverter and NAND gates to circuit and changing decoder to respond one pulse earlier than in Fig. 1, the control signal and clock pulse are synchronized accurately. After rising, the control signal is always high except for the half clock period before its next rising edge.

28. Memory circuits

Memory, peripherals share microprocessor address range

by James A. Kuzdrall
Candia, N.H.

Designers find that the direct addressing mode of the M6800 microprocessor and similar devices cannot be beaten for convenience and efficiency. This mode allows the user to directly address the lowest 256 bytes in the machine—the bytes in locations 0 through 255.

Instructions that use the mode consist of one byte to designate the operation to be performed, plus a second byte to designate the address of the operand. By contrast, other addressing modes have to supply one bit for each of the 16 lines of the memory bus and therefore require a two-byte address for the operand. Thus the direct-addressing mode saves one byte, or 33% of program memory space, in each instruction.

Usually the designer sets aside a portion of the RAM for the easily accessed locations 0–255. However, it is also convenient to assign some of these locations to the peripheral-interface adapter chips that interface the microprocessor to peripheral equipment. The reason is that, in applications requiring a large amount of data input and output, the addresses of the PIA chips may be as active as the RAM addresses.

The circuit arrangement shown in the accompanying diagram allows the direct addressing range of memory locations to be used for both random-access memory and peripheral interface adaptors with a minimum of hardware. It provides control for RAM in locations 0–239, PIAs in locations 240–255, and ROM in locations 1,024–4,095. Although the decoding is not complete because address lines A_8, A_9, A_{12}–A_{15} are not fully decoded, the decoding does prevent two devices from being active on the data bus simultaneously.

In the circuit, decoding an address to reach RAM or a PIA requires only two integrated circuits—a 74LS10 triple NAND gate and a 74LS139 dual decoder.

Gate U_{1B} enables the decoder when valid memory-address data is present and the data is stable (ϕ_2 from clock U_{10} is high). Then address lines A_{10} and A_{11} of the central processing unit are decoded to make one of the 2Y outputs low. Decoder outputs 2Y1, 2Y2, and 2Y3 each select a 1-kilobyte section of ROM, i.e. ROM-1, ROM-2, or ROM-3. If both A_{10} and A_{11} are low, however, so that 2Y0 is low, the RAM and interface adapters are enabled. RAM-1, U_4, is selected if the address is below 128 (A_7 low). U_5 is enabled for addresses between 128 and 255 (A_7 high), but inhibited by gate U_{1A} for addresses 240–255.

To activate the interface adapters (U_6–U_9) for these unused addresses, the inhibit signal is inverted by U_{1C}. The decoder outputs 1Y0-1Y3 of U_2 provide the final selection among the interface adapters. The decoding meets all worst-case timing and loading requirements.

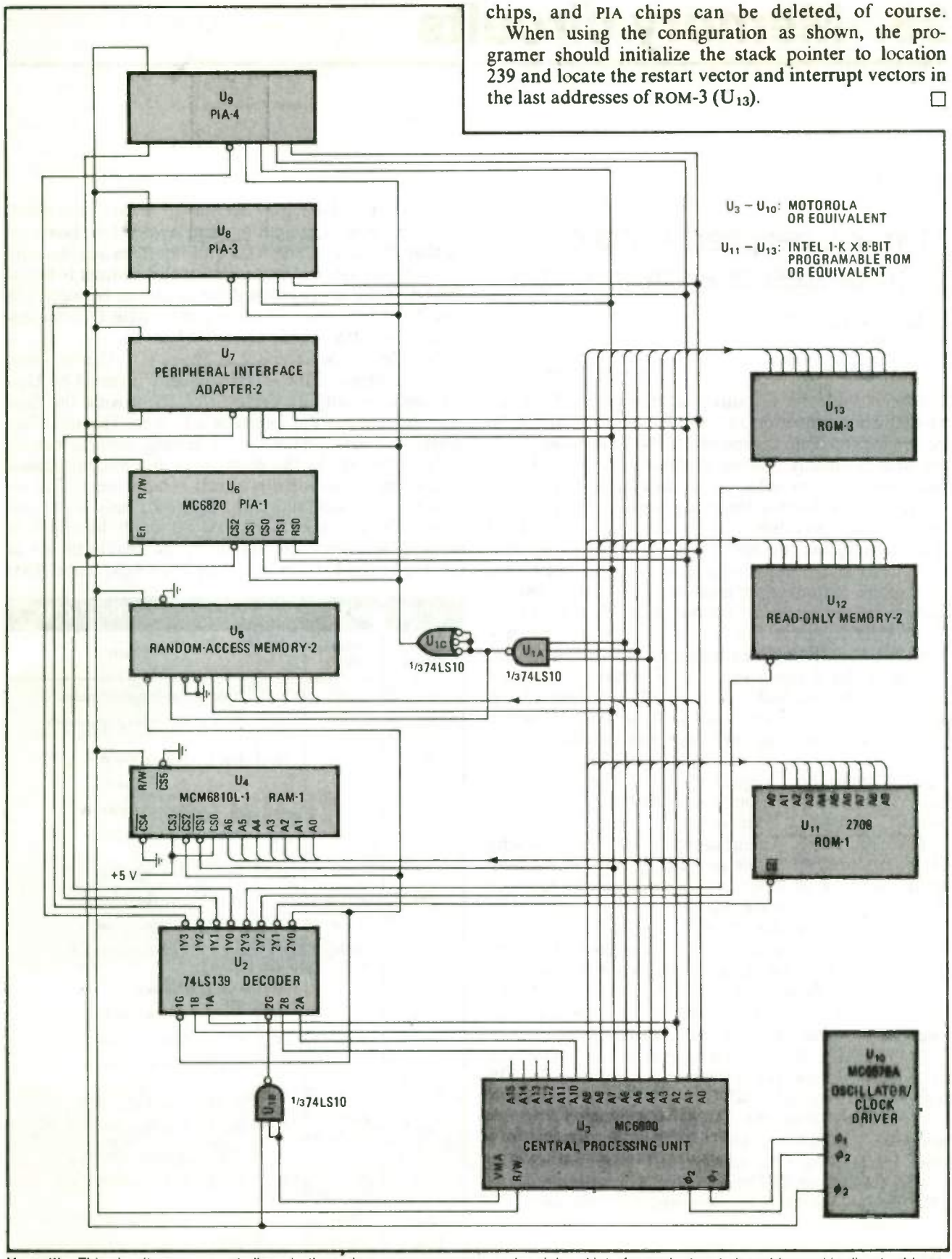
The table shows the contents of the microprocessor address locations for this circuit arrangement. The selection of devices addressed is shown only as an example. For instance, more RAM can easily be added in memory locations 256–511 using the enable inputs of the MCM6810L-1 devices. Unneeded ROM chips, RAM

CONTENTS OF MICROPROCESSOR ADDRESS LOCATIONS

Starting address	Finishing address	Chip	Contents
0	127	U_4	RAM-1 Random-access memory
128	239	U_5	RAM-2 Random-access memory
240	–	U_6	PIA-1 Data register A
241	–	U_6	PIA-1 Data register B
242	–	U_6	PIA-1 Control register A
243	–	U_6	PIA-1 Control register B
244	–	U_7	PIA-2 Data register A
245	–	U_7	PIA-2 Data register B
246	–	U_7	PIA-2 Control register A
247	–	U_7	PIA-2 Control register B
248	–	U_8	PIA-3 Data register A
249	–	U_8	PIA-3 Data register B
250	–	U_8	PIA-3 Control register A
251	–	U_8	PIA-3 Control register B
252	–	U_9	PIA-4 Data register A
253	–	U_9	PIA-4 Data register B
254	–	U_9	PIA-4 Control register A
255	–	U_9	PIA-4 Control register B
1024	2047	U_{11}	ROM-1 Read-only memory, program
2048	3071	U_{12}	ROM-2 Read-only memory, program
3072	4087	U_{13}	ROM-3 Read-only memory, program
4088	4095	U_{13}	ROM-3 Restart and interrupt vectors

chips, and PIA chips can be deleted, of course.

When using the configuration as shown, the programer should initialize the stack pointer to location 239 and locate the restart vector and interrupt vectors in the last addresses of ROM-3 (U_{13}). □



Versatile. This circuit arrangement allows both random-access memory and peripheral interface adapters to be addressed in direct-addressing-mode locations of M6800 microprocessor. This is convenient in operations with lots of data input and output. Logic gates enable the decoder for valid stable addresses and enable or disable the RAM and PIA sections. Lines A_2 and A_3 are decoded for final selection of PIA.

Feedback latch reduces memory recovery time

by Joseph McDowell and William Moss
Monolithic Memories Inc., Sunnyvale, Calif.

The cycle time of wire-ORed semiconductor memories can be improved with the addition of a feedback gate to a NAND gate latch. The resulting three-gate configuration, which also includes a diode and a resistor, provides latched data outputs from open-collector memory packages with significantly reduced turn-off delay.

For open-collector devices, like S_1 through S_N in the diagram, the common problem is choosing a pull-up resistor that is small enough for fast turnoff and large enough for the current sinking capability of the package's open-collector driver. Turn-on speed is not usually a problem, since capacitors C_1 through C_N are driven from a low-impedance saturated transistor.

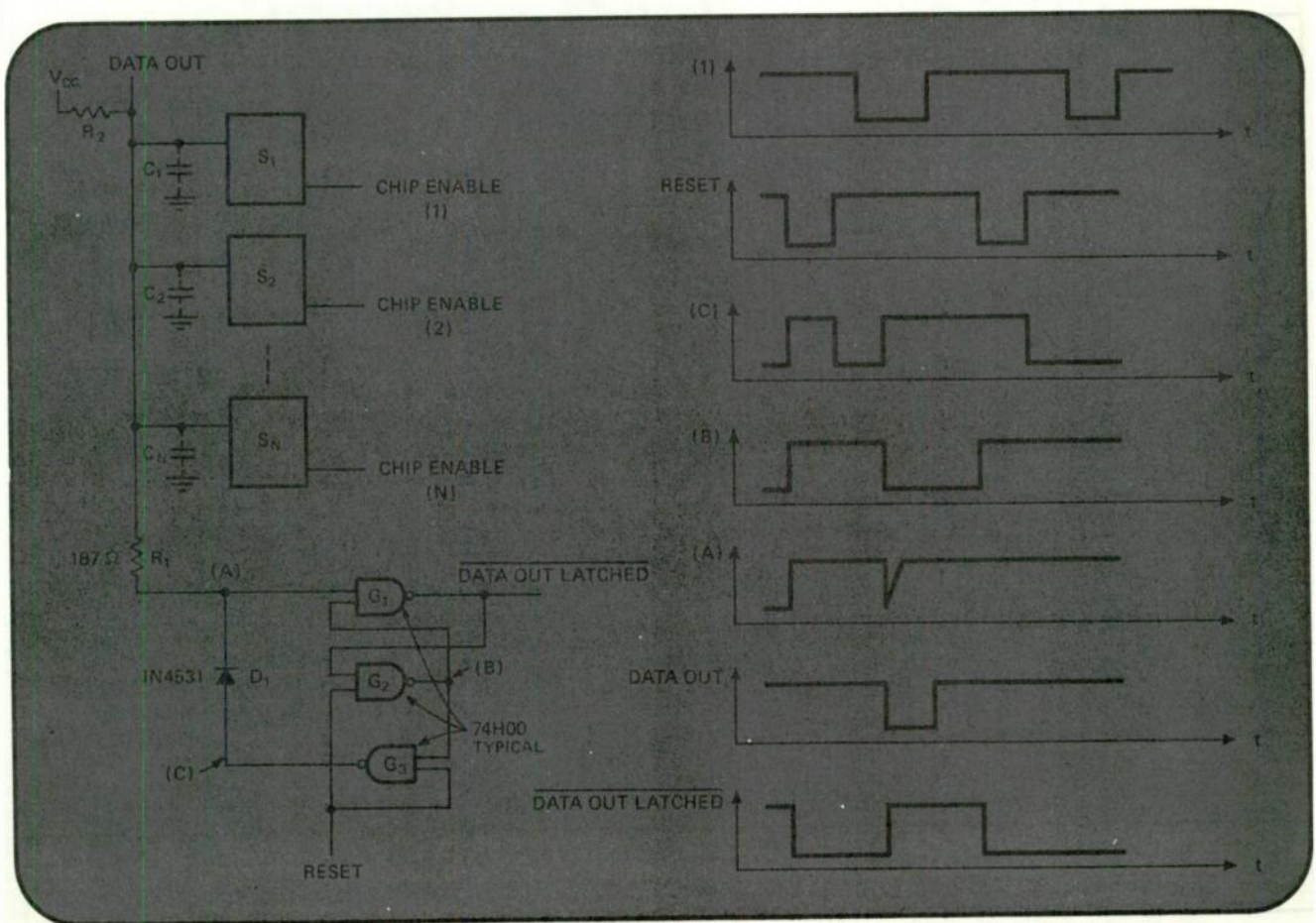
However, turn-off speed or recovery time is determined by the RC time constant at the wire-ORed node. If many memory outputs turn on at once (for example when all low-logic signals are stored in a 72-bit memory word), the change in the power supply load (about 1 ampere in 10 nanoseconds for 15-milliampere open-collector drivers) may require a large pull-up resistor to keep voltage noise within specifications at the expense of turn-off speed.

The illustrated latch employs the common cross-couple gate arrangement of G_1 and G_2. A feedback gate, G_3 actively pulls up the wire-ORed line (like a tri-state gate) after the cross-coupled gates latch. Diode D_1 isolates G_3 from node A, allowing low-level signals to be sensed at this point. To avoid transistor-transistor logic high-level signal problems at node A, D_1 should have a low forward-voltage drop.

Resistor R_1 is used to limit the current from gate G_3 to the open-collector outputs of memories S_1 through S_N. The value of R_1 must be small enough to provide an acceptably low signal level at the latch input. Only the output leakage of the wire-ORed memories and the input leakage of the feedback latch determine the maximum value of pull-up resistor R_2. Recommended values for resistor R_2 range from 1 to 10 kilohms, depending on power supply load considerations.

For 16 wire-ORed memory packages and a 4.7-kilohm pull-up resistor, the feedback latch can reduce turn-off time from 70 to 10 nanoseconds.

Speeding up wire-ored memories. Cross-coupled gates G_1 and G_2, along with feedback gate G_3, trim turn-off delay for array of wire-ORed memories (S_1 through S_N). Three-gate feedback latch uses diode to isolate G_3 so that low-level signals can be detected at wire-ORed node A. Resistor R_1 prevents surge currents from G_3. Maximum value of pull-up resistor R_2 is determined by leakage currents.



Register-addressing system accesses within nanoseconds

by C.A.N. Conde, C.A. Correia, and A.D. Figueiredo
University of Coimbra, Portugal

Addressing systems for shift registers with circulating memories need not be slow and complex. A system containing synchronous binary counters and exclusive-OR gates can considerably speed up clock rate while reducing circuit complexity. For an eight-bit system, propagation delay can be reduced to only 37 nanoseconds.

Generally, shift-register-addressing systems are slow because they compare the address of a counter that is triggered by the clock pulse with the address of a reference register. Instead, it is faster to use up/down synchronous counters in their down-counting mode, as shown in the diagram for an eight-bit system.

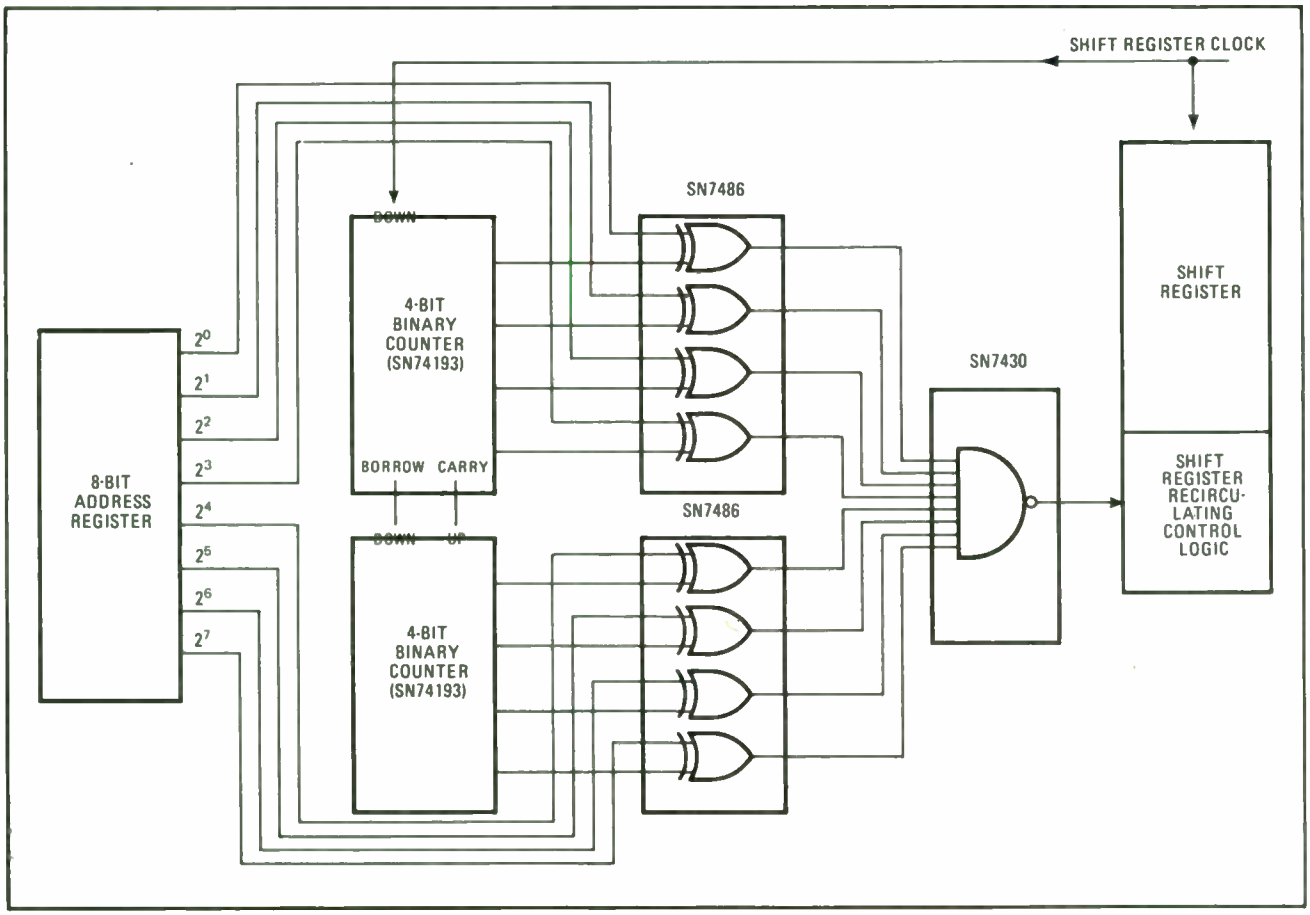
When the eight-bit binary counter, which is formed by the two four-bit counter packages, is in its down-counting mode, it generates successive output clock cpulses (1111 1110, 1111 1101, ... , 0000 0001, 0000 0000, 1111 1111). If, for example, the address register is storing the number 3 (binary equivalent 0000 0011) as the address to be referenced, the counter, after three clock pulses, will contain the binary number 1111 1100, which is the complement of the binary equivalent of number 3.

All the outputs of the exclusive-OR gates will then be logic 1, producing a logic 0 output at the NAND gate to the control logic. This logic 0 output can now be used to gain access to the shift-register bit given by the reference address.

For any address, a logic 0 exists at the output of the NAND gate only when the address is the complement of the binary counter state. And this condition will occur only after the counter generates a number of pulses equal to the contents of the address register.

Although quite fast, this system does have a drawback—it works for binary-coded data but not for binary-coded-decimal data. □

Gaining access. High-speed eight-bit addressing system for shift register cuts propagation delay to only 37 nanoseconds. Exclusive-OR gates compare the outputs of the address register to the outputs of the synchronous binary counter. When these outputs are complementary, the output of the NAND gate becomes logic 0, providing access to the control logic for the system's shift register.



Buffer speeds response time of first-in, first-out memory

by Jim Edrington
Applied Research Laboratories, University of Texas, Austin, Texas

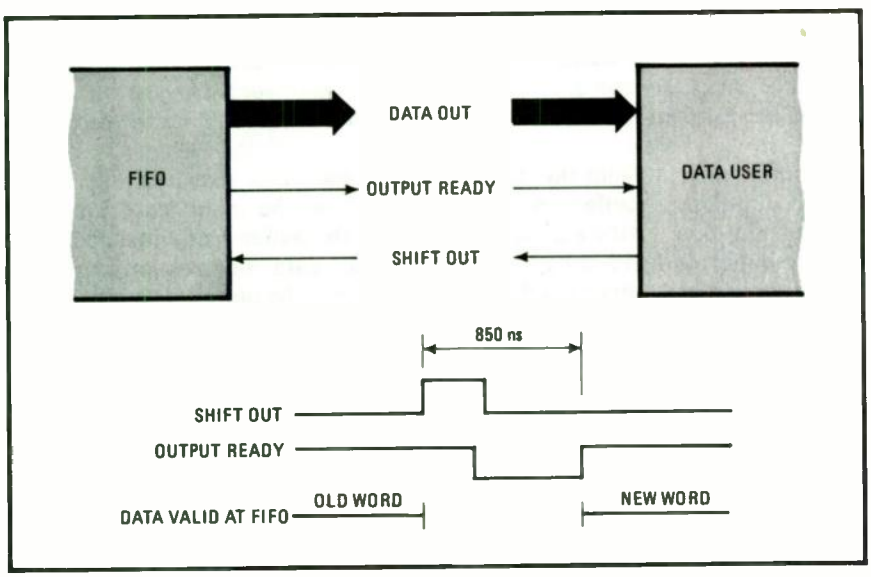
A pair of integrated circuits can interface a first-in, first-out serial memory to a computer or other digital system with which the FIFO is otherwise incompatible. The interface, consisting of a parallel-access shift-register buffer and a dual flip-flop, is connected exactly like the original FIFO interface but has a response time of less than 50 nanoseconds instead of 850 ns.

One of the most popular FIFOs is the 64-word-by-4-bit type 3341, an MOS device made primarily by Fairchild. Its input or output data rate is 1 megahertz, but it takes a long time to respond to a request for data transfer.

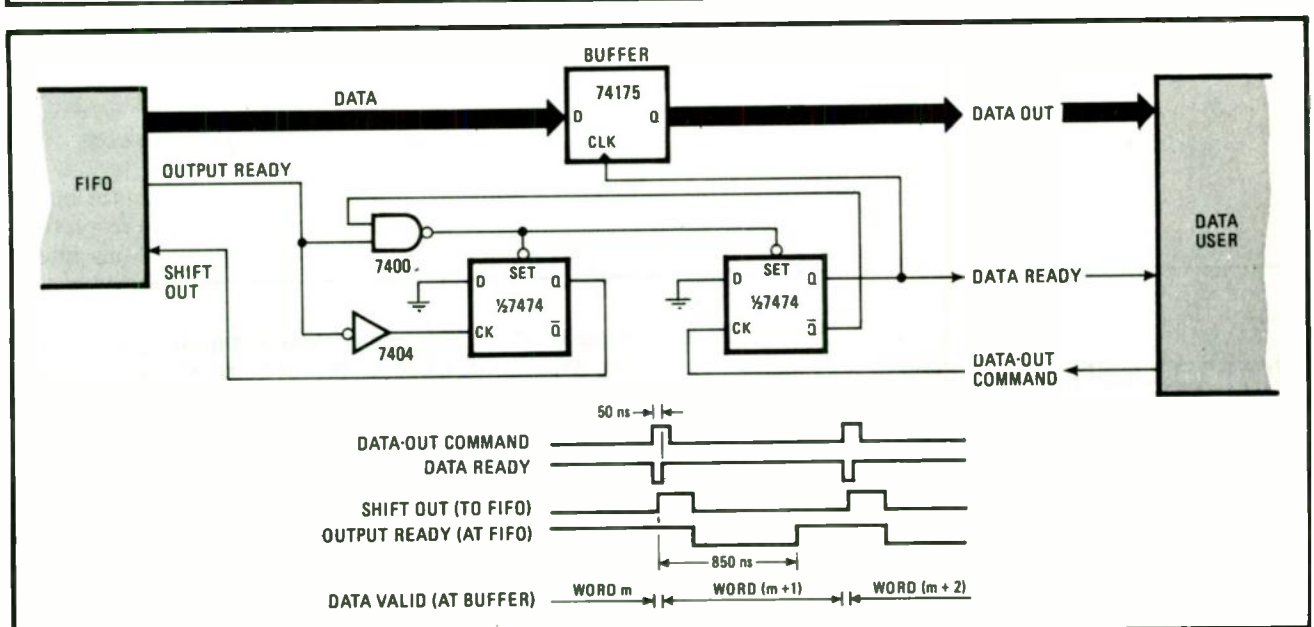
This delay is illustrated in Fig. 1. After reading the word on the FIFO output, the device using the data sends a shift-out signal to the FIFO, asking for a new word. The output-ready line of the FIFO then goes low for 850 ns, during which no valid output word can become available for transfer. When a new word is ready, the output-ready line goes high again.

Such a long delay between a request and an acknowledgment cannot be tolerated by the many digital systems that include fast transistor-transistor logic. An example is the direct-memory-access port of most computers. The DMA operates with a periodicity of 1,000 ns, which is comfortably longer than 850 ns, but unless it receives a data-ready signal within about 200 ns of the previous transfer, it will skip a cycle. In other words, the FIFO transfers words fast enough to work with the typical DMA, but neglects to alert the DMA till too late.

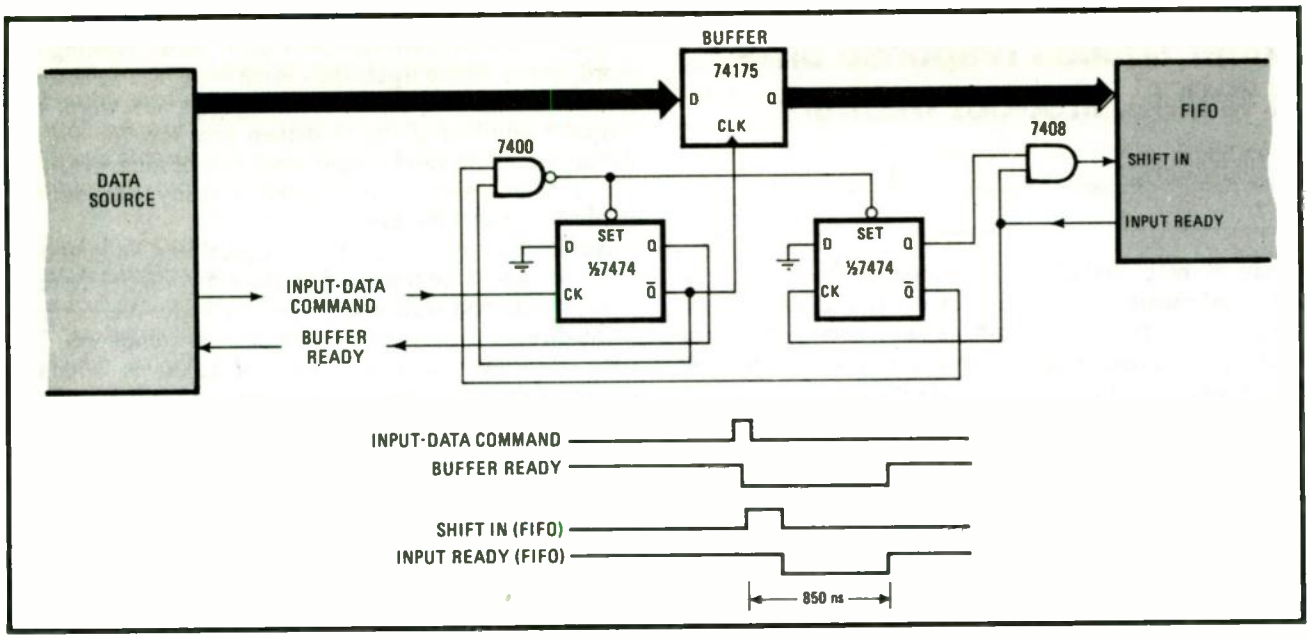
To provide a faster acknowledgment, a TTL parallel-



1. Slow acknowledgment. User system reads data word at FIFO output and sends a shift-out signal telling the FIFO to make a new word available. Then 850 nanoseconds elapse before the FIFO acknowledges that the new word is ready. This delay is too long for fast systems, even though their cycle period is 1,000 ns.



2. Fast acknowledgment. Here, user system reads data word at buffer register, and buffer then takes new word from FIFO and is ready for next data-out command in 50 ns. FIFO has 850 ns to prepare its new output word.



3. Feeding FIFO. Buffer gives prompt acknowledgment to data source that data has been read; when buffer-ready line goes low, source knows that data has been taken. Slow acknowledgment from buffer to FIFO does not hold up a system that requires fast acknowledgment.

access register such as the 74175 is used as a buffer stage between the FIFO and the computer. Two flip-flops provide control for the buffer. The shift-out flip-flop controls the interface between the FIFO and the buffer; it requests a new output word as soon as the buffer register is empty and a new word is available from the FIFO. The data-ready flip-flop takes the place of the FIFO's output-ready signal; it is set true whenever the TTL buffer is loaded with a new word, and it is cleared by a request for data from the DMA. In essence, the TTL buffer is reloaded immediately after each DMA request in time for the following DMA request, as shown in Fig. 2.

A similar circuit may be applied to the input of the FIFO to speed acknowledgment that data has been taken from the data source. In this case, shown in Fig. 3, the buffer register serves to hold the input word until the FIFO can accept it. When the buffer-ready line goes low, the DMA, I/O port, or other data source knows that the input word has been read into the buffer. The source can then immediately change state to validate a new word.

In neither case is the overall data flow rate increased—the upper limit is still the FIFO's internal rate. However, the buffer permits the FIFO to be used with many devices for which its response would otherwise be too slow. □

Storing computer data with a cassette recorder

by Richard Eckhardt
Massachusetts Institute of Technology, Cambridge, Mass.

Two simple interface circuits permit data from a teletypewriter to be recorded and played back on a portable cassette tape recorder. This means that a conventional tape recorder can be employed as a compact reusable storage device for minicomputers, with a teletypewriter operating as the only input/output equipment. And remember that a single 120-minute cassette will hold as much information as 600 feet of paper tape.

Teletypewriter data is transmitted at the rate of 10 characters per second (110 bits per second), a frequency that is far too low for most audio recorders. Therefore, the data is converted to tone bursts at a frequency the recorder can use. On playback, the tone bursts are detected, and the original data format is reconstructed.

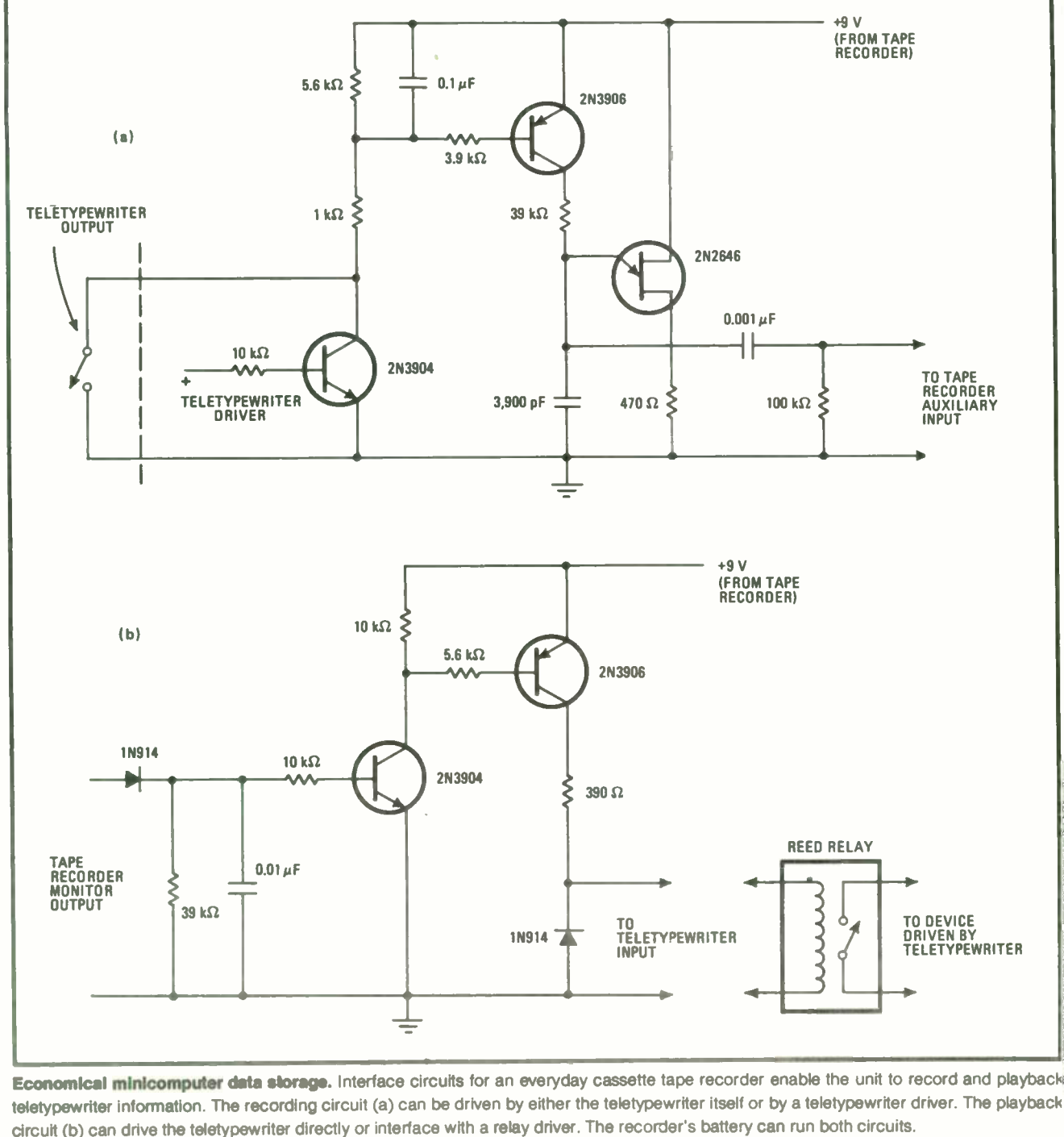
The teletypewriter-to-recorder interface circuit (a) can be driven either directly by the teletypewriter output or by the circuitry that drives the teletypewriter.

The output of a teletypewriter resembles the opening and closing of a switch. In the interface circuit, this switching waveform is first filtered slightly to remove bounce, and then it is used to gate a unijunction oscillator. If a teletypewriter driver is used instead as the input device, its drive current is fed to the base of a transistor that simulates the teletypewriter's switching action.

The circuit's output is a sawtooth waveform having a frequency of 6 kilohertz. It is applied to the recorder's auxiliary input (high-impedance low-sensitivity input). If the recorder does not have this input, it can be simulated by placing a 470-kilohm resistor in series with the microphone input.

The recorder-to-teletypewriter interface circuit (b) detects the recorder's output, and then rectifies and filters it so that a positive voltage is developed whenever a tone is present. A bleeder resistor is placed across the recorder output lines to produce the proper decay when the tone is removed. This decay voltage is then used to turn on a two-transistor driver that operates the teletypewriter. The output of this detector circuit can also be used to drive a reed relay to produce switch closures like those of a standard teletypewriter output.

It should also be noted that both interface circuits run off of a 9-volt supply, which can often be taken from the recorder's battery pack. □



Economical minicomputer data storage. Interface circuits for an everyday cassette tape recorder enable the unit to record and playback teletypewriter information. The recording circuit (a) can be driven by either the teletypewriter itself or by a teletypewriter driver. The playback circuit (b) can drive the teletypewriter directly or interface with a relay driver. The recorder's battery can run both circuits.

One NOR gate starts shift-register loop

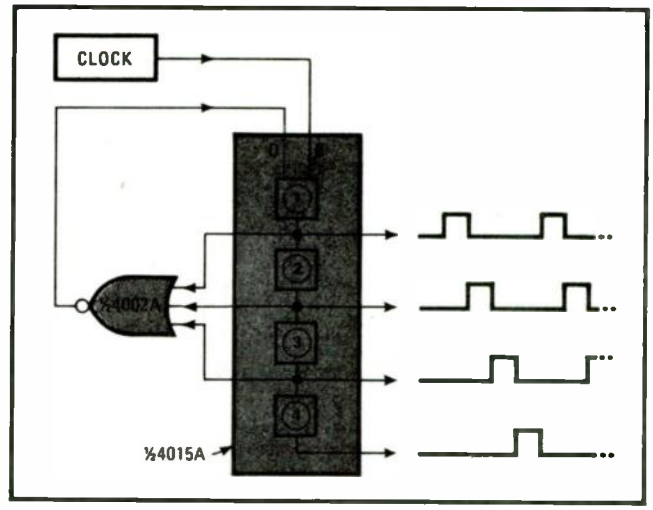
by Jean-Pierre Dujardin
Ohio State University, Columbus, Ohio

A circulating shift register with a single logic 1 in the loop is required in cyclic-triggering operations such as sampling transducers in time-sharing telemetry. Systems for starting this type of circuit are often complex, but the arrangement shown here simply uses a NOR gate with the four-stage shift register.

As the waveforms show, the output terminals of the 4015A shift register go high in a continuing sequence from stage one through stage four and then back to stage one again. The 4002A three-input NOR gate starts this operation and keeps it going.

The input terminals of the NOR gate are connected to the first three output terminals of the shift register. When these terminals are at logic 0, the output terminal of the gate is at logic 1, which is brought to the data input terminal (D) of the register. The next clock pulse transfers the logic 1 at D into the first stage of the register. When at least one of the inputs to the gate is a logic 1, the output from the gate is a 0, which is presented to the register input. Thus, after a maximum of three clock pulses, a single 1 is circulating.

This circuit requires no external timing to introduce the single 1 into the loop and no resetting. If external noise introduces errors, they are automatically corrected. Extension of the system to more than four shift-register stages is straightforward: outputs from all but the last stage are fed into a NOR gate that, in turn, feeds the D input of the first stage in the register. □



C-MOS ring circuit. Arrangement of NOR gate and four-stage shift register provides a pulse output that circulates to each of the output terminals in sequence, moving from one stage to the next as the clock cycles. The two C-MOS ICs determine performance level.

29. Microprocessors

Hardware helps in tracing microprocessor program

by Jeffrey L. Zurkow
Hampshire College, Amherst, Mass.

Debugging microprocessor programs can be especially difficult because most microprocessors lack full control panels and register displays. Software "debug packages" can of course be written, but they are complicated because they must continually modify the user's program in order to trace and control its execution. However, much of their complexity can be eliminated if hardware is added that triggers an interrupt after the execution of each instruction in the user program.

As with any interrupt, the computer saves the address of the next instruction and branches to an interrupt service routine. The service routine can recover this address and print it out along with the contents of the machine's registers, halt and accept operator instructions, set breakpoints, and modify registers before returning to program execution.

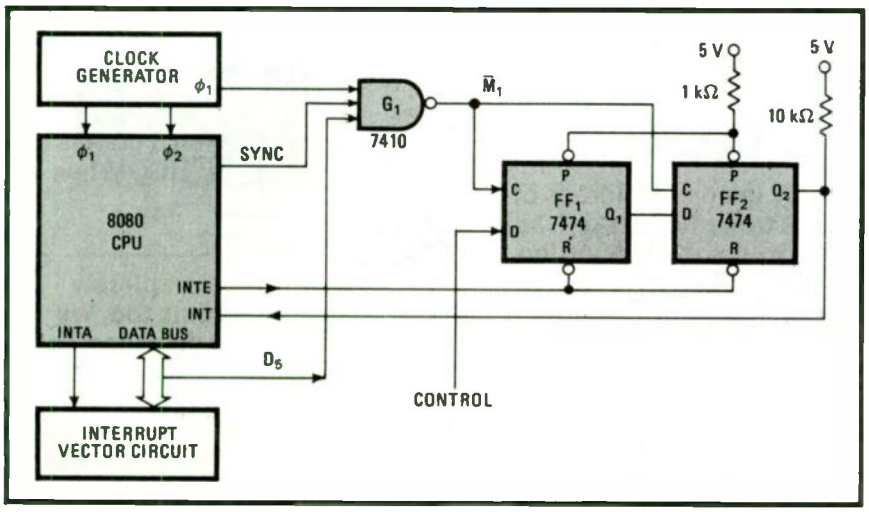
The two circuits shown here are for use with the Intel 8080 microprocessor, but a similar approach should work for other machines. Both circuits perform essentially the same function, but the first latches its interrupt request until the central processing unit responds, while the second saves one flip-flop on the assumption that request latching takes place in the external interrupt-vector circuit. The interrupt-vector circuit, assumed to be present in both cases, is responsible for strobing a restart instruction onto the data bus whenever the CPU outputs an interrupt-acknowledge signal; the restart causes the CPU to save the address of the next instruction (the return address) on its stack, and branch to the interrupt service routine.

An interrupt is requested by driving the 8080's interrupt line high. If interrupts have been enabled by the execution of an interrupt-enable instruction, the interrupt will occur upon the completion of the current instruction. Interrupts will automatically be disabled, and an interrupt-acknowledge signal will be output. The CPU interrupt-enable output line indicates whether interrupts are enabled (high) or disabled (low).

The beginning of each instruction is marked by a CPU status signal called M_1, determined by the coincidence of the signals SYNC, $\phi 1$, and D5. SYNC and D5 are 8080 output pins, while $\phi 1$ is a TTL-level signal representing phase 1 of the two-phase processor clock. The circuits of Figs. 1 and 2 cause an interrupt request on the *second* M_1 pulse following an interrupt-enable instruction. The next instruction should be a return or jump to the program being traced; an interrupt occurring on the return from the service routine would result in an infinite loop, so this instruction is intentionally not traced.

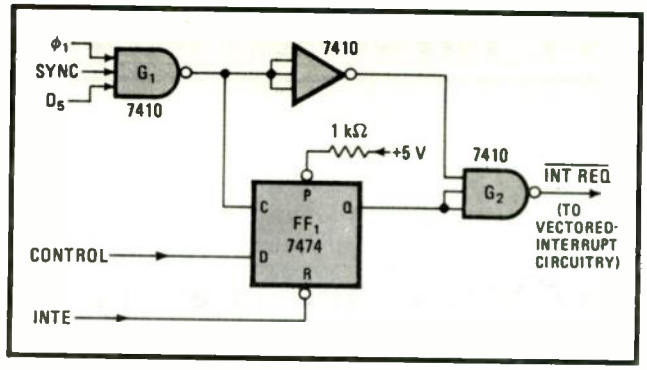
In the circuit of Fig. 1, the two flip-flops are held reset as long as interrupts are disabled. After an interrupt-enable instruction, which turns the line labelled INTE on, the first M1 pulse sets FF_1. The next M1 pulse sets FF_2, causing an interrupt request to be issued via Q_2. Acknowledgment of the request turns INTE off, resetting the flip-flops.

In Fig. 2, the first M1 pulse after an interrupt-enable sets FF_1. The next M1 pulse causes the output of NAND gate G_2 to go low, thus again requesting an interrupt. The line labeled control in both figures may be used to disable the instruction-interrupt feature; interrupts will not occur while control is held low. In practice, this signal comes from a latch which can be set and reset as an



1. Instruction interrupt. When CONTROL is high and interrupts are enabled by the program, the circuit shown requests an interrupt at the beginning of each CPU instruction. The 8080 CPU completes the instruction before honoring the request. Flip-flops FF_1 and FF_2 cause the first instruction following an interrupt enable to be ignored, thus allowing successful return from the interrupt-handling routine.

2. Simplification. When the microprocessor system already includes hardware that latches the interrupt request, this simplified circuit can be used. The other flip-flop in the 7474 package is available for use as a control signal latch.



output device under program control, allowing tracing to be turned on or off.

The only special requirements for the interrupt service routine are that it not re-enable interrupts until ready to return, unless it first turns off tracing. The return linkage is standard: interrupt-enable, immediately followed by return. □

Converter lets processor drive teletypewriter

by Richard C. Pasco
Stanford University, Stanford, Calif.

An inexpensive circuit can replace a lengthy software routine at the interface between a teletypewriter and almost any microprocessor [see articles on pp. 209, 210]. But only six integrated circuits are needed in an improved version that employs the standard 8-bit ASCII code, and only five ICs in the modification that processes the Baudot code.

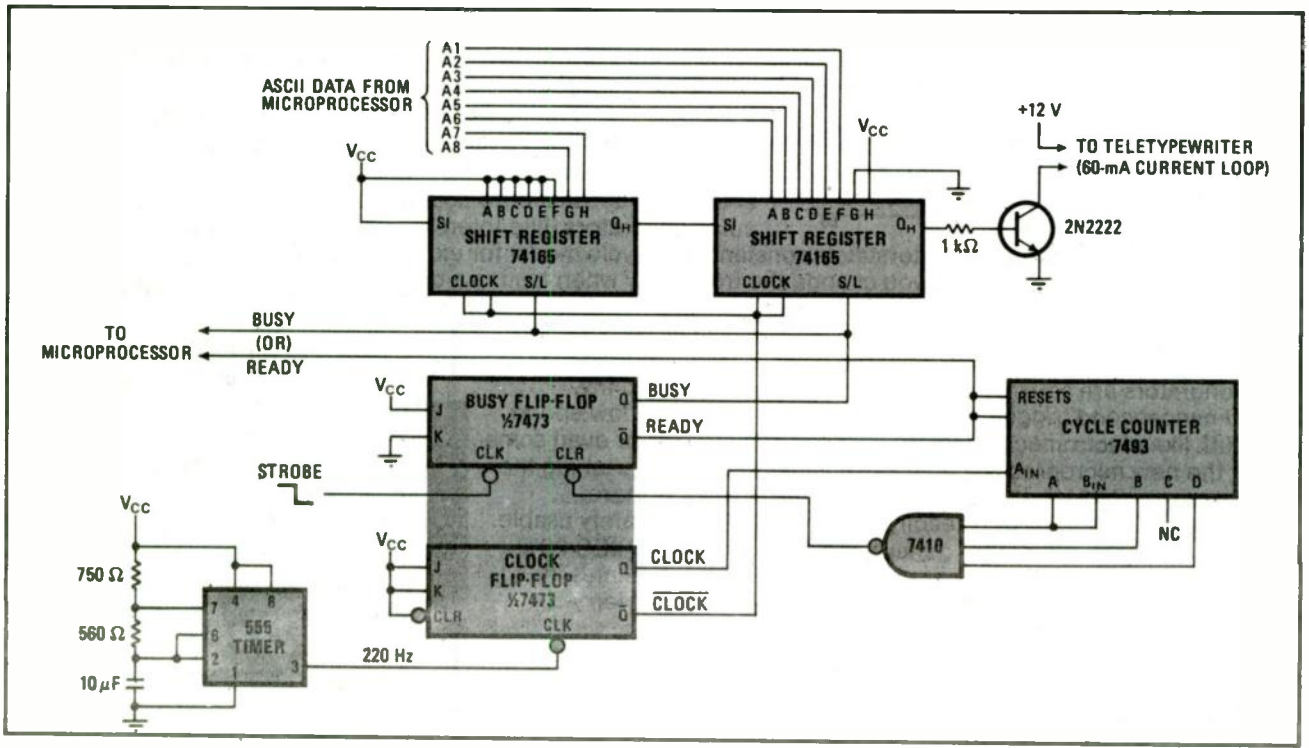
This parallel-to-serial converter has many applications. It will change the parallel output of a keyboard into a serial format for transmission by telephone via a modem, and it will interface the output of any parallel-output device with a teletypewriter for printing.

The converter's operation is easily followed with the aid of the accompanying circuit diagram. Initially the converter is in the READY mode—that is, the BUSY flip-flop is cleared. This keeps the 16-bit shift register in the LOAD mode and the cycle counter reset. The output of the shift register is held high because the parallel load input of its last stage is connected to V_{CC}.

Upon a negative-going transmission of the STROBE line, the BUSY flip-flop is set. This puts the shift register into the SHIFT mode, locking-in the data present at its inputs, and removes the reset from the cycle counter.

On the first negative-going transition of the clock after this strobe, the cycle counter enters state 1, and simultaneously the shift register shifts a logic zero to its output. This logic zero is the START signal.

On the next nine clocks, the shift register's output consists of 8 data bits and a high corresponding to the



Serial feed. Data from microprocessor, parallel-fed into shift register, is fed out serially to teletypewriter for printout. The STROBE and BUSY signals synchronize the circuit with the processor. Ten characters per second are transmitted in standard 8-bit ASCII code, but circuit is easily modified for Baudot code. This hardware eliminates a software routine for interfacing device to teletypewriter; parts cost less than $5.

STOP pulse. Meanwhile the cycle counter passes to states 2 through 10.

The next clock puts the cycle counter into state 11, but the gate detects this and clears the BUSY flip-flop. This in turn raises the READY line, resets the cycle counter, and puts the shift register back into the LOAD mode. Thus, the transition from state 10 to the READY mode proceeds asynchronously within a few nanoseconds. During this transition the shift-register output remains high because a logic 1 is loaded from the V_{CC} line.

Transmission at 10 characters per second results if a new character is provided within one clock period (9.09 ms) of this READY indication. Even if a new character is received immediately, however, the output will remain at 1 and transmission will not begin until the next clock. This insures a minimum stop pulse duration of two clock periods. If no character is received, the converter will wait in the READY mode indefinitely.

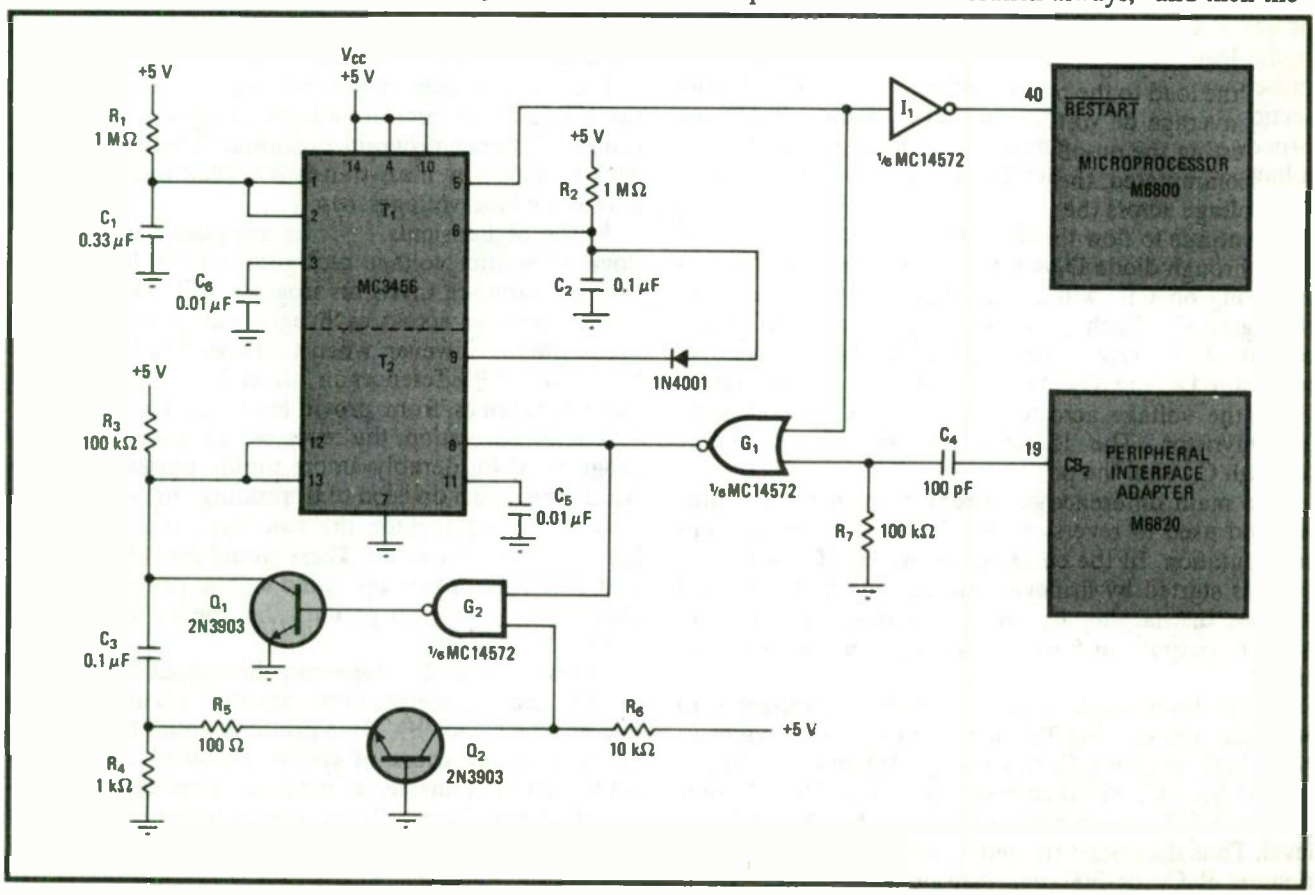
The following modifications adapt the circuit to the Baudot code. Delete the left-hand 74165, and connect the SI and A inputs of the right-hand 74165 to V_{CC}. Then replace the 7410 gate with a 7404 inverter driven off the 7493's D output (the A output now connects only to B_{in}; B and C outputs are left with no connection). □

Dual-555-timer circuit restarts microprocessor

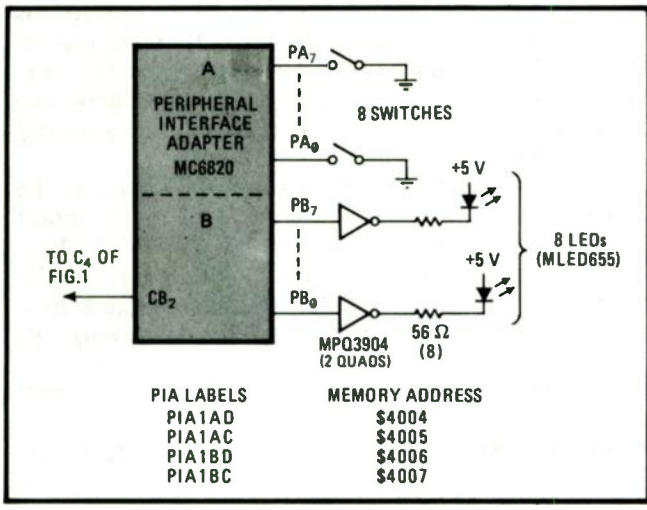
by James R. Bainter
Motorola Semiconductor Products, Phoenix, Ariz.

If noise on one of its bus lines garbles an instruction sequence, a microprocessor system will operate incorrectly—unless monitored by a timing circuit such as the one described here. When the circuit detects a garble, it generates a restart signal that causes the microprocessor to start its program all over again. The circuit also generates the power-on starting signal for the system.

Take the case of the M6800 microprocessor, which employs instructions composed of three 8-bit binary numbers, or bytes. The first byte is the operation code—describing the task to be accomplished—and the second and third bytes, if required, contain either data or address information. Now, suppose the hexadecimal number 20FE is to be loaded into the index register of the M6800. The instruction in machine code (hex representation) is CE,20,FE, and the three bytes reside in three consecutive memory locations. If noise from one of the data, address, or control buses were to make the processor skip the CE, the next byte, 20, would be interpreted as the operation code for "branch always," and then the



1. Generates a fresh start. Dual-timer circuit applies starting pulse to microprocessor and also restarts it if noise bursts or other troubles cause it to get off program or stuck in a loop. Improper operation is indicated by absence of timing pulse to T_2 from a adapter program.



TEST PROGRAM

Machine Code (HEX)			Assembly Listing		
CE	00	34		LDX #$0034	00→DDRA; $34→PIA1AC
FF	40	04		STX PIA1AD	
CE	FF	34		LDX #$FF34	$FF→DDRB; $34→PIA1BC
FF	40	06		STX PIA1BD	CB 2 LOW
FE	40	04	START	LDX PIA1AD	SWITCH DATA TO X(HIGH)
09			D1	DEX	
26	FD			BNE D1	X=0 ??
86	34			LDA A #$34	
C6	3C			LDA B #$3C	
F7	40	07		STA B PIA1BC	CB2 HIGH
B7	40	07		STA A PIA1BC	CB2 LOW
7C	40	06		INC PIA1BD	INC LEDS AT PIA1BD
20	EB			BRA START	GO TO START ALWAYS

2. Program listings. Automatic restart test program, stored in RAM, generates the pulse from the interface adapter. Switches connected to PA_7—PA_0 are read into the index register (X), which then decrements down to zero. Control lead CB_2 pulses, and then LEDs blink on in sequence if the microprocessor system is functioning properly. START follows four instructions programing interface adapter.

byte FE would cause the processor to branch always on itself—in effect locking itself up in a loop with no exit.

One way of restoring proper operation is to restart the system by pulling down the restart pin. In the case of the MC6800, this means driving pin 40 of its low-voltage condition—a job done by the circuit in Fig. 1.

The circuit is implemented with an MC3456 dual-555-type timer. Timing portion T_1 and timing networks R_1, C_1 and R_2, C_2 generate a 400-ms restart signal when power is applied. During normal program execution a signal lead applies a periodic pulse to T_2. In Fig. 1 this pulse comes from CB_2, the number 2 control lead from section B of a peripheral interface adapter. But if the processor goes off into never-never land or gets stuck in a loop with no exit, timer T_2 causes T_1 to generate a restart signal.

The circuit operates as follows. Assume pin 5, the output of T_1, is in the logic 0 (low-level) state. The pulses occurring on CB_2 will be coupled via capacitor C_4 to NOR gate G_1. Each pulse will appear inverted at the output of G_1, retriggering T_2 and discharging C_3 via transistor Q_1 and G_2. The transistor-gate combination of Q_2 and G_2 insures the discharge of C_3 is complete. The pulse is 5 microseconds long if the system clock frequency is 1 megahertz.

When the C_3 discharge current drops below 0.7 milliampere, Q_2 turns off, turning off Q_1 and allowing C_3 to recharge. If no input pulse arrives within 10 ms, C_3 will charge up to 0.67 V_{CC} level, and output pin 9 of T_2 will go low, discharging C_2. When C_2 discharges to 0.33 V_{CC}, T_1 output pin 5 will go high, generating a restart signal.

A high-level signal on pin 5 will also be presented to NOR gate G_1, causing T_2 pin 8 to go low. This resets T_2 pin 9 high, allowing C_2 to recharge. When C_2 recharges to 0.33 V_{CC}, C_1 will then recharge to 0.67 V_{CC}. T_1 output pin 5 will remain high until C_1 reaches the 0.67-V_{CC} level. Thus the restart (no pulse) signal will have a duration of R_1C_1 or 300 ms. This long restart signal is needed to turn on the power in a processor system that uses crystal-controlled clocks.

The test program in Fig. 2 is stored in the system's random-access memory. It generates the pulse on CB_2 and tests out the circuit shown in Fig. 1. It reads the switches at the A side of the interface adapter and places the switch data in the upper half of the index register, which it then decrements down to zero. Next, it stores a hex 30 in the B side control register, causing CB_2 to go high, followed by a hex 34, causing CB_2 to go low. The combination of these two instructions has thus caused a positive pulse on CB_2 that lasts for five machine cycles (5 μs for a 1-MHz clock).

The program then increments light-emitting diodes at the A side of the interface adapter, to give a visual indication of proper program execution. Then it branches back to where the switch data is loaded into the upper half of the index register.

As the higher-order switches are placed in the open (logic 1) position, the index register will be loaded with a larger number, and the program will take a longer time to decrement the index register down to zero. Thus the frequency of the pulses on CB_2 will be lower. With the values of R_3, C_3 in Fig. 1, timer T_2 will time out if a pulse does not occur on CB_2 at least once every 10 ms.

A real-life operating system would not use the test program of Fig. 2 to generate timing pulses to T_2. Instead the regular program residing in the system memory would include the two steps that drive CB_2 high and then low again. These would provide the pulse that indicates proper operation of the program; if the pulse failed to appear periodically, the T_1 timer would restart the program.

During system development, the output of T_2 pin 9 can be used to generate other signals, such as interrupts to print stack contents. This printout would be useful in pinpointing the cause of system problems. The signal could also be connected to a counter to record the number of system "hiccups" over a given time period. □

Interfacing a teletypewriter with an IC microprocessor

by Steven K. Roberts
Cybertronic Systems, Louisville, Ky.

The lengthy software service routine generally required to interface a teletypewriter and an IC microprocessor, such as the Intel 8008, can be eliminated by the circuit shown here. A shift register and some control logic are all that it takes, bringing total component cost to only about $6.50.

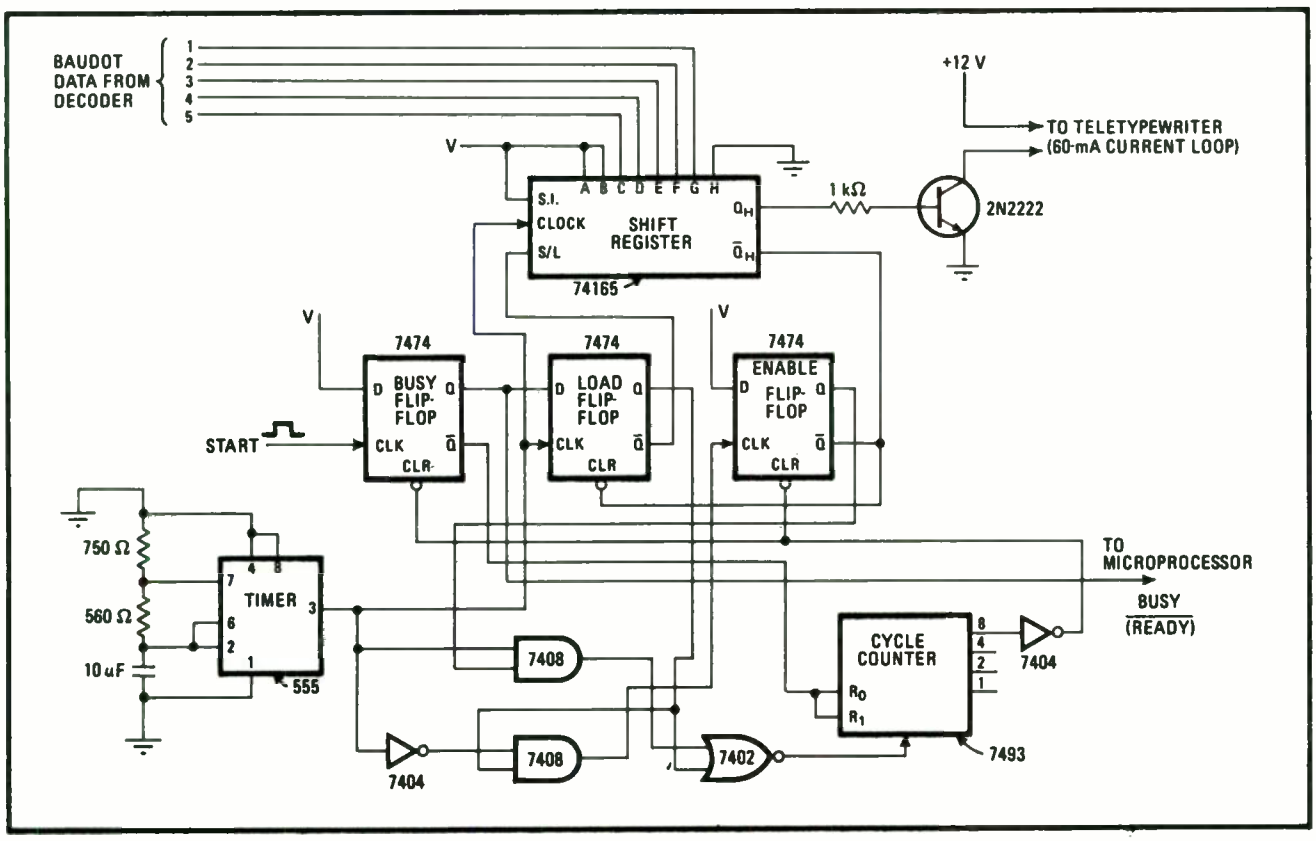
In the 8008 system, synchronization with the central-processing unit is accomplished through this microprocessor's READY line, making modification of the teletypewriter itself unnecessary. The hardware configuration given in the figure is designed for a 10-character-per-second Model 28 Teletype, which uses the five-level Baudot code. If the intended application will not easily accommodate data storage in the Baudot code, conversion may be accomplished with a read-only memory, such as National's MM5221TM. (A Model 33 Teletype presents no decoding problem.)

During the time that the input parallel data is valid, the circuit receives the START pulse, which sets the BUSY flip-flop and takes the READY line low. The BUSY flip-flop also removes the reset from the cycle counter and enables the LOAD flip-flop, which is set on the next clock pulse. This action loads the data at the input to the shift register and increments the cycle counter once.

On the succeeding clock pulse, the ENABLE flip-flop is set, and the data in the register begins to shift to the right. For each shift pulse, the cycle counter is incremented by one until it reaches a binary count of 8. Then, the BUSY and ENABLE flip-flops are both reset, and the READY signal is restored to the microprocessor so that the central-processing unit can resume operation.

In the data character presented to the shift register, bit H, which is constantly held low, corresponds to the teletypewriter START pulse. Similarly, the register's A and B bits are tied high, corresponding to the teletypewriter STOP pulse. Since the STOP signal must be applied to the teletypewriter for approximately 1.5 times longer than the other pulses, the BUSY flip-flop is reset on the falling edge of the clock, during the time that bit A is present at the register's Q_H output. The serial output of the register switches the 60-milliampere teletypewriter current loop through the transistor.

The clock signal for the circuit is derived from the IC timer that is free-running at approximately 75 hertz. For teletypewriters that operate at 6 characters per second, the clock frequency should be about 45.5 Hz. □



Software bypass. Digital interface circuit provides synchronization between a teletypewriter and a microprocessor chip through the latter device's READY line. Normally, a long software routine is needed to make the interface. The input data is in the parallel Baudot code, and the output is for a 10-character-per-second teletypewriter. A free-running IC timer is used to produce the clock signal.

ICs interface keyboard to microprocessor

by Donald P. Martin and Kerry S. Berland
Martin Research Ltd., Chicago, Ill.

A compact, economical interface between a keyboard and a microprocessor can be designed with only three integrated-circuit chips. The ICs are a 5740 MOS scanning keyboard encode, a 2812 MOS first-in/first-out (FIFO) memory, and a 74125 quad three-state buffer. All three can be mounted with the standard array of keyswitches and diodes on a single circuit board.

The 5740 keyboard encoder has 10 scan inputs and nine scan outputs. A unique combination of one input and one output is assigned to each key, adding up to 90 keys in all. The keys are wired between the scan inputs and the outputs with a diode in series, as shown in the circuit diagram. The diodes block sneak signal paths and eliminate "phantom key" effects if several keys are pressed at the same instant.

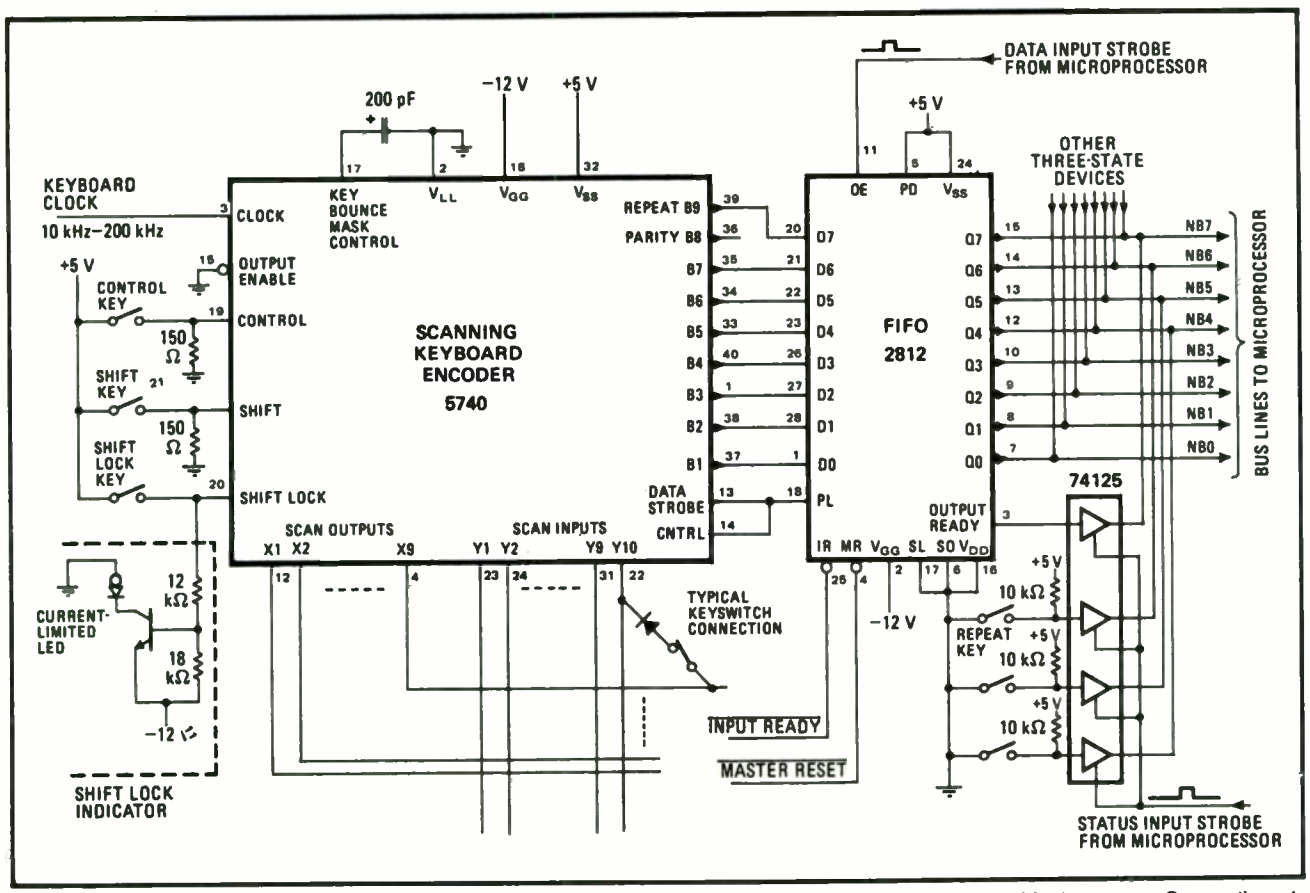
Internal ring counters simultaneously scan both the key matrix and an internal read-only memory. When a key is pressed, the ROM word corresponding to that key is transferred into a one-character nine-bit output latch. The word includes the seven-bit ASCII code for the character, parity bit B8 (which is not used in this design), and the selective repeat bit B9. The 5740 requires an external clock oscillator in the 10-to-200-kilohertz range to drive the scanning counters; this can be obtained from the main timing circuit of the microprocessor.

The internal circuitry of the encoder also performs other necessary functions; it suppresses keybounce effects, responds to key closures even if the previous key has not yet been released, and senses the shift, shift lock and control mode keys.

When the encoder recognizes a keystroke, it sets its data strobe output high. This terminal is wired directly to the encoder's data strobe control, an input terminal that resets the encoder output on the next falling edge of the keyboard clock. The data word is thus available at the encoder for only one clock period.

If no more data storage were provided than the one character stored by the encoder, the microprocessor would have to test for new keyboard data at a rapid rate. This requirement would be a severe constraint on the software, so the 2812 FIFO is included in the interface to provide storage of up to 32 characters.

The keystroke that sets the encoder data strobe high also strobes the parallel load (PL) input of the FIFO and loads the ASCII character into the FIFO. The loaded character moves down through the 32 positions until it either reaches the output or is stopped by a previously



Interface. Three ICs connect keyboard to microprocessor. Encoder provides up to 90 keys. FIFO stores 32 characters. Connections to microprocessor are made through three-state devices to the same 8 bus lines as used by other data sources. All three ICs can be mounted with keyswitches and diodes on a single circuit board, so when keyboard is not included in system, neither are interface components.

stored character. When there is at least one character stored in the FIFO, the output ready signal goes high. This signal is periodically tested by the microprocessor to see whether there is new data from the keyboard. With the FIFO providing buffer storage, the microprocessor needs to test for input data far less frequently.

The FIFO's parallel dump (PD) control is permanently enabled (wired to +5 volts). However, the parallel dump function is also internally gated with the output enable (OE) terminal; therefore the first-received character will not be dumped until the OE terminal is activated. Thus a single strobe to the 2812 first reads the keyboard word into the microcomputer, then dumps the word out of the FIFO, moving the next keyboard character into the output position. The delay between the leading edge of the data input strobe and the appearance of valid data on the microprocessor input bus is less than 400 nanoseconds for the 2812.

When power is first applied, the FIFO registers are cleared by a signal from the master reset circuit of the microprocessor. This signal goes low for a fraction of a second, preventing the FIFO from taking on initial random states that could be interpreted as keyboard data.

To load information into the microprocessor, status input and data input instructions are used. The microprocessor periodically pulses the status input strobe line. This pulse activates the 74125 three-state buffer, which puts the FIFO's output ready bit on the high-order input bus line of the microprocessor. (This is input bit 7, or NB7.) The microprocessor tests this bit to see whether keyboard data is available; if the bit is high, indicating that a character is stored in the FIFO, the microprocessor executes a data input instruction. This instruction activates the output enable terminal of the FIFO, and impresses the keyboard data word on to the input bus to the microprocessor.

The seven lower-order bits of the keyboard data word are the ASCII-encoded character. The high-order bit, NB7, is the selective repeat bit B9. The repeat switch is connected to the next-highest bit through an extra three-state buffer. The repeat function is implemented easily through a few instructions stored in the ROM. □

PROM decoder replaces chip-enabling logic

by Roy Blacksher
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A microprocessor-based system with up to 6 kilobytes of memory and two input/output ports can be easily configured by using a single 32-word-by-8-bit programable read-only memory as the decoding element. In this application, the PROM generates all the chip-enable signals for the memory and also provides the clock pulses for the I/O ports so that it replaces a lot of random logic. And because the 6 kilobytes of memory are ample for most microprocessor applications, this arrangement is practical as well as simple.

The circuit diagram shows the implementation of the system, the heart of which is a Signetics 2650 microprocessor. The memory, which is segmented into 1-kilobyte banks, can be all ROM, all random-access memory, or any combination of both. The diagram shows 3 kilobytes

of ROM and 3 kilobytes of RAM. Each RAM bank consists of eight 2108 1-k-by-1-bit static RAMs, while a ROM bank consists of a single 2608 1-kilobyte ROM. Each of the I/O ports is an 8T31 8-bit bidirectional I/O interface element.

Ten of the address lines, A_0 through A_9, run from the microprocessor to all the six memory banks. The PROM enables just one of these ROMs or RAMs to read or write at a memory location indicated by the 10-line memory bus. The bus can have 2^{10} or 1,024 different address descriptions, and the enable signals from the PROM can apply these to any one of the six memory banks, so the total number of unique memory locations for data from the 8-bit data bus is 6 kilobytes.

The 2650 microprocessor multiplexes address and I/O information on two of its lines—i.e., lines A13-E/$\overline{NE}$ and A14-D/$\overline{C}$. In memory operation, these serve as the two highest-order address lines and thus determine which 8-kilobyte page of memory is addressed. In I/O operations, if line A13-E/$\overline{NE}$ is low, then either port D or port C is enabled, depending on whether line A14-D/$\overline{C}$ is high or low. The M/$\overline{IO}$ line of the microprocessor indicates whether the A13-E/$\overline{NE}$ and A14-D/$\overline{C}$ lines are in memory or I/O operation; the M/$\overline{IO}$ line is high for memory operation and is low for I/O.

As the schematic shows, input terminal A_4 of the PROM is driven by the M/$\overline{IO}$ line from the processor. Therefore A_4 must be high in any PROM input that enables one of the six memory banks, and it must be low to enable, or clock, either I/O port.

The WRP (for write-pulse) line from the processor is connected to input terminal A_3 of the PROM. This line must be high to enable any RAM for either reading or writing. The state of the WRP line does not matter for ROM or I/O operation.

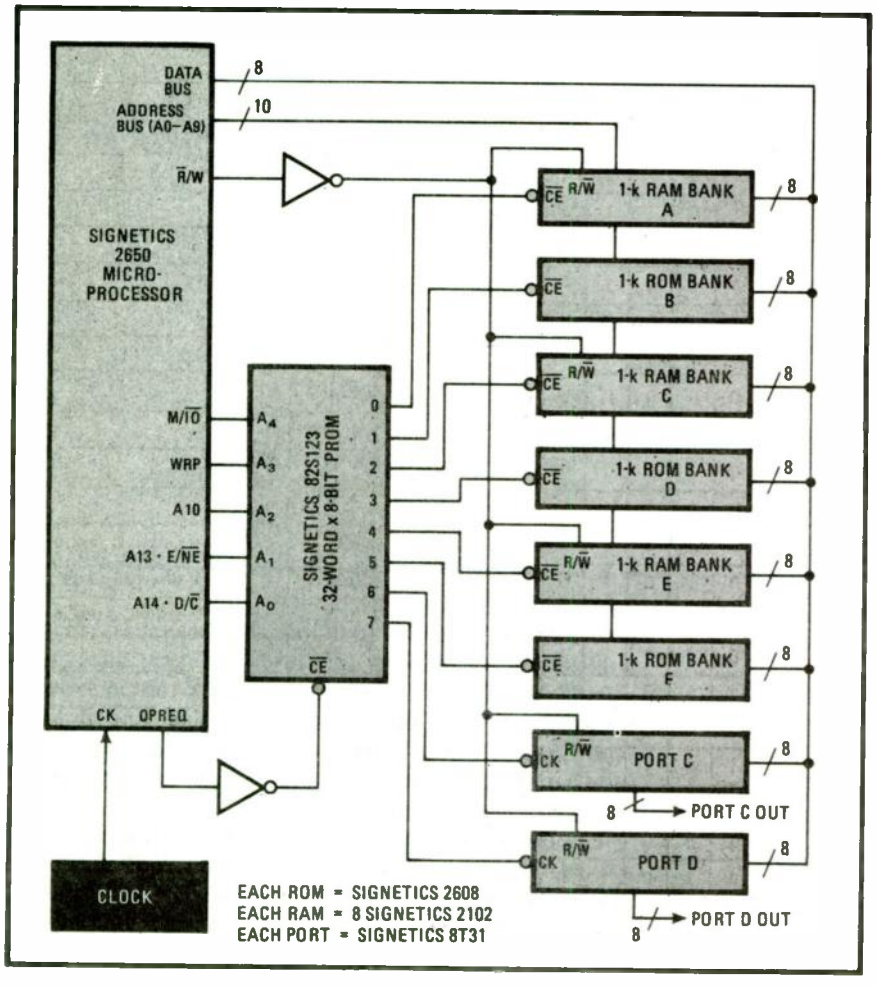
PROM input terminal A_2 is driven by microprocessor address line A_{10}. This line must be high to enable a ROM and low to enable a RAM.

Input terminals A_1 and A_0 of the PROM are driven by the multiplexed lines already discussed; they determine page number in memory, or choose between ports in I/O operation.

The one other input to the PROM is the operation-request (OPREQ) line from the processor, which enables the PROM. This line must be high to enable any RAM, ROM, or port.

The ROMs and RAMs are enabled by low signals; hence the notation ($\overline{RAM\ A}$) indicates that RAM A is enabled, ($\overline{ROM\ B}$) means that ROM B is enabled, etc. However, the I/O ports are clocked, or enabled, by high signals, so (PORT C) means that port C is enabled.

The PROM transfers the microprocessor's control and address lines into appropriate control signals to enable the memory and I/O according to the relationships shown in Table 1. In program form, the coding of the PROM is as shown in Table 2. Notice that input words 0 through



PROM in aid. Control and address lines from microprocessor are decoded by PROM to enable any one of the memory banks or I/O ports. This arrangement provides 6 kilobytes of memory, which is enough for most microprocessor applications, and requires fewer parts and less space and money than random logic for decoding.

TABLE 1. ENABLING CONDITIONS FOR ROMs, RAMs, OR I/O PORTS
$(\overline{\text{RAM A}})$ = (OPREQ) (M/$\overline{\text{IO}}$) (WRP) ($\overline{\text{A13}}$ · E/$\overline{\text{NE}}$) ($\overline{\text{A14}}$ · D/$\overline{\text{C}}$) ($\overline{\text{A10}}$)
$(\overline{\text{ROM B}})$ = (OPREQ) (M/$\overline{\text{IO}}$) (A13 · E/$\overline{\text{NE}}$) ($\overline{\text{A14}}$ · D/$\overline{\text{C}}$) (A10)
$(\overline{\text{RAM C}})$ = (OPREQ) (M/$\overline{\text{IO}}$) (WRP) (A13 · E/$\overline{\text{NE}}$) ($\overline{\text{A14}}$ · D/$\overline{\text{C}}$) ($\overline{\text{A10}}$)
$(\overline{\text{ROM D}})$ = (OPREQ) (M/$\overline{\text{IO}}$) (A13 · E/$\overline{\text{NE}}$) ($\overline{\text{A14}}$ · D/$\overline{\text{C}}$) (A10)
$(\overline{\text{RAM E}})$ = (OPREQ) (M/$\overline{\text{IO}}$) (WRP) ($\overline{\text{A13}}$ · E/$\overline{\text{NE}}$) (A14 · D/C) ($\overline{\text{A10}}$)
$(\overline{\text{ROM F}})$ = (OPREQ) (M/$\overline{\text{IO}}$) ($\overline{\text{A13}}$ · E/$\overline{\text{NE}}$) (A14 · D/$\overline{\text{C}}$) (A10)
(PORT C) = (OPREQ) ($\overline{\text{M/IO}}$) ($\overline{\text{A13}}$ · E/$\overline{\text{NE}}$) ($\overline{\text{A14}}$ · D/$\overline{\text{C}}$)
(PORT D) = (OPREQ) ($\overline{\text{M/IO}}$) ($\overline{\text{A13}}$ · E/$\overline{\text{NE}}$) (A14 · D/$\overline{\text{C}}$)

Table settings. Six output lines from the microprocessor go to the PROM, as shown in the circuit diagram. Table 1 indicates the states these lines must have to enable any one of the memory banks or I/O ports. (A read/write signal, $\overline{\text{R}}$/W, from the microprocessor directly to the RAMs determines whether a byte is read into or out of a RAM; if the PROM enables one of the I/O ports instead of a memory bank, the $\overline{\text{R}}$/W signal determines whether the port reads data on to the data bus or off it.) Table 2 contains redundancy because many of the input lines are "don't care" lines for memory banks or for I/O ports.

15 all have A_4 low, producing I/O operation, and words 16 through 31 have A_4 high for memory operation.

The arrangement described here decodes only the first 10 address lines (A_0 - A_9) of the microprocessor, along with the two page-address lines A13-E/$\overline{\text{NE}}$ and A14-D/$\overline{\text{C}}$. Lines A_{11} and A_{12} are not decoded and are therefore "don't care" lines, so the same 1 kilobyte of information can appear four places on one page. Only the first three pages are used in this system, although the ROM and RAM position on each page can be reversed by simply recoding the PROM. Recoding also allows the use of page 3. □

TABLE 2. CODING OF 82S123 PROM

WORD	INPUTS					OUTPUTS								COMPONENT ENABLED
	A_4	A_3	A_2	A_1	A_0	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	1	1	1	1	1	1	1	PORT C
1	0	0	0	0	1	1	0	1	1	1	1	1	1	PORT D
2	0	0	0	1	0	0	0	1	1	1	1	1	1	–
3	0	0	0	1	1	0	0	1	1	1	1	1	1	–
4	0	0	1	0	0	0	1	1	1	1	1	1	1	PORT C
5	0	0	1	0	1	1	0	1	1	1	1	1	1	PORT D
6	0	0	1	1	0	0	0	1	1	1	1	1	1	–
7	0	0	1	1	1	0	0	1	1	1	1	1	1	–
8	0	1	0	0	0	0	1	1	1	1	1	1	1	PORT C
9	0	1	0	0	1	1	0	1	1	1	1	1	1	PORT D
10	0	1	0	1	0	0	0	1	1	1	1	1	1	–
11	0	1	0	1	1	0	0	1	1	1	1	1	1	–
12	0	1	1	0	0	0	1	1	1	1	1	1	1	PORT C
13	0	1	1	0	1	1	0	1	1	1	1	1	1	PORT D
14	0	1	1	1	0	0	0	1	1	1	1	1	1	–
15	0	1	1	1	1	0	0	1	1	1	1	1	1	–
16	1	0	0	0	0	0	0	1	1	1	1	1	1	–
17	1	0	0	0	1	0	0	1	1	1	1	1	1	–
18	1	0	0	1	0	0	0	1	1	1	1	1	1	–
19	1	0	0	1	1	0	0	1	1	1	1	1	1	–
20	1	0	1	0	0	0	0	1	1	1	1	0	1	ROM BANK B (PAGE 0)
21	1	0	1	0	1	0	0	0	1	1	1	1	1	ROM BANK F (PAGE 2)
22	1	0	1	1	0	0	0	1	1	0	1	1	1	ROM BANK D (PAGE 1)
23	1	0	1	1	1	0	0	1	1	1	1	1	1	–
24	1	1	0	0	0	0	0	1	1	1	1	1	0	RAM BANK A (PAGE 0)
25	1	1	0	0	1	0	0	1	0	1	1	1	1	RAM BANK E (PAGE 2)
26	1	1	0	1	0	0	0	1	1	1	0	1	1	RAM BANK C (PAGE 1)
27	1	1	0	1	1	0	0	1	1	1	1	1	1	–
28	1	1	1	0	0	0	0	1	1	1	1	0	1	ROM BANK B (PAGE 0)
29	1	1	1	0	1	0	0	0	1	1	1	1	1	ROM BANK F (PAGE 2)
30	1	1	1	1	0	0	0	1	1	0	1	1	1	ROM BANK D (PAGE 1)
31	1	1	1	1	1	0	0	1	1	1	1	1	1	–

Circuit steps program for 8080 debugging

by John F. Wakerly
Stanford University, Stanford, Calif.

Executing a program one step at a time is an important aid to debugging microprocessor systems. There are two basic approaches to providing a single-step capability. One method is to add hardware to provide a software interrupt after each instruction's execution, and the other is to provide a completely hardware-oriented "front panel" to give the capability to execute single instructions or memory cycles under hardware control.

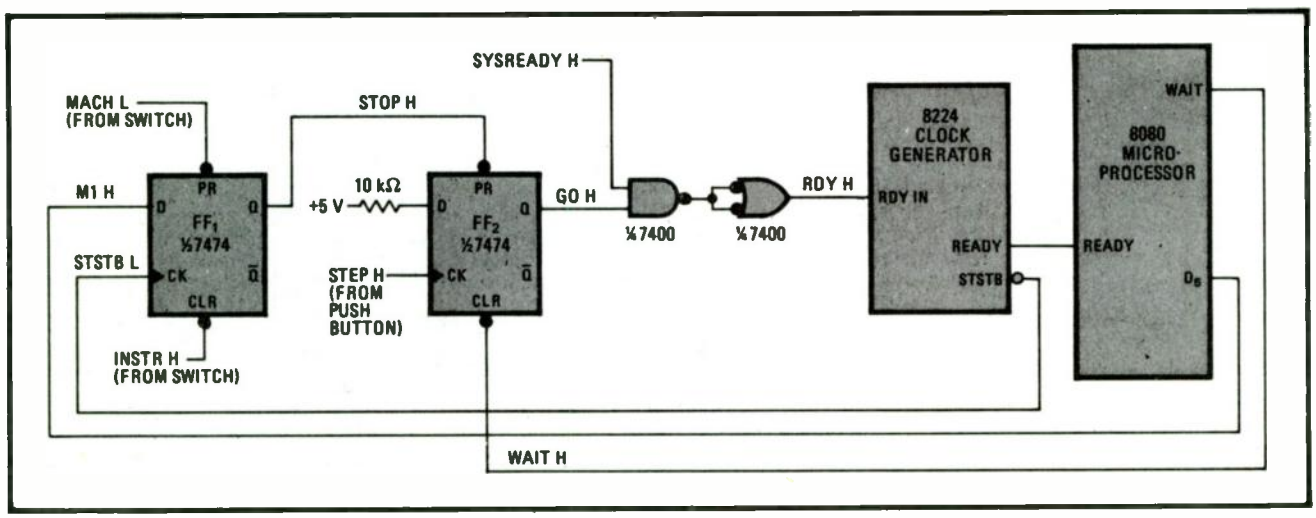
With the first approach, the user can write an interrupt service routine that allows register and memory to be examined at the system teletypewriter or terminal between instruction executions [see preceding article, p. 205]. It takes advantage of the full power and convenience of a software-debugging package, but instructions cannot be single-stepped if interrupts are disabled, and single memory-reference stepping is not possible (there may be several memory references per instruction, and interrupts cannot take place in the middle of an instruction).

The circuit described here is the hardware-implemented "front panel," which enables the user to execute 8080 microprocessor programs either one instruction at a time or one machine cycle (memory or input/output reference) at a time. The circuit uses the READY input of the 8080 to stop the program at each instruction or machine cycle, as selected by the user. A push button then runs the program one step at a time. Between steps, the user can observe the machine state and the current instruction or data on the 8080 data, address, and control lines with a scope, logic probe, or permanent indicator lamps.

The single-step circuit shown in Fig. 1 assumes that an 8224 clock generator is used with the 8080. Without the single-step circuit, a ready signal (SYSREADY H) generated by the memory and I/O systems would be connected to the 8224 RDYIN input. For single-stepping, SYSREADY H (where H denotes active high) is ANDed with the signal GO H. If either signal is low during a memory or I/O reference, the 8080 will go into a wait state until both signals become high. If this circuit is used in a system that does not generate SYSREADY H, then the AND can be removed and GO H connected directly to RDYIN.

A 7474 edge-triggered D-type flip-flop, FF_2, generates the GO H signal. Proper operation of the circuit depends on the fact that a low input on the PR input of the 7474 produces a high output at Q, regardless of any of the other inputs, including CLR. (If both PR and CLR are low, then both Q and $\overline{Q}$ are high.) Thus, if STOP H is low, GO H is high, and the 8080 executes instructions at full speed. However, the 8080 holds WAIT H low just before every memory or I/O reference; thus, if STOP H is high, FF_2 is cleared by the low signal on WAIT H, the 8080 enters the wait state, and instruction execution is stopped. In the wait state, WAIT H goes high and allows GO H to be set high again by clocking FF_2 with the STEP H input. STEP H is the output of a single-step push button, and instruction execution does not begin until this button is pushed.

If only single-stepping at each machine cycle were desired, STOP H could be obtained from a simple switch to select normal operation or single-stepping. However for single instruction stepping, FF_1 is used to detect the beginning of each instruction cycle—the instruction fetch. At the beginning of each machine cycle, the 8080 places a signal M1 H on data-bus output D_5 which



1. Single-step circuit for 8080. This circuit requires only one 7474 dual D flip-flop and half of a 7400 quad NAND package to provide single-instruction and single-machine-cycle-execution capability for an 8080 microprocessor system. It can be modified for a Zilog Z-80.

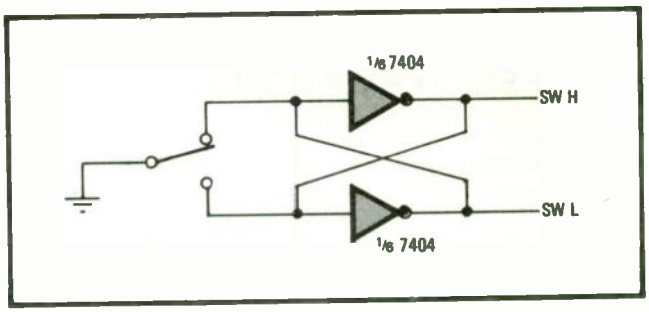
indicates the first machine cycle (fetch) of an instruction. This signal is clocked into FF_1 by STSTB L; thus if M1 H is high, STOP H becomes high, and the 8080 is stopped during the instruction fetch. The data bus contains the fetched instruction.

The PR and CLR inputs of FF_1 are used to determine the mode of operation. If MACH L is asserted (low), STOP H is held unconditionally high, and the 8080 stops at each machine cycle. If MACH L is de-asserted and INSTR H is asserted (high), then M1 H is clocked into FF_1 to generate STOP H, and the 8080 stops at every instruction cycle. If both MACH L and INSTR H are de-asserted, then STOP H is held low, and the 8080 operates normally.

If the inputs MACH L, INSTR H, and STEP H are obtained from switches, they should be debounced. Figure 2 shows an economical debouncing circuit that uses a pair of inverters to debounce an single-pole, double-throw switch. The circuit shorts the high output of an inverter to ground for about 20 nanoseconds at each transition, but this short is not harmful.

An advantage of this circuit over conventional cross-couple NAND gates for debouncing is that three switches can be debounced with one 7404, as opposed to two with one 7400. Also, no pull-up resistors are used.

The single-step circuit can be easily modified for use with the Zilog Z-80 microprocessor. The Z-80 has a separate output pin for $\overline{M1}$, which should be connected to the D input of FF_1. Since this polarity is the opposite of the 8080 M1 output, the STOP H signal should be obtained from the $\overline{Q}$ output of FF_1, and the PR and CLR inputs should be reversed. FF_1 should be clocked by the Z-80 input clock Φ, and the RDY H signal should be connected to the $\overline{WAIT}$ input of the Z-80. Finally, the CLR input of FF_2 should be connected to $\overline{MREQ} + \overline{IORQ}$, which can be obtained from the $\overline{MREQ}$ and $\overline{IORQ}$ outputs of the Z-80 with a single 2-input NAND gate (one quarter of a 7400 package). □



2. Switch-debouncing circuit. Part of a 7404 package debounces spdt switch. Signals are active when switch has position shown.

30. Modulators and demodulators

Digital demodulator for phase-shift-keyed data

by C.A. Herbst
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Exclusive-OR gates and a repeat-modulation scheme can be combined to produce a digital phase-shift-keyed (PSK) demodulator that allows accurate recovery of the reference-carrier pulse train. The demodulation of binary PSK data usually involves two major problems: recovering the reference carrier, and differentiating between the logic 0 and the logic 1 data pulses. This latter problem is resolved easily with differential coding, assigning a logic 1 when the change in carrier phase is 180° and a logic 0 when there is no change.

The first problem, however, cannot be resolved as simply. Usually, the input PSK-modulated carrier frequency is multiplied by 2 to cancel out the phase changes. But this technique, unfortunately, generally results in a degradation of demodulator performance.

A better method is to remodulate the demodulator's local oscillator with the received data so that the phase changes due to input modulation are cancelled out. This produces a virtually unmodulated reference carrier that is equal in phase to one of the two possible input PSK phase states. The ambiguity between the two phase conditions can be resolved by differential encoding.

The circuit shown employs this improved demodulation technique. A quad exclusive-OR IC is used to perform both the demodulation and remodulation functions. Here the exclusive-OR gates are operated as controlled inverters. In the phase-detector portion of the circuit, the PSK input carrier and the remodulated voltage-controlled-oscillator (VCO) signal are normally at quadrature with each other when the system is in lock. This results in a pulse train having a 50% duty cycle at the output of gate G_1. The pulse train is then integrated by the low-pass filter into a dc error signal.

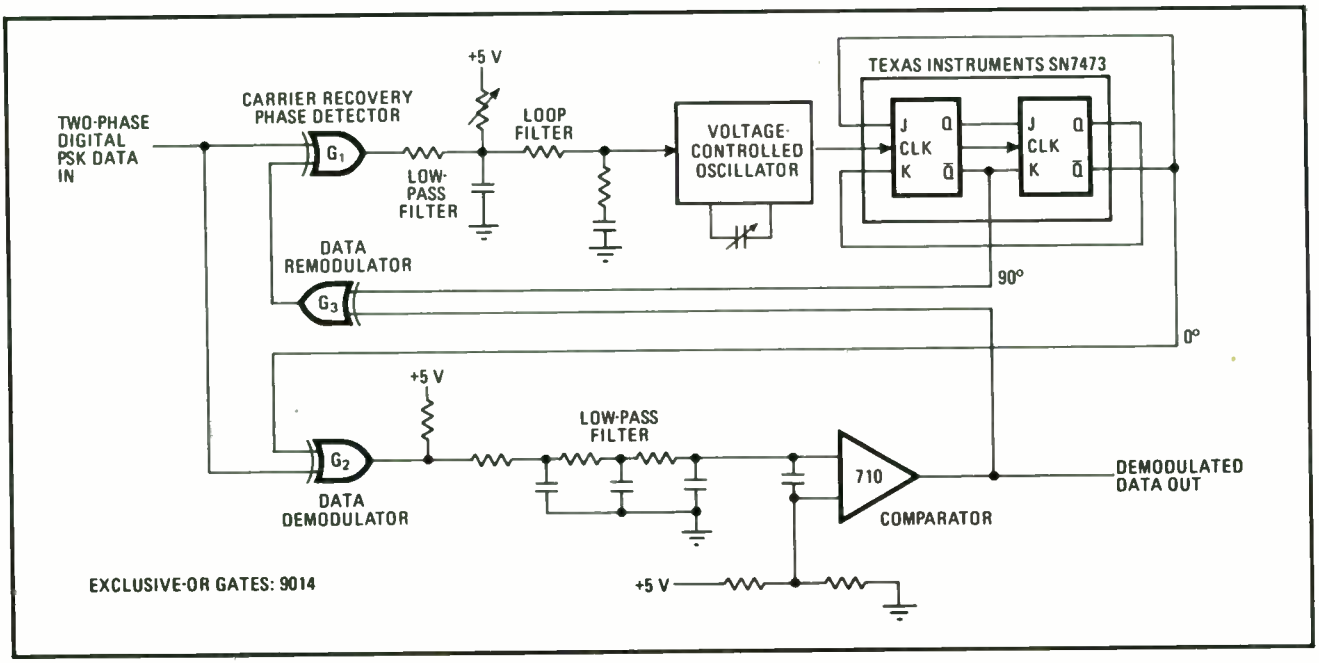
As the phase difference between the input PSK signal and the input VCO signal deviates from its normal 90° shift, the pulse train at gate G_1's output becomes width-modulated. The average dc error voltage then changes, correcting VCO phase and frequency in the direction that reduces demodulation error.

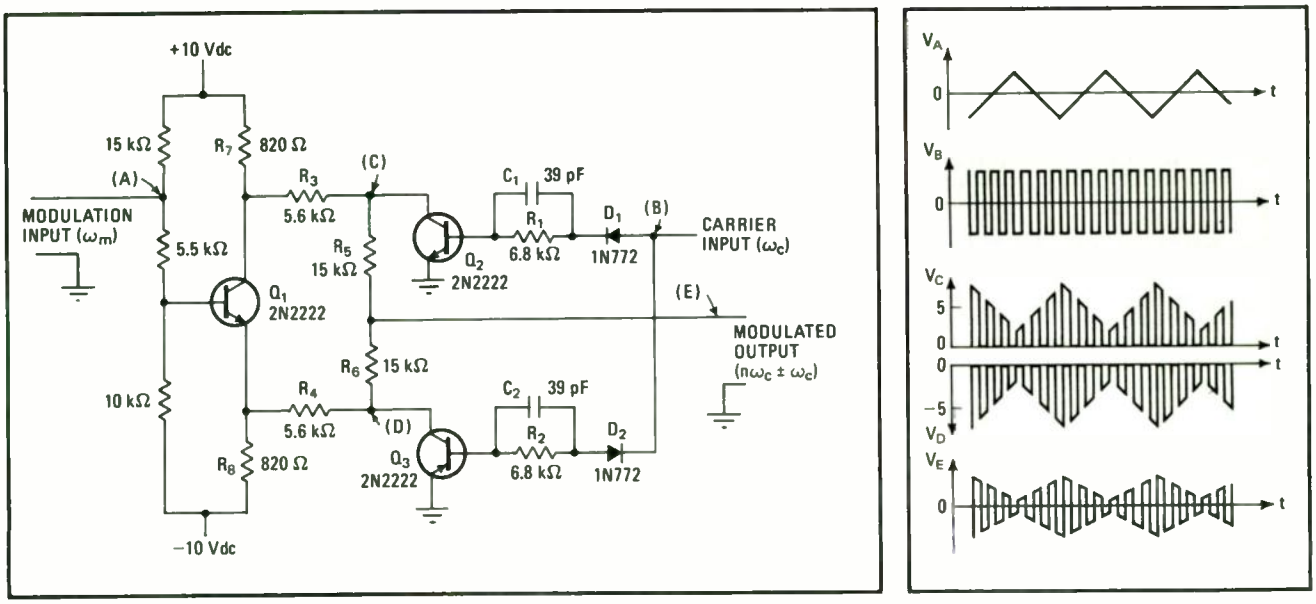
In the circuit's data-demodulator section, the input signal and the VCO output are either mostly in phase or mostly out of phase with each other, depending on the modulation status of the input PSK signal. Therefore, the output of gate G_2 is either logic 0 or logic 1, according to the status of the PSK data.

A second low-pass filter then integrates G_2's gate output signal, which is subsequently squared by the comparator to produce the demodulated output data. This final output signal is also used to modulate the VCO by means of gates G_1 and G_3. □

BIBLIOGRAPHY
C.A. Herbst, "Digital Phase-Locked-Loop with Loss-of-Lock Monitor," EDN/EEE, October 15, 1971.

Unscrambling a binary line. Demodulator for phase-shift-keyed inputs operates exclusive-OR gates as controlled inverters to decode the input data and recover the reference carrier. Input data is remodulated with an error-corrected output from the voltage-controlled oscillator, cancelling out any phase changes from the input modulation. This permits a nearly unmodulated reference carrier to be recovered.





Splitting and chopping. Highly linear amplitude modulator theoretically can operate at half the carrier frequency. Transistor Q_1 splits modulation input into two equal signals that are opposite in polarity and phase. Switch Q_2 passes positive half-cycles of square-wave carrier, while switch Q_3 passes negative half cycles. Chopped modulated signals (points C and D) are then summed by resistors R_5 and R_6.

Amplitude modulator is highly linear

by Donald DeKold
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Besides offering good linearity, an amplitude-modulation circuit can operate at modulation signal frequencies ranging from dc to half of the carrier frequency. At modulation levels as high as 97.5%, the circuit retains its linearity. All signals are directly coupled without inductive or large capacitive elements.

Transistor Q_1 performs as a phase splitter for the modulation signal, which appears at Q_1's emitter with 0° phase shift and somewhat attenuated from its input level. The dc level of the modulation is approximately −5 V dc at Q_1's emitter and +5 V dc at the collector, where the signal is 180° out of phase with the input.

Transistors Q_2 and Q_3 are high-speed switches, driven alternately from saturation to cutoff by the carrier input. This signal, preferably a square wave, is applied to the bases of Q_2 and Q_3 through resistors R_1 and R_2 and diodes D_1 and D_2, respectively. The diodes protect the transistors from excessive reverse base-emitter voltage generated by possible overdrive from the carrier signal. Capacitors C_1 and C_2 speed up Q_2-Q_3 switching times.

The collectors of Q_2 and Q_3 are coupled to the two outputs of phase-splitter Q_1 through resistors R_3 and R_4. These isolate the modulation frequency portion of the circuit from the carrier frequency portion.

The modulation signal appearing at Q_1's collector is switched from its average 5-V dc level to ground by Q_2 on each positive half-cycle of the carrier. A chopped version of the modulation signal then appears at Q_2's collector. Similarly, the modulation signal at Q_1's emitter is chopped by Q_3; Q_3's cutoff-to-saturation transition occurs at each negative half-cycle of the carrier.

Positive and negative chopped modulation signals are then combined by a simple summing network composed of resistors R_5 and R_6. Signal components of the chopped outputs that occur at modulation frequencies are summed to zero. Therefore, under perfectly balanced conditions, the modulated output is spectrally devoid of modulation-frequency components but, of course, contains the modulation sidebands. Theoretically, this permits modulating to an upper frequency limit of one-half the carrier frequency without troublesome filtering problems. The modulation envelope, in this case, is 180° out of phase with the input modulation signal.

The circuit's output is an amplitude-modulated square wave containing harmonics principally at odd multiples of the carrier frequency. (Spectral content is $n\omega_c \pm \omega_m$, where ω_c = carrier frequency, ω_m = modulation frequency, and n = 1, 3, 5, ...) If a sinusoidal carrier is wanted, the output must be filtered. Since modulation frequency components are absent from the output spectrum, a low-pass filter can be employed to select the fundamental carrier frequency and its sidebands. However, a bandpass filter must be used if the output is to be some multiple of ω_c.

Modulator high-frequency performance depends largely on the speed of the switching transistors. For the transistors shown, useful modulated output extends to 1 megahertz. The modulator itself is essentially flat and linear to 250 kilohertz, with visually apparent distortion occurring in the modulation envelope above this frequency. At a carrier frequency of 100 kHz and modulation frequency of 1 kHz, good linear modulation can be obtained to a modulation depth of 95%.

For a modulation input signal of 14 V peak-to-peak, the maximum modulated output level will be 7.4 V peak-to-peak into an open circuit. The minimum carrier input level for a square-wave drive is 2.8 V peak-to-peak. And overdriving does not produce any unde-

sirable effects. The modulation can be any waveform.

A sine wave can be used as the carrier input, but chopping action will not be as good. Minimum sine-wave drive level is 4 V pk-pk. A linear modulation depth of 97.5% can be obtained at a carrier frequency of 10 kHz and a modulation input level of 14 V pk-pk.

Minimum carrier input drive levels remain essentially unchanged at a lower carrier frequency. Modulator performance, however, degrades somewhat at higher output frequencies—maximum linear modulation becomes only 94% at 500 kHz and 88% at 1 MHz. Output level also drops at higher frequencies, but can be improved by using faster switching transistors and lower impedance levels throughout the circuit.

Higher supply voltages offer an alternate method for improving circuit output level. The saturation voltage of the chopping transistors represents the theoretical limit of maximum modulation depth; this voltage becomes less significant when higher supply levels are used. Furthermore, using precision resistor pairs (R_3-R_4, R_5-R_6, and R_7-R_8) assures that positive and negative peak modulation signals are identical at the output. □

Mark/space modulator drives acoustic coupler

by Jack D. Dennon
Computerphone Systems, Renton, Wash.

When data must be transmitted over a voice channel, the circuitry used to translate the logic lows and highs into audio-frequency signals usually includes frequency-trimming potentiometers. But precise enough mark and space audio signals can be obtained from a circuit that uses only standard resistor and capacitor values, provided the supply voltage is well-regulated.

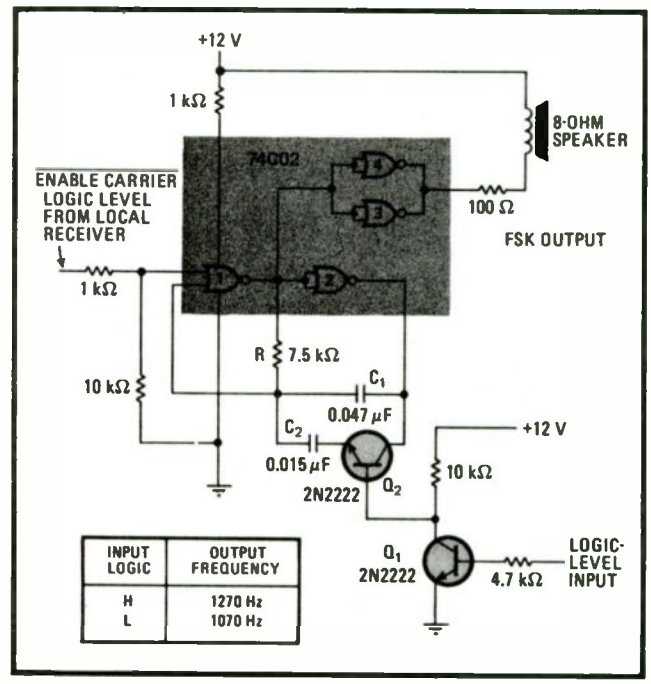
The circuit shown translates serial logic-level data into audio-frequency analog frequency-shift-keyed signals for transmission by telephone, radio, or other voice channels. The modulation function, including provision for a logic-level data input and an active-low enable-carrier input, is implemented with a single complementary-MOS 74C02 quad NOR gate. The output buffer, which consists of gates 3 and 4 of the integrated circuit, has four n-channel transistors paralleled to ground for driving an 8-ohm speaker. The speaker provides acoustic coupling to a telephone handset.

Logic low at the data input turns off transistor Q_1 and turns on transistor Q_2. With Q_2 on, C_2 is switched into the circuit. The frequency of the audio oscillator, made from gates 1 and 2 of the integrated circuit, is proportional to $1/RC$ where $C = C_1 + C_2$. Switching C_2 into the circuit causes the output frequency to shift from K/RC_1 to $K/R(C_1+C_2)$ where K is a constant. With the component values shown, K/RC_1 = 1,269 hertz, and $K/R(C_1+C_2)$ = 1,052 Hz. These frequencies have been found to be sufficiently close to the specified 1,270-Hz mark frequency and 1,070-Hz space frequency for reliable transmission at a data rate of 110 bits per second to a Bell 103 dataset.

The circuit draws about 30 milliamperes from a regulated 12-volt supply. With appropriate changes in the values of components R, C_1, and C_2, supply voltages from 6 to 15 V can be used.

The enable-carrier input to the modulator is driven from a companion receiver circuit to complete the "handshake" sequence at the beginning of a data call; that is, the local receiver asserts the active-low enable carrier shortly after it first hears the 2,225-Hz marking tone coming from the dataset at the other end of the phone line.

Bell 103 line protocol calls for frequency-division-multiplexed simultaneous two-way transmission. The modem originating the call sends 1,270-Hz mark and 1,070-Hz space frequencies and receives 2,225-Hz mark and 2,025-Hz space frequencies from the answering dataset. At the beginning of the call, the answering dataset immediately places its 2,225-Hz mark signal on the line. On a long-distance call, this tone should be allowed to reside alone on the line for at least 400 milliseconds to disable any one-way-at-a-time devices (echo suppressors) on the telephone trunk lines. □



FSK modulator. C-MOS quad NOR gate is audio-signal generator and output driver/buffer for transmitting data over voice channel by frequency-shift-keyed audio signals. The logic-level enable-carrier input must be taken low for the modulator to operate; this input is driven by the local receiver and is used to properly sequence the initial exchange of signals called "handshaking." The enable carrier should be taken low about half a second after the dataset at the other end of the line answers the call with its 2,225-Hz marking tone.

Low-distortion modulator tests hi-fi a-m tuners

by M.J. Salvati
Sony Corp. of America, Long Island City, N.Y.

Most commercially available signal generators do not hold distortion to a level that is low enough to test the frequency response and distortion characteristics of the a-m tuners found in today's high-fidelity equipment. The amplitude modulator shown, however, supplies amplitude-modulated rf signals at a distortion level of less than 0.15%.

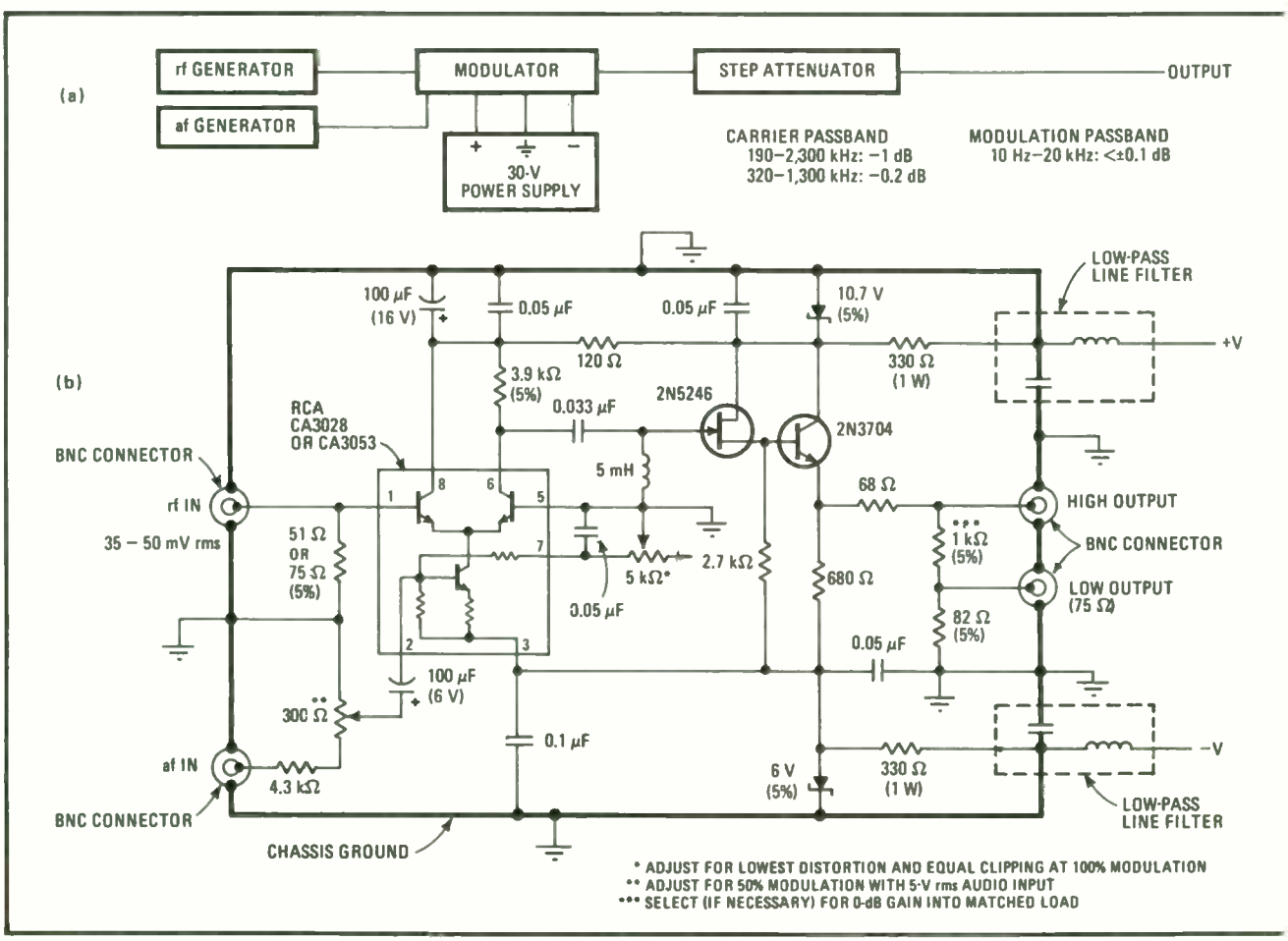
As indicated in the block diagram (a), the modulator (b) is used in conjunction with standard radio-frequency and audio-frequency signal sources. The output level of the over-all test system can be adjusted exactly with the step attenuator that follows the modulator and the vernier level control that is generally included on the rf generator. Also, the modulator gain (for the low-impedance output) can be set at 0 decibels into a matched load, allowing the absolute value of the system's output level to be easily read out from the step attenuator setting and the rf-generator setting.

The rf carrier, which has a root-mean-square amplitude of 35 to 50 millivolts, is applied to the differential input of the IC differential cascode amplifier. And the af signal drives the current-source transistor for this IC's differential transistor pair. Since the current-source transistor controls the gain of the differential pair, the af signal can vary the instantaneous gain of these two transistors, producing up to 100% amplitude modulation of the carrier signal.

The modulated carrier is coupled to the source-follower/emitter-follower combination through a high-pass filter, so that just the carrier and sidebands appear at the circuit's output. The source-follower/emitter-follower combination is essentially an impedance transformer that provides a large current gain for driving low-impedance loads.

The modulator's low output has an impedance of 75 ohms, which can easily be changed to 50 ohms. The circuit's input impedance can also be either 50 or 75 ohms, depending on the value chosen for the input resistor. The high output can drive a low-distortion detector for adjusting or evaluating modulator performance.

Output percent modulation can be indicated by the output-level setting of the af generator (a Krohn-Hite 4100A, in this case) by calibrating the circuit. Although the IC amplifier requires only a 400-mV input for 100% modulation, the modulator can be calibrated with the



Checking out a-m tuners. Amplitude modulator produces less than 0.15% total harmonic distortion. Equipment setup (a) shows that modulator (b) requires only one power supply. Integrated differential cascode amplifier accepts rf carrier input, as well as af modulation input, giving modulated carrier at its output. Combination source-follower/emitter-follower provides high current gain for driving low-impedance loads

300-ohm potentiometer. Here, the circuit produces 10% modulation per volt rms of the af input.

The modulator exhibits only 0.11% total harmonic distortion when providing 30% modulation for a 400-hertz af input and a 1-megahertz rf carrier having an amplitude of 50-mV rms. Only a single 30-volt power supply is needed—neither its positive nor negative terminals is grounded. □

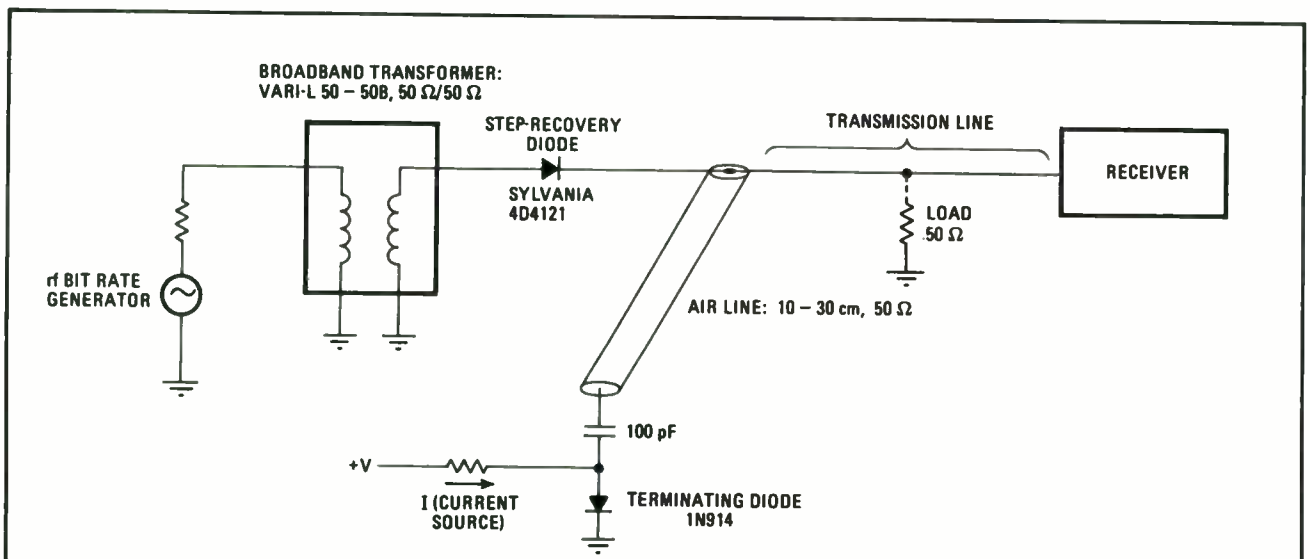
Coherent phase modulation attains data rates of 100 MHz

by Roland J. Turner
General Electric Co., Space Division, King of Prussia, Pa.

Though phase-modulation schemes have till now been limited to modulation rates at video frequencies of 5 megahertz or less, a new technique permits 100- to 200-MHz data rates. The key is an ordinary step-recovery diode that produces a three-level phase code by the simple means of varying the reflection coefficient of the transmission line.

In the modulation setup shown in the figure, the short air line is terminated with an rf diode, whose state determines the reflection coefficient of the transmission line. The state of this terminating diode is established by its drive current. A type 1N914 device is used here, but a hot-carrier or p-i-n diode could be used instead.

The step-recovery diode generates an impulse function each time the input rf sine wave passes through zero in the negative-going direction. This impulse function, which occurs at the input rf bit rate, establishes the



MODULATION	OUTPUT	PHASE SPECTRUM	FREQUENCY SPECTRUM
NONE (REFERENCE 0° PHASE)	T	π/2, π, 0, 3π/2	F(ω), ω, 0, 6π/T, 2π/T
LOGIC 0 (90° PHASE SHIFT)		π/2, π, 0, 3π/2	F(ω), ω, 0, 6π/T, 2π/T
LOGIC 1 (180° PHASE SHIFT)	A	π/2, π, 0, 3π/2	F(ω), 2π/A, 4π/T, ω, 0, 2π/T

High-speed transmission. Data can be transmitted at rf rates of 100 to 200 megahertz with this coherent-phase-modulation scheme. A three-level phase code is set up by changing the reflection coefficient of the transmission line by means of the terminating diode at the end of the air line. The step-recovery diode acts as a waveform generator, producing impulse, doublet, and square-wave functions.

setup's reference phase (no modulation). For this case, the transmission line is terminated in its characteristic impedance, and there is no reflection. Therefore, the reference phase is represented by a 0° phase shift.

As the sine-wave drive signal reverse-biases the step-recovery diode, this device's capacitance drops radically. However, because of the minority-charge storage in the diode, the current charge is not neutralized quickly, and it forces the voltage across the diode to rise very rapidly. The result is an impulse function that lasts only 1 to 2 nanoseconds.

When there is a logic 0 at the end of the air line, this line is terminated in an impedance that's low in relation to the characteristic impedance of the transmission line. The reflection coefficient now is −1, and a doublet waveform is produced at the step-recovery diode. The phase difference between the impulse and doublet waveforms is 90°.

When there is a logic 1 at the end of the air line, this line is terminated in a high impedance with respect to the characteristic impedance of the transmission line. The reflection coefficient becomes +1, and the step-recovery diode generates a double-width square wave, which is 180° out of phase with the reference impulse function.

The three waveforms form a flat comb spectrum with coherent phase modulation on all spectral lines. This means that the phase from one spectral line to the next remains the same. The coherent phase modulation can be used to represent a three-level code in the phase domain.

The 0° phase, which is represented by the impulse function, can be used in a passive receiver to demodulate the other two discrete phases—the 90° and 180° shifts produced by the doublet and square-wave functions. These latter two phases can then represent a binary code in the phase domain that provides coherent phase modulation on all spectral lines of the comb spectrum. For an rf bit rate of 100 MHz, a spectral line will occur at multiples of 100 MHz, up to about 1 gigahertz.

With this type of phase coding, data can be transmitted at half the rf bit rate. For example, if the basic rf bit rate is 100 MHz, information can be transmitted at 50 million bits per second. Additionally, the redundant coherent reception on the many spectral lines makes the receiver immune to Johnson or man-generated noise.

The modulation scheme can also be used for a broadband rf impulse noise jammer by modulating the current of the terminating diode with white video noise. Or, it can be the basis for an rf test function generator for evaluating the transient response of communication subsystems to complex excitation.

The output amplitude of the modulation circuit is 1 volt peak into 50 ohms for the impulse and square-wave functions and 2 V, peak to peak, into 50 ohms for the doublet function. □

FSK modem interfaces cassette and computer

by John I. Compton
Wenner-Gren Laboratory, University of Kentucky, Lexington, Ky.

Serial data from a teleprinter or serial output from a computer can be recorded and played back from cassette tape with the frequency-shift-keyed modulator/demodulator described here. The circuit may also be used as a half-duplex modulator/demodulator to store data or read it out over a telephone line. The system is crystal-controlled, operates at standard FSK frequencies, and needs no adjustment. It can be operated from 5 to 15 volts and costs less than $15 to build.

The block diagram in Fig. 1 shows the principle of the modem circuit, and details are given in Fig. 2.

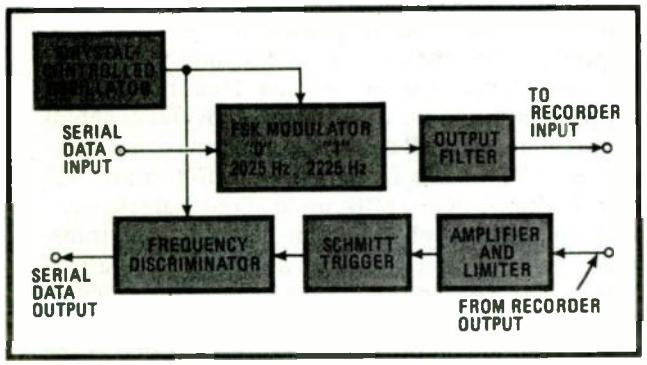
What happens is this. A 14-stage 4020 C-MOS counter is reset to zero when one of two diode arrays, selected by the serial input, decodes a count of 424 for a logical 1 and 464 for a logical 0. In this manner the output frequencies, at Q_9, will be the clock frequency of 950 kilohertz divided by 424 and 464, or 2,240 and 2,047 hertz, respectively. This gives 2,240 Hz for a logic 1 and 2,047 Hz for a logic 0. The resulting square wave is filtered and ac-coupled to the auxiliary input of the recorder. The 4013 D latch on the counter reset prevents false resets that might otherwise be caused by ripple outputs between leading edges of the clock.

Record and play do not occur at the same time, so that the same C-MOS counter can be used in both the modulator and the discriminator. When retrieving data, the recorder's "ear" output is ac-coupled, amplified, and Schmitt-triggered by two Norton amplifiers (National LM3900), and finally shaped by a 4013 D latch. The re-

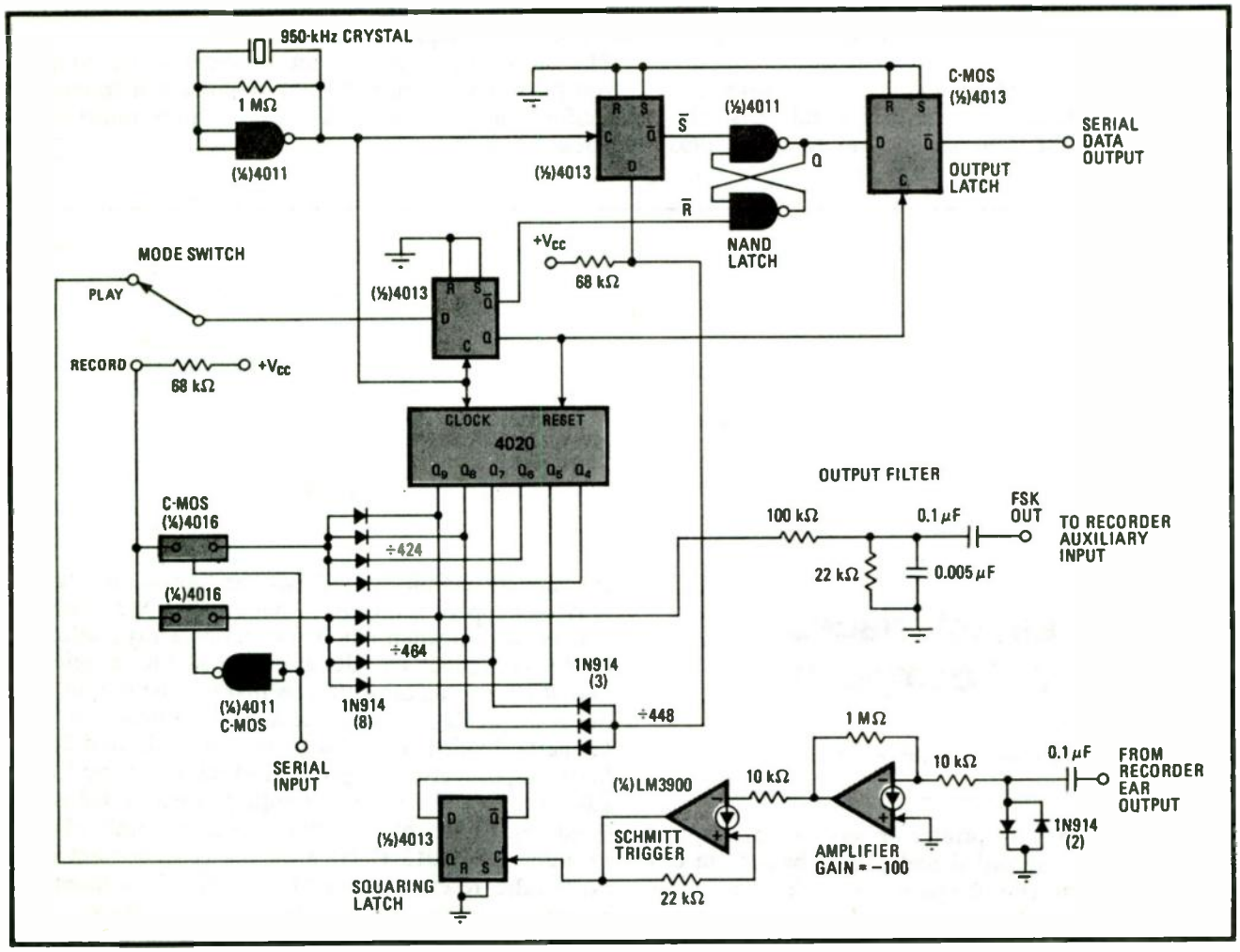
sulting wave form is used for clocking a toggle flip-flop.

The output of the flip-flop stays high for a time equal to one cycle of the recorded data and, with the mode switch in the play position, allows the counter to count system clock pulses for one input period. Then, when the counter has counted a period longer than 472 microseconds, or a frequency of below 2,120 Hz, a three-diode array (decode 448) has an output of 1 and as a result the C-MOS NAND latch is set. At the end of the input period the output latch is set and a logical 1 will appear on the $\overline{Q}$ output line. If the input frequency is higher than 2,120 hertz, the latch does not set, and a logic 1 will appear on the output line. The serial output, which is valid during record and play, provides automatic echo for teletypewriter use. However, the FSK output is valid only while in record mode.

This circuit has recorded and played back an 18,000-character (30-minute) test tape at 110 baud without a single error. A baud rate of 300 can be used with good-quality tape. The recorder can be low quality, however, because this frequency shift allows a 5% tape speed variation without error. Even greater speed variation can be allowed if the frequency shift is larger. □



1. Taping the digits. Modem circuit converts serial digital data to FSK signal for cheap storage on cassette tape, and also converts the taped signal back to digital form for re-entry into a computer or other digital system. The FSK signal can be sent over telephone lines. This circuit can handle a baud rate of 300 without difficulty.



2. How to modem. The heart of this circuit is the 4020 14-bit C-MOS counter. In the record (modulate) mode, the counter divides the 950-kHz crystal frequency by 424 to put out 2,240 Hz when the input digit is a logic 1, and divides by 464 to put out 2,047 Hz when the input is logic 0. In the playback (demodulate) mode, the 4020 determines the incoming frequency by counting clock pulses during one period; a long count, corresponding to the lower frequency, signals a logic 0, and a short count yields a logic 1. All C-MOS components are available from several manufacturers. Other crystal frequencies in the range 0.5–4 MHz can be used if diode code is changed to decode the proper count.

Binary rf phase modulator switches in 3 nanoseconds

by Roland J. Turner
AEL Communications Corp., Lansdale, Pa.

By employing a diode-steered current source, binary rf phase modulation is accomplished by translating transistor-transistor-logic levels to a bidirectional current drive in less than 3 nanoseconds. The rf modulator is intended to provide phase coding and correlation in jamming-resistant radar and secure communication links, where transmission and reception are essential in a hostile environment.

The binary (0° and 180°) phase modulation is effected by switching Schottky diodes in a ring modulator at high video/i-f rates. These high data rates require TTL signal levels to be translated to a ±15-milliampere current drive for the ring modulator in extremely short time intervals. The complete binary rf phase modulator consists of the video driver (a), which employs stripline techniques, and the ring modulator (b).

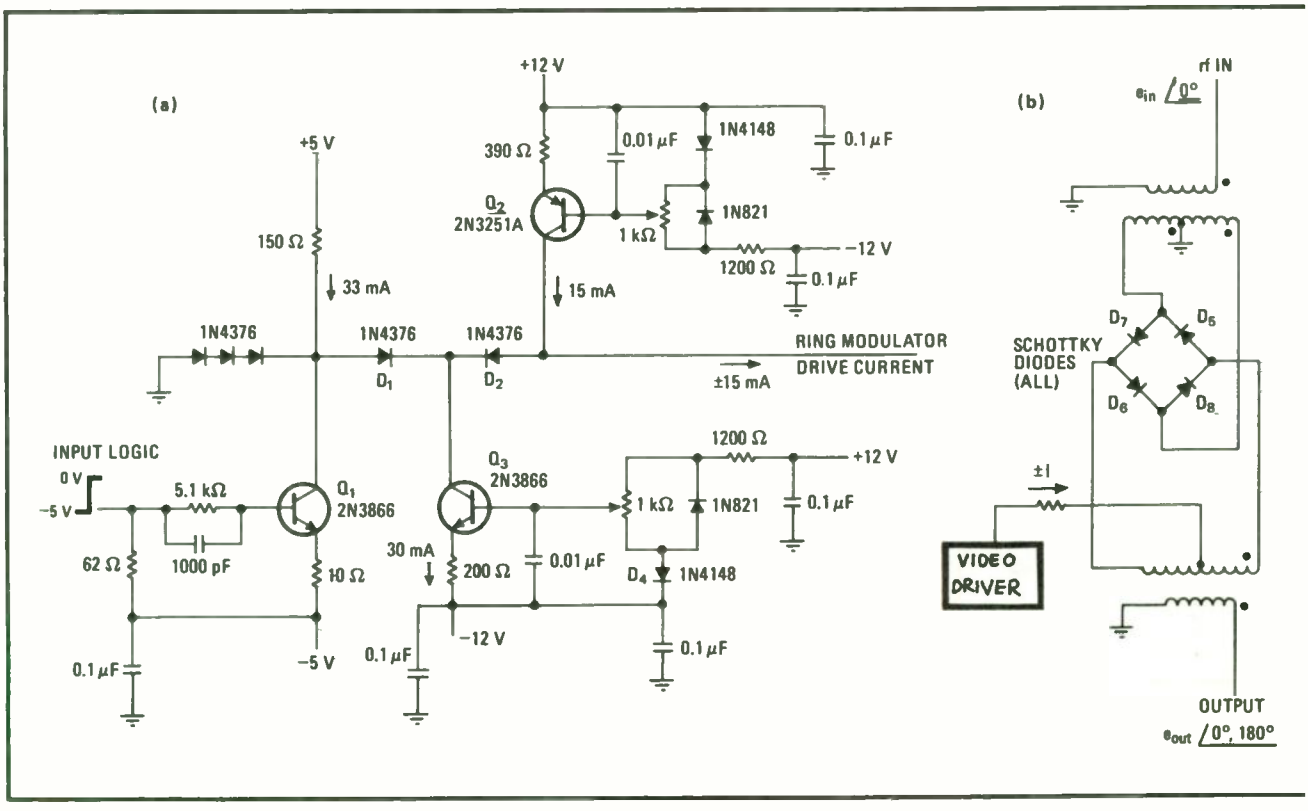
When the input logic level to the video driver is at −5 volts, transistor Q_1 is off, diode D_1 is on, and diode D_2 is off. This forces current source Q_2 to deliver 15 mA to the ring modulator. When the input logic level increases positively from −5 V to 0 V, transistor Q_1 turns on, reverse-biasing diode D_1 so that this device turns off. Diode D_2 now turns on, and current source Q_3 forces 15 mA to be drawn from the video port of the ring modulator. The i-f/rf signal phase is then shifted by 180° as it passes through the ring modulator.

This binary phase modulation is accomplished in only 3 ns because the current sources can force rapid charging of any circuit capacitance. Also, load-circuit switching is forced by impressing a large negative or positive voltage on diode D_1. Since D_1's switching voltage transition is low relative to the drive voltages, switching can be done in a small time interval. (Current sources Q_2 and Q_3 are temperature-stabilized by diodes D_3 and D_4.)

The switching current from the video driver is applied to the video port of the ring modulator. When the driver supplies current (+I) to the video port, Schottky diodes D_5 and D_8 conduct, and the output phase is 180°. When the driver sinks current (−I) from the video port, Schottky diodes D_7 and D_8 are forced to conduct, and the output phase is 0°.

This switching technique is quite useful in applying coded rf phase modulation to an interrogating radar or in applying secure modulation to a secure communication link. The system then becomes very difficult to jam since correlation reception at the receiver enhances detection and suppresses the effects of noise, whether the noise source is Johnson noise or intentional noise jamming. □

Reversing phase at radio frequencies. Phase modulator switches phase of rf signals between 0° and 180°. Video driver (a) translates TT inputs to bidirectional switching current for Schottky-diode ring modulator (b) in under 3 nanoseconds. The driver employs diode-steere current sources (transistors Q_2 and Q_3) to supply or sink 15 milliamperes for the video port of the ring modulator.



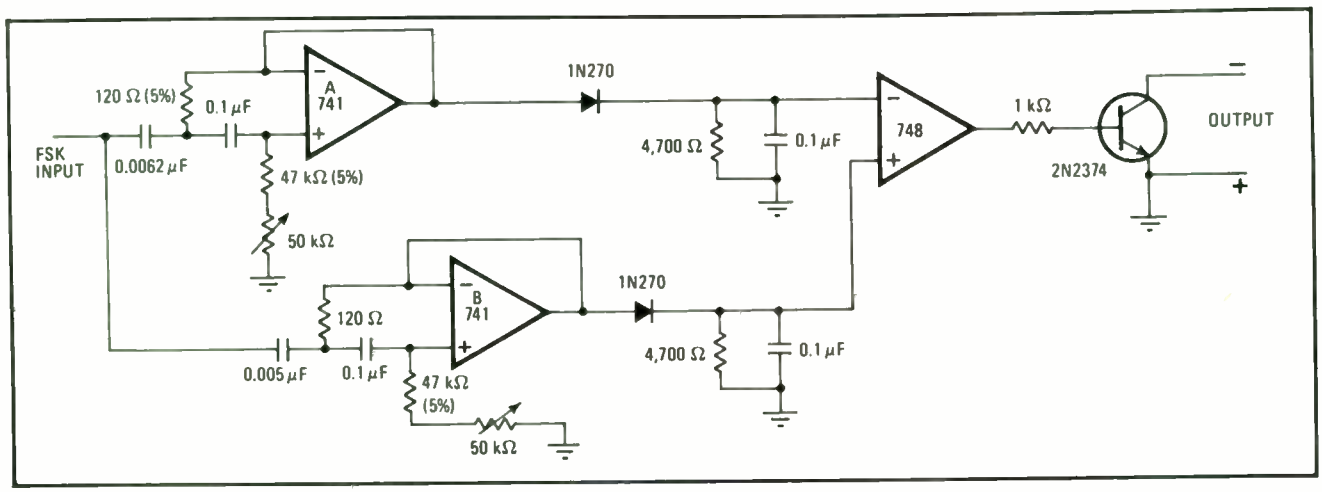
Mark/space demodulator employs active filters

by Michael J. Gordon, Jr.
Psynexus Systems, Wilmette, Ill.

If active filters are used instead of LC-tuned circuits, a frequency-shift-keyed demodulator can be made smaller in size and its performance improved. The active filters eliminate the need for bulky and expensive inductors. The circuit is designed for demodulating 110-baud FSK data. It operates in the originate mode, where a mark equals 2,225 hertz and a space is 2,025 Hz.

When a mark is received, filter B, which is tuned to 2,225 Hz, passes the signal while filter A attenuates it. The outputs of the two filters are then converted to dc and compared by an op amp that is operated in its open-loop mode. Since the output of filter B is sampled by the op amp's noninverting input, the circuit's output transistor is kept in saturation so that the circuit loop is closed. When the input frequency shifts to a space, filter A passes the signal while filter B attenuates it, causing the circuit loop to remain open.

To adjust the circuit, an audio signal is applied at the mark and space frequencies, and the desired peak output produced by varying the two 50-kilohm trimmers. An approximate peak-to-peak voltage of 1.2 volts is required from a low-impedance source. □



Going active. Frequency-shift-keyed demodulator contains two active filters, saving space and improving performance over designs that use conventional LC-tuned circuits. Filter A passes the space frequency of 2,025 hertz, while filter B passes the mark frequency of 2,225 Hz. The op amp operates open loop, summing the filter outputs. For a mark input, the output transistor saturates so that circuit loop closes.

Fast-switching modulator reverses uhf signal phase

by R.N. Assaly
Massachusetts Institute of Technology, Lexington, Mass.

In just a few nanoseconds, a modulator for shaping transmitted ultrahigh-frequency radar signals can switch a signal through three states. The signal can be turned on or off, and while it is on, the phase can be reversed between 0° and 180°. An off signal is attenuated by at least 35 decibels.

The modulator (a) consists of a tri-state driver and a double-balanced mixer, which allows the rf signal to be controlled by video commands. Three values of control current— −30 milliamperes, 0 mA, and 30 mA— are generated by the driver for the three modulator states— 0° phase, off, and 180° phase, respectively.

The transition times of the two input logic signals, designated as code Q and gate P, are enhanced by a dual four-input AND gate. (The gate-P input turns the rf

signal on and off, performing a gating function; the code-Q input reverses the phase of an on signal, thereby coding signal phase.) A line driver then produces the outputs labeled A and B:

$A = \overline{PQ}$ and $B = \overline{PQ}$

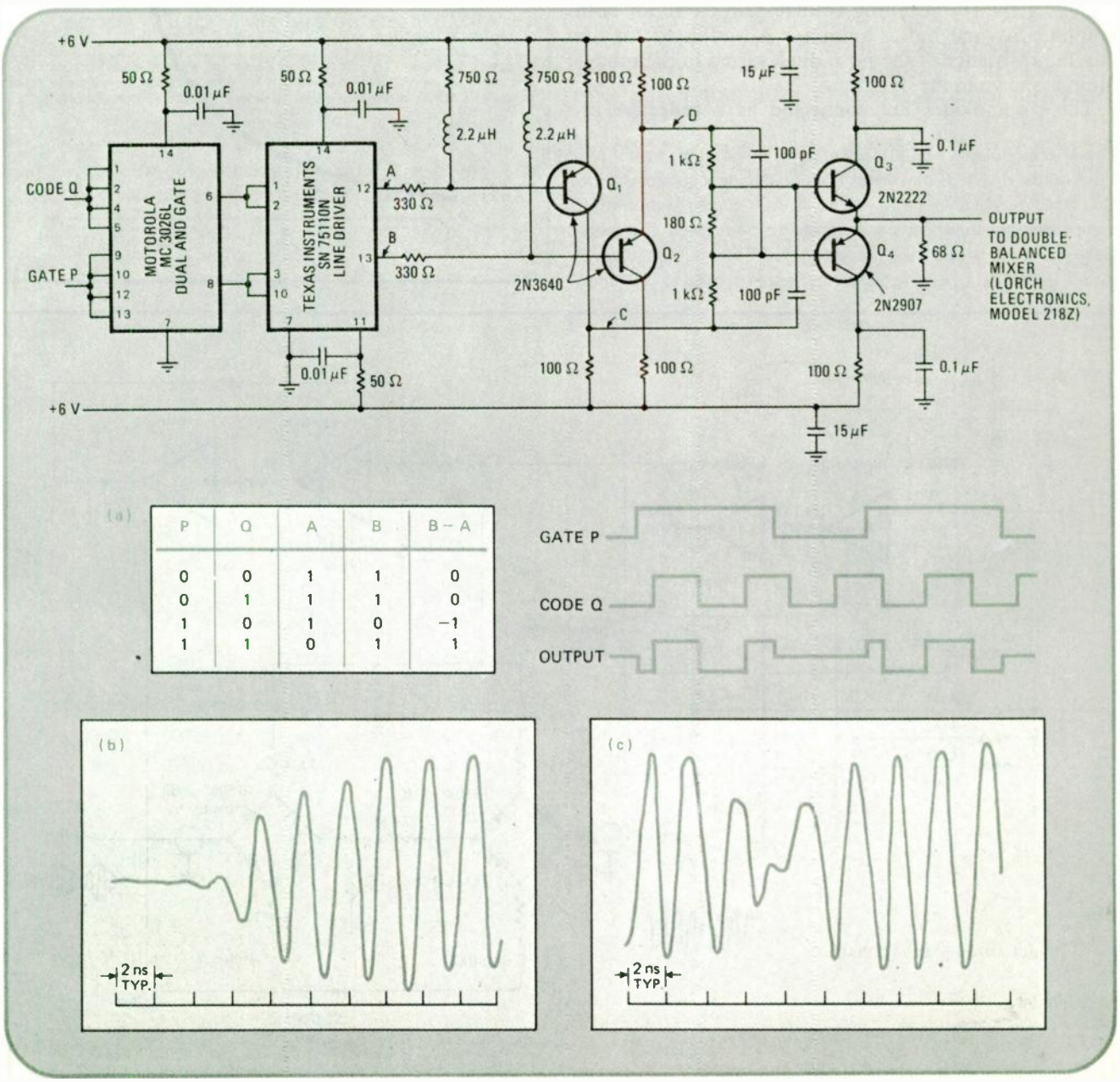
At the tri-state driver output, a difference signal, B–A, is used to provide the three desired states, as shown in the truth table.

To obtain this difference signal, transistor Q_1 inverts the A output of the line driver to produce signal C. And output B passes through transistor Q_2 without inversion, keeping the circuit balanced and resulting in signal D. A resistor network averages signals C and D, which are then applied to output transistors Q_3 and Q_4 that drive the double-balanced mixer.

Since Q_3 and Q_4 do not conduct if their base voltage is less than 0.6 volt, the resistor network holds bias voltage to about 0.5 V during the off state to reduce any delay during driver state transitions. Also, because a large base voltage must be applied either to Q_3 or Q_4 for conduction to occur, mixer current can be held to a very low value. If mixer current increases, to even just a few microamperes, the attenuation of an off signal becomes less than the desired 35 dB. For instance, attenuation degrades to about 30 dB when mixer current becomes approximately 10 microamperes.

Inductors and capacitors in the circuit are simply used to speed up state transitions. The turn-on of a 430-megahertz signal is illustrated in (b), while (c) shows a phase reversal. These transitions took less than 10 ns.

Uhf modulation. Three-state modulator (a) turns off uhf signals or reverses their phase between 0° and 180°. AND gate improves input signal transitions. To balance circuit, line driver output A is inverted by Q_1, while B passes through Q_2 without inversion. Transistors Q_3 and Q_4 drive mixer with difference signal of B–A. Turn-on (b) and phase reversal (c) traces are for 430-megahertz signal.



Variable-gain amplifier yields linear rf modulator

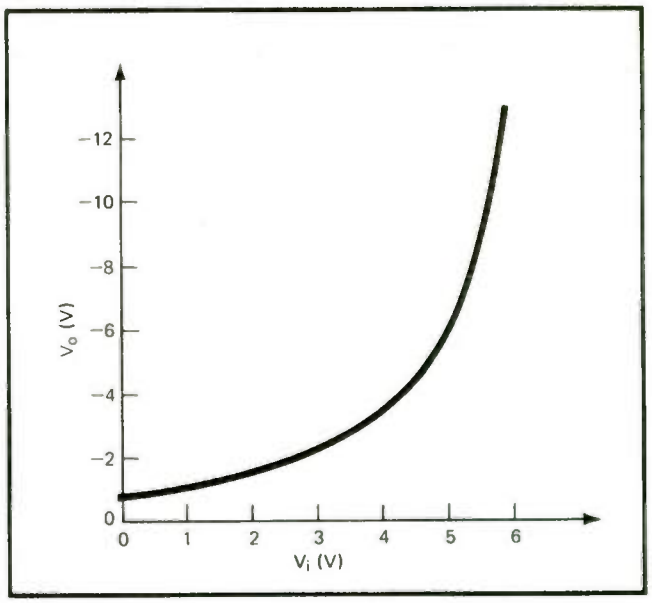
by Michael F. Black
Equipment Group, Texas Instruments, Dallas, Texas

An rf modulator that offers a linear relationship between input control voltage and output rf voltage can be achieved by using a variable-gain amplifier to compensate for the nonlinear characteristics of a p-i-n diode attenuator. Circuit operation remains linear for an input-signal range of approximately 30 decibels.

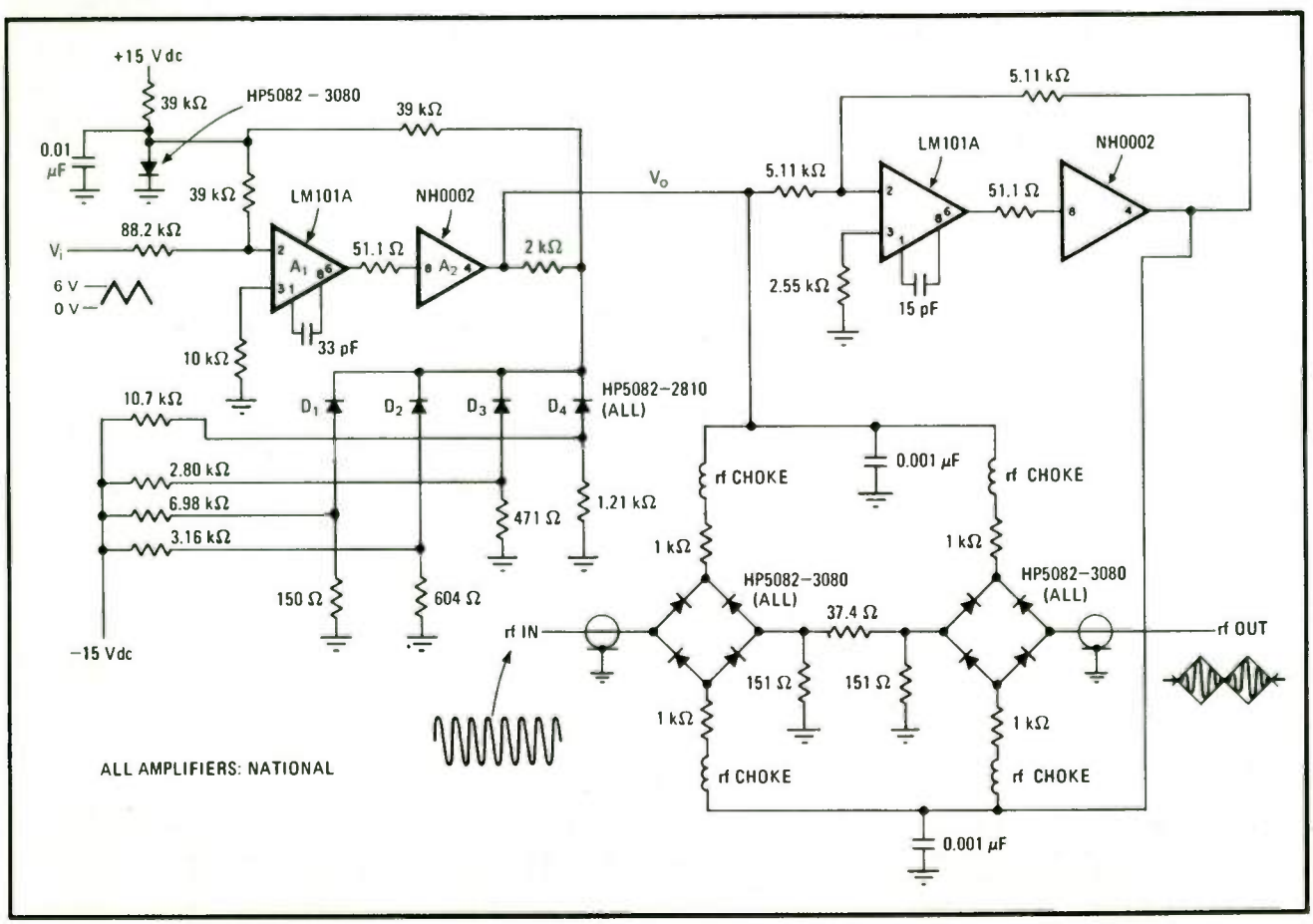
The gain of amplifier A_1 depends on the level of input control voltage V_i. As this modulation voltage increases, diodes D_1 through D_4 conduct, shunting some of A_1's feedback current to ground and raising this amplifier's gain. The resulting voltage-gain curve for both amplifier A_1 and buffer amplifier A_2, adjusted for the varying resistance of the p-i-n diodes used in the modulator, is shown in the diagram.

The p-i-n diodes are connected as a reflective attenuator that has inherent dc balance and offset characteristics to minimize ringing and transient effects. Here, a pad is placed between the two attenuator sections for isolation purposes, but an amplifier can be substituted for the pad if desired.

The values of the attenuator rf chokes are determined by the operating rf carrier frequency and the upper modulation frequency. The circuit performs well from 60 to 150 megahertz, with modulation frequencies as high as 250 kilohertz. □



Linear rf modulator. For 30-decibel signal range, rf modulator provides output rf voltage that varies linearly with input control voltage. Combined gain of amplifier A_1 and buffer A_2 is curved (as shown) to compensate for nonlinear characteristic of p-i-n diode attenuator. Gain is varied by partially grounding feedback current through diodes D_1 and D_4. Operating frequency ranges from 60 to 150 MHz.



31. Multiplexers

Gated MOSFET acts as multiplexing switch

by Glen Coers
Texas Instruments, Dallas, Texas

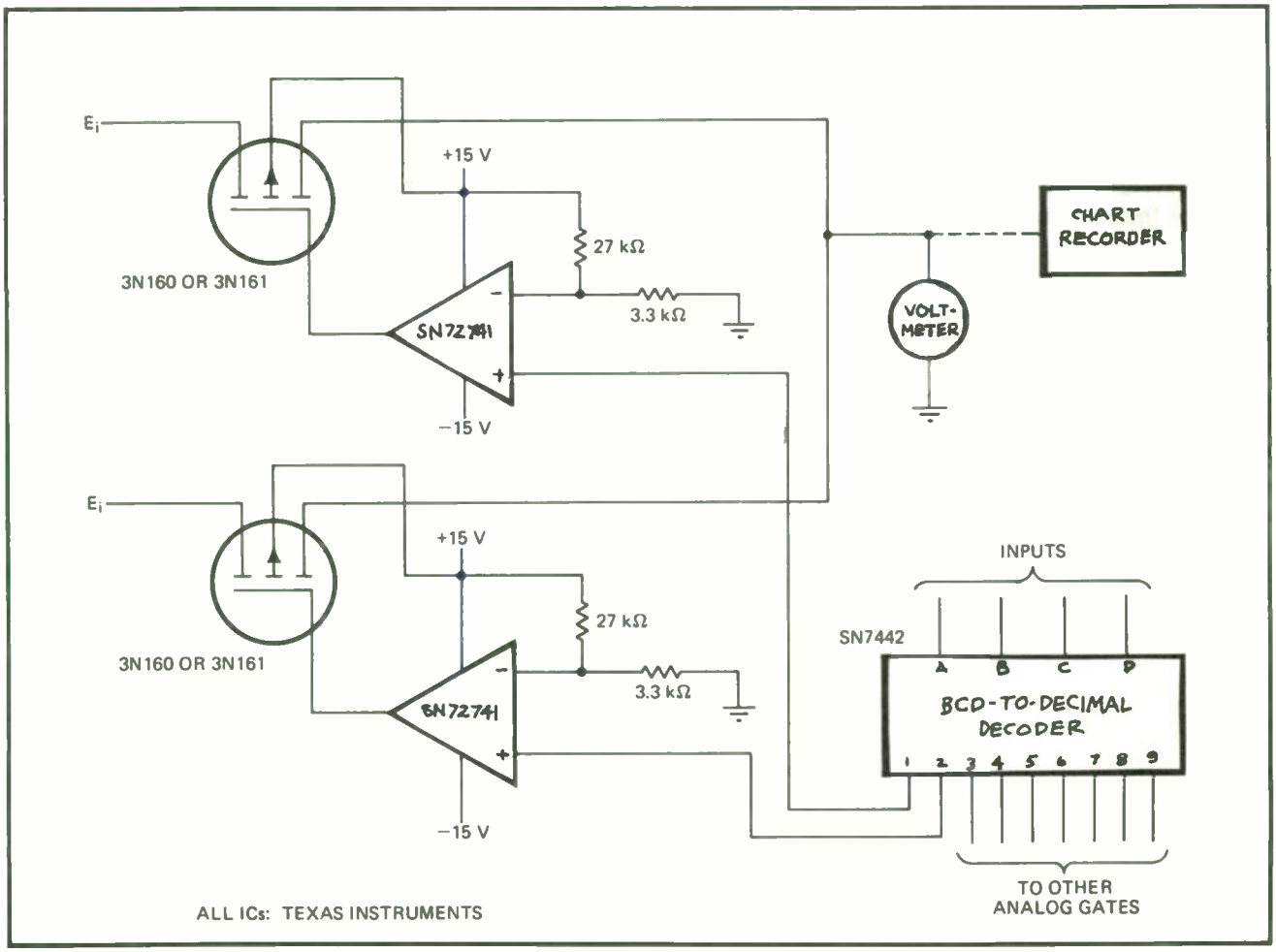
A four-terminal MOSFET makes a handy series analog gate for time-multiplexing either ac or dc signals. An array of these MOSFETs can, for instance, be used to gate a number of voltages that are being monitored periodically by a chart recorder or a voltmeter, as shown in the figure. Here, the BCD-to-decimal decoder switches one MOSFET analog gate at a time for a given interval before switching another.

The decoder outputs are high except for the output number being decoded. An operational amplifier, connected as a comparator, is used to switch each MOSFET on and off. Each comparator's inverting input is set to a dc reference voltage of approximately 1.6 volts.

When a logic 0 appears at the selected decoder output, the associated comparator's output goes to −14 V. The MOSFET that is tied to the comparator output then conducts, gating the analog input voltage to the voltmeter or chart recorder. When the decoder output returns to logic 1, the comparator output switches to 14 V, turning off the MOSFET.

Since MOSFETs are bilateral devices, they can handle both positive and negative voltages. For this circuit, the maximum input voltage swing is ±10 V, but can be extended by raising the level of the positive and negative supply voltages that bias the MOSFET's gate terminal. The multiplexer circuit has good isolation and leakage properties. □

MOSFET gate. Analog signals can be gated selectively by using a BCD-to-decimal decoder to switch array of MOSFETs. All decoder outputs are high, except for the one selected to be the output number. When selected decoder output goes low, output of associated comparator also goes low, turning on MOSFET and permitting analog input to pass to circuit's output. Both positive and negative inputs can be gated.



Wired-OR DTL gates increase multiplexer input capacity

by Eric G. Breeze
Fairchild Semiconductor, Mountain View, Calif.

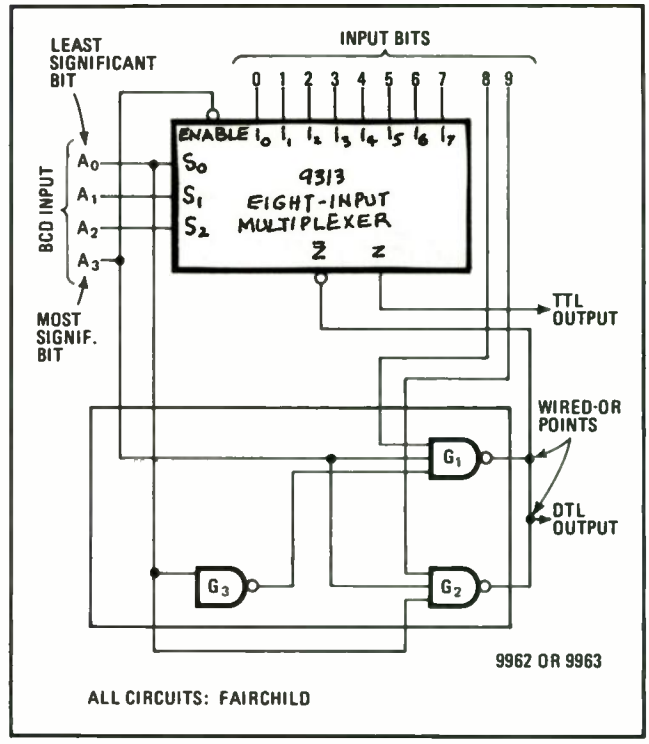
A 10-input multiplexer can be built by adding only one diode-transistor-logic gate package to an eight-input multiplexer that has an open-collector output. Decade multiplexers are not currently available as standard integrated circuits because of the lead constraints of conventional dual-in-line packages. Either an eight-input multiplexer in a 16-lead DIP or a 16-input multiplexer in a 24-lead DIP can be purchased. And modifying the 16-input unit is both an expensive and cumbersome way to build a decade multiplexer.

Only three DTL gates are needed to add two input bits to an eight-input multiplexer, provided the multiplexer has an open-collector output that can be wired-OR like all standard DTL gates. The decade multiplexer illustrated makes use of the OR tie facility of the $\bar{Z}$ output of Fairchild's type 9313 eight-input multiplexer.

The most significant bit of the binary-coded-decimal control input is connected to the ENABLE (active low) input of the multiplexer and to the inputs of gates G_1 and G_2. When the most significant control bit is low (code value of 0 to 7), the multiplexer operates normally, accepting input bits 0 through 7, and G_1 and G_2 are disabled (their outputs are high).

For BCD input selection codes of 8 or 9, the most significant control bit is high, the multiplexer is disabled, and input bits 8 and 9 can pass to the output, since both G_1 and G_2 are enabled. Gate G_3 performs as an inverter for the least significant control bit into the multiplexer to decode input selection code 8.

The type 9313 multiplexer contains an inverter stage after its $\bar{Z}$ output, making both TRUE (Z, TTL-compatible) and ASSERTION ($\bar{Z}$, DTL/TTL-compatible) outputs available. □



Two more bits. Binary-coded-decimal input controls selection of input bits to decade multiplexer. When most significant bit A_3 is low, gates G_1 and G_2 are disabled, and eight-input multiplexer operates normally for input bits 0 through 7. For high A_3 bit, eight-input multiplexer is disabled, but G_1 and G_2 transfer input bits 8 and 9 to output. DTL gates and $\bar{Z}$ output are wired-OR.

32. Multivibrators

Output comparator enhances versatility of one-shot

by Harvey J. Scherr*
Westinghouse Corp., Systems Development Div., Baltimore, Md.

If an operational amplifier is used as an output comparator, a monostable multivibrator can provide wide and accurate output pulses over a broad temperature range. The one-shot is also retriggerable—that is, its output pulse duration can be extended by reapplying the input pulse. In addition, this multivibrator can be reset to accept a new trigger input within its timing period.

Each time an input pulse occurs, timing capacitor C_t is discharged by field-effect transistor Q_1, and comparator A_1 switches off. In the absence of a trigger input, C_t accepts charge from Q_1, and the comparator is turned on. Switching takes place when A_1's input voltages, e_1 and e_2, are equal. Because the comparator is off during the timing interval, there are no output errors introduced by op-amp input offset current.

Output pulse width, T, is determined by the supply voltage, V_{DD}, reference voltage, V_R, and the timing components, R_t and C_t. At the comparator's input:

$$e_1 = e_2 = V_{DD}\exp(-t/R_tC_t)$$

which can be rewritten as:

$$\exp(-t/R_tC_t) = V_{DD}/e_1 = V_{DD}/[V_RR_2/(R_1+R_2)]$$

Output pulse width becomes:

$$T = R_tC_t[\ln(V_{DD}) - \ln(V_RR_2/(R_1+R_2))]$$

If $V_{DD} = V_R$ and $R_1 = R_2$, this equation reduces to:

$$T = R_tC_t\ln(2) = 0.694R_tC_t$$

The timing equations illustrate that output pulse width is completely independent of any transistor junction voltage and therefore is independent of junction temperature dependence. Op-amp offset voltage drift principally determines the one-shot's temperature performance. And since offset drift is typically as low as 10 microvolts/°C, total variation in the multivibrator's timing interval is only about 0.002%/°C.

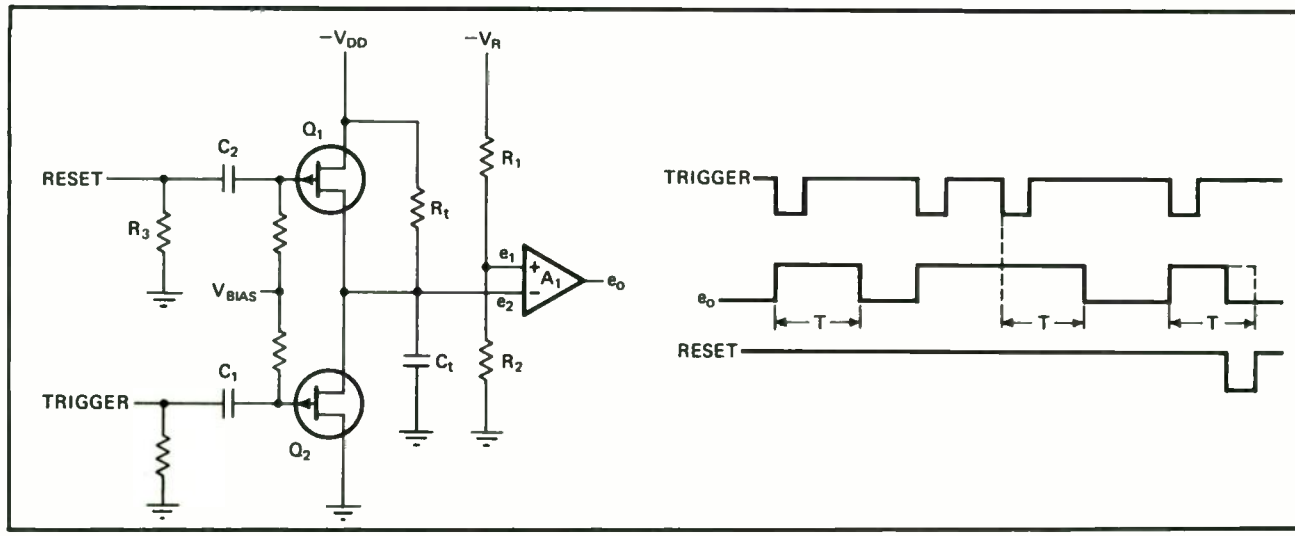
Unusually large time constants can be achieved because the primary restriction on the value of timing resistor R_t is op-amp bias current. R_t must be small enough to allow the voltage developed at A_1's inverting input to turn the comparator on. Since op-amp bias current generally ranges between 0.25 and 0.5 microamperes, resistor R_t can be as large as 10 megohms (when V_{DD} = 10 volts and e_1 = -5 V).

As illustrated in the timing diagram, the multivibrator can be re-initiated during its timing interval to stretch output pulse width. This is possible because transistor Q_1 discharges capacitor C_t every time an input pulse occurs. By adding transistor Q_2, capacitor C_1 and resistor R_3, the circuit can be reset by restoring it to its stable state. A fixed-width reset pulse cancels the remaining portion of the output pulse.

Substituting a resistor for capacitor C_2 alters the multivibrator's timing—a time out then occurs with the absence of a negative voltage from the input terminal. Circuit output polarity is easily reversed by interchanging the connections to the comparator's inverting and noninverting inputs. The active devices used determine component values. □

*Now with Stereo Equipment Sales Inc., Baltimore, Md.

Retriggerable monostable. Input trigger causes Q_1 to discharge capacitor C_t, turning off comparator A_1 and producing output. Before timing period is over, new trigger can be applied to extend output duration. Reset pulse through Q_2 can terminate output during any part of timing interval. Output comparator maintains one-shot temperature stability and permits unusually large time constant to be used.



Multivibrator clock obeys digital commands

by Patrick L. McGuire
General Dynamics, Electrodynamic division, Pomona, Calif.

A simple variable-frequency multivibrator clock source can be made data-dependent by controlling the current into the multivibrator's timing network. When timing resistor values are selected in increments of two (doubling the preceding value), the relationship between binary input and frequency output is linear within 8%.

Inverters with open-collector outputs act as input buffers, providing the necessary pulldown of current from the timing resistors. Diodes are added to prevent signal interference at the inverter outputs.

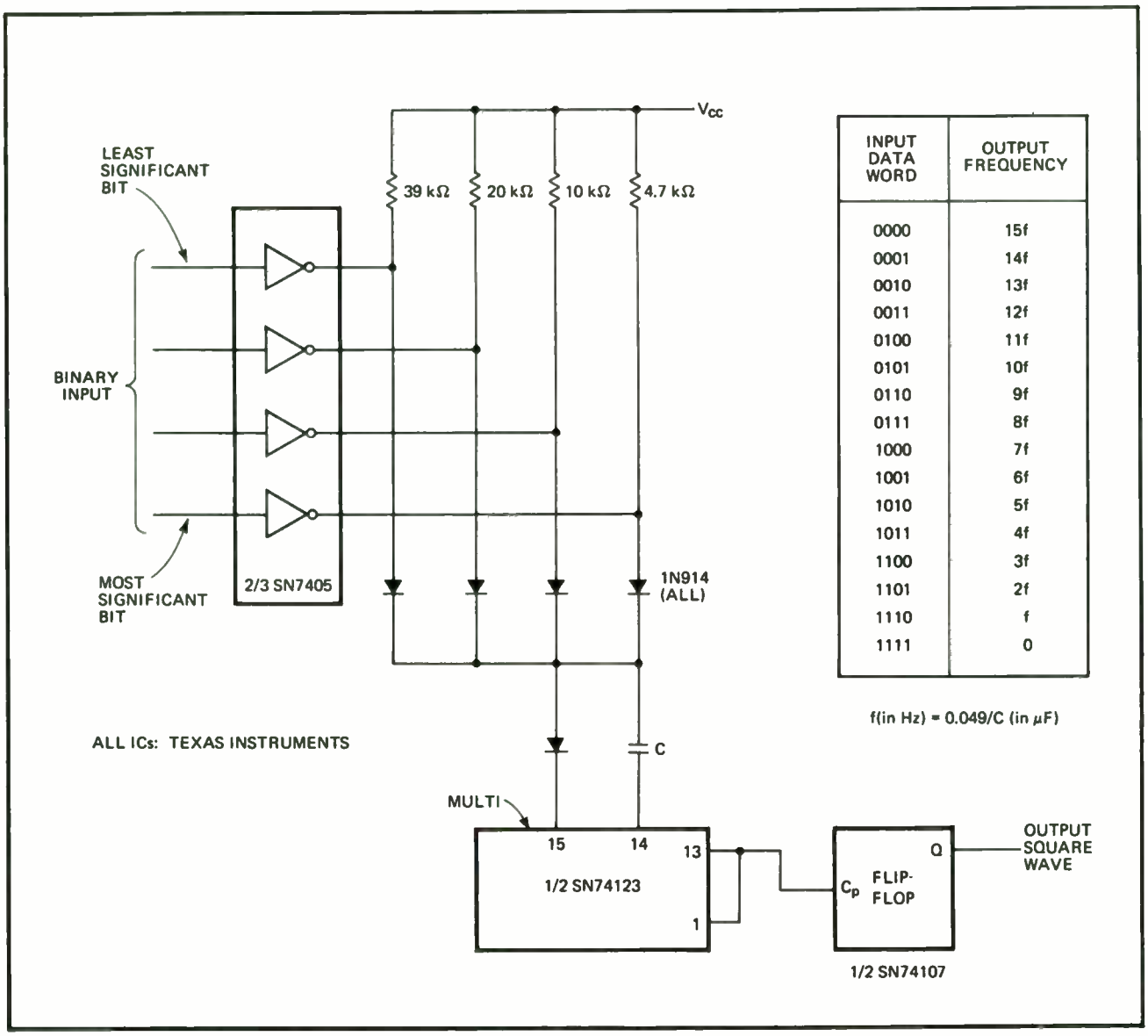
Circuit output is a square wave having a frequency of half the pulse rate from the multivibrator. Output frequency depends on the value of timing capacitor C:

$f = 0.049/C$

where f is in kilohertz and C in microfarads.

The graph shows the multiple of f determined by each input data word. □

Programable clock. Controlling current through multivibrator enables binary input to determine frequency of output square wave. Input/output relationship is practically linear because values of adjacent timing resistors differ by factor of two. Inverters buffer current from timing resistors, while diodes guard against signal interaction between bits. The flip-flop halves output pulse rate from the multivibrator.



INPUT DATA WORD	OUTPUT FREQUENCY
0000	15f
0001	14f
0010	13f
0011	12f
0100	11f
0101	10f
0110	9f
0111	8f
1000	7f
1001	6f
1010	5f
1011	4f
1100	3f
1101	2f
1110	f
1111	0

f(in Hz) = 0.049/C (in μF)

Exclusive-OR gate makes bidirectional one-shot

by Tim O'Toole
Tektronix Inc., Beaverton, Ore.

An exclusive-OR gate is an ideal device for building a bidirectional one-shot by running the same signal into both gate inputs, but putting a time delay on one of the inputs. The gate will then produce a pulse for every rising or falling edge of the input signal, and the width of the pulse is determined by the time delay.

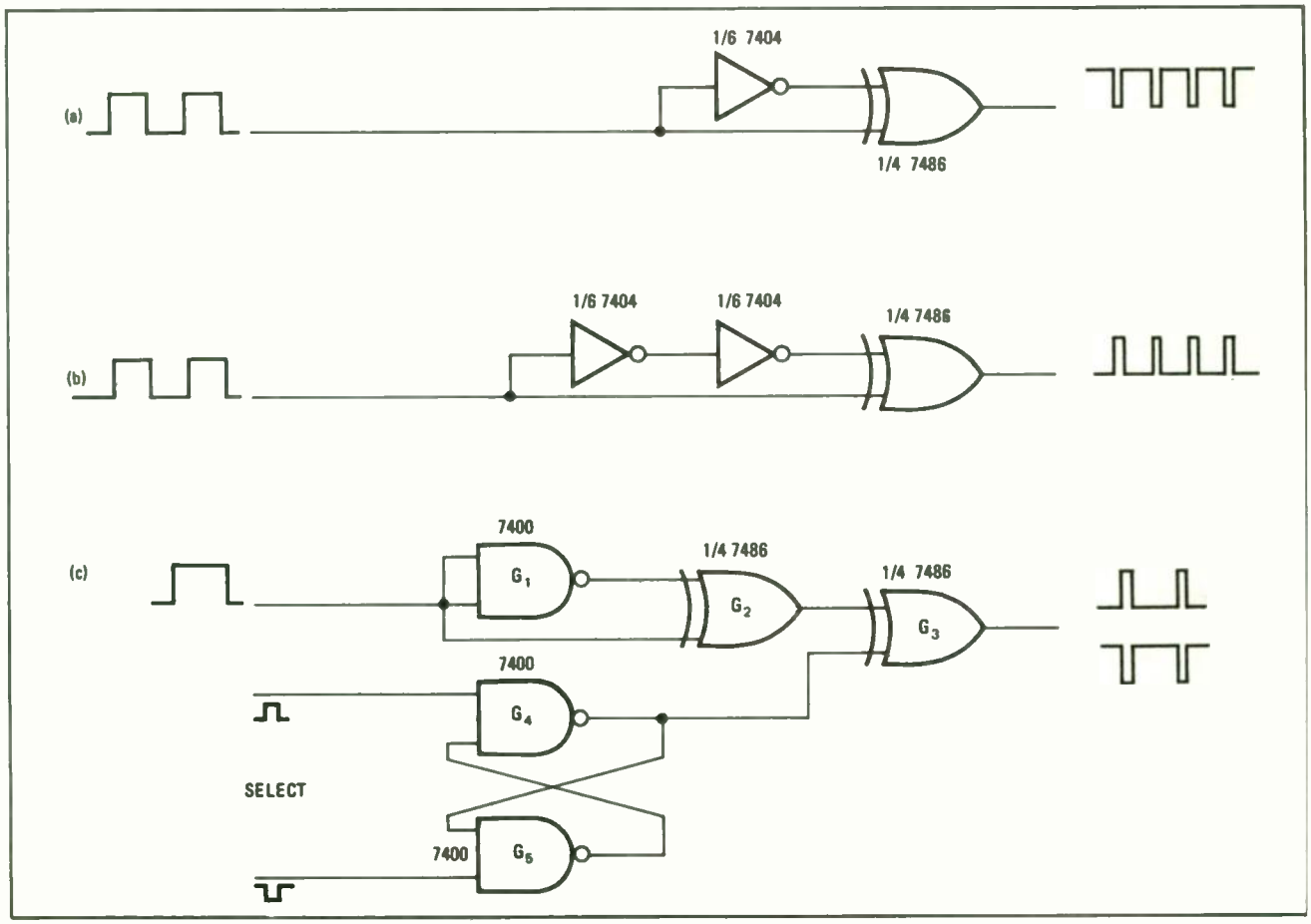
In (a), the gate inputs are inverted with respect to each other so that the gate output is in the high state for either a high or low input signal. When the input signal switches from high to low, both gate inputs are low until the inverter has a chance to change states. During this time, the gate output goes low until the inverter switches and causes the gate output to return to the high state. This process repeats when the input signal switches from low to high. Therefore, for every transition of the input signal, the gate puts out a negative-going pulse having a width equal to the delay time of the inverter.

Two inverters can also be used as the delay element, as shown in (b). Now the gate inputs have the same polarity, causing the gate output to be low for either a high or low input signal. The output will be a train of positive pulses with a width equal to a single inverter's delay time. These output pulses may be easily extended or stretched by inserting an RC timing network between the two inverters.

Applying the operating principles of circuits (a) and (b) permits the realization of a bidirectional one-shot (c) that has an addressable output pulse polarity. Gates G_1 and G_2 simply duplicate the one-shot of (a) and feed one of the inputs of the exclusive-OR output gate, G_3. A flip-flop, comprised of gates G_4 and G_5, drives G_3's other input. The polarity of the output pulses is now selectable, since the state of the flip-flop controls output pulse polarity.

If longer or more accurate output pulse widths are required, the delay element in any of the three one-shots can be changed to a delay line, such as the ones now available in 14- and 16-pin dual-in-line packages. The delay device could even be a standard off-the-shelf one-shot, for example, Texas Instruments' SN74121 or Fairchild's 9601. □

Selectable one-shot polarity. Either positive or negative output pulses can be generated by controlling high/low states of inputs to exclusive-OR gate. One-shot (a) uses time delay of single inverter to produce negative pulse train. One-shot (b) has additional inverter for positive output pulse train. Bidirectional one-shot (c) has addressable output polarity, which is determined by state of G_4-G_5 flip-flop.



Double-duty multivibrator gives complementary outputs

by Edward Beach
National Radio Institute, McGraw-Hill Inc., Washington, D.C.

Depending on its input signal period, a pulse generator operates as a one-shot or as a synchronous astable multivibrator. In either mode, the circuit provides complementary outputs. An ordinary grounding pushbutton switch can serve as the input device.

Gates G_1 and G_2 form a simple latch that prevents the circuit from operating in the absence of an input (high). When the input goes low, the latch changes state, allowing gate G_1 to act as an inverter. Gates G_1, G_3, and G_4 are the pulse-generating portion of the circuit.

If the input remains low for less than three generator time constants, single complementary pulses are produced by gates G_1 and G_4. The leading edge of each output pulse coincides (neglecting gate delays) with the leading edge of each input pulse. The trailing edge of the output pulse (again, neglecting gate delays) resets the latch and disables the generator.

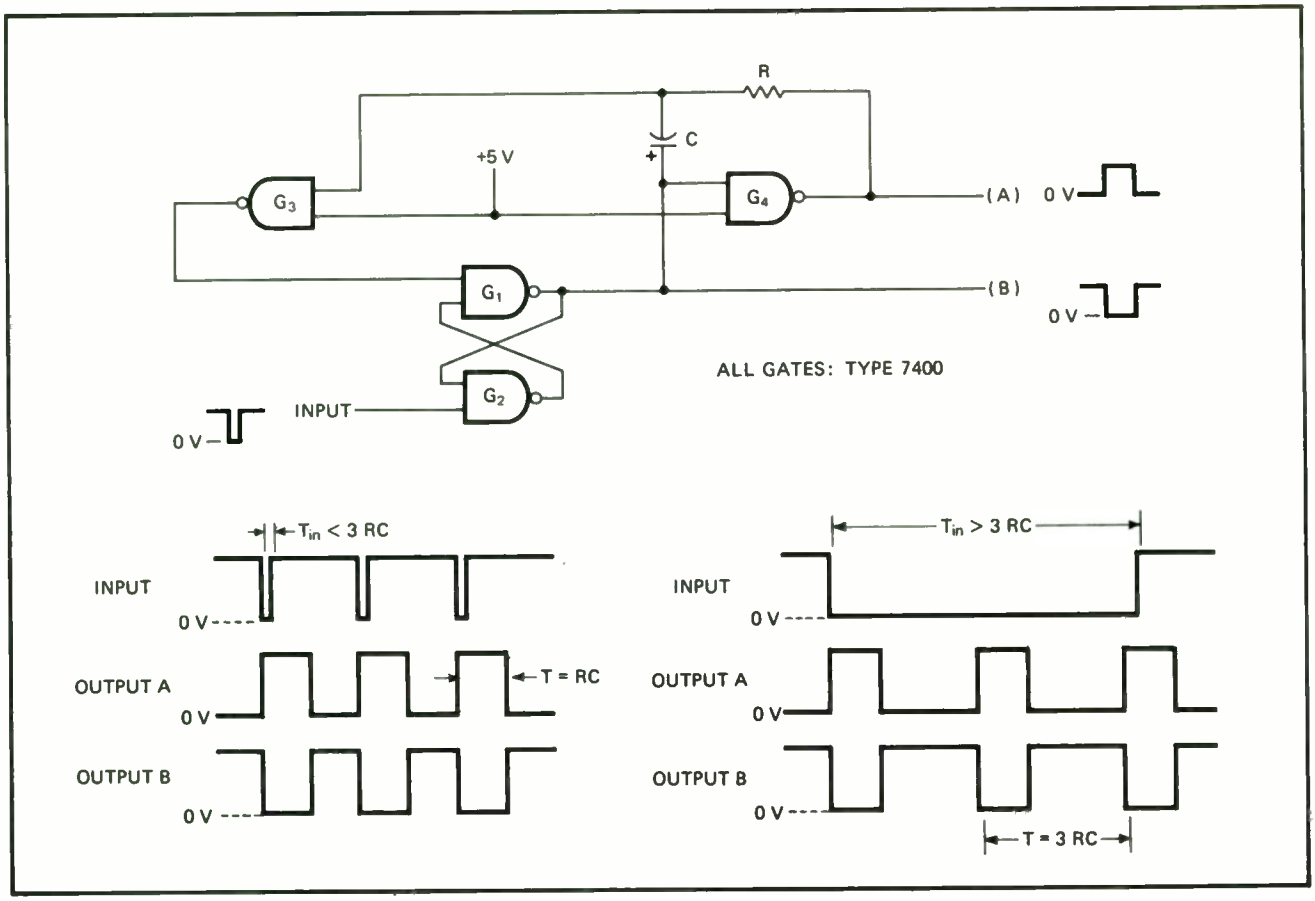
When the input signal remains low for longer than three time constants, at least two complete output pulses with a period equal to approximately three generator time constants are produced. In this case, the pulses begin and end synchronously. The first output pulse coincides with the leading edge of the input, and the last pulse is a full-width pulse, no matter when the input is removed.

Resistor R can range in value from 330 ohms to 1.5 kilohms, while capacitor C can be some value between 0.001 microfarad and 1,000 μF. For example, when R = 1,000 ohms and C = 100 μF, the circuit will produce either a 100-millisecond pulse or a 100-ms pulse train with a repetition rate of about 3 pulses per second.

For critical timing applications, a nonpolarized capacitor should be used when C is a high value; for less-critical applications, an ordinary electrolytic or tantalum capacitor will suffice. Since the reverse capacitor voltage is only about –0.7 volts, an inexpensive capacitor can be used.

The circuit can also function as an inexpensive transistor-transistor-logic clock simply by replacing gates G_1, G_3, and G_4 with half a type 7404 circuit. In addition, gate G_2 could be eliminated and an inverted version of the input signal applied directly to gate G_1, but this could shorten the last pulse in the pulse train. □

Manual pulser. Pushbutton-operated pulse generator functions either as a monostable or astable multivibrator. Low input signal enables G_1-G_2 latch so that G_1 becomes an inverter. Gates G_1, G_3, and G_4 then generate complementary output pulses. When input is low for less than three RC time constants, circuit is a one-shot; when input period exceeds 3RC, circuit is a synchronous astable multivibrator.



Programable monostable is immune to supply drift

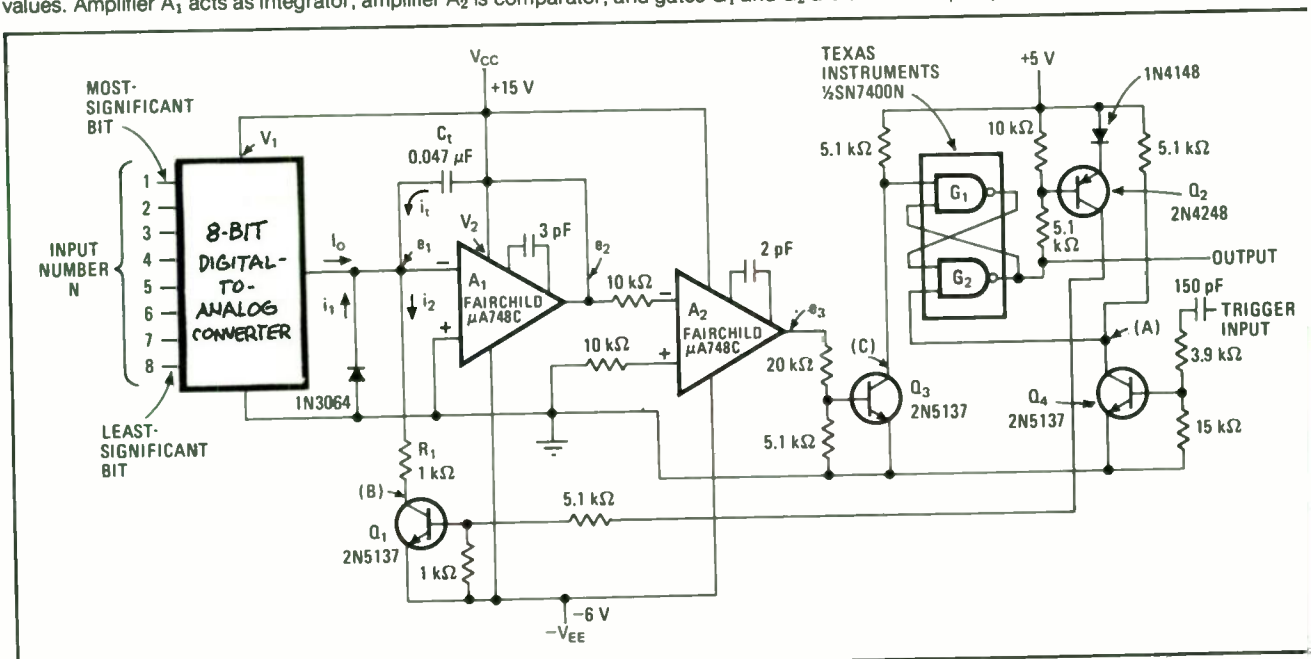
by Mahendra J. Shah
University of Wisconsin, Madison, Wis.

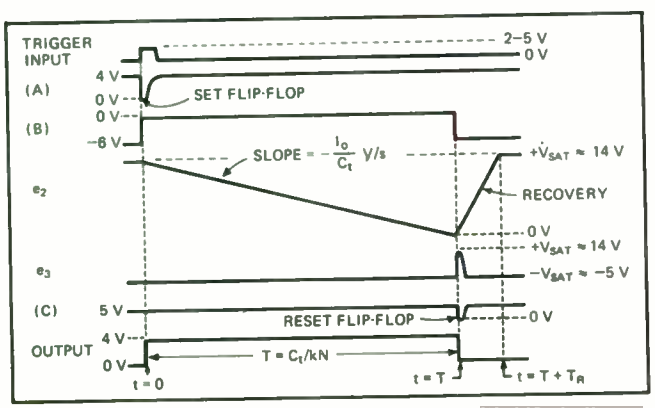
A monostable multivibrator with an output pulse width that is digitally programable is, for all practical purposes, independent of power supply variations. The circuit's output pulse period varies only -0.0055% for a 1% change in the positive supply voltage and only +0.0031% for a 1% change in the negative supply voltage. The monostable is useful in computer-controlled test systems and real-time control systems where digitally controlled pulse width or time delay is needed.

The circuit consists of a low-cost eight-bit digital-to-analog converter (one that does not have an internal reference), an integrator, a comparator, a flip-flop, and the necessary set-reset circuitry. Amplifier A_1 and capacitor C_t form the integrator, amplifier A_2 is the comparator, and NAND gates G_1 and G_2 make up the flip-flop. Transistors Q_1 and Q_2 allow the integrator's output voltage to be reset to the positive saturation voltage of amplifier A_1, while transistors Q_3 and Q_4 enable the flip-flop to be set and reset.

Initially, the monostable's output is low, transistors Q_1 and Q_2 are fully on, and transistors Q_3 and Q_4 are off. Voltage e_1 is at (minus) the forward voltage drop of the diode at the converter's output, voltage e_2 is at $+V_{SAT}$, and voltage e_3 is at $-V_{SAT}$. The current, i_t, flowing through timing capacitor C_t is zero and:

Voltage-stable one-shot. Digitally programable output pulse width of monostable multivibrator drifts less than 0.005% for 1% change in either positive or negative supply. The table shows that product of input number N and output period T is nearly constant over broad range of values. Amplifier A_1 acts as integrator, amplifier A_2 is comparator, and gates G_1 and G_2 are set-reset flip-flop.





INPUT NUMBER N	OUTPUT PERIOD T	PRODUCT N x T
1	70.5 ms	70.5
2	35.0 ms	70.0
4	17.2 ms	68.8
8	9.0 ms	72.0
16	4.45 ms	71.2
32	2.20 ms	70.4
64	1.10 ms	70.4
128	0.56 ms	71.7
255	0.28 ms	71.4
000	2.5 s	0.0

$i_2 = i_1 + I_o$

where I_o is the output current of the d-a converter.

When a trigger input is applied at t = 0, it is differentiated, and transistor Q_4 is momentarily turned on fully. This sets the flip-flop, the monostable output goes high, and transistors Q_1 and Q_2 turn off, making currents i_1 and i_2 zero. Now current i_t is equal to $-I_o$, causing voltage e_2 to become a linear ramp that descends from $+V_{SAT}$ towards $-V_{SAT}$ at a rate of $-I_o/C_t$ volts per second. Voltage e_1 is maintained at virtual ground.

Once voltage e_2 reaches zero at t = T (where T is the monostable pulse width), the comparator (A_2) output switches from $-V_{SAT}$ to $+V_{SAT}$. Transistor Q_2 now turns fully on, resetting the flip-flop and causing the monostable output to go low.

Transistors Q_1 and Q_2 then turn fully on, producing a reset current of:

$i_t = V_{EE}/R_1 - I_o$

This current causes voltage e_2 to rise linearly towards $+V_{SAT}$ at a rate of $(V_{EE}/R_1 - I_o)/C_t$ volts per second. Voltage e_2 reaches $+V_{SAT}$ at $t = T + T_R$, where T_R is the monostable recovery time:

$T_R = V_{SAT}C_t/(V_{EE}/R_1 - I_o)$

The monostable is now ready to accept the next trigger.

The output current for the d-a converter is given by:

$I_o = kV_1N$

where k is a constant that equals 0.68 micromho, V_1 is the converter's supply voltage, and N is the binary input number. The monostable pulse width can be written as:

$T = V_{SAT}/(I_o/C_t) = (V_2 - 0.5\ v)/(I_o/C_t)$

where V_2 is the integrator's positive supply voltage. Substituting for current I_o in this equation yields:

$T = (V_2 - 0.5\ v)C_t/kV_1N$

Since V_1 and V_2 are 15 v—a much higher voltage level than 0.5 v—this equation can be approximated by:

$T = C_t/kN$

which indicates that T should be very nearly independent of the power-supply voltage.

The table in the figure shows the product of N × T to be almost constant over a range of input numbers. □

Astable multivibrator needs only one capacitor

by Glen Coers
Texas Instruments, Dallas, Texas

Two large capacitors are required for most astable multivibrator designs. But, by using a programable unijunction transistor (PUT), one of these can be eliminated, and only one inexpensive Mylar capacitor is needed.

The multivibrator in the diagram, for example, is designed to operate at 1 hertz. Its output symmetry can be adjusted with timing resistors R_1 and R_2—resistor R_1 controls the negative output pulse width (t_1), while resistor R_2 controls the positive output pulse width (t_2). The values of R_1 and R_2, along with the value of capacitor C, determine the output pulse durations:

$R_1 = 1.4t_1/C$

$R_2 = 2.5t_2/C$

At the start of the circuit's cycle, the PUT is off, the bipolar transistor is on, and capacitor C charges through resistor R_1. When the PUT's peak-point emitter voltage (V_p) is reached, the PUT triggers and turns off the bipolar transistor, allowing this device's collector voltage to go toward the supply level.

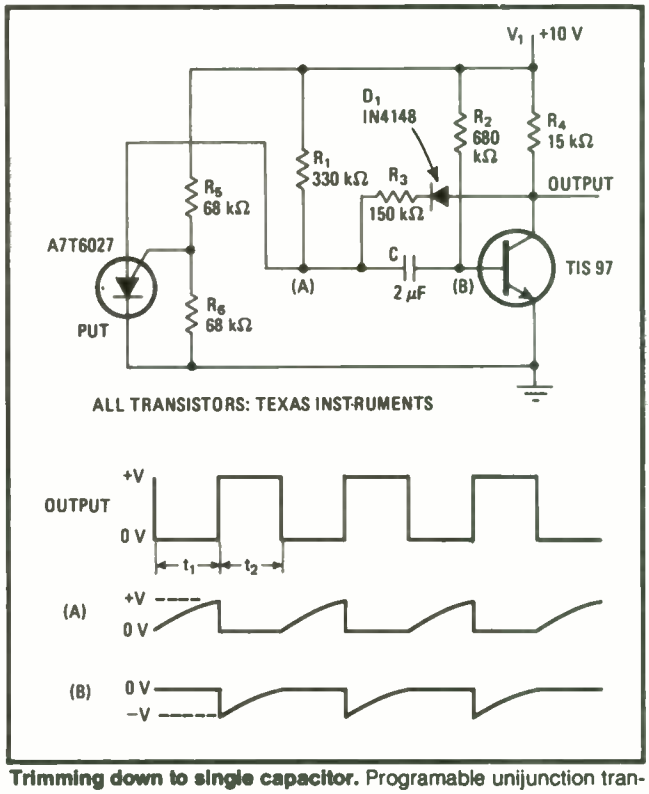
Diode D_1 and resistors R_3 and R_4 provide latching current for the PUT. The value of resistor R_3 can be determined by:

$R_3 = [V_1 - (V_V + V_D)]/I_V$

where V_1 is the supply voltage, V_D is the diode drop, V_V is the PUT's valley-point voltage, and I_V is its valley-point current.

When capacitor C discharges through resistor R_2, the bipolar transistor is turned on so that the latching current is removed from the PUT. This device's gate voltage (V_G) then rises to the level set by the voltage divider formed by resistors R_5 and R_6. The PUT then turns off, capacitor C again begins to charge through resistor R_1, and the cycle repeats.

The value of timing resistor R_1 must be small enough to meet the PUT's peak-point current (I_p) requirement. And the value of the other timing resistor, R_2, must be small enough to assure that the bipolar transistor will turn on. □



Trimming down to single capacitor. Programable unijunction transistor (PUT) eliminates the second capacitor in astable multivibrator circuit. When PUT is off, bipolar transistor is on and capacitor C charges through resistor R_1 until PUT triggers, turning off the bipolar. As capacitor C discharges through resistor R_2, the PUT remains on until the bipolar conducts. Capacitor C then charges again.

IC timer circuit yields 50% duty cycle

by Frank N. Cicchiello
Geometric Data Corp., Wayne, Pa.

When a 555 timer is operated as an astable multivibrator, it normally produces a pulse-type digital output waveform that has a limited duty cycle. Circuit arrangements that allow the 555 to operate with a 50% duty cycle square-wave output may be rather complex, and many are unstable. However, the simple circuit shown here produces a stable square wave with a duty cycle of 50% ±1%. This circuit has no tendency toward hesitant starting or latch-up.

As a start, assume capacitor C_1 to be uncharged. When this is so, a zero-volt signal level is applied to the IC's internal comparator (as seen at pin 6) when power is first turned on. This, in turn, means that the digital output (pin 3), to which resistor R_1 is returned, is at V_{CC}. Therefore, C_1 charges exponentially toward V_{CC} through resistor R_1. When the voltage across capacitor C_1 reaches a value of 2/3 V_{CC}, as seen at pin 6, the IC's internal comparator triggers its internal flip-flop, causing the output (pin 3) to switch to 0 V or ground level.

Now capacitor C_1 discharges toward 0 V through resistor R_1 until the voltage V_{C1} drops to a level of ⅓ V_{CC}, as seen at pin 2, the IC's internal trigger circuit. At this point, the IC's internal flip-flop causes the digital output to switch back to the V_{CC} level, reestablishing the circuit's original conditions for charging C_1.

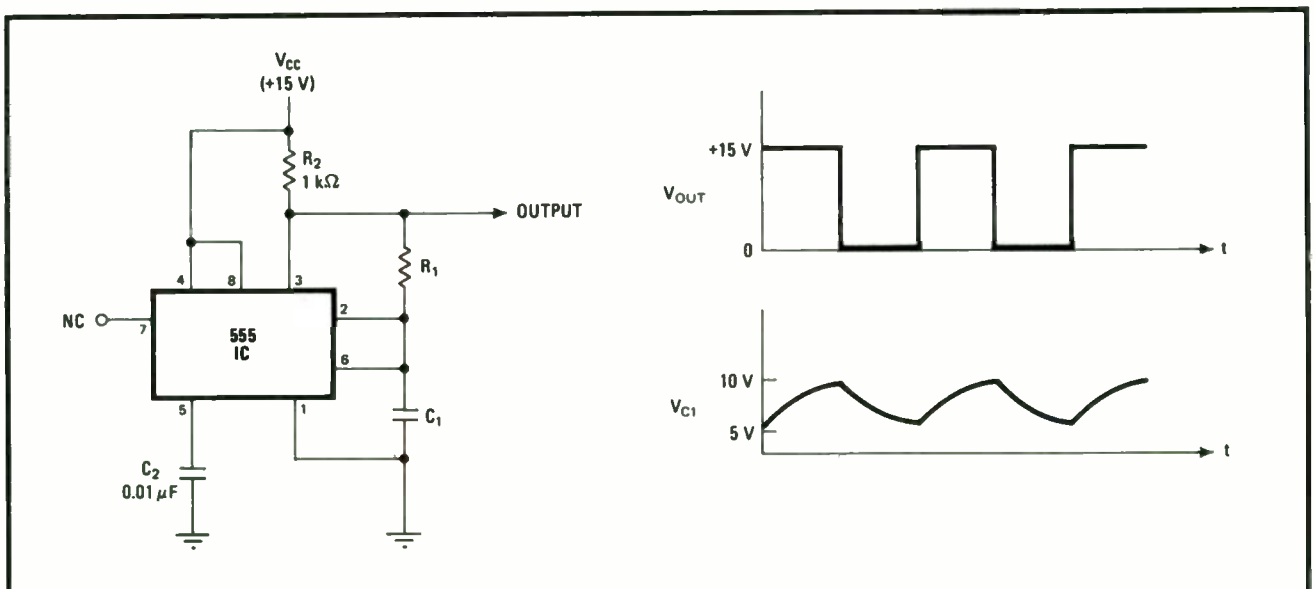
Connecting the trigger to the threshold inputs (pins 2 and 6) produces continued free-running or astable operation of the multivibrator, since these two circuits alternately control the IC's internal flip-flop/output circuit. It also means that the charging cycle need not start with 0 V across capacitor C_1 as previously explained, but may just as well begin its operation on the negative-going slope of C_1's waveform.

Resistor R_2 is a pull-up resistor, which ensures that the digital output voltage level at pin 3 closely approximates V_{CC}. Without it, the TTL-compatible output of the circuit may drop below this desired value. Capacitor C_2 is a bypass capacitor on the IC's unused voltage-control input. Circuit operation follows the formula:

$$t_1 = t_2 = 0.693\, R_1C_1$$
$$T = t_1 + t_2 = 1.386\, R_1C_1$$

so t_1 and t_2 are each equal to half of the period of the output, and T is the period.

The resistance of R_1 should be at least 10 times the value of R_2 but otherwise can be varied without upsetting the duty cycle. Transients occur in circuits that discharge C_1 rapidly, but they don't in this circuit. □



f (DESIGN) (kHz)	C_1 (μF)	R_1 (CALCULATED) (kΩ)	R_1 (ACTUAL) (kΩ)	f (ACTUAL) (kHz)
0.1	0.05	144.3	150	0.0962
1	0.01	72.2	75	0.962
5	0.01	14.4	15	4.81
50	0.001	14.4	15	45.3

All squared away. Free-running multivibrator built around 555 IC has 50% duty cycle because time constants for both charge and discharge are set by R_1C_1. Conventional discharge terminal (pin 7) is not connected in this arrangement. For values of supply voltage V_{CC} anywhere in the range from 5 to 15 volts, the actual output frequencies will not vary from those shown in table by more than 1%.

Programable multivibrator is four-in-one circuit

by Edward Beach
McGraw-Hill Continuing Education Co., Washington, D.C.

One inexpensive transistor-transistor-logic quad dual-input NAND gate and a few other components make up a multivibrator that can be programed for four functions—a simple latch, a monostable multivibrator, an astable multivibrator, or a retriggerable monostable multivibrator. The circuit employs a discrete timing circuit, rather than a conventional TTL timer, to allow a wide range of values to be used for timing components.

The table summarizes the operation of the circuit. With input A held low (to ground), gate G_1 shorts out timing capacitor C_t through diode D_1, and gates G_2 and G_3 operate as a simple reset-set latch. When input A is held high, the circuit becomes a monostable multivibrator. A negative-going trigger (B) sets the latch, removing the short from the capacitor. Now capacitor C_t charges toward the supply voltage (5 V) through resistor R_t until point 1 reaches approximately 3.2 V. The regenerative switch formed by transistors Q_1 and Q_2 then rapidly discharges capacitor C_t, resetting the latch.

The circuit's output pulse duration (T), which equals approximately $1.3R_tC_t$, can be adjusted from about 280 nanoseconds to well over several hours in length. For the longest period, requiring timing component values of 10 megohms and 1,000 microfarads, a very low-leakage capacitor must be used.

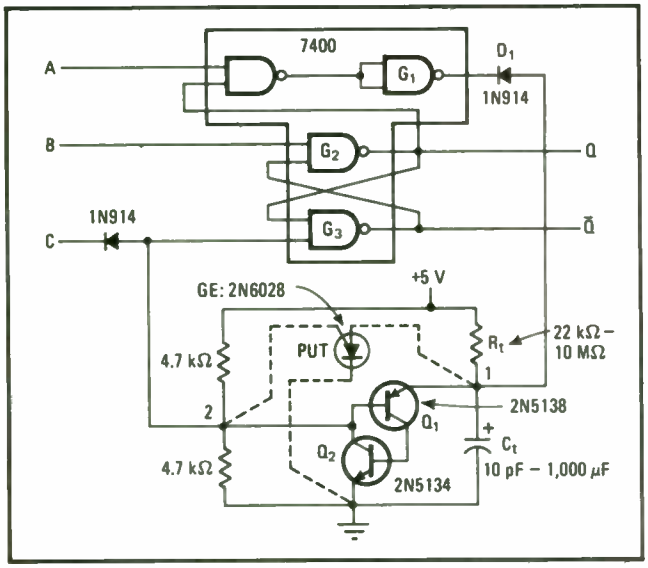
Input C acts as a direct clear for all circuit functions. Bringing C to ground potential clears the monostable by discharging capacitor C_t so that the circuit is ready for another input signal.

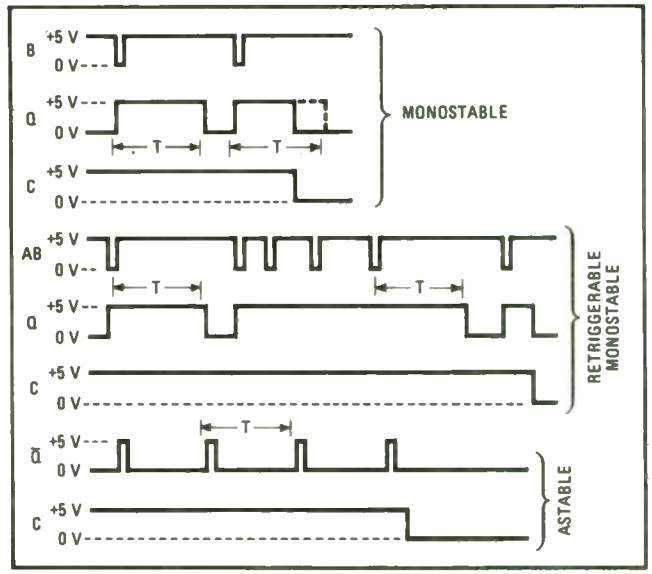
Tying inputs A and B together produces the retriggerable monostable multivibrator. Its timing period begins at the end of a negative-going trigger input. If the circuit has not timed out before the arrival of another trigger, capacitor C_t is discharged, and the timing cycle is started again.

Grounding input B while holding inputs A and C high allows the circuit to act as an astable multivibrator, producing positive pulses at its $\overline{Q}$ output. Negative-going pulses could be taken from point 2, if desired.

A programable unijunction transistor (PUT) can be used instead of transistors Q_1 and Q_2. It is connected as shown in the schematic. □

CIRCUIT FUNCTION			
A	B	C	OPERATING MODE
LOW	SET	RESET	R-S LATCH: B = SET, C = CLEAR
HIGH	⊓	HIGH	MONOSTABLE: $T = 1.3\ R_tC_t$, C = CLEAR
HIGH	LOW	HIGH	ASTABLE: $\overline{Q}$ = OUTPUT, C = CONTROL
A TIED TO B		HIGH	RETRIGGERABLE MONOSTABLE: C = CLEAR





Versatile multivibrator. Input signals determine operating mode of four-function multivibrator, which can be a reset-set latch, a monostable multi, an astable multi, or a retriggerable one-shot. Discrete devices in the timing network permit output pulse period to range from 280 nanoseconds to more than several hours. The programable unijunction transistor (PUT) can be used to replace transistors Q_1 and Q_2.

Monostable's pulse width is programable

by C.F. Reeves
Del Mar, Calif.

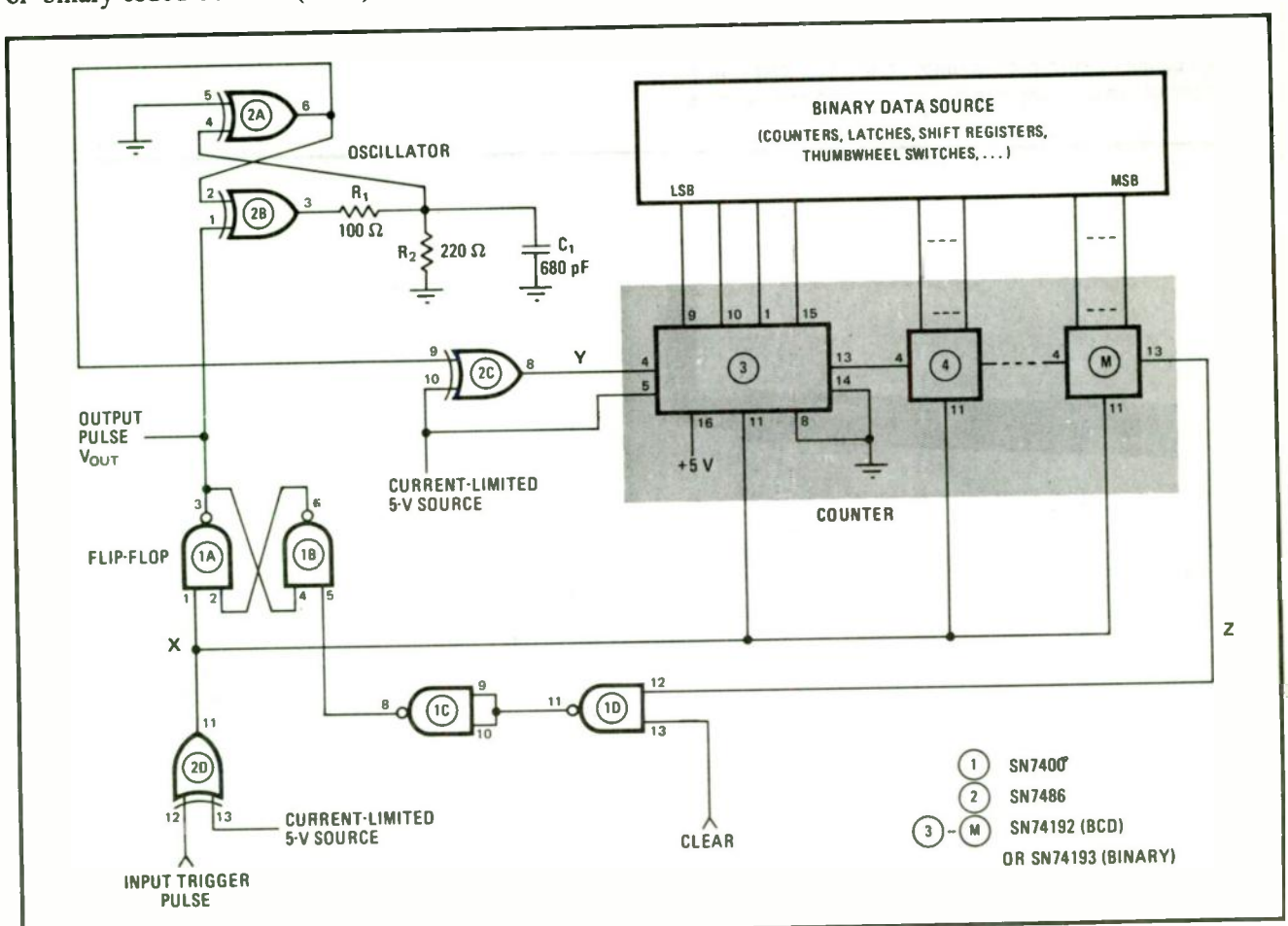
Variable-width pulses are required in many systems, and the widespread use of microprocessors as control elements makes numerical control of the pulse widths increasingly important. A numerically controlled one-shot multivibrator can be built that is particularly useful when the pulse-width range required is impractical or unattainable with conventional RC-time-constant one-shots.

For each input trigger pulse, the circuit produces an output pulse whose width is determined by an input binary number. The number may be taken from binary or binary-coded-decimal (BCD) sources such as shift registers, counters, bistable latches, thumbwheel switches, or the like.

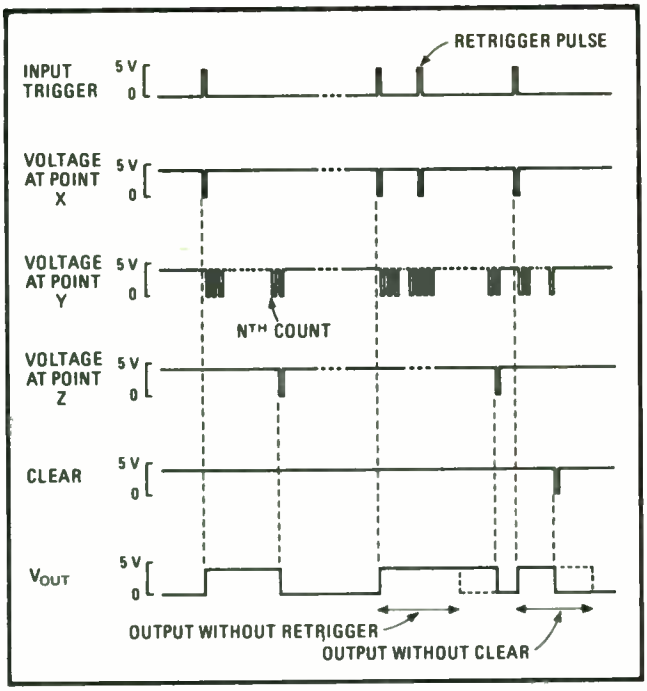
Functionally, the circuit is identical to the conventional one-shot in that it has one stable state and one temporary or quasistable state. The fundamental difference lies in the timing element that determines how long the circuit can remain in the quasistable state. In the conventional one-shot, this monostable period is set by the time constant of a resistor-capacitor network. The circuit shown here sets the monostable period by counting a preselected number of periods of a clock oscillator.

The range is thus limited only by the number of counter stages used. In Fig. 1 gates 2A and 2B form a clock oscillator that is gated on by a high logic level at pin 1. Resistors R_1 and R_2 and capacitor C_1 set the frequency at 10 megahertz. Gate 2C is an inverting buffer for the output pulses from the clock.

The input trigger pulse loads the counter chain (components 3 through M) with the number supplied by the binary data source. Simultaneously the trigger sets an



1. By the numbers. Binary number set into counter from data source determines duration of output pulse from this monostable circuit when input trigger pulse is applied. Output voltage V_{OUT} is high while counter counts the given number of cycles from the oscillator, as shown in Fig. 2. Typical applications for this circuit include variable-time-delay generation and pulse-code modulation.



2. Count. Waveforms for one-shot multivibrator in Fig. 1 illustrate operation. Input trigger makes V_{OUT} high and starts oscillator. Counter counts N cycles of oscillation (where N is decimal value of binary number set on counter by control source), then makes V_{OUT} low and stops oscillator. A trigger pulse applied during operation prolongs output pulse through countdown of newly loaded number. Output can be cut off at any time by grounding the clear terminal.

R/S flip-flop (1A and 1B), the output of which gates on the 10-MHz clock oscillator. The clock pulses cause the counter chain to count down to zero, whereupon the borrow pulse is generated at point Z. The borrow pulse resets the R/S flip-flop, disabling the clock oscillator and terminating the output pulse.

The width of the output pulse is determined by the binary input data and the clock frequency according to the following relationship:

$$PW = (N+1)/f_c$$

where N is the decimal value of the binary input number, and f_c is the clock frequency. The numerator is (N+1) instead of N because the counter generates the borrow pulse when leaving the zero state rather than when entering it. The output pulse-width range is determined by the number of 4-bit counter stages, K, and is expressed as $1{:}10^K$ for BCD input data and $1{:}16^K$ for binary input data. As the waveforms of Fig. 2 show, the one-shot is retriggerable. When an input trigger pulse occurs while the counter chain is counting down from a previous trigger, the chain simply reloads with the value of the binary data source and begins a new countdown. The result is a single elongated pulse. An additional circuit feature is that the output pulse may be terminated at any time by applying the logic zero to the "clear" input terminal. □

33. Operational amplifiers

Helping a 709-type op amp to outperform itself

by Jiří Dostál
Research Institute for Mathematical Machines, Prague, Czechoslovakia

A complementary-transistor output stage turns the 709-type operational amplifier into a far better performer than it is by itself. Such a stage can extend the device's unity-gain bandwidth to 15 megahertz, its slew rate to 300 volts/microsecond, its full-power frequency to 5 MHz, and its dc gain to 300,000. Moreover, the resulting over-all amplifier settles in only 3 μs to within 0.01% of the full-scale output voltage.

The circuit's high-frequency and pulse characteristics are derived from the output stage. Its input offset characteristics are principally those of the op amp.

At dc or low frequencies, the gain of the op amp is multiplied by the gain of the output stage. The equivalent differential resistance between the collectors of transistors Q_1 and Q_2 is designed to be about 100 kilohms, making the gain of the output stage approximately equal to 7. Resistor R_1 is included to keep the stage's gain at this value, in case the differential resistance changes. Resistor R_2, on the other hand, reduces output distortion by assuring that the op amp's output emitter-follower is effectively biased off.

At the circuit's upper frequency limit, the op amp rolls off rapidly and the gain of the parallel feed-forward path dominates. The transfer function of the op amp becomes that of an integrator, which is formed by series resistor R_3 and the feedback collector capacitances, C_{C1} and C_{C2}, of transistors Q_1 and Q_2. The circuit's small-signal bandwidth can be written as:

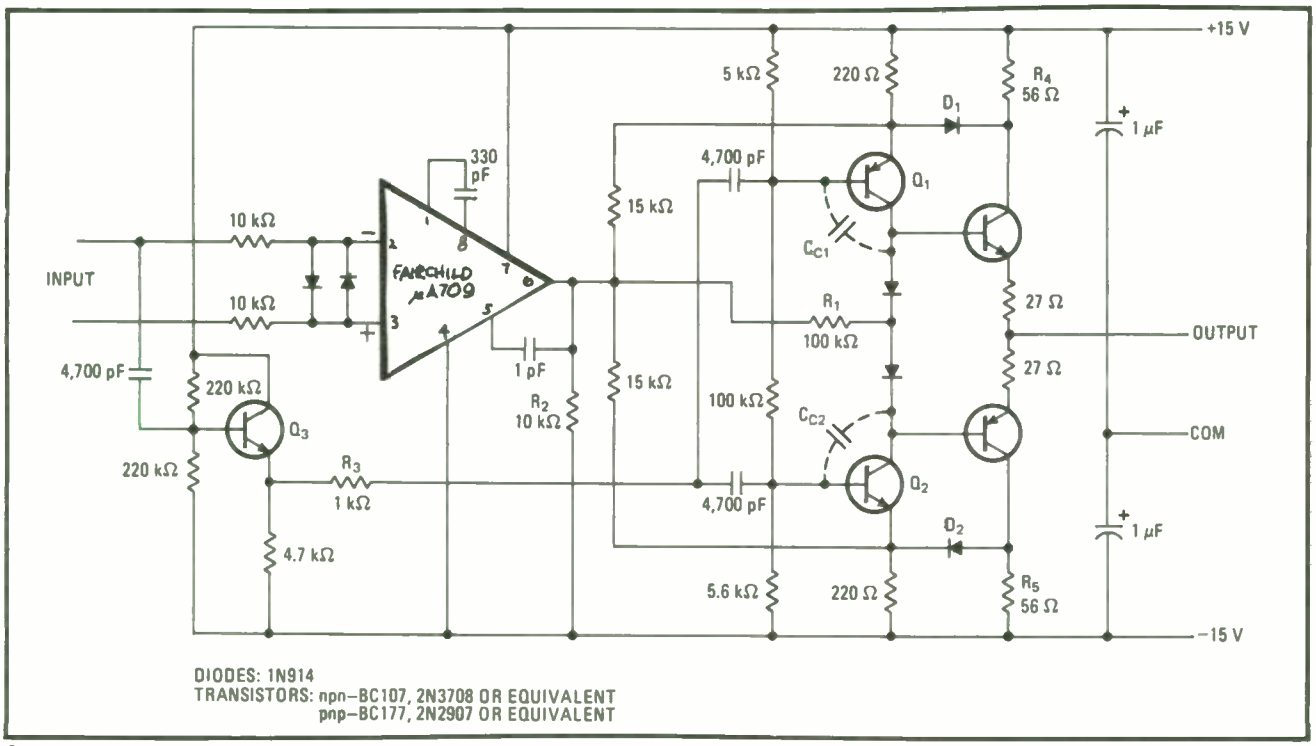
$$f_t = 1/[2\pi R_3(C_{C1}+C_{C2})$$

which is approximately 15 MHz when C_{C1} and C_{C2} are each 5 picofarads. The emitter current of transistor Q_3 sets the circuit's slew rate:

$$S.R. = I_{E3}/(C_{C1}+C_{C2})$$

which is around 300 V/μs for an emitter current of 3 milliamperes.

The constant base potentials of transistors Q_1 and Q_2 are used to limit any output short-circuit currents, which are sensed by resistors R_4 and R_5 and diodes D_1 and D_2. If desired, the signal line to the op-amp's noninverting input can be biased within the common-mode range of the 709-type op amp. □



Super amplifier. Output stage made up of complementary transistors increases the speed and extends the frequency response of the 709-type op amp. The over-all amplifier, which can be powered by one ±15-volt supply, has a unity-gain bandwidth of 15 megahertz and slews at the rate of 300 volts/microsecond. At high frequencies, the op amp is like an integrator, and capacitances C_{C1} and C_{C2} dominate.

Complementary output stage improves op-amp response

by Robert Gagnon and Richard Karwoski
Raytheon Co., Equipment division, Sudbury, Mass.

The performance of a conventional 741-type operational amplifier can be considerably enhanced if it's given a complementary-transistor output stage. The op amp's gain-bandwidth product is extended from its normal 1 megahertz to 7.5 MHz for a 250-ohm load resistor, while slew rate is increased from 0.5 to 5 volts/microsecond. Similarly, the full-power bandwidth reaches 50 kilohertz, as opposed to 15 kHz, and the bandwidth at a voltage gain of -2 becomes 2.5 MHz, rather than 330 kHz.

The output stage (a), which contains transistors Q_1 and Q_2, acts as a current buffer, providing extra load drive capability. It is basically a bootstrap configuration using degenerative feedback. Transistor Q_2 is the principal source of load current, and the stage's dynamic input impedance is the product of the load resistance and the current amplification factors of both Q_1 and Q_2.

The two outboarded transistors form two complementary pairs with the output transistors inside the op amp—outboarded transistor Q_1 complements internal transistor Q_3, while Q_2 complements Q_4. This configuration (b) makes it possible to keep voltage gain independent of output load conditions and to be determined by a resistance ratio:

$$e_o/e_i = R_2/R_1$$

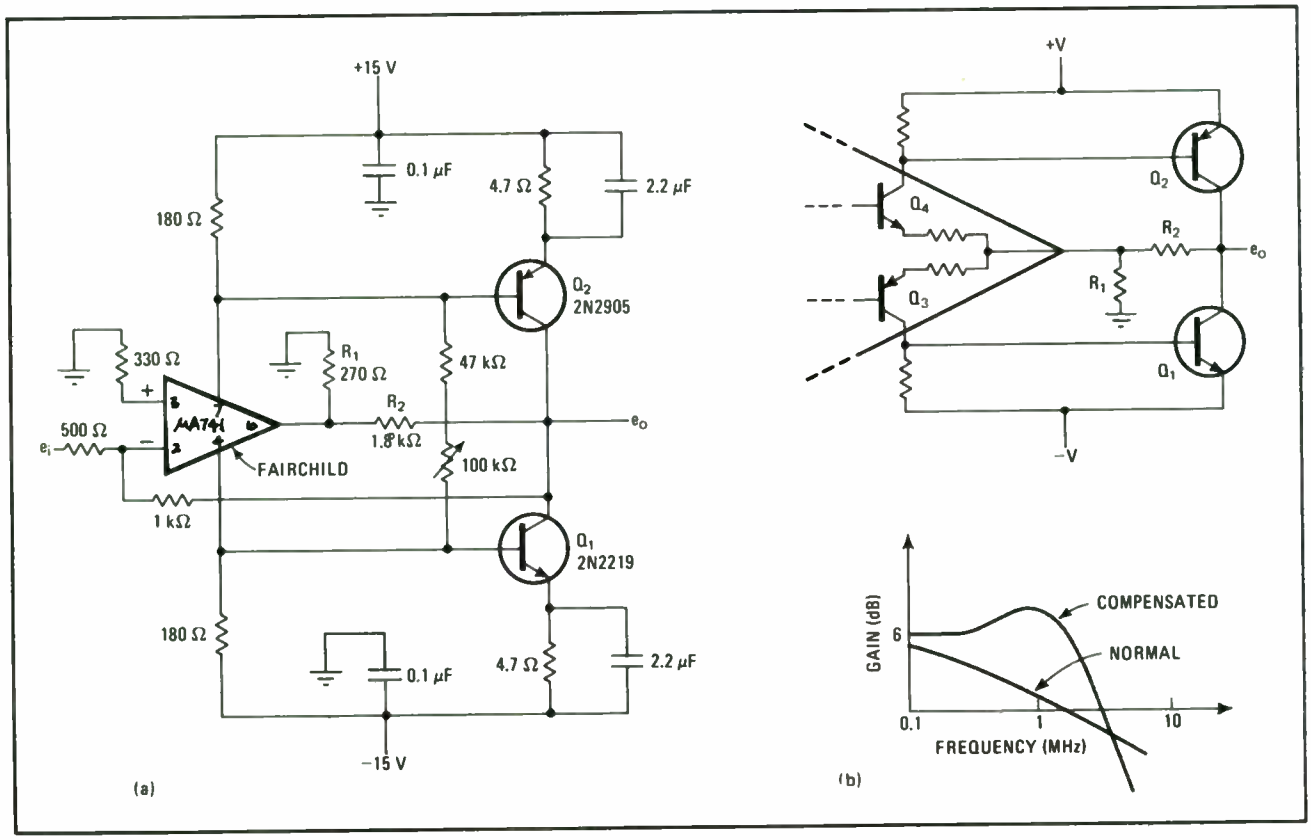
where R_1 is the load resistance for the op amp, and R_2 is the input resistor to the output stage.

If $R_2/R_1 = 10$, the op amp output voltage swing need only be ±1 V to realize a circuit output voltage swing of ±10 V. In practice, a resistance ratio of 6.7, with $R_1 = 270$ ohms, yields the best over-all results because of how the op amp responds to this load resistance value.

For a load resistance of around 300 ohms, the op amp's maximum output voltage swing is reduced by about 30%, but its slew rate remains approximately 0.5 V/μs for small voltage excursions. By fixing the gain of the output stage at about 10, the slew rate of the overall circuit is increased by a factor of 10, and the op amp's frequency response is extended.

Undesirable high-order effects of the 741-type op amp are far enough beyond its nominal 1-MHz crossover frequency that instability due to the gain added by the output stage is not a problem. A 100-kilohm cermet potentiometer is included in the circuit to permit cancellation of crossover effects. It should be adjusted at the full-power bandwidth limit—50 kHz and a maximum output voltage of 20 V peak-to-peak. □

Boosting op amp performance. Output stage (a) multiplies op amp slew rate by 10 and extends crossover frequency to 7.5 megahertz. As shown in (b), external transistors Q_1 and Q_2 complement internal transistors Q_3 and Q_4, respectively. Resistor R_1 acts as op amp load resistance so that resistance ratio R_2/R_1 fixes overall circuit gain. Additional gain lets op amp operate at low output voltage.



Controlling op amp gain with one potentiometer

by T. Frank Ritter
San Antonio, Texas

A single potentiometer and a few resistors can control the gain of an operational amplifier from a selected negative value, through a null, to its positive open-loop gain. The variable-gain circuit, which is shown in (a), maintains a high input impedance, even at high amplification. It makes a convenient wide-range voltage reference for a voltage regulator because it eliminates the need to switch the op amp's circuit for above- or below-reference operation.

A graph of voltage gain versus potentiometer rotation is also shown in (a). The equation for output voltage can be written as:

$$E_o = [E_i R_F/(R_I + R_1)][(R_1/R_2) - (R_{I+}/R_{I-}) + (R_1/R_F)]$$

where R_I is the resistor at the op amp's noninverting input, and R_{I-} the resistor at the inverting input. Varying feedback resistor R_F changes the magnitudes of both the positive and negative gains without changing the appearance of the graph; varying resistance ratio R_{I+}/R_{I-} shifts the null point.

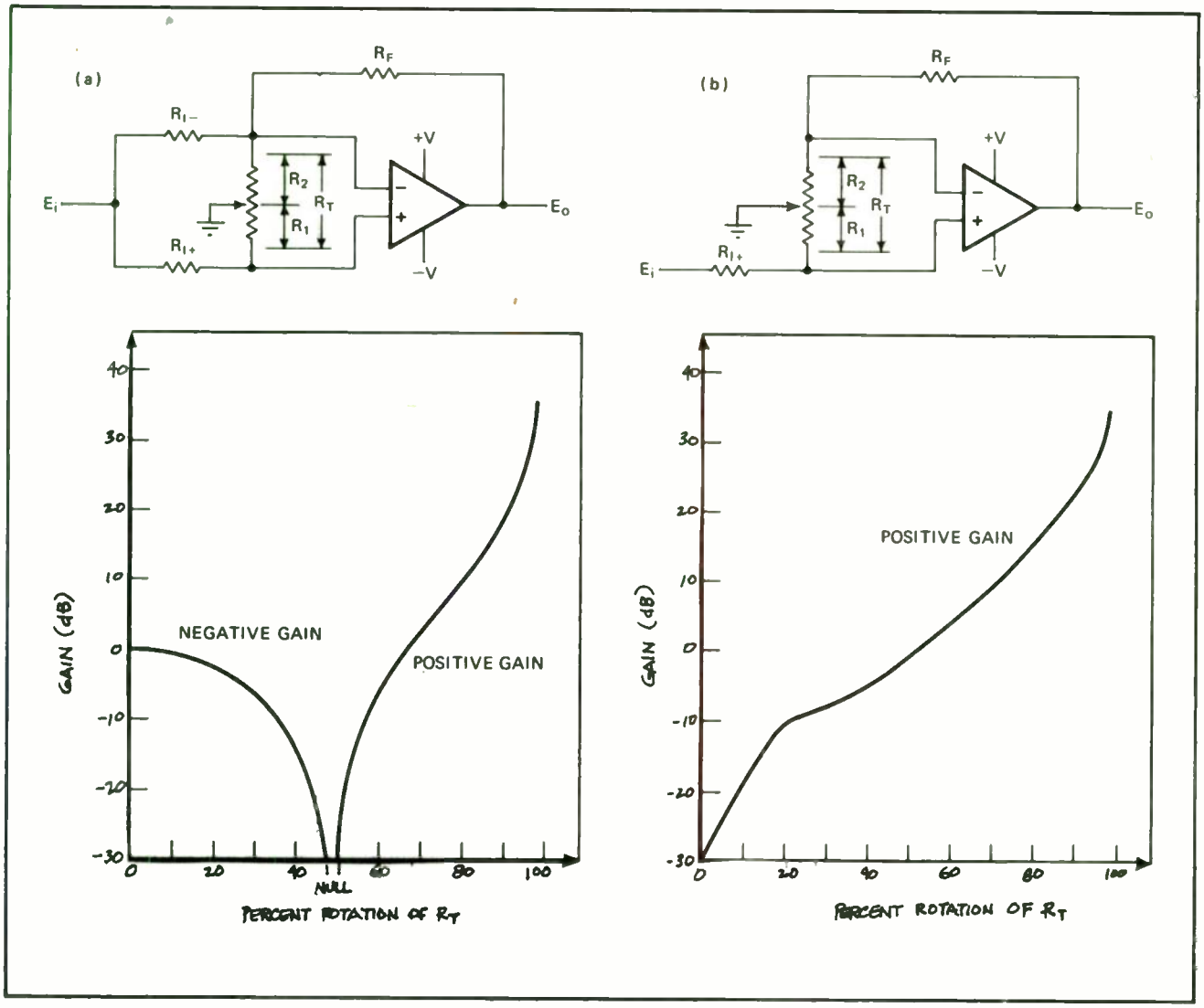
As resistor R_{I-} approaches infinity, op amp gain varies from null to positive infinity only, as illustrated in (b). The equation for output voltage becomes:

$$E_o = [E_i R_F/(R_{I+} + R_1)][(R_1/R_2) + (R_1/R_F)]$$

As can be seen from the figure, the gain curve for this circuit is nearly logarithmic.

For a potentiometer rotation of 10% to 90%, amplifier gain can be varied over four decades. The gain at 50% rotation is the ratio $(R_f + R_2)/(R_{I+} + R_1)$. Any general-purpose differential op amp can be used in the circuit. □

Wide-range gain adjustment. Potentiometer varies gain of operational amplifier (a) from chosen negative value to positive open-loop value. Null point can be shifted by changing resistance ratio of noninverting input resistor R_{I+} to inverting input resistor R_{I+}. Removing R_{I+} permits positive gains to be controlled over wide range, as shown in (b). Circuit's input impedance remains high over full gain range.



FET-controlled op amp permits wide dynamic range

by Henry E. Santana
Hewlett-Packard, Loveland Instrument Division, Loveland, Colo.

When a field-effect transistor is operated as a voltage-controlled resistor, it is usually limited to a relatively small dynamic signal-voltage range. This is due to the nonlinearity of its drain-source resistance over a wide range of drain-source voltage.

But a wide-range voltage-controlled amplifier can be realized if a pair of FETs is connected in the bridge configuration shown in the diagram. The inverting terminal of the operational amplifier is kept at virtual ground, permitting the range of each FET's drain-source voltage to remain small, regardless of how broad the actual signal-voltage range is. This also assures that the excursions of V_{DS} will remain well within the FET's pinch-off region.

The circuit's voltage-transfer function can be written as:

$$A_V = -(R_2/R_1) + N(R_1+R_2)/R_1 + NR_2r_{on}[1 - (V_{GS}/V_P)]$$

where r_{on} is the on-resistance of the right-hand FET, V_{GS} is the gate-source voltage, and V_P is the pinch-off voltage. Variable N represents a resistance ratio:

$$N = r_{on}/(r_{on}+R_1)$$

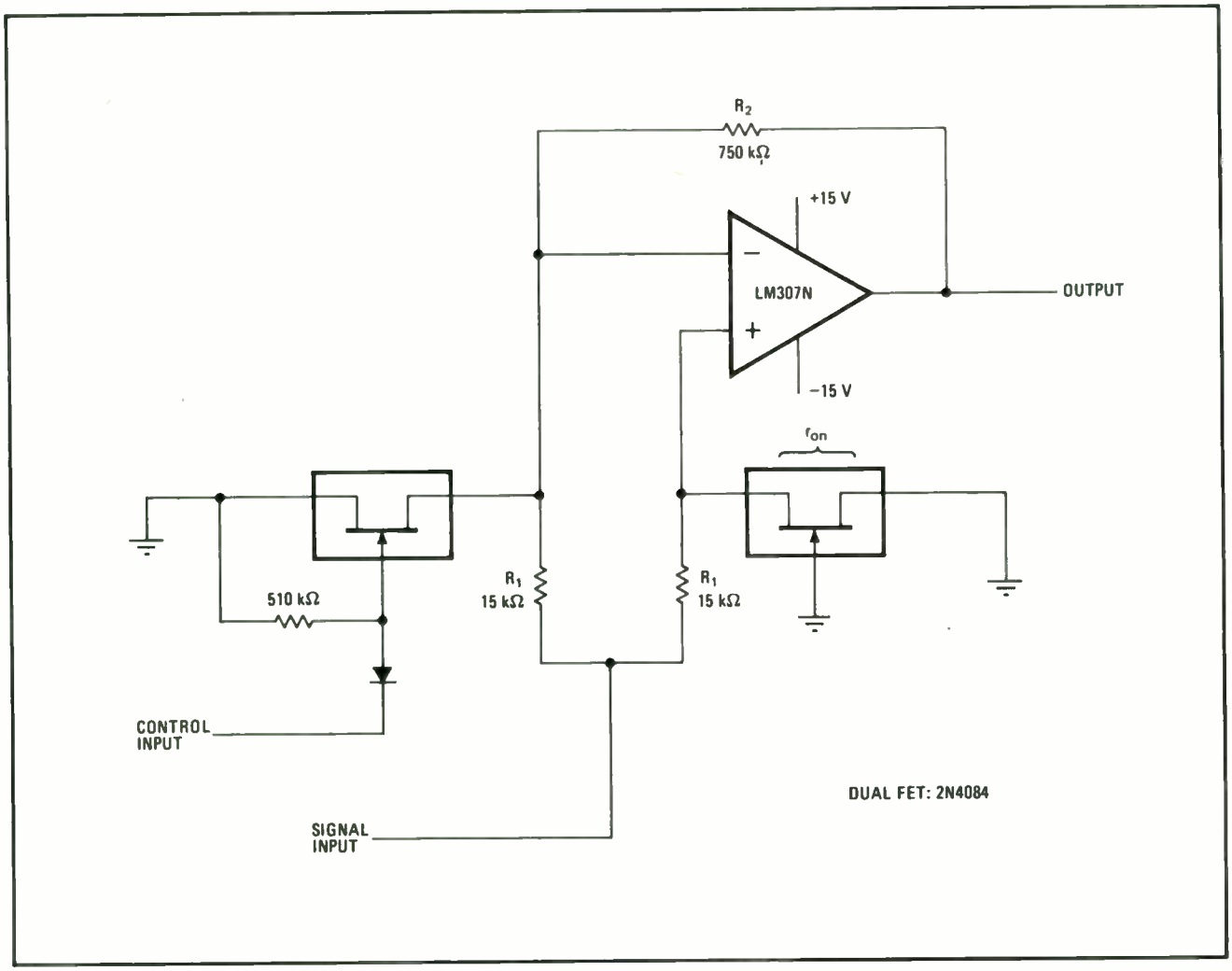
If N is very small, and r_{on} is much less than R_1, then:

$$AV = -(R_2/R_1)(V_{GS}/V_P)$$

Although N must be small, it must, nevertheless, be greater than zero for the circuit to work. The control voltage for the circuit can range from 0 to V_P, and the peak ac input-signal voltage is determined by $I_{DS}R_1$.

Applications for this voltage-controlled amplifier include automatic gain control, true rms conversion, amplitude compression, and signal modulation. □

Wide-ranging. Voltage-variable amplifier can operate over a broad range of input-signal voltages. The FETs, which function as voltage-controlled resistors, are wired in a bridge configuration. Their inherent resistance nonlinearity is avoided by limiting each FET's drain-source voltage range, no matter how large the signal voltage becomes. The op amp's inverting input is held at virtual ground.



Series-connected op amps null offset voltage

by Lawrence Choice
Burr-Brown Research Corp., Tucson, Ariz.

The input offset voltage and offset voltage drift of a differential operational amplifier can be held essentially to zero by connecting a second amplifier at the inverting input of the first. This auxiliary op amp must have an offset voltage and drift that are matched to the primary op amp. The additional amplifier will then act as a floating voltage source, canceling any offset voltage.

As shown in (a), unity-feedback amplifier A_1 is connected to the inverting input of amplifier A_2, providing a floating offset voltage source between A_2's non-inverting input and its output. (If A_1's offset characteristics were matched with opposite polarity to those of A_2 then A_1 could be placed at A_2's non-inverting input.) Letting V_{OS} represent the input offset voltage of A_2, V_{A1} the voltage across A_1, A_o the open-loop gain of A_2, and E_1 and E_2 the two input signals, then output voltage E_o can be written as:

$$E_o = -A_o(E_1-E_2) - A_o(V_{A1}-V_{OS})$$

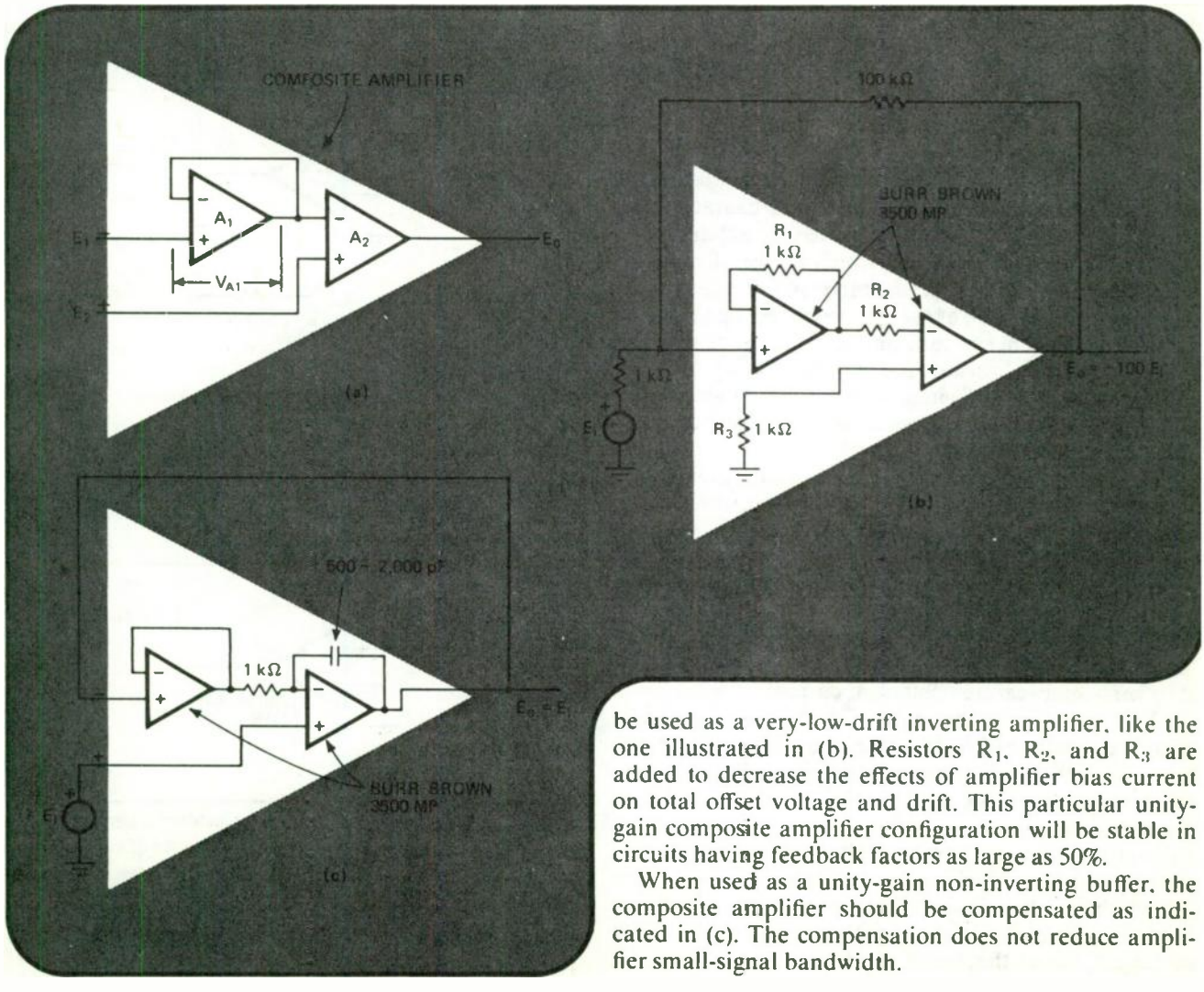
If $V_{A1} = V_{OS}$, then:

$$E_o = -A_o(E_1-E_2)$$

The composite amplifier consisting of A_1 and A_2 can be used as a very-low-drift inverting amplifier, like the one illustrated in (b). Resistors R_1, R_2, and R_3 are added to decrease the effects of amplifier bias current on total offset voltage and drift. This particular unity-gain composite amplifier configuration will be stable in circuits having feedback factors as large as 50%.

When used as a unity-gain non-inverting buffer, the composite amplifier should be compensated as indicated in (c). The compensation does not reduce amplifier small-signal bandwidth.

Getting rid of offset voltage. Letting amplifier A_1 act as floating voltage source (a) effectively eliminates offset voltage and offset voltage drift of amplifier A_2. As long as A_1 and A_2 are matched, their offset voltages cancel, keeping offset of composite amplifier at zero. Composite amplifier of (a) can be used as conventional single operational amplifier for either inverting (b) or non-inverting (c) applications.



Continuing biasing improves clamping amplifier

by Jerry Graeme
Burr-Brown Research Corp., Tucson, Ariz.

A clamping amplifier can be made faster and more accurate by biasing its zener clamping element so that it is always on. This biasing technique also results in reduced clamp capacitance, sharper turn-on, broader bandwidth, and lower thermal drift.

Clamping amplifiers or feedback limiters are frequently used to provide amplitude limiting for signal clipping, signal squaring, or overload protection. One of the simplest clamping elements for these applications is a zener diode.

A zener diode connected across the feedback resistor of an operational amplifier will conduct when the op-amp output level reaches the zener voltage. The zener overrides the feedback resistor and limits the op-amp output swing at the zener voltage. To obtain bipolar amplitude limiting, two zener diodes are generally connected, in series-opposing fashion, across the feedback resistor, as shown in (a).

Zener diodes used in this way, however, impose serious limitations on the clamp because of their large capacitance, insufficiently sharp turn-on characteristic, high leakage current, and undesirable thermal drift.

Zener parasitic capacitance, which is typically a comparatively high 700 picofarads, can result in a long turn-on time for the clamp, as well as restricted signal bandwidth. For the zener to turn on, its capacitance must be charged through resistor R_1, which is often a large value, to preserve the circuit's input resistance. Signal bandwidth is limited because resistor R_2 is capacitively shunted by the zener.

When the zener conducts, it goes from a high-resistance state to a low one. But since this transition is not abrupt, sharp limiting cannot be achieved, and the clamping is rounded. Even in its high-resistance state, the zener, through its leakage current, introduces error into the amplifier's summing junction. Furthermore, when the zener is on, the clamp level it sets is subject to thermal drift since the zener will probably not be held at its zero-temperature-coefficient current.

All of these limitations can be overcome to a significant extent with the biased zener clamp of (b). Here, the zener is continuously biased on so that it does not limit the op-amp output swing until the diode bridge places the zener in the feedback path.

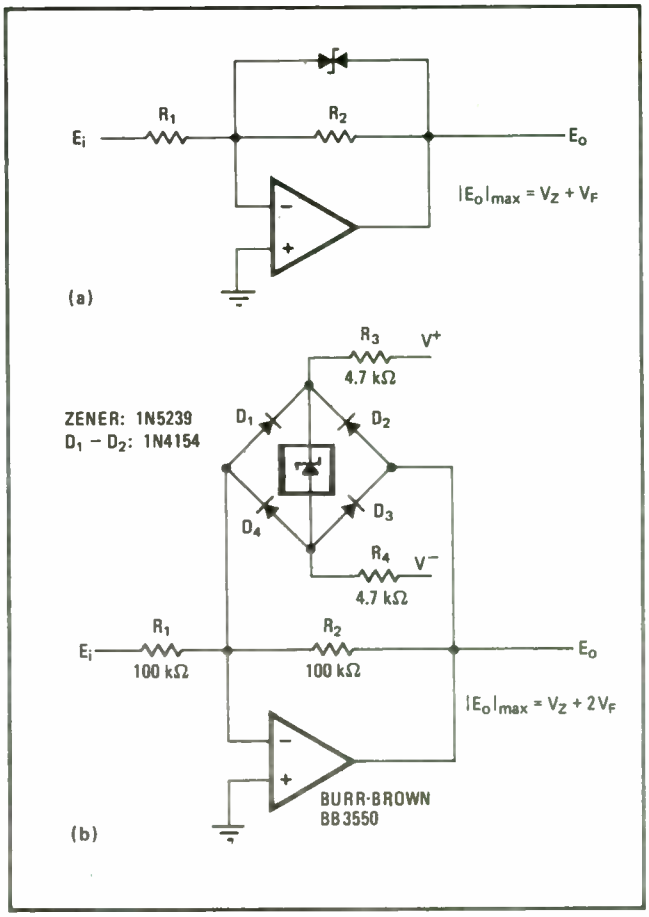
Clamping occurs when the voltage across resistor R_2 can support the zener voltage as well as forward-bias two of the bridge diodes. Positive-polarity signals are clamped when diodes D_1 and D_3 conduct, connecting the zener across the feedback path. When diodes D_2 and D_4 conduct, the zener limits signals of the opposite polarity. Since the same zener is used for both signal polarities, the output clamping will be symmetrical.

The continuous zener bias dramatically reduces the clamp's shunt capacitance, sharpens the clamping response, and often means lower thermal drift. To reduce thermal drift, resistor R_3 is chosen to produce a zener thermal variation that is canceled by that of two bridge diodes. When the clamp is on, the zener current is approximately:

$$I_Z = (V^+ + V_F)/R_3 \text{ or } (-V^- + V_F)/R_3$$

where V_F is the forward voltage of a junction diode, and V^+ and V^- are the supply voltages. (This equation neglects the signal current from resistor R_1, which is generally small compared to the zener current.)

Sharper clamping is achieved by avoiding the zener turn-on characteristic and leakage current. The clamping circuit is now turned on by the bridge diodes, and the sharper turn-on of these junction diodes improves



Whetting sharpness of zener clamp. Standard zener-type clamping amplifier (a) can be slow and sloppy because of large zener capacitance and zener leakage. But a dramatically faster and crisper response can be obtained by adding a bridge of junction diodes to keep the zener always biased on, no matter the input signal polarity. The improved clamp (b) also provides more bandwidth and less drift.

clamping sharpness by around 8:1. Zener leakage current no longer reduces signal current as the clamping level is approached. Leakage to the amplifier summing junction is now the much smaller leakage of junction diodes D_1 and D_4.

Additionally, the capacitance of the clamping circuit is reduced by avoiding the charging and discharging of the zener capacitance. Only small voltage changes, the ones produced by signal current flow in the continuously biased zener, occur across the zener capacitance. Large voltage changes are restricted to the junction diodes, which have a far lower capacitance than the zener. The equivalent clamp capacitance that must now be charged through resistor R_1 is merely the combined capacitances of diodes D_1 and D_4. Typically, this represents a 100:1 reduction from the basic zener clamp capacitance so that turn-on time is faster.

And lastly, the bandwidth-limiting capacitive shunt on resistor R_2 is reduced by more than 100:1. Amplifier signals that do not turn the clamp on are not even affected by the small bridge-diode capacitance. When the bridge diodes are off, fixed voltages are established at one end of diodes D_1 and D_4 by the zener and its bias resistors. The only signal swing on these two input shunting diodes, then, is the very small summing junction signal. The equivalent capacitive shunt of resistor R_2 is reduced to $2C_F/A$, where C_F is the forward capacitance of a junction diode, and A is the open-loop gain of the op amp. (This capacitance is negligible compared to other parasitic capacitances.)

For the components shown in the figure, large- and small-signal bandwidths are boosted from 3 kilohertz to 400 kHz; clamping sharpness error is reduced from 0.8 volt to 0.1 V; clamp leakage current is decreased from 400 nanoamperes to 7 nA; and clamp-level thermal drift is brought down from 7 mV/°C to 0.6 mV/°C. □

BIBLIOGRAPHY:

J. Graeme, "Applications of Operational Amplifiers—Third-Generation Techniques," McGraw-Hill, 1973.

G. Tobey, J. Graeme, and L. Huelsman, "Operational Amplifiers—Design and Applications," McGraw-Hill, 1971.

More applications for the 741-type op amp

by Edward Beach

McGraw-Hill Continuing Education Center, Washington, D.C.

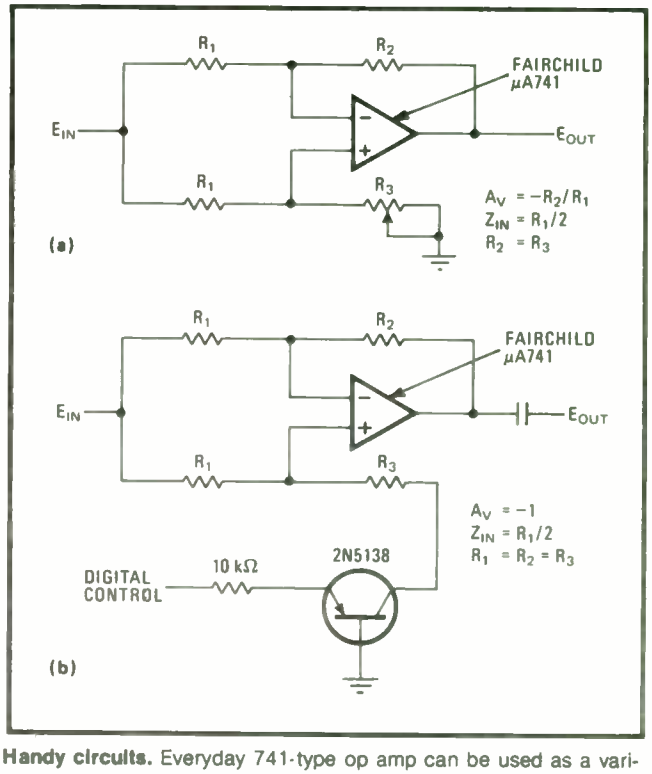
The large common-mode rejection ratio of the popular 741-type op amp makes it possible to realize a variable-gain amplifier and even an analog switch quite inexpensively. The gain of an op amp can easily be changed by varying the proportion of the signal applied to both its inputs. If equal signals exist at each input, there is no output because of the op amp's common-mode rejection, but applying more signal to one input than the other will result in useful gain.

For the variable-gain amplifier of (a), resistors R_1 and R_2 are selected in the usual manner—with regard to the required input impedance ($R_1/2$ in this case) and overall gain ($-R_2/R_1$). Feedback resistor R_2 may have to be trimmed to provide maximum attenuation when the gain-control resistor, R_3, is set to its maximum value ($R_3 = R_2$). In practice, the voltage gain can be varied from zero to $-R_2/R_1$ as the gain control goes from maximum to zero, and there will be no shift in the dc output.

The circuit can also be used as an analog switch, as shown in (b). For this application, however, there are a few restrictions. The output must be capacitively coupled, the input signal must be less than 1.2 volts peak to peak, and the amplifier must be set up for unity gain ($R_1 = R_2 = R_3$). But within these limitations, the circuit makes an excellent analog switch.

When a logic 1 (2.4 to 4 V) is applied to the digital control input, the transistor saturates, effectively grounding resistor R_3 to give an attenuation of 70 to 90 dB. As the transistor turns on, the op amp's noninverting input goes to approximately 0.6 V dc, causing the dc output voltage to also be 0.6 V and making an output coupling capacitor necessary.

A logic 0 (ground) input turns the transistor off, allowing the op amp's noninverting input to float so that the signal passes through the amplifier. If the signal becomes positive enough to forward-bias the transistor's base-collector junction, the output signal will be distorted on positive peaks. □



Handy circuits. Everyday 741-type op amp can be used as a variable-gain amplifier (a) or an analog switch (b). Only four external resistors are needed for the amplifier circuit, which maintains the same dc output as the gain is varied. For the analog switch, the op amp passes the input signal when the digital control line is grounded. The 741's large common-mode rejection permits it to perform well.

Combined op amps improve over-all amplifier response

by William Ott
Burr-Brown Research Corp., Tucson, Ariz.

By interconnecting a low-drift op amp with a wideband op amp, the best characteristics of both amplifiers can be preserved in a composite amplifier that offers the added benefit of increased open-loop gain. Typically, wideband op amps tend to produce significant errors because they exhibit a large offset voltage drift with time and temperature. But in the composite amplifier, the low-drift op amp can continuously compensate for the input offset voltage of the wideband op amp.

The composite amplifier of (a) is an inverting-only configuration. Low-drift amplifier A_1 senses the offset voltage between ground and the summing junction of wideband amplifier A_2. Any offset that is present will be integrated by A_1 to develop an offset-compensating voltage at the noninverting input of A_2.

This integration continues until the summing junction voltage is offset from ground by only the input offset voltage of low-drift A_1 (including the effects of A_1's input bias currents on resistors R_1 and R_2). The offset voltage of the composite amplifier, therefore, is essentially that of the low-drift op amp.

For the differential-input composite amplifier of (b), A_1 amplifies the offset voltage at the inputs of A_2. Low-drift amplifier A_1, then, supplies an offset-compensating voltage for the offset-nulling input of A_2.

In this way, the output of amplifier A_1 reduces A_2's offset voltage to that of the low-drift op amp, plus the offset from the bias current in resistors R_1 and R_2. As with circuit (a), the offset voltage and the offset voltage drift of the wideband op amp are essentially replaced by those of the low-drift op amp.

The open-loop gain of both composite amplifiers is $A_{O2}(1+\alpha A_{O1})$, where α is defined as $E_x/A_{O1}E_i$, and A_{O1} and A_{O2} are the dc open-loop gains of amplifiers A_1 and A_2, respectively. For the inverting-only configuration of (a), the quantity, αA_{O1}, is the response of the integrator formed by amplifier A_1, resistor R_1, and capacitor C_1. For the differential-input configuration of (b), α is essentially a constant and is independent of frequency; it is the change in the offset voltage of amplifier A_2 due to a change in A_1's output voltage, E_x.

If the inverting-only composite amplifier is to have a single pole in its open-loop gain response to insure gain stability, then:

$$R_1C_1 = A_{O2}/2\pi f_{c2}$$

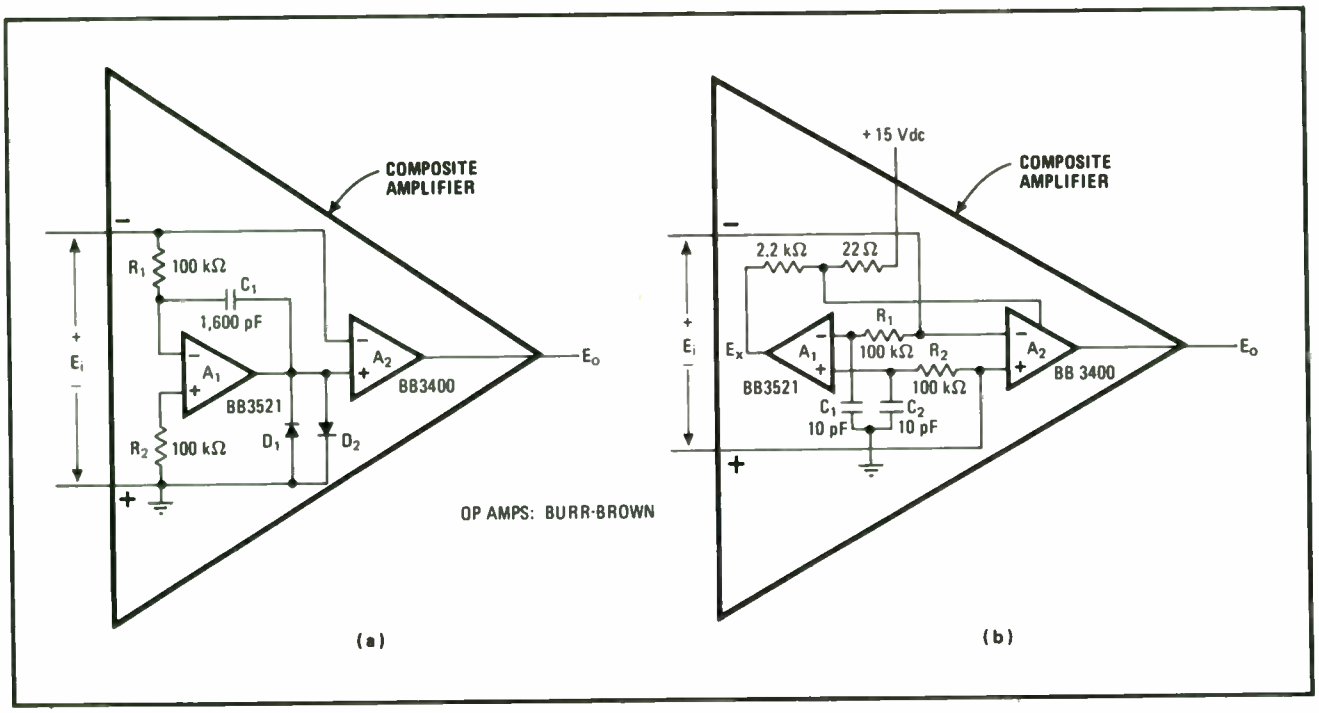
where f_{c2} is the unity-gain bandwidth of amplifier A_2. The bandwidth of the composite amplifier is essentially equal to f_{c2}, about 100 megahertz. The over-all offset voltage is about 200 microvolts, with a drift of 1 μV/°C. The over-all open-loop gain is around 200 decibels.

For the differential-input composite amplifier to have a single pole in its open-loop gain response:

$$\alpha = -f_{c2}/A_{O2}f_{c1}$$

where f_{c1} is the unity-gain bandwidth of amplifier A_1. Like the inverting-only amplifier, the differential-input amplifier has an over-all bandwidth of 100 MHz, an offset voltage of 200 μV, and an offset voltage drift of

A good combination. Two op amps—a low-drift one (A_1) and a wideband one (A_2)—can be wired to produce a composite amplifier that is both fast and stable. Circuit (a) is an inverting amplifier, while circuit (b) is a differential amplifier. Both amplifiers provide an over-all bandwidth of 100 megahertz, an over-all offset voltage of 200 microvolts, and a total offset voltage drift of 1 μV/°C.



1 μV/°C. The circuit's over-all open-loop gain, however, is somewhat smaller—140 dB.

Besides less offset voltage drift and more open-loop gain, the differential-input amplifier offers the additional advantage of improved common-mode rejection at low frequencies. For low-frequency operation, the common-mode rejection of the wideband op amp is essentially replaced by that of the low-drift op amp, which typically provides much better common-mode rejection.

In circuit (a), diodes D_1 and D_2 at the output of the low-drift op amp prevent a latch-up condition from occurring. Latch-up is possible in the composite amplifier when the low-drift op amp's output saturation voltage exceeds the wideband op amp's common-mode range.

And in circuit (b), there are two low-pass filters (formed by resistors R_1 and R_2 and capacitors C_1 and C_2) at the inputs of the low-drift op amp. They prevent high-frequency common-mode voltage swings from unbalancing the input stage of the low-drift op amp and changing its input offset voltage. □

Op amps multiply RC time constants

by Quentin Bristow
Geological Survey of Canada, Ottawa, Ont., Canada

Unusually long time constants can be generated with considerable accuracy by combining readily available low-value resistors and capacitors with a couple of general-purpose operational amplifiers. Besides being physically smaller than their higher-value counterparts, low-value components offer tighter value tolerances and do not have leakage or polarity problems. Furthermore, when high-value resistors are used, field-effect-transis-

tor-input op amps must be employed. They are more expensive than general-purpose op amps and do not provide as good input offset and temperature drift specifications.

A number of instrumentation applications require time constants in the order of seconds or minutes. Circuit (a), for instance, can be used to stretch one-shot output pulses, or as a low-pass insertion filter for monitoring slowly changing meteorological, oceanographic, or other geoscientific phenomena where low-frequency noise is undesirable. This network can multiply a basic RC time constant by a factor as large as 10,000. (For example, a 100-second time constant can be realized with R = 100 kilohms and C = 0.1 microfarad.)

When V_i is a step input, output voltages E_1 and E_2 rise exponentially to final values $-V_i$ and $+V_i$, respectively, with a time constant (taken at 63% of the final level) of $(N+2)RC$.

$$E_2 = -E_1 = V_i[1 - \exp(-t/(N+2)RC)]$$

The actual values of resistors R_1 and R_2 are not critical because the time constant is determined by ratio N and the values chosen for R and C. The components indicated provide a time constant of 50 seconds.

The drift and noise of either output referred to the original input V_i will be the same as that obtained when amplifier A_1 is operated at a closed-loop gain of $N+1$, modified of course, by the filtering effect of the time constant generated. After capacitor C is removed, the circuit can be seen to be an op amp (A_1) connected for a closed-loop gain of $N+1$, since amplifier A_2 is simply a unity-gain inverter.

The offset null trimmer permits the E_1 output to be set initially to zero for a zero input. Generally, the trimmer can be omitted for values of N less than 50. To avoid a tedious time lag in circuit output response when making this adjustment, one end of the capacitor should be disconnected temporarily.

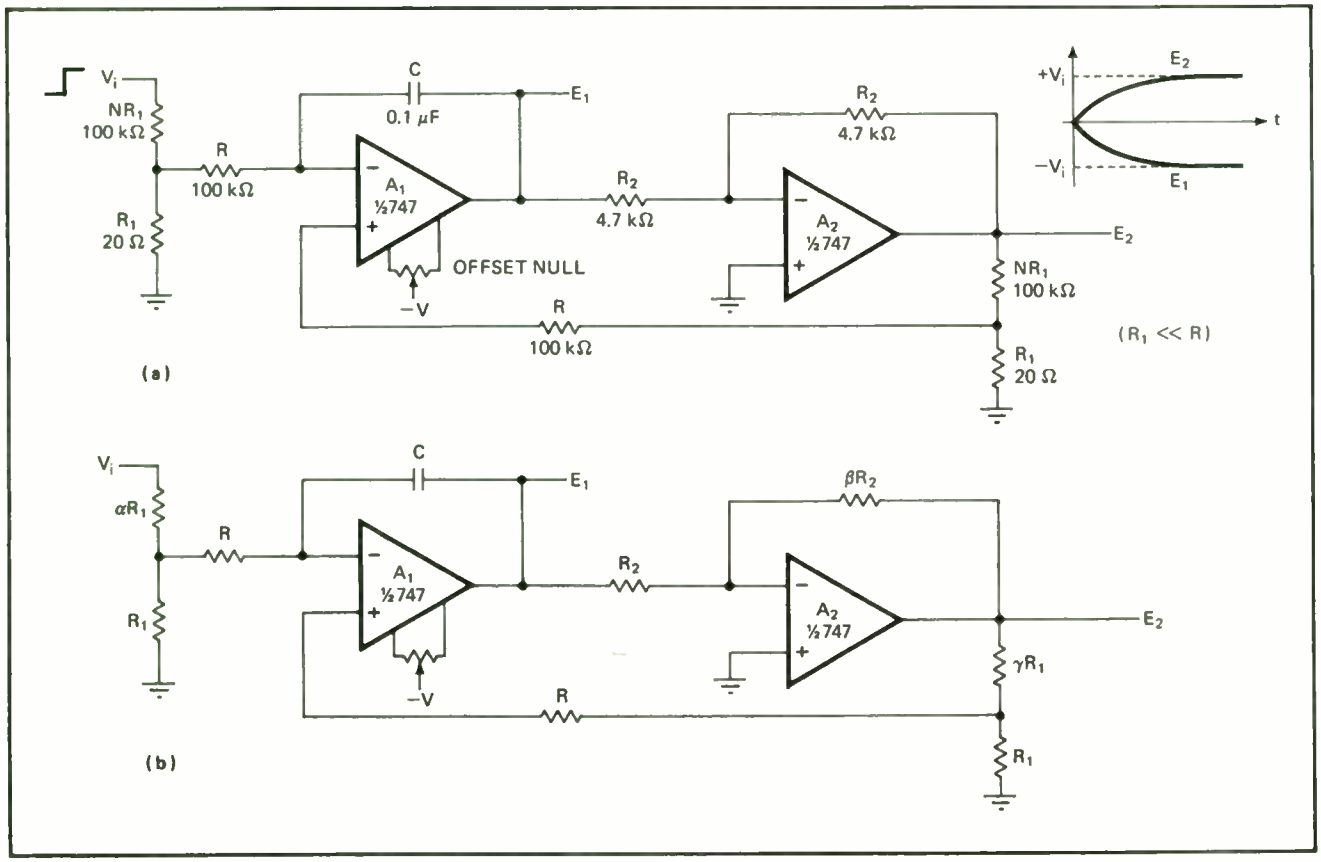
Gains other than plus or minus unity can be obtained at outputs E_1 and E_2 by making the input attenuation and feedback ratios unequal; they are both $1/(N+1)$ for circuit (a). Also, the inverting gain of amplifier A_2 can be other than unity. As shown in circuit (b), input attenuation can be controlled by ratio α, feedback by ratio γ, and inverting gain by ratio β. The two outputs become:

$$E_1 = -V_i(\gamma+1)[1 - \exp(-t\beta/(\beta+\gamma+1)RC)]/(\alpha+1)\beta$$

$$E_2 = V_i(\gamma+1)[1 - \exp(-t\beta/(\beta+\gamma+1)RC)]/(\alpha+1)$$

In applications where desired drift and noise specifications cannot be met by a 747-type op amp, amplifier A_1 can be stabilized with a temperature-controlled differential preamplifier, such as Fairchild's μA727B. This integrated circuit has an on-chip proportional temperature regulator, affording tight control of chip temperature at about 100°C. The 727-plus-747 combination provides excellent dc stability at high closed-loop gains and can be treated circuitwise as a single op amp. If a preamplifier is added, the null offset trimmer is no longer effective. □

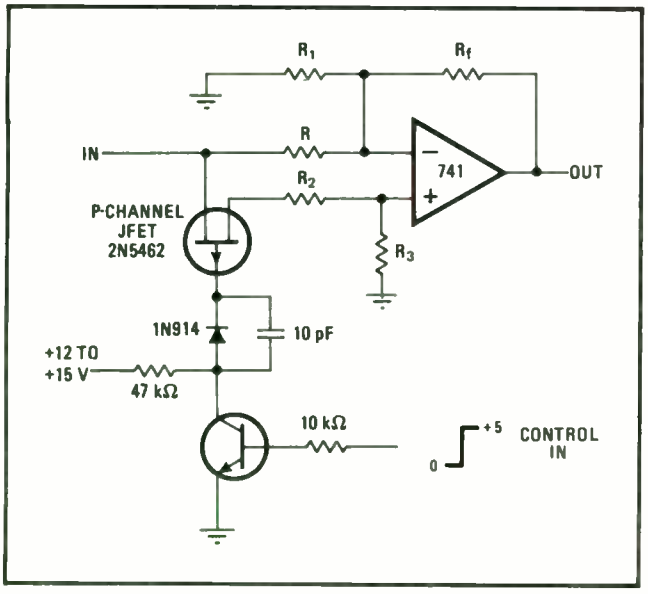
Extending RC time constants. Low-value resistors and capacitors and two op amps can generate time constants that are several minutes long. Output voltages E_1 and E_2 exponentially approach level of step input V_i. Time constant, which is 50 seconds for circuit (a), primarily depends on R, C, and ratio N. For circuit (b), there are three controlling ratios: α for input attenuation, γ for feedback, and β for gain.



FET programs op amp for invertible gain

by Ken A. Dill and Mark Troll
Revelle College, University of California, La Jolla, Calif.

With only a few inexpensive components, an amplifier can be built with a gain of either +N or –N, depending on whether a field-effect transistor is turned off or on. Such a circuit is useful for programable inversion of analog signals or for programable phase-shifting of 180°



FET inverts op amp. Amplifier gain can be programmed either positive or negative, depending on whether the field-effect transistor is conducting or not conducting. Gain is the ratio of R_f to R; for gains of ±1, R_f, R_2, and R_3 are all equal value, and R_1 is half the value.

for signals that are symmetrical with respect to ground. When a comparator is added to program the inverter, the circuit becomes a precision rectifier, the output of which is:

$$V_{out} = |V_{in} - V_{ref}|$$

When the FET is off, the input signal goes only to the inverting input terminal of the operational amplifier; the gain is:

$$V_{out}/V_{in} = -R_f/R$$

But when the FET is on, the gain is:

$$V_{out}/V_{in} = \eta A/[1+(ARR_1)/(R_1R_f+RR_f+RR_1)]\theta \times [f-)R_1R_f)/(R_1R_f+RR_f+RR_1)]$$

where A is the open-loop gain of the op amp, and

$$f = R_3/(R_2+R_3)$$

Since A is large, this reduces to:

$$V_{out}/V_{in} = (f-1)(R_f/R) + f[(R_f/R_1)+1]$$

To make +N and –N numerically equal, choose the resistance values so that $R_f/R = N$. From that, it follows algebraically that:

$$N = (f-1)(N) + f[(NR/R_1)+1]$$
$$2N = fN + (fNR/R_1) + f$$
$$2NR_1 = fNR_1 + fNR + fR_1$$
$$2NR_1 - fNR_1 - fR_1 = fNR$$
$$R_1 = NRf/[2N-(N+1)f]$$

For the simplest case—a gain of ±1—all amplifier input and feedback resistors have the same value, except R_1, which is half that value.

The gate of the FET is controlled by a standard analog switch configuration, which allows the inputs to be 0 or +5 volts, compatible with TTL. □

34. Optoelectronic circuits

Negative feedback keeps LED intensity constant

by Ken Erickson
Interstate Electronics Corp., Anaheim, Calif.

In applications where a passing object is detected as it partly obscures a light beam, a light source with a constant intensity may be desirable. A light-emitting diode, which has a longer life and switches faster than an incandescent lamp, would also be desirable, if it weren't for the fact that its light intensity may vary with temperature, especially as the device ages. But a LED's light intensity can be kept constant by the circuit shown here.

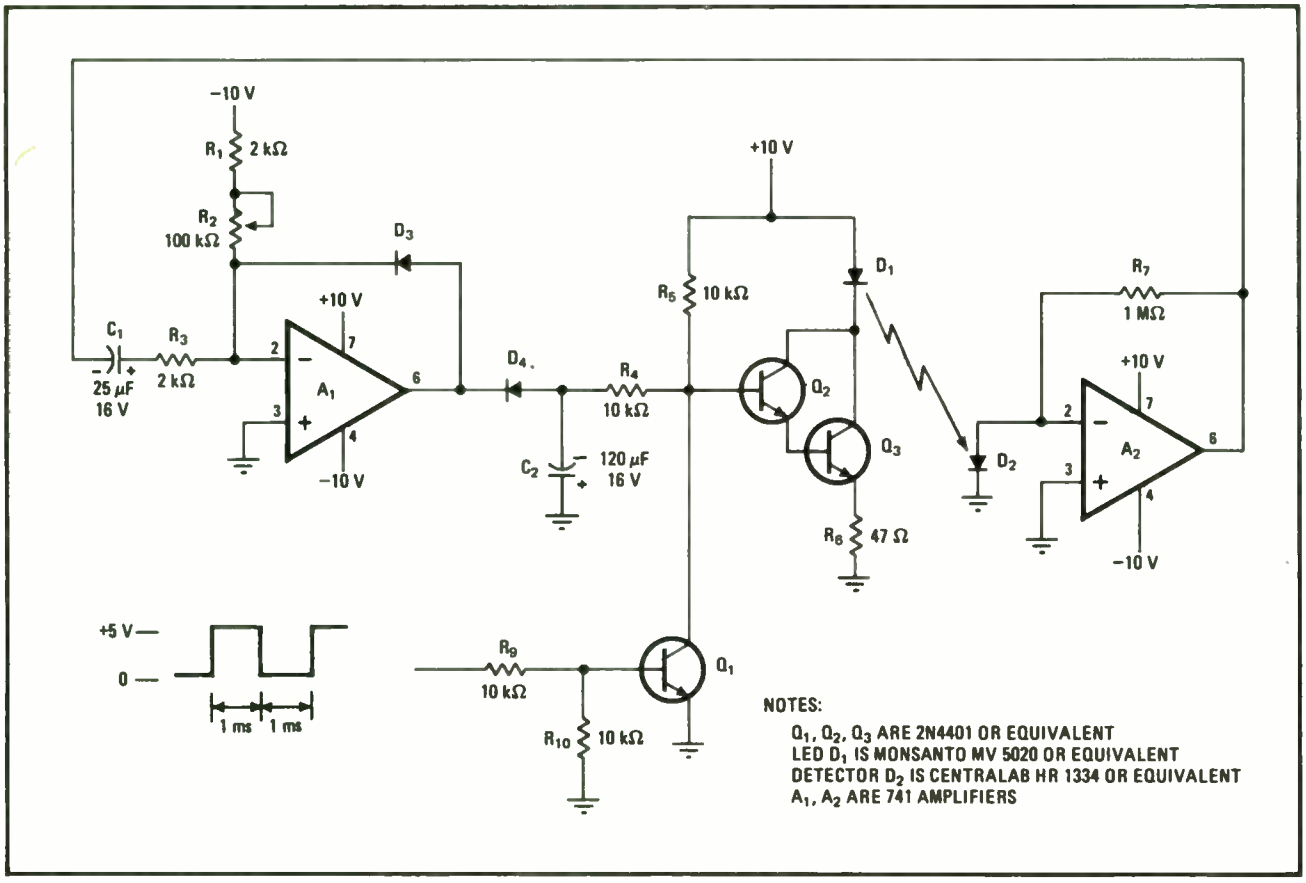
Light intensity is regulated by a silicon planar photovoltaic diode, D_2, the ac response of which is almost constant with temperature or time. Its current is converted to voltage by amplifier A_2 and resistor R_7. This diode is connected in a short-circuit mode to minimize its dark current.

D_1, a light-emitting diode, is driven by Darlington-connected transistors Q_2 and Q_3; its current is proportional to the voltage at the base of Q_2. Transistor Q_1, which is driven by a positive-going square wave, chops the dc level at the base of Q_2 so that it operates in an ac mode.

When the capacitively coupled output of amplifier A_2 is positive, amplifier A_1 charges capacitor C_2, when necessary, to maintain the current through R_3 equal to the current through R_1 and R_2. Because the current through R_1 and R_2 is constant, the amplitude of the square-wave signal at the junction of C_1 and R_3 is held constant.

When the output of A_2 is negative, the capacitively-coupled output of amplifier A_1 goes positive, but is clamped to 0.7 volt by diode D_3. This clamping maintains the output of the amplifier in the active region so that a virtual ground potential is maintained at its summing point. The light intensity level is adjusted by potentiometer R_2. The peak-to-peak voltage at the output of amplifier A_2 is held at $40/(R_1 + R_2)$ volts, where R_1 and R_2 are in kilohms.

Diode D_2 can be mounted near the LED, but to one side of the direct beam, so that it picks up enough light to generate the feedback signal but doesn't interfere with the primary detection function. □



Steady glow. Feedback loop senses variations in output of light-emitting diode, which may occur as temperature changes. Photodiode response is almost constant with temperature; it is amplified, and signal controls another amplifier whose output controls LED drive circuit.

Analog voltage sensor controls LED threshold

by Thomas Mazur
Motorola Semiconductor Products, Phoenix, Ariz.

Most light-emitting diodes are found in alphanumeric displays and optically isolated circuits where they are usually controlled, either directly or indirectly, by digital logic systems. Analog LED control circuits can also be useful, provided that distinct light/dark LED transitions can be obtained. The scanning circuit in the diagram employs silicon unilateral switches, which function like four-layer diodes but have a gate control to produce sharp LED transitions for voltage-level sensing applications.

There are N circuit sections, depending on the number of voltage levels to be sensed. Each section consists of a LED, a silicon unilateral switch, a zener diode, a bipolar transistor, and two biasing resistors. The unilateral switch begins to conduct when its terminal voltage reaches a critical level, nominally 8 volts. Once the switch is turned on, its terminal voltage decreases to approximately 1 V.

While switch voltage is increasing, the LED and the transistor's base-emitter junction become forward-biased. LED current, which is limited by the emitter resistor, rises until the unilateral switch conducts. Since the transistor junction and the LED require around 2 V to be forward-biased, the LED shuts off when the switch voltage drops to 1 V.

Whether the switches are on or off, the voltage across the transistors continues to increase with rising input voltage. Because the transistors are separated by zener diodes, each succeeding section operates only after input voltage V_i increases by zener voltage V_Z. Therefore, accurate LED turn-on levels (V_D) can be set and, with the switches providing an abrupt turnoff, incremental control of each LED can be achieved.

Assuming that all the zeners have identical voltage ratings:

$(V_i)_{MIN} = V_{Z1} + V_{EB1} + V_{D1}$

$(V_i)_{MAX} = NV_Z + V_S$

where V_{EB} is transistor emitter-base junction voltage, and V_S is the critical voltage level of the preceding unilateral switch.

The LEDs may be operated sequentially or in an overlapping fashion by varying the type of zener used in each section. For a sequential mode:

V_S is less than or equal to $V_Z + V_{EB} + V_D$

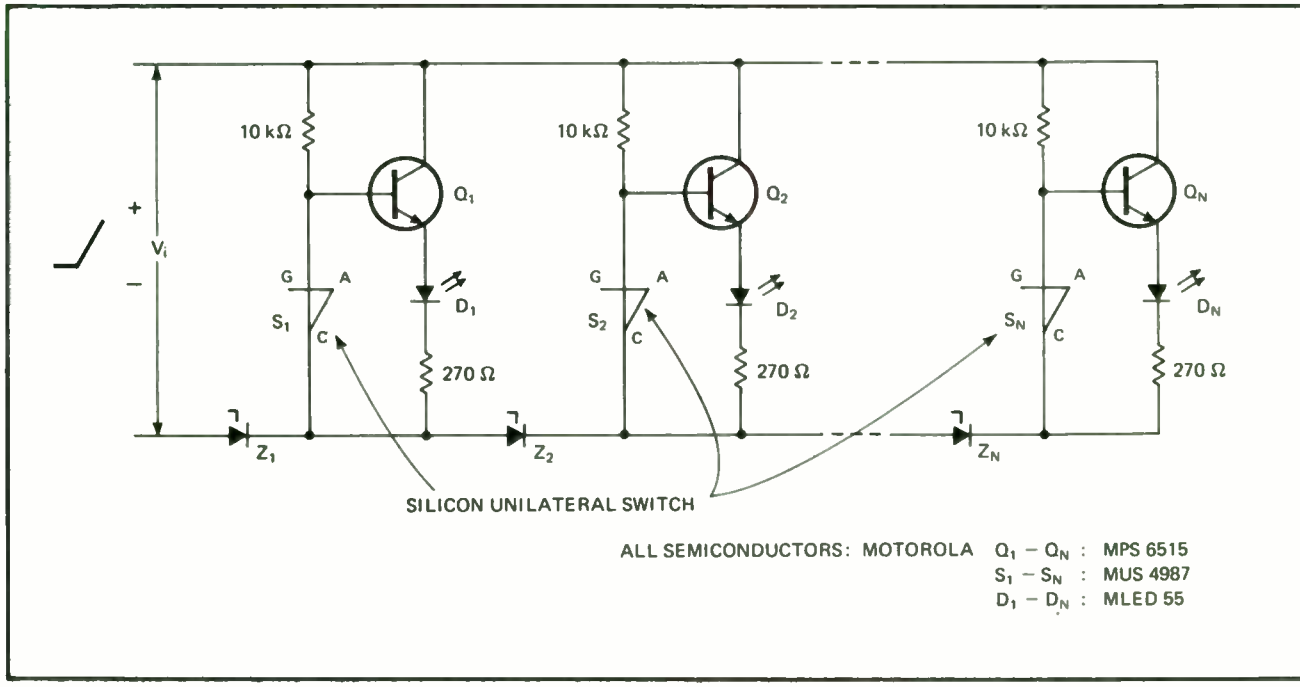
For an overlapping mode:

V_S is greater than or equal to $V_Z + V_{EB} + V_D$

In addition, the level of V_S may be reduced by connecting a zener diode between a switch's gate and cathode terminals.

The scanning circuit may be modified to provide highly discernible visual indication by replacing the emitter resistors by constant-current sources. This supplies the LEDs with uniform current pulses, allowing each one to produce a constant light output. Another modification permits the circuit to serve as a data transfer mechanism—phototransistors can be inserted between the LEDs and the emitter resistors so that the LEDs can be optically modulated. □

LED scanning circuit. Silicon unilateral switches S_1 through S_N require 8 volts to trigger, but only 1 V to stay on. Rising input voltage forward-biases transistor Q_1 and light-emitting diode D_1. LED emits light until switch S_1 conducts; it goes dark abruptly when switch voltage drops to 1 V. Zener diodes Z_1 through Z_N establish voltage levels that are sensed by each section of scanning circuit.



Matched optical couplers stabilize isolation circuit

by Arnold Nielsen
Ford Motor Co., Dearborn, Mich.

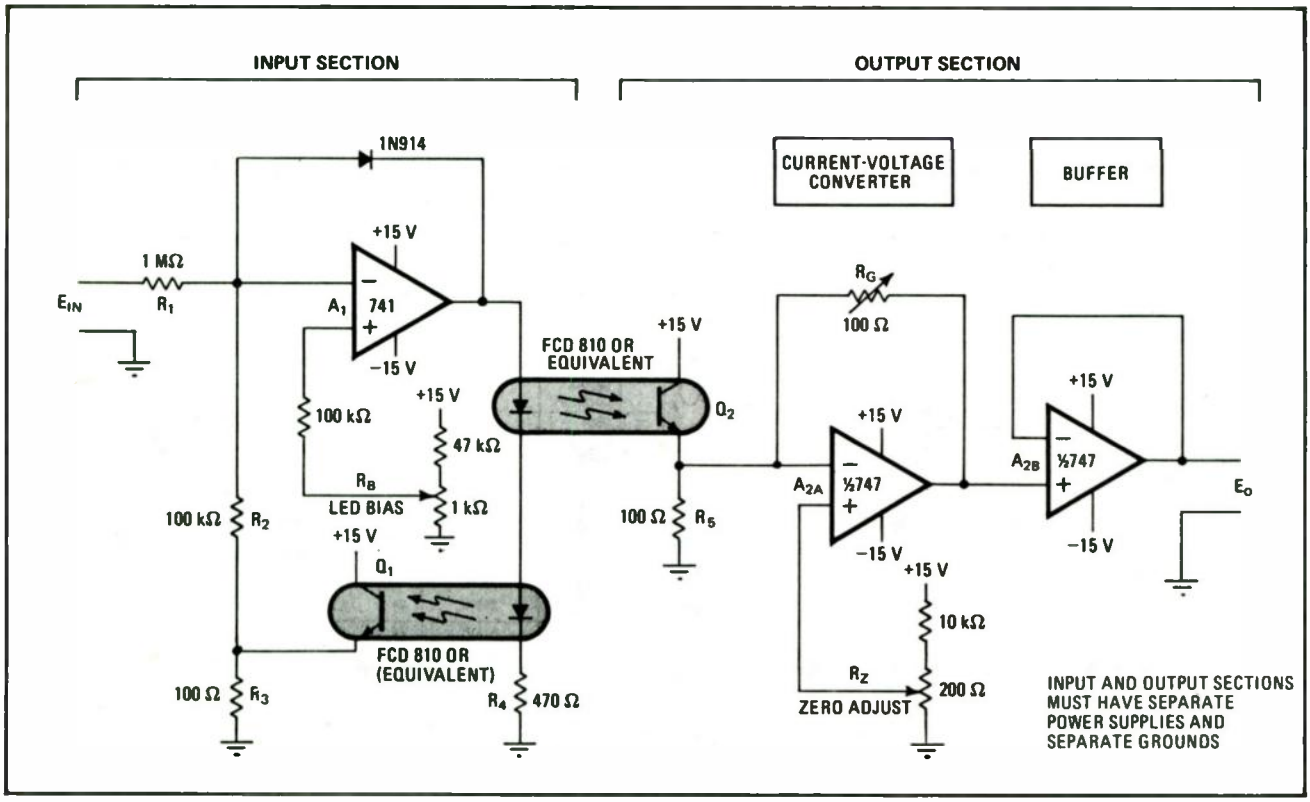
Temperature independence in an isolation circuit can be achieved by using a matched pair of optical couplers. In any optocoupler, the transfer characteristic is a function of T, and therefore the gain of an isolator with a single coupler depends on the temperature. But a second coupler in a feedback arrangement can cancel out temperature effects if the thermal characteristics of the two couplers are alike.

As the diagram shows, the light-emitting diodes of the two couplers are connected in series so that an input signal causes the same current to flow through both of them. One LED couples the input section of the circuit to the output section, and the other LED provides the feedback path that stabilizes the circuit. Thus, any temperature effect that changes coupling to the output section also changes the amount of feedback so that over-all circuit gain remains constant. The feedback also compensates for coupling nonlinearity.

A voltage from the LED bias potentiometer is fed to the noninverting-input terminal of operational amplifier A_1. This voltage, amplified through A_1, sets the LEDs in their most linear operating range. When an input signal is applied to the inverting terminal, operational amplifier A_1 drives the LEDs to a level at which collector current from Q_1 makes $I_{R2} = I_{R1}$, so that the inverting input is at virtual ground. (The 1N914 diode protects the LEDs against negative overvoltages; it is not part of the feedback circuit for A_1.) Because the LEDs are in series and are matched, $I_{R3} = I_{R5}$.

In the output section, the collector-to-base capacitance of Q_2 tends to decrease the frequency response of the circuit. This tendency is overcome by operating op amp A_{2A} in the current-to-voltage-converter mode, which maintains the signal voltage at the inverting input of A_{2A} and across Q_2 at virtual ground. Amplifier A_{2B} provides buffering at the output. The output voltage, E_O, is given by

$$E_O = I_{R5}R_G = I_{R3}R_G$$
$$\approx (R_2 + R_3)I_{R2}R_G/R_3$$
$$\approx (R_2 + R_3)E_{IN}R_G/R_1R_3$$



Stabilized by feedback. To avoid ground loop in instrumentation system, isolation between input and output is provided by optical coupling and by use of separate power supplies for each section. Temperature-sensitivity of optocoupler is compensated by second coupler in feedback loop of input op amp. The light-emitting-diodes are forward-biased for best linearity, and the feedback circuit further cancels nonlinear effects. Circuit operates with input signals of 0 to ±3 V at frequencies from dc to 50 kHz. Gain is 0.1 for circuit shown.

Therefore the gain (or attenuation) of the circuit can be stated as

$$E_O/E_{IN} \approx (R_2 + R_3)R_G/R_1R_3$$

For the component values shown in the diagram, the gain is approximately 0.1.

When the circuit is turned on, a sine wave is fed into the input. The output is displayed on a scope, and R_B is adjusted for symmetrical clipping as the signal amplitude is raised to 3 V. Then the input terminals are short-circuited, and potentiometer R_Z is adjusted so that the output voltage is zero. Finally, a 1-V signal is applied to the input, and R_G is adjusted to give the desired output level (0.1 V in this example). The gain then remains constant to within ±5% for any operating temperature between 0°C and 80°C.

The input signal can have any value from 0 to ±3 V, and the frequency response is determined mainly by the op amps used. The circuit shown here operates from dc to 50 kilohertz, where the signal is down 3 dB. The degree of isolation depends on the isolation resistance of the power supplies used for the input and output sections of the circuit. Therefore, power supplies that have high isolation resistance and electrostatic shielding are recommended, especially at low-millivolt signal levels. Isolation of at least 80 dB should be achieved without difficulty.

This circuit can be used as a single isolation amplifier or as part of a signal-distribution system. In the system application, one signal is common to all of the input sections, but the output sections are completely isolated from one another. □

Optocoupler converts ac tone to digital logic levels

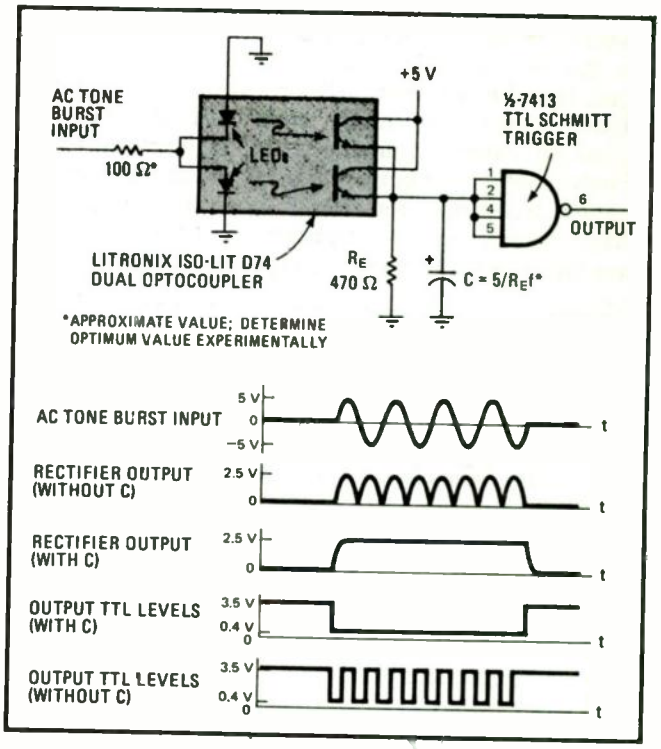
by Louis E. Frenzel
Heath Co., Benton Harbor, Mich.

In some tone signaling, telemetry, and data communications applications, it is necessary to convert an ac tone burst or a few consecutive sine-wave cycles into a logic pulse of the same duration. This can be done by rectifying and filtering the tone burst, then shaping it as required to develop the binary logic levels. In the circuit described here, the rectification of audio-frequency signals is performed by optical couplers—an approach that uses a minimum of components and therefore ensures low cost, high reliability, and small size.

A dual optocoupler using LEDs and phototransistors is connected so that it operates as a full-wave rectifier. The advantage of an optocoupler here is that the usual push-pull ac signal source (center tapped transformer, two op amps, etc.) is not required, considerably reducing the circuit's size, weight, and cost.

The ac tone burst can be applied directly to the LEDs in the optocoupler, as shown, if enough signal power is available. Otherwise, an amplifier can be used; a 741 op amp works well. The two LEDs in the coupler conduct on alternate half-cycles of the ac input, so that a pulsating dc signal is developed across emitter resistor R_E. The transistors in the optocoupler are connected as emitter followers with a common emitter resistor. Capacitor C filters the pulses across R_E into a dc level. The value of C is a function of the size of R_E, the frequency of the tone burst, f, and the size of the load. A capacitance of $5/R_Ef$ is a good starting value, but it should then be adjusted for optimum results.

The dc across R_E and C is shaped by a 7413 TTL Schmitt trigger IC. The output is a clean rectangular pulse with the proper TTL logic levels, as shown in the attached waveforms.



Rectify lightly. Dual optocoupler is full-wave rectifier for ac pulse signals, driving Schmitt trigger to produce rectangular pulses at TTL logic levels. Parts count, cost, size, and weight of circuit are all low; reliability is high. Waveforms show performance and also illustrate frequency-doubler operation of circuit when capacitor is removed.

An optocoupler can be used to advantage in any application requiring full-wave rectification for frequencies well beyond the audio range.

Removing the filter capacitor from the circuit described turns the output into a series of rectangular pulses occuring at twice the frequency of the input. With this minor modification, the circuit performs as a frequency doubler. □

Optically coupled ringer doesn't load phone line

by William D. Kraengel Jr.
Valley Stream, N.Y.

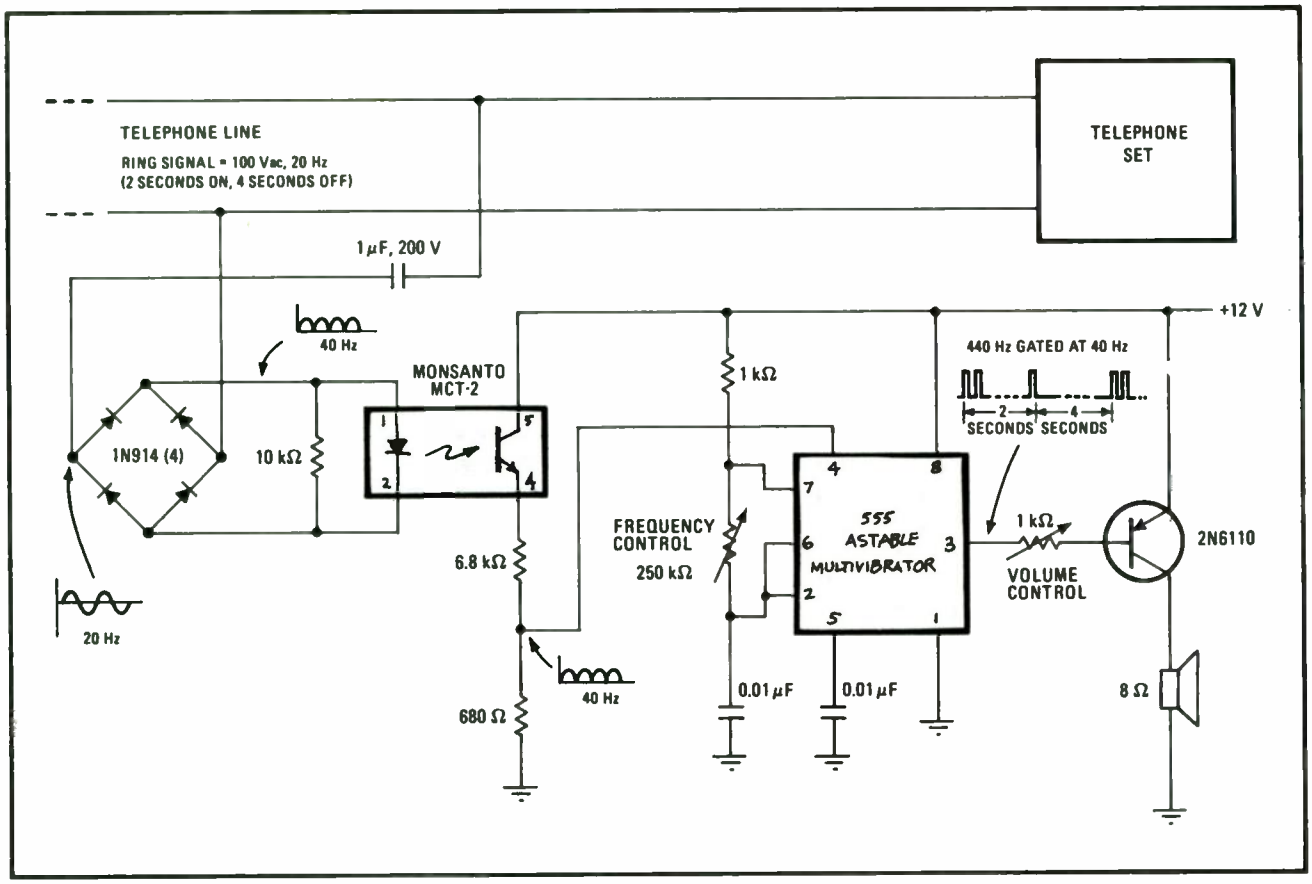
If passed through an opto-coupler, the ringing signal on a telephone line can be made to operate a remote ringer without overloading telephone-company lines, without interfering with company service, and without degrading operation of the line receiving the signal. The opto-coupler can also be used to operate other equipment, such as a telephone message recorder. The arrangement imposes only a 10-milliampere load on the ac ringing signal and no load at all on the dc voice signals.

In this arrangement, the opto-coupler transfers the ringing signal to the rest of the remote-ringer circuitry and also isolates that circuitry from the telephone line. The output current from the opto-coupler activates a 555 timer that is configured as an astable multivibrator; the audio frequency from the multivibrator, amplified and fed to the remote loudspeaker, then sounds whenever a ringing signal comes in on the telephone line.

As indicated on the circuit diagram, the telephone ringing signal of about 100 volts at 20 hertz has a cycle of 2 seconds on and 4 seconds off. This signal is applied to the light-emitting diode of the opto-coupler through a 1-microfarad capacitor; the capacitive reactance at 20 Hz is about 10 kilohms, which limits the current of the light-emitting diode to 10 mA. The frequency is doubled by the full-wave bridge simply because a 40-Hz gating rate in the sound from the loudspeaker is more pleasing to the ear than a 20-Hz rate.

The 40-Hz output from the coupler is applied to the reset input of the 555 multivibrator. The free-running frequency of the multivibrator is set at a nominal 440 Hz, which is the frequency of the ring-back tone in a telephone, or at whatever frequency is most pleasing to the listener. The frequency can be adjusted by the 250-kilohm resistor. The free-running duty cycle, which would be fixed at 50% by the 1-kilohm resistor, is approximately 35% here because of the 40-Hz modulation of the gating signal.

The output from a 555 timer is sufficient to drive a small speaker through a current-limiting series capacitor with no further amplification. In most applications, however, power-amplification is required. The amplification need only be of the switching type because of the rectangular output of the 555. At current levels below



Remote ringer. Opto-coupler flashes telephone-ringing signal to remote-ringer circuitry and isolates that circuitry from phone line. Circuit puts 10-mA load on ac ringing signal, and no load on dc voice signals. Frequency and volume at remote loudspeaker can be adjusted.

50 mA, the 555 is more effective as a current sink than as a current source; for maximum efficiency and power output, therefore, a pnp switching transistor is used.

The component values shown produce an output power of about 5.5 W, which is almost the theoretical maximum that can be obtained with a single 8-ohm speaker, a V_{CC} of 12 V, and a 35% duty cycle. Higher output-power levels can be achieved by greater amplification or lower speaker impedance. At higher levels, multiple speakers can be used in a series-parallel arrangement, with each speaker using a matching L-pad for individual level control.

This circuit draws a standby power of about 120 mW from the 12-V dc supply. To reduce standby power to almost zero, a dual opto-coupler can be used. The second isolated and synchronized output is used to gate a triac static switch that turns on the power supply.

Even though this optical-coupling technique avoids severe loading of the line, the telephone company should be consulted before the ringer is installed. □

35. Oscillators

One-op-amp oscillator keeps sine-wave amplitude constant

by Dale Hileman
Sphygmetrics Inc. Woodland Hills, Calif

A sine-wave oscillator needs precisely controlled feedback to keep its output amplitude constant. But this need complicates its design. A typical unit contains two or three operational amplifiers and perhaps a dozen other components, not to mention an awkward split-stator variable capacitor if a wide, adjustable frequency range is necessary, as in a laboratory sine-wave generator.

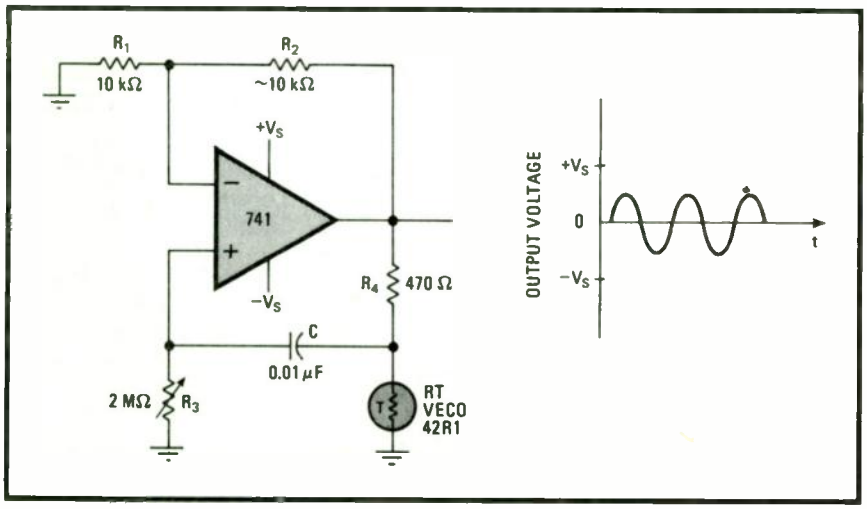
The circuit in the diagram, however, maintains a constant output amplitude over a 10-to-1 frequency range without being unduly complex. From only a single op amp, a half-dozen other parts, and just one variable resistor to adjust frequency, it generates a nearly perfect sine wave.

To produce this sinusoidal output waveform, the circuit includes a voltage divider consisting of R_4 and negative-temperature-coefficient thermistor RT in the feedback loop to the noninverting input. The thermistor stabilizes the feedback; if the output increases, the resistance of RT decreases and thus reduces the regeneration. Resistors R_1 and R_2 in the negative-feedback path prevent oscillations from building up to become distorted.

The amplitude of the output signal in this oscillator configuration is extremely sensitive to feedback variations, so only a small change in the thermistor resistance is required to stabilize the output signal. This principle has the same effect that a very high loop gain would have in any other servo-type system. As a result, the output level is held constant over a wide frequency-adjustment range.

The frequency of oscillation, which is an inverse function of the product R_3C, is controlled by varying R_3. A clean sinusoidal output ranging from 2 to 20 kilohertz is generated as the frequency is varied. A resistor may be connected in series with R_3 to avoid distortion near the extreme low-resistance setting. A different value for C of course gives a different tuning range.

Supply voltage is not critical—values of $\pm V_S$ can be in the range from 3 to 18 volts. The amplitude of the output sine wave, which must be substantially less than V_S to avoid distortion, is set by selection of R_2. If this resistor is a potentiometer, it must not be a noisy one because noise in the feedback loop produces a disproportionately noisy output. A ±10-V supply typically allows an output sine wave of 10 V peak to peak. □



Watch the sines. Voltage divider, consisting of R_4 and NTC thermistor RT, controls the positive feedback in op-amp oscillator circuit to produce clean constant-amplitude sine waves over the 2-to-20-kHz frequency range Resistors R_1 and R_2 in negative-feedback path hold overall amplifier gain near unity amplitude is set by value of R_1.

Low-distortion oscillator uses state-variable filter

by Walter G. Jung
Forest Hill, Md.

The state-variable filter, which in any case excels as a flexible active-filter design block, can also be made to oscillate with only a little additional circuit complexity. With high-performance quad op amps now readily available, a single integrated circuit makes a ultra-low-distortion sine-wave oscillator with a output frequency of up to 5 kilohertz and three output phases for driving servo or instrumentation systems.

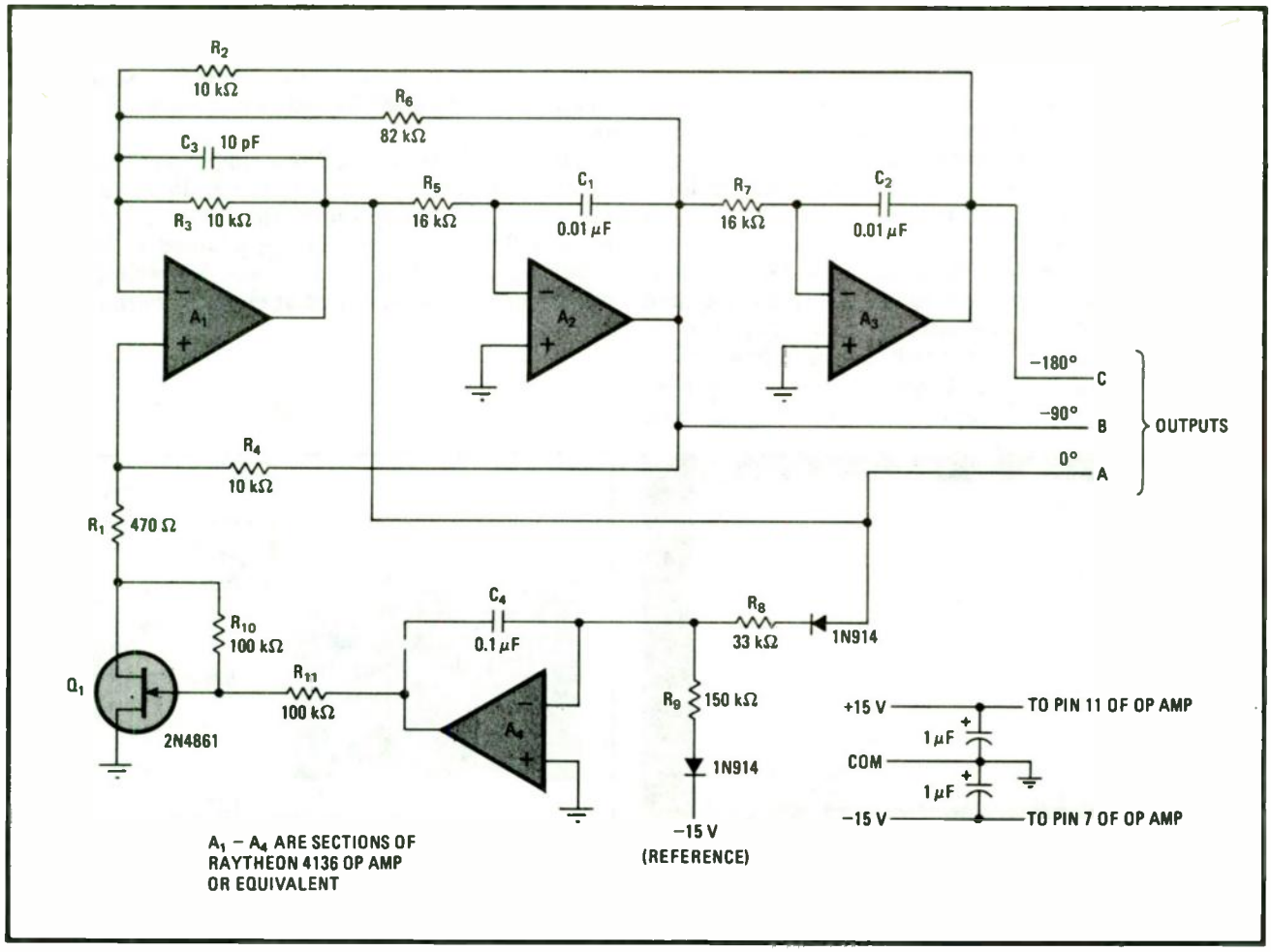
The schematic diagram shows the circuit of the oscillator. Operational amplifiers A_1, A_2, and A_3 comprise the state-variable filter, with its normal negative feedback path via R_4; positive feedback to sustain oscillation is provided by R_6. The oscillation frequency is given by:

$$f = \frac{1}{2\pi RC}$$

where R is the value of equal resistors R_5 and R_7 and C is the value of equal capacitors C_1 and C_2. For the circuit shown, f is 1 kilohertz.

As in other sine-wave oscillators, the positive and negative feedback paths must be carefully balanced to attain—and sustain—low-distortion operation. The balance is achieved by use of some type of automatic gain control; in this circuit the mechanism is the variable channel resistance of field-effect transistor Q_1.

The agc circuit in itself comprises an active loop that serves several important purposes. The integrator A_4 filters and smoothes the rectified output to provide a dc control voltage for the gate of Q_1. Low ripple on this control voltage is necessary to prevent modulation distortion on the output. The high dc gain of the integrator automatically adjusts the loop to the required dc bias for Q_1 in spite of parameter variations, thus eliminating



State-variable oscillator. Addition of regenerative feedback via R_6 changes state-variable filter into sine-wave oscillator with three phases of output. Filter uses three of the amplifiers in a quad op amp IC; the fourth amplifier is part of agc loop that ensures ultra-low distortion.

the necessity for device selection. The output voltage is regulated to a value that causes the average current in R_8 to be equal to that in R_9. Thus R_9 and the -15-V supply serve as a reference, and the agc loop tracks this reference to maintain the output peak voltage at about 10 V.

Resistors R_{10} and R_{11} provide a local feedback path around Q_1, to reduce distortion drastically below the straightforward connection. The high values of feedback resistance (100 kilohms) in relation to Q_1's "on" resistance (nominally 100 ohms) prevent undesirable interaction of the ac and dc signals.

In operation, the total harmonic distortion at the A output is on the order of 0.02%, and distortion in the B and C outputs is considerably less because of the low-pass filtering in the A_2 and A_3 integrator circuits. All outputs appear at the same level, with the phase relations shown.

The prototype of this circuit uses a Raytheon 4136 quad op amp, which has a 3-megahertz bandwidth. The Harris 4741, with similar ac characteristics, is another suitable unit. The Motorola 3403 and National 348, both 1-MHz devices, provide ultra-low-distortion performance at frequencies up to 2 kHz. The main asset of a quad device for this circuit is its cost-effectiveness—the entire circuit can be built for $10 or less. □

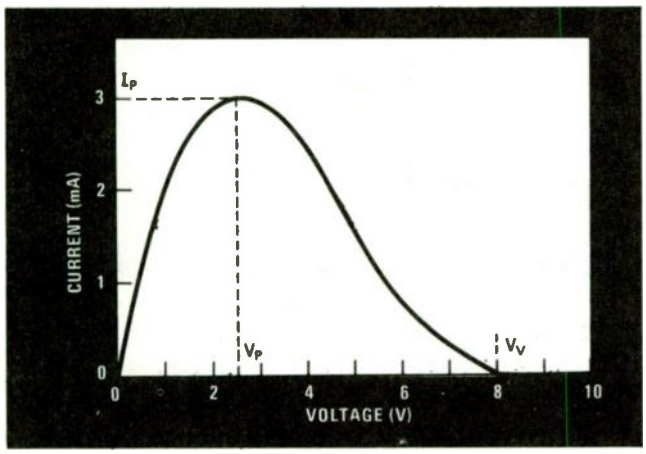
Complementary JFETS form bimode oscillator

by Gregory Hodowanec
Newark, N.J.

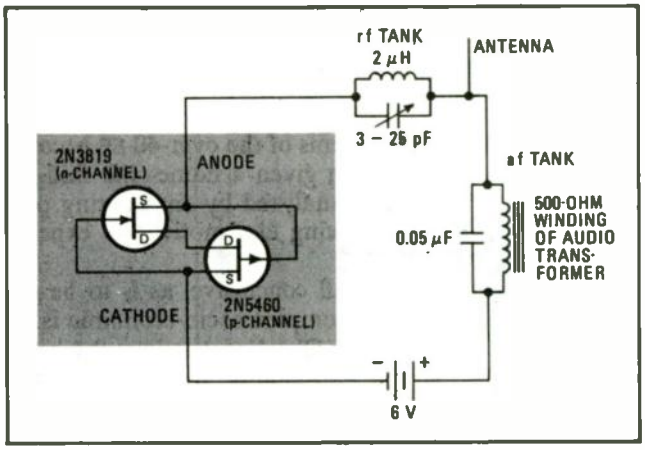
A complementary pair of junction field-effect transistors can be interconnected to form a negative-resistance two-terminal device, which makes a simple oscillator. In monolithic form this configuration is called a lambda diode [*Electronics*, June 26, 1975] and is available with a wide range of characteristics. If two discrete JFETs are connected to make the diode, they do not have to be matched, but can be chosen to provide various values of peak current and negative-resistance-voltage range. Figure 1 shows current as a function of voltage for a combination consisting of an n-channel 2N3819 and a p-channel 2N5460.

The JFET "diode" can be made to oscillate at frequencies ranging from audio to vhf. All that is required is to connect the diode in series with an inductance-capacitance tank circuit and supply a bias voltage in the negative-resistance region. Figure 2 shows a simple bimode oscillator circuit capable of oscillating at both audio and radio frequencies simultaneously. Oscillation is at approximately the natural resonances of each tank circuit. The radio-frequency tank, consisting of a 2-microhenry choke shunted by a trimmer capacitor, can be tuned over a wide range centered near 20 megahertz. The audio section uses the 500-ohm winding of a miniature audio output transformer and a 0.05-microfarad ceramic capacitor for oscillation at approximately 440 hertz. The audio section cleanly amplitude-modulates the rf section, as demonstrated by reception of the radiated signal on a communications receiver. Power output is in the order of 25 milliwatts and the signal has a range of several hundred feet with no antenna on the oscillator. The range can be extended to several thousand feet with a short length of antenna, so a form of this oscillator can be adapted to radio-control appplications.

This circuit can be used as a simple signal source for many experimental purposes. The audio section can be eliminated or shorted out if an unmodulated signal is desired. The circuit can also be adapted to any design requiring a low-level signal source. Variable frequency control can be incorporated at either or both frequency levels. □



1. Negative resistance. Current-voltage characteristics are shown for a "diode" consisting of the arrangement of the two complementary JFETS shown in Fig. 2. For any terminal voltage between 2.5 V and 8 V, the combination has a negative resistance.



2. Bimode oscillator. JFET-combination "diode" and two tank circuits can oscillate at audio frequency and radio frequency simultaneously. Resultant signal is rf modulated by af; either component can be varied for communications or control applications.

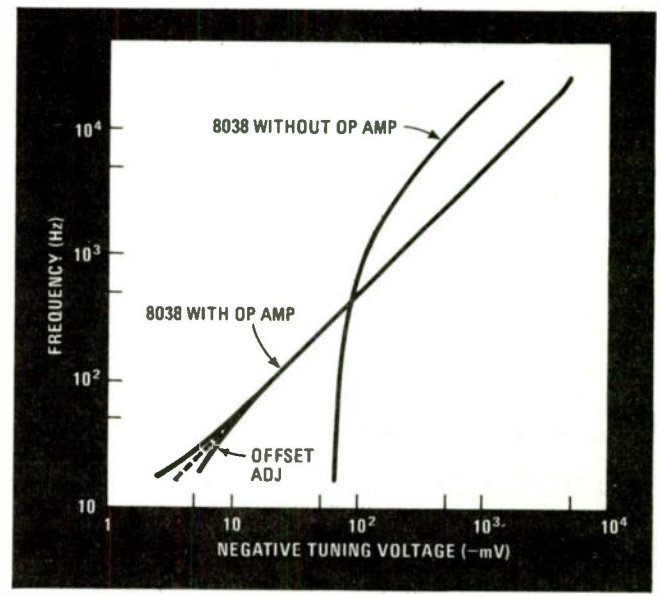
Modified function generator yields linear VCO

by Antonio Tagliavini
Bologna, Italy

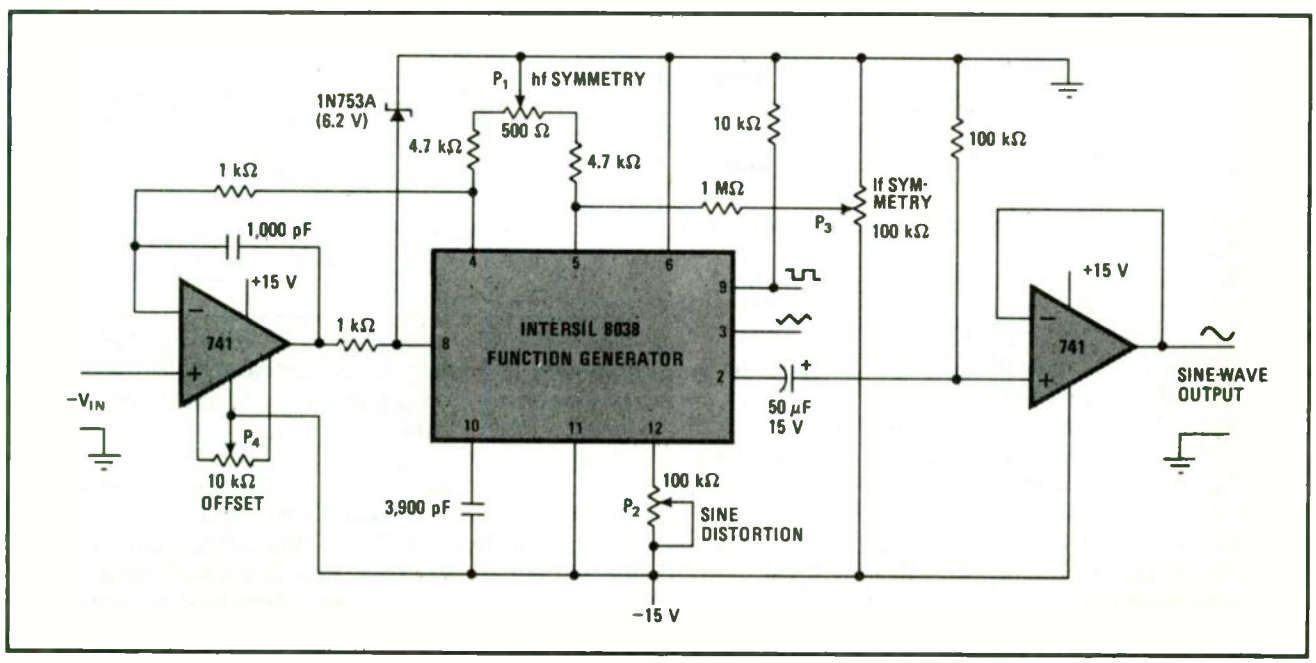
Because of its wide sweep capability, the Intersil 8038 integrated function generator is useful for realizing a voltage-controlled oscillator with a sine-wave output. But because of the limitations of the 8038's integrated current sources, its frequency-versus-voltage characteristic is nonlinear over a good part of its sweep range. As Fig. 1 shows, however, the tuning can be made linear over the entire audio range if an external operational amplifier is added before the function generator's control input.

The 8038 contains two current sources. One is always operating, supplying an external integrating capacitor with a constant current I. The other is switched on and off by a level comparator, supplying the capacitor with a current -2I when on. Therefore the capacitor is charged by I and discharged by -I, producing a symmetrical triangular wave (which is then converted into a sine wave) with a frequency that is proportional to current I. This current does not vary linearly with the input voltage, and therefore the relationship between input voltage and frequency is not linear.

To linearize the relationship, the timing voltage is applied to the control input terminal of the 8038 (pin 8) through an operational amplifier, as shown in Fig. 2. The op amp drives the integrated non-switched current source, and because the voltage fed back to the inverting input terminal of the op amp must equal V_{in}, the



1. All straightened out. Voltage/frequency characteristic of the Intersil 8038 voltage-controlled audio-frequency oscillator is not linear. But if the input voltage is applied to the 8038 through an operational amplifier, with feedback through one of the integrated current sources on the IC chip, the tuning curve becomes a straight line.



2. Line straightener. Linear VCO circuit uses 741 op-amp input to linearize one of the two current sources in the 8038 function generator. Because the two sources are inherently matched, the second source tracks the first and also gives linear current-to-voltage response. Output op-amp buffer provides low output impedance. Pots shape sinusoidal output wave form and maintain linearity at low frequencies.

current supplied by this source varies directly with V_{in}. The two integrated current generators in the 8038 are inherently matched, so the switched source tracks the non-switched one and therefore is also linearized. The switched source drives a current inverter/doubler that provides the current -2I.

The 1N753A zener diode protects the control input of the function generator IC against voltages more positive than +0.6 volt and more negative than -6.2 V. The output operational amplifier is merely a buffer, and may be omitted if low output impedance is not required.

Three potentiometers permit shaping of the output waveform. First, at a high frequency, P_1 is adjusted to obtain a symmetrical wave shape (square wave from pin 9). Then P_2 is set for best sinusoidal output. Finally P_3 is trimmed for good symmetry at the low-frequency end of the tuning curve. The offset adjustment, P_4, is then adjusted to provide tuning linearity.

With component values shown, the VCO covers the entire audio range (20 to 20,000 hertz). □

ECL tuned oscillators are voltage-stable

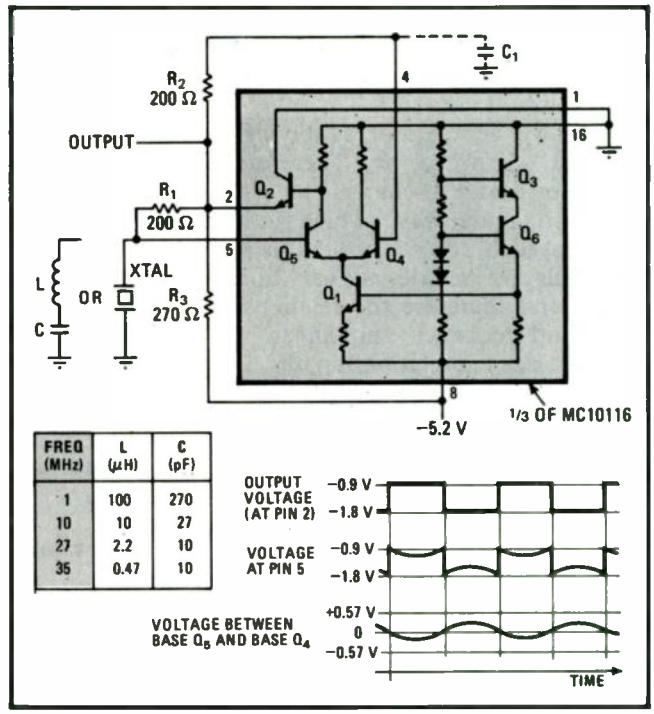
by Tom Hornak
Hewlett-Packard Co., Palo Alto, Calif.

A simple square-wave crystal oscillator or LC oscillator can be built by using one third of an MC10116 integrated circuit, which is a triple differential amplifier in the MECL 10,000 series. It has better frequency stability than a similar oscillator that uses a resistor and capacitor as the frequency-determining elements [see article, page 260]. A 1-volt variation n supply voltage to the RC oscillator caused fractional frequency changes ranging from 0.09 at 10 megahertz to 0.02 at 50 MHz. The same voltage variation changes LC oscillator frequencies of 1, 10, 27, and 35 MHz by less than 0.003; and crystal oscillator frequencies of 10 and 20 MHz are changed less than 5×10^{-6}.

Details of the tuned oscillators are shown in the figure. Transistors Q_1, Q_4, and Q_5 form a differential amplifier. The output signal supplied by emitter follower Q_2 is fed back via resistors R_1 and R_2 to the bases of Q_4 (positive feedback) and Q_5 (negative feedback). If no crystal or LC combination is connected to the bases of Q_4 and Q_5, the feedback signals cancel each other because of the high common-mode rejection of the differential amplifier, and the circuit is thus quiescent.

When an LC circuit or a crystal is connected between the base of Q_5 and ground, the negative-feedback signal is attenuated by the divider consisting of R_1 and the low impedance of the LC circuit or crystal at the series-resonant frequency. Because positive feedback dominates, the circuit oscillates.

The top waveform represents the oscillator's output voltage, i.e. a square wave alternating between ECL logic levels. The middle waveform displays the idealized signal on the base of Q_5, i.e. the output square wave with its fundamental frequency component attenuated by the divider. The bottom waveform represents the difference between the other two waveforms, which is the voltage acting between the bases of Q_5 and Q_4. This voltage, clipped and amplified by the differential amplifier, constitutes the oscillator output voltage. □



Stable. ECL-oscillator frequency, determined by crystal or LC tank circuit, is insensitive to variations in supply voltage. Capacitor C_1 balances stray capacitances (e.g. from crystal holder) that might cause parasitic oscillations; its value is $(R_1/R_2)C_{stray}$.

Antilog function generator keeps VCO output linear

by J. A. Connelly and C. D. Thompson
Georgia Institute of Technology, Atlanta, Ga.

Accurate voltage control of oscillator frequency is crucial for such applications as electronic music synthesizers, filter test circuits, and phase-locked loops. In the voltage-controlled oscillator (VCO) described here, each 1-volt change in the control voltage changes the output frequency by one octave with a maximum deviation of ±0.4% over the entire audio range. This precision is achieved by temperature-compensation and buffering.

Circuit can be built with readily available parts, and the design equations allow adjustability and flexibility to meet a variety of specific needs. The total range of oscillation frequency can be shifted down one octave, for example, by doubling the capacitance of C_1 in the VCO.

This VCO is basically a relaxation oscillator: current source Q_5 charges low-leakage polystyrene capacitor C_1 until unijunction transistor Q_4 fires (at about 9 V); C_1 then discharges rapidly, and the cycle starts all over again. The sawtooth output voltage essentially results from the voltage across C_1 minus a couple of junction voltages, buffered by high-impedance MOSFET Q_2; by Q_3, which carries the current to fire Q_4; and by the unity-gain op amp. Most of the resistors limit transistor currents to safe levels.

The oscillation frequency is determined by the charging current into C_1. This current, which is the collector current from Q_{5B}, depends upon the control voltage because the base-to-emitter voltage V_{BE} in both halves of Q_5 is derived from the control voltage, thus,

$$I_C = \beta I_S \exp(qV_{BE}/kT)$$

where β is the short-circuit current gain, I_S is the reverse saturation current, kT/q is 0.026 per volt at 27°C, and V_{BE} is scaled from the control voltage V in a voltage-divider network:

$$V_{BE} = VR_{TC}/(R_{IN} + R_{TC})$$

Therefore, the collector current is given as a function of the control voltage by

$$I_C = \beta I_S \exp\left[\frac{qR_{TC}V}{kT(R_{IN} + R_{TC})}\right] = \beta I_S K^V$$

In this expression, the scale factor K is just a substitution that replaces several terms: that is,

$$K = \exp\left[\frac{qR_{TC}}{kT(R_{IN} + R_{TC})}\right]$$

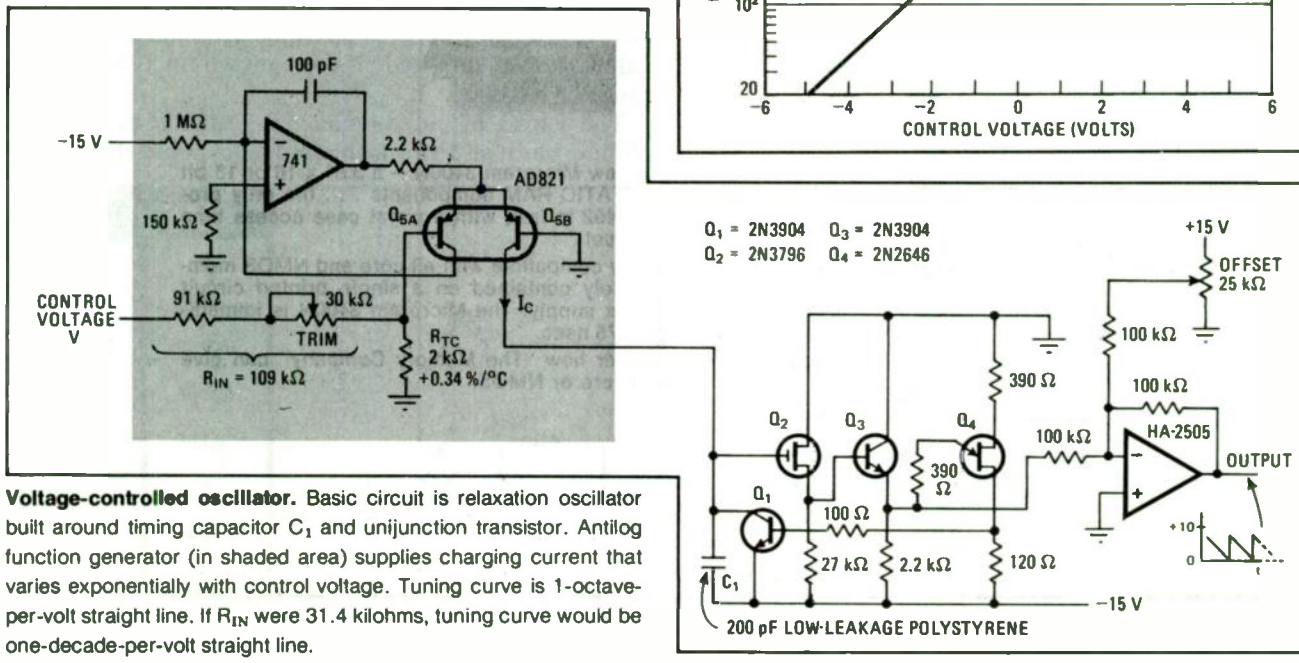
Current I_C is an antilog function (or exponential function) of voltage, and therefore the current source is called an antilog function generator.

Because the frequency is directly proportional to I_C,

$$f \sim K^V = f_0 K^V$$

where f_0 is the free-running frequency (i.e., the oscillator frequency when control voltage V is zero). The frequency f_0 depends on the parameters of Q_5, the firing voltage of Q_4, and the capacitance of C_1.

The value of scale factor K is set by the resistors R_{IN}



Voltage-controlled oscillator. Basic circuit is relaxation oscillator built around timing capacitor C_1 and unijunction transistor. Antilog function generator (in shaded area) supplies charging current that varies exponentially with control voltage. Tuning curve is 1-octave-per-volt straight line. If R_{IN} were 31.4 kilohms, tuning curve would be one-decade-per-volt straight line.

and R_{TC} in the divider network. If K is 10, the oscillation frequency changes by one decade when V changes by 1 V. With the resistance values shown in the circuit diagram, however, K is 2, so the frequency changes by one octave when V changes by 1 V.

The temperature sensitivity of I_C is compensated by the temperature coefficient of thermistor R_{TC}, +0.34%/°C, which is equal in magnitude and opposite in sign to the effect of q/kT in the expression for K. Thus, scale factor K is independent of temperature if the thermistor and Q_5 have equal temperatures. To ensure this condition, the thermistor is mounted in thermal contact with the header of Q_5.

The tuning curve shows the experimental performance of the VCO. The maximum departure from the straight-line relationship is only ±0.4% over the audio-frequency range from 20 Hz to 20 kHz. Outside that range, the voltage control becomes less precise. □

Common silicon diodes stabilize oscillator

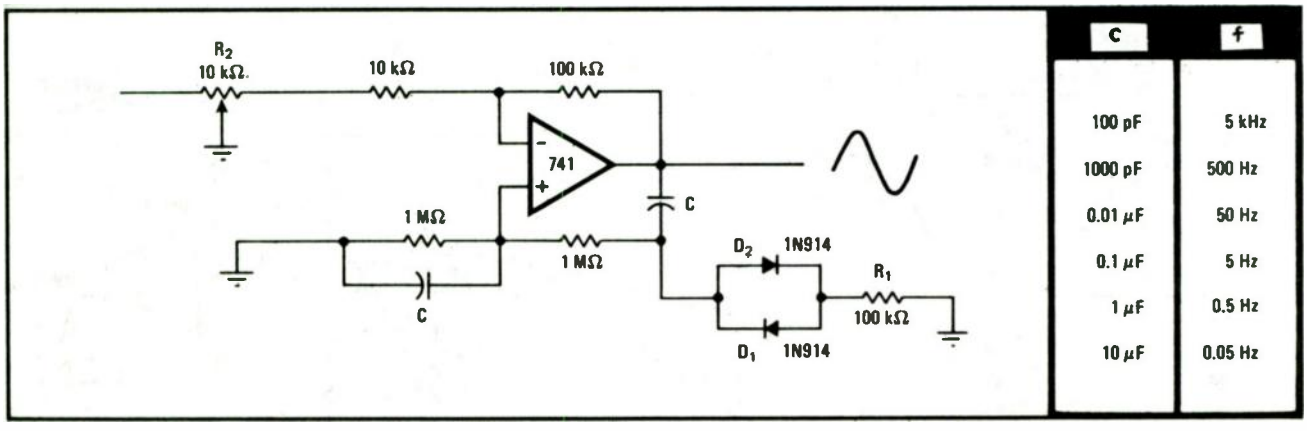
by Dale Hileman
Sphygmetrics Inc., Woodland Hills, Calif.

Two ordinary silicon diodes connected front-to-back in the feedback path of a Wien-bridge oscillator stabilize the feedback without introducing hunting or distortion. Stabilization makes them superior to the more commonly used thermistors or incandescent lamps, which have thermal inertia that introduces hunting when power is turned on or the frequency is changed, and to zener diodes, which distort the waveform.

The front-to-back connection of the silicon diodes simulates a back-to-back series connection of zener diodes, which might otherwise be used at this point in the circuit. Resistor R_1 is added to soften the effect of the knee of the forward-conduction characteristic, which would otherwise introduce distortion.

The best way to change the frequency of this circuit is to change the two capacitors, which must be closely matched. By this means, the output amplitude is always the same, regardless of the frequency. With the circuit values shown, amplitude is constant within ±0.3 dB over range of 100,000 to 1.

The setting of potentiometer R_2 establishes the amplitude, but it also affects the frequency somewhat. □



C	f
100 pF	5 kHz
1000 pF	500 Hz
0.01 μF	50 Hz
0.1 μF	5 Hz
1 μF	0.5 Hz
10 μF	0.05 Hz

Stabilizer. Front-to-back diodes in oscillator's feedback path acts as stabilizer, yet do not cause hunting or distortion, as lamps or zeners sometimes do. Capacitors, which control frequency, are matched; amplitude control is by potentiometer, which also affects frequency.

Stable crystal oscillator works over wide supply range

by Terence King
Oroco Communications Inc., Middletown, N. Y.

If single-gate MOSFETs are wired as a modified Pierce oscillator and an isolating source-follower, they form a crystal oscillator that has unusual supply-voltage stability. This crystal-controlled clock is not expensive to build, interfaces easily with transistor-transistor-logic circuits, and can operate directly from a 5-volt supply.

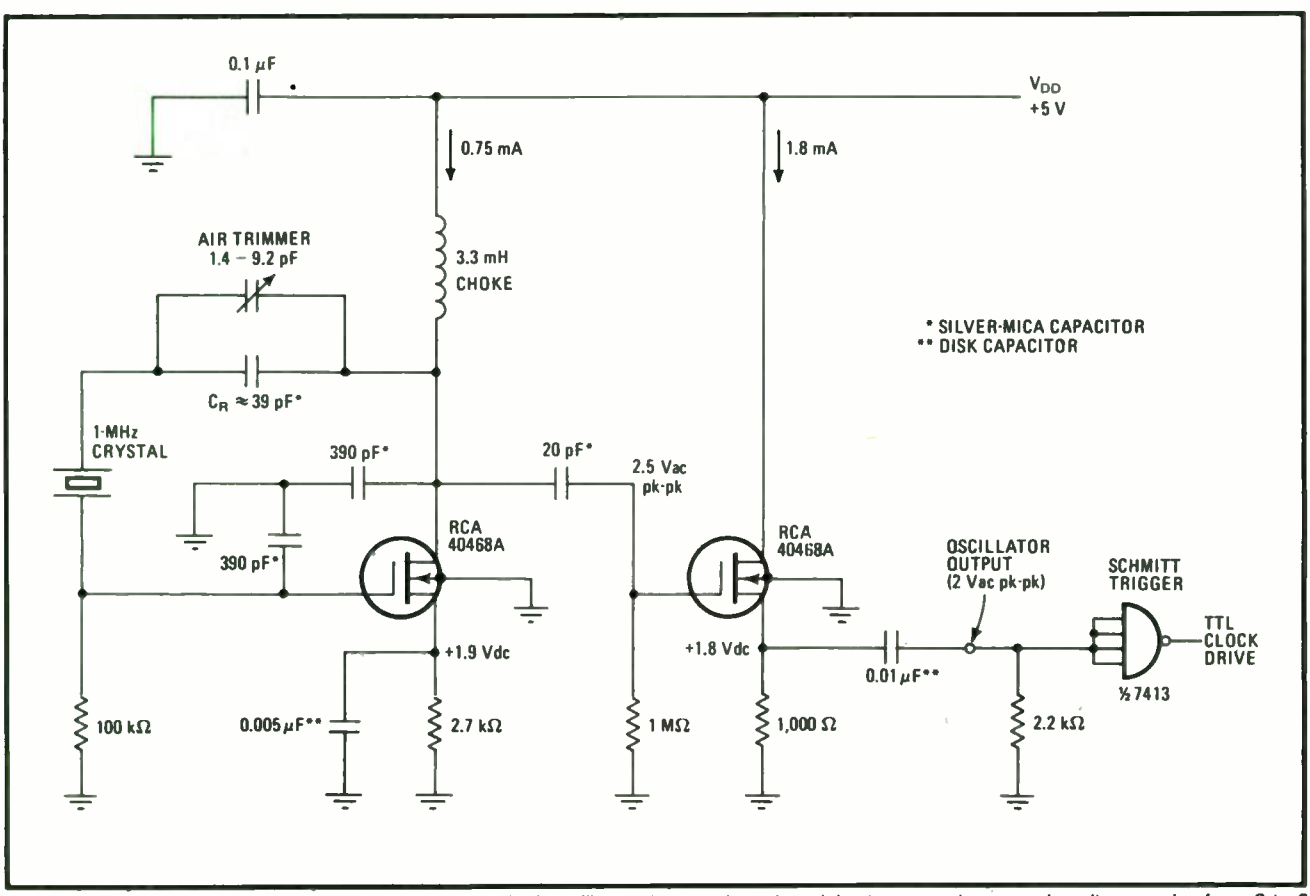
Changes in output frequency due to supply-voltage variations are very small because of the high-value source resistors in both stages and the large fixed capacitances in the gate and drain loops of the oscillator stage. Even if the supply voltage increases from 3 to 9 V, output frequency changes by less than 1 hertz from its nominal 1-megahertz value.

Since the circuit itself is very stable, the over-all performance of the oscillator depends principally on the quality of the crystal. A good oven-stabilized crystal should maintain a stability of one part in 10^{-8} per day after warmup. And if ambient temperature is fairly stable, the whole circuit will approach this performance.

An excellent interface to TTL circuits can be provided by a type-7413 Schmitt trigger. The pulldown resistor of 2.2 kilohms biases the Schmitt trigger within its hysteresis characteristic without excessively loading the oscillator's source-follower. A type-7413 trigger will provide reliable TTL driving with as little as a 3-V supply applied to the oscillator.

The Schmitt's output is rich in rf harmonics and can be beat against a WWV broadcast of the National Bureau of Standards at 10 MHz, allowing adjustment of the oscillator to within 0.1 Hz of its nominal operating frequency without much difficulty. This sort of monitoring also permits relatively sensitive day-to-day checks of the circuit's short-term and long-term stability. Oscillator performance can then be established as a secondary frequency standard that is traceable directly to the National Bureau of Standards.

Capacitor C_R sets the range of the calibration of the trimmer capacitor. The value of C_R may vary with different makes and types of crystals. □



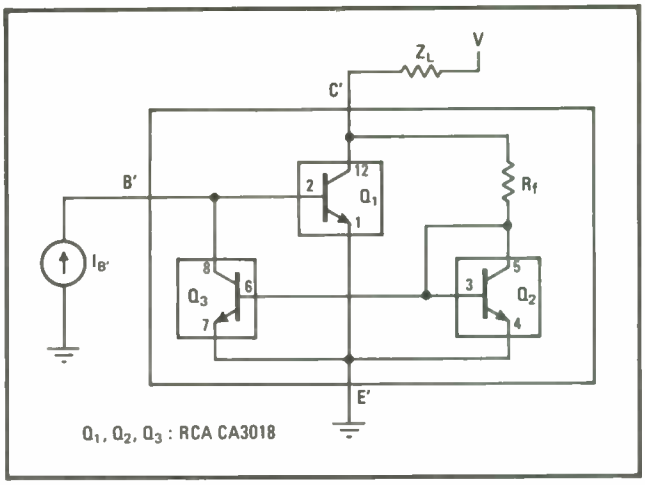
Supply immunity. Output frequency of crystal-controlled oscillator changes less than 1 hertz even when supply voltage varies from 3 to 9 volts. The circuitry—a modified-Pierce-oscillator MOSFET and a source-follower MOSFET—is so stable that over-all oscillator performance depends mostly on the crystal. A Schmitt trigger makes an excellent interface for using the oscillator to drive TTL devices.

Negative-resistance generator has controllable response

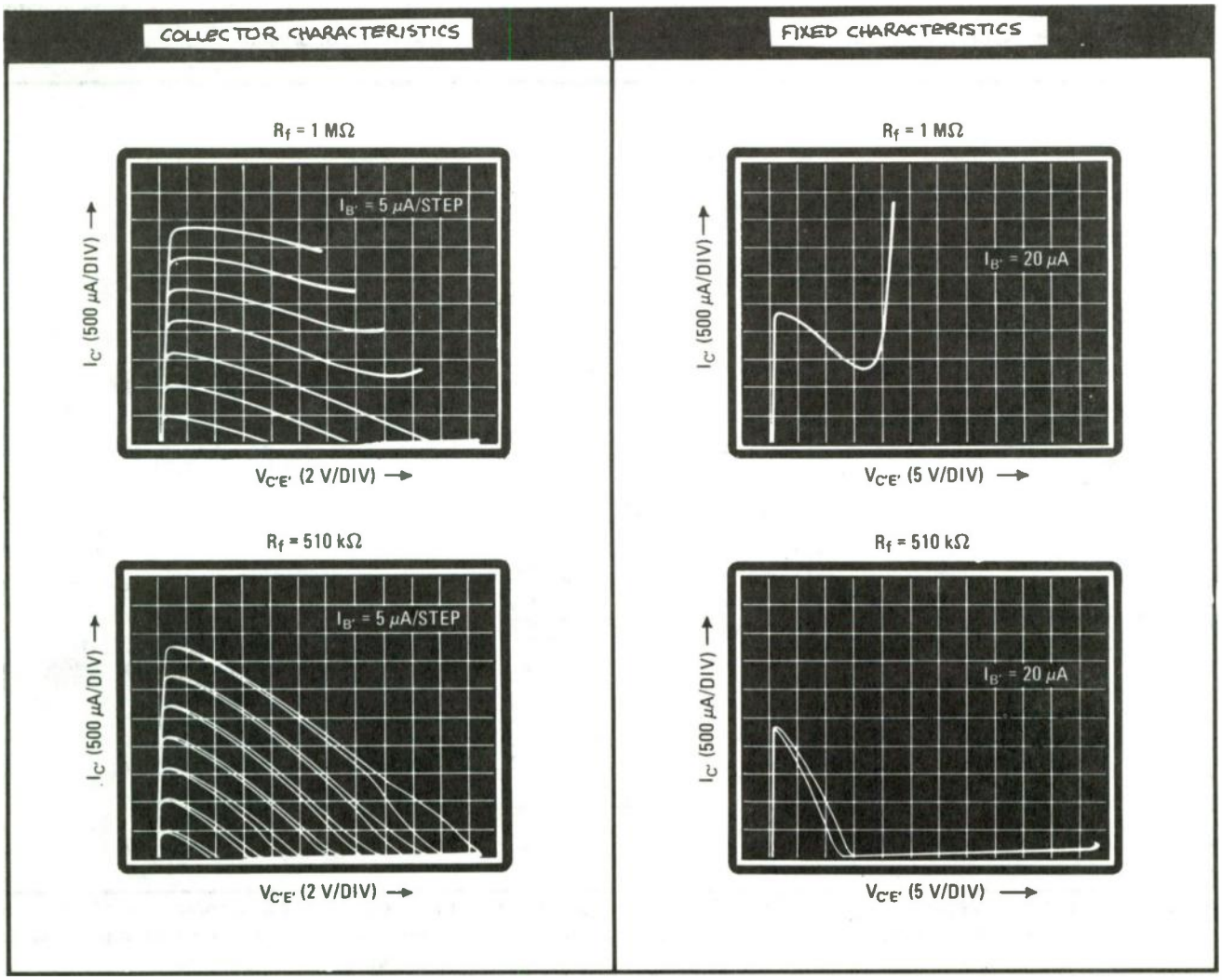
by Samuel E. Bigbie
IBM General Systems Division, Boca Raton, Fla.

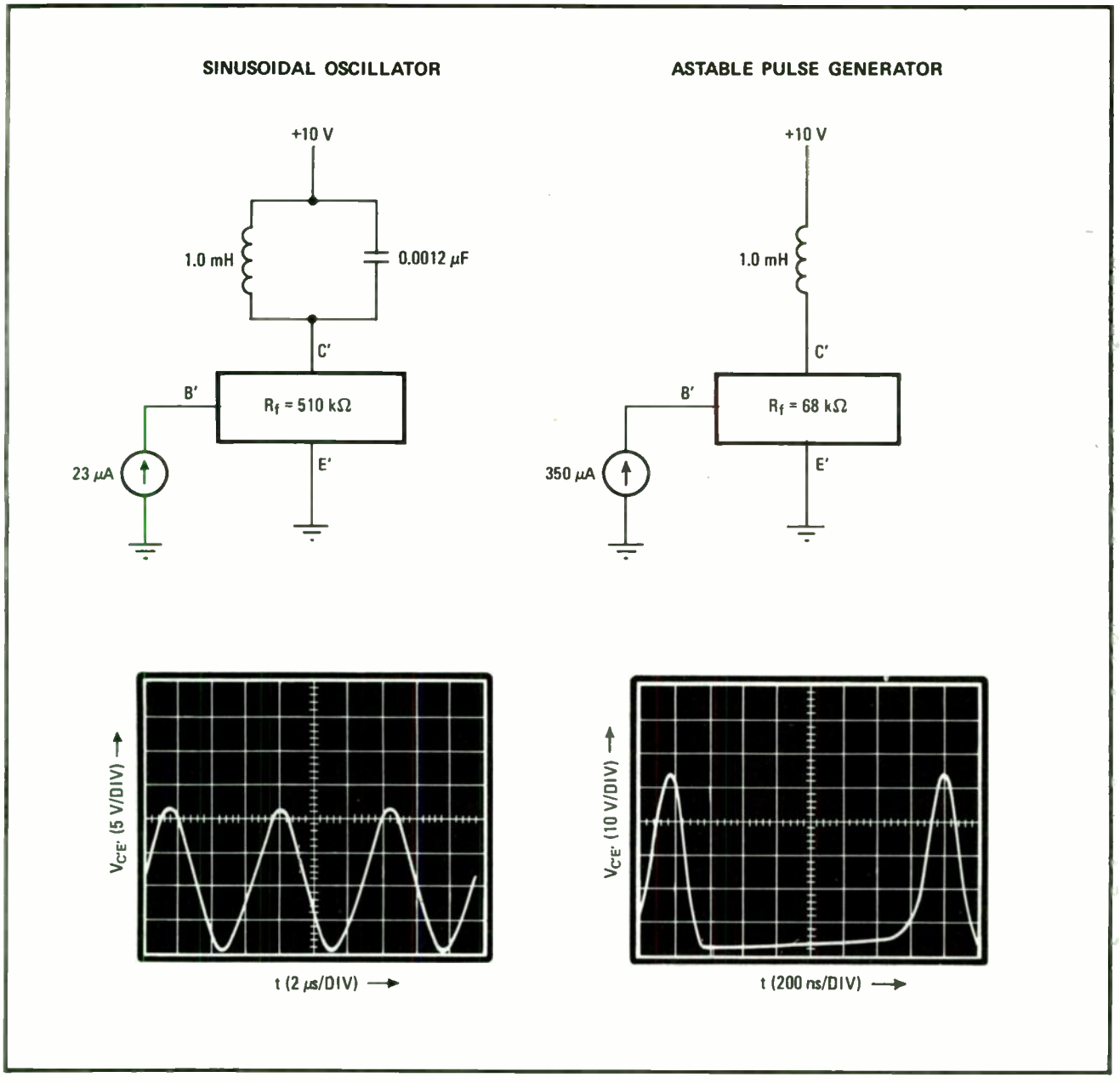
A negative-resistance generator, consisting of three matched transistors, has a current-voltage characteristic that varies with feedback resistance, but not with frequency. When driven by a current source and loaded by an LC resonant circuit, the generator can be operated as a self-starting sinusoidal oscillator. It also can be used for monostable, bistable, or astable pulse generation, as well as oscillator stabilization and switching networks.

The maximum collector current of transistor Q_1 depends on the amount of bias current available at its base terminal. Feedback resistor R_f, along with transistors Q_2 and Q_3, make up a voltage-to-current converter that decreases the base drive of transistor Q_1 when this



Positively negative. Three matched transistors form negative-resistance generator with stable, predictable operating characteristics. Circuit can be treated as transistor that develops negative impedance at terminal C'. Transistors Q_2 and Q_3 and resistor R_f decrease base current of transistor Q_1 whenever Q_1's collector voltage increases. Circuit makes dependable oscillator or pulse generator.





device's collector voltage is increasing.

The negative resistance appearing at Q_1's collector is present at frequencies from dc to several megahertz. The upper frequency limit is determined by the frequency response of both transistor Q_1 and the voltage-to-current converter.

The generator circuit is effectively a three-terminal transistor (with pins labeled B′, C′, and E′). An input current source provides the base current for transistor Q_1, while resistor R_f determines the amount of current fed back to Q_1's base. Because transistors Q_2 and Q_3 are a matched pair and their bases are connected in common, their collector currents will be nearly equal.

As the base current supplied to transistor Q_1 increases, the voltage drop across load impedance Z_L also increases, lowering the potential at Q_1's collector. This lowered potential decreases the collector current through transistors Q_2 and Q_3. The reduced collector current through transistor Q_3 represents an increased impedance at Q_1's base terminal. (A decrease in Q_1's base current has the opposite effect, since Q_3's collector current will be reduced.)

The circuit's operating characteristics are illustrated by the scope traces showing generator performance for two different values of resistor R_f, and for both a fixed and changing bias current. As can be seen, the negative-resistance slope becomes steeper as the value of R_f decreases, from 1 megohm to 510 kilohms, in this instance.

When the load impedance is a parallel LC tank circuit, the negative resistance generator acts as a sinusoidal oscillator, as shown in the figure. Using only an inductor as the load impedance yields an astable pulse generator, which has an output pulse amplitude that equals the breakdown voltage of the combined transistors between terminals C′ and E′. □

BIBLIOGRAPHY

Millman, Jacob, and Taub, Herbert, *Pulse, Digital and Switching Waveforms*, McGraw-Hill Book Co., New York, 1965, pp.452–512.

ECL IC oscillates from 10 to 50 MHz

by William A. Palm
Control Data Corp., Minneapolis, Minn

One of the simplest of oscillators, the emitter-coupled-logic type outlined in Fig. 1, uses one third of the circuitry of an MC10116 ECL integrated circuit. Besides the IC, the only elements required for the oscillator are resistor R and capacitor C. The frequency of oscillation equals 1/3.4 RC.

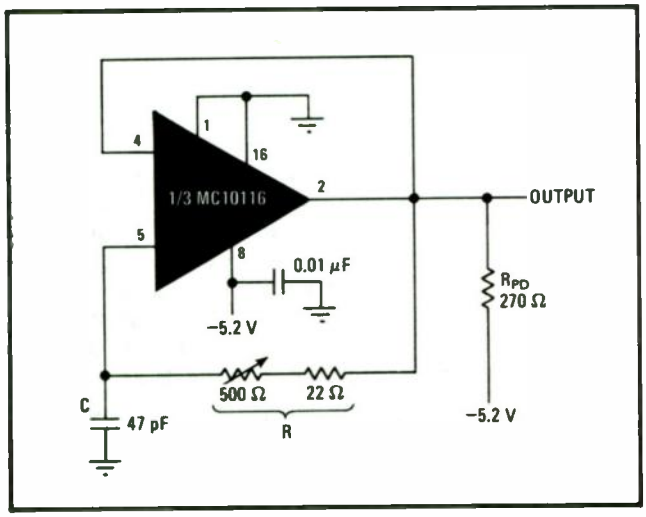
Details of the oscillator are shown in Fig. 2. Transistor Q_1 is a constant-current source for the differential amplifier made up of Q_4 and Q_5. The output signal, taken from emitter-follower Q_2 at pin 2, is fed back to Q_4 as the oscillator reference voltage at pin 4. Thus, pins 2 and 4 are always at the same voltage, and they switch between the ECL levels shown in the waveforms.

Operation of the circuit is indicated by the waveforms of voltage at pins 2 and 4, and at pin 5. The capacitor charges and discharges through resistor R when pins 2 and 4 go higher or lower than pin 5. When pins 2 and 4 are high, Q_4 conducts and Q_5 is off; the capacitor charges up until Q_5 starts to conduct, whereupon Q_4 cuts off and the voltage at pins 2 and 4 drops. The capacitor then discharges; when the capacitor voltage gets low enough, Q_4 starts to conduct, Q_5 cuts off, and the voltage at pins 2 and 4 jumps up. Thus, the capacitor voltage at pin 5 chases the voltage at pins 2 and 4, but never reaches their level because of the limited gain of the amplifier (approximately 8).

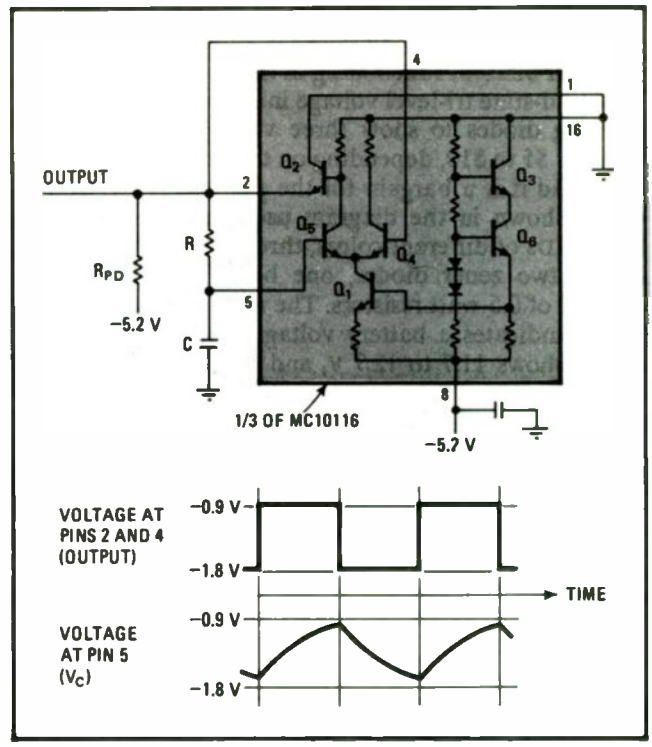
Values of R and C are not critical. The resistance of R can be as high as several kilohms or as low as 20 ohms. As R becomes smaller, pull-down resistor R_{PD} must also become smaller to keep emitter-follower Q_2 in conduction. For maximum oscillation frequency, R can be 20 ohms and C a few picofarads. The adjustable oscillator in Fig. 1 oscillates at frequencies in the range from 10 to 50 megahertz. Other choices for C and R can produce osillation at frequencies ranging from audio to vhf.

The frequency equation is inaccurate at the upper ranges because of propagation time, stray capacitance, and the difference between charge and discharge impedances presented at the output. It is desirable to buffer the oscillator through a second stage of the ECL IC.

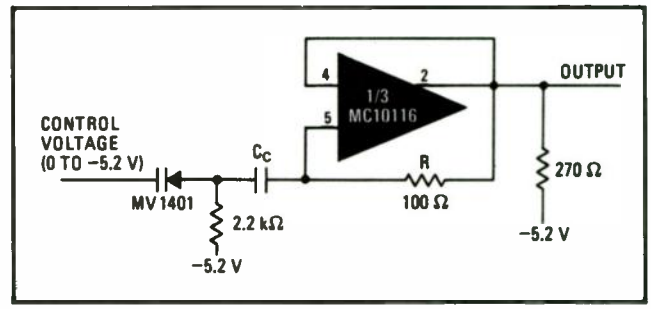
Use of a varactor diode in place of capacitor C, as shown in Fig. 3, makes the circuit a voltage-controlled oscillator. A varactor with a capacitance range of 10:1, such as the MV1401, works well. Coupling capacitance C_C can be much larger than the diode capacitance, or can be chosen to limit the range of deviation. The oscillator in Fig. 3 operates at (15 ±10) MHz for a voltage swing of 0 to −5.2 volts at the VCO input. □



1. Oscillator. Extremely simple connections to emitter-coupled-logic IC result in an oscillator that provides square-wave output. Adjustment of R tunes frequency across a range of 10 to 50 MHz. Different R and C permit band-switching over a 10:1 range of frequencies.



2. Operation. Circuit diagram shows how ECL oscillator operates. Output voltage is fed back to Q_4. Capacitor voltage at pin 5 tries to reach voltage at pin 4, causing output to switch between different ECL levels. Oscillator can never hang up.



3. Voltage tuning. Varactor diode in place of C makes circuit a voltage-controlled oscillator. This VCO operates at (15 ±10) MHz.

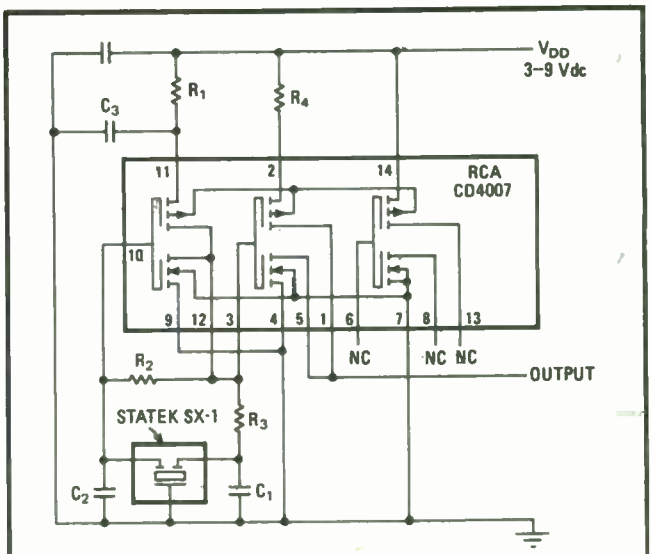
C-MOS minimizes the size of crystal oscillators

by S.S. Chuang
Statek Corp., Orange, Calif.

The improved manufacturing technology and dropping costs of crystals, coupled with the advantages of complementary-MOS, are making the crystal-controlled oscillator a better design choice than the less accurate and less stable RC and LC oscillators.

Ultraminiature quartz crystals can now be produced with photolithographic techniques, such as those used for making integrated circuits. This means that these crystals can be manufactured in volume by batch processes at very low cost. They are rugged devices that are shaped like tuning forks, typically measuring 150 to 250 mils long, 25 to 40 mils wide, and 1 mil thick. These crystals are available with operating frequencies as low as 10 kilohertz and are excellent for fabricating hybrid-circuit constructions.

For only a few dollars, a C-MOS crystal oscillator (a), which can be powered from a supply voltage between 3 and 9 volts, can be built. And with the proper component selection, this oscillator will draw as little as 10 microamperes from a 5-V supply. Another low-power os-

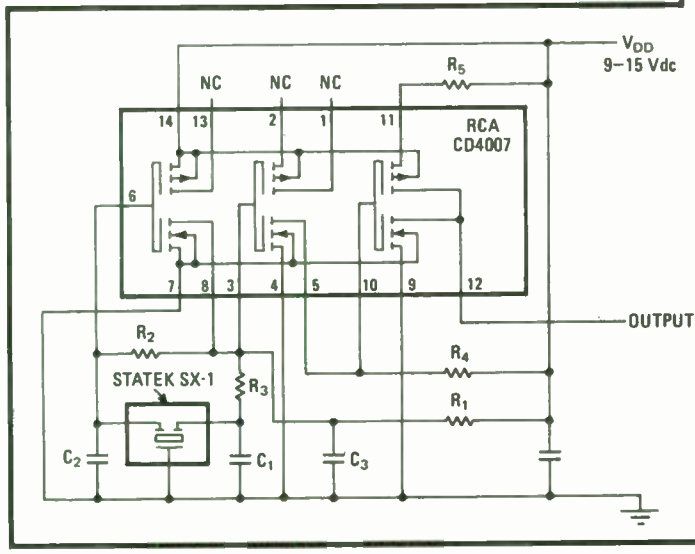


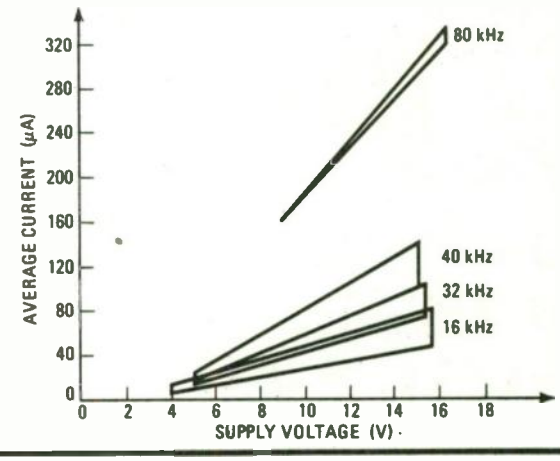
(a)

TYPICAL COMPONENT VALUES						
Frequency (kHz)	C_1 (pF)	C_2 (pF)	R_1 (kΩ)	R_2 (MΩ)	R_3 (kΩ)	R_4 (kΩ)
10–40	20	5	100	22	500	10
40–100	10	0	100	22	50	10

(b)

TYPICAL COMPONENT VALUES							
Frequency (kHz)	C_1 (pF)	C_2 (pF)	R_1 (kΩ)	R_2 (MΩ)	R_3 (kΩ)	R_4 (kΩ)	R_5 (kΩ)
10–40	20	5	1000	22	330	220	10
40–100	10	0	500	22	100	86	10





Perfect circuit mates. Crystals that are manufactured like ICs make ideal companion components for the conventional C-MOS inverter. Resulting low-power crystal oscillator is both small and inexpensive. Supply voltage can be 3 to 9 volts, as in (a), or 9 to 15 V, as in (b).

cillator design (b) can also be built to run from a higher supply voltage, from 9 to 15 V.

In both circuits, a standard C-MOS inverter package is used to make up the oscillator and buffer amplifier sections. Supply voltage V_{DD} must be sufficiently greater than the sum of the threshold voltages of the n- and p-channel MOSFETs to provide a bias current for the amplifier. This current allows the circuit to develop enough gain to start and maintain oscillation. For either circuit, the driving voltage for the crystal must not exceed 2 V peak to peak. The tables list typical component values for two ranges of operating frequencies.

In oscillator (b), an n-channel MOSFET is used in the oscillator stage as well as the first stage of the buffer amplifier. Complementary MOSFETs form the output stage of the buffer amplifier. The crystal-drive voltage is limited to between 0.6 and 1.4 V. Supply voltage V_{DD} can be 5 to 15 V for frequencies of 10–60 kHz, and 9 to 15 V for frequencies over 60 kHz. The graph is a plot of the average current drawn by this oscillator for various supply voltages and operating frequencies.

The components in each of the oscillators perform the same functions. Resistor R_1 sets the gain of the amplifier in the oscillator stage, thereby determining the circuit's output voltage and the crystal-drive level. This resistor also reduces the current drain of the over-all circuit. Its value depends on operating frequency and supply voltage.

Resistor R_2 is a biasing resistor, and it must be large enough to avoid affecting the phase of the circuit's feedback network. Resistor R_3 limits the crystal-drive level, while providing a voltage that is large enough to drive the first stage of the buffer amplifier. This resistor also supplies the appropriate phase shift when the crystal "tank" circuit is operated slightly below anti-resonance.

Resistor R_4, as well as resistor R_5 for oscillator (b), determines the output voltages of the first and second stages of the buffer amplifier, in addition to limiting the current in the buffer amplifier. It must be large enough to allow the amplifier to saturate, yet small enough to give the amplifier sufficient drive capability.

Capacitor C_1 sets the level of the crystal-drive voltage; it also provides the appropriate phase shift in the feedback network. Capacitor C_2 governs the input voltage of the oscillator stage; its value is optimized by trading off frequency stability against gain. The decoupling capacitor, C_3, is selected, along with resistor R_1, to give an RC time constant that isolates the circuit from low-frequency noise. In the n-channel design, capacitor C_3 can even be eliminated. □

ECL gates stretch oscillator range

by William Blood
Motorola Semiconductor Products Inc., Phoenix, Ariz.

The frequency range of crystal-controlled oscillators can be extended easily with emitter-coupled logic gates. Selecting the proper crystal and the right number of frequency doublers results in accurate frequency signals over the range of 150 to 250 megahertz. Standard crystals are normally limited to less than 150 MHz because of the number of crystal overtones required to achieve higher frequencies.

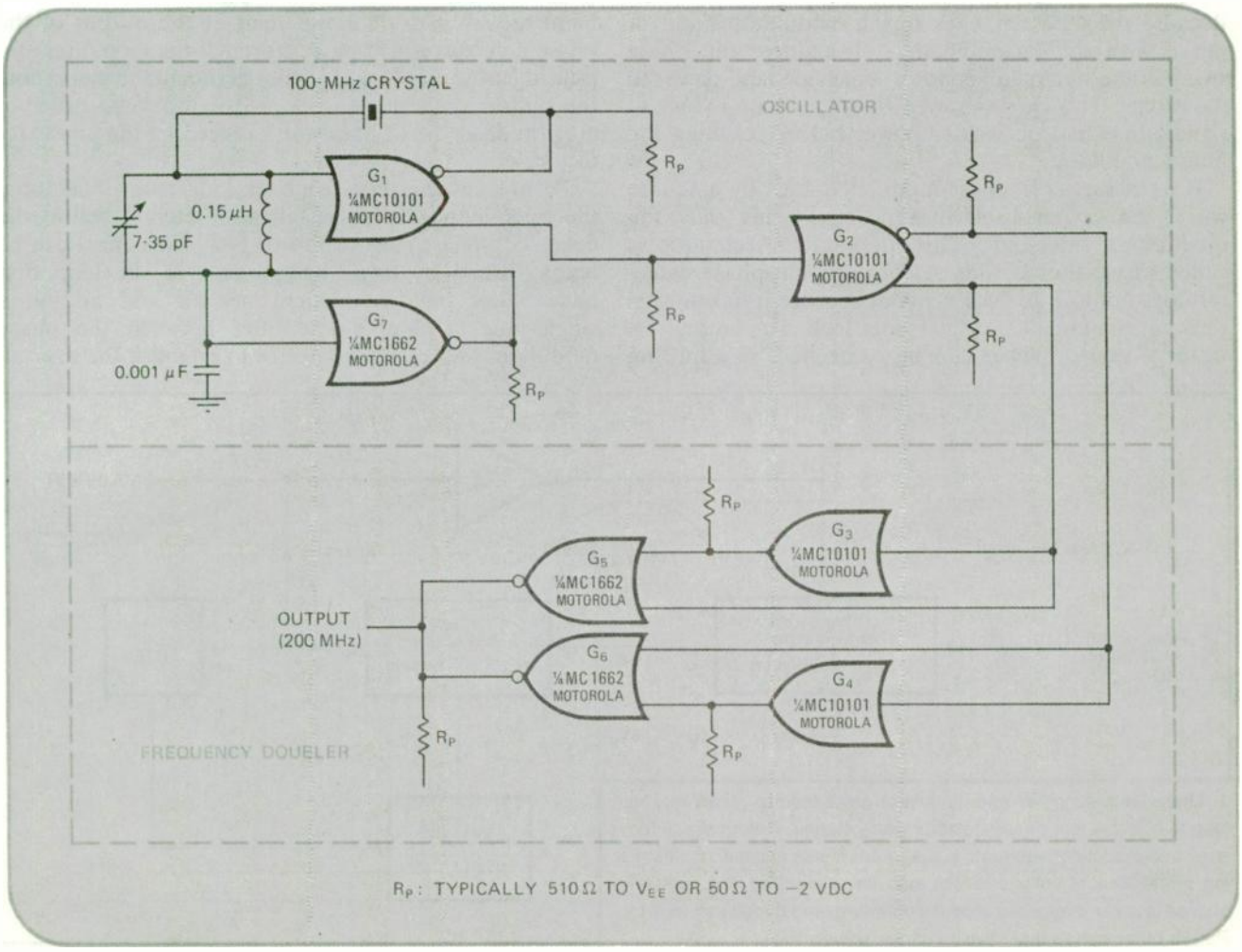
A 200-MHz crystal-controlled oscillator that is built with only two integrated circuit packages is shown in the diagram. Two types of ECL gates, one with a propagation delay of 1 nanosecond and the other with a 2-ns delay, are used for best performance.

In the oscillating section of the circuit, the crystal is in series with a feedback loop from the NOR output of a 2-ns gate, G_1. The LC tank circuit tunes the 100-MHz crystal overtone, and also acts as a fine-tuner. Another 2-ns gate, G_2, from the OR output of G_1, buffers the oscillating section and provides a complementary output.

The frequency doubler section of the circuit consists of two 2-ns gates (G_3 and G_4) performing as phase shifters, and two high-speed 1-ns NOR gates (G_5 and G_6) operating as summers. For a 50% output duty cycle, the complementary 100-MHz signals should be delayed one-fourth of a cycle, or 2.5 ns. This may be done precisely with delay lines, or approximated with gates G_5 and G_6, as shown. The gating method is easier to implement and causes only a slight offset in output duty cycle. Gates G_5 and G_6 combine the four-phase 100-MHz signals, yielding a 200-MHz output frequency, when their outputs are wired-OR.

A third 1-ns gate G_7 is used as a bias generator for the crystal oscillating section. Tying the output of this NOR gate back to its input assures that the oscillating section remains biased in the center of its linear region over wide temperature and power supply extremes.

Speeding up crystal oscillators. Emitter-coupled logic gates can increase the frequency output of crystal-controlled oscillators to 250 megahertz. For 200-MHz output, LC tank tunes 100-MHz overtone of crystal, while gate G_2 forms complementary 100-MHz signals. Phase shifters G_3 and G_4 and wired-OR summers G_5 and G_6 then delay and double these signals. Gate G_7 provides buffered bias supply for gate G_1.



36. Phase-lock circuits

Feedback in phase-locked loop linearizes phase demodulator

by Ron Rippy
Rf Technology Branch, Goddard Space Flight Center, Greenbelt, Md.

The phase of a carrier wave is easy to change, and therefore phase modulation (PM) is convenient in many applications. However, most phase detectors have at least two shortcomings: restriction of the linear operating region to about ±60° and an inability to lock to PM signals that have no carrier power. The circuit in Fig. 1 uses phase-compressive negative feedback to avoid these limitations. The linear operating region is set mainly by a phase modulator, rather than by the usual product detector, and extends to at least ±160°.

As shown in the circuit diagram, the data output from an ordinary phase-locked loop (PLL) is amplified, reversed in phase, and fed back to a linear phase modulator that is connected ahead of the product detector. Because the data fed back to the modulator is out of phase with the incoming data, it reduces the phase swing of the signal and restores some sideband power to the carrier. This carrier power allows the loop to lock to signals that had no carrier power before reaching the phase modulator.

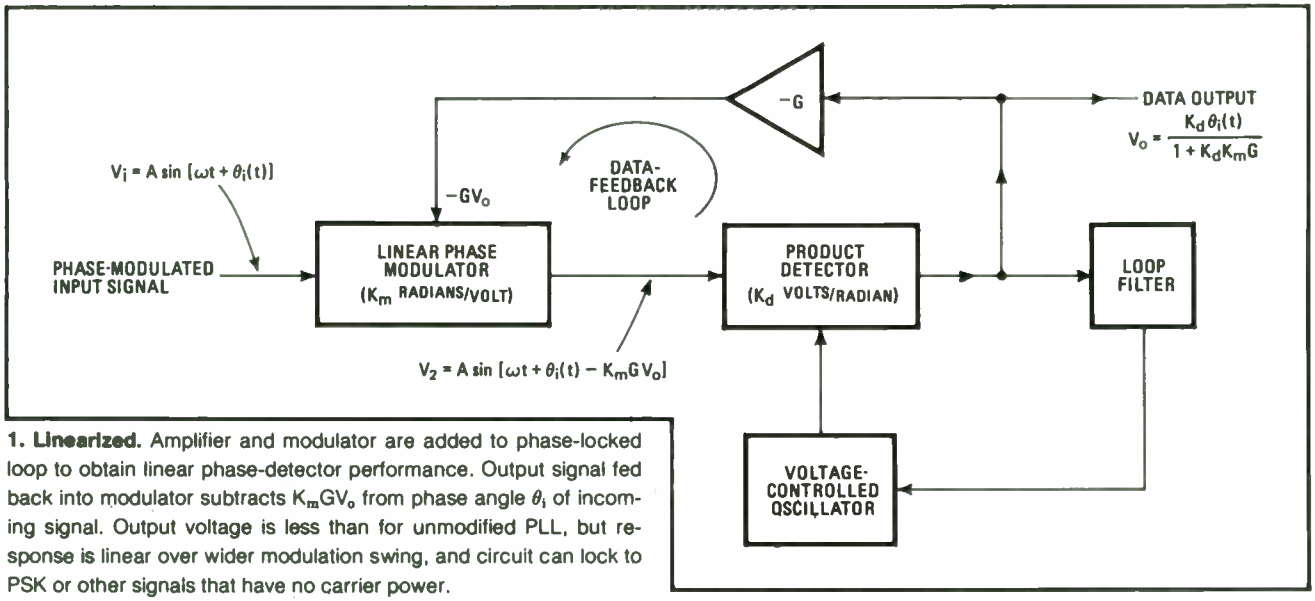
If an rf carrier is phase-modulated ±90° by a square wave, the carrier itself disappears, leaving only the modulation sidebands. This modulation technique is called phase-shift-keying. A conventional phase detector does not lock to such a signal because it has no carrier, but the circuit in Fig. 1 does lock. The amount of restored carrier power can be controlled by adjusting the gain of the feedback amplifier. This circuit can also be used to detect biphase modulation.

The compressive negative-feedback arrangement also tends to keep the product detector operating in its linear region at high modulation angles, where severe distortion would otherwise occur. The improvement in linearity is illustrated in Fig. 2, which shows the output of the phase detector when the input signal is a 2.2-gigahertz carrier modulated 160° by a triangular voltage. Without feedback, the detector distorts both the positive-going and negative-going ramps by turning them into segments of a sine wave.

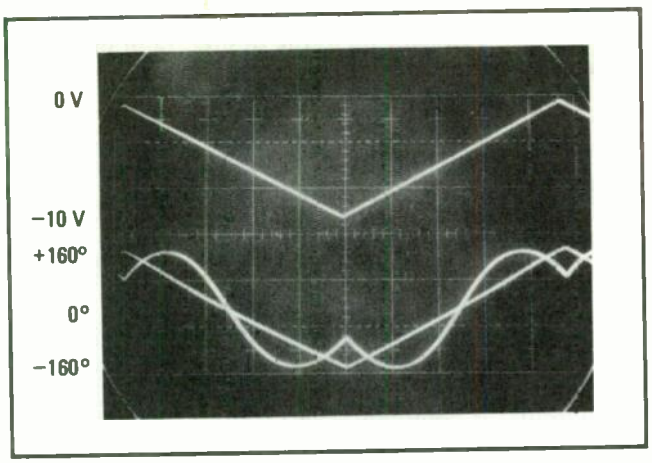
When the feedback loop is connected, however, the modulation swing is reduced, and operation in the linear region of the product detector is restored.

Another advantage of using feedback is that it increases the pull-in range of the phase-locked loop. When the loop is out of lock, the input signal is multiplied by the voltage-controlled-oscillator signal to produce a beat frequency that is fed back to the phase modulator. The beat note produces a modulation spectrum having one PM sideband that is always synchronous with the VCO frequency. This synchronous sideband results in a dc component at the output of the phase detector, which passes through the loop filter and pulls the VCO into lock. From experimental observation, the pull-in range appears to be of the same order of magnitude as the i-f bandwidth preceding the phase detector.

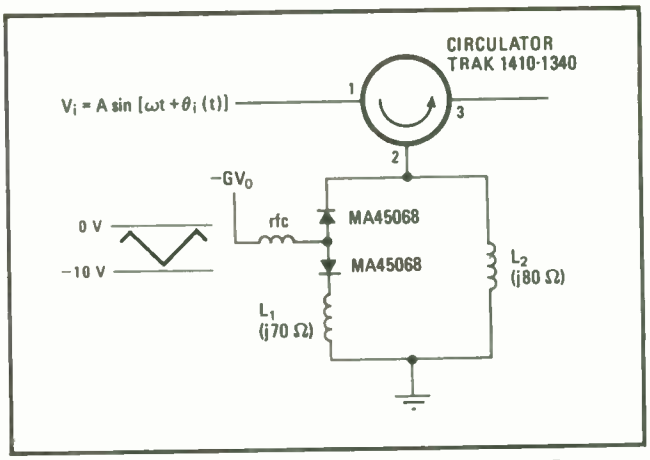
To prevent the data-feedback loop from oscillating, the open-loop gain must fall to 0 decibel before the open-loop phase shift climbs to 180°. This effect can be accomplished by using components in the loop that have wider bandwidth than needed and adding a single-pole or double-pole filter between the phase modulator and product detector to establish the over-all



1. Linearized. Amplifier and modulator are added to phase-locked loop to obtain linear phase-detector performance. Output signal fed back into modulator subtracts K_mGV_o from phase angle θ_i of incoming signal. Output voltage is less than for unmodified PLL, but response is linear over wider modulation swing, and circuit can lock to PSK or other signals that have no carrier power.



2. What you see is what you get. Effect of data-feedback loop on linearity is shown in scope photo. Top trace shows triangular voltage that modulates incoming 2.2-GHz carrier. Lower traces show detected angle without feedback (curved) and with feedback (linear).



3. Modulator. The linear phase modulator that is part of Fig. 1 can be realized at vhf and higher frequencies by use of a circulator and a variable reactance. Reflected signal in port 2 changes phase as voltage on back-to-back varactors changes.

data-loop bandwidth. If any sharp filtering is needed, it should be done ahead of the phase modulator. Then the data-loop bandwidth can be left rather wide to ensure a flat frequency response without degrading the phase-detection performance in the presence of noise.

Figure 3 shows the linear phase modulator that was used to implement the circuit for the test in Fig. 2. This modulator is useful at vhf and higher frequencies. (A similar modulator with a 3-dB hybrid in place of the circulator has been used at frequencies as low as 500 kilohertz.) The carrier enters port 1 of the circulator and travels to port 2, which is terminated in an LC combination that is voltage-tuned by two varactor diodes. Because this termination is purely reactive, all of the energy at port 2 is reflected to the rf-output port.

The angle of the reflected carrier varies with the modulating signal applied to the diodes. One modulator section of this type will produce about ±90° of linear modulation. Two sections were cascaded to produce the ±160° phase shift in Fig. 2. □

Phase-locked loop adjusts to varying signal conditions

by Charles A. Watson
E-Systems Inc., Greenville, Texas

In many phase-locked receivers, the gain of the amplifier in the phase-locked loop must be changed to adapt the loop gain to varying signal conditions. If the amplifier's gain and offset voltage are changed simultaneously, the signal-acquisition time can be shortened, and signal-to-noise ratios can be optimized.

When the entire loop, including the phase detector, operates from a single supply, the output of the phase detector must be other than zero to have the VCO rest at its midrange frequency, If not of the proper magnitude, this nonzero output offsets or even saturates the loop amplifier, driving the VCO to some non-midrange frequency.

Therefore, an offset voltge, which permits the loop to be adjusted for a midrange VCO rest frequency, is usually introduced at the loop amplifier. If the loop amplifier's gain must be changed to accommodate varying input-signal conditions, this offset voltage must also be changed to maintain the same VCO midrange frequency.

The figure contains a block diagram of a phase-locked loop (a) that includes a switched-gain amplifier, which provides offset compensation for the loop amplifier in response to remotely commanded gain adjust-

ments. The schematic (b) for this variable-gain amplifier, which only requires a quad comparator and a single transistor, is also given in the figure.

When the input logic command to the circuit is high, comparators $COMP_1$ and $COMP_2$ clamp resistors R_1 and R_2 to ground. The circuit's voltage gain can be written as:

$$A_{v(1)} = \left(\frac{R_1}{R_1+R_3}\right)\left(\frac{R_4}{R_2+R_4}\right)$$

Since $R_1 = R_2 = R_3 = R_4$, then:

$$R_4/R_2 = R_3/R_1$$

and:

$$A_{v(1)} = 1$$

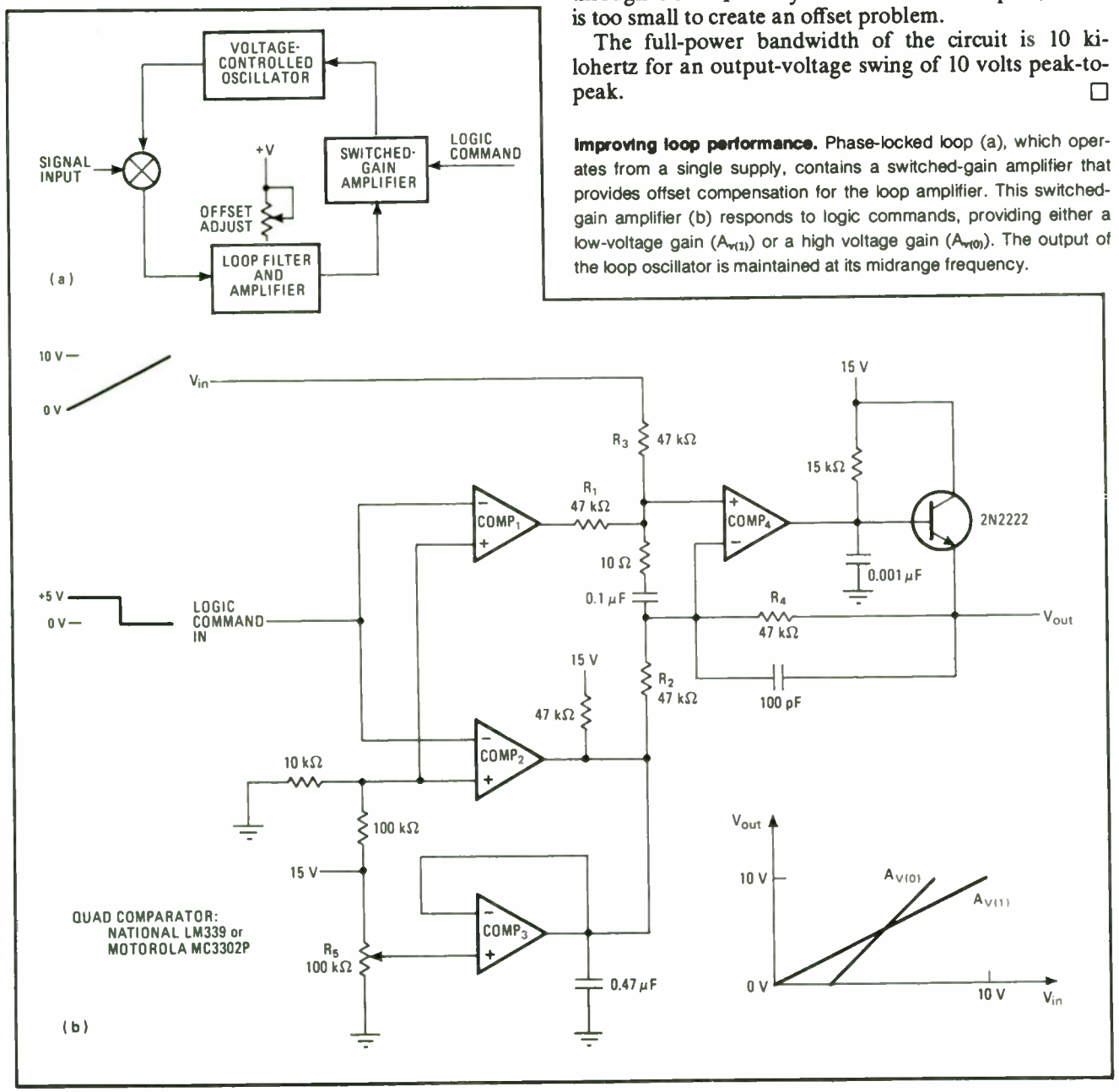
When the input-logic command to the circuit is low, comparators $COMP_1$ and $COMP_2$ unlatch so that resistor R_1 is no longer grounded and comparator $COMP_3$ performs as a voltage-follower, clamping the voltage across resistor R_2 to the desired midrange offset value. The circuit's voltage gain can now be written as:

$$A_{v(0)} = (R_2+R_4)/R_2 = 2$$

Therefore, if the relationship of $R_4/R_2 = R_3/R_1$ is maintained, the circuit's gain can be switched between $A_{v(1)} = 1$ and $A_{v(0)} = (R_2+R_4)/R_2$. Potentiometer R_5 is used to adjust the offset voltage for the circuit's high-gain mode.

Offset and drift problems are minimal with this circuit because the comparators have unusually low output-saturation characteristics (10 millivolts at 0.1 milliampere). Also, when the circuit is in its low-gain mode, the outputs of comparators $COMP_1$ and $COMP_2$ appear as common-mode (temperature-tracking) signals to output comparator $COMP_4$. Moreover, when the circuit is in its high-gain mode, the leakage current through $COMP_1$ is only around 0.1 nanoampere, which is too small to create an offset problem.

The full-power bandwidth of the circuit is 10 kilohertz for an output-voltage swing of 10 volts peak-to-peak. □



Improving loop performance. Phase-locked loop (a), which operates from a single supply, contains a switched-gain amplifier that provides offset compensation for the loop amplifier. This switched-gain amplifier (b) responds to logic commands, providing either a low-voltage gain ($A_{v(1)}$) or a high voltage gain ($A_{v(0)}$). The output of the loop oscillator is maintained at its midrange frequency.

Circumventing BCD addition in digital phase-locked loops

by Larry Martin
Hewlett-Packard Co., Palo Alto, Calif.

Many of the applications for a digital divide-by-N phase-locked loop require the locked oscillator to be offset by a fixed frequency. Usually, the first stage of the programable binary-coded-decimal divider circuit adds the input frequency to the desired offset frequency. This BCD addition, however, can be eliminated by detecting the proper number at the output of the counter divider chain.

If a receiver is tuned to 118.15 megahertz, and its intermediate-frequency stage is at 10.7 MHz, the local oscillator must then operate at 128.85 MHz. A standard divide-by-N circuit (a) adds the i-f frequency to the input frequency, takes the BCD nines complement of the sum, and then loads the result into a programable counter divider chain. Detection occurs when the counter outputs are all nines. The input number is then reloaded on the next clock pulse and the process repeats.

Let N be the input number; in this case, N = 11815 and the desired offset is 1070. The number at the outputs of the BCD adders is N + 1070, which becomes 19999 –(N + 1070) at the outputs of the complementing circuits. Therefore, the number of counts that occurs before the divider resets is the divider state that is sensed. Or, the input frequency is divided by:

19999 –[19999 –(N + 1070] = N + 1070

which can be rewritten as:

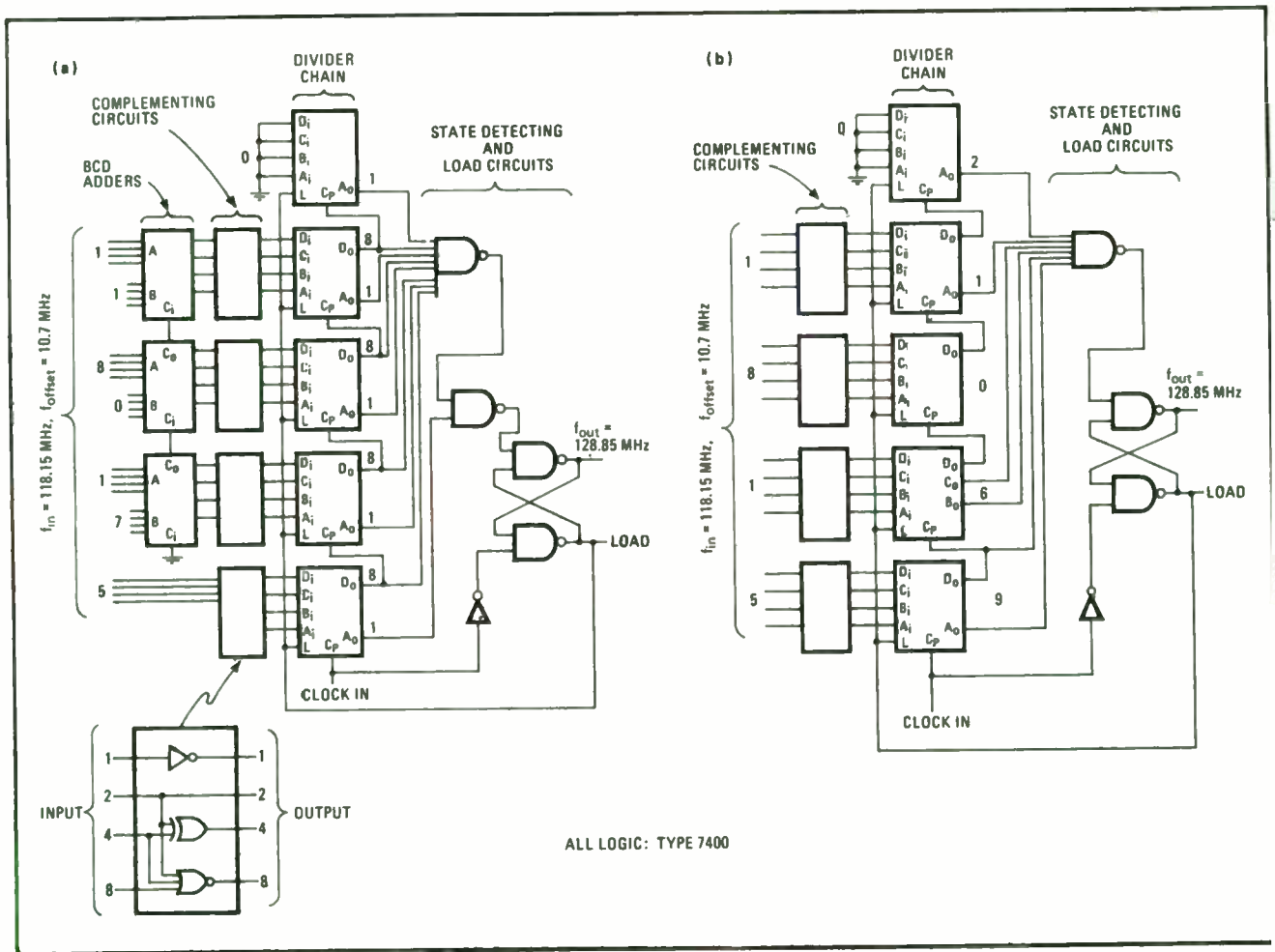
19999 + 1070 –(19999 – N) = N + 1070, or

21069 –(19999 – N) = N + 1070

By counting to 21069, instead of 19999, the proper number of counts still occurs before the divider resets. The BCD adders, then, can be removed simply by detecting a different output state of the counter, as shown in (b).

Since the divider is an up-counter, detection of the desired output state should be done when the proper outputs are ones. Because there are only six ones in 21069, as opposed to nine in 19999, one fewer output gate is needed. □

Frequency offsetting. Standard divide-by-N circuit (a) sums input frequency (118.15 MHz) with offset frequency (10.7 MHz), takes nine complement of sum, and then detects signal when counter outputs are all nines. BCD adders and one output gate can be omitted, as in (b) by detecting sum of nines complement and offset frequency (19999 + 1070 = 21069). Correct count is still reached before divider resets



Phase-locked loop includes lock indicator

by J.A. Connelly and G.E. Prescott
Georgia Institute of Technology, Atlanta, Ga.

One problem with phase-locked loops is that it's often hard to tell exactly when the loop is locked to the input signal. In many applications, it would be very useful to include a lock indicator in a phase-locked loop to display the state of the loop.

For example, in automatic test equipment, the lock indicator would afford a simple, yet efficient, way to measure the tracking and capture ranges of a phase-locked loop. Also, various low-pass filter configurations could be evaluated easily by sweeping the loop's input frequency range. A straightforward implementation for a phase-locked loop with lock indication is shown in the figure.

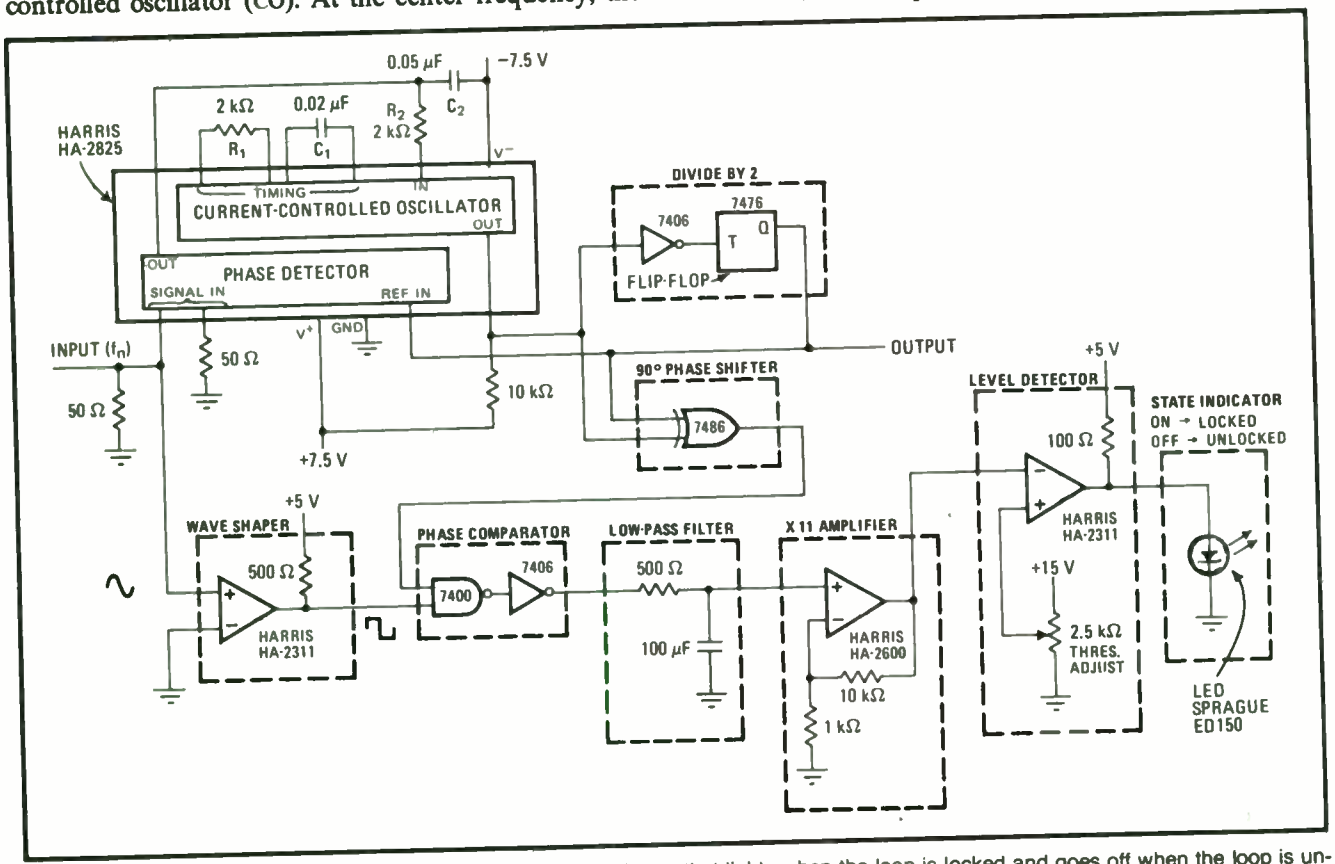
A phase-locked loop can be in its locked state over a range of input frequencies. The center frequency of this range occurs when the frequency of the input signal (f_n) is identical to the free-running frequency of the loop's controlled oscillator (CO). At the center frequency, the output of the CO will be shifted by 90° with respect to f_n. The CO frequency will track variations in f_n until the phase error of the feedback signal with respect to f_n reaches a limit set by the loop gain. For input-frequency variations beyond this limit, the loop reverts to its unlocked mode of operation, and the CO output returns to its free-running frequency.

In the circuit drawn here, the loop's feedback path is altered by breaking the normal feedback loop and inserting a divide-by-2 network. Since this network halves the CO output frequency, the CO free-running frequency must be doubled to achieve normal loop operation.

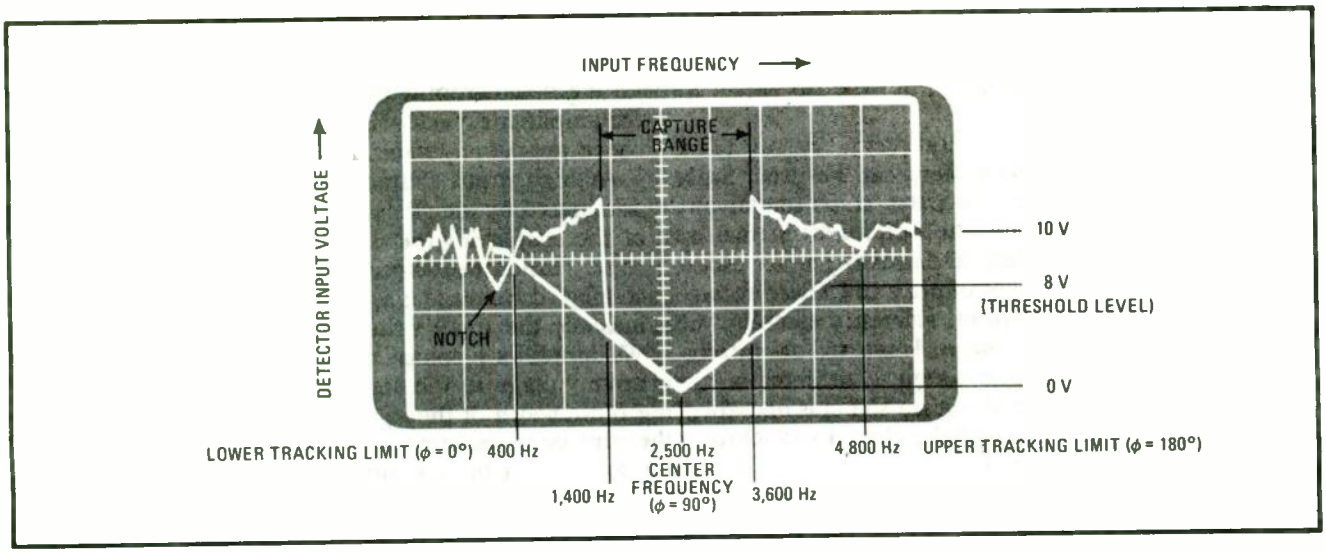
Both the output of the CO ($2f_n$) and the output of the divide-by-2 network feed a phase shifter, which produces a signal that lags the output from the divide-by-2 network by exactly 90°. The signal from the phase shifter is then compared with the input frequency, after this latter signal has been squared up by a wave shaper.

Whenever the input frequency is half the free-running frequency of the CO, the output of the CO will be shifted by 90° with respect to the input. The phase shifter introduces an additional 90° shift, causing the inputs to the phase comparator to be 180° out of phase with each other. Comparing two signals that have the same frequency but that are 180° out of phase produces a constant zero-level output.

However, if the input frequency changes, the inputs



Monitoring loop state. This phase-locked loop has an LED indicator that lights when the loop is locked and goes off when the loop is unlocked. The loop's normal feedback path is opened to accommodate the lock-indicator circuitry. And the free-running frequency of the loop's controlled oscillator must be doubled because of the divide-by-2 network. The circuit's output frequency characteristic is also shown.



to the phase comparator will no longer be exactly 180° out of phase. Instead, they will be skewed somewhat, depending on the phase error between the feedback signal and f_n. Variations in the input frequency cause a series of narrow pulses to be fed into the low-pass filter, which attenuates high frequencies and applies a dc voltage to the level detector.

As the input-frequency deviations from the free-running CO frequency become larger, the phase comparator and low-pass filter produce correspondingly larger dc voltages for the level detector. For a locked loop, the output of the level detector is high, and the LED lock indicator is turned on. When the loop is unlocked, the detector's output goes low, turning off the LED.

For the components shown here, resistor R_1 and capacitor C_1 set the CO free-running frequency at 5,000 hertz, making the input center frequency equal to 2,500 Hz. Resistor R_2 and capacitor C_2 serve as the conventional low-pass filter for the loop. The loop's capture range can be expressed as:

$$\textit{capture range} = \pm(8\pi^2)/[2\pi C_2(R_2+R_{in})]^{1/2}\ Hz$$

where R_{in} is the CO input impedance, which is approximately 500 ohms for the part used here.

The actual output frequency characteristic of the entire loop is also shown in the figure. This waveform is obtained by slowly sweeping the loop's input-frequency range, while monitoring the input voltage to the loop's level detector. The minimum voltage is developed when the loop is locked—the input frequency and the CO output are 90° out of phase. Any input-frequency deviation from this null point will result in a positive dc voltage. The steep edges within the V portion of the characteristic define the capture range of the loop. These abrupt transitions are created as the loop suddenly enters the locked mode from the unlocked condition.

When the input and CO output signals are either 0° or 180° out of phase, the inputs to the phase comparator will be in phase, and the voltage to the detector will be at its maximum level. At this point, the loop becomes unlocked, and the CO and input frequencies are no longer related. The notch appearing at the left end of the V trough is caused by beat frequencies that occur as the loop attempts to capture the input signal. For proper circuit operation over a wide frequency range, the threshold voltage of the level detector should be set lower than the minimum amplitude of this notch.

Through the threshold adjustment, the reference voltage for the level detector can be set as close as is practical to the maximum input detector voltage, without tripping the detector for the unlocked condition. When the input detector voltage drops below this reference level, the output from the detector goes high, lighting the LED to indicate that the loop is locked. In this circuit, the reference voltage is set at approximately 8 V.

If a bank of switchable active filters is used as the loop's normal filter, the lock indicator can serve as a control circuit for changing the tracking and capture ranges of the loop automatically. It does this by switching the loop filter upon loss of track. □

Logic gates and LED indicate phase lock

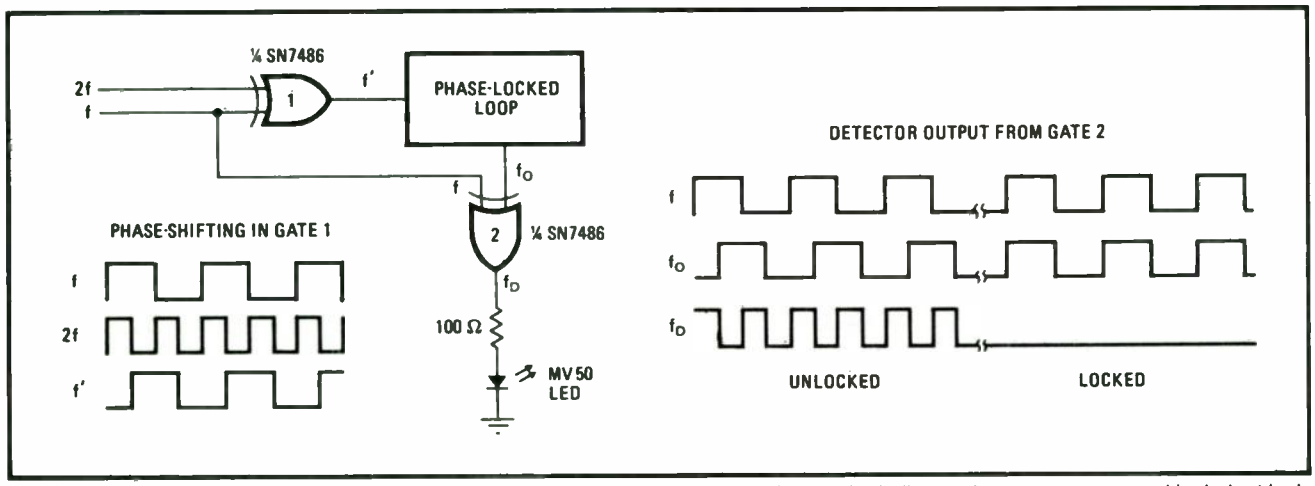
by R. P. Leck
Bell Laboratories, Crawford Hill, Holmdel, N.J.

Phase-locked loops are widely used for signal processing and digital applications such as fm demodulation, tone-decoding, and clock synchronization. If the error signal is accessible, signal acquisition and locking in the PLL can be observed from decrease of error voltage to zero. For integrated-circuit PLLs without an error-signal terminal, however, acquisition and lock can be indicated by two exclusive-OR gates and a light-emitting diode. The LED glows brightly when the input signal is first applied, then dims as the loop signal pulls into synchronism, and it goes out when the loop locks.

If the locked signal from the loop were in phase with the input to the loop, a single exclusive-OR gate would suffice for the indicator. In fact, however, the locked signal lags the input by 90°, so a second gate is needed to introduce an extra quadrature shift on either the input or output signal. As shown in the figure, the phase is shifted by applying frequencies f and 2f to an exclusive-OR gate. In the circuit shown here, the extra 90° is added to the locking signal before it goes into the loop; this procedure is convenient when f is generated by counting down from a master oscillator, because 2f is readily available.

From the square waves at f and 2f, gate 1 develops the 90°-shifted signal f′ that is the input to the loop-phase detector. Gate 2 functions as an auxiliary phase detector, comparing the phase between the loop output, f_O, and the non-phase-shifted input f. The output from gate 2, f_D, drives the light-emitting diode that indicates acquisition and lock.

When the loop is locked and its natural frequency is close to f, the inputs to the detector coincide. The resulting pulse width of the signal present at its output is either tiny or nonexistent, so the LED is turned off. When the loop is out of lock and its natural frequency is far from f, maximum output pulse width is obtained and the LED is turned on at its maximum brightness. As the loop acquires lock, the output-pulse width decreases, decreasing the brightness of the LED. □



Loop monitor. Phase-locked loop has LED monitor that glows brightly when loop is unlocked, dims as loop nears sync, and is dark at lock. Output from loop lags input by 90°; therefore, to permit comparison of output with locking signal, signal is shifted 90° before entering loop.

Analog multiplier/divider simplifies frequency locking

by Moise Hamaoui
Fairchild Semiconductor, Mountain View, Calif.

In phase-locked loops, servo systems, and TV receivers, it is often necessary to lock two different frequencies together. The conventional method is quite cumbersome. First the higher of the two frequencies is divided down to a value close to that of the lower frequency. Then a signal that is proportional to the difference between the stepped-down frequency and the low frequency is generated. Lastly, this signal is used to adjust the high frequency so that it is locked to the low frequency.

The analog multipler/divider shown, however, locks the two frequencies in one step. The block diagram illustrates how the circuit accepts pulses of frequency f_{in} and generates pulses at frequency $f_{out} = Mf_{in}$, where M is a constant determined by the designer.

Dc voltages V_1 and V_2 are proportional to the two frequencies to be locked together:

$V_1 = K_1 f_{in}$

$V_2 = K_2 f_{out}$

The output voltage is the difference between these two:

$V_{out} = A(V_1 - V_2) = A(K_1 f_{in} - K_2 f_{out})$

where A is the gain of the differential amplifier. The output frequency is given by:

$f_{out} = KV_{out} = KA(K_1 f_{in} - K_2 f_{out})$

which can be rewritten as:

$(K_1 f_{in} - K_2 f_{out})/f_{out} = 1/KA$

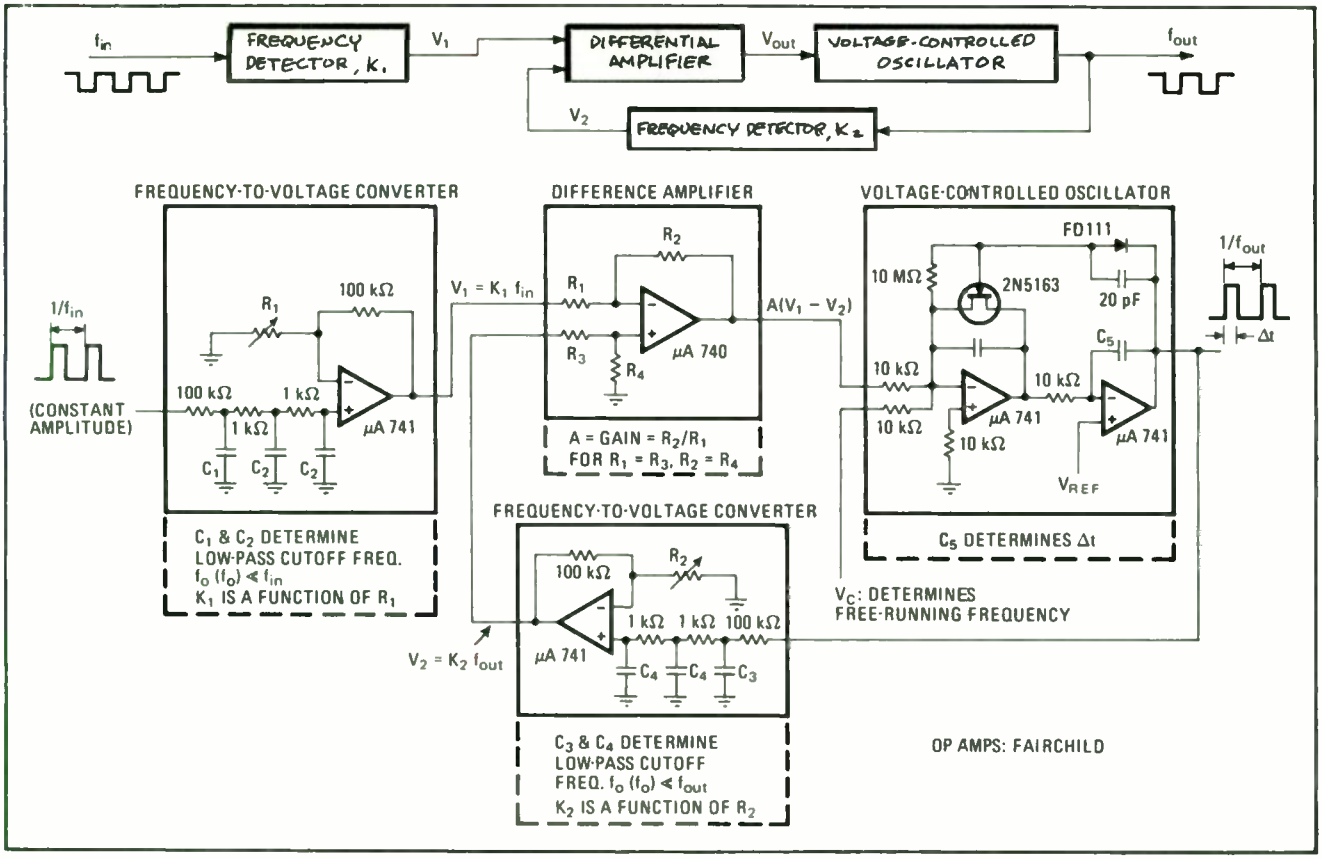
As amplifier gain A becomes very large:

$K_1 f_{in} - K_2 f_{out} \approx 0$

Solving for f_{out} yields:

$f_{out} = (K_1/K_2) f_{in} = M f_{in}$

By varying K_1 and K_2, then, the input frequency can be multiplied or divided by any factor. For the hardware implementation shown, either f_{in} or f_{out} may range from 30 hertz to 10 kilohertz. □



Step saver. In single operation, analog multiplier/divider locks two different frequencies together. Differential amplifier accepts voltages V_1 and V_2, which are proportional to the frequencies to be locked. Varying the constants, K_1 and K_2, multiplies or divides the frequencies.

37. Phase shifters

Outputs of op-amp networks have fixed phase difference

by Richard K. Dickey
California Polytechnic State University, San Luis Obispo, Calif.

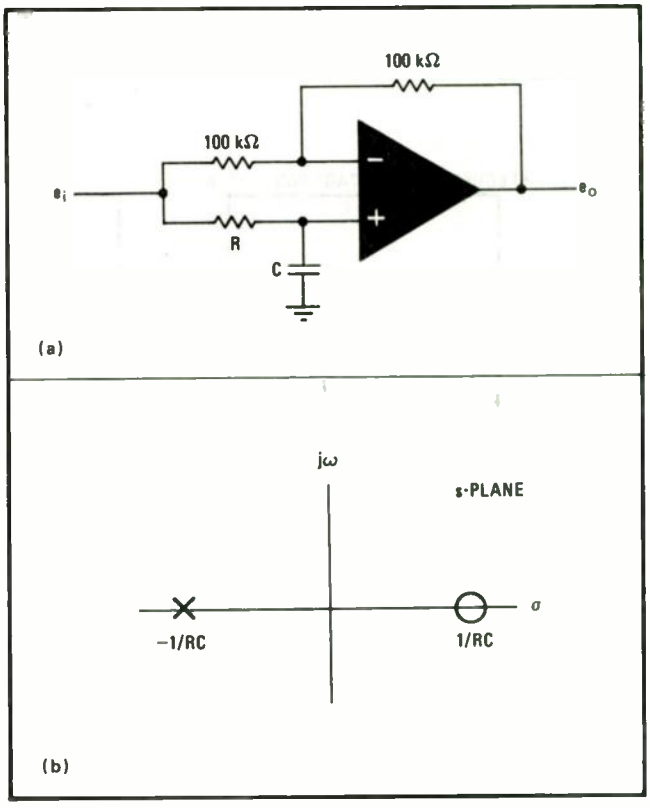
In the phasing method of single-sideband generation, two modulating signals are derived from the audio input. The two signals must have equal amplitudes, but must differ in phase by 90° at all frequencies in the audio band. A differential-phase-shift system that provides these two signals can be made from resistors, capacitors, and operational amplifiers.

The basic section of the constant-phase-shift system is the op-amp circuit shown in Fig. 1. The transfer function of this circuit is

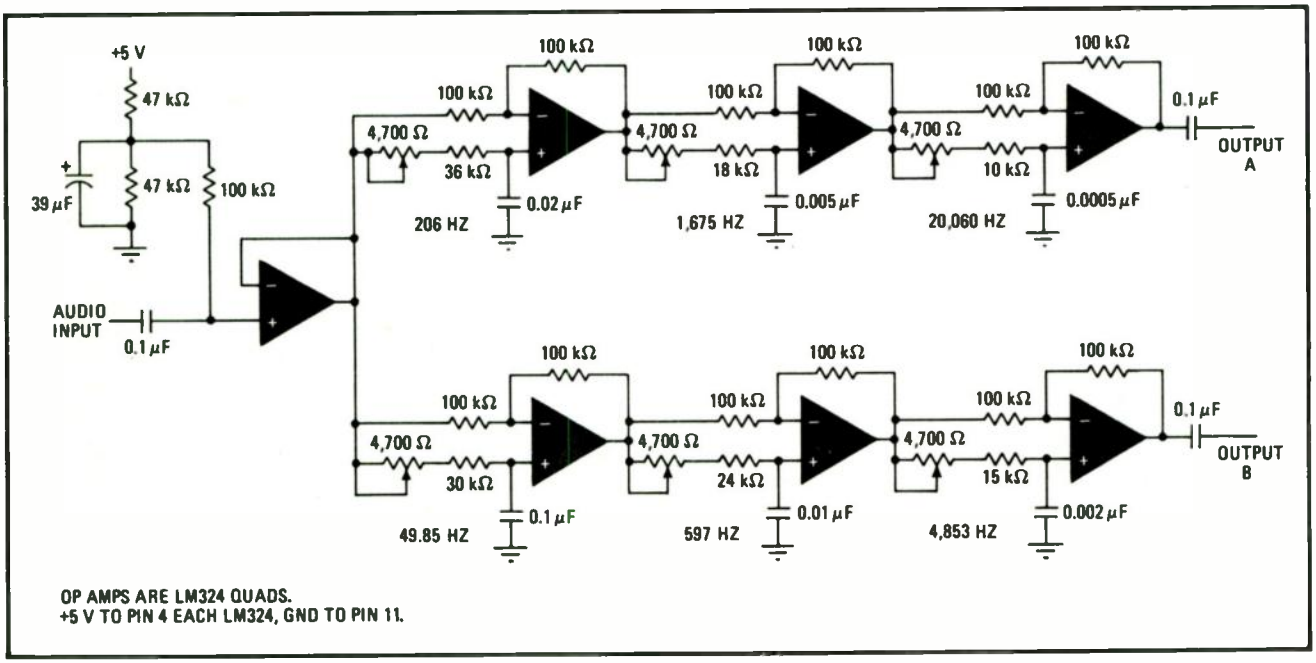
$$e_o/e_i = (1 - j\omega RC)/(1 + j\omega RC)$$
$$= 1 \angle -2 \arctan \omega RC$$

Thus the gain is always unity, and the phase shift decreases from 0 to −180° as frequency increases from zero to infinity. The shape of the phase-shift curve depends upon the time constant RC, i.e., upon the locations of the singularities in the s-plane plot that is included in Fig. 1.

If three of these basic sections are cascaded, the over-all gain remains constant at unity, and the over-all phase shift through the network falls from 0 to −540° at



1. Basic section. Op amp connected as shown (a) is a unity-gain phase shifter. Singularities of circuit are shown (b) in s-plane plot. Phase shift ranges from 0 at dc to −180° at infinite frequency; however, gain is unity at all frequencies.



2. Quadrature. Differential phase shifter converts audio-frequency input signal to two outputs, 90° out of phase, for SSB modulation. Simple transformerless circuit uses quad op amps driven by a single-ended 5-volt supply. The individual sections are adjusted for 90° phase shift at the frequencies indicated on the figure; the two outputs are then in quadrature to within 2° from 100 Hz to 10 kHz.

a rate that is determined by the three RC products.

Two such phase-shift networks, fed from a common input (as shown in Fig. 2), can be designed so that the phase shift through one lags behind the phase shift through the other by 90° over a substantial frequency range. The time constants are chosen so that the singularities of the two networks interlace.

The all-pass system in Fig. 2 provides two equal-amplitude outputs that differ in phase by (90 ± 2)° over the frequency interval from 100 hertz to 10 kilohertz. The various R and C values were calculated from the table published by S.D. Bedrosion, "Normalized Design of 90 Degree Phase Difference Networks," IRE Transactions on Circuit Theory, June 1960, pp. 128–136. In each section, RC = $\frac{1}{2\pi f}$, where f is the 90° frequency for that section as shown in Fig. 2. An exception is the 20,060-Hz stage, where R was decreased to compensate for the inherent phase shift in the op amp.

Each section of each network should be individually adjusted to an exactly 90° phase shift at the indicated frequency. This adjustment can be made by connecting the input and output of that section to the horizontal and vertical inputs of an oscilloscope, and then varying the 4,700-ohm potentiometer until the Lissajous figure is a circle. Alternatively, a phasemeter can be used.

Each op amp is one quarter of an LM324 quad amplifier. The input biasing network allows operation from a single 5-volt supply. □

All-digital phase shifter handles 5-to-1 bandwidth

by Aleardo Salina
Siai Marchetti, Vergiate, Italy

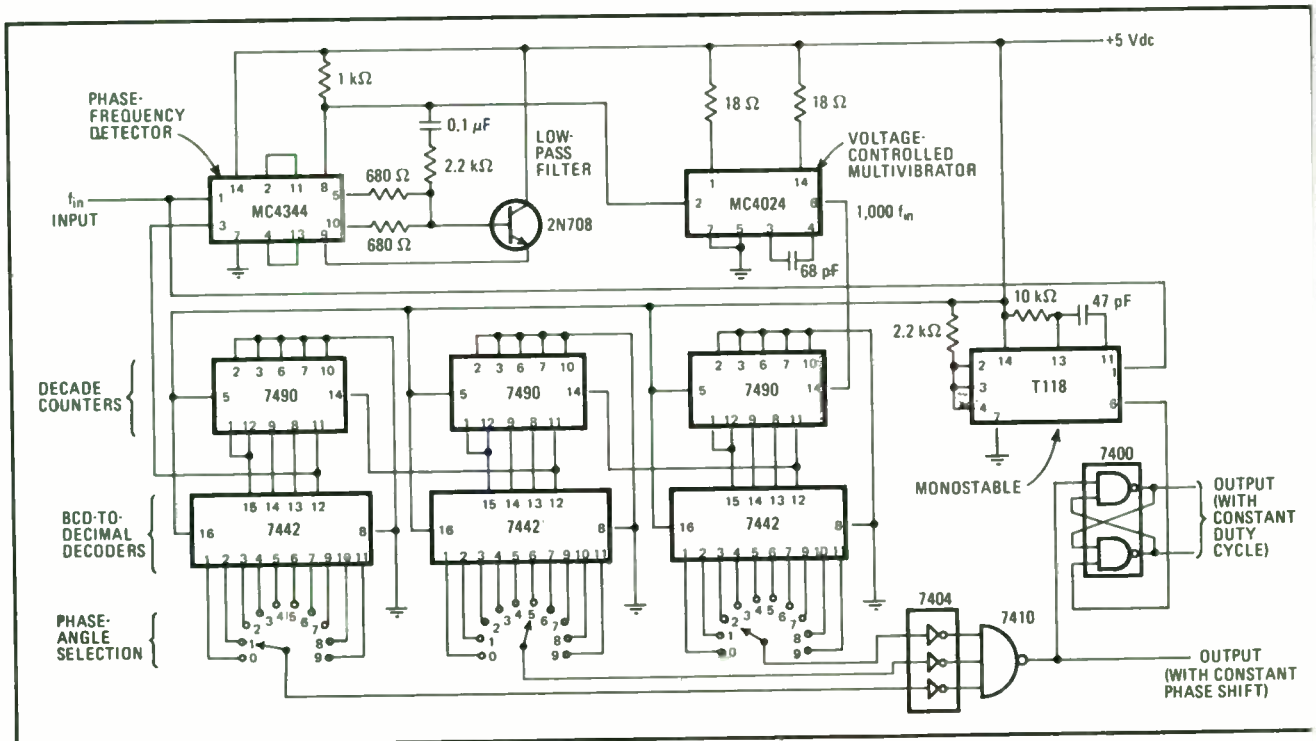
A digitally programable phase-shift network can be made to maintain the phase shift at its output constant, even though the frequency at its input varies by as much as a factor of five. The circuit consists mainly of digital ICs, including its input-detector stage.

The desired phase shift is switch-selectable through a three-stage counter/decoder network. Any phase shift between 0° and 360° can be chosen. Here, the angle selected is divided into 1,000 bits, but a finer resolution can be obtained by increasing the number of decade counters.

For the component values indicated, the circuit's phase angle stays locked for input frequencies from 2 to 10 kilohertz. This operating frequency range can be shifted by changing the values of the low-pass filter components and the value of the timing capacitor for the voltage-controlled multivibrator.

The circuit also produces an output whose duty cycle remains constant. □

Locking phase digitally. Circuit produces the phase shift (between 0° and 360°) selected by the three switches. This digitally programed phase angle does not change, although the input-signal frequency may vary from 2 to 10 kilohertz. The circuit's operating frequency can be changed by adjusting the low-pass filter and the timing of the voltage-controlled multivibrator. There is also a constant-duty-cycle output.



Frequency doubler and flip-flop make adjustable phase shifter

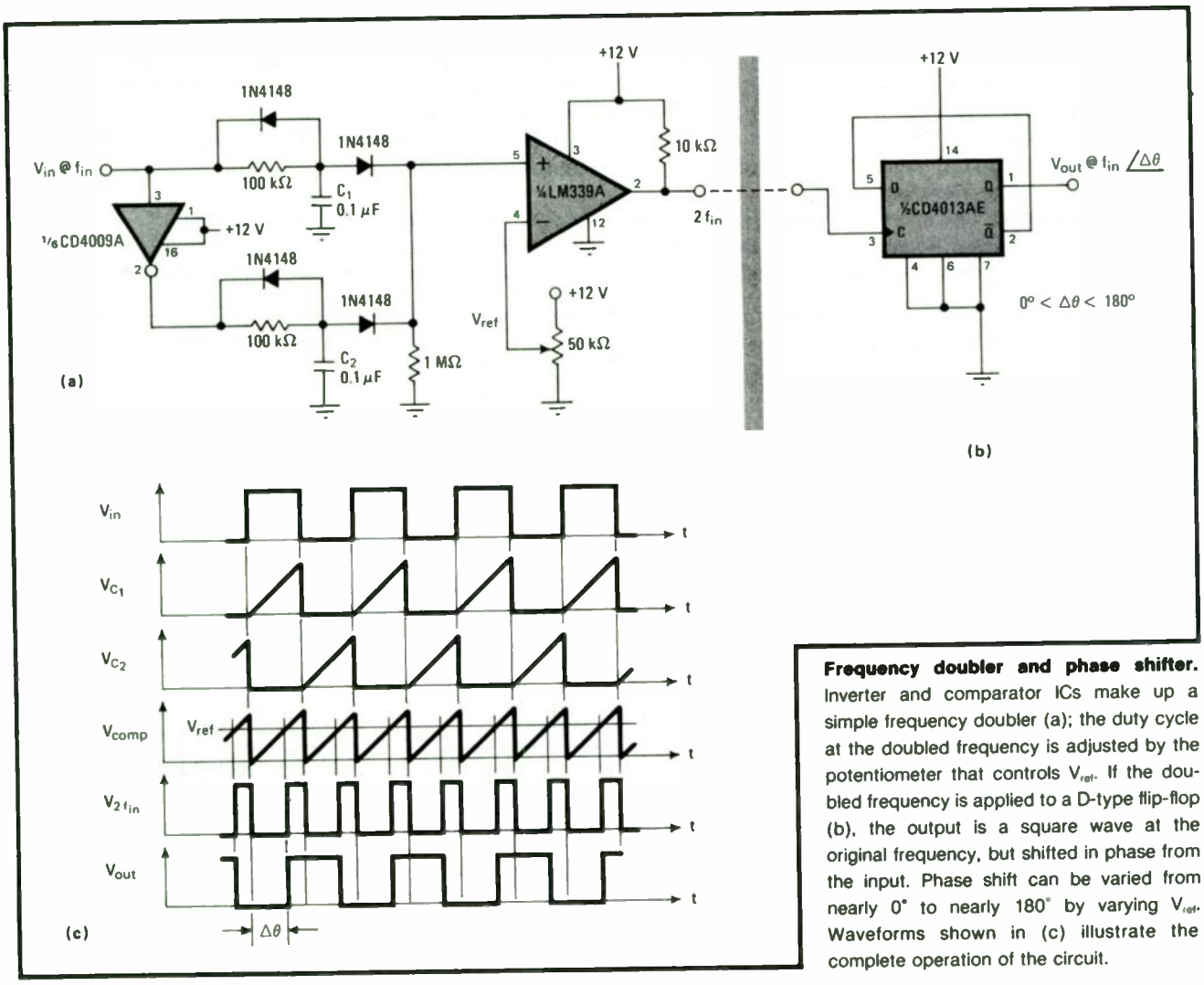
by Vladimir Brunstein
Nova Electric Mfg. Co., Nutley, N.J.

A frequency doubler for operation at the voltage levels of either complementary-MOS or transistor-transistor logic can be built with an inverter and a comparator. And if the doubled signal is then fed into a flip-flop, the output has the original input frequency, shifted in phase by an amount that depends on the reference voltage applied to the comparator. This shifter has been used to adjust the phase of the output from a phase-locked-loop device.

In the doubler circuit (a), the rectangular input signal and its inverted form are applied to capacitors C_1 and C_2. Their triangular ramps, which are 180° out of phase, are added through diodes to produce a sawtooth wave at twice the input frequency. This sawtooth is applied to the noninverting input of the comparator, producing a output at $2f_{in}$ with a duty factor that depends on the setting of the reference voltage at the inverting input.

Adding an edge-triggered D-type flip-flop to the circuit (b) yields an output signal of frequency f_{in}, phase-shifted with respect to the input signal. Varying the reference voltage V_{ref}, the phase shift between the output and the input signal can be set at any value between 0° and 180°. However, the duty factor of the output is always 50%. The frequency limit is set by the frequency band of the comparator used.

The component values shown were used for 60-hertz operation in a circuit that phase-locks the output of an uninterruptable power supply to the ac line. Connecting the output of the power supply back into the line provides a load that is inductive or capacitive, depending on the phase shift that is set by the reference-voltage potentiometer. □



Frequency doubler and phase shifter. Inverter and comparator ICs make up a simple frequency doubler (a); the duty cycle at the doubled frequency is adjusted by the potentiometer that controls V_{ref}. If the doubled frequency is applied to a D-type flip-flop (b), the output is a square wave at the original frequency, but shifted in phase from the input. Phase shift can be varied from nearly 0° to nearly 180° by varying V_{ref}. Waveforms shown in (c) illustrate the complete operation of the circuit.

38. Potentiometer circuits

Linear pot and op amp provide tapered audio volume control

by Robert C. Moore
Applied Physics Laboratory, Johns Hopkins University, Silver Spring, Md.

Tapered potentiometers are used in audio amplifiers to compensate for the nonlinear response of the human ear. However, at a lower cost, a linear potentiometer and an operational amplifier can approximate the response of the tapered pot.

The audio taper for potentiometers is described by the gain function

$$V_{out}/V_{in} = f(\alpha) = 10^{2(\alpha-1)}$$

where the potentiometer displacement α can range from $\alpha = 0$ (in the full counter-clockwise position) to $\alpha = 1$ (in the full clockwise position). Signal attenuation through the potentiometer can be expressed in decibels as

$$Attenuation = 20\log(V_{in}/V_{out}) = 40(1-\alpha)\ dB$$

This expression shows that the attenuation in decibels is proportional to the potentiometer displacement from the full clockwise position. To obtain this reverse-logarithmic-gain function, special nonlinear potentiometers are usually used.

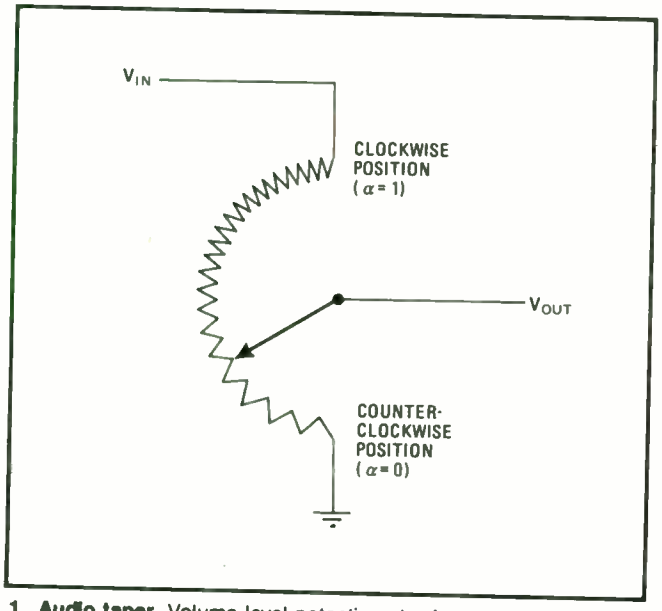
Because these potentiometers cannot be loaded heavily without distorting the gain function, in practical audio applications they are usually followed by a gain stage or a high-input-impedance voltage follower. However, the reverse-logarithmic-gain function can be closely approximated by using a linear potentiometer, a single operational amplifier, and one fixed resistor, as shown in Fig. 2. The operational amplifier adds the capability of voltage gain; in this circuit the maximum voltage gain is 8, or 18 dB. The voltage-transfer function for the circuit of Fig. 2 is

$$V_{out}/V_{in} = (-8\alpha)/(9-8\alpha)$$

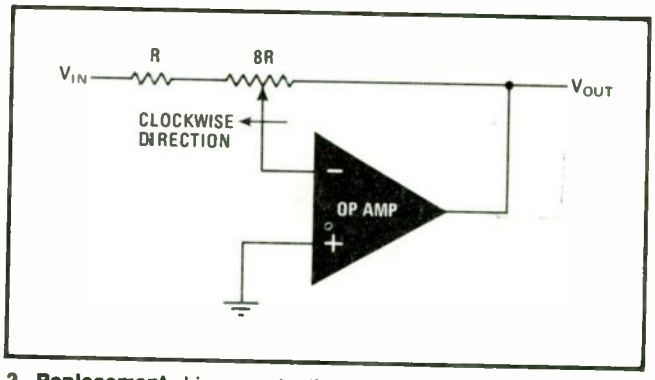
which closely approximates the attenuation function

$$Attenuation = 40(1-\alpha) - 18\ dB$$

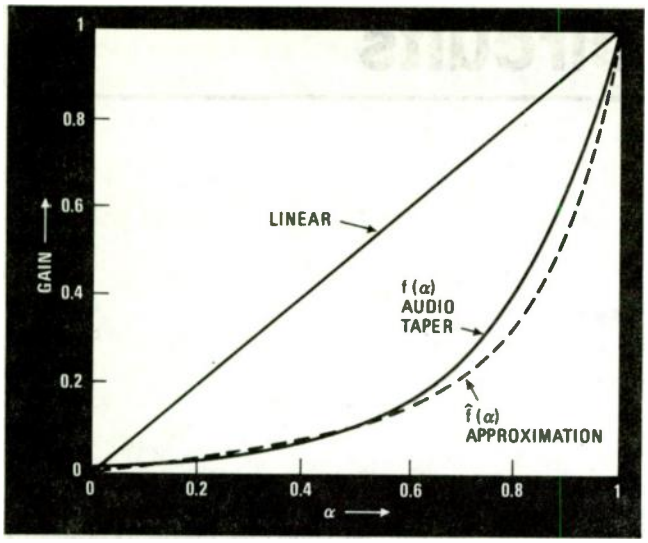
over most of the range of α. As a desirable advantage,



1. Audio taper. Volume-level potentiometer for sound systems has tapered resistivity to compensate for exponential response of human ear. Expensive tapered pot (which should be followed by a buffer stage to prevent loading effects) can be replaced by a linear pot, fixed resistor, and op amp.



2. Replacement. Linear potentiometer, fixed resistor, and operational amplifier, connected as an inverting amplifier, provide transfer function that approximates performance of audio-taper pot plus 18 dB of gain. The minimum input impedance is R.



3. Comparison. Approximation to audio taper is excellent for potentiometer-displacement values α below 0.5 and good everywhere else. The approximation is exact at $\alpha = 0.5$.

the attenuation goes to infinity at $\alpha = 0$.

The transfer function of the circuit in Fig. 2 is normalized to

$$\hat{f}(\alpha) = \alpha/(9 - 8\alpha)$$

and compared to the true audio taper in Fig. 3. The approximation, which is good everywhere, is especially close at the low values of α, where compensation for the reduced hearing sensitivity at low sound levels is most important. The two functions agree exactly at $\alpha = 0.5$.

Because it uses a linear potentiometer, this circuit is less expensive than the normal audio-taper level-control, and it is much more convenient to use in new designs.

The value of R can easily be chosen to suit the op-amp and the circuit impedance; for example, a 100-kΩ pot and a 12.4-kΩ fixed resistor can be combined with a 741 op amp. □

Series resistance improves potentiometer linearity

by Harry H. Schwartz
Electrodesign Ltd., Ville Lasalle, Quebec, Canada

Adding a series resistance to one end of a loaded linear potentiometer can reduce loading error by a factor of five or more. The price for this gain in linearity is a voltage loss across the pot. But losses in amplification or drive in the order of 3 to 4 decibels can usually be tolerated in view of the marked improvement in linearity.

As shown in (a), voltage E_i is applied to potentiometer R_p and series resistor R_s. The load resistor is R_m, the output voltage is E_o, and θ is the per-unit variation of the pot wiper. Letting:

$Y_\theta = E_o/E_i$, $P_m = R_m/R_p$, and $P_s = R_s/R_p$

the voltage transfer function can be expressed as:

$$Y_\theta = \theta P_m/(P_m P_s + P_m + \theta P_s + \theta - \theta^2)$$

If $Y_0 = Y_\theta$ when $\theta = 0$ and $Y_1 = Y_\theta$ when $\theta = 1$, then output impedance ratio Z_o is:

$$Z_o = Y_\theta/Y_1 = \theta/[1 - (1-\theta)(P_s - \theta)/(P_m + P_s + P_m P_s)]$$

For three points of this equation, the values of Z_o and are the same; or, since there is no linearity error, the $Z_o = \theta$. These points occur at $\theta = 0$, $\theta = 1$, and $\theta = P_s$

The well-known curve (b) for a loaded potentiomete can be written in terms of θ and P_m:

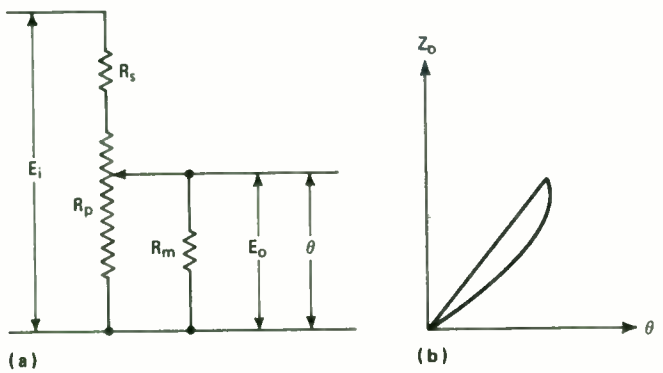
$$Z_o = \theta/[1 + \theta(1-\theta)/P_m]$$

When the load resistance is very high, P_m approache infinity, and the pot output is the straight black line. Fo finite values of P_m, the nonlinear colored curve is ob tained. As P_m becomes smaller, linearity error grows.

A short computer program (c) that solves the genera equation for impedance ratio Z_o can be used to dete mine the effect of series resistance ratio P_s for variou values of load resistance ratio P_m. Generally, the large the magnitude of P_s, the greater is the error reductio The program varies P_s from 0 to 2 in steps of 0.1 and from 0 to 1 in steps of 0.05 for P_m values of 1, 2, 5, 1 20, and 50.

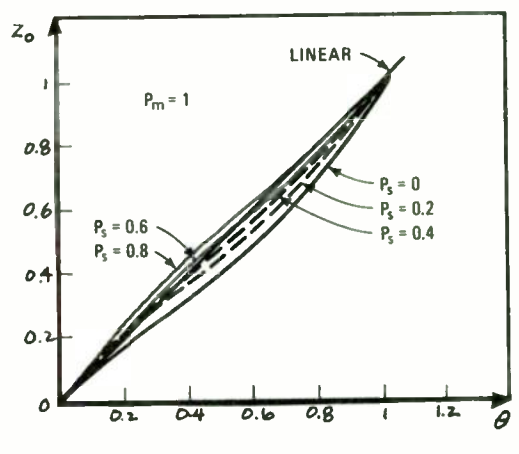
The plot of (d) shows that output linearity for P_m = is improved by a factor of five when P_s is increase from 0 to 0.6. In (e), linearity error is plotted against for $P_m = 5$ and $P_m = 10$ for P_s values between 0 ar 0.6. Again, linearity is greatly improved. Values of should be held to 0.5 or less so that the series volta loss is tolerable.

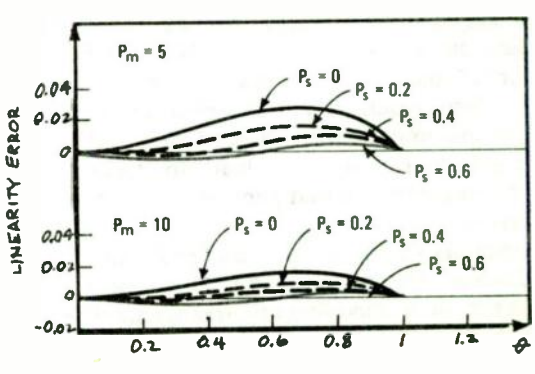
Reducing loading effects. Output of loaded potentiometer (a) becomes nonlinear, as shown by graph (b), with smaller load resistance rati ($P_m = R_m/R_p$). Increasing series resistance ratio ($P_s = R_s/R_p$) decreases loading error and improves linearity. Computer program (c) finc output impedance ratio Z_o for several values of P_m, P_s, and wiper position θ. Graphs (d) and (e) show effect of P_s on Z_o and linearity error.




```
READY
PLIST
10      DATA 1, 2, 5, 10, 20, 50
30      READ P1
40      FOR P2=0 TO 2 STEP .1
45      PRINT " PM="P1," PS="P2
46      PRINT
47      PRINT " A","Z"
48      PRINT
50      FOR A=0 TO 1 STEP 5.00000E-02
60      LET Z=A/(1-((1-A)*(P2-A))/(P1 + P2 + P1 * P2))
70      PRINT A, Z
80      NEXT A
85      PRINT
86      PRINT
90      NEXT P2
95      PRINT
96      PRINT
100     GOTO 30
110     END
READY
RUN
```

(c)





39. Power supplies

Voltage doublers power microprocessor PROMs

by Andrew Longacre Jr.
University of New Orleans, New Orleans, La.

When a single-voltage microprocessor system is augmented with some extra components that operate at different voltages, the power-supply requirements can be conveniently met by adding doubler circuits to a full-wave bridge rectifier. These extra supplies are enough to power memory or peripheral elements that do not operate at the standard single-supply system voltage.

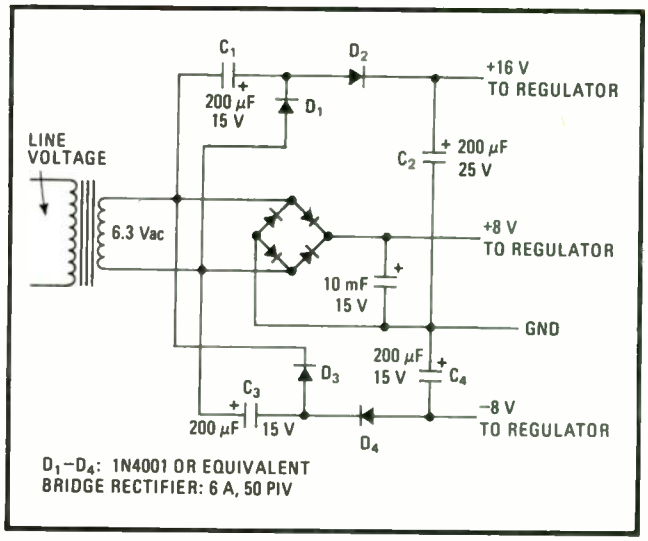
For example, Motorola's M6800 microprocessor family is designed to run from a single supply of +5 volts, the same voltage required by the transistor-transistor logic that is often used in peripheral and support functions. The M6800 family lacks, however, any sort of programable read-only memory or that designer's friend, the erasable PROM, and unfortunately, the familiar versions of these memory devices require additional supply voltages at +12 v and/or −5 v. A terminal interface conforming to the RS-232C standard, if desired, also requires a supply at −5 v.

A typical M6800 development system therefore may involve implementation of unbalanced power supply requirements like:

+5 v at 2.5 A
+12v at 50 mA
−5 v at 50 mA

These requirements can all be met from a single 6.3-v/3-A filament transformer by amending the conventional full-wave bridge configuration with two voltage-doubling circuits, as shown in the figure. A low-voltage prepackaged diode bridge carries the bulk of the rectified current in charging a 10,000-microfarad capacitor to about 8 v (9 v peak) for regulation down to +5 v. Two capacitors and two diodes form each of two voltage-doubling circuits—a positive one that generates about +16 v (18 v under no load) for regulation to +12 v, and a negative one that generates just about −8 v for regulation to −5v.

Capacitors C_1 and C_2, plus diodes D_1 and D_2, make up the doubler that provides +16 v across C_2. They are connected in a diode-pump arrangement; C_1 charges through D_1 to 8 v when the bottom of the transformer secondary is positive, and C_2 adds this voltage to that of the secondary during the next half cycle as C_2 charges through D_2 and one bridge rectifier.



Add-on sources. Voltage-doubler circuits, added to full-wave bridge rectifier, provide extra positive and negative voltage supplies. Bridge provides over 2.5 A at +8 V to drive a regulator IC for +5-V output. Upper doubler delivers 50 mA at +16 V for regulation to +12 V, and lower doubler delivers 50 mA at −8 V for regulation to −5 V. The extra sources meet the voltage and current requirements of microprocessor peripherals that cannot use the +5-V source.

Similarly, capacitors C_3 and C_4, together with diodes D_3 and D_4, constitute the extra elements that provide −8 v relative to ground. Capacitor C_3 charges to 8 v through diode D_3 when the bottom of the secondary is positive. When the top of the secondary is positive, C_3 charges capacitor C_4 through D_4 and one of the bridge rectifiers.

Necessary regulation is added to the circuit by use of three-terminal integrated-circuit regulators (not shown in the circuit diagram). An LM342H-12 driven by +16 v provides the regulated +12-v output. An LM323K (or three LM309Ks driving separate parts of the load circuit), connected to the +8 v, provides the regulated +5 v, and an LM320H-5.0 connected to the −8 v provides the regulated −5-v output.

With the components shown in the figure, each of the required voltages is provided at the desired current level. Where requirements vary, either of the voltage doublers can be modified to provide more current simply by scaling upward both of its capacitors; however, one would not retain this fundamentally unbalanced configuration where the current requirements at the three voltages approach equality. □

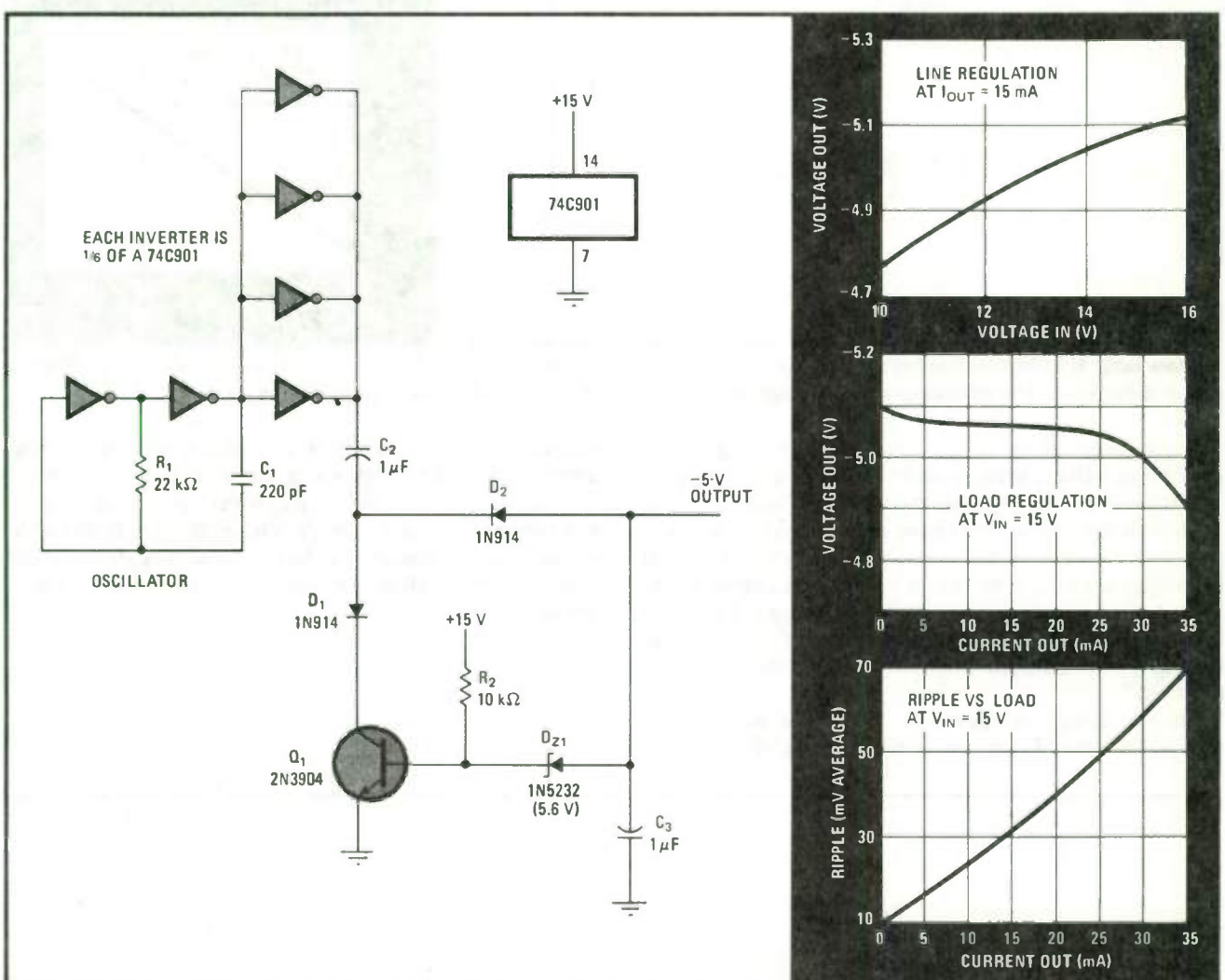
Inverting dc-to-dc converters require no inductors

by Craig Scott and R.M. Stitt
Burr-Brown Research Corp., Tucson, Ariz.

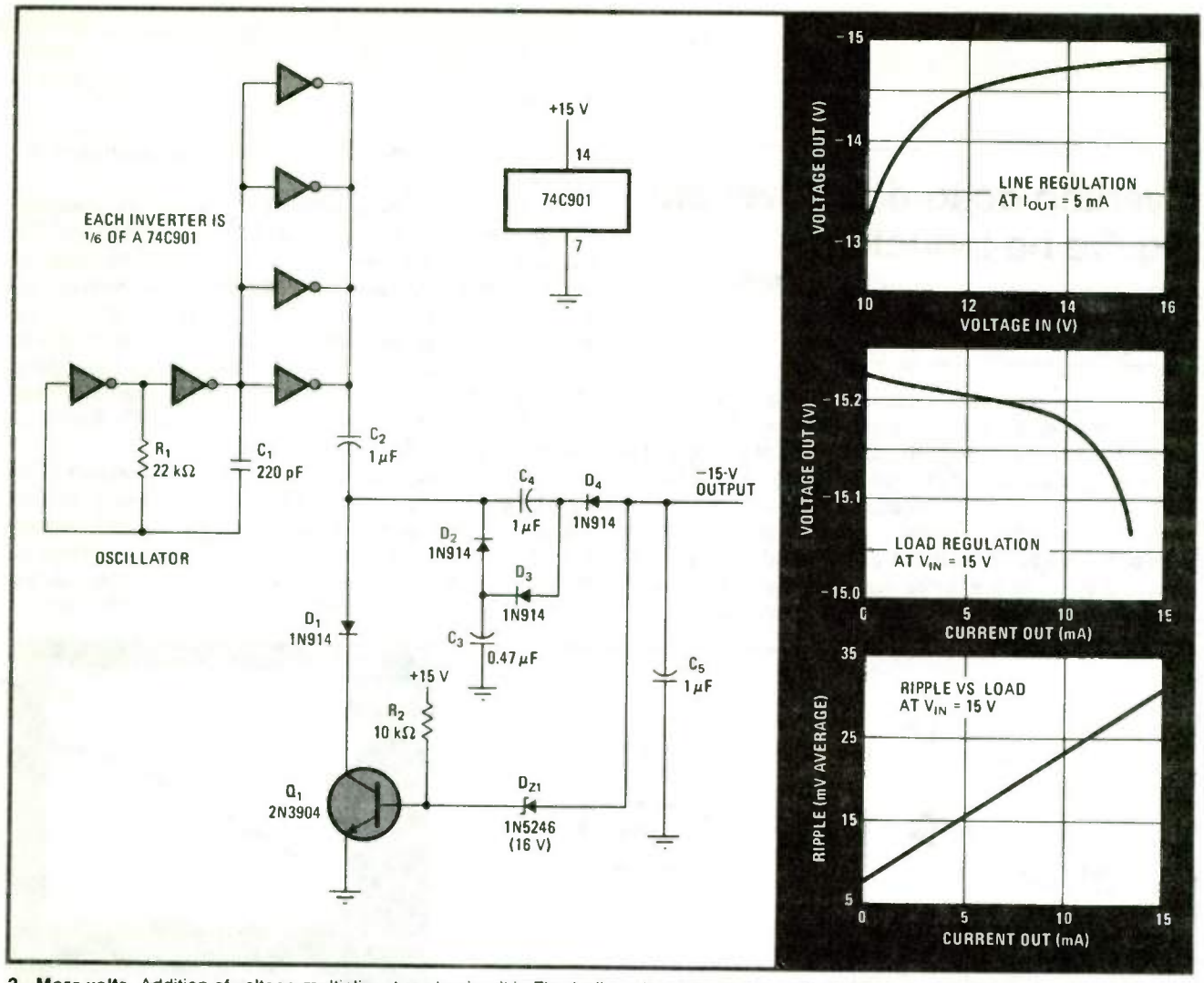
Many systems require a modest negative power source where only a positive power supply is available. Such a negative voltage can be produced by an inverting dc-to-dc converter installed right where it is needed. This arrangement is especially convenient in systems where the dc power is supplied remotely because only two wires need to be run to the point of use, instead of three. The inverting dc-to-dc converter described here requires no expensive transformers or inductors. Noise spikes associated with switching inductive loads are therefore eliminated.

To understand the operation of the circuit, consider first the −5-volt converter shown in Fig. 1. Resistor R_1, capacitor C_1, and two inverters form a free-running 100-kilohertz oscillator. The remaining four inverters in the hex-inverter package form a power driver. On the positive swing at the output of the power driver, C_2 is charged through diode D_1 and transistor Q_1 (assuming that Q_1 is on). When the output of the power driver drops back to zero, D_1 reverse-biases and D_2 forward-biases, so charge is transferred to C_3.

As the cycle repeats, C_3 is charged to a negative voltage that approaches the positive-output swing minus the diode drops, power-driver drop, and the drop across Q_1. Q_1 is held on by R_2 until the base-drive current is shunted away by the breakdown of D_{Z1}. This occurs when the negative output voltage exceeds the break-



1. Converts and Inverts. Dc-to-dc converter provides inverted regulated output of −5 volts without use of transformer or inductor. Instead, it puts negative potential on C_3 by discharge of C_2 during off-cycle of oscillator. Performance curves show data for typical units.



2. More volts. Addition of voltage-multiplier stage to circuit in Fig. 1 allows it to deliver a regulated output of −15 V. These inverting-converter circuits are convenient for producing negative voltages at locations remote from the main positive power source.

down voltage rating of D_{Z1}, less the V_{BE} of Q_1. Thus, the output voltage is regulated at $V_{out} = -(V_{Z1} - V_{BE})$.

With the output loaded, the negative output voltage of this circuit evidently cannot exceed that of the positive power-supply input in size. It is possible, however, to modify the circuit so that it produces a negative voltage equal to or larger than the input voltage. By adding a voltage-multiplier stage to the circuit of Fig. 1, for instance, the maximum possible output voltage can be doubled.

Such a circuit is shown in Fig. 2, in which C_4 is charged through D_3 on the positive swing of the power-output stage. However, now C_4 is charged from the negative voltage that appears at the negative terminal of C_3. The voltage across C_4 then approaches twice the input voltage, minus the drops. This voltage is transferred to the output capacitor as before. The negative-output voltage can therefore approach twice the input voltage, less the drops. □

IC timers control dc-dc converters

by P. R. K. Chetty
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An integrated-circuit timer such as the MC1455 can be used as the control element in a simple dc-to-dc converter regulator. Shown below are a current step-up converter regulator and a polarity-reversing voltage step-up converter regulator. Both are regulated to within 0.5% for load currents of 300 milliamperes, and have a ripple of less than 5 mA.

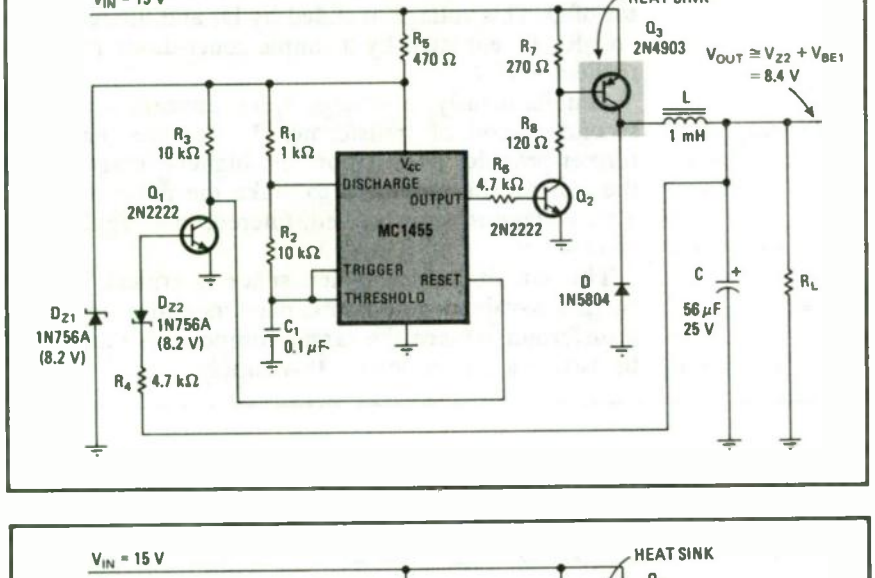
In these circuits the MC1455 operates as an astable multivibrator, turning the pass transistor on and off to keep the output-filter capacitor charged to the desired output voltage. Overvoltage is prevented by a feedback arrangement that turns off the multivibrator when the capacitor voltage reaches a predetermined level.

The astable-mode connection of the timer causes the voltage across capacitor C_1 to oscillate between $V_{CC}/3$ and $2\ V_{CC}/3$ at a frequency of approximately $1.44/(R_1+R_2)C_1$—about 1.3 kilohertz. The maximum operating voltage of the timer is 16 volts, but here its V_{CC} is clamped at 8.2 v by zener diode D_{Z1}. The input voltage therefore can have any value within the ratings of the pass transistor and the filter capacitor.

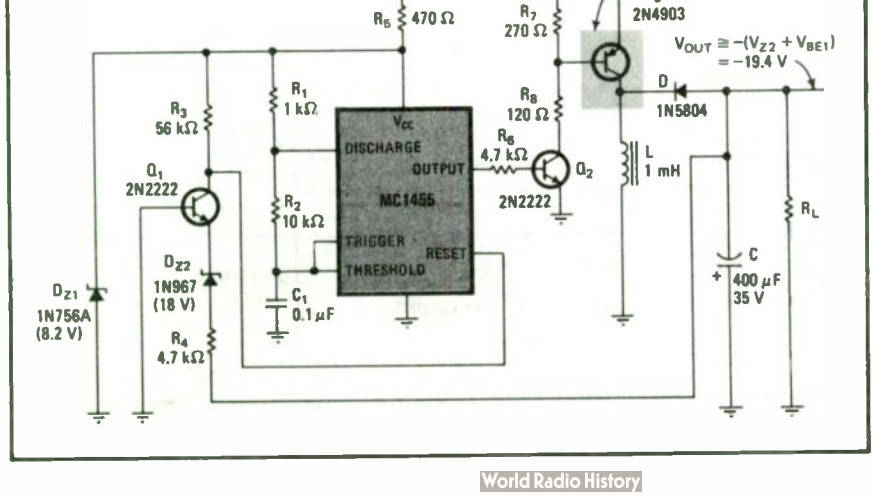
Figure 1 shows the current step-up converter regulator. When the output of the control timer is high, transistor Q_2 is turned on and therefore pass transistor Q_3 is turned on. Collector current from Q_3 flows through inductor L into the load and the filter capacitor. When the output of the timer goes low, the transistors turn off. Diode D commutates the current flow flowing through the inductor when Q_3 switches off. If there were no feedback circuit, the output voltage would depend upon the input voltage and the duty cycle.

The feedback circuit consists of R_4, zener diode D_{Z2}, transistor Q_1, and R_3, Whenever the output voltage exceeds $(V_{Z2}+V_{BE1})$, Q_1 turns on and drives the reset terminal of the 1455 low. The transistors Q_2 and Q_3 therefore stay off, allowing the output voltage to decrease. Thus the output voltage V_{out} is maintained approximately equal to $(V_{Z1}+V_{BE1})$.

The performance of the circuit in Fig. 1 is as follows:



1. Converted and regulated. Dc-to-dc converter includes IC timer for regulation. The MC1455, connected as free-running multivibrator, switches Q_3 on and off. If output gets too high, feedback circuit drives timer reset low to hold switch off. Regulation is less than 0.5% at 300 mA, and ripple is less than 5 mA. Output voltage is lower than input voltage, so current can be stepped up.



2. Polarity reversed. Positions of inductor, commutating diode, and feedback elements are changed here for negative output voltage. This circuit arrangement can step up magnitude of either voltage or current; components chosen here provide voltage step-up. Regulation is same as before.

Input voltage, V_{in} = 15 V
Output voltage, V_{out} = 8.4 V
Load current, I_{out} = 300 mA
Ripple, I_r (for I_{out} = 300 mA) = 5 mA
Load regulation (for V_{in} = 15 V and I_{out} = 0–300 mA) equals or is less than 0.5%
Line regulation (for V_{in} = 15–25 V and I_{out} = 300 mA) equals or is less than 2.5%

The polarity-reversing circuit of Fig. 2 differs from Fig. 1 in the arrangement of L, C, D, and the feedback elements. When Q_3 switches off, the commutating current in L charges C to produce an output voltage that is negative with respect to ground. This voltage is applied to the anode of D_{Z2} through limiting resistor R_4. Whenever the output is more negative than $-(V_{Z2} + V_{BE1})$, the timer reset goes low, allowing the voltage across the capacitor to become less negative. The output voltage of this circuit is therefore maintained at approximately $-(V_{Z2} + V_{BE1})$. This circuit can provide an output voltage equal to, less than, or greater than the input voltage.

The performance of the circuit in Fig. 2 is as follows:
Input voltage, V_{in} = +15 V
Output voltage, V_{out} = −19.4 V
Load current, I_{out} = 300 mA
Ripple and regulation are the same as in the earlier example. □

Compact dc-dc converter yields ±15 V from +5 V

by Thomas Durgavich
Massachusetts Institute of Technology, Cambridge, Mass.

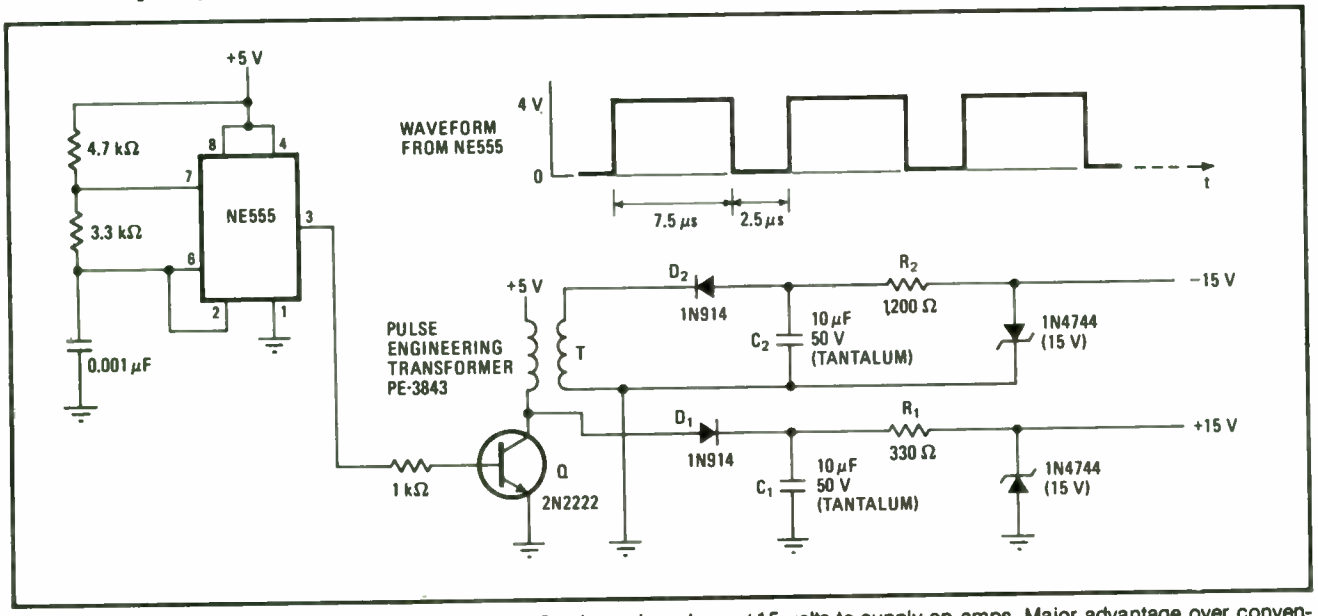
Many digital systems use a few operational amplifiers that require voltages of +15 V and −15 V, when all other elements require only 5 V. Both the +15 V and −15 V can be supplied at 10 milliamperes by a dc-to-dc converter that is compact enough to be built right on a printed-circuit board.

In this circuit, the NE555 operates as an astable multivibrator at 100 kilohertz with a 75% duty cycle. The value of frequency need not be exact, but this waveform has been found to optimize operation of the circuit.

The pulse train from the multivibrator drives the base of transistor Q to switch current on and off in the primary coil of transformer T. When the current is switched off, a spike of about 20 V occurs at the collector of Q. This voltage, rectified by D_1 and filtered by C_1 and R_1, is regulated by a simple zener-diode regulator to yield +15 V.

Simultaneously, a voltage spike appears across the secondary coil of transformer T. Because the transformer provides dc isolation, the higher-voltage end of the coil can be grounded to make the pulse negative. This voltage is also rectified, filtered, and regulated to yield −15 V.

This circuit is ideal when space is critical because small low-valued tantalum capacitors and a tiny pulse transformer replace the larger components that would be used in a conventional ±15-V supply. □



Space saver. Bipolar dc-to-dc converter operates from 5 volts and produces ±15 volts to supply op amps. Major advantage over conventional supply is small size, allowing assembly right on circuit board with other elements of system that it serves.

Power-supply add-on yields variable-ratio output

by Ying-Lau Lee
Cambridge, Mass.

A single-ended power supply can be converted into a double-ended supply with the addition of an operational amplifier, a transistor, and a few resistors. The two output voltages need not be equal and in fact can be made to have a ratio as big as 10:1 with the proper choice of resistor values.

The circuit is simple and works essentially as a parallel regulator. Potentiometer R_1 is set to the desired ratio of V_1/V_2; the 741 operational amplifier then compares the potentiometer voltage with the voltage at the collector of transistor Q and tries to minimize the difference by biasing Q to produce that ratio. If V_2 is too large, for example, the op amp drives Q farther into conduction. The drop across Q (i.e., V_2) then decreases.

The values of resistors R_2 and R_3 depend upon the maximum load allowed, input voltage, output voltage ratio, and transistor current gain h_{FE}. Approximate values for these resistors are calculated as follows:

$$R_2 = 0.8\,(V_1/V_2)R_{L2}$$
$$R_3 = h_{FE}\,V_{IN}R_{L1}R_2/V_1(R_{L1}+R_2)$$

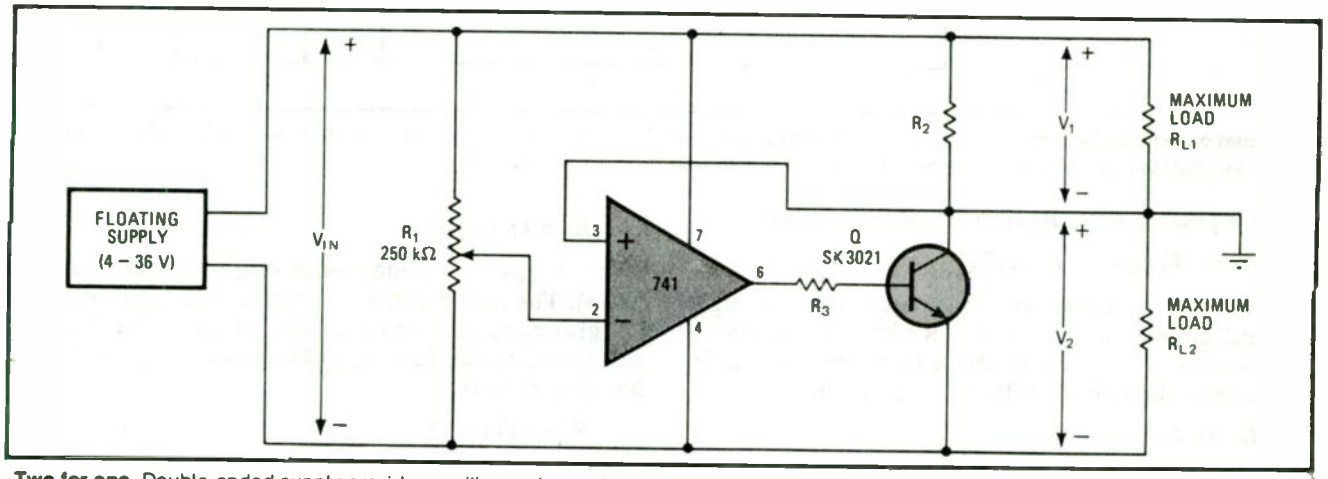
With R_2 and R_3 fixed, V_1/V_2 can be varied ±10% by adjustment of R_3.

If the outputs were balanced, no current would flow to ground. For unbalanced outputs, Q and R_2 carry the ground current. Transistor Q must be able to dissipate a power given by the following equation:

$$P_D = V_1V_2(R_{L1}+R_2)/R_{L1}R_2$$

The SK3021 transistor that is suggested in the schematic can dissipate 35 watts, but a lower-power device will be satisfactory in many cases. If Q drains too much current from the 741, a Darlington pair should be used to provide greater current gain.

Regulation of the output voltages is approximately that of the floating supply that is their source. The minimum value of output voltage V_2 is about 3 v (limited by the 741). The 741 is used for the operational amplifier because it is internally compensated and has overload protection. □



Two for one. Double-ended supply provides positive and negative voltages from a single source. Output voltages can be equal, or in ratio as great as 10:1. Potentiometer allows adjustment of V_1/V_2 around a "ballpark" value determined by resistors in circuit.

Regulated power supply is adjustable from 0 to 38 V

by Frank P. Miles
Rochester, N.Y.

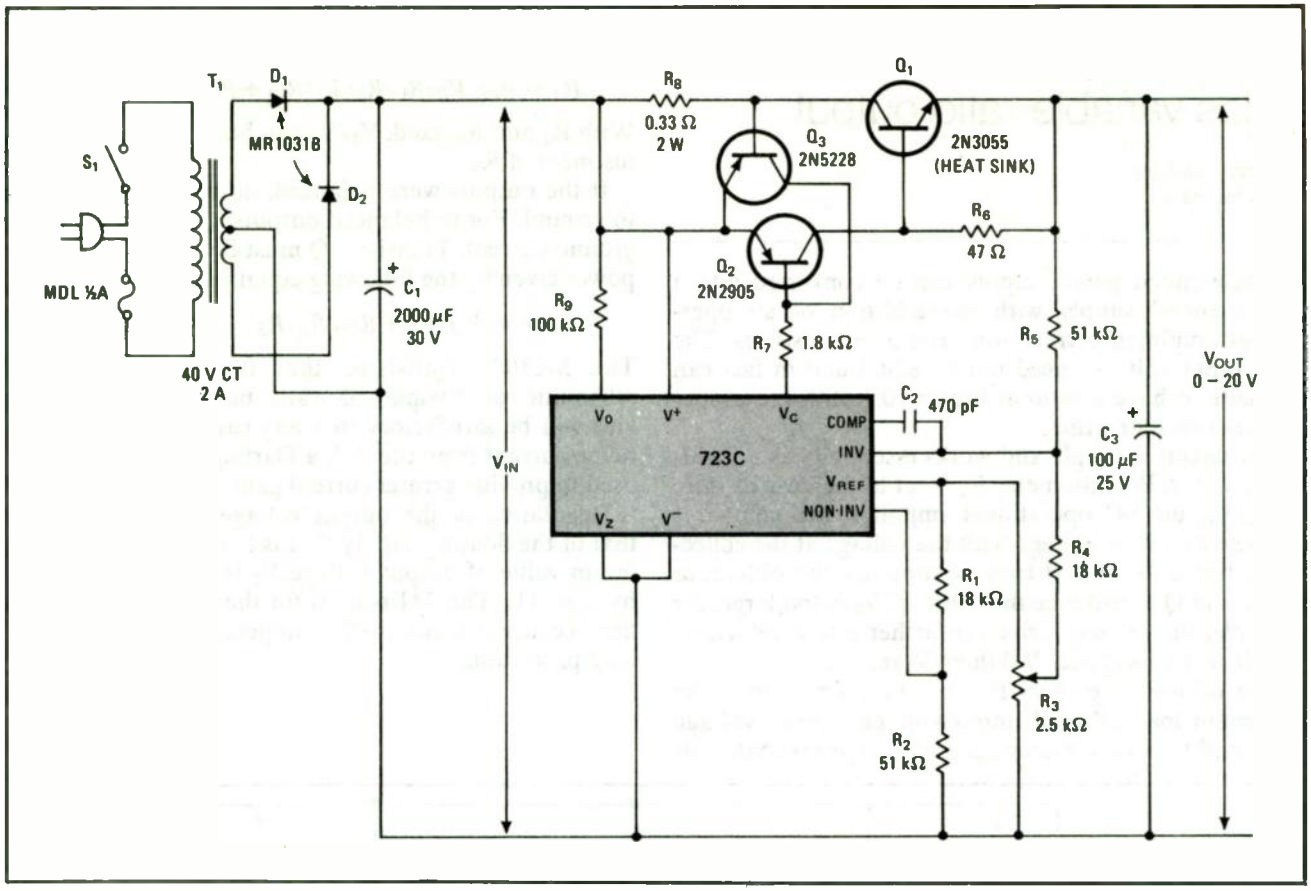
Through careful biasing of the error-sensing and the output driver for a 723C voltage regulator, a power supply that is variable from 0 to 38 volts can be designed. The stability of the circuit over both time and temperature is excellent, depending only on the internal reference of the chip and being essentially independent of output level. And finally, the circuit requires few components; most notably, it requires no zener diodes external to the 723C.

The schematic shows how simple it is to custom-design the supply. R_3 is a 2.5-kilohm potentiometer, chosen to keep the reference current below 5 milliamperes. $R_1 = R_4$ and $R_2 = R_5$ for best bias stability and output-range swing. The leakage-limiting resistor R_6 has a value of 47 ohms; it increases the safe operating area of Q_1.

The maximum output voltage is given by

$$V_{OUT(max)} = (R_2/R_1)V_{REF}$$

where the reference voltage V_{REF}, a characteristic of the 723C, is typically 7.15 v. Resistor R_1 is picked to be high enough to minimize loading of R_3, but small enough to avoid bias-current problems at the error-am-



Regulated power supply. Setting of R_3 gives output voltage as low as 0 V, or as high as V_{IN} minus small drop across Q_1. Value of V_{IN} must not exceed 40-V limit of the 723C. Components shown here are for 0–20-V, 2-A supply.

plifier inputs. Resistor R_2 is then calculated from

$$R_2 = (V_{OUT(max)}/V_{REF})R_4$$

The other resistors are calculated from straightforward circuit considerations. Resistor R_7 limits the output drive of the 723C to about 10 mA because the internal zener diode is used. Its value, in kilohms, is

$$R_7 \approx 0.1\ V_{IN} - 0.62$$

where V_{IN} is the unregulated voltage out of the rectifier. (The value of V_{IN} must not exceed the 40-V limit of the 723C.) R_8, calculated in ohms, provides the proper current-limit point:

$$R_8 \approx 0.65/I_{LIMIT}$$

where I_{LIMIT} is the maximum output current (in amperes). The pass transistor characteristics and heat sink are also determined by the value of I_{LIMIT}. Resistor R_9, calculated in kilohms, maintains zener regulation for low output currents:

$$R_9 \approx 5V_{IN} - 31$$

The output voltage from this supply can be as low as 0 V, or as high as V_{IN} minus a small drop across the pass transistor. The component values shown in the circuit diagram are chosen for a 0–20-V, 2-A supply. □

Gate bias circuit for n-MOS runs from 5-V TTL supply

by Bud Broeker
Motorola Semiconductor Products, Phoenix, Ariz.

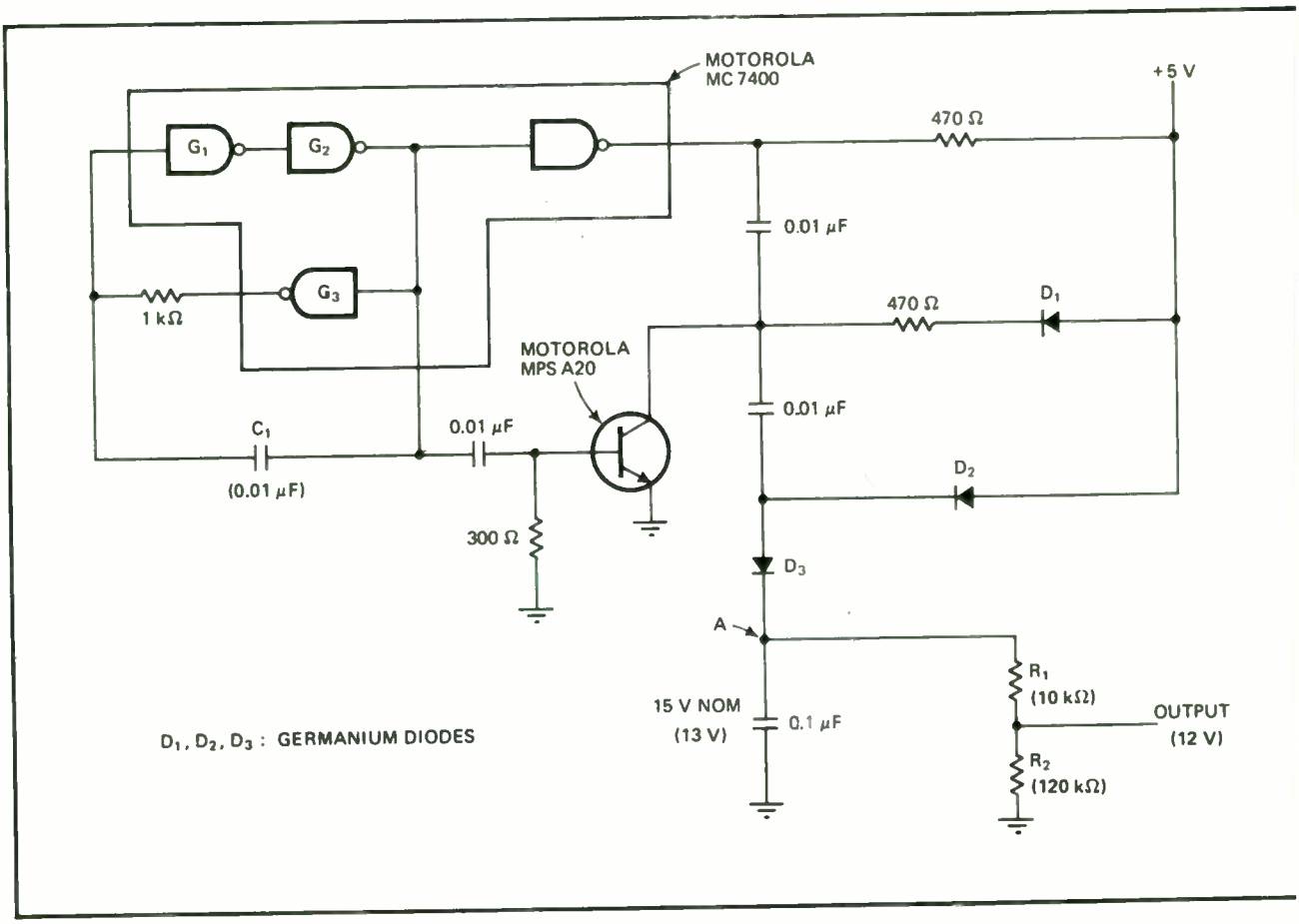
Complete compatibility with both transistor-transistor-logic circuits and diode-transistor-logic circuits is one of the major advantages that n-channel metal-oxide semiconductors have over p-channel MOS devices. For some n-MOS devices, however, another power supply, in addition to the 5-volt supply used by bipolar logic, is needed to bias the n-MOS gate. Because the current required for this n-MOS gate bias supply is very small—on the order of a leakage current—the higher-voltage n-MOS supply can be made to operate directly from the 5-V bipolar supply.

The circuit shown provides a typical bias voltage of 12 V while operating from the bipolar supply. It is primarily intended for a CRT display system that contains mostly TTL circuits, except for a 128 × 9 × 7 n-MOS character generator.

The bias supply consists of a pulse generator formed by gates G_1, G_2, and G_3, and a voltage tripler, which develops a nominal 15-V output (minus three diode drops) at point A. Germanium diodes are used here for D_1, D_2, and D_3 to minimize the size of the diode drop, but Schottky diodes can be substituted. A voltage divider network, composed of resistors R_1 and R_2, is used to reduce the voltage produced by the tripler (at point A) to the desired n-MOS bias voltage.

For the CRT display system, a bias current of not more than 10 microamperes at a bias voltage of 12 V is needed. But if capacitor C_1 is 0.01 microfarad, the voltage at point A is equal to 13 V. To reduce the effect of variations in the n-MOS bias current on the tripler, the divider network, with R_1 = 10 kilohms and R_2 = 120 kilohms, causes the tripler's load current to be 100 μA. And the output voltage of the over-all circuit is now at the desired 12-V level and remains within an acceptable tolerance of less than 10% variation. □

An n-MOS voltage booster. Bias supply for n-channel MOS devices operates directly from 5-volt supply used to power TTL devices. The higher potential sometimes required for n-MOS can be derived this way because n-MOS requires only leakage-level bias current. Circuit employs pulse generator (G_1, G_2, and G_3), voltage tripler, and voltage divider (R_1 and R_2) to develop 12-V output. Nominal output is 15 V.



Filament transformer output drops cost of 400-Hz supply

by Glen Coers
Texas Instruments, Components Group, Dallas, Texas

Power supplies with a 400-hertz output are often needed in testing servo systems and aircraft equipment, but they can be expensive to build when their output voltage must be on the order of 115 volts, root mean square. This being the equivalent of a peak-to-peak voltage of 325 V, the circuit transistors would have to have very high operating voltage ratings, and since there are no integrated amplifiers that can handle ±160 V, a discrete amplifier would be required.

Alternatively, the number of parts and component costs can both be considerably reduced by generating the 400-Hz sine wave at some low voltage level and then stepping it up with a transformer. This approach allows low-cost transistors and integrated circuit operational amplifiers to be used, yet it produces enough output power to operate small motors, servos, resolvers, and synchros. Larger output transistors and a larger transformer will, of course, increase output power.

The audio oscillator of (a) provides the sine-wave input for the amplifier of (b). The frequency-determining components for the oscillator are resistors R_1 and R_2 and capacitors C_1 and C_2. These are returned to the non-inverting input of an op amp that functions as the circuit's oscillating element.

Voltage gain for the amplifier is supplied by an op amp, while discrete transistors supply current gain. The input sine-wave frequency can vary from 60 to 400 Hz when a conventional filament transformer is used at the output. With the components shown, an output current of about 250 milliamperes is obtainable.

The amplitude of the input sine wave depends on the amount of feedback in the amplifier network. If the feedback factor is low, a small signal can drive the amplifier, but the output driving impedance becomes high, possibly causing current limiting in the output stage and therefore poor voltage regulation. If the feedback is high, a higher level of input voltage will be required, but the output driving impedance becomes lower and regulation is improved.

Here, op-amp closed-loop gain (A_{vc}) is 10, making the required drive voltage around 1 V rms. The value of feedback resistor R_f is determined by:

$R_f = R_s(A_{vc}-1) = 9$ kilohms

where R_s is source resistance. Feedback factor β is set by R_f and R_s:

$\beta = R_s/(R_s+R_f) = 0.1$

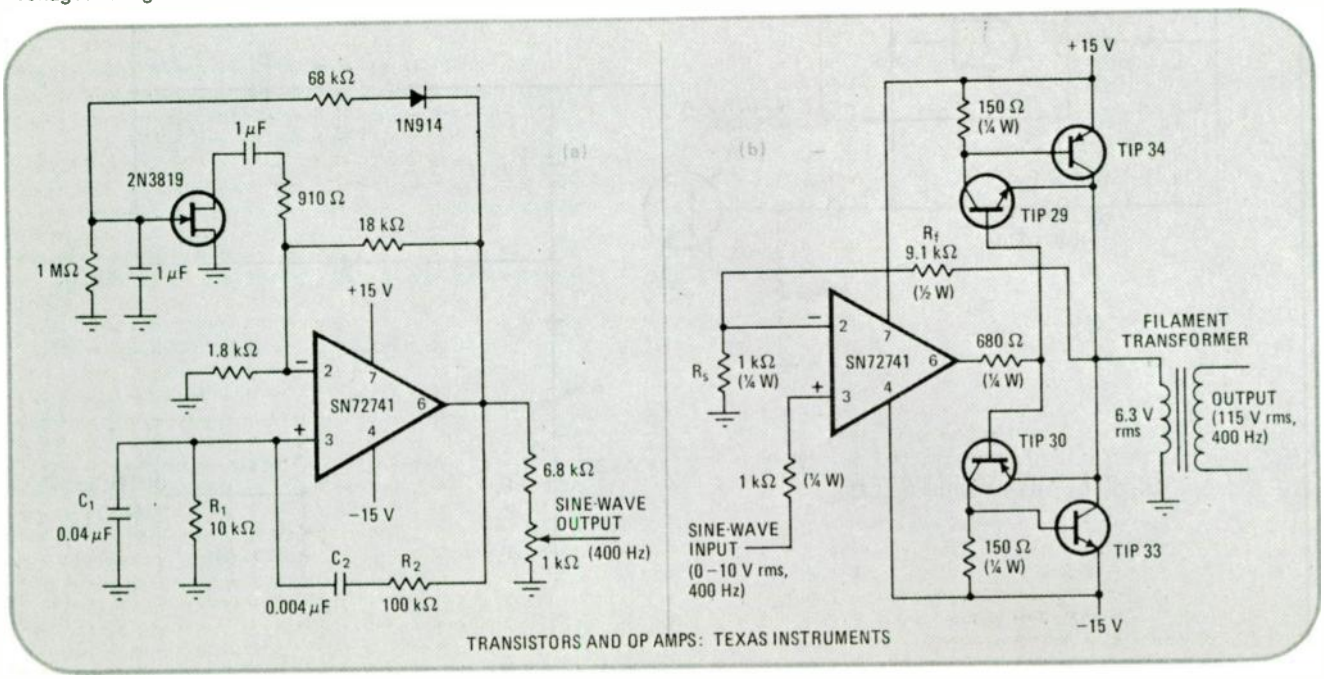
while closed-loop output resistance R_{out} becomes:

$R_{out} = R_o/A_{vo}\beta = 0.01$ ohms

when open-loop output resistance R_o equals 50 ohms, and open-loop gain A_{vo} is 50,000. This last equation indicates that circuit regulation should be adequate because the effective driving impedance is much lower than the load impedance.

The output transistors are connected in a bootstrap arrangement, eliminating two base-emitter voltage drops and allowing more ac voltage to be developed. A Darlington configuration could be substituted, but there would be a 5% drop in the available output voltage. Adjusting the 400-Hz drive voltage varies output voltage between 0 and 144 V rms. □

Servo supply. Amplifying low-level high-frequency sine-wave input cuts parts and price of 400-hertz 115-volt rms power supply. Audio oscillator (a) provides 1-V rms sine wave for amplifier (b). Standard filament transformer delivers output currents of up to 250 milliamperes and voltages as high as 144 V rms. Bootstrap arrangement of amplifier's output transistors optimizes available output voltage.



IC timer and voltage doubler form a dc-dc converter

by Todd Gartner
Motorola Inc., Automotive Research & Development, Franklin Park, Ill.

A dc-dc converter in which an IC timer serves as a free-running relaxation oscillator is ideal for powering op amps in battery-operated equipment or whenever a single positive supply is all that's available. Furthermore, the converter develops an output voltage of −15 V that is regulated to within ±1% for load currents of up to 30 milliamperes. The circuit's no-load current is 11 mA.

The free-running frequency of the timer is determined by resistors R_A and R_B and capacitor C_T. The output from the timer is used to drive the voltage-doubler network consisting of diodes D_1 through D_4 and capacitors C_1 through C_4.

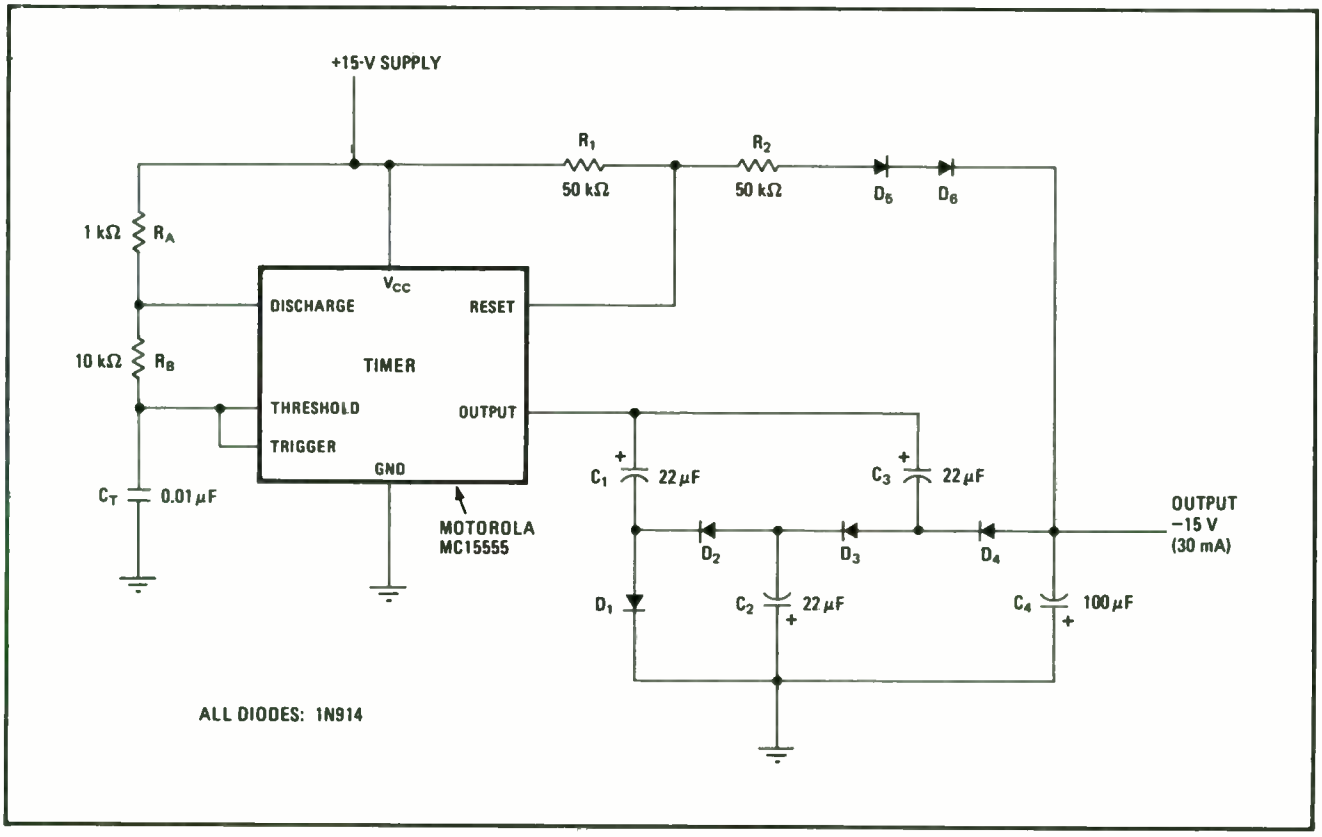
Without the feedback connection between the output of the voltage doubler and the reset input of the timer, the circuit's output under a no-load condition will float to about 30 V minus four diode voltage drops. With the feedback connection, the voltage divider formed by diodes D_5 and D_6 and resistors R_1 and R_2 places a 0.7-V voltage at the timer's reset input when the negative output voltage equals the positive input supply voltage in magnitude.

If the output voltage becomes more negative than −15 V, the timer's oscillation is inhibited, and therefore, the drive signal to the voltage doubler is removed. This type of circuit action provides switching-mode regulation of the output voltage.

The voltage doubler deserves a closer look because it may not be immediately apparent how it works. When the timer's output goes positive, capacitor C_1 is charged through diode D_1, and diode D_2 is reverse-biased. When the timer's output becomes negative, some of the charge on capacitor C_1 is transferred to capacitor C_2 through diode D_2, and diode D_1 is now reverse-biased.

As the output from the timer swings positive again, capacitor C_3 charges through capacitor C_2 and diode D_3 to approximately twice the supply voltage. For the timer's negative output swing, this charge is transferred to capacitor C_4 via diode D_4, doubling the output voltage from the timer. Such a voltage-doubler arrangement requires the driving source to supply, as well as sink, current.

The output voltage of the dc-dc converter will track the input supply voltage with reasonable accuracy. If resistors R_1 and R_2 are replaced by a single 100-kilohm potentiometer, the output voltage can be made contin-



For op amps. This dc-dc converter produces a −15-volt output from a +15-V supply input. The IC timer, which is wired as a free-running relaxation oscillator, drives a voltage doubler. The timer is reset so that its output is inhibited if the converter's output tries to go more negative than −15 V. The converter's output is regulated to within ±1% for load currents of up to 30 milliamperes.

uously variable down to zero. To regulate the output more fully against input voltage changes, resistor R_2 may be replaced by an appropriate zener diode. Diodes D_5 and D_6 are optional—they are used to offset the positive 0.7-v reset threshold of the timer to improve the circuit's output-to-input voltage tracking. □

SCR zero-cross trigger limits maximum load power

by Richard Eckhardt
Electronics Consulting & Development, Cambridge, Mass.

A zero-cross trigger for a silicon controlled rectifier will limit the maximum power delivered to a load if it is made to fire the SCR only on alternate cycles of the ac line input. Such an SCR triggering circuit is useful for driving loads rated at less than 110 volts. There are two advantages to limiting SCR conduction in this way—large amounts of power do not have to be wasted through dissipation, and the load can be powered continuously without the need for a power transformer.

With a zero-cross trigger, the SCR is fired only when the voltage across it is at or near the zero point in the driving ac waveform or pulsating dc waveform. Zero-voltage firing minimizes the generation of noise spikes that may occur when the voltage and current to the load are changed too rapidly.

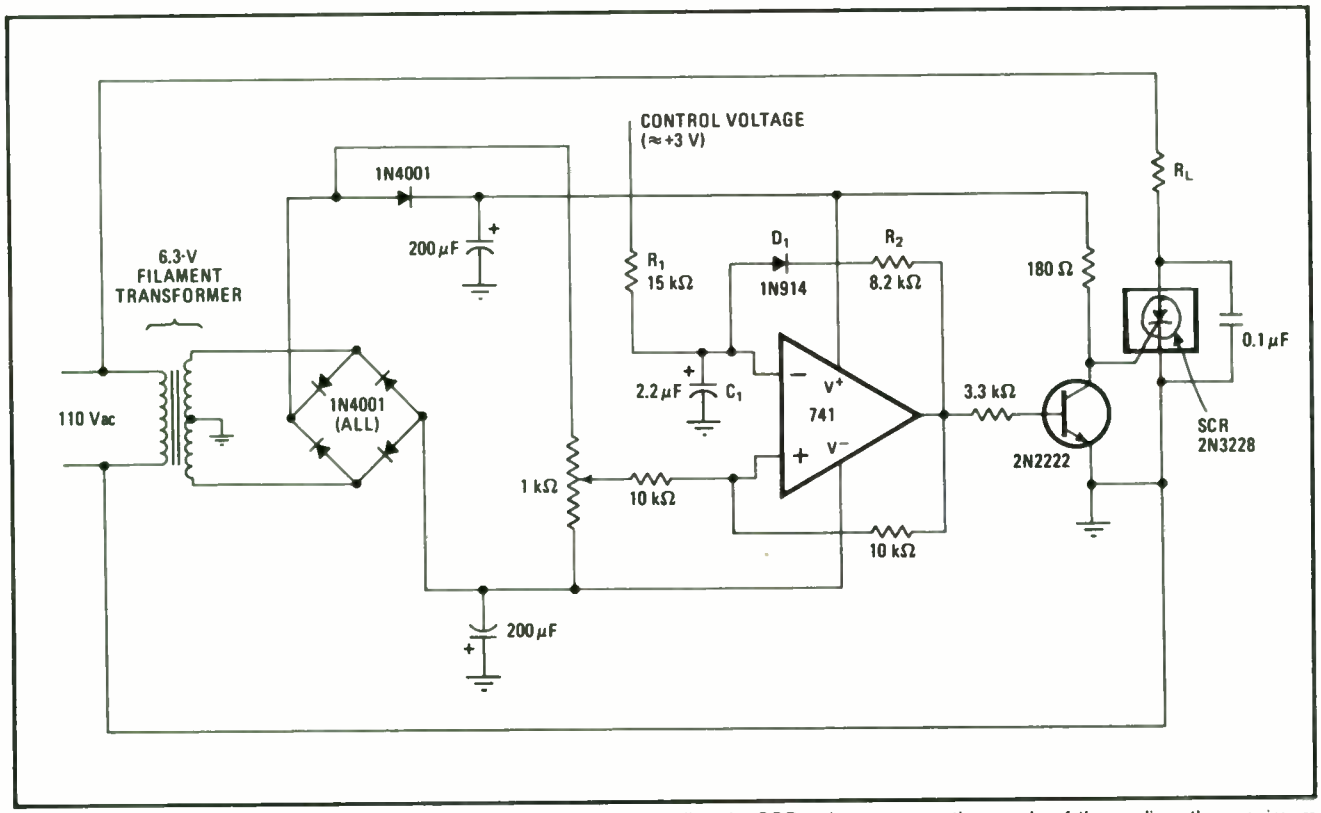
The zero-cross trigger shown here employs a general-purpose operational amplifier as a comparator. The control-voltage input varies the power applied to the load by governing the ratio of SCR on cycles to SCR off cycles. To increase the power supplied to the load, the control voltage is made larger.

Some of the pulsating dc voltage produced by the rectifier bridge is applied to the noninverting input of the op amp. The control voltage, which goes to the op amp's inverting input, charges capacitor C_1 through resistor R_1 until the capacitor's voltage exceeds the minimum point of the pulsating dc voltage.

When this happens, the output of the op amp goes negative, switching off the transistor and permitting the SCR to fire. Since the SCR is triggered at the minimum point of the pulsating dc voltage, the SCR turns on only when the ac voltage across it is at or near zero. The output of the op amp remains low until capacitor C_1 discharges through diode D_1 and resistor R_2.

This capacitor must be charged again by the control voltage before the SCR can be fired again. The charging time of capacitor C_1 determines how many successive cycles of the input voltage are included in the interval between SCR firings.

The circuit's dynamic range is established by the resistance ratio of charging resistor R_1 to discharging resistor R_2. □



Power limiting without power waste. Because this zero-cross trigger fires its SCR only on every other cycle of the ac line, the maximum power delivered to the load can be limited without the need for a power transformer or wasteful power dissipation. The control-voltage input determines the ratio of SCR on cycles to SCR off cycles. The larger the control voltage is, the greater the power to the load.

Handy supply provides fixed and variable outputs

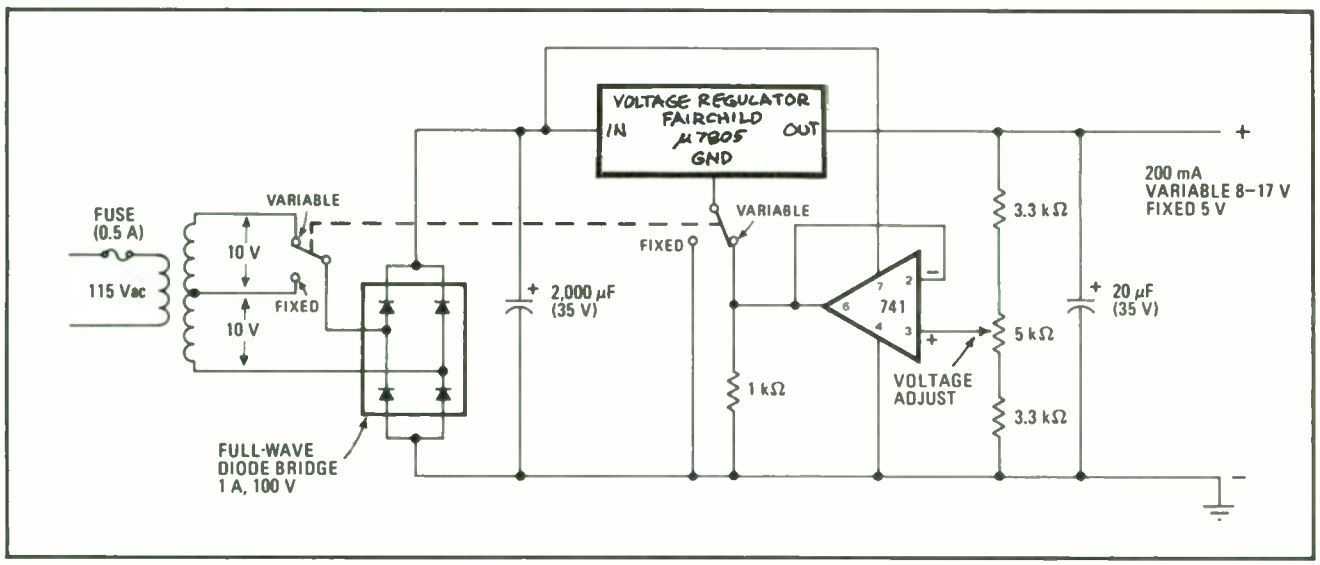
By John Predescu
Buchler Instruments Division, Nuclear-Chicago Corp., Fort Lee, N.J.

The advantages of today's integrated three-terminal voltage regulators are fully exploited by a versatile power supply that, besides being inexpensive (about $15) and easy to put together, provides a switch-selectable fixed or variable output. The variable output, which can be adjusted between 8 and 17 volts, is ideal for C-MOS logic, and the fixed output of 5 V is ideal for TTL circuits. Output current is 200 milliamperes.

The double-pole double-throw switch permits the same IC regulator and diode bridge to be used for both the fixed and variable outputs. The switch bypasses the operational amplifier network and taps the transformer's secondary voltage at the halfway point. A 5-V output can then be obtained from the IC regulator without exceeding this device's power dissipation rating.

If a second supply circuit is built and the positive side of its output grounded, a complete ±15-V op-amp supply can be made. Regulation is better than 1%. □

Convenient power supply. Line-powered supply, which makes use of a single three-terminal 5-volt IC regulator, offers switch-selectable fixed and variable outputs. The variable (8- to 17-V) output is obtained by employing a conventional op amp in the regulator's output loop. For the fixed (5-V) output, only half the transformer secondary voltage is taken so that the regulator's power rating is not exceeded.



Eliminating current spiking from dc-to-dc converters

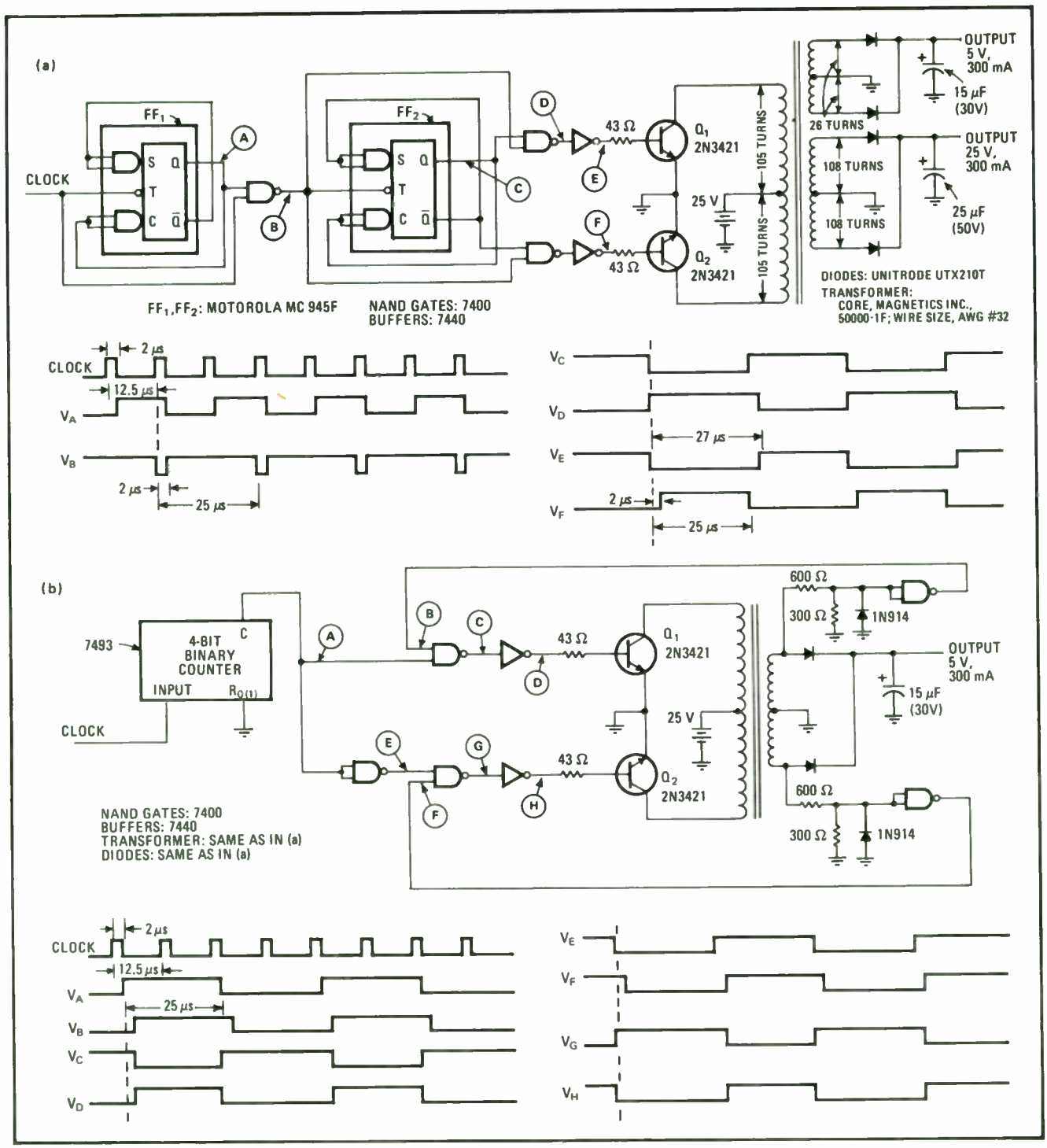
by Carlo Venditti
Charles Stark Draper Laboratory, MIT, Cambridge, Mass.

When the two inverter transistors in a push-pull dc-to-dc converter conduct at the same time, current spiking will occur and at worst destroy the circuit, at least degrade its efficiency. These undesirable effects can be prevented by delaying a clock pulse train with standard logic circuits.

Ideally one transistor turns on as soon as the other turns off. But because of their storage time constants, one is often still on when the other is beginning to conduct. All risk of simultaneous conduction will, however, be eliminated if the square-wave base drive signals to the transistors are made asymmetrical. The delay provided by logic gates ensures that, for a short length of time, there is no current drive signal at all. This delay can be fixed (constant) or controlled by feedback.

The figure shows two ways of designing a nonspiking static push-pull dc-to-dc converter. In (a), the current-drive delay time is fixed, and in (b), the delay depends on a feedback signal. In both cases, the transistor on-time is made smaller than the transistor off-time.

There are two output voltage levels for the converter in (a)—5 and 25 volts at a current of 300 milliamperes. The converter in (b) has just the one 5-V 300-mA output. Although a clock pulse generator operating at 80 kilohertz is used to synchronize each converter, the



Improving dc-dc converter efficiency. These dc-dc converters employ push-pull inverter transistors that switch at 20 kilohertz. Conventional digital ICs are used to delay the drive signals to the switching transistors so that these devices cannot conduct simultaneously, causing unwanted current spikes. The converter in (a) has a fixed delay, while the delay of the converter in (b) depends on a feedback signal voltage.

switching frequency is only 20 kHz in each case, and the nominal transistor on/off time is 25 microseconds (total period of 50 μs).

In the fixed-delay circuit of (a), flip-flops FF_1 and FF_2 generate the basic square-wave drive for transistors Q_1 and Q_2. The flip-flops divide the clock frequency down from 80 to 20 kilohertz, and the NAND gates provide the delays for the transistor drive signals.

The resulting asymmetrical driving waveforms have an on-time of 23 μs and an off-time of 27 μs. This means that each transistor experiences a 2-μs delay in its drive signal. For the transistors used here, this delay prevents current from flowing into the transformer primary for 0.5 μs. The width of the delay pulse (2 μs here) is too wide if the converter's output ripple voltage increases and too narrow if there is no deadband for the transformer primary current.

In the feedback-adjusted-delay circuit of (b), a binary counter, rather than flip-flops, divides the clock frequency down to 20 kHz. NAND gates again provide the

appropriate delays for producing asymmetrical transistor drive signals.

The feedback voltage, which is taken from the transformer secondary, determines when the transistors turn on, while the reference voltage from the counter output determines when they turn off. To delay the turn-on feedback signal properly, the storage time of the rectifier diodes, as well as the flux flyback time of the transformer, must be taken into account. For circuit (b), the deadband time is 0.3 μs. □

BIBLIOGRAPHY

Alphonso H. Marsh, "Gating Scheme Maximizes dc-dc Converter Efficiency," Electronic Design, June 22, 1972, p 100.

Robert F. Downs, "Minimize Overlap to Maximize Efficiency in Saturated Push-pull Circuits," EDN/EEE, Feb. 1, 1972, pp. 48–50.

SCR crowbar circuit fires quickly and surely

by Steve Summer

Hauppauge, N.Y.

A monolithic voltage regulator's presence in an SCR crowbar circuit makes the circuit fast-acting, dependable, and capable of producing fast-risetime drive currents as large as several amperes. The circuit shown in the diagram is simple yet effective, providing a drive current of 200 milliamperes with a risetime of 1 microsecond. The 723-type IC regulator is used as a comparator that contains its own stable reference voltage source. The setpoint of the comparator establishes the protection voltage level for the power-supply bus.

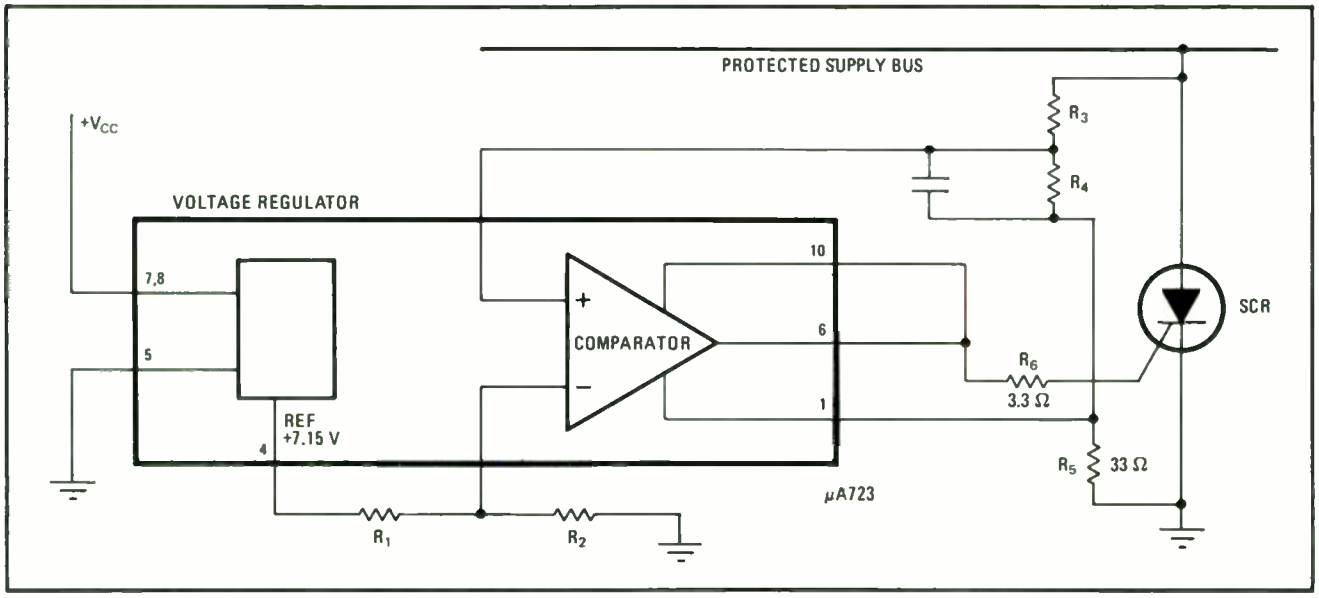
A satisfactory crowbar circuit for good power-supply protection generally asks a lot of the crowbar SCR. Typically, power supplies have large output capacitances that impose high surge currents and di/dt levels on the crowbar SCR when it is fired. These large current surges can cause SCR failure or degradation if the SCR drive current is inadequate or soft (has a slow risetime).

The gate drive required to attain the SCR's specified surge and di/dt capability may be many times greater than the worst-case gate drive needed for turn-on. In addition, for best di/dt resistance, the risetime of the gate drive should be quite short, preferably less than a microsecond.

Many simple crowbar circuits use such devices as zener diodes to fire the crowbar SCR. Although this results in a soft turn-on that will fire the SCR at least once, the dependability of such a scheme is questionable.

The circuit shown, however, is hard-firing. Resistors R_1 and R_2 make up a voltage divider that nominally sets the voltage at the inverting input of the comparator to 2 volts. Another voltage divider, consisting of resistors R_3 and R_4, samples the power-supply bus and drives the comparator's noninverting input. When the voltage on the power-supply bus exceeds the setpoint of the comparator, the output of the regulator rises. This voltage rise, which appears across resistor R_5, adds (in phase) to the voltage at the comparator's noninverting input, providing rapid regeneration, as well as a fast-rising pulse to drive the SCR.

Resistor R_6 limits the SCR drive current to about 200 milliamperes, a value that is adequate for sensitive-gate or amplifying-gate devices. To obtain larger drive currents of up to several amperes, an emitter-follower stage can be added at the output of the regulator. The capacitor acts as a filter to prevent the crowbar from firing in response to transient voltages. □



Hard-firing SCR. Crowbar protection circuit employs an IC voltage regulator to produce a fast-risetime large-value gate drive current for the SCR. The regulator, which is used as a comparator, has its own voltage reference source. When the voltage on the power-supply bus exceeds the set point of the comparator, the regulator's output voltage increases, producing a large fast-rising pulse that fires the SCR.

C-MOS voltage monitor protects Ni-Cd batteries

by William Wilke
University of Wisconsin, Madison, Wis.

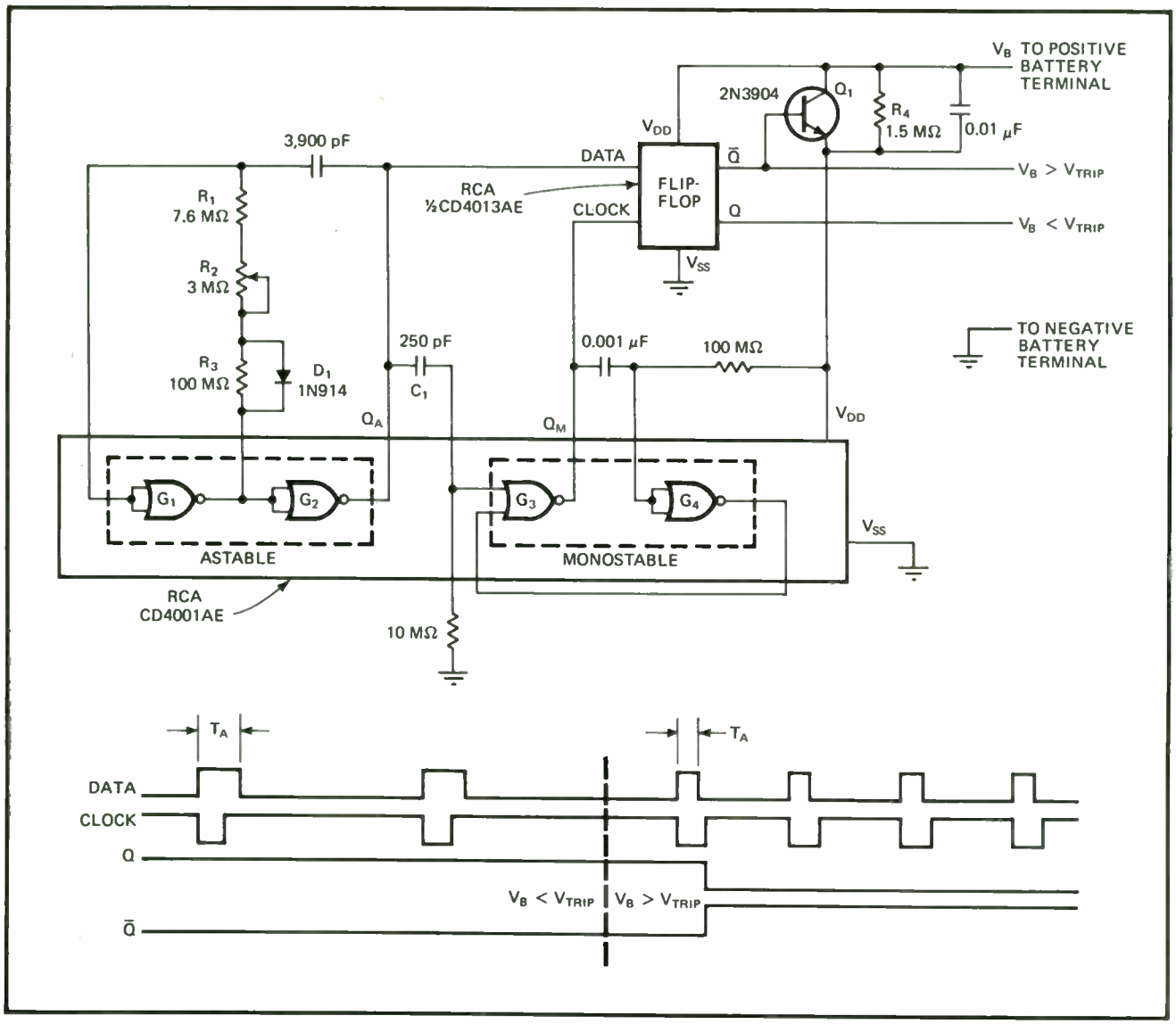
If nickel-cadmium batteries are permitted to discharge completely, they can be permanently damaged. To prevent this, a voltage monitor can be employed to turn off the equipment being supplied by the batteries when their voltage falls below a safe level. The monitor circuit shown draws as little as 0.5 microampere, has an adjustable voltage trip point and hysteresis, and it turns itself back on when the batteries are recharged.

The circuit basically consists of two complementary-MOS multivibrators—a monostable and an astable—and a network that compares their outputs. NOR gates G_1 and G_2 form the astable multivibrator, which has a period that varies with changes in the supply voltage, V_{DD}, obtained from the battery. On the other hand, NOR gates G_3 and G_4 make up a positive-edge-triggered monostable multivibrator that has an output pulse width that remains relatively constant even with some changes in the supply voltage.

The astable output, Q_A, is coupled through capacitor C_1 to fire the monostable, and the output is also fed to the DATA input of a D-type flip-flop. The monostable's output, $\bar{Q}_M$, drives the CLOCK input to this flip-flop.

Resistors R_1 and R_2 are adjusted so that the periods of the astable and the monostable are equal to each other when battery voltage V_B is at the desired trip voltage (V_{trip}). If battery voltage becomes higher than the trip voltage, the astable's period, T_A, decreases, and when the positive edge of the CLOCK pulse from the monostable reaches the flip-flop, its DATA input is low so that its $\bar{Q}$ output goes high.

At battery voltages below the trip voltage, the



Battery watchdog. Voltage monitor for nickel-cadmium batteries detects when battery voltage (V_B) is above or below desired level (V_{TRIP}). Here the trip point is 3.6 volts, and hysteresis is 0.2 V. C/MOS circuitry keeps current drain to as little as 0.5 microampere. The period of the astable varies with changing battery voltage, while the period of the monostable stays constant. Circuit costs under $6 to build.

astable's period increases. The flip-flop's DATA input, herefore, is still high when the clock fires, forcing the lip-flop's Q output to be high. In this way, the flip-flop Q and $\overline{Q}$ signals indicate whether battery voltage V_B is ess than trip voltage V_{TRIP} or V_B is greater than V_{TRIP}.

Diode D_1 and resistor R_3 are added to give the astable a duty cycle of approximately 10%. This addition assures that the output pulse width of the monostable remains independent of the rate at which the monostable is retriggered.

Circuit hysteresis is proportional to the value of resistor R_4, which bypasses transistor Q_1. When batter voltage falls below V_{TRIP}, the flip-flop $\overline{Q}$ signal goes low shutting transistor Q_1 off and further lowering the effec tive V_{DD} supply voltage by the size of the IR drop acros resistor R_4.

For the components shown, the voltage monitor has trip point of 3.6 volts, which is appropriate for thre series-connected batteries. Hysteresis is 0.2 V, and cur rent drain is 3 μA when V_B is greater than V_{TRIP}, bu only 0.5 μA when V_B is less than V_{TRIP}. Total parts cos is approximately $5.50.

Inexpensive power supply produces zero-ripple output

by Rod Spencer
Chlorescope Systems, Linden, N.J.

Here is an easy way to build a low-cost power supply in which ripple voltage can be brought virtually to zero. Through a feedback arrangement, the ripple voltage is inverted and summed to cancel the normal ripple.

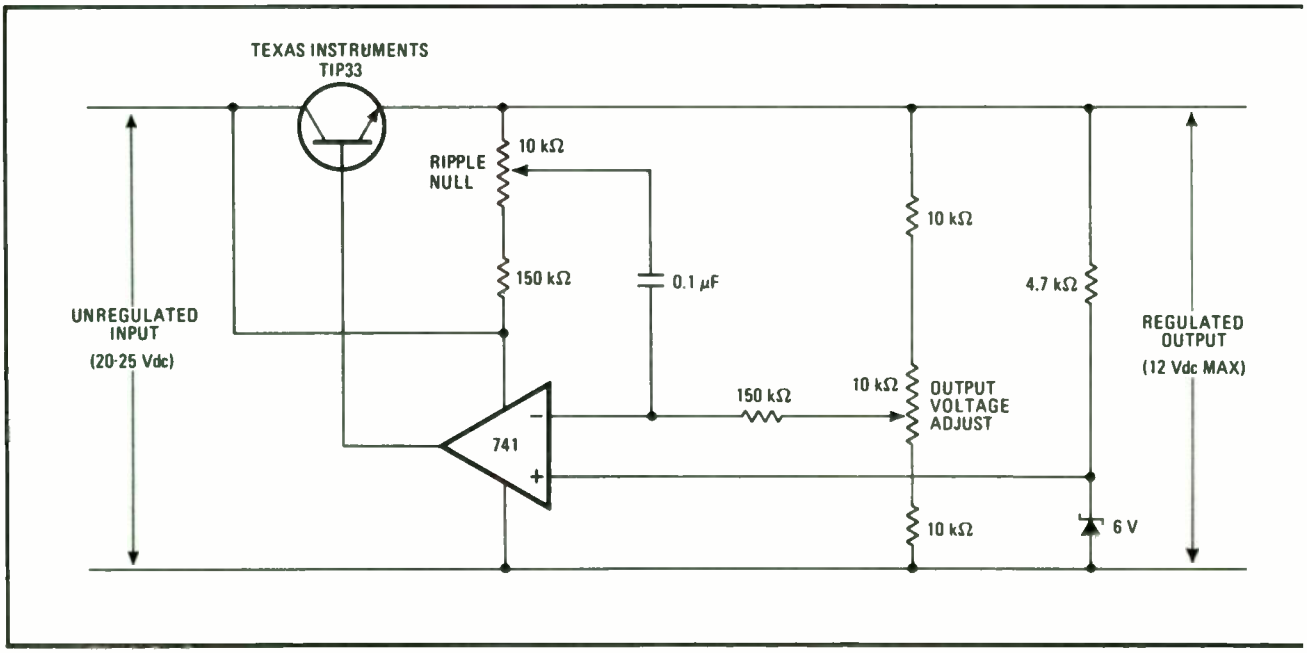
As indicated in the figure, an operational amplifier and a series-pass transistor are connected in the standard manner. However, a portion of the unregulated ripple voltage is fed into the op amp's inverting input.

When the wiper of the RIPPLE NULL potentiometer is set up toward the output voltage bus, the supply's ripple is normal. But when the pot wiper is set down toward its unregulated-input end, a phase shift of 180° is intro duced, and the ripple is reversed. If this RIPPLE NULL adjusted properly, the supply's ripple voltage can b completely eliminated.

To adjust the circuit, first set the regulated outpu voltage to the desired level and then subject the outpu to the maximum load condition. Next, use an oscillo scope to monitor load voltage, and trim the outpu ripple voltage to zero. This supply's ripple will remai essentially zero for any load condition less than th maximum.

Representative component values are shown in th figure, and parts should be chosen to satisfy a particula application. The series-pass transistor, of course, is se lected to meet load requirements. And, if an op am cannot supply a sufficient base drive for the transisto chosen, a Darlington pair can be used instead.

Canceling ripple. Low-cost power supply employs inverting feedback loop to eliminate output ripple voltage almost entirely. Some of the ci cuit's unregulated ripple is applied to the op amp's inverting input, where it is reversed. This "negative" ripple cancels the supply's norm "positive" ripple. The technique can be made to satisfy a variety of application requirements by adjusting the component values.



Timer circuit generates precision power-on reset

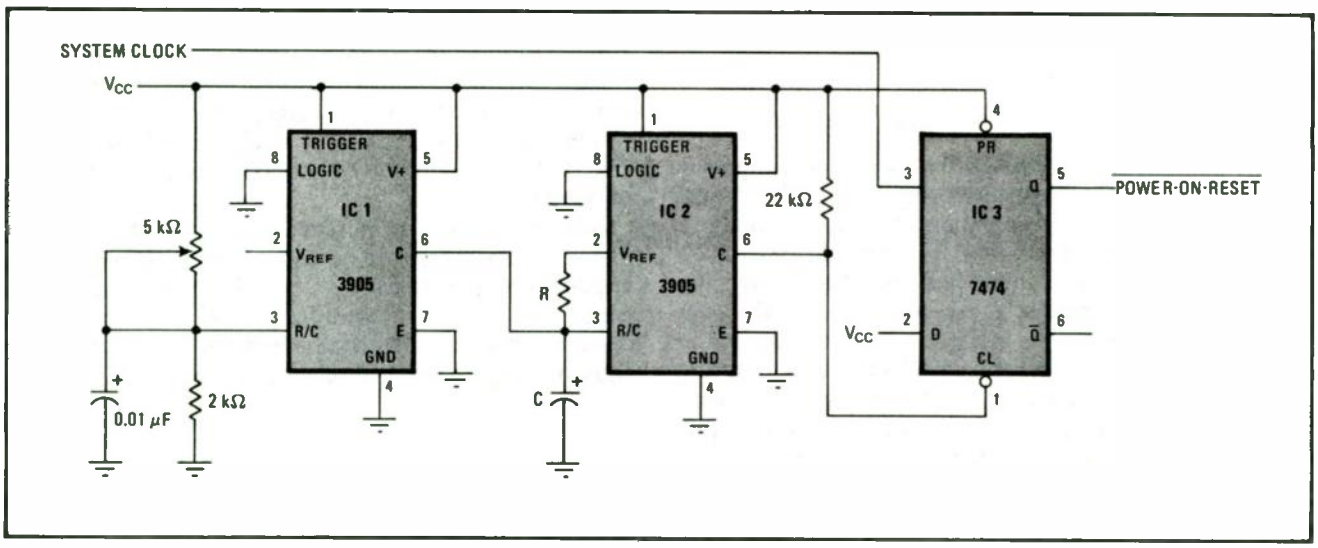
by Jim Felps
Texas Instruments Inc., Austin, Texas

Digital systems are commonly initialized with a power-on reset, generated automatically when the power switch is turned on, but at no other time. A typical circuit simply holds a reset line long enough for all the power transients to die out, then drops it. Its duration isn't well defined, and it doesn't respond to dips or glitches in the primary power line.

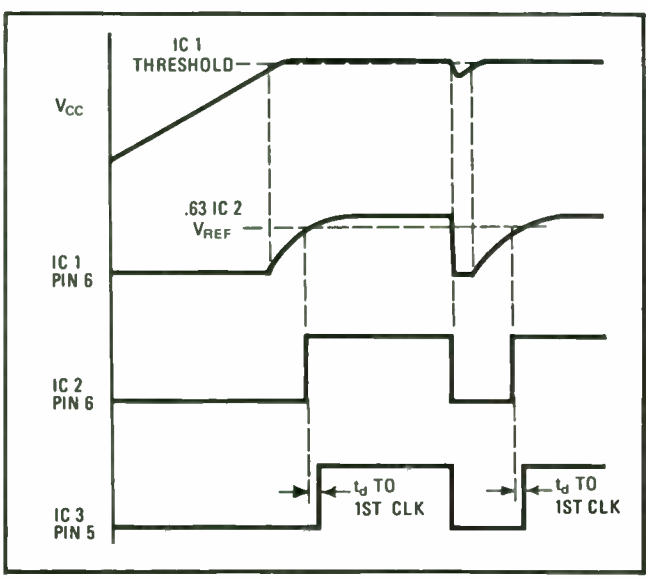
Until recently, a more precise power-on reset circuit would have been too complex and too costly to be justified. Now, however, new integrated circuits are available that contain voltage comparators and references that work at supply voltages as low as 4.5 volts. One such IC is the National Semiconductor LM 3905 N—a comparator, reference, and precision timer all in one eight-lead package.

In a power-on reset circuit based on the 3905 (Fig. 1), the timing begins only when the incoming V_{cc} has reached a suitable level, which can be very precisely established, and it is repeated if V_{cc} later drops even momentarily below that level. As a result, all logic circuits in the system are properly reset, even if the power reaches its nominal level only after an exceptionally long rise time, and no random logic failures can be caused by a power-line glitch.

IC 1 is a 3905 used as a comparator, which monitors the level of V_{cc} (nominally 5 volts for transistor-transistor logic). It keeps the reset on whenever V_{cc} is less than



1. Reset generator. One comparator, one timer and a flip-flop join forces to produce a precisely timed power-on reset.



2. Sequence. When V_{cc} reaches a threshold defined by the setting of the 5-kilohm potentiometer, IC 1 turns on. Its rise is delayed by the RC network on IC 2. After one time constant, the clear input to IC 3 is released, and the flip-flop is set by the next clock pulse.

4.75 V; its triggering level is established by setting V_{cc} at 4.75 and adjusting the 5-kilohm potentiometer at the point where the circuit's output (pin 5 of IC 3) just switches. Thereafter, when power is turned on and V_{cc} rises above this 4.75-V threshold (Fig. 2), IC 2, a 3905 used as a timer, is released. One time constant later, as determined by the RC network connected to pins 2 and 3 of IC 2, an ordinary 7474 D-type flip-flop, IC 3, is released. By this time the system clock should be running smoothly; at the next positive-going clock pulse the flip-flop is set, thus removing the power-on reset.

If the level of V_{cc} drops below 4.75 V at any time, both timers and the flip-flop immediately go down, generating another reset to the rest of the system. Restoration of V_{cc} initiates the power-on sequence again.

If less precise reset timing is necessary, IC 2 may be omitted. The output of IC 1 then rises as soon as the threshold has been passed, and the flip-flop is set by the next clock pulse. If several power supplies have to reach their nominal levels before the reset terminates, a separate 3095 as comparator can be connected to each supply and all the outputs (pin 6) connected to each other as a wired OR. □

Crowbar protection circuit senses load voltage directly

by Thomas E. Skopal
Acopian Corp., Easton, Pa.

The triggering point of the overvoltage-protection crowbar circuit for a power supply can be decreased without increasing the circuit's sensitivity to transients. The trick is to have the crowbar circuit sense the voltage across the load, rather than the output voltage of the power supply, as is usually done.

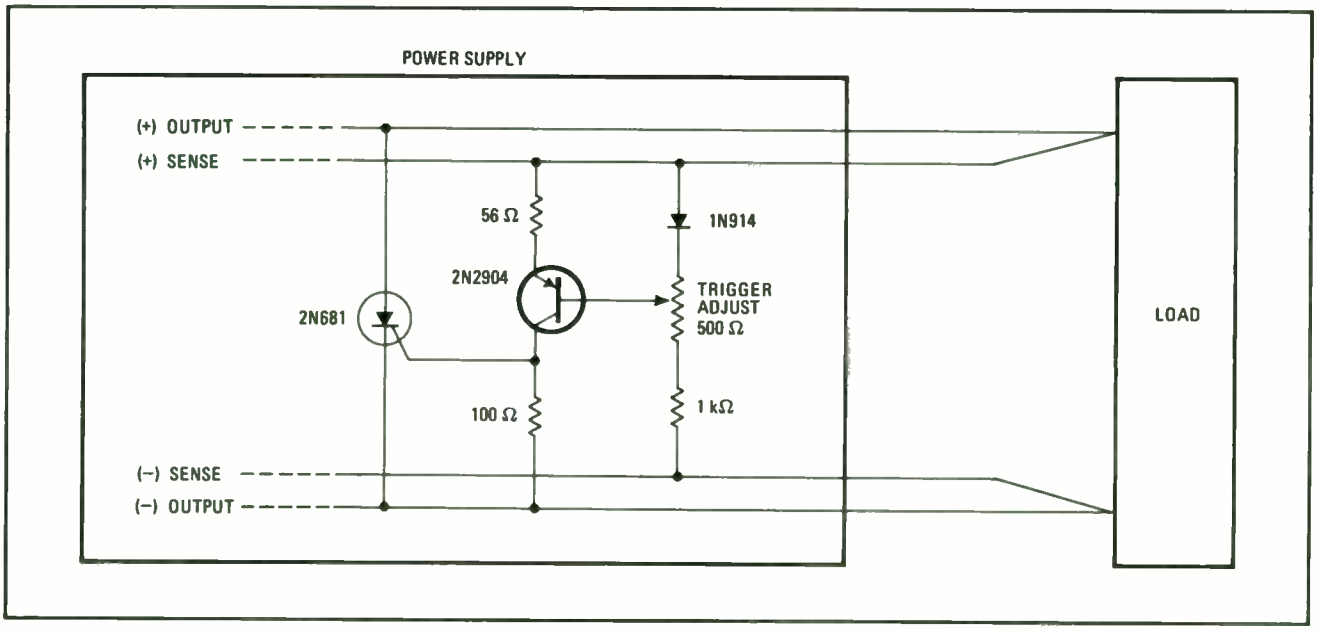
To provide maximum protection, a crowbar circuit is generally set reasonably close to the operating voltage required by the load. Typically, a compromise setting of about 15% above the load's operating voltage is chosen, because commonly encountered transients may cause spurious crowbar triggering and interfere with normal system operation if a tighter differential is used.

However, when voltage drops in the supply's output wiring exceed 2% or 3% of the output voltage—a common occurrence with low-voltage, high-current logic supplies—the system designer is faced with a dilemma. If he compensates for these drops with an increase in power-supply output voltage, the differential will be reduced and the crowbar's sensitivity to transients increased. And if crowbar setting is increased to maintain the same differential, load protection is degraded.

This conflict can be resolved by using the four-terminal crowbar circuit shown in the figure. It senses the voltage across the load, much as a supply's remote-sensing connections may be used to automatically compensate for voltage drops caused by long wires.

The crowbar's triggering point is a function of the voltage seen by the load, as opposed to the output voltage of the supply, and it is unaffected by the amplitude of the wiring voltage drops. Since the sensing connections of the crowbar share the sense lines of the supply's regulator, no additional system wiring is required.

The diode in the circuit provides temperature compensation for the transistor. The component values given are appropriate for power supplies having outputs of 4 to 10 volts and of up to 20 amperes. □



Better protection. Crowbar circuit protects a power supply from overvoltages by sensing the voltage across the load, instead of the supply's output voltage, which is the usual approach. This means that overvoltage sensing will not be affected by wiring voltage drops, nor will there be an increased sensitivity to voltage transients. The components shown here are for a power supply of 4 to 10 volts at up to 20 amperes.

Pulsed standby battery saves MOS memory data

by K. C. Herrick
Fisher Berkeley Corp., Emeryville, Calif.

A simple pulsed battery supply can reduce standby power necessary for MOS random-access memories to one-thousandth of the operational requirement. In many systems, this power-saving scheme allows inexpensive batteries to be used with essentially shelf-life longevity. In some cases, merely a capacitor can supply enough standby power to sustain memory until an auxiliary power source can come on-line.

A typical RAM cell consists of a cross-coupled multivibrator with active MOS transistor loads. When there is a power failure, the potential across the multivibrator declines toward zero. As long as its inputs are kept off, the cell is isolated from external influence, except for

leakages, when the MOS transistors cease conducting.

The charges remaining on the gates of the cross-coupled transistors then begin to leak off exponentially. If power is reapplied within a short period of time, however, sufficient differential charge levels remain on the gates to re-establish flip-flop conduction in the same state as when power failed.

It is this cell characteristic that can be exploited to save standby power. The potential across the multivibrator must be reapplied periodically, at a rate fast enough to replenish the MOS gate charges before they decline below threshold levels and for long enough to re-establish fully the charge levels. Usually, a sufficient rate is 1,000 hertz with a pulse width of 1 microsecond. For any given type of memory and upper temperature limit (leakages increase with temperature), the required duty cycle may vary.

Of course, the potential needed must be reapplied within the maximum period of time that is allowable (for example, 1 millisecond). The little-used series multivibrator and a 14-volt battery (a) will do the job. The nominal memory cell potential is 15 V, less one diode drop, or about 14.3 V.

When power fails, diode D_1 disconnects the RAM's V_{DD} line from the main supply. The memory potential of $V_{CC} - V_{DD}$ declines in magnitude until the voltage of $14 - (V_{CC} - V_{DD})$ is large enough to start the series multivibrator. Oscillations usually begin when the voltage across the multivibrator becomes about 0.75 V. The components shown yield a pulse width of about 1 μs and a pulse interval of about 500 μs.

If a rechargeable battery is used, the diode and resistor connected with dashed lines may be added to allow the battery to charge while the main power is applied. The memory's peripheral-circuit supply voltage V_D can become zero and remain zero during the loss of main power, without any effect on data retention.

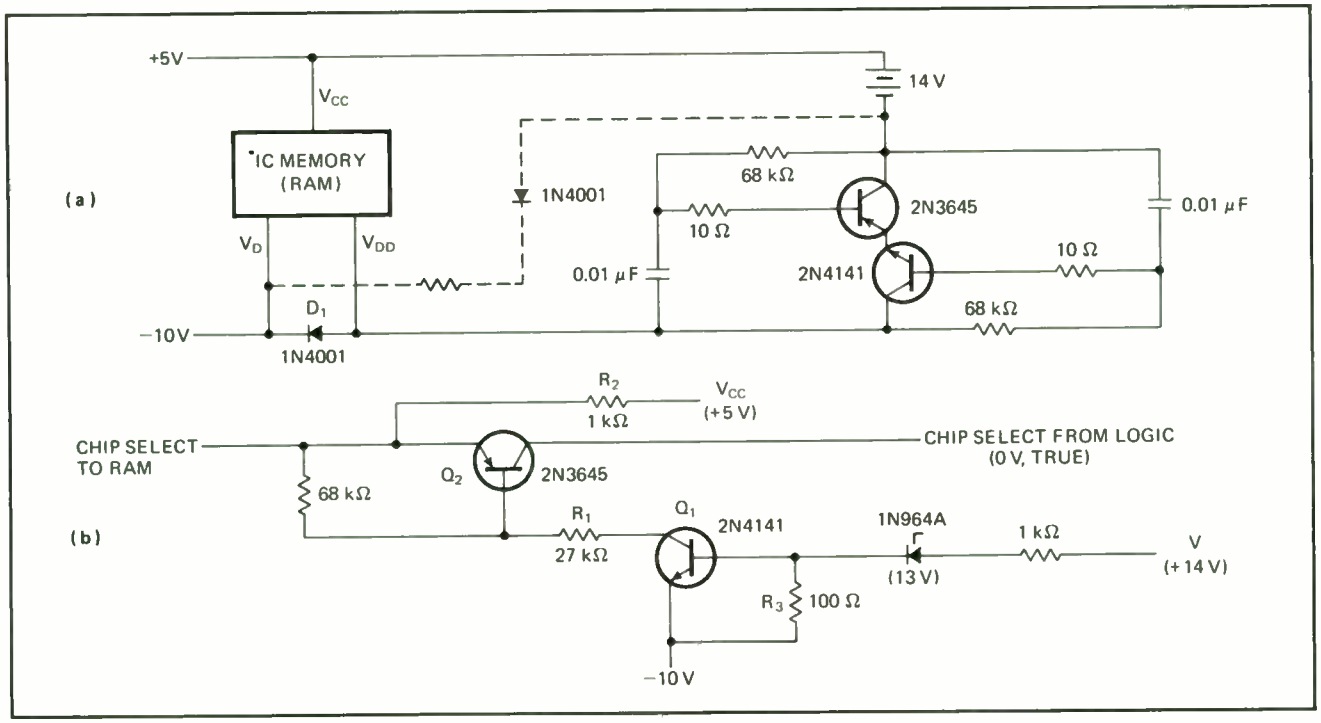
While the memory supply voltage is decreasing, the memory's chip-select input must be held FALSE at the V_{CC} (+5 V) potential. TTL devices or other elements driving this line may change state erratically when the 5-V logic supply loses voltage. The presence of these stray signals may cause a RAM cell to change state.

A circuit for maintaining the chip-select line at the instantaneous V_{CC} level is shown in (b). Since the 14-V (in this case) semi-regulated supply is the power source for the 5-V regulated logic supply, in the event of power failure the 14-V source will lose voltage before the logic supply.

Transistor Q_1 is normally kept on by base current from the 14-V supply via zener diode D_1. Collector current from Q_1 biases Q_2 on. Base current from Q_2 causes only a negligible drop below 5 V in the FALSE voltage level of the memory chip-select line, due to the high resistance ratio of R_1 to R_2. Whenever a zero chip-select voltage is applied to Q_2's collector from the control logic, Q_2 conducts, and its emitter voltage changes to the TRUE level (O V).

Upon power failure, the 14-V and 10-V supplies begin to lose voltage. Transistor Q_1's base current will become zero when resistor R_3's voltage drops below about 0.7 V. At this time, voltage V equals 10.7 V–20.7 V above −10 V or 5.7 V more positive than V_{CC}—a value that still maintains the 5-V V_{CC} level. When Q_1 stops conducting, Q_2 is cut off, and the memory's chip-select input line is connected only to V_{CC} via resistor R_2. Therefore, even if V_{CC} decreases in value, the chip-select line remains at the V_{CC} potential. □

Preserving memory contents. Series multivibrator and battery (a) allow MOS random-access memory to retain data when power fails. Circuit takes advantage of MOS charge retention property so that pulsed voltage is sufficient to refresh memory. Dashed components let battery recharge when main power is restored. Protection circuit (b) for chip-select line prevents erratic logic signals from changing memory state.



One lamp can monitor battery voltage

by N.D. Thai
Huntec Ltd., Toronto, Ont., Canada

A single lamp can monitor an unregulated voltage, for instance from a battery, indicating whether that voltage is high, low, or normal. For a normal voltage, the lamp stays off; for a high voltage, the lamp stays on; and for a low voltage, the lamp flashes on and off. The low and high voltage limits are independently settable, and the flashing frequency is also adjustable.

Two complementary-MOS NOR gates perform the logic for the circuit. The voltage applied to the input of gate G_1 is AV, where A is a constant determined by the setting of potentiometer R_1. Similarly, the voltage applied to the input of gate G_2 is BV, where B is a constant determined by the setting of potentiometer R_2. Constant B is made larger than constant A.

A logic 1 is applied to both gate inputs when voltage V goes high. Voltage BV then exceeds the gate threshold voltage (V_T), or:

V is greater than $V_T/B = V_H$

where V_H represents the high voltage limit. The output of gate G_2 is low, and the lamp stays on. A logic 0 is applied at both gate inputs if voltage V goes low. Voltage AV is now smaller than the gate threshold voltage, or:

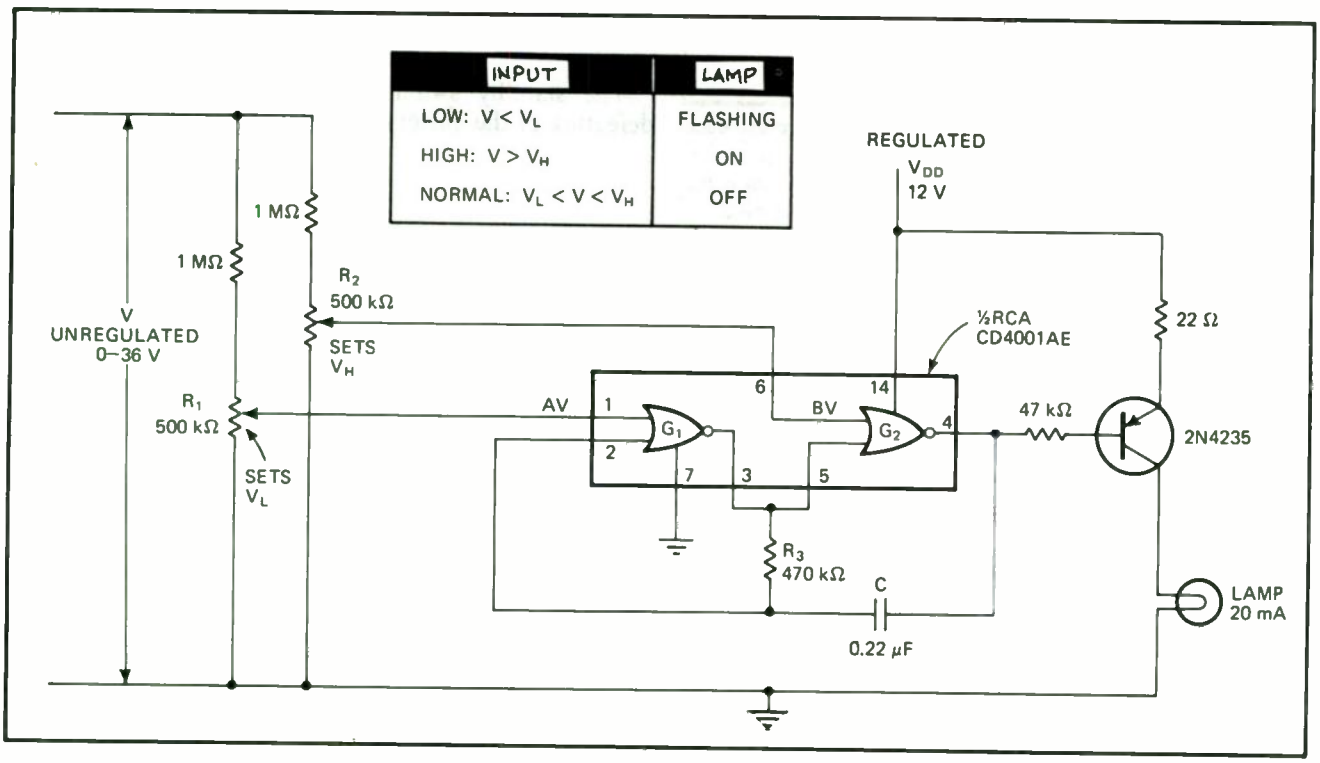
V is less than $V_T/A = V_L$

where V_L is the low voltage limit. The two NOR gates, resistor R_3, and capacitor C form a conventional astable multivibrator that drives the lamp with a square wave. The flashing frequency (assuming $V_T = V_{DD}/2$) is approximately equal to:

$f = 1/(1.4)R_3C$

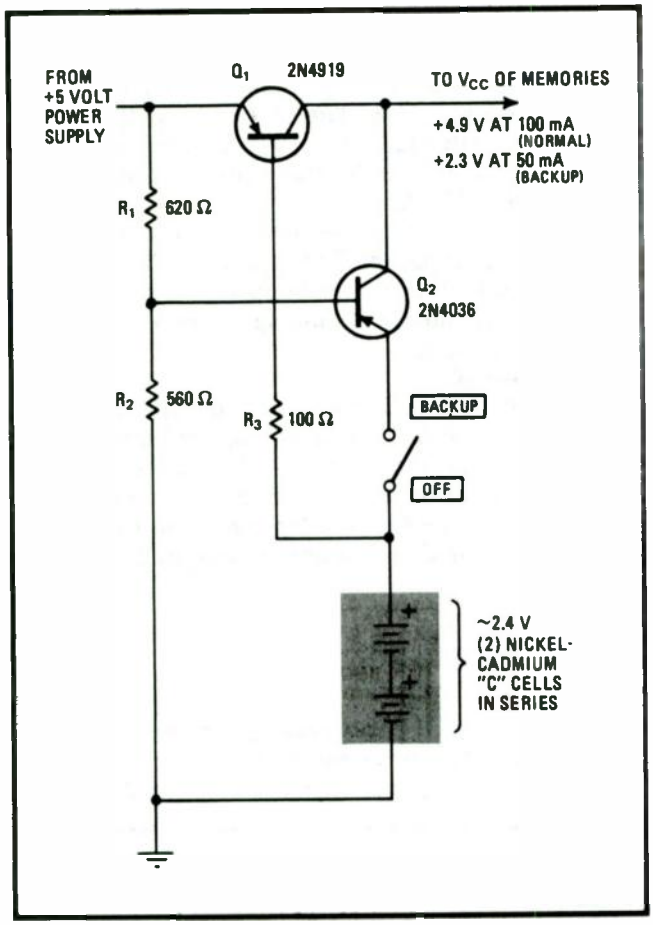
When voltage V lies between the low and high limits (that is, if voltage AV is greater than threshold V_T and voltage BV is less than threshold V_T), a logic 1 is applied to the input of gate G_1, while a logic 0 is applied to the input of gate G_2. The lamp remains off because the output of gate G_1 is low and the output of gate G_2 is high. □

Lighting the way. Single lamp indicates when unregulated (battery) input voltage is low, high, or normal by flashing, remaining on, or remaining off. The low voltage limit, V_L, is set by potentiometer R_1, the high voltage limit, V_H, is set by potentiometer R_2, and the flashing frequency is determined by resistor R_3 and capacitor C. Complementary-MOS NOR gates are used as the logic elements in this voltage monitor.



2.4-V battery backup protects microprocessor memory

by Raymond N. Bennett
Advanced Technology Laboratories Inc., Bellevue, Wash.



Memory saver. A series pair of nickel-cadmium "C" cells, each nominally rated at 1.25 volts, puts out about 2.4 volts and can deliver 2.3 volts to microprocessor memories to prevent loss of data in the event of supply failure. Transistors saturate to less than 100 mv.

Using diodes to isolate a backup battery from the power supply of microprocessor memories works fine—if the 0.7- to 1.0-volt drop across each diode can be tolerated. A more efficient circuit (see figure) substitutes saturable switching transistors that have a drop of less than 100 millivolts, which minimizes current drain and therefore extends battery life.

Moreover, the voltage of the nickel-cadmium battery supply need only be 2.4 volts, since during a power failure a saturated transistor then delivers all of 2.3 v to the memories. That is more than enough for such metal-oxide-semiconductor devices as the 2102 static random-access memory, which begins to lose data if its supply drops below about 2 v.

The circuit shown in the figure is connected between the +5-v power-supply line and the supply input of the memories. When the 5-v supply is functioning normally, transistor Q_1 is biased heavily into conduction by the difference between the supply voltage and that of the Ni-Cad batteries: 5 v − 2.4 v = 2.6 v. The voltage delivered to the memories is then about 4.9 v, since the drop across Q_1 is at most 100 millivolts. During this time, the R_1-R_2 voltage divider holds transistor Q_2 off, and the batteries receive a charge of about 20 milliamperes through R_3 and the base-emitter junction of Q_1.

When power failure occurs and the 5-v supply drops below about 3.1 v (which is 2.4 v + V_{BE}), Q_1 begins to cut off, isolating the dying 5-v supply from the load. At the same time, Q_2, biased by the R_1-R_2 voltage divider, begins to conduct, connecting the backup batteries to the load. The reverse bias on transistor Q_1 prevents the Ni-Cads from discharging through the supply circuit.

Both Q_1 and Q_2 were chosen for their very low saturation characteristics. Although their current ratings seem far in excess of what is needed, the result is that they exhibit a $V_{CE(SAT)}$ of less than 100 millivolts. But any pnp power transistors of the same general qualifications as those specified, such as the GE Powertab series, should suffice.

The standby switch has been included to permit defeating of the battery backup feature. □

Four-ampere power supply costs just $13 to build

by Joseph Ennis
Automation Industries, Inc., Vitro Laboratories Division, Silver Spring, Md.

The cost of building a regulated power supply can be lowered to around $13 if a large capacitor is used to store energy at a higher voltage than is necessary. Under normal operating conditions, the supply, which is primarily intended for powering a stereo amplifier, can deliver an output of 4 amperes at 20 volts with load fluctuations down to 18 hertz and with regulation to better than 5%.

A high-value capacitor, one measuring tens of thousands of microfarads, stores charge so that only a small amount of transformer iron is needed to produce the 4-A operating current. The resulting higher-than-required capacitor voltage is then dropped to the desired 20-V level with a transistorized series regulator. Moreover, two inexpensive incandescent lamp bulbs are used for short-circuit protection, rather than a more costly current foldback technique.

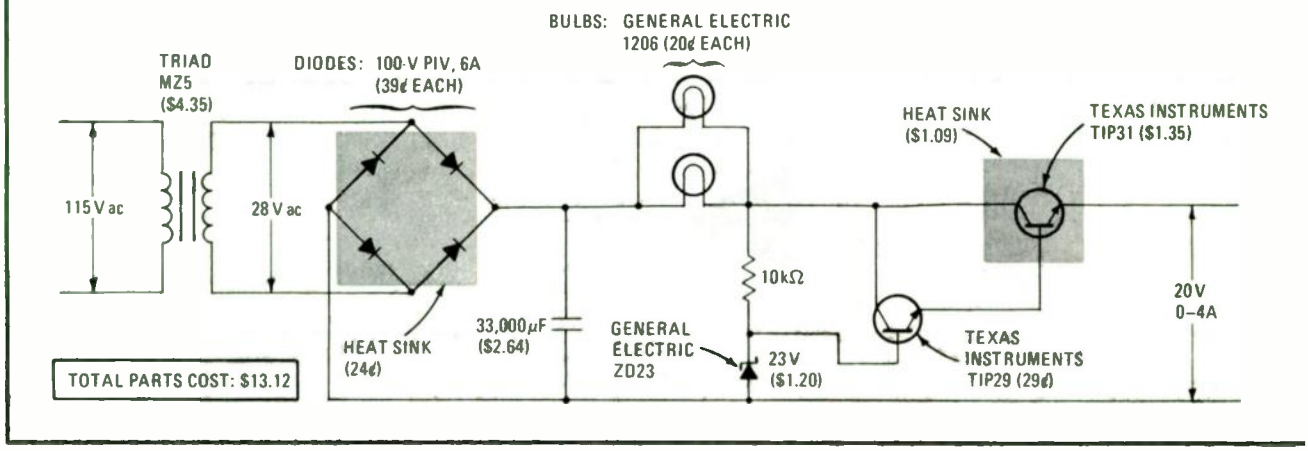
With no load at the output, the transformer charges the capacitor to about 39 V through the diode bridge. The transformer, which has a no-load secondary voltage rating of 28 V ac, can deliver the 4-A operating current but will not deliver this voltage under loading because of its core and copper losses. Although capacitor voltage may drop to around 24 V during peak loading, the series regulator will continue to provide a smooth 20-V output.

A current of more than 4 A could be controlled by the regulator transistor with the appropriate heat sinking, but the heat sink would cost more than the transistor. The heat-sink area is designed to handle only normal worst-case operating conditions and does not allow for any current foldback dissipation.

Instead, this dissipation is provided by two replacement-type automobile lamp bulbs. Besides acting as fuses when there is a short circuit at the output, they reduce the voltage drop across the regulator transistor, thereby decreasing the power it has to dissipate during normal supply operation.

To change the supply's output voltage to 15 V, the 23-V zener is replaced by a 17-V one. If a 5-V supply is needed, a transformer with a secondary voltage lower than 28 V should be selected to reduce the voltage drop that the regulator must handle. A negative-voltage supply can be constructed by substituting complementary transistor types TIP30 and TIP32 for the type TIP29 and TIP31 transistors.

Economical regulated supply. Parts cost for power supply is pared to absolute minimum by storing energy in 33,000-microfarad capacitor at higher-than-required voltage level. This allows a fairly lossy, and therefore inexpensive, transformer to be used. Incandescent lamp bulbs serve as fuses in case of a short circuit and reduce voltage seen by series-regulator transistor. Output is 20 volts at 4 amperes.



40. Programmable gain controls

Digital word sets gain of amplifier

by Craig J. Hartley
Baylor College of Medicine, Houston, Texas

Digital control of gain or attenuation is often desirable in programable systems or when the gains of many circuits have to be varied simultaneously. In the circuit shown, the gain or attenuation of an analog signal is controlled by means of a binary input. The circuit, which is similar to a multiplying digital-to-analog converter, uses a single 741 operational amplifier for gain or attenuation, plus two transistors for each control bit.

The circuit has two parts. The first is a noninverting operational amplifier; the second is a set of resistors that can be connected in parallel to produce various values for an equivalent single resistor R_C between switch S and ground.

The value of R_C is determined by the digital inputs. When the input labeled 1 is low, transistors Q_1 and Q_2 are saturated, so that the 100-kilohm resistor R is connected from switch S to ground. When input 1 is high, Q_1 and Q_2 are off, so the bottom of R is open-circuited.

Similarly, if inputs 2, 4, and 8 are low, they connect R/2, R/4, and R/8 to ground. Therefore the control inputs can be considered as a binary number with negative logic (high voltage = 0, low voltage = 1) so that the total resistance connecting the switch to ground is

$$R_C = R/N$$

where N is the value of the binary input number. For example, if N equals 5, the binary number is 0101, which means that inputs 1 and 4 are low; therefore R and R/4 are connected in parallel to provide a resistance of R/5 from S to ground.

When switch S is in position A, the gain of the op amp is

$$G_A = E_o/E_i = 1 + R_F/R_C = 1 + NR_F/R$$

The values of R_F and R are equal, so

$$G_A = 1 + N = 1, 2, 3, 4, \ldots$$

For a 4-bit control word, the maximum G_A value is 16.

When the switch is in position B, the op amp is connected as a voltage follower fed by a voltage divider, so the gain is

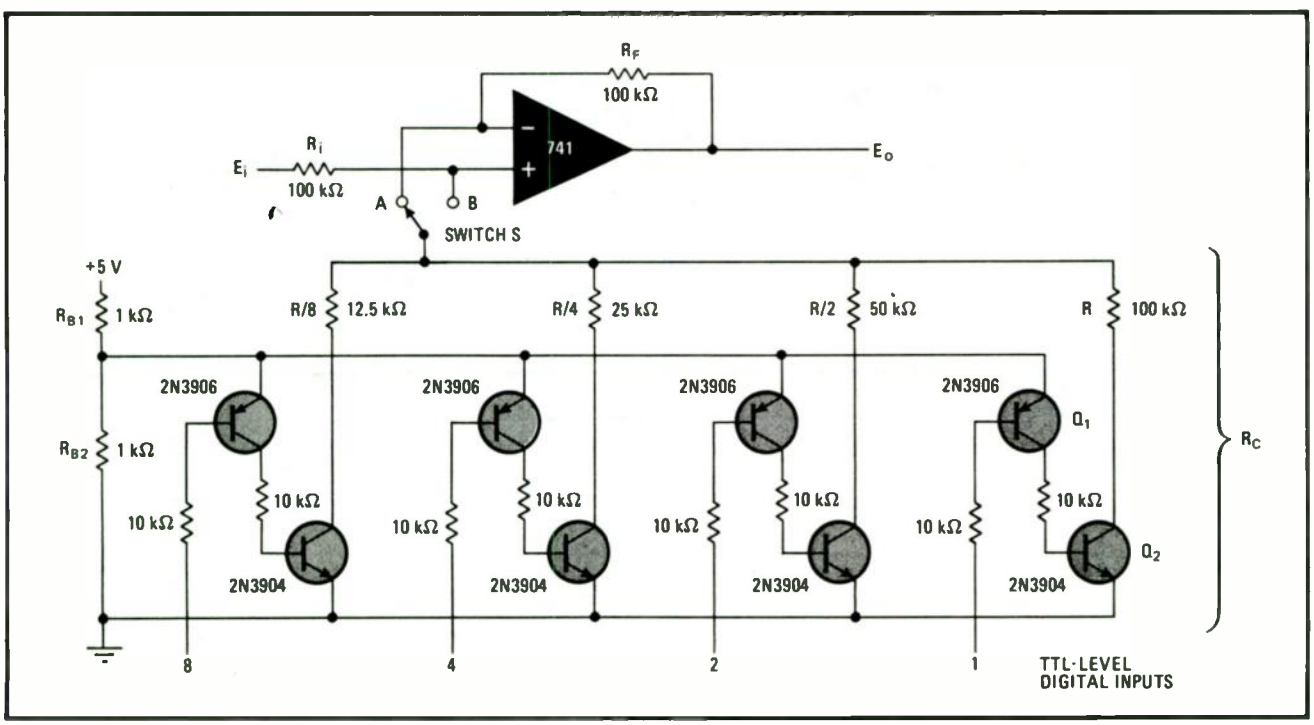
$$G_B = R_C/(R_i + R_C) = (R/N)/(R_i + R/N)$$

Because R_i is equal to R,

$$G_B = 1/(N+1) = 1, \tfrac{1}{2}, \tfrac{1}{3}, \tfrac{1}{4}, \ldots$$

Thus the circuit can amplify (switch position A) or attenuate (switch position B).

The circuit as shown will handle analog input levels



Programable gain or attenuation. The operational-amplifier circuit has a gain of $G_A = N + 1$ or $G_B = 1/(N+1)$, depending on whether switch S is set to position A or position B. The number N is the value of the negative-logic binary number applied to the digital inputs. If programable sign-reversal is required, a digitally controlled inverter [*Electronics*, March 6, p. 85] can be used in tandem with the amplifier.

of ±7 volts, and the digital inputs will accept TTL logic levels. The bias resistors and supply voltage can be varied as needed for use with other logic forms. The offset is about 0.02 v maximum in the B mode and 0.25 v maximum in the A mode and is a function of gain. Additional digits can be added for finer control. □

D-a converter forms programable gain control

by Jim Edrington
The Applied Research Laboratories, University of Texas, Austin, Texas

A monolithic multiplying digital-to-analog converter can be used with an operational amplifier to produce a simple digitally controlled amplifier. Logic voltages applied at the 10 input terminals of a converter such as the Analog Devices AD7520 control the gain. These voltages can provide 2^{10} discrete levels of amplification for an analog signal applied to the operational amplifier. The integrated circuit can handle analog signals up to ±10 volts, and the digital input levels are compatible with transistor-transistor logic and complementary-MOS.

A BCD-to-decimal decoder drives the d-a converter in the circuit of Fig. 1, giving gains as high as 60 decibels in 10 6-dB steps. The circuit requires only a few components because the multiplying converter IC contains the C-MOS switches and precision-resistor ladder network that set the gain of the amplifier.

The 741 op amp is connected as a conventional inverting amplifier, with an input resistor and a feedback resistor. As shown in Fig. 2, these resistors are elements of the d-a converter, and its control inputs determine the amount of resistance in the feedback loop.

Current from the output of the op amp that enters terminal 15 (V_{REF}) of the converter sees a resistance of R. This current, I_{REF}, divides in half at every node of a ladder network made up of resistors R and 2R. Part of this current goes to ground, and the remainder goes to the inverting input terminal of the op amp (virtual ground). In Fig. 2, since only the second control bit is high, I_F, the current fed back, is $I_{REF}/4$.

The input signal to the amplifier circuit is applied to terminal 16 of the AD7520 (the terminal marked $R_{FEEDBACK}$) because the internal resistor at this terminal matches the others in the converter. The input signal also sees a resistance of R and delivers a current equal to I_F. The gain of the amplifier circuit is

$$e_o/e_i = -I_{REF}R/I_FR = -I_{REF}/I_F$$

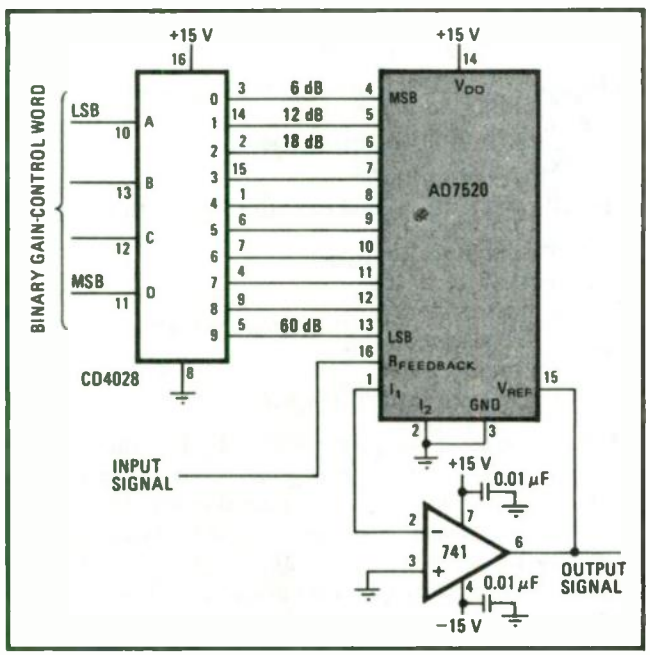
For the example in Fig. 2, where I_F is $I_{REF}/4$, the gain is –4, or 12 dB.

The input word in Fig. 1 causes only one of the AD7520's control inputs to go high. The voltage gain of the amplifier can be written as (-2^{n+1}). Expressed in decibels,

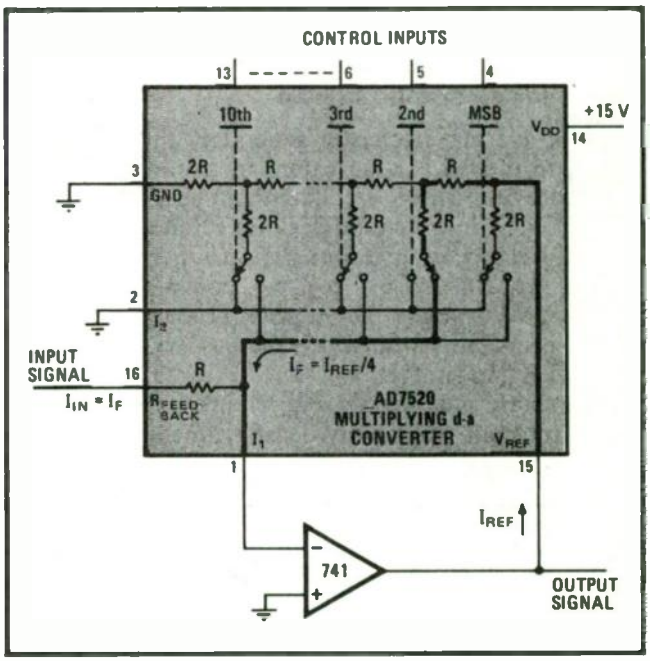
$$G = 6(n+1)\ dB$$

where n = 0, 1, . . . 9 is the value of the input word.

External resistors may be added in series or parallel at the amplifier's input to change the over-all gain or to allow input summing. Any standard op amp may be used, but fast op amps should be compensated carefully because many are unstable in low-gain configurations. □



1. Programable gain. Amplifier has gain of 6(n + 1) dB, where n is decimal value of binary-input word. Component count for circuit is low because the switches and resistors that control gain are all in AD7520 IC. Voltage levels for input logic are compatible with TTL and C-MOS, and analog input signal can be as large as ±10 V.



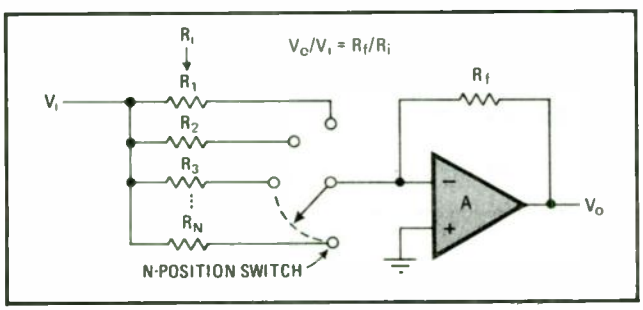
2. Resistors. Ladder network in AD7520 multiplying d-a converter provides feedback path for op amp. Current I_{REF} divides in half at every node of ladder, and switches set by control inputs determine current I_F that gets back to op amp's input terminal. Circuit gain is I_{REF}/I_F; for configuration shown, gain is –4, or 12 dB.

Combination logic cuts parts in digitally controlled amplifier

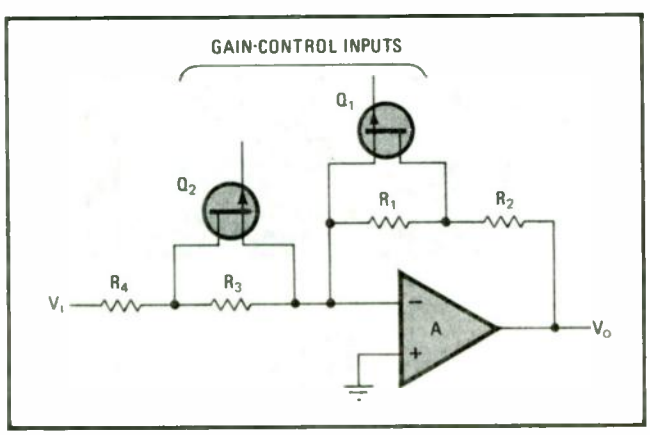
by Reinhard Metz
Bell Laboratories, Naperville, Ill.

Measurements on communications and transmission systems often require circuits that permit digital control of amplification or attenuation. These circuits may require many components when many different levels of amplification are required. However, N levels can be realized by using approximately $\log_2 N$ components in various combinations, instead of using N components without forming combinations.

A circuit arrangement that uses N different resistors to provide N different values of amplification (or attenuation) is shown in Fig. 1. The gain of the inverting operational-amplifier stage is equal to the ratio of feedback resistance, R_f, to input resistance, R_i. Here a different R_i is switched in for each desired level of gain.



1. Controllable gain. Ratio of feedback resistance to input resistance in op-amp circuit determines gain. Here N different values of R_i provide N different values of amplification (or attenuation).



2. Combinations control. Control voltages on two FETs switch R_1 and R_3 in or out of circuit in four possible combinations, providing four different values of gain. These values of gain, when expressed in dB, obey a simple rule: the sum of the highest and lowest is equal to the sum of the middle two. An amplifier can therefore be designed to provide equal increments of dB gain (or loss).

The technique of using various combinations of a set of resistors is shown in its basic form in Fig. 2. Using one op amp and four resistors, but only two field-effect transistors, this stage provides four digitally controllable gain values. The four on- and off-state combinations of the control inputs to the two FETs determine four possible values for the ratio of feedback resistance to input resistance in the inverting amplifier configuration, and thus determine the four values of gain and/or loss. The sources of the FET are at virtual ground, and therefore signal fluctuations cannot affect their on-off states. Also, no switch-drive decoding is required because there are already only two switches for four levels.

The four values of amplification or attenuation through the circuit in Fig. 2 obey a useful relationship: if a, b, c, and d are the gains or losses expressed in decibels, the sum of the highest and lowest is equal to the sum of the other two. To demonstrate the relationship, let

$$a = 20 \log \frac{R_1 + R_2}{R_4}, \text{ or } \frac{R_1 + R_2}{R_4} = 10^{a/20}$$

$$b = 20 \log \frac{R_1 + R_2}{R_3 + R_4}, \text{ or } \frac{R_1 + R_2}{R_3 + R_4} = 10^{b/20}$$

$$c = 20 \log \frac{R_2}{R_4}, \text{ or } \frac{R_2}{R_4} = 10^{c/20}$$

$$d = 20 \log \frac{R_2}{R_3 + R_4}, \text{ or } \frac{R_2}{R_3 + R_4} = 10^{d/20}$$

Multiplying the first equation by the last yields

$$\frac{R_1 + R_2}{R_4} \quad \frac{R_2}{R_3 + R_4} = 10^{(a+d)/20}$$

and multiplying the second equation by the third yields

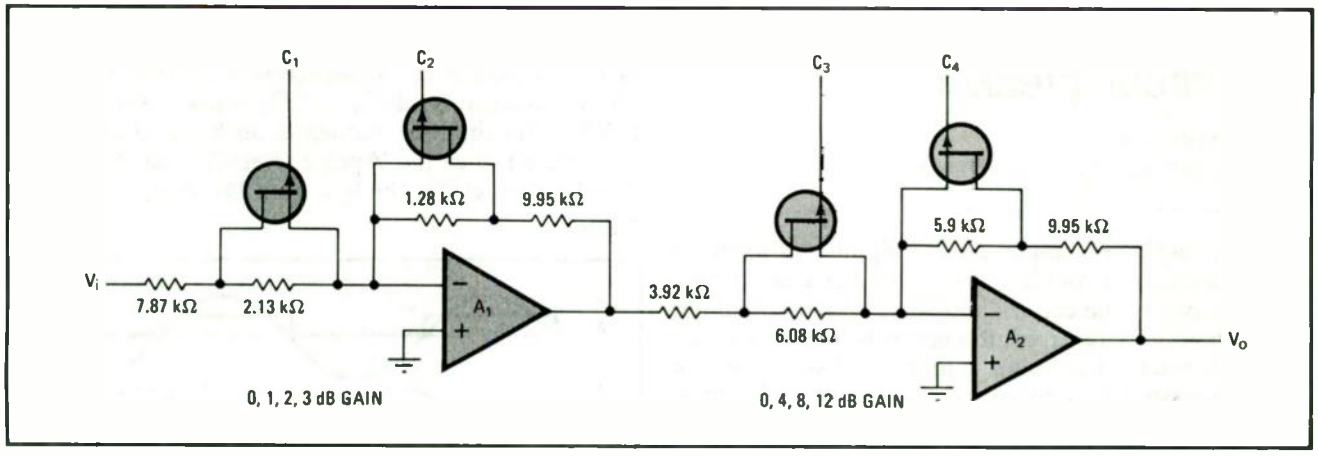
$$\frac{R_1 + R_2}{R_3 + R_4} \quad \frac{R_2}{R_4} = 10^{(b+c)/20}$$

The left sides of these two expressions are equal, and therefore

$$10^{(a+d)/20} = 10^{(b+c)/20} \text{ or } a + d = b + c$$

Thus, for any set of resistors R_1, R_2, R_3, and R_4, the sum of the highest and lowest gains or losses (expressed in dB) is equal to the sum of the middle two. In particular, this relationship is satisfied by any "symmetrical" set of gains, such as 0, 1, 2, 3 dB, or −10, −5, +5, +10 dB. Also, any equal-stepped set of gains or losses is symmetric.

A cascade of s stages, controlled by only 2s digital inputs, can extend controlled amplification/attenuation to any desired set of 4^s symmetrically spaced dB steps. Figure 3 shows a two-stage amplifier in which the gain is adjustable from 0 to 15 dB in 16 1-dB steps. The values of the resistors are calculated directly from the



3. More steps. Cascade of two symmetrically stepped stages provides 4^2 values of gain, with only 2 × 2 control terminals. Levels in each stage are chosen so that gain is adjustable from 0 to 15 dB in 16 1-dB steps. More generally, cascading s stages, controlled by only 2s digital inputs, can provide any desired set of 4^s symmetrically spaced steps of dB amplification or attenuation.

equations for a, b, c, and d, with the unity gain (0 dB) set at

$$\frac{R_3 + R_4}{R_2} = \frac{10\,k\Omega}{10\,k\Omega} = 1$$

The approximately 50-ohm on resistance of a FET is taken into account by increasing the R_4s and R_2s, and decreasing the R_1s and R_3s from the calculated values.

Although Figs. 2 and 3 show 4^s different values of gain, where s is the number of stages, 2^s can be easily achieved by including one stage with only two values of gain if one value of gain in each stage is 0 dB. □

41. Protection circuits

Phase-sequence detector trips circuit breaker

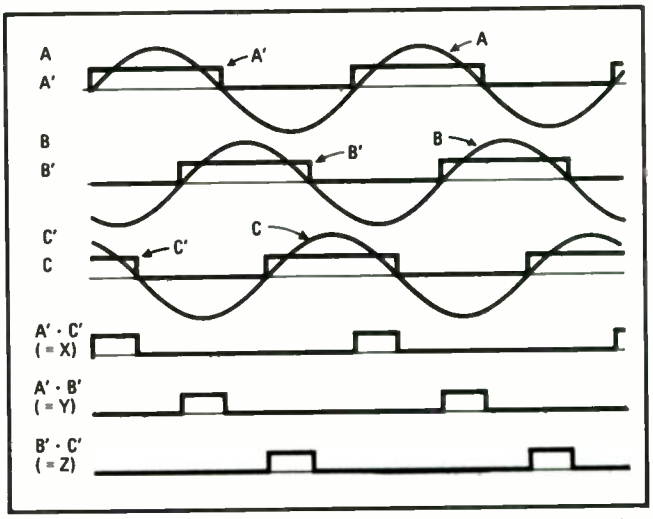
by Terry Malarkey
Motorola Semiconductor Products Inc., Phoenix, Ariz.

Some three-phase line-powered equipment is sensitive to the direction of rotation of the three phases. For example, if two of the connections to a three-phase motor are inadvertently reversed, the motor will reverse direction—a disaster if the motor is used to drive a pump or the compressor of an air conditioner. To guard against this failure, a low-power circuit can be built from standard complementary-MOS components that will detect the phase inversion and trigger a circuit breaker. Moreover, the circuit, which interfaces directly with C-MOS logic, can be appended easily to a line-undervoltage or line-unbalanced detector.

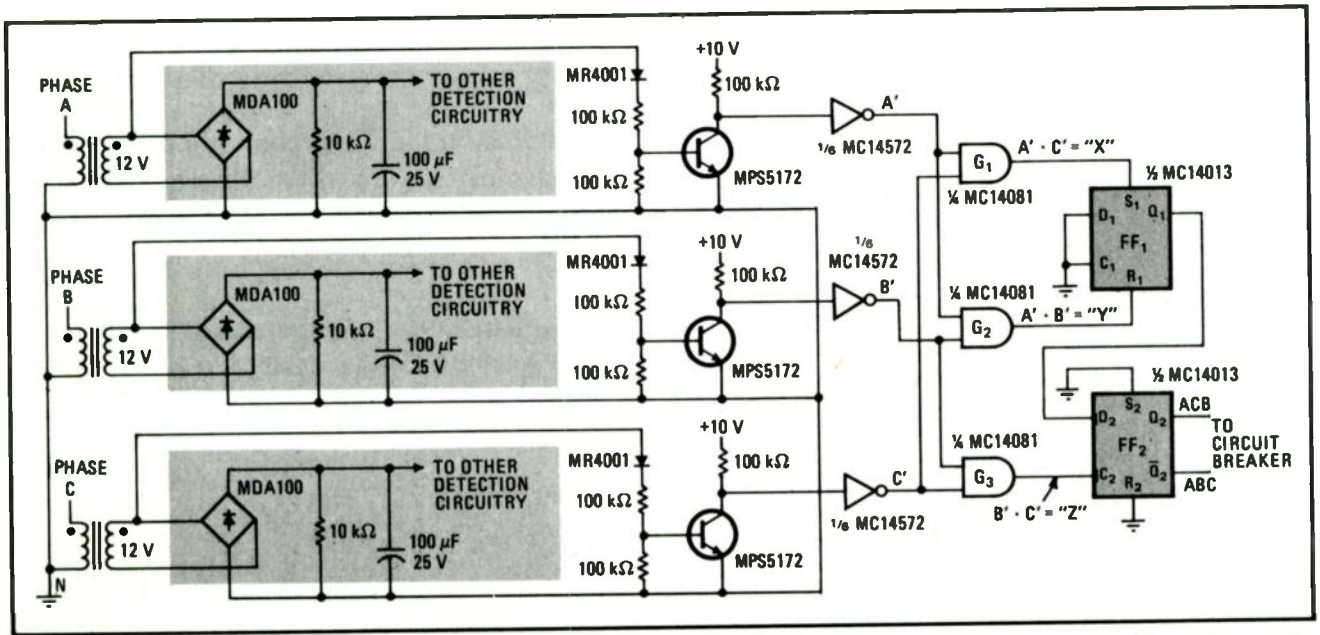
In the circuit (Fig. 1), the line voltages are stepped down and isolated by control transformers. The sine waves for phases A, B, and C are half-wave-rectified and shaped by the MR4001 diode and MPS5172 transistor, and shaped again by a C-MOS inverter. The resulting rectangular waveforms are shown as A′, B′, and C′ in Fig. 2.

The shaped outputs A′, B′, and C′ are now combined with one another in the AND gates G_1, G_2, and G_3, to produce the waveforms A′•C′, A′•B′, and B′•C′ (or X, Y, and Z in Fig. 2). The pulses X, Y, Z appear sequentially; this sequence will change to YXZ if, for instance, the B and C phases are interchanged.

The X, Y, and Z pulse trains are applied to D-type flip-flops FF_1 and FF_2 in such a way that the $\bar{Q}_2$ output of FF_2 is high if the sequence is XYZ (i.e., if the line phase sequence is ABC), and $\bar{Q}_2$ is low if the sequence is YXZ. For the XYZ sequence, an X pulse sets Q_1 and D_2 high, but then the Y pulse resets Q_1 and D_2 low. The Z pulse then clocks the low from D_2 to Q_2, making $\bar{Q}_2$ high.



2. Operation. Line phases A, B, and C are rectified and shaped to produce waveforms A′, B′, and C′. Overlaps of these rectangular waves produce AND-gate outputs A′•C′, A′•B′, and B′•C′; for convenience these outputs are referred to as X, Y, and Z. Line-phase sequence ABC generates XYZ; sequence ACB generates YXZ. These pulse trains cause flip-flop outputs to signal any phasing error.



1. Phase Insurance. Incorrect sequence of line phases is detected by flip-flops, which trigger circuit breaker to prevent three-phase motor from running in reverse. Phase sequence ABC makes $\bar{Q}_2$ high, but sequence ACB makes Q_2 high; either output can be used to control protection devices. This phase-reversal detector can be a simple addition to other control circuitry, as shown here.

Either Q_2 or $\bar{Q}_2$ can be used to trip a circuit breaker via a solid-state or electromechanical relay, and thus pull a valuable piece of equipment off the line before it is damaged.

The MDA100 bridge rectifier, 10-kilohm resistor, and 100-microfarad capacitor, shown in the gray area of Fig. 1, are representative of typical applications requiring line-voltage detection. They are included in Fig. 1 to demonstrate how easily the phase-sequence detector can be added to other detection circuitry. They can, of course, be omitted; and the "bottom" of the transformer can be connected directly to circuit ground. □

Current and power limiter protects switching transistor

by R.M. Stitt
Burr-Brown Research Corp., Tucson, Ariz.

Although a switching transistor dissipates little power in normal operation, it must be protected from destructive current and power overloads. Current-limiting alone is not sufficient protection; power-limiting is also necessary. But fortunately, a few components can be added to conventional current-limiting circuitry to provide power-limiting. A voltage rise across a transistor is sensed and used to cut down the drive current.

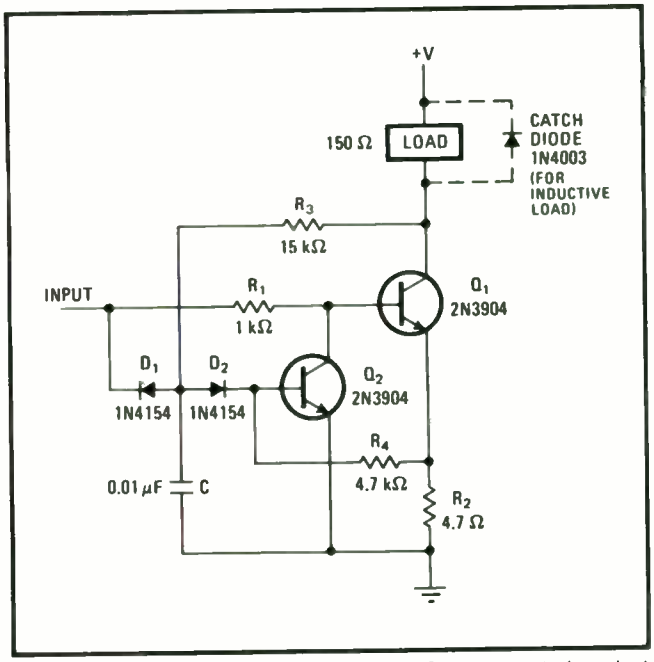
To understand why current-limiting alone fails to provide adequate protection, consider a switching transistor controlling a 100-ohm load connected to a 100-volt supply. The power dissipated in the load might be about 100 watts, but the maximum power dissipated in the transistor is merely the load current times the transistor's saturation voltage (if switching losses are neglected). The load current is about 1 ampere, so the transistor dissipates less than 1 W. A designer might use a 3-W device and provide a current-limiting level of 1.5 amperes.

Suppose, however, that the load is short-circuited so that the collector of the switching transistor is connected directly to the 100-V supply. Then the transistor dissipates 150 W, which destroys it.

To prevent this destruction, a power-limiter is required. Power-limiting can be added to a standard current-limiter by use of only four simple components. In Fig. 1, Q is the switching transistor, and the conventional current-limiter is formed by Q_2, R_2, and R_4. The power-limiter consists of capacitor C, diodes D_1 and D_2, and resistor R_3. To illustrate the operation of the circuit, assume that Q_1 is saturated and in normal operation. As the load current increases, the voltage drop across R_2 increases, turning on transistor Q_2 and thus shunting drive current away from the base of Q_1. Therefore, Q_1 begins to come out of saturation, so its collector voltage rises. This voltage across Q_1 further turns on Q_2 through R_3 and regeneratively turns off Q_1.

Diodes D_1 and D_2 form a switch so that the collector voltage of Q_1 is sampled only when its input is high. This switch also resets the power-limiting circuitry with each cycle of the input. The value of capacitor C is chosen to give the power-limiting portion of the circuit a turn-on delay, allowing time for Q_2 to become saturated. This delay also permits higher current transients to flow during switching, such as those that might occur in a switching regulator in which the catch diode must be discharged during each cycle.

The current-limiting portion of the circuitry is active at all times, protecting the switching transistor from current overloads. The circuit was set up to be driven by a TTL-level signal and to switch a 100-mA load at 400 Hz to +15 V. The protection circuit can easily be modified for nearly any input and output configuration. If a pnp-transistor switch is to be protected, transistor Q_2 should also be a pnp, and the polarities of D_1 and D_2 should be reversed. □



Two-way protection. Switching transistor Q_1 is protected against excess current and/or excess power dissipation. If load current approaches limit, IR_2 drop turns on transistor Q_2 to shunt base drive from Q_1. A voltage rise across Q_1 acts through R_3 to turn on Q_2 and turn off Q_1. Capacitor C provides delay that allows Q_2 to saturate with each new cycle, and lets power-limiter ignore transient high currents. Diodes D_1 and D_2 reset power-limiter when input is low.

Diodes switch high power to protect sonar receiver

by F. E. Hinkle
Applied Research Laboratories, The University of Texas, Austin, Texas

A sonar system that uses the same transducer for both transmission and reception must include a transmit/receive (T/R) switch. This switch protects the sensitive receiving amplifiers from the high-power pulses applied to the transducer elements during the transmission phase. It also prevents the transmitter circuit from degrading the returned signal during the receiving phase.

In the solid-state switching network described here, pairs of diodes perform the transmit/receive switching automatically, without any extra driving or timing circuits. They are simply driven by high signal voltages into conduction during transmission and lapse into nonconduction during reception. This system transmits kilowatts of power efficiently and is adaptable to various numbers of transducer elements.

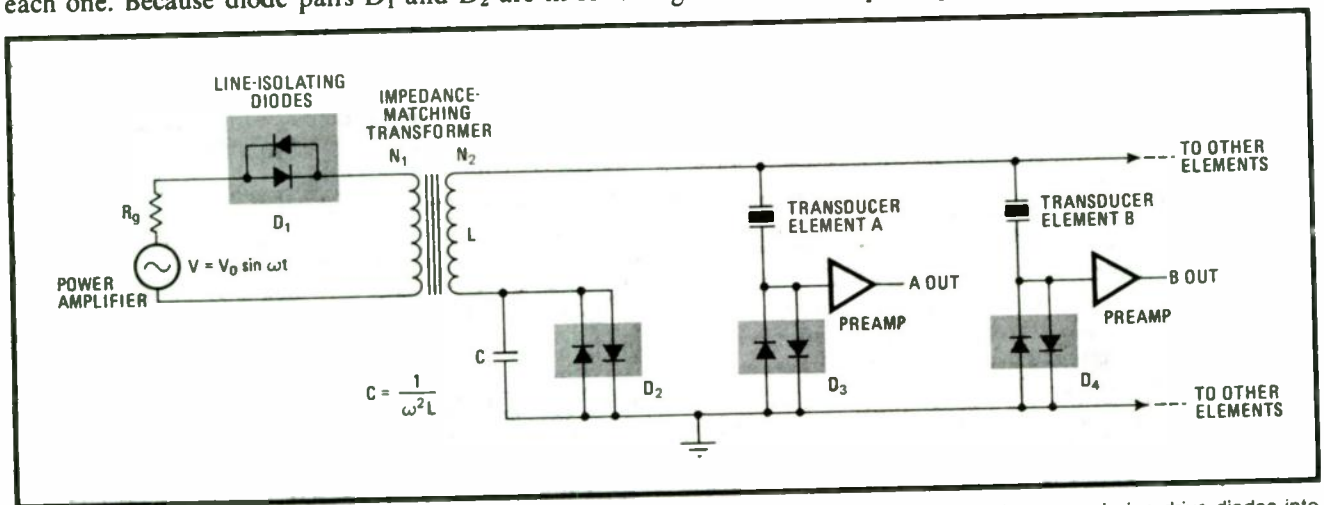
Figure 1 shows the circuit of the automatic solid-state transmit/receive switch. A transformer matches the impedance of the power amplifier to the impedance of the transducer load. Diode pairs D_1, D_2, D_3, and D_4 are placed in the circuit to pass the high currents and voltages that are present when the transducer is used for signal transmission. When the voltage is greater than 1 volt peak-to-peak, the diodes conduct and therefore appear to be short circuits.

Figure 2a shows the equivalent circuit during the transmission phase. Note that all transducer elements are in parallel, so that the same voltage is present across each one. Because diode pairs D_1 and D_2 are in series with the primary and secondary of the transformer, respectively, they must be able to carry the full source and load currents during transmissions. Diode pairs D_3 and D_4 need to carry only the currents that flow through transducer elements A and B, respectively. Diodes D_3 and D_4, acting as short circuits, protect the preamplifiers from the kilovolt-level voltages during the transmission phase.

At the end of the high-power transmitter pulse, all of the diodes stop conducting. Pulse echoes that return to the transducer elements generate only millivolt-level signals, so all of the diodes act as open circuits. (In reality, the diodes look like small capacitors—typically less than 100 picofarads.)

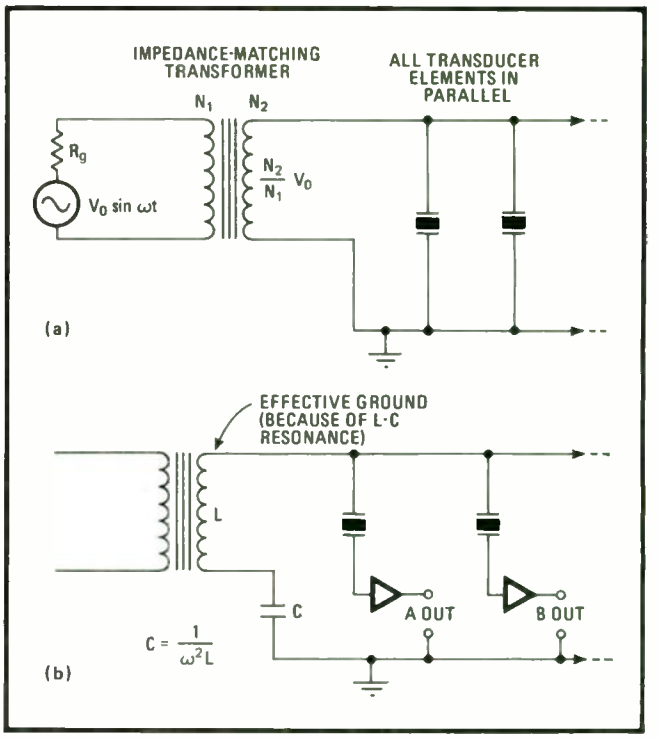
Figure 2b shows the ideal equivalent circuit of the system in this receiving condition. Note that capacitor C is made series-resonant with the secondary of the transformer, i.e., $C = 1/\omega^2 L$ where ω is the angular signal frequency and L is the inductance of the transformer secondary coil. This LC resonance, by creating an effective ground at the common side of all of the transducer elements, prevents crosstalk between them. The preamplifiers are connected to the other side of each element, and each amplifies only the signals from the element it is connected to. Because each element has its own amplifier channel, directional reception can easily be optimized by giving different gains, or weights, to each element. Diode pair D_1 open-circuits the primary side of the transformer to keep noise from entering the effective ground circuit from the power amplifier during the receive mode.

In the system, this transmit/receive technique is used to drive 5 kW into a transducer, which has 16 different elements that all have different gains during the receive mode. A directional receiving beam pattern is formed by summing the signals from all of the elements together after the preamplifier. If it is also necessary to



1. Self-controlled. Automatic solid-state transmit/receive switch uses pairs of diodes. High voltages during transmission drive diodes into conduction so that they appear as short circuits. Low voltages during reception leave diodes nonconducting so that they appear as open circuits. Capacitor C resonates L so that common sides of all transducer elements are grounded during receive mode.

2. T and R equivalents. With diodes short-circuited by high voltages that occur during the transmit phase (a), all transducer elements are in parallel and have equal voltages. During the receive phase (b), the diodes act as open circuits. Each element's signal is amplified separately, so that a directional beam-reception pattern can be formed by controlling the weight (i.e., amplifier gain) for each signal.



weight the elements separately during transmissions, several transformers can be employed to give different drive voltages across the elements.

The diodes used in the working circuit are the 1N3899 and the 1N3899R, which differ only in polarity. These 20-ampere units are stud-mounted for convenient installation and heat-sinking. For signal frequencies on the order of 10^4 hertz, the value of capacitor C is about 0.01 microfarad; because it is shunted by diode pair D_2, it does not need a high voltage rating and therefore can be mica or ceramic. The preamplifiers are type 739 operational amplifiers.

Since the transmit/receive switch does not use relays, no settling time is required prior to transmission. With no moving parts, this transmit/receive switch is quiet, efficient, and very reliable. Power limitations are defined largely by the current capabilities of diode pairs D_1 and D_2 together with the transformer. □

Sensing resistor limits power-supply current

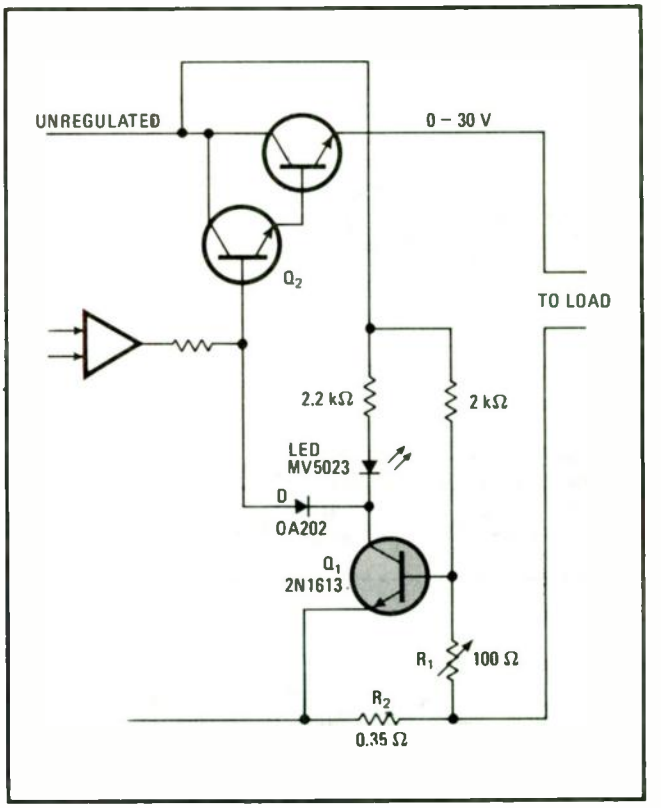
by Theo W. Smit
Euratom, Ispro, Italy

To protect a power supply against the excessive currents that would flow if the load were short-circuited, a simple drive-shunting transistor controlled by a sensing resistor is all that is necessary. As described here, the protection circuit is adjustable and includes an indicator light to warn of the current-limited condition.

The schematic diagram shows the current limiter connected in a 30-volt/2-ampere power supply. If adjustable resistor R_1 is set at zero, then the load current is limited to 2 A. If the current exceeds this level, the voltage drop across R_2 turns on transistor Q_1, which sinks the input current to driver transistor Q_2. Thus the load current is limited to the 2-A level.

If R_1 is set greater than zero, Q_1 turns on at a current less than 2 A, limiting the load to this reduced level.

The light-emitting diode lights up when Q_1 conducts, indicating that the current limiter is in operation. Diode D prevents the LED from lighting if Q_1 is off. □



Protective limiter. To limit current in power-supply circuit, voltage drop across resistor R_2 turns on transistor Q_1 when load current exceeds 2 amperes (current value will be lower if R_1 is greater than 0 ohm). Q_1 then shunts drive current away from Q_2, reducing current to the load. LED turns on to indicate conduction in Q_1.

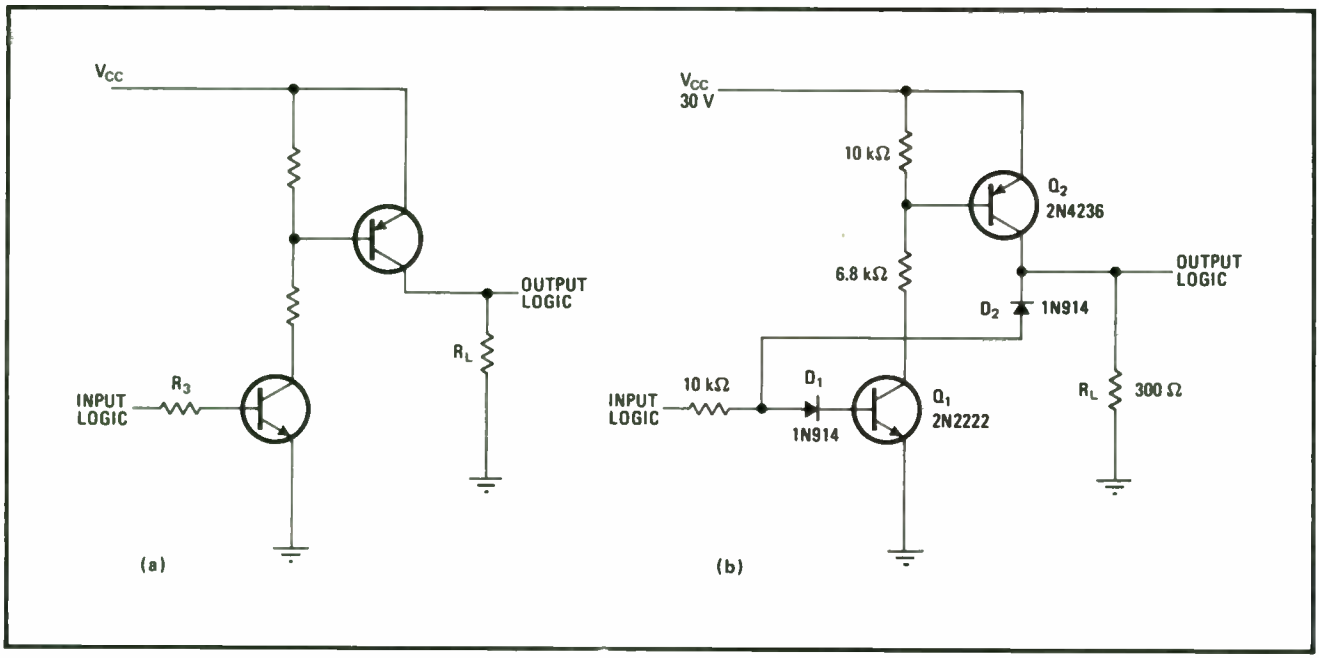
Two diodes protect logic-level translator

by P. R. K. Chetty
Indian Scientific Satellite Project, Bangalore, India

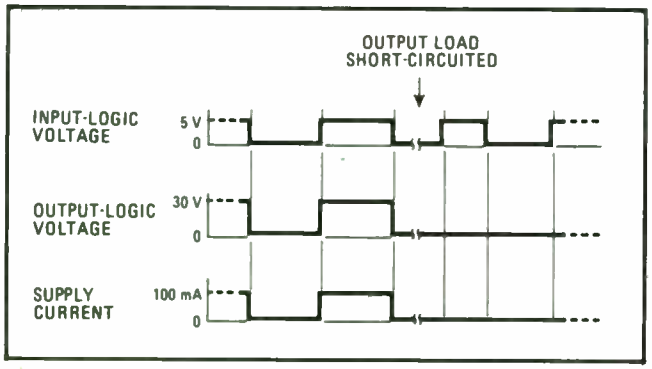
A level translator is used to interface between two circuits that operate at different logic levels. But the translating transistor (or level-up transistor) is often burned out when its load is accidentally short-circuited to ground. The addition of two diodes to the conventional level-up circuit can protect the transistor. Even a transistor that operates at 30 volts (as well as those meeting lower voltage requirements) can be safeguarded by the circuit modification described here.

The conventional translation circuit (or logic level-up circuit) is shown in Fig. 1(a), and a modified version with two protection diodes added is shown in Fig. 1(b). The component values shown are chosen to provide a normal load current of about 100 milliamperes. In normal operation, when the input logic is high (logic 1), diode D_1 is forward-biased; Q_1 is turned on, and therefore Q_2 is turned on. Diode D_2 is reverse-biased, so the output-logic voltage across the load is nearly V_{CC}. When the input logic is low (logic 0), the transistors are turned off, and the output logic is zero.

If the output load is shorted to ground when the input is a logic 1, the anode of D_1 is above ground only by the amount of the forward-voltage drop through D_2. This voltage is not great enough to let Q_1 conduct because a voltage of at least two diode drops, V_{D1} and V_{BE}, would be required to turn on Q_1. Therefore Q_1 is turned off, and, as a result, transistor Q_2 is turned off too, which prevents it from conducting a destructive current straight to ground. The circuit remains shut down as long as the load is short-circuited, and it returns to normal operation when the short is removed.



1. Protection. Conventional logic-level translator shown in (a) is modified by addition of two diodes in (b). Diodes protect translation transistor Q_2 from destructive current that would otherwise flow if load resistor were short-circuited. Diodes turn off both transistors, so no current is drawn from supply while load is shorted. In normal operation, load current of about 100 milliamperes is unaffected by diodes.



2. Waveforms. During normal operation of the logic-level translator, the output voltage and the current from the V_{CC} supply go on and off as the input logic goes high and low. If output load is short-circuited, diodes turn off transistors so that no currents flow.

Levels of input-logic voltage, output-logic voltage, and current from the high-voltage supply are shown in Fig. 2 for both normal operation of the circuit and the short-circuited-output condition. No current is drawn from the V_{CC} supply while the load is grounded. □

Digital transient suppressor eliminates logic errors

by Christopher Strangio
Villanova University, Villanova, Pa.

In digital systems, switching transients occur most often when there is a transition from logic 0 to logic 1 or from logic 1 to logic 0. These transients can introduce errors if their amplitude is large enough to exceed the logic 0 maximum voltage or the logic 1 minimum voltage. Errors are particularly likely to occur at mechanical-to-electrical couplings, as in switches and relays.

The simple digital circuit in the diagram can eliminate these unwanted transients. Initially, the input is low, and the latch and the two monostable multivibrators, MM_1 and MM_2, are reset. On the first positive-going edge at the input, gate G_1 is enabled, triggering MM_1 and making its Q output go high. This sets the latch so that gate G_1 becomes inhibited and the output goes high. Since gate G_2 is also inhibited after MM_1 is triggered, the input is now blocked both from the latch and from the two monostables. After the first positive-going edge, then, any positive-going transients at the input will have no effect on the output.

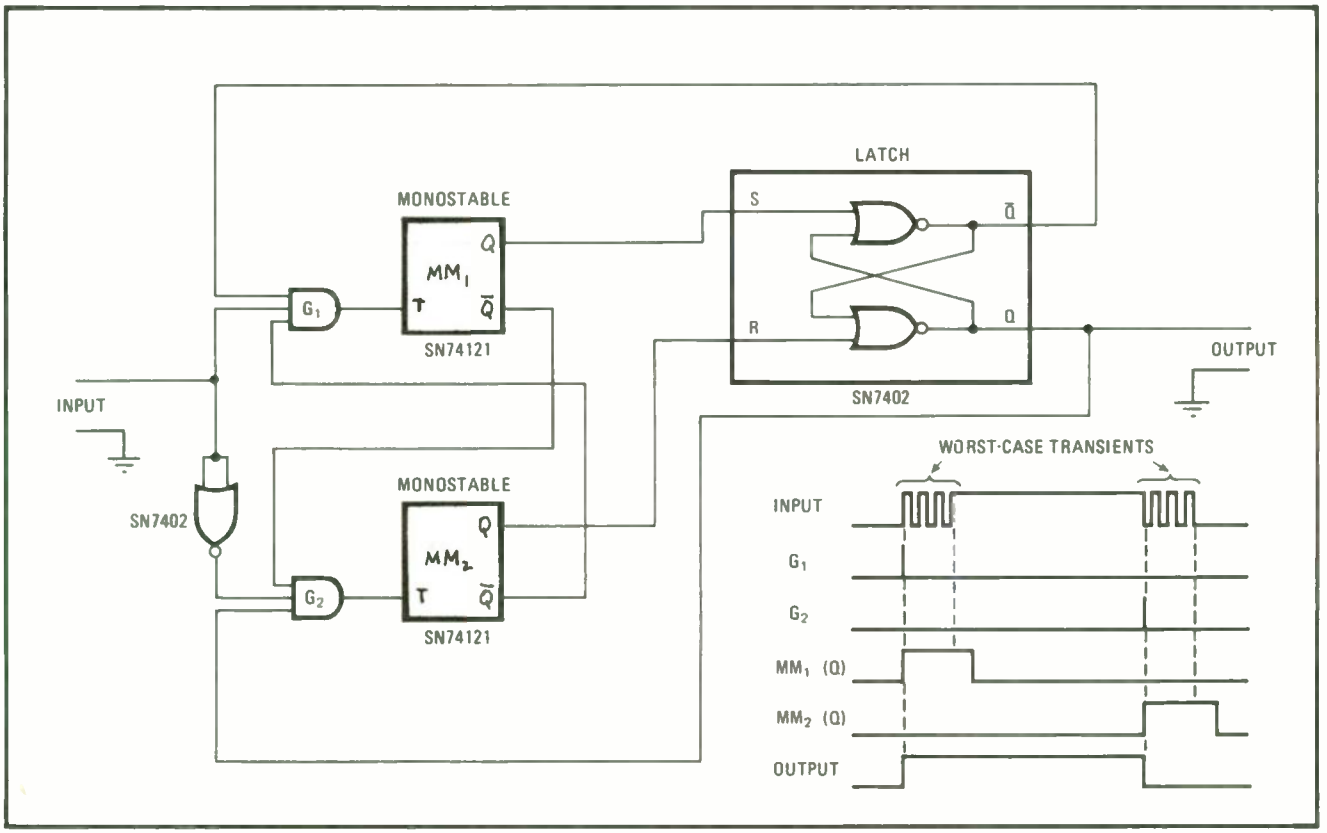
The period of monostable MM_1 determines how long positive input transients are prevented from affecting the state of the output. This period should be adjusted to be slightly greater than the longest possible turn-on transient. When the Q output of MM_1 goes low at the end of the timing period, the next negative-going input transition enables gate G_2, triggering monostable MM_2 and resetting the latch so that the output goes low.

As long as the input remains high, the latch stays set and the output will continue to be high. The first negative-going edge at the input enables gate G_2, causing the Q output of monostable MM_2 to go high. This resets the latch so that gate G_2 becomes inhibited and the output goes low. Since gate G_1 also becomes inhibited once MM_2 triggers, the input is again blocked. All negative-going transients will now be prevented from changing the output logic state.

The period of monostable MM_2 establishes the length of time negative transients at the input are stopped from reaching the output. The monostable timing period should be slightly greater than the longest possible turn-off transient. The output will remain low after the timing cycle of MM_2 is complete, provided that the input remains low.

With the components shown, this digital transient suppressor will be triggered by transients as short as 85 nanoseconds. The circuit can be adjusted to block transients that are between 100 ns and 2 seconds wide, occurring after the initial leading or trailing edge at the input. Voltage excursions below 0 volts are handled by the clamping diodes found in most TTL packages; excursions above 5.5 V may be clipped with a zener. □

Transient suppressor. Both positive-going and negative-going logic transients are prevented from causing output errors by this digital suppressor circuit. Timing period of monostable MM_1 fixes the maximum width of positive transients that will be blocked, while the period of monostable MM_2 determines the maximum width of negative transients. The timing diagram shows waveforms for several key circuit points.



Voltage regulator protects logic pull-up transistors

by Stephen F. Moore
Resdel Engineering Corp., Arcadia, Calif.

A monolithic three-terminal voltage regulator and a Norton-type operational amplifier can provide excellent short-circuit protection—particularly for the transistor that's providing active pull-up at the output of a logic circuit.

All too often, transistors operated in this way are destroyed when the logic output is inadvertently shorted to ground. Sometimes, too, protecting these transistors is further complicated because the logic must be run at 28 volts. An easy solution would appear to be a current regulator. But most current limiters have one of two drawbacks—either they introduce an unacceptably large voltage drop, or they create excessive heat in biasing resistors.

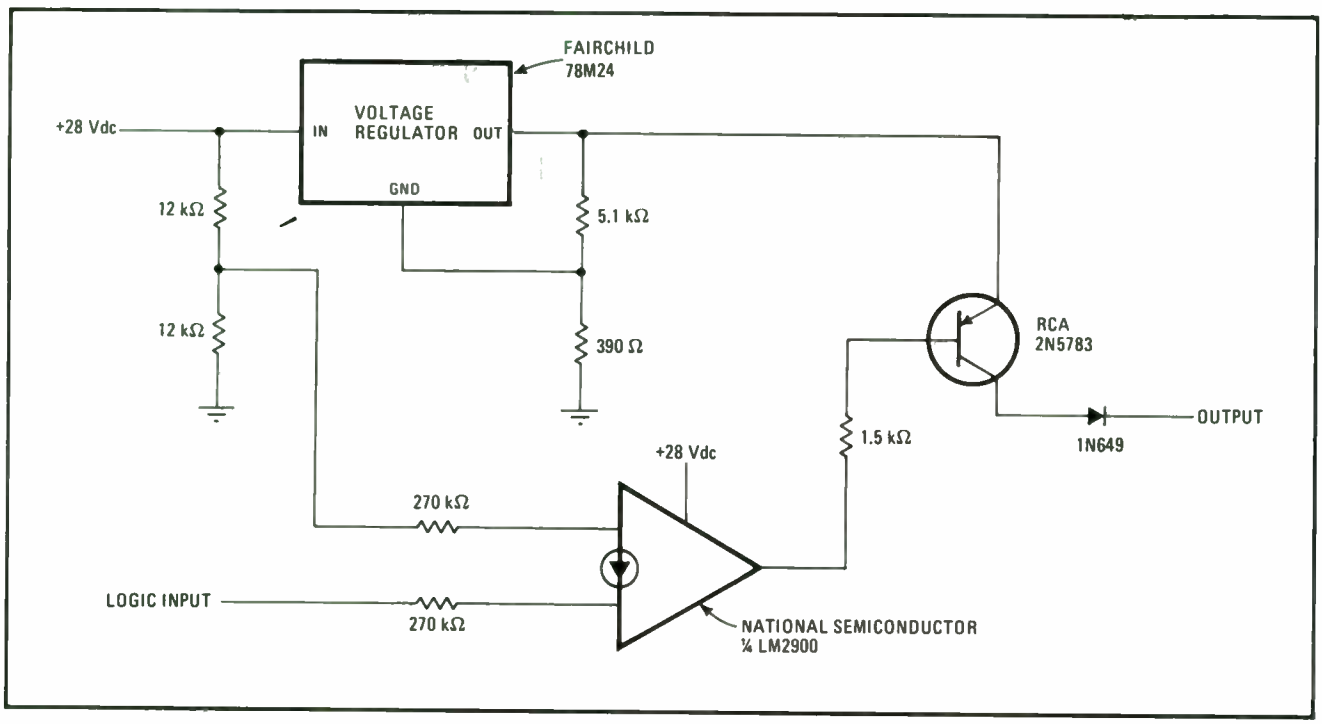
A monolithic three-terminal voltage regulator, however, has neither defect. When the regulator is not overloaded, the voltage drop across the device is only about 1.5 v. When it is overloaded, the heat it creates remains within an acceptable range. Usually, the highest output voltage that one of these regulators can supply is 24 v. But, if the device's ground terminal is biased at 2 v (depending on the manufacturer's recommendations), the output of a 24-v regulator can be increased to 26.5 v.

When connected as shown, the regulator provides current limiting in two ways. Through its internal circuitry, it acts as a surge-current limiter of about 2 amperes. It also operates as a thermal-current limiter that reduces that output voltage when the current demand becomes excessive. This keeps the power dissipated in the regulator from exceeding the maximum allowable limit. Here, the thermal-current limiting will start at around 400 milliamperes.

Limiting the current available for the active-pull-up transistor will prevent the transistor from being destroyed as long as it is kept in saturation or in cutoff. A Norton amplifier allows both these conditions to be met—its current-sinking capability is greater than 30 mA, and it has an active pull-up in its output circuit. Because of the voltage drop across the regulator, this active pull-up creates a reverse bias on the transistor being protected, eliminating the need for the transistor's pull-up resistor. Also, a Norton amplifier will work reliably with a single-ended power supply at, as well as above, a supply voltage of 28 v.

The diode at the output of the circuit protects the transistor from overvoltages. For example, this diode will guard against an overvoltage caused by an inductive kickback that could forward-bias the base-collector junction of the transistor. □

Guarding against short circuits. An IC voltage regulator and a Norton amplifier keep this active-pull-up transistor from being permanently damaged if the input logic signal is mistakenly shorted to ground. The regulator provides both surge-current limiting and thermal-current limiting. The Norton amplifier keeps the transistor either fully saturated or fully cut off, and the output diode protects against overvoltages.



Power-failure detector is good for short lapses

by K.C. Seino,
Fermi National Accelerator Laboratory, Batavia, Ill.

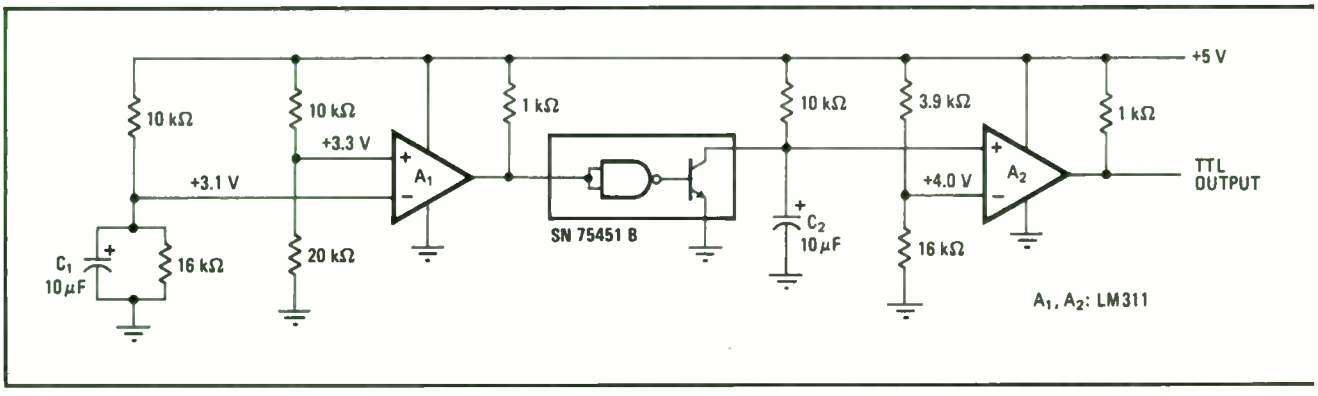
A power-failure-detection circuit for a digital system should be reliable for any interruption, whether it lasts for milliseconds or hours. It should also produce reset and restart timing pulses. The conventional power-clear circuit, which consists of a gate with an RC delaying network at its input, works well for power failures of long duration, but not after a momentary failure. Nevertheless, the system must still be reset and checked before it is restarted.

Two voltage comparators and an open-collector gate can be the basis of such a circuit as shown in Fig. 1. The diagram shows the LM 311, which can be operated with only a +5-volt power supply, and the peripheral driver SN 75451 B, useful because of its small physical size. But any comparator or open-collector gate with the proper specifications can be used.

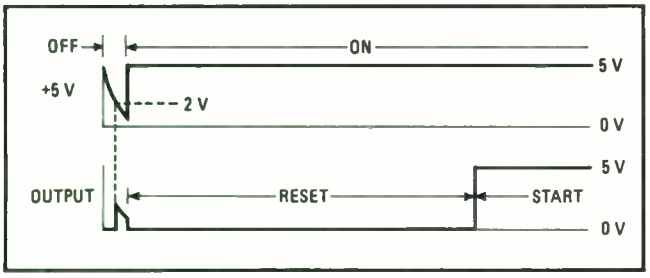
When power is present, the (+) input of comparator A_1 stays higher than the (–) side, and the output is high. The NAND gate inverts the level, cutting off the transistor. As soon as power starts to go down, the (+) input, nominally at 3.3 v, quickly drops below the 3.1-v level on the (–) input, which is maintained briefly by capacitor C_1. This reversal of the input levels causes the output of A_1 to become low; capacitor C_2, which is normally fully charged, discharges through the transistor, which turns on when the output of A_1 drops.

While the power-supply voltage is less than about 2 v, the output of both amplifiers simply follows whatever may be available on the supply line. But when full power is restored, the capacitor C_2 begins to recharge. This takes time—the recharge path is through the 10-kilohm resistor, and the time constant is 100 milliseconds. The output of A_2 stays low until the capacitor voltage reaches 4.0 v, as shown in Figs. 2 and 3. This condition can be used as a reset pulse, and the transition to the high level when the capacitor voltage passes 4 v can generate a start pulse.

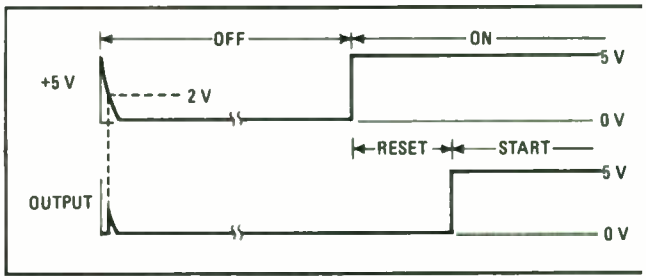
For a longer or shorter reset time, the 10-kilohm and 10-microfarad values can be changed. □



1. Reset and restart. Two voltage comparators and a gate can reset a digital system and restart it after any power interruption, be it a glitch or a complete blackout. Wide variety of ICs can be used. Key components are the RC network at the input of A_2.



2. Short failure. Even a momentary failure that falls below 2 volts can cause problems. Reset begins the moment power is restored; start pulse is generated after restored power recharges capacitor.



3. Long failure. In the event of a total power failure, the output stays down after power is restored, again until capacitor has been recharged. Duration of reset depends on RC time constant.

How to prevent spurious tripping of protection circuits

by Thomas E. Skopal
Acopian Corp., Easton, Pa.

Users of power supplies sometimes find that crowbar circuits for overvoltage protection trip unnecessarily. The spurious tripping is caused by transients that are not dangerous to the load circuit, but that have enough amplitude to momentarily raise the voltage seen by the circuit to a level greater than its trip voltage.

The protection circuit is susceptible to this unwanted tripping because the trip level is set close to the rated output voltage of the supply and because the circuit is designed for quick response. The tripping should be prevented by suppressing the transients, not by reducing the sensitivity of the protection circuit.

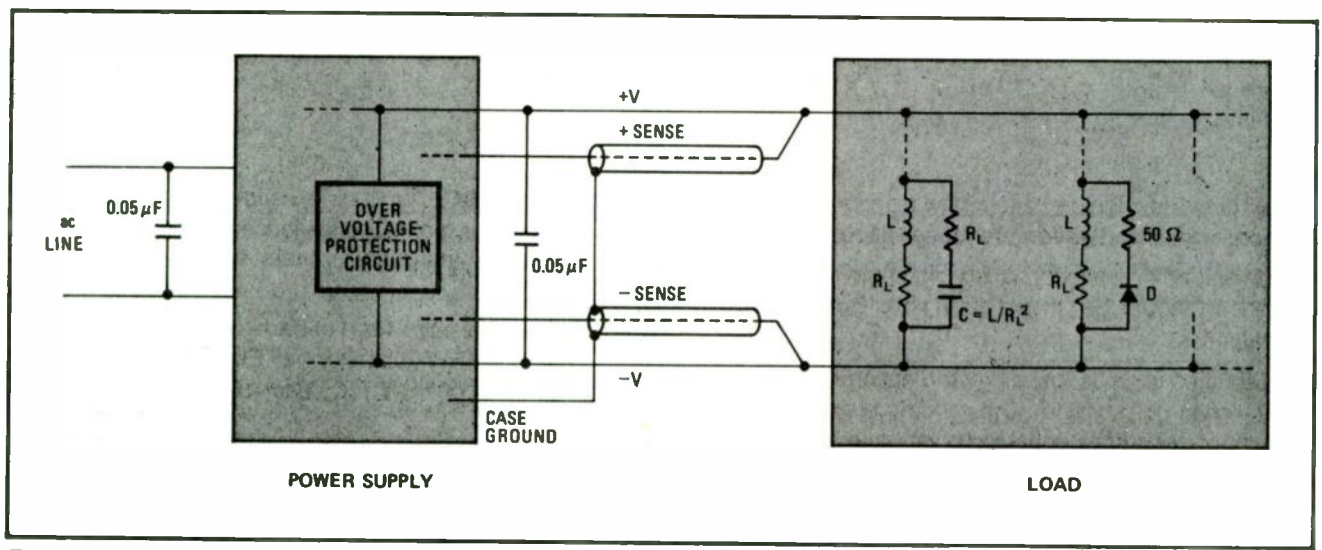
Transients can reach the crowbar circuit in three ways: by coupling through the power supply from the ac line, by conduction through the output wiring from transient-generating elements in the load, and by picking up radiated transients in the system wiring.

Bypassing the input and output terminals of the power supply usually reduces transients from all causes to insignificant levels. To be most effective, nonpolarized capacitors should have good high-frequency characteristics, as provided by Mylar, disk ceramic, and mica types; a value of 0.05 to 1.0 microfarad is most effective. (The output capacitor of a typical power supply is usually an electrolytic type, which is intended for stabilizing the regulator circuit and for filtering, but is not an effective bypass for high frequencies.)

If additional leads are used for remote sensing or for output-voltage programing, shielded wire should be used, with the shields grounded only at the power-supply end. Bypassing these leads would help to suppress transients, but would also tend to slow the response of the supply, so shielded wire is used instead.

Crowbar operation is affected by electromechanical components in the load. Relays, counters, and solenoids tend to generate sizable transients that can damage a sensitive circuit; therefore, such transients must be suppressed at their source. They are most effectively suppressed by an RC network across the inductance. (Resistance in series with the bypass capacitor is necessary to prevent the high current surge that would otherwise flow into C when the load is energized. This current would burn switch contacts and cause noise.) The resistor value should equal the resistance of the load component, R_L, and the capacitor value should be equal to L/R_L^2, where L is the load inductance.

As an alternative, transients from an inductive component in a dc circuit may be suppressed simply by a diode connected across the component, back-biased relative to the supply voltage. The reverse voltage resulting from collapse of the magnetic field is shunted through the diode, and its amplitude is limited to the forward drop of the diode. However, this shunt diode tends to slow turnoff. The decay time-constant is given by $L/(R_L + R_{diode})$; if speed is critical, some suppression can be sacrificed for speed by adding a resistor (50 to 500 ohms) in series with the diode. □



Transient suppression. Suppressing all transients generated within or induced into a system prevents unnecessary tripping of power-supply overvoltage protectors. Four techniques described in the text are illustrated in this circuit. Capacitors at input and output terminals of the supply normally reduce transients to insignificant levels. Leads for remote sensing use shielded wire, grounded only at the supply end. Transients from electromechanical load element are suppressed by RC shunt. Reverse emf from inductive load is shunted through diode.

C-MOS reset circuit ignores brief outages

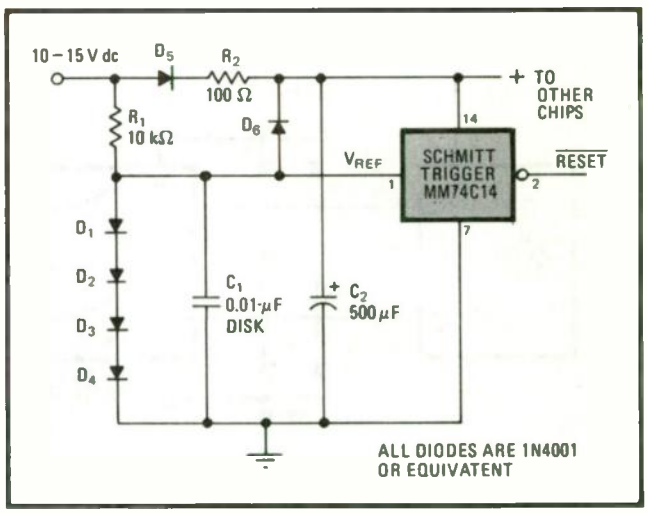
by Roger F. Atkinson
ITEC Inc., Huntsville, Ala.

If the voltage supply to a C-MOS circuit drops much below 3 volts during a power failure, a reset signal is necessary to initialize the logic and perhaps also to indicate that the power has failed. But, unlike conventional power-fail circuits, the reset should ignore transient interruptions that do not drop the supply below 3 volts, the level at which the logic states of the latches, counters, and the like may change randomly.

Such a reset signal can readily be derived. An isolated reference voltage is applied to the input of a Schmitt trigger having threshold voltages that are a function of the logic-supply voltage.

In the complementary-metal-oxide-semiconductor circuit shown, the Schmitt trigger is a National MM74C14. Diodes D_1 through D_4 and resistor R_1 establish a reference voltage of approximately 2.5 volts across capacitor C_1. D_5 isolates the energy-storage capacitor C_2 from the supply and from any higher-current loads such as relays and displays that are not needed during a power failure. D_6 assures that the reference cannot exceed the supply voltage by more than one diode drop.

When power is first applied, C_2 is at zero volts. As C_2 charges through D_5 and R_2, the reference at first exceeds the high threshold of the Schmitt trigger, causing its output to go low and thus resetting associated circuits. This signal remains low until the logic supply voltage (across C_2) is high enough (about 8 V) for the low threshold to exceed the reference and to switch the Schmitt high. During subsequent power failures—



Resets if necessary. During brief interruptions of dc power, the charge on C_2 maintains voltage to C-MOS digital circuits, preserving their logic states. But if the power failure lasts so long that the voltage across C_2 drops below 3 V, the Schmitt trigger resets the logic circuits when power is restored.

provided the logic supply voltage across C_2 remains above 3 V—the high threshold (about 80% of supply at low voltages) will remain above the reference, so that the Schmitt output will not switch when power is reapplied. However, should the supply fall so low that the high threshold is lower than the reference when power is restored, the Schmitt output will go low, thus resetting the logic. The reset can activate a warning indicator.

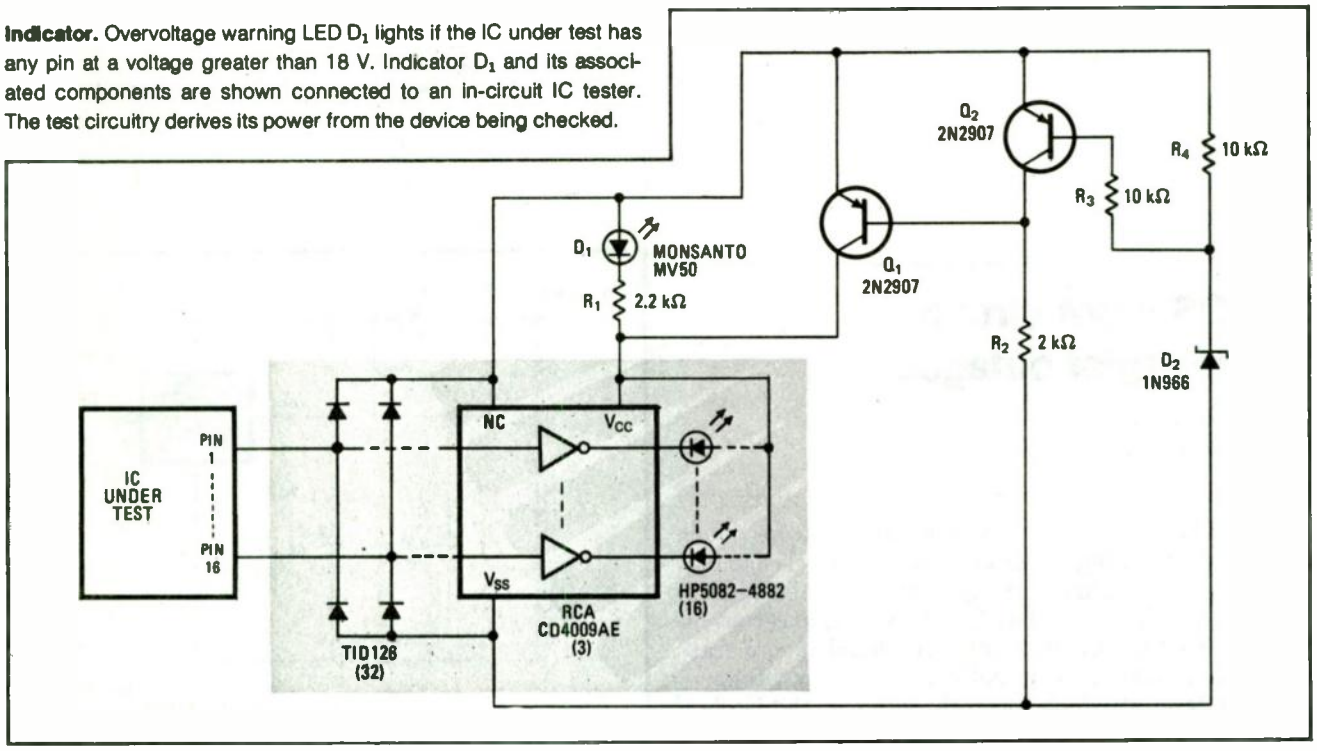
R_2 and C_2 delay the rise of the logic-supply voltage, controlling the length of the reset pulse. Other C-MOS Schmitt circuits might be used. To maximize endurance during power outages, resistive loads on the C-MOS outputs should be avoided. The circuit shown allows an MM74C193 up/down counter to retain its count for more than 10 minutes. □

Overvoltage indicator can be added to C-MOS IC tester

by Rajni B. Shah
Rohde & Schwarz, Fairfield, N.J.

A warning light that signals the presence of an overvoltage can be added to the features described in "In-circuit IC tester checks TTL and C-MOS" [*Electronics*, May 30, 1974, p. 120]. A light-emitting diode glows if the IC under test has any pin voltage greater than 18 V. The warning circuit, like the rest of the test circuit, draws its power from the IC being checked. As described here, it can operate at overvoltages as high as 30 V.

The indicator circuitry, shown below, is connected to the tester described previously. Warning LED D_1 is shunted by Q_1, which is normally held in conduction by the potential applied to its base through R_2. Q_2 is normally inhibited by the base connection through R_3. If the voltage at any IC pin exceeds 18 V, however, zener diode D_2 breaks down, and Q_2 starts to conduct. Conduction in Q_2 pulls the base of Q_1 up to turn off Q_1. The voltage drop across Q_1 then is sufficient to light up LED D_1, indicating the overvoltage. □

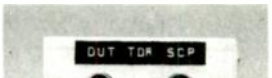


Indicator. Overvoltage warning LED D_1 lights if the IC under test has any pin at a voltage greater than 18 V. Indicator D_1 and its associated components are shown connected to an in-circuit IC tester. The test circuitry derives its power from the device being checked.

42. Pulse generators

Nanosecond-pulse generator is powered by two D cells

by M. J. Salvati
Sony Corp. of America, Long Island City, N.Y.



2. A box of pulses. Complete pulse generator, including batteries and fixture for time-domain reflectometry, is housed in a standard 3-by-2-by-5¼-inch aluminum box. Unit runs for 180 hours on two dry cells. Shown unlabeled at the right is the two-position frequency switch.

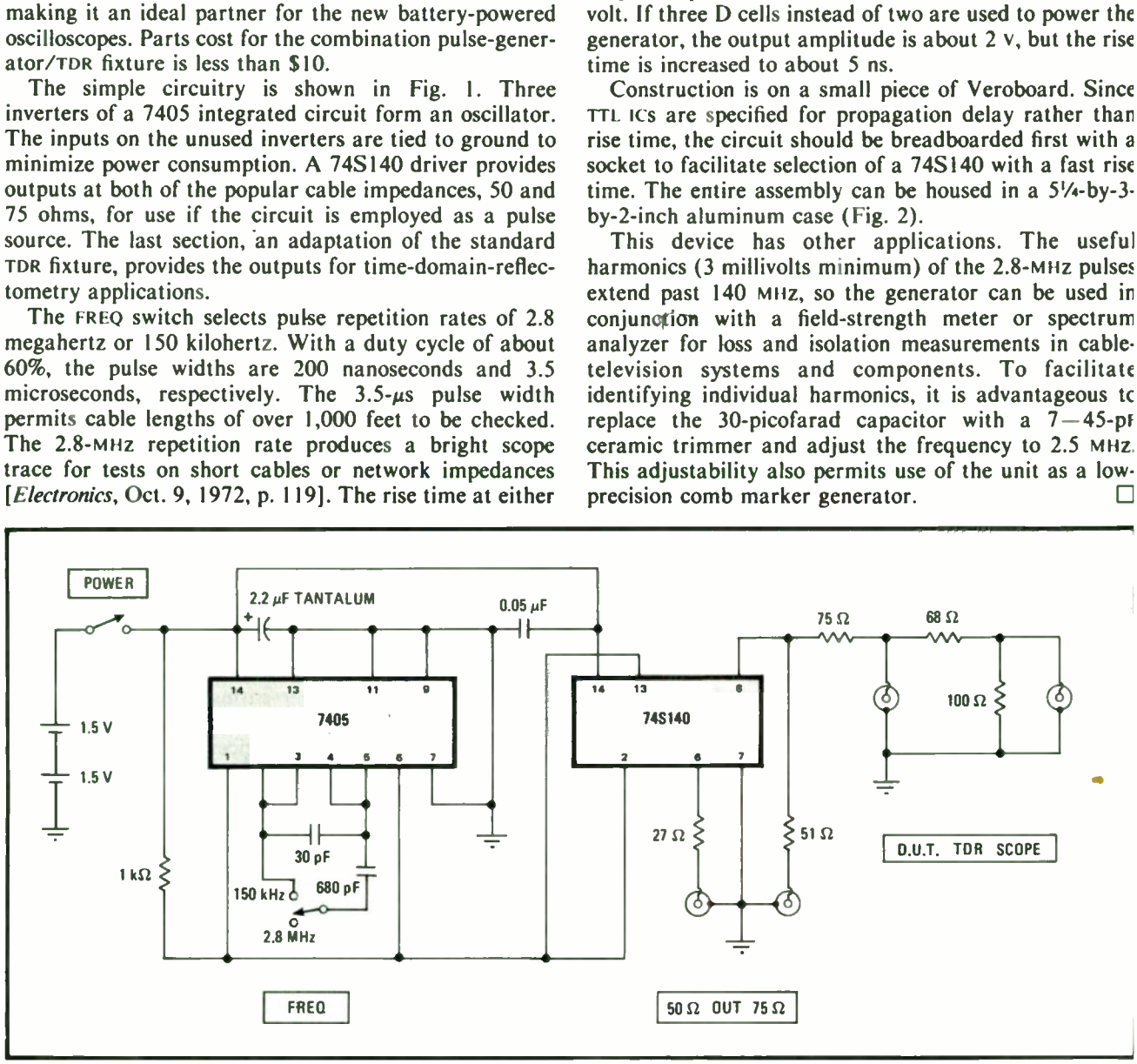
A pocket-size source of nanosecond pulses is handy for field work in time-domain reflectometry and many other measurement applications. This pulse generator operates for about 180 hours from a pair of standard D cells, making it an ideal partner for the new battery-powered oscilloscopes. Parts cost for the combination pulse-generator/TDR fixture is less than $10.

The simple circuitry is shown in Fig. 1. Three inverters of a 7405 integrated circuit form an oscillator. The inputs on the unused inverters are tied to ground to minimize power consumption. A 74S140 driver provides outputs at both of the popular cable impedances, 50 and 75 ohms, for use if the circuit is employed as a pulse source. The last section, an adaptation of the standard TDR fixture, provides the outputs for time-domain-reflectometry applications.

The FREQ switch selects pulse repetition rates of 2.8 megahertz or 150 kilohertz. With a duty cycle of about 60%, the pulse widths are 200 nanoseconds and 3.5 microseconds, respectively. The 3.5-μs pulse width permits cable lengths of over 1,000 feet to be checked. The 2.8-MHz repetition rate produces a bright scope trace for tests on short cables or network impedances [*Electronics*, Oct. 9, 1972, p. 119]. The rise time at either repetition rate is a little over 4 ns, a speed achieved by operating the TTL ICs below their rated voltage. The output amplitude into 50- or 75-ohm loads is about 0.8 volt. If three D cells instead of two are used to power the generator, the output amplitude is about 2 V, but the rise time is increased to about 5 ns.

Construction is on a small piece of Veroboard. Since TTL ICs are specified for propagation delay rather than rise time, the circuit should be breadboarded first with a socket to facilitate selection of a 74S140 with a fast rise time. The entire assembly can be housed in a 5¼-by-3-by-2-inch aluminum case (Fig. 2).

This device has other applications. The useful harmonics (3 millivolts minimum) of the 2.8-MHz pulses extend past 140 MHz, so the generator can be used in conjunction with a field-strength meter or spectrum analyzer for loss and isolation measurements in cable-television systems and components. To facilitate identifying individual harmonics, it is advantageous to replace the 30-picofarad capacitor with a 7—45-pF ceramic trimmer and adjust the frequency to 2.5 MHz. This adjustability also permits use of the unit as a low-precision comb marker generator. □



1. Field man's friend. Compact nanosecond-pulse generator powered by two dry cells delivers 0.8-volt pulses to either 50-ohm or 75-ohm output jacks; three batteries give 2 V, at some cost in rise time. Conections provide for use in time-domain reflectometry.

Generating pulses with C-MOS flip-flops

by F.J. Marlowe and J.P. Hasili
RCA Laboratories, Princeton, N.J.

A complementary-MOS D-type flip-flop and just a single external resistor and capacitor form a handy edge-triggered one-shot. What's more, two of these one-shots will form a simple gated oscillator when they are cross-coupled and a NOR gate is inserted in the feedback path.

The C-MOS flip-flop uses little power and can operate from a wide range of power-supply voltages (3 to 15 volts). In addition, because of its high MOS input impedance, the flip-flop allows very large resistance and capacitance values to be used. For instance, a gated oscillator circuit containing 1-megohm resistors and 500-picofarad capacitors will have an output period of 20 minutes.

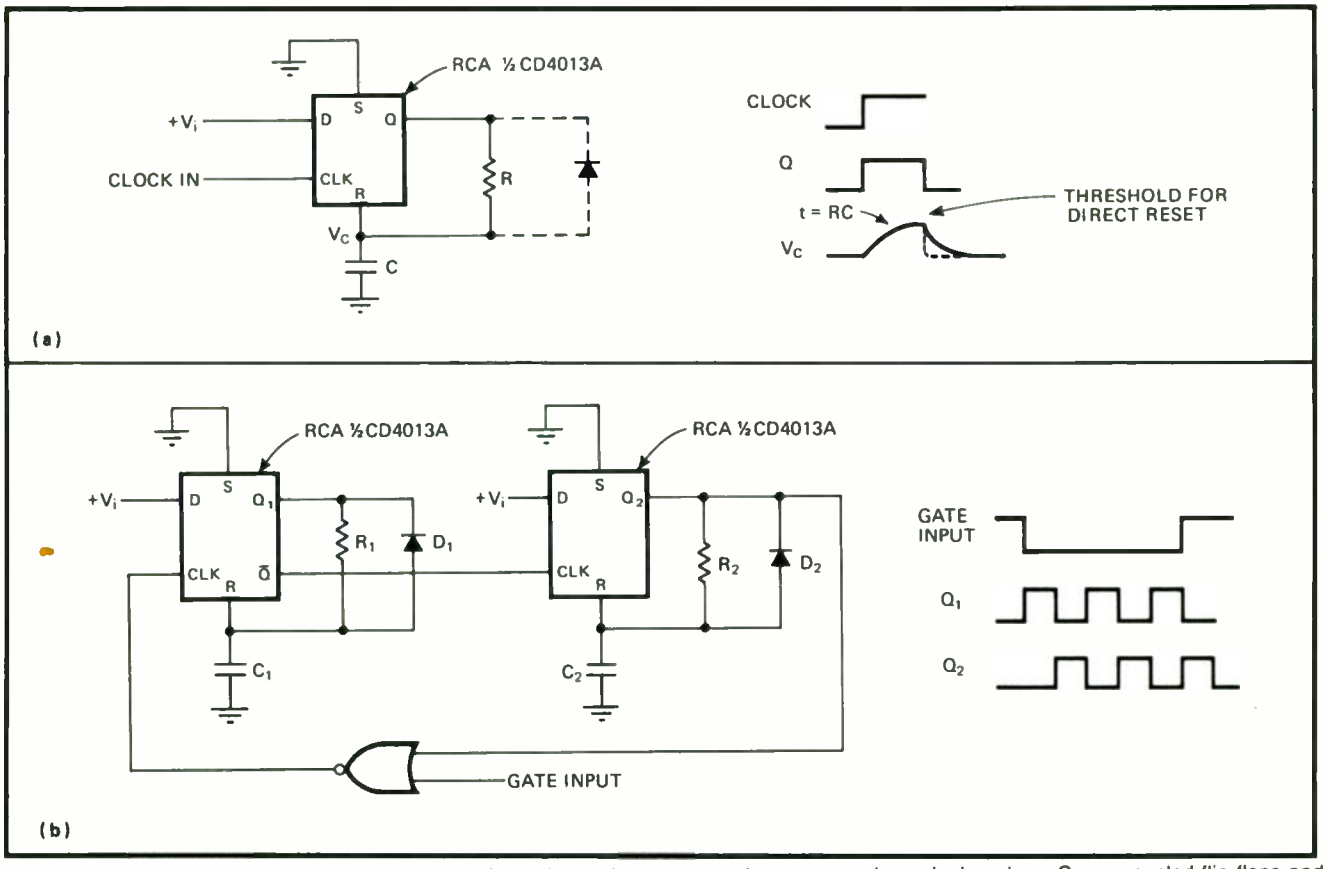
In the one-shot circuit of (a), a positive transition on the clock input switches the Q output from low to high, which in turn charges capacitor C through resistor R. When capacitor voltage, V_C, reaches the flip-flop threshold for direct reset, the Q output returns to the low state independently of the clock level, and capacitor C discharges through resistor R.

The circuit works well for a wide range of resistance and capacitance values, but if resistor R is less than 4 kilohms, the Q output amplitude and rise time may be badly degraded by the flip-flop's output impedance, which is about 400 ohms. As a refinement, a diode can be placed across resistor R to speed up the recovery time of the capacitor discharge (the dashed line in the plot of capacitor voltage V_C). This speed up in recovery time is important—if a positive clock transition occurs before the capacitor is fully discharged, the next one-shot pulse interval will be shorter than it should be.

By cross-coupling two of these one-shots, a convenient two-phase oscillator with complementary outputs can be made with only a single dual flip-flop package. The oscillator's output duty cycle can be varied by using different RC time constants for each one-shot.

Furthermore, placing a NOR gate in the feedback path, as shown in (b), permits the oscillator to be gated. When the gate input goes low, the oscillator is started with the same phase each time. When the gate input returns to its high state, the oscillator completes the cycle and then stops. Additional gating can also be provided through the data (D) inputs or the direct set (S) inputs. Diodes D_1 and D_2 fully discharge capacitors C_1 and C_2 after each half cycle, so that the oscillator's first few cycles will last no longer than its steady-state cycles.

Since the charging rate of the capacitors in these circuits depends on the voltage of the power supply, timing stability and accuracy are functions of power-supply regulation. □



Pulse generators. Lone C-MOS D-type flip-flop (a) requires only two external parts to produce single pulses. Cross-coupled flip-flops and NOR gate (b) make gated oscillator having adjustable duty cycle. Time constants can be long because of flip-flop's high input impedance.

Preset generator produces desired number of pulses

by Glen Coers
Texas Instruments, Components Group, Dallas, Texas

Computer systems and medical instruments are likely applications for a digital pulse generator that will deliver, on command, any desired number of full-width pulses from 1 to 999. Three 10-position switches set the number wanted.

Rotary switches S_1, S_2, and S_3 fix the number of output pulses. S_1 controls the most significant digit, while S_3 controls the least significant digit. For example, if S_1 is set to 3, S_2 to 6, and S_3 to 8, the number of output pulses will be 368.

Gates G_1 through G_4 eliminate any count error caused by contact bounce from toggle switch S_4. When S_4 is placed in its count position, flip-flop FF_1 inhibits gate G_4 until the trailing edge of S_4's count pulse occurs, so that even the first output pulse is full width.

Placing S_4 in its count position results in a high at both inputs to G_2, enabling this gate (its output goes low) and resetting the decade counters to zero. The count command also causes one input of G_1 to go low, making its output high. This clears flip-flop FF_1 and keeps its Q output low. The high from G_1 also drives FF_1's preset function high, as well as one of the inputs to G_4. The output from G_5 is now low.

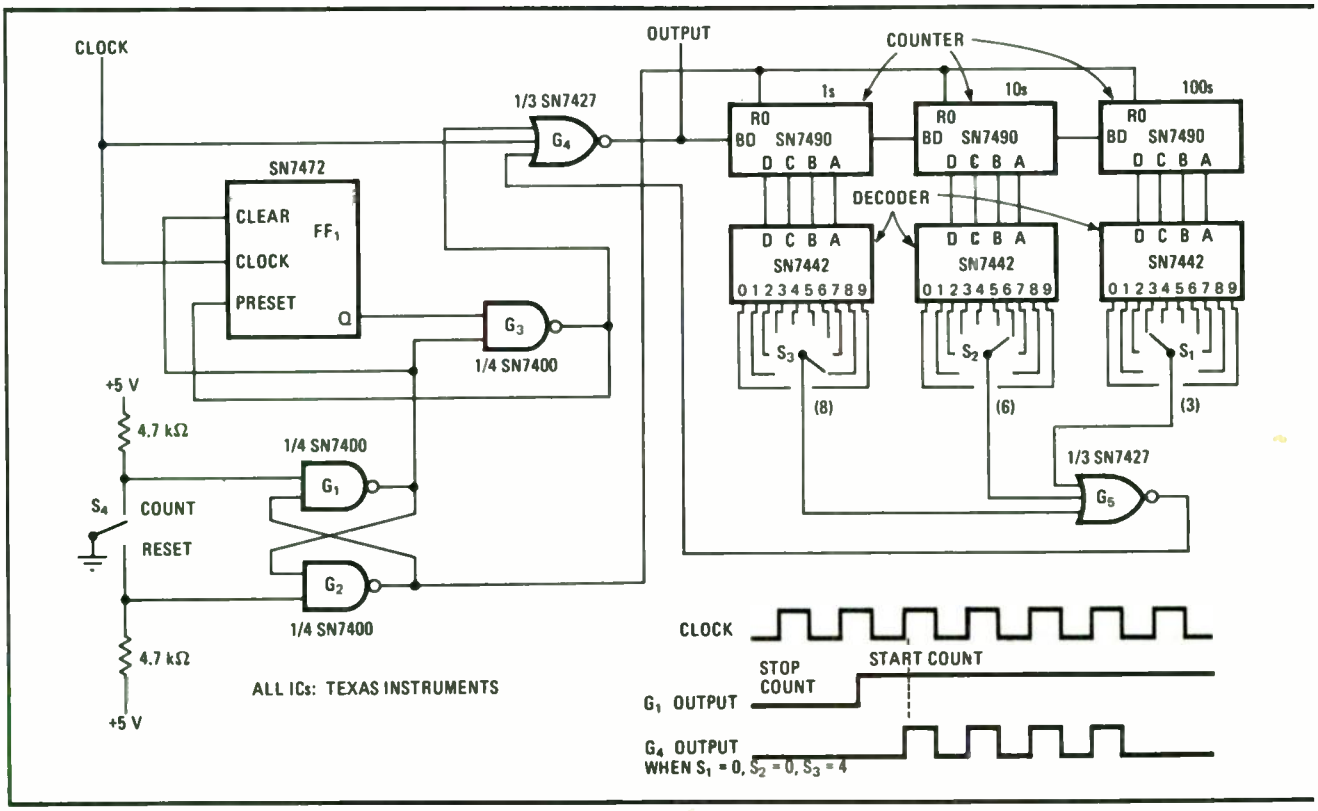
The first negative edge of a clock pulse triggers the flip-flop and makes Q go high. The output of G_3 then goes low, presetting the flip-flop to maintain Q in the high condition. When G_3's output goes low, one input to G_4 also goes low, enabling this gate so that clock pulses are passed to its output.

The binary-coded-decimal count that is accumulated in the divide-by-10 arrangement of decade counters is transferred to the BCD-to-decimal decoders. A decoder output goes low when that decoder reaches the setting of its associated rotary switch. When all three decoder outputs are low, gate G_5 is inhibited (its output goes high). This causes one input to G_4 to go high, stopping the transfer of pulses.

Placing switch S_4 in its reset position drives one input to gate G_2 low, making its output go high and operating the reset function of the decade counters. Both inputs of G_1 are now high, while its output, the clear function of the flip-flop and one input to G_3 are low. This clears Q to a low condition, causing G_1's output, FF_1's preset function, and one input to G_4 to go high. The circuit is now ready to start a new count.

Adding more counters, decoders, and switches will, of course, increase the number of pulses that can be counted. □

Pulse counter. Three rotary switches control number of output pulses that can be generated; settings may range from 1 to 999. Flip-flop and gates G_1 through G_4 assure that all output pulses are full width. Toggling switch S_4 to its count position allows gate G_4 to transfer clock pulses to divide-by-10 arrangement of decade counters. Each BCD-to-decimal decoder counts to setting of its rotary switch.



Controlling duty cycle and rep rate independently

by W.D. Harrington
University of Florida, Communication Sciences Laboratory, Gainesville, Fla.

A pulse generator with a frequency range of 10 hertz to 10 kilohertz can provide a voltage-controllable output duty cycle that does not change with variations in operating frequency. This constant-duty-cycle generator can be used as a constant-phase triggering source. The falling edges of its output pulse train can trigger another pulse train, producing phase-shifted pulses, with the phase shift being controlled by a voltage.

The duty cycle, D, is adjusted (from 5% to 95%) with voltage V_D, and is a ratio of V_D to supply voltage V_P:

$$D = V_D/V_P = \tau/T$$

where τ is output pulse width, and T is output pulse period. Pulse width τ is determined by the time required for the reference ramp voltage, V_R, to rise from zero to V_1 volts. Voltage V_1 is the feedback voltage that is applied to the inverting input of the comparator.

The ramp, which is formed by charging and discharging capacitor C with a constant current, has a rise time of I_{CC}/C amperes per second. Transistor Q_1 acts as the constant-current source, while transistor Q_2 acts as the shorting switch for discharging capacitor C. The drive pulses for Q_2 must be significantly narrower than period T, but wide enough to discharge capacitor C.

Feedback voltage V_1 is the amplified difference voltage between the duty-cycle adjustment voltage, V_D, and the dc value of the output pulse train, V_2. Voltage V_2 is determined by the low-pass filter formed by resistor R_F and capacitor C_F. Since ramp voltage V_R rises at a constant rate, a decrease in voltage V_2 reduces output pulse width τ, while a rise in V_2 increases τ by action of the comparator.

As the circuit's input frequency, f, is made higher (output pulse period T is made smaller), dc filter voltage V_2 tends to rise since:

$$V_2 = V_P\tau f$$

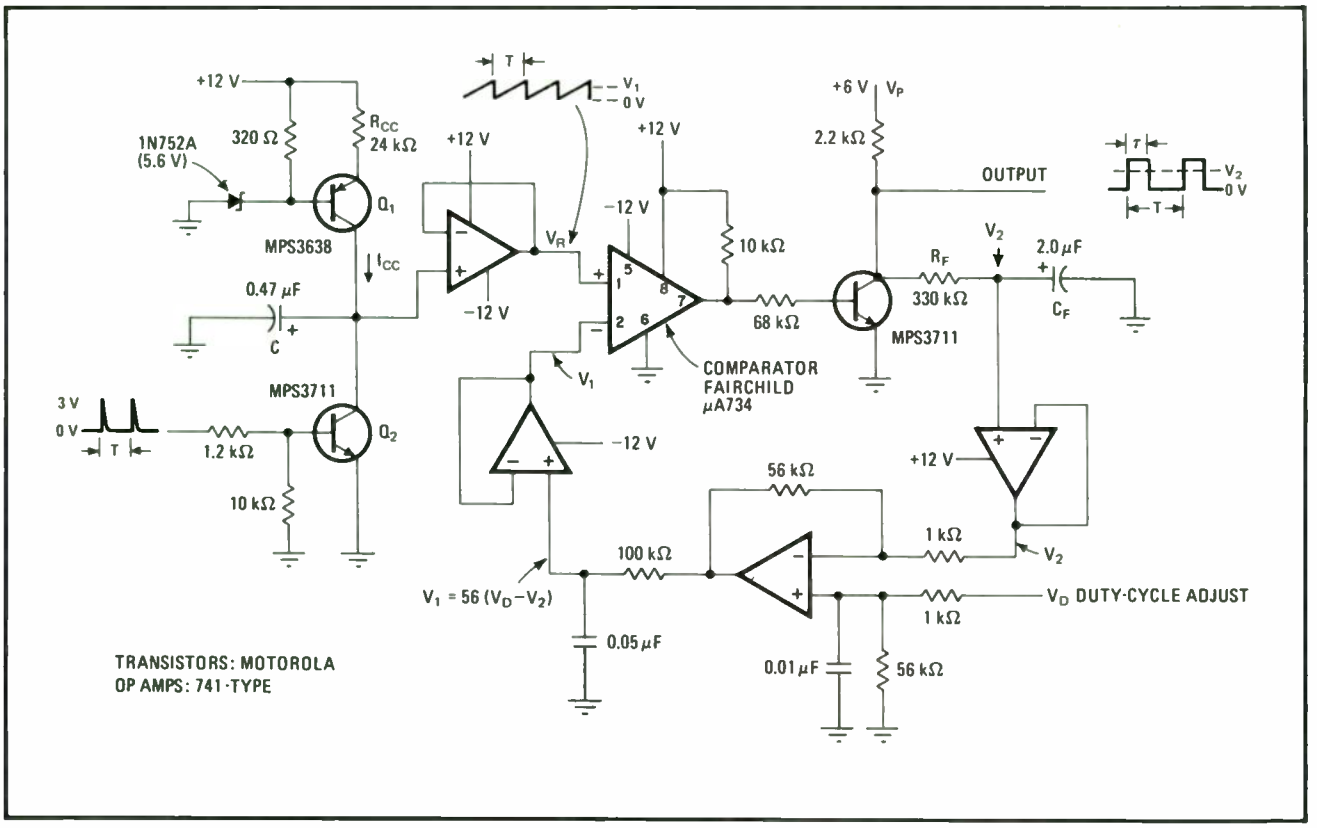
A rise in voltage V_2 causes voltage V_1 to drop, reducing output pulse width τ so that voltage V_2 remains constant. This feedback action, therefore, prevents the duty cycle (τ/T) from changing when the input frequency is varied. The variation of feedback voltage V_1 is:

$$V_1 = I_{CC}V_D/CV_Pf$$

which shows that feedback voltage V_1 is inversely proportional to driving frequency f and directly proportional to duty-cycle adjustment voltage V_D.

The circuit can be used as a phase modulator by modulating control voltage V_D, but the modulating frequency is limited by the rolloff of low-pass filter R_FC_F. The operating frequency range of the generator may be broadened by changing the value of resistor R_{CC} and using wideband operational amplifiers instead of the general-purpose 741-type units shown. □

Voltage-controlled duty cycle. Pulse generator has separate controls for output pulse period (T), output pulse width (τ), and output duty cycle (τ/T). Duty cycle is varied by changing voltage V_D, the period is controlled by input frequency, and pulse width depends on the ramp input to the comparator. Feedback action prevents duty cycle from changing when input frequency goes from 10 hertz to 10 kilohertz.



Pulse generator accuracy is immune to aging

by Frank Cicchiello
Digilog Systems Inc., Willow Grove, Pa.

This pulse generator for driving digital circuits won't change frequency, even after its components have aged or are replaced. And pulse repetition rate remains stable over a wide temperature range.

If any or all of its active devices are replaced or have aged, the generator exhibits only a 1.5% worst-case variation in rep rate. Replacing or aging any or all of the passive components causes a worst-case change of 1%. Typically, rep rate varies merely 0.5% over a 50°C temperature range, and all variations amount to less than 2% when taken collectively.

When the dc supply voltage (V_{CC}) is turned on, timing capacitor C_1 charges exponentially through resistor R_1 until capacitor voltage reaches the threshold voltage (V_T) of programable unijunction transistor (PUT) Q_1. This triggering level is established by the voltage divider formed by resistors R_2, R_3, and R_4. For optimum temperature stability when the supply is greater than 10 volts:

$$V_T = 0.5V_{CC}$$

Pulse rep rate is determined by:

$$\text{rep rate} = 1/[0.78R_1C_1 + (0.5 \times 10^{-12})R_1C_1]$$

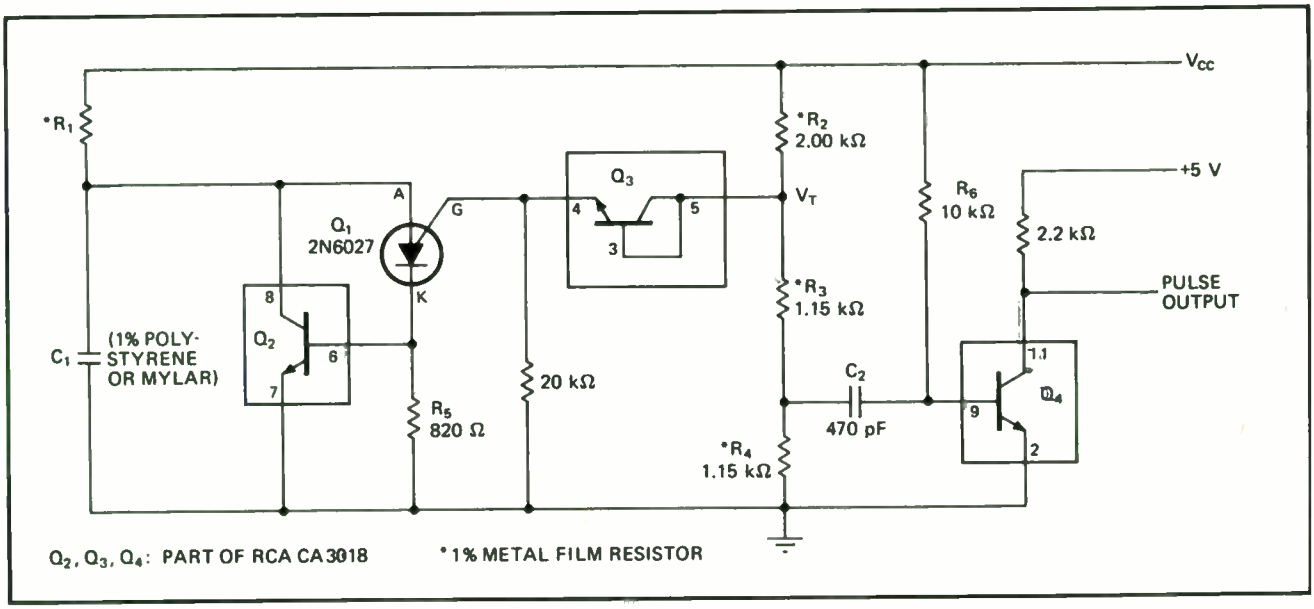
Once its triggering threshold is reached, the PUT switches, causing its gate voltage to swing in the negative direction. This produces a positive-going pulse across cathode resistor R_5, which turns on transistor Q_2 and discharges capacitor C_1.

The function of Q_2 is twofold. It rapidly discharges C_1 by passing the discharge current around the anode-cathode junction of the PUT. And it also effectively eliminates the PUT's valley-current offset. This allows timing resistor R_1 to have a value as low as 2 kilohms, rather than a value above 100 kilohms, as normally required. Output pulse rep rate can then vary over a 250:1 range for a given value of C_1 (500 picofarads to 1 microfarad). Output frequency can be up to 1 megahertz.

PUT temperature stability is assured by diode-connected transistor Q_3, which matches the temperature characteristic of the PUT's anode-gate junction, even if current flow is in the microampere region. Although most standard diodes cannot do this, almost any low-leakage diode-connected silicon transistor may be used for Q_3.

Negative-going pulses from the PUT are directly coupled to the base of transistor Q_4 through transistor Q_3; capacitor C_2 provides ac coupling. If pulses shorter than 4 to 5 microseconds (typical for this circuit) are required, the R_6C_2 time constant of Q_4's input coupling network can be reduced to differentiate the input signal and produce narrower positive-going output pulses. The output pulse train is compatible with both transistor-transistor and diode-transistor logic. □

Stable pulse generator. Power supply charges capacitor C_1 until threshold of programable unijunction transistor Q_1 is reached, Q_1 then switches, turning on transistor Q_2, which discharges C_1. Diode-connected transistor Q_3 dc couples resulting pulse to output transistor Q_4. Generator's repetition rate changes only 2% for worst-case variation of all its components, even if they age or are replaced.



Generator's duty cycle stays constant under load

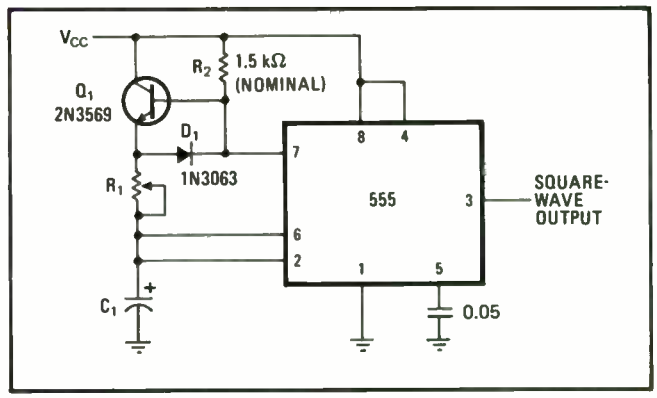
by Arthur R. Klinger
School of Health Care Sciences, Sheppard AFB, Wichita Falls, Texas

In the 555 timer, configured as a square-wave generator, adding one transistor and a diode to the RC timing network permits the frequency to be varied over a wide range while maintaining a constant 50% duty cycle [see article, p. 373].

In one simple configuration, a capacitor's charge and discharge currents flow through only one resistor. The high and low periods should be equal at any frequency, but, with heavy loads, the output may be offset by 1 volt or more from V_{cc} or ground. This varies the potentials across the RC network, creating quite large changes in duty cycle or frequency. Noise on the output lines can also cause erratic changes in the periods.

The circuit shown in the diagram removes the timing network from the output. While the timer's output is high, Q_1 is biased into saturation by R_2, so that charging current passes through Q_1 and R_1 to C. When the output goes low, the discharge switch (pin 7) cuts off Q_1 and discharges the capacitor through R_1 and D_1. With the same impedance in both paths, the high and low periods of the square wave are equal.

Q_1 should have a high β value so that R_2 can be large and still drive the transistor into saturation. With R_2 large, the IC's discharge transistor, which can sink 20 to 30 milliamperes, gets most of that current from the discharging capacitor and very little through R_2. The voltage drops in Q_1, D_1, and the internal discharge switch



Workhorse. This configuration of the 555 timer can drive a heavy load without distorting its square-wave output, even over a very wide frequency range, unlike simpler hookups.

decrease the effective voltage across R_1, causing the actual periods to be slightly longer than those given by the astable and bistable formulas in the data sheets—0.69RC and 1.1RC, respectively. A high-conductance germanium or Schottky diode for D_1 would minimize these diode-voltage drops in D_1 and Q_1.

For precise square waves, the on characteristic of Q_1 should be the same as that of D_1 and the IC's internal pull-down switch. To optimize this balance, set the timing network to its highest frequency range, and adjust R^2 while monitoring the square wave output. Once adjusted at this frequency, an excellent square wave is maintained for all combinations of R_1 and C_1.

Since the usual current-limiting resistor is not needed, the minimum value of R_1 can be as little as a few hundred ohms. Such a small resistance carries large charge and discharge currents, leading to a frequency range twice as wide as the usual configuration provides. For example, if R_1 = 10 megohms, the frequency range can exceed 20,000 to 1 for a single choice of C. □

Generator independently varies pulse rate and width

by Mahendra Shah
Univ. of Wisconsin, Space Science and Engineering Center, Madison, Wis.

Capacitor charging current can be used to change the output frequency of a voltage-controlled pulse generator that also offers an independent control over output pulse width. The generator's output-pulse frequency can range from 1 to 75 kilohertz and output pulse width from 100 nanoseconds to 18 seconds. A dual retriggerable one-shot performs the actual pulse generation, while an operational amplifier and a couple of transistors convert the control voltage into a proportional charging current for the frequency timing capacitor.

The voltage divider created by resistors R_1 and R_2 determines the voltage level at the noninverting input of the op amp. Since the op amp and emitter-follower Q_1 form a unity-gain buffer having a high input impedance, the large open-loop gain of the op amp keeps the noninverting input voltage (V_1) equal to the inverting input voltage (V_2):

$$V_1 = V_2 = [R_2/(R_1+R_2)]V_i$$

and Q_1's emitter current becomes:

$$I_{E1} = V_2/R_3$$

Both V_1 and V_2 can range between 0 and 2 volts.

Transistor Q_1 has a minimum h_{FE} of 250, making its base current much smaller than its collector current so that constant current I_{C1} is maintained nearly equal to constant current I_{E1}. Because transistor Q_2 is also a large-h_{FE} device, it draws very little base current and almost all of I_{C1} passes through resistor R_4 and diode D_1.

Furthermore, the base-emitter voltage of Q_2 and the forward voltage drop of D_1 are about the same, permitting voltage V_3 to be written as:

$$V_3 = R_4 I_{C1}$$

And the constant charging current, I_{C2}, for timing capacitor C_1 can be expressed in terms of voltage V_1:

$$I_{C2} = R_4 V_1/R_3 R_5$$

One-shot OS_1 can be retriggered during its on state within 100 nanoseconds of the end of the timing period, fixed by its timing components. The positive trigger input of OS_1 is connected to its $\bar{Q}$ terminal, and a small capacitive load (C_2) is added at the $\bar{Q}$ terminal to increase

the retriggering delay by about 20 ns.

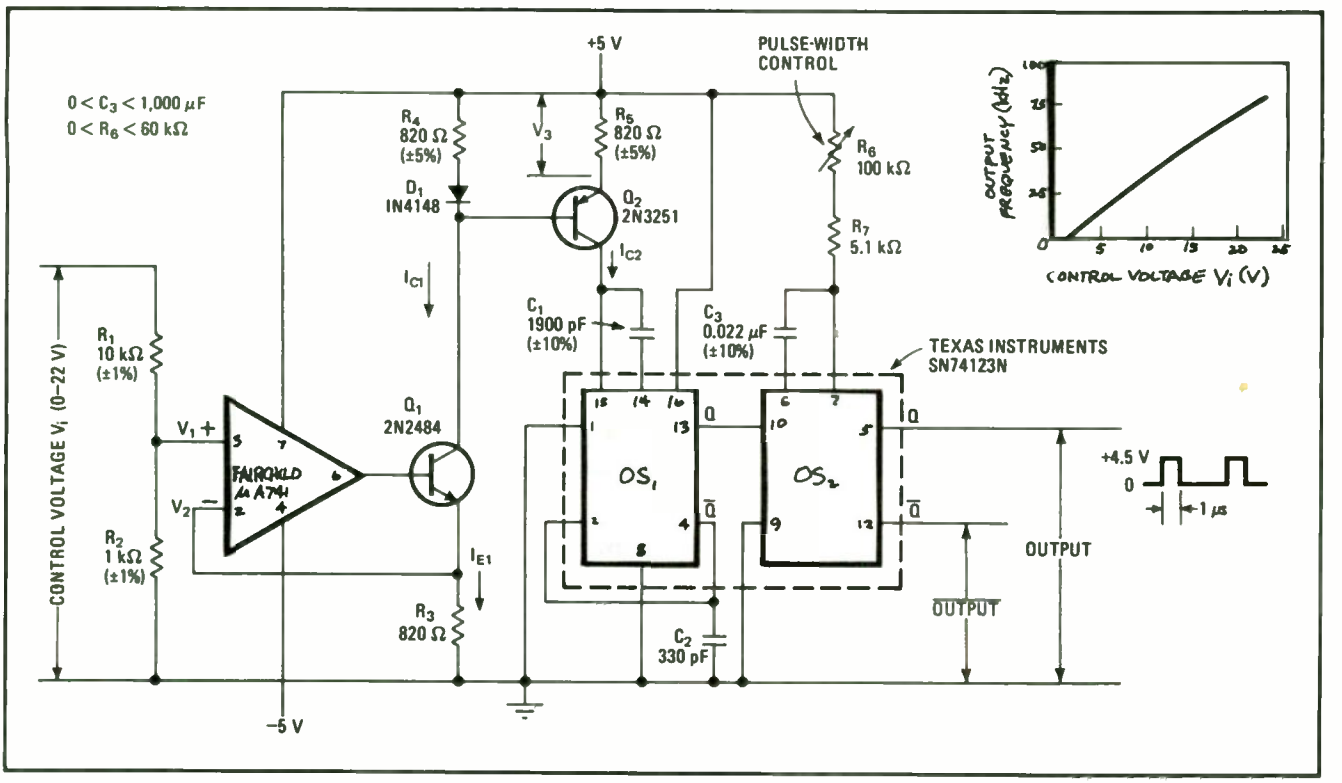
At the end of OS_1's timing cycle, its Q output makes a high-to-low transition, and its $\bar{Q}$ output makes a slightly delayed low-to-high transition, retriggering OS_1 back into its on state for another timing period. This cycle repeats at frequency f:

$$f = 1/(T_1 + 60\text{ ns})$$

where T_1 is OS_1's on-time. One-shot OS_2 is triggered by the low-to-high transitions of OS_1's Q output; these transitions generate positive-going pulses at OS_2's Q output. The width of OS_2's output pulses is controlled independently by resistors R_6 and R_7 and capacitor C_3.

Timing period T_1, which is usually much greater than 60 ns, is inversely proportional to voltage V_1. The circuit's output pulse frequency is almost linearly proportional to voltage V_1 and, therefore, to control voltage V_i. The graph shows that the pulse generator's frequency is practically linear over the control voltage range of 5 to 22 V (0.45 to 2 V for V_1).

Generator frequency range can be extended to higher or lower frequencies by scaling the value of capacitor C_1, but this capacitor's charging current, I_{C2}, should not be made greater than a few milliamperes. Voltage control of output pulse width can be obtained by replacing resistors R_6 and R_7 with a voltage-controlled constant-current source. □



Voltage-variable rep rate. Input control voltage determines output frequency of pulse generator. Collector currents developed by transistors Q_1 and Q_2 are directly proportional to control voltage V_i. Constant current I_{C2} charges timing capacitor C_1, controlling pulse frequency of one-shot OS_1, which is retriggered by its own $\bar{Q}$ output. OS_1's Q output triggers one-shot OS_2, which controls output pulse width.

Generating nanosecond pulses with TTL monostables

by Robert J. Broughton
Yale University, New Haven, Conn.

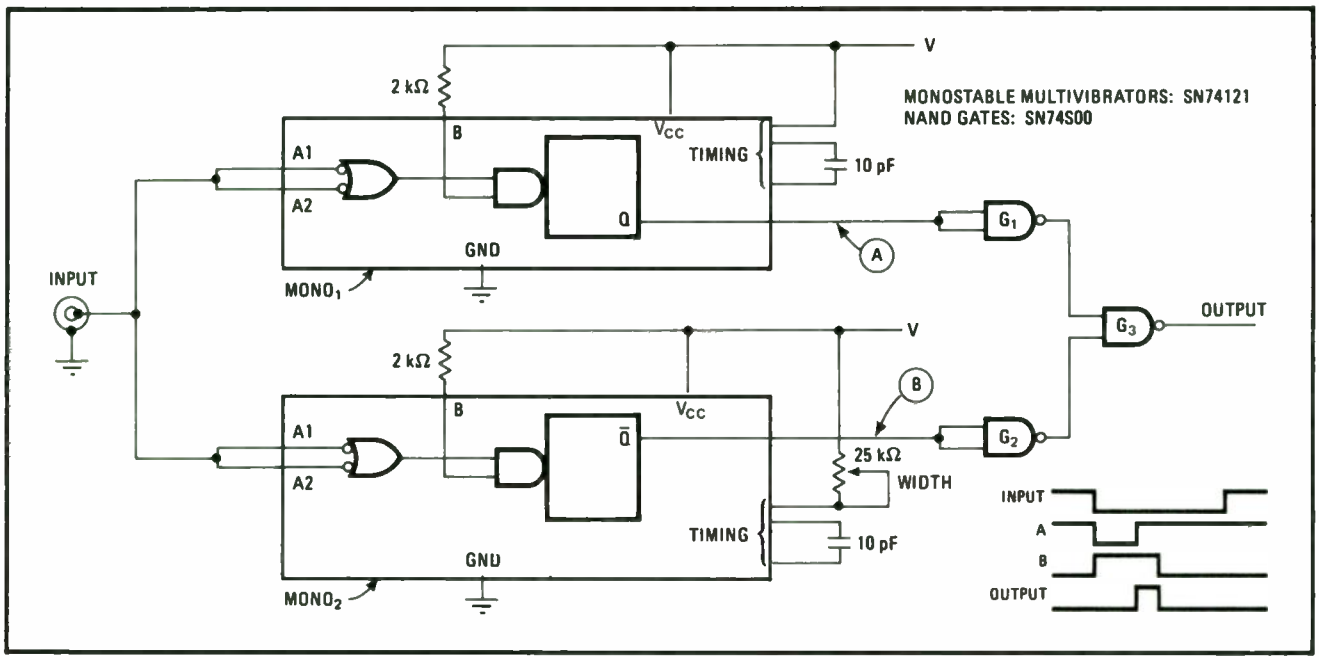
Narrow fast pulses—with widths down to a few nanoseconds and rise and fall times of 2 ns—can be produced by a circuit based on transistor-transistor logic. The circuit's output pulse width is variable, and pulses as wide as 220 ns can be obtained.

The trick is to take the difference between two pulses generated by a pair of standard TTL monostable multivibrators. The input signal is applied to the edge-triggered inputs of $MONO_1$ and $MONO_2$. Those two monostable inputs are wired in parallel, while the Schmitt-trigger monostable inputs are kept high by the 2-kilohm resistors tied to the supply voltage.

$MONO_1$ is wired to produce a 30-ns pulse, which is conditioned by a Schottky-TTL NAND gate, G_1, to speed up its rise and fall times. Similarly, $MONO_2$ generates an output pulse that is complementary to the one generated by $MONO_1$ and that is conditioned by a second Schottky-TTL NAND gate, G_2. The width of this pulse is adjustable from 30 ns to more than 250 ns.

The third and last Schottky-TTL NAND gate, G_3, accepts the conditioned pulses from gates G_1 and G_2. The

output of this gate is a fast narrow pulse whose width is the difference between the pulses produced by $MONO_1$ and $MONO_2$. An output pulse having a width of 8 ns and rise and fall times of 2ns can be easily obtained with the generator circuit. □



Pulse generator. A pair of standard TTL monostables can be made to produce sharp nanosecond pulses by using a Schottky-TTL NAND gate to accept their complementary outputs. The pulse width of $MONO_1$ is fixed at 30 ns, while the pulse width of $MONO_2$ is variable from around 30 ns to better than 250 ns. Gate G_3 takes the difference between these two pulse widths. Output rise and fall times are 2 ns.

Single switch regulates number of pulses

by Mahesh Bhuta
IBM Corp., General Products division, San Jose, Calif.

A simple SCR ring counter or a serial-in/parallel-out shift register will make a pulse generator produce a predetermined number of pulses at the activation of a single switch. The number of pulses generated depends on which switch is closed. A pulse frequency of 100 kilohertz is easily attainable.

Circuit (a), which contains the SCR ring counter, employs a conventional astable multivibrator as its basic pulse source. Transistors Q_1 and Q_2 make up this multivibrator. When any one of the switches is closed, transistor Q_1 turns on, triggering the astable.

The astable includes an SCR so that transistor Q_2 will always saturate before transistor Q_1. When Q_2 generates the first output pulse, the rising edge of this initial pulse fires SCR_A, enabling the astable to operate in its free-running mode. Bleeder resistor R_B provides the holding current for SCR_A.

The output from transistor Q_3 is fed to the SCR ring counter. Capacitors C, diodes D, and resistors R form the steering circuit that enables the appropriate pulse from Q_3 to fire the appropriate number of SCRs. If k pulses are desired, the kth switch is activated, the astable will generate k pulses, and the kth pulse will fire the kth SCR, making its anode go to 0.3 volt. This immediately deprives transistor Q_1 of its base drive, and the astable is turned off.

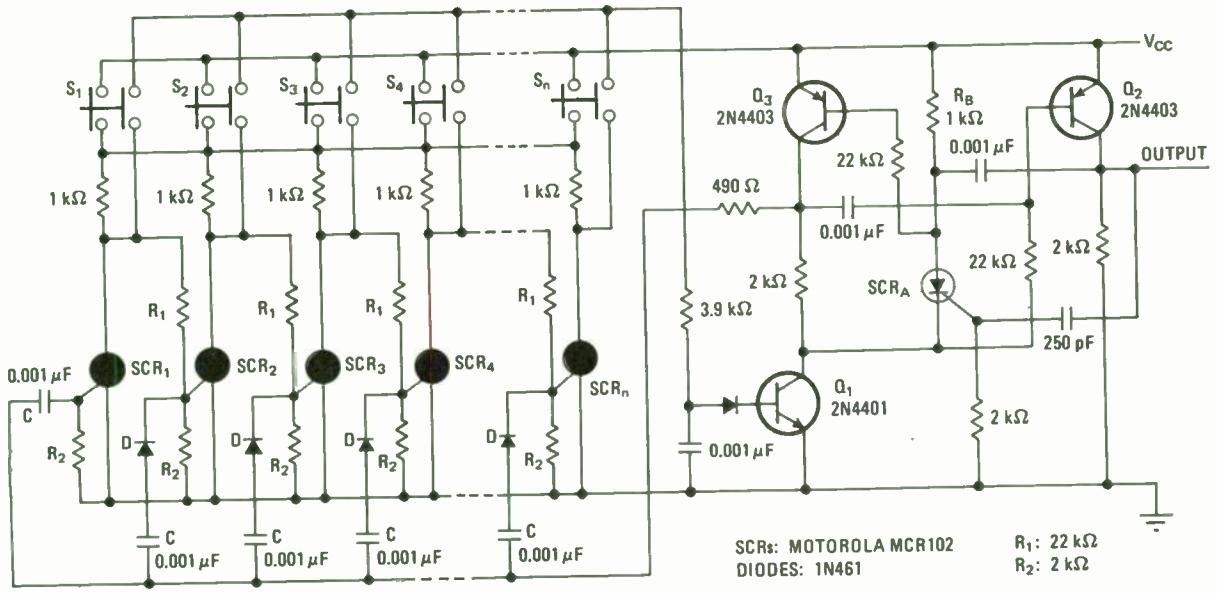
When the kth switch is released, the power to the SCR counter is removed, and the SCRs are switched off. The counter is automatically reset so that it is ready to generate the next desired set of pulses.

The SCR counter can be replaced with a serial-in/parallel-out shift register, as shown in (b). The register's SERIAL inputs are tied high. When the switches are in their normally closed positions, the register's CLEAR input and all its outputs are low.

Transistors Q_1 and Q_2 are connected as an astable multivibrator. When any one of the switches is activated, transistor Q_1 turns on. The rising edge of the first pulse from transistor Q_2 will trigger the SCR, which will stay on because of bleeder resistor R_B.

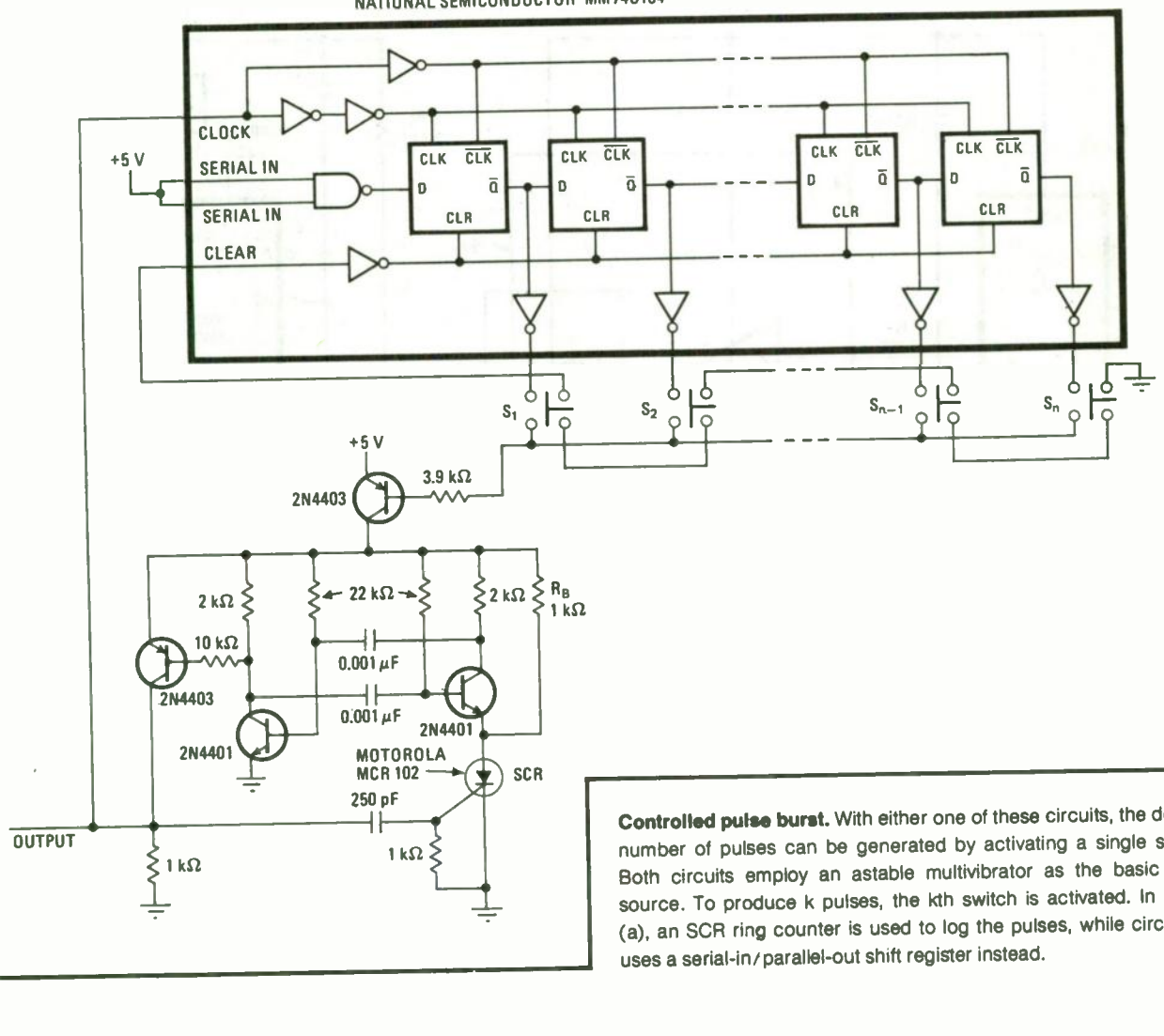
The output pulses from the astable provide the clock signal for the shift register. Each pulse advances the register until the kth output—the one that is connected to the base of transistor Q_1 through the kth switch—goes high. Once this happens, the astable switches off. When the kth switch is released, the register's CLEAR input goes low, and the shift register is automatically reset. The next set of pulses can now be generated. □

(a)



(b)

SHIFT REGISTER:
NATIONAL SEMICONDUCTOR MM74C164



Controlled pulse burst. With either one of these circuits, the desired number of pulses can be generated by activating a single switch. Both circuits employ an astable multivibrator as the basic pulse source. To produce k pulses, the kth switch is activated. In circuit (a), an SCR ring counter is used to log the pulses, while circuit (b) uses a serial-in/parallel-out shift register instead.

Binary input determines pulse-generator frequency

by Mahendra J. Shah
University of Wisconsin, Madison, Wis.

A digitally programable pulse generator for computer-controlled test systems and real-time control systems can be put together quite economically. The generator's output frequency is linearly related to the input binary number, and its output-pulse width can be varied over a 20:1 range by manually adjusting a potentiometer.

The circuit consists of: a low-cost 8-bit digital-to-analog converter having a current output; an integrated one-shot and its reset circuitry (transistor Q_1, resistors R_1, R_2, and R_3, and capacitor C_1); an op-amp integrator (including emitter-follower Q_2, resistor R_4, and capacitor C_2); and a zero-crossing comparator (transistor Q_3, diode D_1, and resistor R_5).

With transistor Q_1 off and transistor Q_2 on, the output current from the converter linearly discharges capacitor C_2 to almost zero, turning transistor Q_3 off. This causes Q_3's collector voltage to rise toward the 5-volt supply level, firing the one-shot and causing its Q output to go high. Reset components R_2, R_3, and C_1 differentiate this output transition, producing a positive pulse at the base terminal of transistor Q_1 and turning this device on.

For the interval (recovery time T_R) that transistor Q_1 remains on, capacitor C_2 charges to its maximum voltage. Transistor Q_1 then turns off, permitting the cycle to repeat. Meanwhile, the one-shot completes its timing cycle and generates a pulse of width T_P.

The length of reset interval T_R depends on the threshold voltage of transistor Q_1, the desired output-signal amplitude, and the time delay provided by resistors R_1, R_2, and R_3, and capacitors C_1 and C_2. The total output period is given by:

$$T_T = C_2 V_{E2max}/I_o$$

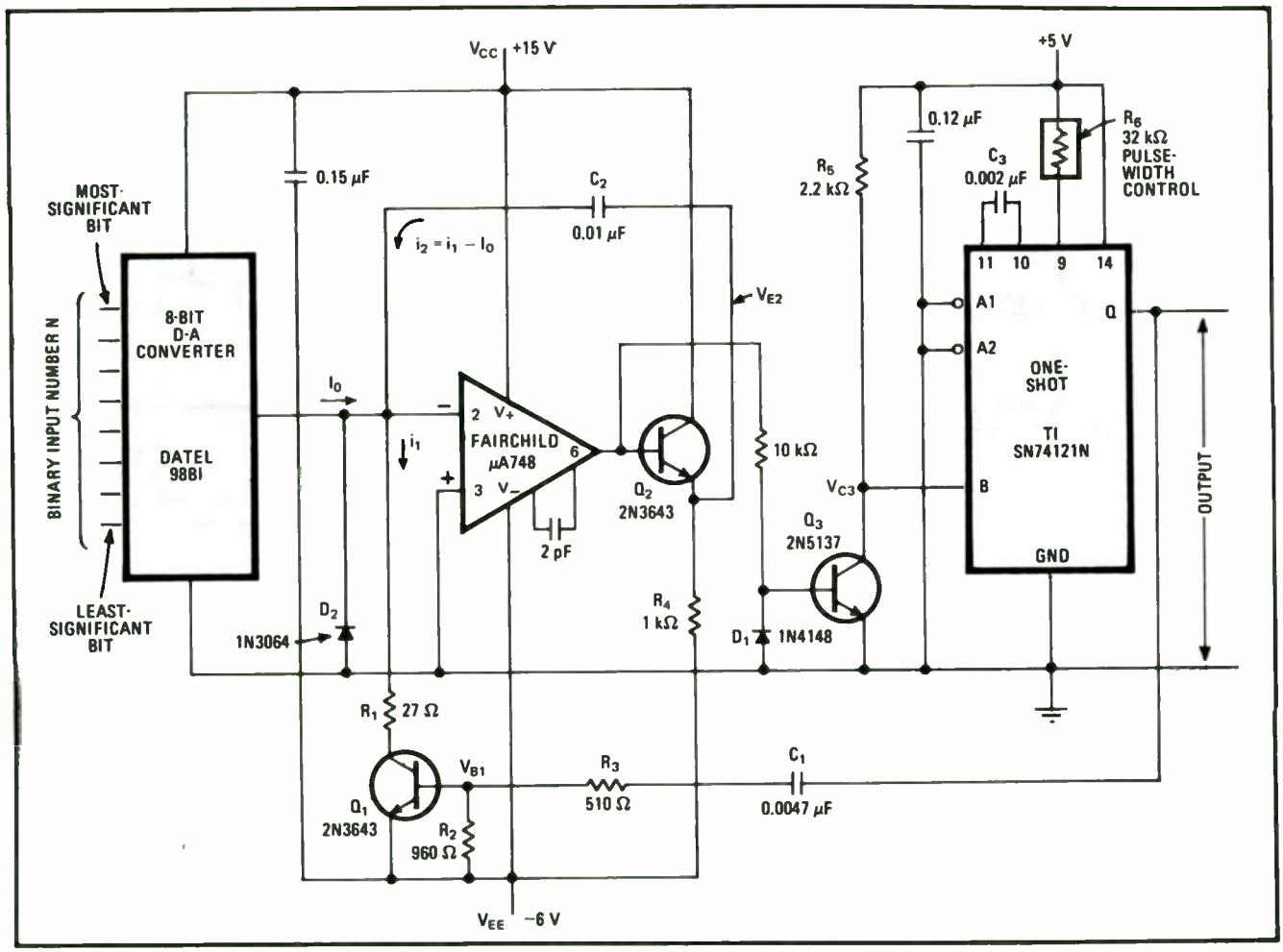
where:

$$I_o = kNV_{CC}$$

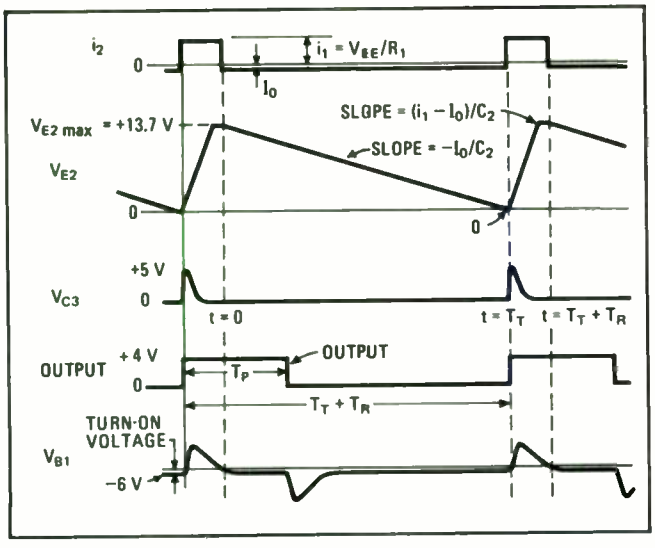
where k is a constant (0.68 micromho), and N is the input binary number. The output-pulse frequency can be written as:

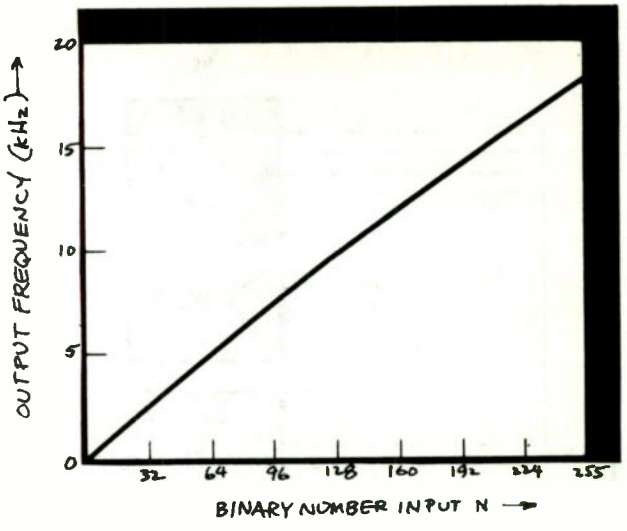
$$f = 1/(T_T + T_R)$$

When the recovery time is much smaller than the total period, as is the case here, the output frequency for the



Digitally variable. Pulse generator offers adjustable output frequency and output pulse width; pulse frequency changes linearly with the binary input. When transistor Q_1 is off and transistor Q_2 on, converter output current discharges integrator capacitor C_2 until transistor Q_3 turns off. This triggers the one-shot, producing an output pulse and turning on transistor Q_1 so that capacitor C_2 can charge up.





pulse generator can be approximated by:

$$f = kN/C_2$$

which is linear with respect to input number N, as indicated by the plot. Output-pulse width is variable and is given by:

$$T_P = 0.69R_6C_3$$

The largest value of T_P is limited by the one-shot's recovery time, as well as by the fact that T_P should be greater than the recovery time but smaller than the total period.

Diode D_1 prevents the base-emitter voltage of transistor Q_3 from exceeding its reverse breakdown rating. Diode D_2 protects the d-a converter from possible damage from a large negative voltage at its output. □

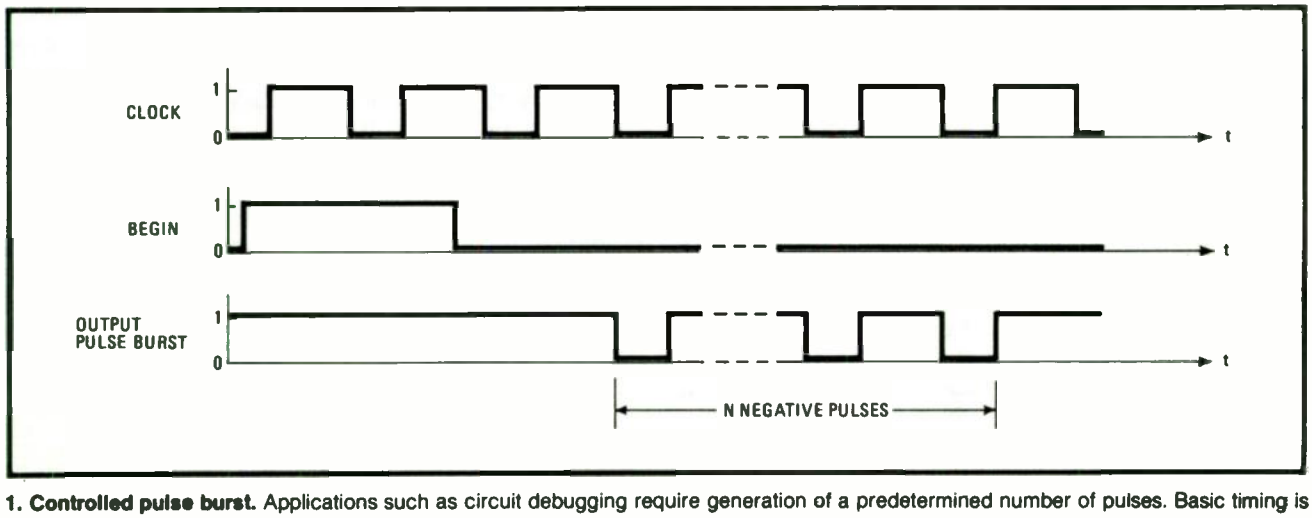
Pulse generator produces programable burst

by John F. Wakerly
Stanford University, Stanford, Calif.

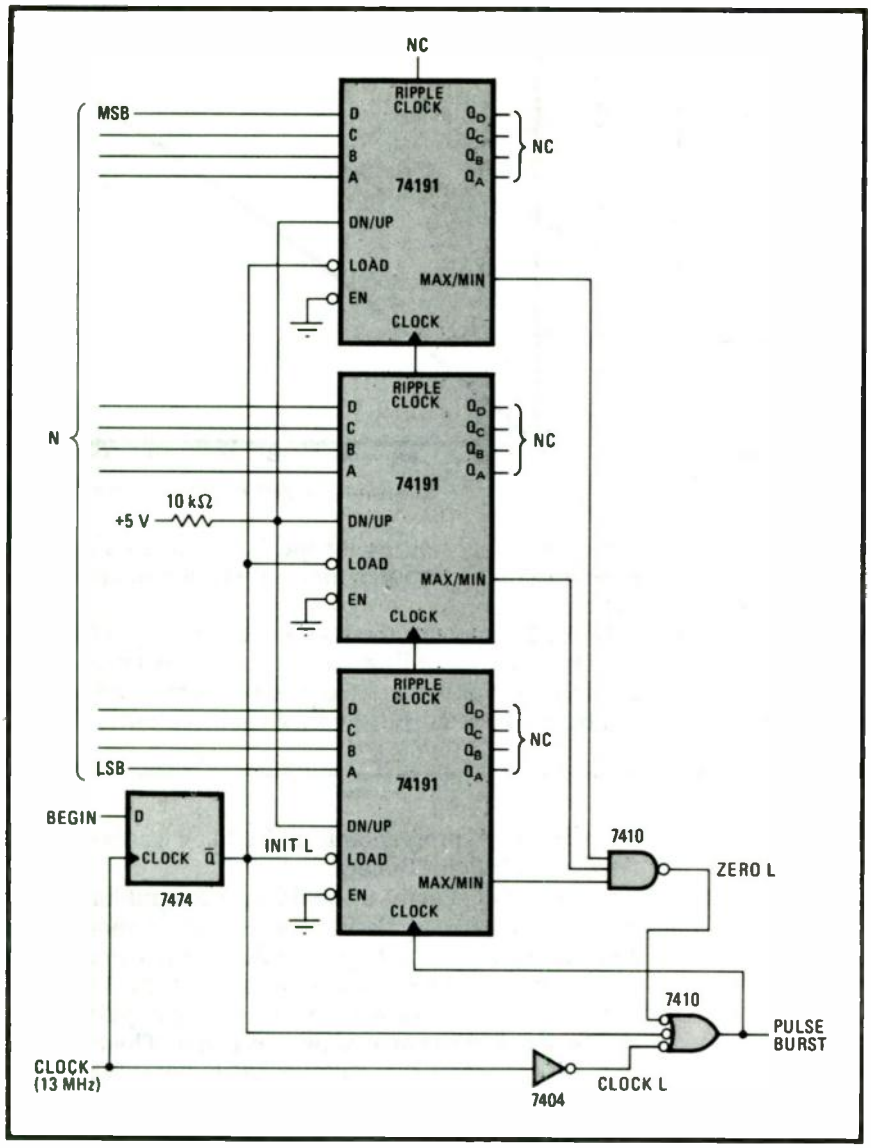
In debugging digital circuits it's often desirable to pass a predetermined number of pulses from a free-running clock and then stop, without producing any shortened pulses or glitches. There are also many systems, such as graphics interfaces, where such a capability may need to be built in. A programable pulse-burst generator is a circuit that fulfills this need.

This kind of generator should have n input lines to set N, the number of pulses to be passed. It should also have a begin input to begin a pulse burst, a clock input for the free-running input clock, and a pulse-burst output for the programed number of output pulses. The circuit should behave as shown in Fig. 1. The begin input is not synchronized with the clock, but it is assumed to be asserted for at least one clock period. The pulse-burst output is normally high; after begin is asserted and then de-asserted, N negative pulses are produced at this output in synchronization with the clock input.

A circuit that has the desired behavior has been built



1. Controlled pulse burst. Applications such as circuit debugging require generation of a predetermined number of pulses. Basic timing is provided by a free-running clock, and the pulse burst is initiated by a begin signal that lasts for at least one clock period. Note that the negative output pulse sequence follows the first rising clock pulse after the begin command goes low.



2. Compact circuit. This arrangement has 12 input lines, and therefore can produce pulse bursts of any length less than 2^{12}; for example, if the binary input number N is 000000000100, the output burst consists of four negative pulses. The circuit shown uses few packages. It operates at clock rates up to 13 MHz at room temperature and up to 10 MHz under any conditions. Adding more counters enables it to produce longer pulse bursts, while changing the counter type adapts it for BCD inputs.

from commercially available MSI counters (see Fig. 2). In this circuit n = 12, so that any burst of length less than 2^{12} can be generated. Three 74191 up/down counters are used to form a 12-bit down-counter. A D-type flip-flop is used to synchronize the begin and the clock inputs. The flip-flop output labelled init L (where L indicates active low) is used to load the counters with the number N and to hold the pulse-burst output high while the counters are being loaded. When the begin signal is removed, the counters count and the pulse-burst output passes pulses as long as the zero-low signal is high. The zero-low signal is derived from the max/min outputs of the counters and is used to hold the pulse-burst output high when the counters have counted down to zero. Thus, if the counters are loaded with N, exactly N negative pulses are passed before the counters count down to zero. Note that the circuit behaves properly even for N = 0.

For the circuit to work properly, all changes of zero-low must take place while clock-low is low. This sets a minimum time that the clock input must be high—about 50 ns typically for the parts shown. This time is computed as the sum of the delay of the 74191 counter clock to the max/min terminal and two TTL gate delays.

The generator can be extended to handle longer bursts by simply cascading more 74191 counters and using a wider NAND gate to produce the zero-low signal. The cascading can always be done with the ripple-carry outputs as in Fig. 2 without degrading the maximum system speed because only the least significant counter is active when the critical transition of the zero-low signal from high to low is made. At this time, the max/min outputs of all other counters have long since been high; on all other transitions, the max/min output of the next lower-order counter goes low before any max/min output goes high, holding the zero-low signal high.

The programable pulse-burst generator of Fig. 2 can be made to accept binary-coded-decimal inputs by simply substituting 74190 BCD counters for the 74191s. Positive pulses can be produced instead of negative by simply inverting the pulse-burst output. □

Bootstrap circuit generates high-voltage pulse train

by Lawrence H. Bannister
Center for Space Research, MIT, Cambridge, Mass.

A circuit can easily be built to generate a high-voltage pulse train from a low-voltage power supply. Such a circuit is used in a recently developed spacecraft instrument to generate a 400-hertz square wave with an amplitude of 4 kilovolts from 20 identical 200-volt stages connected in series. A high-voltage supply is not needed because each stage includes a capacitor that functions as a floating power supply for the next stage. These capacitors are charged in parallel and then connected in series so that the pulse generator does its own dc-to-dc conversion.

The schematic of Fig. 1 is drawn to emphasize the modularity of the circuit. To simplify the explanation, it is assumed that all transistors and diodes are perfect switches, having infinite impedance when turned off and zero voltage-drop when turned on.

Suppose, first, that transistors $Q_{1\text{-}1}$, $Q_{1\text{-}2}$, . . . $Q_{1\text{-}N}$ are all turned off. Then diodes $D_{1\text{-}1}$, $D_{1\text{-}2}$, . . . $D_{1\text{-}N}$ are forward-biased and transistors $Q_{2\text{-}1}$, $Q_{2\text{-}2}$, . . . $Q_{2\text{-}N}$ are driven to saturation. Capacitor $C_{1\text{-}1}$ charges through the path $D_{3\text{-}1}$, $C_{1\text{-}1}$, $D_{2\text{-}1}$, and $Q_{2\text{-}1}$. Concurrently, $C_{1\text{-}2}$ charges through the path $D_{3\text{-}2}$, $C_{1\text{-}2}$, $D_{2\text{-}2}$, and $Q_{2\text{-}2}$. So, in this circuit condition, all of the capacitors charge in parallel, and the potential difference across each capacitor is equal to the supply line voltage of 200 volts:

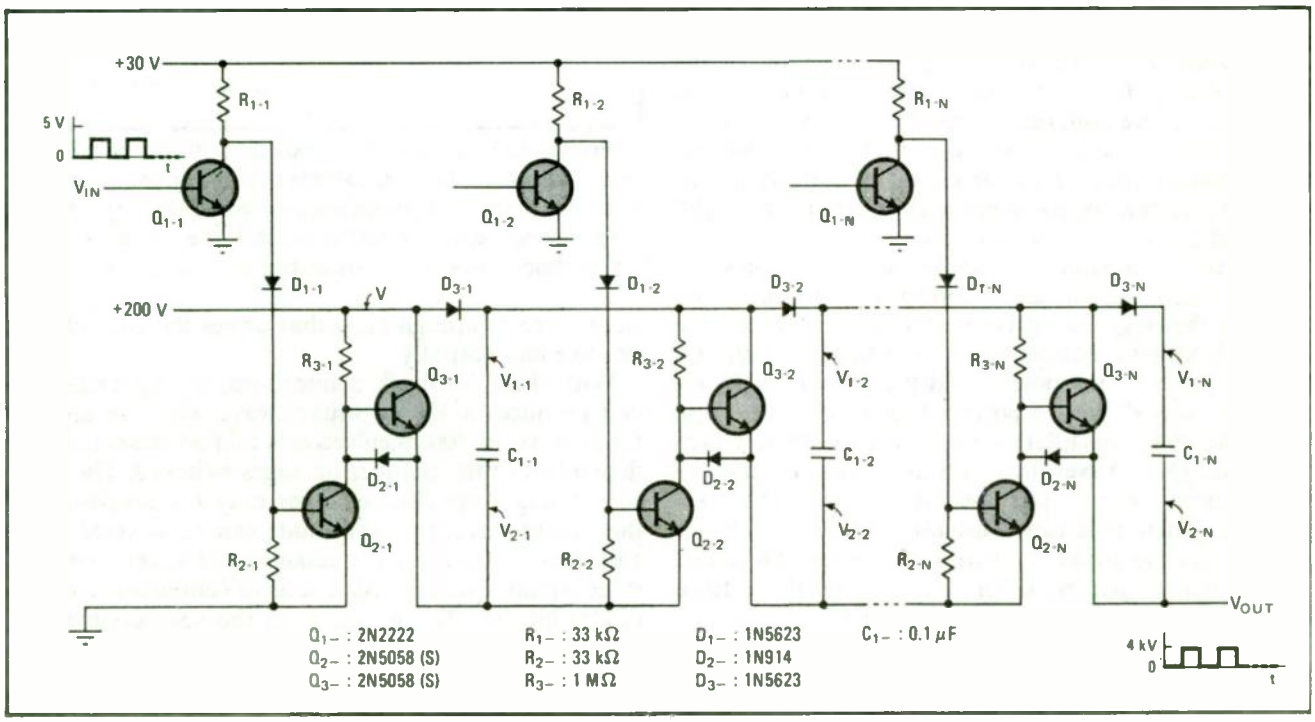
$$V_{1\text{-}N} = V_{1\text{-}2} = V_{1\text{-}1} = V = +200\ v$$
$$V_{out} = V_{2\text{-}N} = V_{2\text{-}2} = V_{2\text{-}1} = 0$$

If, now, $Q_{1\text{-}1}$ is turned on, diode $D_{1\text{-}1}$ no longer conducts, so $Q_{2\text{-}1}$ turns off. Current through resistor $R_{3\text{-}1}$ then causes $Q_{3\text{-}1}$ to turn on, and the emitter potential of $Q_{3\text{-}1}$ approaches its collector potential so that $V_{2\text{-}1} = V = +200$ v. And, because $C_{1\text{-}1}$ was previously charged to the supply voltage, $V_{1\text{-}1} = V_{2\text{-}1} + V = 2V = +400$ v.

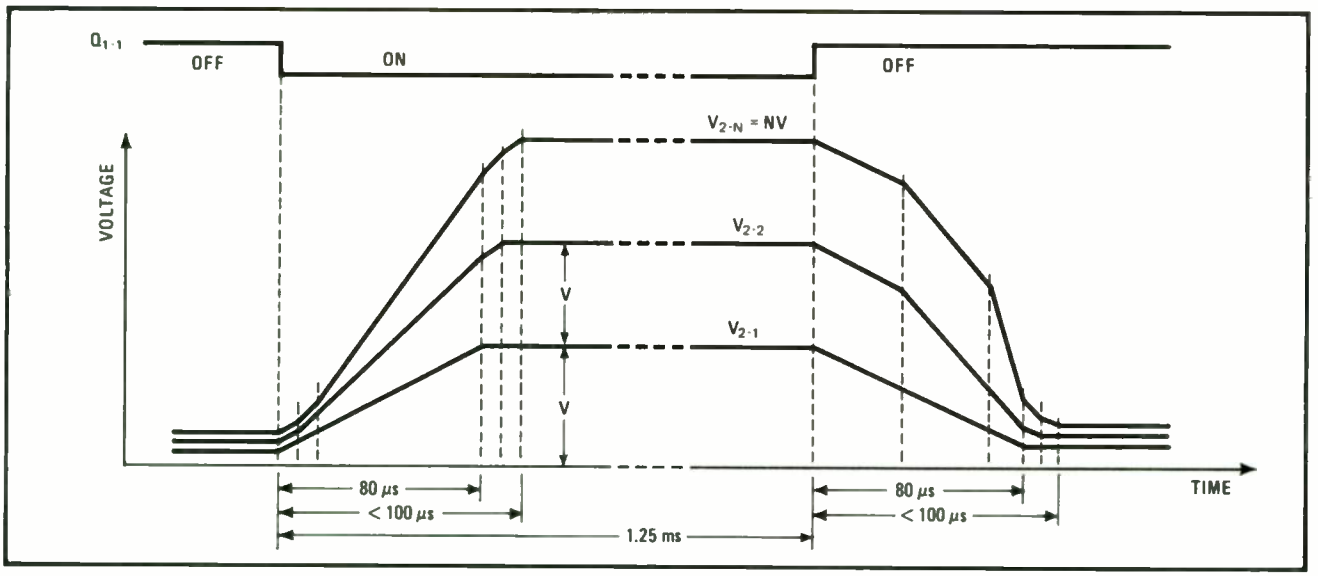
Now, regardless of the state of $Q_{1\text{-}2}$, when $V_{2\text{-}1}$ becomes positive, $D_{1\text{-}2}$ becomes reverse-biased, and therefore $Q_{2\text{-}2}$ turns off. Current through $R_{3\text{-}2}$ then causes $Q_{3\text{-}2}$ to turn on, and the emitter potential of this transistor approaches its collector potential so that:

$$V_{2\text{-}2} = V_{1\text{-}1} = 2V = +400\ v$$
$$V_{1\text{-}2} = V_{2\text{-}2} + V = 3V = +600\ v$$

As illustrated by Fig. 2, this sequence continues along the series of stages, each stage increasing the positive level of the pulse by V volts. The final output voltage is NV volts, where N is the number of stages and V is the



1. Kilovolt generator. Square wave of 4 kV at 400 Hz is produced by circuit with 20 low-voltage stages. Each stage includes a capacitor (C_1) that acts as a floating power supply for the next stage. The capacitors are charged in parallel and then connected in series. If lower output voltage is desired, input can be applied to $Q_{1\text{-}2}$ or $Q_{1\text{-}3}$ or . . . instead of $Q_{1\text{-}1}$. (Actual circuit also includes elements shown in Fig. 3.)



2. Timing. The stages start switching sequentially, as diodes $D_{1\text{-}1}$, $D_{1\text{-}2}$, . . . successively become back-biased, but after all stages are switched, they change voltage levels concurrently. Therefore the rise time is essentially that of a single stage. Similarly, the fall time is essentially independent of the number of stages. The output amplitude is the product of the power-supply voltage and the number of stages.

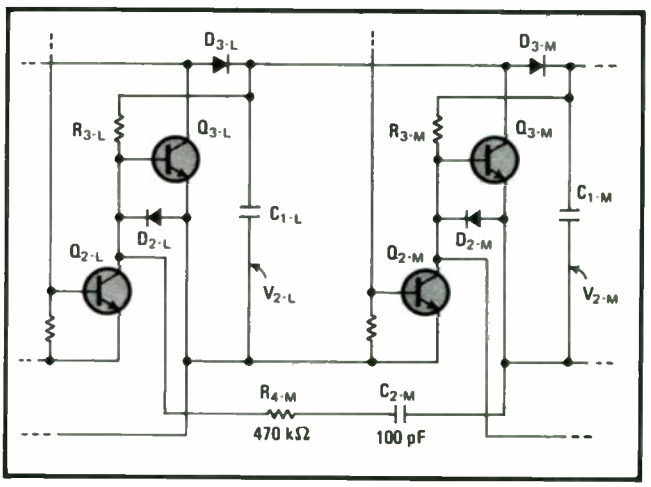
supply voltage. Because the stages switch concurrently, the total pulse rise time is only slightly longer than the rise time of one stage.

Smaller-amplitude pulses can be generated by switching only the last few stages to the "high" state. For example, if $Q_{1\text{-}1}$ remains off, but $Q_{1\text{-}2}$ is turned on, the first stage will remain in the "low" state with $V_{1\text{-}1}$ = V = +200 v but all subsequent stages will switch to the "high" state so that V_{out} = (N - 1)V. If only $Q_{1\text{-}N}$ is turned on, the preceding stages will remain in the "low" state and the output pulse amplitude will just be V volts. Generally, then, the output-pulse amplitude can be selected in increments of V up to a maximum of NV.

The positive-going edge of the pulse generated by the circuit of Fig. 1 is quite slow because, in each stage, when Q_2 is turned off, the potential at the base of Q_3 increases exponentially toward a limiting value. Further, the output impedance of the circuit is quite large because the current in R_3 approaches zero in the "high" state and Q_3 never really saturates.

The circuit modification shown in Fig. 3 prevents these problems by the use of positive feedback in and between the stages. R_3 is connected to provide positive feedback within the stage; when Q_2 is turned off and Q_3 starts to conduct, the potential at the top end of R_3 remains V volts above the potential at the emitter of Q_3. Thus, the potential difference across R_3 is sensibly constant, and Q_3 is driven by a constant current supply so that its base potential increases linearly until the base-collector junction is forward-biased. Q_3 then behaves like an inverted switch transistor with a very low offset voltage that is just the difference between the voltage drops of the base-emitter and base-collector diodes.

R_4 and C_2 provide positive feedback from one stage to the immediately preceding stage to speed the switching action. For example, when the stages switch to the "high" state, $V_{2\text{-}L}$ increases toward LV while $V_{2\text{-}M}$ increases toward MV. The difference between these voltages, MV - LV = (L+1)V - LV = V, causes a transient current through $R_{4\text{-}M}$ that drives the base of $Q_{3\text{-}L}$ positive more rapidly.



3. Feedback. To achieve 400-Hz operation, the circuit in Fig. 1 is modified as shown here. R_3s provide positive feedback within each stage, and R_4s and C_2s provide positive feedback from each stage to the preceding stages. Without the feedback, rise time is about 1 ms; with feedback, rise and fall times are both less than 0.1 ms.

With these feedback connections, the operating circuit produces a 400-Hz square wave with rise and fall times of about 100 microseconds that are essentially independent of the number of stages switched. The number of stages switched changes only the amplitude of the square wave; this amplitude can be selected in increments of 200 v, up to a maximum of 4,000 v for a 20-stage circuit. The only high-voltage components are the diodes labelled D_1 in Fig. 1. In the spacecraft instrument, series strings of diodes are used as D_1 to provide the necessary isolation for the higher-voltage stages of the pulse generator. □

Delay line in shift register speeds m-sequence generation

by J.T. Harvey
Amalgamated Wireless (Australasia) Ltd., North Ryde, Australia

The clock rate of a shift-register generator of maximal-length pulse sequences is significantly increased when a delay line replaces one or more of the register's stages. High-speed m-sequences, as maximal-length pulse sequences are called, are needed for testing data links, for generating repeatable pseudo-noise, and in spread-spectrum techniques.

Repetitive sequences of pulses can be generated by connecting the output of a shift register back to the input in some way, setting in some initial condition that is not all zeroes, and turning on the clock. In this situation, the length of the repeating pulse sequence that emerges from the register depends upon the feedback arrangement and perhaps upon the initial condition—if the register has N stages, the sequence may repeat after only two, N, or some other number of pulses.

However, the m-sequence is independent of the starting condition. This follows from two facts. First, its length is $2^N - 1$ pulses (the all-zero condition never appears in the register). Second, its generation involves every possible combination of 1s and 0s in the shift register except for the all-zero combination.

A typical m-sequence generator is shown in Fig. 1. The feedback signal in the four-stage device is obtained by taking the exclusive-OR (XOR) of the outputs from the last and next-to-last flip-flop stages. The resulting sequence repeats after $(2^4 - 1)$ bits, i.e., 15 bits. It goes 1, 1, 0, 0, 0, 1, 0, 0, 1, 1, 0, 1, 0, 1, 1, and then repeats. Various feedback combinations must be used to achieve the maximum-length pulse sequence from registers with various numbers of stages, but it is of interest to note that generators having 2, 3, 4, 6, 7, or 15 stages can operate by feeding back the XOR of the outputs from the last and next-to-last stages.

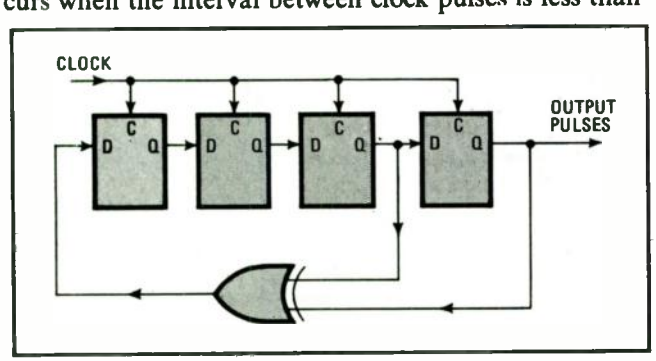
The limit to high-speed operation of this device occurs when the interval between clock pulses is less than the combined effective propagation delay in a shift-register stage and the XOR gate. For a given family of logic, the propagation time of the XOR is typically slightly less than that of a shift-register stage. Thus, the clock rate at which an m-sequence generator can operate is typically 0.5 to 0.7 of the rate at which the shift register can operate alone.

Provided that operation is required over a limited range of clock frequency (most are operated at a fixed clock rate), then the first stage of the shift register can be removed and a delay line substituted. This arrangement is shown in Fig. 2. The optimum delay is the interval between clock pulses less the exclusive-OR-gate propagation delay. The gate and delay line thus simulate a delay-free gate and one shift-register-stage delay. The maximum frequency of operation is then the maximum shifting rate of the flip-flops.

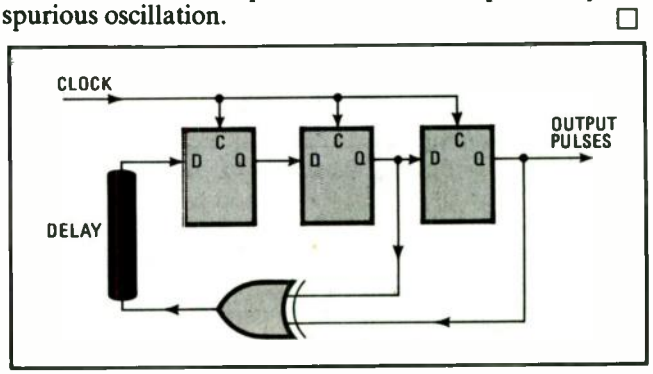
To demonstrate this idea, some experiments were conducted with MECL III logic, for which 270-megahertz flip-flop clock rate and 2.7-nanosecond gate propagation time worst-case figures are claimed. A pair of MC1670L D-type flip-flops were connected in a ring counter, which was observed to operate to 310 MHz. The same shift-register was used in a two-stage m-sequence generator with the addition of an MC1672L XOR gate, one section of which was used as an output buffer. At this point, the maximum clock rate was found to be only 215 MHz. Then this generator was converted to a three-stage device by the addition of a 20-cm length of 50-ohm coaxial cable, and satisfactory operation was observed in the range from 220 to 310 MHz, giving a speed improvement of up to 44%.

The susceptibility of the circuit to noise will be greatest near these speed limits. When a 90-cm length of cable was used, four-stage operation was observed in the range from 245 to 310 MHz, and a 220-cm length gave six-stage operation (63-bit sequence) at frequencies from 265 to 310 MHz. Similarly, 260 cm of coaxial cable yielded a seven-stage 127-bit sequence for clocks from 275 to 310 MHz.

For a given number of stages, an increase in the external delay decreases the upper and lower clocks in roughly the same ratio, while an increase in the number of simulated stages decreases the range in the clock rate. At least one shift-register stage must be used in front of the first feedback tap to eliminate the possibility of spurious oscillation. □



1. Maximizes. Four-stage shift register with feedback arrangement cycles through all possible states except the all-zero condition, producing an output sequence of $2^4 - 1$ pulses. This is the maximum-length sequence (m-sequence) from a four-stage register. Speed of the m-sequence is limited by the propagation delay in the XOR gate.



2. Faster. In modified m-sequence generator a delay line simulates one stage of the shift register, so the output pulse sequence is the same as for the circuit of Fig. 1. The delay line is designed so it, plus the XOR gate, offers the same propagation delay as one register stage, permitting a 44% increase in clock rate for the m-sequence.

One-shot with feedback loop maintains constant duty cycle

by H.P.D. Lanyon
Worcester Polytechnic Institute, Worcester, Mass.

Electronic equipment often generates a sequence of fixed-length pulses with a variable repetition rate. A circuit can be built that adjusts the widths of the pulses to produce an output train with a constant duty cycle. The output-pulse rate is the same as the input rate, which can vary over a range of 1,000:1. This circuit can control device loading, for example, protecting a transistor from being driven beyond its safe dissipation rating.

The key element of the circuit is a 74121 one-shot multivibrator that is triggered by the input pulses. The normal programing resistor for the 74121 is replaced by a transistor that has its effective impedance changed by a feedback loop to maintain the desired duty cycle. The duty cycle is set by a single potentiometer.

As the circuit diagram indicates, the output from terminal 6 of the multivibrator is fed through resistor R_I to the inverting input of a 741 operational amplifier. This voltage, V'_O, is either high (V_H) or low (V_L). Potentiometer R_P sets the noninverting input to a reference potential, V_{REF}, so that the instantaneous current flowing through R_I is equal to $(V'_O - V_{REF})/R_I$. The value of R_I must be chosen so that this current does not exceed the 74121's limit of 400 microamperes. The current causes the feedback capacitor C_I alternately to charge and discharge, resulting in changes of the amplifier-output voltage V_f as a function of time.

If the instantaneous input period is τ and the output duty cycle is α, V'_O is in the high state for a time $\alpha\tau$ and in the low state for $(1 - \alpha)\tau$. The average current $\bar{i}$ through R_I is given by the formula

$$\bar{i}\tau = [(V_H - V_{REF})\alpha\tau + (V_L - V_{REF})(1 - \alpha)\tau]/R_I$$

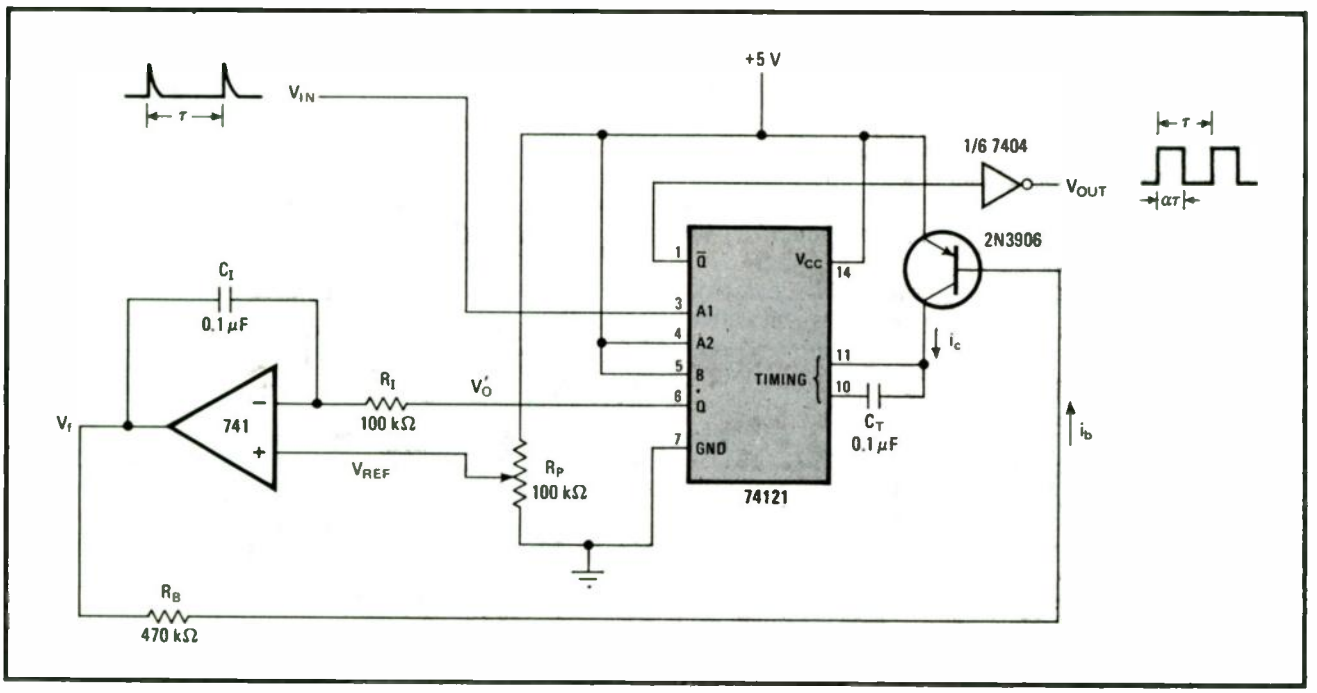
In steady-state operation, when the output waveform has the desired duty cycle α_{set}, the average current to the capacitor must be zero, maintaining a constant operating point from one cycle to the next. Therefore

$$\alpha_{set} = (V_{REF} - V_L)/(V_H - V_L)$$

i.e., the output duty cycle is independent of the input repetition rate $1/\tau$, and depends only on the values of V_{REF}, V_H, and V_L. In general, the values of V_H and V_L are dependent on the output loading. Therefore, to avoid loading problems at the output of the circuit, the output is taken from the $\bar{Q}$ output (pin 1) of the 74121 through an inverting gate (1/6 of a 7404) rather than from the Q output (pin 6).

If the instantaneous α of the circuit is greater than α_{set}, $\bar{i}$ is positive, and the amplifier's output voltage V_f becomes more negative during a complete cycle of operation. Conversely, if α is less than α_{set}, V_f becomes more positive. The time constant for response to such an imbalance is R_IC_I, which should be larger than the longest expected τ in normal operation to minimize the variations in V_f from its average value and ensure that the amplifier does not saturate at any point of the duty cycle. Normally V_f is between −14 V and +6 V.

Voltage V_f controls the base current of the 2N3906 pnp transistor, and thus controls the collector current that charges the 74121 one-shot multivibrator. The ef-



Constant duty cycle. Input to this circuit is a train of fixed-length pulses with variable repetition rate, but op-amp output voltage changes effective transistor impedance to maintain constant duty cycle over a 1,000:1 range of input-pulse frequency. Using the components shown, the on-time of the 74121 monostable can be changed from 30 μs to 30 ms, allowing a 33% duty cycle to be maintained from 10 to 10,000 baud. It is possible to vary the duty cycle all the way from 20% to 80% by the setting of potentiometer R_P.

fect of making V_f more positive is to decrease the base current, $(5 - V_{BE} - V_f)/R_B$, resulting in an increase in the effective resistance of the transistor. Since the duration of the on state is proportional to this resistance, the value of α increases to a value closer to α_{set}. The value of 470 kilohoms for R_B is chosen to limit the maximum collector current i_c to approximately 5 milliamperes, which is consistent with the currents through the programing resistors normally used with the 74121. Assuming a minimum transistor impedance of 500 ohms at the maximum repetition rate, the value of timing capacitor C_T is chosen to determine the length of the on pulse. The maximum value of transistor impedance appears to be about 500 kΩ, so a given choice of fixed components allows a 1,000:1 range of input frequencies.

The analysis of the circuit has stressed the average value of V_f, rather than the instantaneous departures from this value that occur in normal operation of the circuit. This approach is reasonable because the function of the feedback circuit is to supply charge to the capacitance C_T so that the 74121 switches on and off at the correct point of the cycle; the instantaneous variations in current during this charging period are not important in this function.

The operation of the circuit is not critically dependent on the values chosen for R_I, C_I, R_P, or R_B. Neither is it particularly dependent on the bandwidth of the operational amplifier or the linearity of the system in steady-state operation. The input-pulse train must be properly terminated, because reflections at the input can cause the circuit to maintain the required duty cycle with multiple triggering of the 74121. Therefore, a 50-ohm resistor should be hung across the multivibrator input if it is fed through a 50-ohm cable. □

Adjustable pulse generator features rate alarm

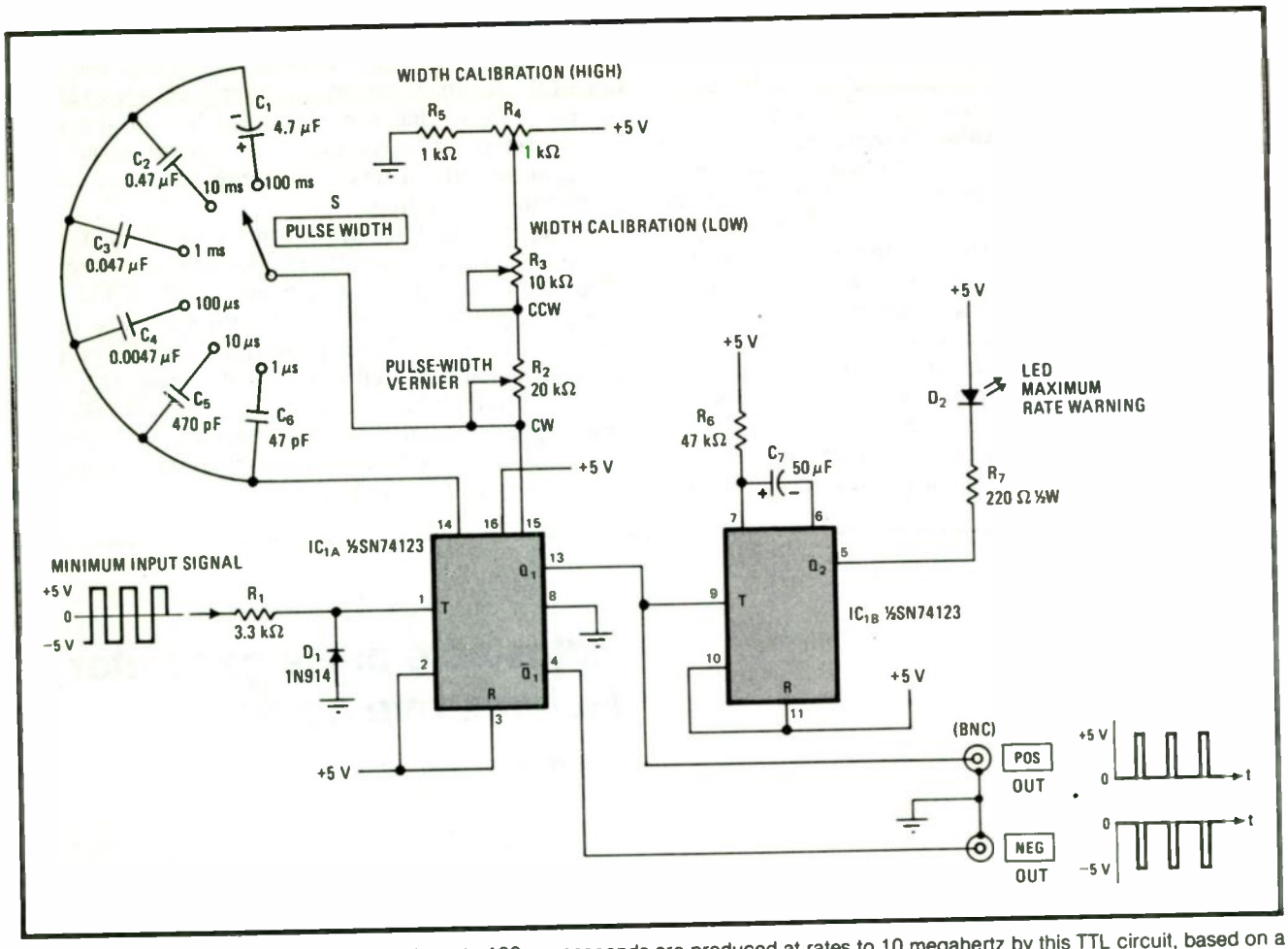
by Frank N. Cicchiello
Geometric Data Corp., Wayne, Pa.

A TTL dual monostable multivibrator integrated circuit driven by a clock emits pulses of either polarity with widths adjustable in six decade ranges from 100 nanoseconds to 100 milliseconds. Output rise and fall times of the pulses are 15 ns or less, and the frequency can be greater than 10 megahertz. The most novel feature of the generator, however, is a maximum-pulse-rate indicator light that switches on if the clock rate is increased so that it is no longer compatible with the pulse width; that is, if the clock period is equal to or less than the pulse width.

Each negative-going transition of the clock signal applied to resistor R_1 causes one pulse to be generated by the one-shot multivibrator, IC_{1A}. Pulse width is determined by the circuit time-constant R_PC_P, where C_P is any capacitor from C_1 to C_6, and R_P is the sum of R_2 through R_5. Positive-going output pulses are available from IC_{1A}'s Q output, and negative-going ones from its $\bar{Q}$ output.

If the rate of the incoming clock signal is so high that its period is less than the desired pulse width, IC_{1A} is retriggered during its pulse-forming time (this type of one-shot multivibrator is retriggerable at any point in its operating cycle). Retriggering keeps the output of IC_{1A}, which is connected to the input of the second one-shot circuit, IC_{1B}, constantly at +5 volts. If IC_{1B} is untriggered for a time equal to its time-out period (approximately 2 seconds for listed values of R_6 and C_7), the output of IC_{1B} switches to ground level at Q_2, and the light-emitting diode lights.

The circuit includes potentiometers for vernier adjustment of pulse width and for calibration. The procedure is as follows:



Fast and narrow. Adjustable-width pulses down to 100 nanoseconds are produced at rates to 10 megahertz by this TTL circuit, based on a single dual-monostable integrated circuit driven by any suitable clock. If the input clock rate is raised so high (or the output pulse width is made so small) that the width exceeds the period, Q_2 goes low and lights the warning LED.

1. Adjust input clock frequency to 500 Hz.
2. Set switch S to 1-ms position.
3. Set R_3 to midrange.
4. Set R_2 to full clockwise (cw) position.
5. Adjust R_4 for 1-ms output-pulse width.
6. Set R_2 to full counter clockwise (ccw) position.
7. Adjust R_3 for 100-microsecond output-pulse width.

Repeat steps 4–7 until the rotation of R_2 from full counterclockwise to full clockwise changes the width of the output pulse from 100 μs to 1 ms.

The warning indicator can be checked by switching switch S to the 10-ms position. The indicator will light until the output pulse width is less than 1 ms.

Any function generator can provide a suitable clock signal. If a bipolar generator is used, diode D_1 eliminates negative pulses. □

43. Rectifiers

Rectifying wide-range signals with precision, variable gain

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz.

Millivolt-level signals cannot be rectified directly because they are smaller than the typical 0.7-volt drop across a forward-biased diode. An operational amplifier can reduce this loss to around 10 microvolts. But such circuits have a fixed gain when designed straightforwardly, whereas variable gain is needed for range control in many applications—amplitude detection in ac voltmeters, for example.

Varying the gain has usually required either the adjustment of more than one resistor or, in very complex circuits, the use of a separate input amplifier. With the precision rectifier shown in the diagram, however, variable gain is achieved without a gain-control amplifier.

Gain is controlled by a single variable resistor, which can be a potentiometer or a multiple-tap resistor. In addition, this circuit has a high input impedance without an input buffer and requires only one resistance match. It has a gain range from unity to several thousand, for signals from 1 millivolt to 10 v.

Rectification results when the feedback diodes are switched by a reversal of the signal polarity, which in turn reverses the circuit gain polarity. With the diodes in one orientation, the signal path to the output is a noninverting amplifier; when they switch, it becomes a voltage follower and an inverting amplifier.

An input of positive signals produces a positive current i_1 that turns diodes D_2 and D_3 on and D_1 and D_4 off. This connects the noninverting amplifier A_1 to the output with a gain of $1/x$, where x is a fraction representing the potentiometer setting. In this mode A_2 is merely a ground return for the resistance xR_1; its output is disconnected from the circuit output by the reverse-biased diode D_4. Thus the circuit output, controlled by A_1 alone, is $e_o = e_i/x$.

When the input signal swings negative, so does the current i_1. It switches off D_2 and D_3 and turns on D_1 and D_4. Now the output of A_2 is connected to the circuit output, and A_1 merely maintains a signal equal to e_i at its own inverting input. In doing so it also develops this signal across the resistance xR_1. That resistance acts as the input resistor to A_2, connected as an inverting amplifier. With a gain of $-1/x$, this inverting amplifier develops $e_o = -e_i/x$, the negative of that produced by positive signals. Since the polarity of the gain switches with that of the input signals, the output signal is always positive, and $e_o = |e_i/x|$.

Gain can be varied from unity to several thousand to accommodate a wide range of signal levels. To insure continually equal gain for positive and negative signals, it is only necessary to match the resistor R_2 to the total potentiometer resistance R_1. Op amp gain error directly affects circuit gain, but identically for both positive and negative signals.

Otherwise, circuit accuracy depends upon the noises, dc errors, and ac responses of the op amps. Noise isn't generally a major source of error in the practical signal range of 1 mV to 10 V, as long as the resistance levels are low enough to limit the effects of noise currents at the amplifier inputs.

Ideally, the diodes would switch just as the input signal crosses zero, but the op amps' dc offset voltages—the input levels below which the amplifiers produce no outputs, as a result of mismatched transistors in the amplifiers—cause the circuit to depart from this ideal. The error currents are:

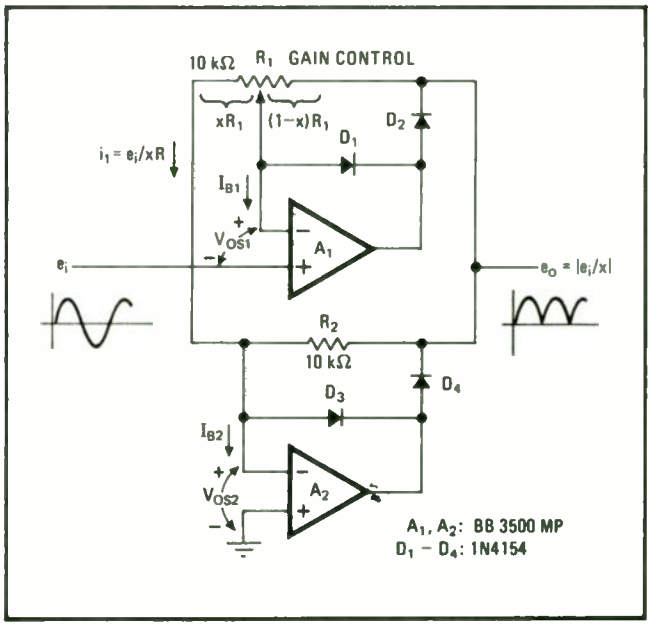
$$(V_{os1} - V_{os2})/xR_1 + I_{B1}$$

and

$$(V_{os1} - V_{os2})/xR_2 - I_{B2}$$

This switching-point offset limits the circuit's operation with very small signals. To extend it, the amplifiers are chosen for low bias currents, and the op-amp offset voltages are nulled. Matched op amps insure low initial dc errors and thermal drifts.

Another output offset is produced by input currents flowing through the feedback resistances. This offset cannot be removed by the op-amp null controls without again offsetting the diode switching, but it is minimized



Precision rectifier. Variable gain is achieved without a separate gain-control amplifier, since the control potentiometer varies the gains of both amplifiers identically. Circuit gain ranges from unity to several thousand. Forward or reverse biasing of diodes make the circuit either an inverting or noninverting amplifier.

by the choice of suitable op amps and resistances.

High-frequency performance is limited by the speed with which the op-amp outputs can turn off one rectifying diode and turn on the other. While the first diode is being turned off, the signal with the wrong polarity passes, and while the second diode is turning on, no signal passes. Ideally, this transition should be instantaneous, but in practice it always takes a finite time, limited by the operational amplifiers' slewing rates and their bandwidths, which are expressed by the speed with which the amplifiers can swing their outputs through two diode voltage drops, $2V_f$.

If the input signal is small, the rate of change of the amplifier output voltages equals the rate of change of the input signal multiplied by the open-loop gain of the amplifier at the signal frequency, $A(f_i)$, and therefore the transition time is the time required for the input signal to change by $2V_f/A(f_i)$. For larger signals the rate of change of the amplifier output voltage can be no more than its slewing rate limit S_r, so that the transition time is $2V_f/S_r$. These considerations limit the usable bandwidth of the precision rectifier to about 1 kilohertz. □

Comparator and D-MOS switch rectify small signals linearly

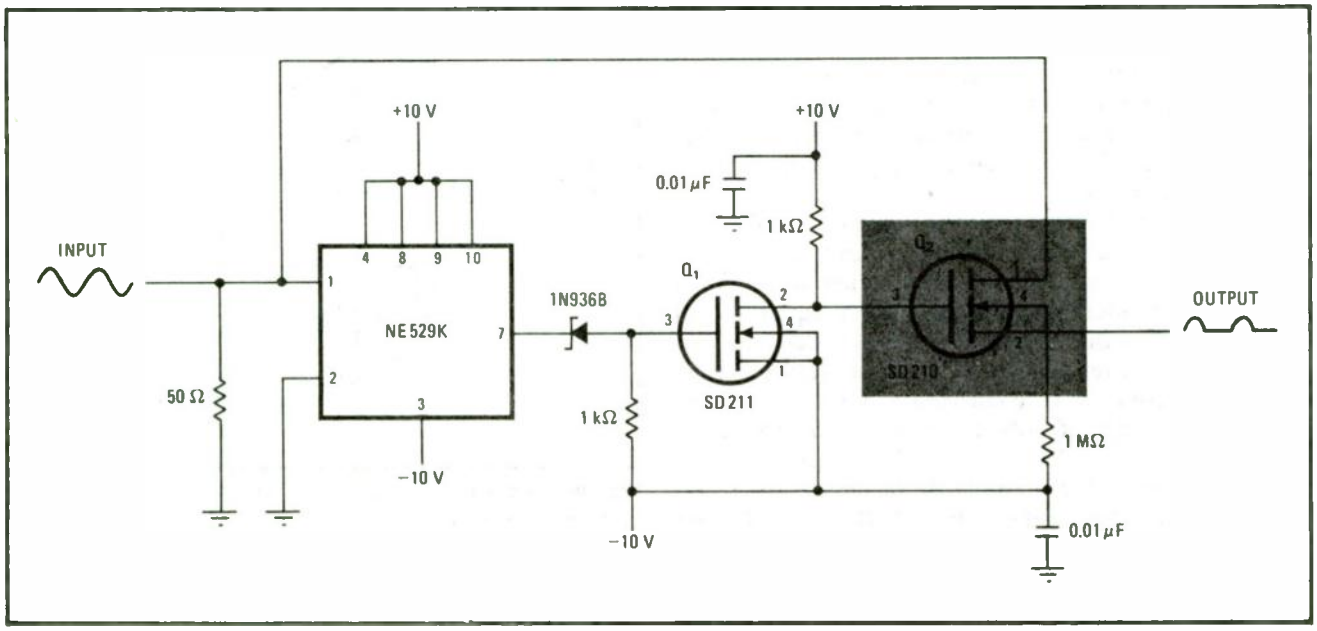
by Tom Cooper
TRW Systems, Redondo Beach, Calif.

Rectifying low-level signals with conventional silicon diodes has always been cumbersome. The reason: input signals lower than the diode's turn-on voltage of approximately 0.6 volt result in a nonlinear output that is generally made linear by the addition of one or two operational amplifiers. But if an analog comparator and a two-FET switch are used instead of the silicon-diode-and-amplifier combination, it's possible to rectify waveforms with amplitudes as low as 6 millivolts at frequencies as high as 3 megahertz, while providing an output that can be filtered to yield a dc value directly proportional to the amplitude of the input signal.

The circuit is shown below. In this precision half-wave rectifier, the input signal is applied to field-effect transistor Q_2 and also to the NE529 high-speed comparator (20-ns propagation delay), which senses the zero crossings of the input voltage. The output from the comparator passes through a level-setting zener diode and drives a high-speed analog switch (2-ns turn-on time) that consists of double-diffused metal-oxide-semiconductor (D-MOS) FETs Q_1 and Q_2. The comparator and Q_1 drive Q_2 into the on state at each positive zero crossing of the input waveform that is to be rectified, and into the off state at each negative zero crossing.

Because Q_2 is on when the input signal applied to its source terminal is positive and is off when the input is negative, the output from Q_2 is a half-wave-rectified version of the input waveform. □

Half-wave rectifier. Analog switch Q_2 is driven on and off at the zero crossings of the low-level input signal, producing a precise half-wave-rectified version of the input waveform. Amplitude can be as low as 6 mV and frequency as high as 3 MHz.



Full-wave rectifier needs only three matched resistors

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz.

Precision rectifiers or absolute-value circuits will accurately rectify even a millivolt-level signal for applications requiring precise magnitude detection. But because of their low input resistance, most of these circuits require many resistors to be matched. With the precision rectifier drawn in the figure, however, a high input impedance can be achieved without the addition of a buffer amplifier—and only three resistors have to be matched.

In an absolute-value conversion, the input signal is converted from a bipolar form to a unipolar form, a standard requirement for magnitude detection in many average-reading measuring instruments. There are several absolute-value circuits that can be built with an operational amplifier to obtain the desired high accuracy for full-wave rectification.

In these circuits, rectification is carried out without sacrificing a significant portion of the input signal to forward-bias the rectifying diodes. These diodes are placed in the op-amp's feedback loop so that the high gain of the op amp reduces signal loss. This means that only very small signal changes are needed to drive the diodes into and out of conduction, and millivolt-level signals can be rectified.

Most precision rectifier circuits have a low input impedance, which is set by input summing resistors, so that a buffer amplifier must often be added. However, the need for an additional op amp is avoided by the circuit shown because its input impedance is the common-mode input impedance of an op amp, and the usual input summing resistors are eliminated. This results in a typical input resistance either of 25 megohms for an op amp having a bipolar-transistor input or of 10^{12} ohms for an op amp having a FET input.

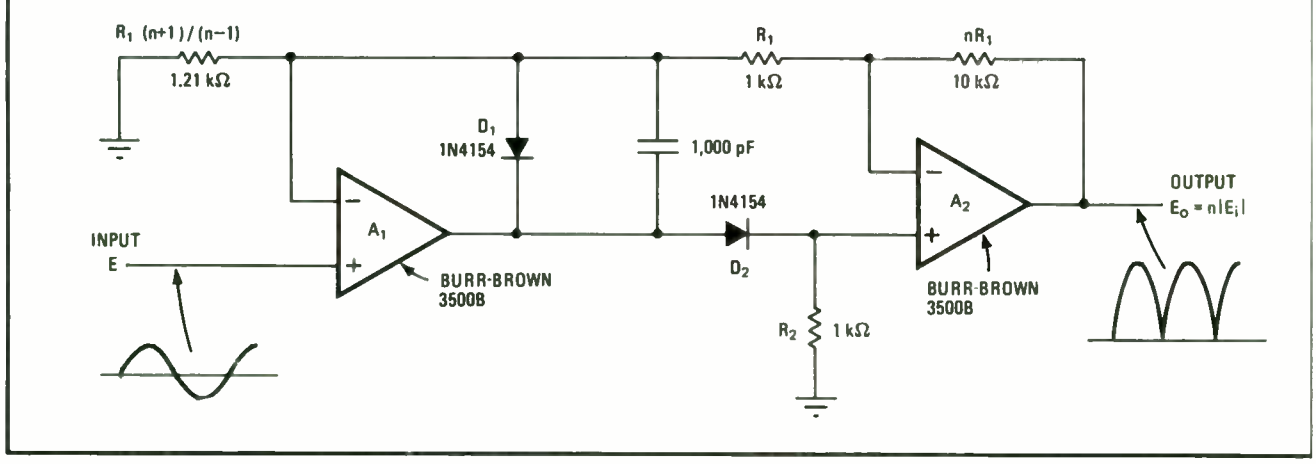
Full-wave rectification is produced by diode switching that reverses the polarity of the net circuit gain when the polarity of the input signal reverses. The polarity of the output signal is therefore prevented from changing. This feature, coupled with the circuit's equal-gain magnitude for input signals of either polarity, results in an absolute-value conversion.

Gain polarity is switched by the diodes as they alternate the connection of the output of amplifier A_1 between the two inputs of amplifier A_2. Positive input signals cause the output of A_1 to become positive, reverse-biasing diode D_1 and forward-biasing diode D_2. Since the output of A_1 is now connected to the noninverting input of A_2, amplifier A_2 provides a gain having a positive polarity.

Gain magnitude is controlled by three feedback resistors that are designated as multiples of R_1 in the diagram. Feedback forces the output of amplifier A_2 to the level that develops a voltage equal to E_i across the $R_1(n+1)/(n-1)$ resistor. For the positive-signal case, the associated gain (E_o/E_i) is n. Since both amplifiers are connected in a common feedback loop for the positive-signal mode, additional phase compensation may be required with the capacitor shown.

Negative input signals are amplified by a gain of opposite polarity. They cause the output of amplifier A_1 to swing negative, forward-biasing diode D_1 and reverse-biasing diode D_2. Now amplifier A_1 drives the inverting, rather than the noninverting, input of amplifier A_2. Because the noninverting input of A_2 is connected to ground through resistor R_2, A_2 acts as an inverting amplifier, providing a negative gain for the signal supplied by A_1.

With its feedback shorted by diode D_1, amplifier A_1 performs as a voltage-follower, supplying inverting am-



Improved rectifier circuit. High-accuracy full-wave rectifier requires matching only three resistors. The circuit has a high input impedance, without an extra buffer amplifier, because the common-mode input impedance of amplifier A_1 faces the circuit's input. For positive signals, amplifier A_2 is noninverting so that circuit gain is + n. For negative signals, A_2 becomes inverting, and circuit gain is −n.

plifier A_2 with a signal that equals input voltage E_i. The over-all circuit gain is now -n. Circuit gain, therefore, is switched from +n for positive signals to -n for negative signals.

The performance of the circuit is limited by a number of factors, including resistor matching, as well as the amplifiers' input offset voltages, input bias currents, fastest slewing rates, and maximum gains.

The input offset voltages and input bias currents introduce a deadband around zero, in addition to an output offset. These two errors are removed by first nulling the offset voltage of amplifier A_1 to eliminate the deadband, and then nulling the offset voltage of amplifier A_2 to get rid of the output offset. Because of the interaction of these two nulls, this procedure must generally be repeated. The slewing rate and gain of amplifier A_1 and the diode capacitances also create a deadband around zero that limits the upper rectification frequency.

Any deviation from the resistor-matching ratios indicated here will produce a gain error that, in some cases, will make the gain magnitudes different for the two input signal polarities. This gain error can be removed by first adjusting the circuit's gain for negative signals through trimming resistor R_1 or resistor nR_1. Circuit gain for positive signals can then be matched to the negative-signal gain by adjusting resistor $R_1(n+1)/(n-1)$. Prior to these gain trims, it may be necessary to null out any existing deadband error since this error can also produce unequal outputs for equal positive and negative input signals.

With the component values shown, the circuit can accept a maximum input voltage of 2 V peak-to-peak and produce a maximum output voltage of 10 V. Circuit gain is 10. □

BIBLIOGRAPHY

J. Graeme, "Applications of Operational Amplifiers—Third Generation Techniques," McGraw-Hill, 1973.

G. Tobey, J. Graeme, L. Huelsman, "Operational Amplifiers—Design and Applications," McGraw-Hill, 1971.

Op amp with feedback makes full-wave rectifier

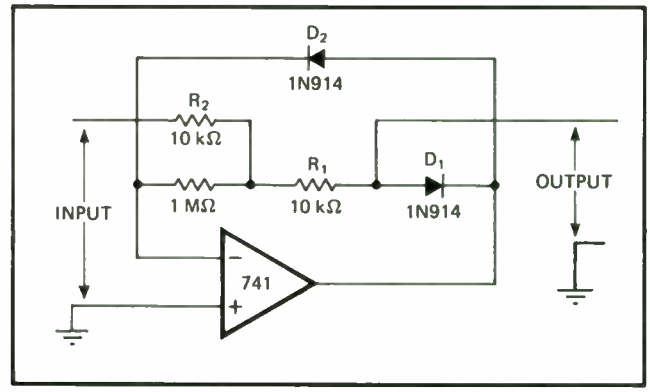
by Richard Knapp and Roger Melen

Stanford University, Palo Alto, Calif.

A feed-forward resistive element allows one operational amplifier to do the job of two op amps—perform full-wave rectification of low-level signals. The resulting circuit is useful for a wide variety of frequency-doubling and small-signal rectification applications, such as ac-to-dc converters, absolute-value detectors, and frequency multipliers.

For both positive and negative inputs, the op amp's inverting input is always at virtual ground. And for either input polarity, output voltage is developed by input current flow through feedback resistor R_1.

Diode D_1 is forward-biased during positive inputs, while diode D_2 remains off. Input current flows primarily through resistor R_1 to the output. During negative inputs, diode D_2 conducts and diode D_1 is off, maintaining the op amp's inverting input at virtual ground.



Full-wave rectifier. Inverting input of operational amplifier remains at virtual ground for both positive and negative input voltages so that output voltage is always developed by input current flow through feedback resistor R_1. Diode D_1 conducts only during positive inputs, and diode D_2 is on only for negative inputs. Normally, two amplifiers are required to perform full-wave rectification.

Circuit output impedance is approximately equal to the resistance of diode D_1 for positive voltages and to the sum of $R_1 + R_2$ for negative voltages. □

44. Security circuits

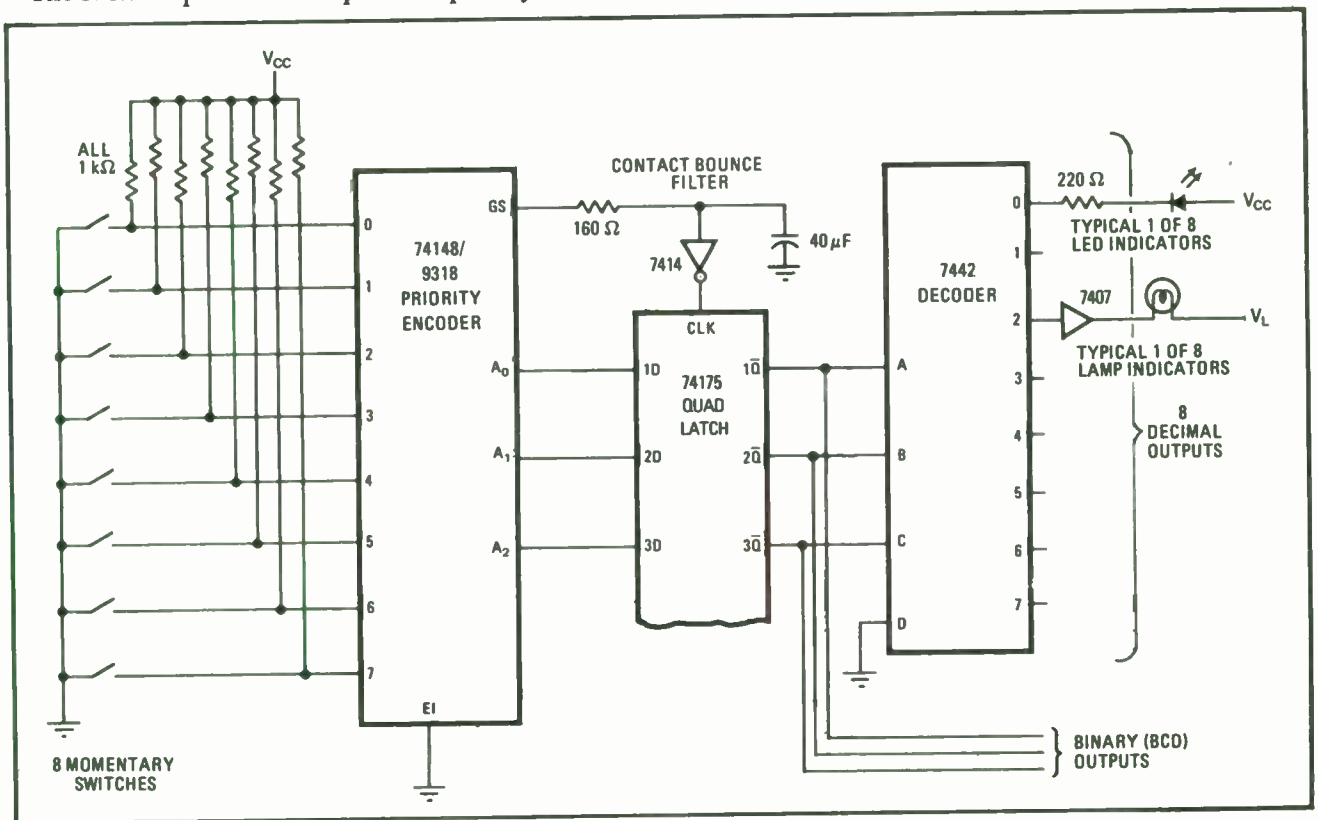
Latch circuits interlock remote switches electrically

by Jack Elias
Honeywell Inc., Fort Washington, Pa.

As many as eight momentary switches can be interlocked electrically even when they are physically separated from one another—an impossible task for mechanical interlocks. The keyboard-type momentary switches provide both binary-coded and individual outputs and are much more reliable than mechanically interlocked switches. The electrical interlock consists of an encoder, decoder and quad switch latch plus a Schmitt trigger and a few passive components.

The switches provide the inputs to a priority encoder, such as a TI 74148 or Fairchild 9318, which translates the identity of any actuated switch into a binary-coded output. The encoder also has an output, termed GS, for group-select, indicating when any one or more inputs are actuated; it provides a clock pulse for a 74175 quad latch, which stores the binary-coded output of the encoder. An RC filter and a Schmitt trigger remove uncertainty caused by switch bounce. The outputs of the flip-flops go to a 7442 decoder, which can drive either light-emitting diodes directly or incandescent lamps through buffers. Of course, the outputs can drive other circuits or systems that require the interlock.

If a second switch is actuated before the first is released, it has no effect because the Schmitt trigger has already generated its clock. Likewise, if the first switch is released while holding the second one down, the first switch's indication will be held until all the switches are released. The circuit can be expanded by cascading the encoders and using a larger decoder. □



Interlock. Momentary switches are interlocked from simultaneous operation by encoding them into a set of latches and then decoding the latch states to drive indicators or other apparatus. Circuit is more reliable than mechanical interlock, and switches can even be remote.

Auto intrusion alarm uses C-MOS circuits

by F. E. Hinkle
Applied Research Laboratories, University of Texas, Austin, Texas

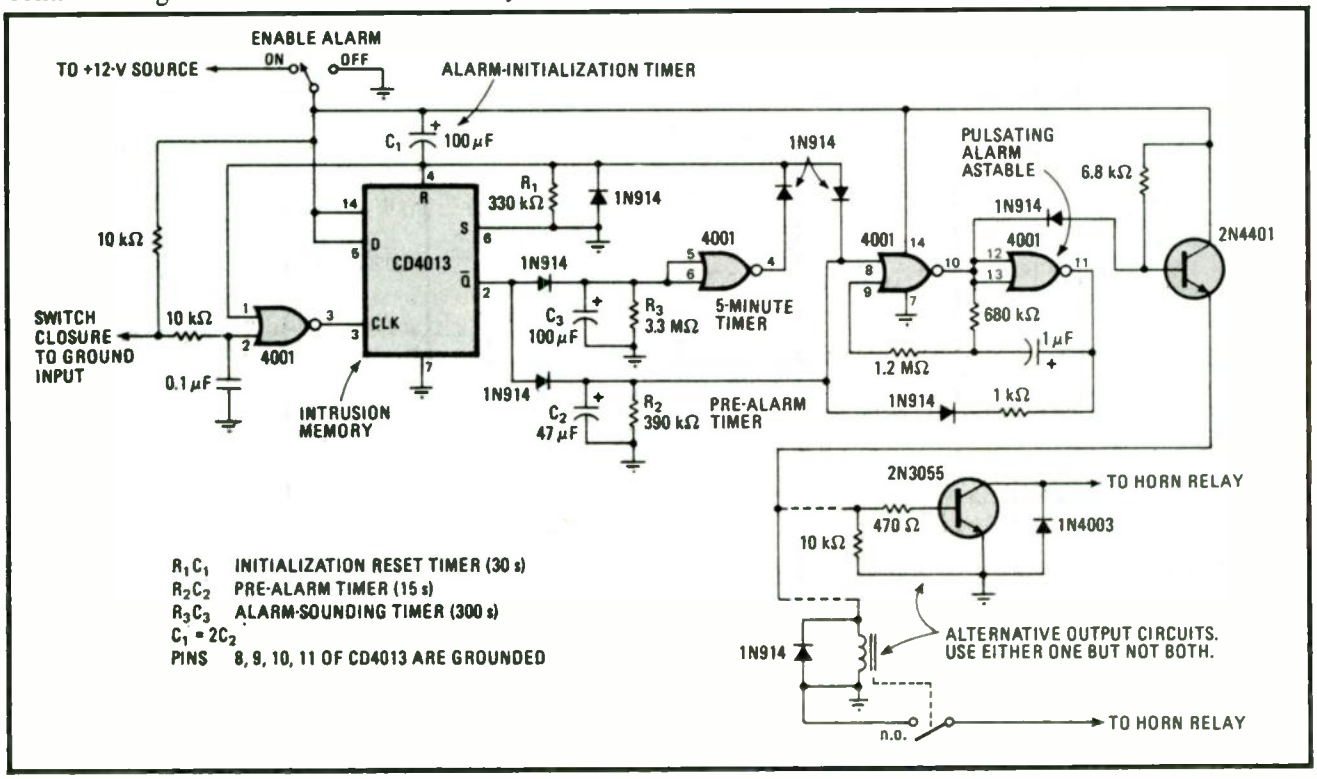
A sophisticated alarm circuit that uses the horn of the car and incorporates multiple time delays has been designed around two C-MOS packages—a natural choice for use in automobile intrusion alarm systems because of their extremely low power consumption.

The circuit, which is armed by a hidden switch located inside the car, has a short delay period after it is enabled, to permit the driver to leave the car without tripping the alarm. Thereafter, opening a door or trunk lid will trigger the alarm and, following another short interval (to permit the driver to enter the car and disable the alarm) the horn is pulsed approximately 60 times per minute, so as not to sound stuck. After several minutes, the alarm circuitry resets itself, ready for another intrusion. All of the time delays can be adjusted by changing resistor values.

The figure shows the schematic of the alarm circuit using a CD4001 quad NOR gate and a CD4013 D-type flip-flop. The input to the circuit is taken from the door switches that control the dome light and short to ground when any door is opened. The alarm's input signal is normally 12 volts and also goes to ground when the doors are opened. The driver enables the alarm by a hidden spdt switch connecting 12 V to the circuitry.

Resistor-capacitor combination R_1C_1 develops a reset command signal to the intrusion memory when the alarm is enabled. This time delay permits the driver and passengers to leave the automobile prior to the arming of the flip-flop. Once the reset time delay expires, the flip-flop is ready to detect a switch closure to ground at the input. When a closure to ground occurs, a positive-going signal clocks the D-type flip-flop. Capacitors C_2 and C_3 were initially charged to 12 V during the reset interval, and they begin to discharge. R_2C_2 discharges below the NOR gate input threshold first, causing the 1-hertz astable oscillator to turn on. This astable is used to drive a small relay or transistor that turns the horn relay in the car on and off. If C_1 equalled C_2, the voltage on the reset of the CD4013 at turn-on would be half of the supply voltage, which is not a valid state. Therefore C_1 is made twice C_2, giving a reset voltage of two thirds the supply voltage. R_3C_3 discharges below the NOR gate input at a much later time, generating a reset command to the intrusion memory. Thus, the complete process can repeat itself if another intrusion is detected.

When the driver enters the car, the alarm is turned off but will be initialized instantly if turned on again. In practice, a time delay of 30 seconds was chosen for the R_1C_1 time constant. R_2C_2 was chosen to be 15 seconds, and R_3C_3 is 300 seconds. Either a relay or an npn transistor may be used to trigger the horn relay in the car, depending on how much current must be controlled; both these alternative output circuits are shown in the diagram. Since only two C-MOS ICs are used, the circuit fits easily on a small circuit board and mounts under the dash. If the trunk or hood switch is paralleled with the door switches, then it too will trip the alarm. □



Smart alarm. C-MOS intrusion detector for an automobile uses only two ICs, yet provides a high degree of flexibility. Delay times are provided to aid in the arming and disarming of the alarm. Once the pulsating-horn alarm is sounded, it resets automatically after several minutes.

Twin oscillators form intruder detector

by Joshua Premack
Honeywell Inc., North Hopkins, Minn.

A system that can detect an intruder approaching an ungrounded metal object, such as a steel desk or a parked vehicle, is one job for a highly sensitive capacitive sensor. When scaled to operating frequencies high enough to give adequate bandwidth, the circuit is also suitable for many other applications, such as a capacitive microphone, capacitive seismic sensor, or an indicator of the eccentricity of the path of a rotating object.

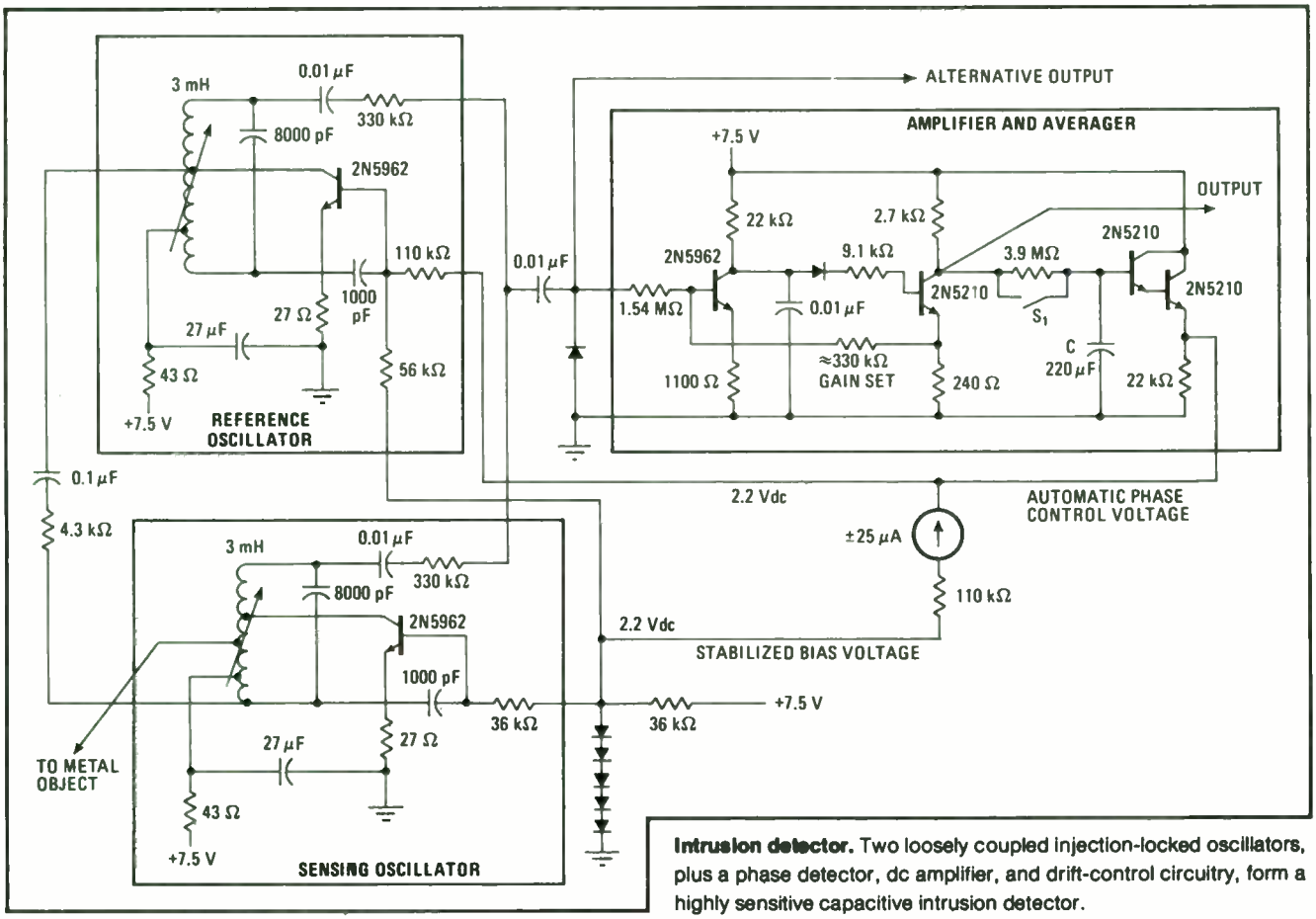
The circuit is based on the behavior of a pair of mutually synchronized oscillators. One oscillator is used as a reference, and the other is connected by a tap on its tank-circuit inductor to the object being protected. By this auto-transformer action, the loading effect on the oscillator, caused by the resistive component of the object, is reduced to an acceptable value. The protected object's capacitance is connected to an effective circuit capacitance of 2×10^6pF. A sensitivity of a few picofarads is available with a good signal-to-noise ratio. Bandwidth for a 33-kilohertz carrier is ± 25 hertz at 3 decibels down. If one of the oscillators, both of which have a small fixed coupling between their tuned circuits, is tuned to approach the frequency of the other, their combined output produces beats that indicate their frequency separation.

As tuning is continued in the same direction, the beat frequency decreases until the coupling pulls the oscillators into synchronism, whereupon the beats stop abruptly instead of decreasing smoothly to zero. At this adjustment, the oscillators are at the same frequency but are 90° apart in phase. As tuning is continued, the phase angle varies through 0° to 90° in the opposite direction. Then, with further tuning, the beats reappear.

If the coupling between the oscillators is reduced, the beat-free tuning interval narrows, but the ±90° phase shift always occurs between the onset and cessation of beats. This interval may be made very narrow by using very little coupling—provided that the oscillators are kept from drifting in frequency. Drift compensation is achieved with feedback by converting phase difference to an error voltage in a slow-feedback system, so that an interval of 5 to 6 pF on a base value of 8,000 is quite satisfactory.

In the intrusion-detection system, the two essentially identical oscillators have resistive coupling between the collector and base, which theoretically should keep the oscillators 180° out of phase when synchronized. The oscillators are actually designed to operate only 150° to 160° out of phase. Their outputs are summed at the junction of the two 330-kilohm resistors.

If the oscillators were exactly 180° out of phase, the voltage at the junction would be zero. The non-zero



Intrusion detector. Two loosely coupled injection-locked oscillators, plus a phase detector, dc amplifier, and drift-control circuitry, form a highly sensitive capacitive intrusion detector.

voltage at this point is the quiescent value, which increases as the capacitance in the sensing oscillator changes. This voltage is usable as an output of the circuit, especially when a wide dynamic range is wanted.

A two-stage dc amplifier provides an output and also charges a large capacitor—220 microfarads—through a 3.9-megohm resistor. This voltage changes very slowly in response to sudden changes in the capacitance of the sensing oscillator. This output also supplies part of the base bias for the reference oscillator, which compensates for any tendency of the oscillator to drift.

Before tuning the oscillators to synchronism and to the desired phase position, the time constant of the averaging circuit is shortened from 858 seconds to 0.594 second by closing the switch across the 3.9-megohm resistor. The tuning of the sensing oscillator is varied until the tuning meter dips suddenly, indicating that the oscillators are synchronized. When the meter reads zero, and after allowing several seconds to charge averaging capacitor C fully, the switch S is opened and the sensor is operational. This operation is easily automated.

When used as an intrusion detector, the circuit may be attached to ungrounded metal objects that have lossy (30% to 125% dissipation factors) capacitance, ranging from 500 to 15,000 picofarads. Overload-recovery time of the system from transients is in milliseconds, and that of desired signals is in the seconds range. The use of two injection-locked oscillators as a sensor is covered by patents 3,222,664 and 3,293,631.

No exotic measures were taken in the manufacture of these sensors, but care should be exercised to ensure good oscillator stability and tracking. Rapid temperature fluctuations should not be imposed on oscillator components, nor should large temperature differentials exist between the two oscillator assemblies. Careful attention should be given to confining the coupling between the oscillators to the desired path. Stray inductive coupling, common power-supply impedance, and possible paths where oscillator outputs are fed to the detector should be controlled. □

Electronic combination lock offers double protection

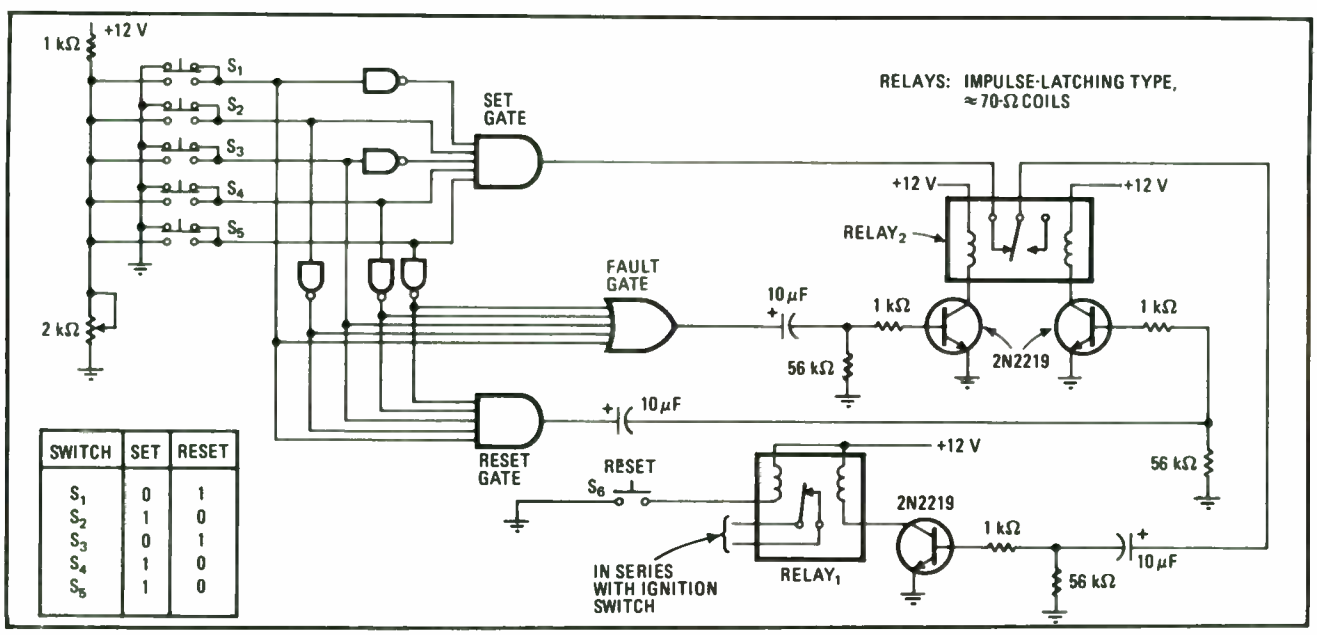
by Louis F. Caso
Bethpage, N.Y.

If you need a doubly safe lock, try the electronic combination lock shown here. It will not unlock unless the correct combination of switches is depressed, and if the wrong combination is chosen, the lock will not open until it is reset with another combination.

The circuit in the figure is intended for installation in an automobile, but it can be easily modified for other applications. When the correct combination of switches S_1 through S_5 is depressed, the output of the SET gate goes to logic 1, closing the contacts of $RELAY_1$. When the car's ignition is turned off, this relay should be reset (contacts opened) by using switch S_6.

To open (set) the lock, switches S_2, S_4, and S_5 are depressed simultaneously. If an error is made, the output of the FAULT gate goes to logic 1, and the contacts of $RELAY_2$ will open. When this happens, the lock must be reset before the opening combination can be used again. Switches S_1 and S_3 are depressed simultaneously to reset the lock.

Any secret combination of push buttons can be selected by arranging the switches as desired. For most applications, the multiple-input logic gates can be obtained by interconnecting standard dual-input gates. □



Safe and sound. To open this electronic combination lock, depress the correct combination of switches S_1 through S_5. But if an error is made, the lock must be reset with another switch combination before it can be opened again (The switches are depressed simultaneously.) The circuit shown here is for locking an automobile ignition, but it can be readily adapted for other uses.

Digital combination lock is virtually crackproof

by Dale Platteter
Naval Weapons Support Center, Crane, Ind.

All the sandpaper in the world wouldn't help a safe-cracker open a 15-digit combination lock with the electronic "tumblers" described here. In fact, it could take more than a million and a half years to generate the correct code, if combinations were tried at the rate of one every 10 seconds.

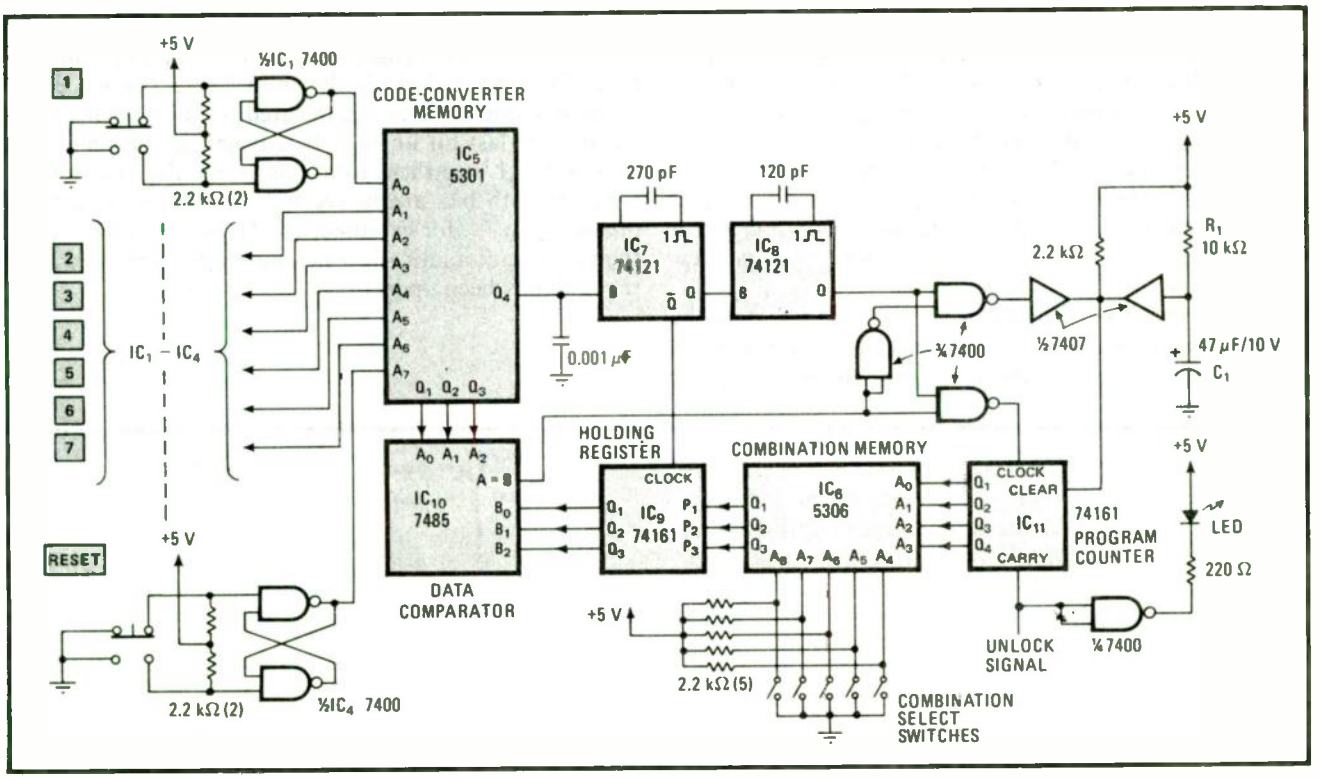
Would-be thieves are further discouraged by the automatic reset of the circuit on entry of any incorrect number—which requires that the entire sequence be re-entered and thus disrupts any orderly trial-and-error approach. In addition, the 512-by-4 bit programable read-only memory that stores the correct combination has room for as many as 32 easily selectable combinations, enabling the code to be changed periodically.

The circuit compares the combination entered with one stored in memory, a digit at a time, and latches a transistor-transistor-logic output high after the entire code is correctly entered. The reset button is pushed before the combination is entered to ensure that the lock is ready for entry of the first digit. The operator also presses it to start over after he thinks he may have made a sequence error.

Only eight possible inputs—the reset and seven numbers—may be encoded, because the binary words representing each are 3 bits long. But it's a good idea to use a standard 0–9 push-button array and allow one, two, or all three of the spare buttons (0, 8, and 9 in this example) to serve as reset. This increases security of the lock, since no unauthorized person will know which button to push for reset.

Integrated circuits IC_1-IC_4 in the figure are quad NAND gates connected as R-S flip-flops to debounce the single-pole, double-throw push buttons. The entered numbers are encoded by IC_5, a Monolithic Memories Inc. type 5301 256-by-4-bit PROM programed according to the truth table in Table 1. This chip was selected to simplify programing, because its background is initialized to logic 1 and the reset code of 111 means most of the addresses will be logic 1s. The unlocking codes are programed into the combination memory, IC_6, an MMI type 5306 512-by-4 bit PROM.

Shown in the figure are code-selecting switches that determine the 5 most-significant bits of the address-data inputs (A_4 through A_8) and hence, which of the possible 32 combinations is selected. The five data lines may be programed from a remote location for the temporary exclusion of particular "key holders," or just to change



Maximum security. A total of 13 integrated circuits is used in this digital combination lock, which requires a sequence of 15 digits to open. The design permits easy changing of sequence length and number of possible digits, and the memory stores up to 32 combinations.

PROM PATTERN FOR CODE-CONVERTER MEMORY (IC 5)

Address (Binary)								Decimal	Output				Comments
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		Q_4	Q_3	Q_2	Q_1	
1	1	1	1	1	1	1	1	255	0	1	1	1	No inputs
1	1	1	1	1	1	1	0	254	1	0	0	1	Enter 1
1	1	1	1	1	1	0	1	253	1	0	1	0	Enter 2
1	1	1	1	1	0	1	1	251	1	0	1	1	Enter 3
1	1	1	1	0	1	1	1	247	1	1	0	0	Enter 4
1	1	1	0	1	1	1	1	239	1	1	0	1	Enter 5
1	1	0	1	1	1	1	1	223	1	1	1	0	Enter 6
1	0	1	1	1	1	1	1	191	1	0	0	0	Enter 7
0	1	1	1	1	1	1	1	127	1	1	1	1	Reset
–All remaining addresses–									1	1	1	1	Error input–reset

PROM PATTERN EXAMPLE FOR COMBINATION MEMORY (IC 6)

Address (Binary)									Decimal	Output				Digit
A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		Q_4	Q_3	Q_2	Q_1	
1	1	1	1	1	0	0	0	0	496	x	0	0	1	1
1	1	1	1	1	0	0	0	1	497	x	0	0	0	7
1	1	1	1	1	0	0	1	0	498	x	1	0	0	4
1	1	1	1	1	0	0	1	1	499	x	0	1	0	2
1	1	1	1	1	0	1	0	0	500	x	1	1	0	6
1	1	1	1	1	0	1	0	1	501	x	1	0	1	5
1	1	1	1	1	0	1	1	0	502	x	1	0	1	5
1	1	1	1	1	0	1	1	1	503	x	0	1	1	3
1	1	1	1	1	1	0	0	0	504	x	0	0	0	7
1	1	1	1	1	1	0	0	1	505	x	0	0	1	1
1	1	1	1	1	1	0	1	0	506	x	0	0	0	7
1	1	1	1	1	1	0	1	1	507	x	0	1	0	2
1	1	1	1	1	1	1	0	0	508	x	1	0	0	4
1	1	1	1	1	1	1	0	1	509	x	1	0	0	4
1	1	1	1	1	1	1	1	0	510	x	0	1	1	3
1	1	1	1	1	1	1	1	1	511	x	1	1	1	Reset

Remainder of memory is used to store 31 additional combinations
x = not used

the combination in the interest of security.

Timing of the circuit is controlled by two monostable multivibrators. When any button or combination of buttons is pressed, the MSB output (Q_4) of the code-converter memory, IC_5, goes high and triggers the first monostable, IC_7. The rising edge of its Q output latches the binary word at the output of the combination memory, IC_6, into the holding register, IC_9, a 4-bit programable binary counter. After 375 nanoseconds, the rising edge of the $\overline{Q}$ output of IC_7 triggers the second monostable, IC_8.

While the Q output of IC_8 is high, which occurs for 165 ns, a 4-bit magnitude comparator IC_{10}, compares the entered and stored words. If the words of IC_5 and IC_6 are identical, the A = B output of the comparator will go high, incrementing the program counter, IC_{11}, another 4-bit binary counter, through the NAND-gates. If the words differ, the program counter is reset, and the entire combination must be entered again.

Upon entry of the correct combination, the program counter advances 15 counts, and the carry output goes high. This is the unlock signal, indicated by a light-emitting diode. It can drive external TTL circuits, or may be buffered to control a solenoid-operated lock.

The program counter could assume any initial state when power is applied. To prevent opening of the lock when power is periodically interrupted, a power-on reset circuit made up of the R_1-C_1 charging network and a buffer clears the program counter for the first few milliseconds.

If less security is permissible, the circuit may be simplified to keep down the component count and cost. A priority encoder such as the 74147 may be used in place of IC_5, sacrificing the automatic reset effected when two or more buttons are simultaneously pressed. A smaller memory may be used if 32 different combinations are not needed, and the power-on reset circuit may be eliminated.

A 2-bit word length might even be used, greatly reducing circuit complexity. It still could require as much as 4½ years to crack at the rate of one 15-digit combination every 10 seconds—and burying those three possible input numbers in a complete 0–9 push-button array would increase security many times over. The system is completely expandable—word length (hence number of inputs) and sequence length are easily adjusted to suit one's needs.

A PROM sample programing pattern for the combination 174265537172443 is shown in Table 2. Each of the 15-digit combinations is allocated 16 bits of memory, leaving the last bit unused. It is beneficial, as shown, to program 111 into these locations (since the first address is 0, the 16th bits are in every 2^n-1 address, where n is greater than 3—for example, 15, 31, 63, etc.). Reset will then occur automatically when any digit is pressed after the lock has been opened. □

45. Sensors

Capacitive transducer senses tension in muscle fibers

by Robert M. Wise
Medical College of Virginia, Richmond, Va.

Tension in muscle fibers can be measured by the same capacitive transducers that measure displacement and pressure. The ubiquitous NE555 timer and an NE560B phase-locked loop combine with a specially made capacitor to produce an analog output whenever there's a change in capacitance. Tuned circuits are not required, and both size and stability of the timer permit design versatility.

The heart of the circuit is the timer. When pins 2 and 6 are connected, the timer triggers itself and runs free as a multivibrator. The transducer charges through R_1 and R_2 and discharges through R_2. The frequency is precise and independent of supply voltage. Charge time is:

$$t_1 = 0.693\,(R_1 + R_2)\,C_T$$

Discharge time is:

$$t_2 = 0.693\,(R_2)\,C_T$$

Frequency of oscillation is then:

$$f = 1/T = \frac{1.44}{(R_1 + 2R_2)\,C_T}$$

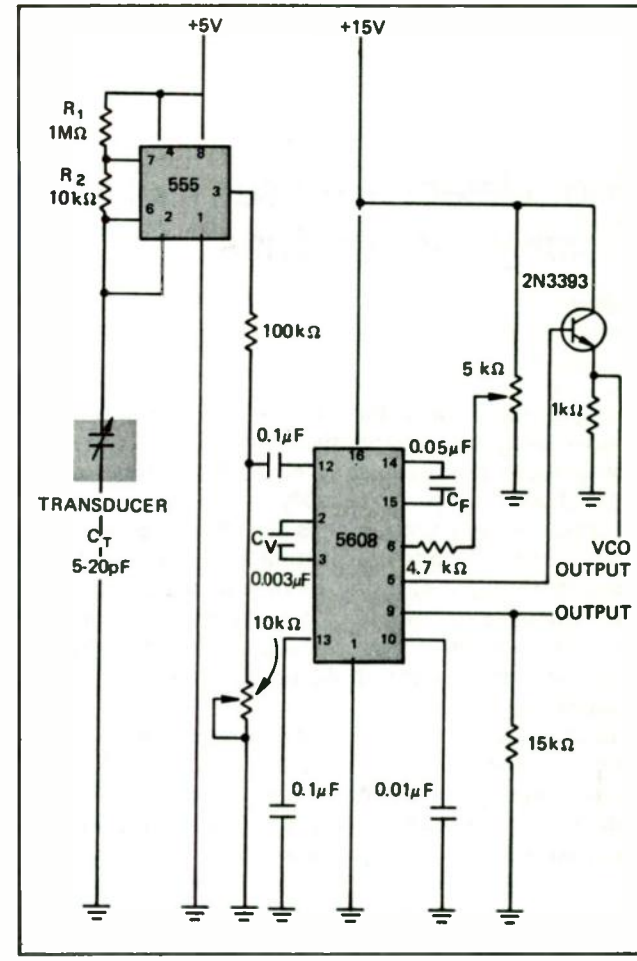
Any frequency between 0.1 hertz and 100 kilohertz can be selected; the component values shown in the figure are for a frequency of about 100 kHz.

The input signal to the 560B is phase-compared to an internal voltage-controlled oscillator. Error signal at the output of the comparator is filtered, amplified, and fed back to the VCO. Input frequency to the phase-locked loop through pin 12 must be attenuated to facilitate proper lock and capture of the transducer signal by the VCO. The voltage should be between 20 and 50 millivolts peak to peak.

The frequency of the VCO, which should be adjusted to coincide with the zero-position frequency of the transducer, is determined principally by the capacitor C_V connected between pins 2 and 3 of the NE560B:

$$f_{VCO} = 300/C_V$$

where C_V is expressed in microfarads. Fine adjustment of f_{VCO} can be made by a regulating current injected into pin 6 through a 4.7-kilohm resistor and controlled by the setting of the 5-kilohm potentiometer. The zero-position frequency of the transducer is measured at pin 12 of the phase-locked loop, and the VCO frequency is measured from pin 5 through the 2N3393 emitter-follower transistor to avoid pulling the VCO.



Frequency modulation. Capacitive transducer modulates frequency of 555 multivibrator. Frequency is detected in 560B phase-locked loop that produces dc output voltage. Arrangement is stable and compact, has fast response, and does not require any tuned circuits

A filter capacitor C_F between pins 14 and 15 sets the desired bandwidth of demodulated information. The approximate value of C_F in microfarads can be found from the formula

$$C_F = 13/B$$

where B is the bandwidth in Hz. The 0.05-μF value shown gives a clean output swing of 100 millivolts.

The de-emphasis network uses an external capacitance of 0.01 μF in conjunction with an 8-kilohm internal resistance at pin 10 to produce a 75-microsecond time constant for the demodulated output at pin 9. The 100 mV output swing rides on a 12-V offset voltage. □

Photodetector senses motion in noisy surroundings

by Richard T. Laubach
National Cash Register Co., Cambridge, Ohio

A digital phototransistor amplifier, consisting of a few readily available inexpensive components, can detect slowly moving objects in an electrically noisy environment. The circuit works reliably, even if long cables link its optical sensing section to its amplifying section.

The circuit detects objects that break the light beam between the light-emitting diode and the phototransistor. When the light beam is interrupted, transistor-output voltage V_1 increases, causing the potential at point A to rise until the threshold voltage (about 8 volts) of inverter I_1 is reached.

Both inverters I_1 and I_2 then switch, and voltage V_2 jumps from 0 to 12 v. This voltage jump supplies additional current at point A through feedback resistor R_f, reducing the pull-up resistance seen by the phototransistor so that voltage V_1 jumps from 8.5 to 11 v when voltage V_2 makes its low-to-high transition.

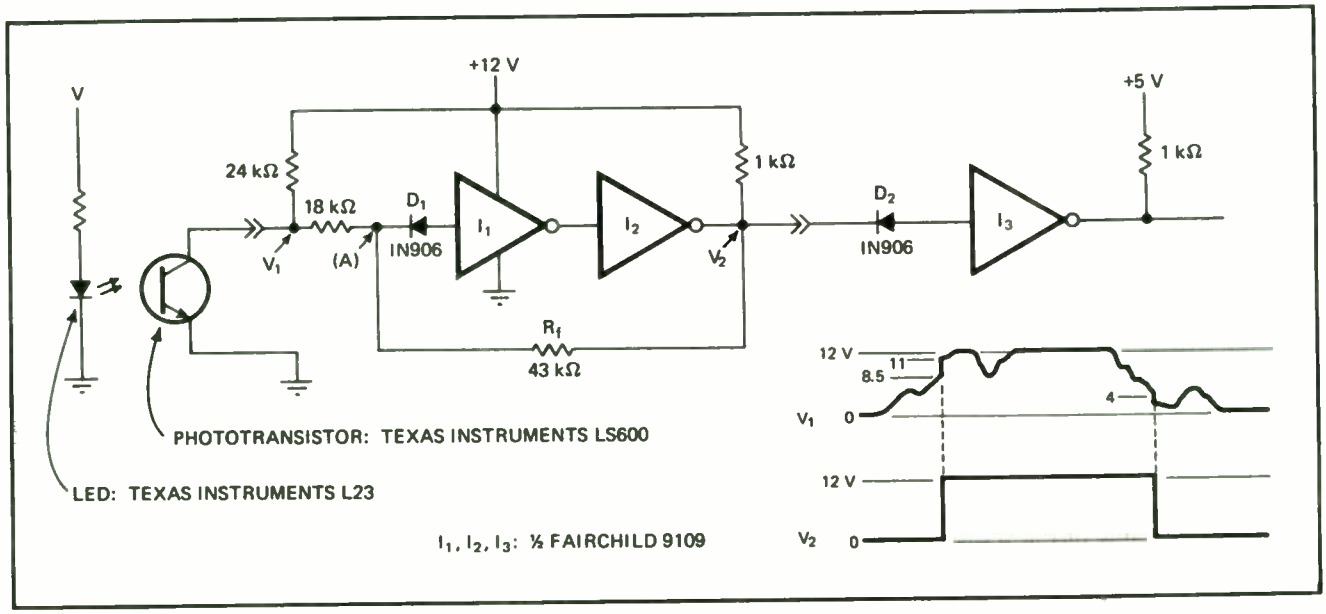
Besides protecting the input of inverter I_1, diode D_1 isolates point A, allowing the potential at this point to rise to 12 v. Without the diode, point A would be clamped at I_1's threshold voltage of 8 v and voltage V_1 would never reach 12 v.

Once the circuit is in its high state, transistor voltage V_1 must drop below 4 v to pull point A below I_1's threshold and to switch V_2 back to ground. When V_1 becomes less than 4 v, the phototransistor's pull-up resistance increases and speeds up the rate of decline of V_1. Feedback resistance R_f causes V_1's switching voltage levels to be different—first 11 v, then 4v—thereby providing 7 v of hysteresis and noise immunity.

Inverter I_3 and diode D_2 buffer voltage V_2, converting it to a 5-v transistor-transistor-logic signal. If desired, the 12-v output of V_2 can be used directly as the logic input voltage.

The circuit is operating successfully in an electromechanical printer where the cable from the phototransistor to the amplifier input is a twisted pair of wires 10 feet long that run near solenoid driver cables. Moving printed matter is detected by an existing circuit without any output-signal bounce, even though the edge of the matter momentarily stops as it breaks the light beam. □

Optical detector. When object breaks LED light beam, phototransistor output voltage V_1 increases, switching on inverters I_1 and I_2. Voltage V_1 then jumps up because additional current through resistor R_f to point A decreases phototransistor pullup resistance. Voltage V_2 stays high until V_1 drops to 4 V, increasing pullup resistance and causing V_2 to return to ground. Inverter I_3 converts V_2 to TTL-compatible output.



Two-component light sensor has high voltage output

by Thomas T. Yen
Statham Instruments Inc., Oxnard, Calif.

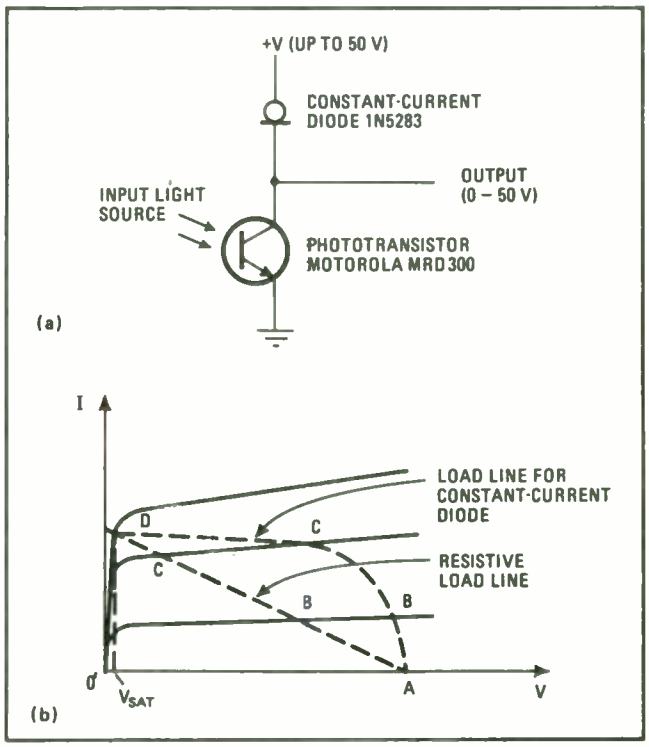
An output voltage of up to 50 volts can be developed by a light-sensing circuit that uses a constant-current diode as the load for a phototransistor. The circuit, which is drawn in (a), provides high noise immunity because its output remains relatively constant until the input light-level threshold is reached. Since the circuit can operate over a wide range of voltages, it is compatible with C-MOS devices. And, at high light levels, it is also compatible with TTL and DTL devices because of the high-current-sinking capability of its phototransistor.

The current-voltage characteristics of a typical phototransistor are shown in (b). The nonlinear load line of the constant-current diode and the linear load line of a resistor, the standard phototransistor load element, are superimposed on the I-V curves for comparison at four light levels.

At level A, the phototransistor is cut off, while at level D, it is saturated. When the input light intensity goes from intermediate level C to saturation level D, or vice versa, the change in the phototransistor's output voltage is far larger for the nonlinear load than for the linear load. In circuit (a), therefore, the output voltage remains high until the input light intensity is large enough for the phototransistor's light current to match the diode's pinchoff current. At this point the circuit's output voltage decreases abruptly and becomes the saturation voltage of the phototransistor.

When the input light changes from bright to dark, the circuit's output voltage rises slowly, as the constant current from the diode charges the phototransistor's collector capacitance. In this circuit, the charging time will be on the order of 100 microseconds. The output rise time can be shortened either by clamping the output to a lower final voltage or by using a diode with a higher current rating.

With the components shown, the circuit is limited to medium-speed (1 kilohertz) applications—for example, an event-counting sensor for industrial purposes. Faster operating speeds can be realized by substituting a photodiode for the phototransistor. But, a photodiode requires a low-current diode, one with a rating on the order of 20 microamperes, and such a constant-current diode is not currently available. Furthermore, integrating the constant-current diode and the phototransistor on the same chip would permit the circuit's risetime to be optimized, because device capacitance could then be minimized through the chip layout. □



Light detector. Constant-current diode acts as a nonlinear load for a phototransistor so that the output voltage of this light sensor (a) remains high until the phototransistor's current equals the diode's pinchoff current. When the input light threshold is reached, the circuit's output switches to the saturation voltage of the phototransistor, as shown by the I-V curves (b) of a typical phototransistor.

46. Switching circuits

Doubling breakdown voltage with cascoded transistors

by Peter T. Uhler
Tinker Air Force Base, Midwest City, Okla.

When bipolar transistors are connected in series to increase their over-all breakdown voltage for power-circuit applications, high-voltage zener diodes are usually needed to protect the transistors. And generally, besides being expensive, these high-voltage zeners have rather modest power ratings.

An alternate approach, a saturating cascode switch, effectively doubles transistor breakdown voltage without requiring costly zeners. The cascode switch generates 600-volt rectangular positive-going pulses with 350-v transistors. It employs a shunt, rather than series, approach for additional load protection.

In the region of operation where output voltage (V_o) is greater than half the supply voltage ($V_{CC}/2$), the switch works as a conventional cascode amplifier, and the collector currents of transistors Q_1 and Q_2 are equal. The base voltage of Q_2 never exceeds $V_{CC}/2$ (unless Q_2's reverse collector saturation current, I_{CBO}, becomes significant), because of the voltage divider formed by the two same-value biasing resistors, labeled R. Therefore, the maximum voltage drop across each transistor is effectively limited, and the need for zener diode clamps is eliminated.

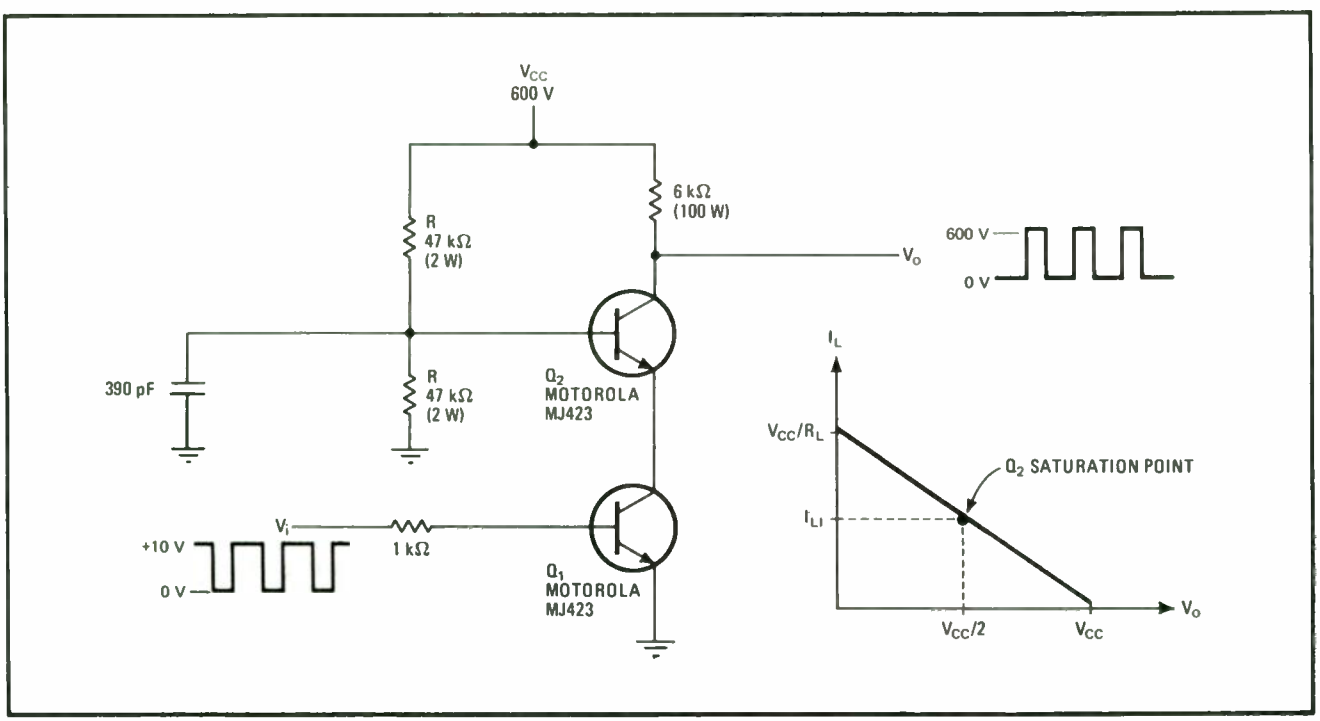
As load current I_L exceeds the midpoint current value (I_{L1}) shown on the static load line, transistor Q_2 saturates and transistor Q_1 becomes the sole controlling element. The load resistance for the switch is now the parallel combination of the load resistance itself and half the biasing resistance ($R_L \parallel R/2$), which is essentially equal to R_L since $R/2$ is much greater than R_L.

Only a slight discontinuity occurs in the load line when transistor Q_2 saturates, so that the circuit's output voltage is practically a continuous function of its input voltage throughout the entire output voltage range of 0 to 600 v. The capacitor at the base of Q_2 eliminates the positive-going charge-storage transient that is generated if this transistor is forced out of saturation rapidly.

The biasing resistance value of $R/2$ must be small enough to prevent Q_2's reverse saturation current (I_{CBO}) from causing a significant rise in the potential at Q_2's base. Also, the $R/2$ resistance value must be less than the factor, $h_{FE}R_L$, to assure that Q_2's collector-emitter voltage is a decreasing function of collector current.

The saturating cascode switch can be modified to handle even higher voltages by using three transistors and two separate biasing resistor pairs to bias the transistors at supply voltages of $2V_{CC}/3$ and $V_{CC}/3$. □

Eliminating high-voltage zeners. Cascoded transistors generate 600-volt pulses without using high-priced high-voltage zener diodes for protection. Biasing resistors limit voltage across transistors to $V_{CC}/2$. When V_o is greater than $V_{CC}/2$, transistors Q_1 and Q_2 behave like conventional cascode amplifier. When V_o is less than $V_{CC}/2$, Q_2 saturates, and only Q_1 determines load current.



Solid-state dpdt switch provides current reversal

by Don DeKold
Santa Fe Junior College, Gainesville, Fla.

When the dc current flowing through a load is periodically reversed, the alternating square-wave voltage developed across the load has a peak-to-peak amplitude that is twice the magnitude of the power-source voltage. A circuit that provides periodic current reversal is useful for driving loads that otherwise might become polarized by the steady passage of a unidirectional current.

Dc-to-ac inverters may be used for periodic current reversal, but they usually require a power transformer of relatively large size and weight. Additionally, these circuits frequently have sizable standby currents because they generally contain saturating transformers, making them inefficient under light load conditions.

The solid-state circuit in the diagram solves these problems. It acts as a double-pole double-throw switch that periodically reverses the current through its load resistor, R_L.

Transistors Q_1 and Q_2 are the active elements in an ordinary astable multivibrator. They alternate between saturation and cutoff at the multivibrator's basic pulse-repetition rate. Transistors Q_3 and Q_4, which are driven by transistors Q_1 and Q_2, respectively, also alternate between saturation and cutoff, but are 180° out of phase with Q_1 and Q_2.

The load-driver section of the circuit is made up of four Darlington pairs, labeled transistors Q_5 through Q_8 in the figure. A single pnp pair, such as the one designated transistor Q_5, is connected in complementary fashion to an npn pair, such as the one identified as transistor Q_6. Each Darlington pair is an output stage that is either saturated or cutoff, depending on the operating state of transistors Q_1 through Q_4.

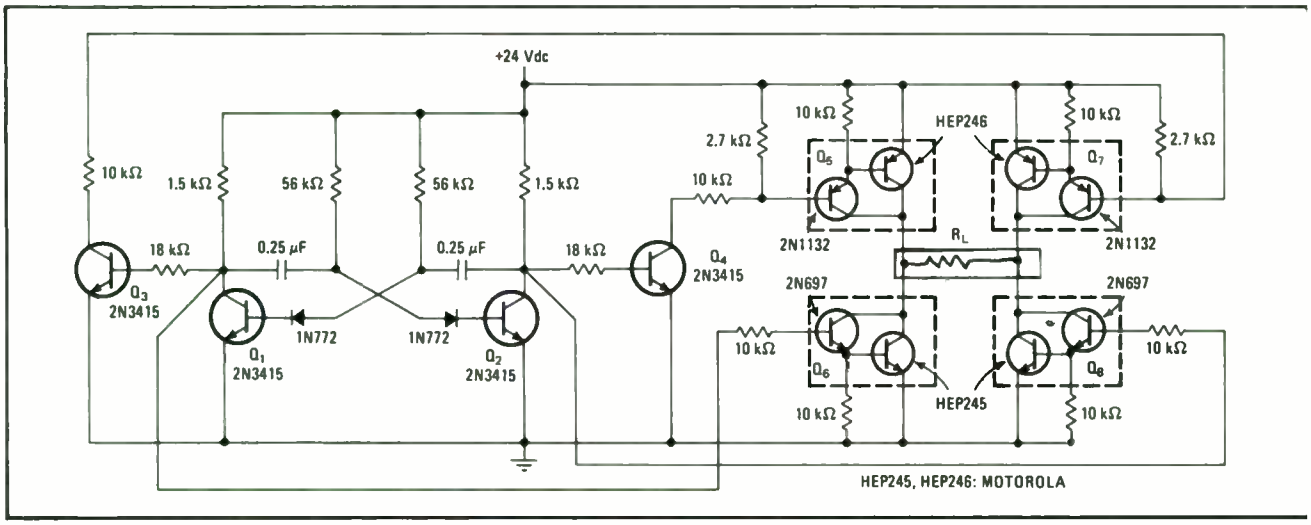
Diagonally opposite output stages (such as transistors Q_5 and Q_8) are switched on at the same time as the two other diagonally opposite pairs (transistors Q_6 and Q_7) are switched off. This condition holds for half of the multivibrator's period and reverses for the other half, as indicated by the table.

The circuit's efficiency is very high because practically all of the supply voltage is applied across the load during each half of the operating cycle. The transistor states change at the pulse-repetition rate of the multivibrator producing an alternating current through the load. In effect, the circuit is a solid-state double-pole double-throw switch that is toggled at the frequency of the multivibrator. If the multivibrator stalls or does not start when power is applied, both transistors Q_1 and Q_2 will saturate, cutting off the other devices and preventing any load current from flowing.

With the components shown, the circuit supplies an alternating current of 1.6 amperes to a 24-volt load. Standby current is about 25 milliamperes, and the multivibrator frequency, which is unaffected by loading, is 57 hertz. If desired, a heavier load can be driven, since the type HEP245 and HEP246 transistors are rated at 3 A. The supply voltage, of course, may be any value that does not exceed device-breakdown voltages.

Operating frequencies in the kilohertz range can be achieved by merely decreasing the values of the two multivibrator capacitors. If a higher output voltage is wanted, the circuit can directly drive a step-up transformer, but arc-suppression diodes must be placed across each output stage. Loading of the output must never short either terminal to ground. □

OPERATING CYCLE	
FIRST HALF	SECOND HALF
Q_1 ON Q_2 OFF Q_3 OFF Q_4 ON Q_5 OFF Q_7 OFF Q_6 ON Q_8 ON	Q_1 OFF Q_2 ON Q_3 ON Q_4 OFF Q_5 ON Q_7 ON Q_6 OFF Q_8 OFF



Current-reversal switch. Solid-state circuit periodically reverses load current, making amplitude of square-wave load voltage twice the level of supply voltage. Operating frequency is determined by astable multivibrator formed by transistors Q_1 and Q_2. Four Darlington pairs, labeled transistors Q_5 through Q_8, make up the output stages. Diagonally opposite pairs are on while the other two pairs are off.

Attenuating transients in analog FET switches

by Leland Shaeffer
Siliconix Inc., Santa Clara, Calif.

Analog field-effect-transistor switches may be high-speed devices, but the faster they are toggled, the greater is the risk of unwanted output switching transients. The amplitude of these glitches or spikes can be greatly attentuated by synchronizing the toggling of one FET switch with a second FET switch through logic pulses that have variable rise times and fixed fall times.

Undesirable spiking can occur at the output of an analog switch during toggling because, inside the device, charge can be coupled through either its gate-source or gate-drain capacitance. Previous attempts to cancel these glitches by applying out-of-phase spikes from a second switch failed because turn-on and turn-off times generally vary too much between devices.

In the circuit shown here, TTL inverters having open-collector outputs are used to develop the synchronizing logic pulses. Since these inverters have a pull-down current that is an order of magnitude greater than their pull-up current, the rise time of their output pulses can be increased without appreciably affecting the fall time of their output pulses. Fixed resistors (R_L) establish the pull-up currents for the inverters.

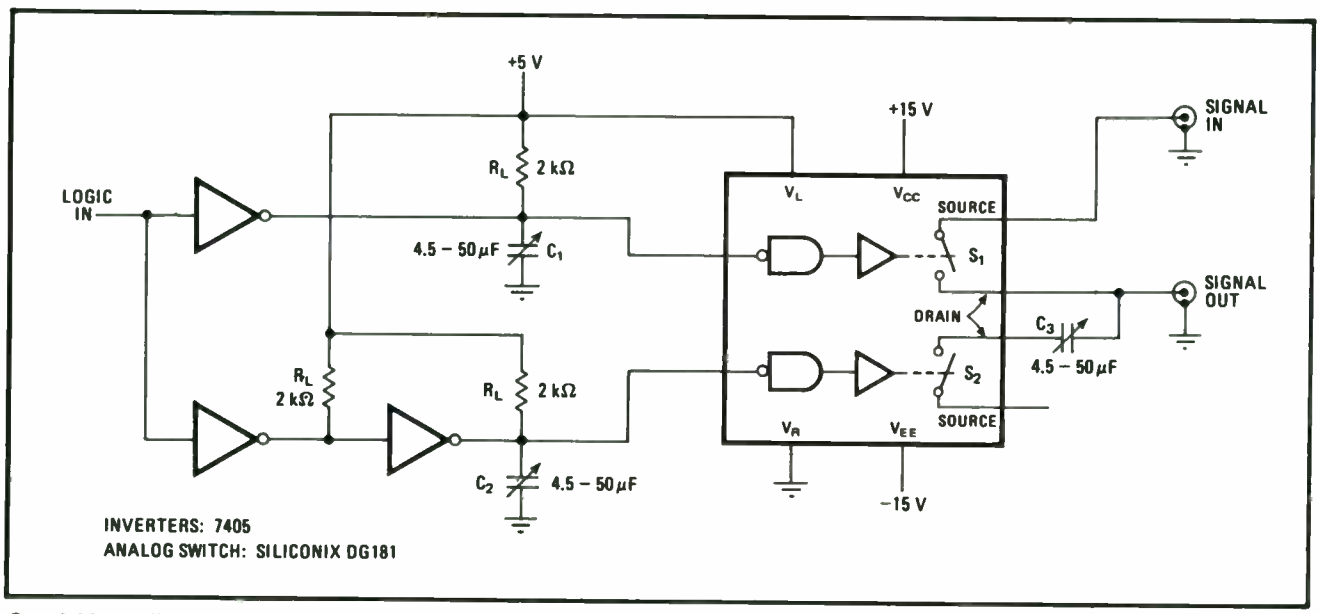
The output rise times of the inverters determine the times required to reach the toggling thresholds of analog switches S_1 and S_2. For the FET devices used here, this threshold is approximately 1.4 volts. Variable capacitors (C_1 and C_2) at the outputs of the inverters permit the rise times of these units to be set at the values needed to synchronize switches S_1 and S_2.

Now the turn-on of switch S_1 can be made to coincide with the turn-off of switch S_2, and the turn-off of S_1 can be synchronized with the turn-on of S_2. When the switches are properly matched in this way, the transients appearing at the output of S_1 can be reduced by a factor of 5 or more if R_L is greater than or equal to 10 kilohms and C_1 and C_2 are about 12 picofarads. For R_L = 75 ohms, the magnitude of the unwanted transients will at least be halved.

Transient attenuation can be improved still further by connecting a zener diode (a 6.8-v device, in this example) shunted with a bypass capacitor in series with the negative power supply. The glitches will then be reduced by an additional factor of 2 for both R_L = 75 ohms and R_L = 10 kilohms. However, the analog output voltage swing, which is normally +15 v to −7.5 v, will now be limited to +15 v and −½ v.

To adjust the circuit properly, first set capacitor C_3 at its minimum value and adjust capacitor C_1 for a minimum turn-off transient. The value of capacitor C_3 is then increased until maximum transient cancellation is obtained. Next, capacitor C_2 is adjusted for a minimum turn-on transient. Capacitors C_1 and C_2 will interact slightly with each other, and some compromise may be necessary in the adjustment of C_3 for minimum turn-on and turn-off transients.

In the circuit drawn in the figure, only one signal source is used, and switches S_1 and S_2 provide single-pole, single-throw switching action. To accommodate a second signal source and obtain single-pole, double-throw action, the drain of S_1 is connected directly (without capacitor C_3) to the drain of S_2. The second signal source is then applied to the source terminal of switch S_2. When the switches are wired in this manner, the make-before-break interval is about 30 nanoseconds. □



Squelching spikes. Switching transients at the output of an analog FET switch can be greatly attenuated by synchronizing the turn-on and turn-off of one switch with those of a second switch. Open-collector TTL inverters produce logic pulses whose output rise times can be varied while their output fall times remain fixed. The turn-on of switch S_1 is made to coincide with the turn-off of switch S_2, and vice versa.

Transistor gating circuit cuts signal delay to 100 ps

by Arthur J. Metz
Tektronix Inc., Beaverton, Ore.

Frequently in emitter-coupled-logic design, a high-speed data signal must be gated by a dc control signal that is generated by a contact closure or a transistor-transistor-logic gate. When the propagation delay in the high-speed signal path must be held to a minimum, a simple transistor circuit can probably provide the fastest way to perform the gating function.

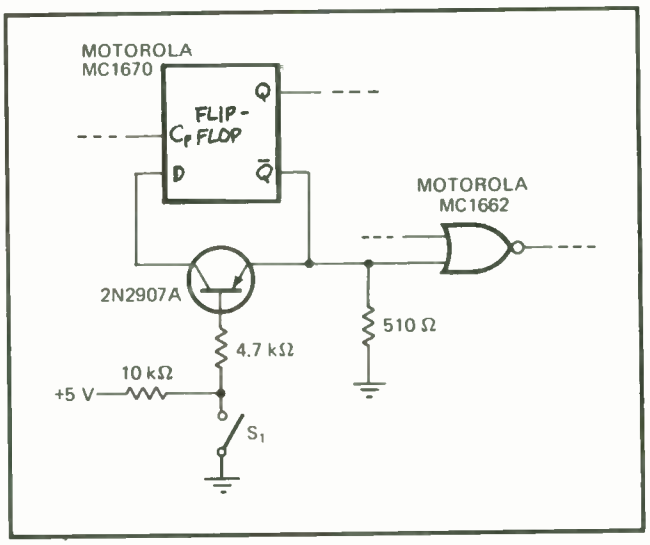
Propagation delay for the transistor gate is as low as 100 picoseconds, compared to the 1-nanosecond delays of the fastest integrated-circuit gates presently available. Moreover, the transistor gate consumes less power and costs less than the IC gate, especially if an additional IC gate package is needed to perform the gating function.

A typical application for the transistor gate is shown in the figure. Here, signal delay between the flip-flop's $\overline{Q}$ output and its D input must be minimized to realize the fastest possible toggle rate.

With switch S_1 open, the transistor's base-emitter junction is reverse-biased. An internal pull-down resistor of about 50 kilohms at the flip-flop's D input holds all data inputs near ground potential, reverse-biasing the flip-flop's input stage (by more than 3 volts) and assuring the rejection of any signal that passes through the internal capacitance of the transistor. When the switch is closed, the transistor saturates and provides a low-impedance signal path. For TTL applications, the function of switch S_1 is implemented by the appropriate TTL device.

The noise immunity of the gating circuit is maintained by keeping the transistor's collector-emitter voltage drop low. (With the type 2N2907A transistor, which has excellent saturation characteristics, the V_{CE} drop can be held to approximately 10 millivolts by using a forced beta of 0.1.) Driving several high-impedance inputs or perhaps one low-impedance input will cause some loss of noise immunity. Although driving a terminated line is not recommended, the gate may be driven from a terminated line.

As with any ECL design, care must be taken in laying out the circuit to realize maximum performance. Since the full logic-voltage swing appears at the transistor's base terminal, the base biasing resistor should be located close to that terminal to eliminate the transmission line effects of an interconnecting lead. □



Gating ECL signals. Bipolar transistor gate can transfer logic signals with propagation delay of as little as 100 picoseconds. With switch closed, transistor saturates and gates signals from flip-flop's $\overline{Q}$ output to its D input. When switch is open, transistor is cut off, and strong reverse bias at D input rejects all unwanted stray signals. The switch can be a pair of contacts or a TTL device.

Op amp cancels video switching transients

by Steven E. Holzman
Electromagnetic Systems Laboratories, Sunnyvale, Calif.

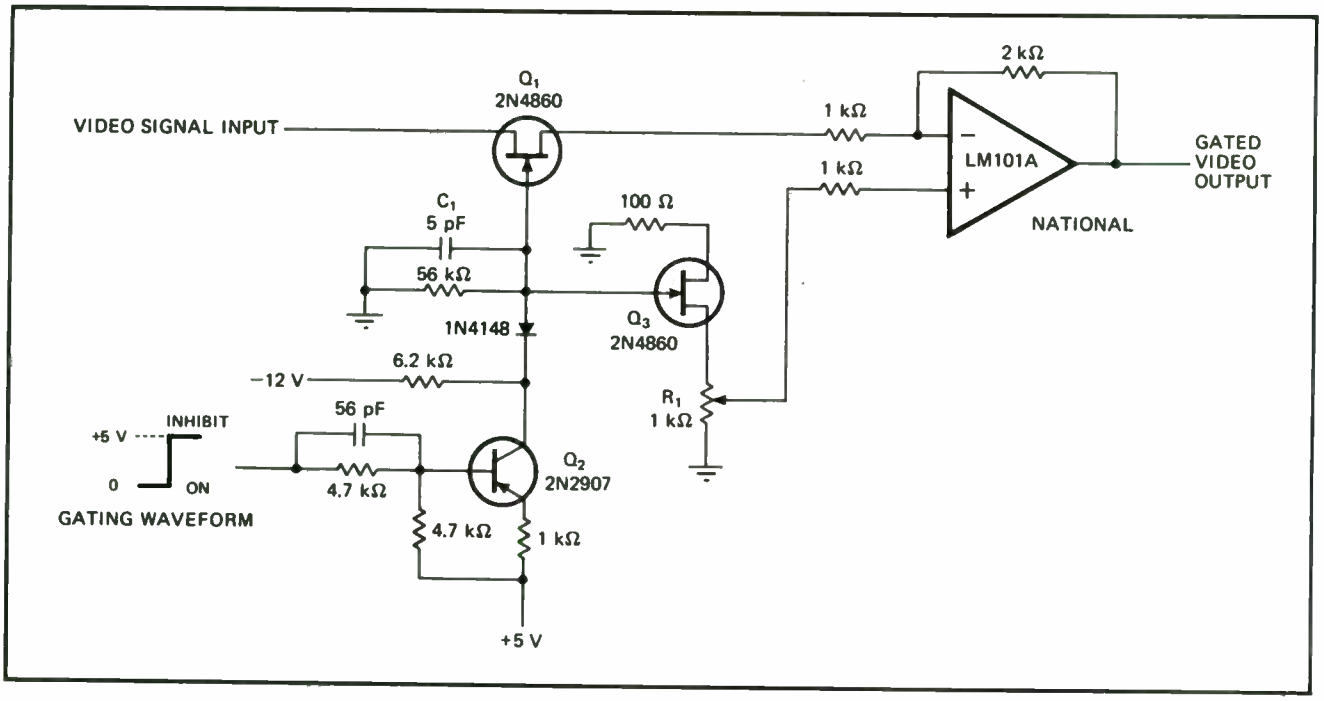
The common-mode rejection of an ordinary operational amplifier can help to minimize switching transients in low-level video gates. The transients are caused by the leading and trailing edges of the switching waveform.

The video gate basically consists of a switching field-effect transistor (Q_1), its associated TTL-compatible driver (bipolar transistor Q_2), and an output op amp. Transients are generated when the switching waveform edges pass through the FET's gate-drain junction.

By adding a second FET (Q_3) and its biasing resistors the transients can be eliminated by forcing them to cancel through the op amp. Since the transients from transistor Q_1 will be identical to those from transistor Q_3 the op-amp's common-mode rejection stops these unwanted spikes from reaching the output.

Capacitor C_1 helps maintain equal feedthrough char-

Transient-free video gate. Leading and trailing edges of gating waveform create transients when passing through first FET, Q_1. Including a second FET, Q_3, duplicates signal path of Q_1 and permits op-amp common-mode rejection to cancel most transients. Capacitor C_1 equalizes feedthrough characteristics of the two FETs so that matched pair is not necessary. Bipolar transistor Q_2 makes circuit TTL-compatible.



acteristics for both Q_1 and Q_3. This eliminates the need for a matched pair of FETs. By simply adjusting resistor R_1, nearly all of the transients can be cancelled.

In the circuit shown, the amplitude of the switching transients can be reduced to less than 1 millivolt over an operating temperature range of −20 to +60°C. □

Analog gate and zener diode give 70-dB isolation at 80 MHz

by Roland J. Turner,
General Electric Co., King of Prussia, Pa.

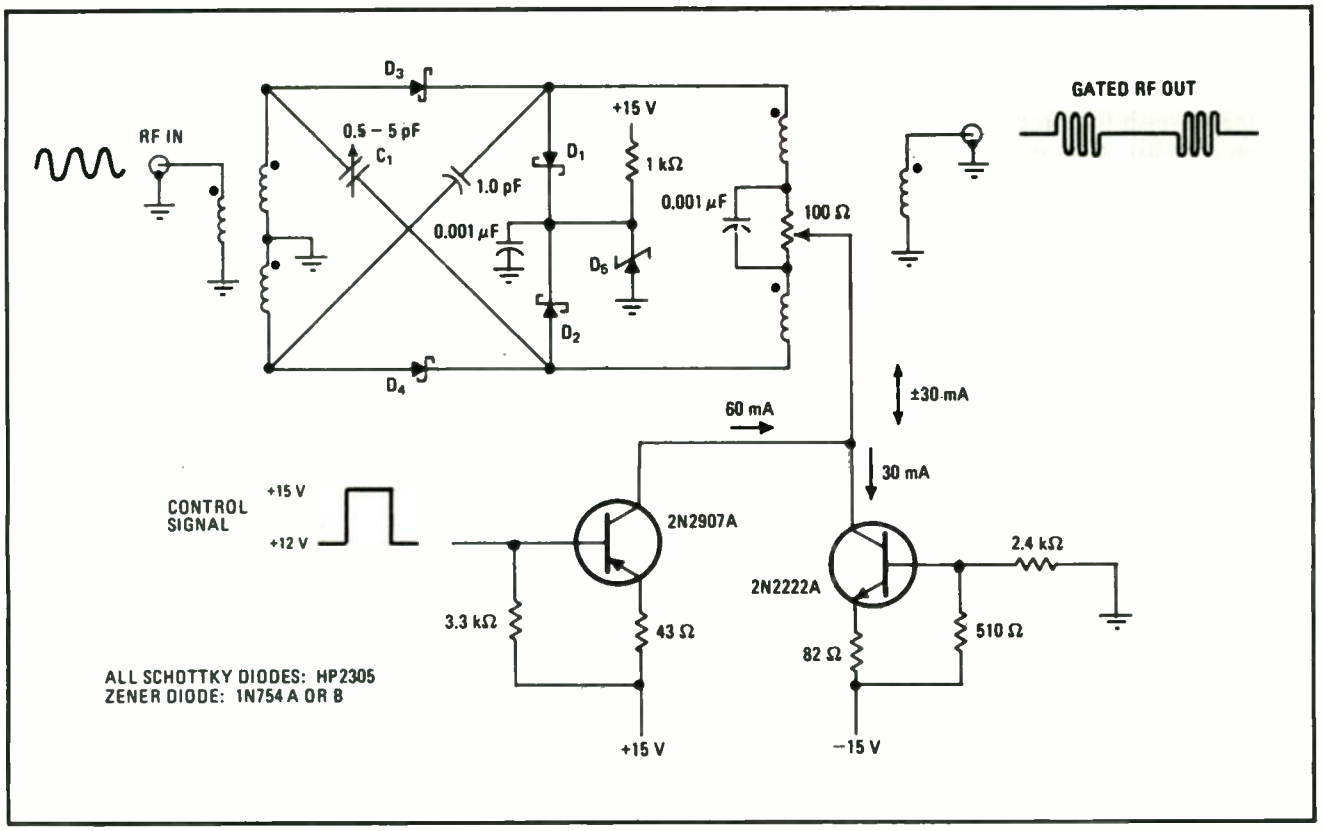
When conventional double-balanced Schottky diode mixers are used as analog signal gates, they have two serious limitations: the "off" impedance of a series diode offers a switch isolation of less than 40 decibels, and the peak radio-frequency input signal cannot exceed the series diode's forward blocking voltage—500 millivolts at room temperature, but falling to 300 mV at higher temperatures. An rf analog gate with both larger signal-handling capability and higher "off" isolation would be very useful, for example, in a pair of switches controlling a transmitter and receiver that share a common antenna.

The analog gate shown in the diagram achieves an "off" isolation of as much as 70 dB at 80 megahertz without using matched diodes. When +30 milliamperes is supplied to the gate, it turns on shunt diodes D_1 and D_2, while the series diodes D_3 and D_4 are reverse-biased by a voltage equal to the zener voltage at D_5 minus the positive swing of the input signal. With the gate biased off in this way, variable capacitor C_1 is trimmed, so that out-of-phase signals cancel signal leakage through the gate.

With a 6-V zener diode, this circuit isolates input signals of as much as 10 V peak to peak—whereas the mixer gate cannot handle even 1 V without letting the signal break through.

On the other hand, when the current is −30 mA, diodes D_3 and D_4 are forward-biased and the shunt diodes D_1 and D_2 become reverse-biased. The Schottky diodes have a dynamic impedance of 10 ohms, which is much less than the typical antenna impedance as seen from this gate (about 200 ohms). Thus the input signal passes through the gate with an insertion loss of less than 0.50 dB.

The gate's on-off status is controlled by the current source shown at the bottom of the diagram. When the control signal is at 12 V, the pnp transistor on the left is turned on, supplying +60 mA—half to the gate to turn it off, and half to the npn current sink on the right. But when the control signal rises to 15 V, the pnp transistor is cut off and the npn device, which stays on, reverses



High isolation. Control signal (lower left) turns on pnp transistor, providing + 30 mA to gate circuit at top, to turn it off and block passage of rf signal to antenna. When control is up, npn device takes over, drawing −30 mA from gate and turning it on. Zener voltage minus positive swing of input signal establishes reverse bias on series diodes, achieving isolation of as much as 70 dB at 80 MHz.

the current passing through the gate connection.

Both input and output transformers are conventional components, with bifilar 1:1:1 windings on Indiana General Q-3 core material. The center tap of the input transformer is grounded, while that of the output is split. At this point an RC network collects the -30-mA current when the gate is on. Because the two shunt diodes may have different voltage drops, the resistance is a potentiometer that can be adjusted to eliminate any dc bias at the output. □

C-MOS touch-switch array controls analog signals

by Max W. Hauser
Berkeley, Calif.

A few inexpensive complementary-MOS ICs can be used to create a bounceless buttonless touch-switch array. The resulting switching circuit takes advantage of the extremely high input impedance of C-MOS devices to detect the ambient signals (electrostatic charge and power-line hum) present on a person's finger. The circuit's outputs are solid-state switches that are capable of controlling audio or analog signals with negligible distortion and that, in many cases, are compatible with existing circuitry. Light-emitting diodes provide a visual display of the current state of these switches.

The heart of each touch-switch (a) is a set-reset flip-flop (one-quarter of a quad latch) whose inputs are biased to the V_{DD} supply through 22-megohm resistors. Under normal (resting) conditions, this renders the inputs inactive, and the flip-flop retains its last state. When a finger or large conductive object touches either the on or off input, a noise voltage appears across the bias resistor at that input and is amplified through the regenerative action of the flip-flop. This sets the flip-flop to the desired output state, where it remains until reset by touching the other input.

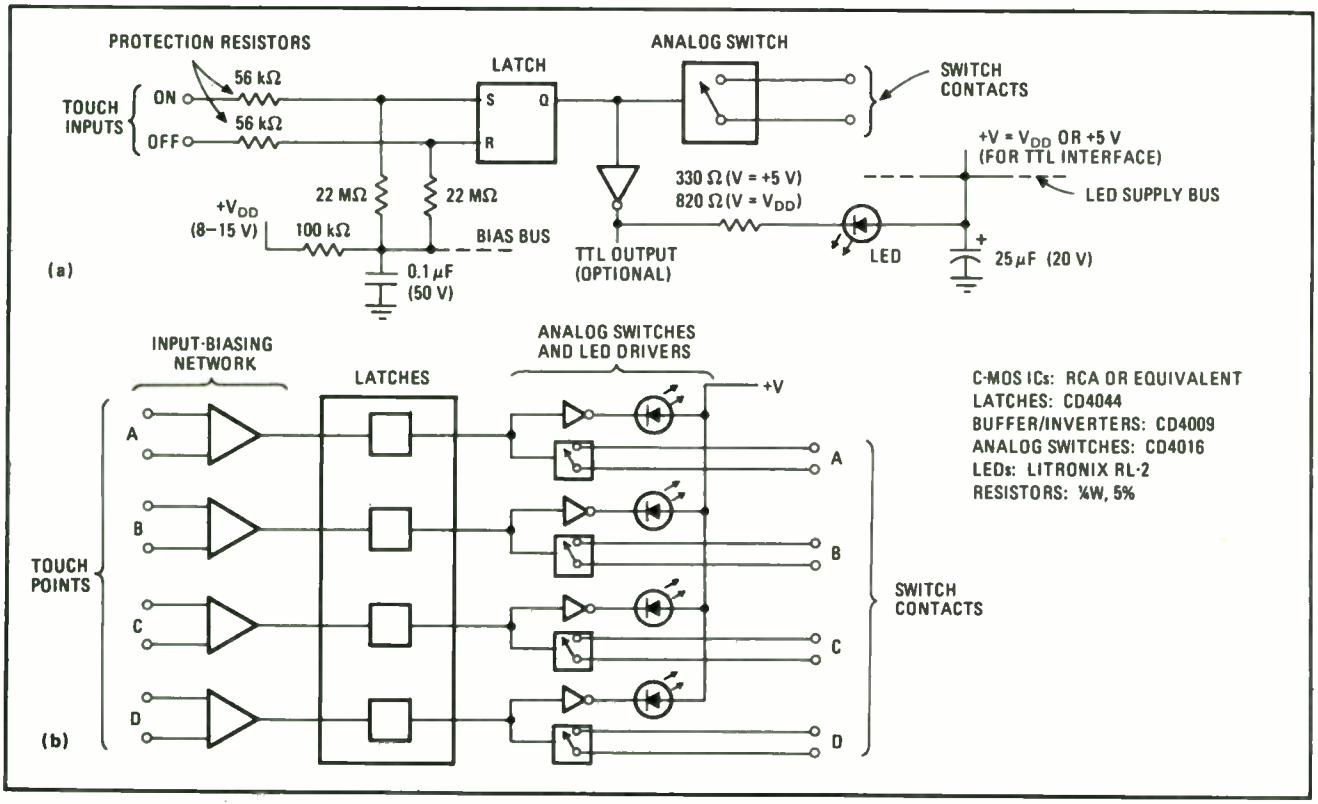
The flip-flop's output simultaneously controls an analog switch and a buffer/inverter that drives a panel-mounted LED. The output from the buffer can also be used to activate a TTL input, provided that the internal pull-up supply (V_{CC}) is made equal to the TTL power-supply voltage. The 100-kilohm resistor and the 0.1-microfarad capacitor serve to decouple the V_{DD} bias supply so that there is no interaction between the input and display portions of the circuit.

The block diagram (b) shows how a quadruple touch-switch array looks. The touch-sensors should be small metal plates—squares or disks having a side or diameter of 1 to 2 centimeters are best. A substantial increase in plate area results in a proportionate increase in the quiescent hum pickup, and can reduce circuit reliability

unless the sensor is mounted very carefully. At the expense of added construction complexity, the LEDs or their mountings can be given a conductive coating, permitting them to serve as the solid-state equivalent of illuminated push-button switches.

Type-CD4016 analog switches work well for noncritical applications, for example, if the circuit is to be used as a source selector for an audio-mixing console. In more critical systems, however, it may be desirable to substitute lower-impedance devices, such as type-CD4066 units. Of course, each flip-flop output can drive many analog switches, and a complex switching arrangement can be created that might be difficult or uneconomical to implement with mechanical devices. Normally closed switching is possible by driving the analog switches with the buffer/inverter outputs, but the circuit's TTL interface must be sacrificed.

In remote locations, where power lines or other major electromagnetic-field sources are not available, it is advisable to install a second contact (at ground potential) on each sensor, so that a slight conduction between the two contacts will assure triggering. Also, to eliminate any chance of damage to the flip-flop inputs from an external power source, the inputs should be protected against excessive current flow with 56-kilohm resistors, as shown. □



Touch-actuated switching. A simple touch-switch (a) can be built with complementary-MOS ICs. The high input impedance of the C-MOS latch permits the ambient signals of a fingertip to be sensed. The latch's output then controls a C-MOS analog switch, which implements the desired switching function. The LED indicates whether this analog switch is on or off. A quadruple touch-switch array is shown in (b).

Switching large ac loads with logic-level signals

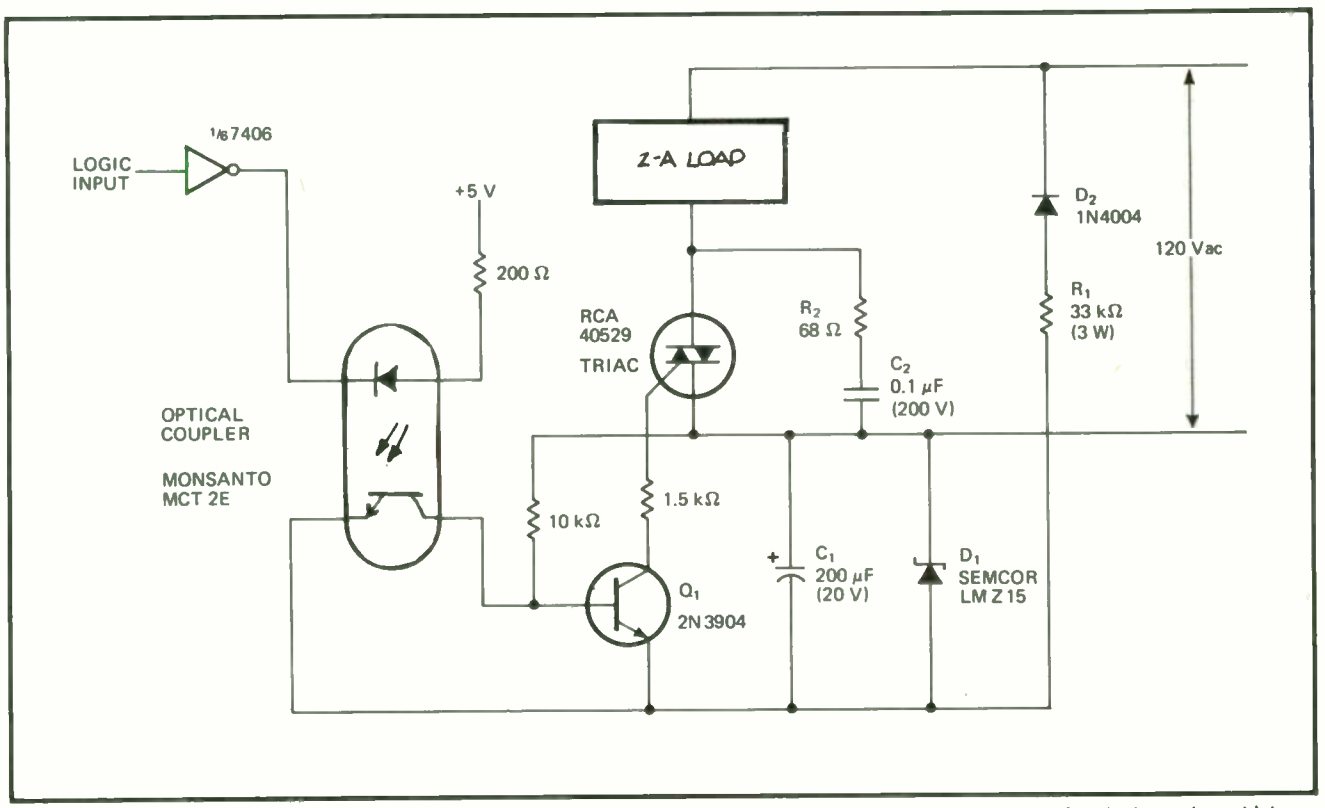
by Lynn S. Bell, *Bell Engineering, Tucson, Ariz.*,
and R. M. Stitt, *University of Arizona, Tucson, Ariz.*

An optical coupler makes it possible for integrated-circuit logic signals to switch safely and without isolation problems ac loads as large as 2 amperes.

In the circuit, capacitor C_1, zener diode D_1, diode D_2, and resistor R_1 provide a -15-volt supply, referenced to point A of the ac line source. A low-input logic signal to the inverter turns off both the light-emitting diode and the phototransistor in the optical coupler. For this circuit, the coupler provides 2,500 V of isolation.

After the coupler turns off, transistor Q_1 saturates, supplying a current of -10 milliamperes to the gate of the triac and turning this device on so that the load is energized. The triac will stay on through a complete half-cycle of the line voltage, once the logic input to the inverter goes low. The triac turns off at the first zero crossing of the load current that occurs after the logic input goes high.

Resistor R_2 and capacitor C_2 suppress possible radio-frequency interference and provide safe di/dt and dv/dt triac operation when driving inductive loads. □



Logic-driven ac load switch. Ac loads as large as 2 amperes can be safely switched by logic signals because of optical coupler, which provides up to 2,500 volts of isolation. A low logic input turns off the coupler's LED and phototransistor, causing transistor Q_1 to saturate. This triggers the triac's gate terminal, firing this device and energizing the load. The R_2C_2 network suppresses transients and rfi.

47. Temperature controls

Diode plus low-cost op amp makes accurate thermostat

by Robert Koss
Adac Inc., Colchester, Vt.

Employing a silicon diode as the temperature-sensing element allows an inexpensive operational amplifier to control temperature to a variation of less than 0.05°C. A type 1N4148 diode, for instance, has a typical temperature coefficient of -2 millivolts/°C.

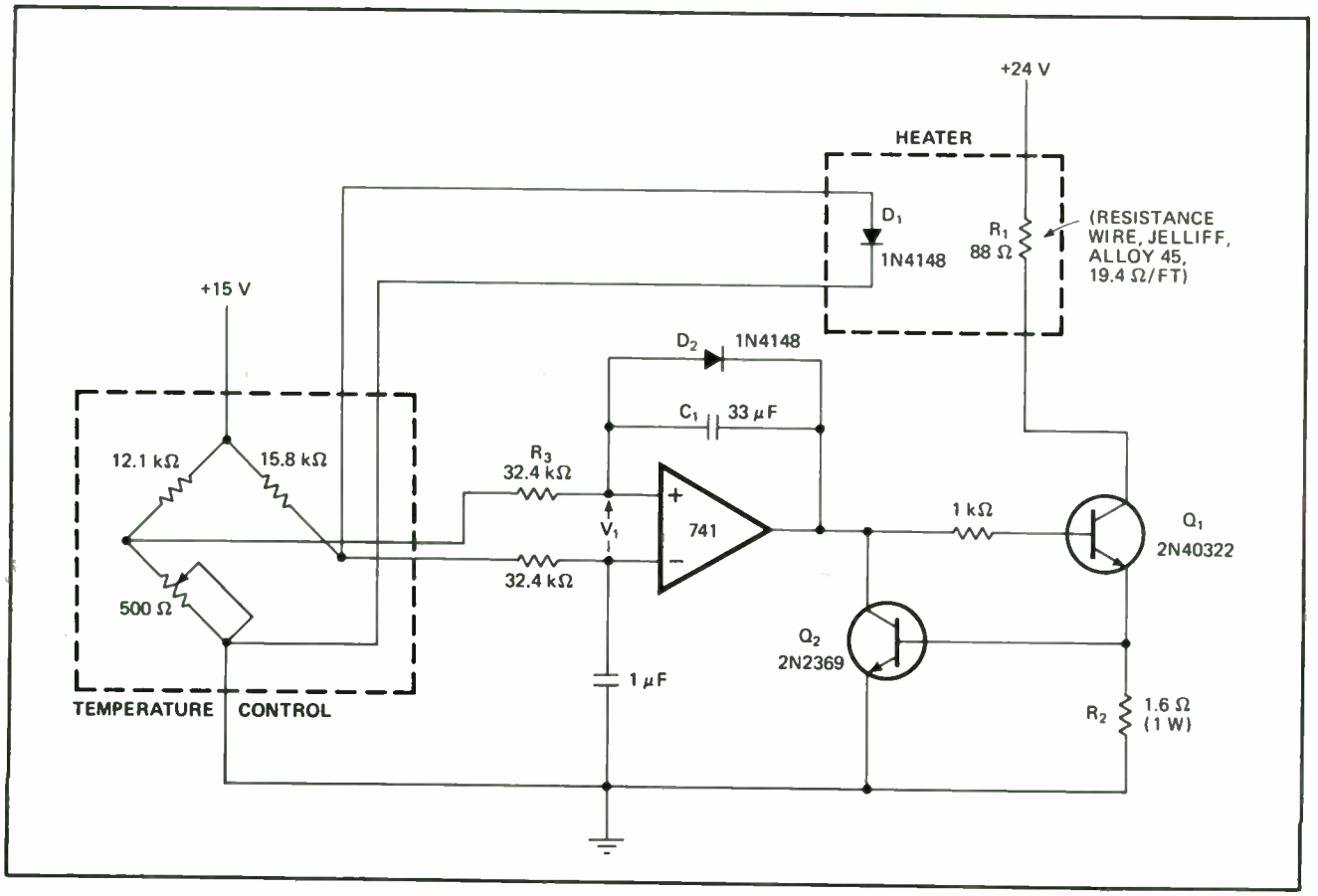
The resistance bridge in the diagram sets the temperature that is sensed by diode D_1 and that is maintained by the heater element, resistor R_1.

When temperature is too low, control voltage V_1 goes negative, limiting the op amp's output to 12–14 volts. Transistor Q_1 conducts and provides the necessary heater current. When temperature is too high, diode D_2 prevents amplifier output voltage from going negative, and transistor Q_1 turns off. Average current then is always positive and is controlled by the amplifier to compensate for changes in temperature.

Transistor Q_2 and resistor R_2 prevent the heater current from exceeding a specified limit. (For this circuit, maximum heater current is 375 mA.) If the voltage drop across resistor R_2 equals Q_2's 0.6-V base-emitter voltage, transistor Q_2 turns on, shorting the amplifier's current-limited output to ground, thus turning off transistor Q_1.

The stability of the control loop depends on several thermal time constants that are not easy to calculate. Computations can be reduced a little by using a relatively large time constant in the feed-forward direction for R_3C_1 and keeping the remaining thermal lags as small as possible. Sense diode D_1 should make good thermal contact with the object to be temperature-controlled. It should also be thermally insulated from changes in external conditions. □

Inexpensive thermostat. Tight temperature coefficient of silicon diode permits low-cost op amp to be used for controlling temperature to within 0.05°C. Resistance bridge sets temperature of heater containing sense diode D_1. For low temperatures, amplifier turns on transistor Q_1, which supplies heater current. For high temperatures, amplifier output remains positive because of diode D_2, but Q_1 stops conducting.



Soldering iron converts to constant-temperature probe

by Mahendra J. Shah
Univ. of Wisconsin, Space Science and Engineering Center, Madison, Wis.

Designing a circuit that has good temperature stability requires pinpointing those components that are the major drift contributors. These components can then be properly specified and compensated for temperature drift, if necessary. Unfortunately, the designer must frequently run temperature stability tests on the entire circuit because he cannot heat individual components selectively. And employing a soldering iron as a selective heat source does not produce precise temperature test results.

However, a conventional line-operated soldering iron can be easily converted into a constant-temperature probe. Since most low-power circuits operate very near ambient room temperature and most circuit components have a low thermal resistance for efficient heat transfer, the device being heated by the probe will be within a few degrees of the probe temperature. The drift contribution of the component can then be measured by noting the change in the circuit parameter of interest.

The temperature-control circuit in the diagram regulates the voltage applied to the tip of a 115-volt, 27-watt soldering iron, allowing tip temperature to be set from near room ambient to 125°C. A potentiometer permits the temperature setting to be varied continuously. The tip-temperature-sensing element is a thermistor, which is installed by drilling a small hole in the tip and then epoxy-mounting the thermistor in place.

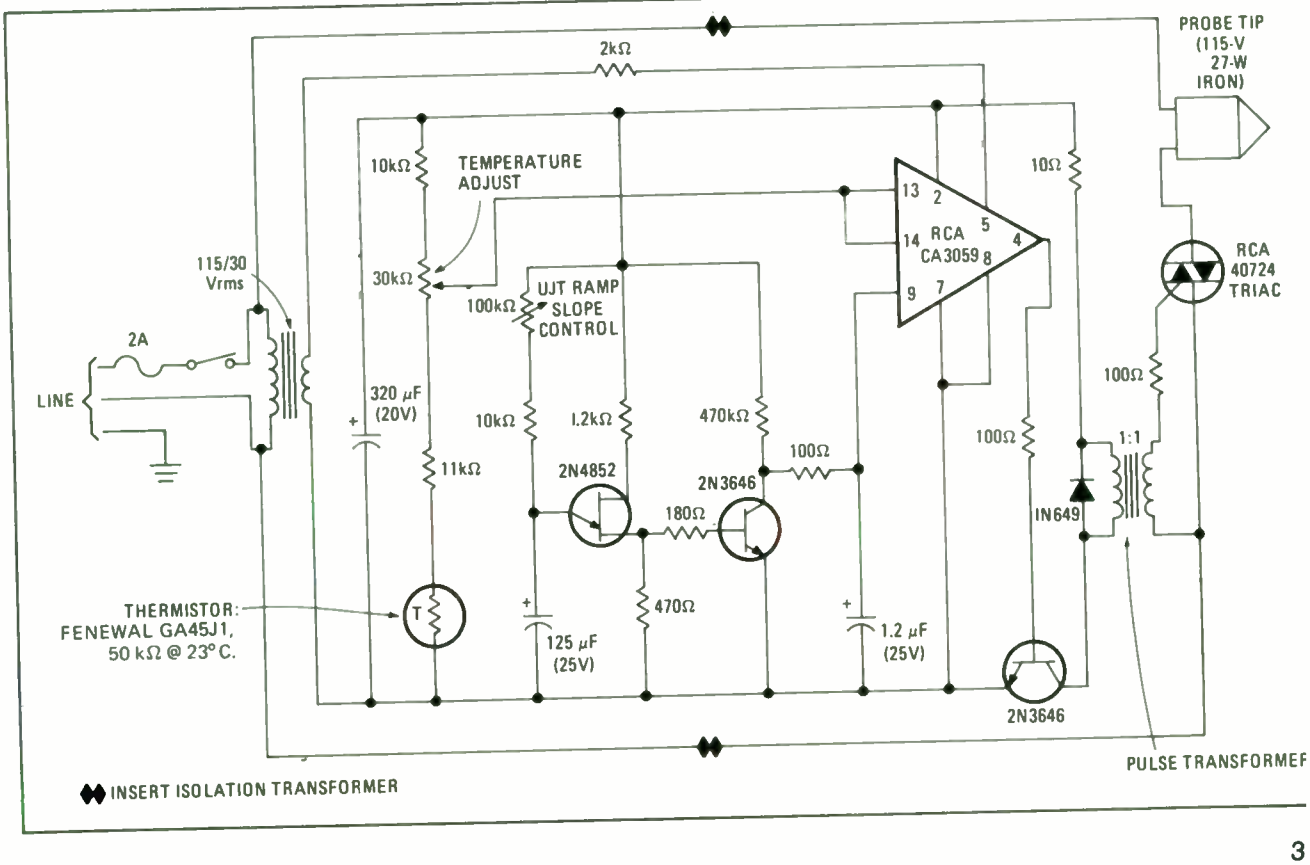
For best results, an isolation transformer should be placed between the source of line power to the tip and the triac at the output of the control circuit. The heat transfer of the probe can be improved by using silicone vacuum grease between the tip and the component under test.

Sometimes, testing component drift with a constant-temperature probe can reduce parts cost. For instance, suppose a regulated 600-v power supply that contains a high-stability zener reference costing about $24 is tested. When the temperature of the whole supply is increased by approximately 50°C, the supply output drops around 5 v.

A transistor junction is found, with the probe, to be the principal cause of the drift. Substituting a general purpose zener selling for about $1 for the high-stability device will decrease over-all supply drift. The temperature-drift errors of the transistor junction and the low cost zener almost cancel each other, since they have about the same magnitude but are of opposite polarity.

It is also possible to build a probe that lowers component temperature below room ambient by using a thermoelectric cooling element in a temperature-control loop.

Pinpointing component drift. Constant-temperature probe can be built by controlling power to tip of soldering iron. Control circuit maintains tip temperature within a few degrees of desired setting, from room ambient to 125°C. Thermistor located inside probe tip acts as the temperature-sensing element. An isolation transformer (not shown) should be placed between the line input and circuit's output triac.



Using transistor arrays for temperature compensation

by Mahendra J. Shah
University of Wisconsin, Madison, Wis.

Monolithic transistor arrays make handy temperature-compensating devices. For instance, a highly temperature-stable zener reference can be realized by employing one of the transistors as a zener diode, a second transistor as a conventional diode, a third transistor as a chip heater, and a fourth transistor as a chip-temperature sensor.

A typical transistor array is shown in (a), RCA's model CA3046. Only two of the five transistors are needed to implement a temperature-compensated zener diode, which is also shown in (a). It is obtained by reverse-biasing the base-emitter junction of one transistor (Q_3 is used here) and then temperature-compensating this device with the forward-biased base-emitter junction of a second transistor (Q_2 here).

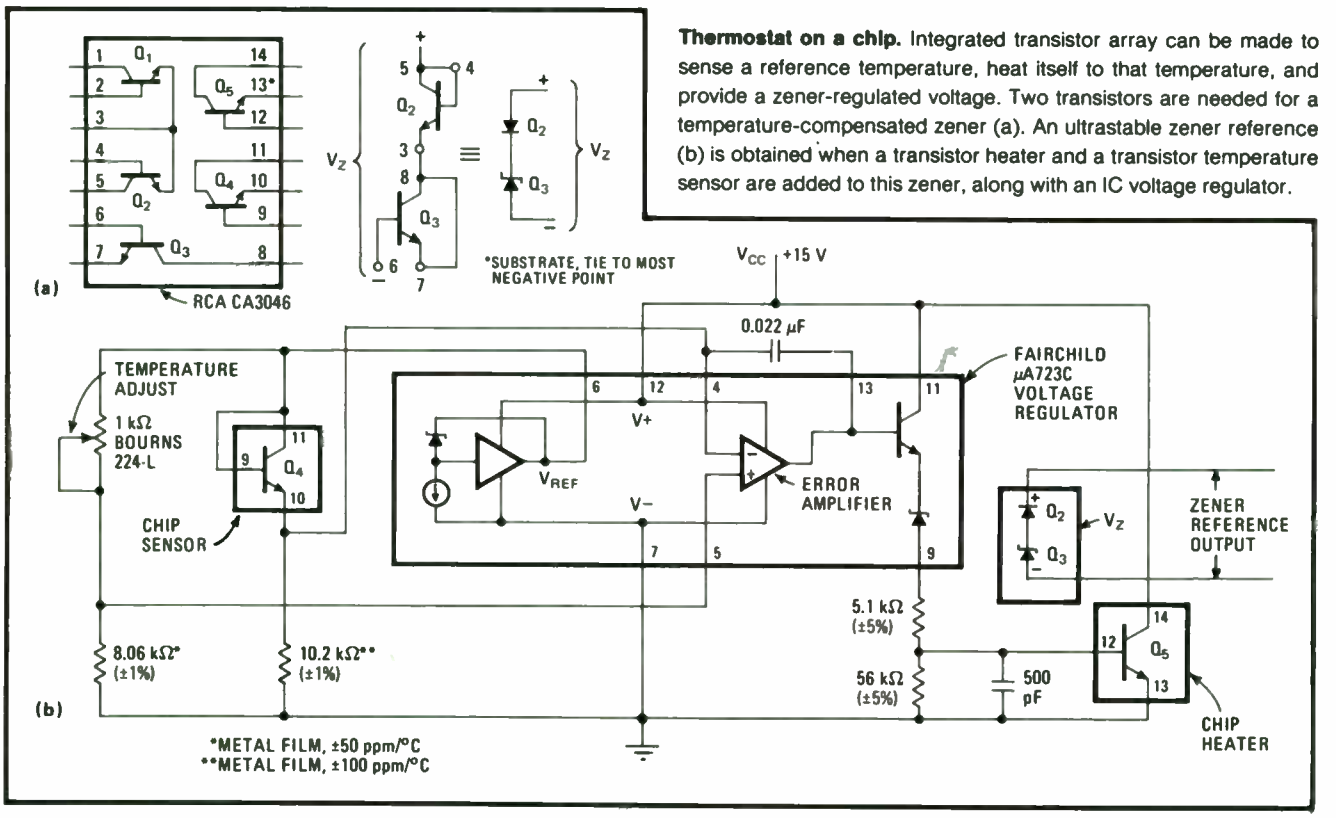
Since all the transistors make good thermal contact with each other, good temperature compensation is provided. For a zener reference current of 200 microamperes, the two-transistor zener develops 7.83 volts and has a temperature coefficient of +196 ppm/°C.

Even better temperature stability can be obtained by making one of the transistors a chip heater, by connecting its collector to the supply voltage. Whatever heat is dissipated in this transistor heats the entire chip. A fourth transistor, with a forward-biased base-emitter junction, can then act as a chip-temperature sensor. It will have a sensitivity of about −2 millivolts/°C. When the heater/sensor arrangement is used with the temperature-compensated zener of (a), the array exhibits a temperature coefficient of merely −3.1 ppm/°C from 33°C to 50°C.

By adding temperature-reference and temperature-control functions to the array (compensated zener, chip heater, and chip sensor), a highly stable zener reference is formed. In (b), an integrated voltage regulator provides these temperature-reference and temperature-control functions with its internal voltage reference and error amplifier.

The potentiometer sets the circuit's temperature-reference voltage, which is compared with the voltage developed by the chip-temperature sensor (transistor Q_4). Any difference voltage between the two passes through the error amplifier before being applied to the chip heater (transistor Q_5). The heater then brings the chip sensor to the temperature that is set up as the temperature reference, keeping the temperature of the entire transistor array constant.

The zener reference circuit, which uses only one power supply, offers a temperature coefficient of +4.25 ppm/°C from 33°C to 50°C for zener current of 200 μA. (Transistor Q_1 of the array is not used.) □



Thermostat on a chip. Integrated transistor array can be made to sense a reference temperature, heat itself to that temperature, and provide a zener-regulated voltage. Two transistors are needed for a temperature-compensated zener (a). An ultrastable zener reference (b) is obtained when a transistor heater and a transistor temperature sensor are added to this zener, along with an IC voltage regulator.

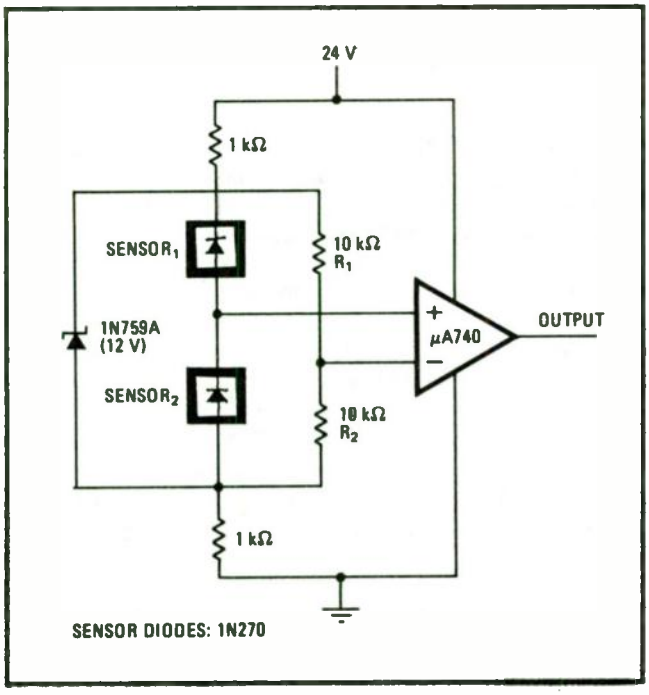
Diode pair senses differential temperature

by Don DeKold
Dekolabs, Gainesville, Fla.

Normally, a germanium diode functioning as a temperature sensor relies on the linear variation of its forward voltage with temperature. But a pair of germanium diodes can be made to serve as a differential-temperature comparator if the circuit exploits a much less used temperature-dependent diode property—the logarithmic variation with temperature of the reverse saturation current. The resulting circuit is useful for industrial-control applications.

When one diode ($SENSOR_1$) is at temperature T_1 and the other diode ($SENSOR_2$) is at temperature T_2, the circuit output will change state as the temperature differential (T_1–T_2) approaches and crosses a differential threshold, $\Delta T_{1,2}$. For the circuit shown here, $\Delta T_{1,2}$ is 13°C—when (T_1–T_2) is less than 13°C, the circuit's output is low; and when (T_1–T_2) is greater than 13°C, the output goes high. The circuit has a fairly wide and useful temperature range of 20°C to 120°C.

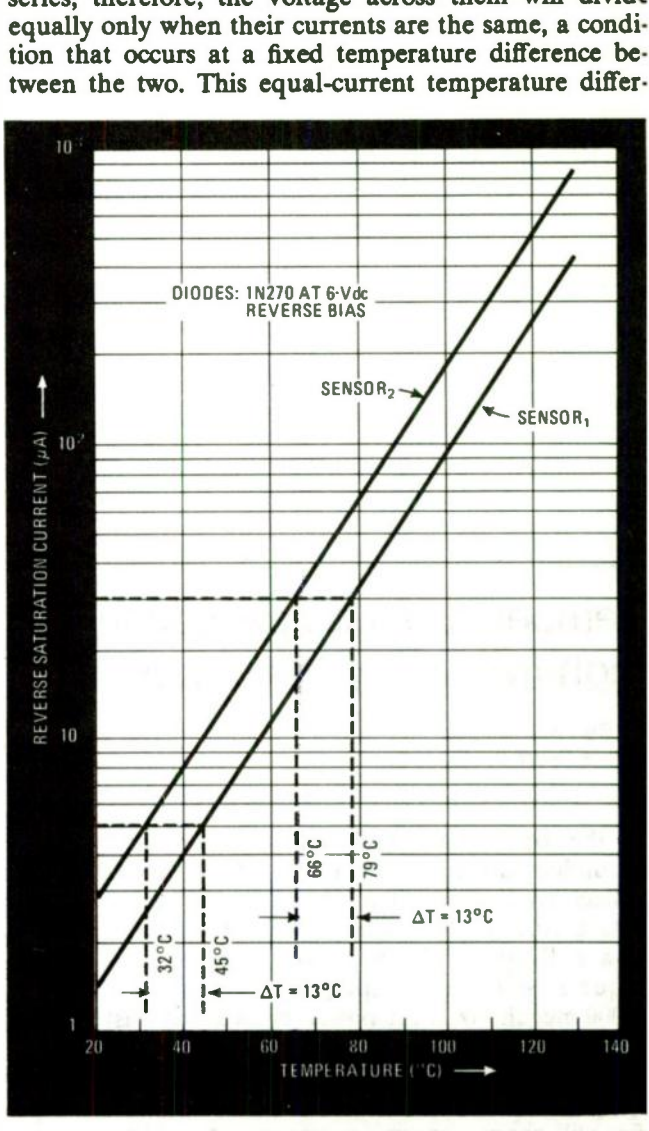
The two diodes, along with resistors R_1 and R_2, form a resistance bridge. The right-hand side of the bridge consists of equal resistances that divide the bridge voltage in half, establishing a reference voltage at the inverting terminal of the FET-input operational amplifier. The noninverting op-amp terminal receives the temperature-dependent voltage, which is derived from the division of the bridge voltage across the diode temperature sensors.



In general, the reverse saturation currents of two unmatched diodes are different at a single temperature. However, when plotted as a function of temperature on semilog paper, the two reverse-current characteristics will be parallel to each other. That is, a diode's reverse current may vary from one unit to the next at a single temperature, but it will increase in an identically proportional manner from one unit to the next as a function of temperature.

For instance, for the type 1N270 germanium diodes used here, the current doubles every 13°C. The doubling is highly regular, producing a nearly linear semilog plot over a fairly wide temperature range, as shown by the graph of reverse saturation current versus temperature for two type IN270 diodes.

Now, when a diode is reverse-biased, it in effect becomes a temperature-dependent current source with a reverse saturation current that is only negligibly influenced by the actual magnitude of the reverse voltage. But as the reverse voltage approaches zero, the reverse current decreases. When two diodes are connected in series, therefore, the voltage across them will divide equally only when their currents are the same, a condition that occurs at a fixed temperature difference between the two. This equal-current temperature differ-



Temperature comparator. Unmatched germanium diodes have different reverse saturation currents at the same temperature. But this difference remains proportionate with changing temperature so that the temperature differential between the two currents stays the same, as shown by the graph. A differential-temperature comparator can be built by connecting two unmatched diodes in a bridge configuration.

ential is the $\Delta T_{1,2}$ threshold for the circuit.

The diode having the lower reverse saturation current acts here as $SENSOR_1$, so that practically all of the bridge voltage will be dropped across it. This keeps the voltage at the noninverting op-amp input below that of the inverting op-amp input, and the circuit's output is low. As the temperature of $SENSOR_1$ increases, its reverse leakage current will also rise.

When $SENSOR_1$ is $\Delta T_{1,2}$ degrees celsius above $SENSOR_2$, the voltages at the op-amp inputs will be equal. With an additional temperature increase of $SENSOR_1$, most of the bridge voltage will then be dropped across $SENSOR_2$. This raises the voltage of the noninverting op-amp input above that of the inverting op-amp input, causing the circuit's output to go high.

Various operating conditions can be set up for the differential-temperature comparator by interchanging the locations of the low-current and high-current diodes or by switching the input connections to the op amp. Different diode pairs will provide different values of threshold temperature. Basically, $\Delta T_{1,2}$ is determined by the ratio of diode leakage currents at a fixed temperature, and this current ratio increases as the comparator differential increases. Diodes with identical reverse currents at the same temperature produce a $\Delta T_{1,2}$ of 0°C.

A FET-input op amp must be used here to assure that there is practically no loading of the bridge diode divider. Minimal loading is particularly important if the absolute temperatures to be compared differentially are low. □

Temperature compensation for high-frequency transistors

by Bert K. Erickson
General Electric Co., Syracuse, N.Y.

If the operating temperature of a high-frequency grounded-emitter power transistor varies widely, the collector resistance of a second transistor can provide temperature compensation, without causing excessive power dissipation in the stage's bias circuit. The technique is suitable for operating frequencies of 300 to 3,000 megahertz, if the power levels are at least 200 milliwatts and ambient temperature variations range from 0°C to 70°C. For this broad a temperature range, the quiescent collector current of a class-A transistor amplifier will change enough to cause noticeable gain variation and waveform distortion.

Conventionally, a current-feedback approach is employed to obtain temperature stability. The resistance in the transistor's emitter circuit is maximized, while the resistance in the base circuit is minimized. But this technique presents assembly problems because of the very high operating frequencies involved. The emitter of these transistors is usually connected to ground with very short wire bonds to eliminate the series resonance of the bypass capacitor. And, although the transistor's emitter is grounded, temperature stability cannot be obtained with a voltage-feedback approach since this would reduce power-conversion efficiency.

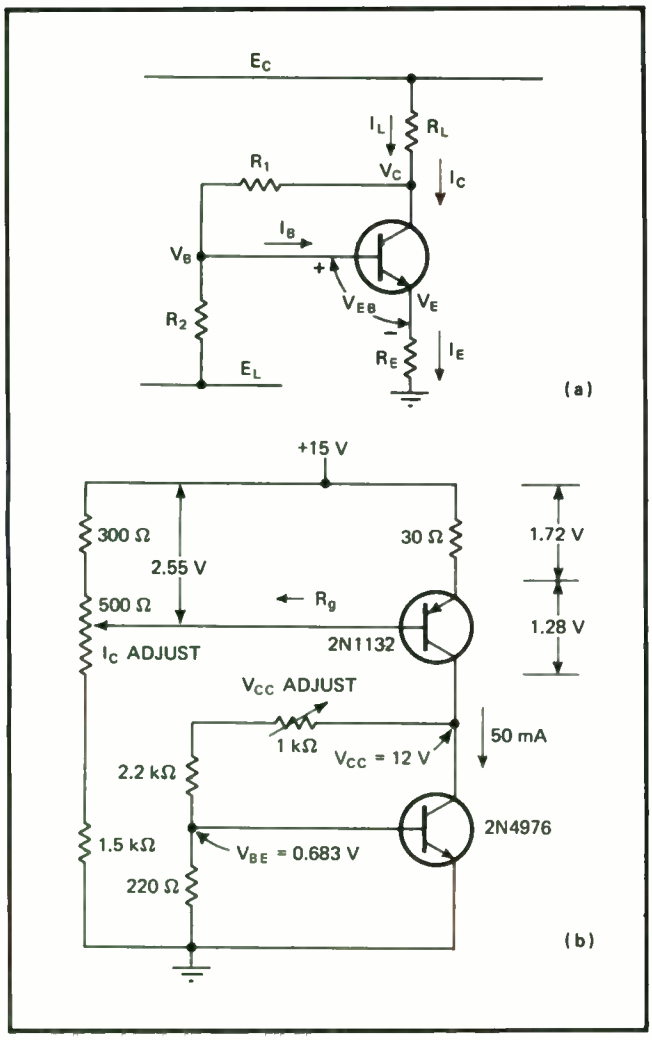
The typical grounded-emitter transistor stage of (a), which is drawn without isolating, coupling, and tuning components for simplicity, has a current stability factor of:[1]

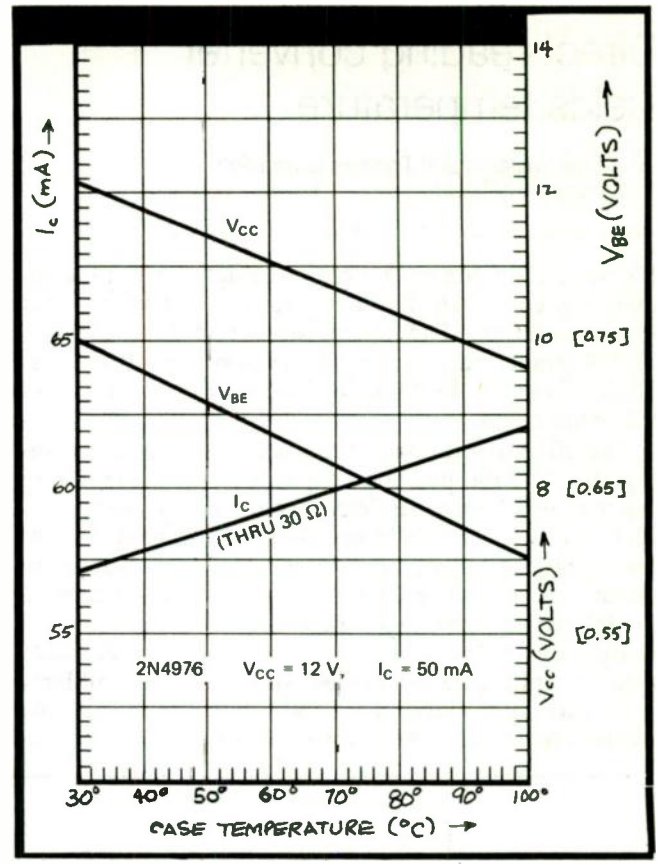
$$S_i = \Delta I_C/\Delta I_{CO} = [R_L+R_1+R_E(1+(R_1+R_L)/R_2)]/[R_L+R_1(1-\alpha)+R_E(1+(R_1+R_L)/R_2)]$$

And the voltage stability factor is:[1]

$$S_v = \Delta I_C/\Delta V_{EB} = -\alpha[1+(R_1+R_L)/R_2]/[R_L+R_1(1-\alpha)+R_E(1+(R_1+R_L)/R_2)]$$

Voltage stability is the preferred sensitivity parameter for a power transistor because the emitter-base voltage.





Nailing down Q point. Grounded-emitter power transistor stage (a) can be compensated for a 70°C temperature range by employing a second transistor as the load resistance (b). The collector resistance of upper transistor improves the voltage and current stability of lower transistor without causing an efficiency-robbing voltage drop. The graph depicts the stage's temperature performance.

V_{EB}, is easily measured and is often used to find the temperature of the collector depletion layer.[2] The voltage stability factor is negative because collector current I_C increases as junction voltage V_{EB} decreases.

Since the term, $R_1(1-\alpha)$, is very small, one way to diminish S_v is to make the load resistance, R_L, as large as possible. Unfortunately, I_C flows through R_L, and the stage's conversion efficiency will be reduced substantially. However, a large R_L can be obtained without the usual voltage drop degradation by using the collector resistance of a second transistor, as in (b).

With the T-model equivalent circuit for the common-emitter transistor, the output resistance of this configuration can be expressed as:

$$r_o = r_c(1-\alpha) + r_e(r_b + \alpha r_c + R_g)/(r_b + r_e + R_g)$$

For this equation:

$$1/r_c(1-\alpha) = \Delta i_c/\Delta v_{ce}|_{i_b}$$

$$\beta = \Delta i_c/\Delta i_b|_{v_{ce}}$$

$$\alpha = \beta/(\beta+1)$$

All of these quantities can be readily obtained from the transistor's collector characteristics.[3]

The upper transistor in (b) provides an output resistance of 1,200 ohms, which yields a predicted voltage stability factor of 14.9×10^{-3} amperes per volt. If a fixed resistor of 1,200 ohms were used, it would have an IR drop of 60 V across it. But the voltage drop across both the transistor and its emitter resistor is only 3 V.

The graph shows the actual characteristics of the transistor stage as temperature rises from 30°C to 100°C. As temperature increases by 70°C, the base-emitter voltage drops by only 0.15 V and the collector current rises only 5 milliamperes. Without temperature compensation, the collector current would be 32 mA higher. □

REFERENCES

1. M.V. Joyce and K.K. Clark, "Transistor Circuit Analysis," Addison-Wesley, 1964, Chap. 3.
2. R.L. Pritchard, "Electrical Characteristics of Transistors," McGraw-Hill, 1967, p. 613.
3. R.P. Nanavati, "An Introduction to Semiconductor Electronics," McGraw-Hill, 1963, p. 163.

Direct-reading converter yields temperature

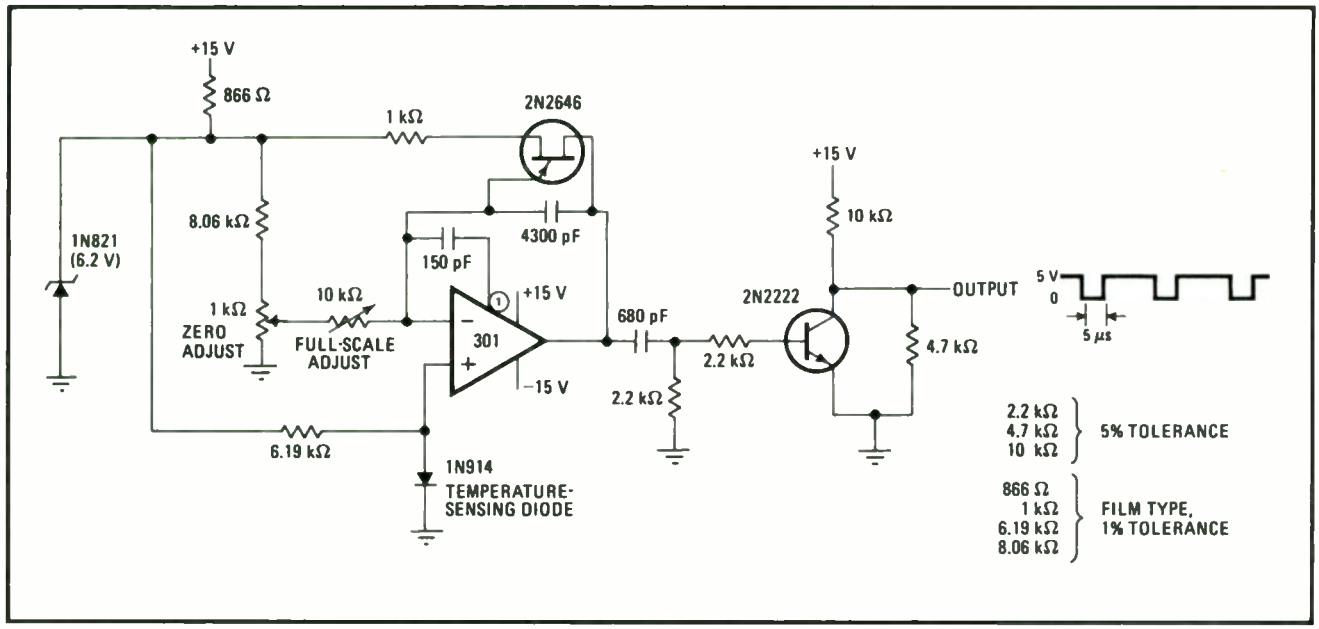
by James Williams and Thomas Durgavich
Massachusetts Institute of Technology, Cambridge, Mass.

It's possible to convert temperature accurately to a numerically equivalent frequency for direct display or for instrumentation. The circuit described here uses an 1N914 temperature-sensing diode to provide 0.1°C resolution from 0°C to 100°C, with accuracy of ±0.3°C over the entire range.

The 301A operational amplifier is set up as an integrator. The 150-picofarad capacitor from the inverting input to pin 1 provides feed-forward compensation for high slew rate. The 2N2646 unijunction transistor resets the integrator when the 4300-pF capacitor charges to about -10 volts. The 1N821 temperature-compensated diode provides a voltage reference that determines the firing point of the unijunction transistor, provides stable zero and full-scale references, and sends a 1-milliampere current through the 1N914 temperature-sensing diode. The 2N2222 transistor and its associated components provide an output pulse that is compatible with transistor-transistor logic.

In operation, the circuit functions as a voltage-to-frequency converter. The voltage at the wiper arm of the 1-kilohm potentiometer is integrated until the transistor's firing point is reached. When the transistor fires, it resets the capacitor. The frequency of oscillation is related to temperature because the diode voltage biases the integrator via the noninverting input. The only variable voltage available to the amplifier is the temperature-dependent (-2.2 millivolts per °C) potential from the 1N914 diode. To adjust the circuit, put the diode in a 100°C environment and turn the 10-kilohm potentiometer till the output frequency is 1,000 hertz. Then put the diode in a 0°C environment, and turn the 1-kilohm potentiometer for 0 Hz out. This procedure must be repeated two or three times, until the adjustments cease to interact. Once the circuit is adjusted, its output frequency is 10 times the sensed temperature within 0.3°C from 0° to 100°C. For example, if the temperature is 37.5°C, the meter will read 375 Hz.

The output frequency can be counted by TTL counters and a 1-Hz square wave. The 1-Hz square wave can be fed to the base of the 2N2222 through a 2.2-kilohm resistor, and the resultant gated pulses at the output can then be fed to TTL counters. □



Temperature-to-frequency converter. Frequency of relaxation oscillator varies with temperature-dependent voltage across 1N914 diode. Over 0°C-to-100°C temperature range, frequency changes linearly from 0 to 1,000 Hz. Therefore frequency meter at output can show temperature directly. Accuracy is ±0.3°C. Excellent performance and low cost (less than $5 for parts) make this circuit outstanding.

48. Timing circuits

Silent timer warns of tape run-out

by Vernon R. Clark
Applied Automation Inc., Bartlesville, Okla.

At concerts and lectures especially, a cassette tape often runs out unnoticed. One solution is to install timing circuitry in the cassette-recorder case that will cause a light to flash when it's time to reverse or replace a cassette or to switch to another recorder. This silent warning system is also useful in duplicating cassette masters, where a preset recording time is important.

The alarm circuit operates from any voltage in the 5- to-15-volt range and can either be connected to the recorder bus or use its own battery. When the circuit is turned on, a light-emitting diode begins to blink once or twice per second, indicating that the circuit is functional and ready to start timing. When the start-timing button is pushed, the LED stops flashing and stays off for the duration of the timing period. At the end of the timing period, the LED begins to flash again, giving the signal to flip the tape.

The two main components of the circuit are a 14536 programable-timer integrated circuit and a 74C00 quad NAND gate IC. The timer contains an oscillator and a 24-stage counter. It counts pulses from the oscillator and, when some specified counter stage goes high, delivers a positive output pulse from the decode-out terminal (pin 13). Which of the counter stages triggers the output is specified by the voltages on pins 9, 10, 11, and 12. If these pins are high, high, low, and low, respectively (logic 1100), an output appears every time that stage 12 of the counter goes high. With all four pins high (logic 1111), output appears when stage 24 goes high.

Since this system was designed for a standard C90 cassette, which runs for 45 minutes a side, the timer is adjusted to provide a timing period of 44 minutes, or 2,640 seconds.Therefore the oscillator frequency is set at

$$f_{osc} = 2^{23}/2{,}640 = 3.2 \text{ kilohertz}$$

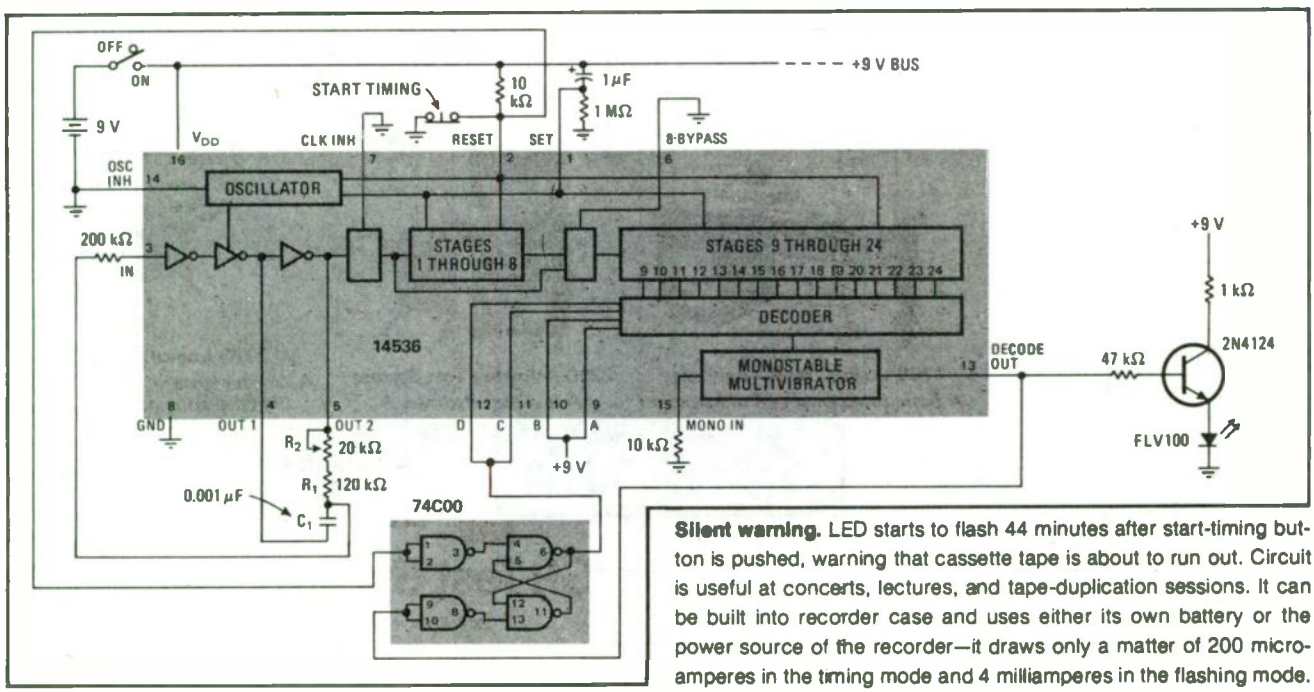
so that counting stage 24 will go high 44 minutes after the counter starts counting pulses from the oscillator (provided the decoder logic is 1111).

With this oscillator frequency, if the decoder terminals are set at logic 1100, stage 12 goes high after 2^{11} pulses, or

$$2^{11}/3.2 \text{ kHz} = 0.65 \text{ second}$$

The oscillation frequency is set by the time constant of C_1 and $(R_1 + R_2)$. A frequency meter is connected to pin 5, and R_2 is adjusted till the meter shows 3.2 kHz.

The circuit operates as follows: while the on-off switch is off, all pins are low. When the switch is turned on, pins 9 and 10 of the timer go high because they are wired to the positive-voltage bus. Therefore the decoder is programed with logic 1100, and the LED begins to flash every 0.65 second. When the start-timing button is pushed, the quad NAND circuit sets the decoder to logic 1111, so the LED stops flashing and the 44-minute count begins. After 44 minutes, the decode-out terminal (pin 13) goes high, resetting the decoder to 1100 so that the alarm signal flashes again. □



Silent warning. LED starts to flash 44 minutes after start-timing button is pushed, warning that cassette tape is about to run out. Circuit is useful at concerts, lectures, and tape-duplication sessions. It can be built into recorder case and uses either its own battery or the power source of the recorder—it draws only a matter of 200 microamperes in the timing mode and 4 milliamperes in the flashing mode.

Compensating the 555 timer for capacitance variations

by Kenneth Lickel
Philips Medical Systems Inc., Shelton, Conn.

With the 555 timer, any error in the value of the external timing capacitor causes a corresponding error in the duration of the output pulse. If several fixed timing resistors are used to permit selection of various output pulse widths, it may be desirable to compensate for the capacitor variation instead of changing each timing resistor. The circuit below allows correction for capacitor tolerance variations up to ±12.5% by adjustment of a single variable resistor.

The output pulse width, t, is given by the time required for the timing capacitor to rise to the value of the control voltage, V_{CON}. That relationship can be shown by the equation:

$$V_{CON} = V_{CC}(1 - e^{-t/RC})$$

or

$$t = -RC\ ln(1 - V_{CON}/V_{CC})$$

This equation shows that the pulse duration depends on the ratio of V_{CON} to supply voltage V_{CC} for given values of timing resistor R and timing capacitor C.

In the technique used to compensate for error in the timing-capacitor value, the ratio V_{CON}/V_{CC} is varied with an external resistance that shunts the 10-kilohm resistance inside the timer. As the circuit diagram shows, this external resistance consists of a 200-kilohm variable resistor R_A in series with a 17.8-kilohm fixed resistor R_B. The ratio V_{CON}/V_{CC} determined by the voltage-dividing network is:

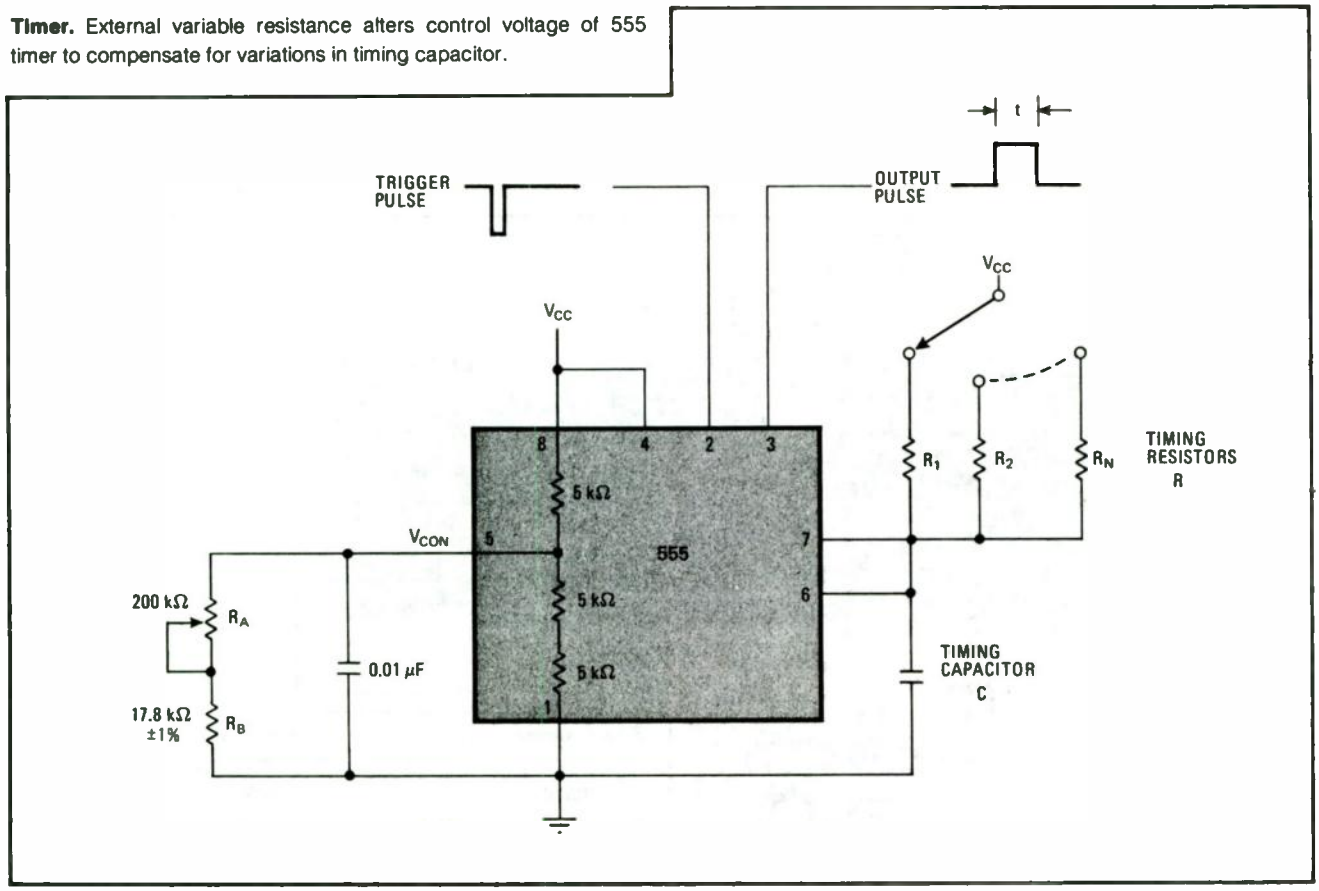
$$V_{CON}/V_{CC} = R_p/(R_p + 5\ k\Omega)$$

where

$$R_p = (10\ k\Omega)(R_A + R_B)/(10\ k\Omega + R_A + R_B)$$

If R_A is set at its minimum value (zero):

Timer. External variable resistance alters control voltage of 555 timer to compensate for variations in timing capacitor.



$R_p = 6.4\ k\Omega$

and

$V_{CON}/V_{CC} = 0.56$

Therefore, the pulse duration is

$t_{min} = 0.83\ RC$

Similarly, if R_A is set at its maximum value (200 kilohms), the pulse duration is:

$t_{max} = 1.07\ RC$

Thus the variation of R_A can vary the output-pulse width by ± 12.5% about a nominal value of (0.83 + 1.07)RC/2. For the circuit shown, therefore, the nominal width of the output pulse is:

$t_{nom} = 0.95\ RC$

If values for the timing resistors and capacitor are calculated from this formula, then capacitor variations of ±12.5% can be compensated by adjustment of R_A. If wider tolerances are desired, R_B must be reduced; new values must then be calculated for R_p, V_{CON}/V_{CC}, t_{min}, t_{max}, and t_{nom}. □

Discriminator displays first of four responses

by John S. French
Western Electric Co., Inc., Sunnyvale, Calif.

A first-response discriminator, which turns on a light indicating the first switch to close and simultaneously locks out the other switches, can be useful in sports, games, behaviorial learning studies, and experiments in physical science. The circuit shown here indicates which of four switches closes first. It uses three low-drain C-MOS integrated circuits and a 9-volt radio battery.

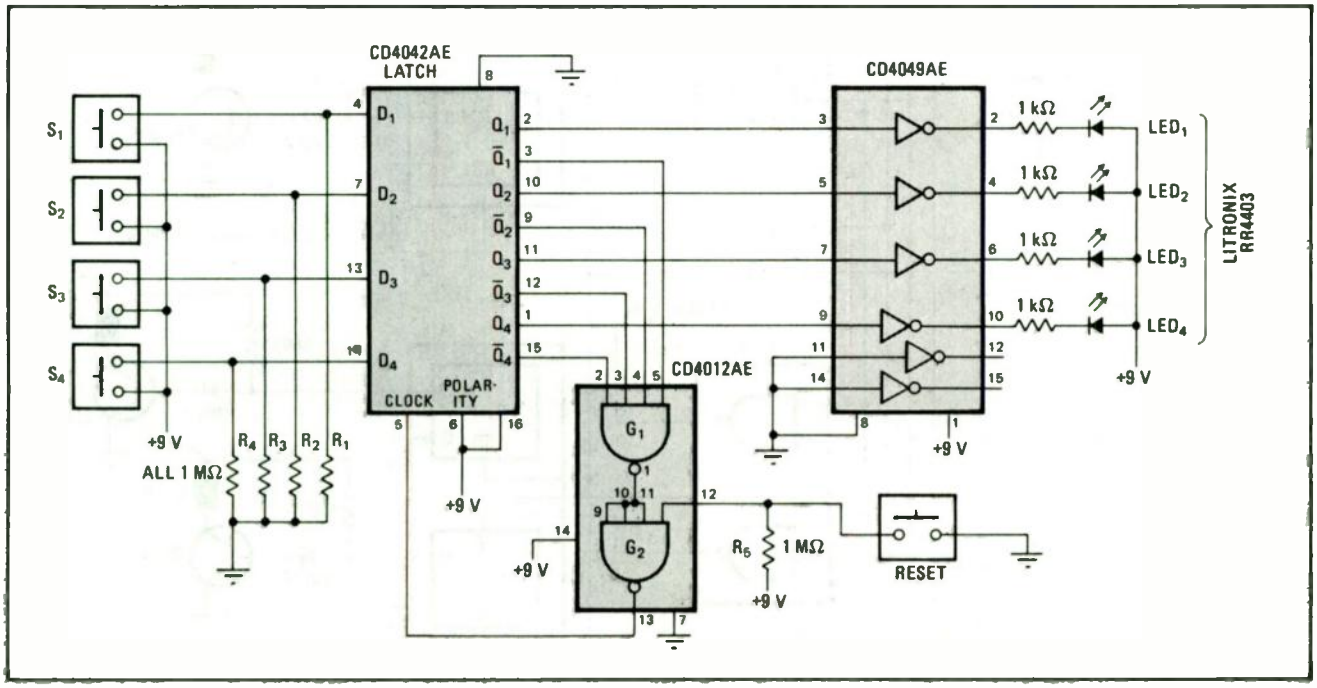
When the push-to-close switches S_1 through S_4 are open, inputs D_1 through D_4 to the 4042 quad latch are low. Therefore outputs Q_1 through Q_4 are low, and $\bar{Q}_1$ through $\bar{Q}_4$ are high. These four high inputs to NAND gate G_1 make G_1 low and G_2 high. The high output from G_2 is applied to the clock input of the latch; with the clock thus enabled, the outputs of the latch can follow the inputs.

If switch S_1 is closed, D_1 goes high and therefore Q_1 goes high, allowing light-emitting diode LED_1 to light. Simultaneously, $\bar{Q}_1$ goes low, sending G_1 high but G_2 and the clock input of the latch low. The clock low locks the latch so that D_2, D_3, and D_4 no longer control Q_2, Q_3, and Q_4. As a result, even if S_2, S_3, or S_4 is closed, the corresponding LED does not light.

The circuit is reset by momentary closing of the reset switch to set G_2 and clock high. If S_1 through S_4 are open, Q_1 through Q_4 go low for the next trial.

Expansion of this circuit to handle N inputs is straightforward. Only two NAND gates are required, but one of them must have N inputs. □

Designer's casebook is a regular feature in Electronics. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



Who's on first? The first switch to close lights up its associated LED, and blocks all other LEDs from lighting if their switches are closed. Circuit can distinguish first-closed switch for time differences as small as 0.05 microsecond. Cost of parts for entire circuit is under $10.

Simple logic arrangement identifies first event

by Stephen Phelps
Santa Fe Community College, Gainesville, Fla.

An inexpensive, straightforward circuit is capable of detecting and indicating which of four switches closes first. This first-response discriminator, which costs less than $5 to build, can be operated from a 6-volt lantern battery. Since it is made up of TTL integrated circuits, it can resolve "ties" with nanosecond accuracy.

The circuit is useful in behavioral-science applications to determine the first response of any one of four subjects, or in scientific studies where it is important to pinpoint what event is occurring first. Another application, one of more popular interest, is eliminating ambiguity in various entertainment games by identifying which player reacts first or quickest.

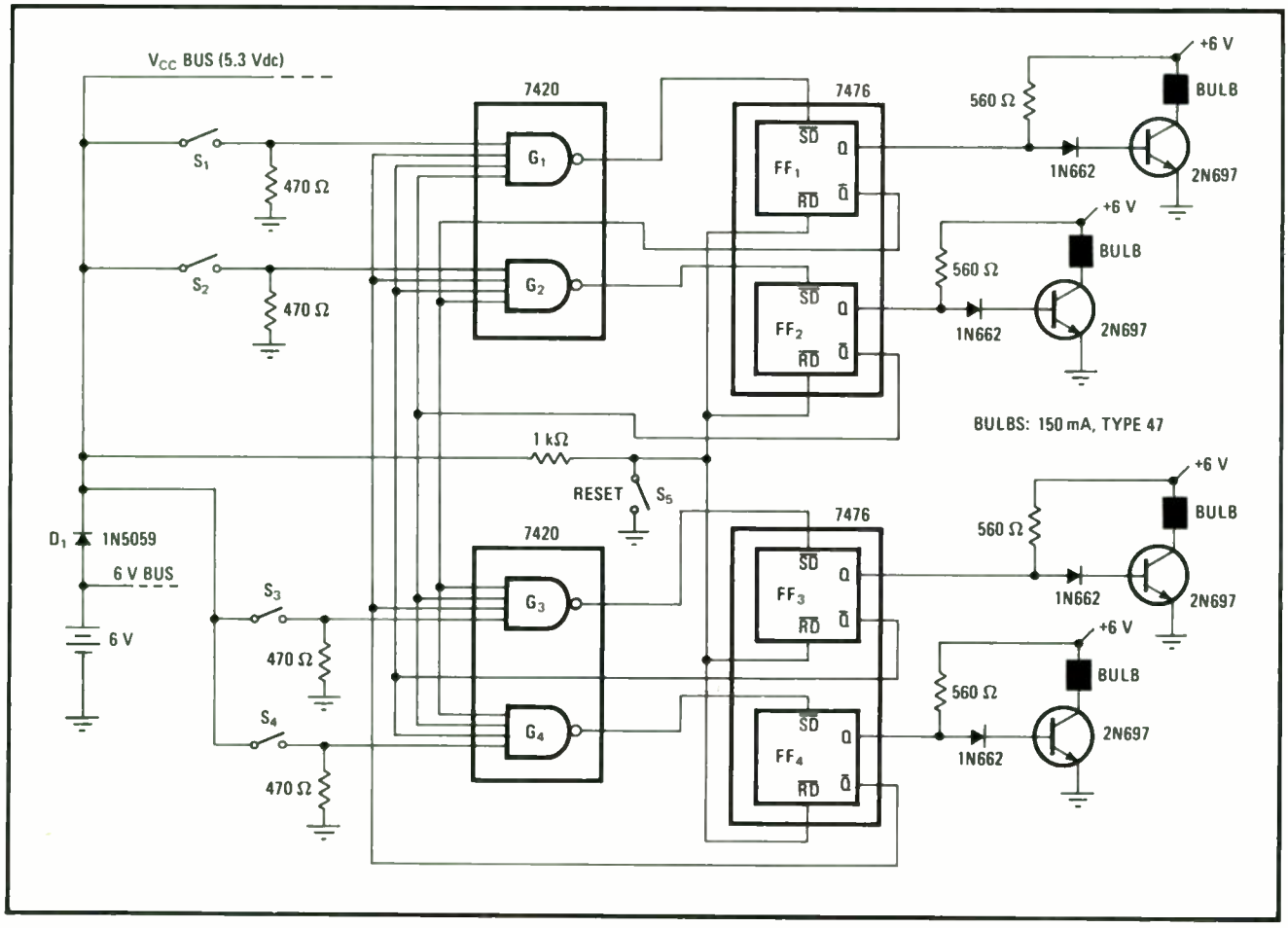
Each of the circuit's four input switches, S_1 through S_4, is initially open, keeping NAND gates G_1 through G_4 inhibited. Flip-flops FF_1 through FF_4 are initially reset by applying a logic 0 to each $\overline{RD}$ input via switch S_5. The Q output of each flip-flop is initially low, grounding the base current of the lamp-driver transistors so that all the lamps are dark. And the high $\overline{Q}$ output of each flip-flop is applied to every NAND gate except the one associated with its own flip-flop.

The first switch to close enables its respective NAND gate, producing a low gate output, whose negative-going edge sets the corresponding flip-flop. The Q output of that flip-flop then goes high so that the associated lamp-driver transistor switches on and lights its lamp. Meanwhile, the $\overline{Q}$ output of the triggered flip-flop goes low, inhibiting the other three NAND gates and preventing the second, third, and fourth switch-closings from propagating to the output.

Diode D_1 is a high-current silicon device that is used primarily to drop the lantern-battery voltage to about 5.3 V to observe the limitation on TTL supply voltage of 5.25 V maximum. This diode also protects the logic in the event of a reversal of power-supply polarity. If a 5-V supply is used, the diode is not needed.

This first-response discriminating scheme may be extended to cover N inputs, as long as N N-input NAND gates are used, and TTL loading rules are observed. □

Finding the first. Battery-operable logic circuit indicates which of its four input switches, S_1 through S_4, closes first. All the flip-flops are initially reset (by switch S_5) with their Q outputs low. The first switch to close enables its associated gate, which then sets the associated flip-flop. This lights the appropriate output lamp and inhibits the other NAND gates so that the other lamps remain dark.



Making music with IC timers

by Kenneth R. Dugan
General Telephone and Electronics, Clearwater, Fla.

The versatile 555-type IC timer has yet another application—as a poor-man's music synthesizer for playing the musical signature of simple songs. Two timers are needed: one generates the rhythm, while the other produces the tones.

The circuit shown is intended for use as an audible alarm for a telephone exchange; it plays the first 10 notes of "A Pretty Girl Is Like a Melody." With the CONTROL INPUT lead of $Timer_1$ returned to the V_{CC} supply line, the tune will recycle continuously. But if a relay or flip-flop is connected to this lead, the number of times that the tune recycles can be controlled.

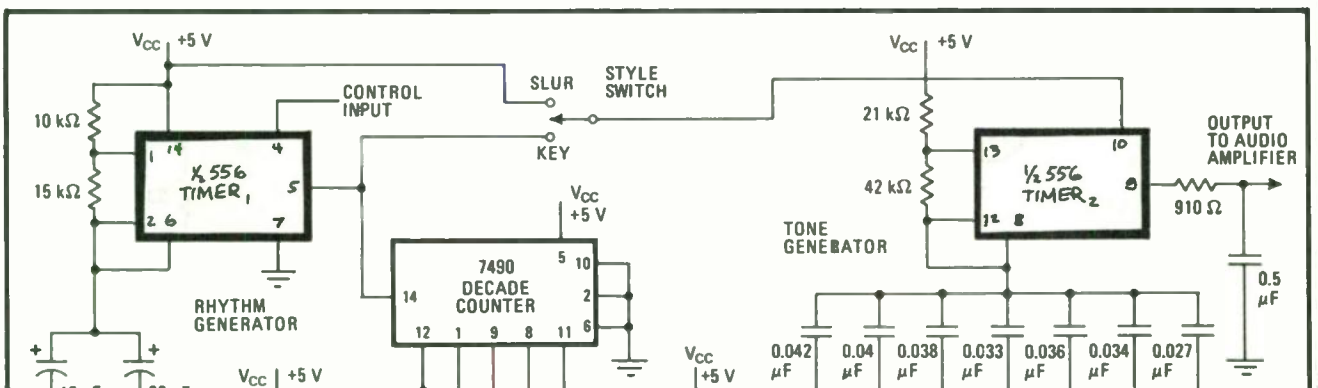
Since the output for $Timer_2$ is a pulse train having a duty cycle between 40% and 60%, a low-pass filter is used to soften the somewhat harsh audio quality of this waveshape. The setting of the STYLE switch causes the notes to either step or glide through the tune.

When used in conjunction with a diode bridge that detects the presence or absence of a ringing generator on the telephone line, the circuit can be programed to play a distinctive musical signature as a personalized telephone bell signal. Of course, many different combinations of resistors and capacitors can be used to obtain the desired music frequencies.

TONE-GENERATOR FREQUENCIES FOR "A PRETTY GIRL IS LIKE A MELODY"

COUNT	TONE CAPACITOR (μF)	FREQUENCY (Hz)
0	0.042	329
1	0.040	349
2	0.038	370
3	0.033	440
4	0.038	370
5	0.036	392
6	0.034	415
7	0.033	440
8	0.027	523
9	0.033	440

One less IC package is needed if a dual 556-type timer is employed, as done here, instead of two individual 555-type timers. □



Tuneful timers. This music synthesizer, which relies on two IC timers, can play a simple 10-note song. $Timer_1$ generates the rhythm for the tune, while $Timer_2$ generates the tones. If the CONTROL INPUT is tied to the supply line, the tune recycles continuously. The position of the STYLE switch determines whether the tones are played individually or blended. This circuit plays "A Pretty Girl Is Like a Melody."

Extending time delay with an emitter-follower

by Victor Hatch
Peripheral Power Systems, San Jose, Calif.

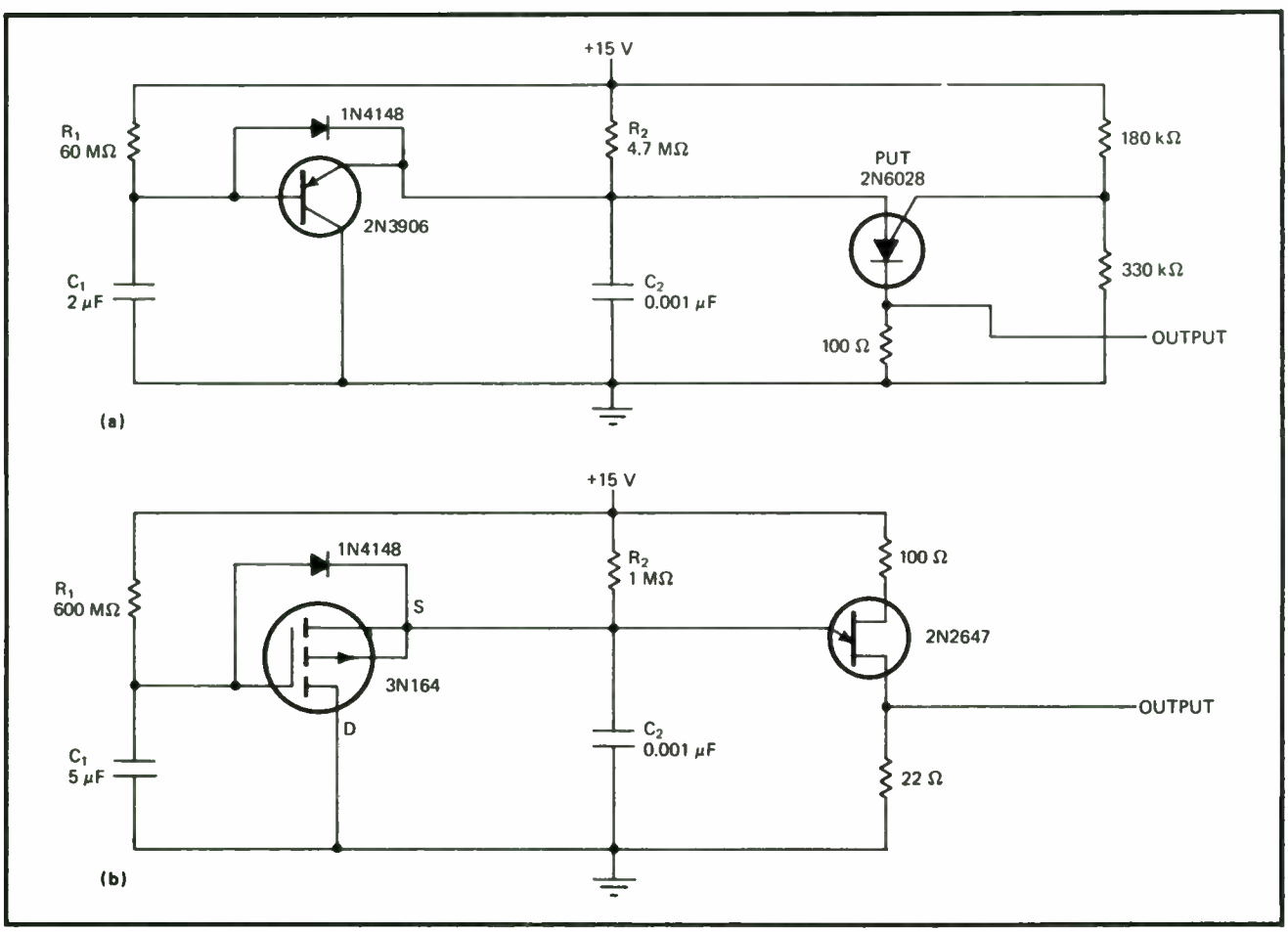
When a long delay is needed between pulses, two unijunction transistors are frequently tied together so that one of them periodically changes the triggering point of the other. A better approach—one that permits very large time constants to be realized—is to use a programmable unijunction transistor (PUT) and an emitter-follower. In this way, the peak point current needed to fire the PUT can be obtained when a high value of resistance is used in the timing network.

The circuit shown in (a) produces an output pulse every 2½ minutes. Resistor R_1 and capacitor C_1 are the timing components that set the circuit's operating frequency. Resistor R_2 assures that circuit oscillation will be sustained by providing a bias current that is greater than the PUT's peak point current (0.15 microampere in this case) for turning the PUT on and less than the PUT's valley current (25 μA in this case) for turning the PUT off. Capacitor C_2 biases the PUT until the diode conducts and capacitor C_1 begins to discharge.

Even longer time delays can be realized by using the circuit shown in (b)—a unijunction transistor (UJT) and a p-channel enhancement-mode MOSFET that is connected as a source-follower. This particular configuration produces one pulse an hour. Timing resistor R_1 can have a higher value here because the gate current of the MOSFET source-follower is lower than the base current of the transistor emitter-follower.

Again, the value of resistor R_2 determines the proper bias currents. It must supply the UJT with a turn-on bias current that is larger than the sum of the device's peak point current and emitter leakage current, and a turn-off bias current that is smaller than the device's valley current, which is usually several milliamperes. □

Stretching the off time. Emitter-follower (a) allows high values of resistance to be used in timing circuit of programable unijunction transistor. The resulting large time constant extends the time between output pulses to 2½ minutes for the components shown. With conventional UJT and a source-follower (b), the delay can be made even longer. Here it's one pulse an hour.



Getting extra control over output periods of IC timer

by Arthur R. Klinger
United States Air Force, Sheppard Air Force Base, Wichita Falls, Texas

The 555-type IC timer, which is a versatile circuit building block, becomes even more useful when its low and high output periods are controlled fully. The two circuits shown here, for example, enable the designer to have full-range, completely independent control over the timer's output periods, or, conversely, to make the periods fully dependent so that the output duty cycle can be varied easily over a wide range while keeping output pulse rate constant.

Circuit (a) is for independent control over the periods. Diodes D_1 and D_2 provide separate paths for the timing capacitor's (C) charging and discharging currents. Potentiometers R_1 and R_2 control the high and low periods independently over the timer's complete normal range. Resistor R_3 is included to provide the same minimum fixed resistance in the discharge loop as resistor R_4 provides in the charging loop.

When $R_1 = R_3$ and $R_2 = R_4$, a single calibrated dial can be shared by potentiometers R_1 and R_2 (through a concentric control). If $R_1 = R_2 = 10$ megohms and $R_3 = R_4 = 1{,}000$ ohms, the ratio of high-to-low or low-to-high periods can approach 10,000:1.

Circuit (b), which is only a slightly modified version of circuit (a), makes the periods dependent. As potentiometer R_1 is varied, one period is decreased while the other is increased proportionately. If $R_1 = 10$ megohms and $R_2 = R_3 = 1{,}000$ ohms, the timer's duty cycle will range from about 0.01% to 99.99%, with little change in the output pulse frequency.

In both circuits, the voltage drop across the diodes decreases the effective voltage across the RC timing network, so that the output periods will be smaller than they usually are. Normally, the timer's high output period can be described by:

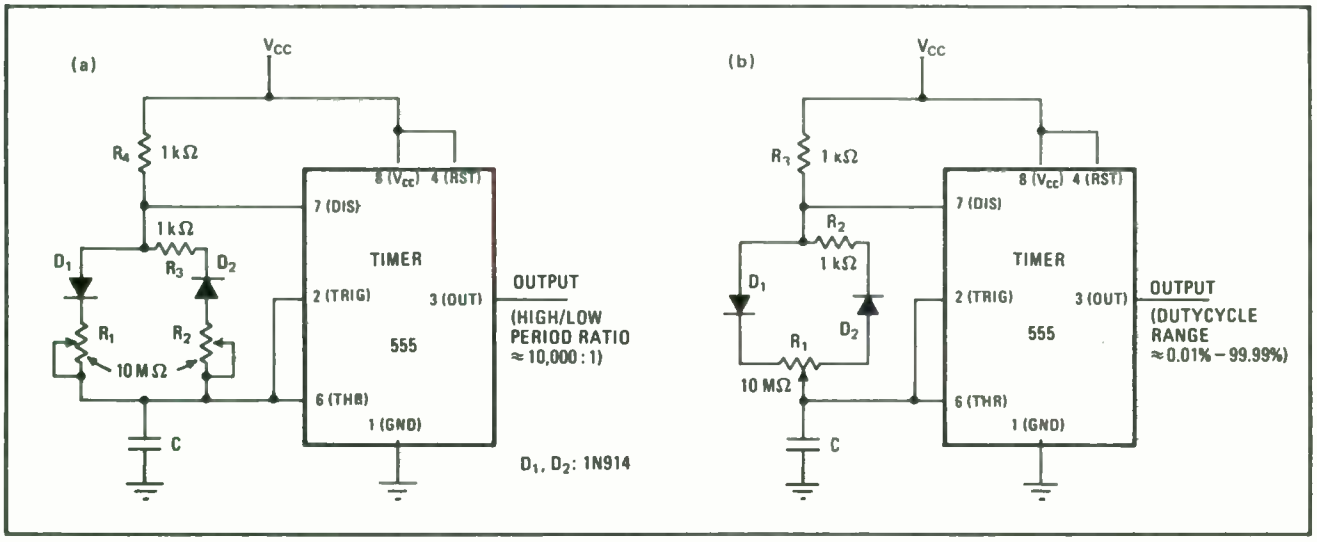
$$T_{HI} = RC\,ln[(V_{CC} - V_1)/(V_{CC} - V_2)]$$

where R is the total resistance in series with timing capacitor C, V_{CC} is the supply voltage, V_1 is the low trigger threshold, and V_2 is the high trigger threshold.

For these circuits, however, the constant voltage drop across the diodes must be accounted for. If each diode drop is approximately 0.6 volt, then:

$$T_{HI} = RC\,ln[((V_{CC} - 0.6) - V_1)/((V_{CC} - 0.6) - V_2)]$$

The lower the supply voltage, then, the greater is the effect of the diode drop. When the timer is operated in its astable mode, the period is roughly 0.76RC for a 15-V supply, and for astable operation with 5-V supply, the period is about 1.4RC. This means that the timer's output periods will be more sensitive to variations in the power-supply voltage, which may be a disadvantage in some applications. □



Simple but effective. When a pair of diodes is used to separate the charging and discharging paths of an IC timer, the high and low output periods of this device can be controlled easily. The periods can be made independent of each other, as in (a), or fully dependent without changing the output pulse frequency, as in (b). The diode drops, however, make the timer more sensitive to supply variations.

Digital clock/calendar offers dual-mode display

by Gregory A. Baxes
BaKad Electronics, Mill Valley, Calif.

Besides indicating whether the time being displayed is a.m. or p.m., an easily assembled digital clock/calendar features a choice of a 12-hour or 24-hour mode. Furthermore, the calendar section has a switch for conveniently setting the number of days in the month. The clock section, of course, also has a switch for selecting either the 12- or 24-hour operating mode.

The entire circuit is built with TTL ICs, and the display is made up of the seven-segment type of readout. MSI devices—presettable decade counters—are used for the units display of both the clock and the calendar. These counters are preset by switch S_1 to reset to 1 in the 12-hour mode and to 0 in the 24-hour mode. Conventional decade counters are used for the tens display for both the clock and the calendar.

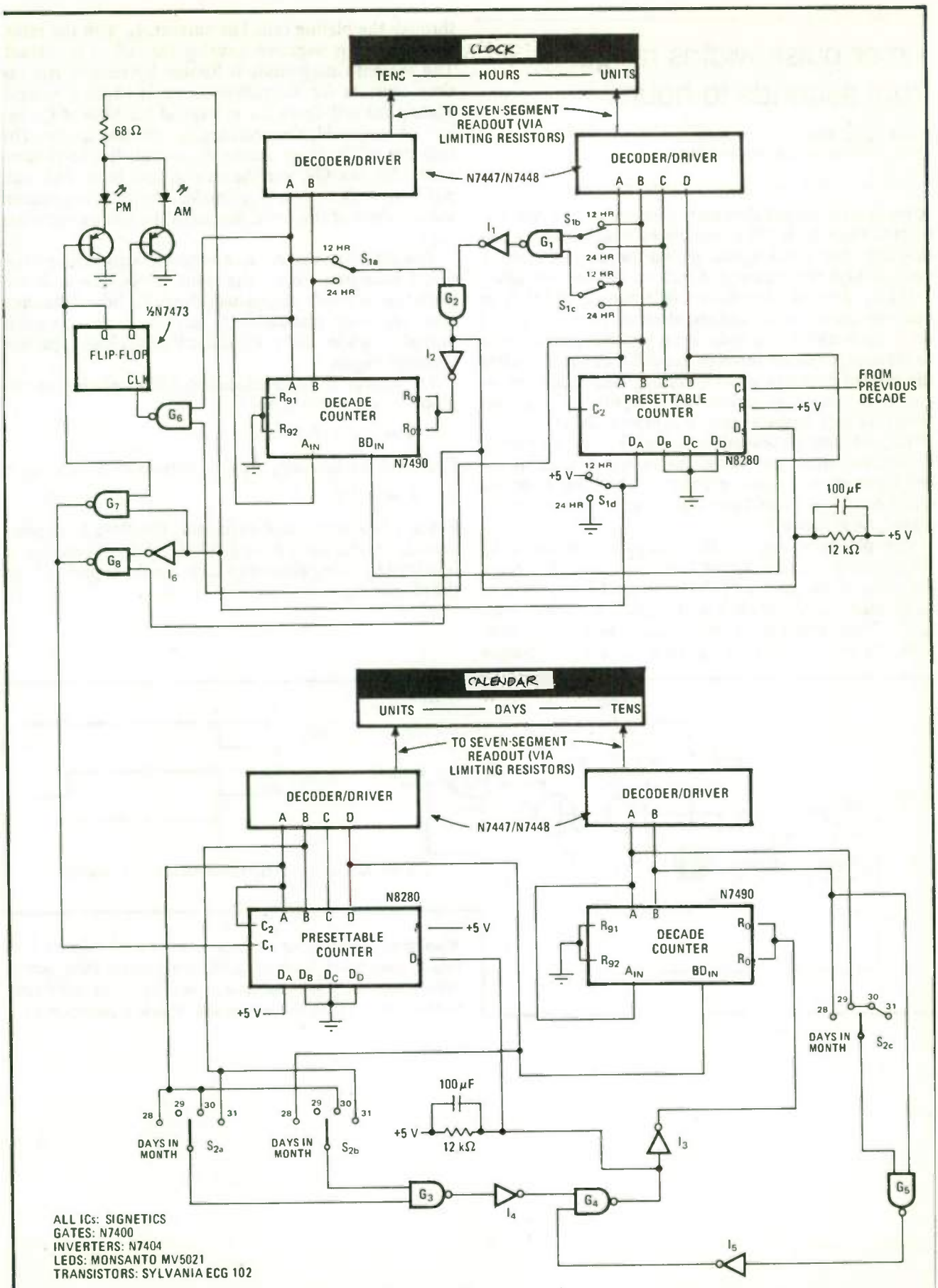
Gates G_1 and G_2 and inverters I_1 and I_2 sense the binary outputs of the clock counters, resetting both the tens and units counters upon a "13 o'clock" pulse or a "24 o'clock" pulse, depending on the operating mode. Likewise, in the calendar section, gates G_3, G_4, and G_5 and inverters I_3, I_4, and I_5 sense the binary outputs of both counters and reset the calendar upon receipt of the "monthly" pulse chosen by the setting of switch S_2.

Gate G_6 senses the "12 o'clock" output from the clock counters, triggering the flip-flop and also advancing the a.m./p.m. indicator. Gates G_7 and G_8 and inverter I_6 determine when a clock pulse reaches the calendar units counter. In the 12-hour mode, the clock pulse will come from the a.m./p.m. indicator; in the 24-hour mode, the pulse is initiated by inverter I_2 since this device resets the clock tens counter at "24 o'clock."

The reset pulse for both the clock and calendar units counters is a logic high applied to the data strobe (D_S) input of these counters. A reset pulse causes them to strobe their data (D_A, D_B, D_C, and D_D) inputs and, in effect, to reset to either 1 or 0, depending on the operating mode.

Transistors Q_1 and Q_2 can be any small-signal pnp transistor that can drive the light-emitting-diode a.m./p.m. indicators. The 68-ohm resistor limits the current to the LED that is currently lit. In the 24-hour mode, the a.m./p.m. indicator is off. □

Convenient timer. Uncomplicated design for digital clock/calendar keeps the user in mind. The clock section can display time as either a 12-hour or a 24-hour period, depending on the setting of switch S_1. In the 12-hour mode, the clock lights an LED lamp to indicate whether the time is a.m. or p.m. The calendar section can be set, with switch S_2, for the number of days in the present month.



ALL ICs: SIGNETICS
GATES: N7400
INVERTERS: N7404
LEDS: MONSANTO MV5021
TRANSISTORS: SYLVANIA ECG 102

Timer pulse widths range from seconds to hours

by Ken Erickson
Interstate Electronics Corp., Anaheim, Calif.

A timer with output durations ranging from a few seconds to more than 100 hours can be built around a plating cell, thus avoiding the special low-leakage components or high resistances that such timers often require.

When the current direction in a plating cell is from reservoir electrode to working electrode, silver is plated onto the working electrode in an amount proportional to the charge passed through the cell. Conversely, when the current direction is from working electrode to reservoir electrode, silver is removed from the working electrode. As long as the electrode is plated, the impedance of the cell is only a few kilohms; but after all the plating is removed from the anode, the impedance across the cell increases to several megohms. When this happens, transistor Q_1 is turned on; otherwise, when the cell is plated, Q_1 is cut off.

The plating charge is the charge on capacitor C. When the input and output have both been low for a long time, C has charged fully to about 3.6 volts, and at 1,000 microfarads as shown, it holds 3.6×10^{-3} coulomb. Then, when the external input to gate G_1 goes high, its output drops to ground, and C discharges through the plating cell. The current, I_d, with the reference shown, is negative, causing the cell to be plated. The current's magnitude is limited by resistor R_1; the time constant for the values shown is about 1 second. Plating the cell drops the voltage at the base of Q_1 below its threshold, thus turning Q_1 off and Q_2 on. The collector of Q_2 drops almost to ground; this level is inverted by gate G_2, and the output goes high. This output feeds back to gate G_1 to make the circuit's operation independent of the input line once the timing cycle has begun.

The deplating current flows continuously through R_2; it is 1 microampere for the value of R_2 shown. When deplating is nearly completed, the cell's impedance begins increasing gradually, Q_1 turns back on, the timer output goes low, and if the timer input is low, capacitor C charges again.

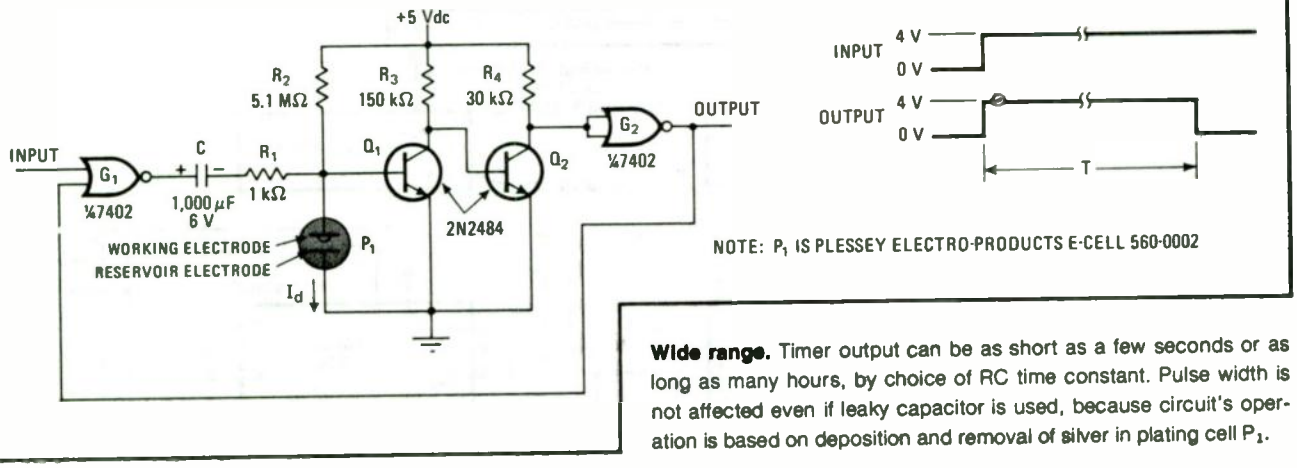
The charge transferred during either plating or deplating is represented by

$$Q = CV = I_d T$$

From this relationship, the time to transfer this charge is

$$T = CV/I_d$$

For a 1,000-microfarad capacitor, the time to deplate the cell is 3,600 seconds—a full hour. Other times can be obtained by using different values for the capacitor C or the resistor R_2. □



Wide range. Timer output can be as short as a few seconds or as long as many hours, by choice of RC time constant. Pulse width is not affected even if leaky capacitor is used, because circuit's operation is based on deposition and removal of silver in plating cell P_1.

49. Triggers

Schmitt trigger prevents clock train overlap

by R.R. Osborn
Roberts Enterprises, Flagstaff, Ariz.

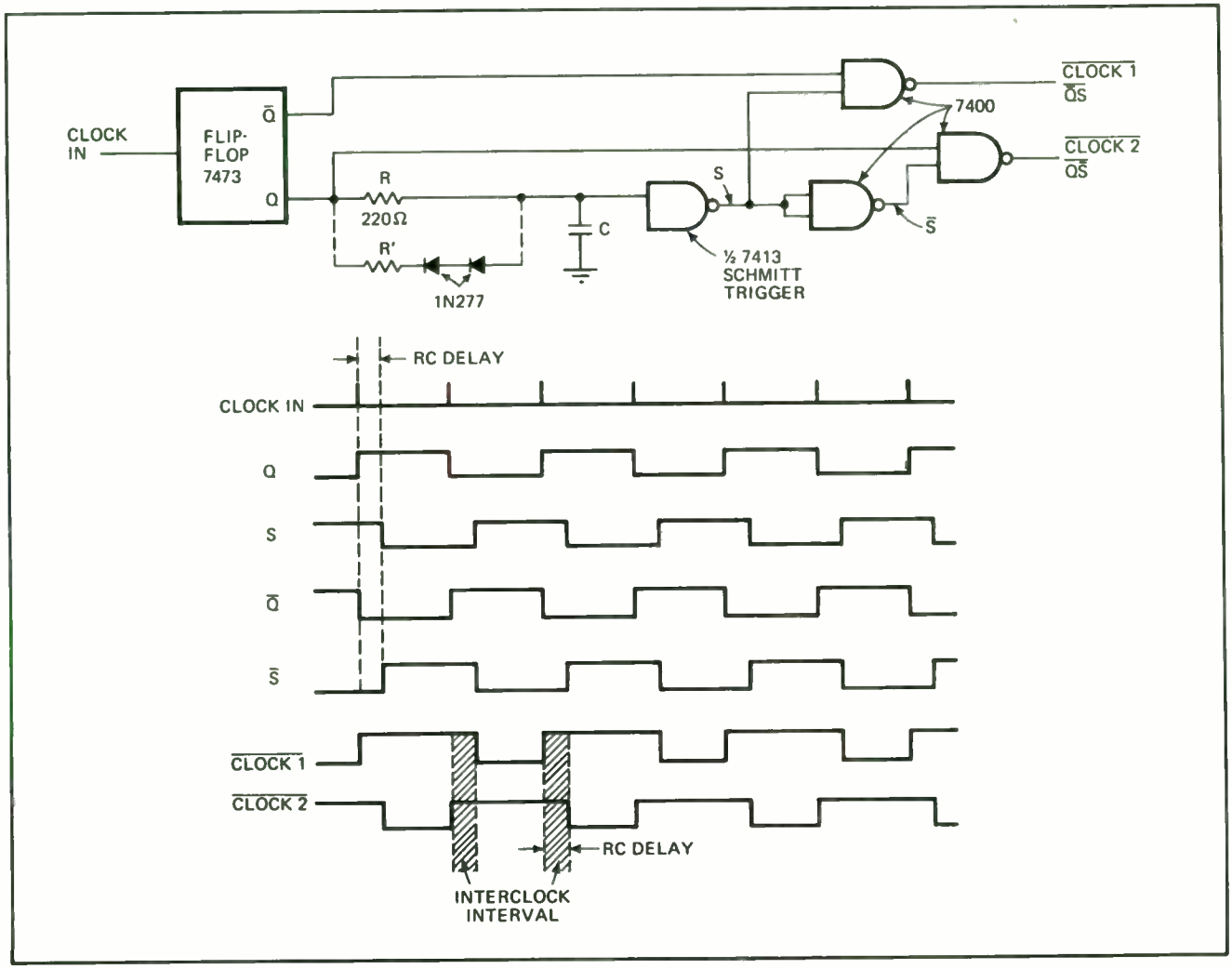
Non-overlapping clock trains are often required in digital systems, especially when transistor-transistor-logic circuits must be interfaced with metal-oxide-semiconductor logic circuits. A single integrated Schmitt trigger, using only one RC time constant, can provide the appropriate delay between clock trains. Moreover, the temperature stability of the IC Schmitt trigger assures that the separation between output clocks remains constant, despite changing temperature.

The Schmitt trigger delays the Q output of the flip-flop for the time fixed by resistor R and capacitor C; it does not delay the flip-flop's $\bar{Q}$ output. The delayed and undelayed pulse trains then pass through a combination of NAND gates, producing the two desired non-overlapping output clocks.

Interclock intervals, which occur when both clock outputs are high, are unequal if resistor R alone sets the delay, because of the flip-flop's output levels and the Schmitt trigger's input current. Adding resistor R′ and two diodes, as shown by the dashed lines, allows the interclock intervals to be made equal to each other. The value of R′ can range from 0 to 5 kilohms.

Capacitor C can vary from 0 to 1,000 microfarads, producing interclock intervals of 30 nanoseconds to 1 second. The time between input clock pulses must always be greater than the output clock interval; input clock frequency can be as high as 10 megahertz. □

Staggering clock phase. Circuit produces two non-overlapping output clock trains from single input clock to flip-flop. Q output of flip-flop is delayed by Schmitt trigger for one RC time constant. Delayed clock from Q and undelayed clock from $\bar{Q}$ are combined by NAND gates to yield separate output clock trains. Adding dashed components yields equal interclock intervals. Clock speed can be as fast as 10 MHz.



Integrated timer operates as variable Schmitt trigger

by Maj. Arthur R. Klinger
United States Air Force, McCoy Air Force Base, Fla.

The bargain-priced 555-type IC timer—already a proven and versatile circuit building block—can also be used as a variable-threshold Schmitt trigger. The triggering circuit has a high input impedance, a latching capability, a threshold voltage that can be adjusted over a wide range, and simultaneous open-collector/totem-pole outputs.

The usual circuit diagrams (a) of the timer can be redrawn with conventional logic symbols to illustrate the operation of the triggering circuit. As shown in (b), the timer can be thought of as a comparator that has a high input impedance and that drives a Schmitt trigger having a high-input-impedance latch and a buffered strobed output.

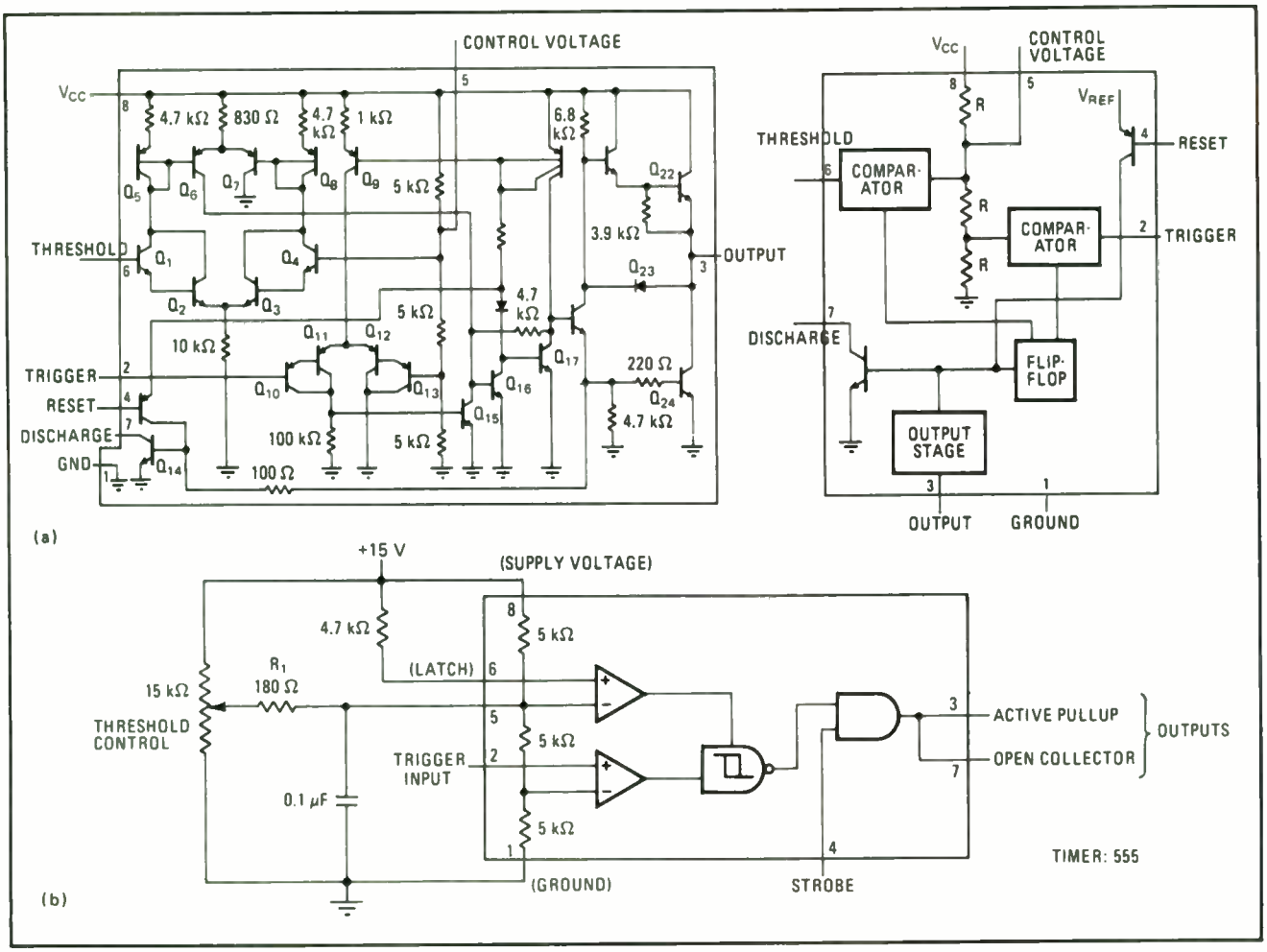
Transistors Q_1 through Q_8 make up one of the noninverting comparators, while transistors Q_9 through Q_{13}, as well as transistor Q_{15}, form the second noninverting comparator. This last comparator drives the Schmitt trigger created by transistors Q_{16} and Q_{17}.

Although it seems that the two comparators are simply ANDed together at the input of the Schmitt, the limited source/sink current capability of the first comparator allows the second comparator to take precedence. The first comparator, then, merely acts as a latch, allowing the other comparator, in combination with the Schmitt, to be triggered when the latching input (pin 6) is high. When this input goes low, the Schmitt and, therefore, the circuit's output are locked in whatever state the Schmitt is in.

A resistor (of 4 kilohms to 100 kilohms) from the latching input to the supply unlatches the Schmitt and, at the same time, tends to decouple this input from high-frequency line noise. Theoretically, in some applications, the timer's control input (pin 5) and latching input could be tied together directly to the supply, but both inputs are very susceptable to noise.

The timer's trigger input (pin 2), which has an input impedance of approximately 1 megohm, drives the Schmitt. The Schmitt's threshold can be varied from about zero to just below the bias voltage existing at the latching input by controlling the voltage at pin 5.

Analog/digital interface. Standard 555-type timer (a) can be regarded as a Schmitt trigger having two high-impedance driving comparators and a buffered strobed output. Triggering circuit of (b) provides a controlled threshold range, which can be varied from almost zero to 8 volts. Upper comparator acts as a latch, while the lower comparator and the Schmitt provide the normal triggering action.



A normal strobe function is provided by the timer's reset input (pin 4); the timer is active when the reset input is high. The latching input, of course, can be pulled low to catch the last device state whenever desired. Active pull-up and open-collector outputs are available simultaneously at pins 3 and 7. Both of these outputs can sink a considerable amount of current.

If intermediate control voltage levels are used at pin 5, the threshold level at pin 6 will still be predictable, and the impedance level for this input will remain high. Supply voltage can range from 4.5 to 16 V, and operating frequency can range from slowly varying dc to at least 2 or 3 megahertz.

As with any high-speed functional IC, certain precautions should be observed for the timer. Since its comparators can respond to pulses as short as 20 nanoseconds, the control and threshold inputs should be bypassed or decoupled from the supply line whenever possible. Also, the source impedances at the two comparator inputs should be kept balanced to minimize the effects of offset currents. Moreover, when the trigger input is overdriven to about -0.2 V or lower, the timer's output returns to its high state, doubling the frequency of recurring input waveforms.

Because of noise and bias levels, problems may arise occasionally when the control input is tied directly to the supply or to less than about 0.5 V. (The latter bias condition corresponds to a 0.25-V input threshold.) Resistor R_1 should be 180 ohms or more to avoid these potential problems. □

50. Voltage references

Stable voltage reference uses single power supply

by Mahendra J. Shah
University of Wisconsin, Madison, Wis.

When an integrated circuit differential operational amplifier is used in a voltage reference source, two supplies usually are needed—both positive and negative. Moreover, additional circuitry is generally required to establish output polarity. But if one supply line is grounded, only one supply becomes necessary—the one that gives the desired output polarity.

So long as the non-inverting input of the operational amplifier is maintained at some positive potential, even a tiny one, the output of the reference source will also be positive. Similarly, small negative potentials at the non-inverting input will result in negative outputs.

The voltage reference source shown employs a single 15-volt supply to give a positive output. To produce a negative output voltage, the positive supply line is grounded, the negative supply line is run to -15 V, and zener polarity must be reversed.

Zener diode D_Z establishes the reference voltage (V_Z) and the reference current (I_Z) for the circuit so that a constant-current source is provided by resistor R_1 and the buffering action of the op amp. Zener current is:

$$I_Z = V_Z R_2 / R_1 R_3$$

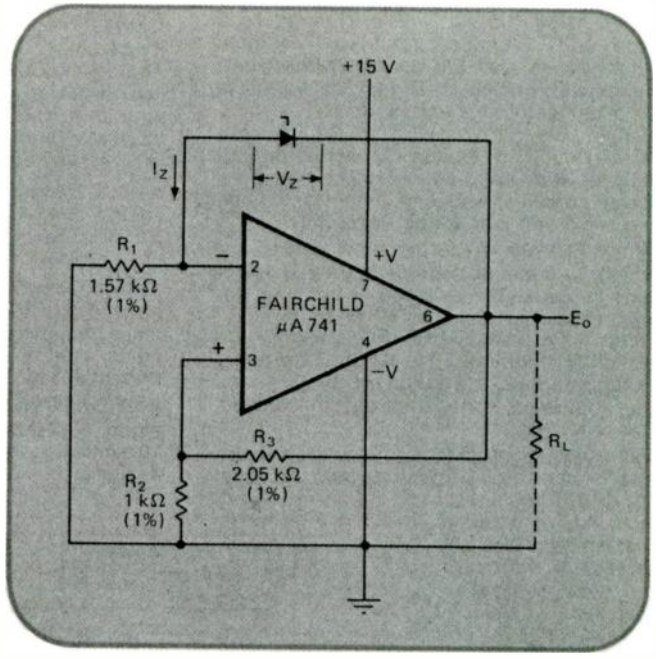
Due to the configuration of the op amp's output stage, circuit output voltage (E_o) will always be greater than 0.5 V when a positive 15-V supply is applied and the negative supply line is grounded. Therefore, a few tens of millivolts will always appear at the op amp's non-inverting input, making the output positive:

$$E_o = V_Z(1 + R_2/R_3)$$

With the positive supply line grounded and -15 V at the negative supply input, E_o will always be less than -0.5 V. The negative voltage at the op amp's noninverting input causes a negative output:

$$E_o = -V_Z(1 + R_2/R_3)$$

The reference zener voltage of 6.4 V yields a zener current of about 2 milliamperes. For a positive supply, output voltage is 9.547 V; temperature coefficient, 1.9 parts per million/°C; voltage stability, 9.5 ppm/V; and output impedance, 53 milliohms. For a negative supply, temperature coefficient remains the same; but output voltage becomes -9.560 V; voltage stability, 2.6 ppm/V; and output impedance, 21 milliohms.



Eliminating dual supplies. Voltage reference source has either positive or negative output, depending on polarity of supply used to bias op amp. Positive supply results in positive voltage at op amp's non-inverting input and, therefore, positive output. Negative supply produces negative output. In either case, final output voltage is about 10 volts. Zener diode acts as reference.

Single-supply reference source uses self-regulated zener

by William Goldfarb
Cornell University, Ithaca, N. Y.

Temperature-compensated zener diodes provide a reference voltage that remains stable despite changes in time and temperature. But they exhibit a rather large dynamic impedance, from 100 to 400 ohms, and current supplied to them must be regulated precisely.

By using voltage comparison, one of these reference zeners can be made to control its own current, eliminating the need for a separately regulated temperature-compensated current source. A precision voltage reference source can then be realized with only a single unregulated power supply. And the cost of the circuit will be dominated by the cost of the zener, keeping parts cost to somewhere around $6.

The voltage reference source in the diagram provides a nominal output voltage of 10 volts that is stable to within ±7 millivolts. It can operate over a supply voltage range of 12 to 18 v. With the output voltage at V_{REF}, the current through the zener is:

$$I_Z = V_{REF} - V_Z/R_1$$

The current-booster transistor actively keeps the voltage at the inverting input of the operational amplifier at:

$$V_I = V_{REF}R_2/(R_2+R_3) = I_ZR_1$$

Zener current I_Z can then be expressed as:

$$I_Z = V_{REF}R_2/R_1(R_2+R_3)$$

And reference voltage V_{REF} is held to:

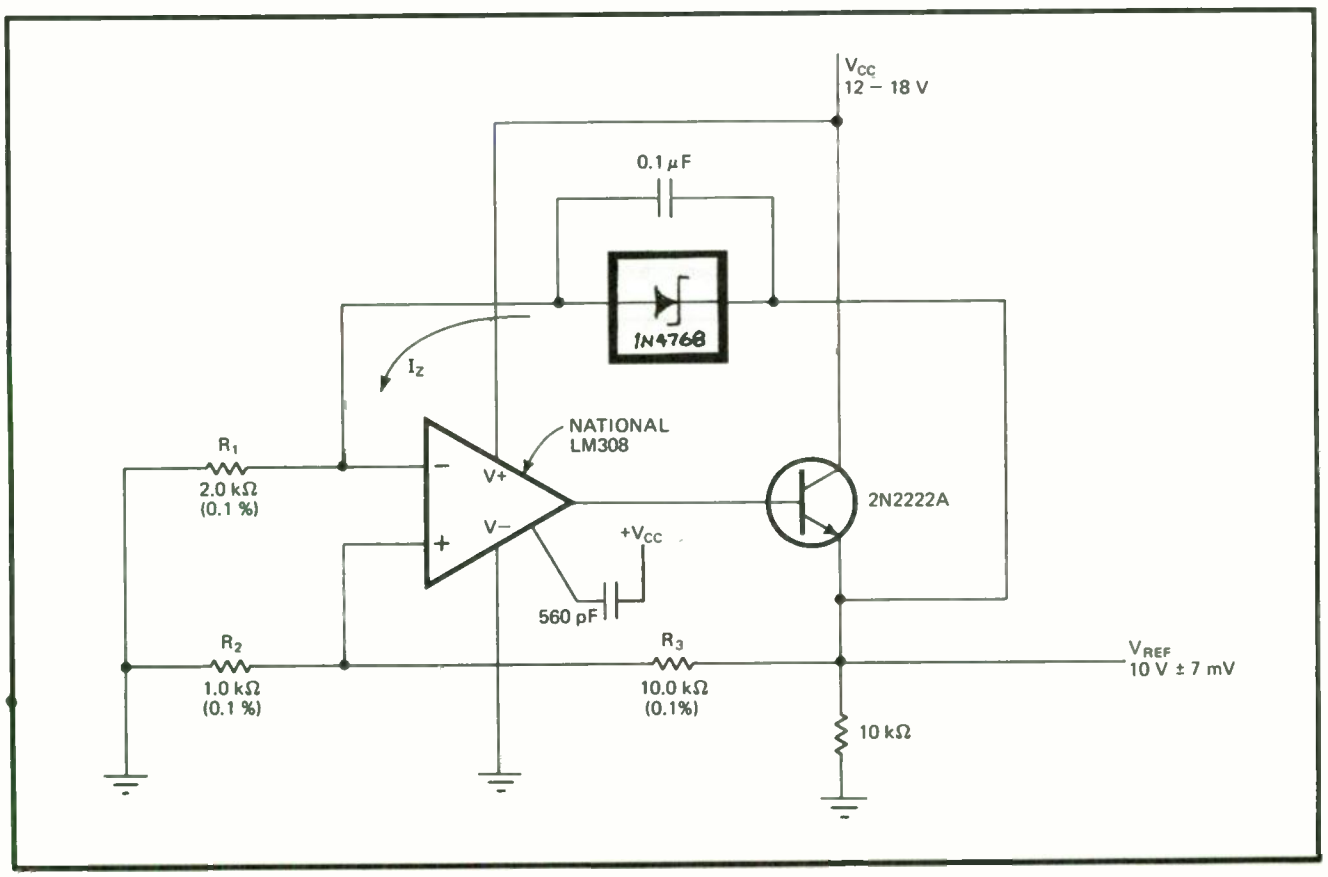
$$V_{REF} = V_Z(R_2+R_3)/R_3$$

A pitfall in any dc bootstrap scheme like this is the possible existence of stable states other than the desired one. For this circuit, such a state exists when the output voltage is zero. Connecting a capacitor between the power supply and the op amp's compensation input prevents the circuit from being locked into the zero-output-voltage state when it is first turned on. The capacitor causes the turn-on transient to put the circuit into the desired condition, with the output voltage at V_{REF}.

For the components shown, the output is stable to within ±7 mV over a temperature range of 0°C to 75°C, even with a supply variation of ±10%. The output current is 30 milliamperes maximum. The capacitor across the zener serves to attenuate noise that may be generated by the zener at high operating frequencies.

A negative output voltage can be obtained by reversing the diode, using a pnp instead of an npn transistor, and grounding the op amp's positive supply input. □

Making do with one supply. Voltage reference source, which operates from a single power supply, maintains its output at 10 volts ±7 millivolts over a 75°C temperature range and with ±10% supply variations. Through voltage comparison, the zener reference regulates its own current, thereby eliminating the usual zener constant-current source. The circuit's maximum output current is 30 milliamperes.



Variable voltage source has independently adjustable TC

by Nathan O. Sokal
Design Automation Inc., Lexington, Mass.

A reference voltage source, which is built around a suitably stable general-purpose operational amplifier, offers an adjustable output-voltage magnitude, as well as an adjustable output-voltage temperature coefficient. Both the voltage magnitude and the temperature coefficient may be varied independently of each other.

The output voltage can be positive or negative, and it is continuously variable from 0.7 to 13 v. The temperature coefficient is also continuously variable, from −0.3%/°C to +0.3%/°C. For the circuit shown in the figure, the output voltage is positive. To obtain a negative voltage, the polarities of all the diodes and the supply (except to the op amp) are simply reversed.

The temperature coefficients of the zener-diode voltage, the resistance values, the op-amp input offset voltage, the op-amp input bias and offset currents, and the power-supply voltage need not all be zero. Rather, their values as functions of temperature must be stable with time and retrace well with temperature cycling. This is also true of the V-I characteristics of diodes D_1 and D_2. Moreover, these two diodes do not have to be matched.

If a narrower range of output voltage is adequate, part of resistance R_1 should be a stable fixed resistor. Likewise, if a narrower temperature-coefficient range is satisfactory, part of resistance R_2 should be a stable fixed resistor. Resistances R_1, R_2, and R_3 should be multi-turn potentiometers if both wide-range adjustment and high resolution are desired. Or they should be combinations of potentiometers and fixed resistors if a narrow adjustment range will do. Or they should be only fixed resistors when the desired output voltage and temperature coefficient need not be adjusted.

The fixed resistors used in this circuit should be film or wire-wound types for good long-term stability. A reference-type zener diode, such as the 1N4894, will improve voltage stability still further. All the resistors and semiconductor devices should be thermally coupled to each other for a good transient response to changes in ambient temperature.

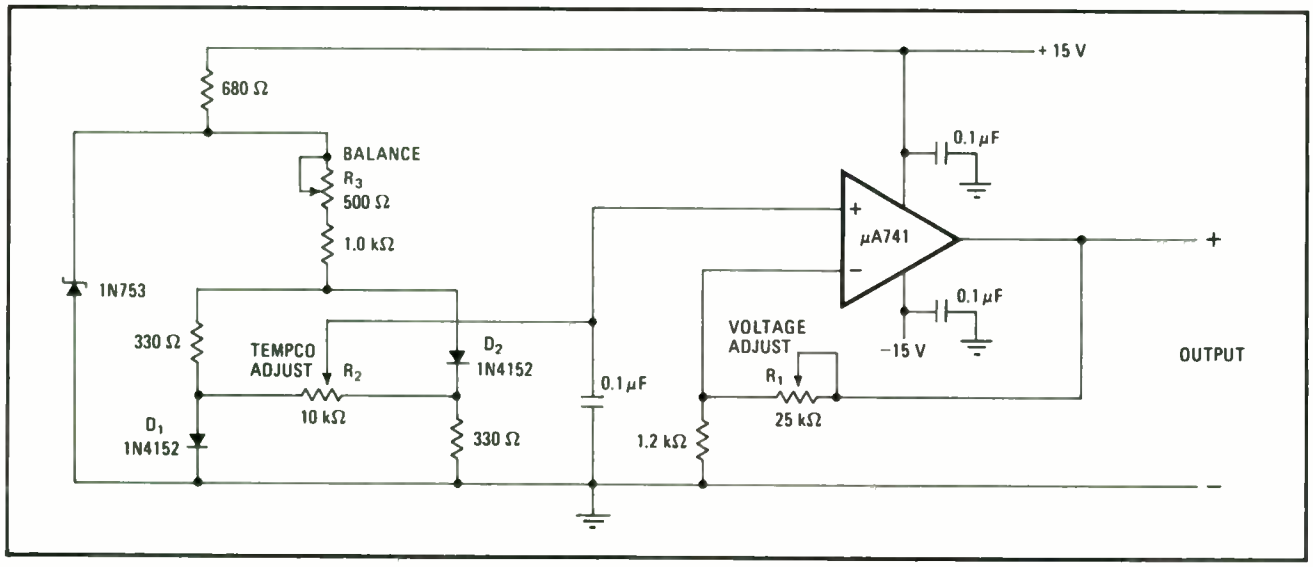
A simple procedure can be followed to adjust the circuit to desired operating conditions. First, set potentiometers R_1 and R_2 approximately at their mid-range positions. Then adjust potentiometer R_3 until the voltage across R_2 is zero at the reference temperature. This is the temperature at which it must be possible to adjust the temperature coefficient without changing the output voltage. Next, position potentiometer R_1 to give the desired output voltage at the reference temperature.

The last step is to adjust potentiometer R_2 for the desired temperature coefficient. This adjustment, which should not affect the output voltage at the reference temperature, can be made by heating or cooling the entire circuit to some temperature other than the reference temperature and then adjusting R_2 to obtain the desired output voltage at that temperature.

As a precaution, the circuit's output voltage should be checked for changing temperature. If it is not within the desired tolerance, repeat all the adjustment steps but the first one. Usually no such repetition will be needed.

More output current can be obtained from this reference voltage source by adding an npn power transistor, wired as an emitter-follower, at the circuit's output. The output from the op amp goes to this transistor's base, and resistor R_1 is then connected to the transistor's emitter, which becomes the circuit output. If the output voltage is negative, a pnp emitter-follower should be used. Without an emitter-follower, the output current can be as large as 10 milliamperes for most general-purpose op amps. □

Stable voltage source. The output voltage of this reference voltage source can be adjusted from 0.7 to 13 volts. And the circuit's output-voltage temperature coefficient is also adjustable, from −0.3%/°C to +0.3%/°C. These two adjustments are independent of each other. Potentiometer R_1 sets the output voltage, potentiometer R_2, the temperature coefficient, and potentiometer R_3, the reference temperature.



51. Voltage regulators

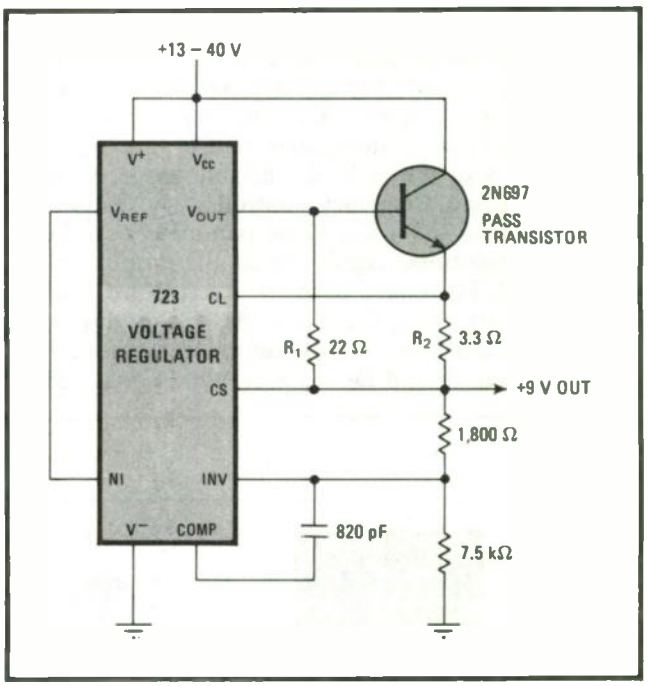
Extra resistor helps regulator share load with transistor

by Dale Hileman
Sphygmetrics Inc
Woodland Hills, Calif.

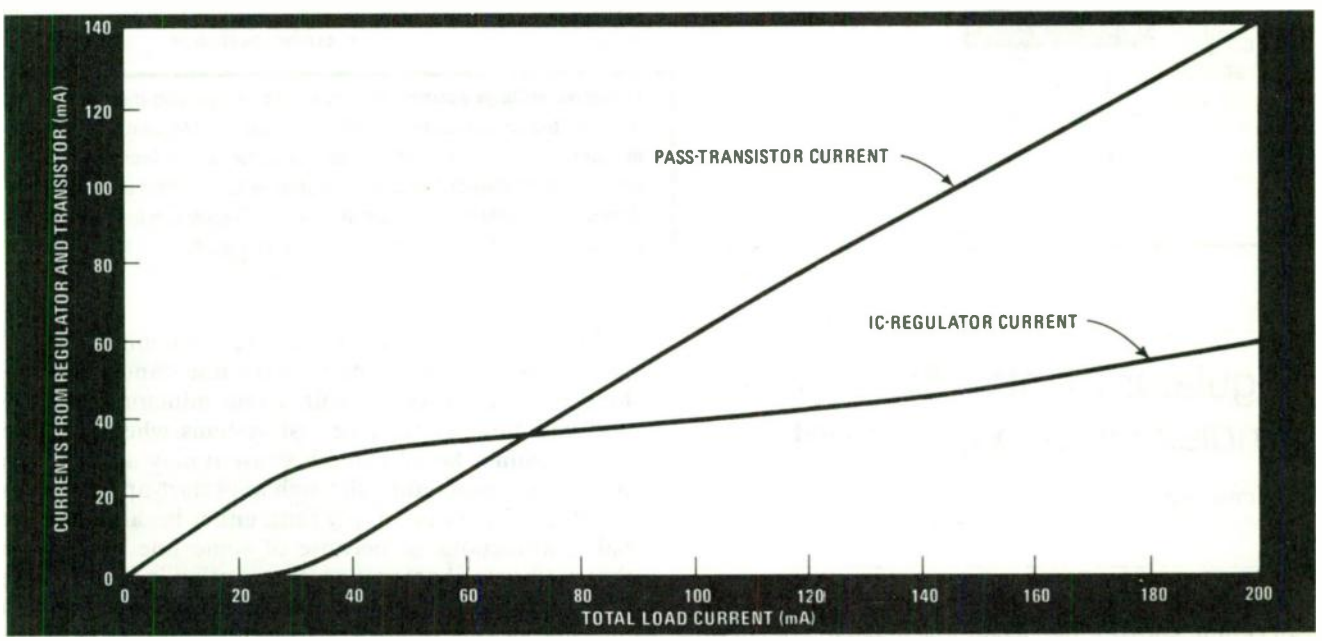
A pass transistor is used with an IC voltage-regulator circuit when the load current required is greater than the integrated circuit can handle. But the capability of the IC is then wasted because it has to furnish only a small base current to the transistor. The addition of a single resistor allows the IC to share the load with the pass transistor. By increasing the total output-current capability of the circuit, this simple change makes it possible to use a smaller transistor for a specified load.

In the schematic diagram shown as Fig. 1, resistor R_1 is added to a typical type-723 IC regulator circuit between the output terminal of the IC and the load. The extent to which the IC then shares the load current with the pass transistor is a function of the current level.

At low current levels, the IC carries the entire load, as shown by the graph in Fig. 2. However, the transistor begins to share the load when the current is high enough for the voltage across R_1 to exceed the base-to-emitter junction voltage, which is about 0.6 V for a silicon transistor. □



1. Add an R. . . . Resistor R_1 is added to voltage-regulator circuit so that the IC can deliver some of the load current in addition to driving the base of the external pass transistor.



2. . . . to share the load. Small load currents are drawn entirely from the integrated circuit. The pass transistor takes on an increasing base-to-emitter junction voltage. This arrangement permits a given circuit to deliver more current or use of a smaller pass transistor for a given load requirement. The total load current is the sum of the currents through resistors R_1 and R_2.

555 as switching regulator supplies negative voltage

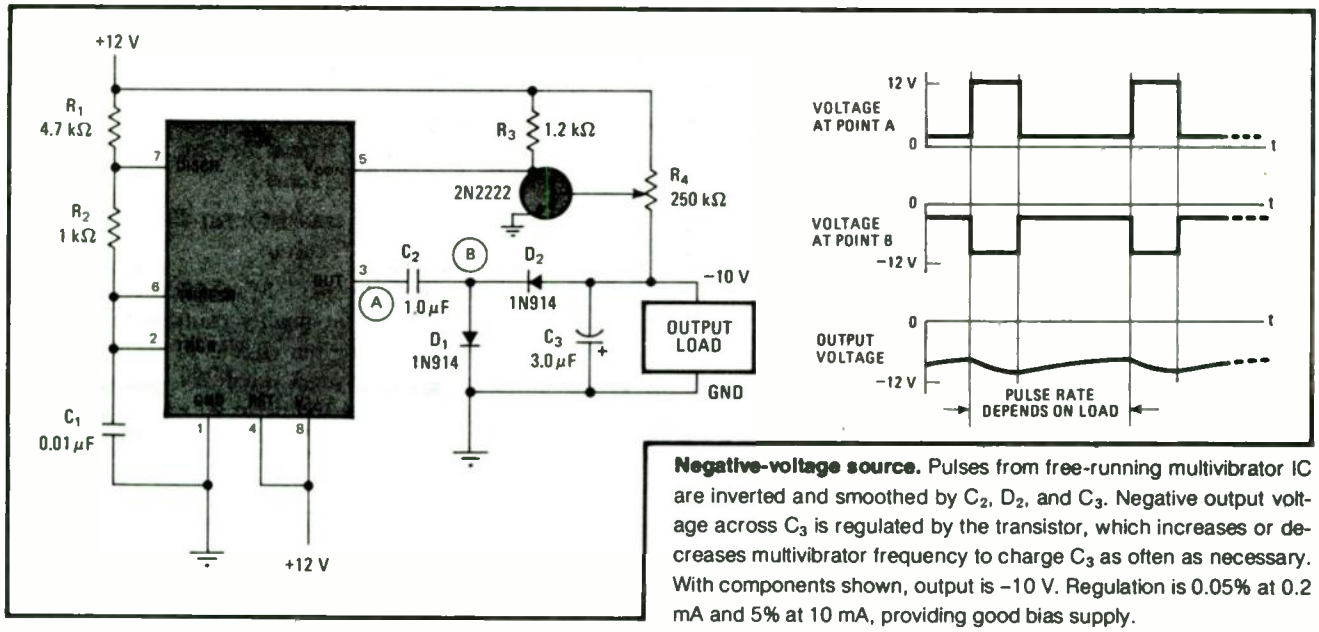
by S.L. Black
Western Electric Co., Columbus, Ohio

Latest addition to the 555 IC timer's seemingly endless bag of tricks is its use to generate a negative dc biasing voltage from a positive source. A current of well over 10 milliamperes can be delivered, and a form of switching regulation is employed to assure a constant output voltage. All of this is done with little more than an npn transistor and the 555 integrated circuit.

The 555 is operated in the astable mode, with the pulse width and frequency controlled by resistors R_1 and R_2 plus capacitor C_1. These parameters can be selected for maximum regulation at the output voltage level desired. Terminal 3 of the IC is connected to a network consisting of C_2, C_3, and diodes D_1 and D_2. Series capacitor C_2 causes the pulse train to lose its ground reference, so that D_1 and D_2 can rectify the signal and capacitor C_3 can filter it into a negative dc output voltage. The magnitude of this output voltage depends on the amplitude and repetition rate of the pulses coming from the IC.

To regulate the output voltage, the 2N2222 transistor varies the control voltage of the 555, increasing or decreasing the pulse repetition rate. Resistor R_3 acts as a collector load for the transistor; the base is driven from potentiometer R_4, which compares the output voltage to the supply voltage. If the output voltage becomes less negative, the control voltage goes closer to ground, causing the repetition rate of the 555 to increase so that C_3 recharges more frequently. If the output voltage becomes more negative, the control voltage goes closer to the positive supply voltage, so the repetition rate decreases, and C_3 is recharged less often.

The output voltage can be set to any level from 0 to −10 volts by means of potentiometer R_4. With the components shown in the figure, this circuit supplies −10 V from a 12-V source. Regulation is less than 5% at a current of 10 mA and less than 0.05% at 0.2 mA. □



Negative-voltage source. Pulses from free-running multivibrator IC are inverted and smoothed by C_2, D_2, and C_3. Negative output voltage across C_3 is regulated by the transistor, which increases or decreases multivibrator frequency to charge C_3 as often as necessary. With components shown, output is −10 V. Regulation is 0.05% at 0.2 mA and 5% at 10 mA, providing good bias supply.

Regulator for standby supply handles large load currents

by James Allen
Honeywell Inc., Aerospace Division, St. Petersburg, Fla.

A simple voltage regulator for a standby-power source can supply amperes of current at whatever voltage is required. Additionally, the circuit, which includes current-limiting and short-circuit protection (current foldback), can produce large current pulses.

There are many systems that require noninterruptible power sources—for example: gyro test stands involving long test sequences, volatile semiconductor memories, and computer systems or test systems where a power failure cannot be tolerated because it may destroy components or mean going through long start-up sequences.

If the primary dc supply fails, either because of internal malfunctions or because of some line disturbance that momentarily causes an interruption in its ac source, the standby power supply cuts in and continues to supply the necessary load current. Usually, the power source for this standby or backup supply is a bank of storage batteries. However, the voltage level provided by these storage batteries is not normally the voltage

level needed by the backup supply for the system.

The regulator in the figure offers ample voltage and current capability. And it can be conveniently and easily tailored to suit a specific application. (The figure also contains plots of the regulator's dc-output characteristic and pulse-current performance.)

The zener voltage of the zener diode determines the output voltage at which the regulator begins to conduct. Current limiting is provided by the combination of control transistor Q_1 and field-effect transistor Q_2, which acts as a voltage-variable resistor. The current-limit level is set by the ratio of resistor R_1 to resistor R_2:

$$I_{max} = 3.1[1 + (R_1/R_2] \text{ amperes}$$

The current foldback of the regulator is obtained through transistor Q_3 and resistor R_3. The voltage level (V_f) at which foldback begins is determined by the ratio of resistor R_4 to resistor R_5:

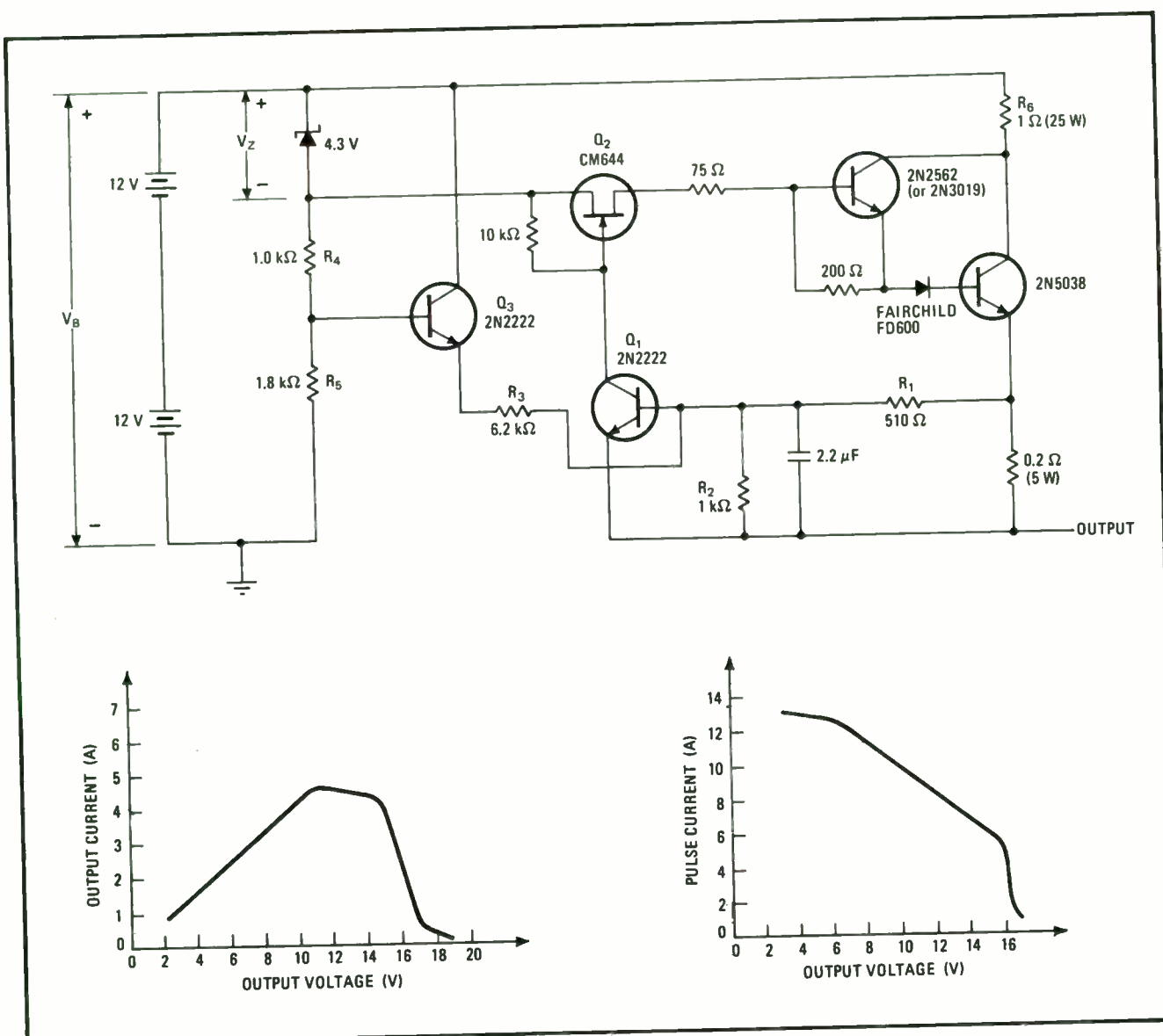
$$V_f = [R_5/(R_4 + R_5)](V_B - V_Z - 2V_{BE3} \text{ volts}$$

where V_B is battery voltage, V_Z is zener voltage, and V_{BE3} is base-emitter voltage of Q_3. The slope of the current foldback curve is set by the ratio of R_1 and R_3.

$$\Delta V/\Delta I = 0.2R_3/R_1 \text{ V/A}$$

Since the regulator will normally be operating into a large-capacity load that will probably exhibit large dv/dt variations initially, it should be able to supply a significantly larger amount of charge during turn-on. This pulse current capability is provided by the capacitor, which delays the feedback current so that transistor Q_1 does not conduct for several hundred microseconds. The magnitude of this pulse current is determined by the value of resistor R_6. □

Watchdog backup power source. Readily adaptable regulated standby-power supply can produce several amperes of current at the desired voltage level, as shown by its output characteristic. The circuit's pulse-current capability (also plotted) is ample and able to satisfy large initial turn-on load current demands. Both current limiting and current foldback are included to protect the regulator circuit.



Temperature limiting boosts regulator output current

by Mahendra J. Shah
University of Wisconsin, Space Science & Engineering Center, Madison, Wis.

The efficiency of a precision monolithic voltage regulator can be significantly improved by limiting the junction temperature of the regulator's internal current-limiting transistor.

Conventional current limiting severely restricts the regulator's peak and average output current capability. As an example, consider the 723-type regulator, which can supply an output voltage of 7 to 37 volts. This device has a maximum storage (junction) temperature of 150°, a maximum imput/output voltage differential of 40 v, and a maximum load current of 150 milliamperes.

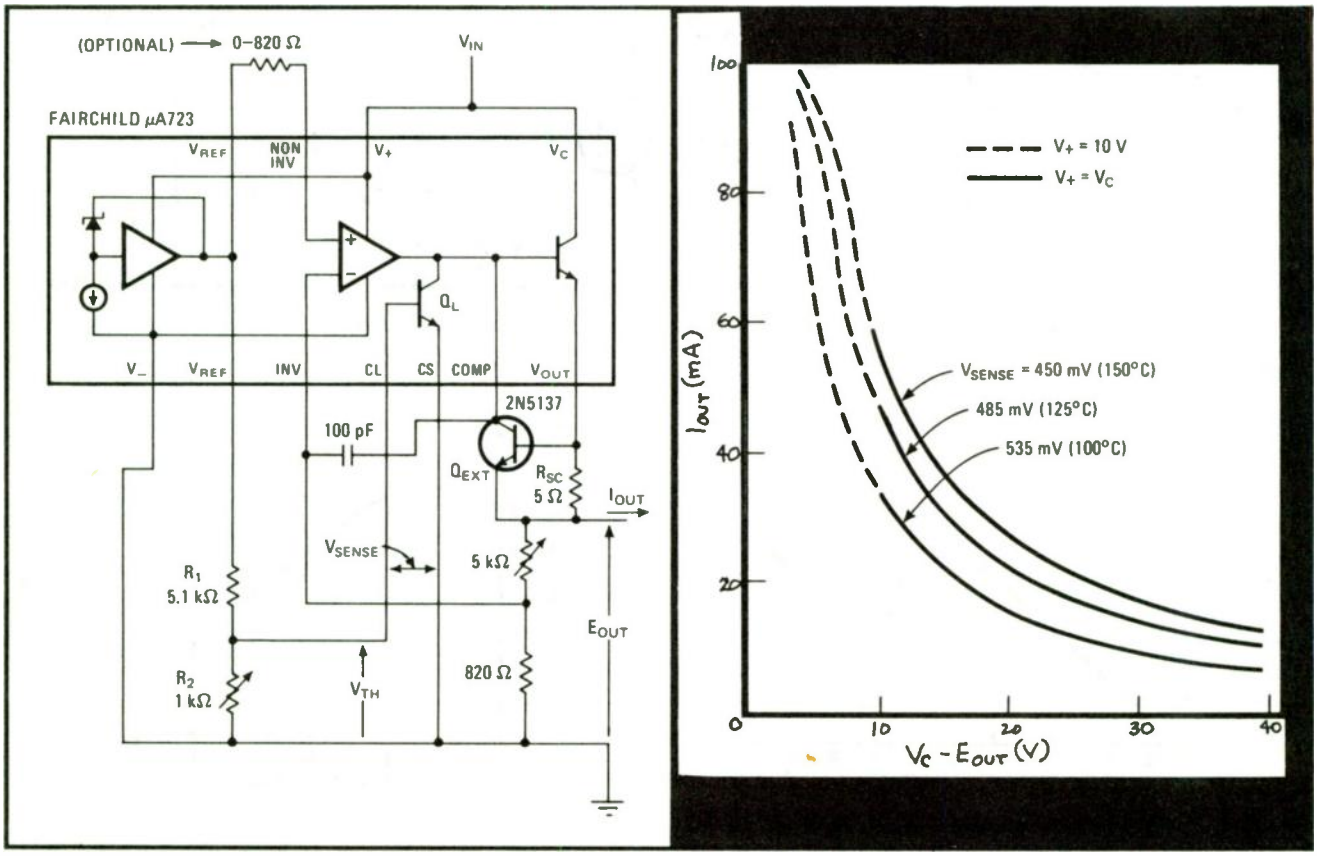
When the regulator's metal-can package is used without a heat sink, its internal power dissipation should be limited to 800 milliwatts at an ambient temperature of 25°C. If the input voltage to the regulator is 40 v, conventional current limiting places the worst-case current limit at 20 mA, or 800 mW/40 v. (The worst-case condition is an output short circuit to ground.) And a foldback-current-limiting approach requires a limit knee setting of 24.2 mA, or 800 mW/(40 – 7) v.

Both of these approaches significantly limit the regulator's output current capability when the regulator must supply a load continously at both intermediate and high output voltage levels, or when it must supply peak currents at any output voltage level. In contrast, temperature limiting protects the regulator from burnout, while allowing it to provide the maximum possible output current (both continuous and pulsed), regardless of output voltage level, ambient temperature, and the amount of heat sinking.

Conveniently, the regulator's own current-limiting transistor, Q_L, can be used to implement this temperature limiting. The transistor's base-emitter junction, which has a temperature sensitivity of –1.8 millivolts/°C, can act as a temperature sensor for the regulator. And the collector terminal of transistor Q_L can be connected to limit the regulator's output current.

A stable voltage source is needed to bias Q_L's base-emitter junction at the threshold voltage (V_{th}) that cor-

Better short-circuit protection. Current-limiting transistor Q_L of monolithic voltage regulator acts as an on-chip thermostat, controlling its own base-emitter junction temperature and, therefore, limiting regulator output current. The threshold bias voltage (V_{th}) of Q_L's base-emitter junction is set to limit this junction's temperature to a value determined by Q_L's sense voltage (V_{sense}).



responds to Q_L's sense voltage (V_{sense}) for a given junction temperature. V_{sense} is the voltage required across Q_L's base-emitter junction to implement output current limiting. Values for sense voltage, limit current, and junction temperature can be obtained from the datasheet plot of the regulator's current-limiting characteristics as a function of junction temperature.

The threshold bias voltage is easily obtained from the regulator's internal voltage reference source and the voltage divider formed by resistors R_1 and R_2. Some other regulators, like Motorola's MC1460, MC1560, MC1461, MC1561, MC1463, MC1563, MC1469, and MC1569, have a provision for junction-temperature limiting, but they require an external regulated voltage source.

When the actual junction temperature of transistor Q_L is lower than the junction-temperature limit, Q_L's base-emitter voltage is higher than the threshold bias voltage, so that Q_L is off. But when Q_L's actual junction temperature rises to the junction-temperature limit, Q_L's base-emitter voltage drops slightly below the threshold bias voltage, and Q_L turns on, limiting its maximum junction temperature by first limiting the regulator's output current.

The external current-limiting transistor, Q_{XT} and its associated resistor, R_{SC}, are needed to limit regulator output current below the 150-mA secondary breakdown limit of the regulator's internal output transistors. (The optional resistor can be included to minimize output voltage drift.) The graph shows the regulator's output current capability over the full range of input/output differential voltage for three sense-voltage settings. □

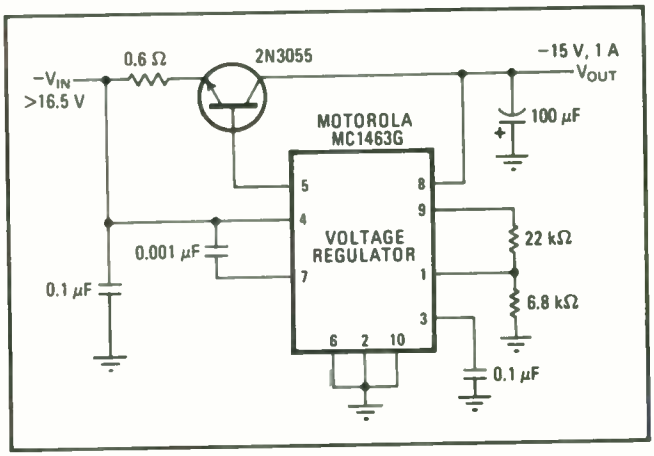
Boosting IC regulator current with almost no power loss

by Don Kesner
Motorola Inc., Semiconductor Products Div., Phoenix, Ariz.

When the output current of a monolithic voltage regulator is boosted by the addition of a series-pass transistor, the regulator's efficiency is usually lowered because of the base-emitter voltage drop of the outboarded transistor. This added transistor voltage loss raises the input/output voltage differential of the over-all circuit, thereby causing a power loss.

The circuit shown, however, increases regulator current capability without this power loss. The output pin (pin 6 here) of the regulator is grounded so that the device's internal series-pass transistor does not contribute to the over-all input/output saturation characteristics. With this bypass technique, the low voltage differential of the IC alone can be maintained (typically at 1.5 volts here).

For the regulator indicated in the diagram, the absolute minimum differential is based on internal current-source saturation and cannot be lowered, but it is usually large enough to prevent the external transistor from saturating. Even with a type 2N3055 transistor as the booster, there is no significant difference in the minimum voltage differential with or without current boosting, and with or without a current-limiting resistor. □



Current boosting with minimal power loss. External series-pass transistor increases current capability of monolithic voltage regulator, but decreases power efficiency of over-all circuit. Grounding regulator's normal output terminal (pin 6) bypasses internal series-pass transistor, maintaining over-all circuit's voltage differential (V_{IN} – V_{OUT}) at that of the IC alone and making power loss negligible.

Adding foldback resistor provides overload safety

by William J. Riley
General Radio Co., Bolton, Mass.

A single resistor can solve the common problem of dissipating power in a voltage regulator. Including this additional resistor in an ordinary current-limiting power-supply regulator provides effective current-foldback overload protection.

Without resistor R_F, the circuit in the diagram is a typical power-supply regulator. The output current is sensed by resistor R_S and limited to:

$I_{LIMIT} = V_{BE1}/R_S$

when transistor Q_1 turns on. (V_{BE1} is Q_1's base-emitter voltage when Q_1 is conducting.) Although this current-limiting prevents instantaneous damage to series-pass transistor Q_2, it may not protect Q_2 from overheating under a sustained short-circuit condition.

Current foldback, achieved by simply adding resistor R_F, can overcome the problem. During normal operation, resistor R_F has no effect but to reduce the current-limiting threshold to approximately:

$I_{LIMIT} = V_{BE1} - (E_i - E_o)(R_B/R_F)/R_S$

In the event of an overload, the output voltage falls, and the increasing current through resistor R_F causes the limit current to also fall, approaching a short-circuit value of:

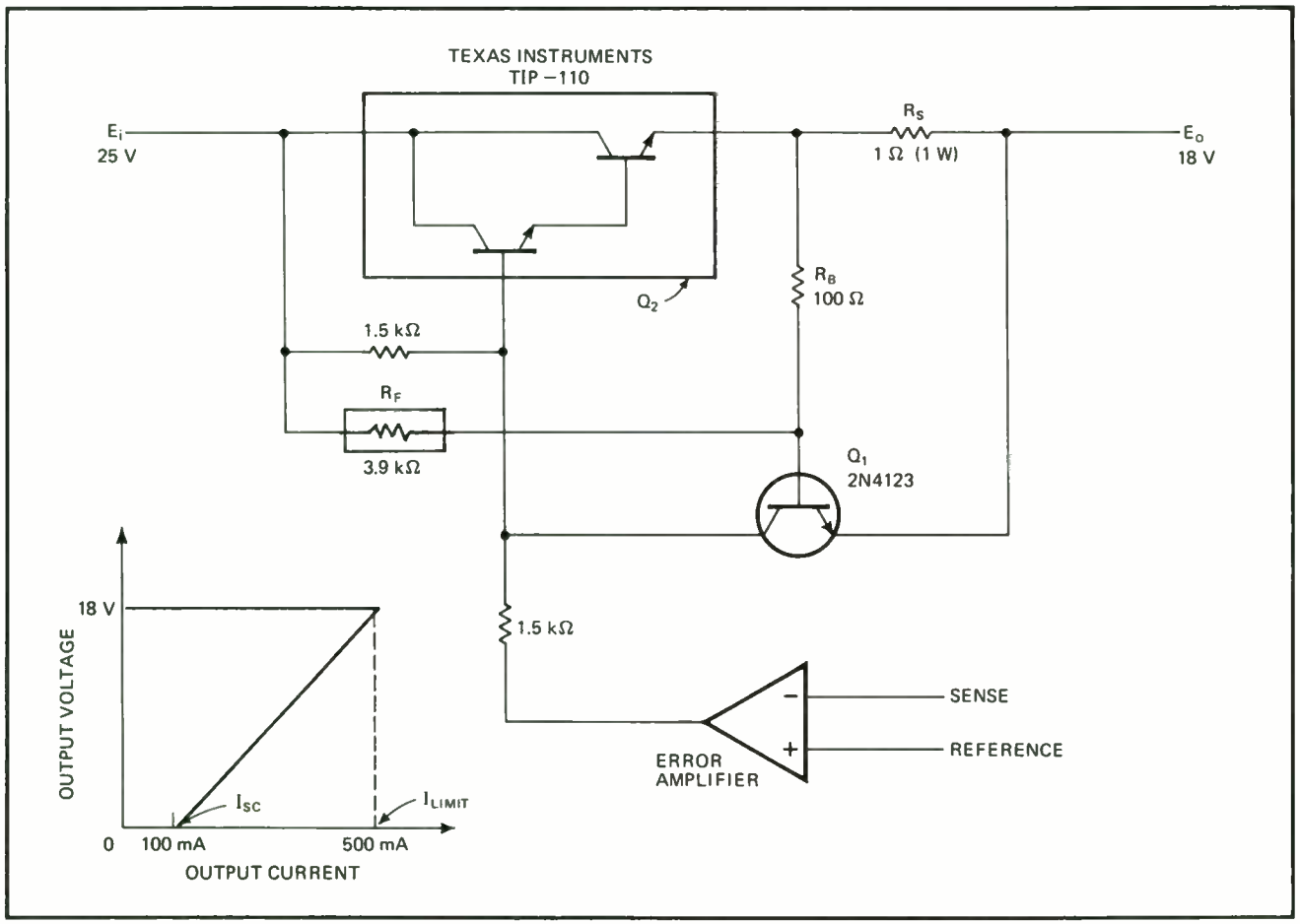
$I_{SC} = V_{BE1} - E_i(R_B/R_F)/R_S$,

which is considerably smaller than I_{LIMIT}. Therefore, this current foldback action, illustrated in the volt-ampere characteristic, greatly eases the heat-sinking requirements for series-pass transistor Q_2.

The output voltage will return to normal after the short is removed, as long as the foldback is not so great that the output current is reduced to zero. The current-limit threshold is sufficiently stable for most applications. It becomes smaller for increasing unregulated input voltage, as well as for increasing ambient temperature. This keeps the dissipation of transistor Q_2 within its rated limit.

Typical nominal component and parameter values are shown in the figure. □

Resistor folds back current. Amount of power dissipated, during overload, in conventional current-limiting voltage regulator can be decreased by adding a foldback resistor between transistor Q_1 and the unregulated input voltage. Resistor R_F eases heat-sinking requirements of transistor Q_2 by folding back current when there is an overload. Output voltage can be returned to normal after overload is removed.



Current-sharing design boosts regulator output

by Marvin Vander Kooi
National Semiconductor Corp., Santa Clara, Calif.

When a higher-than-rated current must be supplied by a monolithic voltage regulator, an external boost transistor is usually employed. Most normal current-boosting schemes, however, require additional active devices to duplicate some of the worthwhile safety features of the integrated regulator—for instance, short-circuit current limiting, safe-operating-area protection, and thermal shutdown.

The regulator circuit in the figure retains these safety features by extending them to the external pass transistor through a current-sharing design. This regulator, which is intended for transistor-transistor-logic circuits, has an output voltage of 5 volts at 5 amperes and a typical load regulation of 1.4%.

Resistors R_1 and R_2 provide the necessary current division, assuming that the transistor's base-emitter voltage equals the diode drop. Then the voltage drops across resistors R_1 and R_2 are equal, and the currents through R_1 and R_2 are inversely proportional to their resistances. With the resistance values shown, resistor R_1 has four times the current flow of resistor R_2.

For reasonable values of transistor beta, the transistor's emitter current (from resistor R_1) will approximately equal its collector current, while the current through resistor R_2 will equal the current flowing through the monolithic regulator. Under overload or short-circuit conditions, therefore, the protection circuitry of the packaged regulator not only limits its output current, but also limits the output current of the pass transistor to a safe value, thereby preventing device damage.

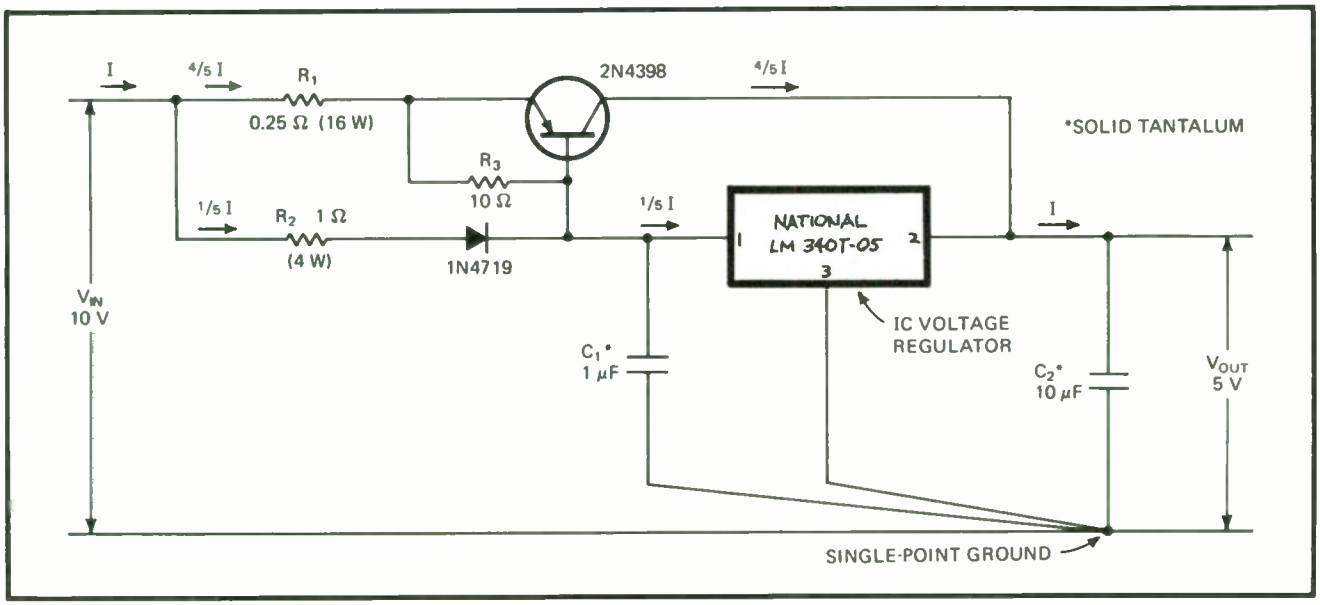
Thermal-overload protection is also extended to the external pass transistor when its heat sink is designed to have at least four times the capacity of the regulator's heat sink. This is because both devices have almost the same input and output voltages and share load current in a 4:1 ratio. During normal operation, up to 1 A of current flows through the regulator, while up to 4 A flow through the outboarded pass transistor.

Under instantaneous overload conditions, the over-all circuit will supply approximately 9 A of output current (for junction temperatures varying from 0°C to 70°C). This reflects the 1.8-A current limit of National's LM340T regulator, causing the times-four current limit for the pass transistor to be 7.2 A. If the short-circuit condition is continuous, the regulator heats up and limits the total steady-state current to about 7.5 A.

For optimum current-sharing between the regulator and the pass transistor as the temperature changes, the diode should be located physically near the pass transistor. Also, the diode's heat-sinking arrangement should keep it at the same temperature as the pass transistor. If the LM340T is used and mounted on the same heat sink as the pass transistor, the regulator should be electrically isolated from the heat sink, since its case (pin 3) is at ground potential, but the case (collector) of the pass transistor is at the regulator's output potential.

Capacitor C_1 prevents unwanted oscillations, while capacitor C_2 improves the output impedance of the over-all circuit. Resistor R_3 provides a path to unload the excessive charge that develops in the base region of the pass transistor when the regulator suddenly goes from full load to no load. The circuit's single-point ground system allows the regulator's sense terminals (pins 2 and 3) to monitor load voltage directly, rather than at some point along a possibly resistive ground-return line carrying up to 5 A of load current. □

Sharing the load for TTL. Current-boosting scheme for IC regulator divides input current in 4:1 ratio between the regulator and an external pass transistor. This current-sharing preserves the IC's short-circuit, overload, and thermal-shutdown safety features. The circuit provides an output of 5 volts at 5 amperes, regulated to 1.4%. The protection diode and the transistor should be kept at the same temperature.



Economical series regulator supplies up to 10 amperes

by J.E. Buchanan and C.W. Nelson
Westinghouse Electric Corp., Systems Development Division, Baltimore, Md.

A highly efficient series regulator made of standard IC components is an ideal high-current digital-logic supply. It provides an output voltage of 5 to 6 volts at a current of up to 10 amperes, without needing separate bias sources or special transformers.

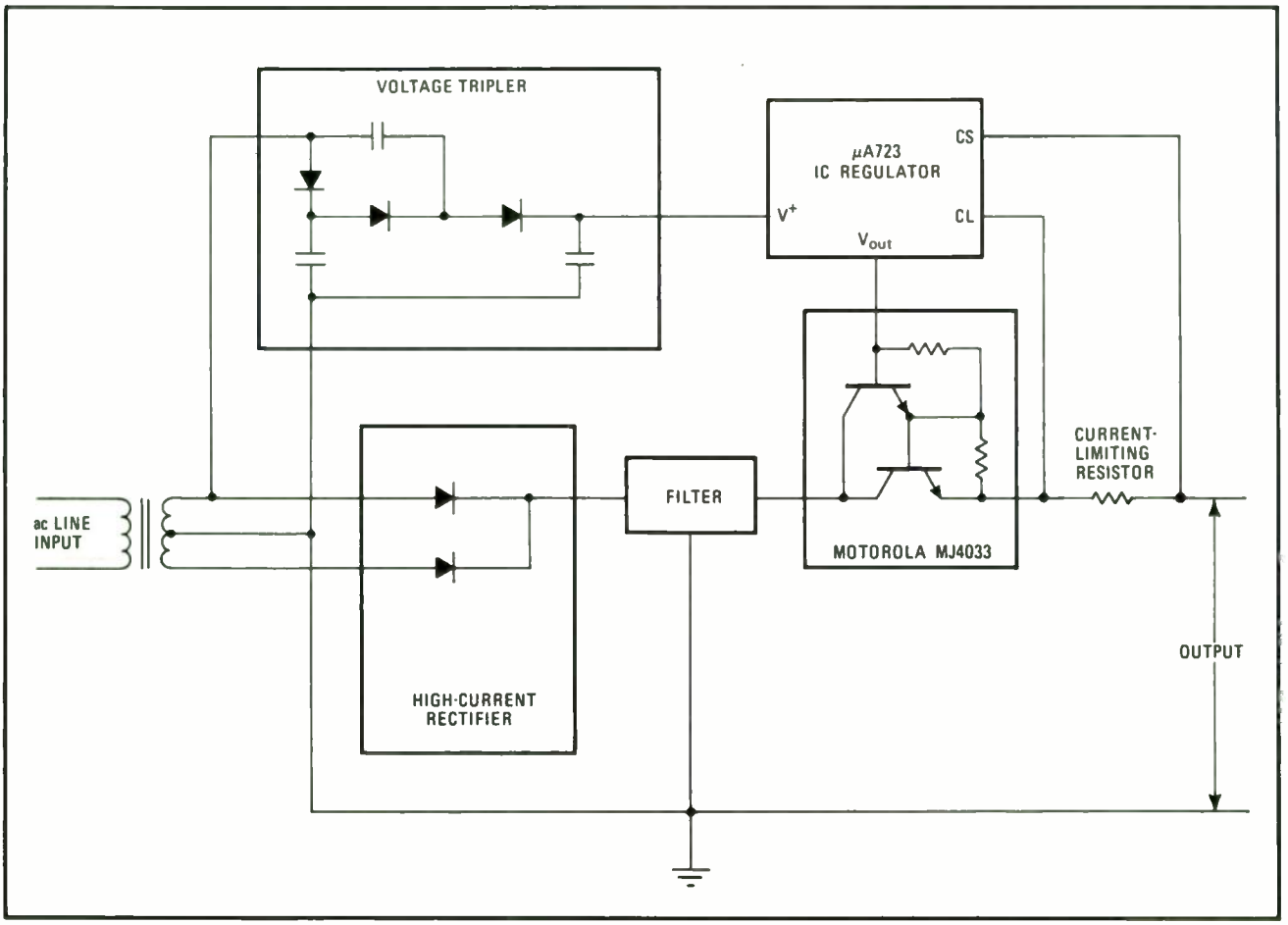
As shown in the figure, a standard transformer is used at the input of the circuit. The transformer's output voltage is rectified and filtered in a conventional manner for the high-current-supply path to the output of the circuit.

This transformer voltage also goes to a voltage tripler, which raises it so that it becomes large enough to drive the IC regulator without help from any outside bias supply. Most three-terminal IC regulators require 10 V or more to bias their internal references properly, preserving their stability with changing input, load, or temperature conditions.

The IC regulator, in turn, drives a high-current power Darlington transistor pair, which is biased by the high-current rectifier. The Darlington pair acts as the circuit's series-pass element and increases the low-milliampere current output from the IC regulator to several amperes.

The circuit's efficiency is very good because the voltage of the high-current supply path can be kept low, permitting the Darlington pair to be driven near saturation with a minimum high-current source voltage. A single transistor can be used instead of the Darlington pair if a lower output current is desired. □

High-current logic supply. This series regulator develops 5 volts at 10 amperes for powering digital-logic circuits. High efficiency is achieved by using a voltage tripler, which operates directly from the input-line transformer, to bias the IC regulator's internal reference. This eliminates the need for a special bias supply or a special transformer. The Darlington transistor pair serves as the series-pass element.



Switching regulator produces constant-current output

by Steven E. Summer
Hauppauge, N.Y.

The high efficiency that can be achieved with switching regulators need not be restricted solely to voltage regulators. By taking advantage of the convenience of a monolithic voltage regulator, a free-running constant-current switching regulator having a 1-ampere output can be built for applications like battery charging.

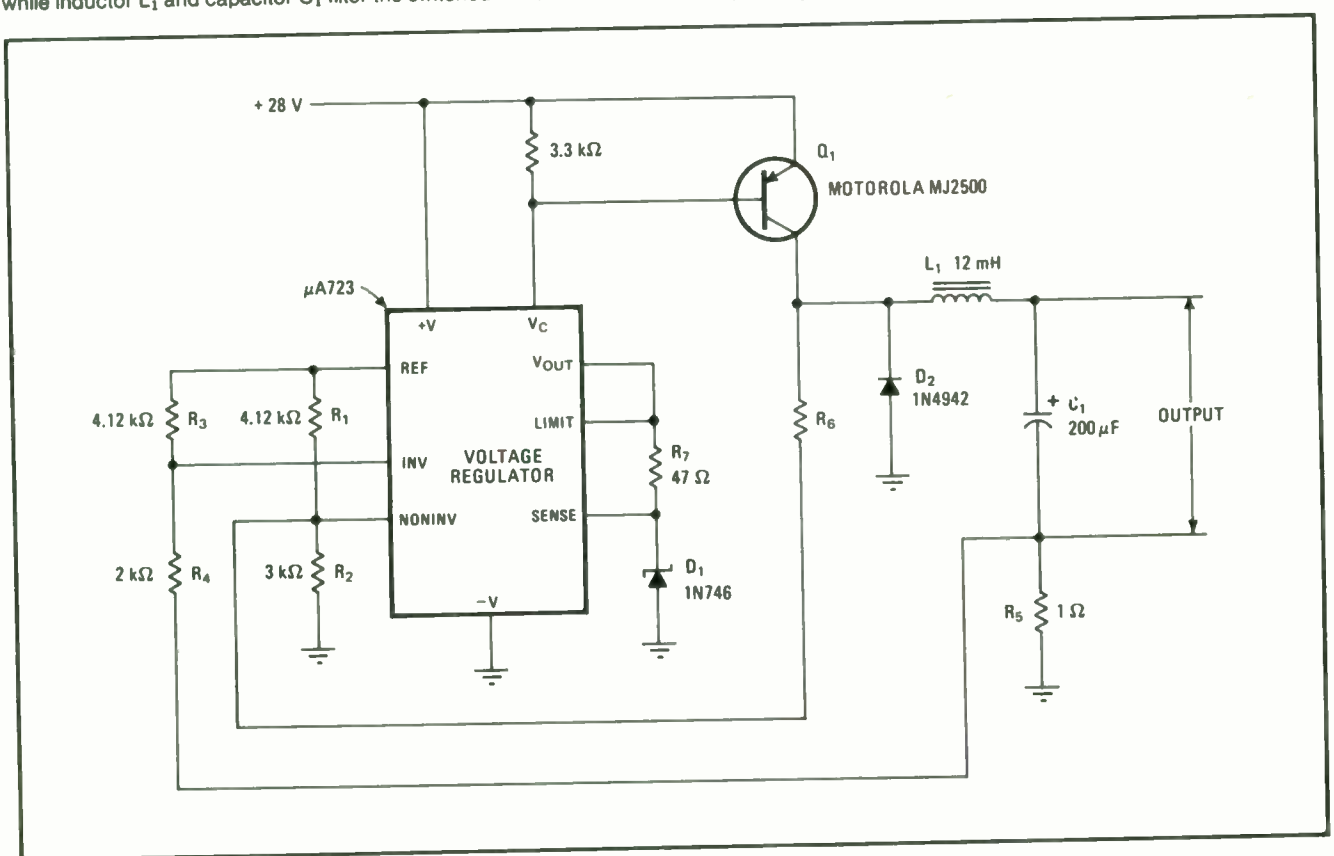
A 723-type IC regulator acts as the circuit's reference and comparator. The IC's 7.15-volt internal reference is scaled to approximately 3 V by the voltage divider formed by resistors R_1 and R_2. These resistors also feed the IC's noninverting input, while resistors R_3 and R_4 drive the IC's inverting input. The lower end of resistor R_4 is connected to shunt resistor R_5, and approximately 1 V appears across this shunt when the IC's comparator terminals are nearly balanced.

A hysteresis voltage of around 28 millivolts is applied to the IC's noninverting input through resistor R_6. This sets the minimum output ripple of the circuit at 28 milliamperes peak to peak. But if the storage time of output transistor Q_1 is significant, the ripple current will be higher.

When the circuit's feedback loop calls for a current increase, the output stage of the IC regulator conducts and a current pulse of 12 mA flows into the V_C terminal. (The size of the current pulse is determined by resistor R_7.) This current pulse drives transistor Q_1.

The zener diode (D_1) is used to bias the output stage of the IC regulator, while the junction diode (D_2) operates as a freewheeling diode. Inductor L_1 and capacitor C_1 filter the switched waveform. The circuit's maximum operating frequency depends on the size of the load and is typically 20 kilohertz. □

Constant-current source. Switching regulator circuit provides a 1-ampere constant-current output that has a peak-to-peak ripple of 28 milliamperes. The integrated 723-type voltage regulator functions as a reference source and a comparator. Transistor Q_1 is a current booster, while inductor L_1 and capacitor C_1 filter the switched waveform. The circuit's operating frequency can be as high as 20 kilohertz.



Regulating supply voltage all the way down to zero

by Brother Thomas McGahee
Don Bosco Technical School, Boston, Mass.

Precision monolithic voltage regulators make it fairly easy to design a high-performance power supply with a minimum of external components. These regulators have one general fault, however—they cannot regulate to any voltage lower than their reference, which is usually about 7 V. Sometimes, a voltage divider can be used to reduce the reference voltage, but if the reference voltage is reduced below approximately 2 V, good regulation can no longer be maintained.

The circuit shown in the figure, on the other hand, allows the reference voltage to be adjusted all the way down to the offset voltage of the regulator's internal op amp. REGULATOR$_1$ and its associated circuitry form a bias supply that provides a voltage of about −7 V for the V$^-$ terminal of the main regulator (REGULATOR$_2$). Since the noninverting input of this regulator is connected to the common ground of the circuit, its reference voltage appears to be +7 V with respect to this V$^-$terminal.

There will be a 7-V drop across resistors R_2 and R_3. When R_1 is set to its minimum value, the circuit's output voltage will be equal to the reference voltage. If the output is measured with respect to the V$^-$ terminal of REGULATOR$_2$, it will be 7 V. But if it is measured with respect to the common ground, it will be zero.

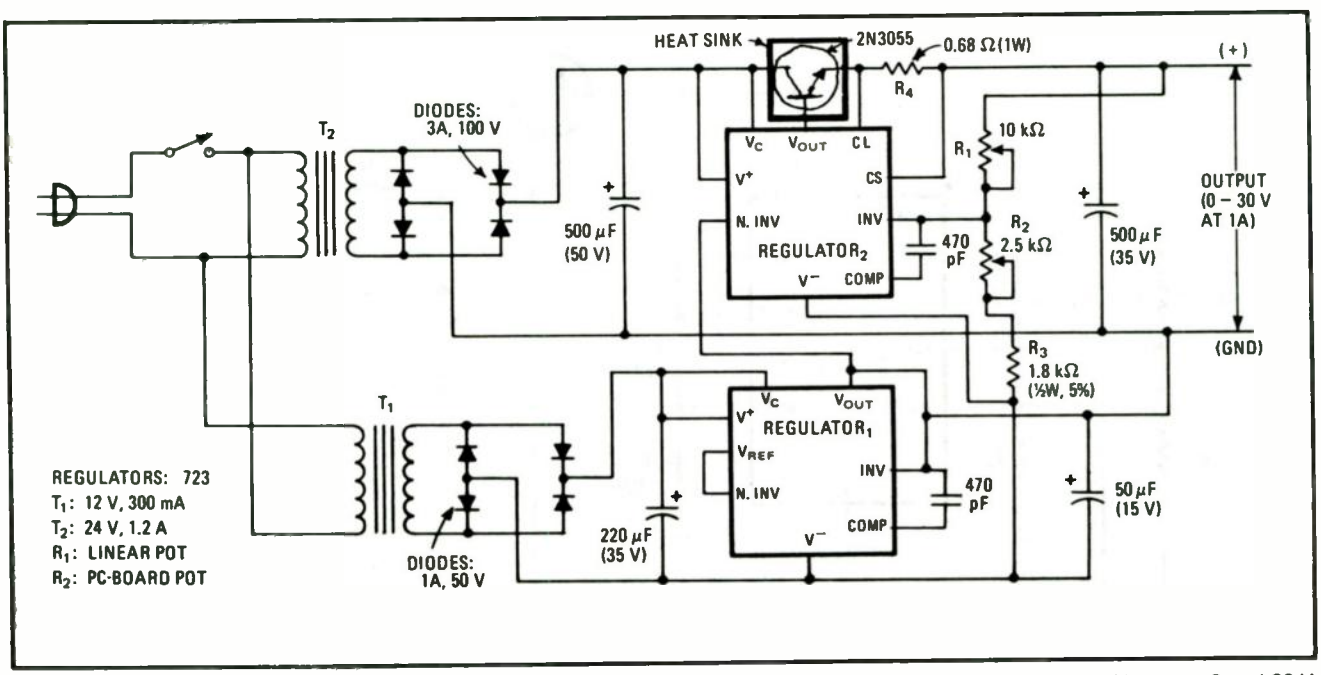
The maximum voltage available at the output is determined by the value of resistor R_2. For the component values shown here, the maximum voltage may be set anywhere from 16 to 39 V. But voltages above 30 V will not be regulated very well because the supply is using a 24-V transformer (T_2).

The equation for the output voltage is:

$$V_{OUT} = R_1 V_B/(R_2+R_3)$$

where V_B is the absolute value of the bias voltage (7 V in this case). The bias supply normally will be producing about 12 milliamperes of current. Under worst-case conditions, however, it may be required to provide a maximum of 40 mA. Transformer T_1, therefore, should be a 12-V unit capable of supplying at least 50 mA (since REGULATOR$_1$ will require some current itself).

The transistor at the output of REGULATOR$_2$ boosts the circuit's output current. Resistor R_4 acts as the current-limiting resistor. □



Variable supply. This power supply, which employs two IC voltage regulators, produces a regulated output voltage of between 0 and 30 V. REGULATOR$_1$ provides the bias voltage for REGULATOR$_2$ so that the latter device can operate with respect to a common ground. The lowest regulated output voltage, then, is approximately zero, rather than the reference voltage of REGULATOR$_2$.

Regulator for op amps practically powers itself

by Richard Eckhardt
Electronics Consulting & Development, Cambridge, Mass.

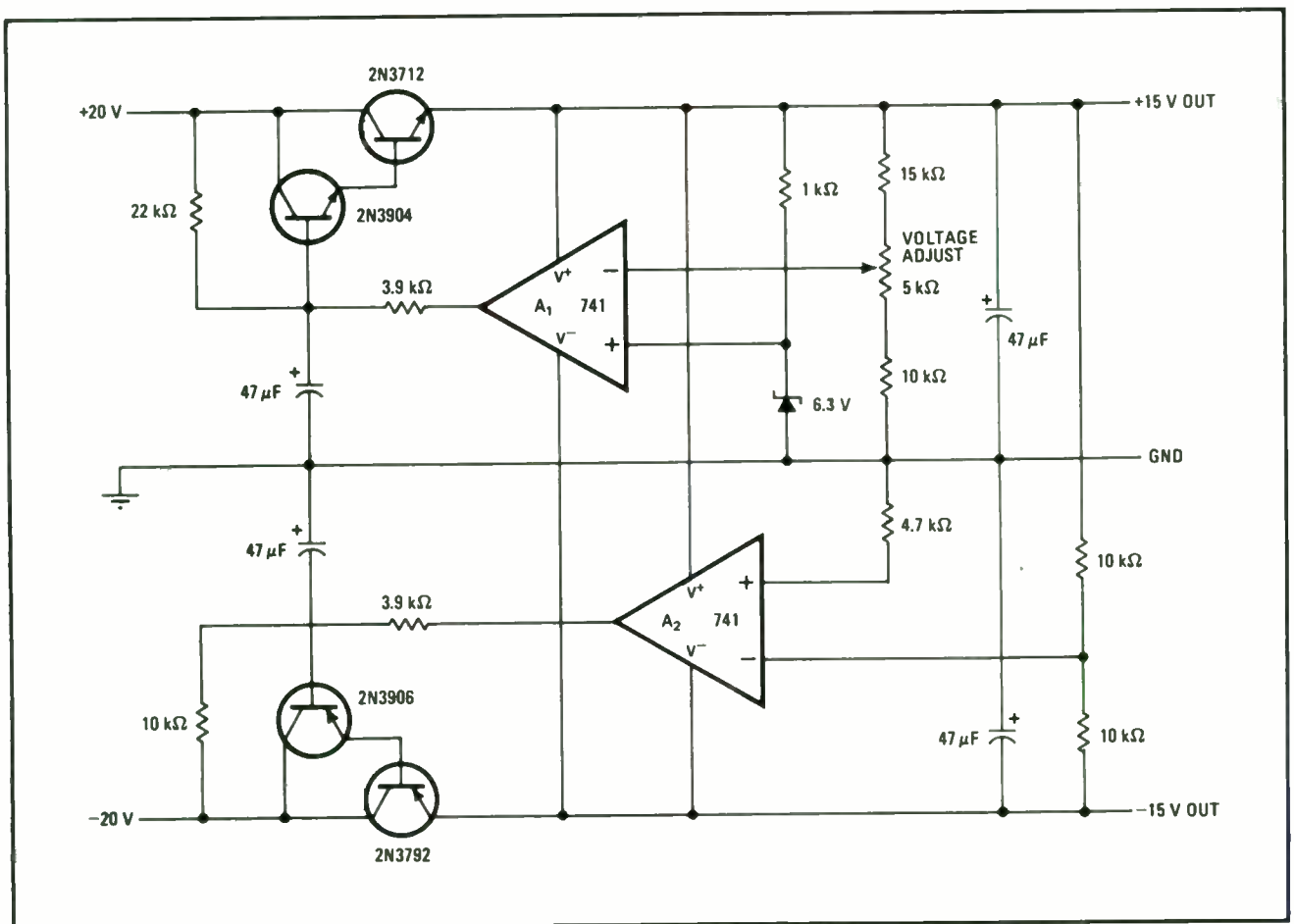
Here's a rather novel way to build a dual-voltage regulator for powering operational amplifiers that offers good tracking, as well as low ripple. Tracking between the two output voltages is good because only one reference source is used for both the positive and negative sides of the regulator. Although the circuit employs two op amps itself, they are powered by their own outputs. Furthermore, the circuit's output-current capability is on the order of several amperes, and output ripple is held to less than 1 millivolt peak-to-peak.

The circuit, shown in the figure, operates as a conventional series-pass regulator on its positive side to develop its +15-volt output. Amplifier A_1 is used for error-detection. The pass transistor for the positive side is biased on from the unregulated +20-V input supply voltage. The output voltage from amplifier A_1 then adjusts this transistor's output.

On the negative side (−15-V output) of the regulator, amplifier A_2 operates as a unity-gain follower. The pass transistor on the negative side is biased in a manner similar to its positive counterpart. The value of the biasing resistor for the negative pass transistor is different from the value of the biasing resistor for the positive pass transistor in order to bring A_2's output closer to the negative supply voltage.

Since amplifier A_2 is wired in a follower configuration, the reference voltage developed by the zener diode can be used for both the positive and negative sides of the regulator. The two output voltages, therefore, track each other within approximately 50 mV.

With suitable modification, the same circuit approach can be used to build a regulator for devices other than op amps that require a split supply. □



Split supply. Regulator circuit for op amps develops ±15-V outputs from a ±20-V unregulated source with less than 1 millivolt of ripple. Although the regulator uses op amps itself, they receive their power inputs from their own outputs. Ampflier A_1 acts as an error detector, while amplifier A_2 is a voltage follower. The single zener voltage reference means that tracking is good between the positive and negative sides.

Regulating voltage with just one quad IC and one supply

by R. A. Koehler
York University, Toronto, Canada

Full-range, high-performance power supplies are often bulky and expensive because they require two independent voltage sources—one main and one reference—with associated rectifiers, filter capacitors, and reference regulator circuitry.

But only one unregulated source of about 26 volts dc and one ground-sensing quad operational amplifier are necessary in a regulated power supply that provides 1 ampere at 0 to 20 V with foldback current-limiting and overload indication. It achieves line and load regulation within ±0.02% over the full range of load conditions, even when the input voltage varies between 24 and 28 V dc. When the regulator is quiescent, its current requirement amounts to less than 10 milliamperes.

Amplifier A_1 is a self-biased, constant-current amplifier that provides a stable reference voltage [*Electronics*, March 13, 1972, p. 74]. Its output, V_1, depends on the breakdown voltage V_z of the zener diode, D_1:

$$V_1 = V_z[1 + (R_1/R_2)]$$

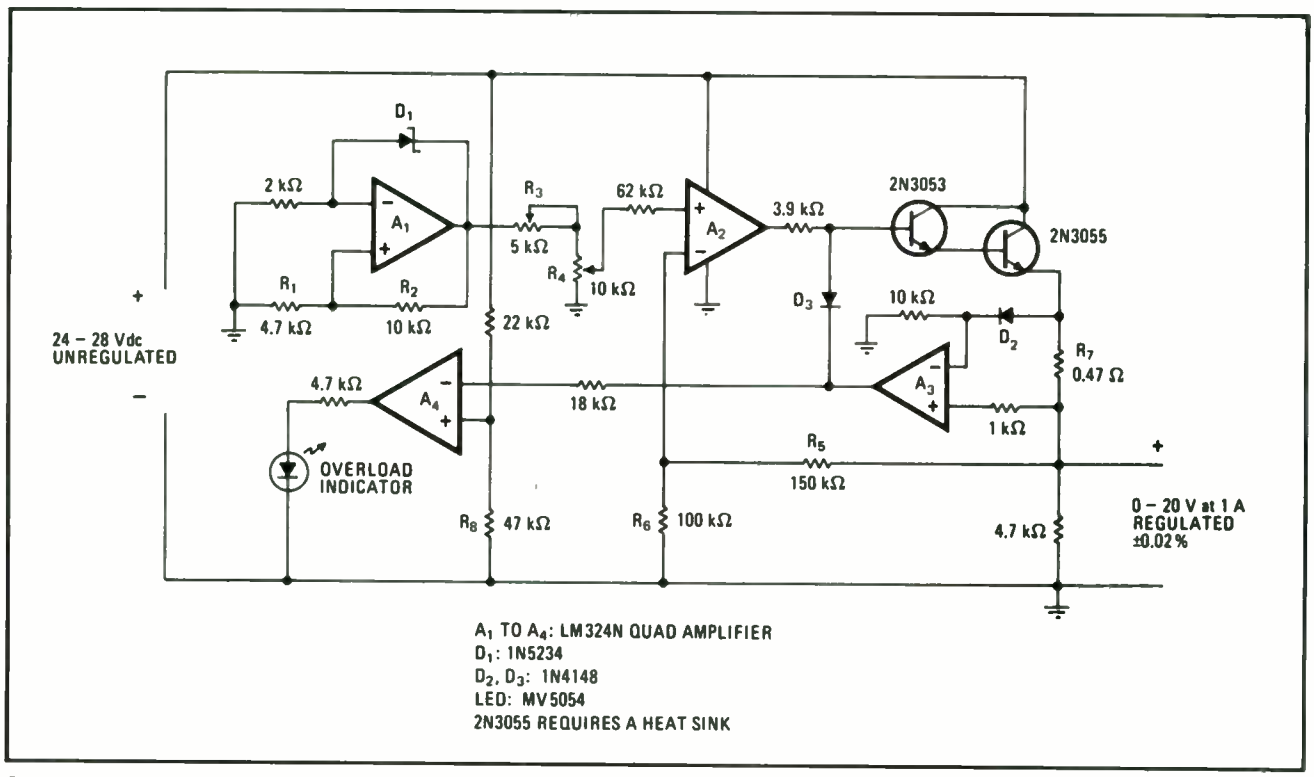
It is approximately 9.1 V for the values shown in the diagram. The potentiometers R_3 and R_4 bring V_1 down to a desired value V_2, which is amplified by A_2 and the Darlington output stage to the output level:

$$V_{out} = V_2(R_5 + R_6)/R_6$$

With R_4 at its maximum-voltage position, variable resistor R_3 sets the voltage at exactly 20 V; thereafter, R_4 varies the output voltage over its full range. The output stage gain is 2.5 for the values shown.

Amplifier A_3 monitors the regulator's output current under varying loads. It compares the voltage across R_7 (a very small resistance) with the drop across diode D_2. Whenever the former is greater than the latter, the output of A_3 drops, biasing diode D_3 forward; thus it reduces the output voltage by removing the drive to the Darlington stage. If the load continues to increase, the output of A_3 becomes low enough to indicate, through amplifier A_4, and a light-emitting diode, an overload condition. The circuit's overload threshold may be changed, if desired, by changing the value of resistor R_8.

The output transistors may be replaced by a single power Darlington, such as 2N6050, to reduce the package count from three to two. □



Op amp regulator. An unregulated 26-volt source becomes a 1-ampere 0-to-20-V supply regulated to within ±0.02% by a simple quad operational amplifier. Input can vary between 24 V and 28 V, and quiescent current is less than 10 mA. A light-emitting diode gives an overload indication, the level of which depends on the value of resistor R_8. Single power Darlington can replace the two transistors.

Regulating high voltage with low-voltage transistors

by Mahendra J. Shah
University of Wisconsin, Madison, Wis.

High-voltage regulation usually calls for high-voltage transistors. But, by absorbing the bulk of the output voltage with a zener diode, only relatively low-voltage devices are needed. The circuit illustrated regulates 250 volts with a 90-v transistor; however, the same concept can be applied to regulating voltages in the kilovolt range.

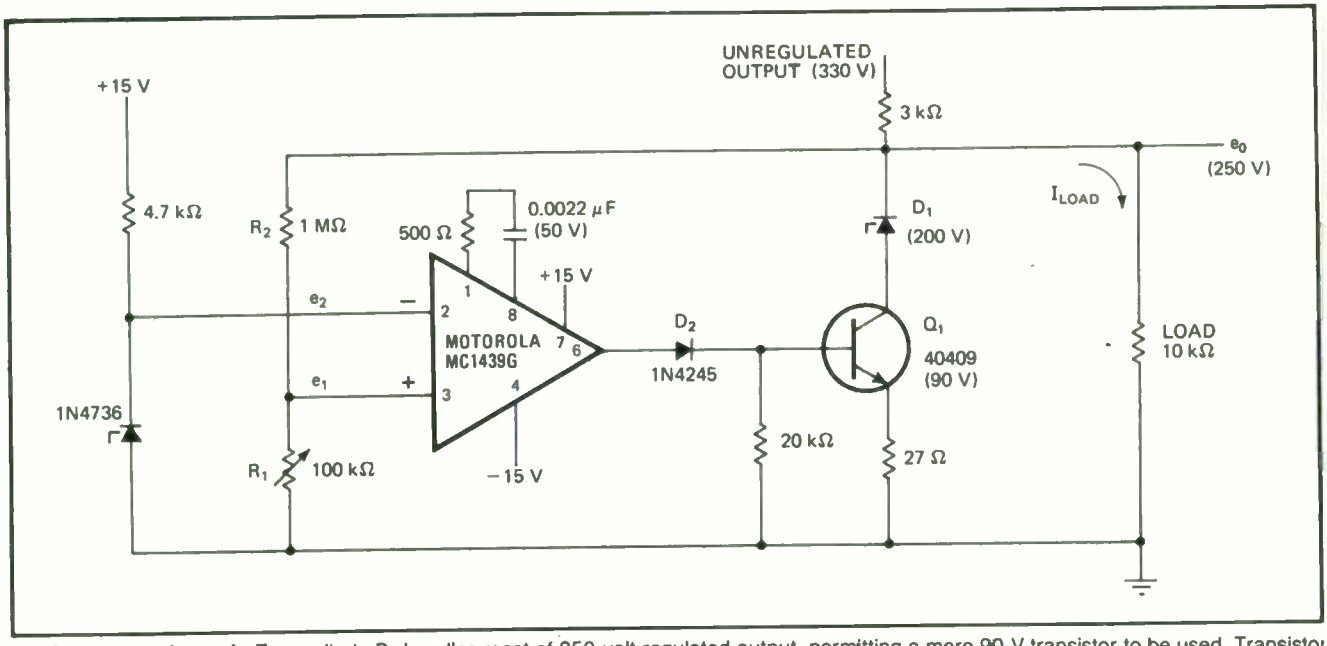
Transistor Q_1 operates as a shunt regulator, monitoring the output voltage, e_o, across the load. Without zener diode D_1, Q_1 would be subjected to nearly all the output voltage. But D_1 absorbs a good part of this voltage because it is in series with the collector of Q_1. This allows Q_1 to operate at the difference voltage between e_o and the voltage across the zener.

The output voltage is divided by resistors R_1 and R_2 and applied to the non-inverting input of an operational amplifier, which functions as a comparator. The op amp compares e_1 with e_2, and maintains output voltage e_o so that $e_1 = e_2$. Regulated output is a function of the comparator's inverting input voltage, e_2, and the resistors of the voltage divider:

$$e_o = e_2(1 + R_2/R_1)$$

Another diode, D_2, protects Q_1's base-emitter junction from reverse breakdown. During normal operation, D_1 is forward-biased, allowing Q_1 to receive base drive for proper regulation.

For the component values shown, voltage regulation from no load to full load (25 milliamperes) is less than 0.04%. Unregulated voltage is 330 v, and the voltage across Q_1's collector-emitter junction is approximately 40 v. □



Putting a zener to work. Zener diode D_1 handles most of 250-volt regulated output, permitting a mere 90-V transistor to be used. Transistor Q_1 acts as conventional shunt regulator for load resistance. Op-amp comparator maintains output voltage to keep its inputs e_1 and e_2 equal, thereby providing proper base drive for Q_1. Regulated output voltage is: $e_o = e_2(1 + R_2/R_1)$. Unregulated output of 330 V is also available.

Regulating high voltages with low-voltage zeners

by Glen Coers
Texas Instruments, Components Group, Dallas, Texas

A regulator for a high-voltage power supply can be built with a low-voltage zener acting as the reference-voltage source. The output of this regulator circuit can be adjusted between 50 and 250 volts, and regulation is typically 0.5%. The circuit is particularly useful when operational amplifiers cannot be employed because the low-voltage positive and negative supplies needed to power them are not readily available.

Zener diode D_1 supplies the reference voltage. It should be chosen according to the temperature coefficient desired and the maximum current required. The field-effect transistor, Q_1, allows resistors R_1 and R_2 to have high values so that output loading can be kept to a minimum and low-wattage resistors can be used. If these resistors were connected directly to the base of transistor Q_2, the circuit would provide poor regulation and have a high dynamic output impedance because of Q_2's low input impedance.

The regulator's output voltage can be written as:

$$V_o = (V_{D1} + V_{BE} + V_{GS})(R_1 + R_2)/R_1$$

The open-loop gain of transistor Q_2, which is equal to 67 decibels, is a function of the FET's transconductance and the circuit's load resistance. The feedback factor, β, for the regulator is:

$$\beta = R_1/(R_1 + R_2)$$

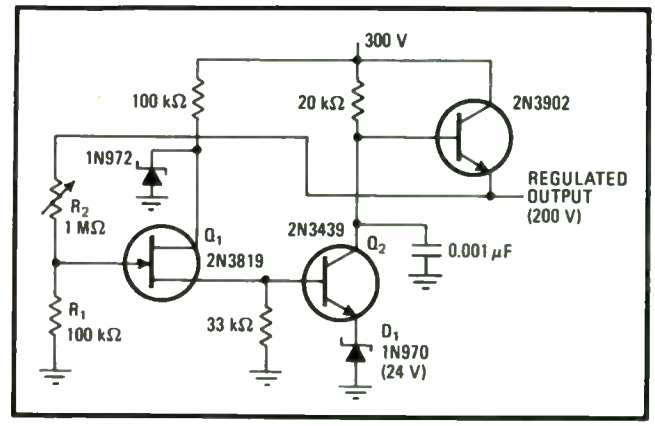
where $R_2 = 9R_1$

The closed-loop voltage gain, which equals 20 dB, can be expressed as:

$$A_{VC} = AV_o/(1 - AV_o\beta)$$

And the gain with feedback becomes:

$$A_{Vf} = 67 - 20 = 47 \text{ dB}$$ □



Discrete-component regulator. High-voltage power-supply regulator produces output of 50 to 250 volts at a typical regulation of 0.5%. A low-voltage zener, D_1, provides the reference voltage, establishing the circuit's current output and its temperature coefficient. The field-effect transistor, Q_1, allows large-value low-wattage resistors to be used for R_1 and R_2, thereby minimizing loading.

REGULATOR PERFORMANCE

INPUT VOLTAGE	OUTPUT VOLTAGE	LOAD CURRENT	OUTPUT VOLTAGE
270 V 300 V (Δ = 30 V) 330 V (Δ = 30 V)	199.2 V 200.4 V (Δ = 1.2 V) 201.2 V (Δ = 0.8 V)	0 mA 50 mA (Δ = 50 mA) 100 mA (Δ = 50 mA)	200.3 V 200.0 V (Δ = 0.3 V) 199.5 V (Δ = 0.5 V)