

**Elektor
Electronics
USA**

Elegant L-C-R Bridge

The Complete Preamplifier

8031 Single Board Computer

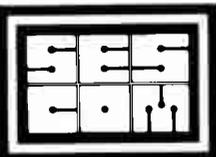
A PC Multi-measurement Card

1.5-70MHz SWR Meter

A Logic Analyzer



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MODEL #.	DESCRIPTION (Width x Depth x Height)	PRICE \$
1RU5	19 x 5 x 1.75 in. (482.6 x 127 x 44.45mm)	28.00
1RU7	19 x 7 x 1.75 in. (482.6 x 177 x 44.45mm)	30.00
1RU10	19 x 10 x 1.75 in. (482.6 x 254 x 44.45mm)	32.00
2RU5	19 x 5 x 3.50 in. (482.6 x 127 x 88.9mm)	30.00
2RU7	19 x 7 x 3.50 in. (482.6 x 177.8 x 88.9mm)	32.00
2RU10	19 x 10 x 3.50 in. (482.6 x 254 x 88.9mm)	34.00
3RU5	19 x 5 x 5.25 in. (482.6 x 127 x 133.35mm)	38.00
3RU7	19 x 7 x 5.25 in. (482.6 x 177.8 x 133.35mm)	40.00
3RU10	19 x 10 x 5.25 in. (482.6 x 254 x 133.35mm)	42.00

The above rack chassis are made of .063 aluminum. The front and rear panels are clear brushed anodized. All hardware is included. Assembly Required.

Metal Cabinets



MODEL #.	DESCRIPTION (Width x Depth x Height)	PRICE \$
MC-1A	4 x 3 x 2 in. (101.6 x 76.2 x 50.8mm)	15.00
MC-2A	6 x 3 x 2 in. (152.4 x 76.2 x 50.8mm)	17.00
MC-3A	8 x 3 x 2 in. (203.2 x 76.2 x 50.8mm)	19.00
MC-4A	4 x 5 x 3 in. (101.6 x 127 x 76.2mm)	17.00
MC-5A	6 x 5 x 3 in. (152.4 x 127 x 76.2mm)	19.00
MC-6A	8 x 5 x 3 in. (203.2 x 127 x 76.2mm)	21.00
MC-7A	4 x 7 x 4 in. (101.6 x 177.8 x 101.6mm)	19.00
MC-8A	6 x 7 x 4 in. (152.4 x 177.8 x 101.6mm)	21.00
MC-9A	8 x 7 x 4 in. (203.2 x 177.8 x 101.6mm)	23.00

The above cabinets are made of .063 aluminum. The front and rear panels are clear brushed anodized. All hardware and rubber feet are included. Assembly Required.

Punch Kits and Punches



Model #.	Description	Price \$	Model #.	Description	Price \$
HP-1	5 JR TOOL KIT	49.00	HP-2	XX TOOL KIT	129.75
HP-3	BENCH MOUNT	15.00	HP-4	BENCH MOUNT	15.00
PD-1	ROUND 1/16"	6.00	PD-30	ROUND 1/16"	9.50
PD-2	ROUND 5/64"	6.00	PD-31	ROUND 5/64"	9.50
PD-3	ROUND 3/32"	6.00	PD-32	ROUND 3/32"	9.50
PD-4	ROUND 7/64"	6.00	PD-33	ROUND 7/64"	9.50
PD-5	ROUND 1/8"	6.00	PD-34	ROUND 1/8"	9.50
PD-6	ROUND 9/64"	6.00	PD-35	ROUND 9/64"	9.50
PD-7	ROUND 5/32"	6.00	PD-36	ROUND 5/32"	9.50
PD-8	ROUND 11/64"	6.00	PD-37	ROUND 11/64"	9.50
PD-9	ROUND 3/16"	6.00	PD-38	ROUND 3/16"	9.50
PD-10	ROUND 13/64"	6.00	PD-39	ROUND 13/64"	9.50
PD-11	ROUND 7/32"	6.00	PD-40	ROUND 7/32"	9.50
PD-12	ROUND 15/64"	6.00	PD-41	ROUND 15/64"	9.50
PD-13	ROUND 1/4"	6.00	PD-42	ROUND 1/4"	9.50
PD-14	ROUND 17/64"	6.00	PD-43	ROUND 17/64"	9.50
PD-15	ROUND 9/32"	6.00	PD-44	ROUND 9/32"	9.50
PD-16	SQUARE 1/8"	66.90	PD-45	ROUND 19/64"	9.50
PD-17	SQUARE 5/32"	66.90	PD-46	ROUND 5/16"	9.50
PD-18	SQUARE 3/16"	66.90	PD-47	ROUND 21/64"	9.50
PD-19	REC. 1/8 x 3/16"	66.90	PD-48	ROUND 11/32"	9.50
PD-20	REC. 1/8 x 7/32"	66.90	PD-49	ROUND 23/64"	9.50
PD-21	REC. 1/8 x 15/64"	66.90	PD-50	ROUND 3/8"	9.50
			PD-51	ROUND 25/64"	9.50
			PD-52	ROUND 13/32"	9.50
			PD-53	ROUND 27/64"	9.50
			PD-54	ROUND 7/16"	9.50
			PD-55	ROUND 29/64"	9.50
			PD-56	ROUND 15/32"	9.50
			PD-57	ROUND 31/64"	9.50
			PD-58	ROUND 1/2"	6.00
			PD-59	ROUND 33/64"	6.00
			PD-60	ROUND 17/32"	6.00
			PD-61	SQUARE 1/8"	66.90
			PD-62	SQUARE 5/32"	66.90
			PD-63	SQUARE 3/16"	66.90
			PD-64	REC. 1/8 x 3/16"	83.10
			PD-65	REC. 1/8 x 1/4"	83.10
			PD-66	REC. 1/8 x 5/16"	83.10
			PD-67	REC. 1/8 x 3/8"	83.10
			PD-68	REC. 1/8 x 1/32"	75.10

Rub-On Letters

MODEL #.	DESCRIPTION	PRICE \$
LT-1	CAPITAL LETTERS HELVETICA 14 pt.	3.95
LT-2	LOWER CASE LETTERS HELVETICA 14 pt.	3.95
LT-3	NUMBERS HELVETICA 14 pt.	3.95
LT-4	CAPITAL LETTERS HELVETICA 10 pt.	3.95
LT-5	LOWER CASE LETTERS HELVETICA 10 pt.	3.95
LT-6	NUMBERS HELVETICA 10 pt.	3.95
LT-7	CAPITAL LETTERS HELVETICA 6 pt.	3.95
LT-8	LOWER CASE LETTERS HELVETICA 6 pt.	3.95
LT-9	NUMBERS HELVETICA 6 pt.	4.95
LT-10	DIAL MARKING (DOTS)	4.95
LT-11	DIAL MARKING (LINES)	3.95
LT-12	WORDS (AUDIO) HELVETICA 10 pt.	3.95
LT-12	WORDS (AUDIO) HELVETICA CAPS 6 pt.	3.95
LT-12	WORDS (AUDIO) HELVETICA UPPER AND LOWER CASE 6 pt.	3.95

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SUBSTITUTIONS: We reserve the right to substitute higher quality (but identical part) at our option, unless you specify no substitution at the time of the order.

Component Parts

TRANSISTORS:				
PART NO.	DESCRIPTION	1-9	10-99	100 +
2N3904	NPN T092	.12	.10	.08
2N3906	PNP T092	.12	.10	.08
2N2102	PNP T039	.80	.67	.54
2N4037	PNP T039	.90	.75	.60
PN2219A	NPN T0237	.40	.34	.28
PN2905A	PNP T0237	.40	.34	.28

DIODES:				
PART NO.	DESCRIPTION	1-9	10-99	100 +
1N34A	GE DIODE	.17	.15	.13
1N4001	SI DIODE	.13	.11	.10
1N4148	SI DIODE	.09	.07	.06

LINEAR INTEGRATED CIRCUITS:				
PART NO.	DESCRIPTION	1-9	10-99	100 +
LF351N	SINGLE OP-AMP	.60	.54	.48
LF353N	DUAL OP-AMP	1.05	.95	.84
NE5534N	SINGLE OP-AMP	1.28	1.15	1.02
NE5534AN	LOW NOISE SINGLE OP-AMP	1.80	1.62	1.44
NE5532N	DUAL OP-AMP	1.85	1.67	1.48

I C SOCKETS:				
PART NO.	DESCRIPTION	1-9	10-99	100 +
SOC-8	8 PIN TIN	.11	.10	.09
SOC-14	14 PIN TIN	.12	.11	.10
SOC-16	16 PIN TIN	.13	.12	.11
SOC-18	18 PIN TIN	.15	.14	.13
SOC-20	20 PIN TIN	.19	.16	.15

CARBON FILM RESISTORS:				
PART NO.	DESCRIPTION	1-9	10-99	100 +
CF + VALUE	5 % 1/4W	.05	.02	.01

ALL STANDARD VALUES 1.0 OHM THRU 1.0M OHM

POTENTIOMETERS:				
PART NO.	DESCRIPTION	1-9	10-99	100 +
10KA	10K AUDIO TAPER	2.00	1.80	1.60

CONNECTORS:				
PART NO.	DESCRIPTION	1-9	10-99	100 +
XLR F CA	3 PIN CABLE FEMALE	3.20	2.88	2.56
XLR M CA	3 PIN CABLE MALE	2.75	2.48	2.20
XLR F CH	3 PIN CHASSIS FEMALE	3.60	3.24	2.88
XLR M CH	3 PIN CHASSIS MALE	2.60	2.40	2.08
1/4 ST	1/4" STERIO JACK	.97	.87	.78
3.5 ST	3.5mm STERIO JACK	.97	.87	.78
RCA	RCA PHONO JACK CHASSIS	.65	.59	.52

CAPACITORS: Axial Lead Electrolytic				
PART NO.	DESCRIPTION	1-9	10-99	100 +
AC 1/50	1uf - 50V	.38	.35	.30
AC 4.7/25	4.7uf - 25V	.39	.35	.30
AC 10/25	10uf - 25V	.39	.35	.30
AC 47/25	47uf - 25V	.46	.42	.37
AC 100/25	100uf - 25V	.69	.62	.55
AC 220/35	220uf - 35V	.97	.87	.78
AC 470/35	470uf - 35V	1.34	1.21	1.07
AC 1000/35	1000uf - 35V	2.22	2.00	1.78

CAPACITORS: Radial Lead Electrolytic				
PART NO.	DESCRIPTION	1-9	10-99	100 +
RC 1/50	1uf - 50V	.26	.24	.21
RC 4.7/25	4.7uf - 25V	.28	.26	.23
RC 10/25	10uf - 25V	.31	.28	.25
RC 47/25	47uf - 25V	.39	.35	.28
RC 100/25	100uf - 25V	.41	.36	.33
RC 220/35	220uf - 35V	.61	.55	.49
RC 470/35	470uf - 35V	.99	.90	.80
RC 1000/35	1000uf - 35V	1.27	1.15	1.02

Sheet Metal Punches

MODEL #.	HOLE SIZE	PILOT HOLE	PRICE \$
PUNCH 1	3/8"	ROUND 3/16"	8.95
PUNCH 2	7/16"	ROUND 7/16"	8.95
PUNCH 3	1/2"	ROUND 7/32"	8.95
PUNCH 4	9/16"	ROUND 7/32"	11.95
PUNCH 5	5/8"	ROUND 7/32"	11.95
PUNCH 6	11/16"	ROUND 7/32"	11.95
PUNCH 7	3/4"	ROUND 7/32"	11.95
PUNCH 8	13/16"	ROUND 7/32"	11.95
PUNCH 9	7/8"	ROUND 7/32"	11.95
PUNCH 10	1"	ROUND 5/16"	12.95
PUNCH 11	1-1/16"	ROUND 5/16"	12.95
PUNCH 12	1-1/8"	ROUND 5/16"	12.95
PUNCH 13	1-3/16"	ROUND 5/16"	12.95
PUNCH 14	1-1/4"	ROUND 5/16"	13.95
PUNCH 15	1-3/8"	ROUND 5/16"	13.95
PUNCH 16	1-1/2"	ROUND 5/16"	15.95
PUNCH 17	1-5/8"	ROUND 5/16"	20.95
PUNCH 18	1-3/4"	ROUND 5/16"	23.95
PUNCH 19	2-5/8"	ROUND 1/2"	59.95
PUNCH 20	11/16"	SQUARE 1/2"	31.95
PUNCH 21	3/4"	SQUARE 1/2"	35.95
PUNCH 22	1"	SQUARE 1/2"	45.95
PUNCH 23	21/32 x 5/16"	REC. 1/2"	45.95
*PUNCH 24	*THURST RACES FOR PUNCHES (FOR EASIER PUNCHING) 1" thru 1-3/4"		9.95



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- PC transistor tester
- Phones in the air
- Decadic voltage dividers
- Simple function generator
- Serial video card

Front cover

A consortium of British scientists led by a team from University College London (UCL) has developed a fully automated technique for producing three-dimensional images by computer. The picture shows the consortium leader, Dr Jan-Peter Muller of UCL working on an image of the Big Horn mountain range in central Wyoming, USA. The information originates from a pair of satellite photographs of the area taken from different angles—in this instance by the French satellite "Système pour l'observation de la terre" (SPOT). The new system automatically "matches" easily identifiable features within the picture and, by use of geometry, the heights of these features can be determined. This data can then be used to create a colour image of terrain height (left screen). The system relates patterns of images to produce a three-dimensional representation of the object in question.

Dept. of Photogrammetry and Surveying
UCL
Gower Street
LONDON WC1E 6BT

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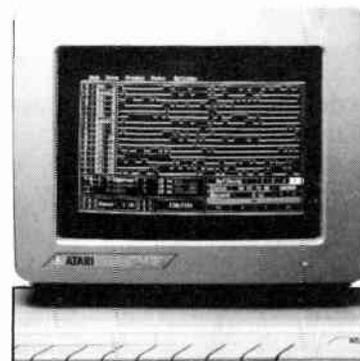
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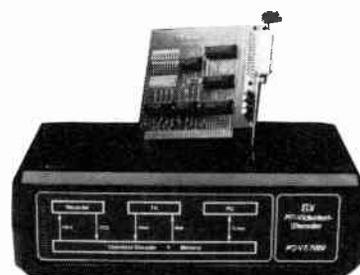
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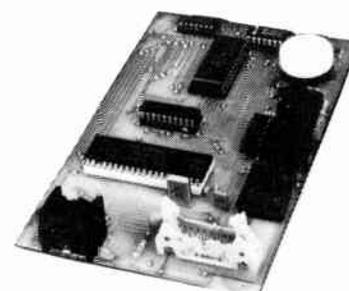
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BULLOCK ON BOXES

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Since 1980, readers of *Speaker Builder* magazine have delighted in the scope and clarity of Bob Bullock's explanations of vented-box loudspeaker systems. Now, for the first time, these articles have been collected into a single invaluable volume: *BULLOCK ON BOXES*.

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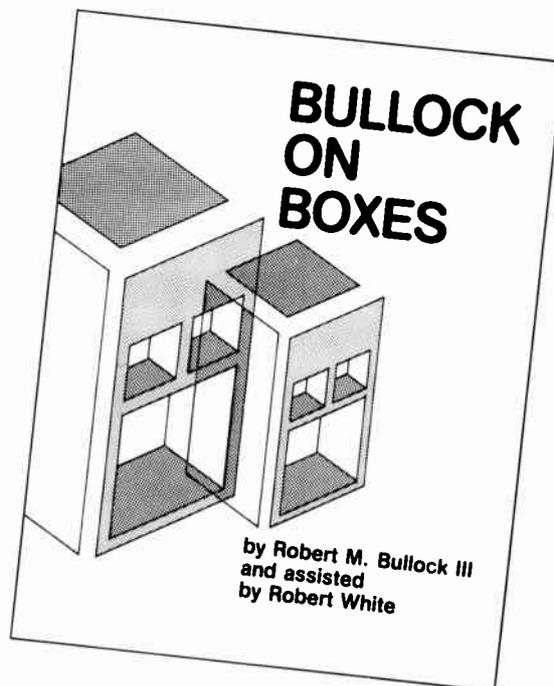
A professor of applied mathematics at Miami University (Ohio) since 1966 and long-time hands-on speaker buff, Dr. Bullock brings an unparalleled range of experience to the pages of *BULLOCK ON BOXES*. Fully indexed and referenced, with glossary, bibliography, and more than 100 illustrations, *BULLOCK ON BOXES* is a practical handbook and lasting reference indispensable to every serious speaker builder. Order yours today!

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[NOTE: In general, BOXRESPONSE automatically generates alignments for a given driver. BOXMODEL does not do this, but instead compares up to four given alignments simultaneously. Both programs display various performance aspects of passive-radiator or vented-box systems.]

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Data Communications



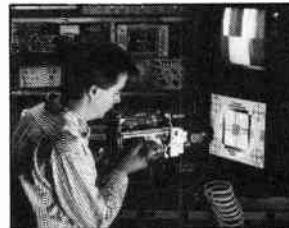
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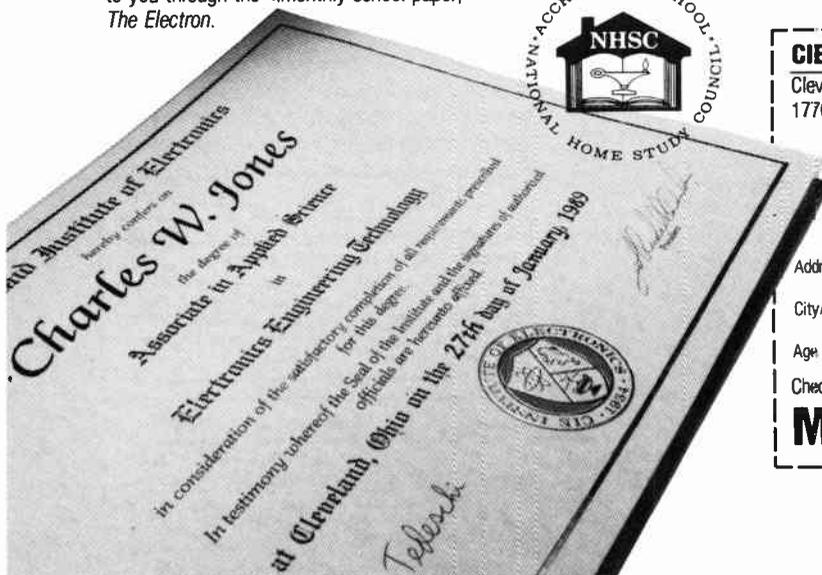
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Speaker Designer™

Release 1.2 by **Stuart E. Bonney**

A loudspeaker system design aid and modeling tool for use with both closed and vented systems over the frequency range from 10 to 300Hz. Computes and displays system frequency response, power handling capabilities, and relative sound pressure level (SPL) outputs for each of 26 discrete frequencies over this range. Includes one year support by the author when the user registers this Shareware product. Each **\$19.50**

IBM 5¼" 360K DS/DD **SPD-1B5**

Loudspeaker Modeling Program by **Ralph Gonzalez** (SB 1, 2, 3/87)

LMP produces a full-range frequency response prediction for multi-way loudspeakers, including the effect of the crossover, driver rollofs, interdriver time delay, "diffraction loss," etc. (Includes author support.) Each **\$17.50**

Specify:

Apple II 5¼" SS/DD **LMP-1A5**
Apple Macintosh 3¼" SS/DD **LMP-2M3G**
IBM PC/XT/AT 5¼" DS/DD **LMP-2B5G**
Commodore 64 5¼" DS/DD **LMP-1C5**

"Souped-Up" LMP provides professional-quality graphics and a fast, friendly, user interface. Remains compatible with LMP data files and is available for IBM PC (CGA, EGA, VGA, or Hercules graphics) and Macintosh computers. The Macintosh version also provides square wave analysis with audible output. Each **\$49.50** (upgrade price: \$39.50*)

Specify:

IBM PC/XT/AT 5¼" DS/DD **LMP-3B5G**
Apple Macintosh 3¼" SS/DD **LMP-3M3G**

*Original LMP disk or sales receipt must be included w/ order.

Driver Evaluation and Crossover Design

by **G. R. Koonce** (SB 5/88)

Disk 1 evaluates the suitability of drivers for closed, vented and passive radiator enclosures, and allows detailed designs of vented boxes.

Disk 2, in addition to driver evaluations, allows the design of first-, second-, and third-order crossovers. 5¼" IBM: 360K, DS/DD. Each **\$12.50**

Specify:

Driver Evaluations **DRI-1B5**
Crossover Design **CRS-1B5**

Active Filter Design

by **Fernando Garcia Viesca** (SB 4/88)

Calculates component values for Butterworth filters in four configurations: High- and low-pass in second- and third-order. (Includes author support.) Each **\$17.50**

IBM 5¼" 360K DS/DD **ACT-1B5**

Two-Way Active Crossover Design by **Gary Galo** (SB 5/88)

Performs the calculations for the eight two-way active crossover designs described by Bob Bullock using formulas exactly as given in the articles; plus a program to calculate V_{TH} . (Includes one year user support.) Each **\$20**

Specify:

IBM 5¼" 360K DS/DD **TWO-1B5**
IBM 3½" 720K DS/DD **TWO-1B3**

Stepped Volume Controls

by **Joseph O'Connell** (TAA 4/88)

These ready-to-run Mac programs come on a 3¼-inch SS/DD disk initialized as a 400K disk for compatibility with all machines. Also included are the Pascal source codes, should you wish to customize them for your own use. Program A. Precisely matches the resistor values to the measured or estimated source and load impedances, yielding great accuracy. Your volume control can have 3 to 99 positions. The program will ask you how many dB each step should be attenuated and has provisions for a standard audio taper or any other taper you devise. Program B. Calculates the taper that will result with your actual resistor values, because you are limited to standard values or with series and parallel combinations. It can also show the effects of different source and load impedances on the taper. Both programs (contained on the same disk) allow you to save their output to a text file and include author support via mail. Each **\$25**

Apple Macintosh 3¼" SS/DD **SVC-1M3**

BOXRESPONSE

Model-based performance data for either closed-box or vented-box loudspeakers with or without a first- or second-order electrical high pass filter as an active equalizer [SB 1/84]. The program disk also contains seven additional programs as follows:

Air Core: This program was written as a quick way of evaluating the resistance effects of different gauge wire on a given value inductor. The basis for the program is an article in *Speaker Builder* (1/83, pp. 13-14) by Max Knittel. The program asks for the inductor value in millihenries (mH) and the gauge wire to be used. (NOTE: only gauges 16-38.)

Series Notch: Developed to study the effects of notch filters in the schematics of some manufacturers. Enter the components of the network in whole numbers (i.e., 10 for 10 μ F and 1.5 for 1.5mH) and indicate whether you want one or two octaves on either side of resonance. Output is frequency, phase angle and dB loss.

Stabilizer 1: Calculates the resistor-capacitor values needed to compensate for a known voice coil inductance and driver DC resistance.

Optimum Box: A quick program based on Thiele/Small to predict the proper vented box size, tuning and -3dB down point. It is based only on small signal parameters, therefore, it is only an estimate of the response at low power (i.e., limited excursion).

Response Function: Calculates the small signal response curve of a given box/driver combination after inputting the free-air resonance of the driver (f_s), the overall "Q" of the driver (Q_{TS}), the equivalent volume of air equal to the suspension (V_{AS}), the box tuning frequency (f_b), and the box volume (V_b). Output is the frequency and relative output at that frequency.

L-Pad Program by Glenn Phillips: Appeared in *Speaker Builder* (2/83, pp. 20-22). It is useful for padding down a tweeter or midrange while still retaining the same load as the driver itself.

Vent Computation by Glenn Phillips: Calculates the needed vent length for 1, 2 or 4 ports of the same diameter. Input box volume in cubic feet and required tuning frequency (f_b), output is vent length and vent area for each case.

Medium: 5¼" SS/DD Disk. Price, **\$25.**

Specify:

BOXRESPONSE

Apple **BOX-1A5**
Commodore 64 (Disk) **BOX-1C5**
Commodore 64 (Cassette) **BOX-3CC**
IBM **BOX-1B5**

IBM Plus Graphics

BOXRESPONSE **BOX-2B5G \$50**

PASSIVE CROSSOVER

This disk is a result of Mr. Bullock's extensive research concerning first-, second-, third-, and fourth-order passive crossovers in *Speaker Builder* 1, 2 & 3/85; **\$25**

Specify:

PASSIVE CROSSOVER CAD

Apple **PAS-1A5**
Commodore 64 (Disk) **PAS-1C5**
IBM **PAS-1B5**

IBM Plus Graphics

CROSSOVER CAD **PAS-2B5G \$50**

CALSOD

Computer-Aided Loudspeaker System Optimization and Design by **Witold Waldman**

CALSOD is a new entry into the field of crossover network optimizing software available for the IBM PC desktop computer. It combines the transfer function of an LC network with the acoustic transfer function of the loudspeaker, by using some form of iterative analysis. CALSOD creates, through the process of trial-and-error curve fitting, a suitable transfer function model which it can then optimize. The program is the subject of CALSOD author Witold Waldman's research paper "Simulation and Optimization of Multiway Loudspeaker Systems Using a Personal Computer" which appeared in the *Audio Engineering Society Journal* for September 1988, pp. 651-663. CALSOD differs considerably from other software since it models the entire loudspeaker output of a multiway system, including the low-end response, and the summed responses of each system driver.

The program performs a lot of tricks. One of the more spectacular of these allows the designer to specify the location of the driver acoustic centers using an XYZ coordinate system. Thus, if the designer ex-

pects to mount a driver combination on a flat baffle, the summed response can be optimized to compensate for rearward displacement of a woofer's acoustic center with respect to a tweeter. CALSOD can model up to seven drivers at a time in a four-way system giving the summed response and acoustic phase response of the entire system.

The CALSOD program comes on a single 360K floppy, and requires one directory and two subdirectories in installation, plus access to the DOS GRAF-TABL file, which it uses for a couple of special symbols. The 133-page User Manual, provided on a second disk, is well written, adequately describes the various program functions, and contains an excellent tutorial example, which demonstrates the use of the program.

Specify:

IBM 5¼" 360K DEMO . . . **CAL-2B6D \$ 5.00***
IBM 2 x 5¼" 360K DS/DD . . . **CAL-2B6 \$65.00**
IBM 3½" 720K DS/OD . . . **CAL-2B4 \$67.50**

* Usable as credit toward later purchase of full CALSOD.

NOTE: OLD COLONY SOFTWARE SHOWN ON THIS PAGE IS NOT RETURNABLE FOR REFUND OR CREDIT. ALSO, BECAUSE OF UNREASONABLE TAXATION REQUIREMENTS BY THEIR STATE, WE REGRETFULLY ARE UNABLE TO SELL SOFTWARE TO RESIDENTS OF CONNECTICUT.

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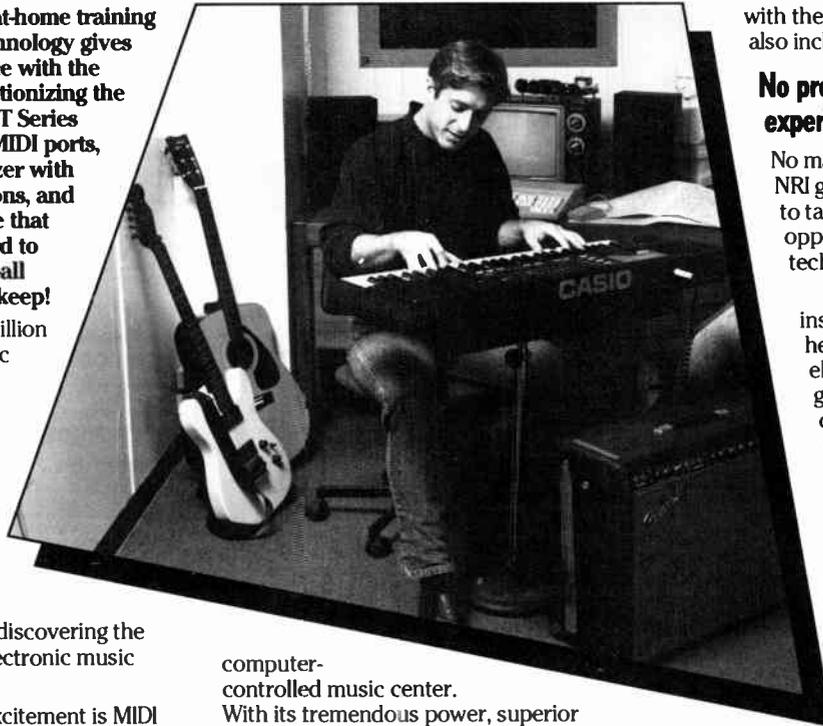
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VIDEO/AUDIO SURROUND SOUND PROCESSOR

SM-333 ▲▲▲★

It has inputs for VCR, Video Disc and Compact Disc and can also be used with FM tuners, tape decks and LP discs - in fact anything that can be connected to your pre-amplifier. It also has front panel control of dynamic noise reduction DNR, surround level, effect and time delay up to 50 milliseconds. Rear panel outputs for front and rear stereo speaker amplifiers. The unit may be purchased as a kit or fully assembled ready to plug in.

SPECIFICATIONS

Frequency response 20 Hz to 20KHz • Total harmonic distortion Front channel 0.05% • Rear channel Less than 0.25% • Input signal voltage 0.1 to 3.5V • Output Front channel 0.1 to 3.5V • Rear channel 6.6V • Delay time 5 to 50 milliseconds • Input impedance 47 K • Power requirements 100-120 VAC 60 Hz • Dimensions 14.2" wide 4.82" deep 2.1" high
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Complete Kit: \$65.00
Assembled & Tested: \$75.00

60W + 60W Stereo Power Amplifier (with Mic. input)

SM-302 ▲▲★

The SM-302 is a fully self-contained power amplifier. It is designed to be used with a wide variety of preamplifiers and the exciting Mark V surround sound processor. Assembly is greatly facilitated because all components mount directly on the printed circuit board and interconnect wires are held to a minimum. Added benefits: hiss/hum noise and distortion are also minimized. The SM-302 provides three input jack pairs. One pair will accept a high impedance microphone. The two remaining pairs are for high level and low level input sources. These input jacks are selected by a panel mounted side switch.

SPECIFICATIONS

Frequency response 20Hz to 20 KHz • Total harmonic distortion < 0.1% • Power output 60W per channel into 8 ohm load • 33W per channel into 16 ohm load • Input sensitivity Mic 10mv • Lo 3800mv • Hi 640 mv • Signal to noise ratio Better than 70 db • Power consumption 100W • Dimension 360 mm x 75 mm x 200 mm



Complete Kit: \$67.00
Assembled & Tested: \$78.00

Universal Audio/Video KARAOKE Mixer Pre-Amp.

SM-888 ★

The SM-888 is smartly styled and has a variety of functions such as echo mode, echo depth and a graphic equalizer to suit various environmental and individual tastes. The graphic equalizer is very effective to create a more lively effect. SM-888 features include two microphone jacks for mixing, LD (laser disk) and VCR connection terminals, built in phone pre-amp and tape recorder jacks and all the facilities you need for live recording. An integral signal amplifier allows sources with varying signal levels to be controlled for best results. Additional connections are provided for CD (compact disc) and FM tuner inputs.

SPECIFICATIONS

Frequency Response 20Hz to 20KHz • T H D < 0.01% from 20 Hz to 20 KHz • Input Sensitivity 3 mv rms • Input impedance 47 K • AV (audio) 300 mv at 47 K • AV (video) direct connection • FM tuner 300 mv at 47 K • CD 300mv at 47 K • AUX 300 mv at 47 K • MIC 3mv at 600ohms Useable 300 ohms to 47 K • Line output 10 to 15 v with 300mv input Equalization 100 Hz • 10 db 250 Hz • 10 db 1 KHz • 10 db 10 KHz • 10 db • Echo delay time 62 to 220 ms • Power Requirements 110/220 VAC 50/60 Hz • Power consumption 28 W • Dimensions 17" W x 2-1/2" H x 7-7/8" D 432 mm x 64 mm x 200 mm



Assembled & Tested: \$225.00

100W + 100W NEW CLASS A DC STEREO PRE AND MAIN AMPLIFIER TA-1500 ▲▲▲▲

The TA-1500 is a fully integrated stereo amplifier including a preamplifier. It has inputs for magnetic phono tuner, aux mic and tape in/out. Controls include volume, balance, mic gain, bass, treble and mid-band tone controls and input selector. It is also possible to connect an external separate pre-amplifier. Other features are fully complementary DC coupled circuitry with fast acting speaker protection relay. Power supply components are included on the printed circuit board and requires only the addition of an external transformer. The Mark V model 001 is a suitable transformer.

SPECIFICATIONS

Power output 80 watts per channel into 8 ohms 100 watts per channel into 4 ohms • Total harmonic distortion Less than 0.03% • Frequency response Aux input 5 to 50000 Hz ± 0.2db • 2db • Frequency response Power amplifier section DC to 200 KHz • Sensitivity Phono 2.5 mV @ 47 K Preamp 150 mV @ 47 K Mic 6 mV @ 10 K Output Tape 150 mV @ 47 K Preamp 1V @ 600 ohms • Power transformer 26 V to 32 V AC • 2 @ 6 A (Mark V Model 001) • P.C. Board Dimensions 10.5" x 6.13" x 2.25" • Heat sink 5.13" x 2.63" x 3" (Each) Use rack mount cabinet LG 1924 or LG 1925

Complete Kit: \$73.70
Assembled & Tested: \$95.81

300 W HI-FI POWER AMPLIFIER (MONO)

TA-3600 ▲▲▲▲

The TA-3600 is an extremely high power amplifier specifically designed to reproduce the high dynamic range available on compact discs.

It has low noise, high stability, low distortion, extended frequency range and high efficiency in a compact package. Two of these units with appropriate power supply and pre-amplifier are required for stereo reproduction.

SPECIFICATIONS

Power output 300 watts sine wave into 8 ohms 540 watts music power into 8 ohms • Frequency response 10Hz to 20 KHz • Total harmonic distortion Less than 0.05% • Intermodulation distortion Less than 0.05% • Sensitivity 1 V ms at 47K • Power requirements 60 to 75 VDC at 8 amp • Dimensions 8" x 7 1/2" x 2 1/2"



Complete Kit: \$85.00
Assembled & Tested: \$110.00
Transformer: \$43.00

80W + 80W PURE DC STEREO MAIN POWER AMPLIFIER

TA-802 ▲▲▲

Modern circuit design utilizes full complementary power output and differential cascode input stage. DC coupling provides superb transient response. A special output circuit guards against short circuits and overload operation.

SPECIFICATIONS

Power output 80 watts per channel into 8 ohms Total harmonic distortion Less than 0.05% at rated power Intermodulation distortion Less than 0.05% at rated power Frequency response DC to 200 KHz -0db -3db @ 1 watt Power requirements 30 VAC x 2 @ 6 amp May use Mark V model 001 transformer P.C. Board 8-1/2" x 5" x 1-1/8" Heat sink 5-1/8" x 2-5/8" x 3" (Each)



Complete Kit: \$45.94
Assembled & Tested: \$59.72

120W MOSFET POWER AMPLIFIER (MONO)

TA-477 ▲▲▲

This amplifier is designed specifically for low TIM distortion. It uses parallel MOSFET output transistors. This is a very popular kit because of its superior sound reproducing ability and high power reserve. BUILD TWO KITS FOR A PROFESSIONAL STEREO AMP!

SPECIFICATIONS

T H D Less Than 0.007% • Power output 120 watts into 8 ohms • Frequency response 8 Hz to 20KHz ±0.0-1db • Sensitivity 1V • Power requirements 55 VDC @ 3 amps May use Mark V Model 003 Transformer



Complete Kit: \$68.00
Assembled & Tested: \$85.00

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AMPLIFIERS		KIT	ASSEMB.
MODEL	DESCRIPTION		
TA-28MK2	Digital Voice Memo ▲▲	\$ 30.00	
TA-50A / B	Multi-Purpose Melody Generator ▲	12.84	\$ 17.20
TA-50C	Multi-Purpose Melody Generator ▲	13.65	18.71
TA-120MK2	35W Class 'A' Main Power Mono Amp ▲▲	31.50	42.80
TA-300	30W Multi-Purpose Single Channel Amp ▲	20.00	29.00
SM-302	60W + 60W Stereo Power Amplifier (with Mic. input) ▲▲★	67.00	78.00
TA-323A	30W X 2 Stereo Pre-main Amp ▲	31.50	42.80
TA-377A	Hi-Quality FET Stereo Pre-Amp ▲▲▲	59.95	75.00
TA-400	40W Solid State Mono Amp ▲	28.00	34.93
TA-477	120W Mosfet Power Mono Amp ▲▲▲	68.00	85.00
TA-800MK2	120W + 120W low Tim Pre-Main Stereo Power Amp ▲▲	63.92	
TA-802	80W + 80W DC Stereo Main Power Amp ▲▲	45.94	59.72
TA-820A	60W + 60W OCL DC Pre-Main Stereo Amp ▲▲	40.39	49.37
TA-1000A	100W Dynamic Class 'A' Main Power Mono Amp ▲▲	59.69	80.58
TA-1500	100W X 2 Class 'A' DC Stereo Pre-Main Amp ▲▲▲	73.70	95.81
TA-2200	Fet Super Class 'A' DC Pre-Amp ▲▲▲	47.70	58.24
TA-2400A	Electronic Echo & Reverberation Amp ★		96.00
TA-2500	HQ Pre-Amp w/10 band graphic equalizer ★		68.80
TA-2800	HI-FET IC Pre-Amp w/3 way tone control ▲	48.90	63.57
TA-3000	Stereo Simulator (For Mono TV or Any Mono Source) ▲▲	27.00	38.50
TA-3600	300W HQ Hi-Fi Power Mono Amp ▲▲▲	85.00	110.00
POWER SUPPLIES		KIT	ASSEMB.
TR-100A	0-15V 2A Regulated DC Power Supply (w/Case) ★		\$ 69.50
TR-355A	0-15V 5A Regulated DC Power Supply ▲	\$ 15.65	21.76
TR-355B	0-30V 3A Regulated DC Power Supply ▲	15.65	21.76
TR-503	0-50V 3A Regulated DC Power Supply ▲▲	16.75	23.65
INSTRUMENTS		KIT	ASSEMB.
SM-43	3" Multi-Functional Led D P M (w/ABS plastic case) ▲▲	\$ 34.50	\$ 43.00
SM-48	4" Hi-Precision D P M ▲▲▲	38.00	48.00
SM-48A	4" Hi-Precision D P M (w/ABS plastic case) ▲▲▲	41.20	52.00
SM-49	3" Multi-Functional LCD D M P (w/Hold Function) ▲▲	36.00	44.50
SM-100	150MC Digital Frequency Counter ▲▲▲	79.00	90.00
FC-1000A	1 GHz Frequency Counter ★		179.00

* Free gift for any purchase before April.

MISCELLANEOUS		KIT	ASSEMB.
MODEL	DESCRIPTION		
TY-238	3 Channel Color Light Controller ★		\$ 65.00
TY-25	Stereo Loudspeaker Protector ▲	\$ 14.85	20.85
TY-35	FM Wireless Microphone ▲	11.25	
TY-36	AC/DC Quartz Digital Clock ▲	19.00	26.20
TY-38	Sound / Touch Control Switch ▲	12.00	
TY-41MK V	Infrared Remote Control Unit (w/Case) ▲▲▲	22.00	35.00
TY-42	Bar / Dot Level Meter ▲▲	24.15	33.81
TY-43	3 1/2" Digital Panel Meter ▲	29.00	38.00
TY-45	20 Steps Bar / Dot Audio Level Display ▲▲	38.45	46.14
TY-47	Superior Electronic Roulette ▲▲	19.46	27.24
SM-222	7 Band Hi-Fi Graphic Equalizer ▲▲▲	26.80	38.80
SM-328	4 Channel Professional Color Light Controller ★		145.00
SM-333	Audio/Video Surround Sound Processor ▲▲▲★	65.00	75.00
SM-666	Dynamic Noise Reduction ▲	26.00	34.00
SM-888	Universal Audio/Video KARAOKE Mixer Pre-Amp ★		225.00
10 000uF	80 V Capacitor (Suggested for TA-3600 TA-477 TA-1000A TA-820A)		23.00
METAL CABINETS WITH ALUMINUM PANEL		KIT	ASSEMB.
MODEL	H" x W" x D" MATCHING		PRICE
LG-1273	3" 12" 7" TA-2800 TA-377A TA-2200		\$ 22.85
LG-1684	4" 16" 8" TA-323A TA-377A TA-2200		\$ 27.50
LG-1924	4" 19" 11" TA-802 TA-820A TA-1500 TA120MK 2 TA-800 TA-1000A		32.80
LG-1925	5" 19" 11" TA-477 TA-800MK2 TA-1500 TA-1000A TA-3600		35.80
LG-1983	2 1/2" 19" 8" TA-377A TA-2800 TA-2200 TA-120MK 2		29.25
POWER TRANSFORMERS		KIT	ASSEMB.
MODEL	DESCRIPTION	MATCHING	PRICE
001	28V x 2 6A to 30V x 2 6A	TA-800MK2 TA-802 TA-820A TA-1000A TA-1500	\$ 27.00
002	36V x 2 3A	TR-503 TA-323A TA-400 TA-300	22.00
003	40V x 2 6A	TA-477	28.00
004	24V x 2 6A	TA-120 MK 2	22.00
005	26V x 2 3A	TR-355B	16.00
006	18V x 2 5A	TR-355A	15.50
007	53V x 2 8A	TA-3600	43.00

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range



The MDM 85 is a mid range 75mm soft dome unit of extremely high standard, both from a design and technical viewpoint.

It incorporates the renowned Morel double magnet and Hexatech voice coil techniques, and results in a unit of above average sensitivity with extremely low distortion and high power handling capability.

With an output level of 96dB distortion in the area of 400-800Hz is slightly over 1% falling to 0.015% from 1Khz.

There are two different types available, one with a rear enclosure and one without (MDM 85NE). The type with the rear enclosure can be fitted into a cabinet as an integral unit.

The MDM 85NE without the rear enclosure can only be fitted into a system having a separate housing to enclose the unit. A volume of 0.7 litre is recommended for this housing, which is essential to prevent interaction with the bass unit compressions and expansions. This housing must be filled full with damping material, such as fibreglass or rock wool.

The Thiele small parameters are given for both types under specifications. The contribution of this unit to a suitably designed system will be evident in the clarity and detail given in the 500-5000Hz region.

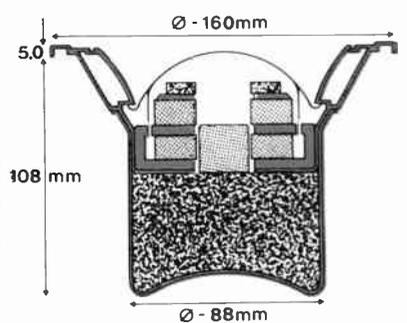
Specification

MDM 85 (with enclosure)

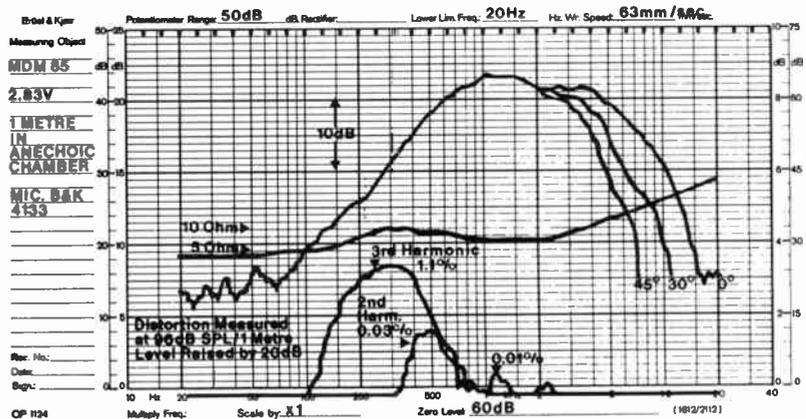
Overall Dimensions	Ø - 160mm x 113mm
Nominal Power Handling Din	300W
Transient Power 10ms	1500W
Voice Coil Diameter	75mm (3")
	Hexatech Aluminium
Voice Coil Former	Aluminium
Frequency Response	300-5000 Hz
Resonant Frequency	250 Hz
Sensitivity	92 dB (1W/1M)
Nominal Impedance	8 ohms
Harmonic Distortion for 96 dB SPL	<1%
Intermodulation Distortion for 96 dB SPL	<0.25%
Voice Coil Inductance @ 1 KHz	0.2mh
Air Gap Width	1.05mm
Air Gap Height	3.0mm
Voice Coil Height	6.0mm
Flux Density	1.0T
Force Factor (BXL)	4.6 W8/M
Rdc	5.2 ohms
Rmec	37.90
Qms	0.29
Qes	2.66
Q/T	0.20
Vas	0.33 litre
Moving Mass including Air Load	7.0 grams
Effective Dome Area	63.50 cm ²
Dome Material	Chemically Treated Fabric
Nett Weight	1.25 kg

Variations to specification for MDM 85NE (without enclosure)

Overall Dimensions	Ø - 160mm x 60mm
Frequency Response	250-5000 Hz
Resonant Frequency	170 Hz
Rmec	39.33
Qms	0.19
Qes	1.81
Q/T	0.17
Vas	0.7 litre
Nett Weight	1.05 kg



Specifications given are as after 24 hours of running.



morel (U.K.) Ltd.

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Nacton Rd. (Ransomes)
Industrial Estate,
Ipswich, IP3 9RT
England
Tel: (0473) 719212
Telex: 987601 Morel G.

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The compact discs in this copiously documented set are unique. For the first time, they offer the consumer a tool for verifying the qualities and defects of a given CD player, with no required measuring equipment or in-depth technical knowledge. However, they have been shown to yield startling performance demonstrations even under the strictest of laboratory conditions.

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FORGING FIBER LINKS

The old saying about advancing two steps forward and one step back has never been more aptly applied than in describing the introduction of Information Technology (IT) to the intelligent building.

During the early 1980s, many large companies, eager to take advantage of the advances in computer technology, installed shiny new copper cabling systems to link their PCs and terminals with the corporate mainframe. The popular concept of a PC or a terminal for everyone soon followed. Cabling systems designed as the absolute answer to the needs of their day eventually had to be extended to meet the rapid growth in demand for computer access. At the same time, communications technology was developing toward the advent of the local area network, then toward the wide area network—additional ways of making more efficient collective use of processing power.

All these IT innovations offered dramatic improvements in operating efficiencies for the corporate user, but all carried with them a severe penalty. Additional cabling on a grand scale was required to link these elements of IT with one another. Many buildings began to groan under the strain.

Ducts and trunking became overloaded, buildings had to be restructured to accommodate the ever-growing demands for more and more cable links. What were thought to be definitive cabling systems became redundant when major staff re-grouping was required. Nobody knew which cables went where. Rather than try to use the considerable *in situ* capital investment—far from being written down in value—and find out what connected to what and if it would cope, it was easier to install new cables and make new connections.

Meanwhile, another force was conspiring to influence the demands of IT. The software industry was developing and improving its applications. A new level of sophistication was reached with CAD/CAM, CIM, and DTP and the birth of the workstation to handle them. Software became more user-friendly. At the same time, these innovations consumed vast amounts of processor memory and imposed further demands on data communications provision.

Optical fiber data links were always available as an alternative to overfilled ducts and high data rates, but the average user had no need of such a vast signal carrying capacity. The slightly increased cost of fiber, coupled with a fear of what was perceived as new technology, deterred all but the most far-sighted and those with the highest population of terminals. Today, the scene has changed and most new premises built for housing knowledge

workers have at least a fiber backbone with probably one or two spurs of fiber linking the distant users with the mainframe or the data switch. The situation has progressed with fiber carrying all the heavy traffic and copper linking the majority of the individual users.

New buildings have always been easier to deal with in terms of cabling. Today, the exercise has been further simplified by a major rationalization of building communications requirements. This has been achieved through the introduction of integrated cabling systems designed to handle telecommunications and data. The advantages of an integrated cabling system are the variety of communication protocols it can serve and its flexibility to allow moves and changes after installation.

Probably the most interesting of the integrated cabling systems is AT&T's Systimax™ Premises Distributions Systems or PDS. Over 4,000 PDS installations exist in the US and more than one hundred in the UK. The system was introduced in 1984 in the US where about 50% of all data cables within new office buildings are part of structured cabling systems. In the UK the present volume is around 15% but rising fast. A very high penetration is likely for larger installations.

For voice and the less demanding terminals, twisted copper pairs will remain satisfactory for the time being. PDS is capable of handling numerous protocols through the use of baluns, and it uses the same cables, plugs, and adaptors for voice and data. Simple dual wall socket outlets marked with symbols denoting telephone or data use are provided. Changing office layout or type of service required at the desk is carried out quickly and easily. Telephones and terminals can be moved from one office to another with little disruption and expense. Unlike previous all-copper cable systems, PDS accommodates simple upgrade paths in line with most future needs. However, for real future proofing, the only solution is to run fiber to the desk, a decision some major institutions are already implementing.

By the end of the century, optical fiber is expected to become the dominant medium for data communication. Today, an optical fiber system offers a better life expectancy than any other part of IT. In the meantime, copper cable is far from becoming redundant. Peaceful coexistence between the two is the new way—each fulfilling its own specific function and combining to form a highly efficient blend of technologies.

When configured as a backbone infrastructure and especially when taken to every desk, optical fiber represents true technological future proofing.

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ECONOMICAL 8-CHANNEL VHF TWO-WAY MOBILE

Midland LMR has introduced a compact 8-channel programmable wideband two-way FM mobile radio. For VHF use, the 70-1336 offers adjustable output power of 15-30W and covers a 24MHz frequency range (136-150MHz or 150-174MHz) at rated specifications, without retuning. This PLL frequency-synthesized mobile has built-in tone- and digital-coded squelch (CTCSS/DCS), randomly programmable by channel in any combination. It features a die-cast chassis and, with a bracket support on the mount, meets or exceeds MIL Standard 810C/D for shock and vibration.

The mobile measures 2" x 7" x 8 7/8". Options include priority scanning of 40 channels per second, a slide rail mounting kit, a



DTMF decoder, and a DTMF encoder microphone with ANI.

For additional information, contact Midland LMR, Marketing Dept., 1690 N. Topping, Kansas City, MO 64120, (800) 643-5263, ext. 1690.

LOGIC CONTROLLER CONTROLS SOLENOIDS

Electronically controlling machinery, equipment, and instruments using pneumatic or hydraulic solenoids is now easier, thanks to a programmable logic controller from BASICON. The Single Board Controller's 7" x 9" size and low power requirement (1W at 24V) allow for a sealable, non-vented enclosure, protecting the system from harsh industrial and commercial applications.

During beta-testing, the SBC-64A was used to control machine tools, carton folders, camera motion and lens zooming, and audio/visual mixing. Because of its convenience and accuracy, the built-in floating point arithmetic enabled the unit to position commercial satellite receiving antennae.

Compared to other Ladder Logic Controllers, the SBC-64A provides greater flexibility with its built-in Basic language. The system can be programmed with either a sim-

ELECTRONICS SCENE

A COMPUTER-SIMULATED ELECTRONICS LABORATORY

Global Specialties has announced PROTO-LAB, a computer-simulated electronics laboratory for building and testing circuits. Included is an instructional experiment workbook. Together, program and workbook help you discover fundamental electronic design principles. The lab comes with voltmeter, ammeter, dual-trace oscilloscope, ohmmeter, wattmeter, and sweep generator. Protolab is also stocked with resistors, capacitors, inductors, current sources, and AC and DC voltage sources.

Each experiment is conducted on the simulated Protoboard breadboard. You construct operating circuits by placing the components with a mouse, and you use the test instruments to probe the circuit's operation. Voltages and currents can be measured on the meters and waveforms on the dual trace oscilloscope.

Protolab was designed to operate on IBM PCs (PC, XT, AT, 286, and 386) or Macintoshes (MAC512E, MACXL, MAC Plus, MAC SE, and MAC II). The PC version requires a mouse, mouse driver, 384K RAM, and CGA (640 x 200) video, but not a hard drive.

The PROTOLAB packages are priced at \$99.95 (PC) and \$129.95 (Macintosh). To order or for more information, contact Global Specialties, 70 Fulton Terrace, New Haven, CT 06512, (203) 624-3103, FAX (203) 648-0060.

ple terminal or with an MS-DOS based PC.

The SBC-64A system provides 32 opto-isolated inputs and 32 open collector outputs, all marked with LEDs for visual confirmation of operation. It has RS-232/422/485 for program development and machine-to-machine or host communication. The system can be expanded with more memory, A/D and D/A connections, clock/calendar, digital I/O, keyboard, and display. For easy troubleshooting and maintenance, the SBC-64A is equipped with quick connect, industrial grade screw terminals. After the operational logic has been programmed and tested, the program can then be moved to the built-in EEPROM, where subsequent power-up automatically runs it.

For further information, contact BASICON at 14273 N.W. Science Park Dr., Portland, OR 97229, (503) 626-1012.

WorldRadioHistory

68000 TRAINING SYSTEM

Intelligent Systems Solutions Corp. has introduced a 68000-based microprocessor training system. It consists of a 68008 microprocessor, two serial ports, a timer/counter/square wave generator, a built-in logic probe, a dual speed 8/2MHz clock, 64K static RAM (32K battery backed up), and 32K EPROM. Two slots are available for wirewrap experiments or for system expansion. Also, the trainer has a removable breadboard with access to the system's signals.



The trainer has a debugger with commands to deposit, examine, download, and upload programs, and it can execute a single instruction or subroutine. The debugger allows seven permanent breakpoints and a temporary one. The system's disassembler shows how the condition codes are affected, and it shows the privilege level, as well as the instruction itself. You can use either serial port to interface with the trainer.

The suggested retail price is \$749. Contact I.S.S.C. at 6521 S. Terrace, Tempe, AZ 85283, (602) 829-6503.

FIELD SERVICE PARTS TESTER

B&K Precision is offering a new hand-held parts tester with digital readout, designed for field service of general industry applications. The Model 815 tests capacitance from 0.1pF to 20μF in capacitors, switches, and other components with an accuracy of 0.75% to 1.5%. Resistance measurement spans from 0.1Ω to 20MΩ. Transistors are tested by measuring h_{FE} values (gain) and I_{CEO} (leakage). SCRs, diodes, and LEDs are tested for forward junction voltage. Batteries are tested under load for voltage output.

The 815 can withstand damage from a 5-foot fall, from overloads, and from water. Also, its case seals out grease, dirt, and other contaminants. Other features include a 3½ digit 0.8" LCD readout, tilt stand for bench use, test leads, and component insertion sockets.

To receive more information, contact B&K Precision, Maxtec International Corp., 6470 W. Cortland St., Chicago, IL 60635, (312) 889-9087.

ELECTROFORMER SERIES OF BALANCED I/O DEVICES

The EF201 and EF202 from Audio Teknology are high performance input (FT202) and output (FT201) devices providing true equivalent transformer balancing action, along with lower distortion and wider bandwidth than actual I/O transformers. Both devices provide high common mode rejection ratios at least equal to those of audio quality transformers, and the EF201 maintains rejection during clipping overloads. The devices use a Dielectric isolated (Di) process developed specifically for high performance audio applications. This process enables discrete quality audio transistors of matched NPN and PNP types to be fabricated on a monolithic structure.

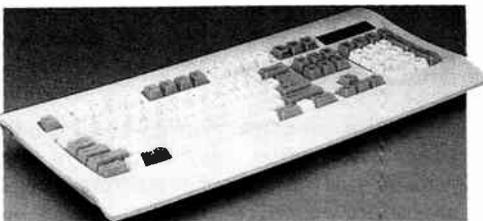
To receive further information, contact Audio Teknology, Inc., 7558 S.W. Bridgeport Rd., Portland, OR 97224, (503) 624-0405, FAX (503) 624-0194.

FIRST IN THE IOcomm LINE OF COLOR MONITORS

The CM-4210, a 1,024 x 768, .28 dot pitch color monitor from IOcomm, produces picture stability and clarity by working like a fixed-frequency machine. But it still scans three main frequencies for compatibility.

The CM-4210 comes with 6-foot cables and has ergonomic control placement, extra-wide system ventilation, and power supplies that take anything from 88-264V AC. The monitor is upwardly compatible from VGA to 800 x 600 to 1,024 x 768. Its tilt-and-swivel base moves with ease. The monitor has a track failure rate of a fraction of 1%, well below the industry's standard of 2%, and it meets or exceeds US DHHS standards, as well as the German TUV.

Having a maximum resolution of 1,280 x 1,024, with 17 diagonal inches, the CM-8720 takes care of full- and split-screen displays, CAD, multitasking, and windows. IOcomm offers support programs ranging from direct RMA handling to insured warranties.



IOcomm also manufactures the IO-101 WC keyboard. Its rolling surface provides a place to rest your palms to aid in typing comfort.

For further information, contact IOcomm, 12700 Yukon Ave., Hawthorne, CA 90250, (213) 644-6100, FAX (213) 644-6068.

ELECTRONICS SCENE

NEUTRIK GETS THE MESSAGE ACROSS

Neutrik USA has introduced three models of its Infomatic digital recording and announcing system (the 4000 System, the Compact, and the Mini). Designed for recording, storing, and replaying digitally stored sound, the microprocessor-based system is ideal for use in airports, museums, police departments, and railroad stations, where high-fidelity reproduction of sound is required.

The 4000 System is expandable to a playing time of 68 minutes and can store up to 256 messages. With 32 playback channels, the Infomatic 4000 can provide service for 32 customers at once. An optional interface makes the unit keypad interactive with the message recipient. The 4000 features a 100 telephone line capacity; three bandwidths (3.5, 7, and 14kHz); optional disk drive; and SRAM, DRAM, or EPROM. Use with other Infomatic systems allows for unlimited channel availability.

The Compact is a recording/playback/memory system. This model comes with an internal voltage regulator and connections for playback, remote, and record. Its internal memory can be SRAM (64 sec.), EPROM, or DRAM (128 sec.).

The Mini is a digital playback unit, complete with a DC power supply. It features 32 seconds of playing time, output to telephone or loudspeaker, PAXB compatibility, and EPROM memory.

Neutrik offers a free Infomatic system configuration on request. For more information, contact them at 195-S3 Lehigh Ave., Lakewood, NJ 08701, (908) 901-9488.

SUPPORT FOR MULTIVENDOR STANDARD ON THE PC BUS

National Instruments, Data Translation, Strawberry Tree, Analogic, Sciteq, Guide Technology, Computer Boards, and Rapid Systems have announced their support for PCXI, a multivendor standard on the PC bus. Designed by Rapid Systems to satisfy the need for a modular instrumentation, data acquisition, and control standard on the PC bus, PCXI accommodates hundreds of PC cards within one specification.

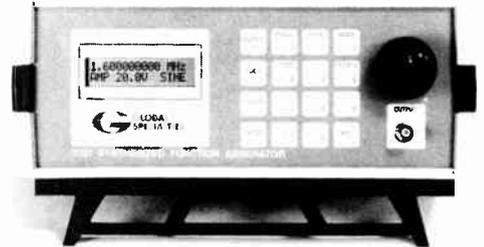
The PCXI standard establishes the basis for the first generation of low-cost automated test systems—based on the PC, software standards, and card instruments. PCXI specification allows for a wide range of test system configurations, from a small, portable system with few instruments to a large ATE system with numerous devices.

PCXI is module based. The instrument-on-

WorldRadioHistory

2003 SYNTHESIZED FUNCTION GENERATOR

Global Specialties announces the 2003, a synthesized function generator. The 2003 has a frequency range of DC to 1.6MHz, with sine, square, triangle, and ramp outputs. Up to 16 preset frequencies can be programmed into memory and sequenced in the "frequency hop" mode, making the unit ideal for repetitive test applications, such as amplifier performance checks or production environments. Tone bursts can be generated using the external trigger/gate feature, and internal linear/log sweep is available across the entire frequency range.



The 2003 has a 32-character two-line LCD display and a keyboard and rotary encoder for selecting functions and tuning frequencies. The rotary encoder allows analog style tuning; the keyboard provides direct access and mode selection. An optional RS-485 serial interface lets you set functions from a PC. Multiple generators can operate on a single loop, each with its own address, making the unit ideal for automated testing applications. The digitally controlled output is 20V p-p into an open circuit, 10V p-p in 50Ω, with DC offset adjustments.

Contact Global Specialties, 70 Fulton Terrace, New Haven, CT 06512, (203) 624-3103, FAX (203) 468-0060.

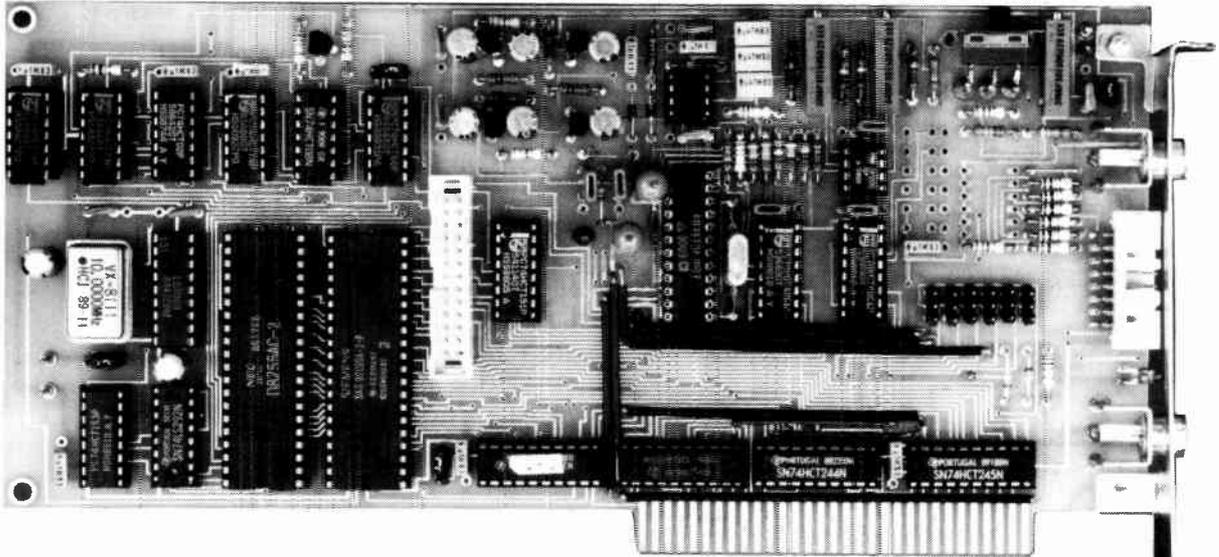
a-card modules slide into the passive backplane and are interchangeable with any PC card manufactured according to the Industry Standard Architecture (ISA). The modules' 1.2" slot spacing provides shielding of the PC card and space for large components.

A typical PCXI test system consists of a power supply module, a CPU module, and a video module, plus as many instrument-on-a-card modules as the application requires. PCXI is upward compatible to 386/486 architecture. Also, additional memory, disk storage devices, IEEE 488 interfaces, printers, plotters, and modems (phone/fax) can extend its ATE capabilities.

For more information, contact Tom Bardeen, President, Rapid Systems, 433 N. 34th St., Seattle, WA 98103, (206) 547-8311, FAX (206) 548-0322.

MULTIFUNCTION MEASUREMENT CARD FOR PCs

PART 1: DESIGN BACKGROUND AND CIRCUIT DESCRIPTION



The high-performance insertion card described in this article allows your IBM PC-XT, PC-AT or 100% compatible to measure direct voltage at 12-bit accuracy, as well as frequency and a host of other parameters related to pulse-shaped signals. The accuracy and versatility afforded by the card are of a level associated with much more expensive, industrially rated products. The menu-driven control software developed for this exciting project allows you to keep tabs on up to eight voltages quasi-simultaneously, while up to eight remaining inputs can be used for time-related measurements including frequency, duty factor and pulse duration, not forgetting the event counter. Connected to the sensors and timing devices of your choice, this card turns a PC into a powerful central controller in a complex measurement and control system.

J. Ruffell

ALTHOUGH its ability to deal with numbers is often the main reason for using a PC, it is interesting as well to look at interfacing such a machine to the real world, which, as most of us see it, is analogue rather than digital. Invariably, a PC needs to be fitted with a special interface card to allow it to handle analogue quantities such as voltage, temperature, pressure, or relative humidity. The card described in this article is such an interface. Effectively, it turns your PC into a multifunction measurement station.

The analogue-to-digital conversion func-

tion of the card allows analogue quantities in the form of voltages to be translated into their digital equivalents, which are numbers that can be processed and evaluated by the PC. Two inputs are available for this purpose, each fitted with an eight-channel multiplexer for multi-point measurements. The software allows one of these channels to be selected for accurate monitoring and analysis. In addition to this versatile voltmeter function, the card can also function as a frequency meter combined with a pulse/pause (duty factor), a pulse-on/off time meter, and an event counter.

Block diagram

The block diagram in Fig. 1 shows the general structure of the measurement card. A number of buffers and an address decoder are connected between the PC expansion bus on the one hand, and two programmable peripheral interfaces (PPIs) and one analogue-to-digital converter (ADC), on the other. The PPIs take care of the communication between the PC and a number of lines of the ADC (which functions as a voltmeter) as well as the communication with the ICs that form the frequency meter.

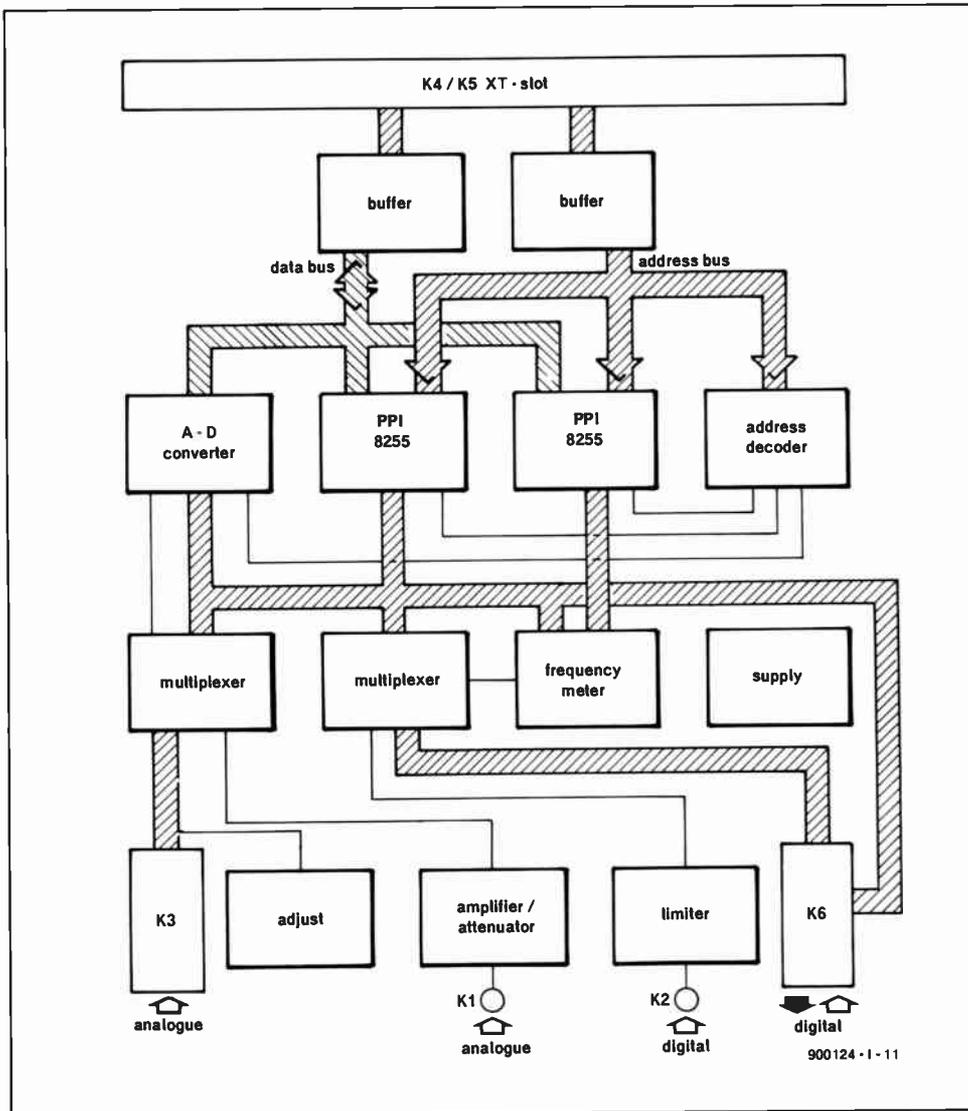


Fig. 1. Block diagram of the PC measurement card, showing the general structure of the design and the main buses used for data and control signals.

The bus interface merits a few words only, since it has been used in previously published circuits in this magazine. The address and data buffers ensure that the loading of the relevant PC bus lines is kept to a minimum. The buffers are followed by an address decoder formed by a programmable array logic IC (PAL). The PAL outputs are used to give the two PPIs and the ADC their proper addresses in the PC's I/O map. Here, the function of the PPIs is to allow those ICs that are either relatively slow or not really intended for use in a computer environment, to be connected to the PC expansion bus. By virtue of the PPIs, it is possible to apply software control to the multiplexers and the discrete frequency meter, and also to monitor, by means of polling, the status of several components in the system.

The ADC chip used here is suitable for direct connection to a computer bus. Its software selection is accomplished by the OUT_0 output signal supplied by the address decoder. The EOC (end of conversion) and BUSY signals supplied by the ADC are read via a PPI.

The power supply is symmetrical. The ± 12 V supply of the PC is stepped down to ± 8 V on the card, and is also used to derive special reference potentials of ± 5 V. The digi-

tal components on the card are powered direct from the PC's 5-V supply.

Entering into details

Although a block diagram is quite useful to become acquainted with the overall structure of a circuit, a fully detailed circuit diagram is required to understand how the various functions are realized in practice. Hence, the operation of the measurement card will be discussed with reference to the circuit diagram in Fig. 2.

Connectors K4 and K5 (to the left in the circuit diagram) connect the circuit to the XT-slot in the PC. Circuits IC1, IC2 and IC3 provide the necessary buffering. The first, IC1, is a bidirectional type since its task is to buffer the databus, on which two-way communication is required. The other two buffers work in one direction only.

The address decoding is accomplished by IC7, a PAL. This IC, which is supplied ready-programmed, has been used before in a PC extension card project, see Ref. 1. Apart from the three selection signals, the PAL also supplies the reset signal for the ADC interrupt bistable, IC6A, and the enable signal for bus buffer IC1. The base address of the card can be set with the aid of jumper JP1 (position A:

MAIN SPECIFICATIONS

- **DC voltmeter**
 - ADC input range: 0 – 5 V
 - ADC resolution: 1.22 mV (12-bits)
 - ADC conversion time: 3 μ s
 - Level shifter: 0 – 5 V (input –2.5 V to +2.5 V)
 - 8 multiplexed inputs with 7 optional resistive dividers and 1 adjustable attenuator (0.1 – 300 V, autoranging)
- **Frequency meter**
 - Range: 0.0025 Hz – 10 MHz
 - Max. error: 0.0001%
 - Accuracy: 6 digits
 - Autoranging
 - 8 multiplexed inputs (TTL)
 - Arithmetic period measurement
 - Internal or external reference frequency
- **Event counter**
 - Range: 32 bits
 - Max. count frequency: 10 MHz
 - User-defined trigger edge
- **Pulsetime measurement**
 - Range: 0 – 400 s
 - Resolution: 0.1 μ s
 - High/low indication
 - Arithmetic duty cycle measurement

300H; position B: 310H). Table 1 shows the functions of the addresses assigned to the card.

The analogue circuitry is found back at the top of the circuit diagram. To the right we see an analogue multiplexer, IC12, which is used to control a stepped attenuator built from discrete components (R23 – R32). The attenuator is followed by a chopper-stabilized amplifier (Ref. 2), IC11, whose output signal is fed to a second analogue multiplexer.

The component values in the attenuator and the chopper opamp circuit are chosen such that the measurement ranges 0.1 – 0.3 – 1 – 3 – 10 – 30 – 100 – 300 V are created on channel I0. The other inputs of the multiplexer accept the signals on connector K3. Control signals ASEL0, ASEL1 and ASEL2 determine which of the eight signals at the multiplexer inputs is fed to ADC IC4, via buffer IC9B and level shifter IC9A. The ASEL signals are supplied by one of the PPIs, IC4. The arrangement allows a maximum of eight signals to be applied sequentially to the ADC. In the current circuit configuration, input I1 (pin 1 of connector K3) is used to calibrate the ADC. The calibration circuit can be disabled by fitting jumper JP10, when input I1 may be used as an additional measurement input.

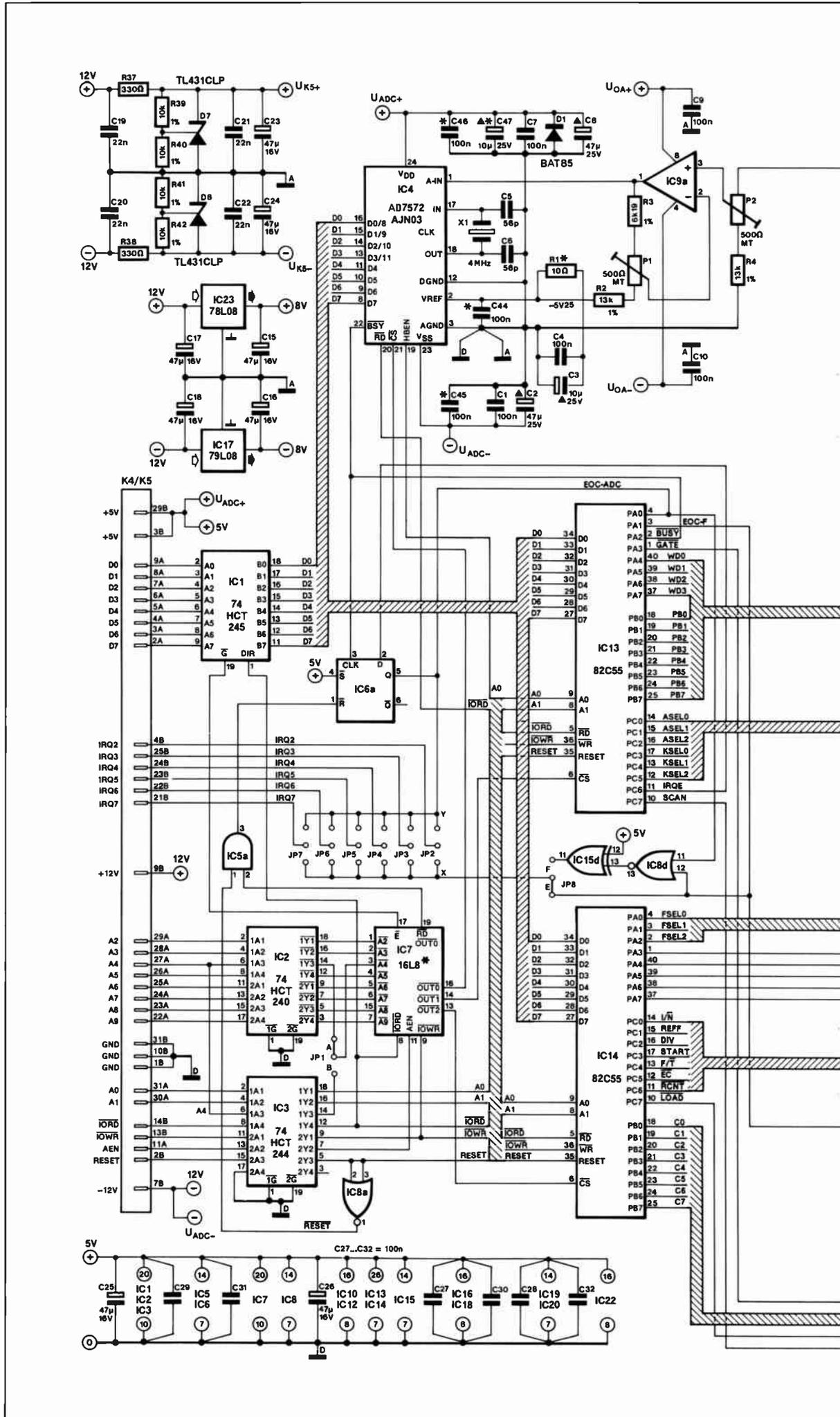
It should be noted that inputs I1 to I7 are not fitted with a protective network, so that any attenuator used on these inputs must include a form of protection against overvoltage. The simplest way to accomplish this is

probably to fit a pair of anti-parallel diodes. Note, however, that these diodes are not required, even undesirable (because of their leakage current), when measuring sensor voltages that can not exceed the operating area of the multiplexer (± 5 V). Depending on the desired measurement range, you must calculate the values of R_6 to R_{19} yourself. It will be clear that high-value resistors are preferred to keep ground currents in check. Each resistor junction in the attenuator may be decoupled with a capacitor ($C_{33} - C_{39}$).

Level shifter IC9A allows negative voltages to be measured. With the aid of the buffer/amplifier ahead of it, the level shifter enables voltages between -2.5 V and $+2.5$ V to be measured at an accuracy of 1.22 mV.

The heart of the circuit is a Type AD7572A analogue-to-digital converter from Analog Devices. This IC is supplied in four versions. The -A suffix version used here is the fastest with a conversion time of only $3 \mu s$. It requires a 4-MHz quartz crystal, X1, and a wire link in place of resistor R1. If you feel you can make do with a longer conversion time, you may want to use one of the slower, less expensive, versions of the AD7572. These, however, require a lower quartz crystal frequency, say, 1.25 MHz for a version with a conversion time of $10 \mu s$. At the lower clock frequencies, it may be necessary to adapt the values of capacitors C5 and C6 to ensure that the oscillator starts reliably. When the older version of the AD7572A, the AD7572, is used, resistor R1 must be fitted at its appropriate position on the PCB.

The ADC used has an internal reference that supplies a voltage of -5.25 V at pin 2. This voltage is used for the on-chip A-D conversion circuitry as well as for the pre-



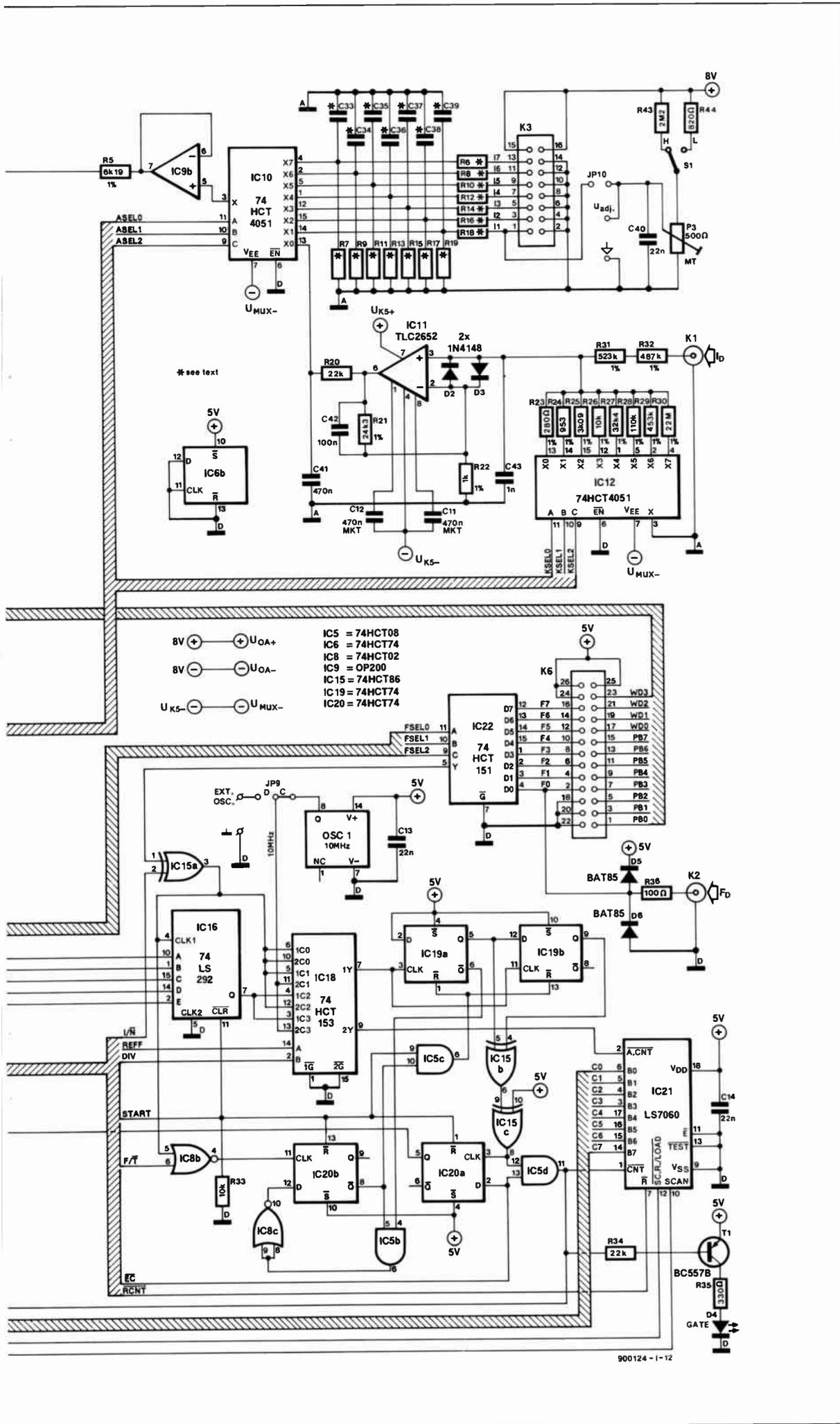
viously mentioned level shifter. The voltage level at pin 22 of the ADC indicates whether or not the A-to-D conversion process is complete. This allows the computer to monitor the conversion status with the aid of the PPI, although this type of check is really only useful when using either a slow ADC or a very fast computer. In most cases, a conversion time of 3- μ s is too fast in any case for the computer to execute the relevant start instructions, and evaluate the results. This is particularly so when the control program is written in a higher language.

The above discussion may suggest that a fast ADC is extravagant and a superfluous luxury. Bear in mind, however, that a fast ADC can take more samples of a measurand within a short period, allowing the software to calculate the correct value on the basis of the sampled values. This type of software-based filtering effectively eliminates the adverse effects of spurious pulses and noise on the measurement results, and brings true 12-bit resolution within easy reach.

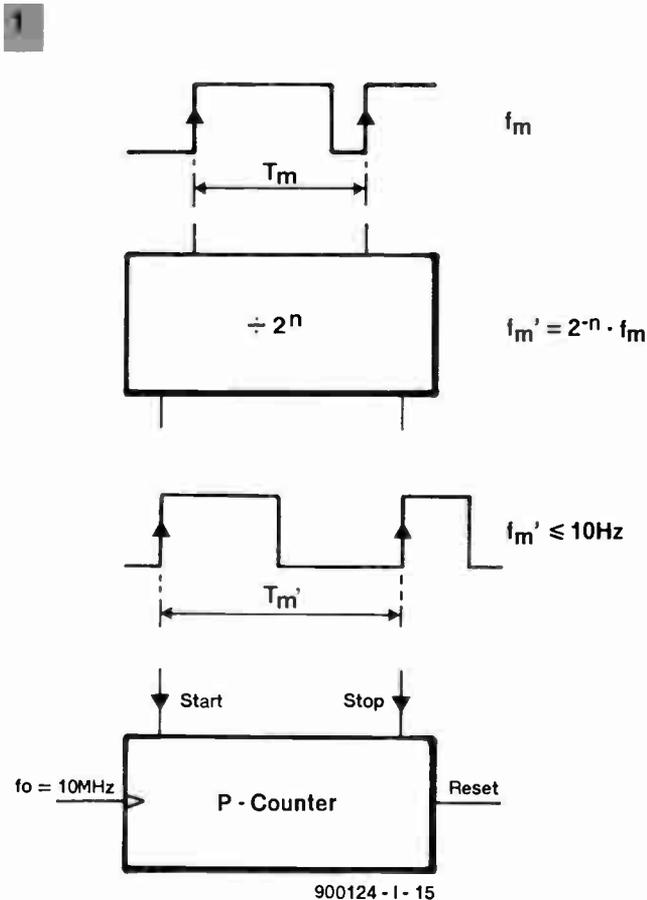
A different principle

A fairly unusual principle is adopted for the measurement of frequency. In most frequency meters, the frequency of the input signal is measured by counting the number of leading or trailing pulse edges that occur within a fixed period, called the gate time. In this system, the measurement error increases considerably as the number of counted pulses decreases within

Fig. 2. Circuit diagram of the multifunction measurement card for PCs. The main functions of the card are a voltmeter and a frequency/pulse meter. Both are implemented with a very high accuracy of 12 bits and 1 p.p.m. respectively.



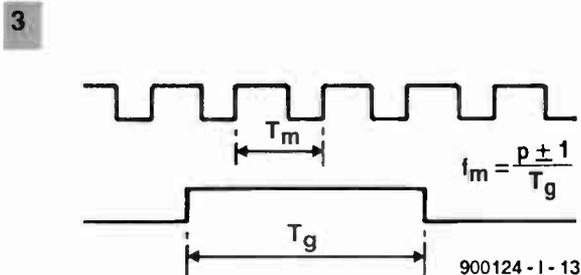
FREQUENCY MEASUREMENT: A DIFFERENT APPROACH



In all probability, the simplest way of measuring frequency is counting the number of periods (p) of a signal within a fixed gate time (T_g). Unfortunately, this method has one important disadvantage: the so-called ± 1 -error, which means that the last pulse in a measurement or conversion is always undetermined. Owing to this error, the accuracy of the simple measurement drops inevitably with the input frequency (see Fig. 1). Although the effect of the ± 1 -error can be reduced by increasing the gate time, measurement times rapidly rise to excessive lengths when dealing with low frequencies. For

example, a 6-digit (0.0001%) accurate measurement of a 1 Hz signal would require a gate time of 277.8 hours! Clearly, this is a totally impractical measurement time.

In addition to lengthening the gate time, the accuracy may also be improved by first multiplying the frequency to be measured with a known reference frequency, and subsequently measuring the product frequency. The result may then be used to calculate the original input frequency. Unfortunately, multiplying signals whose frequencies differ by a considerable amount is not so simple, so that



this measurement method is far from ideal.

A much more efficient method to determine the frequency of a signal is based on period time measurements, where a circuit counts pulses supplied by a stable reference during one period of the measurand (see Fig. 2). In this way, the measurand switches the reference on and off. As in the 'simple' measurement system, the accuracy achieved is dependent on the frequency to be measured — since a fixed reference frequency is used, the effect of the ± 1 -error rises with the frequency to be measured. This is caused by the 'gate time' becoming shorter with higher input frequencies, so that fewer periods of the reference source can be counted. Remember, the effect of a ± 1 -pulse error is ten times greater with 1,000 counted pulses than with 100 counted pulses.

The accuracy of this type of measurement may be increased by lowering the input frequency. This is fairly simple to accomplish by dividing the input signal by a known factor. As illustrated in Fig. 3, the real frequency may then be computed on the basis of the lowered frequency and the divisor.

Briefly recapitulating, the method of counting reference periods has two advantages over counting input signal periods:

- the time required for the measurement equals the period time of the (scaled-down) input frequency, and thus remains within acceptable values;
- the fact that signal division may be applied instead of signal multiplication allows a simpler circuit to be used.

In practice

Among the target requirements of the PC measurement card was a maximum permissible measurement error of 1 p.p.m. (or $1 \times 10^{-4}\%$) as a result of the ± 1 -error. This value was not set just like that — it can be shown that it is the maximum permissible error if the measurement is to have 6-digit accuracy. Mathe-

matically, this requirement can be expressed as:

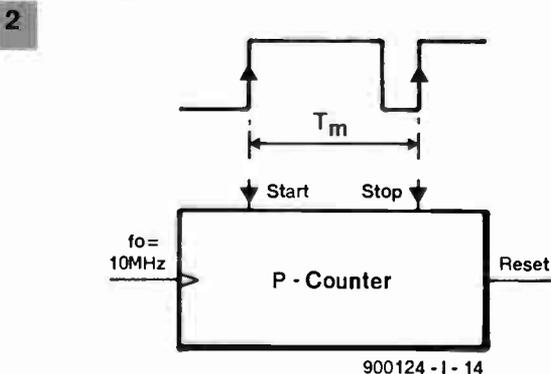
$$f_m \leq 1 \times 10^{-6} f_o \quad [1]$$

where f_m is the frequency to be measured, and f_o the frequency supplied by the reference source. Since the reference operates at 10 MHz in this case, equation [1] rules a maximum value of f_m of 10 Hz. This means that the scaled-down frequency, f'_m , must comply with equation [1]. In other words: $f'_m < 10$ Hz. In terms of hardware, the input signal is scaled down by IC16, a 74LS292. This IC allows a divisor 2^n to be programmed, where n may take discrete values from 2 to 31. From this, it can be shown that n must comply with

$$n > (\log_{10} f_m / 10) / (\log_{10} 2) \quad [2]$$

to ensure the required measurement accuracy.

From equation [2] it follows that f_m must be known before n can be computed, while at the same time n must be known for accurate measurement of f_m . Although this looks like a chicken-and-egg problem, acceptable results may be obtained for the setting of n by performing a rough approximation of f_m . In practice, the problem is solved as follows. First, f_m is estimated with the aid of a preliminary measurement, carried out with a factor, n , of nought. This factor results in the shortest measurement time. If the result of the preliminary measurement is greater than 10 Hz, the frequency is entered as f_m in equation [2]. Next, the computer calculates the optimum value of n , and sets the programmable divider to the required divisor. Next, the real measurement follows. The result of it (f'_m), multiplied by 2^n provides the frequency of the input signal, at the required accuracy of 6 digits. When the preliminary measurement results in a value of f_m smaller than 10 Hz, the 'first go' is already sufficiently accurate, and thus obviates a second measurement. □



Address	Function
3x0	Read ADC lower byte
3x1	Read ADC upper byte
3x2	Read ADC lower byte
3x3	Read ADC upper byte
3x4	Port A IC13 (input)
3x5	Port B IC13 (not used)
3x6	Port C IC13 (output)
3x7	Control IC13
3x8	Port A IC14 (output)
3x9	Port B IC14 (input)
3xA	Port C IC14 (output)
3xB	Control IC14
JP1 = A:	x = 0
JP1 = B:	x = 1

All addresses in hexadecimal

Table 1. Functions of addresses assigned to the measurement card.

the gate time. This principle is, therefore, not practical for the measurement of very low frequencies, since these would require gate times of minutes, or even hours, to ensure the necessary accuracy. Hence, the present PC measurement card is based on a totally different principle for measuring frequency. This principle, which is explained separately on the previous page, does not have the above disadvantage of low accuracy at low frequencies.

As with the voltage meter circuit, a multiplexer (IC22) is fitted between the inputs and the actual measurement circuit. One of these eight inputs is provided with a protection circuit, and taken to a pin on connector K2. The remaining seven are connected to K6 only. From the output of the multiplexer, the selected signal is fed to XOR gate IC15A. This gate may be used to invert the signal under the control of the I/ \bar{N} line. The output of the

State	DIV	REFF	1Y	2Y
Event count	n.a.	L	n.a.	f_m
Pulsetime	L	H	f_m	f_o
Frequency:				
first go	L	H	f_m	f_o
real	H	H	f_m	f_o

f_m = frequency of input signal
 $f'_m = f_m/2^n$
 f_o = 10-MHz reference frequency
n.a. = not applicable

Table 2. Control signal programming to select the various functions of the card.

XOR gate is connected to a 2ⁿ divider, IC16, a multiplexer, IC18, and a NOR gate, IC8B. The multiplexer thus has three input signals: the input signal (in true or inverted form), the input signal divided by 2ⁿ, and the 10-MHz clock signal supplied by oscillator block OSC1. Control signals REFF and DIV on the A and B inputs determine which input signals appear at the multiplexer outputs, 1Y and 2Y. The multiplex configuration is shown in Table 2.

Circuits IC19A and IC19B form a two-bit shift register that is used to detect exactly one period during frequency measurements. Following a reset pulse, both Q outputs are low. They are also low after two leading edges of the clock signal. As long as only one output is low (during one period of the clock signal), the clock signal is passed to a 32-bit counter, IC21 (a Type LS7060), via XOR gates IC15B-IC15C and AND gate IC15D. Note that the counter is an LSI chip, not a device from the 74LS series. Simultaneously with the enabling of the 32-bit counter, the gate LED, D4, lights to indicate that a measurement is being performed.

The measurement is started in a relatively simple manner. First, the 32-bit counter is cleared with the aid of the $\bar{R}CNT$ signal. The START signal goes low, and resets the other registers. Next, START goes high, so that the shift register enables the counter during one period.

After one period of the input signal, the signal EOC-F is actuated (START = high) via bistable IC20A. Next, the counter can be read via IC14 with the aid of signals SCAN and LOAD.

A relatively simple arithmetic operation allows the period to be deduced from the results of the frequency measurement. In addition, the pulse on-time can be measured. Since it is possible to invert the input signal, it is a relatively simple matter to measure both the 'high' time and the 'low' time of the input signal. The circuit based on bistable IC20B and its associated gates perform this task elegantly. The PC uses the F/T signal to select between frequency measurement and pulse time measurement, while the logic level on the I/ \bar{N} line determines whether the measured time corresponds to the 'low' or the 'high' part of the input pulse. When I/ \bar{N} is logic low, IC15A will not invert the input signal. Consequently, IC19A is reset by the first leading edge after the START command. From that moment on, counter IC21 remains enabled until IC19A is reset by the next pulse transition, which is trailing. This resetting takes place via IC20B.

During the measurement, a NOR gate, IC8B, propagates the measurand to the clock input of bistable IC20B, which is thus clocked at each trailing edge of the input signal. By virtue of IC5B, this clock signal is only effective with IC19A set, when a logic one is applied to the input of IC20B. Once IC20B is set, IC19A is reset, and the counter disabled. Because the \bar{Q} output is fed back to the data input of the bistable (via IC5B), the state of IC19A and IC21 is frozen until the next start pulse occurs. The appearance of the EOC-F

signal at the Q output of IC20A indicates that the measurement is complete. Next, the program reads the counter state. The pulse 'low' or 'high' time is simple to compute since it is the counter value divided by the reference frequency. The resolution of this measurement is 100 ns.

As indicated above, the 'high' time of the input signal is measured with I/ \bar{N} not active. When this signal is active, IC5A inverts the input signal, and the 'low' time is measured like the 'high' time, as explained in the previous paragraphs.

For the pulse-related measurements a 10-MHz reference frequency is used. This frequency is supplied by a quartz crystal block, OSC1. Jumper JP9 allows an optional, external, oscillator to be connected.

A feature of the card that has not been discussed so far is its ability to function as an event counter. In this mode, the input signal is connected to the clock input, pin 2, of the counter, via IC18. The counter will count pulses as long as $\bar{E}C$ (event count) is active, i.e., logic low. This is arranged by the software. In contrast to the situation with the other measurement modes, the event counter mode requires the START signal to remain inactive. To complete the story, we must mention that the signal I/ \bar{N} determines which pulse edge of the input signal is used to advance the counter.

In the centre of the circuit diagram we find six jumpers labelled JP2 to JP7. These jumpers allow the interrupt signal supplied by the card to be connected to one of the interrupt lines on the PC expansion bus. As usual with PC insertion cards, due care must be taken to use a free as well as appropriate interrupt line. In most IBM PCs, the interrupt line assignment is as follows:

IRQ2:	reserved
IRQ3:	COM2: (serial I/O)
IRQ4:	COM1: (serial I/O)
IRQ5:	hard disk
IRQ6:	floppy disk
IRQ7:	LPT: (parallel I/O)

The measurement card may be set to use IRQ3 without problems if the PC is a type with only one serial port (COM1 on IRQ4). Where IRQ3 is in use by COM2, it is nearly always possible to move the measurement card to IRQ2.

The IRQ line assigned to the measurement card must be set in hardware as well as in software. The software setting is accomplished by modifying one line in the configuration file, ADCF.CFG. Further details on the use of interrupt lines are provided in the READ.ME file on the diskette.

Finally, jumper JP8 allows us to either combine the interrupts from the frequency meter and the ADC (jumper position F), or use them separately (jumper position E). ■

Next month's second and final instalment of this article will deal with the construction and practical use of the measurement card, and with the control software developed for it.

MEASUREMENT TECHNIQUES (3)

by F.P. Zantis

Following the discussion in our previous issue on the measurement of voltage, this month's instalment deals with the measurement of current and power.

STRICTLY speaking, each and every moving-coil or moving-iron measuring instrument is an ammeter. The deflection of the pointer is proportional to the level of the current flowing through the instrument. However, only a small number of them have been constructed specially for the measurement of current. In most electronic laboratories and workshops, multimeters are habitually used for measuring current.

The full-scale deflection of the instruments used in multimeters varies roughly from $50\ \mu\text{A}$ to $500\ \mu\text{A}$. Since the levels of the currents to be, or being, measured are normally much higher than those values, the metering range must be extended. This is usually done by shunting the meter with an appropriate resistance through which the larger part of the current flows. When a metering range is selected in a multimeter, a different shunt resistor is switched in parallel with the meter—see Fig. 15.

Current measurements by digital meters are transformed to voltage measurements, for which shunt resistors are also required. The potential drop measured across the appropriate resistor is proportional to the current through it. Here again, the ammetering range is extended by the use of a number of resistors.

The measurement of alternating currents is subject to errors, tolerances and problems that are similar to those experienced in measuring alternating voltages. For instance, the measurement is true for only one frequency. Also, the true r.m.s. value is indicated only for a truly sinusoidal current. However, there are, fairly expensive, so-called true-r.m.s. multimeters that indicate the r.m.s. value irrespective of the waveform of the measurand.

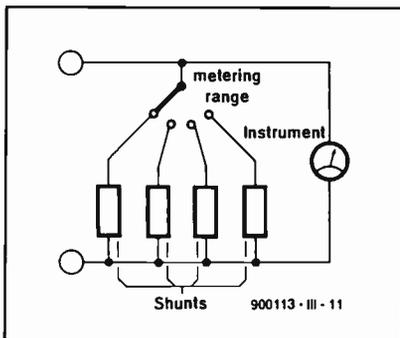


Fig. 15. The metering ranges of current meters are extended by placing resistors called shunts in parallel with the meter.

Errors in current measuring

Errors in current measurements occur because of the frequently not very high accuracy of the instrument or through the effect the instrument has on the measurand. As in voltage measurements, the internal resistance of the instrument causes a measuring error. To measure a current, the circuit through which it flows has to be opened to enable the meter to be inserted in series. That does, of course, increase the total resistance in the circuit by an amount equal to the internal resistance of the measuring instrument. The higher the internal resistance, the greater the measuring error. For instance, if a circuit has a resistance of $3\ \Omega$ and a potential of $12\ \text{V}$ is applied across it, a current of $I = U / R = 12/3 = 4\ \text{A}$ flows. If now a meter with an internal resistance of $0.5\ \Omega$ is inserted into the circuit, the current will be $12/(3+0.5) = 3.43\ \text{A}$. That is a measuring error of no less than 17%! The higher the sensitivity of the measuring instrument, the smaller its internal resistance and, consequently, the error.

Indirect current measurement

The level of a current is determined more accurately when the voltage drop it causes across a resistance is measured. The error that occurred in the example in the previous paragraph then becomes negligibly small. The level of the current through the resistance is calculated with the aid of Ohm's law. This method of indirectly measuring the current is normally far preferable over the direct method. Furthermore, it has the advantage that the circuit under test need not be broken into, which, especially in the case of a

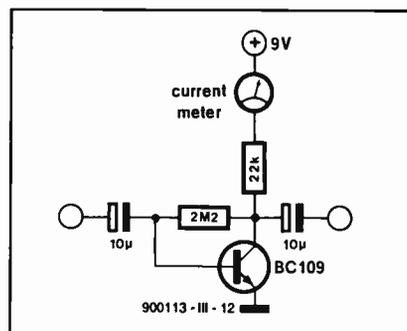


Fig. 16. In difficult cases, the direct method of current measurement may be used to indirectly measure voltages to reduce the measurement error.

printed circuit, may be fairly difficult if not impossible.

On the other hand, a direct measurement of current with a simple multimeter may solve a seemingly insoluble difficulty in measuring a voltage. Consider, for instance, the circuit in Fig. 16 where, to enable the operating point to be set, the drop across the collector resistor must be measured. To do this with a $20\ \text{k}\Omega/\text{V}$ multimeter, a fairly large measuring error would be caused by the internal resistance of the instrument. Here, it is far better to measure the current through the resistor as shown, always provided that the internal resistance of the meter is sufficiently small. The voltage across the resistor is, by Ohm's law, the product of current and resistance.

Note that in the previous paragraph it is not possible to measure the base current, since that is too small to be measured with the usually available instruments.

To estimate the measuring error as precisely as possible, it is necessary to know the internal resistance of the ammeter at the selected metering range. Unfortunately, manufacturers only specify this for the voltage ranges. It is, therefore useful to know how to determine it for the current ranges. This may be done by measuring the current from a constant-current source. Then, successively connect a number of resistors of different values in parallel with the meter inputs as shown in Fig. 17. When the meter indicates half the level of current measured before any resistance was connected in par-

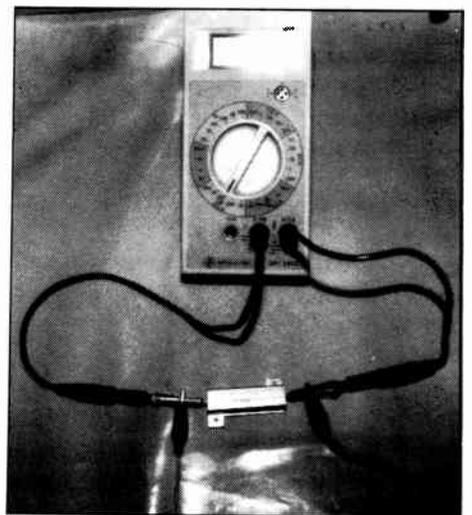


Fig. 17. Multimeter with external shunt resistor.

allel, the internal resistance of the meter is equal to the value of the resistor then shunting the meter inputs.

Extending the metering range

Some multimeters have, in addition to several fused current ranges of up to 2A, an unprotected range of up to 10 A, or even 20 A. In principle, however, most multimeters may be used for measuring high currents, but this entails extending their metering range(s).

The current range(s) of a multimeter may be extended by the same method as used above to determine the internal resistance. If, for instance, a resistor whose value is equal to the internal resistance of the instrument is connected across the input terminals, half of the measurand flows through it. In other words, the indicated value must be multiplied by 2 to obtain the true value of the current. When two such resistors are connected across the input terminals, two thirds of the measurand flows through them and the meter reading must be multiplied by 3. With the well-known formula $P = I^2 R$, the power dissipated in the shunt resistor(s) may be calculated. Unfortunately, resistors with the required power rating are normally available only in the 10% tolerance range, which does not bode well for accurate measurements. A further drawback is that the required resistance values are normally not available as standard resistors, so that series-parallel combinations must be used. An aid to calculating the needed resistance values will be given in the form of a small basic program later in the series

Current measurement with an oscilloscope

For measuring large currents, the indirect method is normally much easier to realize. When the circuit under test has no current-carrying resistor across which the voltage that determines the current can be measured, one must be added. For that purpose, any resistor may be used whose value is small compared with that of the overall circuit. It is in-

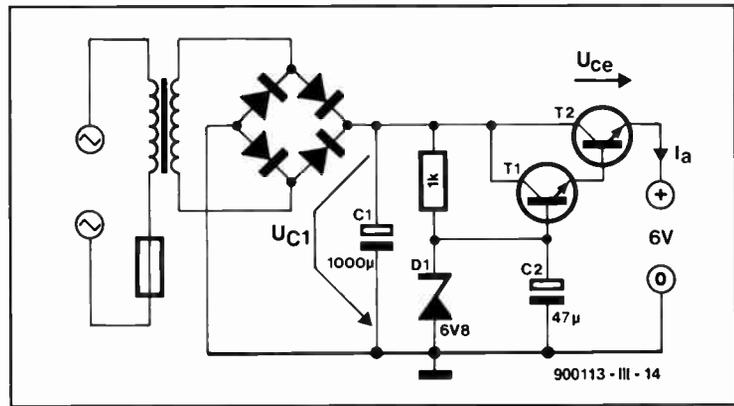


Fig. 19. Circuit of a typical series regulator in a power supply. The example in the text is the same when an integrated voltage regulator is used.

serted into the loop whose current is to be measured and the voltage across it measured. The current is then easily calculated with the aid of Ohm's law. For certain values of resistance, the calculation is very simple. If, for instance, a 1-Ω resistor is used, the value of the measured voltage in volts is equal to the current in amperes. Also, if a 0.1-Ω resistor is used, the indicated value in volts must be multiplied by 10 to give the current in amperes. With this method it is possible to use almost any oscilloscope as an ammeter; even current peaks can be detected—see Fig. 18.

Even in indirect measuring of current, the tolerance of the shunt increases the measuring error.

If the current must be measured without opening the circuit under test, a current probe needs to be used. This is placed around the wire or cable through which the measurand flows. Its output is supplied to an ammeter or oscilloscope. Such probes are suitable only for measuring medium to high currents. Probes that operate on the transformer principle are suitable only for measuring alternating currents, whereas those that use a Hall generator may be used for d.c. and a.c. measurement.

Some tips

Except when current is measured with a probe, the circuit under test should be switched

off when it is being prepared for the test. Only when the measuring instrument is secured to it should the power be switched on. Also, make sure that no large charging currents (caused by uncharged electrolytic capacitors, for instance) can overload the instrument or blow its fuses.

When the approximate value of the measurand is not known beforehand, the highest metering range of the instrument used should be selected. The most appropriate range may then be selected once the measurement is underway.

Measurement of power

Special power meters with separate current and voltage circuits are hardly ever necessary. In most cases, it is perfectly all right to measure current and voltage separately in the circuit under test and then calculate the power dissipated.

A typical example is the dissipation in a series regulator—see Fig. 19. In this circuit, a regulated voltage of 6 V is obtained from the unregulated potential across C_1 . The dissipation in T_2 , which is the product of voltage U_{ce} across T_2 and output current I_a , is converted into heat.

Of interest is the operating point at which the dissipation in the transistor is a maximum. That point depends to some extent on the voltage across C_1 . The relation between power

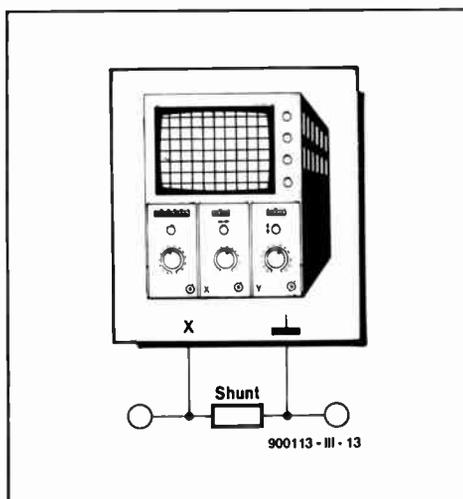


Fig. 18. An oscilloscope may be used for indirect measuring of current.

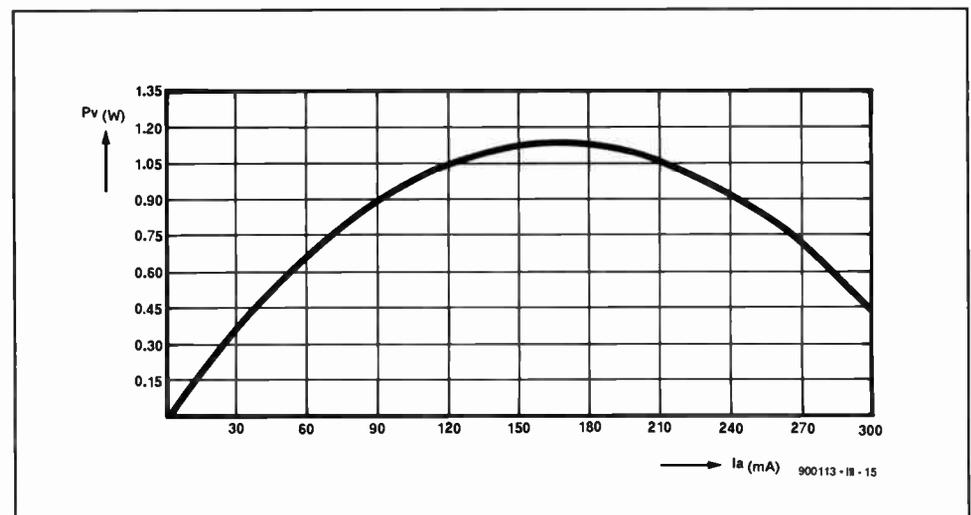


Fig. 20. Curve showing power dissipation vs output current in a typical series regulator.

dissipation, P_v , and output current, I_a , is shown in Fig. 20. Maximum dissipation is reached when the output current is slightly larger than half the permissible value of 330 mA. This leads to the conclusion that U_{c1} is load-dependent. When the current rises, U_{c1} drops which, since the output voltage is constant, causes the potential across T_2 to drop also. This results in a reduction in the power dissipation in the transistor.

The determination of the power in this example is straightforward since only a direct voltage and a direct current are involved. The process would have been just as painless if low-frequency sinusoidal quantities had been involved. It is, for instance, possible to calculate the input power of the transformer in Fig. 19 once the voltage and current are known. A word of caution here, though: since the alternating measurands are operating with a reactance, that is, the transformer winding, the calculation will result in the **apparent power**. This is not of such practical use as the **active (or true) power**. To determine that, the power factor $\cos\phi$ must be known. The true power, P , is then calculated from

$$P = U \times I \times \cos\phi.$$

The power factor may be determined with the aid of a dual-trace oscilloscope as shown in Fig. 21. One trace shows the voltage and the other the current. Not the magnitude of the two measurands is important, but the phase difference between them: this is the distance between the zero crossing of the voltage and that of the current. Unfortunately, the current in Fig. 21 is measured inverted; this cannot be avoided, however, and must be allowed for in the calculation. A number of scopes have an invert mode facility, which enables inversion of the trace on the screen.

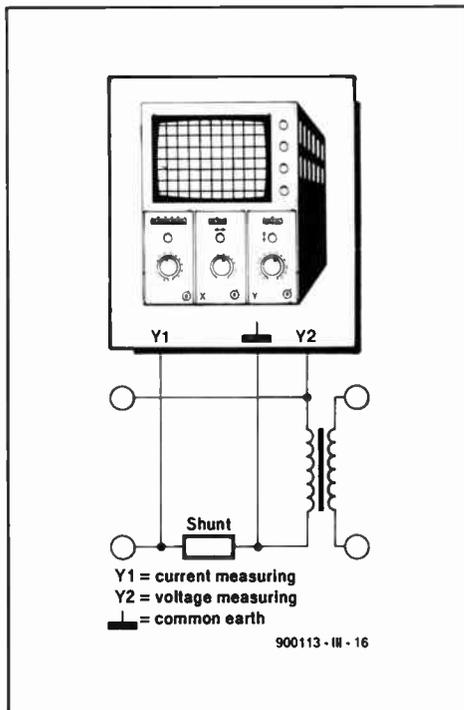


Fig. 21. Phase shift may be measured with the aid of a dual-trace oscilloscope. One signal will be inverted since there is only one common earth.

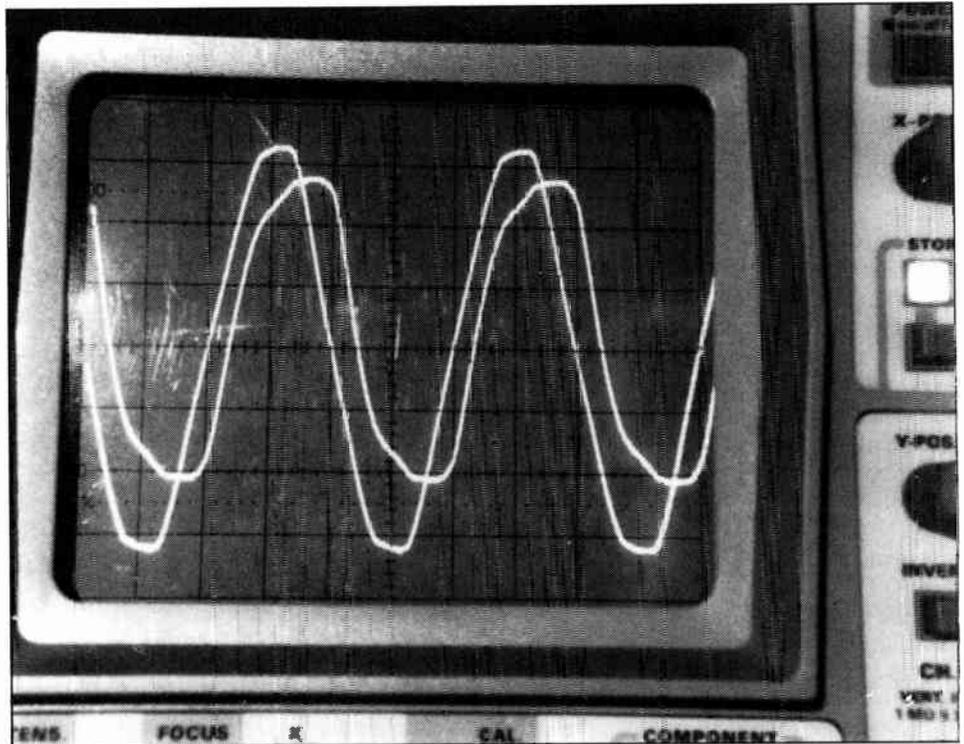


Fig. 22. Measurement of phase shift between voltage and current pertaining to a soldering iron operated from the mains via an isolating transformer.

Such a screen is shown in Fig. 22: the two traces pertain to the voltage and current of a soldering iron operated from the mains via an isolating transformer. The value of the shunt is 1 Ω ; the error caused by it may be ignored. The phase shift between the two traces is 2 scale divisions. Since a period of 360° extends over 20 divisions, the phase shift, ϕ , amounts to

$$\phi = (360 / 20) \times 2 = 36^\circ,$$

and the power factor is

$$\cos\phi = \cos 36^\circ = 0.809.$$

Such measurements on the mains must be made with the aid of an isolating transformer, since otherwise a short-circuit may be caused by the earth of the oscilloscope.

The relation between the input power and output power of a transformer is the efficiency, ϵ . To get a correct analysis of the behaviour of a mains-operated power supply, some additional calculations are necessary. These types of measurement become easier to handle when the subsequent computation is carried out by a computer and relevant software. A suitable table may be designed with the aid of a table calculation program. Constants and formulas may be taken from memory, so that only the actual measurements need to be entered. The results, that is, input power, output power, power dissipation, efficiency, and so on, then become available in tabular form, from which relevant curves or bar diagrams may be produced almost immediately the measurements have been taken. A printer may be found useful to put all the information to paper.

Power measurements become a little more difficult when switching regulators or phase gating circuits are involved. The waveform is then not sinusoidal, so that most multimeters do not give a correct result: a true RMS meter is then required. The two waveforms may also be displayed on the screen of a dual-trace oscilloscope for analysis. For a worthwhile result, it is best to redraw the curves on suitable graph paper, as for instance in Fig. 23, to arrive at a power curve. The average value deduced from that curve is the required power.

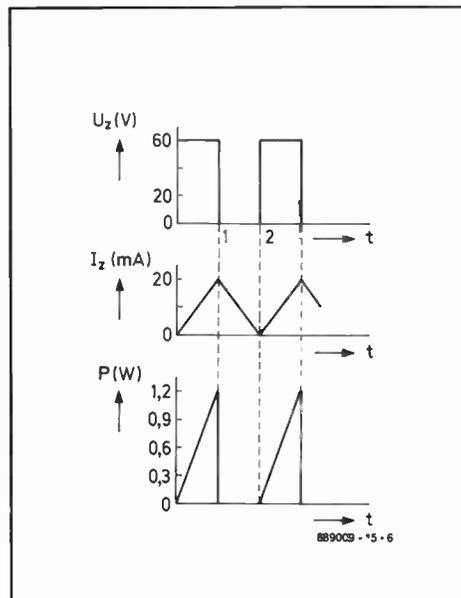


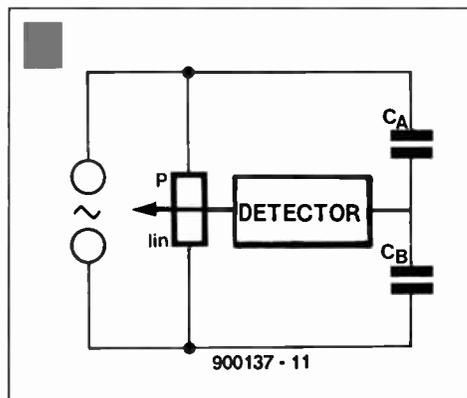
Fig. 23. A dual-trace oscilloscope may also be used to determine the power when voltage and current are not sinusoidal.

A SIMPLY ELEGANT L-C-R BRIDGE

The balanced bridge described in this article measures capacitance from 1 pF to 10 μ F, resistance from 1 Ω to 10 M Ω , and inductance from 1 μ H to 100 μ H. Ideal for checking the values of non-marked or otherwise non-identifiable components, the instrument costs next to nothing, and can be built from parts from the junk-box.

E. Chicken, MBE, MSc, BSc, CEng, FIEE (G3BIK)

THE first design of the instrument proposed here was a basic capacitance-measuring bridge which consisted of nothing more than two capacitors, a 10-k Ω carbon linear potentiometer, a crystal ear-piece, and a total of four solder joints, as shown in Fig. 1.



An alternating voltage at audio frequency was required to feed the bridge, and a quick glance around the author's radio shack showed a number of possible sources, e.g., an oscilloscope which offered a 1-kHz square-wave signal at 1 V_{pp} on its front panel for self-calibration, an RF signal generator which offered a 1-kHz sine-wave at a few volts rms, a home-made AF oscillator with a 2-V output, and, if the worst came to the worst, the audio output from the transistor broadcast radio tuned to the pop-music channel!

All were tried and found to provide a fully audible signal in the crystal earpiece, and rotation of the balance potentiometer spindle yielded a clearly discernible and sharp null, more than adequate to afford repeatable accuracy of measurement.

The capacitors were replaced with resistors, with equally promising results for the measurement of resistance.

But what of inductance in the RF range? A few turns of enamelled copper wire were wound on to an available 7-mm former with an iron-dust slug core. A 100-pF capacitor was soldered across the coil. Its resonant frequency was adjusted to about 15 MHz with the aid of a gate dip oscillator. Next, the inductance of the coil was calculated to be ap-

proximately 1 μ H. That would be the 'unknown' inductor of low value.

Another coil was wound with about ten times as many turns to produce a higher value of inductance. The actual value was not important, as will be explained later.

With the two inductors connected into the bridge in place of the two capacitors, again it was possible to obtain a sharp audio-null to indicate balance.

Turning the core in the 1- μ H coil to produce a different value of 'unknown' inductance required the potentiometer to be re-adjusted to restore balance. This demonstrated the viability of the simple bridge as a measuring device suitable for all three types of passive component, i.e., for inductance (L), capacitance (C) and resistance (R).

Balanced bridge for L-C-R measurement

Consider first the simple resistive potential divider shown in Fig. 2a. The potential difference, or voltage drop, across R_a is

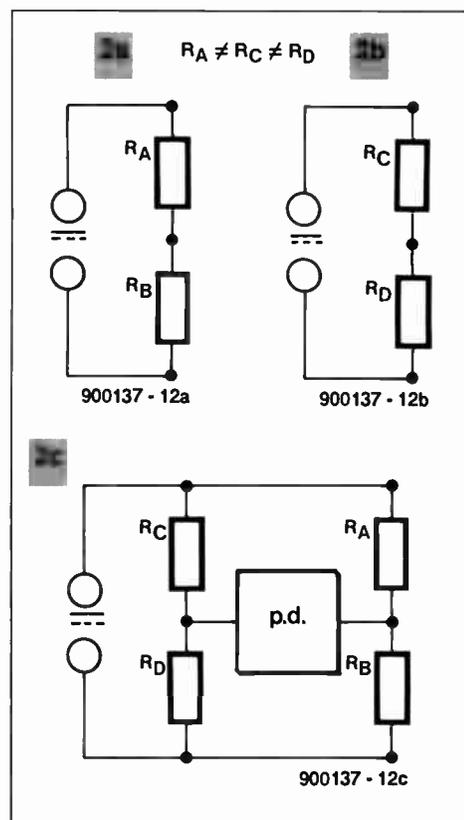
$$U_s \frac{R_a}{R_a + R_b}$$

where U_s is the supply voltage. Now consider the other resistive potential divider in Fig. 2b, which incorporates unspecified but different values of resistor from those in Fig. 2a. The potential difference, or voltage drop, across R_c is

$$U_s \frac{R_c}{R_c + R_d}$$

Connecting the two potential divider networks in parallel to form a basic resistive bridge, and feeding them both from the common voltage supply, as shown in Fig. 2c, does not alter the two equations given for the potential differences across R_a and R_c .

If, however, the voltage drop across R_a is different from that across R_c , then a voltage detector connected between junction R_a - R_b and junction R_c - R_d will indicate the difference between the two voltage-drop



values. But, if the voltage drop across R_a is equal to that across R_c , the potential difference will be nought, and the voltage indicator will read zero or a voltage 'null'. The electrical bridge formed by the two potential divider networks R_a - R_b and R_c - R_d is then said to be balanced, and that will also be so irrespective of whether d.c. or a.c. is used for the voltage supply. The mathematical equation for such a null condition is given by

$$U_s \frac{R_a}{R_a + R_b} = U_s \frac{R_c}{R_c + R_d}$$

which simplifies to

$$\frac{R_a}{R_b} = \frac{R_c}{R_d}$$

If the value of R_b is known and fixed, and if the ratio R_c/R_d is known, it is possible under

this null condition (i.e., when the bridge is at balance) to determine the actual value of an unknown resistor R_a from

$$R_a = R_b \frac{R_c}{R_d} = (\text{known } R_b) \times (\text{ratio } R_c/R_d)$$

For example, if R_c is made equal to R_d , their ratio is 1.0, and the null condition becomes $R_a = R_b$, irrespective of the actual values of R_c and R_d . Only their ratio is of importance.

Further, if the ratio R_c/R_d is made adjustable and calibrated, and if the value of the known resistor R_b is made to be switch-selectable, the unknown resistor, R_a , can be quantified over a wide range of values.

Scale design: the basics

For convenience, R_c and R_d can be replaced by a linear-law rotary potentiometer of any convenient resistive value, to be provided with a circular scale and a pointer knob. The scale is then calibrated to read the ratio of resistive values measured between the centre tag and the two outer tags of the potentiometer, for different angles of spindle-rotation.

At mid-travel, for example, the resistance measurements between the centre tag and the two outer tags would be equal in an ideal linear-law potentiometer. At three-quarters traverse, the resistance of one section would be some three times that of the other section, giving a ratio of 3:1 and vice-versa.

In other words, as the spindle is rotated away from mid-position in one direction, the ratio will increase from 1.0 upwards towards infinity, and in the other direction it will decrease from 1.0 towards zero.

Although the rotational movement of a standard linear-law carbon potentiometer is restricted to about 300 degrees of travel, fortuitously and very conveniently the ratios $\times 10$ and $\times 0.1$ fall at approximately 90 degrees on either side of mid-travel. So, if mid-travel is positioned at the top of the scale, i.e., at 360 degrees, then the dial can be marked $\times 0.1$, $\times 1.0$, and $\times 10$ at 270, 360 and 90 degrees respectively, and $\times 0.01$ and $\times 100$ at 240 and 120 degrees respectively; to a first approximation.

The value of a resistor is thus readily determined by rotating the potentiometer until a null is detected. The ratio indicated on the scale is subsequently multiplied by the value of the known resistor, R_b . Mathematically,

$$R_a = R_b \times [\text{ratio } R_c/R_d \text{ at null}]$$

By assigning a selection of different values for the *known* resistor R_b , the range of measurement for the *unknown* resistor, R_a , can be conveniently modified. To simplify measurement even further, it is preferable to use whole number values for the *known* resistors, e.g., 100 Ω , 10 k Ω , 100 k Ω , etc. These known resistors, which for convenience can be range-selectable, are then renamed *range re-*

sistors, and the switch escutcheon is marked with their values. An example: if a null occurs at, say, $\times 0.05$ on the 1,000 Ω range, the unknown resistor has a value of $(1,000 \times 0.05) = 50 \Omega$.

Inductance measurement

The above principle of measurement can also be applied to inductance, with resistors R_a and R_b replaced by inductors L_a and L_b . To be effective, the bridge *must* be fed with an a.c. voltage at a frequency, f , high enough to produce inductive reactances X_a and X_c respectively, sufficient to provide potential differences suitable for null detection.

The simplified potential difference equations at null condition are:

$$X_a = X_b \frac{R_c}{R_d}$$

where X for inductive reactance is

$$X = 2 \pi f L$$

So, this equation simplifies to:

$$L_a = L_b \frac{R_c}{R_d}$$

which conveniently uses the same ratio multiplier R_c/R_d as for resistance measurement, hence the same ratio scale can serve for both resistance and inductance.

Capacitance measurement

For the measurement of capacitance with inductors L_a and L_b replaced by capacitors C_a and C_b , again the voltage supply must be a.c. to provide, in this case, capacitive reactances X_a and X_b .

The simplified equation for potential difference in the null condition is

$$\frac{X_a}{X_b} = \frac{R_c}{R_d}$$

where X for capacitive reactance is

$$X = \frac{1}{2 \pi f C}$$

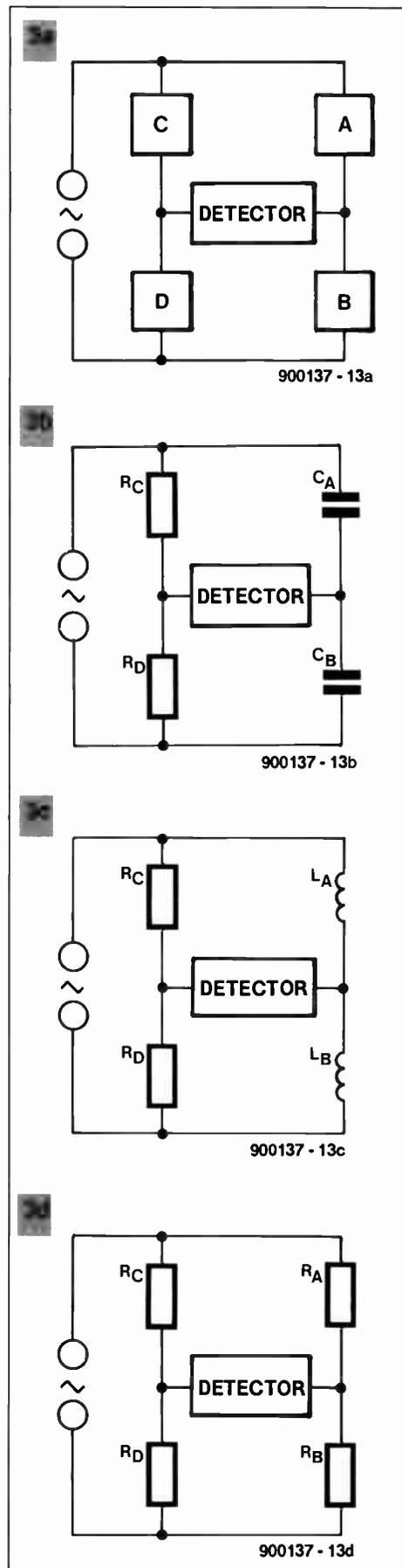
$$X_a = X_b \frac{R_c}{R_d}$$

which simplifies to

$$C_a = C_b \frac{R_d}{R_c}$$

Note that in this expression the ratio multiplier, R_d/R_c , is inverted with respect to the one used for the resistance and inductance measurements. In practice, this means that a mirror-image of the ratio scale is required for the measurement of capacitance. So, the scale

$$0.01 \quad 0.1 \quad 1.0 \quad 10.0 \quad 100.0$$



becomes

$$100.0 \quad 10.0 \quad 1.0 \quad 0.1 \quad 0.01, \text{ etc.}$$

Again, a selection of range capacitor values for C_b will provide the desired range of measurement, and for user convenience,

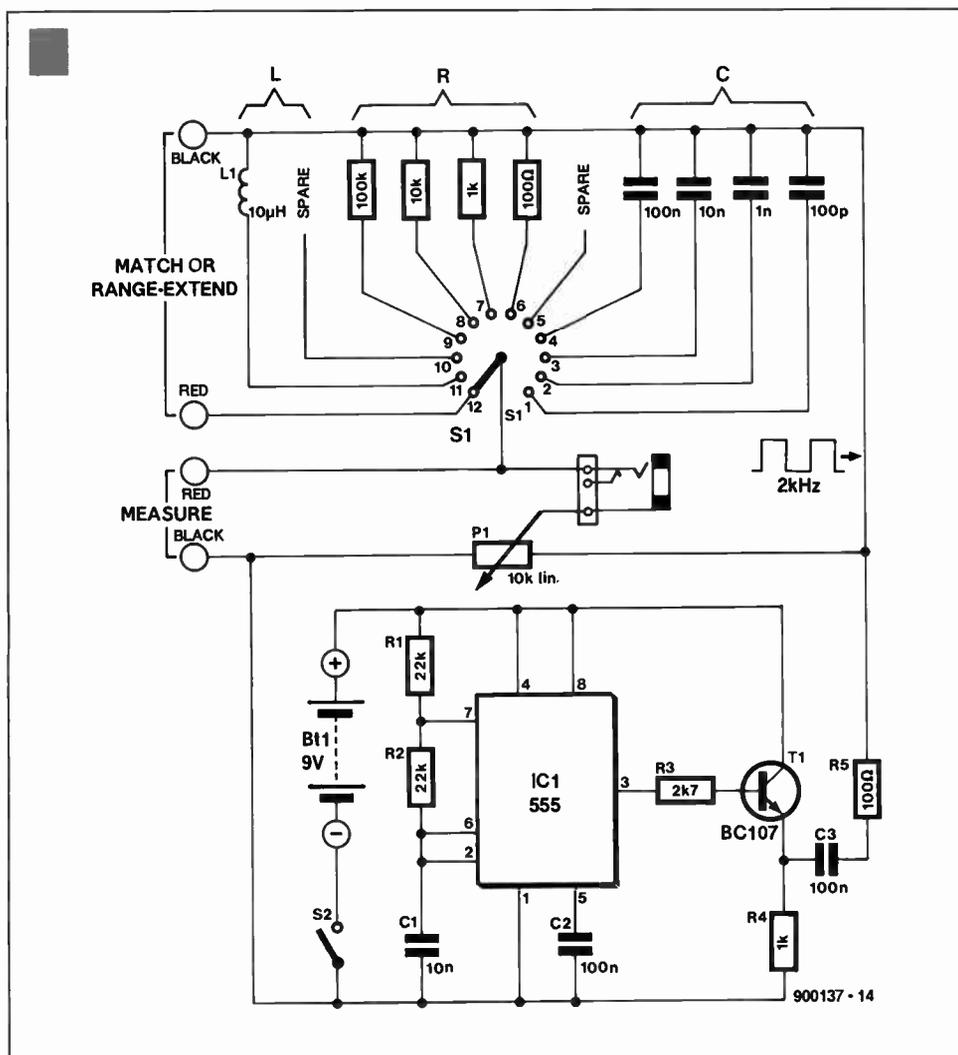


Fig. 4. Circuit diagram of the L-C-R meter.

they should be round numbers, e.g., 100 pF, 0.1 µF, etc.

Circuit design concept

The circuit diagram of the L-C-R bridge is given in Fig. 4. A rectangular wave of about 9 V_{pp} is provided by a 555, IC1, configured as an astable multivibrator, with a repetition frequency of about 2 kHz.

The 2-kHz output from the astable is buffered by an emitter follower transistor, T1, to minimize loading of the 555 output circuit by the bridge when this is switched to the lower resistance/reactance ranges.

A crystal earpiece is used for the null detector. Its high impedance offers a better audible signal than would an electromagnetic version to help with the determination of the null, particularly when measuring inductance.

Accuracy of measurement depends mainly on the accuracy of the component values switched into the circuit by the L-C-R range switch, S1, and on the quality of the linear-law potentiometer, P1, used for the balance control.

The prototype of the L-C-R bridge was built with a standard off-the-shelf linear carbon potentiometer for the balance control (a 1,000-Ω version should serve equally well), low-tolerance, high-stability resistors and capacitors, and a commercially available

moulded RF inductor of 10% tolerance.

It was considered that a single 10-µH range inductance would provide a wide enough range of inductance measurement for normal RF purposes, but provision has been made for extending the measuring range for each type of component. This can be provided permanently by wiring an additional L_b, C_b, or R_b on to the range switch, or temporarily by connecting an appropriate component across the MATCH terminals with the RANGE switch in the 'match' position.

The MATCH terminals serve also to allow value matching of a pair of external components. When the two are exactly equal in value, the null falls exactly at the '1.0' position on the ratio scale, and when not matched, the scale indicates the relative value of the component connected to the MEASURE terminals compared to that at the MATCH terminals.

Although no d.c. polarizing voltage has been included for electrolytic or tantalum capacitors, the bridge can be used for the measurement of such capacitors, without problems.

Current drain from the 9-V PP3 battery is only about 7 mA.

Construction

Because electrical shielding is not required, the components are housed in a low-cost

COMPONENTS LIST

Resistors:

2	100Ω 1% metal film	1 for range switch, 1 for calibration
2	1kΩ 1% metal film	1 for range switch, 1 for calibration
2	10kΩ 1%, metal film	1 for range switch, 1 for calibration
2	100kΩ 1%, metal film	1 for range switch, 1 for calibration
2	22kΩ	R1;R2
1	2kΩ	R3
1	1kΩ	R4
1	100Ω	R5
1	10Ω linear potentiometer	P1

Capacitors:

2	100pF 1% silvered mica	1 for range switch, 1 for calibration
2	1nF 1% silvered mica	1 for range switch, 1 for calibration
2	10nF 1% polystyrene	1 for range switch, 1 for calibration
2	100nF 5% polyester	1 for range switch, 1 for calibration
2	10nF ceramic	C1;C2
1	100nF ceramic	C3

Inductors:

1	10µH encapsulated polypropylene
1	10µH air-cored, self-wound (see text)

Semiconductors:

1	555	IC1
1	BC107	T1

Miscellaneous:

1	enclosure, ABS plastic, 120×65×40 mm, with lid
1	1-pole, 12-way rotary midget wafer switch, plastic spindle/bush
1	miniature on/off switch
1	3.5-mm panel mounting jack socket
1	crystal ear-piece
1	DIL socket 8-way
1	35-mm square section of 0.1-inch hole-spacing copper-strip board
2	4-mm terminal post, red
2	4-mm terminal post, black
1	PP3 battery with twin press stud and holder

plastic container with removable flat cover. Externally accessible components, i.e., balance potentiometer, range switch, MATCH and MEASURE terminals, ear-piece socket and battery switch, are mounted on to the removable panel.

One lead of each of the 'range' components is soldered directly to the appropriate lag-terminal of the RANGE switch, and the other lead of each component is soldered to a self-supporting ring of tinned copper wire.

The RANGE switch is a single-pole 12-position rotary midget wafer type, with a plastic spindle and fixing bush, to minimize stray capacitance which might adversely affect the measurement at the lower picofarad range. A flat on the spindle allows a push-on knob to be used, of the type which has a moveable cover-cap to allow alignment of the pointer.

The drawing in Fig. 6 shows a suitable escutcheon for the L-C-R SELECT/RANGE switch.

The linear-law carbon potentiometer used for the balance control also has a plastic spindle and fixing bush, but preferably without a flat on the spindle, to allow a grub-screw type of pointer knob to be aligned to the '1.0' mark on the ratio-scale.

The 555 integrated circuit, transistor T1, and the eight associated passive components are assembled on to a 35-mm square piece of 0.1-inch hole-spacing copper strip board. It is reasonable to use an 8-way DIL socket for the 555. The actual lay-out of the few components on the board is uncritical, hence does not warrant a guidance sketch. The finished 2-kHz oscillator board is small enough to be self-suspended by its connecting wires, but its PP3 battery may need an elementary fixing bracket or zip-strap.

Four 4-mm terminal posts for the MEASURE and MATCH pairs of terminals allow the components to be either loosely plugged in, or more securely screw-fastened to suit the circumstance.

The size of the enclosure is not critical, indeed the prototype used a plastic box of about the same general shape and size as a standard wall-socket box of 75×75×45 mm, but a box with a panel of, say, 65×120 mm would accommodate a circular scale of readable dimension plus the range switch escutcheon, with room to spare for the terminals, battery switch, and ear-piece socket.

Calibration

The ratio scale needs to be calibrated for optimum results, because the linear-resistance characteristic of the chosen balance potentiometer may not necessarily be the same as that used in the author's prototype. The sample scale shown in Fig. 5 may be used for guidance.

Although the standard potentiometer has a rotational travel of about 300 degrees, it is recommended that the usable ratio scale be confined to ± 90 degrees about centre (ratios: $\times 0.1$, $\times 1.0$, $\times 10$), or at most ± 120 degrees (ratios $\times 0.01$, $\times 1.0$, $\times 100$).

The easiest way to calibrate the scale is to remove the pointer knob and temporarily affix a circular paper-scale centrally over the fixing bush, with the '1.0' mark uppermost at 360 degrees.

The circular scale should have two circular bands, one marked 'R/L' for resistance and inductance, and the other marked 'C' for capacitance.

Plug in the ear-piece, select the 100 Ω range, and switch on the oscillator. The parts list recommends the availability of four duplicate low-tolerance high-stability resistors. These will be used as the external standards for calibration/test of the scale.

Connect the 100 Ω resistor to the MEASURE terminals, and carefully rotate the balance pot spindle until a null is obtained in the ear-piece. Loosen the grub-screw in the pointer-knob, and carefully position the knob on to the spindle with its pointer exactly at '1.0' (360 degrees) position of the scale, taking

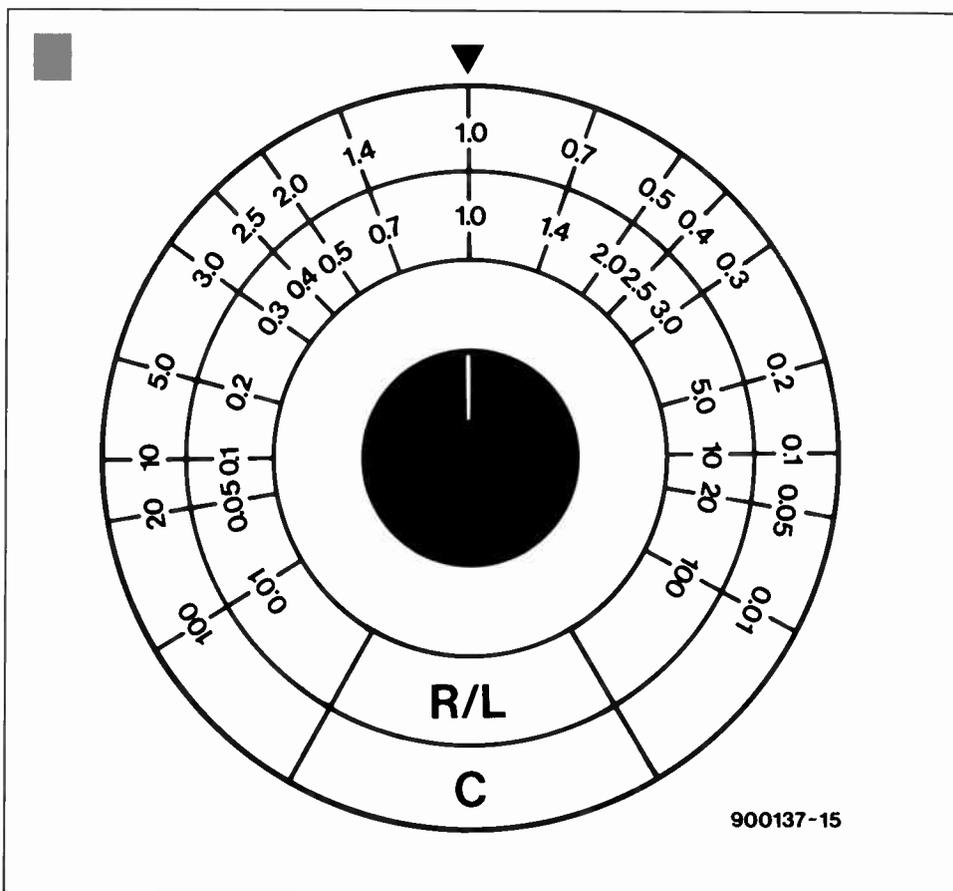


Fig. 5. Scale design for the balance control.

care not to move the spindle. Tighten the grub-screw, and rotate the knob to either side of '1.0' to check that the null is still coincident with the '1.0' mark.

Select the 1,000 Ω range and, with the 100 Ω resistor still connected, adjust the pointer for null in the ear-piece. This should occur at about 270 degrees. Mark the R/L scale ' $\times 0.1$ ' at that position (i.e., 1,000 $\Omega \times 0.1 = 100 \Omega$).

Switch to the 10 k Ω range, when the null should appear at about 240 degrees, and mark the R/L scale ' $\times 0.01$ ' at that position

(i.e., 10 k $\Omega \times 0.01 = 100 \Omega$).

Replace the 100 Ω resistor by the 1,000 Ω resistor and, with the RANGE switch set to 1,000 Ω , check that the null is at '1.0' (360 degrees).

Switch to the 100 Ω range, still with the 1,000 Ω resistor, when the null should occur at about 90 degrees. Mark the R/L scale ' $\times 10$ ' at that position (i.e., 100 $\Omega \times 10 = 1,000 \Omega$).

Replace the 1,000 Ω resistor by the 100 k Ω resistor, set the range switch to 1,000 Ω , and the null should occur at about 120 degrees, and mark the R/L scale ' $\times 100$ ' at that posi-

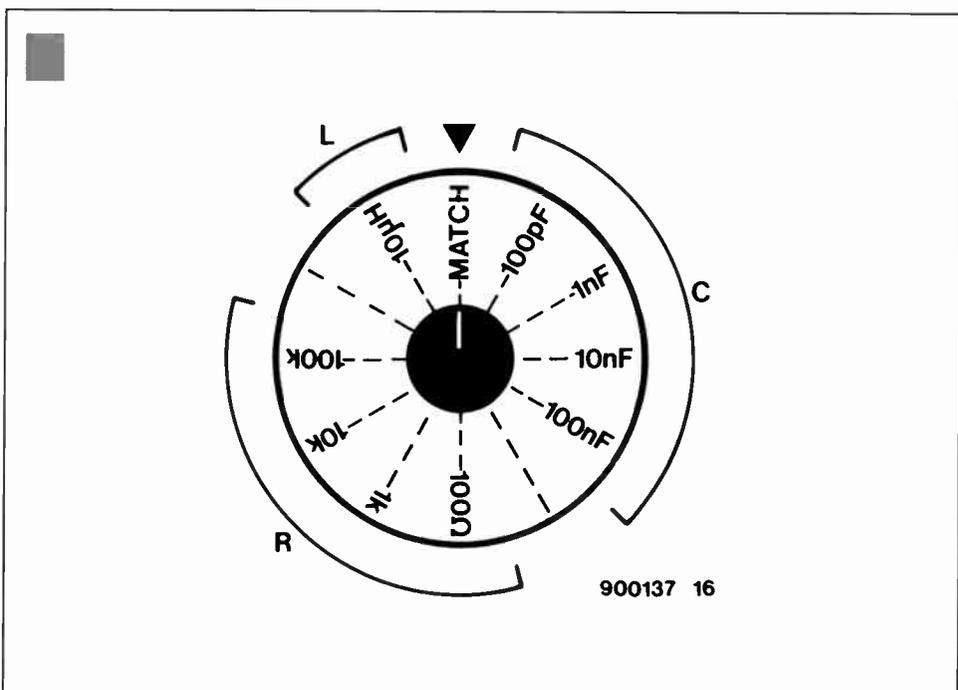


Fig. 6. Range switch escutcheon.

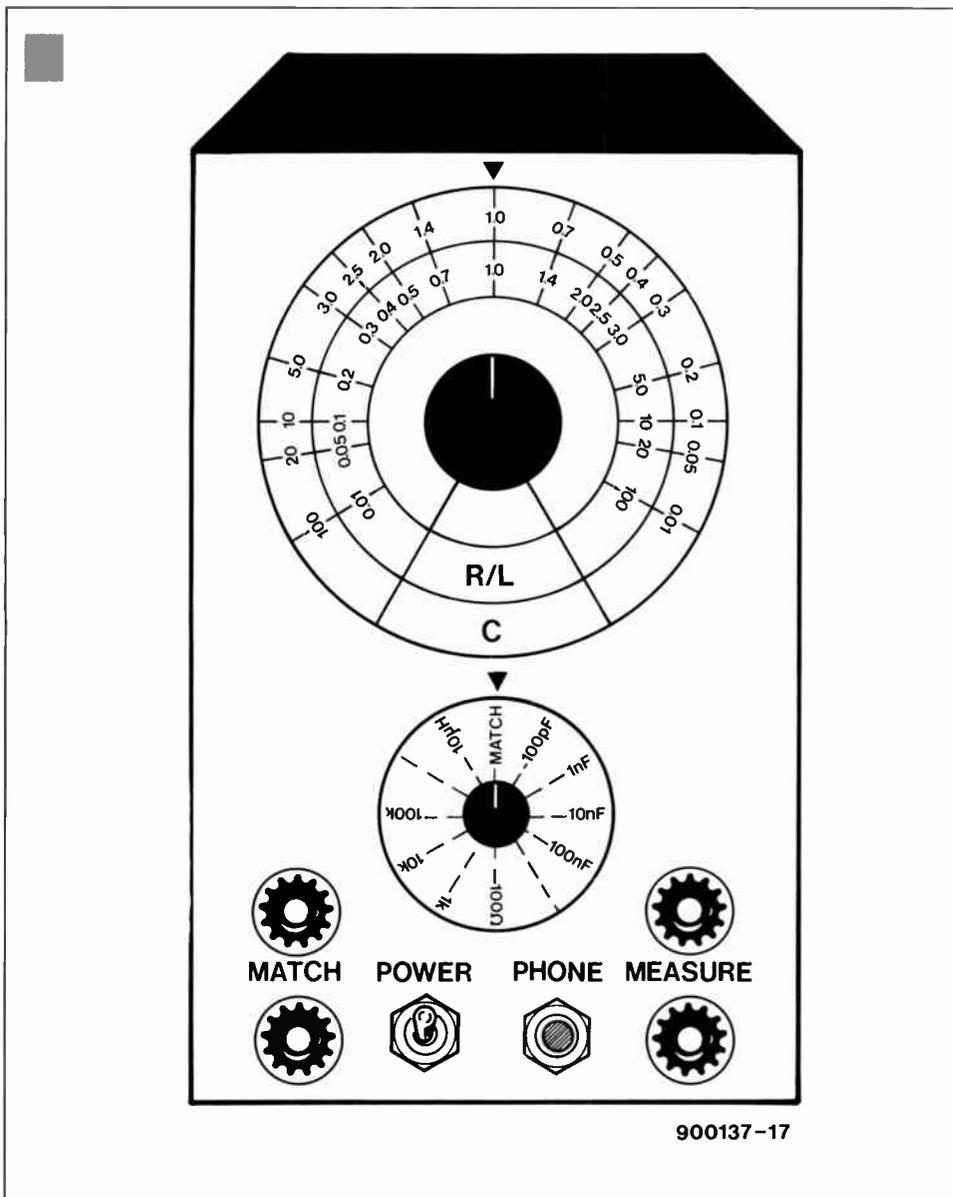


Fig. 7. Suggested front panel layout of the L-C-R bridge.

tion (i.e., $1,000 \Omega \times 100 = 100 \text{ k}\Omega$).

It will now be obvious that the ratios $\times 0.1$ to $\times 1.0$ and $\times 1.0$ to $\times 10$ each span about 90 degrees of travel, whereas the ratios $\times 0.01$ to $\times 0.1$, and $\times 10$ to $\times 100$, each span only about 30 degrees of travel. This means that calibration points beyond less than $\times 0.1$, and greater than $\times 10$, become increasingly cramped — but still very repeatable and acceptably accurate provided that care is taken with the calibration of the intermediate points in each sector.

Nulls are still very detectable even further towards the end-stops of travel, but the cramping is even more pronounced. That is where the advantage of a large diameter scale becomes apparent. The majority of *in vivo* measurements will however fall within the ± 90 degree bands, where the scale is uncramped and clearly readable.

To calibrate the intermediate scale-points, it is advisable to restrict them to the 120 degree sectors on either side of '1.0', and to use whole numbers for the external calibration resistors rather than the decimal values of the 'preferred' series. The easiest way to do this is to use a $1,000 \Omega$ standard linear-law potentiometer with a wire con-

nected to its centre tag, and another to one of its outer tags, and to set it to a selection of values by means of an ohm-meter, i.e., 200, 300, 400 ... 900Ω , etc. These values are then used to establish the intermediate scale points, i.e., $\times 0.02$, $\times 0.03$, $\times 0.04$... $\times 0.09$ using the $10 \text{ k}\Omega$ range; $\times 0.2$, $\times 0.3$, $\times 0.4$... $\times 0.9$ on the $1,000 \Omega$ range; and $\times 2$, $\times 3$, $\times 4$... $\times 9$ using the 100Ω range.

Similarly with values between $20 \text{ k}\Omega$ and $90 \text{ k}\Omega$ on a $100 \text{ k}\Omega$ potentiometer, to give scale points of $\times 20$, $\times 30$, $\times 40$... $\times 90$ using the $1,000 \Omega$ range.

The resistance calibration scale applies equally to the measurement of inductance, but a mirror-image scale is required for capacitance measurement. The same calibration positions pertain, but the C scale must be marked with the inverse values from the R/L scale points, rounded up for practical purposes, i.e., as shown in the table. Calibration is now complete, and the bridge is ready for use.

Does it work?

Yes. Results when measuring resistance can be accepted with confidence, as can mea-

R/L marking	C marking
0.1	10
0.2	5.0
0.3	3.3
0.4	2.5
0.5	2.0
0.6	1.7
0.7	1.4
0.8	1.3
0.9	1.1
1.0	1.0
0.01	100
0.02	50
20	0.05
80	0.013

urements of capacitance, provided that the capacitors being measured are of good electrical quality. However, regarding the measurement of inductance, it must be borne in mind that the balance equations have been simplified by assuming zero resistance in the small values of inductance to be measured.

In practice, this will not be the case, depending on the construction of the particular RF coil. For example, the moulded $10 \mu\text{H}$ inductor used in the prototype has a series resistance of about 0.3Ω owing to the very thin wire used for the coil, and whilst this does not unduly detract from the calibration accuracy when measuring inductors wound with similarly thin wire gauges, it does create inaccuracies when trying to measure the values of coils with heavier gauge wires, e.g., 14 to 24 SWG (14 to 25 AWG).

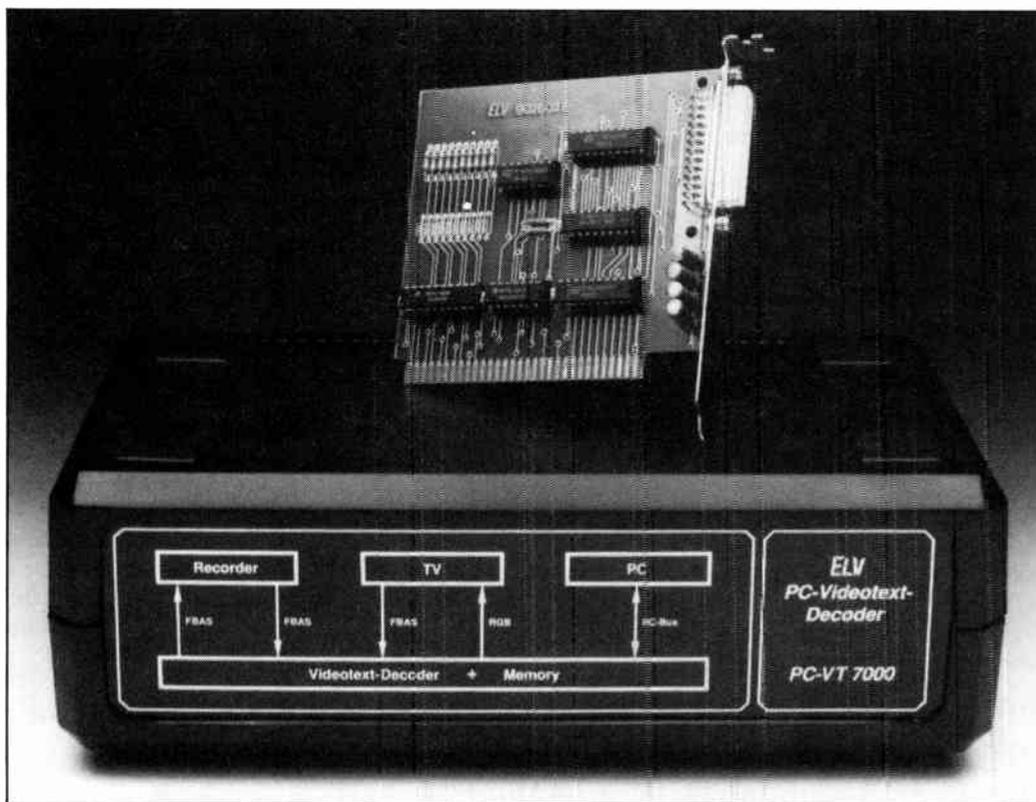
The solution to the measurement of inductance of heavier gauge coils is nevertheless quite simple, by using the MATCH terminals with an alternative 'standard' $10 \mu\text{H}$ inductor connected across them, but wound from thick wire. A suitable alternative $10 \mu\text{H}$ air-cored coil can be constructed easily by close-winding 24 turns of 20 SWG (1.0 mm dia., or 21 AWG) enamelled copper wire with a winding-span of about 24 mm on to a PVC former of 25 mm outside diameter; or 32-turns of 20 SWG wire by 32 mm span on to a 20 mm outside o.d. PVC former; or 69 turns by 69 mm span of 20 SWG wire on to a 12.5 mm former. In each case, allow 10 mm end-tails.

Measurement of thicker-wire unknown inductance now follows normal procedure, but with the switch set at its 'match' position instead of the 'L' position, and with the $10 \mu\text{H}$ thick-wire standard inductor connected to the MATCH terminals.

To get the feel of the bridge, try measuring a selection of L, C and R components, and the effect of tolerance on nominal values. Then try matching component values by connecting pairs of nominally equal values to the MATCH and MEASURE terminals until null is obtained at '1.0' on the scale. Try also extending/modifying the range of measurement by connecting a known value component to the external MATCH terminals. And for interest only, try measuring the relative effect of an iron-dust slug versus a brass slug in a low-value RF inductance. ■

PC-CONTROLLED VIDEOTEXT DECODER PC-VT7000

PART 2: I²C INTERFACE AND CONSTRUCTION OF THE UNIT



This second and concluding part of the article deals with the operation of the I²C PC insertion card that forms the link between the computer and the main decoder. As usual, we close off the article with full constructional details of the project.

THE term I²C refers to a control and data bus system developed by Philips Components for use on ICs in consumer electronics equipment (Ref. 2). The I²C system is used here to control the SDA5243 ECCT on the main decoder board (see Part 1 of this article). A special PC insertion card has been developed to ensure the fastest possible two-way communication between the ECCT and the PC, with the aid of the I²C bus.

The block diagram of the I²C bus controller card is shown in Fig. 6. At the side of the PC extension slot, an address comparator compares the I/O addresses supplied by the PC with a user-defined address. If the addresses match, the comparator supplies an appropriate enable signal to a 'control logic' block, which, in turn, switches on two data-bus buffers and an 8-bit D-latch. When the card is written to with an appropriate I/O address, data on the PC databus is copied to an 8-bit D-latch. The open-collector drivers

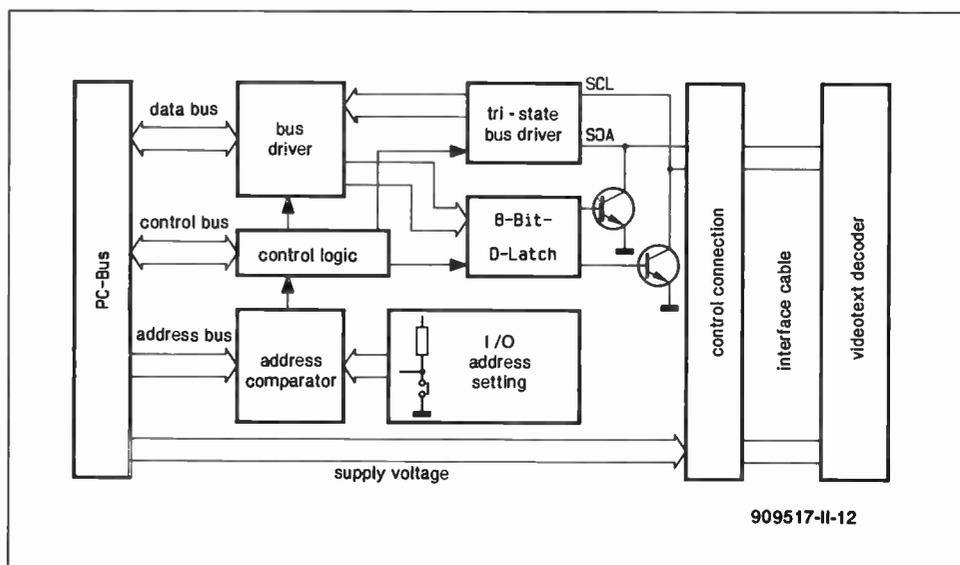


Fig. 6. Block diagram of the I²C card. This forms an interface between the PC and the main decoder, which is a separate unit in this project.

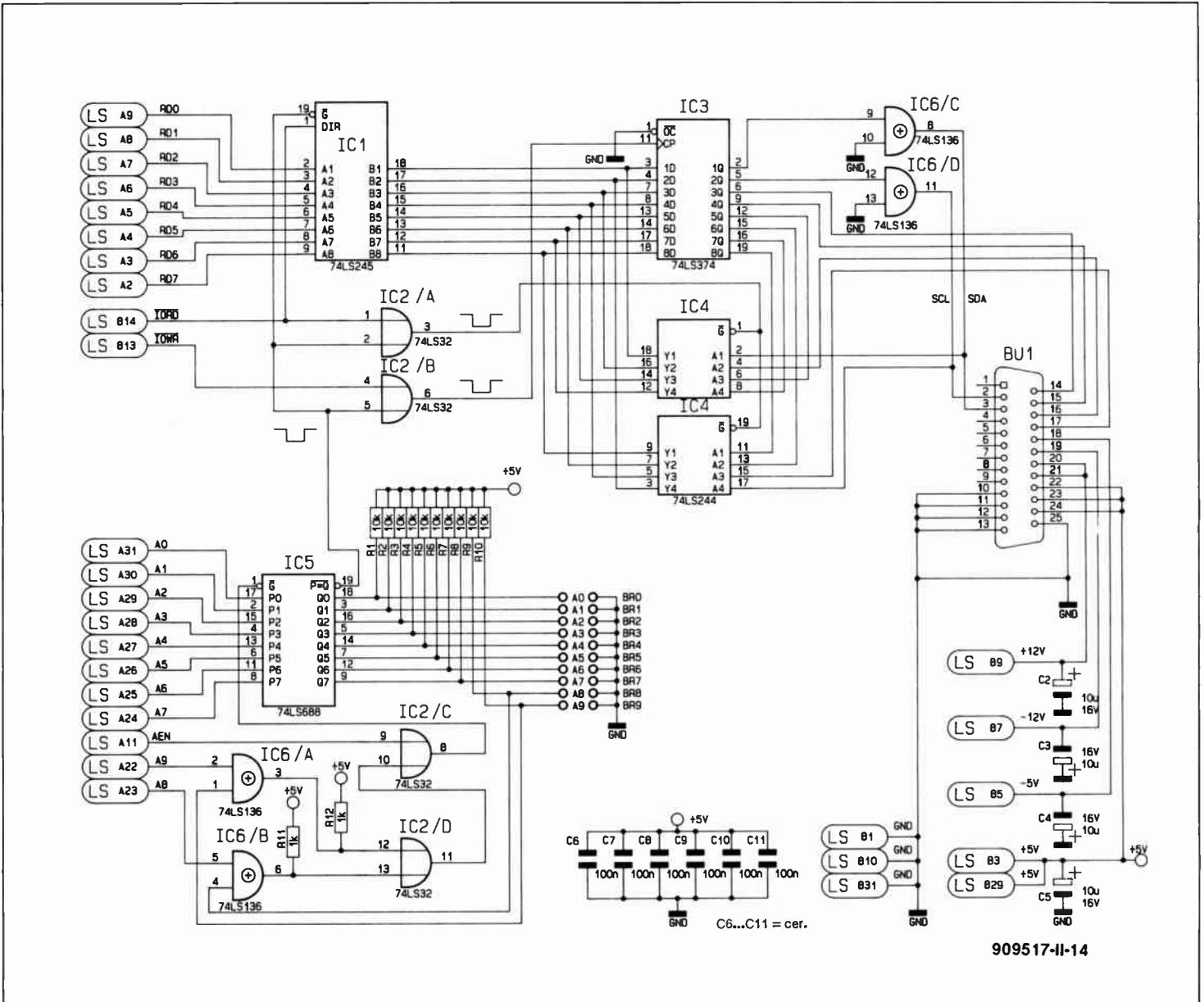


Fig. 7. Circuit diagram of the I²C card. Basically an I/O mapped PC interface, the circuit provides the bidirectional SCL and SDA lines.

at the outputs of the D-latch provide the transmit function of the insertion card for two I²C lines, SCL (serial clock) and SDA (serial data). Since these lines are bidirectional, provision is also made to convey information from the videotext decoder to the I²C card. A 3-state busdriver is enabled when the PC reads from the card address. The SCL and SDA information captured by the 3-state busdriver is fed to the PC via the databus buffer.

Circuit description of the I²C card

Figure 7 shows the detailed circuit diagram of the PC-compatible I²C interface card. The bidirectional databus buffer is formed by IC1, a 74LS245. The data direction is switched under the control of PC bus line \overline{IORD} (pin B14), which is also connected to IC2A. The second PC control line, \overline{IOWR} (pin 13) is connected to another gate, IC2B. The two OR gates IC2A and IC2B form the 'control logic' block shown in Fig. 6. Their function is enabled by the address compar-

tor when the card is addressed by the PC. The address of the card in the PC's I/O map is defined by wire jumpers BR0 to BR9. A '0' is set for a particular address bit by fitting the associated wire. The address comparator, IC5-IC6A, is not enabled until PC bus line AEN is logic high, while at the same time either \overline{IORD} or \overline{IOWR} is logic low. If this condition is satisfied, and if the card is addressed by the PC, the output of IC5, pin 19, changes from high to low, thus enabling the rest of the circuit via IC2A-IC2B. The logic level on the \overline{IORD} and \overline{IOWR} lines determines whether the PC writes to 8-bit D-latch IC3 (a 74LS374), or reads from 3-state bus driver IC4 (a 74LS244). Outputs 1Q and 2Q of latch IC3 are connected to the inputs of XOR gates IC6C and IC6D. These LS-TTL gates have open-collector outputs, and function as drivers for the I²C lines, SCL and SDA. They have no logic function, and are equivalent to the two transistors shown in Fig. 6. SCL and SDA information received from the videotext decoder reaches the I²C card via inputs A1 and A4 of 3-state bus driver IC4.

The signals on outputs 5Q to 8Q of IC3 are

fed back to the inputs of the IC via buffer IC4. This allows the card to be detected by the control software, and an error message to be generated when it is not fitted or not found at the requested address.

Outputs 3Q and 4Q of IC3, and inputs A2 and A3 of IC4, are taken to a 25-way D-connector, BU1, for future extensions. The 25-way connector also serves to connect the approximately 2-m-long cable to the videotext decoder. Apart from data and commands, this cable also carries the +12 V, -12 V, -5 V and +5 V supply voltages, and a common ground line, from the PC to the decoder board.

Construction

Briefly recapitulating, the PC-VT7000 consists of two units: the main decoder, which is housed in a black, 7000-series ABS enclosure, and the I²C card, which is inserted into a free extension slot in your PC. These two units are linked by a cable.

Decoder board

The construction is best started by fitting all

35 wire links on the main decoder board (Fig. 8). Next, fit the low-profile components, followed by the higher parts. Note that the two slide switches at the rear edge of the PCB, between the two SCART sockets, must be fitted horizontally. Insert and solder six solder pins into the respective holes on the PCB, and use these to secure the terminals of the slide switches. The front sides of the switches must align with the PCB edge, i.e., the plastic part to operate the switch must protrude from the rear panel of the enclosure.

The two SCART sockets are mounted by gently pushing their plastic side locks into the holes provided in the PCB. Next, the 21 pins of each socket are soldered at the track side. For additional support, the SCART sockets are screwed to the rear panel of the enclosure.

The PC insertion card is connected to the decoder by a 2-m-long, 25-way flatcable. At the side of the decoder, this cable is connected to a 26-way header, STL₁ (of which one pin is not used). The short pins of this header are inserted into the PCB holes and subsequently soldered. The cable between the decoder and the I²C card has a 26-way IDC socket at one end, and a 25-way male sub-D plug at the other end. The 26-way IDC connector is plugged on to header STL₁ on the decoder board.

Pin header STL₂ is inserted and soldered like STL₁. STL₂ provides a number of important signals in the system, and is intended for measurements and extensions. Similarly, the eight solder pins near SCART socket BU₂ are intended for (optional) use of the stereo sound inputs and outputs.

As will be recalled from the circuit descriptions, the PC-VT7000 is powered from the computer. All the necessary supply voltages are carried via the I²C card and the cable between this and the decoder.

I²C bus controller card

The lay-out of this double-sided, through-plated board is shown in Fig. 9. The board has pre-tinned contacts for insertion into a PC extension slot.

First, fit the ten wire links, A0 through A9. Leave a little room between these wires and the PCB surface, so that they can be cut later to set the card address. Next, fit the resistors, the capacitors (four electrolytic, and six ceramic types), and then the six ICs.

Align the angled terminals of the 25-way female sub-D connector with the relevant holes in the PCB, and solder them carefully at the track side, taking care to avoid shorting adjacent pins by applying too much solder tin. Next, fit the support bracket supplied with the kit. Place it over the D-connector, and secure it with two M3 screws and nuts. In the PC, remove the rear panel bracket at the location of the slot that you intend to use for the I²C card.

Before fitting the card into the PC, set its address by opening wire jumpers BR0-BR9 as required. Details on the hardware address selection are provided by the READ.ME file on the diskette supplied with the kit. Ready-assembled and aligned I²C boards supplied

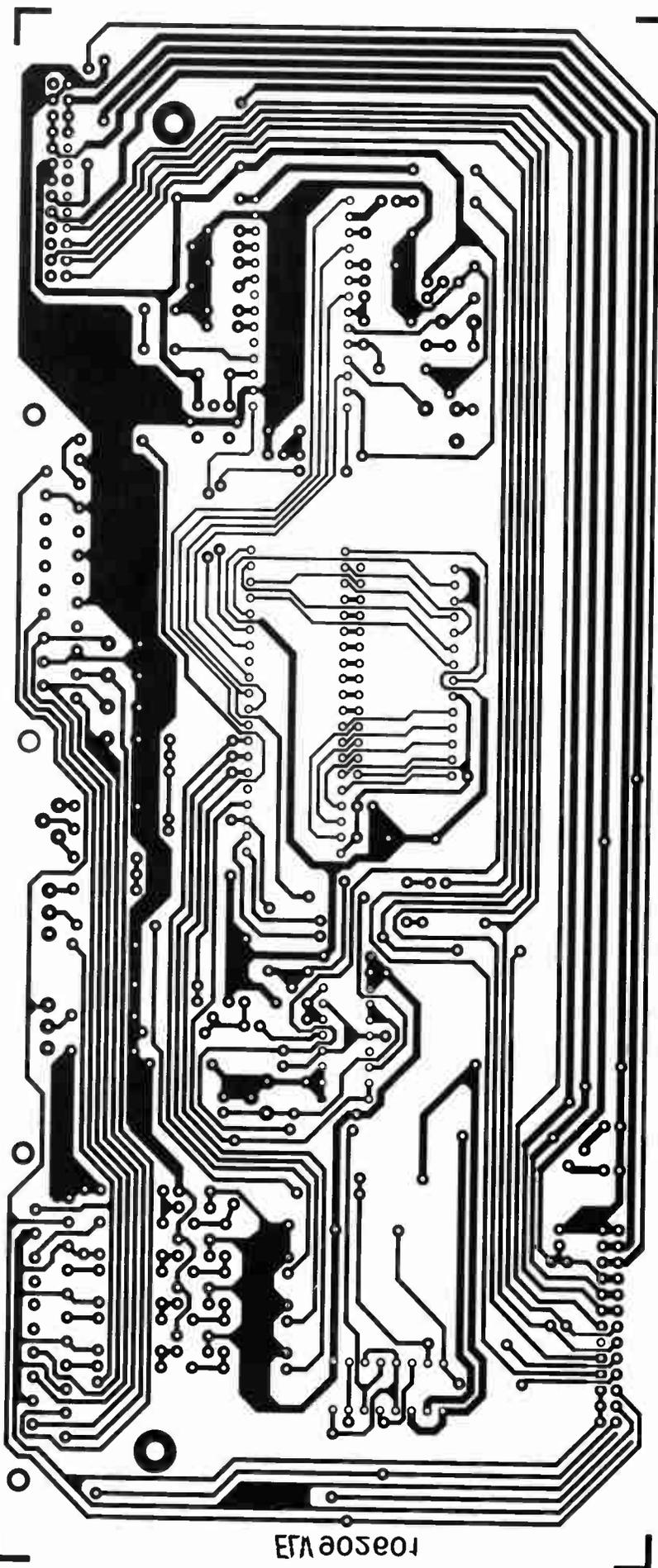


Fig. 8a. Track layout of the single-sided decoder board.

COMPONENTS LIST

DECODER BOARD

Resistors:

- | | | |
|---|---------------|-----------------|
| 6 | 75Ω | R1-R6 |
| 2 | 100Ω | R41;R42 |
| 6 | 220Ω | R7-R10;R34;R37 |
| 1 | 270Ω | R26 |
| 2 | 330Ω | R25;R32 |
| 1 | 470Ω | R30 |
| 3 | 820Ω | R12;R14;R16 |
| 3 | 1kΩ | R24;R28;R29 |
| 1 | 1kΩ2 | R21 |
| 4 | 1kΩ5 | R11;R13;R15;R35 |
| 2 | 2kΩ2 | R17;R31 |
| 1 | 3kΩ3 | R23 |
| 1 | 4kΩ7 | R20 |
| 2 | 10kΩ | R38;R40 |
| 1 | 12kΩ | R19 |
| 1 | 68kΩ | R22 |
| 2 | 100kΩ | R33;R39 |
| 1 | 100Ω preset V | R36 |
| 1 | 100Ω preset V | R27 |

Capacitors:

- | | | |
|---|---------------|-----------------|
| 2 | 15pF | C19;C25 |
| 1 | 18pF | C13 |
| 1 | 47pF | C15 |
| 1 | 100pF | C24 |
| 1 | 220pF | C8 |
| 1 | 270pF | C23 |
| 1 | 470pF | C21 |
| 1 | 1nF | C20 |
| 1 | 10nF | C18 |
| 1 | 22nF | C22 |
| 2 | 47nF | C10;C12 |
| 1 | 68nF | C7 |
| 6 | 100nF ceramic | C1-C4;C16;C27 |
| 1 | 220nF | C9 |
| 1 | 1μF 16V | C11 |
| 1 | 2μF2 16V | C6 |
| 5 | 10μF 25V | C17;C26;C30-C32 |
| 1 | 22μF 16V | C5 |
| 3 | 100μF 16V | C28;C29;C37 |
| 1 | 40pF trimmer | C14 |

Semiconductors:

- | | | |
|---|----------|-------|
| 1 | SDA5231 | IC1 |
| 1 | SDA5243 | IC2 |
| 1 | 6264 RAM | IC3 |
| 1 | CD4052 | IC5 |
| 1 | CD4053 | IC4 |
| 6 | BC548 | T1-T6 |
| 4 | 1N4148 | D1-D4 |

Miscellaneous:

- | | | |
|----|---|---------|
| 1 | 6 MHz quartz crystal | Q1 |
| 1 | 13.875 MHz quartz crystal | Q2 |
| 1 | 10μH inductor | L1 |
| 2 | SPDT slide switch | S1;S2 |
| 2 | PCB-mount SCART socket | BU1;BU2 |
| 2 | 26-way pin headers | |
| 14 | solder pin, 1.3 mm dia. | |
| 1 | printed-circuit board | |
| 1 | enclosure type 7000 | |
| 70 | cm silver-plated wire | |
| 1 | Flatcable, length 2 m, 25-way, ready-assembled with D-connector and IDC connector | |

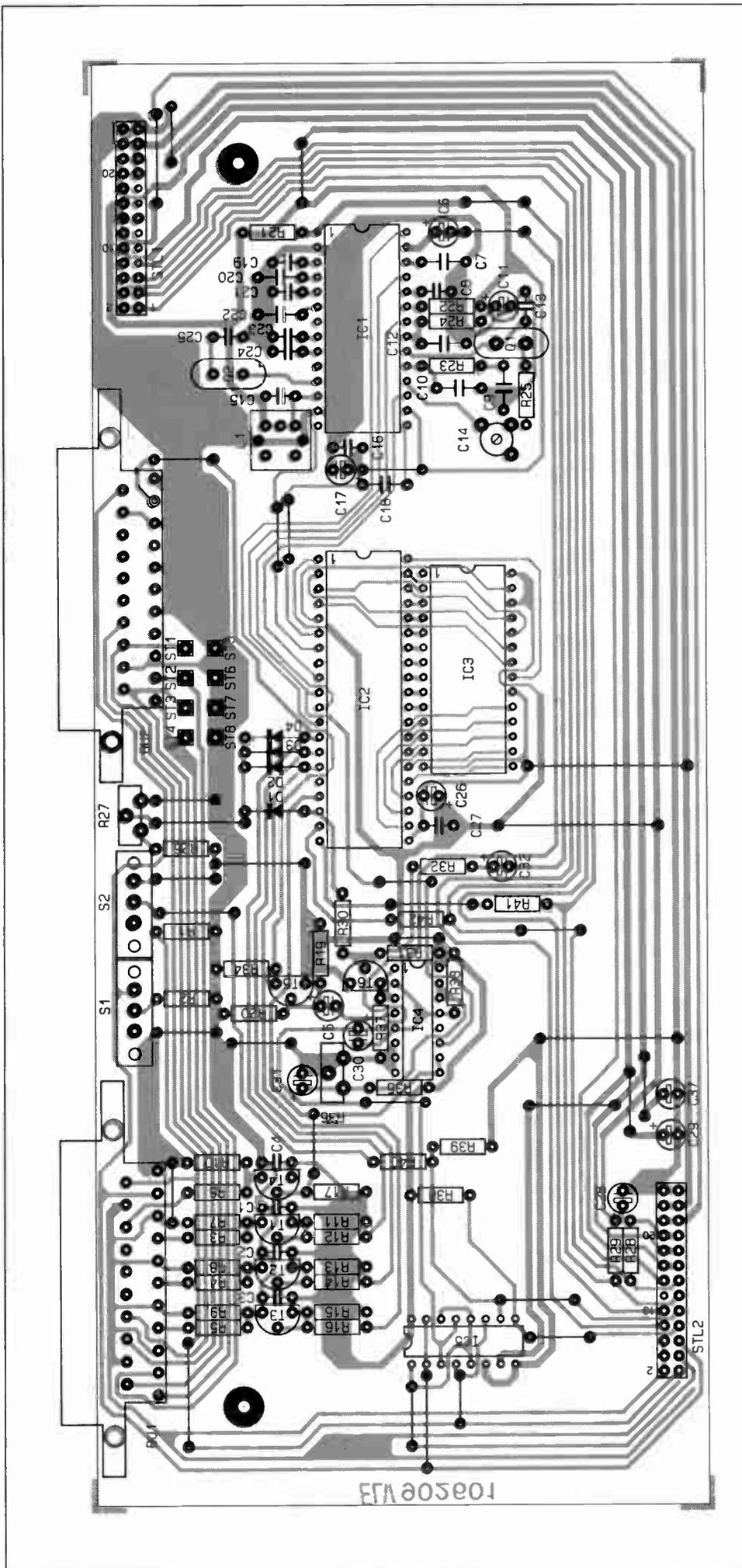


Fig. 8b. Component mounting plan of the decoder board.

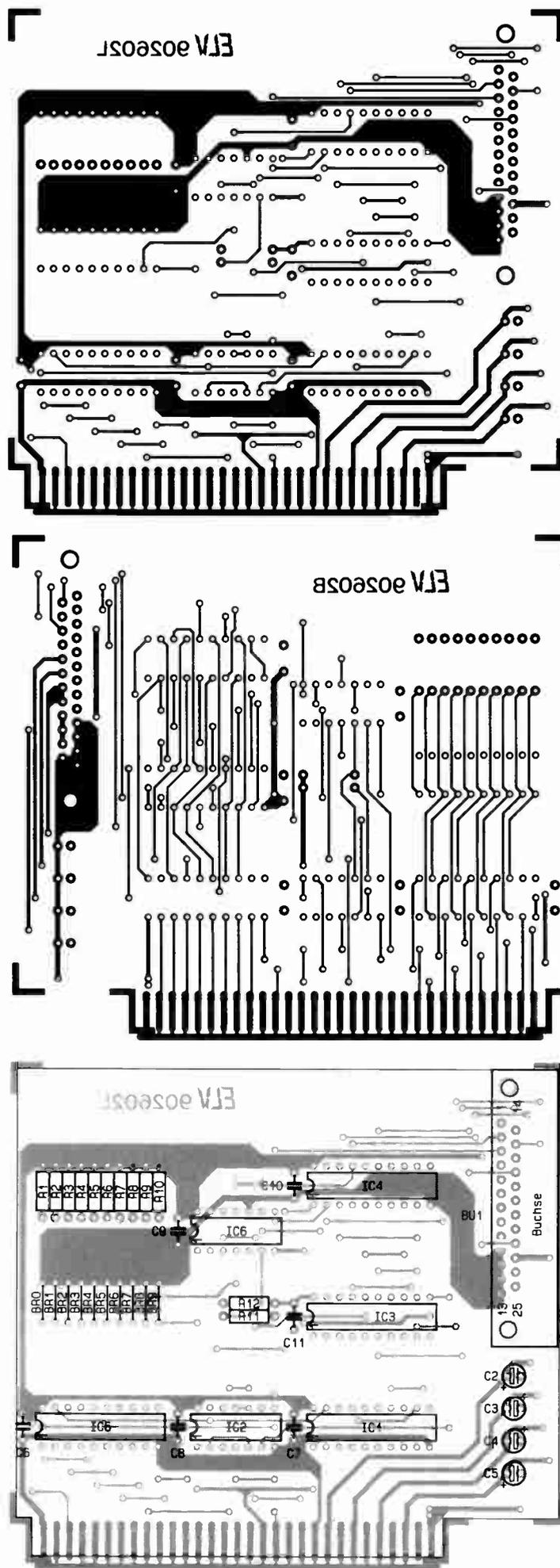


Fig. 9. Double-sided printed circuit board for the I²C interface card.

WorldRadioHistory

COMPONENTS LIST

I²C PC INSERTION CARD

Resistors:

2	1k Ω	R11;R12
10	10k Ω	R1–R10

Capacitors:

6	100nF ceramic	C6–C11
4	10 μ F 16V	C2–C5

Semiconductors:

1	74LS32	IC2
1	74LS136	IC6
1	74LS244	IC4
1	74LS245	IC1
1	74LS374	IC3
1	74LS688	IC5

Miscellaneous:

1	25-way PCB-mount D-connector BU1
1	PC card support bracket
2	M3x6 mm screw
2	M3 nut
12	cm silver-pated wire
1	printed-circuit board

by ELV are set to operate at address 300H.

Alignment

The decoder needs to be adjusted before it is fitted into the enclosure. Although a relatively complex circuit, the decoder is remarkably simple to align.

Start by connecting a TV set to SCART socket BU1. During the alignment, the TV set has the double function of a CVBS signal source, and a display for the Teletext pages.

Run the program on the PC, and call up a Teletext page, say, number 100. If the decoder is correctly aligned, the page will appear on the TV. Without adjustment, however, the TV picture is probably unsteady — the picture may move horizontally, or may be corrupted by diagonally moving lines. Carefully adjust trimmer C14 until the picture synchronizes correctly.

Inductor L1 in the data-clock filter comes pre-aligned with the kit, and must not be adjusted.

Proceed with the adjustment by setting the clamping level for the Teletext subtitling with the aid of preset R36. The following adjustment procedure is required only if Teletext subtitles are to be recorded on a VCR.

Connect a VCR to SCART socket BU2, and switch it to stand-by. The video signal fed to pin 19 of BU2 is taken from pin 20 and routed to pin 19 of BU1 (TV). To prevent the TV switching to RGB input mode, temporarily connect pin 16 of BU1 to ground.

Use the control software to select the superimpose mode. Next, adjust preset R36 until the characters appear clearly in the picture, i.e., with the best possible contrast ratio, and without distortion or excessive brightness. Although this adjustment is perfectly feasible simply by looking at the TV picture, it may also be carried out with the aid of an

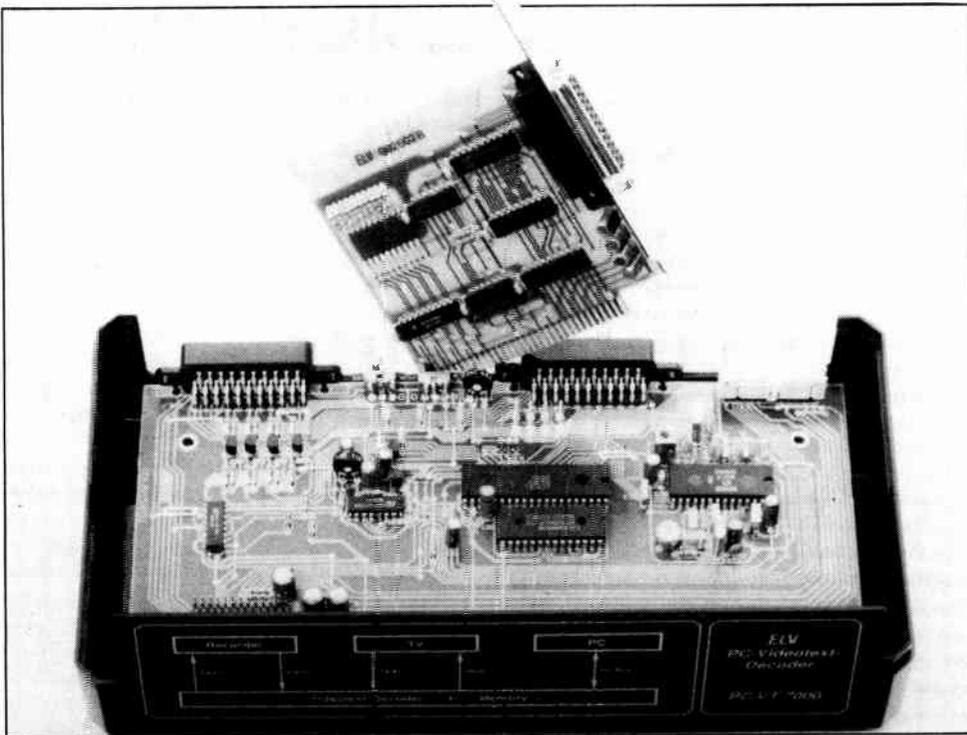


Fig. 10. Opened prototype of the decoder, and the associated I²C card.

oscilloscope. Connect the scope to the collector of T5, and adjust R36 until the black level of the superimpose signal matches that of the background video signal. This completes the adjustment of the PC-VT7000.

Final assembly

If this has not already been done, mount the rear panel to the decoder board, so that the SCART sockets and the plastic pins of the two slide switches protrude from it. The flat-cable is inserted via the slot provided at the right-hand side of the rear panel.

Fit the completed and adjusted decoder

PCB into the lower half of the enclosure supplied with the kit. The ventilation slots are at the front side. Remove the four square blocks from the underside of the bottom half of the enclosure, and insert four M4×70 mm screws into the holes. At the inside of the enclosure, place two 1.5×10 mm dia. plastic washers over each screw at the front side, and one washer over each screw at the rear side.

The decoder board is fitted by passing the two screws at the rear of the enclosure through the two holes in the PCB. At the same time, fit the rear panel. Next, place the four 60-mm-long plastic PCB spacers over the screw ends, and mount the front panel.

A complete kit of parts for the Videotext decoder is available from the designers' exclusive worldwide distributors:

ELV France
B.P. 40
F-57480 Sierck-les-Bains
FRANCE

Telephone: +33 82837213
Facsimile: +33 82838180

Carefully lift the bottom enclosure half, and place two pencils or a folded handkerchief underneath it, so that the heads of the four screws rest on the desk while the enclosure half is a little higher. Carefully place the top enclosure half on to the lower half (the ventilation slots are at the rear side), and temporarily insert four screws into the holes. The ends of these screws partly enter the PCB spacers, and serve to keep these aligned (centred) with the holes in the top half of the enclosure. Now carefully lower the top half. Draw one corner of the enclosure over the edge of the desk, capture the screw at the underside, and push it upwards so that it ejects the screw at the top. Fit an M4 nut, and secure the screw from the underside. The other three screws are fitted likewise. Finally, push-fit the four blocks at the underside, the rubber feet, and the four square covers at the top side of the enclosure. ■

References:

1. "Video line selector", *Elektor Electronics* April 1990.
2. "Inter-IC communications", *Elektor Electronics* September 1990.

Appendix: SAA5243 ECCT register functions

D7	D6	D5	D4	D3	D2	D1	D0
TA	7+P/ 8 BIT	ACQ. ON/OFF	GHOST ROW ENABLE	DEW/ FULL FIELD	TCS ON	T1	T0
-	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
-	-	-	PRD4	PRD3	PRD2	PRD1	PRD0
-	-	-	-	-	A2	A1	A0
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
STATUS ROW BTM/TOP	CURSOR ON	CONCEAL/ REVEAL	TOP/ BOTTOM	SINGLE/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
-	-	-	-	CLEAR MEM.	A2	A1	A0
-	-	-	R4	R3	R2	R1	R0
-	-	C5	C4	C3	C2	C1	C0
D7 (R/W)	O6 (R/W)	O5 (R/W)	O4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)

- bit does not exist

R1	Mode	T0, T1	Interlace/non-interlace 312/313 line control.
R2	Page request address	TCS ON	Text composite sync or direct sync select.
R3	Page request data	DEW/FULL FIELD	Field flyback or full channel mode.
R4	Display chapter	7+P/8-BIT	7 bits with parity checking or 8-bit mode.
R5	Display control (normal)	TA, TB	Test bits; 0 for normal operation.
R6	Display control (newsflash/subtitle)	R2 page request address	Start column for page request.
R7	Display mode	START COLUMN	Selects one of 4 acquisition circuits.
R8	Active chapter	ACQ CCT	Selects bank of 4 pages addressed for acquisition.
R9	Active row	BANK SELECT	Determines which of 8 pages is displayed.
R10	Active column	R4 Display chapter	For normal and newsflash/subtitle.
R11	Active data	R5, R6 Display control	Picture on.
		PON	Text on.
		TEXT	Contrast reduction on.
		COR	Background colour on.
		BKGND	
		R7 Display mode	Boxing function allowed on row 0 (row 1-23, 24).
		BOX ON 0 (1-23, 24)	Row 25 displayed above or below main text.
		STATUS ROW BTM/TOP	Active chapter, row, column and data information written to or read from page memory via the I ² C bus.
		R8 to R11	

ERROR DETECTION AND CORRECTION

by Brian Patrick McArdle

Telecommunications channels are not so reliable that data can be passed over them without corruption. Since data communications has become important, satisfactory methods to identify and, if possible, correct errors have been developed.

CONSIDER the transfer of data as in Fig. 1 between modems over a telephone line or radio link. The channel is corrupted by noise, which could result in a receiver detecting a 1 instead of a 0 or vice versa. If this were to happen in a number of places in a message, the effect could be disastrous: the message might be completely unintelligible. Obviously, there is a need to be able to identify incorrect data bits. The subject is known as **error detection and correction**.

Parity

Parity is a familiar concept and is explained in most technician text books. Consider a block of seven bits that is given an additional bit, known as the parity bit, so that the total block becomes eight bits. The term 'parity' refers to the entire new block and there are two categories.

(a) Even parity means that a block has an even number of 1s. For example, if the data is 1 0 1 0 1 0 1, which has four 1s and three 0s, the parity bit would be 0 giving four 1s and four 0s. The block would become 0 1 0 1 0 1 0 1 with the parity bit as the MSB which is the usual location.

(b) Odd parity if it has an odd number of 1s. The previous example would be 1 1 0 1 0 1 0 1 with five 1s and three 0s.

The 8-bit ASCII code has seven data bits and a parity bit. Thus, the ASCII alphabet has a total of $2^7 = 128$ different symbols. The 8th bit for each symbol is chosen to give even parity. If an error occurs in transmission as in Fig. 1, a parity check would reveal an erroneous symbol. The receiver could ignore the particular symbol, provided that such an occurrence did not happen too often, or, alternatively, request a retransmission.

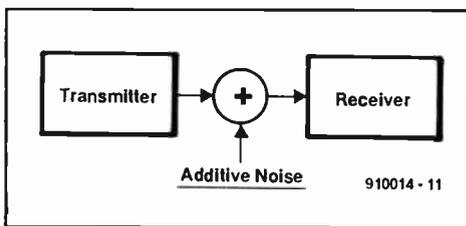


Fig. 1. Communications channel.

In reality, a parity check on each symbol gives very limited protection. The obvious

problem is that two errors within a symbol could cancel each other. Alternatively, when an erroneous symbol is identified, a receiver still cannot deduce the incorrect bit within the block and, consequently, correction is out. Therefore, although the addition of a parity bit into a block is the basis of error detection, it is rarely satisfactory. To identify an incorrect symbol is one thing, but to correct an error in one bit is quite another. The next section explains a method to identify and correct single-bit errors.

Block codes

In the following arrangement, a block consists of data bits plus check bits. For example, a block of size n would have r data bits and $k = n - r$ check bits. The check bits are derived from the data bits. In reality, they are parity bits that are determined by various linear combinations of data bits. For the present, it is assumed that only one error will occur in each block. The significance of this point will be discussed in more detail later on. For a block of size n , there is a total of $2^{n-k} = 2^r$ errors where the corruption is limited to one bit per block. The k check bits can have $(2^k - 1)$ different combinations. This means that at most $(2^k - 1)$ errors can be detected. Hence, there is a requirement that $(2^k - 1) \geq n$ in the values that can be chosen for r and k . For example, if $k = 3$, $(2^3 - 1) = 7$, which means that $n = 7$ and $r = 4$. Therefore, three check bits can check up to four data bits only. The coded block would be $[d_4 d_3 d_2 d_1 c_3 c_2 c_1]$ or some transposition of this order.

In mathematical terms, the encoding operation can be described with the use of a matrix as follows.

$$\begin{bmatrix} 100\dots 0 \\ 010\dots 0 \\ 001\dots 0 \\ \dots\dots\dots \\ 000\dots 1 \\ g_{r+1,1} \dots g_{r+1,r} \\ \dots\dots\dots \\ g_{n,1} \dots g_{n,r} \end{bmatrix} \begin{bmatrix} d_r \\ d_{r-1} \\ \cdot \\ d_1 \\ \cdot \\ c_k \\ \cdot \\ c_1 \end{bmatrix} = \begin{bmatrix} d_r \\ d_{r-1} \\ \cdot \\ d_1 \\ \cdot \\ c_k \\ \cdot \\ c_1 \end{bmatrix}$$

$$c_k = \sum_{j=1}^r g_{r+1,j} d_{r+1-j} \text{ mod } 2 \quad [\text{Eq. 1}]$$

The matrix has n rows and r columns, which correspond to the lengths of the coded and data blocks respectively. The top part is an $(r \times r)$ identity matrix that does not require any explanation. The bottom part is a $(k \times r)$ matrix that generates c_1 to c_k bits from the d_1 to d_r bits. All the coefficients are 0 or 1 and the arithmetic is modulo 2. The requirement is that, if an error occurs in a data bit, the check bits will be able to identify the particular bit in question, which can be corrected. The correction process is simply to replace a 1 by a 0 or vice versa.

The next step is to devise a simple method to identify the exact location of an incorrect bit within the block. The **Hamming Code** is examined as a suitable example because it is widely known. For instance, a block of seven bits consists of four data bits and three check bits in the following format:

position:	7	6	5	4	3	2	1
bit:	d_7	d_6	d_5	c_4	d_3	c_2	c_1

in which the data and check bits are indicated as d and c respectively and d_7 as the most significant bit (MSB). As would be expected, the position of these bits within the overall block is very significant. The positions 3, 5, 6, 7 can be represented as various combinations of 1, 2, 4. Thus, if d_3 is incorrect, c_1 and c_2 will not be validated and so on. The combinations that give c_1 , c_2 , and c_4 in terms of d_3 , d_5 , d_6 , and d_7 are chosen accordingly as shown in Appendix A and the encoding operation is given by

$$\begin{bmatrix} 1000 \\ 0100 \\ 0010 \\ 1110 \\ 0001 \\ 1101 \\ 1011 \end{bmatrix} \begin{bmatrix} d_7 \\ d_6 \\ d_5 \\ d_3 \end{bmatrix} = \begin{bmatrix} d_7 \\ d_6 \\ d_5 \\ c_4 \\ d_3 \\ c_2 \\ c_1 \end{bmatrix}$$

The matrix is known as the GENERATOR

MATRIX. The receiver verifies the block by using the PARITY CHECK MATRIX (see Appendix A), which should produce all zeroes. In simple terms, the receiver generates $c_1, c_2,$ and c_4 from the received data bits. If the generated c_1 and c_2 do not agree with the actual received values, d_3 is incorrect. For example, [1 0 1 1] becomes [1 0 1 0 1]. If d_5 is corrupted such that [1 0 0 0 1 0 1] is received, the generated check bits are $c_1 = 0, c_2 = 0,$ and $c_4 = 1$. Thus c_1 and c_4 do not agree with the detected values, which indicates that d_5 should not be 0 but 1. The same type of result occurs for any other error—provided there is only one error. If two errors had occurred with [1 0 1 1 0 0 1] detected, a check would indicate that d_7 was incorrect. Consequently, the block would be corrected to [0 0 1 1 0 0 1], which now has three errors with two in the four data bits. The importance of the original assumption that the code would only detect and correct an error in one bit per block is now fully clear. However, the overall method is typical of block codes. The various positions for a code with four check bits that can correct up to 11 data bits are given in Appendix B.

Cyclic codes

Cyclic codes are similar to block codes, but there are important mathematical differences. A code word of length n bits is represented as a polynomial of degree $(n-1)$ as follows:

$$w(x) = [w_n w_{n-1} w_{n-2} \dots w_1] = w_n x^{n-1} + w_{n-1} x^{n-2} + \dots + w_2 x + w_1$$

[Eq. 2]

where w_n is the most significant bit (MSB). It is generated by a polynomial known as the GENERATOR POLYNOMIAL, $g(x)$, as follows:

$$w(x) = c(x) g(x) \text{ mod } (x^n + 1)$$

[Eq. 3]

Most books on coding write the modulus as $(x^n - 1)$. In this case, the mathematics refer directly to digital electronics. Actually, $g(x)$ is a factor of $(x^n + 1)$, but the other term, $c(x)$ does not represent the data as might be expected. In mathematical terms, $w(x)$ is the product modulo $(x^n + 1)$ of two polynomials with addition modulo 2 between the coefficients of the various terms. The exact coding mechanism will be shown later on.

A CHECK POLYNOMIAL, $h(x)$, has the same significance as in the previous section with

$$h(x) g(x) = x^n + 1$$

[Eq. 4]

which means that $h(x)$ is the other factor of $(x^n + 1)$. If a received code word $w(x)$ has no error,

$$h(x) w(x) = 0.$$

[Eq. 5.]

Consider the example in the previous section with $n=7$. In this section, this translates to $x^7 + 1 = 0 \text{ mod } 2$. The factors are $(x^3 + x + 1)$ and $(x^4 + x^2 + x + 1)$ and we will use $g(x) = x^3 + x + 1$

and

$$h(x) = x^4 + x^2 + x + 1$$

as per equation 4. At this stage, the term ‘cyclic’ requires some explanation. Let $w(x)$ in equation 2 be rewritten in the form

$$w(x) = c_1 g(x) + c_2 x g(x) + c_3 x^2 g(x) + \dots + c_7 x^6 g(x)$$

[Eq. 6]

The various terms as shown in Appendix C consist of a set of polynomials that is generated by shifting $g(x)$ as in a shift register. Thus, $w(x)$ may be considered as a linear combination of the seven states of $g(x)$ with x as a ‘shift’. The full set of code words is generated by $g(x)$ and hence its name. The reader is referred to the topic of Cyclic Groups in Group Theory for the appropriate mathematical background. If the data is [1 1 0 1], an estimate of $w(x)$, which assumes that the check bits are all zeros, is

$$w'(x) = [1 1 0 1 0 0 0] = x^6 + x^5 + x^3$$

[Eq. 7]

However, $g(x)$ does not divide $w'(x)$ evenly. There is a remainder of 1 in the least significant bit (LSB) position. The correct $w(x)$ is

$$w(x) = [1 1 0 1 0 0 1] = x^6 + x^5 + x^3 + 1$$

[Eq. 8]

in order to satisfy the mathematical conditions. The procedure may be written as a matrix as follows

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 0 \\ 1 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}$$

the derivation of which is in Appendix D. The PARITY CHECK MATRIX to authenticate the code word is explained in Appendix E. If the block was corrupted to [1 1 0 1 1 0 1], this new $w(x)$ on division by $g(x)$ would have a remainder of x^2 . This indicates an error two shifts away from the LSB and the particular bit can be corrected. However, to correct two or more errors, a BCH code, which uses a particular type of generator polynomial, is required and this topic is outside the scope of this article.

Huffman codes

Huffman codes are not for error detection and correction, but deserve special mention because they may be used in conjunction with error detection and correction codes. The most important point is that the data

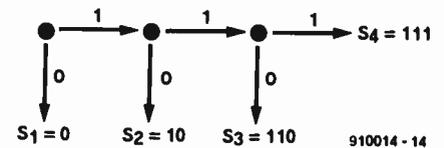
blocks do not have a fixed length. The reasons for this structure structure lie in the nature of language. The symbol E in ASCII is 1000 10 1 and Z is 10 1 1 0 1 0. Each symbol is represented by seven bits excluding the parity bit. However, E occurs 130 times more often in normal text than Z. It has been estimated that normal English is 70% redundant because of these statistical properties. Consequently, the total number of bits required for a full message could be greatly reduced if the common symbols were represented by short blocks and the more uncommon ones by larger blocks. A simple example is Morse code, in which E is one dot, whereas Z is two dashes followed by two dots. Huffman codes utilize this property of redundancy to considerable advantage.

If an alphabet has m symbols, the average number of bits per symbol is

$$\bar{r} = \sum_{i=1}^m p_i r_i$$

[Eq. 9]

where p_i is the probability of occurrence of the i th symbol, which is represented by r_i bits. A Huffman code seeks to keep \bar{r} as small as possible by pairing the symbol with the highest probability with the shortest block. Consider an example of a set {S₁ S₂ S₃ S₄} with four symbols. Normally, each symbol would be represented by a two-bit block, such as: S₁ = 0 0, S₂ = 0 1, S₃ = 1 0, S₄ = 1 1.



A Huffman code would adopt a branch type structure as shown above. In this design, S₁ is represented by only one bit, but S₃ has three bits. If the probabilities are $p_1 = 1/2, p_2 = 1/4, p_3 = 1/6,$ and $p_4 = 1/12,$ application of equation 9 gives

$$r = 1(1/2) + 2(1/4) + 3(1/6) + 3(1/12) = 1.75 \text{ bits/symbol}$$

[Eq. 10]

which is a reduction of 25%. If the probabilities were assigned in reverse order, $\bar{r} = 2.67,$ which is an increase of 67%. Hence, the importance of pairing the largest probability with the shortest block. In the special case where the two values for \bar{r} turned out to be equal, the assignment with the lowest variance would be taken.

The entire area of Huffman codes is quite involved and the reader is referred to the various text books in the references for further information. Its advantage is in reducing the total number of data bits. The sequence of data bits can be broken into blocks and encoded as under ‘‘Block codes’’ and Cyclic codes’’. The receiver simply reverses this process by first decoding the error detection and correction code followed by the Huffman code.

Implementation

The electronic implementation of the codes discussed is relatively straightforward once the actual coding mechanism is understood. Figure 2 shows a digital electronic circuit, which is essentially a shift register, to implement the example under "Cyclic codes". The arrangement is to generate the full code word of data and check bits. The four stages in the register correspond to the data block of four bits, which in turn generates the three check bits. The switch may be an AND gate with one input tied high (logic 1) or low (logic 0) as appropriate. The other input is simply the output of the bistable (flip flop). The addition modulo 2 represented by the \oplus in the diagram is simply an EXOR (exclusive OR) gate. The only change is that three different switch arrangements (open = 0 and closed = 1) are required to generate the three check bits. This corresponds to the three linear combinations in mathematics. Thus, the complete circuit for the coding operation could consist of three shift registers with fixed switch positions in parallel or one shift register with a mechanism to apply three different arrangements of the switches. Alternatively, implementation could be by software, that is, to write a program using the AND and EXOR logic operations of a microprocessor. This method will probably become more common—especially where the codes are more complex than these simple examples.

Figure 3 shows the circuit to check the parity bit generated by the first row of the PARITY CHECK MATRIX (as explained in Appendix E) applied to a code word. The seven stages correspond to the seven bits in the block. The other rows of the matrix simply require different arrangements of the switches. Both circuits are straightforward.

Conclusions

In this article I have attempted to explain the basis of error detection. It is not a detailed analysis and only deals with the correction of single errors.

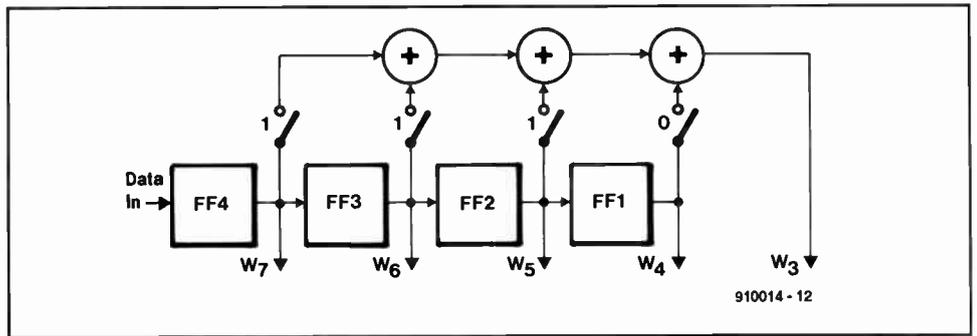


Fig. 2. Shift register as a Cyclic Encoder. The data block $[w_7w_6w_5w_4]$ is shifted into the register. The switches represent the terms of the matrix, such as 1 1 1 0 to generate w_3 . The switch is closed for 1 and open for 0. The same arrangement with different switch settings would be required to generate w_2 and w_1 .

Multiple errors of two or more bits per block are not considered as these require more complex solutions. Nevertheless, it should provide an introduction for students who are familiar with digital electronics, but have not previously studied this tricky topic. An interesting point is the increasing connection between Modern Algebra and Electronics. Twenty years ago, most engineers and technicians would not expect to use Modern Algebra. The reader is referred to the references for further study.

References

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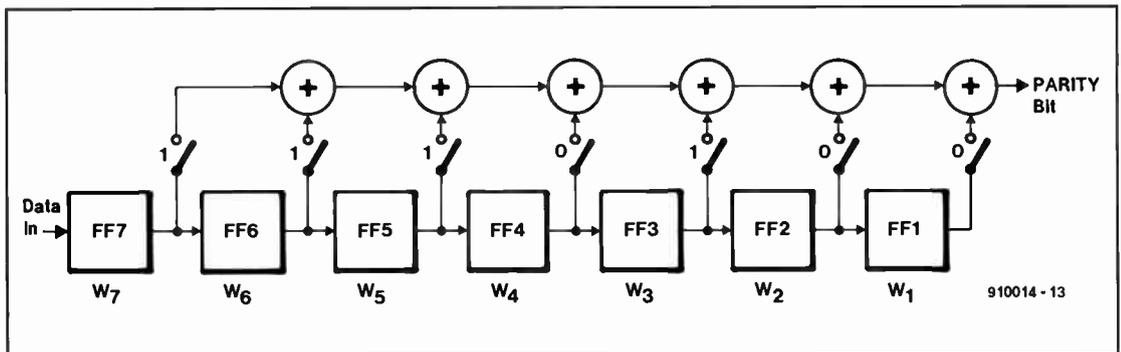


Fig. 3. Shift register to check a code word generated by the circuit in Fig. 2. If the PARITY BIT is 1, one of the seven bits in the shift register that has a closed switch is incorrect. For the first row of the PARITY CHECK MATRIX (see Appendix E) the switches are at 1 1 1 0 1 0 0. For successive rows, the appropriate settings must be used.

Appendix A

$$c_4 = (d_7 + d_6 + d_5) \text{ mod } 2$$

$$c_2 = (d_7 + d_6 + d_3) \text{ mod } 2$$

$$c_1 = (d_7 + d_5 + d_3) \text{ mod } 2$$

If d_7 is incorrect, c_1 , c_2 and c_4 do not agree with calculated values.

If d_6 is incorrect, c_2 and c_4 do not agree with calculated values.

If d_5 is in correct, c_1 and c_4 do not agree with calculated values.

If d_3 is incorrect, c_1 and c_2 do not agree with calculated values.

$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 \\ 1 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} d_7 \\ d_6 \\ d_5 \\ d_3 \\ c_4 \\ c_2 \\ c_1 \end{bmatrix} =$	$\begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}$	$\begin{bmatrix} d_7 \\ d_6 \\ d_5 \\ d_3 \\ c_4 \\ c_2 \\ c_1 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$
Generator matrix	Encoded block	Parity check matrix	

Appendix B

Position: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
 Bit: $d_{15} d_{14} d_{13} d_{12} d_{11} d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1$
 The check bits are thus at positions 1, 2, 4, and 8.

Appendix C

$$x^n = 1 \pmod 2$$

$$x^n + 1 = 0 \pmod 2$$

For $n = 7$ and $g(x) = x^3 + x + 1$, representing the seven-bit state [0 0 0 1 0 1 1] of a shift register, the operation using shift left rather than shift right is

0 0 0 1 0 1 1	$g(x) = x^3 + x + 1$	
0 0 1 0 1 1 0	$xg(x) = x^4 + x^2 + x$	
0 1 0 1 1 0 0	$x^2g(x) = x^5 + x^3 + x^2$	
1 0 1 1 0 0 0	$x^3g(x) = x^6 + x^4 + x^3$	$x^7 = 1$
0 1 1 0 0 0 1	$x^4g(x) = x^5 + x^4 + 1$	
1 1 0 0 0 1 0	$x^5g(x) = x^6 + x^5 + x$	
1 0 0 0 1 0 1	$x^6g(x) = x^6 + x^2 + 1$	
0 0 0 1 0 1 1	$x^7g(x) = x^3 + x + 1$	

Thus, multiplication of $g(x)$ by x is equivalent to a left shift of one step of the shift register. The initial state is reproduced after seven steps.

Appendix D

$w(x) = c(x) g(x) = [w_7 w_6 w_5 w_4 w_3 w_2 w_1]$,
 where
 $c(x) = c_4x^3 + c_3x^2 + c_2x + c_1$,
 and
 $g(x) = x^3 + x + 1$,
 whence
 $c(x) g(x) = c_4x^6 + c_3x^5 + (c_4+c_2)x^4 + (c_4+c_3+c_1)x^3 +$
 $+(c_3+c_2)x^2 + (c_2+c_1)x + c_1$.

$w_7 = c_4$	
$w_6 = c_3$	
$w_5 = c_4 + c_2$	$c_2 = w_7 + w_5$
$w_4 = c_4 + c_3 + c_1$	$c_1 = w_7 + w_6 + w_4$
$w_3 = c_3 + c_2$	$w_3 = w_7 + w_6 + w_5$
$w_2 = c_2 + c_1$	$w_2 = w_6 + w_5 + w_4$
$w_1 = c_1$	$w_1 = w_7 + w_6 + w_4$

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} w_7 \\ w_6 \\ w_5 \\ w_4 \end{bmatrix} = \begin{bmatrix} w_7 \\ w_6 \\ w_5 \\ w_4 \\ w_3 \\ w_2 \\ w_1 \end{bmatrix}$$

Remember that the arithmetic is modulo 2.

Appendix E

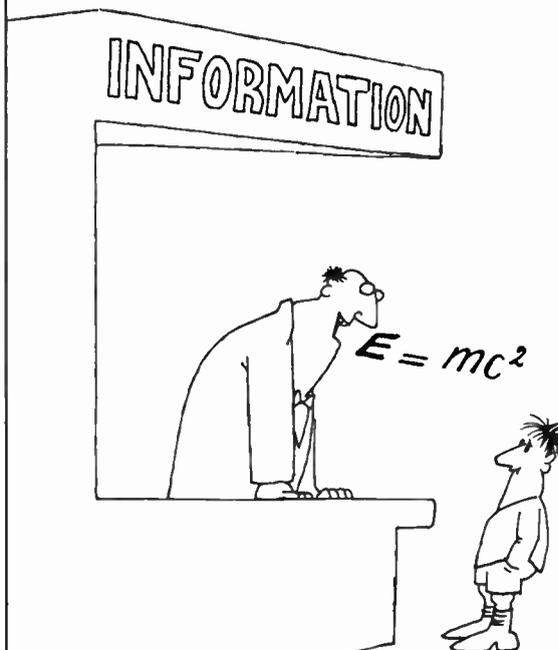
$h(x) = x^4 + x^2 + x + 1$ PARITY CHECK POLYNOMIAL
 $w(x) = w_7x^6 + w_6x^5 + w_5x^4 + w_4x^3 + w_3x^2 + w_2x + w_1$
 $\therefore h(x) w(x) = x^6(w_7 + w_6 + w_5 + w_3) + x^5(w_6 + w_5 + w_4 + w_2)$
 $+ x^4(w_5 + w_4 + w_3 + w_1) + x^3(w_7 + w_4 + w_3 + w_2)$
 $+ x^2(w_6 + w_3 + w_2 + w_1) + x(w_7 + w_5 + w_2 + w_1)$
 $+ (w_7 + w_6 + w_4 + w_1)$

$$\begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 1 & 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} w_7 \\ w_6 \\ w_5 \\ w_4 \\ w_3 \\ w_2 \\ w_1 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

From equation 6, the PARITY CHECK POLYNOMIAL applied to a correct code word should give 0. The PARITY CHECK MATRIX should give the zero vector.

Appendix F

An important parameter, known as the **Hamming Distance**, was not covered under 'Block codes' as it was not required. Consider the (7, 4) Hamming code. Any two code words differ in at least three bits. This minimum distance is known as the Hamming Distance. If the distance were only two, an error could only be detected but not corrected. Detection of a double error would require a distance of four.



LOGIC ANALYSER PART 1

by K. Nischalke and H.J. Schulz

A logic analyser is primarily intended for carrying out measurements in fairly complex circuits, where an oscilloscope begins to show its deficiencies. Unfortunately, it remains a pretty expensive instrument and it is for that reason that a design is offered here that can be built by most enthusiasts at a reasonable cost.

STRICTLY speaking, it is not quite right to compare an oscilloscope with a logic analyser, because basically an oscilloscope displays voltage or current as a function of time, whereas a logic analyser shows data as a function of time. Both instruments may, therefore, be required in a number of applications. For instance, suppose that a logic analyser has indicated that the data of a certain signal are not quite right. It is then possible to check with a scope whether that is caused by the voltage behaviour of the signal (for example, a logic 1 may have become stuck at 1.5 V).

Furthermore, a logic analyser has more input channels than an oscilloscope. That is a very definite advantage when microprocessors are being tested. Even an old-fashioned 8-bit device with 16 address lines requires more than the maximum four channels available on an oscilloscope. Looking at the discrete signals associated with these devices does not mean much, but their interrelation is of great importance.

Like an oscilloscope, a logic analyser needs to be triggered, but the trigger signal must be specially adapted for working with digital information. Instead of being triggered at a certain voltage level, the logic analyser is triggered by a given pattern of bits present at the inputs.

A computer and associated software have become inseparable parts of the modern logic analyser, and in proprietary instruments they form an integral part of the construction. The present instrument is intended for operation with an external computer, either an IBM PC or compatible or an Atari.

Block diagrams

The general design of the analyser is shown in Fig. 1. The interface in the computer is connected to the busboard of the analyser. The analyser proper consists of a control board and up to four RAM cards.

The control of the analyser is an independent circuit whose parameters are determined by the computer. That independence is imperative, because few computers can handle clock frequencies of 25 MHz or 100 MHz in real time. The prime tasks of the circuit are the control of the triggering and the addressing of the memory. The length of the memory is always 2 K, while its width lies

between 16 bits (1 RAM card) and 64 bits (4 RAM cards).

Data are input into the RAM card(s) via a probe. The probe(s) does not consist of much more than a number of buffers, which are, however, indispensable for the correct transport of digital signals, where fundamental frequencies may be as high as 25 MHz. At the same time, it keeps the load on the circuit under test to a minimum. Furthermore, it provides a much neater connection between the analyser and the circuit under test.

The connection between the probe(s) and the RAM card(s) consists of a one-metre cable, while those between the probe(s) and the circuit under test are made by short, discrete cables. This arrangement obviates the frequently encountered spaghetti-like mess of cables. When longer connections are required, two or more probes may be connected in series.

The block diagram of the analyser, insofar as the RAM cards and the control board are concerned, is shown in Fig. 2.

When data are written via the probe(s), clock frequencies of 100 MHz, 25 MHz, 1 MHz or an external clock may be chosen. The somewhat different mode of operation at 100 MHz will be discussed later. The clock frequency determines how often the data at the inputs of the probe are clocked (sampled) in the

SPECIFICATION	
Memory	2048 samples per channel 8192 samples per channel (100 MHz mode)
No. of channels per RAM card	16 4 (100 MHz mode)
Number of RAM cards	up to 4
Clock	100 MHz; 25 MHz; 1 MHz internal external up to 25 MHz
Clock qualifier	2 (not in 100 MHz mode); may be set high, low or disabled
Type of trigger	centre
Trigger pattern	set per channel: 0, 1 or X
Duration of trigger pattern	20 ns–5.12 µs; 'arm' triggering: 20 ns–2.56 µs
Trigger window	40 ns–81.92 µs

latch at the input. Note that only in the 100 MHz mode the input latch/shift register operates as a shift register. Once the input data are sampled, they are written into RAM with the aid

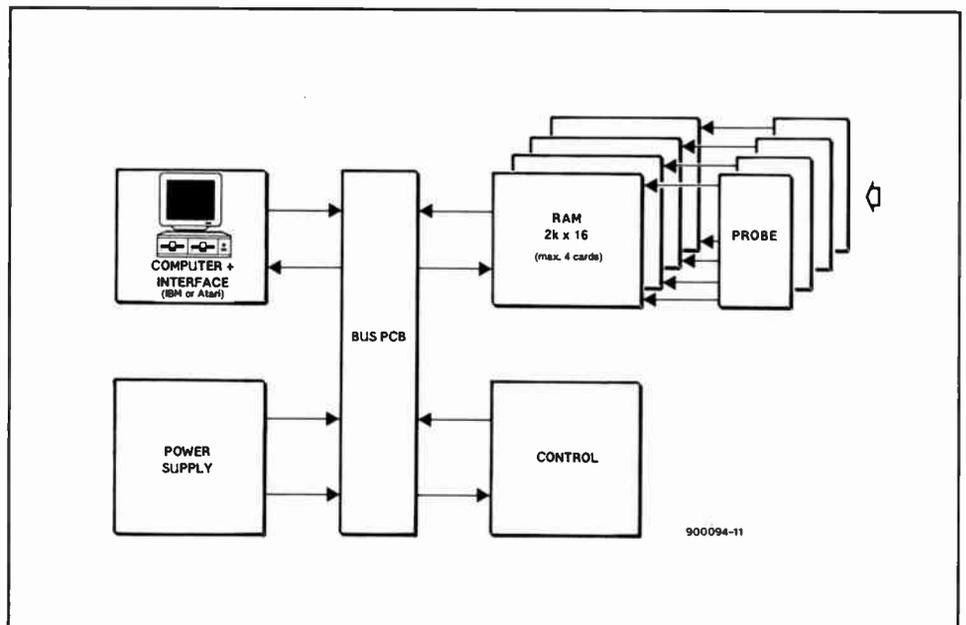


Fig. 1. General design of the logic analyser.

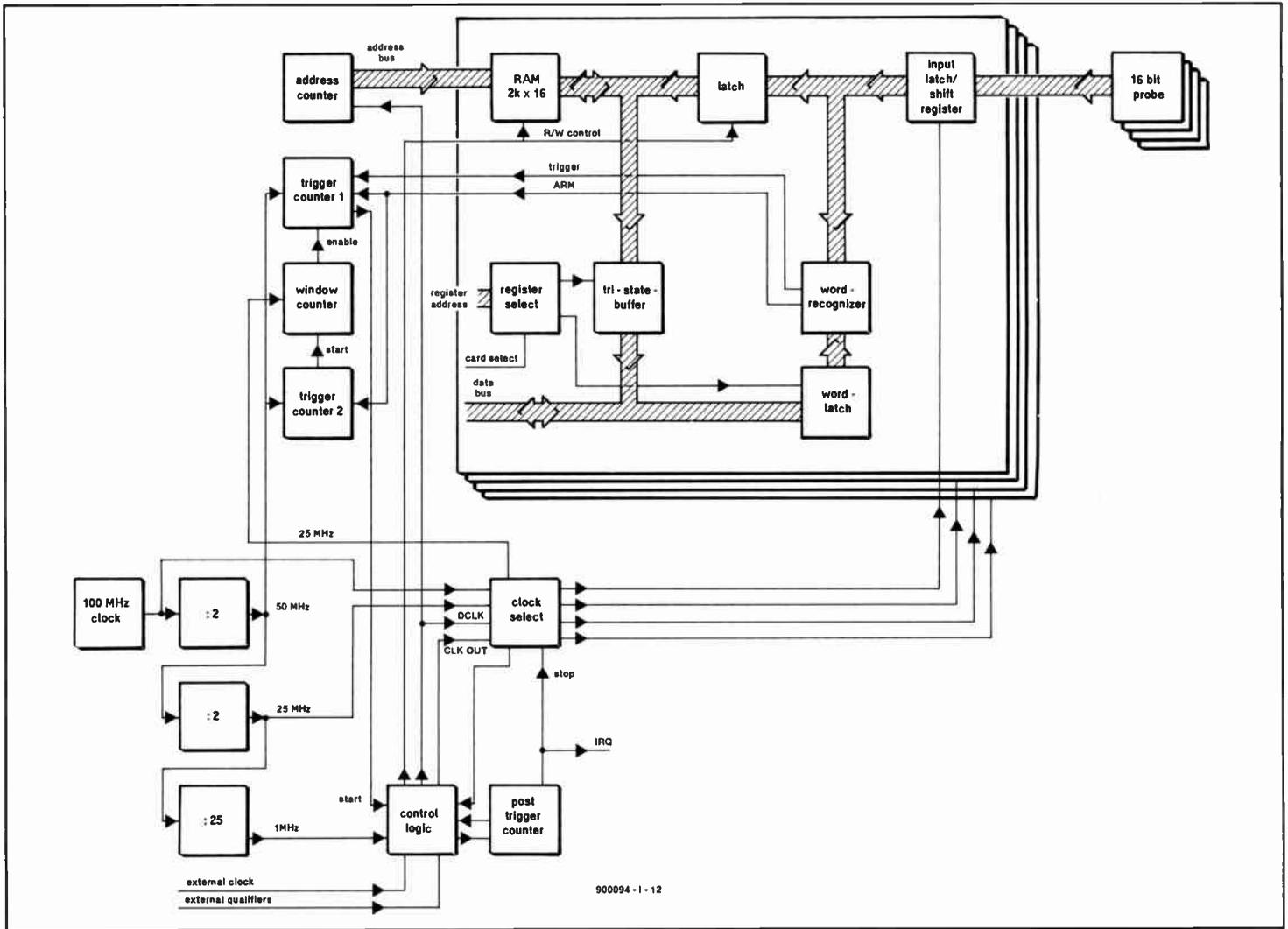


Fig. 2. Block diagram of the RAM cards and the control board of the logic analyser.

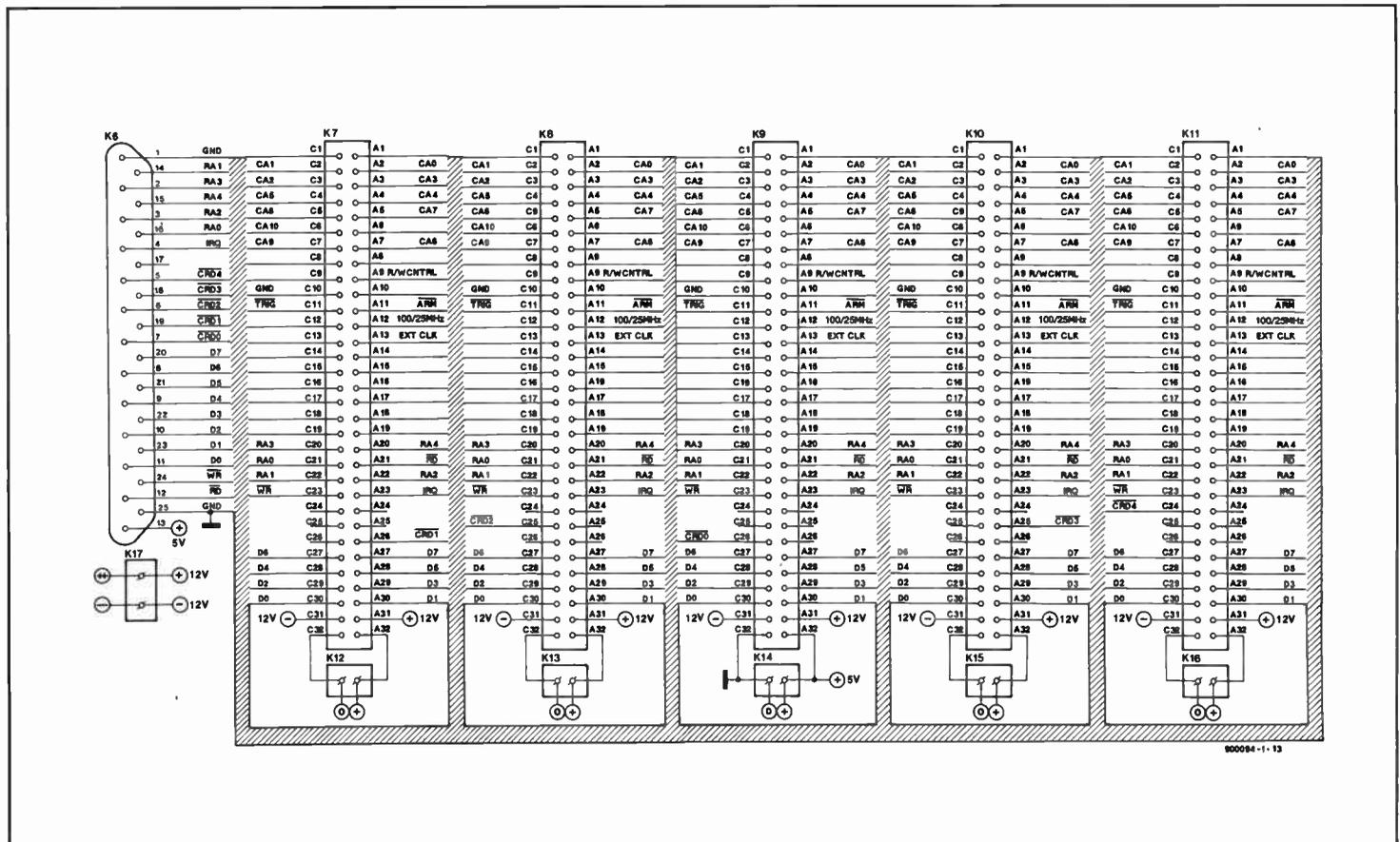
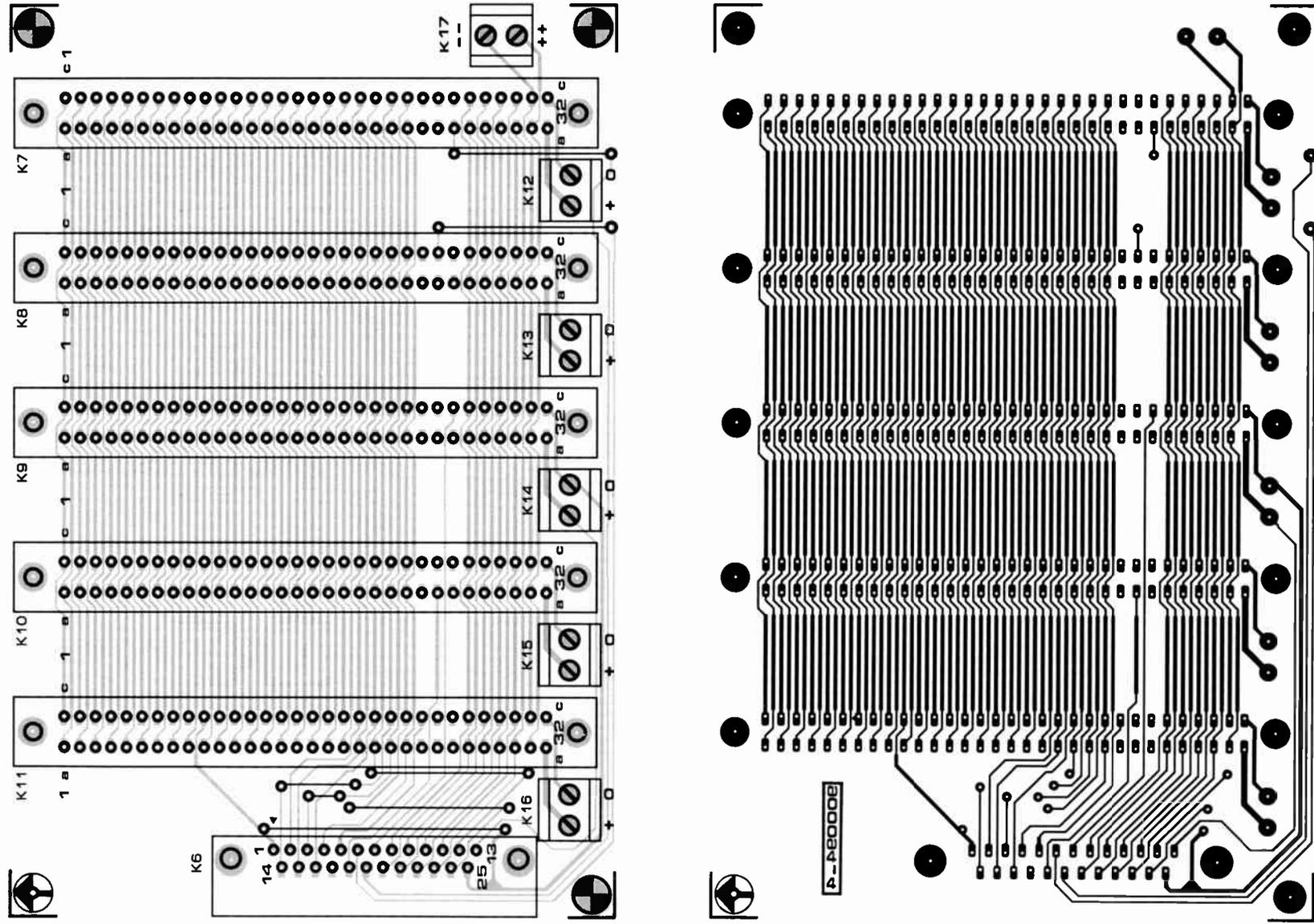


Fig. 3. The busboard is hardly more than an assembly of wiring and connectors.



K₆ = 25-way male D connector, right-angled for PCB mounting.

K₇-K₁₁ = 32-way female AC connector to DIN 41612 for PCB mounting.

K₁₂-K₁₇ = 2-way PCB terminal block.

Fig. 4. The printed circuit busboard of the logic analyser.

of the signal R/W control. Subsequently, the address counter is increased by 1. This process continues uninterruptedly; when the RAM has been written to capacity, the process starts anew: the oldest data are replaced by the new data. The advantage of this arrangement will be discussed later.

To enable the analyser being triggered, the sampled data are compared with the data in the word-latch by the word recognizer. This latch has information as to whether each bit should be a 0, a 1 or 'don't care' to comply with the trigger conditions. Once the wanted word pattern has been accepted by the recognizer, it is passed to trigger counter 1 via lines 'trigger' and 'arm'. Note that these lines have a separated function in the 100 MHz mode only: normally, they are electronically interconnected. When these lines indicate that the desired trigger condition is present, counter 1 will verify that this condition is present for as long as the counter counts. If this is not so, the analyser is not triggered. When the counter has stopped counting, the trigger condition is met and the analyser is started. Counter 2 and the window counter only function in the 100 MHz mode.

When counter 1 has started the analyser, the control logic block clocks the post-trigger counter which checks how many samples have been taken of the input data after triggering. As soon as 1024 samples have been taken, the post-trigger counter stops the analyser and gives an interrupt to the computer. This arrangement ensures that no more than 1024 bytes can be written to RAM before triggering takes place, so that later the computer can analyse data before and after triggering. This is the reason that before triggering the data are written into RAM continuously.

As soon as the analyser is disabled, the block register select and the three-state buffer in the computer divide the 16-bit wide words into two 8-bit wide bytes which are then pro-

cessed in the computer.

The basic operation of the circuit is not much different in the 100 MHz mode, but everything happens just a little faster. This, however, creates a problem: the RAM cannot cope with this higher speed. This is the reason that the shift register used as input latch in the other modes is used as a high-speed shift register in the 100 MHz mode. Four successive data samples are input into the register, which has the effect of lowering the frequency at which the data is offered to the RAM to 25 MHz. The latch between the shift register and the RAM ensures that the data are present long enough at the inputs of the RAM, because, in spite of their shifting, the data at the outputs of the shift register will not remain stable for longer than 10 ns.

Unfortunately, when the shift register is used as a latch, 16 inputs per RAM card are available. Because of the shift operation, that is limited to four inputs per card in the 100 MHz mode. On the other hand, four times as much data can now be written into RAM since four samples may be located at one address. Furthermore, because of the lower number of inputs, the word recognizer may be bisected, which increases the number of instants that triggering takes place.

Because of the bisecting of the word recognizer, the signals 'arm' and 'trigger' are separated. When the section of the recognizer that provides the 'arm' pulse accepts the trigger condition, counter 2 is started. Like trigger counter 1, this counter must check whether the trigger condition lasts long enough. If that is so, the window counter is started. As long as this counter runs, three situations may occur: (a) the 'arm' trigger word appears again; (b) the second trigger condition is met; and (c) the window counter has counted to capacity. In the first case, trigger counter 2 and the window counter are reset, so that the triggering process starts anew. The second trig-

ger condition is met when counter 1, after it has been triggered by the second section of the recognizer, has counted to capacity and gives a start pulse. In other words, the analyser is started if it is first triggered by the 'arm' signal and then, within a given time (the window), by a second signal. In the third case, the period (the window) during which triggering should have taken place has lapsed. The circuit will then wait for the first trigger ('arm') to recur. The double triggering is of particular advantage when measurements are carried out in microprocessor systems in which certain bit patterns occur regularly. The intercoupling of two bit patterns greatly improves the provision of a stable and unambiguous triggering.

The software

What may be done with the data collected by the hardware is shown in Fig. 5, which is the (German) program for Atari computers. The English translation, which has unfortunately been delayed beyond this issue, and the program for IBM PCs and compatibles, which is virtually identical to that for the Atari, will be published in a future issue.

Both trigger words may be set in the column at the extreme left on the monitor screen, but note that trigger word 2 is not active. The program can handle up to four trigger settings. Which of these is selected at any one time is indicated by the figure under the column containing the trigger words. Beside this is the setting of the minimum duration of the trigger pattern and the length of the trigger window.

The column beside that for the trigger words contains the names of the signals. Apart from the standard indication "channel so and so", these signals may be given more informative names. Also, it is possible to arrange them in a different order on the screen and to display them more than once. For example, associated signals may be placed side by side on the screen without the necessity of changing over test probes. The column may also be used to indicate from which test probe the signal comes.

The larger part of the screen is, of course, reserved for the display of signals, and it can handle up to 16 of these simultaneously. Other channels may be brought on to the screen by scrolling via the window at the bottom left. The control for shifting the signals to the left and right is situated at the bottom right. Above that is an indication where the (so far invisible) cursor is situated with respect to the triggering point, and which data (hexadecimal) are portrayed.

The block 'solution' enables the determining of how many samples are required on the screen simultaneously.

The pull-down menus provide the following functions: (a) information about the program (desk); (b) storing on disk of the data to be analysed (datei); (c) printing of the data (printer); (d) selecting the clock frequency (mode); and (e) various functions (options).

(to be continued)

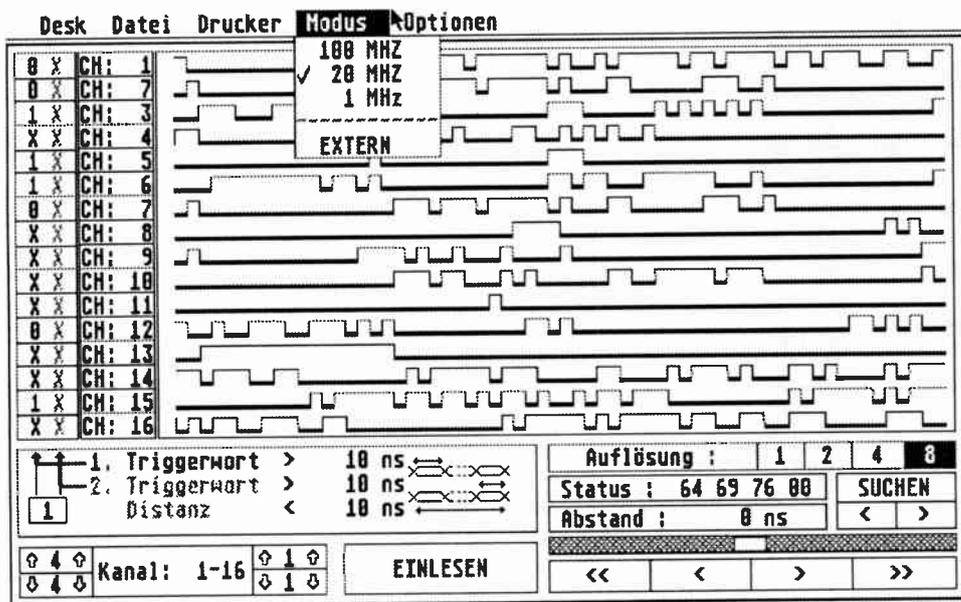


Fig. 5. Screen view showing what the program can do. Drucker = printer; Modus = mode; Optionen = various functions; Triggerwort = trigger word; Kanal = channel; Einlesen = to write; Datei = data in; Auflösung = resolution; Suchen = to search; Abstand = distance. (Proper English translation will be published soon).

23/24-CM FM ATV RECEIVER

This review deals with the recently introduced 23/24 cm FM Amateur Television (ATV) receiver from EHC (Valves) Ltd. At the time of writing, it is the only complete system that can be purchased in a 'ready-to-go' state. That is, all you have to is connect the DC shack supply, plug in a 24-cm aerial, a video monitor and a loudspeaker or headphones, tune in a signal, and away you go.

by Mike Wooding,
G6IQM

ALTERNATIVELY, the IF board and the down converter sub-sections can be purchased separately for inclusion in your own system, or for building your own version of the receiver. However, this option will require a number of external components such as a meter, controls, sockets, etc., to be added.

Description

The receiver is housed in a grey coloured moulded impact-proof PVA plastic box measuring 23.5×18.25×9.5 cm including the feet, with the control knobs on the front panel, and the sockets on the rear panel making the unit 21.5 cm deep in total. The case also features adjustable front feet, allowing the unit to be tilted upwards to facilitate reading the meter.

The front panel controls comprise, from the left to the right: an on/off switch, a TUNING control, a VID. GAIN control and a VOLUME control. Also featured on the front panel is a red LED for ON/OFF indication, and the tuning-frequency meter. The front panel bezel is sign-written with the various control and switch functions.

The rear panel connections are as follows: a 3.5-mm jack socket for the loudspeaker/headphone connection, a phono socket for video output, a BNC socket for aerial connection, and a DC socket for the power supply input. Also mounted on the rear panel is a 20-mm fuse holder.

Internally, the receiver has a die-cast box and two printed circuit boards mounted onto the housing chassis. All earth connections are bonded to this chassis for screening security.

The die-cast box, measuring 120×95×35 mm, houses the down converter with power connections made via feed-through capacitors, and the IF output by means of a coaxial cable. The aerial input socket mounted through the rear panel of the hous-



ing is a bulkhead coaxial cable connection type, connected to the down converter by a short length of coaxial cable.

The two PCBs are the wide-band IF amplifier and the IF receiver assemblies. Both boards are constructed from double-sided copper-clad material, and are custom-built for each unit. All interconnecting wires and cable are neatly formed and retained with cable ties.

The TUNING control is a precision 10-turn potentiometer, which facilitates fine-tuning of the band with only one control. The VID. GAIN and VOLUME controls are ordinary 270-degree potentiometers. The tuning frequency meter is a standard 90-degree movement type with the scale calibrated with a logarithmic frequency read-out scaled in 10-MHz steps, with main divisions at 1240, 1260, 1300 and 1320 MHz.

Circuit outline

The number of controls has been kept to a minimum, i.e., tuning, video gain, volume and changeover from 5.5 MHz to 6.0 MHz sound subcarrier. This latter switch also changes the polarity of the video output from negative on 6 MHz (UK and most of Europe) to positive on 5.5 MHz (France).

The first down converter section (housed in a die-cast box) uses parallel-tuned circuits to give a good rejection of broadcast TV signals, radar and other in-band signals. All the SHF and UHF tuned circuits are etched on

to the printed circuit board, including the first local oscillator, which reduces frequency drift to a very low level after only a few minutes warm-up. The output from the first down converter is 168 MHz, which is routed to a second down converter. This is external to the die-cast box, and comprises a dual-IC tuned

circuit that converts the first IF of 168 MHz to a second IF at 39 MHz for input to the demodulator.

The 39-MHz signal is amplified by another dual-IC circuit and then buffered by an emitter follower stage, which matches the signal to the phase-locked loop demodulator. After demodulation, the video signal passes through an emitter follower buffer stage, a standard (non-switchable) CCIR de-emphasis circuit, and an audio subcarrier trap. The latter is followed by a video amplifier and a 75-Ω video output buffer.

The audio subcarrier is extracted at the buffer stage following the demodulator, and is fed into a switchable filter network to select either 5.5 MHz or 6.0 MHz, depending on the signals being received. After the filter stage, the signal is routed to a single IC audio demodulator, and from there to an output stage. The audio volume control varies the output from 0 to about 1 W into an 8-Ω load, or 2 W into a 4-Ω load.

The receive frequency indication meter is driven by sampling the tuning voltage applied to the varicap tuning diode. A potentiometer network allows the meter range to be adjusted to compensate for the different characteristics of different varicap diodes.

Bench test

In view of the fact that the receiver is supplied as a complete unit, the nature and depth of the bench test were different com-

pared to other reviews I have conducted in the past. However, what I consider to be essential tests I was able to carry out, and the results are discussed below.

The **noise floor** of the receiver with the aerial input terminated with a 50- Ω load was averaged out at -85 dBm. Three spurious signals were found at 1116 MHz (signal level: -25 dBm), 2232 MHz (-35 dBm) and 3348 MHz (-60 dBm). However, although they were at not inconsiderable levels, there did not appear to be any detraction in the performance of the down converter.

It ought to be said here that in virtually all circuits employing these relatively simple, but stable, oscillators working at the direct conversion frequency, harmonics and spurious signals will inevitably be produced. The trick is to tailor the circuitry such that they are either suppressed, or at frequencies outside the operating range of the receiver itself. Also, care must be taken that these harmonics and spurious signals do not desensitize the front end of the converter, especially when this is based on GaAs-FET devices and strip-line techniques.

The **sensitivity** of the receiver was checked by injecting signals from the Racal Dana 9087 Signal Generator, and tracking the output of the second IF stage with the Marconi 2383 Spectrum Analyser. With an input frequency of 1249 MHz, a signal level of -71 dBm was required to give an IF signal 3 dB up on the noise floor, or, in other words, just about the minimum signal level that could be detected as sync pulses. At the other end of the band, 1320 MHz, a slightly lower input of -72 dBm was required to give a 3-dB lift. These signal levels of around -70 dBm equate to a performance of the receiver similar to that of most of the equipment at present operated by ATV-ers.

The **maximum signal levels** before the IF stages went into limiting were -29 dBm at 1249 MHz, and -27 dBm at 1320 MHz, which indicated a good large signal handling capability (-30 dBm is equivalent to 1 mW).

Being unable to apply an external modulating signal greater than 100 kHz to the Racal signal generator, I had to inject a modulated signal into the demodulator itself at the second IF frequency from the Philips PM5646 Television Pattern Generator, and view the output on a video modulator. The resulting picture showed good definition and a linear chrominance response.

Using the same method as above, a 1-kHz audio signal was also injected from the test pattern generator, and the resultant audio signal measured on the HP 8903B Audio Analyser. The frequency recovery was found to be excellent, with the measured output signal reading 998 Hz. The distortion level at maximum output into a 8- Ω load was measured at 3.154%.

The **current consumption** of the receiver at a supply voltage of 13.5 V was measured at about 225 mA with no audio output, and 520 mA at full audio output.

Off-air tests

To conduct the off-air tests I simply compared the unit against my own Wood & Douglas/BATC home brew system, which has given me excellent results in the past. Having two 24-cm aerials of the same type and at the same height, and separate video monitors made this task easy.

First, I used the signals from GB3RT, the Coventry 24-cm FM ATV repeater, which I receive normally at P5 (broadcast quality). The pictures from the review unit were just as good as my own system, once the correct video output level was obtained with the front panel control. The tuning control, being a multi-turn type, allowed for easy tuning across the signal, enabling me to fine tune with considerable ease. The picture did have a tendency to bounce about somewhat until the correct tuning point was achieved, and the demodulator took a second or two to stabilize. This I took to indicate that owing to the strength of the received signal the IF stages were in limiting, hence perhaps slightly overloading the following stages. This has to be tempered a little by explaining that the signals I receive from GB3RT, although it is some 16 km away, are very strong indeed.

Next, I turned the aerials northwards towards GB3GV, the Leicester 24-cm FM ATV repeater, which I normally receive at P3 to P4. The results from the review unit were marginally worse than my own unit as far as the strength of the received picture itself was concerned, but the actual definition of the picture itself was, to all intents and purposes, identical.

Having checked at the top of the band, it was time to see how it fared where most of us ATV-ers operate, at the bottom end, around 1249 MHz. For this purpose I enlisted (as usual) the good offices of my fellow GB3RT group members Tony G0HOV, and John G1IJT. The received pictures all exhibited good video definition and chrominance response (apart from Tony's camera, but that's another story). By moving the aerial away from each station I was able to simulate very low received signals, and only at very low levels was the review unit found to be less sensitive than my own, but this was at picture strengths barely reportable as P1 (corresponding to just discernible prominent features, locked syncs).

The final test was to monitor my own transmissions. Again with the aid of Tony as the receiving station (for licence complicity purposes, you understand) I transmitted at an output level of 2.5 W from my basic transmitter, and then at 60 W with my linear amplifier connected in. The results from the review unit at both power levels were the same, and quite a bit worse than with my own system. The resultant video output was quite unstable at times, with obvious sync crushing taking place in the overloaded demodulator. As with my own system, there was also a multitude of points along the tun-

TEST EQUIPMENT USED FOR THIS REVIEW

- Marconi 2383 Spectrum Analyser and Tracking Generator
- Racal Dana 9087 Signal Generator
- Philips PM5646 Television Pattern Generator
- Hewlett Packard 8903B Audio Analyser
- Philips PM3226 Digitising Oscilloscope
- Fluke 8050A Digital Multimeter
- Racal Dana 9232 Bench Power Supply

ing scale where my transmissions could be found.

Perhaps this test is a little unfair in expecting the unit to perform without fault, but it must be remembered that this is the *modus operandi* in many an ATV shack. The ability to monitor your own transmitted signal is a must, and most of us admit to doing it by using our own receivers, rather than 'sniffing' the output RF and demodulating that back to video.

Conclusions

Overall I quite liked the unit. As it stands, it is at present the only complete receiver available fully built, aligned and ready to go. The presentation is tidy, and the operation simplicity itself.

I do not really like the external video output level control. I feel that the output should be internally preset at 1 V at 75 Ω , which is the international standard. This would overcome the tendency of many people to incorrectly drive their video monitors and cause poorer pictures to be displayed.

I also feel that the CCIR de-emphasis network should be made switchable. There are many stations who do not use pre-emphasis in their transmissions, or at best, incorrect levels of emphasis. To be able to select the de-emphasis network allows for the correct reception of such signals. Otherwise, poorly defined and blurred pictures result, which hardly helps to boost confidence in the receiver.

The FM ATV receiver is available from EHC (Valves) Ltd., 7 Pavement Square, Lower Addiscombe Road, Croydon. Telephone: (081 654) 7172, at a cost of £230.00 including VAT. Carriage is extra at £3.34.

Finally, I wish to thank Mr. Brian Aylward of EHC (Valves) Ltd., for the loan of the review unit, and for his advice and assistance. ■

THE COMPLETE PREAMPLIFIER (1)

by T. Giffard

After the several 'spartan' preamplifiers we have published over the past few years, we feel the time has come to offer our readers a more sophisticated design, one with more controls than just a selector switch and a volume control. Although the design presented has quite a few useful features, and offers very good signal handling qualities, we have been able to keep its price to a reasonable level.

LOOKING around in hi-fi dealers' and retailers' shops (and talking to the manager or owner), it appears that a majority of (prospective) preamplifier buyers are interested in at least some of the following features. First on the list is a copying facility that is independent of the selector switch; second, the possibility of recording from one recorder to another; third, a tone control with variable cut-off frequencies; fourth, a headphone output (which means that the main amplifier can be switched off if listening only via the headphones is required); fifth (and surprising in these days of the Compact Disc), a dynamic pickup input. And, of course, the preamplifier must not degrade the signal in any way.

With these requirements, and that of low cost, in mind, we have come up with a unit that meets them handsomely and still offers the possibility of using ICs of different price classes.

The design lends itself to fairly easy construction. The source and record selector switches are housed on a busboard, together with the input and output connectors, while the remainder of the electronics is fitted on a motherboard. The controls are connected to the circuitry via a number of terminals that are situated at the front edge of the motherboard.

Overview

The block diagram of the preamplifier—see Fig. 1, shows that there are six inputs, of which one is the dynamic pick-up input. If that input is not needed, it may be transformed to a normal line input by a simple wire bridge. The CD input has provision for adding a board (for instance, a digital-to-analogue converter) at a later date.

The input signals are fed to two rotary switches: one for selecting the input mode (i.e., the signal that will be processed, and the other for selecting a signal to be recorded. In that way, it is possible to record from a CD and continue listening to the tuner. Standard rotary switches are used since these are much cheaper than the 12 relays that would otherwise be necessary. The switches are located

immediately adjacent to the the inputs at the rear of the enclosure, so that long signal paths are avoided.

Either switch is followed by a buffer, which in turn is followed by a stereo/mono switch which uses a summing opamp. This obviates the level differences that frequently occur in stereo/mono systems.

The tone control is a low-high design with two cut-off points at either side. The control range has been kept fairly limited to avoid overdriving of subsequent stages; it is, however, more than adequate for normal usage and offers smooth operation. For those who do not want tone control in any circumstances, it may be taken out of circuit by a simple 'tone defeat' switch.

The balance and volume control are followed by the output amplifier, which provides the only amplification of the line signals. The opamp chosen for this stage is able to drive loads of 600 Ω and higher.

A relay providing a delay at switch-on is provided at the output: this gives the unit a few seconds after the supply is switched on to stabilize during which period no signal is applied to the output.

The output amplifier also supplies part

of the signal to a special headphone amplifier that consists of an opamp and discrete output stage. It provides enough power for driving low-resistance headphones.

The circuits

The blocks of diagram Fig. 1 are easily recognized in the circuits of Fig. 2. and Fig. 3. The circuit has been split into two to correspond more closely to the drawings of the associated printed-circuit boards.

Figure 2 shows the record and source switches S_1 and S_2 with associated buffers, IC_1 and IC_2 , and all inputs and outputs with the exception of that for the headphones. Each input is shunted by a potential divider, for instance, R_1 - R_2 for the lefthand CD channel. These dividers largely determine the input impedance of 47 k Ω . It is advisable to use the dividers only if really necessary, since they may adversely affect the cross-talk between the left- and right-hand channels, as well as between the inputs. If dividers are not used, resistors R_1 , R_3 , R_5 , and so on should be replaced by wire bridges.

The CD input has some additional facilities. Normally, the analogue CD signal is

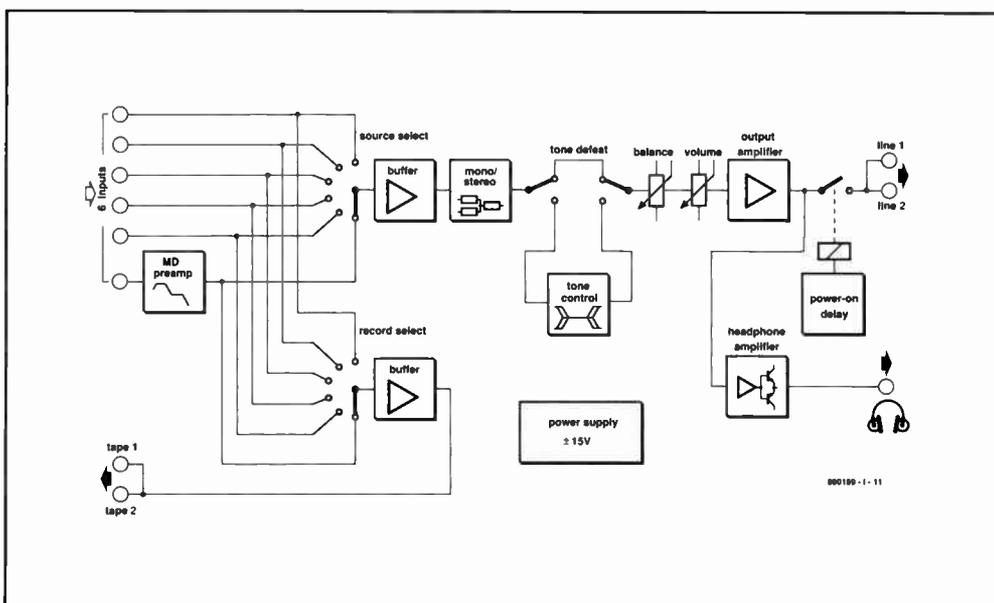


Fig. 1. Block diagram of the preamplifier.

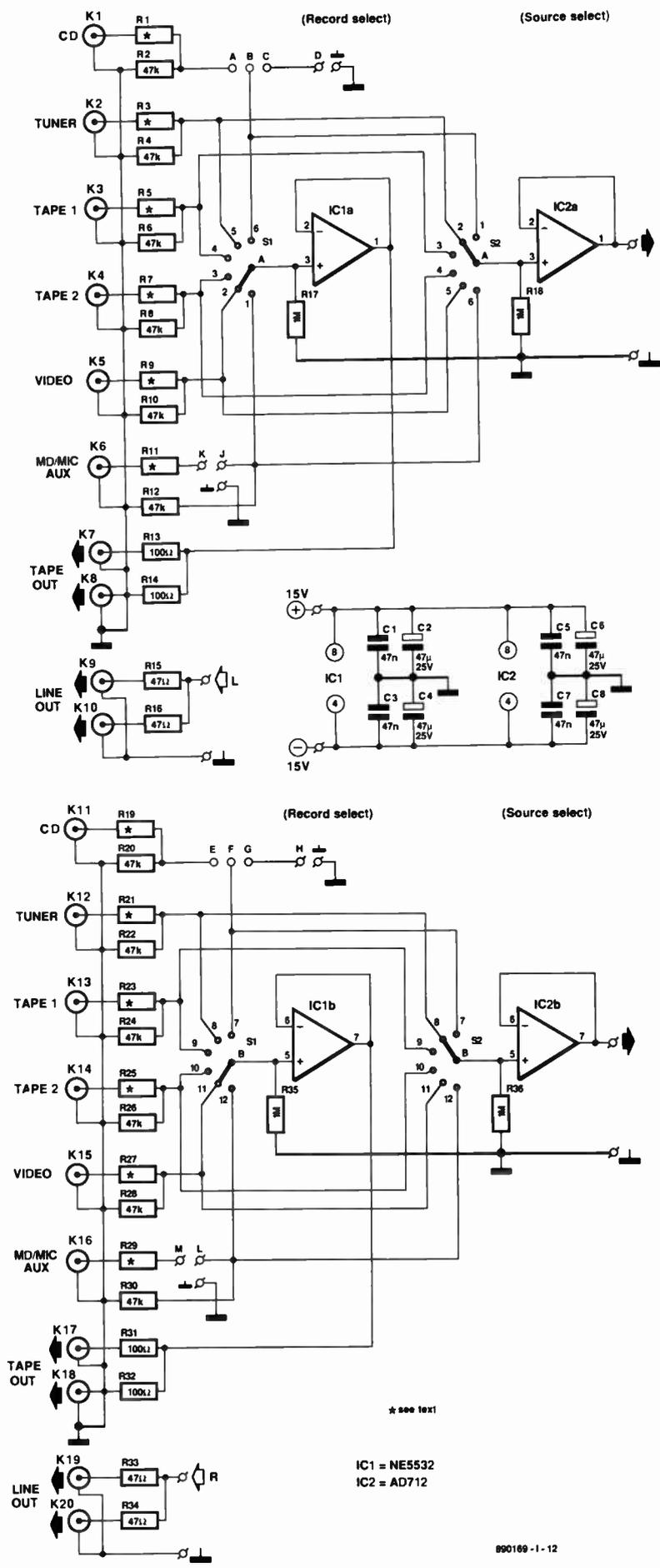


Fig. 2. Circuit diagram of the busboard

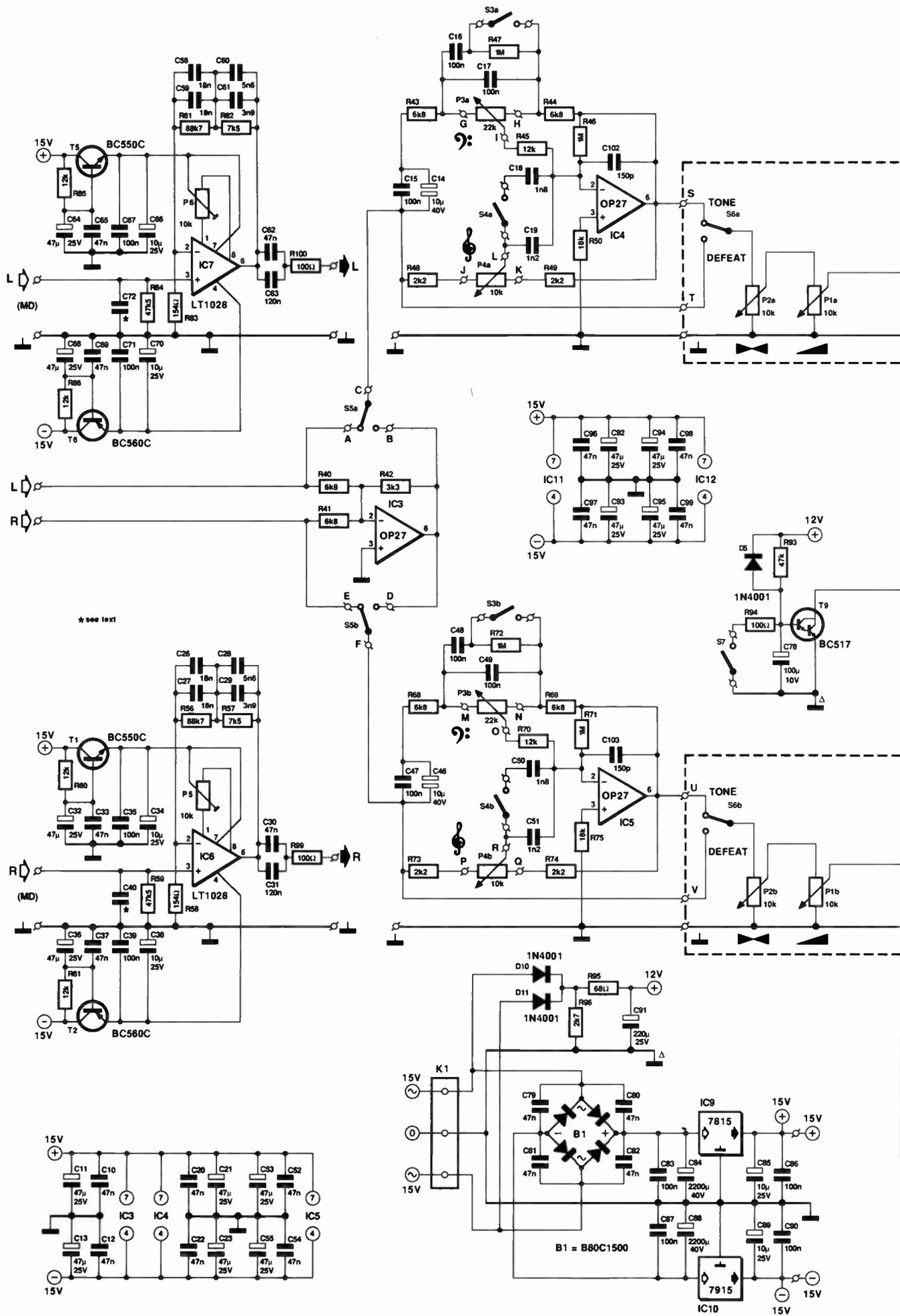
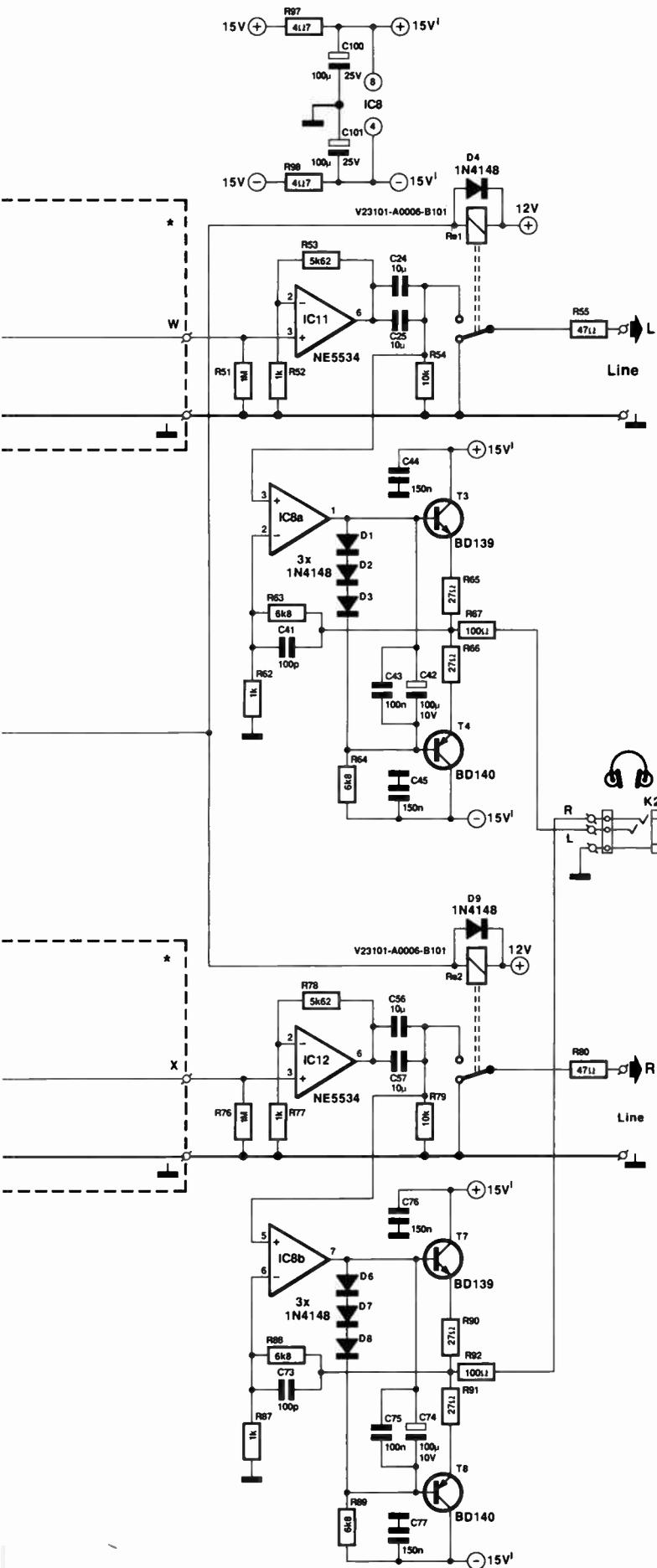


Fig. 3. Circuit diagram of the motherboard.



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applied direct to the CD input. A wire bridge between A and B (E and F) feeds the signal to the two rotary switches. Terminals C, D and ground (G, H and ground) enable a digital input, coupled to a separate digital-to-analogue amplifier, to be provided at a later stage.

The dynamic pick-up input also has additional facilities. Normally, the associated preamplifier on the motherboard is connected between K and J (left-hand channel) and between M and L (right-hand channel). If a dynamic pick-up input is no longer required, the input may be used as microphone input, for which the preamplifier is easily adapted, or as line input, in which case the preamplifier is not used and J-K and M-L must be linked by wire bridges.

The opamps shown in the circuit diagram are not necessarily the cheapest types, but they are the best for the particular purpose as far as our prototypes showed. This aspect will be touched upon again in Part 2 under Construction. For the moment, as an example, buffer IC₁ is a Type 5532, an inexpensive yet excellent double opamp, whereas buffer IC_{2a}, a Type AD712, is a much dearer type. This type was found necessary to obviate audible switching noises when S₂ is turned. These noises result from the change in total resistance at the input of the opamp: if, for instance, the CD input is used, R₁₈ is shunted by R₂. If an opamp with transistor inputs, such as the NE5532, were used, the change in resistance would cause a corresponding change in the output of the opamp. An opamp with FET inputs, such as the AD712, hardly reacts to the resistance change. If notwithstanding this a Type 5532 is used, R₁₆ and R₃₆ should be reduced to 220 k Ω . The input impedance will then reduce to about 39 k Ω , and this means that the ratio of the potential divider will change slightly.

Apart from the inputs, the busboard also contains all the outputs: two tape outputs with an output impedance of 100 Ω , determined by R₁₃, R₁₄, R₃₁, and R₃₂; and two line outputs, also with an output impedance of about 100 Ω , determined by R₁₅, R₁₆, R₃₃, and R₃₄, and R₅₅ and R₈₀ on the motherboard.

The circuit contained on the motherboard is shown in Fig. 3. Since the design of the left- and right-hand channels is identical, only the left-hand one will be referred to in what follows.

The preamplifier for the dynamic pick-up is shown somewhat away from the main circuit to emphasize its short connections to terminals J-K and L-M on the busboard. The opamp chosen for this stage is a very-low-noise Type LT1028. If that is found too expensive, the cheaper OP27 or 5534 may be used. The RIAA (IEC) correction is provided by R₈₁-R₈₃ and C₅₈-C₆₁. Network R₁₂-C₆₂-C₆₃ forms a high-pass filter with a cut-off frequency of 20 Hz to conform to the IEC requirement. If that frequency is thought unnecessary, the values of C₆₂ and C₆₃ may be increased.

The input of the preamplifier for the dynamic pick-up is entirely DC-coupled to obviate any degradation of the signal by cou-

pling capacitors. The input capacitance is determined primarily by C₇₂, whose value depends on what is required by the pick-up. If that is not known, 47 pF may be assumed. Because of the direct coupling, the offset of the opamp depends on the internal resistance of the pick-up and P₆ is therefore provided to cancel the offset as appropriate.

The supply lines to this sensitive stage have been provided with additional filters (around T₅ and T₆) to even out any ripple on the ± 15 V supply. It should be noted in this context that the use of an LT1028 is justified only in conjunction with low-impedance signal sources (<400 Ω). If a standard high-impedance dynamic pick-up is used, an OP27 will be perfectly all right, since the total noise then consists primarily of the thermal noise emanated by the pick-up.

The mono-stereo switch, S₅, is preceded by a summing amplifier, IC₃, that provides true addition of the left- and right-hand channels without any attenuation when stereo signals are to be processed as mono ones. Passive circuits always introduce some attenuation.

Although the design of the tone-control stage, IC₄, appears conventional, it has some interesting aspects. Usually, the connections to the ends of the carbon tracks of the 'high' potentiometers are via capacitors that determine the onset of the control. If the onset frequency is to be altered, the value of both capacitors needs to be changed. In the present design, only one component per channel needs to be altered. Switches S₃ and S₄ enable two different onset frequencies to be selected. The circuit is consequently somewhat simpler as regards wiring and switching.

A 1 M Ω resistor, R₄₅, provides a feedback loop that prevents the output of the opamp from rising to unwanted heights if the wiper of the 'low' potentiometer occasionally loses contact with the carbon track. Capacitors C₁₄ and C₁₅ have been added to ensure that the offset of the input buffers is not amplified in the tone control stage. This parallel network of a bipolar and a film capacitor guarantees faithful signal processing even at high frequencies. The control range for various onset frequencies is shown in Fig. 4 (published in our next issue). If required, the entire tone control may be taken out of circuit by S₆.

It is recommended to use the very best quality potentiometers for the balance and volume controls, for instance, Alps types. These are not cheap, but they give consistently good performance over a long life. In some locations, a real balance control may be difficult or even impossible to obtain: the right type has half-silvered tracks so that no attenuation occurs in the centre position. If so, a standard linear stereo potentiometer may be used with a 2k2 resistors soldered between its wiper and the pole of S_{6a}: the attenuation in the centre position is then minimal.

The line amplifier, IC₁₁, is a Type NE5534, which has the advantage of being able to deliver more than 8 V r.m.s. into a 600 Ω load. Its amplification has been set at $\times 6.6$

to give a sensitivity at the line inputs of 150 mV r.m.s. for a nominal output of 1 V r.m.s. (if a 'real' balance control is used).

Immediately at the output of the opamp are two parallel-connected 10 μ F film capacitors, C₂₄ and C₂₅, that isolate any offset in the preamplifier from the power amplifier in use (remember that all opamps in the signal path are DC coupled when the tone control is not in circuit). The layout of the printed-circuit board allows the use of either MKT or MKP types.

The output contains a relay that provides a delay at switch-on to suppress any switching noises in the power amplifier. This relay may be switched off if listening via headphones only is required. The delay circuit is based on T₉. When the supply is switched on, capacitor C₇₈ is charged slowly via resistor R₉₃, so that it takes a little time before the base-emitter junction voltage has reached the value at which the transistor switches on. When the supply voltage is removed, C₇₈ discharges fairly rapidly via D₅ and the relay is deenergized virtually instantly. The circuit has its own rectifier network, R₉₅-R₉₆-C₉₁-D₁₀-D₁₁, that makes rapid switch-off possible.

The headphone amplifier consists of a Type 5532, IC_{8a}, and a discrete complementary output stage, T₃ and T₄. Three diodes, D₁-D₃, ensure correct class-A operation. The amplifier delivers sufficient power for driving low-impedance and insensitive headphones (with the exception of electro-static ones that often require a real power amplifier). The 100 Ω resistor in the output limits the maximum current, which can rise to 100 mA with an output impedance of 8 Ω . The amplification of the stage has been set to a value at which clipping of the line output voltage of 1 V just does not occur.

The supply of the output stages, IC₈, T₃, T₄, T₇, and T₈, has its own decoupling, provided by R₉₇, R₉₈, C₁₀₀, and C₁₀₁, to prevent any feedback to the other opamps in the amplifier when the output current is high.

The power supply of the preamplifier is simplicity itself: a bridge rectifier, B₁, decoupled by capacitors C₇₉-C₈₂, buffer capacitors C₈₄ and C₈₈, and two regulator ICs, IC₉ and IC₁₀. Note that each IC in the preamplifier has additional supply decoupling in the form of an electrolytic and a ceramic capacitor.

(to be continued)

IN QUEST OF A PANGRAM – FINAL PART

by Lee C.F. Sallows

Bimagic pairs and banana-grams

A T a still later stage, I constructed a second set of matrix cards representing number-words in Dutch. Besides another series of ordinal pangrams, one of the fruits of this excursion into a new language was:

Dit autogram bevat vijf *a*'s, twee *b*'s, twee *c*'s, drie *d*'s, zevenenveertig *e*'s, zes *f*'s, vijf *g*'s, twee *h*'s, veertien *i*'s, vijf *j*'s, een *k*, twee *l*'s, twee *m*'s, zeventien *n*'s, twee *o*'s, een *p*, een *q*, zes *r*'s, vierentwintig *s*'s, achttien *t*'s, twee *u*'s, elf *v*'s, negen *w*'s, een *x*, een *y* en vijf *z*'s.

Happily, this furnishes the first-ever truly impeccable magic translation, an earlier find being:

This autogram contains five *a*'s, one *b*, two *c*'s, two *d*'s, thirty-one *e*'s, five *f*'s, five *g*'s, eight *h*'s, twelve *i*'s, one *j*, one *k*, two *l*'s, two *m*'s, eighteen *n*'s, sixteen *o*'s, one *p*, one *q*, six *r*'s, twenty-seven *s*'s, twenty-one *t*'s, three *u*'s, seven *v*'s, eight *w*'s, three *x*'s, four *y*'s, and one *z*.

Notice that “*en*” is now reproduced as a fully-fledged “*and*”. Strictly, it is inaccurate to speak of a translation in such cases, since the number-words themselves are not (in general) preserved. A preferable expression might be *transcription*. Another point, you might say, is that translations are inherently interpreter-dependent, whereas it is hardly likely that personal preference would influence an outcome here.

Hardly likely, yet the local curvature of logological space can warp judgement much as it can warp a sense of humour. Here, for instance, is a different English rendering of the same Dutch sentence, which is nevertheless another flawless magic transcription:

This autogram contains five *a*'s, one *b*, two *c*'s, two *d*'s, twenty-six *e*'s, six *f*'s, two *g*'s, four *h*'s, thirteen *i*'s, one *j*, one *k*, one *l*, two *m*'s, twenty-one *n*'s, sixteen *o*'s, one *p*, one *q*, five *r*'s, twenty-seven *s*'s, twenty *t*'s, three *u*'s, six *v*'s, nine *w*'s, five *x*'s, five *y*'s, and one *z*.

Sceptics may care to verify this assertion, barely credible at first sight. Once you have done so, it will be clear that even *magic* translations may depend upon the whim of an interpreter.

What is disturbing here is that the two English autograms, although differing in the number-words they use, exhibit indistinguishable texts. Or, to put it the other way around: although identically worded, the sentences list different numbers of letters. Certain minds seem to balk at this confrontation with a single text composed of thirty-

one *e*'s this time and twenty-six the next. I have even known the delight of hearing someone patiently explain to me that such a thing can only be a patent logical impossibility!

Logic, however, should never be confused with logologic. The pair of autograms above is, of course, no more than a single text to which two solutions have been found. In concrete terms: having halted at a first solution, the machine was set running again so as to examine all remaining combinations and in this case succeeded in finding another one. The possibility of such *bimagic* sentences had been in my head from the first. Little did I dream that such a pair might also have a magic Dutch translation! As usual, though, the unexpected bonus is only a spur to greed, and one ends up regretting that the foreign version is not bimagic, too. Discovery of a magic quadruple is an obvious goal for future research.

Though at first sight twisty, the cunning interlock between bimagic pairs is neatly brought out through a rather whimsical example:

This angram contains four *a*'s, two *b*'s, two *c*'s, one *d*, twenty-seven *e*'s, eight *f*'s, four *g*'s, five *h*'s, ten *i*'s, one *j*, one *k*, one *l*, two *m*'s, twenty *n*'s, fifteen *o*'s, one *q*, six *r*'s, twenty-seven *s*'s, eighteen *t*'s, five *u*'s, five *v*'s, seven *w*'s, three *x*'s, four *y*'s, one *z*, but no -.

This angram contains four *a*'s, two *b*'s, two *c*'s, one *d*, twenty-seven *e*'s, eight *f*'s, four *g*'s, five *h*'s, eleven *i*'s, one *j*, one *k*, two *l*'s, two *m*'s, twenty *n*'s, fifteen *o*'s, one *q*, six *r*'s, twenty-seven *s*'s, nineteen *t*'s, five *u*'s, six *v*'s, eight *w*'s, three *x*'s, four *y*'s, one *z*, but no -.

Abstracting the non-overlapping items for comparison shows:

ten <i>i</i> 's	eleven <i>i</i> 's
one <i>l</i>	two <i>l</i> 's
eighteen <i>t</i> 's	nineteen <i>t</i> 's
seven <i>w</i> 's	eight <i>w</i> 's.

The four numbers on the right are (by coincidence) all one greater than those on the left: a difference of one *i*, one *l*, one *t*, and one *w*. Cancelling common letters in the two lists will leave precisely that: the text on the right contains an extra *i*, *l*, *t*, and *w*. Differences at the meaning level exactly parallel those at the typographical level. Replacing one list with the other is thus an autogram-preserving change. A similar but more complicated pair of lists can be extracted from the previous example.

Notice that, despite suggestive associations, a pair of sublists so derived can never comprise true *anagrams* (they cannot con-

tain exactly the same letters). The letter content being identical, the *numbers* named could only be the same, and this is not the case. Taking into account both their slippery character and the *ban* on *anagrams*, I propose a special name for these curiosities: *bananagrams*. Beside their occurrence in bimagic autograms, a search for *bananagrams* could easily form a separate study in its own right.

How rare are bimagic cases? Of the roughly one in eight initial texts to yield a simple autogram, again something like one in eight of these turn out to have dual solutions. Is this coincidence, or might a theory be developed for predicting it? One might suppose the frequencies will change with different kinds of text, and yet experiments in Dutch give very similar results. Trimagic autograms (and their associated trimagic *bananagrams*) are naturally even rarer. Several hundred runs with the machine have located only one (with the unstimulating text, “this twenty-first pangram scored . . .”). A finer example of the polymagic genre is:

This pangram tables but five *a*'s, three *b*'s, one *c*, two *d*'s, twenty-eight *e*'s, six *f*'s, four *g*'s, six *h*'s, ten *i*'s, one *j*, one *k*, three *l*'s, two *m*'s, seventeen *n*'s, twelve *o*'s, two *p*'s, one *q*, seven *r*'s, twenty-nine *s*'s, twenty *t*'s, five *u*'s, six *v*'s, eight *w*'s, four *x*'s, four *y*'s, and one *z*.

But this pangram tables five *a*'s, three *b*'s, one *c*, two *d*'s, twenty-nine *e*'s, six *f*'s, six *g*'s, eight *h*'s, eleven *i*'s, one *j*, one *k*, three *l*'s, two *m*'s, seventeen *n*'s, fourteen *o*'s, two *p*'s, one *q*, eight *r*'s, twenty-eight *s*'s, twenty-two *t*'s, six *u*'s, four *v*'s, eight *w*'s, four *x*'s, four *y*'s, and one *z*.

The false modesty of the first is countered by the second one turning the tables!

So much then for the products of the pangram machine. Far from everything has found room for inclusion here. Aside from space considerations, the charm of such baubles is limited, one autogram soon seeming much like another. A few enthusiasts will continue to find fascination, I suppose, and indeed new topics in logology remain to be explored. One can only surmise what developments the future may reveal. Perhaps the magic sentences to come will possess a potency beside which these early essays in the craft will pale. That is certainly to be expected.

Among many possibilities that will suggest themselves to logophiles is the extension beyond letter-level autograms to those enumerating every sign employed. There is a point worth raising in this connection. In the example shown at the start of this article, the listing of signs uses full names such as “comma” and “hyphen”. Seen retrospectively

tively, this now seems less expedient than bringing them into line with the letters by reproducing the sign itself and adding an 's. Differences in British and American usage are among the recommendations for this change. Strictly speaking, however, quotation marks (or points) are demanded in using a sign as a name for itself. When this is done, the apostrophe can be dispensed with and we arrive at: "... five 'a's, two 'b's, ... one 'z', twenty-seven 's, twenty-three''s, seven 's &, last but not least, two '&'s, for instance. This is, I believe, the most natural and formally correct method, and I recommend it as a notational standard to be adopted by others. The desirability of a universal system will be apparent to interested parties.

Having said that, it is worth noting that the impulse toward sign-enumerating texts comes from a striving for completeness. This ambition can be fulfilled so long as conventional signs are treated as the atomic constituents of printed text. Atoms can be split, however, much like hairs. Reductionists will see the dot over the *j* as a typographic electron spinning in geostationary orbit above its nucleus. As such, it will qualify for separate listing. Idealists will insist that ligatures were made in Heaven, and what God hath joined may no man tear asunder. Still others may contemplate descent to more hellish levels:



Perhaps my hesitation in giving an exact definition of the term "autogram" will now be more explicable. On consideration, it is probably a good idea to confine use of the expression to normal practice and leave the subatomicists to invent their own labels.

Aside from practical constraints, the initial text used in searching for an autogram is the sole determinant of success or failure. Time was when rambling and even dubious phrasing passed muster. Kousbroek's pangram has changed all that; prolix or otherwise suspect formulations can no longer expect uncritical acclaim. At the other pole, however, is the prospect of zero-text autograms—simple, self-enumerating lists, without even the "and" at the end. Since the ten non-critical letters are excluded, an inventory of this kind would comprise at most sixteen items. The shortest such list will in a sense be the ultimate autogram.

Also relevant in this context, though of less interest to logophiles perhaps, are *self-enumerating numbers*. A digit can never be catalogued as occurring zero times, so "0" can be used as a quotation mark to distinguish use from mention.

9000302020302090

—that is to say, nine zeros, three twos, two threes, and two nines. On analogy with pangrams, pandigits can be found, too:

210007010402010302040
10501060207010801090

The 0-convention is admittedly arbitrary, but even if rationalized it would be hasty to suppose these oddities of any mathematical significance.

Still further contingencies for the future are metamagic autograms in which both words and letters come up for self-enumeration. More complicated monsters will present themselves to thought. Less fanciful are pairs of mutually-enumerating texts or even longer loops, although the difficulties these impose should not be underrated. A dyad such as

The sentence on the right contains . . .	The sentence on the left contains . . .
--	---

can not be handled independently. In effect, a magic combination must be found involving twice as many terms. Even so, the second sentence is a straightforward function of the first (or vice versa), so that the problem need not imply construction of a machine having twice as many channels. I leave it to readers to explore the ramifications of this interesting puzzle. This brings me to a final word on the pangram machine.

Disconcertingly, more than one person

who has seen the machine seems to have thought that at root it is "really" a computer. That is a misunderstanding. The term *computer* is now well established; it refers to a device incorporating a stored program of data and instructions. There is nothing in the pangram machine corresponding to a central processing unit (CPU), an arithmetic logic unit (ALU), a memory, or a program.

In fact, as I subsequently discovered, the machine is a closer cousin to a "mechanical number sieve" invented by D.H. Lehmer in the 1920s. His device shares two things in common with mine. One is the basic odometer mechanism which sees to it that *combinations* of parameters are systematically called up for testing. The other is a *parallel* monitoring system that signals the odometer to halt only if every parameter simultaneously meets a certain (not necessarily identical) condition. In Lehmer's apparatus, the former is a motor-driven set of non-concentric parallel gears with holes drilled at special points on their periphery. The monitoring system is a light beam and photocell arrangement that disconnects the motor when an alignment of holes is detected. The positions of these holes represent various finite arithmetic solutions to an equation. A combination of such cases can yield a general solution. Note well the condition to be satisfied here (hole present at a certain location); in

Slimmerick*

by Lee Sallows

"Here's a quirky quotation," said Quine,	30
"That precedes a prediction of mine:	29
If a limerick's good	16
Then its syllables could	21
Only add up to be thirty-nine' . . ."	23
Quipped a self-referentialist (Me),	28
"Self-fulfilling is my prophecy:	26
If <i>this</i> limerick ends	18
As its author intends	18
Then its word count will reach twenty-three!"	36
Answered Quine, ". . . I'd been waiting for you,	32
On discovering <i>letters</i> too few:	26
For I'd already guessed	19
Your whole poem's expressed	23
In <i>three hundred and seventy-two</i> !!	27
	<hr/>
	372

* "Slimmerik" is Dutch for a "cunning one".
The first two lines of the poem carry an allusion to the contemporary philosopher W.V. Quine's famous rendering of Epimenides' paradox
"This sentence is false":

"Yields a falsehood when appended to its own quotation"
yields a falsehood when appended to its own quotation.

Here the subject of the sentence—the phrase in quotes—is appended to its own quotation; the resulting sentence is, in fact, a quirky quotation preceding a prediction that the operation will yield a falsehood. Quine's object was to achieve self-reference while avoiding the expression "this sentence" which, it has been argued, cannot really refer to anything.

the pangram machine the criteria to be met (agreement with claimed numbers) are themselves a function of the parameters. Readers interested in further details of Lehmer's sieve will find an excellent and entertaining account in Albert H. Beiler's *Recreations in the Theory of Numbers* (Dover Books).

A challenge

The fact that two people working independently on quite different problems should have evolved closely similar mechanisms for their solution is remarkable. It suggests that the principle involved may have yet broader application. Indeed, I would like here to advance the view that the self-arresting odometer technique deserves a wider familiarity. There is a certain class of brute-force search for which it is a fundamental algorithmic structure. That is not to say I am advocating the construction of purpose-built machines (however enjoyable that might be). My idea is that an electronic *combination sequencer*, as I propose calling it, might easily comprise a standard hardware unit for integration into a (parallel) computer. This is not the place to elaborate on the idea. Suffice it to say that such a union could combine the speed of the former with the flexibility of the latter to produce a universal machine capable of accepting search problems from very different domains.

The increase in speed that both (a later version of) Lehmer's device and the pangram machine show over a conventional computer is directly attributable to their *parallel processing*. Of course, non-conventional or "super" computers using parallel processing also exist. This is worth mentioning since in *Scientific American* A.K. Dewdney has given wide publicity to a remark of mine which seemed less reckless in its original context within a letter to Martin Gardner: "I bet ten guilders [about three pounds] nobody can come up with a self-enumerating solution to the sentence beginning 'This computer-generated pangram contains . . . and . . . within the next ten years.'" Parallel processors, I should like to emphasize, are excluded from this wager.

Human perversity being what it is, not improbably some will not rest until I have been made to eat those words (it is incredible how seriously some people can take such artless taunts!). I can only hope a respectable interval will be allowed to elapse before someone succeeds. In fairness, it must be said that much of the data contained herein could be put to use in greatly narrowing the area of a brute-force search. Frankly, I have often wondered how far one might go in returning to the computer armed with the insights and information gleaned via the machine. Besides this, from the present perspective it is clear that a cooler analysis of the problem at the very beginning would have saved me a great deal of frustration later. Furthermore, subsequent discussion with various mathematicians and computer

scientists make it clear that I am very far from having explored all software approaches; in particular, a modified version of the iterative algorithm originally tried is widely regarded as holding great promise. Leaving aside the wager, my warmest encouragement goes out to any who might like to pursue this question. There still remain a host of pangrams yet to be produced in all the languages remaining. Of even keener interest, though, will be to learn of any new approaches pioneered.

Closing thoughts

An act of magic consists in doing what others believe impossible. Together with magic squares and the marvellous tessellations of Maurits Escher, autograms are among a class of objects that achieve their magical effect through creating an unbelievable *coincidence*. In the first, the coincidence is between row and column sums; in the second, between figure and ground shapes; in the third, it is between a message and its medium. These three are all examples of what Sigmund Freud (of all people) would have called *overdetermined* structures—overdetermined because they embody the simultaneous satisfaction of independent (sets of) criteria.

Of course there is already a discipline whose concern is with the creation of overdetermined textual structures: a highly technical field in which the distillation of meaning and the coalescence of form with content

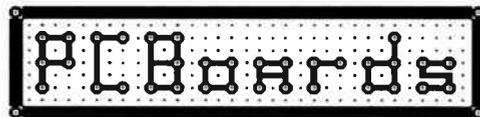
have ever been focal concepts. Its name is *poetry*. Let none suppose that anything but poetry has been our purpose here.

This epilogue contains three *a*'s, one *b*, two *c*'s, two *d*'s, thirty *e*'s, four *f*'s, two *g*'s, six *h*'s, ten *i*'s, one *j*, one *k*, two *l*'s, one *m*, twenty-one *n*'s, seventeen *o*'s, two *p*'s, one *q*, six *r*'s, twenty-seven *s*'s, twenty-one *t*'s, three *u*'s, five *v*'s, nine *w*'s, three *x*'s, five *y*'s, and one *z*. ■

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DESIGN IDEAS

The contents of this column are based solely on information supplied by the author and do not imply practical experience by *Elektor Electronics*

Advanced input stage for a left/right revolution counter

by H. Matjaz

MOST left / right revolution counters are based on a shutter fixed on the axle of the motor that interrupts two infra-red sensors—see Fig. 1. Whether the counter counts up or down depends on which IR sensor is interrupted in the first place. Most constructors connect the IR sensors directly to the input of the counter. The minimum distance between the sensors is normally 5 mm.

A problem occurs when the motor stops at the exact moment the shutter is directly between the two sensors. The motor could then be turned the other way and the counter would count, although it should not. The problem arises, of course, because of the way the sensors are connected to the counter. Clearly, an input circuit is required that obviates this and similar problems. The one proposed here counts correctly, irrespective of how many times the motor changes direction or at which angle it stops.

Method of counting

The method of counting is based on the traditional shutter and two IR sensors as shown in Fig. 1. The counter must count UP when the sensors are interrupted in the sequence shown in Fig. 2a. Logic high means that the sensor is interrupted; logic low that it is not interrupted.

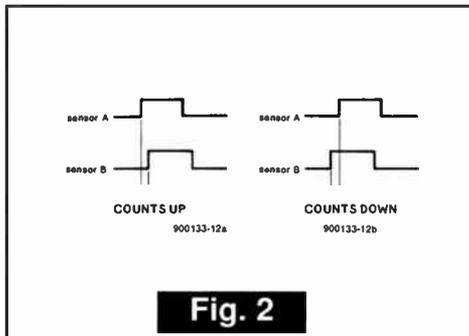


Fig. 2

Circuit description

The circuit of the input stage is shown in Fig. 3. When both sensors are not interrupted, the level at A and B is high (+5 V). When sensor A is interrupted, the level at A goes low. When sensor B is interrupted, the level at B goes low. Schmitt triggers Type

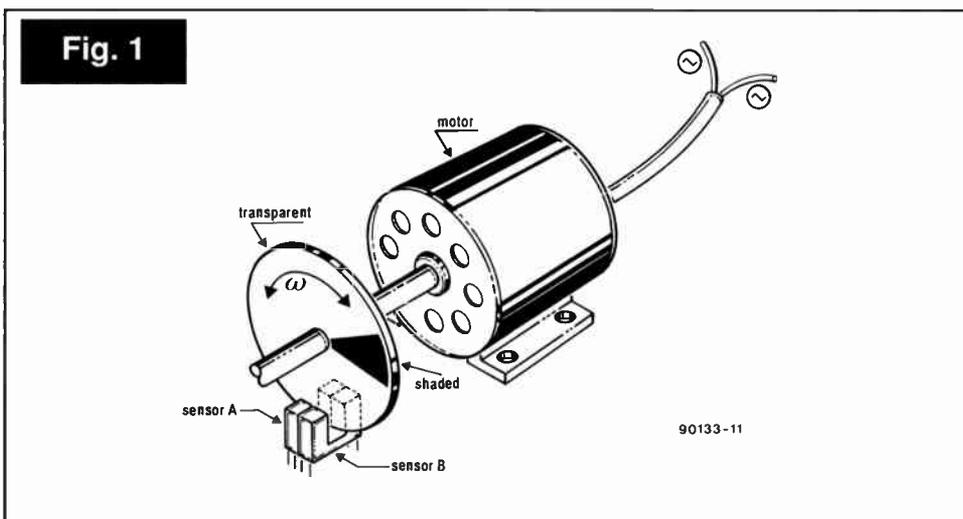


Fig. 1

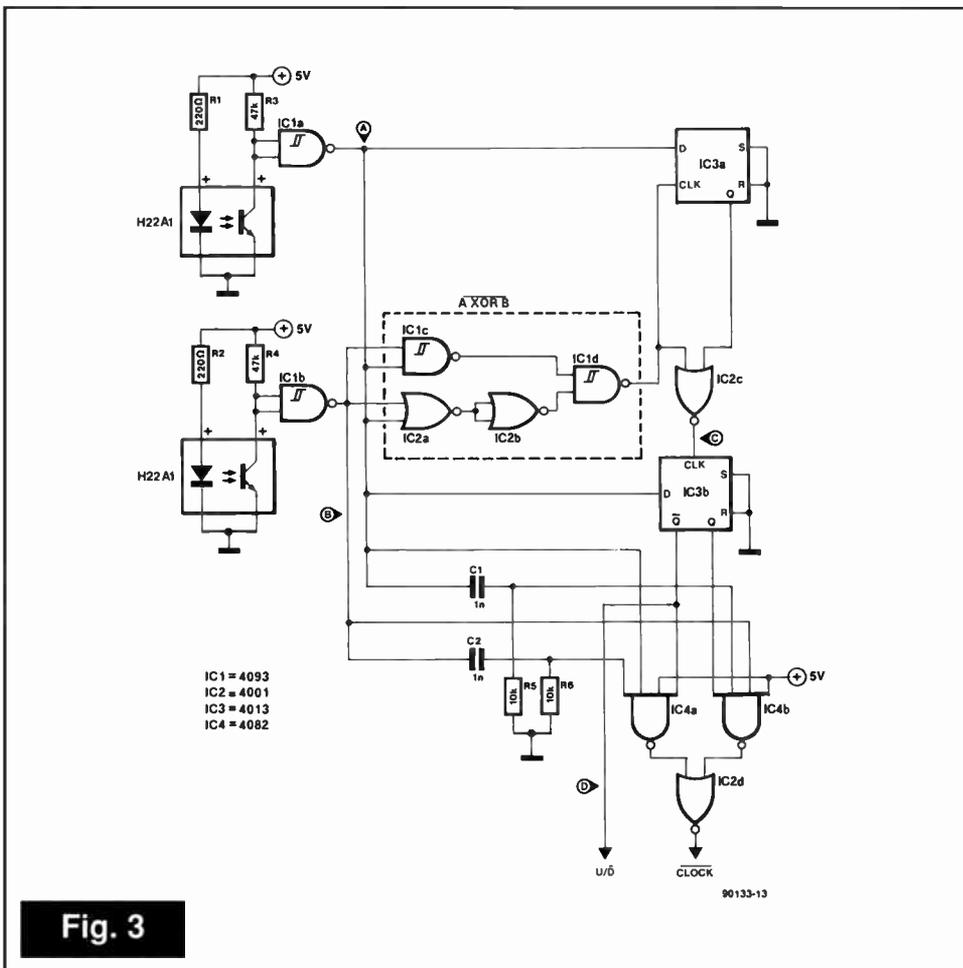
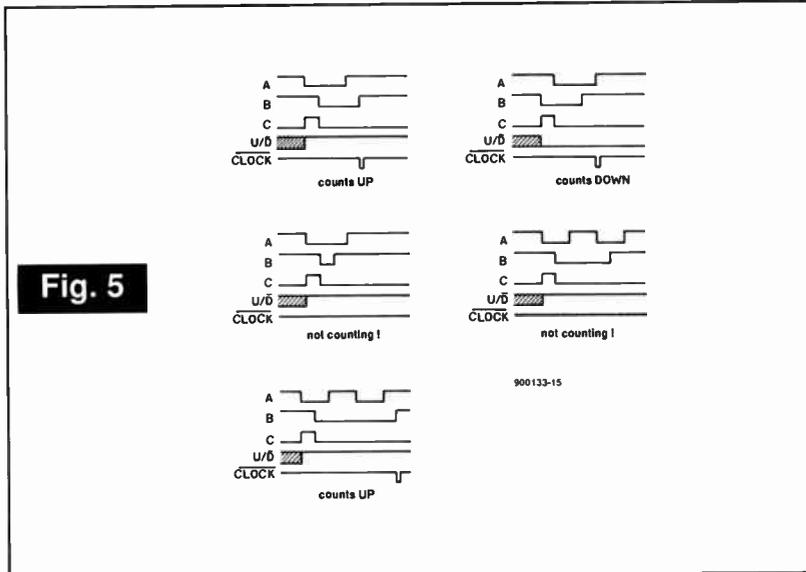
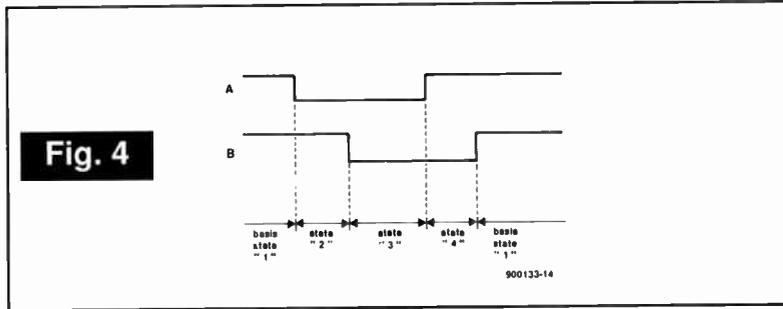


Fig. 3



4093 are used here to ensure that the transition of the sensor output from high to low or vice versa is fast enough for the circuit to operate satisfactorily.

Production of an UP counting $\overline{\text{CLOCK}}$ pulse depends on three conditions being met:

- the level at D must be high;
- the level at A must be high;
- the level at B must change from low to high.

Similarly, production of a DOWN counting $\overline{\text{CLOCK}}$ pulse depends on:

- the level at D being low (that is, the Q output of IC_{3b} is high);
- the level at B being high;
- the level at A changing from low to high.

The four possible states are given diagrammatically in Fig. 4. Gates IC_{1c}, IC_{1d}, IC_{2a}, IC_{2b}, IC_{2c}, IC_{3a}, and IC_{3b} cause the level at D to be high only on the transition from state '1' to state '2'. The level at D is low on transition from state '1' to '4'. This means that the $\overline{\text{CLOCK}}$ for UP counting is produced only when sequential transition from state '1' to state '4' occurs (1-2-3-4-1). For DOWN counting, the transition should be 1-4-3-2-1. Some examples of when counting takes place or not are given in Fig. 5. Time constants R₅-C₁ and R₆-C₂ determine the width of the $\overline{\text{CLOCK}}$ pulse: for instance, if R₅ = R₆ = 10 kΩ and C₁ = C₂ = 1 nF, the width is 10 μs.

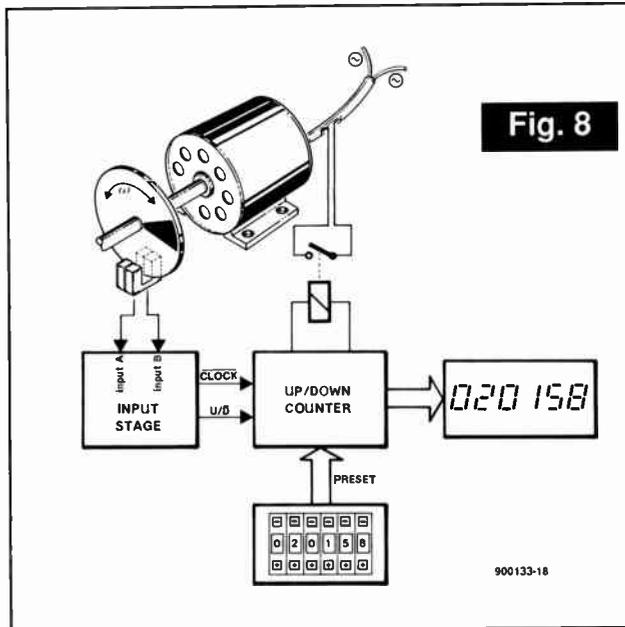
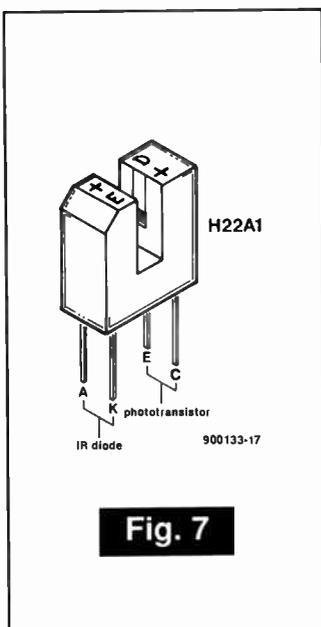
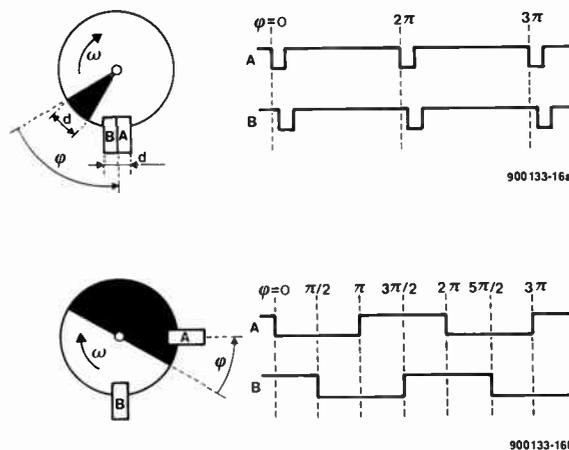
When U/ $\overline{\text{D}}$ is high, the counter must count UP, otherwise DOWN.

The shutter is made of transparent material with a sector blacked as shown in Fig. 6. The sector may have various areas, while the sensors may be placed in a number of locations. Two will be discussed.

The size of the shutter sector and the position of the two sensors in Fig. 6a is suitable for devices where the counting UP must be at the same angle as the counting DOWN ($\phi = 0$). This arrangement would find application in, for instance, a transformer winding system.

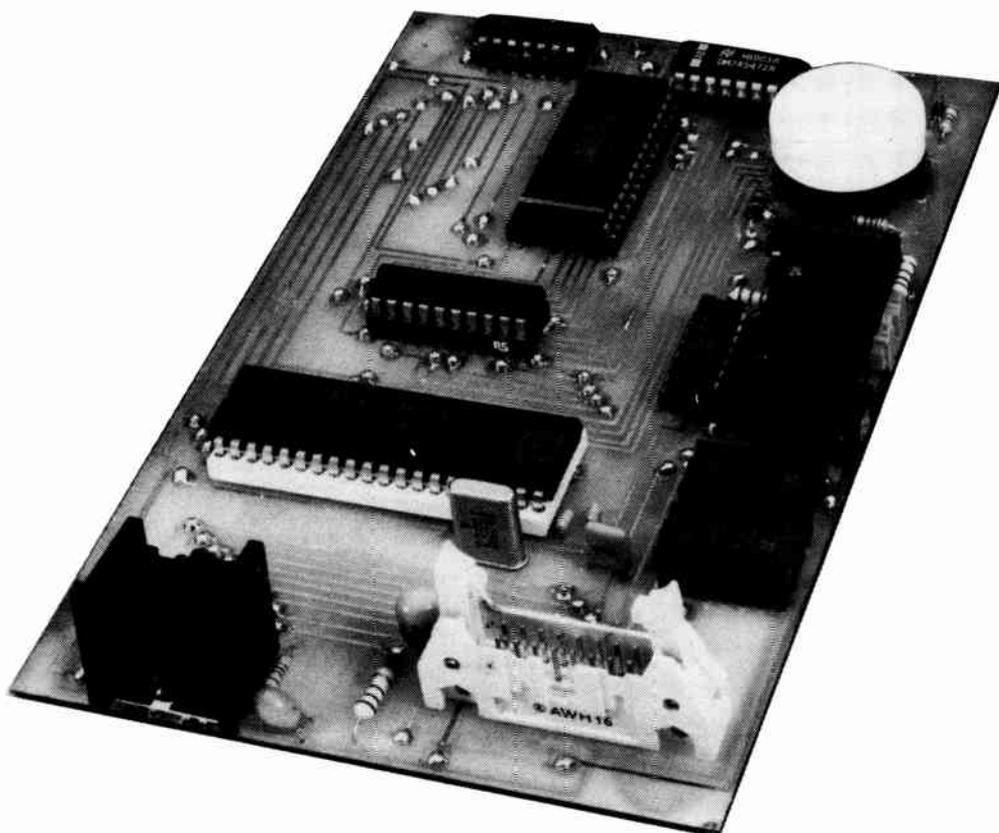
The size of the sector and the sensor positions shown in Fig. 6b are suitable for applications where the motor has a high angular velocity.

The construction of a typical IR sensor, the Type H22A1, is shown in Fig. 7, while a typical application of the input stage is given in Fig. 8.



8031 SINGLE BOARD COMPUTER

Intel's 8031 embedded controller chip contains all the essential ingredients of a microcomputer — I/O ports, a UART, interrupt lines, 16-bit timers and counters, an 8-bit CPU, and 128 bytes of RAMstack. All that is additionally required to form a fully functional computer is an operating system, a means of getting machine code to the CPU, a few operating switches and a visual display. Such a computer is described here.



R. Grodzik

THIS project uses the Intel 8031 microcontroller to form a self-contained, machine code programmable computer board, measuring only 100 × 160 mm. The operating system, all 240 bytes of it (probably the world's smallest...), is contained in a pre-programmed PROM. The project is aimed in particular at experienced software and hardware designers who want to use the 8031 in stand-alone application circuits, such as automated control.

Circuit description

The block diagram of the single board computer, Fig. 1, shows the main elements of the computer: the 8031 MPU (master processing unit), 8 KBytes of RAM (random-access memory), a PROM (programmable read-only memory) and a data indication based on two LED displays. A handful of logic ICs complete the computer.

Port 1 (lines P1.0–P1.7) provides eight I/O lines, (latched input or output), whose logic status is continuously monitored by an intelligent hexadecimal display. Port 3 (lines P3.1–P3.4) provides four additional I/O lines, of which three have a dual function of external interrupt and counter input.

The computer is controlled by the operating system firmware resident in IC3, a PROM. The instructions in this PROM enable the 8031 to read the data from the serial input port, and send it to the RAM. In addition,

the PROM provides the interrupt vectors for the system.

A major and useful feature of the board is the provision of battery back-up for the 6264 static RAM. As shown in the circuit diagram, Fig. 2, the RAM supply switching circuit consists of IC6, R6, R7, R8 and D3. With a 5-

volt supply present on the board, the 3.6-V NiCd battery is permanently charged via D3, which is forward biased. Resistors R7 and R8 form a potential divider. The voltage drop across R8 drives transistor T2, whose collector voltage is brought low. Via the output of IC6B, a logic low is applied to pin 1 of IC6A.

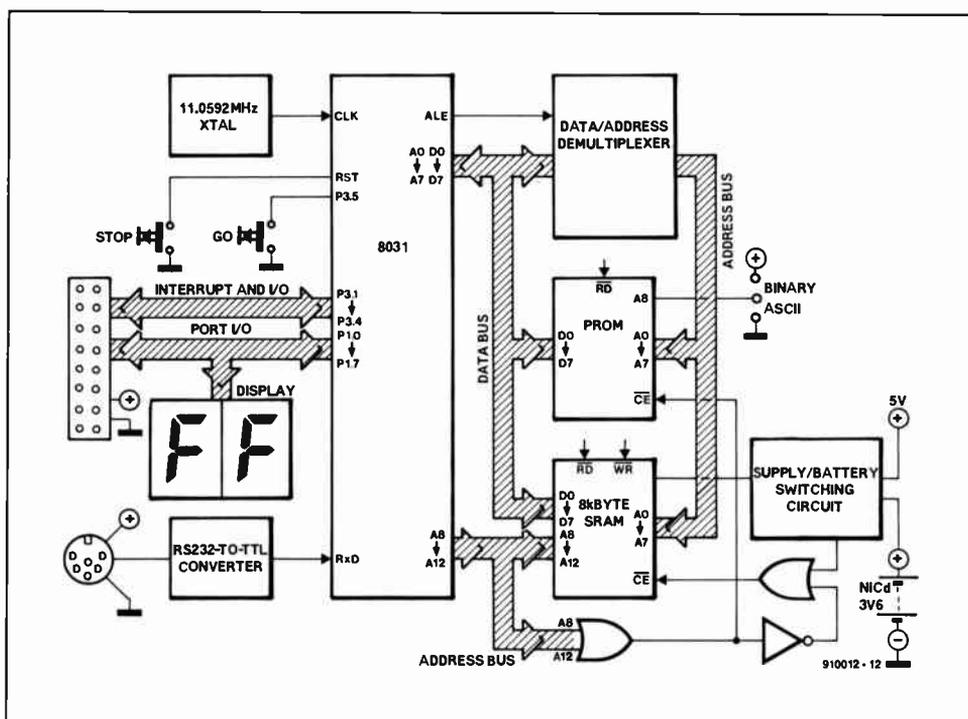


Fig. 1. Block diagram of the single-board computer.

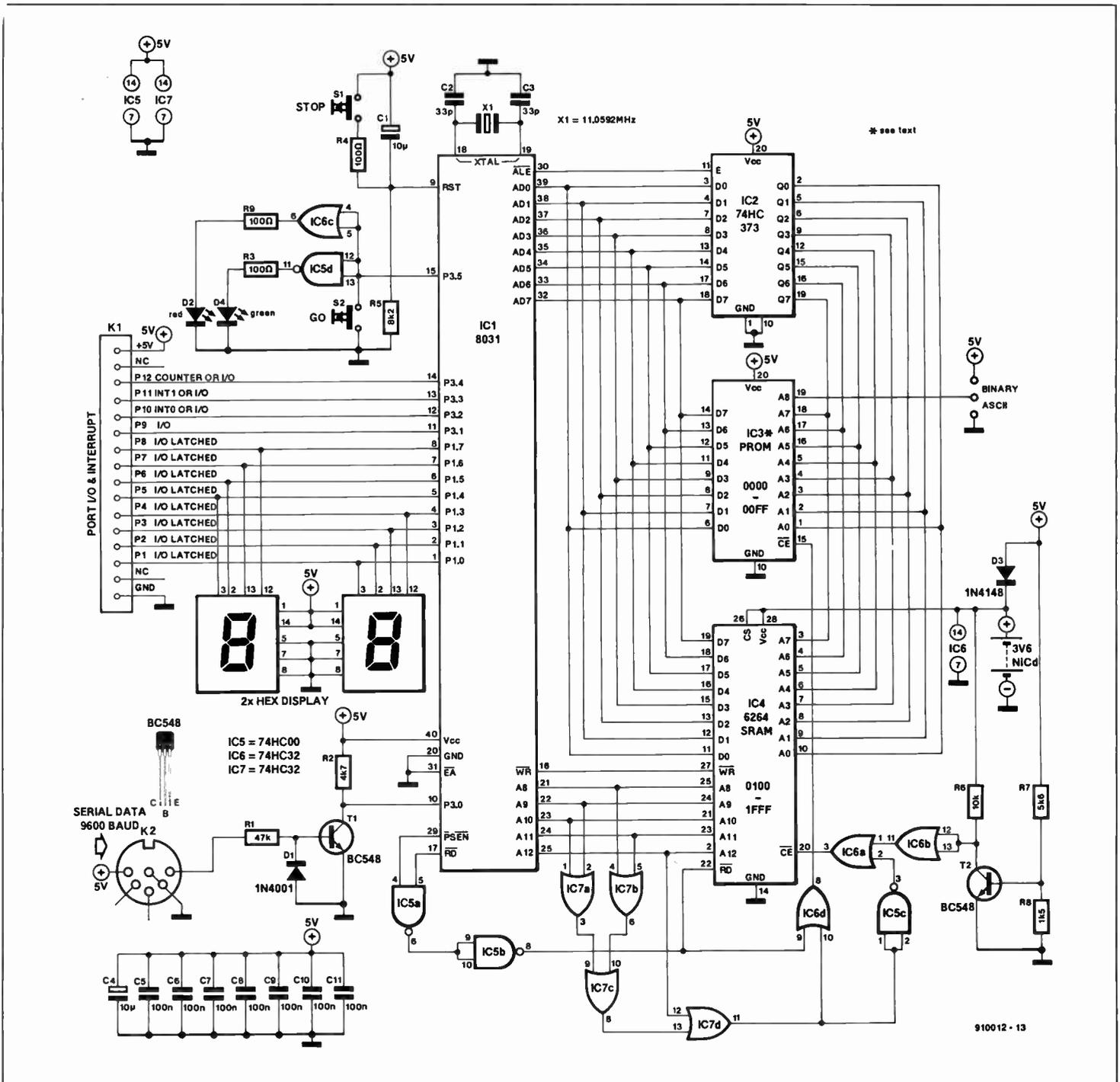


Fig. 2. Circuit diagram of the 8031-based computer. Data downloaded from the PC is shown on two 'Intelligent' hex display devices connected to port 1 of the 8031.

Pin 2 of IC6A remains high when the PROM is addressed. Above address $00FF_h$, one or more of the inputs of IC7, configured as a five-input OR-gate, go high, which in turn is inverted by IC5C. Next, a 'low' is applied to pin 2 of IC6A; pin 3 of IC6A goes low and thus enables RAM IC4, while at the same IC3 is disabled.

When power is removed from the board, diode D3 becomes reversed biased, preventing any current from the battery reaching the base of T2. Consequently, this transistor remains off, with its collector at battery voltage. The output of buffer IC6B (pin 11), is therefore high. This propagates through IC6A to pin 20 of IC4, thus disabling the RAM. Simultaneously, keep-alive voltage is supplied to pins 26 and 28 of IC4 to retain the memory contents.

Programming the computer

These days, most people have access to a personal computer (PC), and with the addition of one of many communications software utilities available, or, indeed, an 8031 assembler, it is relatively simple to produce machine code and download it via the PC's serial port to the input of the UART contained in the 8031. The code then resides in the on-board 8 KByte-large battery-backed RAM, which ensures that the downloaded program will remain intact in the event of loss of power. This method of programming a computer is particularly attractive because it dispenses with the time-consuming practice of programming and erasing EPROMs whilst debugging the software. Here, it is a simple matter to re-edit the code on the host

PC, and then download the final version to the computer board at 9600 baud. Even for the full eight kilobytes, the transfer only takes a few seconds.

The author has deliberately avoided the use of Intel-hex or Motorola-s protocols. Object code can be downloaded in binary or ASCII format. The binary code is accommodated as byte-wide RS232 transmissions: 8 data bits, 1 stop bit, no parity, 9600 bits per second. Alternatively, each byte can be downloaded as two ASCII words: i.e., $2F_h = 32_{ASCII}$ followed by 46_{ASCII} . Line feeds, return codes and spaces must not be used in this format because the board's operating system will identify them as invalid codes, and the display will start blinking rapidly.

The board control switches could not be simpler: one 'go' and one 'stop' push-button.

Pressing the 'stop' button initialises the computer; the display will indicate '00' when the system is up and running. The board is now ready to receive data at its serial port. The display will twinkle as the data is accepted, and the last code received will be displayed. The received data (if ASCII) is converted by the operating system to machine code (bytes) and placed from start address 0100_h onwards in the external memory. It will be clear that binary code does not require translation, and may be fed direct to the RAM. The content of the PROM on the computer board, a 74S472, is given as a hex-dump in Fig. 4.

Memory map and interrupt vectors

The 8 Kbytes of external RAM occupy address range 0100_h to 1FFF_h (see Fig. 3). The first page, addresses 0000_h to 00FF_h, is occupied by the PROM. Therefore the maximum addressable range of the RAM is 7936 bytes (1F00_h).

The three interrupt vectors (from external interrupts INT0, INT1 and timer 0) point to addresses at the top of the user RAM:

INT0 interrupt vector	1FFD _h
TIMER 0 interrupt vector	1FFA _h
INT1 interrupt vector	1FF7 _h

At these locations, a jump to the address of the interrupt service routine is usually placed, e.g.:

```
1FFD: 02 02 00    LJMP 0200
```

to jump to address 0200_h and service the interrupt request from there. The TIMER 1 interrupt is reserved for use by the operating system and therefore not available for general programming.

As shown by the memory map of the system, Fig. 3, page 0 of the RAM (addresses 0000_h-00FF_h) is reserved for use by the operating system. To execute the program, simply press the 'go' button. Execution of the program will commence at address 0100_h. Connect on an ADC or DAC to the port lines, and there you have it: computer control of the outside world. Data acquisition, monitoring, counting, timing — the list is endless; it all depends on you.

Construction

Construction of the 8031 computer is fairly simple, as relatively few parts are involved. A double sided PCB is used with special purpose 0.8-mm pins for pinning through. These pins are much better than odd bits of thin wire which tend to break or fall through. The CMOS displays are static sensitive and fairly expensive, so use the standard static precautions when handling these devices. It is recommended to fit the displays and all ICs in sockets, which make for easier fault-finding. The NiCd battery is secured to the PCB with a few drops of two-component glue.

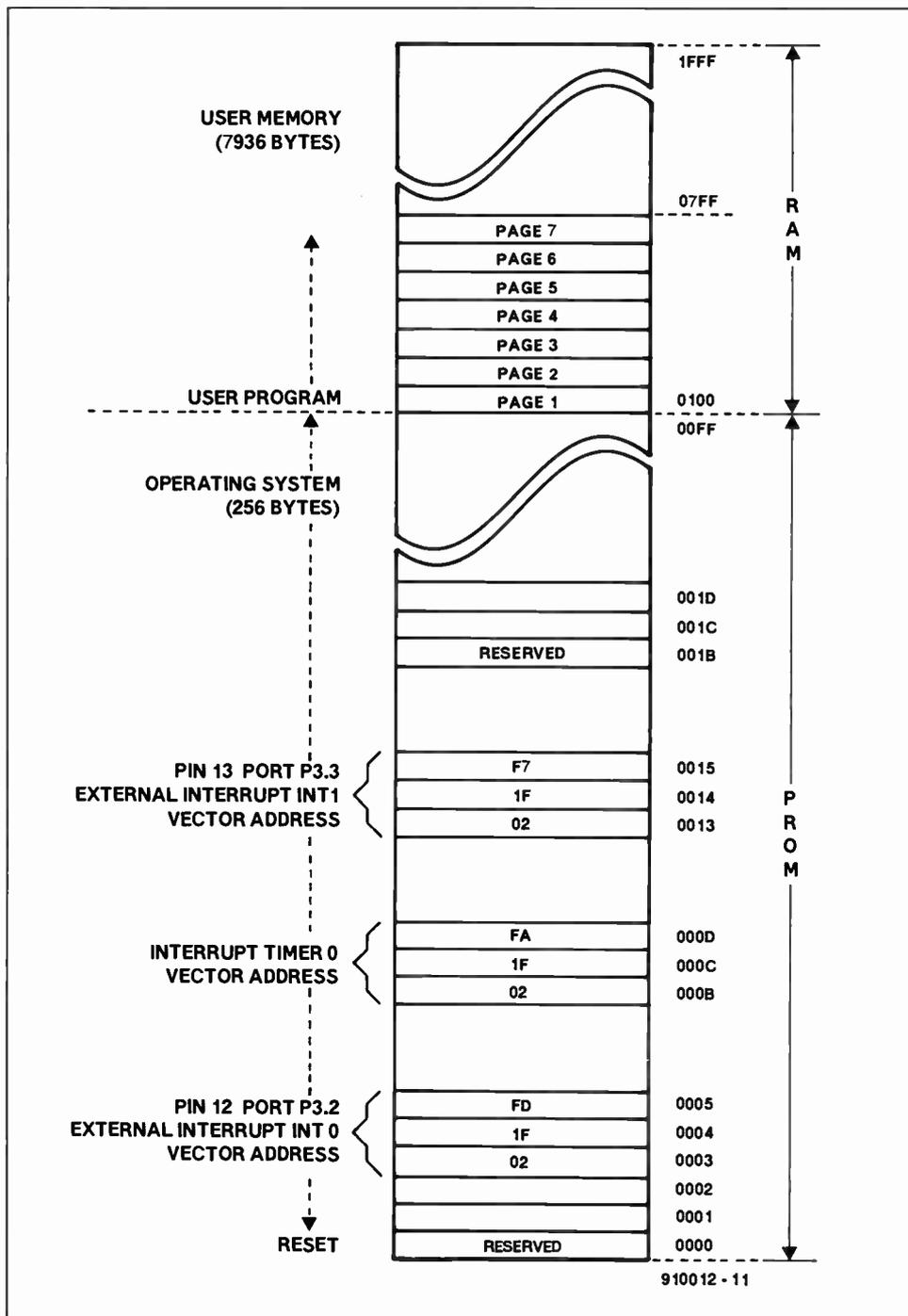


Fig. 3. Address map of the system. The first 256 bytes in the address space are reserved for the firmware PROM that contains the operating system and a number of interrupt vectors. The user memory has a size of slightly less than eight kilobytes.

For binary download operation, strap pin 19 of IC3 to +5 V (pin 20); for ASCII downloading, strap pin 19 of IC3 to 0 V (pin 10).

Once the discrete components, the crystal and IC sockets have all been soldered into place, check for solder bridges and 'dry joints'. Use an ohmmeter to check for continuity between all parts of the circuit. Next, apply power (5 V), and with the aid of a logic probe, ensure that the supply voltages and 0 V potentials are present at the appropriate pins of each IC socket. For example, check IC2 pin 20 (+5 V), and pin 1 and pin 10 (both 0 V).

Disconnect the power and insert IC1, the 8031, into its socket. This is where the author's fault-finding tool, an inexpensive transistor radio, comes in. Power up the

board, tune into the medium-wave band and you should hear a hum of microprocessor activity. Placing your finger on the PROM socket to simulate software will modulate the output from the radio. If this does not happen, proceed no further, as there is probably an open or short on your circuit board. Investigate and rectify. Next, switch off and populate the board with the remaining ICs. Power up and check with a logic probe that pins 32 up to and including 39 of IC1 are strobing. If everything is all right, the display reads '00'. If not, recheck everything.

Connecting up

Data connections to the serial port are via a 6-way DIN socket and mating plug. Note that the board is also powered via this DIN

COMPONENTS LIST

Resistors:

1	47K	R1
1	4K7	R2
3	100Ω	R3;R4;R9
1	8kΩ2	R5
1	10kΩ	R6
1	5kΩ6	R7
1	1kΩ5	R8

Capacitors:

2	10μF 16V tantalum bead	C1;C4
2	33pF	C2;C3
7	100nF ceramic	C5 - C11

Semiconductors:

1	8031 or 80C31	IC1
1	74HC373	IC2
1	PROM 74S472 (see note)	IC3
1	6264	IC4
1	74HC00	IC5
2	74HC32	IC6;IC7
2	1N4148	D1;D3
2	BC548	T1;T2
2	LED (1 green, 1 red)	D2;D4

Miscellaneous:

2	keyboard rocker switch with indicator (RS 319-843)	S1;S2
1	11.0592 MHz quartz crystal	X1
1	16-way IDC box header	K1
1	PCB-mounting 6-way DIN socket	K2
1	3V6 NiCd battery	
	0.8-mm pcb pins	

Note:

The pre-programmed PROM and the PCB artwork for this project are available from: R. Grodzik • 53 Chelmsford Road • BRADFORD BD3 8QN • ENGLAND. The price of the PROM is £15.00 including P&P.

SPRINTplus listing of file A:8031.prm in device National Semi DM74S472

```

00000: 02 00 C0 02 1F FD FF FF FF FF FF 02 1F FA FF FF
00010: FF FF FF 02 1F F7 FF FF FF FF FF 02 00 3A FF FF
00020: C2 F0 90 01 00 D2 B5 75 98 50 75 89 20 75 8D FD
00030: D2 8E D2 AF D2 AB 80 FE 80 FC 20 B5 09 75 09 00
00040: 75 08 D0 C2 8E 32 30 98 F1 C2 8E C2 98 E5 99 54
00050: 7F F5 90 12 00 68 10 F0 08 C4 F5 70 D2 F0 D2 8E
00060: 32 25 70 F0 A3 D2 8E 32 F8 54 F0 B4 30 02 80 18
00070: B4 40 06 C3 E8 94 47 40 02 80 13 E8 B4 40 02 80
00080: F8 C3 94 37 22 00 00 00 E8 C3 94 3A 40 02 80 0B
00090: E8 94 2F 40 06 C3 E8 94 30 80 E9 74 00 F5 90 12
000A0: 00 AB 74 88 F5 90 12 00 AB 80 F0 7E 80 1E 7F FF
000B0: 1F BF 00 FC BE 00 F6 22 FF FF FF FF FF FF FF FF
000C0: 74 00 F5 90 02 00 20 FF FF FF FF FF FF FF FF
000D0: 12 00 AB C2 B5 02 01 00 FF FF FF FF FF FF FF FF
000E0: FF FF
000F0: FF FF
00100: 02 00 6B 02 1F FD FF FF FF FF FF 02 1F FA FF FF
00110: FF FF FF 02 1F F7 FF FF FF FF FF 02 00 3A FF FF
00120: C2 F0 90 01 00 D2 B5 75 98 50 75 89 20 75 8D FD
00130: D2 8E D2 AF D2 AB 80 FE 80 FC 20 B5 09 75 09 00
00140: 75 08 63 C2 8E 32 30 98 F1 C2 8E C2 98 E5 99 F5
00150: 90 F0 A3 D2 8E 32 7E 80 1E 7F FF 1F BF 00 FC BE
00160: 00 F6 22 12 00 56 C2 B5 02 01 00 74 00 F5 90 02
00170: 00 20 FF FF
00180: FF FF
00190: FF FF
001A0: FF FF
001B0: FF FF
001C0: FF FF
001D0: FF FF
001E0: FF FF
001F0: FF FF

```

910012 - 14

Fig. 4. Hexdump of the firmware PROM, a type 74S472.

socket. At the host computer end, connect a single screened cable to the ground and TXD pins of the serial port. Also tie the RTS and CTS pins together.

All the port I/O, interrupt, and power lines of the 8031 computer are brought out to a 16-way IDC pin header (K1), for connection via ribbon cable to peripheral devices. As shown in the photograph of the prototype, the pin header is a box type connector with eject headers.

For further reading

Various publications are available from

Intel, detailing the programming of the 8031:

- (1) Intel 8-bit Embedded Controller Handbook (1989) (RS code 910-749);
- (2) Intel Embedded Controller Applications Handbook (RS code 910-777);

These books, and data sheets on the 8031, are available from

Intel Literature Sales • P.O. Box 7641 • Mt. Prospect • IL 60056-7641 • USA.

or, in the UK, from

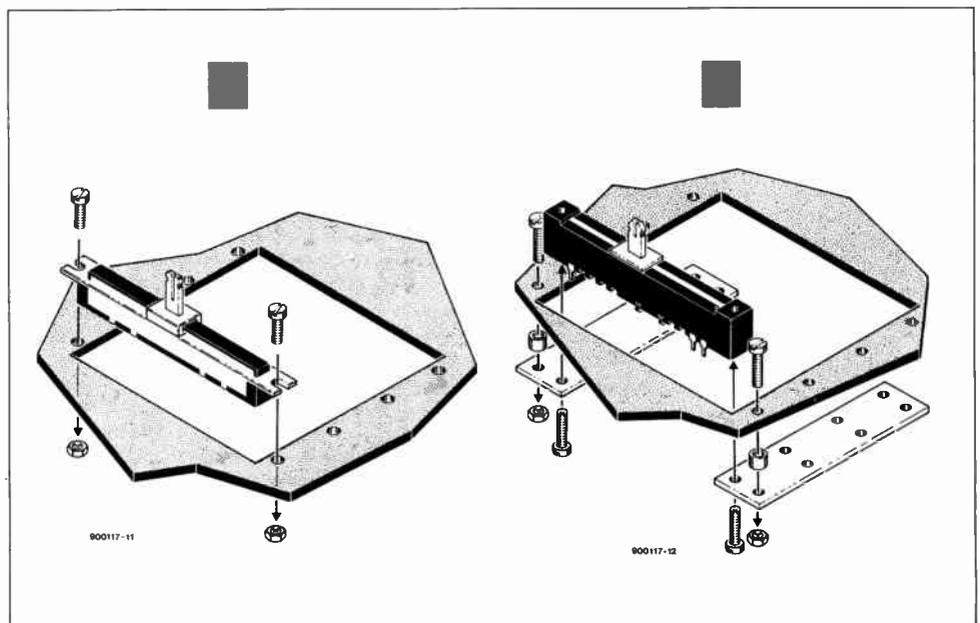
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SLIDE POTENTIOMETERS IN THE VIDEO MIXER — AN UPDATE

We understand that the mounting of the slide potentiometers in the video mixer published last year has caused a small difficulty with some constructors.

There appear to be two types of slide potentiometer around, which, although they have the same track length, are mounted differently. In some cases, the type with two mounting lugs (Fig. 1) requires a few washers, or short PCB spacers, to be positioned at the right height above the PCB. The second type (Fig. 2) has two holes through the potentiometer body. To enable this type to be secured to the PCB, mount two small support plates and two spacers at the track side of the PCB, as shown in Fig. 2. The length of the spacers is determined by the required height of the slide potentiometer above the PCB surface. ■

"Video Mixer", *Elektor Electronics* January, February and March 1990.



WorldRadioHistory

SWR METER FOR 1.5 – 70 MHz

Waste not, want not! Radio amateurs are a breed of electronics enthusiasts who like to see every milliwatt of their precious RF power arriving where it belongs: at the antenna terminals. However, budgets being what they are (RF plugs and low-loss coax cable are pretty expensive...), impedance mismatches occur readily between the transmitter and the aerial, causing power reflection. The low-cost instrument described here will tell hams operating in the 160 m through 4 m bands the ratio of the forward to the reflected RF power.

J. Bareford

A standing-wave ratio (SWR) meter is an indispensable RF power monitoring instrument found in almost any radio amateur's shack. It is often connected permanently between the transmitter/receiver rig and the coax cable to the antenna. During transmissions, it provides a relative indication of the transmitted power, as well as an indication of the ration of the forward RF power (i.e., the power fed to the antenna) to the reflected RF power (i.e., the power reflected into the transmitter owing to a mismatch at some point in the transmission line).

Since most radio amateurs have several transmitters and antenna systems, it is good operating practice to check the antenna match at a low power level, before starting a

transmission. In this way, hams protect their precious RF amplifiers from going up into smoke owing to a gross mismatch, a faulty coax relay, or a totally absent antenna connection. During the transmission, hams have one eye on the tuning scale, and the other on the needle of the moving-coil meter in the SWR instrument. Just for reassurance? No, a must to ensure the best possible signal at the receiving station.

Standing-wave ratio

The ratio of the forward RF power to the reflected RF power is called the standing-wave ratio, or SWR. Since, in the actual SWR meter, we are working with one, definitely established, transmission line impedance,

the term 'power' may be replaced by 'voltage'. Thus, in a transmission line system where a mismatch exists, we have a forward voltage, U_F , and a reflected voltage, U_R . This allows the SWR to be determined from

$$SWR = \frac{U_F + U_R}{U_F - U_R}$$

From this, it is seen that an SWR of 1 corresponds to optimum matching of the transmitter to the coax and antenna system. That is not to say that there are no losses: it only means that the transmitter output is matched to the load impedance formed by the transmission line, which includes the aerial, i.e., the load at the far end of the cable. In fact, the effect of an improperly matched antenna becomes smaller as the attenuation on the cable rises. This is because both the forward and the reflected power are subject to the same attenuation. A good discussion of the relative importance of the SWR is found in Ref. 1. Incidentally, long runs of lossy coax cable often form the perfect dummy load: any length of (matched) coax cable that introduces an attenuation of more than, say, 20 dB at the test frequency, will reflect so little power that it looks like a perfect resistance to the transmitter (keep an eye on the dissipation, though!).

Typical, tolerable, SWR values resulting from small mismatches are in the range from 1.5 to 2.0. Most radio amateurs would agree that an SWR greater than 2 is a definite cause for investigating the mismatch, as then more than 11% of the transmitted power is 'wasted' by reflection. The cause of the mismatch may be found in an incorrectly tuned RF amplifier, a piece of coax with the wrong impedance (the notorious 50/75-Ω prob-

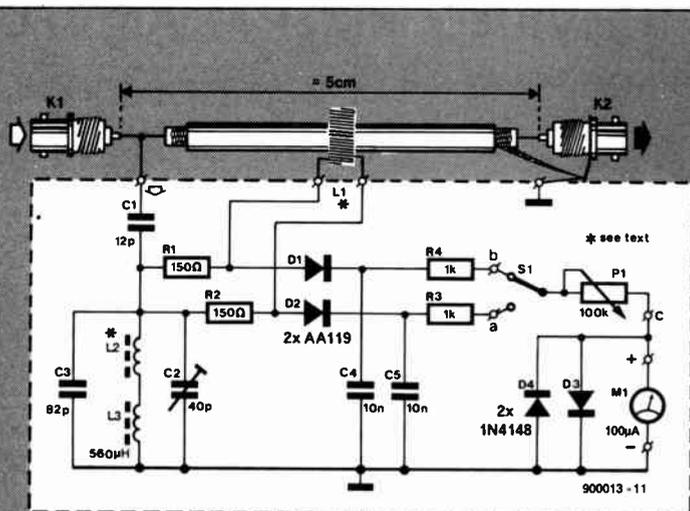


Fig. 1. Circuit diagram of the SWR meter. The RF energy produced by the transmitter is coupled capacitively via C1, and inductively via L1 to establish the ratio of the forward to the reflected power.

lem), birds on your aerial, a frozen-over aerial, the hectic of a contest, water in your coax cable, or a couple of faulty RF connectors somewhere on your attic or on the roof. Whatever the cause, make sure you eliminate it before starting to transmit, since many RF amplifiers, particularly those used for SSB (single-sideband) and other linear modes, do not like output mismatches, and produce an excessively wide output spectrum, causing splatter in the band and annoyance to your fellow hams in the neighbourhood.

The circuit

The circuit diagram of the present SWR meter is conventional, see Fig. 1. The forward and reflected powers induce RF voltages in a toroid inductor, L1, which is positioned around a short length of coax cable. Note that the cable is grounded at one side of the instrument only (a coax cable grounded at both ends does not radiate).

The RF voltage supplied by the transmitter is capacitively coupled via C1 to serve as a kind of reference against which the forward and reverse powers are measured. The coupling capacitor is connected to a tuned circuit, L2-L3-C3-C2, that serves to balance the measurement circuit at higher frequencies (in the 6 m band and possibly the 4 m band also).

The forward and reflected voltages are rectified by two diodes, D1 and D2, to establish the relative powers and thus the SWR. The AA119s used are low-capacitance point-contact germanium diodes with a low threshold voltage of about 0.2 V. A toggle switch, S1, allows the user to select a (relative) forward power indication, or reflected power relative to forward power.

Construction

The layout of the double-sided printed circuit board is shown in Fig. 2. Be sure to avoid overheating the trimmer, C2, while soldering its terminals. As shown in the photograph in Fig. 3, the two BNC sockets are connected by a short length of thin 50-Ω coaxial cable, of which the screening braid is connected to the socket and the board at the antenna side only. In the prototype, the coax cable was a 40-mm long piece of RG174U, which has an outside diameter of about 3 mm.

The winding data of the two inductors in the instrument, L1 and L2, are as follows:

Pick-up inductor L1:

Wind 30 turns of 0.2-mm dia (SWG36; AWG34) enamelled copper wire on a FT 37-43 ferrite ring core from Amidon Associates Inc. An alternative core is the FB 43-2401. Distribute the wire evenly on the core. Carefully remove the enamel coating at the ends. Put the coax cable through the hole in the core, and solder the wire ends of the inductor to the holes marked 'L1' on the PCB. Connect the coax cable to the BNC sockets as indicated above.

Choke L2:

This is made from 6 turns of 0.2 mm dia. (SWG36; AWG34) enamelled copper wire through a 3-mm long ferrite bead. After winding the inductor, carefully remove the enamel coating at the ends, and solder the device in place.

The completed printed circuit board fits in an Eddystone or Hammond diecast enclosure of about 11×6×3 cm. The size of the rectangular clearance in the lid of the enclosure depends on the meter you use. The lid is drilled to accept the threaded shafts of the sensitivity control potentiometer and the forward/reflected power switch. The connec-

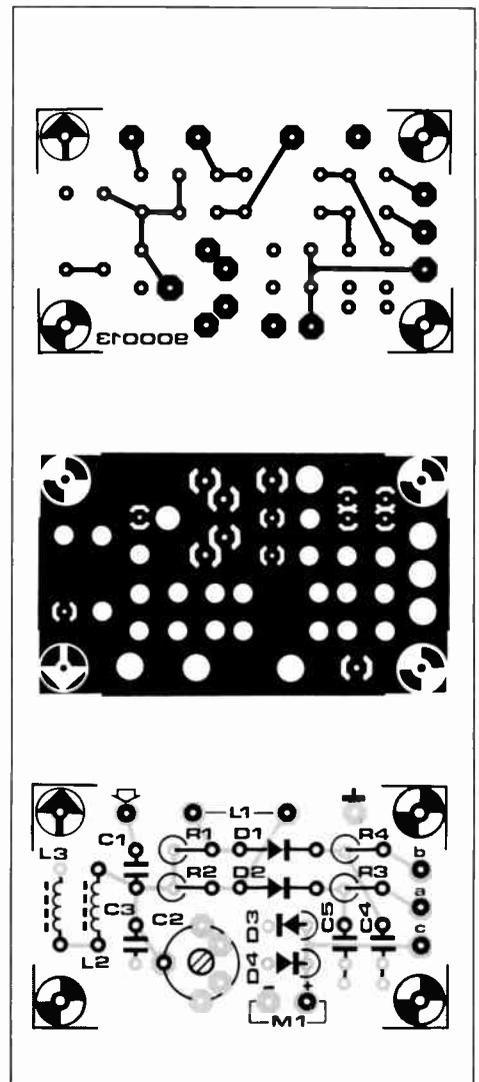


Fig. 2. Double-sided, not through-plated, printed circuit board for the SWR meter.

COMPONENTS LIST

Resistors:

2	150Ω	R1;R2
2	1kΩ	R3;R4
1	100kΩ linear potentiometer	P1

Capacitors:

1	12pF	C1
1	40pF trimmer	C1
1	82pF	C3
2	10nF	C4;C5

Semiconductors:

2	AA119	D1;D2
2	1N4148	D3;D4

Inductors (see text):

1	FT37-43 (Amidon)	L1
1	3-mm ferrite bead	L2
1	560μH	L3

enamelled copper wire 0.2 mm dia.

Miscellaneous:

1	miniature SPDT switch	S1
1	100μA moving-coil meter	M1
2	BNC socket	K1;K2
1	diecast enclosure, e.g., Hammond type 1590B	

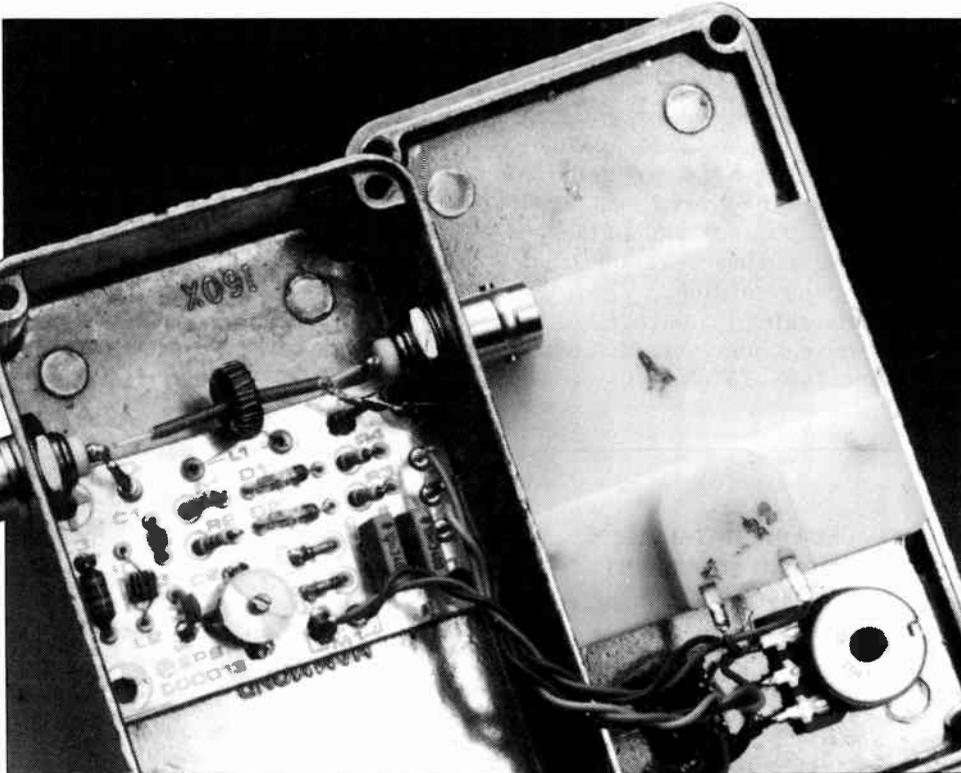


Fig. 3. A look inside the prototype. Note that the toroid core, L1, is fitted around the 3-mm dia. coax cable connected between the input and output BNC sockets.

tions between the board and the external components are shown in Fig. 4.

Test and practical use

Connect the completed SWR meter between a short-wave transmitter and a load you know to be non-reflective, e.g., a dummy load of the appropriate impedance and power rating. Transmit at a continuous output power. If the indications of forward and reflected power appear to be reversed, swap the terminals of L1, or change the lettering of the switch on the instrument.

If you work in the short-wave bands only, there is probably no need to adjust the balance trimmer, C2. If you do work at 50 MHz or 72 MHz (UK only), connect a dummy load to the output of the SWR meter, and adjust the trimmer for minimum reflected power indication while transmitting at a relatively low power.

Use the SWR meter as follows after making any change to your rig or antenna system: transmit at a continuous level, select forward power, and adjust the sensitivity control, P1, for full meter deflection. Next, switch to reflected power. The higher the indication, the worse your antenna match. ■

Reference:

1. "Losses encountered when interconnecting cables having the incorrect impedance". by Dr. P. Brumm, DL7HG. *VHF Communications* issue 3/1974.

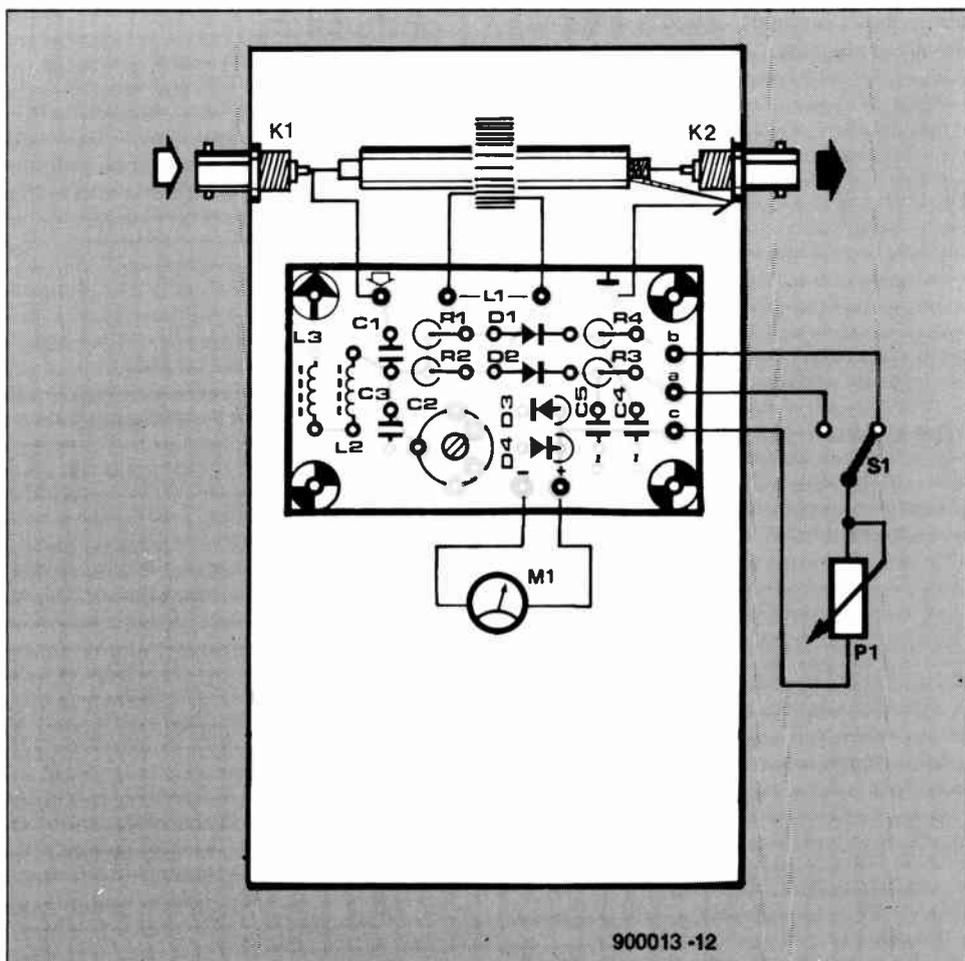
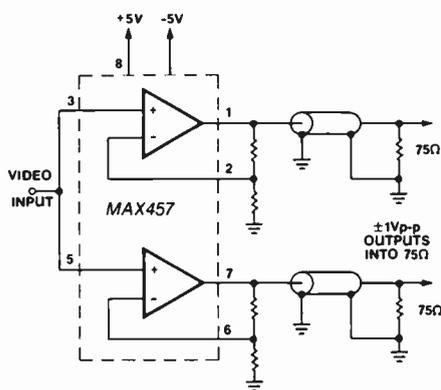


Fig. 4. Where to connect the external components.

DUAL 70 MHz CMOS VIDEO AMPLIFIER



Maxim Integrated Products introduces the MAX457, a monolithic IC comprising two 70 MHz CMOS video amplifiers which can drive 75 Ω loads. These amplifiers operate from ± 5 V supplies, and together consume only 350 mW. The only necessary external components are two resistors for gain setting, and two decoupling capacitors.

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ELECTRONICS SCENE

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BIRD FULL-LINE CATALOG OF MEASURING EQUIPMENT

Bird Electronic Corp. has released its 60-page full-line catalog of RF power measuring equipment and accessories. It also includes hundreds of photos and detailed descriptions, specifications, and ordering information.

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The catalog is available at no charge to qualified service establishments, laboratories, RF engineers, and buyers from Bird Electronic Corp., 30303 Aurora Rd., Solon, OH 44139, (216) 248-1200.

WORLD SATELLITE TV AND SCRAMBLING METHODS

By Franklin Baylin, Richard Maddox and John McCormac

ISBN 0-917893-11-5

342 pages—illustrated

Price \$39.95 + \$2 shipping

World Satellite TV and Scrambling Methods is a must for anyone interested in satellite television technology and scrambling systems. The authors have explored all components of home satellite systems from the point of view of a technician who must understand their design, operation, and repair.

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Nearly one-third of the book is devoted to a detailed study of broadcast formats (including NTSC, PAL, SECAM, and MAC), digital techniques, as well as basic scrambling and encryption methods. This material is a backdrop to a discussion of all current American and European satellite TV technologies, including the VideoCipherII, RITC, IRDETO, Oak Orion, Filmnet, Sky Channel, EuroCipher, B-MAC, D2-MAC, VideoCrypt, and Teleclub Payview III systems.

The preceding information is a prelude to the chapters on troubleshooting and setting up a test bench. Throughout the text, expert guidance on testing, servicing, and tuning is complemented by more than 200 photos, diagrams, tables, and wiring schematics.

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CABLE TELEVISION TECHNOLOGY AND OPERATIONS

By Eugene R. Bartlett

ISBN 0-07-003957-7

425 pages—illustrated

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Even though cable TV systems represent a multi-million dollar market, few technicians have at least a basic knowledge of their design and operation. Although *Cable Television Technology and Operations* is aimed at entry level cable TV technicians, it should also prove useful as a reference for those familiar with the subject. This is due to the emphasis on elementary background and the abundance of reference material.

The book covers everything related to cable TV systems—from the power supply to the cable termination, including planning, in-

NEW BOOKS

stallation, and testing. Chapter 3 has an excellent introduction to transmission line technology, covering signal reflections, cable losses, the choice of coax cable, line amplification, and minimum signal levels specified by FCC regulations. Chapter 6 discusses test and measurement procedures, providing details of the function of video insertion test (VIT) lines and notes on how to carry out such tests and interpret the results.

Although the subtitle indicates HDTV systems are discussed, little information is provided on this subject, probably because the five standards agreed by the CCIR during the 17th Plenary Assembly last May were not known when the book was written. However, its depth of information provides a solid basis for the practical implementation of HDTV signals on future systems.

Cable Television Technology and Operations is a useful, if not essential, desk-and-field reference work for all cable TV technical staff: system engineers and designers, operators, installers, and managers.

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ISBN 0-471-92360-5

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Digital signal processing applied to television technology has increased the capability of program-making facilities and improved recording and transmission. It is an essential technology for high-definition television receivers.

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400-watt laboratory power supply

October 1989 and November 1990

A number of constructors of this popular project have brought the following problems to our attention.

1. The onset point of the current limit circuit lies at about 3 A, which is too low. Solve this problem by replacing T1 with a Type BC517 darlington transistor, and R20 with a 82k Ω resistor.

2. Depending on the current transfer ratio of the optocoupler used, the transformer produces ticking noises. This effect, which is caused by overshoot in the pre-regulation circuit, may be traced with the aid of an oscilloscope monitoring the voltage across C26 at a moderate load current. The capacitor must be charged at each cycle of the mains

frequency, and not once every five cycles. The problem is best solved by reducing the amplification of the regulation circuit. Replace R17 with a 39 k Ω resistor, and create feedback by fitting it between the base and the collector of T3. Also add a resistor in series with the optocoupler. These two changes are illustrated in Figs. 1 and 2. Lower R16 to 10 k Ω , increase C24 to 10 μ F, and increase R15 to 270 k Ω .

3. Excessive heating of the transformer is caused by a d.c. component in the primary winding. This is simple to remedy by fitting a capacitor of any value between 47 nF and 470 nF, and a voltage rating of 630 V, across the primary connections. This capacitor is conveniently mounted on to the PCB terminal block that connects the transformer to the mains.

4. One final point: when using LED

DVMs for the voltage/current indication, their ground line must be connected to the positive terminal of C12.

Hard disk monitor

December 1989

In some cases, the circuit will not reset properly because the CLEAR input of IC3A is erroneously connected to ground. Cut the ground track to pin 3 of IC3, and use a short wire to connect pin 3 to pin 16 (+5 V).

Microprocessor-controlled telephone exchange

October 1990

In some cases, the timing of the signals applied to IC17 causes a latch-up in the circuit, so that the exchange does not detect the state of the connected telephones properly. Solve this problem by cutting the track to pin 1 of IC17, and connecting pin 1 to ground (a suitable point is the lower terminal of C6).

The text on the fitting of wires on the BASIC computer board (page 19, towards the bottom of the right-hand column) should be modified to read: 'Finally, connect pin 6 of K2 to pin 7 of IC3 (Y7 signal).'

S-VHS/CVBS-to-RGB converter (2)

October 1990

The capacitor marked 'C37', next to R21 on the component overlay (Fig. 7b and ready-made printed circuit board), should be marked 'C39'.

In case they are difficult to obtain locally, inductors type 119-LN-A3753 (L1) and 119-LN-A5783 (L2) may be replaced with the respective types 119-ANA-5874HM and 119-ANA-5871HM, also from Toko, Inc. Suggested suppliers are Cirkit Distribution Ltd., and C-I Electronics.

EPROM simulator

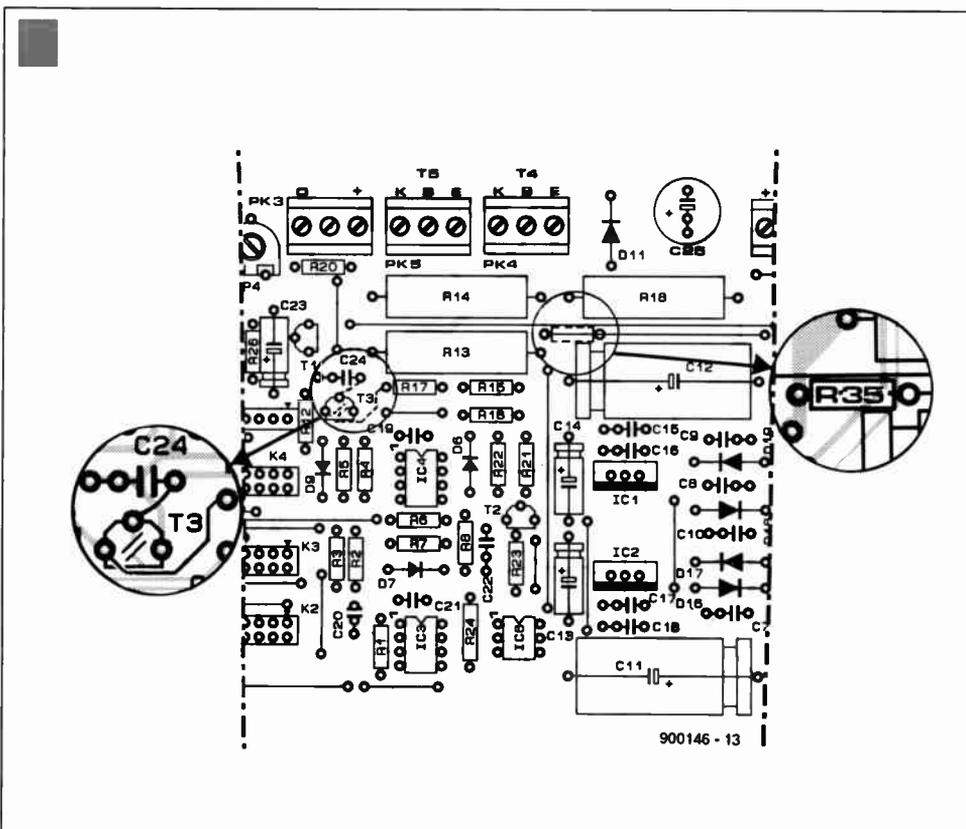
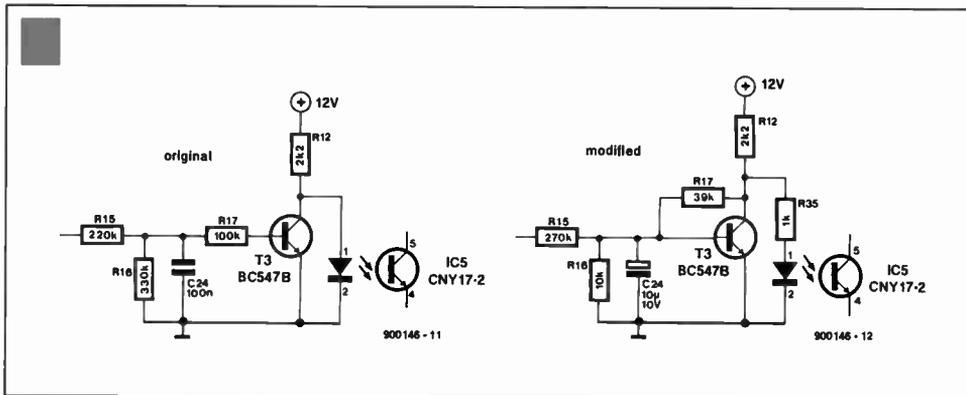
December 1989

Counters IC3 and IC4 may not function properly owing to a too low supply voltage. This problem may be solved by replacing IC12 with a 7806. Alternatively, use BAT85 diodes in positions D1 and D2.

Programmer for the 8751

November 1990

The ready-programmed 8751 for this project is available at £35.25 (plus VAT) under order number ESS 7061, not under order number ESS 5951 as stated on the Readers Services pages in the November and December 1990 issues.



CORRECTIONS CORRECTIONS CORRECTIONS

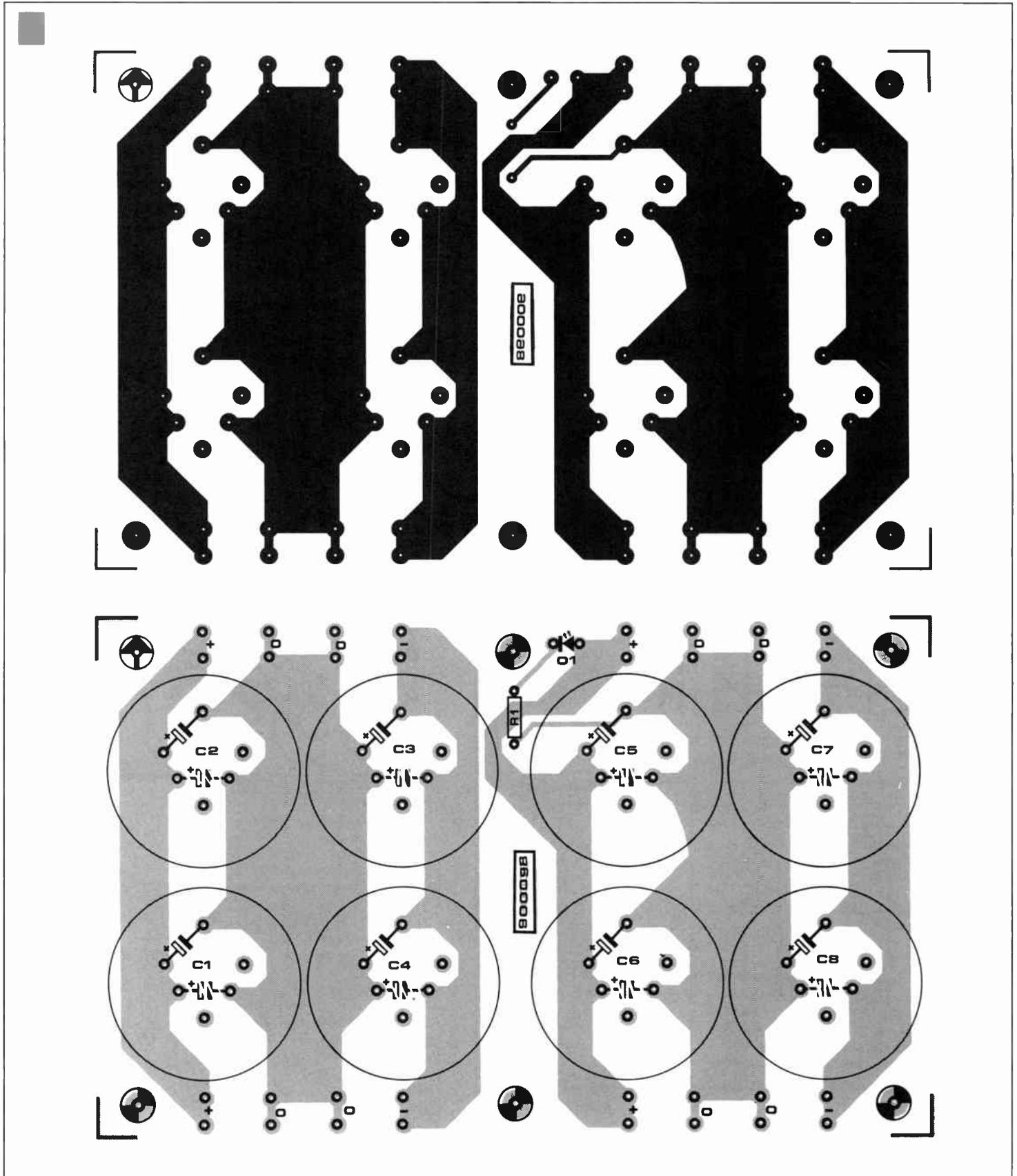
Medium-power A.F. amplifier

October and November 1990

A circuit board to accommodate the smooth-

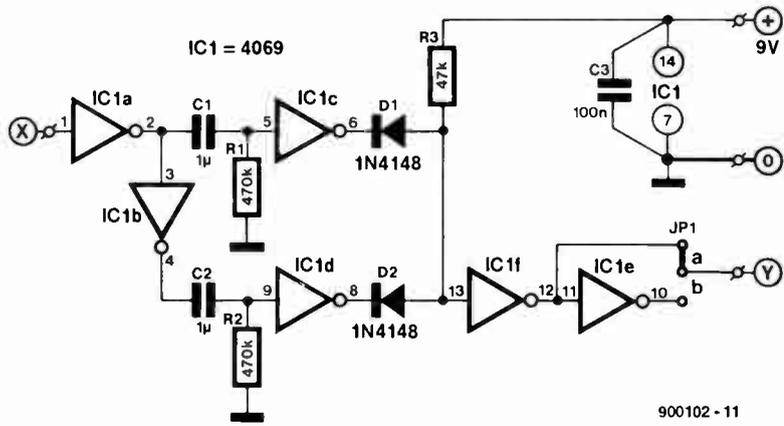
ing capacitors in the symmetrical power supply section of the amplifier was designed after publication of Part 2 of this project. The track layout (mirror image) and the compo-

nent mounting plan are given in Fig. 3 to assist readers in producing this PCB, which is not available ready-made. ■



INTERVAL CONTROL FOR CAMCORDERS — AN UPDATE

1

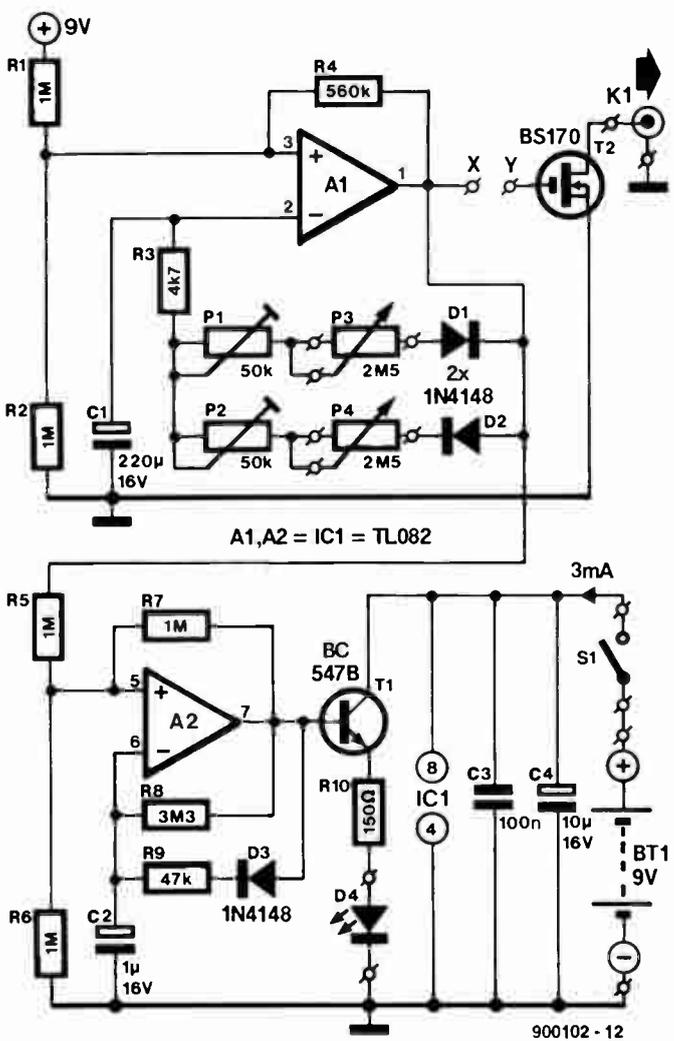


THE original design of an interval control for camcorders (Ref. 1) works with camcorders that are switched on when the RECORD switch is pressed, and off when the switch is released. However, there are also types with a toggle function of the RECORD switch. These are switched on when the RECORD switch is pressed, and off when the same switch is pressed again.

To allow the control to be used with the latter type of camcorder, the original circuit must be fitted with the extension shown in Fig. 1. The extension is inserted between terminals X and Y as indicated in Fig. 2. The track layout and component mounting plan in Fig. 3 show where to create terminals X and Y on the PCB.

With some camcorders, the proposed extension has one disadvantage: after switching on the camcorder, you are not sure whether it records or not when LED D4 flashes. If this problem occurs, make a habit of pressing the RECORD switch once, to make sure that the LED flashes when the camcorder is recording. ■

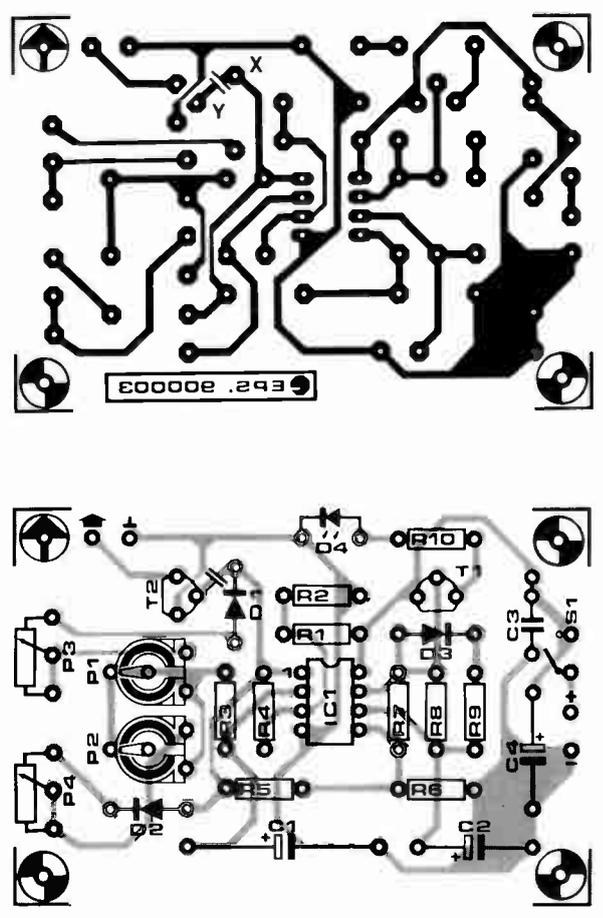
2



Reference:

"Interval control for camcorders", *Elektor Electronics* March 1990.

3



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A general description, hardware block schematic, software structure, DC characteristics, and instruction sets are given for over 70 microprocessors. To prevent the book from becoming unwieldy (and to keep costs down), timing diagrams and AC characteristics have, however, been omitted. The detailed information on all manufacturers mentioned will, however, enable any additional information to be obtained quite readily.

Included in the book are, among others:

- the 68000 series
- the 6502 family
- Z80; 8080; and 8085
- Intel's 8086; 80186; 80188; 80286; 80386
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302 CIRCUITS

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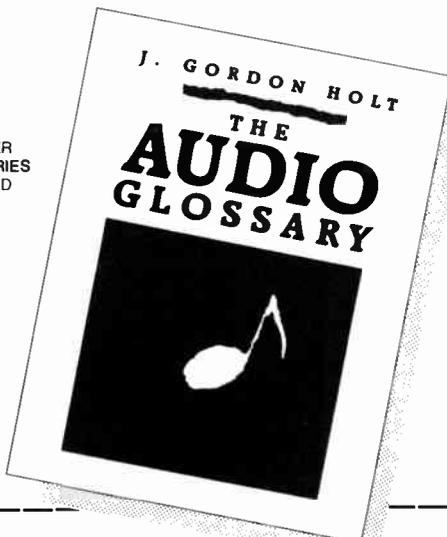
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	880178-2	13.30	1
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MOSFET power amplifier	87096	24.70	2
Digital model train	87291-1	8.40	2
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	886126	8.20	2
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Digital model train	87291-2/3	8.60	4
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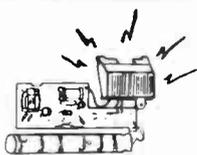
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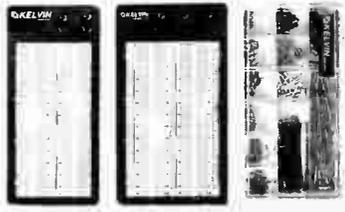


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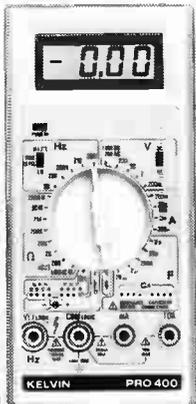
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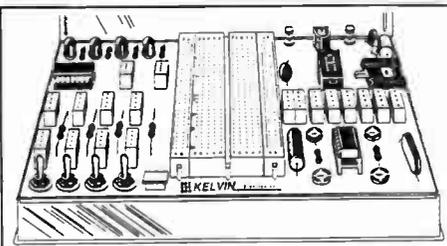


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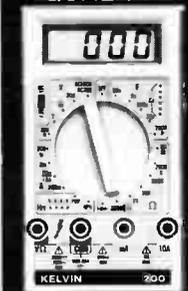
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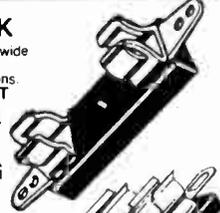
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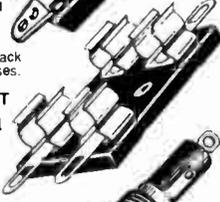
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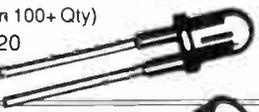
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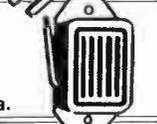
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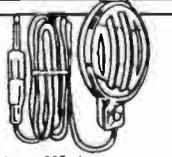
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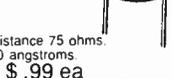
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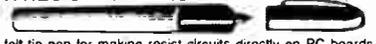
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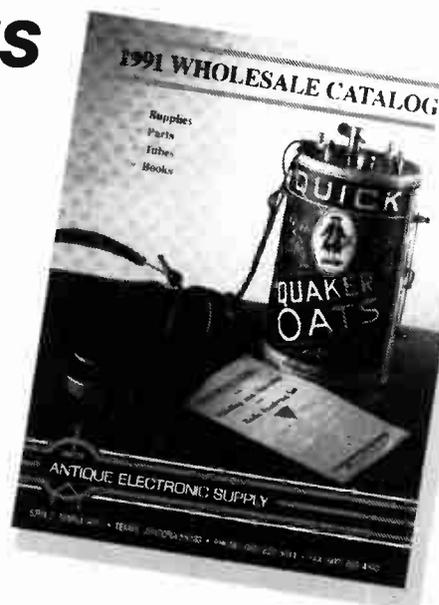
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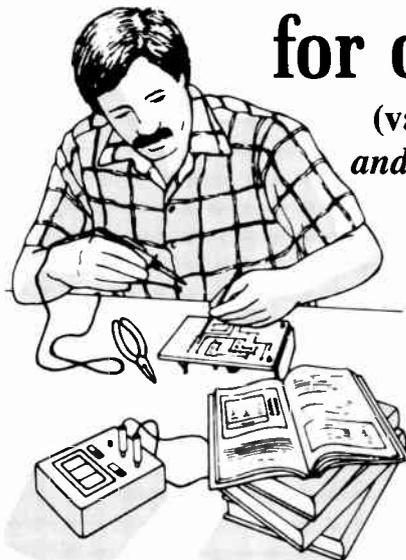
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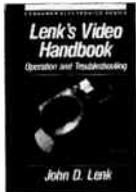
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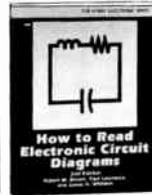
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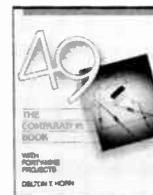
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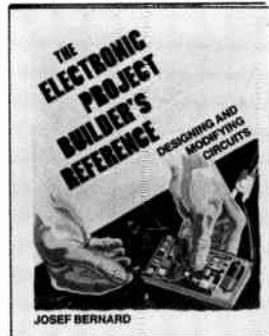
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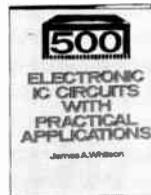
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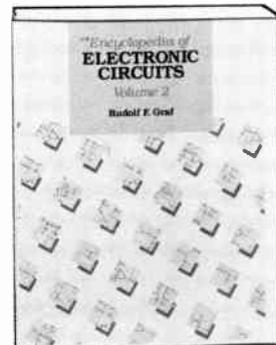
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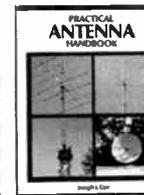
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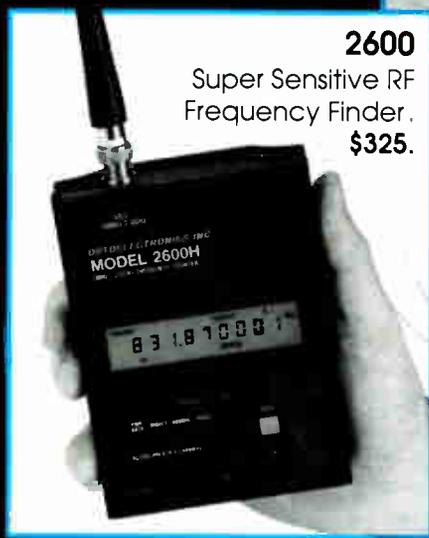
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