Proceedings of the Fourth Annual *WIRELESS* Symposium

FEBRUARY 12-16, 1996
SANTA CLARA CONVENTION CENTER, SANTA CLARA, CA

Sponsored by
Microwaves & RF Magazine

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ACKNOWLEDGMENTS

Initial plans for the WIRELESS Symposium and Exhibition included as many system-level technical presentations as possible. Unfortunately, in 1993 when this conference was first founded, many wireless systems were in their infancies and such papers were unavailable. But what grew from that first conference was a convocation of talented presenters sharing sage design advice on device and circuit levels.

As the WIRELESS Symposium and Exhibition has matured, so has the level of presentations, to a point where many system-level papers are included in the conference. To those who attend the conference or read this digest, much appreciation is offered for your patience because we are now reaching those initially-hoped-for system levels at the Fourth Annual WIRELESS Symposium and Exhibition.

Special thanks are offered to all the WIRELESS authors and presenters, whether their papers are at the device, circuit, or system level. While attending their talks or reading their papers, bear in mind that personal sacrifices were made to complete these articles and prepare presentations in time for the conference. In addition, in a field where time to market is everything, these authors spent valuable time traveling to Santa Clara for the WIRELESS Conference.

Gratitude is also due to all WIRELESS Program Chairpeople, whose support and guidance have helped to improve the technical quality of the WIRELESS Symposium year after year. It is the insights and advice of these Program Chairpeople that help make the WIRELESS Symposium and Exhibition a true engineer's conference.

Last, but certainly not least, thanks are offered to all of you attending the WIRELESS Symposium and Exhibition. Your continued support and appreciation makes all the effort worthwhile.

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Cellular/Cordless Design

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A Low Power Receiver Chip-Set Meeting Analog Cellular Specification

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Abstract

A highly integrated 3 volts receiver chip-set for AMPS system is described in this paper. The chip-set consists of three ICs from the Philips RF/Wireless family: the SA601 (LNA+mixer front-end), the SA606 (FM/IF system), and the SA7025 (PLL frequency synthesizer), which combined draws less than 25mA in operation. Measurement results show that the receiver meets all the AMPS radio receiver specifications including sensitivity, selectivity, and intermodulation spurious requirement. Practical design techniques are also covered in this paper. The chip-set offers low power, small size, and reliable receive path for modern analog cellular system.

Introduction

Philips Semiconductors is dedicated to playing a major role in the wireless communication market. Key to this goal is Philips' commitment for design assistance at all levels. This is the purpose of the SA601/SA606/SA7025 combo-board. The SA601 is a combined RF amplifier and mixer designed for high-performance low-power communication systems from 800-1200MHz. The SA606 is a low-voltage high performance monolithic FM IF system that, when combined with the SA601, results in a high performance double down-conversion FM receiver. With the SA7025, this adds another piece to the puzzle. This monolithic low power, high performance dual frequency synthesizer adds the 1st and 2nd LO's to the SA601 and SA606, respectively. Philips has combined the SA601, SA606, and SA7025 ICs onto a single board which highlights how well all three chips work together. Although this paper is directed toward meeting AMPS specification, the chip-set can also be used for other wireless applications such as ETACS and ISM band systems.

System Architecture

The block diagram of the complete chip-set solution is shown in Figure 1. Antenna frequencies from 869 to 894MHz are first fed into the LNA which has a 1.6dB noise figure at 900MHz with 11.5dB gain. The signal then goes into an 881MHz SAW filter for image frequency (two IF above the carrier) attenuation. The output of the SAW filter is down-converted by the 1st LO, which is controlled by the SA7025 PLL device. After mixing, the 1st IF frequency (83.16MHz) is created and is fed into the IF SAW filter. This SAW filter is used to knock off the image frequency sitting at two times the 2nd IF frequency above the carrier as well as the adjacent and alternate channels. This IF signal then goes into the SA606 for FM demodulation. To get the 2nd IF frequency, the 83.16MHz IF signal is mixed with the 2nd LO frequency (82.71MHz), which is phase-locked by the SA7025. The resultant 450kHz signal then goes through two ceramic filters. The output of the filter is divided into two paths. One path goes into the external Quad tank for 90 degree phase shift operation. The other path goes directly into the quadrate detector. After mixing and filtering, the audio signal becomes available at the audio output pin of the SA606.

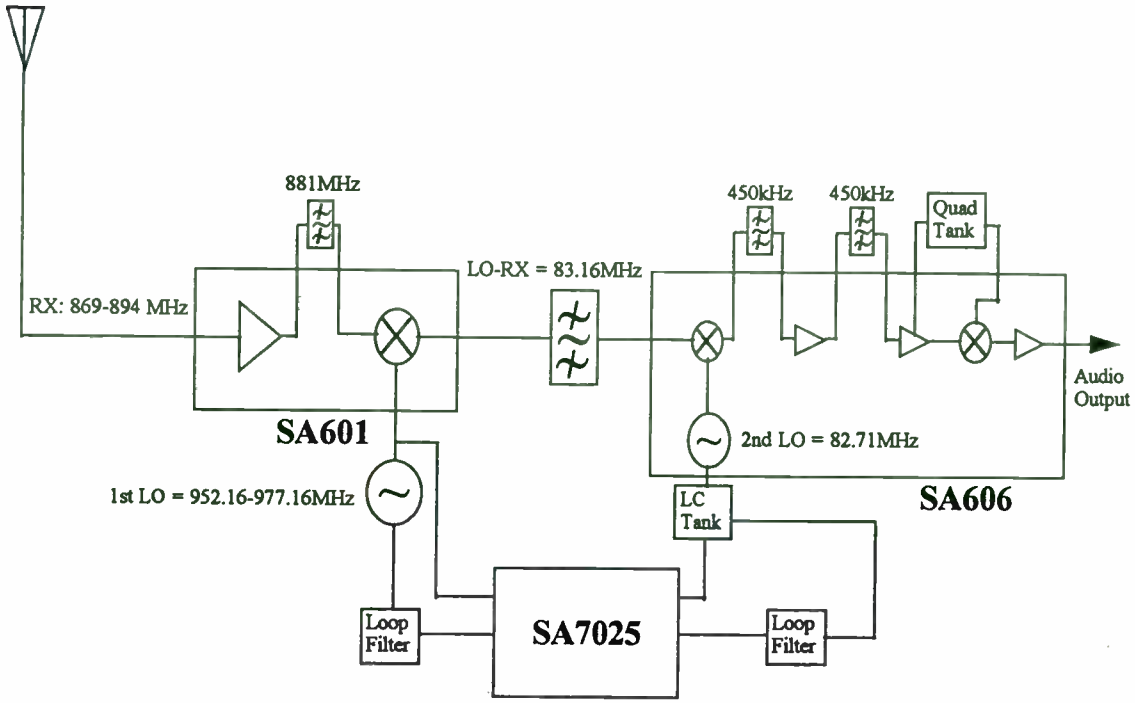

Figure 1 System Architecture

Layout Considerations

The layout of any high frequency board is critical and always challenging. Understanding each board separately is the key to combining them. Before a single-board layout was attempted, the SA601, SA606, and SA7025 individual demoboards were cascaded together with an RF SAW filter and 1st IF SAW filter. The performance with this configuration was satisfactory, thus permitting the combination of all ICs and filters on one board.

For the SA7025, the VCO is one of the most critical components of the board. Good isolation of the VCO with respect to the SA601 must be maintained because of its strong output. Also the VCO should have solid grounding underneath it.

Overall, shielding of each major IC block is highly recommended to avoid any interfering signals degrading performance and should be considered as the layout is being designed.

Impedance Matching

Impedance matching to the IF SAW filter is an involved task because the impedance of this particular filter is 850Ω // -2pF. Because of the high impedance, different steps and procedures to impedance match the IF SAW filter are referenced to application note AN1000: Evaluation of the SA601/SA606 demoboard published by Philips RF/Wireless Communication. By following those steps, improved performance will be noticed. For example, when the IF SAW filter is properly matched, the frequency response is flat and when the filter is not matched, the frequency response

shows group delay distortion (Figure 2). This group delay distortion will degrade the demoboards distortion and sensitivity.

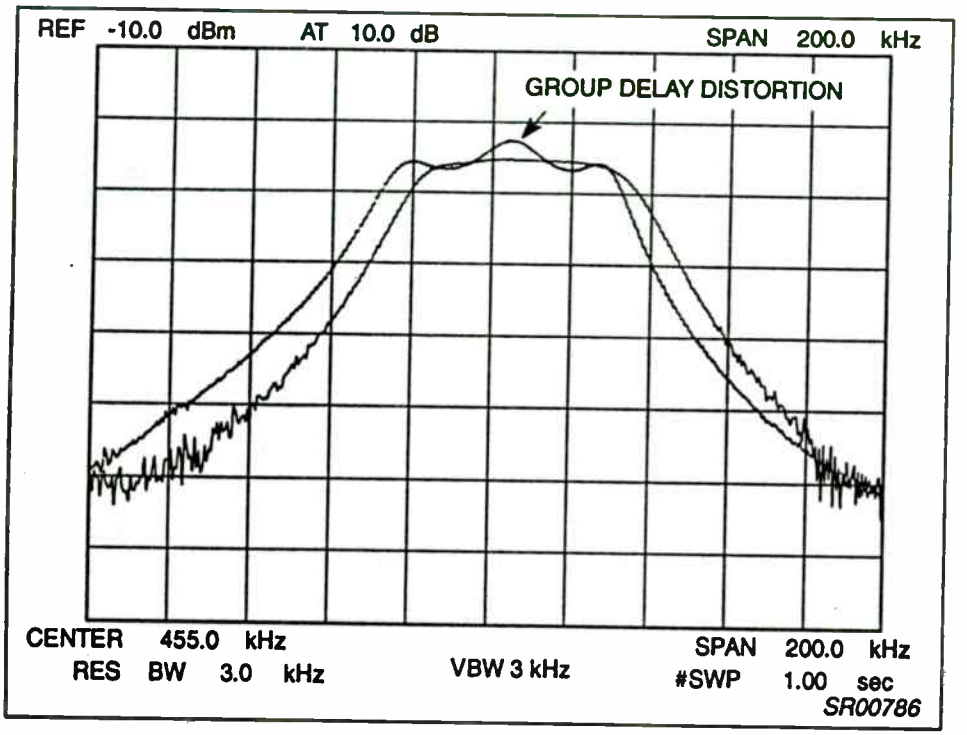

Figure 2 Group Delay Distortion

Frequency Synthesizer

The 1st and 2nd LO's are both phase-locked to the SA7025, which offers low noise and faster channel switching capability. The main synthesizer can be tuned between 952 and 977MHz with 30kHz channel spacing while the aux synthesizer is fixed at 82.71MHz. Because of the use of the fractional-N feature, the main synthesizer has a comparison frequency of 240kHz.

Replacing the crystal with a PLL is a key factor in cutting down the cost of the receiver while not sacrificing for the performance. In addition, crystal oscillator tuning will be eliminated by using a PLL. Figure 3 and 4 shows the circuits of the crystal oscillator and LC tank circuit. The internal transistor of the SA606 provides the needed element to configure a Colpitt oscillator. The frequency of oscillation is determined by:

$$f_{osc} = \frac{1}{2\pi (LC_T)^{0.5}}, \qquad \text{where } C_T = C1//C2//C3 + C4//C_{D1}$$

The shunt 10k resistor from Pin 3 to ground increases the operational current on the device which helps oscillation without affecting the internal DC bias. A 1nF coupling capacitor is sufficient to send the signal back to the SA7025.

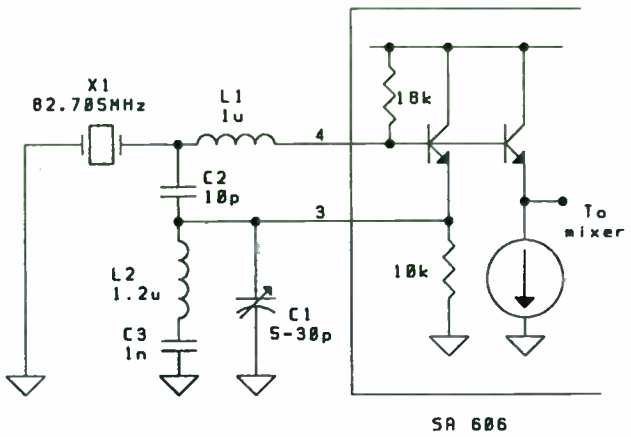

Figure 3 Crystal Oscillator

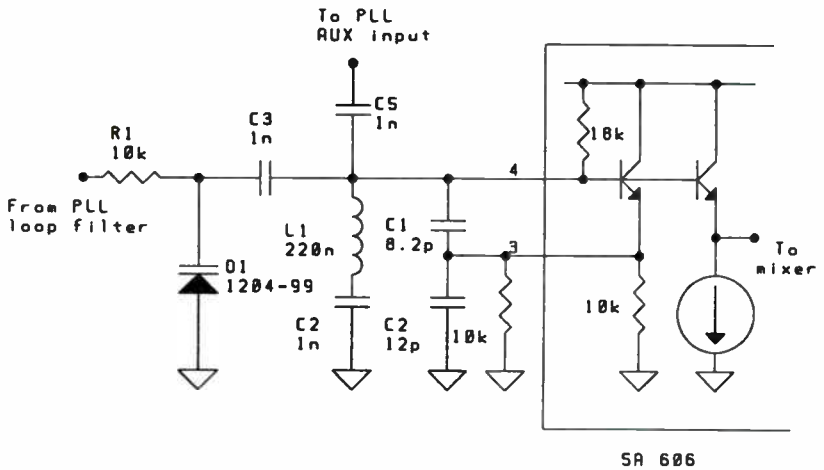

Figure 4 LC Oscillator

Receiver Performance

Table 1 provides the experimental data which pass key parameters of the IS-19-B Specifications (AMPS). The data was taken on two boards at low band, mid band, and high band frequencies. Both boards showed near repeatable results. For Adjacent Channel rejections the specification requires 16dB and both boards exceed this by 30dB. The Alternate Channel rejection and Intermodulation Spurious Response rejection exceed the specification by 6dB and 4dB

respectively. As for 12dB SINAD, the demoboard performs around -119.5dBm when AMPS specification requires -116dBm.

Frequency	12 dB SINAD	Adjacent Channel Above (+30kHz)	Adjacent Channel Below (-30kHz)	Alternate Channel Above (+60kHz)	Alternate Channel Below (-60kHz)	Intermodulation Spurious Response (+60kHz & +120kHz)	Intermodulation Spurious Response (+60kHz & +120kHz)
Board #1: Adjacent and Alternate Channel; FM dev = +8kHz, FM mod = 400Hz							
RF = 880.68MHz; LO = 963.84MHz	-119 dBm	50 dB	46 dB	73 dB	72 dB	71 dB	71 dB
RF = 869.04MHz; LO = 952.2MHz	-120 dBm	50 dB	46 dB	73 dB	72 dB	72 dB	72 dB
RF = 894MHz; LO = 977.16MHz	-119.5 dBm	50.5 dB	46.5 dB	73.5 dB	72.5 dB	71.5 dB	71.5 dB
Board #2: Adjacent and Alternate Channel; FM dev = +8kHz, FM mod = 400Hz							
RF = 880.68MHz; LO = 963.84MHz	-120.5 dBm	53.5 dB	46.5 dB	74.5 dB	73.5 dB	72.5 dB	69.5 dB
RF = 869.04MHz; LO = 952.2MHz	-121 dBm	54 dB	47 dB	74 dB	73.5 dB	73 dB	69 dB
RF = 894MHz; LO = 977.16MHz	-121 dBm	55 dB	46 dB	74 dB	74 dB	72 dB	70 dB
Requirements per IS-19-B: 2.3.1 RF Sensitivity: -116dBm or better 2.3.2 Adjacent and Alternate Channel Desensitization: 16dBm min for adjacent channel; 60dB min for alternate channel. 2.3.3 Intermodulation Spurious Response Interfence: 65dB min.							

Table 1 Measured Results

Conclusions

A receiver chip set for AMPS system is presented. Data shows that the chips set passes all the major RF specifications required by AMPS. By replacing the crystal that drives the 2nd LO with a PLL, one can cut down the cost in receiver design while preserving performance.

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A Digital Receiver for GFSK Modulated Signals at 902–928 MHz

Marc Brendan Judson and Dr. Yanpeng Guo, Philips Semiconductors

Abstract — A digital receiver for GFSK modulated signals in the 902 – 928 MHz ISM band will be presented. This solution showcases the Philips SA601 and Philips SA639 as excellent choices for 3 Volt Front-End and FM/IF applications from 800 MHz to 1.2 GHz and data rates in excess of 2 Mbps, respectively. To facilitate the development of products using this type of receiver architecture, a complete description of a currently available evaluation board along with its associated bit error rate performance data is provided. A brief comparison of this data to current receiver BER specifications will also be given.

I. INTRODUCTION

In North America the FCC allows unlicensed operation in three designated frequency bands for Industrial, Scientific and Medical (ISM) applications with power levels of less than 1 Watt if the long term average power is minimized through spread spectrum technology. This sets the stage for the development of a vast array of low power, short distance wireless digital communication products for untethered computing, cordless telephony and other applications. To facilitate the development of these communication products, a digital receiver reference design for GFSK modulated signals in the 902 – 928 MHz ISM band is currently available from Philips Semiconductors and described here in detail.

II. RECEIVER DESCRIPTION

A. Front-End Design

A.1 Amplification and Image Rejection

The Front-End of the receiver shown in Fig. 1 incorporates a Philips SA601 integrated low noise amplifier (LNA) and Mixer, a Siemens-Matshusita B4637 915 MHz surface acoustic wave (SAW) bandpass filter, a differential to single–ended conversion network and a Siemens-Matshusita B4535 110.592 MHz SAW bandpass filter.

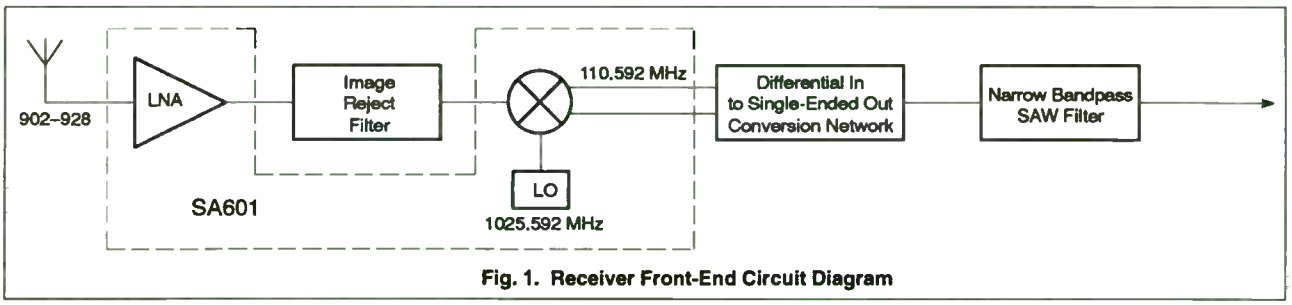


Fig. 1. Receiver Front-End Circuit Diagram

The 902 – 928 MHz RF signal initially goes through a network which optimizes the LNA for best noise figure and gain. The LNA then amplifies the signal by more than 10 dB and is then passed through a network for matching the LNA output to the 50 Ω input of the 915 MHz SAW filter.

This SAW filter should have a bandwidth wide enough to pass the frequency band and also be much less than twice the first IF frequency for rejecting the first IF image frequencies. The first IF frequency was chosen to be 110.592 MHz, which matches that used in the Digital European Cordless Telephone (DECT) standard. This first IF frequency minimizes intermodulation components and moves the image frequencies further away from the wanted RF band where they can be more easily filtered. The image reject SAW bandpass filter provides a 3 dB bandwidth of approximately 43 MHz and about 1.3 dB attenuation in the center of the passband as shown in Fig 2. The signal then passes through a network for matching the mixer input to the 50 Ω output of the image reject SAW bandpass filter.

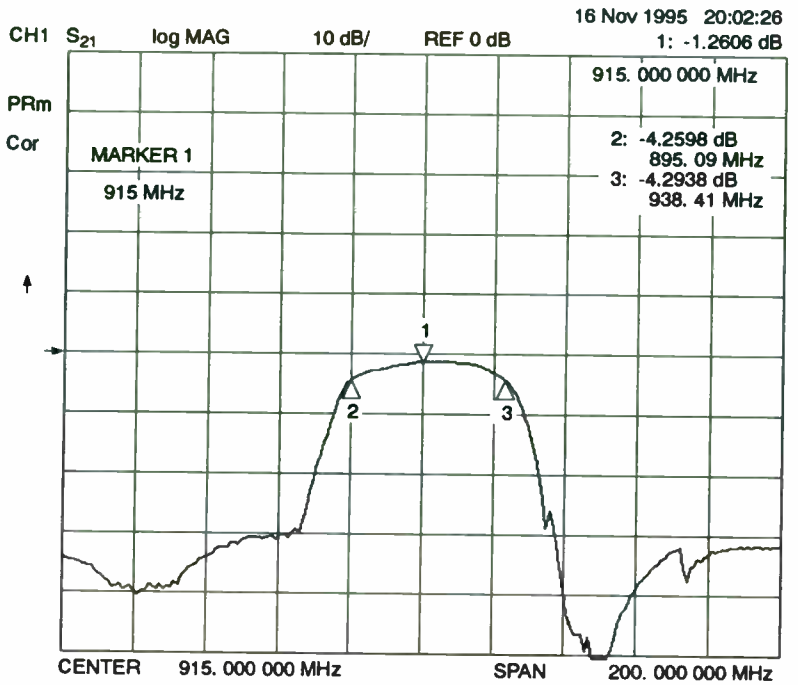


Fig. 2. Image Reject Filter Response

The easiest way to implement the matching networks required for the LNA output and the Mixer input is to use a series inductance shunt capacitance network. In this configuration, the series inductance can be implemented by a printed spiral inductor on the printed circuit board. This enables you to obtain the necessary match with just one additional external component and allows you to tune the inductance during initial board development stages by simply shorting out the windings of the spiral inductor.

A.2 Mixer Output Matching Network and IF Filtering

The mixer inside the SA601 then mixes the RF signal with an externally generated high side LO at 1012.592 – 1038.592 MHz. The power level of the LO is –5 dBm which optimizes both the $IP3_{IN}$ and the noise figure of the mixer. This mixer provides approximately 8 dB gain with a noise figure of 9.5 dB. The down converted signal at 110.592 MHz appears at two open-collector differential outputs from the mixer. These signals are then sent to a network which simultaneously combines the differential outputs into a single-ended output and provides the correct impedance matching over a narrow bandwidth to the first IF 110.592 MHz SAW filter. [1]

To understand the basic operation of the differential to single-ended conversion network, the open-collector differential outputs can be modeled as two current sources with infinite output impedance and 180° out of phase from each other as shown in Fig. 3. To these outputs the simple network shown in Fig. 5 can be used to provide the differential to single-ended conversion as well as provide some additional LO rejection due to its low pass nature.

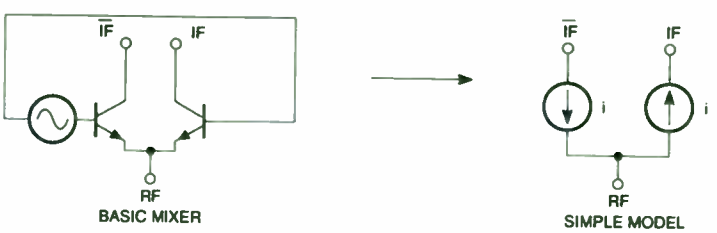
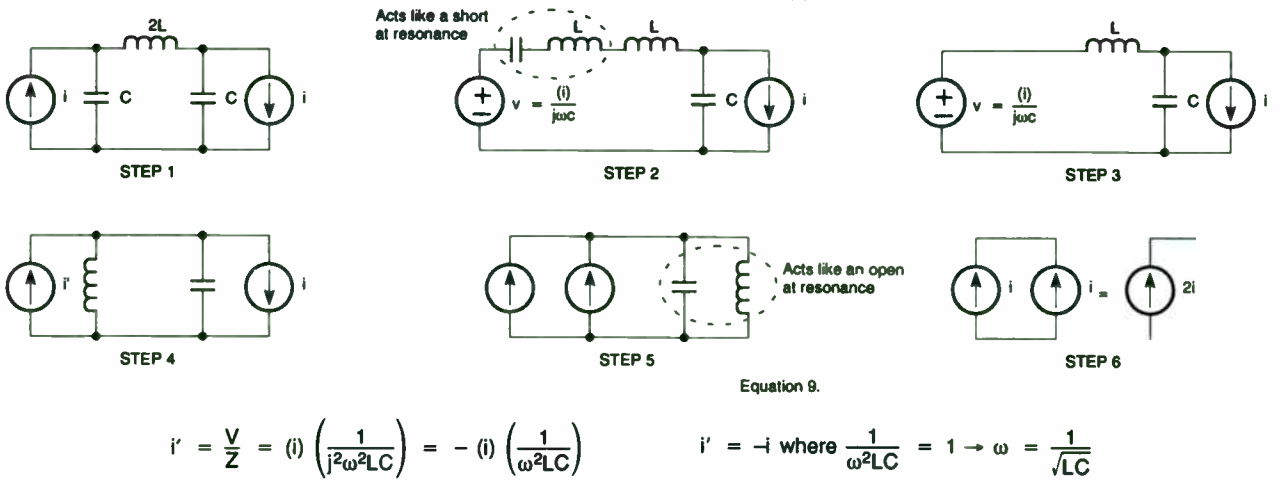


Fig. 3. Circuit Model of Differential Open-Collector Output



Equation 9.

$$i' = \frac{V}{Z} = (i)\left(\frac{1}{j^2\omega^2 LC}\right) = -(i)\left(\frac{1}{\omega^2 LC}\right) \qquad i' = -i \text{ where } \frac{1}{\omega^2 LC} = 1 \rightarrow \omega = \frac{1}{\sqrt{LC}}$$

Fig. 4. Equivalent Circuit Transformations at Resonance

The operation of this circuit can be analyzed simply by first performing a Norton to Thevenin transformation of one of the current sources and its associated capacitive load as shown in step 2 of Fig. 4. At resonance the resulting series capacitance will combine with a portion of the inductance placed between the open collector outputs creating an effective short circuit as shown in step 3. For simplicity, the open-collector outputs are assumed to be fed from V_{CC} through an RF choke and are shown with equal capacitive loads and, therefore, each will resonate with exactly half the inductance. Next, a Thevenin to Norton transformation is done on the resonant equivalent circuit resulting in the equivalent circuit shown in step 4. At resonance, the parallel RC combination shown in step 5 will present an effective open circuit, and the current source previously operated on has been shifted in phase by 180°. So, the end result is that, at resonance, the two differential open collector outputs have been converted into a single-ended current source. [2]

Now that the output conversion has been accomplished, this output needs to be connected to the 50 Ω input of the 110.592 MHz SAW bandpass filter. We could attach a shunt inductance series capacitive matching network, however, looking back at the circuit shown in step 4 of Fig. 4, if we decrease the shunt capacitance, a shunt inductance will be referred to the output at the same resonant frequency. This technique can be used to reduce the necessary matching network to a single series capacitor as shown in Fig. 5. This capacitor along with a more complete model of the mixer output circuitry, including the shunt resistances due to the output impedance of the current sources and the finite Q of the inductor between them, is shown in Fig. 6. One thing to note from this figure is that the inductor can effect the impedance that is presented to the output.

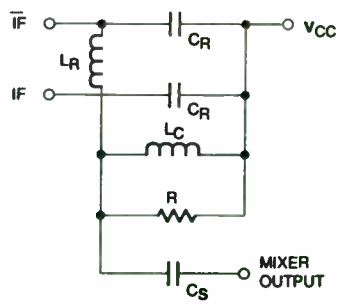


Fig. 5. External Mixer Output Circuit

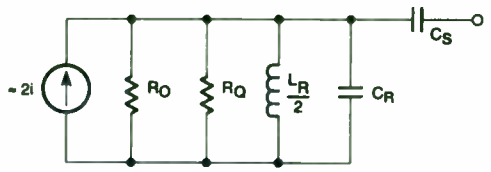


Fig. 6. Non-Ideal Mixer Output Equivalent Circuit

A general procedure for obtaining the proper output circuit is to pick inductance and resonant capacitor values to resonate close to the target resonant frequency according to $\omega^2=1/(0.5LC)$. Adjust the series capacitor to obtain a 50 Ω output impedance at some frequency near the target resonant frequency on a network analyzer. Then make fine tuning adjustments to the resonant capacitors to provide the 50 Ω impedance to the output at the target frequency. For detailed examples of this type of matching, refer to Philips Semiconductors Application Note 1777.

In addition to the above discussion, additional adjustments can be made by lowering the RF choke inductor to minimize the mixer intermodulation products. The analysis of this type of adjustment is complex and best obtained empirically and/or with the help of simulation.

The 110.592 MHz single-ended mixer output signal is then sent to a very narrow band 110.592 SAW bandpass filter. The Siemens-Matshusita B4535 110.592 MHz SAW filter has a 3 dB bandwidth of approximately 1.5 MHz and provides less than 3 dB of attenuation in the center of its passband as shown in Fig. 7. The narrow bandwidth and sharp skirts of this filter successfully attenuate spurious components outside the passband and yet it is still wide enough to accommodate most RF offset specifications. In addition to the 150 nH shunt inductance placed on both the filter input and output to match these ports to 50 Ω, initially placing variable series capacitors in the matching circuits on both sides is recommended. When the second IF mixer input is connected to the output of the filter, the match on the input will be disrupted somewhat. The variable capacitors will enable you to iteratively tune the matching circuits on both sides for optimum receiver performance. These can then later be replaced with fixed values.

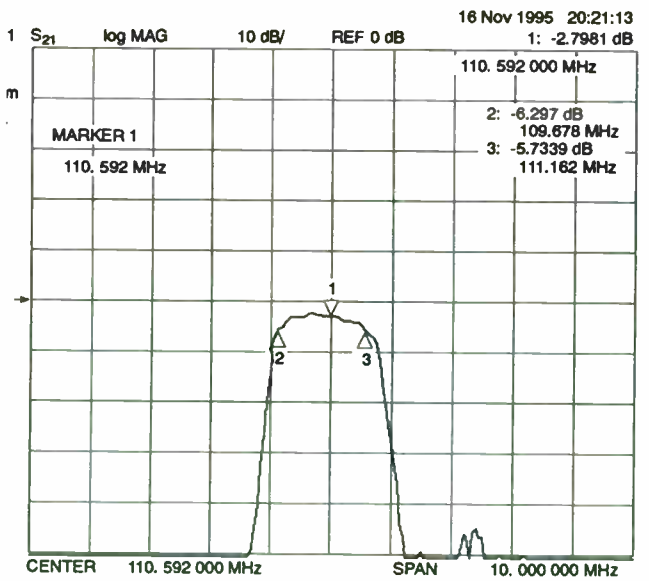


Fig. 7. 1st IF Filter Response

The specifications for the components used in the front-end circuitry are summarized in the table below.

Table 1. Front-End Component Specifications

SA601	LNA	Mixer	Filters	Image Reject Filter	1st IF Filter
Gain	11.5 dB	8.0 dB	f_C	915 MHz	110.592 MHz
Noise Fig.	1.6 dB	9.5 dB	Bandwidth	43 MHz	1.5 MHz
$IP3_{IN}$	-2 dBm	-2 dBm	Attenuation	1.3 dB	2.8 dB

B. FM/IF Circuitry

B.1 Down Conversion, Amplification and Limiting

The 110.592 MHz first IF signal is sent to an active Gilbert cell mixer internal to the SA639 which is mixed with a low side LO frequency of 100.792 MHz as shown in Fig. 8. This mixer provides approximately 12 dB of gain with a noise figure of 11 dB. The SA639 provides active transistor emitter and base connections for implementing the second LO frequency with simple on-board Colpitts, Hartley or Butler crystal oscillator circuits. In this application a modified Colpitts configuration was used to minimize the loading effects of the crystal, as well as reject parasitic oscillation modes.

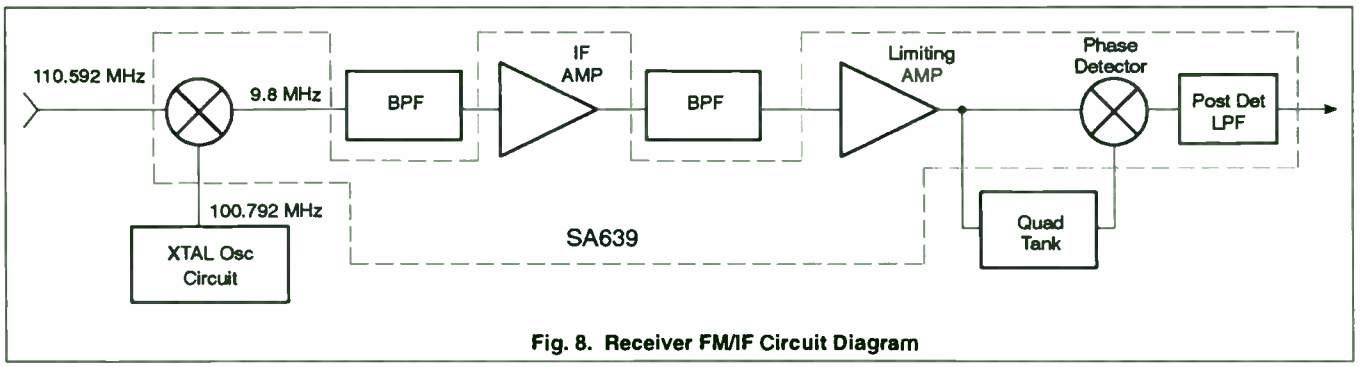


Fig. 8. Receiver FM/IF Circuit Diagram

The 9.8 MHz output of this mixer is single-ended and bandpass filtered with a simple parallel resonant circuit to ground. This presents a high impedance path to ground at resonance, thus passing the signals within its bandwidth to the input of the IF amplifier. The bandwidth of this circuit is set by the Q of the inductor used and can have an effect on the performance of the receiver if chosen improperly. The bandwidth must be sufficient to pass the FM modulated signal and is, therefore, dependent on the FM deviation used, and must also be minimized to prevent excess noise from being delivered to the following amplification stages.

The 9.8 MHz signal is then input to the IF amplifier which provides approximately 38 dB of gain. The signal then goes through a bandpass filter which is configured again as a parallel resonant circuit to ground. This provides a relatively high impedance to ground within the bandwidth of the filter, but must also attenuate the signal by 6 dB prior to the next amplification stage in order to optimize the linearity of the logarithmic received signal strength indication (RSSI). This was accomplished by simply decreasing the selectivity of the filter with a parallel 560 Ω resistor. A portion of the IF amplifier output is sent to the RSSI circuitry and then to a non-inverting amplifier. The inverting input and the output of this amplifier are externally accessible allowing the gain of this amplifier to be defined by two external resistors. These resistors were chosen to provide a gain of approximately 1+(22K/33K) = 1.67 .

The signal is then sent to a hard limiting amplifier which provides approximately 54 dB of gain. This provides an amplitude invariant output signal which then contains the frequency modulated information only. This output is then sent directly to one of the inputs of a Gilbert cell phase detector through a connection internal to the SA639. Another output of the limiting amplifier is brought out externally and passes through a quadrature tank circuit before being sent to the other input of the phase detector.

B.2 Quadrature Tank Circuit Adjustment

The tuning and the selectivity of the quadrature tank circuit has a large effect on the demodulated analog output signal and the receiver performance in general. As the Q of this circuit is increased the phase difference presented to the phase detector for any given modulation of the carrier will increase. The 12 dB SINAD performance of the receiver can be improved by as much as 3 dB with this type of adjustment.

There are two important tradeoffs that should be kept in mind while increasing the Q of this circuit. As the phase shift of the quadrature tank circuit is increased, the range over which this phase shift remains linear with frequency modulation is reduced. This has the effect of creating distortion in the system if the FM deviation exceeds this range. The tuning and the adjustment of the Q of the quadrature tank circuit can be evaluated by plotting the DC level of the demodulated output vs frequency. This can be done easily by injecting the signal through a DC blocking capacitor straight into the limiting amplifier input. If the quadrature tank circuit is properly adjusted, the center of the linear range of the S-curve will be at the IF frequency and the linear range will be wider than twice the FM deviation. [3] An even faster evaluation can be done simply by modulating the injected signal with a triangle wave and incrementally increasing the FM deviation. The demodulated output can be visually evaluated on an oscilloscope. If the quadrature tank circuit is properly adjusted, an undistorted triangle wave with well defined sharp corners will appear at the output. When the quadrature tank circuit is in the center of the linear range, the upper corner of the demodulated triangle wave corresponding to positive frequency deviation and the lower corner of the triangle wave corresponding to negative frequency deviation should distort or become more rounded, simultaneously, as the FM deviation is incrementally increased. If the upper or lower corner distorts prior to the other, the quadrature tank circuit is off center in that direction. This technique can also be used to very quickly determine the linear range of the phase detector.

The other tradeoff resulting from increasing the Q of the quadrature tank circuit is the increase in the change in the DC level of the demodulated output for a given RF frequency offset. This places tougher constraints on the comparator

DC threshold adjustment circuitry which extracts this DC level during the preamble of the communication protocol. Fortunately, the SA639 incorporates an active data switch with external connections to an integration circuit specifically for successfully providing this comparator threshold voltage. During the preamble the data switch is closed while an equal number of ones and zeros are transmitted. The capacitor in the integration circuit is then charged to match the DC level of the demodulated output. The switch is then placed in a high impedance state which inhibits the discharge of the capacitor with less than 100 nA of leakage current. This allows the receiver to tolerate higher RF offsets and thus allows us to adjust the quadrature tank circuit for higher Q, improving the receiver sensitivity. This data switch also has the added feature of maintaining a voltage on the integration capacitor during power down mode in order to decrease the time to bring this voltage to its proper level at power up.

B.3 Phase Detection and Post–Detection Filtering

The demodulated output from the phase detector then goes through a post-detection amplifier which provides both low pass filtering and isolation against load variations. The output and the inverting input of this amplifier are internally connected. This connection node and the non-inverting input are both externally accessible allowing a second order Sallen-Key lowpass filter to be easily configured. In this application the resistors were both set equal to each other at 5.6 kΩ which sets the Q of the second order lowpass filter equal to one-half the square root of the capacitor ratio. In this application the Q of the second order lowpass filter was set to be less than $1/\sqrt{2}$ which minimizes peaking at the corner frequency of the filter response curve.

B.4 Data Regeneration and Timing Adjustment Circuitry

The demodulated lowpass filtered output from the SA639 is input to a voltage comparator. The output of this device goes to V_{CC} when the input voltage is greater than the comparator threshold voltage, and goes to ground when the input voltage is less than the comparator threshold voltage. This is how the digital information is regenerated from the analog demodulated signal of the receiver. It is therefore extremely important that this comparator threshold level be set correctly at all times. This is the purpose of the preamble adjustment period mentioned in the FM/IF section above. A manual adjustment of the comparator threshold voltage is provided to enable evaluation of the circuit without having to generate the necessary protocols.

In addition to the comparator threshold, a manual timing adjustment circuit is also provided for evaluation of the circuitry in the absence of symbol timing recovery circuitry. This is implemented simply by sending the regenerated digital data from the comparator to a positive edge triggered delay flip-flop. An externally connected clock is fed into a multivibrator circuit where its rising edge and pulse duration can be adjusted by a simple external variable RC circuit. This is fed into the clock pulse input of the delay flip-flop which transfers the sampled data to the data outputs at the positive edge of the clock pulse input as shown in Fig. 9.

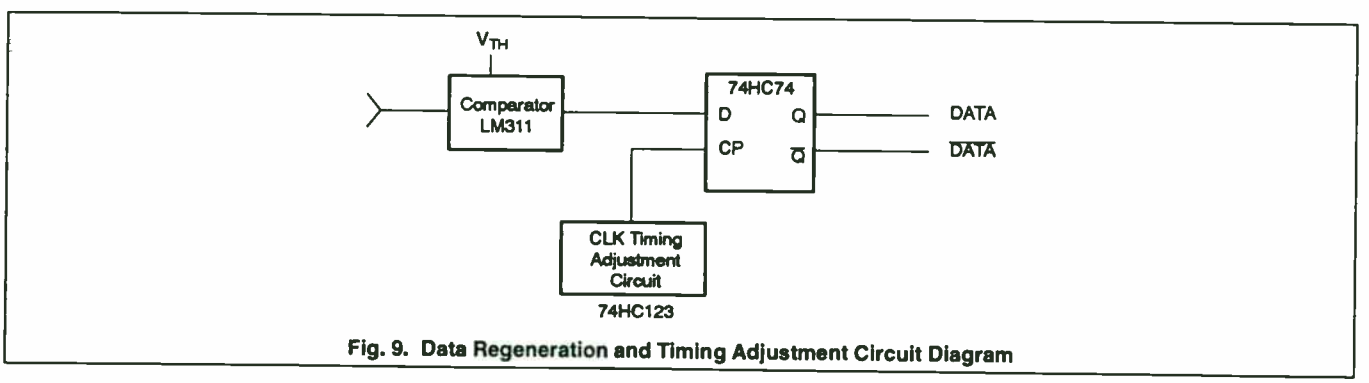


Fig. 9. Data Regeneration and Timing Adjustment Circuit Diagram

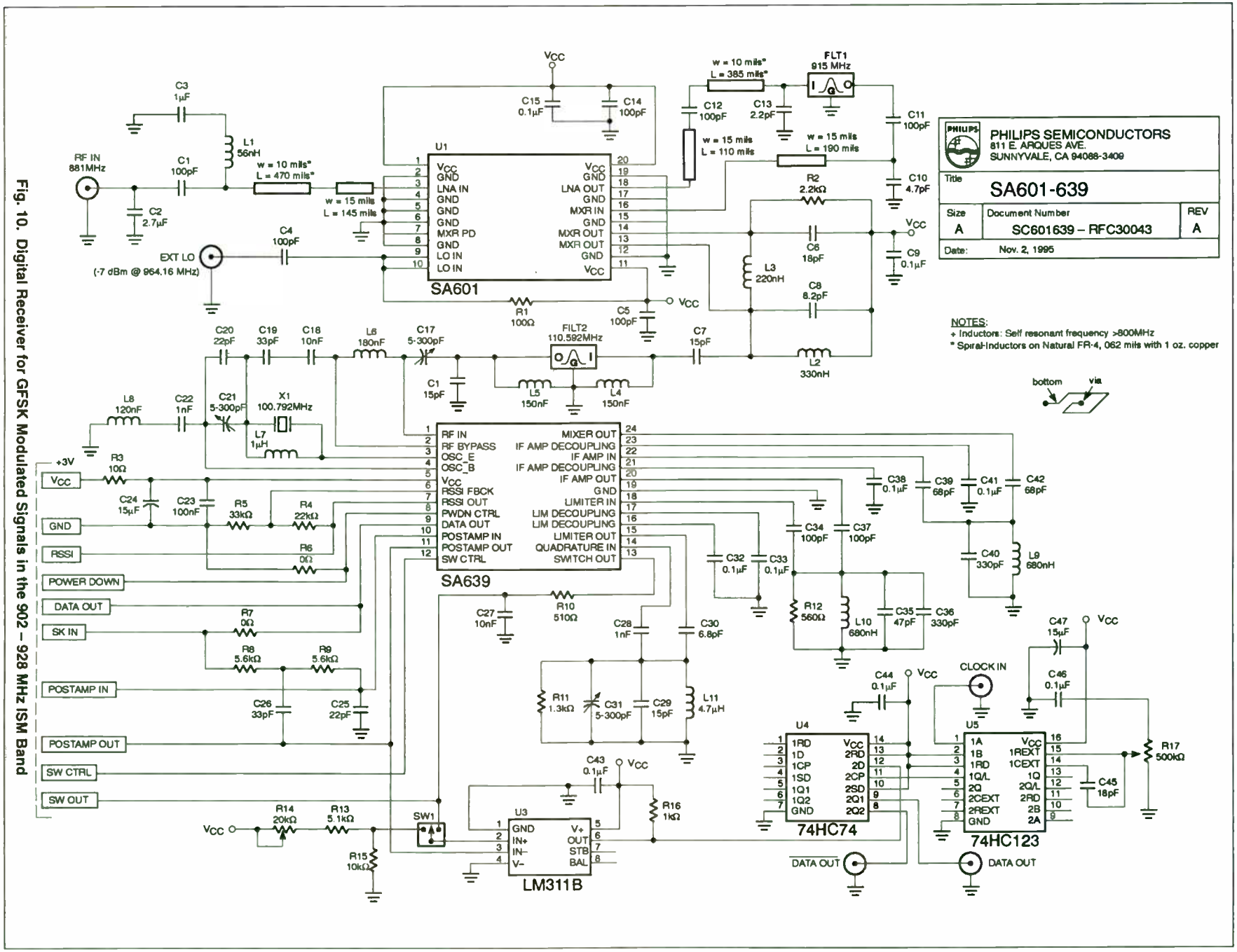


Fig. 10. Digital Receiver for GFSK Modulated Signals in the 902 – 928 MHz ISM Band

D. Board Layout (see Appendix for Board Layout and Components List)

D.1 Grounding, Coupling and Component Location Considerations

There are several important layout considerations relating to proper grounding, trace orientation and component placement on this application board. This mixed signal application incorporates both analog and digital circuit blocks and their respective grounds should be kept separate, only being brought together very near the power supply connection point. The ground connections to the integrated circuit blocks should be kept as short as possible in order to maintain non-reactive low impedance paths to the common ground point. The tuned quadrature tank circuit just prior to the phase detector is very sensitive to its location and ground connection. The 4.7 µH inductor in this circuit should be located as far as possible from the inputs and outputs of the high gain stages of the SA639, and must be connected to a large area top side ground plane with many via connections to the back side ground plane. Also, coupling between the input and output of the first gain stage of the SA639 can be reduced simply by orienting the 680 nH inductors in the parallel resonant bandpass filters perpendicular to each other.

The tuning inductors used to match the LNA input and output need to be isolated from each other because coupling of these points will cause the LNA to oscillate. These printed inductors should be placed on the backside of the application board and surrounded with the backside ground plane as much as possible. The lead trace lengths of these inductors should be oriented perpendicular to each other to further discourage coupling and be brought back to the top side of the board as close to the integrated circuit (IC) pins as possible.

The mixer resonant output matching circuitry has an appreciable recirculation current creating a magnetic field which can couple back to the mixer input. The two differential mixer output leads are brought to the backside of the board near the IC pins and brought back up again a distance away from the IC where the mixer output circuit can be safely implemented.

The first IF path, which includes the 110.592 MHz SAW filter and the matching network prior to the mixer input of the SA639, is strategically placed perpendicular to, and as far away from, the front-end circuitry as possible. This provides additional rejection of the unwanted second IF image frequency at 90.992 MHz from reaching the mixer input of the SA639. [4]

III. RECEIVER EVALUATION

A digital receiver's primary function is to reliably regenerate the original digital information transmitted to it. There are many factors and conditions that need to be considered when specifying the performance of a receiver. The best figure of merit available is the bit error rate which is simply the ratio of errored bits to the total number of bits transmitted. Unfortunately, this measurable quantity is meaningless unless the conditions under which it is measured are very clearly specified. It is often hard to compare the performance of different receivers because the conditions of the applications in which they are used are so varied. The transmission range, taking into account link losses, path losses and especially the limitations placed on transmission power and transmission antenna gain by governing authorities, will determine the sensitivity requirements of the receiver. This, along with the system requirements for the maximum acceptable number of occurrences causing the retransmission of data, will determine a maximum BER at a minimum reference power level for a given application. Other factors which have a significant affect on BER are the data rate, the Gaussian filter bandwidth, the FM deviation used to modulate the carrier, and the frequency offset of the transmitted RF carrier. [5]

There are currently no accepted high data rate protocol/performance standards for digital BTb=0.5 GFSK receivers in the 902 – 928 MHz ISM band. So, in order to evaluate the relative performance of this digital receiver, we will use published higher frequency band specifications as benchmarks.

E. DECT BER Specification Benchmark [6]

E.1 BER Specification Summary

The Digital European Cordless Telephone (DECT) specifications relating to BER are an ideal candidate for this purpose. This standard operates in the 1880 – 1990 MHz band, uses BTb = 0.5 GFSK modulation and provides a data rate of 1.152 Mbps. This standard stipulates that a) a maximum BER of 1E–5 must be observed for all power levels greater than or equal to -73dBm using an FM deviation of 288 kHz. It also requires that b) the BER be less than 1E–3 at a reference power level of -86dBm. It further stipulates that c) this BER must be maintained if the RF transmitted signal is offset from its expected carrier frequency by as much as 50 kHz.

E.2 BER Performance Evaluation

The digital receiver was evaluated under the conditions discussed above. The data rate was set to 1.152 Mbps and the carrier was frequency modulated with a Gaussian low pass filtered signal which provided 288 kHz of FM deviation. Fig. 11 shows the BER performance of the digital receiver as a function of RF input power and FM deviation. This graph indicates that all power levels greater than -85dBm maintain a BER of less than 1E–5. This satisfies DECT criteria a) by a 12 dB margin. A far more stringent requirement is DECT criteria b) discussed above. Fig. 11 indicates this digital receiver can hold a BER of 1E–3 down to RF input levels of –90 dB even with a 10% reduction in FM deviation. This satisfies DECT criteria b) mentioned above by a 4 dB margin.

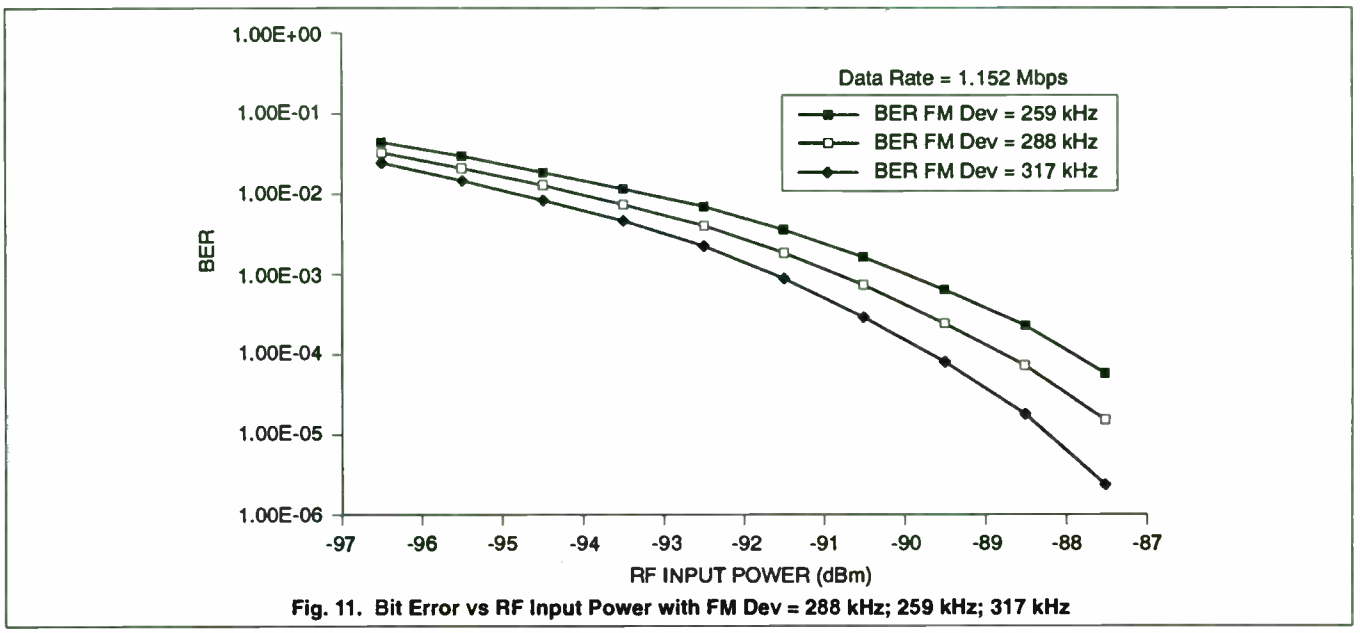


Fig. 11. Bit Error vs RF Input Power with FM Dev = 288 kHz; 259 kHz; 317 kHz

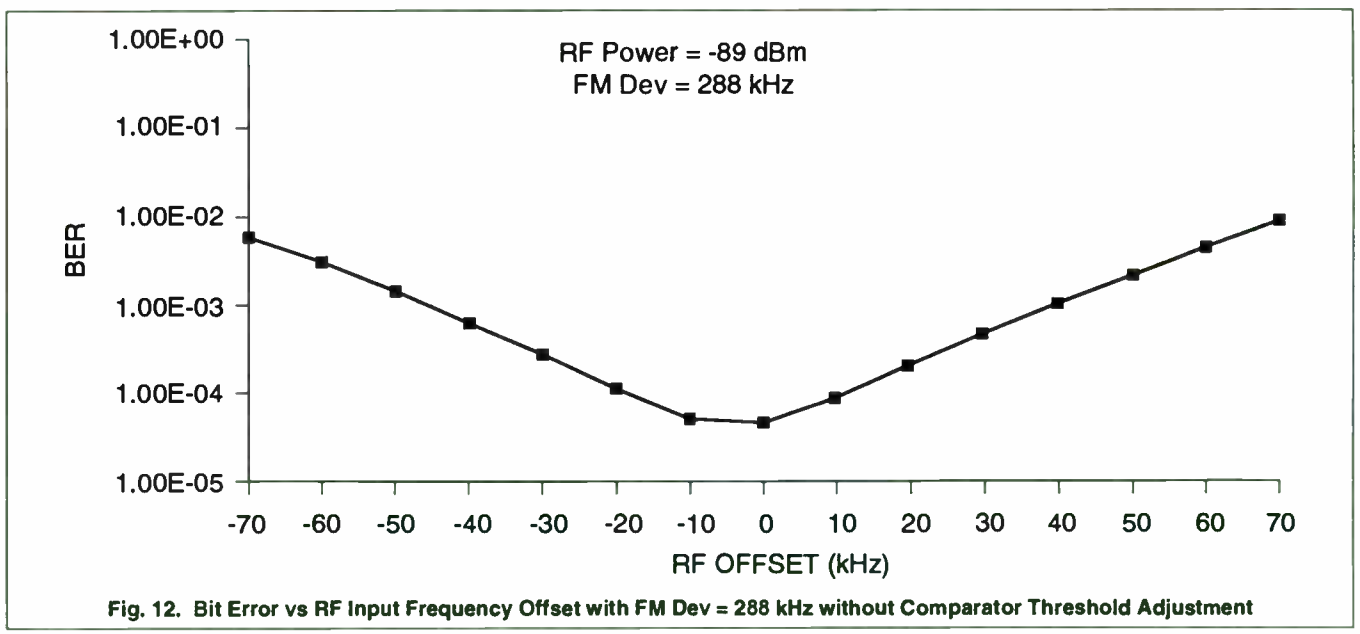


Fig. 12. Bit Error vs RF Input Frequency Offset with FM Dev = 288 kHz without Comparator Threshold Adjustment

Fig. 12 shows the BER performance of the receiver as a function of RF input frequency offset. This indicates the BER performance degradation exhibited at 288 kHz FM deviation with absolutely no comparator threshold adjustment and an RF input level of –89 dBm. An input power level 3 dB lower than the specified reference level was chosen to yield a sufficient number of errors for accurate and timely measurements on the transmission analyzer. The graph shows that under these conditions the BER performance degradation falls off very slowly and would easily meet DECT criteria c) mentioned above with comparator threshold adjustment in the preamble of the protocol and a 3 dB higher RF input level of –86 dBm as specified.

F. 802.11 Preliminary BER Specification Benchmark [7]

F.1 BER Specification Summary

The specifications of the IEEE 802.11 committee for wireless spread spectrum applications in the 2.4 GHz ISM band would also be an excellent candidate for benchmarking the performance of this digital receiver. Unfortunately the Physical Layer specifications have not yet been finalized, so the published preliminary PHY specifications will be used here. This standard uses a data rate of 1 Mbps, GFSK (BTb=0.5) modulation and an FM deviation greater than 110 kHz. It stipulates that a) a framing error rate (FER) of less than 3% must be maintained at a reference RF input level of -80dBm. It further stipulates that b) this FER must be maintained with offsets from the nominal carrier frequency of ±60 kHz.

F.2 BER Performance Evaluation

In an additive white Gaussian noise (AWGN) channel, the frame error rate FER specification can be converted to a statistically equivalent BER with the following formula $BER = 1-(1-FER)^{1/n}$, where n is the number of bits composing a frame. The 802.11 preliminary specifications define a frame as being 400 octets or 3200 bits. For the specified FER of 3%, this yields a BER of 9.5E–6 or approximately 1E–5. Fig. 13 shows the BER performance of the receiver using a 1 Mbps data rate and an FM deviation of 160 kHz. This graph indicates this receiver will hold a 1E–5 BER for RF input levels equal to or greater than –84 dBm. This satisfies criteria a) mentioned above with 4 dB margin to spare.

Fig. 14 shows the BER performance of the receiver as a function of RF input frequency offset for an FM deviation of 160 kHz and an RF input level of –83 dBm. The RF input level again was chosen to be 3 dB lower than specified. This graph indicates the BER performance degradation, exhibited at 160 kHz FM deviation and no comparator threshold adjustment, is more severe than that observed for 288 kHz. This, along with the increase in offset tolerance to ±60 kHz, requires the receiver to depend more on the data switch and the external integrator provided with the SA639 than was required for the DECT specifications. With the proper adjustment of the integrator components, however, criteria b) stated above can easily be met.

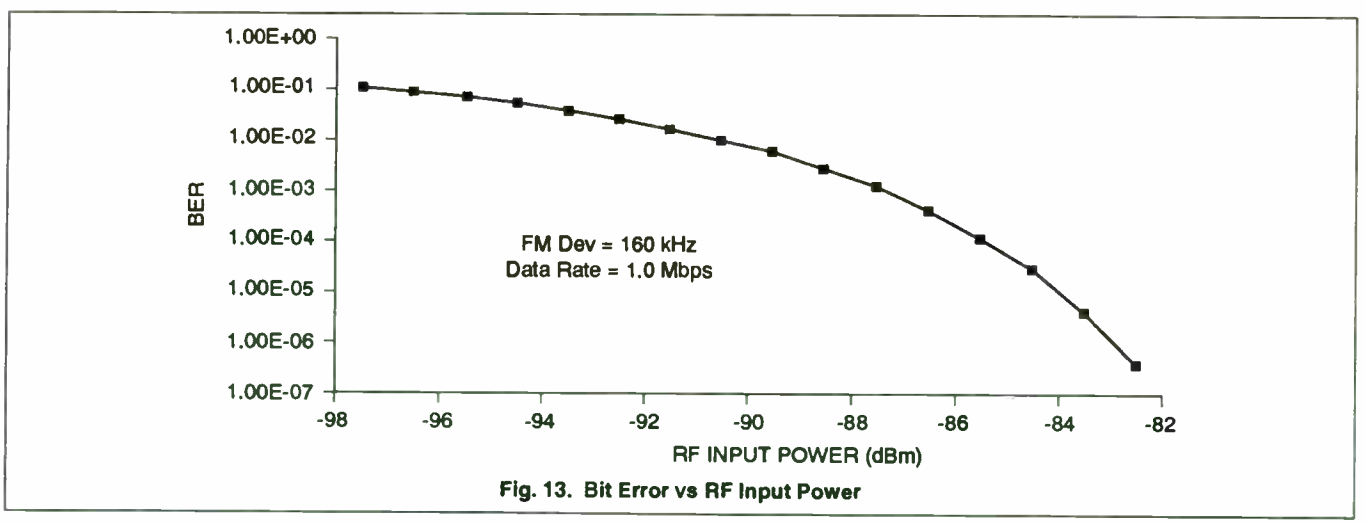


Fig. 13. Bit Error vs RF Input Power

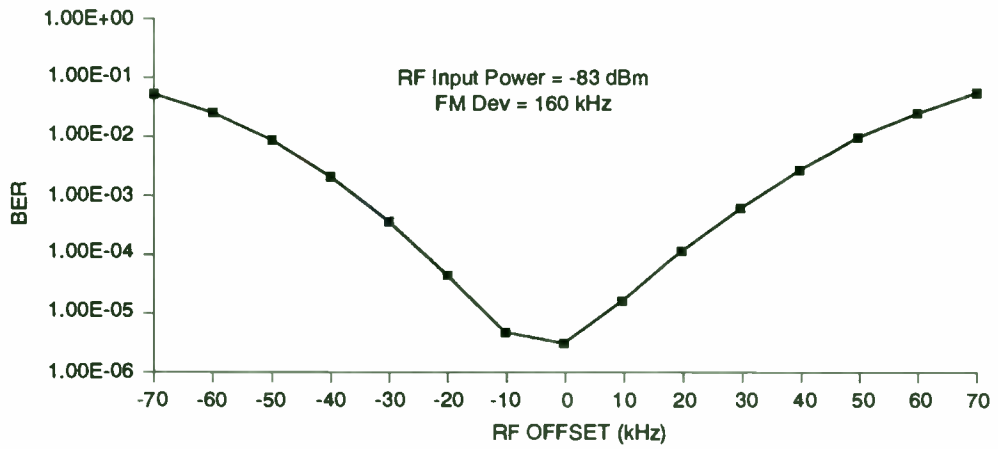


Fig. 14. Bit Error vs RF Input Frequency Offset with FM Dev = 160 kHz without Comparator Threshold Adjustment

IV. CONCLUSION

A 3 Volt digital receiver for GFSK modulated signals in the 902 – 928 MHz ISM band has been presented. A BER evaluation shows that this receiver is capable of meeting BER specifications in the 902 – 928 MHz ISM band similar to those stipulated by existing standards in higher frequency bands. The Philips SA601 3 Volt front-end performed very well in this 902 – 928 MHz application and is capable of operating at frequencies up to 1.2 GHz. The Philips SA639 3 Volt FM/IF exhibited excellent BER performance at a data rate of 1.152 Mbps and can be used for data rates in excess of 2 Mbps.

V. REFERENCES

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VI. APPENDIX

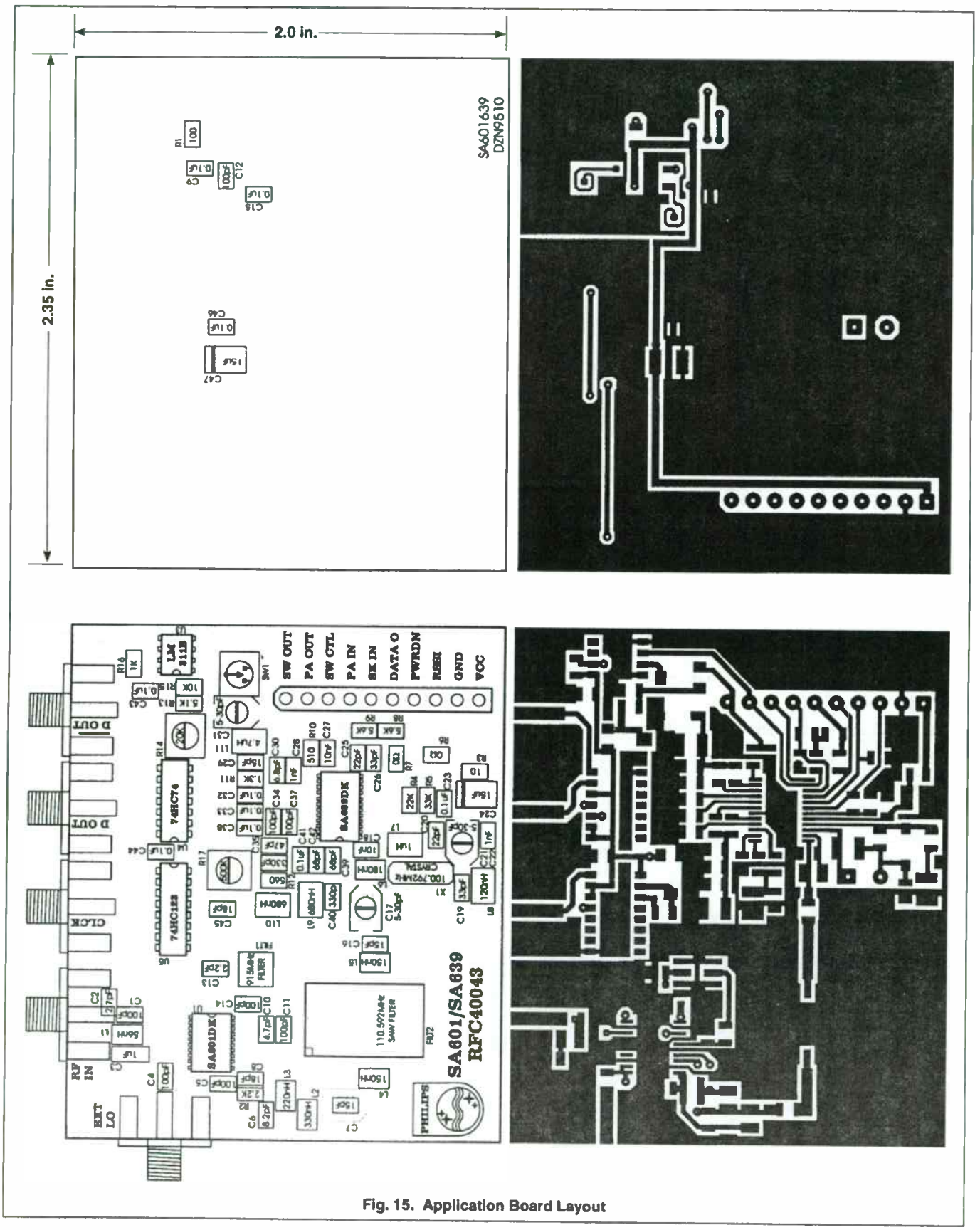

Fig. 15. Application Board Layout

Table 2. Application Component List for SA601/SA639

Application Component List for SA601/SA639					
Qty	**Part Value**	**Part Reference**	**Part Description**	**Vendor Part Number**	**Manufacturer Part Number**
***** Surface Mount CAPACITORS *****					
1	2.2pF	C13	NPO Ceramic 0805 ±.25pF	Garrett 0805CG229C9BB0	Philips Components
1	2.7pF	C2	NPO Ceramic 0805 ±.25pF	Garrett 0805CG279C9BB0	Philips Components
1	4.7pF	C10	NPO Ceramic 0805 ±.25pF	Garrett 0805CG479C9BB0	Philips Components
1	6.8pF	C30	NPO Ceramic 0805 ±.25pF	Garrett 0805CG689C9BB0	Philips Components
1	8.2pF	C6	NPO Ceramic 0805 ±5%	Garrett 0805CG829C9BB0	Philips Components
3	15pF	C7, C16, C29	NPO Ceramic 0805 ±5%	Garrett 0805CG150J9BB0	Philips Components
2	18pF	C45, C8	NPO Ceramic 0805 ±5%	Garrett 0805CG180J9BB0	Philips Components
2	22pF	C20, C25	NPO Ceramic 0805 ±5%	Garrett 0805CG240J9BB0	Philips Components
2	33pF	C19, C26	NPO Ceramic 0805 ±5%	Garrett 0805CG330J9BB0	Philips Components
1	47pF	C35	NPO Ceramic 0805 ±5%	Garrett 0805CG470J9BB0	Philips Components
2	68pF	C39, C42	NPO Ceramic 0805 ±5%	Garrett 0805CG680J9BB0	Philips Components
8	100pF	C1, C4, C5, C11, C12, C14, C34, C37	NPO Ceramic 0805 ±5%	Garrett 0805CG101J9BB0	Philips Components
2	330pF	C36, C40	NPO Ceramic 0805 ±5%	Garrett 0805CG331J9BB0	Philips Components
2	1nF	C22, C28	NPO Ceramic 0805 ±5%	Garrett 0805CG101J9BB0	Philips Components
2	10nF	C18, C27	X7R Ceramic 0805 ±10%	Garrett 08052R103K9BB0	Philips Components
10	0.1µF	C9, C15, C23, C32, C33, C38, C41, C43, C44, C46	Z5U Ceramic 0805 ±20%	Garrett 08052E104M9BB0	Philips Components
1	1µF	C3	Tant Chip Cap ±10%	Garrett 49MC105A016KOAS	Philips Components
2	15µF	C24, C47	Tant Chip Cap ±10%	Garrett TMC-M1AB156KLRH	KOA Speer Electronics
3	5-30pF	C17, C21, C31	SMT Trimmer Cap	Jaco CTZ3S-30C-B	Kyocera TC300020
***** RESISTORS *****					
2	0Ω	R6, R7	Chip Res 0805 1/10W ±5%	Garrett RM73B2A-J000	KOA Speer Electronics
1	10Ω	R3	Chip Res 0805 1/10W ±5%	Garrett RM73B2A-J100	KOA Speer Electronics
1	100Ω	R1	Chip Res 0805 1/10W ±5%	Garrett RM73B2A-J101	KOA Speer Electronics
1	510Ω	R10	Chip Res 0805 1/10W ±5%	Garrett RM73B2A-J511	KOA Speer Electronics
1	560Ω	R12	Chip Res 0805 1/10W ±5%	Garrett RM73B2A-J561	KOA Speer Electronics
1	1kΩ	R16	Chip Res 0805 1/10W ±5%	Garrett RM73B2A-J102	KOA Speer Electronics
1	2.2kΩ	R2	Chip Res 0805 1/10W ±5%	Garrett RM73B2A-J222	KOA Speer Electronics
1	5.1kΩ	R13	Chip Res 0805 1/10W ±5%	Garrett RM73B2A-J512	KOA Speer Electronics
2	5.6kΩ	R8, R9	Chip Res 0805 1/10W ±5%	Garrett RM73B2A-J562	KOA Speer Electronics
1	10kΩ	R15	Chip Res 0805 1/10W ±5%	Garrett RM73B2A-J103	KOA Speer Electronics
1	20kΩ	R14 trim pot	SM Res Trim, 1 TRN 20% J-Hook	Garrett ST-4TA-203	Philips Electronics
1	22kΩ	R4	Chip Res 0805 1/10W ±5%	Garrett RM73B2A-J223	KOA Speer Electronics
1	33kΩ	R5	Chip Res 0805 1/10W ±5%	Garrett RM73B2A-J333	KOA Speer Electronics
1	500kΩ	R17 trim pot	SM Res Trim, 1 TRN 20% J-Hook	Garrett ST-4TA504	Philips Electronics
***** INDUCTORS *****					
1	56nH	L1	Chip Inductor 1008 ±10%	Coilcraft 1008CS-560 ±10%	Coilcraft
1	120nH	L8	Chip Inductor 1008 ±10%	Coilcraft 1008CS-121 ±10%	Coilcraft
2	150nH	L4, L5	Chip Inductor 1008 ±10%	Coilcraft 1008CS-151 ±10%	Coilcraft
1	180nH	L6	Chip Inductor 1008 ±10%	Coilcraft 1008CS-181 ±10%	Coilcraft
1	220nH	L3	Chip Inductor 1008 ±10%	Coilcraft 1008CS-221 ±10%	Coilcraft
1	330nH	L2	Chip Inductor 1008 ±10%	Coilcraft 1008CS-331 ±10%	Coilcraft
2	680nH	L9, L10	Chip Inductor 1012 ±20%	Digikey TKS1023CT-ND	TOKO
1	1.0µH	L7	Chip Inductor 1012 ±10%	Digikey TKS1025CT-ND	TOKO
1	4.7µH	L11	Chip Inductor 1012 ±10%	Digikey TKS1033CT-ND	TOKO
***** FILTERS *****					
1	915MHz	FILT1	915MHz SAW Bandpass Filter	Siemens B4637-915MHz	Siemens
1	110.592MHz	FILT1	110.592MHz SAW Bandpass Filter	Siemens B4535-110.592MHz	Siemens
***** IC *****					
1	SA601	U1	Low voltage LNA & mixer	Philips SA601DK	Philips Semiconductors
1	SA639	U2	Low voltage FM IF system	Philips SA639DK	Philips Semiconductors
1	LM311B	U3	Voltage comparator	Philips LM311BD	Philips Semiconductors
1	74HC74	U4	D Flip-flop	Philips 74HC74D	Philips Semiconductors
1	74HC123	U5	Monostable multivibrator	Philips 74HC123D	Philips Semiconductors
***** IC *****					
1	100.792MHz	X1	100.792MHz Crystal	Reeves & Hoffman 100.792MHz	Reeves & Hoffman
1	SPDT Switch	SW1	SMT 4mm SPDT Selector Switch	Garrett CS-4-12YA	Philips CS-4-12YA
5			SMA Gold Connector	Digikey J502-ND	EF Johnson 142-0701-801
1			10 Pins Gold Test Point	Digikey	3M 929647-01-36-ND
1			Printed Circuit Board	RF#30043	EXCEL 601/639 #30043

Fast-Hopping Fractional-N Phase-Locked Loop Frequency Synthesizer

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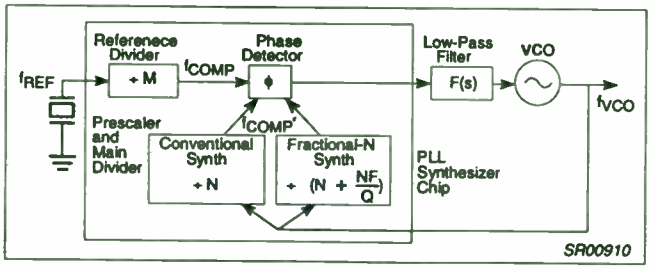
Abstract

Modern frequency-hopping systems require fast hopping phase-locked loop (PLL) frequency synthesizers for channel switching. In general, the switching time of a PLL is determined by the loop lowpass filter bandwidth according to linear control theory. However, since the phase/frequency error information between the reference and synthesizer signals is represented in digital pulse format (comparison pulses), a minimum number of pulses have to be generated before a PLL goes in-lock, no matter how wide the lowpass filter bandwidth is. This paper will take an experimental approach to find out what the fastest switching time a PLL can reach with a given number of comparison pulses. We will also show that a fractional-N PLL with higher comparison frequency can switch faster than a conventional PLL.

Background

Low cost and good performance makes PLL an indispensable device in multiple channel communication systems. In essence, a PLL synchronizes the frequency and phase of the output signal from a VCO with a stable reference signal. Figure 1 shows the most popular single loop conventional and fractional-N PLL to be used as frequency synthesizers. The VCO output signal is a multiple of the comparison frequency, which is the same as the channel spacing for a conventional PLL. The comparison frequency can be higher than the channel spacing for a fractional-N PLL.



Conventional syn.	Fractional-N syn. using mod 8
$f_{vco}=f_{comp}(N)$	$f_{vco}=f_{comp}(N+NF/8)$
900= 0.03(30000)	900 = 0.24(3750 + 0/8)
900.03 = 0.03(30001)	900.03 = 0.24(3750 + 1/8)
900.06 = 0.03(30002)	900.06 = 0.24(3750 + 2/8)

All frequencies are expressed in MHz

Figure 1 PLL frequency synthesizer.

Phase detectors can be implemented in different ways and a common one is shown in Figure 2. This type of phase detector is also known as frequency/phase detector because it detects frequency as well as phase. Because of this nature, a PLL using this type of detector does not have lock-in range and capture range, thus making it lock at any frequency step size.

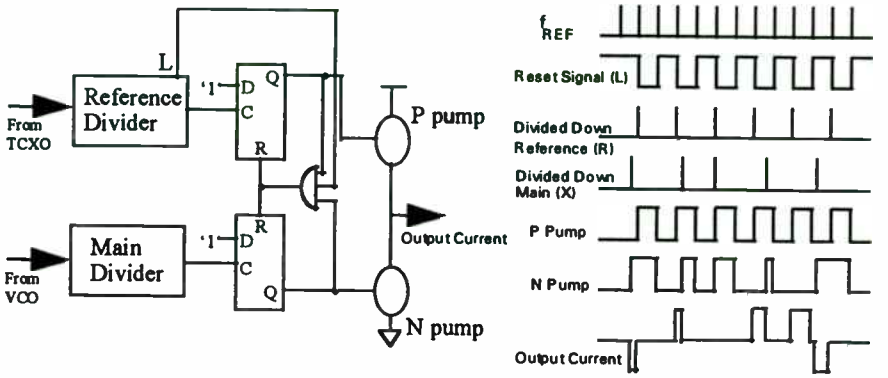


Figure 2 Digital phase/frequency detector of the SA7025.

The switching time of this type of PLL is mainly determined by two factors: comparison pulses/cycles and the loop filter bandwidth. The former one is a statistical phenomenon while the latter one follows the control theory. In order to design a PLL frequency synthesizer to have specific switching time, it is important to find out the effect of these two factors in the design equation.

Design Equations

The following design equations are used to calculate the loop filter values which corresponds to a given switching time for a second order PLL (see reference 1). The lowpass filter is displayed in Figure 3.

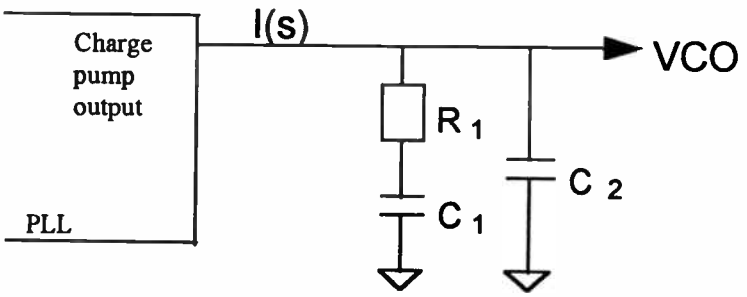


Figure 3 Passive loop lowpass filter

$$\omega_N = \frac{-\ln [\delta * (1-\xi^2)^{0.5}]}{\xi * t_{sw}} \qquad (1)$$

$$C_1 = \frac{K_\phi * K_{VCO}}{N \omega_N^2} \qquad (2)$$

$$R_1 = 2 * \xi \left(\frac{N}{K_\phi * K_{VCO} * C_1} \right)^{0.5} \quad (3)$$

$$C_2 <= C_1/10 \quad (4)$$

δ : final frequency resolution after settling.

$$\delta = \frac{\text{frequency error after settling}}{\text{switching step}} \quad (5)$$

t_{SW} : switching time (sec)
f_N : natural frequency of the 2nd order system(Hz) , $\omega_N = 2\pi f_N$ (rad/s)
N : total divide ratio
ξ : damping factor of the second order system. Typical value is 0.707.
K_{VCO}: VCO gain (Hz/V) or 2π * VCO gain (rad/V)
K_ϕ : phase detector gain = $I_{CP}/2\pi$ (A/rad)

Experiments and Results

Before attempting to find the minimum comparison cycles that are needed for the PLL to lock, we first verify the validity of the above equations. The PLL used in this section is the SA7025 1GHz fractional frequency synthesizer. It allows designers to use a comparison frequency which is five times or eight times higher than the channel spacing. The following are the design parameters used in this section:
t_{SW} = 2ms, step = 25MHz to within 1kHz, f_{ch} = 10kHz, f_{comp} = 80kHz, VCO gain = 12MHz/V
I_{CP} = 1mA, VCO range = 913 to 938MHz.

By using Design Equations 1 to 5, C1=18.5nF(used 18nF+3.3nF), C2=1.8nF(used 1nF+820pF), and R1=10.3kΩ(used 10kΩ). Figures 4 and 5 show the switching time measurement results using the Modulation Domain Analyzer. The lockup window is +/- 1kHz and the time marker is set at 2ms. Results show that the design equations are very accurate. Equal switching time from high to low band and from low to high band means that the PLL has an accurate charge pump which delivers equal amounts of current at different tuning voltages.

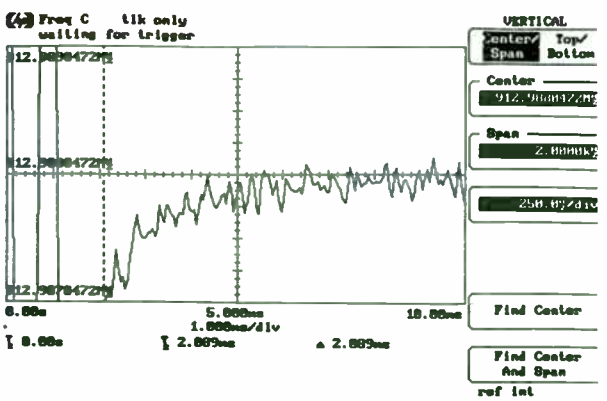


Figure 4 From high to low, t_{SW}=2ms

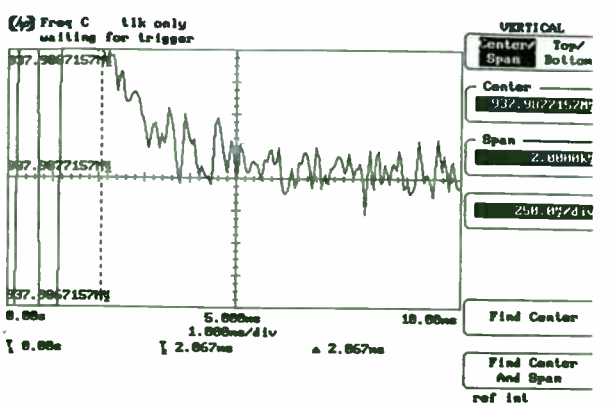


Figure 5 From low to high, t_{SW}=2ms

The next experiment repeats the previous one, except that t_{sw}=1ms instead of 2ms is used in design. The component values then become C1=4.7nF, C2=470pF, and R1=20.4kΩ(used 20kΩ). The switching time measurement results are shown in Figures 6 and 7. From this, we can conclude that the wider the loop bandwidth of the loop filter, the faster the switching time. The design equations still predict the switching time very well.

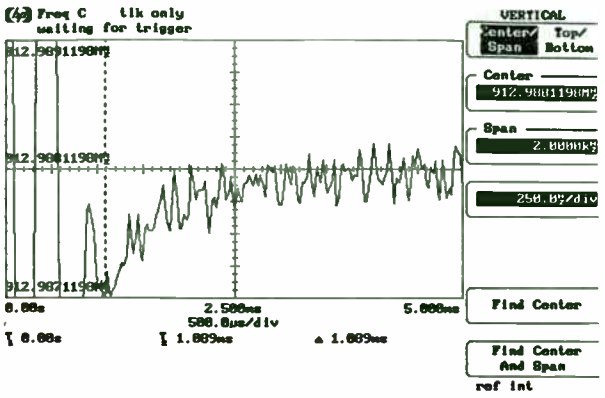


Figure 6 From high to low, t_{sw}=1ms

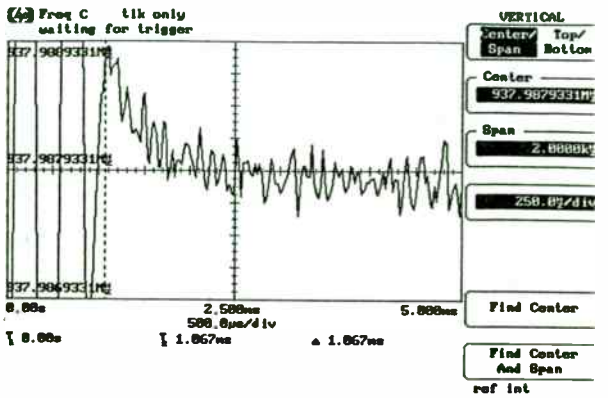


Figure 7 From low to high, t_{sw}=1ms

Next, we try to find out what is the fastest switching time for this PLL. A switching time of 100μs was chosen and the same design equations were used to find the loop components. The values are C1=47pF, C2=4.7pF, and R1=203.8kΩ(used 200kΩ). Figures 8 and 9 show that even though 100μs was intended, only 500μs was achieved. This is the point where the linear control theory breaks down and the random behavior of a PLL comes in. The number of comparison cycles can be calculated by:

Number of comparison cycles = switching time x comparison frequency (6)

Therefore, we have 500μs x 80kHz = 40 cycles.

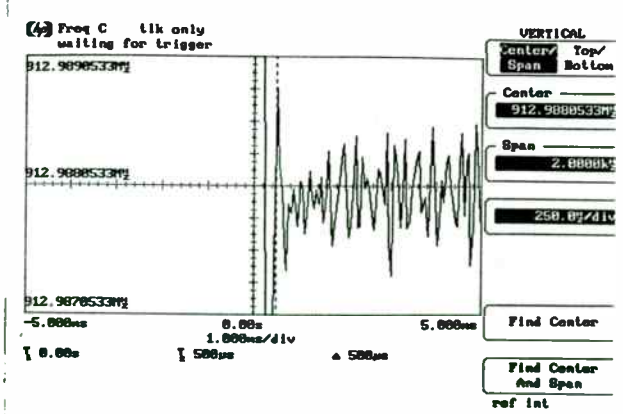


Figure 8 From high to low, t_{sw}=500μs

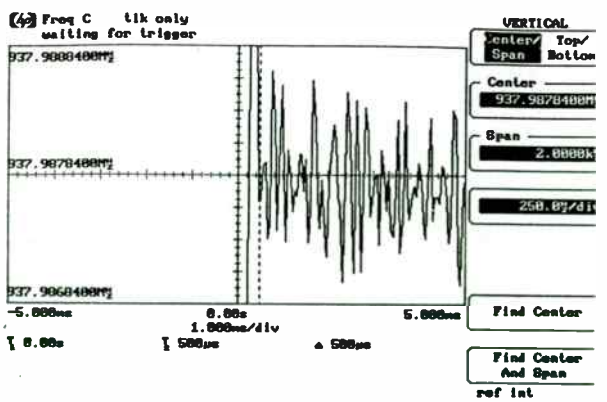


Figure 9 From low to high, t_{sw}=500μs

Designed to have t_{sw}=100μs

To verify that forty cycles is an accurate value, an experiment using a conventional frequency synthesizer (UMA1017) with a 10kHz comparison frequency was performed. Using the same design equations with I_{CP}=3.6mA and t_{SW}=3ms, the component values become C1=19nF(used 15nF+3.9nF), C2=1.2nF, and R1=15kΩ. The measurement results are shown in Figures 10 and 11. A switching time of 4ms was achieved when a 3ms loop was designed. This shows that this PLL has also reached its limit and the number of comparison cycles is the same as the previous experiment (4ms x 10kHz = 40 cycles). Compared to the fractional-N synthesizer, the switching time is exactly 8 times longer.

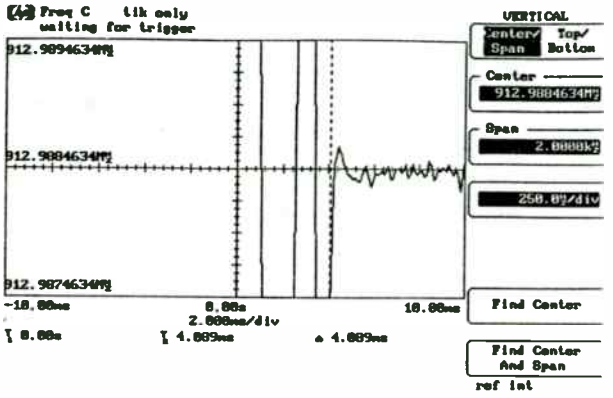


Figure 10 From high to low, t_{SW}=4ms

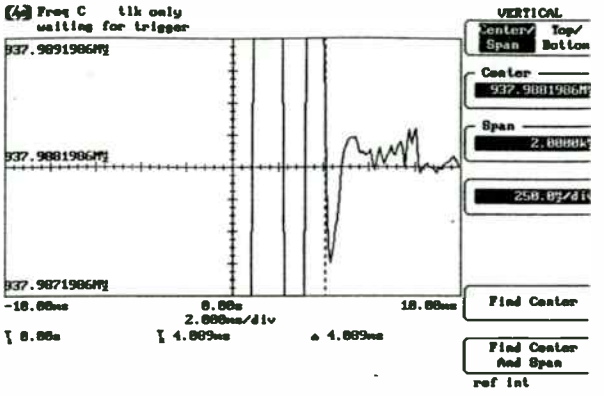


Figure 11 From low to high, t_{SW}=4ms
Designed to have t_{SW}=3ms

Conclusions

This paper has shown that there exists a minimum number of comparison cycles needed for a PLL frequency synthesizer to lock up. Because of this, a fractional-N PLL synthesizer (5 times or 8 times more comparison cycles) clearly has advantage over a conventional one in a frequency-hopping system application. Results show that a fractional-N synthesizer using 8 times higher comparison frequency switch 8 times faster than a conventional synthesizer when the switching time is dominated by the number of comparison cycles. For a 25MHz jump to within 1kHz, the number is 40. If the jump is smaller, the cycles needed will be less. Designers can use this number as a rule of thumb to figure out how fast a frequency synthesizer can switch when designing a loop filter.

References

[1] Best, Roland E., Phase-Locked Loops Theory, Design, and Applications, 2nd edition, McGraw-Hill, Inc., 1993.

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[3] Hugues, Pascal, " AN95102: UMA1018 and UMA1020M/UMA1020AM Low power dual frequency synthesizers, UMA1017 and UMA1019/UMA1019AM Low power single frequency synthesizers," Philips Semiconductors, Caen, France, Oct. 1995.

Acknowledgments

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BROADBAND RF SOLUTIONS FOR CORDLESS PHONES

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ABSTRACT

There are several cordless phone standards, to name a few; CT0, CT1, CT2, CT3 and DECT. This paper discusses the need for second generation digital cordless phones and discusses the CT2 system requirements. Lastly, a RF solution from TEMIC Telefunken that meets ETSI, CT2 specifications, Wireless PBX and cordless phones in the 902 - 928 Mhz band is discussed.

1. INTRODUCTION

A cordless telephone of today implements a radio link between the handset and base station, thereby relacing the cord to the handset. A single handset communicates with one base station and the switch is merely a make or break connection between the subscriber line and the base station. First generation phones were channelized and had access to a single or a few channels. The latter being a feature of high end phones, wherein a user on the basis of perceived communication quality would select the best channel. The user cannot do anything to avoid intereference if the same channel is in use by another user nearby. The method of transmission is analog FM and the handsets transmit power is limited to 10 mW.

To overcome the problems of the first generation systems, namely co-channel interference and security of voice channels against eavesdropping work was initiated on second generation cordless phones that would become elements of a wide network. A compatibility specification was necessary to allow the handset to communicate with more than one base station. The owner of such a handset would have to subscribe to a telepoint service. Finally, it was also very critical to keep the overall hardware robust, simple and low cost.

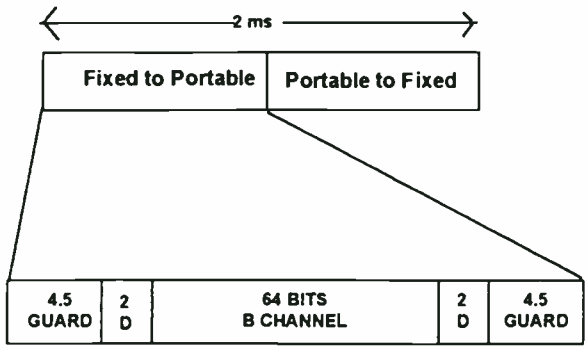
While there are several cordless standards, this paper focuses on the CT2 standard.

2. CT2

Cordless phones, CT0 and CT1 are designed to communicate with a single base station and as a result no compatibility specification was required. A common air interface (CAI) standard in CT2 allows users to interface with different base stations while maintaining complete transparency. Dynamic channel selection allows for the best channel to be selected while the speech coder which is CCITT, ADPCM at 32 kb/s allows for digital transmission and thereby encryption techniques for privacy. The band allocated for the service extends from 864 MHz to 868 MHz. Do note that the band varies in the 839 - 952 MHz for different parts of the world. Total number of carriers being 40; channel 1 carrier is assigned to 864.15 Mhz and channel 40 at 868.05 Mhz. A tolerance of ± 10 kHz is allowed for both portable and fixed elements. Carrier separation is 100 kHz to support single channel per carrier, time division duplex.

Figure 1, shows a CT2 time slot and frame. The frame duration is of 2 ms. The handset or cordless portable part (CPP) transmits to the base station or cordless fixed part (CFP) for 1 ms and the base to the handset the other 1 ms. Each time slot has 64 bits of user information and 4 bits for system control information, D channel. Two guard bands of 8 bits are added. Hence, a 2 ms frame has a total of 144 bits providing an effective rate of 72 kb/s.

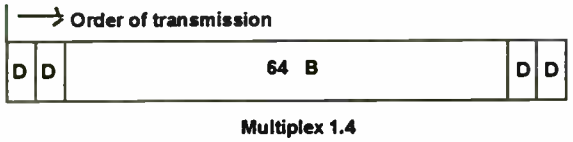
Figure 1. CT2 Time Slot and Frame.



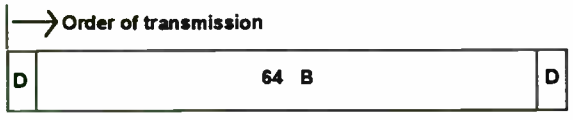
Modulation scheme is binary frequency shift keying, the peak duration lying ± 14.4 kHz and ± 25.2 kHz, with logic 1 taking the higher of the two frequencies. A Guassian filter shapes the modulations and as the bit rate is 72 kb/s and bit transitions are phase continous the result is GFSK.

Signalling of either 1 kb/s or 2 kb/s is achieved by permitting two types of multiplex in the traffic channel, MUX 1.2 operates at 66 bits packets and MUX 1.4 has 68 bits. These packets repeat every 144 bits. Allowance is made for 1 bit of propogation delay.

Figure 2. Multiplex 1



Multiplex 1.4

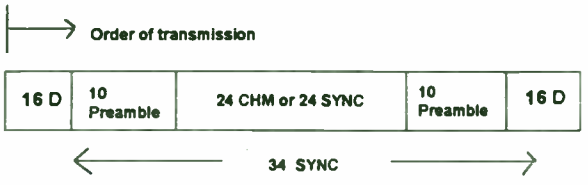


Multiplex 1.2

Layer 1 signalling in CT2 is responsible for channel selection and link initiation. As a result each TDD frame is divided among 3 channels, D channel for signalling, B channel for voice and data traffic and SYN channel for burst synchronization.

MUX 1.2 or MUX 1.4 exchanges traffic between handset and base station once a link has been established. However, while the establishment of link is in process, and both the handset and base station are trying to achieve synchronization, a different pattern of bits is required in MUX 2 which contains no B channel component. The frame is committed entirely to synchronization and channel marker data.

Figure 3. Multiplex 2



A third multipex, MUX 3 is needed so that the base station receiver can detect the call request from the handset. When the base station transmitters are silent during the 1 msec or so per 144 bits, the handset repeats a series of 5 complete 144 bits frames followed by 2 frame intervals during which the handset listens for a response from the base station.

Channel scanning and assessment of channel status can be done by continuously monitoring a channel for 2 secs. or by intermittent scanning, pausing on a channel and sampling it in 200 msecs. intervals for a minimum of 5 samples.

CT2 systems must conform to line system standards that permit a round trip delay of 5 msecs. in the speech part. The TDD scheme introduces a 1 msec. delay, while the ADPCM codec keeps speech processing within 4 msecs.

CT2 allows for low cost hardware, an estimated cell radius of 63m, using a frequency reuse pattern every 200m, it allows for 10,000 users every square mile. By deploying smaller cells in buildings and externally one can increase the total number of users.

3. CT2 RF REQUIREMENTS

Receiver:

Sensitivity	- 100 dBm
Receiver Noise Figure	< 8 dB
Receiver IIP3	- 20 dBm
Compression Point	- 13 dBm
Spurious Emissions	- 36 dBm
RSSI Dynamic Range	75 dB
RSSI Minimum Level	- 105 dBm
Signal to Noise Ratio	15 dB

Transmitter:

Output Power	14 dBm
Low Mode Output Power	- 2 dBm
Harmonics Spurious Emission	- 40 dBc
Adjacent Channel Power	- 20 dBm

4. CT2 CHIP SET

TEMIC has introduced a new CT2 chip set, comprising of four ICs. A GaAs front end U7001B shown in Figure 4, which integrates a power amplifier (50mW), antenna switch and low noise

Figure 4. U7001BG (CT2 Front End IC)

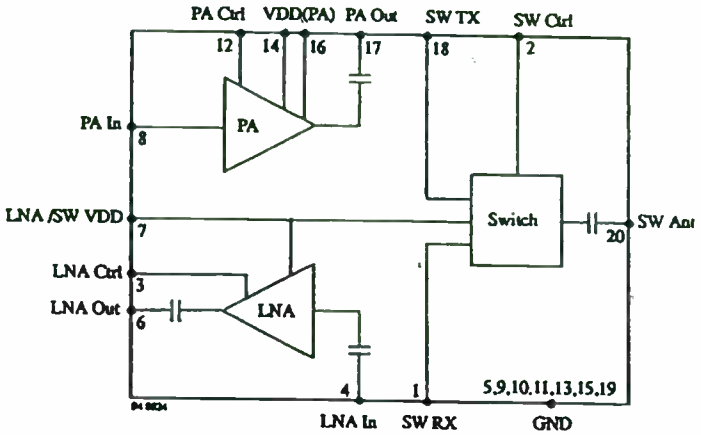


Figure 5. U2783B-FS (1250-MHz/400-MHz Twin PLL)

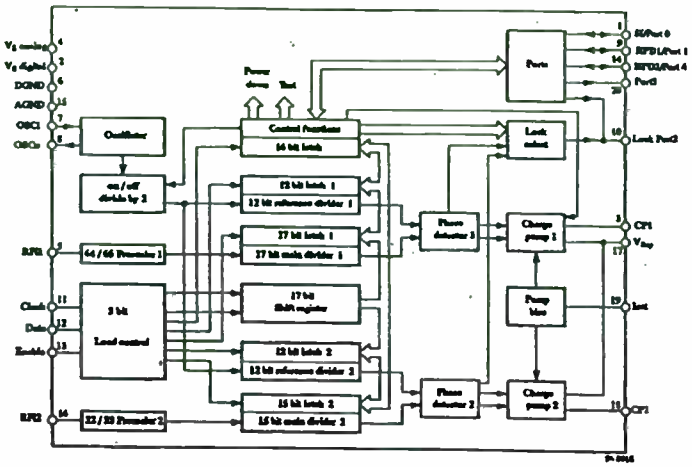


Figure 6. U2760B (CT2-RX/TX IC)

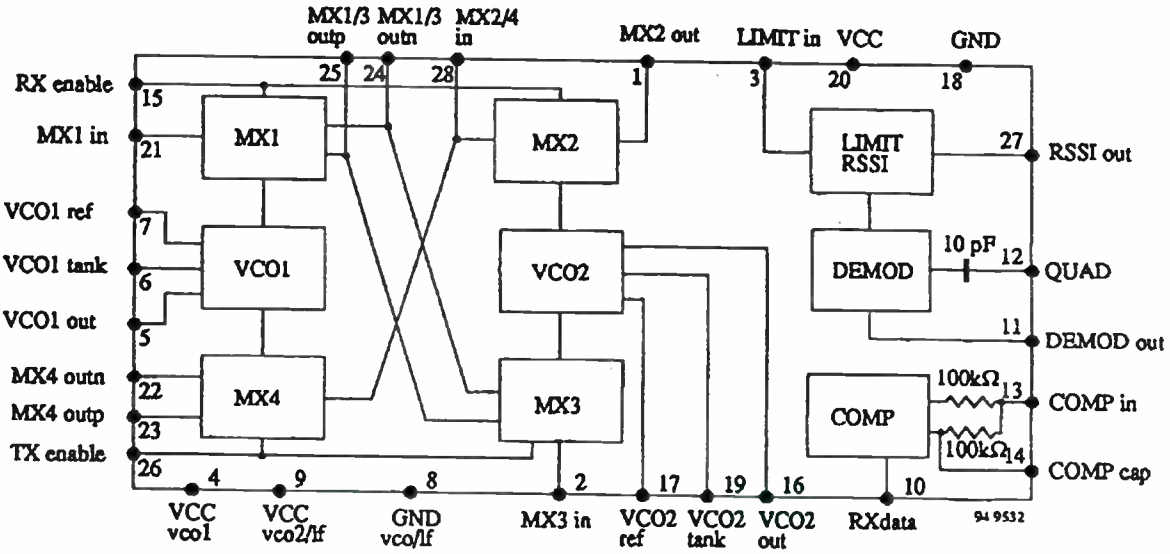


Figure 7. U3770M (CT2 I/Q Modulator and Clock Circuitry)

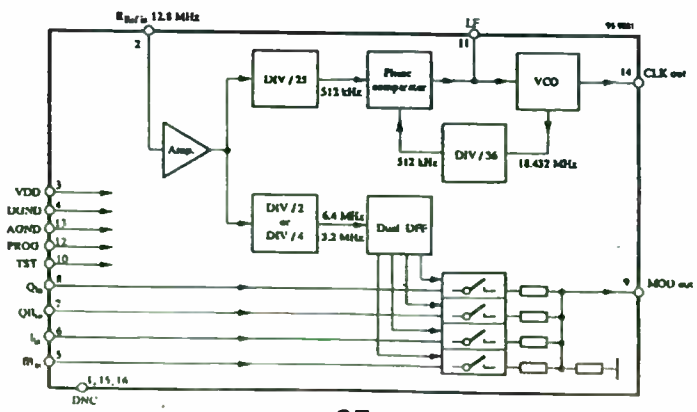
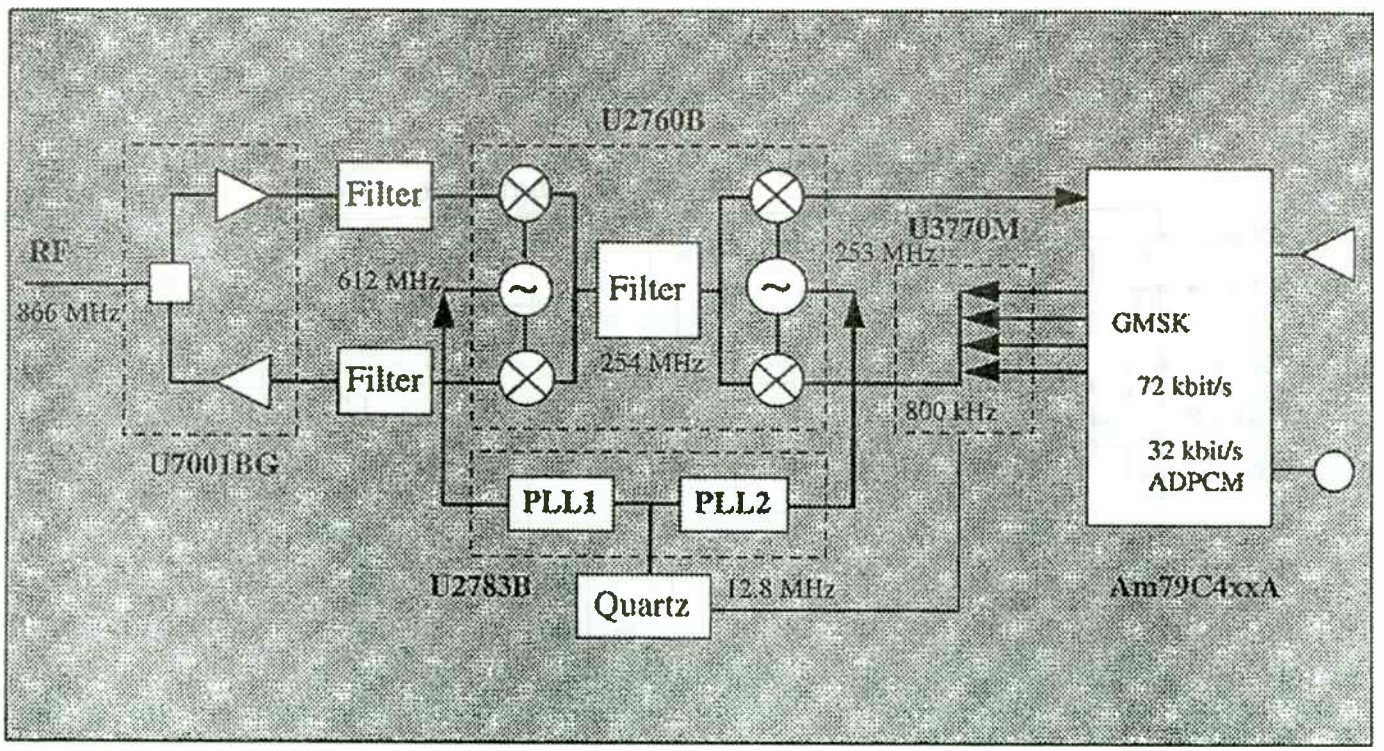


Figure 8. CT2 Radio Block Diagram



amplifier. The power amplifier has an efficiency of 45 percent and in the transmit mode draws 39 mA; while in the receive mode draws 4 mA. It is specially designed to operate from 839 - 952 Mhz. The U2783B is a double PLL, shown in Figure 5, silicon bipolar chip operating at frequencies upto 1250 Mhz and 400 Mhz from 2.7 to 5.5 V with a phase noise floor of - 72 dBc/Hz. U2760B, shown in Figure 6 is the Rx / Tx chip that includes the mixers, VCOs, demodulator and RSSI circuits. Power consuption is 23 mA.

The final TEMIC chip shown in Figure 7 is the U3770M, I/Q Modulator, a CMOS IC that also generates the system clock frequency. These chips interface with AMD's Am79C4xxA, CT2 PhoXTM Controller which implements the baseband and control functions of audio processing, protocol control, data formatting and peripheral functions. A complete working demonstartion board and kit is available from WAVECOM®, France.

The complete CT2 radio block diagram shown in Figure 8 has been successfully been implemented in CT2 phones worldwide, Cordless phones in the 902 - 928 MHz band in N. America and Wireless PBX systems.

5. CONCLUSION

The committment made by different standards authorities and manufacturers worldwide, and allocation of frequencies shows significant promise for this standard. The simplicity and mobility allowed to a user makes it increasingly a consumer product; an extension of our home cordless phone.

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VCO'S FOR WIRELESS APPLICATION

By: Ulrich L. Rohde and Shankar Joshi
Synergy Microwave Corporation

Modern wireless systems require frequency sources which need to combine low power consumption, small size, and good performance. Good performance is defined as sufficient output power, good phase noise, and low pulling. To complicate matters, the trend towards low voltages reduced flexibility in the design to add stabilization circuits.

To accommodate some of these conflicting requirements, Synergy has developed a series of VCO's in the range of 800-1000MHz, 1700-1900MHz, and 2200-2500MHz which meet those criteria. This is accomplished by a combination of novel design techniques which will be explained in this paper. Some of these items are RF/DC feedback, printed conductors, and special electronic tuning circuits.

These types of improvements to the VCO circuits have vastly eliminated microphonic effects and improved the phase nice by at least 15db. Further using IC types of oscillators rather than single transistors, temperature compensation for bias and more uniform output power is achievable.

The paper will show a combination of measurements, design rules, and CAD predictions/optimization.

Dual-Mode Cellular/Satellite Hand-Held Phone Technology

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Ericsson is currently developing dual-mode GSM/Satellite and AMPS/Satellite hand-held phones for the Asian Cellular Satellite (ACeS) System. Using state-of-the-art techniques in circuit integration at RF and baseband (RF and digital ASICs) in conjunction with a judiciously chosen Common Air Interface (CAI) waveform, which allows for significant circuit synergies between cellular and satellite modes, these pocket phones are envisaged to compete favorably in size, weight, and battery life with the best cellular-only products of their era (1998).

The ACeS MSS System will deploy and advanced geostationary satellite which is currently being developed by Lockheed-Martin Corporation. The satellite will span Asia in its footprint, using a significant number of spot beams, and will offer service from India to Japan and from Northern China to Indonesia. The link margin provided by the satellite to the hand-held units will be approximately 10 dB (over and above an AWGN channel subject to a hand-held G/T of -26 dB/K (forward link) at a hand-held average EIRP of -4 dBW (return link). The frequency of operation of the mobile links will be at L-band.

The design challenges for the dual-mode cellular/satellite hand-held phones lie primarily in the RF section. With the phone's average radiated power constrained not to exceed the GSM limit of 250 mW (2 W peak given the choice of an eight-slot TDMA return-link frame format), the antenna design on the hand-held unit must provide 2 dBi gain to meet the average EIRP requirement of -4 dBW. At the same time, the antenna design must be esthetically acceptable, mass producible, and capable of addressing the cellular mode requirements as well (multiple antennas on the phone do not represent an attractive alternative). The receiver front-end must be low-cost, small in size, and provide a low enough noise figure which when combined with the stated antenna gain and expected antenna noise temperature, will yield an overall receiver sensitivity satisfying the requirement of G/T = -26 dB/K.

Fraunhofer Institut
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Radio Transceiver For Field Bus Applications

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Abstract

This article will describe a radio transceiver system developed for digital data transmission using FSK at speeds up to 100kBit/second.
It operates in the European 433 MHz ISM band but may easiliy be modified to operate in different frequency bands.
The transceiver uses cost-effective commercial SAW technology for the oscillator frequency determining elements and filtering in the receiver, resulting in very good performance at low cost.
A microcontroller performs channel coding and appropriate error protection of the transmitted data, giving the user a transparent serial data link.
Originally developed for LON applications, this transceiver may also be included into other field bus systems for home or factory automation.
The article will describe the transceiver architecture and will highlight the specific design problems coming with the relatively high temperature drift of most SAW resonators and the consequences for receiver and transmitter design.
The problem of designing a SAW oscillator suitable for frequency modulation and offering the required frequency deviation while maintaining sufficient linearity and temperature stability will also be investigated.
Measurement results of the transceiver's performance will be included.

MOBILE COMMUNICATIONS

Mobile Communications

Session Chairperson: Paul Khanna,
Hewlett-Packard Co., Communications Components Division
(Santa Clara, CA)

The Location and Monitoring Service as An Alternative to Global Positioning Systems. **Wayne Stargardt,** Pinpoint Communications, Inc. (Dallas, TX) **34**

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The Location and Monitoring Service as an Alternative to Global Positioning System

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1. ABSTRACT

Global positioning systems seem to be coming of age. All of the GPS satellites -- a $13 billion positioning and navigation system sponsored by the U.S. Department of Defense -- have been deployed. Ground-based GPS receivers have been reduced to PC cards, and connect to any portable computer. And now, the technology is cheaper than ever. The receiver-antenna costs less than $500, and signals from the GPS satellites are free. Yes, it appears GPS is coming of age.

Despite its usefulness and the high enthusiasm being shown to apply the technology to any problem requiring location information, GPS is not always the most appropriate solution available. In particular, when applied to problems exhibiting the need for tracking over navigating, especially in urban environments (collectively referred to as automatic vehicle location or AVL applications), GPS is plagued by deficiencies that aren't easily overcome. GPS, a one-way/receive-only technology, provides no way to transmit collected data to another location. The technology is able to determine location and speed only and has no messaging capabilities. GPS, like most satellite systems, require a line-of-site link to the vehicle being located. And finally, GPS is inherently inaccurate in non-military applications; for security purposes, all GPS receivers are subject to data degradation.

While GPS technology does have its limited place, there is an alternative for applications requiring one efficient technology for both accurate automated vehicle location and two-way data transmissions -- the Location and Monitoring Service (LMS). LMS can provide reliable data communications and precise location information simultaneously to an external application or individual.

Location and Monitoring Service, a new class of mobile data communications and AVL service recently defined by the Federal Communications Commission (FCC), provide both services across a single communications link. LMS is not associated with satellite-based systems and, unlike GPS, requires no secondary communications system, such as cellular telephone, for data transmissions of location information.

This paper will explain the technology behind a typical network designed for Location and Monitoring Service and explain its capabilities for

AVL and data communications. It will discuss recent FCC action in allocating spectrum permanently for Location and Monitoring Services that affect some AVL methods. In addition, the paper will discuss the practical applications for LMS.

Keywords: Protocol, Radio-location, data-messaging, spread-spectrum, RF-interference, air-time, mobile-resource-management, shared-band, multilateration, multipath distortion.

2. INTRODUCTION

The design and operation of viable radio-location and messaging systems require both a balance between, and optimization of, many often conflicting requirements. To begin such a design and optimization task it is necessary to come to grips with the many variables involved, technical, economic, and regulatory. Some of the more important include target market identification, service offering, service costs, service pricing in the market, new market adoption rates, message traffic rates, hardware design, link budgets, interference analysis, band sharing, FCC regulation, mobile unit costs, infrastructure cost, etc.

2.1 Mobile Resource Management (MRM)

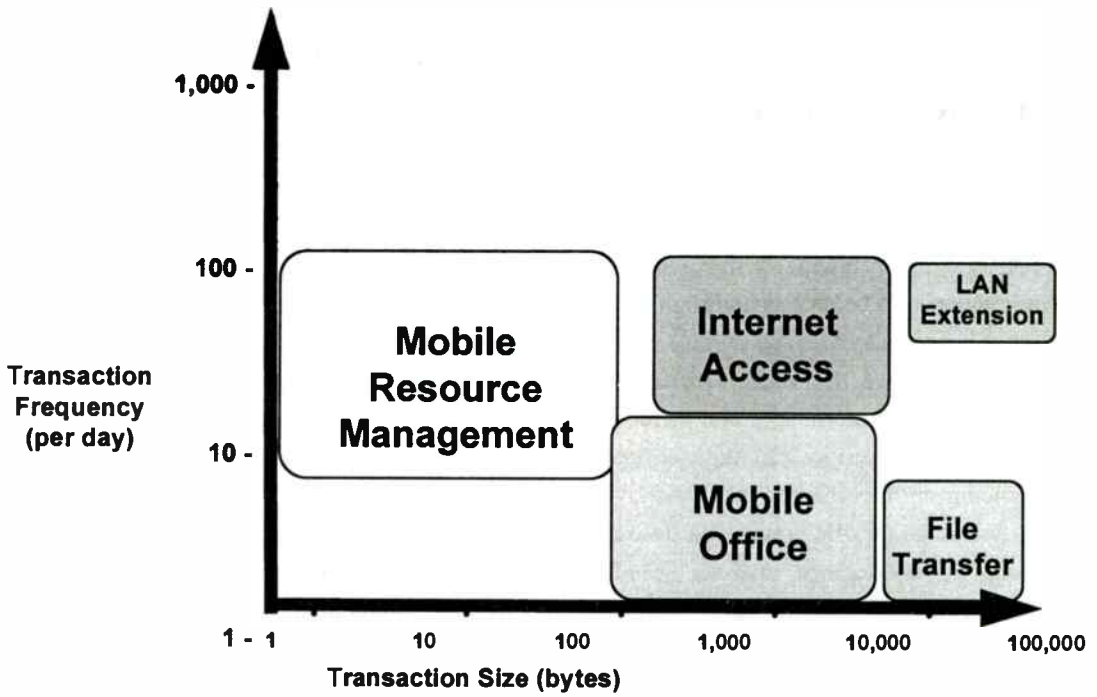
In a wide range of mobile resource management applications, data communication has many advantages — primarily reliability, speed and efficiency compared to voice based communication, or no real time communication at all, that have been traditionally employed. Computers can communicate directly with other computers, so there is less chance of operator error arising. Computers can handle many routine tasks without human intervention and can buffer interactions allowing the human operators to get on with what they can uniquely do until such time as they can attend to the messages intended for them. Most importantly, data communication is exponentially faster than any manual (or verbal) methods, and therein lies the possibility of tremendous operating cost economies.

A very important aspect of mobile data communication is the management of the company resources that are on the road, be they technicians providing service at the customer site, auto parts speeding on their way to an assembly plant, salespeople collecting information on customer needs, or beer being delivered to your favorite pub. There are increasingly more employees and corporate inventory on the road every day; a result of better planning and logistics abilities, and the desire to provide better service to customers. When managers are able to communicate more effectively with that mobile resource, it can be better managed and supported, reducing cost margins and providing better service to the end user.

2.2 Role of Radio-location in Mobile Resource Management

In many applications, an important element in the efficient management of the resource is real time knowledge of the resource's whereabouts. With this information, a mobile resource manager's can achieve dramatic improvements in efficiency, supervisory control, and customer service. Think of the cases of police vehicles being dispatched to urgent events, taxi cabs being coordinated to pick up clients or busses being organized to run on schedule by avoiding bunching or overloading. These are all cases where knowing the location of the vehicle is essential to efficiently managing and supporting the mobile resource.

Transaction Characteristics by Segment



A well designed mobile data network will take into account the typical transaction profile of its target market. Mobile resource management applications are characterized by the relatively short message size used in their transactions. Unlike the "mobile office" applications that make use of e-mail, fax, and data-base file transfers, requiring message sizes from thousands, to potentially millions, of bytes of data, fleet management applications typically require less than a few hundred bytes, and potentially very large numbers of transactions requiring only tens of bytes.

Another important characteristic of mobile support or management applications is the frequency of transactions with individual mobiles. To gain the efficiency that is potential in better management or support requires very frequent communication between the mobile and the support center. Typical feedback from users indicate numbers that range from 5,000 to 20,000 communiques per month per vehicle or employee. This has important network design and economic considerations that we will visit again later.

High volumes of short messages distinguishes mobile resource management and support applications from other data uses. At such small message sizes, the time it takes to set-up and conclude a message transfer becomes a significant factor in the overall network operation. Furthermore, since efficient management of a fleet is often related to the location of the vehicle, and because the vehicles are "on the move," the response time of the network to service requests initiated by the fleet management system or the vehicle becomes a very important factor in service quality evaluation.

The requirement for short *latency* (the time between communication initiation and completion) affects the inbound and outbound message flow aspect of the system design very differently. This is

because the mobile network is not symmetrical in its treatment of inbound and outbound transactions.

A fairly typical arrangement of the network structure has one base station transmitting messages to many mobile transceivers, while many mobile transceivers in a locality typically only communicate with a small number of base stations in the network. The network or the base station can easily control the flow of data outbound to the recipient mobile transceivers, if they are all "listening continuously" to the local base station's broadcasts. However, this matter is not nearly so easy in the reverse direction. In this case, many uncoordinated mobile transmitters may wish to transmit their messages to the network at the same time. If they did, there would be significant message collisions experienced by the base stations. This is the typical channel contention problem; a problem any mobile data network must satisfactorily address in order to successfully support a large user base of mobiles.

2.4 Solution Alternatives & this paper

This paper will discuss a number of different approaches to the kinds of radio-locating and messaging systems that are capable of efficiently and cost effectively supporting the kinds of mobile resource management applications outlined briefly above.

3. A BRIEF OVERVIEW OF TECHNOLOGIES USED IN MOBILE RESOURCE MANAGEMENT

3.1 Satellite Radiolocation Systems

Satellite systems currently being used for commercial vehicle location should more accurately be called radio-navigation systems, since the satellite "system" does not directly determine the location of the vehicle. Rather, using the signals being continuously transmitted by the system allows receivers in the vehicle to determine its own location, in the vehicle. Global Positioning System (GPS) is such a system. If location determined in the vehicle is then to be communicated to the management and support center, then this can only be done via another communication channel, such as a satellite data-link, a cell-phone or an SMR radio-link.

Near the end of the Cold-War, the US military built the Navstar system—later to become the Global Positioning System—to provide an independent navigational facility capable of accurately placing self-guided weapons on remote military targets. It uses a constellation of about twenty four low-earth-orbiting (LEO) satellites that are very accurately coupled in time and position.

The density of satellites is such that at most any time there are enough satellites above the user's horizon to provide an adequate position fix at any time of the day. However, due to the military origins of the system, the commercial users are not able to enjoy the full performance of which the system is capable. The reference signals from which the location of the GPS receiver is determined are programmatically subjected to random-like perturbations, which limit the commercial position-uncertainty of the system to about a hundred meters. (Qualified military users have access to the perturbing codes, which can then be programmatically removed in real time, resulting in position uncertainties about ten times smaller.)

However, by acquiring many position fixes over a period of time (many minutes), and by simultaneously obtaining fixes at both the unknown site as well at a nearby known site, it is possible to improve the quality of the position fix, allowing "survey grade" position fixes with uncertainties in the order of inches. However, such certainty is obtained at the cost of losing "real time" performance.

While GPS uses satellites to establish the radio-navigation reference system, the satellites do not provide any messaging capability (for the commercial user). Once the vehicle's position has been determined by the GPS receiver, an alternative communications pathway must be used to convey that information to the support center. Various organizations have used almost every known means for doing this, from private carrier, SMR voice and data radios, through wireline telephone and US Mail, to cellular telephones and mobile-satellite-data networks.

Another limitation of GPS is encountered in urban environments. A GPS receiver must have line of sight access to multiple satellites in order to calculate its position. In airborne, waterborne, or open road applications, this is rarely a problem. However, in urban environments, buildings and other man made and natural structures can block access to enough satellites to make it impossible to compute a location. In such circumstances, the user must either accept the spotty performance, or combine positions from GPS with estimated positions from a supplementary inertial guidance system when GPS is unavailable.

3.2 Terrestrial Radiolocation Systems

3.2.1 Loran & DECCA Radio-navigation

LORAN and DECCA are low-frequency radio-navigation systems originally developed as navigation aids to shipping. DECCA was originally deployed as a worldwide network, while LORAN was initially deployed to aid navigation in the Great Lakes and coastal waters of the US. The success and widespread use of LORAN by both shipping and aircraft lead to the expanded deployment of reference stations to provide high signal quality coverage across most of North America. Because of the low frequency nature of the signals used by these technologies (and hence very long wavelengths), their resolution is in keeping with their intended use, and position uncertainties in good coverage areas can be less than about a quarter mile.

Significant signal loss occurs between the buildings found in typical urban and some suburban settings due to the very long wavelengths, limiting the effectiveness of the technology in those settings.

3.2.2 Terrestrial Multilateration

While all the systems outlined thus far use hyperbolic multilateration algorithms to find the position of the vehicle from the *effective* time-difference-of-arrival (TDOA) of multiple reference signals at the vehicular receiver, (*effective,* because the time differences are implied from phase difference measurements rather than actual time measurements) there are systems that work off the *direct* TDOA of a single signal transmitted by the vehicle. These systems also typically reverse the direction of the signals, such that the vehicle emits a locating signal (rather than reference stations or satellites transmitting reference signals), which is detected at the nearby network of base stations. The base stations estimate the time-of-arrival of the signals against a time reference common to all the base stations, and send these estimates to a network control center (NCC), where the location is calculated using the hyperbolic multilateration algorithms. In this case the time-differences, and hence positions are calculated remotely from the vehicle, and the results are sent directly (usually via telephone line connections to the NCC) to the vehicle's management and support center. Thus, in such systems, the location of the vehicle is estimated remotely from the vehicle, and does not need to be transmitted across a separate message link. Furthermore, if the vehicular transmitter uses a radio-frequency platform that is compatible with the transmission of both the data and location signals, then no additional channels would be needed to solve the mobile resource management application's need for communication and radio-location.

3.3 Radio-location System's Relationship between TIME, BANDWIDTH & S/N ratio

In the design of radio-location systems, a very important relationship exists between the time it takes to estimate a signal's arrival time to within the precision required by the overall system[1], the bandwidth used by the system, and the signal's quality, usually expressed by its signal-to-noise ratio or signal-to-interference ratio. This relationship (often encapsulated in the form of the *Cramer-Rao bound)* is one of the two key technical issues involved in the choice of operating parameters for a network. The other is the interaction of this relationship with the business/economic model for the network's operation, which determines the network's commercial viability (This will be considered further below).

Fundamentally, this relationship implies that, all other things being equal, the higher the signal-to-noise ratio and the wider the occupied bandwidth, the faster the signal's arrival time can be estimated to within the required uncertainty limit, (and hence the network perform more fixes per unit time).

This implication does not take into account some of the secondary limitations placed on the signal's propagation by the urban and suburban communications environment (such as multipath propagation and shadow fading), nor does the implied fixing rate take into account the effect of signal propagation delay and message processing time requirements of the network.

In the design of high-resolution[2], high-throughput systems[3], these secondary effects play a vital role in the effective throughput of the network, and also dramatically effect the design of the terrestrial infrastructure needed to achieve the necessary performance and throughput.

3.3.1 NarrowBand Systems (FM Voice)

Under the usual urban and suburban conditions found in typical modern cities, narrow-band systems can only provide very modestly small location uncertainties, typically of a quarter to half a mile, whether using phase ranging or comparative signal strength methods to estimate position. With the signal-to-noise ratios used in mobile communications, rates of less than a few tens of fixes per second can be achieved. Increasing the s/n ratio does not improve the situation much, since the low-bandwidth signals are unable to resolve or ameliorate the multipath components that are the major contributors to the position uncertainty.

3.3.2 WideBand Systems (DSS Radar)

Excess delay measurements of the radio signal as scattered by typical urban & suburban environments have shown some statistically repeatable characteristics, which reflect the patterns with which we build the urban environment. A plot of signal excess delay[4] (the amount of additional delay that the signal undergoes due to scattering, compared to the signal's propagation delay if it had traveled line-of-sight) shows a strong peak in the region of 50 to 300 nanoseconds (or feet). To resolve multipath echoes in this range usually requires bandwidths greater than the inverse of the excess delay, or more than 3 MHz to 20 MHz respectively. Such bandwidths are readily achieved by direct-sequence spread-spectrum systems, and

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1 typically expressed in terms such as 'within x-meters for y% of measurements'

2 high-resolution systems have low positional uncertainty

3 greater than hundreds of position fixes per second per network

4 See the paper s by Turin et al — "Simulation of Urban Vehicle Monitoring Systems" and "A Statistical Model of Urban Multipath Propagation." Both appear in IEEE Transaction on Vehicular Technology, Volume VT-21 No 1, Feb. 1972.

have been used in the design of high-performance military RADAR systems for a long time. The use of direct sequence spread spectrum techniques also provides modest additional resistance to in-band interference, as experienced when the band is shared between different users. The attainable process gains are modest in light of necessary trade-offs between conflicting requirements, such as processing gain versus network service throughput, or mobile transmit power level and infrastructure cost, etc.

In practical terms, systems serving the mobile resource management applications have been built using bandwidths between 1 and 25 MHz. However, recent regulatory action by the FCC has restricted the amount of spectrum available for commercial radio-location systems to less than 8 MHz.

Systems capable of resolving the various multipath echoes have recently been built with these wider bandwidths. They use modulation & detection methodologies very similar to those used in the military radar systems. The *later* arrivals can then be separated from the *early* arrivals (the early arrivals having the least excess-delay), significantly improving the quality of arrival-time estimates over those obtained from the more usual "energy centroid of the signal's arrival" approach.

3.3.3 Network Density & Frequency Reuse

A major consideration in the design of the network is the trade-off between the network's service throughput and the cost of the infrastructure. While satellite networks have the advantage of being able to offer national coverage from a few "birds," they are very costly to deploy and maintain, and their ultimate throughput is fixed by the design capacity of the satellite, which is shared over the whole coverage area. For the much higher aggregate capacity needed for typical metropolitan resource management applications, it is less costly to build and maintain a terrestrial network than a satellite network, for almost any network throughput. However, there are many factors to consider in optimizing the deployment design, some of which can dramatically effect the business viability of the network.

Some of the lower priority factors are the cost of base stations, their average spacing, the size of the coverage area, the method and cost for back-hauling data between the base stations and the network control center, the cost of the network control center and the cost of network deployment. The higher priority factors are the effects of protocol design, airtime operation and signal processing (timing and data signal transmission and detection) on the data and radio-location rates, and the availability of frequency reuse to increase the local network's overall throughput.

The reason for the difference between the higher and lower priorities is that to a crude first approximation, the cost of deploying alternative terrestrial radio-location data-messaging network approaches is similar, whereas the real service throughput of different technical approaches can differ by up to nearly *three orders of magnitude*. Such a range can have a very dramatic effect on the business approach, and on the class of service that can be provided to the target market.

At one end of the throughput spectrum are the systems using code-shift schemes for estimating effective signal arrival times, capable of providing maximum position fixes at rates of less than a hundred per second per network, while providing nearly no data-messaging capability. At the other end are systems capable of providing near tens of thousand of fixes per second, while providing aggregate network message throughputs of megabits per second, all in the same licensed bandwidths.

4. SPREAD SPECTRUM PLATFORMS

There are a number of different signal modulations that qualify as "spread spectrum". Each of the differing modulation technologies have their advantages and disadvantages in any particular communications requirement and environment.

4.1 Direct Sequence

Direct sequence systems are capable of providing fast, high-resolution estimates of arrival time, can carry very high speed data, in spite of severe multipath distortion, provide resistance to signal fading in moving vehicles, and provide very fast acquisition of transmitted signals. It does however, only offer modest levels of resistance to in-band interference, and in shared bands, it must often be used along with other techniques, such as spatial diversity, to ensure reliable network operation.

4.2 Frequency Hopping

Frequency hopping systems are capable of providing greater resistance to narrow-band interference in a shared band but, by virtue of the typically narrower bandwidths used, cannot provide much resistance to multipath distortion or fading nor quickly provide the signal arrival-time estimates to within the uncertainties required by typical resource management applications. However, by using large numbers of hopping channels with frequency reuse and effective high-level protocols, very robust, high-capacity data-messaging networks using a shared band can be built.

4.3 Data Modulation & Recovery

At Pinpoint, a direct sequence modulation scheme has been used to yield eight megahertz occupied bandwidth signals using multiple symbols. The scheme uses near-orthogonal coding sequences to modulate a carrier operating in the ISM band. These signals carry both network operational data between the mobile ranging-transponder transceivers and network's base stations, while simultaneously providing very accurate signal arrival time estimates at the base stations. The transceivers use both maximal-length and Gold-codes sequences for spreading codes. The base stations detect the sequences using real-time correlation techniques. The correlators provide their outputs to both code detectors (for data extraction) and DSP's for arrival-time extraction. This scheme provides network operational data throughputs of approximately 256 kilobits per second, and signal arrival time estimates with a line-of-sight uncertainty of less than 5 nanoseconds, at vehicle speeds up to 75 MPH. This approach to a platform for simultaneous data and timing, yields a capacity of up to about 1500 remote position fixes per second, while using a simple airtime protocol in a single wideband channel.

5. MOBILE PROTOCOLS

5.1 Contention & Its Management

Previously we mentioned the contention problem resulting from numerous uncoordinated mobiles attempting the send data to the network at the same time. One way to completely avoid the problem would be for the base station to poll (or interrogate) all the local mobiles sequentially to determine whether it had a message pending, but then the network would spend the majority of its available airtime resource on this activity, without transacting much useful business. At the other extreme, mobiles could transmit their messages whenever ready, and deal with the consequences of the collisions as they occurred. This is the classic ALOHA technique used in Ethernet and other systems. At very low system utilization this works quite successfully, but when the

network traffic increases, the high rate of collisions, and the resulting error recovery efforts of this method, result in severe penalties in terms of potential network throughput.

A more efficient method would be to use a hybrid form of contention management, in which the efficiency of fully scheduled outbound operation is combined with modified form of the ALOHA scheme. In this case the base station regularly signals the mobile transceivers of "windows" during which the mobile's may attempt to gain the base station's attention to request service (indicating to the base station that the transceiver has a specific size message pending "pickup"). Such service requests (SRQ) messages are of very short duration, so that they do not represent a significant proportion of overall airtime. To further minimize the collision probability the SRQ's can be forced to occur in predefined but randomly selected "time-slots," thereby doubling the contention-limits throughput characteristics (slotted-ALOHA.)

5.2 Latency

Such a hybrid, disciplined-slotted-ALOHA approach, combined with frequent SRQ intervals, can reduce the average message latency to very low levels, typically less than two seconds from the time a support application requests a position fix or for a message delivery, until the delivery is confirmed or the position fix is returned. Such short latencies are essential to the efficient management of medium to large fleets of vehicles, such a taxi-cabs, public safety fleets, and public transport bus fleets.

Notice however, that this "average" latency is not the same as *transaction time*, which is the measure of how many of a particular transaction a network can completed per unit time. Much of the action involved in the network is "pipelined," such that base stations may initiate hundreds, or even thousands of position fixes per second, only a few of which may be destined to be delivered to any particular application.

5.3 Network Performance

Networks have been built using these schemes for fast delivery of short, bursty mobile data messages and simultaneous radio-location. They have achieved position fixing rates of up to 1500 fixes per second in minimum configurations, and larger systems will achieve multiples of this through modest frequency reuse. Inbound data rates of about a quarter megabit per second are routinely achieved with very high raw-data reliability, (typically average error rate are less than 2%, compared to the typical 50% error rates due to Raleigh fading found in narrow-band mobile systems). Such small error rates dramatically reduce the system's overhead for error correction, since when an error does occur, its usually due to the complete loss of the whole blocks of data, rather then loss of a few bits of data. Therefore the data-block only need contain error-checking blocks, rather than error-correction blocks or convolutional-coding, which consume much greater overheads. The "lost" blocks are recovered by the higher-level protocol that detects the "lost" or error blocks and requests message retransmission.

6. ECONOMICS

Many alternatives currently exist for voice-channel bandwidth systems capable of delivering wireless data. However, almost all of them are oriented around the voice-circuit paradigm. While this paradigm is eminently suitable for the voice links it was designed to serve, it is quite in-efficient for the relatively short, bursty messages that characterize the majority of mobile digital-messaging.

Imagine, for example, trying to send a hundred byte message over a cellular channel. The call setup

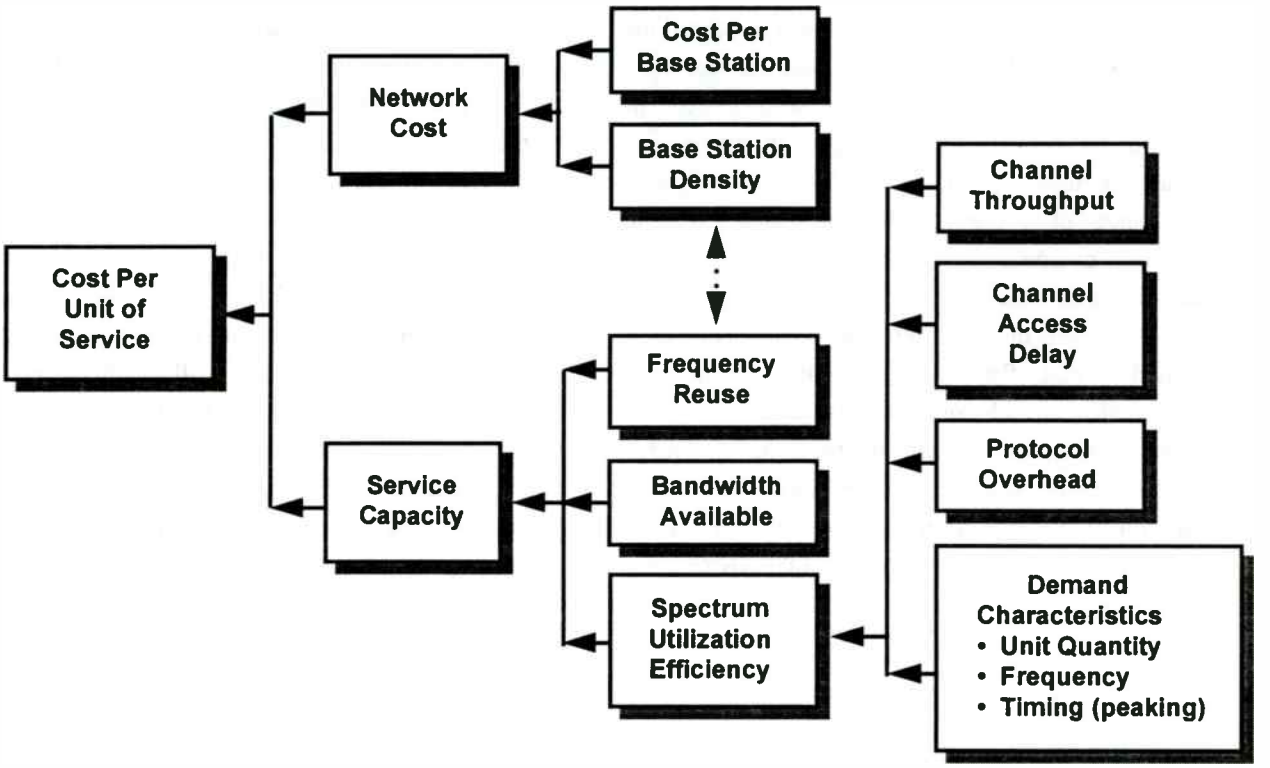
time, from initiating the dial sequence until the cellular modems have synchronized can be as long as thirty seconds, after which the hundred bytes are sent in a second, along with whatever header is needed for the network. Clearly, such a system is not very efficient for this kind of message since more than 97% of the network time was spent in connection-setup overheads. (Cellular was designed for typical call times of a few minutes, in which case the network overhead is only about 10% - a very reasonable amount!)

Moreover, these narrow-band technologies only provide a part of the mobile resource management communication solution. A very large number of mobile applications benefit greatly from knowledge of the mobile's location. As mentioned before, this has typically been supplied by secondary technologies, such as Dead-Reckoning, LORAN or more recently GPS.

The economic viability of a data-messaging and radio-locating network depends on a number of factors. Most important among them is the operating and/or infrastructure cost per unit of throughput. A very low incremental service cost allows the service to be priced very low, encouraging rapid adoption of the service, and early success of the business. It also provides a very important tool for staving off competitors, whether from similar or different competing services offerings.

It is clear that the larger the throughput (provided there are enough service consumers who will pay for it), the lower will be the incremental pricing, or the higher will be the chance that the network will operate profitably. Using Pinpoint's experience as a reference, we will consider here how critically this depends on the design of the network's communication platform and its operating protocol.

Network Economics



6.1 Infrastructure

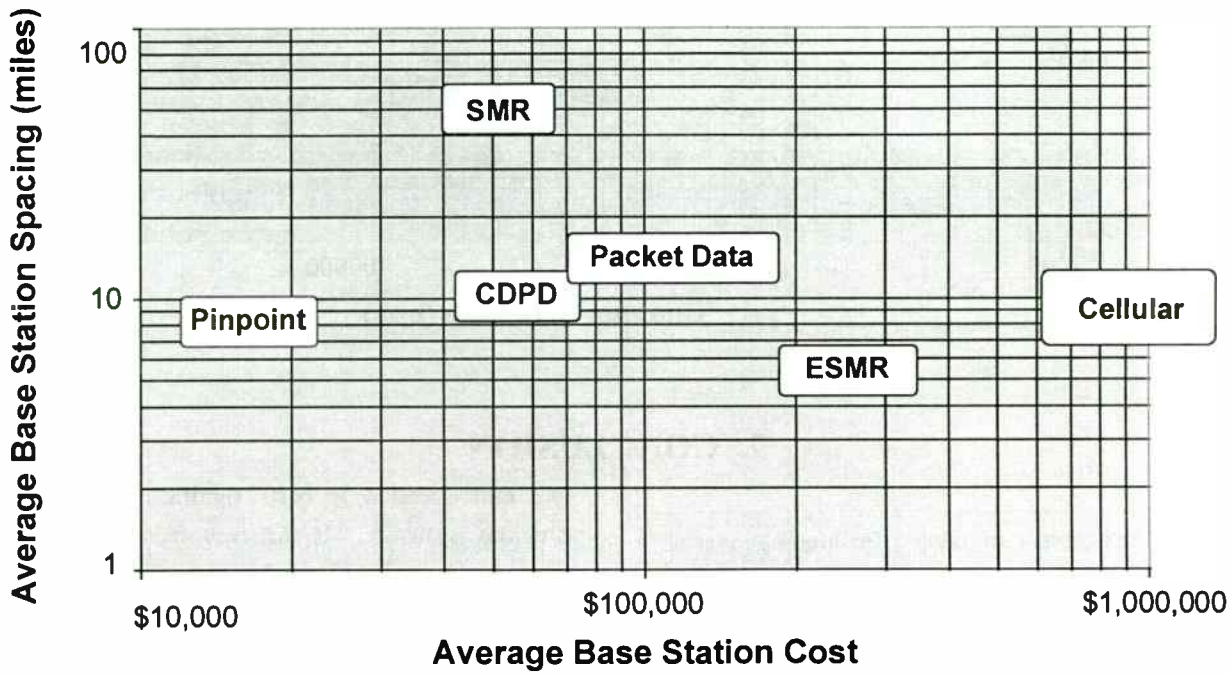
The characteristics of the transmission medium, the limits on available bandwidth, and the limits on available transmission power set the technical stage for the design of a communication system for mobile resource management. The other important factors influencing the business design are the economic ones — with the main outcome being: what will it cost the user to obtain a specific suite of application benefits?

The shared-network and business model developed by Pinpoint have been developed to optimize for rapid market adoption and to spur rapid market growth. That the network and business will achieve these goals is based on providing the network a set of performance parameters that are very easily integrated into support or management applications, a very affordable entry cost of mobile hardware and a low operating cost for the mobile system's manager. (Give the potential subscriber an offer they can't refuse!)

The infrastructure consists of a network control center in each metropolitan coverage area, a network of base stations to provide RF coverage of the region, a backhaul network, provided by either the local telecom provider or microwave links or both, and a national data backbone network that links the regional networks into a transparent national network, that allows transparent "roaming" to the user.

The deployment of the base stations is the major cost element in the infrastructure. It includes the capital cost of site acquisition, base station equipment and installation, and the operating costs of site leasing, equipment maintenance and telecom backhaul communications. The cost of the base station equipment is evolving to the point where it is becoming secondary to the other costs, leading to the search for inexpensive ways to deploy the networks, including inexpensive rooftop space (versus commercial antenna sites), and private microwave backhaul. At the present stage of evolution, base stations are deployed on a roughly five mile spacing "grid" depending somewhat on terrain and urbanization.

Cost of Capacity

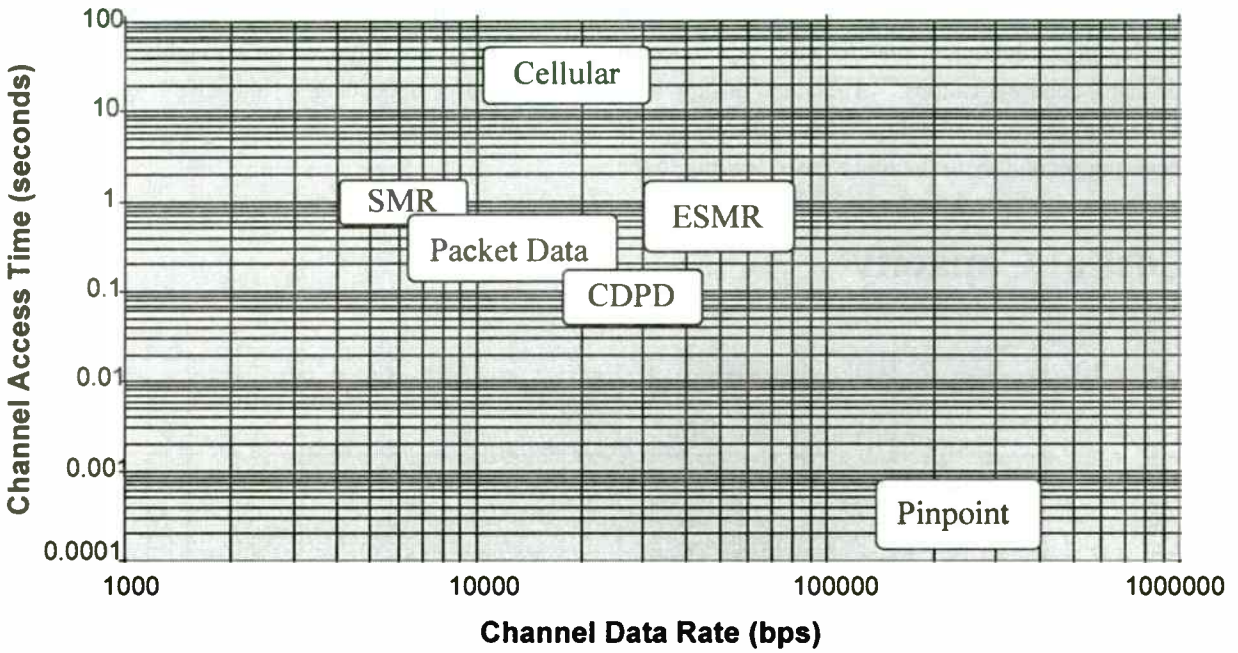


6.2 Capacity

The capacity of the network is easily scaleable. In its simplest deployment,
typical of a large town or small city, the minimum throughput the network would be capable of is up to 1500 position fixes per second, or aggregate messaging up to about a quarter megabit per second. However, since the messages are typically very short, this could also be expressed as about 500 hundred-byte messages per second.

In larger metropolitan areas, the network becomes large enough for frequency reuse to be applied, and the network's throughput scales along with that. In a metro area like Dallas/Fort Worth, the radio-location reuse factor reaches between three and five, while the data-only reuse factor can reach fifteen or more. This can provide tremendous capacity, allowing the network to offer services at even lower cost than in the small cities, where reuse of data-only communications is not feasible.

Spectrum or Channel Efficiency



7. CONCLUSION

The advent of Global Positioning System and the availability of relatively low cost and accurate vehicle location information it provides, has ushered a new era of mobile resource management. It has shown itself to be especially effective in open area, navigation oriented applications. In metropolitan area vehicle tracking applications, however, it shows limitations.

For these applications, a close terrestrial based cousin holds greater promise. A new, wide-band spread-spectrum technology can provide fast, high-capacity, low-cost, mobile packet-data and simultaneous high-resolution radio-location from a single message stream transmitted by the vehicular mobile radio. It provides shared network services for high-speed, fast turn-around mobile data-messaging and radio-location at costs significantly less than previous systems. It achieves these capabilities through a unique combination of previously independently applied technologies, including cellular radio, modern military RADAR techniques for ranging and multipath resolution, custom-designed network and airtime protocols, and efficient airtime management. The design intent has been to deploy a network that will promote rapid market adoption and so spur the explosive growth of mobile resource management applications and markets. Pinpoint anticipates that such growth is also likely to be followed by rapid growth in consumer applications, as has occurred in the cellular and GPS marketplaces.

Low Loss SAW Filters for Mobile Communication

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ABSTRACT

The trend is for mobile radio systems to evolve from analog to digital communication systems. Two of these systems are the Digital European Cordless Telephone (DECT) in Europe and the direct sequence spread spectrum Code Division Multiple Access (CDMA) in the US. With this evolution comes more stringent requirements for IF filters. Typical electrical requirements are for 1% to 2% fractional bandwidth, low loss (5 to 15 dB), phase error < 3.5° rms, shape factors as low as 1.3:1. In addition, they must be low cost and supplied in a small surface mount package.

Classical surface acoustic wave (SAW) filters have drawbacks of high loss, triple transit time spurious, and large size. Resonator filters are limited to small fractional bandwidths and suffer from large group delay ripple. The development of single phase unidirectional transducer (SPUDT) technology has solved these problems. The unidirectionality reduces the insertion loss, the time spurious, and the size. Up to date designs exhibit very small group delay and amplitude ripples and sharp shape factors.

Results will be presented for an IF filter for DECT applications at 112.32 MHz and for a balanced drive IF filter for CDMA applications at 85.38 MHz. These two products exhibit very good performances and are now in mass production.

I. INTRODUCTION

The SPUDT was first reported by Hanma *et al* [1] and later developed by Hartmann *et al* [2] and Lewis [3]. This type of unidirectional transducer structure has the advantages of requiring only a single level fabrication process and of not requiring the phasing networks needed by previously developed "3-phase" and "group type" filter technologies.

The development of this new technology has been slow due to the complexity of the analysis and particularly the synthesis. This is due to the fact that SPUDT's incorporate reflectors inside the transducer which convert the conventional filter's linear optimization problem into a nonlinear optimization problem. Design tools have been recently developed which solve these problems [4-7].

The introduction of products using this new technology has created some confusion about how the filters are to be properly matched. This stems from the fact that the conventional SAW filter needs to be impedance mismatched to obtain a reasonable level of amplitude and phase ripple. The next two sections will describe both the conventional SAW filter and low loss SPUDT SAW filters in terms of simple transmission line models. From these models, the effects that the electrical loading conditions have on the triple transit spurious of the filter, the main cause of amplitude and phase ripples, are determined for both filter types.

This paper will then present two products, one used as an IF filter for DECT (Digital European Cordless Telephone), the second is an IF filter for PCS using the CDMA (Code Division Multiple Access) standard. These products are mounted in hermetic surface mount (SMT) ceramic packages and require simple fixed element matching networks. Both filters utilize SPUDT structures because this solution optimizes both the performance and the cost, meaning small size and low sensitivity to manufacturing, matching, and temperature, all key parameters for high volume production. They were both designed using procedures detailed in [4-7].

II. REVIEW OF A CONVENTIONAL SAW FILTER

A conventional SAW filter consists of two bidirectional transducers, each having a pair of interdigitated metal

electrodes deposited on the surface of a piezoelectric substrate as shown in fig 1. This device can be modeled as shown in the simplified model of fig 2 with a transmission line terminated at both ends and tapped at two places with $\lambda/4$ transmission lines which are coupled through transformers having turns ratios of $\varphi_1(\omega):1$ and $\varphi_2(\omega):1$. The termination impedances Z_o represent the acoustic absorber material (fig 1) at the ends of the substrate. The input and output admittances Y_1 and Y_2 are

$$Y_1 = G_1 + j\omega C_1 \qquad (1a)$$

$$Y_2 = G_2 + j\omega C_2 \qquad (1b)$$

where $G_1=\varphi_1^2 / 2 Z_o$ and $G_2=\varphi_2^2 / 2 Z_o$

The input admittance Y_1 is found with port 2 short circuited. Under this condition, transducer 2 has no reflection. The output admittance Y_1 is found in a similar way.

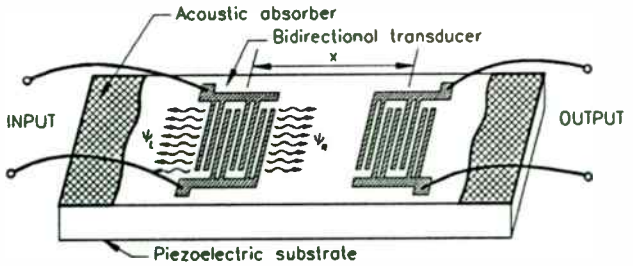


Figure 1 - Conventional SAW filter

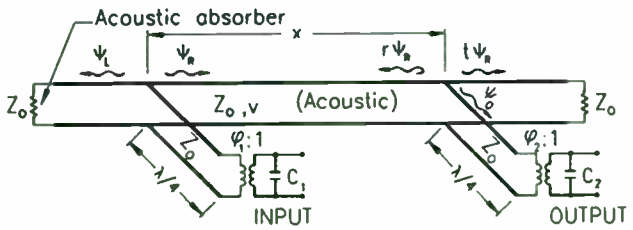


Figure 2 - Transmission line model for Conventional SAW filter

Maximum power transfer from the input to the output is achieved when the input is conjugate matched to Y_1 and the output is conjugate matched to Y_2 as shown in fig 3. From the model of fig 2 it is clear that 1/2 the input power is lost to the acoustic absorber (wave Ψ_L). The remaining signal (wave Ψ_R), is split into three signals at the output transducer (reflected wave $r\Psi_R$, transmitted wave $t\Psi_R$, and output wave Ψ_O). The resultant power delivered to the load is 1/4 the input power or 6 dB loss.

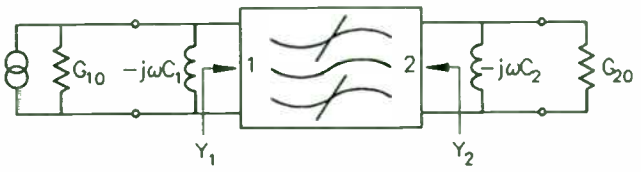


Figure 3 - Conjugate matched filter

The drawback of achieving minimum loss is that a conjugate match of the input and output is a mismatch to the acoustic transmission line, giving a reflection coefficient of $|r| = 0.5$ which results in a 12 dB triple transit (TT) time spurious relative to the main signal. This spurious causes large amplitude and phase ripples. The reflection can be reduced by increasing the value of the load conductance, and it is zero when the load is a short circuit. For the conventional filter the triple transit is approximately twice the filter insertion loss. It can also be shown that the voltage transfer function of this filter for large source and load conductance is related to the turns ratios

$$\frac{V_2}{V_1} \propto -\varphi_1 \varphi_2 e^{-j2\pi fx/v} \qquad (2)$$

The above drawbacks have lead to the development of low loss filter structures using SPUDTs. One type of structure is described in the next section.

III. TWO TRANSDUCER SPUDT STRUCTURE

The simplest low loss filter structure consists of an input and an output SPUDT as shown in fig 4. This structure is the conventional SAW filter structure with the bidirectional transducers replaced with SPUDTs. The SPUDTs shown below are DARTs having regions of electroacoustic transduction and regions of acoustic reflection, resulting in a transducer which ideally emits acoustic waves in only one direction. The electrical model for the ideal case is given in fig 5.

The input and output admittances Y_1 and Y_2 for the SPUDT filter the same as equs 1a and 1b with conductances G_1 and G_2 given by

$$G_1=\varphi_1^2 / Z_o \quad (3a)$$

$$G_2=\varphi_2^2 / Z_o \quad (3b)$$

For this structure, the input admittance Y_1 is found with port 2 conjugate matched (fig 3). Under this condition, transducer 2 has no reflection. The output admittance Y_1 is found in a similar way.

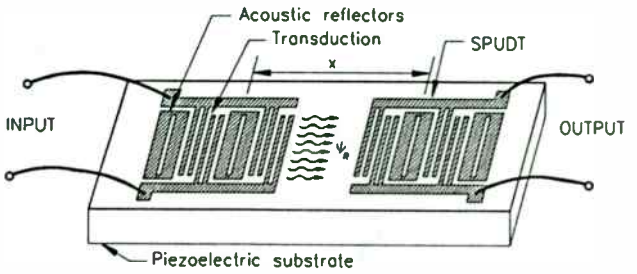


Figure 4 - SPUDT filter

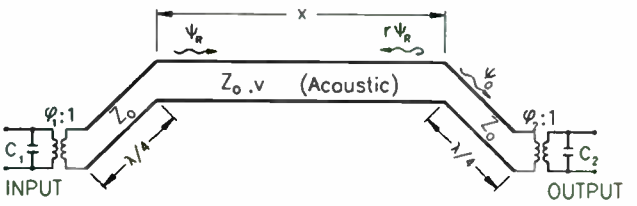


Figure 5 - Transmission line model for SPUDT filter

Achieving minimum loss also has the effect of eliminating triple transit, minimizing amplitude and phase ripples. An added benefit is that the impedance mismatch between the input (output) and the source (load) is small, resulting in a good VSWR.

The practical low loss filter is not perfectly unidirectional, emitting a percentage of it's energy in the backward direction. The majority of SAW low loss filters fall into this category. A transmission line model for the practical low loss filter is given in fig 6. The quarter wave sections of kZ_0 transmission line are a measure of the transducer directionality, being the same for both transducers in this example. The parameter $k = 1$ for the conventional bidirectional transducer and $k = \infty$ for the ideal unidirectional transducer.

The input and output admittances Y_1 and Y_2 for the practical SPUDT filter are given by equs 1a and 1b with conductances G_1 and G_2 given by

$$G_1=\frac{k}{k+1}\varphi_1^2 / Z_o \quad (4a)$$

$$G_2=\frac{k}{k+1}\varphi_2^2 / Z_o \quad (4b)$$

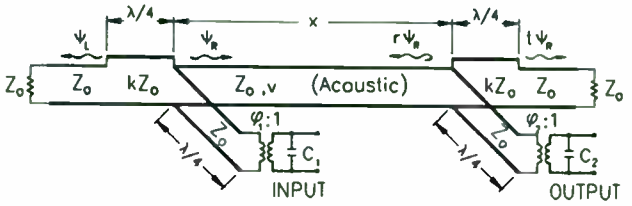


Figure 6 - Transmission line model for practical low loss filter

Zero reflection is obtained when the source and load conductances are as given in equ 5.

$$G_{10}=\frac{k^2-1}{k^2}G_1 \quad (5a)$$

$$G_{20}=\frac{k^2-1}{k^2}G_2 \quad (5b)$$

Thus for a practical low loss SAW filter there is an optimum source and load (and corresponding insertion loss) for which triple transit spurious can be minimized. The required impedance mismatch is a function of the substrate, metal thickness, and relative bandwidth of the filter.

IV. CDMA FILTER

A CDMA IF filter [8], for the cellular phones, has been designed using this SPUDT structure. The interests of such a structure in the CDMA architecture are : the very small phase and amplitude ripples, the low losses, but above all, compared to the classical structure, no triple transit echo in the time domain response.

For this filter the typical performances at room temperature are the following :

Center frequency	85.38 MHz
Insertion loss at f_0	14.5 dB
Passband at 5 dB	1.33 MHz

Rejection at 33 dB	1.71 MHz
Amplitude ripple within f_0±300 kHz	0.35 dB
Phase variations within f_0± 1.26 MHz	1.7 °rms
Ultimate rejection	45 dB

In addition to the above, the filter is required to operate with balanced impedances. This requires that the + and - ports of the input (output) have the same impedance to ground.

To achieve such performances the filter must be tuned as shown on the fig 7. The filter can be easily tuned for other balanced impedances by changing the values of the matching elements. The values of inductors, and capacitors, principally depend on the structure of the PC board and of the associated stray capacitances. For the inductors, ± 2% series and high Q (> 40) must be used to guarantee good insertion loss and amplitude ripple. However, depending upon the configuration of the electronic circuitry, ± 5% inductors series may be used as well.

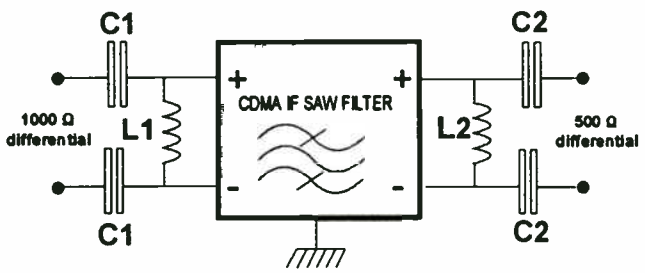


Figure 7 - Schematic of the tuning

Test fixture matching components values :

L1 = 470 nH	L2 = 390 nH
C1 = 3.3 pF	C2 = 3.9 pF

The filter is mounted in a 20.1 x 8 mm² hermetic ceramic SMT package. A typical S21 and group delay response of this filter are shown on the fig 8, with the corresponding time domain response on fig 9.

All the performances of the TMX IF CDMA SAW filter are guaranteed within the total temperature range, which is -25°C to +80°C, and within the inductors and capacitors tolerances. Fig 10 shows the variations of the amplitude ripple and insertion losses at the three critical temperatures +80°C, +25°C (corresponding to the turn over temperature) and -30°C. These measurements have been made on the SAW filter with its full tuning. On this plot the higher losses correspond to the higher temperature.

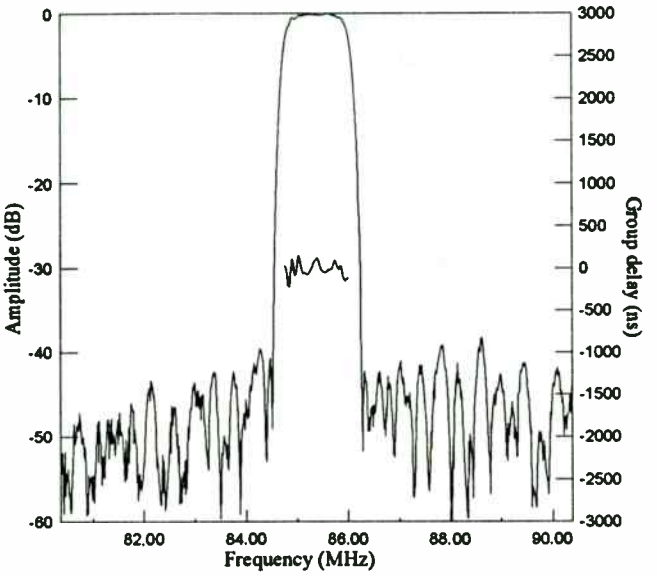


Figure 8 - Typical response

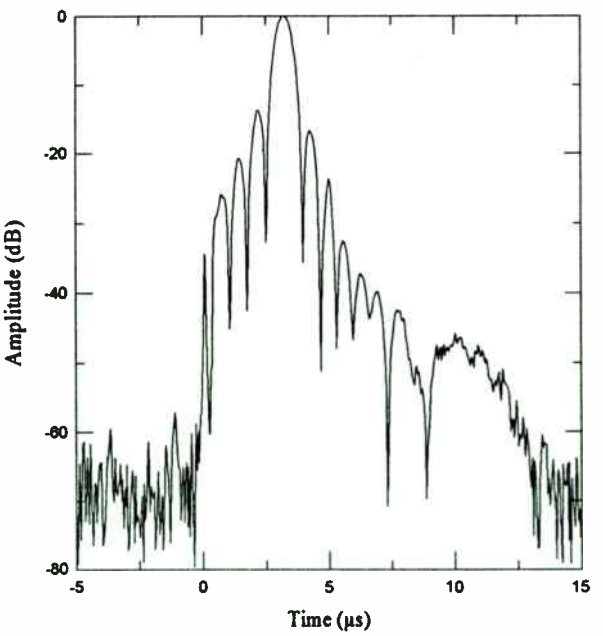


Figure 9 - Typical time domain response

Concerning manufacturing, the reproductibility in high volume production is very good. Figs 11 & 12 present a superposition of 20 filters illustrating the

production. The first plot corresponds to the amplitude transfer function over 15 MHz and the second one to the same response over 2 MHz and with the linearity phase error over 1.26 Mhz.

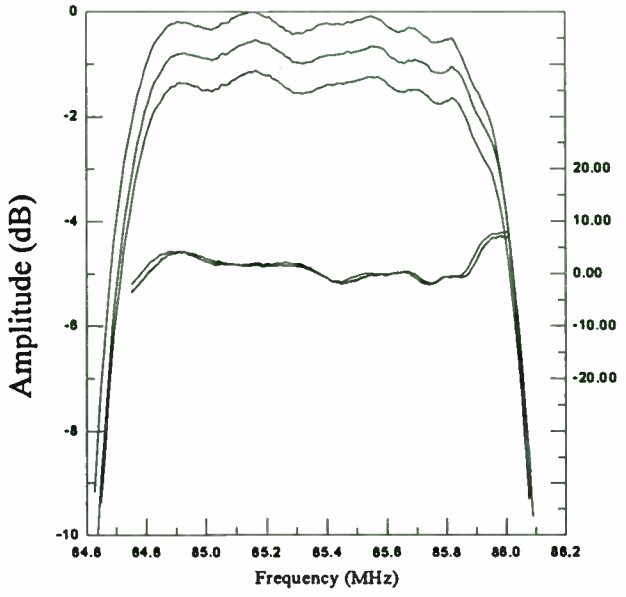


Figure 10 - filter over -30°C,+25°C and 80°C

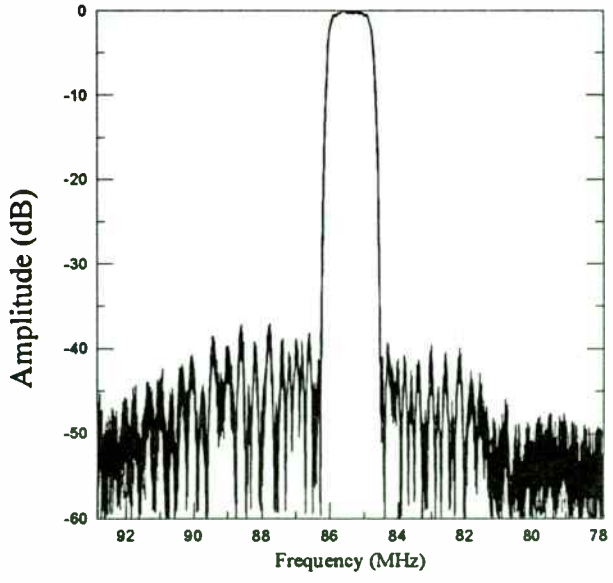


Figure 11 - 20 filters at room temperature

This low cost 85.38 MHz IF SAW filter is available in mass production, it fulfills the mobile radio quality standards. After passing an automated testing procedure the filters are packed in standard tapes and reels for automatic insertion, compatible with most automatic assembly technologies used to built electronic circuits.

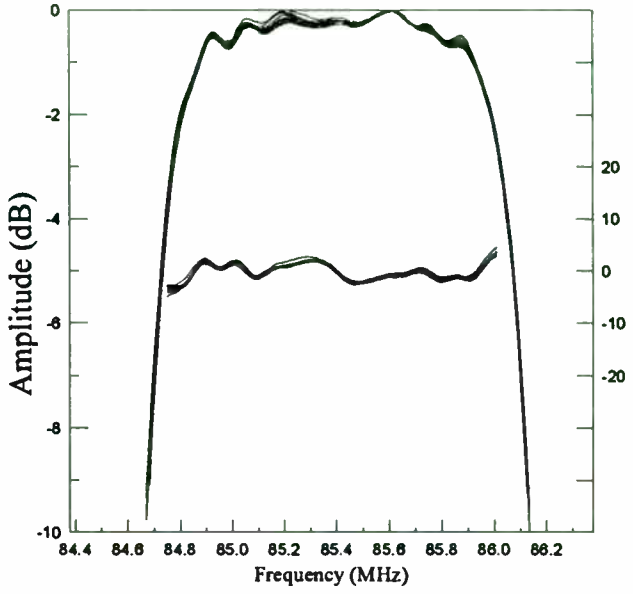


Figure 12 - 20 filters at room temperature

V. DECT IF FILTER

The above low loss design principles have also been used to design a DART filter on a 112 ° YX LiTaO3 substrate [9]. This filter is dedicated to IF filtering for DECT applications. The major advantages of this two transducer SPUDT structure are low temperature and matching sensitivity while exhibiting low insertion loss (typically 6 dB).

The electrical specifications of this filter are the following :

Source and load impedance : 50 Ω
Operating temperature range : 0°C to +55°C
Template center frequency f_0 : 112.32 MHz
Template on the amplitude of the transfer function:

- Bandwidth at -3 dB : ≥0.576 MHz
- Bandwidth at -10 dB : ≤1.00 MHz
- Bandwidth at -15 dB : ≤1.10 MHz
- Bandwidth at -20 dB : ≤1.15 MHz
- Bandwidth at -25 dB : ≤1.20 MHz

- Bandwidth at -28 dB : ≤1.35 MHz
- Bandwidth at -30 dB : ≤1.728 MHz
- Bandwidth at -40 dB : ≤2.00 MHz

Ultimate rejection :

≥ 40 dB from 50 MHz to 109.82 MHz

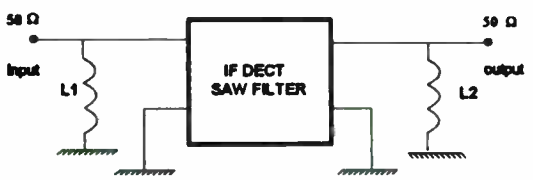
≥ 40 dB from 114.82 MHz to 150 MHz

Insertion loss : ≤8 dB (6 dB typ)

Group delay ripple: ≤600 ns -pp.

($f_0 \pm 0.576$ MHz)

These performances are obtained with a standard parallel inductor for 50 ohms source/load impedances. The filter is supplied in a SMT type package whose size is 13.3 x 6.5 mm^2 packed in tape and reel. The parallel matching inductor values on our test fixture are indicated in fig 12. The values of the inductors can be slightly different when soldering the filter on the final PC board because of the change in stray capacitances. This change in inductor value may slightly affect the measured insertion loss because of the Q of the inductors.

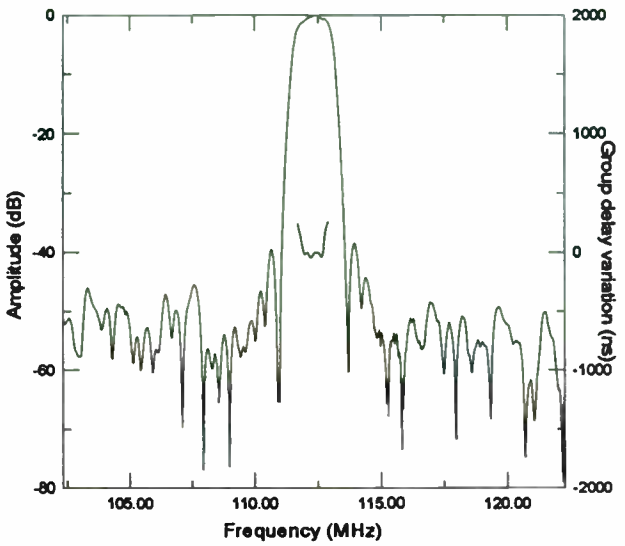


L1= 82 nH (±5%)
L2= 68 nH (±5%)

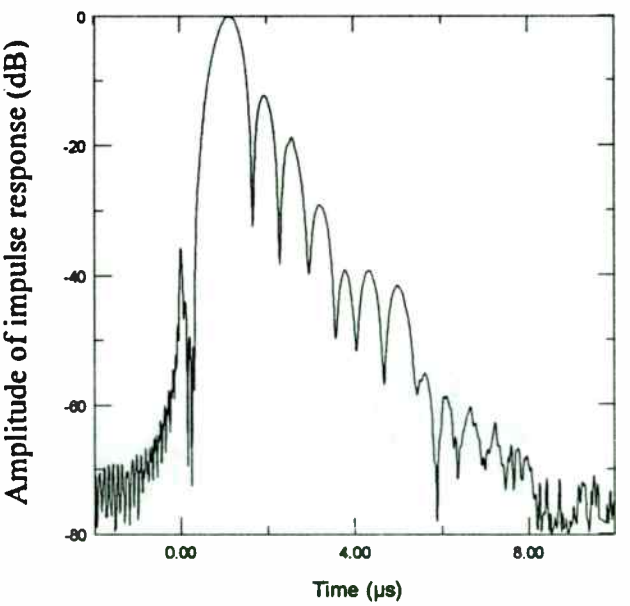
Figure 12 - Schematic of the test circuit.

Fig 13(a) shows a typical transfer function with both amplitude and group delay variations. The reference for minimum insertion loss is 6.3 dB. The impulse response (see fig 13(b)) , of this filter illustrates the efficiency of SPUDT structures to increase the time length of the filter. In a classical SAW filter the impulse response length is directly related to the length of the substrate, corresponding in this case to 3 µs. The reflectors in the SPUDTs extend this length to more than 4 µs. It appears that the triple transit level is 30 dB (the filter delay is 1.03 µs), however this time lobe is in reality part of the designed impulse response of the filter. If it were triple transit then it would have approximately the same time width as the main lobe.

The reproducibility of manufacturing is illustrated on fig 14 where S21 parameter (measured with the same test circuit) of 20 filters are superimposed. Quantitative analysis of dispersion over a more important quantity (150 pieces) has been performed. It appears that variation intervals (maximum - minimum) for center frequency and insertion loss are respectively 30 kHz and 0.5 dB around the mean value.



(a)



(b)

Figure 13 - typical frequency (a) and impulse (b) responses

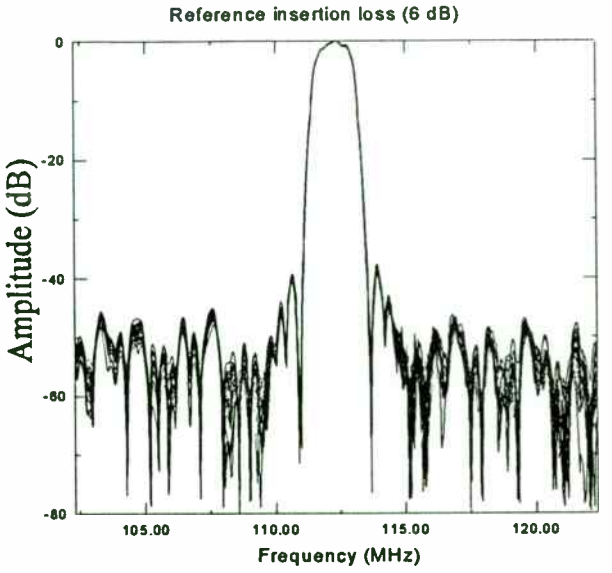


Figure 14 - Superimposed transfer functions of 20 filters

Figure 15 shows the variation of the amplitude of the transfer function in the operating temperature range (3 plots corresponding to 0°C, 25°C and 55 °C). The transfer function of the filter varies in frequency with a coefficient of -18 ppm/°C. The minimum insertion loss typically increases of 0.3 dB from 0°C to 55°C.

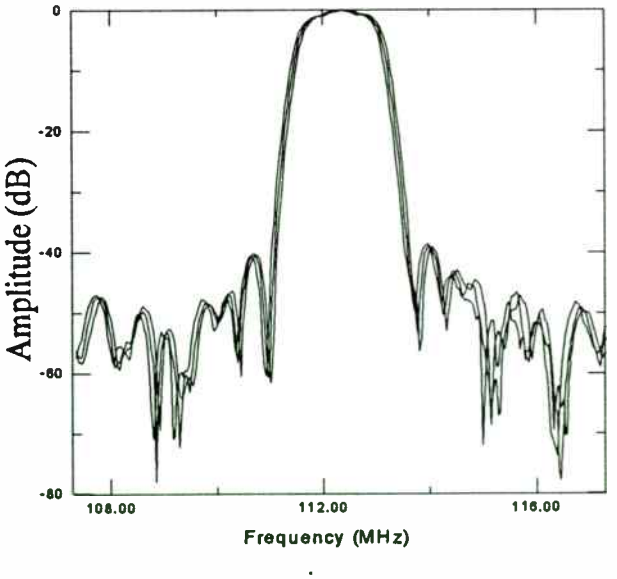


Figure 15 - variation of amplitude response with temperature from 0°C to 55 °C

Figure 16 illustrates the low sensitivity of the filter to matching element variations. Five cases are superimposed corresponding to a relative variation of ±5% of L1 and L2 values (see fig 16). The five L1,L2 combinations are the following :

L1	L2
0 %	0 %
-5 %	-5 %
-5 %	5 %
5 %	-5 %
5 %	5 %

The maximum insertion loss variation is about 0.3 dB over these cases.

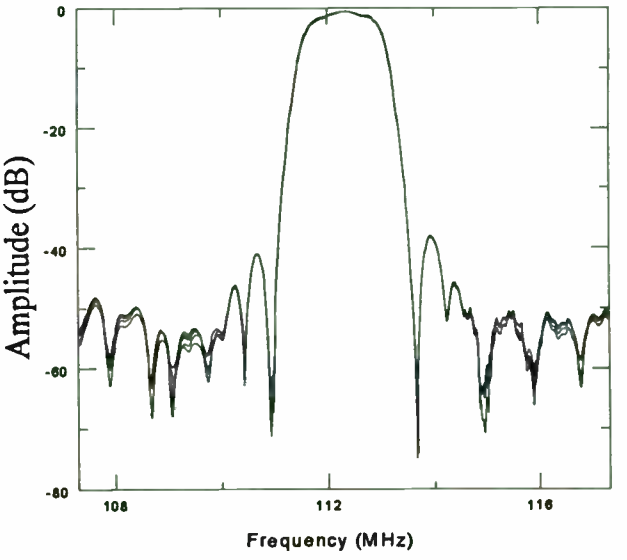


Figure 16 - variation of amplitude response with matching elements tolerances (±5%)

VI. CONCLUSIONS

Transmission line models for both a conventional SAW filter and low loss SPUDT SAW filter have been presented. From these models, the effects of the electrical loading conditions on the triple transit spurious in the filter have been examined. Data on two SPUDT SAW filter products have also been presented: an IF filter for DECT applications at 112.32 MHz and a balanced drive IF filter for CDMA applications at 85.38 Mhz.

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OPTIMUM DIRECT-CONVERSION RECEIVERS

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Abstract - **This paper analyzes the theoretical and practical problems of direct conversion receivers versus superheterodyne receivers. Output data jitter, L.O. frequency offset, discrete components, EMI-RFI and other important problems of direct-conversion techniques are evaluated. A low power, low pushing crystal oscillator is proposed. Measures over Direct Conversion Receivers and equivalent Superheterodyne Receivers are presented and compared. Most of these results are applicable to BFSK direct conversion receivers.**

I. Introduction

Nowadays direct-conversion receivers are beginning to be used for applications such as paging receivers, remote control and other Wireless systems [1,2]. That is due to their advantages over superheterodyne receivers: Low power consumption, small size and low cost. Nevertheless, to achieve the best performance of this architecture, it is necessary to optimize their main subsystems. This paper reviews the most important theoretical and practical problems, limitations and their solutions of direct-conversion receivers specially for BFSK applications.

It must be remembered that direct-conversion techniques are not anything new. The most primitive receivers used direct-conversion. but they were superseding quickly by the "latest" superheterodyne techniques. The benefit of direct conversion receivers lies on low size and power consumption. These reductions of size and consumption are obtained by using monolithic integrated circuits [3]. These ICs contain most of the subsystems of this architecture, specially the baseband signal processing circuits. Silicon Bipolar processes are widely used with direct-conversion receivers due to their relatively good performance, low consumption and relatively low cost [4]. Since some years it is possible to integrate a complete receiver for paging applications. Nevertheless, not all the subsystems are integrated in order to get the best performance or maximum flexibility. So, it is desirable to use some external circuits (usually low noise front-end or local oscillator), made with discrete components. That is specially a good solution if the application does not justify the development of a custom IC.

Furthermore, with adequate bipolar integration processes a noise figure of the transistors for the L.N.A. of 4 dB [5] is not a bad result. If maximum sensitivity is required, like in most personal communications devices for Wireless applications the use of an external L.N.A. with discrete devices that performs a noise figure less than 1.5 dB would be a good choice.

Direct-conversion techniques also present theoretical disadvantages. Theoretically Direct Conversion B.F.S.K. receivers are "2 dB worse" than an ideal incoherent B.F.S.K. receiver. For B.F.S.K applications, the data jitter at the output is an important problem that makes difficult clock recovery of the received signal etc.

So the design of a direct conversion receiver capable of replacing successfully a superheterodyne one, it is not an easy task.

II. Data jitter and L.O. frequency offset.

One of the most important applications of direct conversion receivers is the demodulation of low rate B.F.S.K. signals such as signals of P.O.C.S.A.G. The most widely used architecture used for this application is shown in the figure I. There are other architectures such as frequency-offset, but that showed in figure 1 is widely used [6,7].

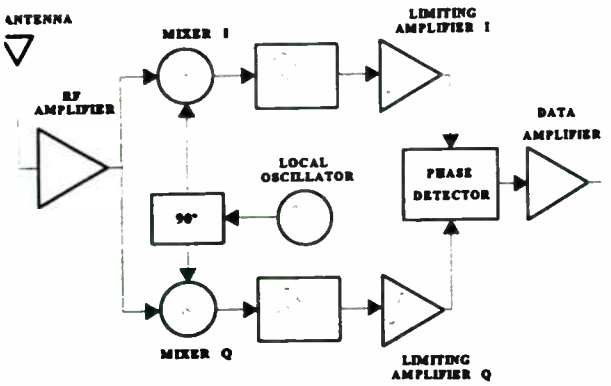

Fig.1. Dual channel D-C receiver

Like it can be observed, the receiver uses two channels and its L.O. is not a coherent system. In a superheterodyne topology it is not a special problem. In a zero IF system with two channels (that uses a standard phase comparator), the instantaneous difference between the frequency of the carrier and the frequency of the L.O. causes an important data jitter in the output signal [8]. For a 1200 baud signal (P.O.C.S.A.G.) a data jitter ≈ 15% of the demodulated signal is something usual with most widely used demodulators. This results are obtained for an L.O made up with a 10 p.p.m. quartz crystal. This data jitter is lower for low data rates and would make the clock recovery at the output impossible for high data rates. Data jitter would be canceled with an ideal phase detector with continuous monitoring of the phase shift between i(t) and q(t) signals. Some authors have proposed architectures based on the use of eight I/Q signals [9]. For high frequency applications this solution is too complicate, expensive and consumes too power to compete with superheterodyne systems. More sophisticated demodulators using only two channels have been proposed to achieve some improvements over standard demodulators [10,11].

To get the best performance of a direct conversion receiver (or any receiver), in a general way it is a rule that the bandpass of their filters must be kept at its minimum value. The response of a true D-C receiver predetection filter is showed in figure 2. Most selectivity of D-C receivers is obtained at baseband. B.F.S.K. receivers usually integrate gyrator filters using with built-in silicon-nytride capacitors [12]. One of the most important problems to achieve god selectivity is the dynamic range at the input of these filters. The filter must be able to select signals with very different levels. The input impedance to the R.F. mixers and amplifiers of the integrated circuits is usually high due to the use of differential amplifier topologies. That simplifies the use of high selectivity filters at the input. The use of a Loop antenna of high Q also contributes to improve the filtering at R.F. [13].

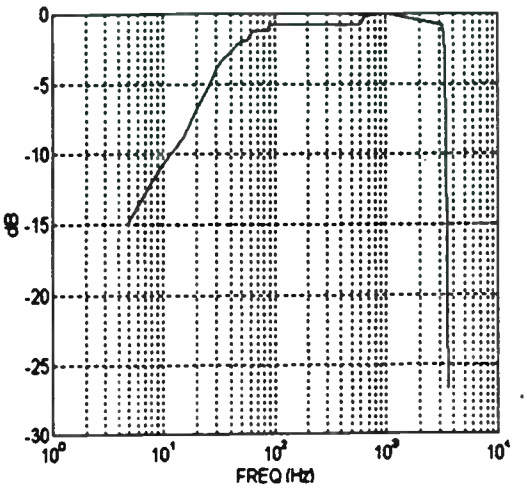

Fig 2. Filter resposnse of a true D-C receiver

The bandpass a widely used D.C. receiver used for paging applications is approximately 4500 Hz. A crystal of standard quality with a tolerance of 50 p.p.m. can vary 8500 Hz the center frequency of the baseband signal. A high quality local oscillator with a tolerance of 10 p.p.m. is generally used. Nevertheless, some tolerance in the bandpass of the baseband filter is also desirable. The theoretical degradations of B.E.R. with local oscillator drift have been showed by Oishi [14]. A measure of this with a true D.C. receiver is showed in figure 3.

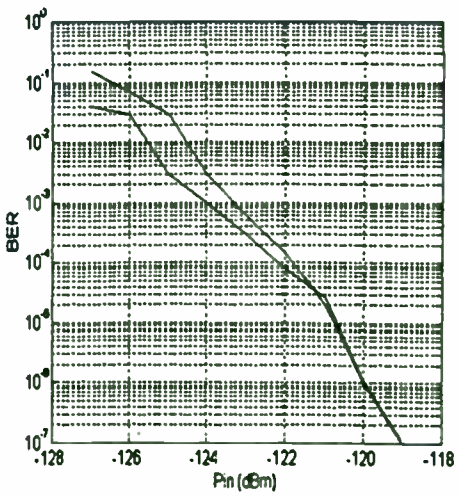

Fig 3. D-C versus Superhet. BER measures

III. Discrete components.

Previously it has been mentioned that the whole subsystems of the D-C receivers are not usually integrated. Special cares must be taken in order to get the best performance when selecting those discrete parts. The next paragraphs analyze the effects of the selection of discrete parts.

a) Discrete transistors: Discrete transistors are used to design the low noise amplifier, the crystal overtone oscillator and seldom the mixer. New bipolar transistors designed for wireless applications with small cases (SOT 23) are preferred. Some are capable of getting a noise figure of 1 dB with low Ic current (1mA) and $V_{CE} \leq$ 2. V. Like in other systems, the best arguments to select these parts are: minimum noise and high IP•3. Due to the low voltages usually present in D-C receivers that are difficult tasks. The experience shows that low noise figure is useful when the source impedances needed for low-noise operation is easy to synthesize. Sometimes is desirable a transistor with a bit higher noise figure if this can be easily obtained. It must be remembered that often the source load of the low noise amplifier varies continuously in a true wireless system, so a stable point of operation is essential. To kept high dynamic range a proper design of this subsystem is crucial due to its relative high consume, many times equal (even greater) than the rest of the receiver. Nevertheless, 1 mA I_c of bias current will give a very low compression point and IP3•. Very low consumption DC receivers incline to saturate in many environments. Therefore, an A.G.C. system is always a good precaution [15,16].

b) Passive components: Most D.C. receivers use components for surface mounting (At the present 0805 is the wide used size). With some inductors and capacitors used with D-C receivers special cares must be taken. The L.O. usually is very simple. To get the best performance cares must be taken when selecting the temperature coefficient of the reactive associate components. To get a temperature stable L.O.
attention must be paid to select capacitors and variable capacitors (usually TC must be negative and great)

Most architectures that use integrated bipolar circuits exhibit relative high impedances at many ports. See figure 4. Therefore, Q of passive components is an important task. Standard coils for S.M.D. (apart from parasitic effects) exhibits a very poor Q due to the thin wire used. That can ruin the noise figure or the selectivity of an input circuit for example. At this points air core inductors are desirable. Some manufacturers sell this kind of coil for S.M.D. The same cares must be taken with capacitors, specially variable capacitors. The tolerance also must be kept at its minimum value at points where a high Q is required.

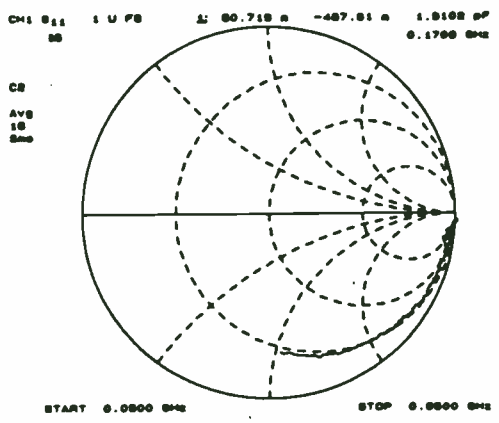

Fig 4. input impedance to a true D-C receiver IC

c) Printed Circuit Board: Designers are looking for minimum size when using D-C receivers, so the length of the connections in the PCB usually is kept as short as possible. In order to optimize space, the lines are usually very thin (10 mils or less), and the use of tortuous lines is something tempting. That yields in the introduction of undesirable inductances, and in I/ Q systems a dangerous lag of the phase of any channel. Apart from this, like is obvious, the radiated power is increased, that is specially undesirable in some D-C receivers. The experience shows that is desirable a greater P.C.B. if the lengths of their lines are kept balanced.

The thickness of the PCB is usually kept at minimum, apart from a mechanical benefit, a thin PCB reduces radiation and R.F. losses.

IV. Radiation of the O.L.

Location of the L.O. is something critical in order to reduce the interference with the received signal. That is a true problem in systems where the receiving antenna is to close to the P.C.B. The best solution is to use modulation systems with the carrier suppressed and to introduce a zero in transfer function of the baseband filter. But if this radiation is too high, risks of desensitization exist in systems

where the receiving antenna is to close to the P.C.B. of the receiver such as pager receivers. That is the reason because the use of ultra-low power L.O. and high gain mixers stages are very adequate for these systems.

The use of cascode low-noise amplifiers also contributes to minimize de radiated power of the L.O. due to its inherent low X_{12} parameter. Cascode amplifiers exhibit more gain than single ended stages and high output impedance. This high output impedance makes easy the use of interstage high Q R.F. filters to minimize desensitization of active mixers due to neighbor interfering signals. Like is the know, the main problem associated to cascode stages is their tendency to oscillate. Taken some precautions these oscillations may be "killed" without sacrificing gain. A series resistor at the collector can be used to make that.

The radiation of the O.L. also can cause desensitization to nearest D-C receivers operating at the same frequency. Therefore, to kept this radiation at its lower value is important in D-C systems.

Figure 5 shows the measure of the radiated output power of a true D.C. receiver for paging applications. Like it can be observed, some harmonics of the L.O. are also radiated, but with a proper design all the components are kept under the maximum legal limits. This measures have been taken into a calibrated anechoic chamber.

The radiation pattern is similar to a dipole.

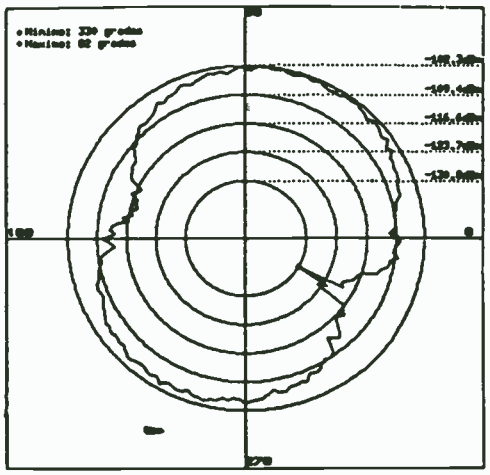

Fig 5. radiation pattern of a true D-C receiver measured into anechoic chamber.

VI Local oscillator.

In previous paragraphs the importance of the stability of the L.O. and the need of a minimum power of this oscillator has been established. Simulations where degradations of the B.E.R. of the output signal are shown has been reported in previous papers. Due to those hard specifications the pushing of the L.O. is another important factor to consider. So low-consumption regulators are used often. Some authors had proposed the use of A.F.C. with D-C receivers [17].

Therefore the L.O. used with D-C Receivers must exhibit low power consumption, low pushing and low pulling, high long term stability, low radiation and low size. Those specifications at a fixed frequency can be accomplished using crystal oscillators.

Low power consumption means a low output power level. Due to the relative high input impedance of the mixers the required signal of the L.O. is typically less than -20 dBm. With a typical efficiency between 2% and 5% the typical power consumption is 500 μW or 200 μW (1V*0.5 mA or 1V*0.2 mA).

The output frequency is usually located at V.H.F. or U.H.F. Therefore, the designer must decide between 7th and 9th overtone crystals or 3th or 5th overtone oscillators plus a frequency multiplier.

When using high overtone crystals greater resistance appears that can cause difficulties to start oscillations due to the low gain of a transistor polarized with low currents (0.2mA-0.5mA) Furthermore, those crystals are hard to manufacture and the oscillator is quite difficult to adjust. By other hand to use frequency multipliers means more components, higher power consumption and a greater P.C.B.

The experience of the authors shows that the optimum oscillators to conjugate low size, low power consumption and easy adjust using the less expensive quartz crystal is showed in figure XX. It uses a 5th overtone crystal and a frequency multiplier using only one transistor. This oscillator is made of one transistor, two coils, five capacitors, two resistors and one crystal.

This oscillator is based on the classic Colpitts oscillator using a 3th or 5th overtone which is selected with the parallel resonant circuit in the collector. At this point a current plenty of harmonics can be extracted.

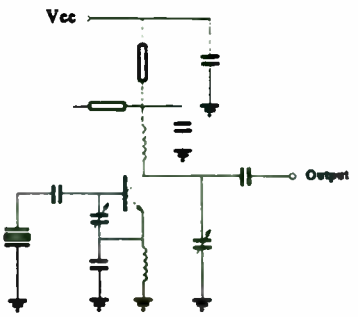

Fig. 6. Proposed optimun crystal oscillator

With this oscillator a low pulling figure can be achieved because the signal is extracted at the collector of the transistor. This point exhibits a very low impedance at the oscillating frequency due to the high Q of the resonator.

Low pushing is crucial in receivers supplied with batteries. That can be achieved working in a low overtone. So the feedback capacitances of the oscillator are quite higher that the parasitic capacitances of the transistor. Therefore, a higher Q is achieved with lower dependence of the oscillation frequency on the variations of the active device due to power supply variations. In table I typical values of pushing and pulling figures that can be achieved with this kind of oscillator are showed.

Table I. Pushing and Pulling Figures

Frequency Pushing		Frequency Pulling	
Vcc ±10%	0.09 p.p.m.	12 db Rtn Lss.	0.17 p.p.m.
Vcc ±20%	0.15 p.p.m.	6 dB Rtn Lss	0.05 p.p.m.

Another important task is the right shielding of the L.O. to avoid the interference of the radiated signal of the O.L. on the received signal. (Some pick up of the L.O. signal is unavoidable). The crystal and the coils must be shielded if shielding is not used.

VII. Comparison between Direct conversion and Superheterodyne techniques

When comparing superheterodyne Wireless receivers versus D-C Wireless receivers, attention must be paid to electrical performance, consumption, size and cost aspects.

a) Electrical performance: If special cares are taken, most direct conversion receivers would exhibit similar electrical performance for many commercial applications like superheterodyne receivers. Nevertheless if the best electronic behavior is the main target, superheterodyne receivers are better. In B.F.S.K. applications (the most usual application for D-C today), the presence of the data jitter inherent to the most widely used D-C architectures is a limiting factor that makes difficultly the clock recovery for very low input signals. This is a penalty in the maximum sensitivity of the receiver, but in many cases the external noise and interference are the true limits of the receiver. By other hand in D-C architectures the problems of image rejection do not exist.

b) Size: Due to the integration of R.F. and baseband subsystems and the channel filters, the reduction of size of a D.C. receiver is quite important. Superheterodyne receivers need the narrow bandpass filter (quartz or ceramic filters) which are voluminous and expensive if high quality is demanded). The size reduction of a superheterodyne versus D-C, conversion is of 60-70 % more or less. Nevertheless that reduction of size is possible if all the subsystems of the receiver are integrated, that is not always possible, specially the integration of the low-noise amplifier.

c) D-C techniques always offer a dramatic reduction of power consumption. The consumption of a D-C receiver usually is four or five times lower than a superheterodyne receiver. Obviously, the dynamic range of these receivers is not very high, so an Automatic Gain Control is a must if high performance is required. It is possible to avoid the use of A.G.C. for B.F.S.K. applications such as paging if the requirements are not very hard. In this case is essential a high dynamic range baseband processing circuits.

d) Cost. In a general way D-C receivers may be cheaper than equivalent superheterodyne of similar performance due to D-C receivers use less parts. The most expensive component of a direct conversion receiver is the integrated circuit and the precision crystal quartz. By other hand the most expensive

parts of superheterodyne receivers are usually the bandpass filters (if a crystal filter is used), integrated circuits for P.L.L. (if used) and work force. But if the application of the customer does not justify making its own integrated circuits and depend on external suppliers, this paragraph must be reviewed. In such a case superheterodyne topology is less sensible to market fluctuations.

Table Cost comparasion betwen D-C and Sphet.

ITEM	D-C	Superhet
Discretes	1/5	1
Monolithics	1	1/6
XTAL	1	1/6 or 1
P.C.B.	9/10	1
Manufact.	1/2	1

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DESIGN S-BAND PLL SYNTHESIZED LOCAL OSCILLATOR UTILIZING CAD.

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The Microwave Multi-point Multi-Channel Distribution System (MMDS) is a method in which traditional CATV Channels are transmitted via Microwave Wireless equipment at an assigned S-band frequency (2500-2700 MHz). The technique is very attractive for countries were DBS or CATV infrastructure does not exist or is too expensive.

The transmitter [1] is basically an upconverter and an amplifier, where the modulated TV channels (200-400) spaced at 6 MHz for the PAL system are upconverted to the 2500-2700 MHz band. The S-band signal is then amplified up to 100 Watt/channel, and is fed to an antenna mounted on a high building in the center of populated areas. One of the key components in the transmitter is the synthesized Local Oscillator (LO) which is used to up-convert the VHF channels to the S-band. This article will attempt to detail a novel method which engineers can follow in designing an LO, utilizing previous technical articles, software and off-the-shelf components available from several RF and Microwave manufacturers.

The targeted specifications are as follows:

LO Level = 9 dBm ± 1 dBm
Frequency output = 2260-2302 MHZ by steps of 6 MHz
Operating Temperature -30 to +50 C.
Frequency stability is ± 500 Hz.
Spur level ≤ -60 dBc
Reference frequency is 10.00 MHz
Phase Noise performance is -94 dBc/Hz @ 10 KHz and -70 dBc/Hz @1 kHz.
additional requirements is that the parts be a common off shelf components. The programming of the synthesizer must be done via hand setting of dip switches to avoid the use of a Microcontroller. As part of a diagnostic system for the complete transmitter, the LO must supply a flag to indicate a locked

condition and also avoid transmitting while not locked to the correct frequency. In addition, a DC- Signal proportional to the LO's RF level at the output is supplied.

The Synthesizer Topology Design:

The simplest and least expensive topology which will meet the requirements listed above is to use the single Loop design as shown in figure-1A. Here, the VCO is running at the desired LO frequency. This is used in conjunction with a cascaded prescaler feedback network which will bring the VCO's frequency down to the range of an PLL IC (10-20 MHz). A VCO capable of running in the range of 2260-2302 MHZ is available from sources such as Z-comm, CA. First, the LO is divided by four using Prescaler UPB582 (NEC, CA), yielding a frequency output of 565-575 MHZ. This output is then level-shifted and scaled again using a dual modulus prescaler MC22022A (Motorola, AZ) with division ratio of 64/65 yielding 8.8-8.9 MHZ. The level is shifted again to feed the PLL chip MC145152 (Motorola, AZ). The PLL synthesizer chip has a Phase detector, a lock detector indicator which goes high as soon as the VCO gets locked in phase and frequency, and two frequency dividers.

The first divider labeled as R is the Reference frequency divider; its division ratio can be programmed via bits RA0-RA3. The second divider is the feed-back divider; its division ratio can be programmed to via the bits N0-N9. Also included is the Dual modulus divider required to toggle the 64/65 prescaler; the toggle control is from the A-counter inside the PLL chip via bits A0-A5.

The VCO output is isolated from load variations by the use of a resistive pad with an attenuation of 10dB. The output is level shifted to supply the desired 9 dBm output. Edge coupled Microstrip line couplers are constructed to implement two 10 dB directional couplers. One is used to sample the VCO output for the feed back loop. The other is used to supply a sample of the RF output to an envelope detector. The envelope detector uses a diode with very low forward voltage to convert the RF level to a DC signal, which then can be buffered and used as a diagnostic measure to indicate that the LO RF level is properly working. Both couplers should not have more loss than 1-dB. The coupler design procedure is a simple and straight forward [3] and also

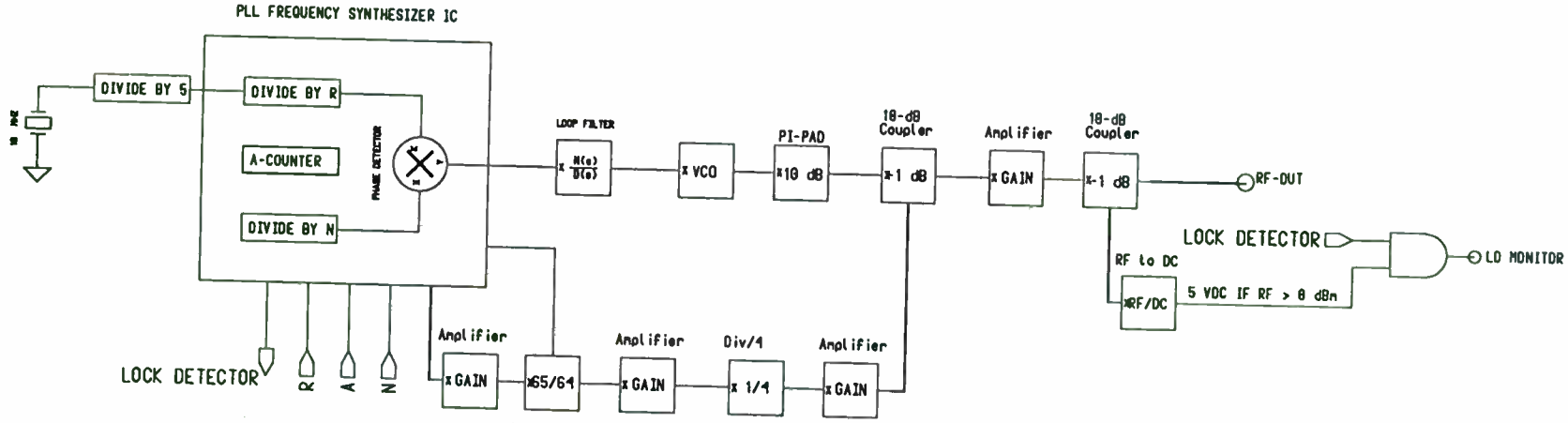

Figure-1A: The Phase Locked Synthesizer System.

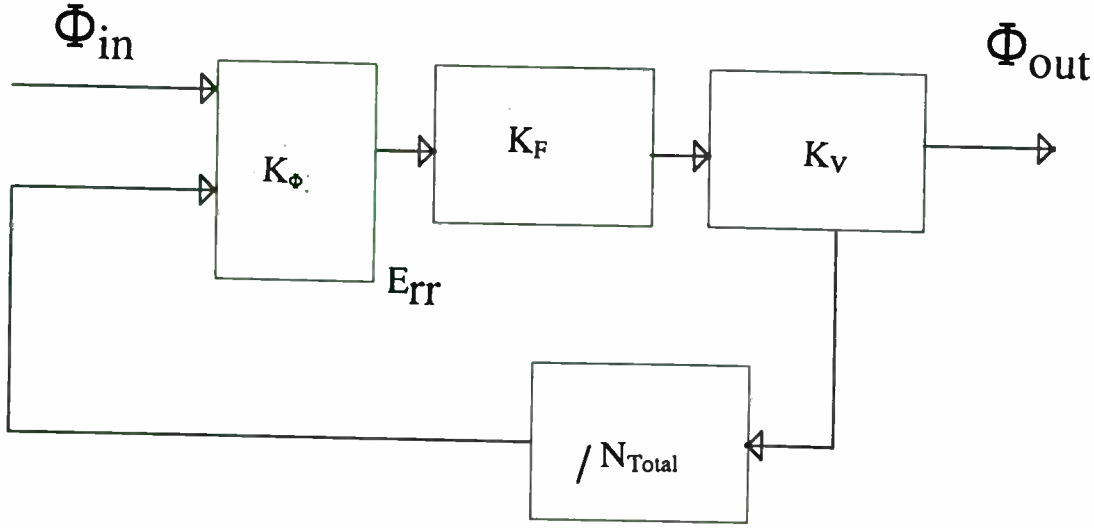

Figure-2: System Block Diagram used to model the Loop.

available as WirePack from Sage Laboratories, Inc (Natick, MA) or as a surface mount from Anaren Microwave Inc. (Syracuse, NY).
To assure a good isolation between the LO port on the mixer/up-converter and the IF port a ferrite isolator with 1 dB loss and more than 28 dB of isolation is used. This can be any drop-in Isolator, such as that supplied by Renaissance Electronics Corp (Boxborough, MA).

Frequency Synthesis:

The first thing we need to do is to determine the phase detector frequency which will allow us to increment the LO by 6.0 MHZ channel steps as necessary, while utilizing the defacto broadcast standard of 10.00 MHz as a reference. For example, we will attempt to synthesize 2278 MHz from a divided ratio of the reference 10.0 MHz. The reference divider R inside the PLL chip allows us to divide by 8, 64, 128, 256, 512, 1024, 1160, 2048. Inspecting these values would lead us to the conclusion that there is no way to synthesize the LO at 6 MHZ steps while utilizing the 10.0 MHz reference.

If the reference is 1.0 MHz, however, then it is feasible. We can utilize the an external divide-by-10, Model SP8799 which is available from GEC-Plessey. Essentially, we still utilize the standard 10 MHz crystal which is less expensive and readily available from several sources, such as the model ER7501 from Electronic Research CO. (Overland Park, KS). Some recent PLL IC chips do offer more possible division ratios for the R-register than the MC145152, but do not offer the luxury of being programmed in parallel as is the case with our current design. The model 145190/91 has a range for the R division ratio of 16-bits, giving divide ratios from 5 to 8191. The only problem with using this chip is that a microprocessor interface or a fairly complex sequential timer-parallel-in-serial out circuit programmer needed. This may not work for us since we would like to keep the system very simple and be able to program it via a set of on/off dip switches which will supply the parallel word.

Using an external divide by 10 the reference is 1.0 MHz. The divide ratio of 8 yields a phase detector frequency of 0.125 MHz, which is the correct frequency to synthesize the LO to 2278 Mhz. The channel spacing now is four times that value or 0.5 MHz. Another combination which has worked well is to use an external prescaler of divide-by-5 (Model SP8740, Plessy),

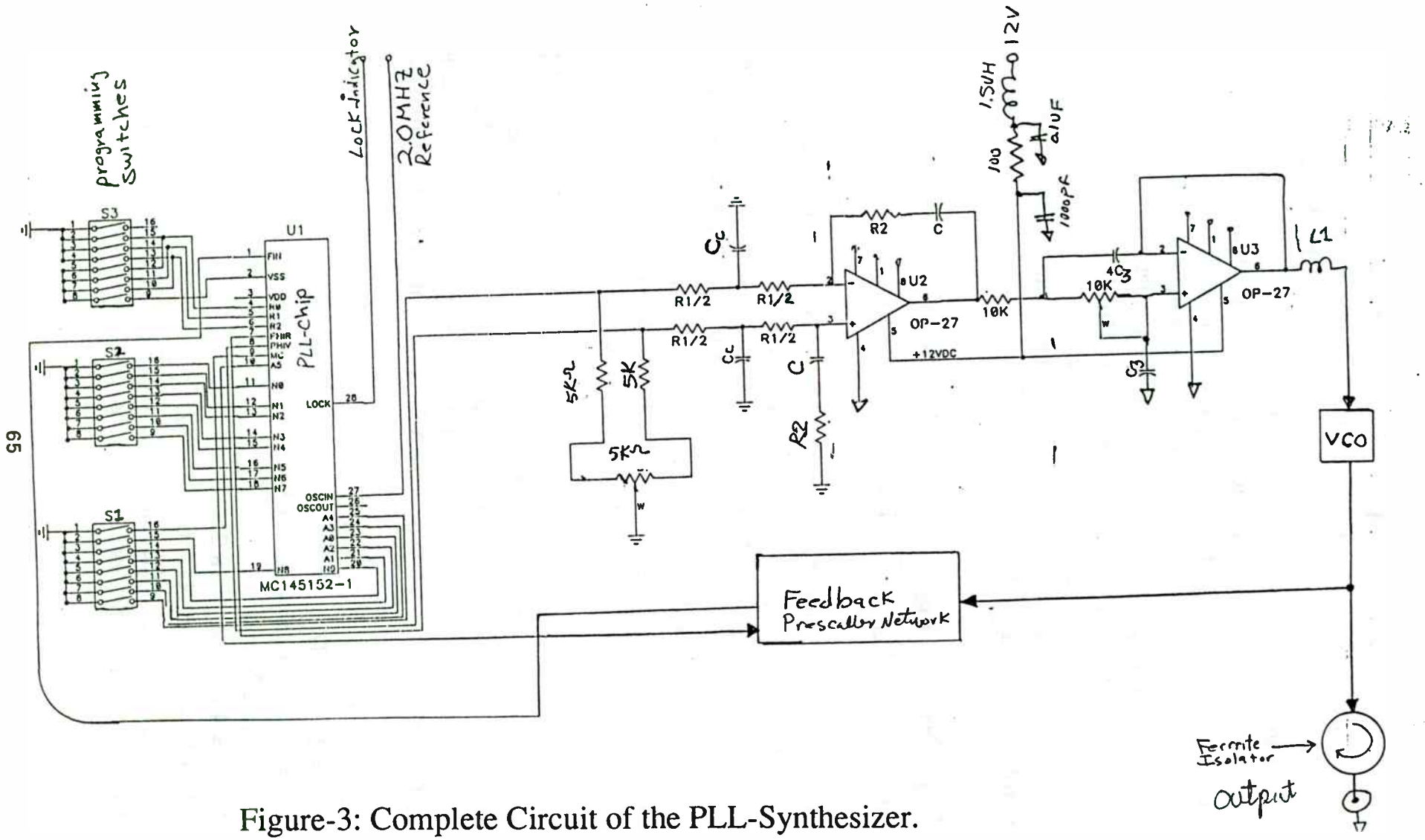

Figure-3: Complete Circuit of the PLL-Synthesizer.

yielding a reference of 2.0 MHz. The ratio of the internal divider would then yield a phase detector frequency of 0.250 MHz. Hence, channel spacing at this point would be four times that value or 1.00 MHz. We choose 250 kHz simply to allow us to have a broader loop bandwidth. This is useful for the purpose of combating Microphonics which can get induced into the VCO circuit. The binary word needed to program the PLL IC with an R-divide ratio (RA0-RA2) of 8 is 000 binary [2]. This can be physically implemented by pulling down pin 4,5, and 6. With the phase detector frequency set to 0.250 MHz we can proceed to show the mathematical algorithm to come up with the required values for the N and A registers of the PLL's internal prescalers. The output frequency from figure-2 can be shown mathematically to follow the relation :

$F_{out} = N_{Total} \times F_{Ref}$ Equation-1

where $F_{Ref} = F_{crystal}/R$ is the Phase detector comparison frequency.

Where F_{out} is the output frequency in MHz . N_{Total} is the total division ratio in the feed back loop prescaler chain which is $N_{Total} = 4(64N+A)$ Where N and A are the division ratio programmed in the N and A dividers inside the PLL and can be programmed via pins N0-N9 and A0-A5 respectively. The value 64 is the P-value of the dual modulus prescaler. F_{Ref} is the phase detector frequency resulting from the R-Divider which is used to divide the Ovenized Crystal Reference oscillator and can be programmed for the division value via pins RA0-RA3. The channel spacing will be $4x\ F_{Ref}$ or in our case would be a 1 MHz steps. It is worth noticing here that the Channel spacing, unlike a conventional PLL synthesizer, is not the same as the Phase detector Frequency, but always four times that. This is due to the fact that the output is always divided by four before it gets synthesized inside the loop. Let's show how the value of 2278 MHz gets synthesized and programmed :

F_{Ref} = 250 kHz or 0.250 MHz
F_{out} = 2278 MHZ
$F_{out} = N_{Total} \times 0.250 = 2278$ MHZ
N_{Total} =18,224 and
$N_{Total} = 4(64N+A) = 18,224$
$64N+A = 4,556$ or $N+A/64 = 71.1875$
Now the N-divider is the integer value of 71.1875 and the A/64 is the Decimal portion. So N=71 and A/64 =0.1875 or A= 12.

Now we need to convert to binary the value 12 and the value 71. N= decimal 71 and = 0001000111 for the 10-bit divider to be programmed via pins 11 through 20 of the PLL-IC. A=12 or 001100 for the 4-bit long word needed for the A-register to program the A-counter via pins 21 through pin 25.

With a simple Excel or MS-Basic program and using the above equations one can construct a table for the N and A registers values needed to program each channel. Figure-3 shows the complete synthesizer circuit, notice that binary ones are implemented by an open pin, because the device has an internal pull-up resistor. The Binary zeros are implemented by pulling the pin to ground as shown in figure-3.

Loop Filter Design:

One of the important sub-systems of the PLL-Synthesizer is the design of the loop filter. The filter circuits have been investigated by a number of people. The design methodology is well established in previous works [10],[4]. The loop is the main factor contributing to the stability of the synthesizer, the loop bandwidth and the switching speed, the spur level introduced by the reference and other close-in spurs (i.e. switching power supply frequency spur, harmonics of the phase detector frequency spur, the dual modulus 64/65 spur, and the divide-by-five spur). The reason that the loop filter is so important in limiting the above spurs is basically because the loop filter drives the varactor diodes. Any amount of AC signal leakage in addition to the error signal will make its way to the varactor and modulate it, resulting in a double side band spur at the frequency of the AC signals. Meanwhile, if we limit the loop bandwidth to cut off those leakages we may not be able to synthesize and reject phase noise close-in to the carrier.

Another disadvantage with narrowing the loop filter is the loss of Microphonics rejection. Microphonics power spectra tend to be from a few 100 Hertz to 10 kHz. So, the wider the loop bandwidth, the faster the system response is and therefore the more rejection of microphonics. A very careful design procedure has to be followed to assure a good compromise between Loop Bandwidth and switching time, canceling phase noise of the LO within the loop band width, and the spur levels.

If we approximate the synthesizer system as a second order loop filter as that shown in figure-2 Where

K_V = The Gain of the VCO Radians/seconds/volts.

K_F = The Transfer function of the loop filter.

K_Φ = The gain of the PLL phase detector and usually is given by

For single ended Phase detector = $Vdd/2\pi$ Volts/Radians

For double ended phase detector = $Vdd/4\pi$ Volts/Radians

where Vdd is the phase detector DC-power supply value.

To start coming up with the design values for the loop filter one needs to determine the gain of the VCO, which is mainly controlled by the capacitance ratio of the varactor. Gain of the VCO is given by :

$$K_V = 2\pi \frac{\text{Upper Frequency} - \text{Lower Frequency}}{\text{Varactor Tuning Range}}$$

and the $$\frac{\text{Upper Frequency}}{\text{Lower Frequency}} = \sqrt{\frac{\text{Upper Varactor Capacitance}}{\text{Lower Varactor Capacitance}}}$$

Let's define the VCO as an integrator of a transfer function of (K_V/S) since really the VCO is an integrator for the Phase error with one pole at the origin. From figure-2, if we write an equation relating the output Phase signal to the input Phase signal we would get the transfer function of the PLL system. We can use it to come up with the design values for the loop filter and reference spur filter.

Φ_{in} = input phase signal to the phase detector .

Φ_{out} = output phase signal.

E_{rr} = Error output of the phase detector .Then by inspection of figure-2

we can write: $\Phi_{out} = E_{rr} K_V K_F / S$ Equation -2

$E_{rr} = [\Phi_{in} - (\Phi_{out} / N_{Total})] K_\Phi$ Equation-3

substituting equation-3 into equation-2 and substituting the transfer function of the VCO as single pole at the origin with its gain K_V results in

$$\Phi_{out} = K_V K_F K_\Phi / S [\Phi_{in} - (\Phi_{out} / N_{Total})] \qquad \text{Equation-4}$$

Rearranging equation-4 the open loop transfer function

$$\Phi_{out}/\Phi_{in} = \frac{K_V K_F K_\Phi}{S + (K_V K_F K_\Phi / N_{Total})} \qquad \text{Equation-5}$$

The loop filter in figure-3 is made of three parts. The loop error integrator, the Sallen-Key low pass filter which assures enough suppression of the reference spur at 250 kHz, and an additional low pass filter resulting from the capacitance of the varactor and inductor L1.

Let's assume for simplicity the model is a second order loop and that the contribution of the additional low pass filters are minimal in the overall transfer function. This should be a valid assumption since the loop bandwidth will be as high as 1000 HZ and that is well below the 250 KHZ cut-off frequency of the combined response of these Sallen key and the L1-Varactor Capacitance Section. Of course, we are assuming that the response of these filters are flat within the loop bandwidth, which really it is. Later, all of these assumptions will be verified when we model the complete loop using CAD tool. The stability, overshoot and switching time will be verified. The extent of the contribution of the ignored Low pass sections will become apparent.

For now, to design the loop filter we will just assume the Differential Loop Integrator shown in figure-3. Usually the loop integrator has only one resistor R1 in its input path. However, splitting the resistor and adding a capacitor C_c will tend to smooth the error pulses, thereby eliminating the high frequency portion of the error pulses which is also where most of the Reference harmonics content are. Also some times the error pulses would tend to have an imulse signal which may cause the Opamp to saturate unless C_c is used.

Another thing we might simplify and assume ideal is the Transfer function of the internal dynamics of the opamp and the finite delay in the Phase detector which can be a Gaussian distributed with its mean at the half period of the

phase detector comparison frequency. The simple model would work well as a starting point for the CAD optimization model. However if the synthesizer has a very wide loop bandwidth we can no longer ignore the effect of the Opamp, the finite delay in the Dividers and the phase detector.

The transfer function of a simple RC integrator is

$$K_F = \frac{1 + R_2 C S}{R_1 CS} \qquad \text{Equation-6}$$

Where R_2, C, and R_1 are the designations of the components shown in figure-3.

Now substituting the value of K_F of equation-6 into Equation-5 results in the famous second order Laplace control theory equation describing a system with a damping factor ξ and some resonance frequency is given by ω_n or

$$\Phi_{out}/\Phi_{in} =$$

$$\frac{K_V K_\Phi (1/C R_1)(1 + C R_2 S)}{S^2 + R_2 C (K_V K_\Phi / C R_1 N_{Total})S + K_V K_\Phi / C R_1 N_{Total}} \qquad \text{Equation-7A}$$

which is in the form of the classical formula of

$$\Phi_{in}/\Phi_{out} = \frac{K}{S^2 + 2\xi \omega_n S + \omega^2_n} \qquad \text{Equation-7B}$$

The values of the damping factor and the natural resonance of the internal structure of the system can control the systems response to an input by controlling the location of Poles and Zeros on the Root Locus of the transfer function [5]. This will also define the system's settling time, and overshoot level. Overshoot can be harmful in some cases where it forces the loop filter (i.e. controller of the system) to saturate to infinity (in our case the Op-Amp would saturate for a finite period to either the upper or lower rail). This would result in an unexpected delay in the system response, due to the time it takes the system to discharge the extra energy resulting from the overshoot, which is the result of trying to respond too fast. So as we can see there is a

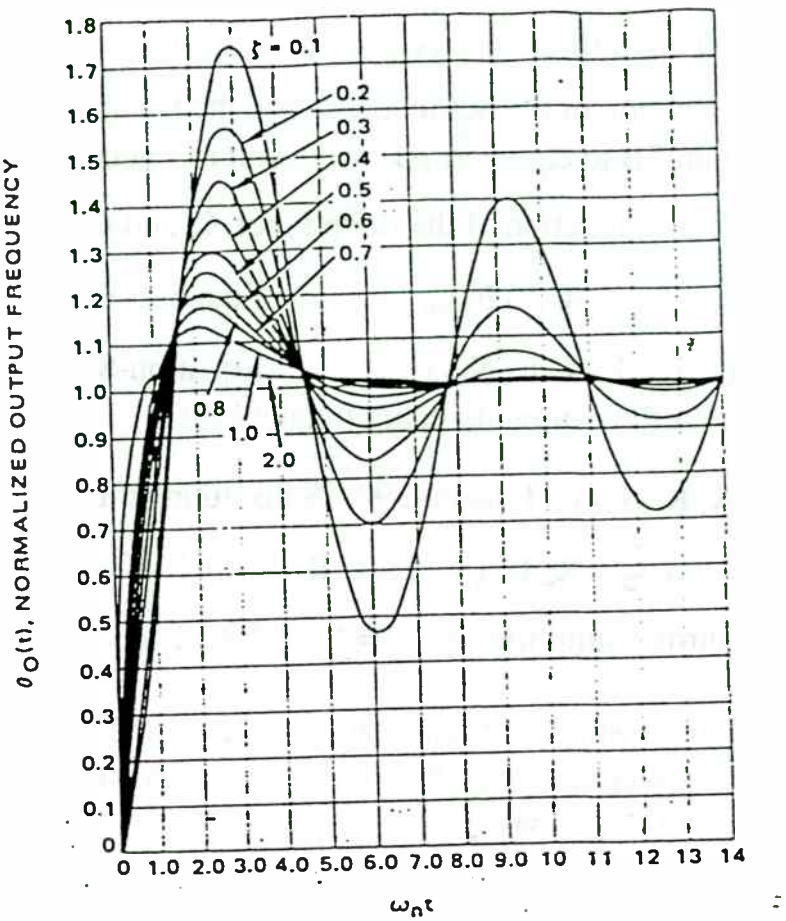

Figure-4: Type Second Order Step Response.

tradeoff between all of these factors. Figure-4 shows the normalized output frequency as a function of the Settling time and the Damping factor ξ. Equating equation-7B to equation 7B will result in a generic formulas for the system behavior as a function of the Loop Filter ξ and ω_n.

We have $\omega^2_n = K_V K_\Phi / C R_1 N_{total}$ Equation-8A

$2 \xi \omega_n = R_2 C (K_V K_\Phi / C R_1 N_{total})$ Equation-8B

from equation-8 A the natural damping frequency is

$\omega_n = \sqrt{K_V K_\Phi / C R_1 N_{total}}$ Equation-9A. Substituting this value in Equation-8B gives $\xi = R_2 C (K_V K_\Phi / C R_1 N_{total}) / 2 \sqrt{K_V K_\Phi / C R_1 N_{total}}$

Which can be further simplified to $\xi = R_2 C \omega_n / 2$ Equation-8B

The loop bandwidth which is not the same as the natural damping frequency can be found by taking the magnitude of Equation-7A and equating it to 0.5 (i.e. equal -3.0 dB) and given by

$$W_{3db} = \omega_n [1+2\xi^2+\sqrt{(2+4\xi^2+4\xi^4)}]^{1/2} \qquad \text{Equation-8C}$$

Notice that ξ and ω_n are a function of the loop filter components C, R_1, and R_2, but also a function of the total division ratio in the feed back or the total prescaler division ratio which is in this case is $N_{Total} = 4(64N+A)$. So the value of ξ and ω_n will vary as we vary the division ratio. The extent of this is that the loop dynamics will change each time we synthesize a new frequency. So the desired value of ξ and ω_n can be assumed at the midband and the geometric mean of N_{Total} then the loop response can be studied as we vary N_{Total} in response to changing the frequency from the lower desired LO frequency to the Upper desired LO frequency. One way to hold the ξ and ω_n constant would be to vary the Loop integrator components to equalize the effect of changing N_{Total}, but this would require some voltage variable resistors and capacitors. This method has not been been explored to any extent.

Another method would be to implement the loop filter via a Digital Signal Processing techniques, an area known as the Digital Control theory, where the loop filter is an adaptive Z-transform of the lumped element equivalence. The system's phase detector signal would be digitized using an A/D. The data then gets manipulated by the Digital loop filter, after which a D/A would put it back on the tuning line. This method had been implemented by several people, but for us it is not feasible from an economical aspect. Using equation 8 and Figure-4 and the frequency synthesis values of N_{Total} derived earlier for the LO output at 2278.00 MHZ. We can proceed designing the loop filter.

N_{total} = 18,224
K_V = (Δ Fvco output/ΔTuning voltage) 2π
= (2300 Mhz-2200Mhz)/(10-2) 2π Radians/second/volts
= 75 x 10^6 Radians/Second/Volts
K_Φ = Phase detector Power Supply/2π Volts/Radians
= 0.796 Volts/Radians for a supply voltage of 9.0 Volts.

Using Figure-4 let's pick an over shoot value of 20 %, then the value of ξ is roughly about 0.8. From the figure $\omega_n t$=5.5.
Now here we have no requirements on the switching speed, since this synthesizer gets set by hand and stays at that specific channel. So let's pick the value of the settling time as 8.0 milli-seconds.

Then $\omega_n t$=5.5 which yields a settling to 5% of the steady state response.

with t= 8 x 10^{-3} seconds ω_n = 687 Radians/seconds. Solving Equation-9B for $\xi = R_2 C \omega_n /2$ = 0.80 yields $R_2 C$ = 0.00232727. Solving Equation-9A $\omega_n = \sqrt{K_V K_\Phi / C R_1 N_{Total}}$ = 687 yielding $C R_1$ = 0.007065

Since usually resistors are available at 1% values and Capacitors have less flexibility on the available parts let's choose the value of C to be equal 1UF. Then R_1 = 7.0 K Ω and R_2 = 2.2 K Ω

One way to predict the change in the loop behavior is to find the range at which ξ and ω_n can be. Since we have

$N_{total\ maximum} = F_{out\ Maximum} / F_{Ref}$ Equation-9

$N_{total\ minimum} = F_{out\ Minimum} / F_{Ref}$

Now substituting equation-9 into Equation-8 yield the range of ω_n.

$\omega_{n\ minimum} = K_\Phi/C\ R_1\ (F_{out\ Maximum} / F_{ref})$ Equation-10

$\omega_{n\ maximum} = K_\Phi/C\ R_1\ (F_{out\ Minimum} / F_{ref})$

and alternately $\xi_{minimum} = R_2\ C\ \omega_{n\ minimum}\ /2$ Equation-11

$\xi_{maximum} = R_2\ C\ \omega_{n\ maximum}\ /2$

From Equation 10 and 11 one can predict the worst case performance of the system in term of the overshoot value, the loop bandwidth and hence the worst case of the reference level. Also the switching time, which is dependent on the loop bandwidth, can be predicted as well. Later we will see that by using a CAD graphical modeling of the PLL Loop we can easily verify the above much more easily and with out the use of complicated Mathematical equations.

As we mentioned earlier we can split R_1 to two halves and then insert a capacitor. This will tend to smooth the transient of phase detector pulses before they propagate to the VCO, in turn modulating it at the reference frequency of 250 KHZ. The value of the inserted capacitor C_c is chosen in such a way to place a pole that is at least ten times the 3dB loop bandwidth as was defined in equation-8C. So

$C_c\ R_1\ /2 = 10/F_{3dB}$ or $C_c = 0.18UF$

For further attenuation of the reference level spur we can incorporated the Sallen-Key low pass filter shown in figure-3. The design is simple and detailed in several articles and text books [2]. one quick method is to assume the value of R3 to be between 1K to 1000 K Ω and then letting C4=4C3. The value of C3 is then chosen so the filters cut-off frequency is ten times the loop Bandwidth.

$$C3 = \frac{0.1}{\omega_{3dB} R}$$

Yielding C3=0.018UF, C4= 0.047UF, while assuming R3=10 KΩ

If the suppression of the reference frequency is still to be attenuated more we can use a higher order low pass filter. where the attenuation of the reference level as a function of the low pass filters order is

$\alpha_{\text{Side-Band}} =$

$20n\ \text{Log}_{10}(\omega_{LP}/2\pi F_{ref})$ dB. Equation-13

Where n = the low pass Filter order.

PLL Computer Model:

Since we have made a few assumptions on the system and reduced the order to a second order system, we must demonstrate by the use of CAD-simulations that the model is somehow close to that predicted by the simple second order solution above. A process of trial and error or CAD optimization will be conducted to overcome any unexpected behavior of the loop. This process can be easily implemented by Pspice or using EESOF/HP-MDS software. Figure 5A shows a model using the Pspice. The detail of the model can be obtained from [10]. Figure 4B Shows the Results of both transient response of the loop to a step in frequency and the simulation of the Gain Margin and Phase Margin. The Model that is presented implements the VCO as a Laplace block with one pole at the origin. The opamp can be modeled by a Laplace function with its transfer function given by :

$$H(s)_{OpAmp} = \frac{A_o}{1 + S(A_o/2\pi GBW)}$$

Where A_o is the Large signal voltage gain and GBW is the Gain-Bandwidth product. Both parameters are usually specified by the manufacturer. For the OP-27 model available from Analog Devices (MA). The $A_o = 2x10^6$ and GBW is 8 MHz.

The delay in the phase detector is usual a fraction of the Phase detector's period. Its magnitude can vary from zero to being complete cycle. The phase detector can be modeled as a Laplace block with its gain given as $Vdd/4\pi$ times the delay of the period of the phase detector's frequency. or

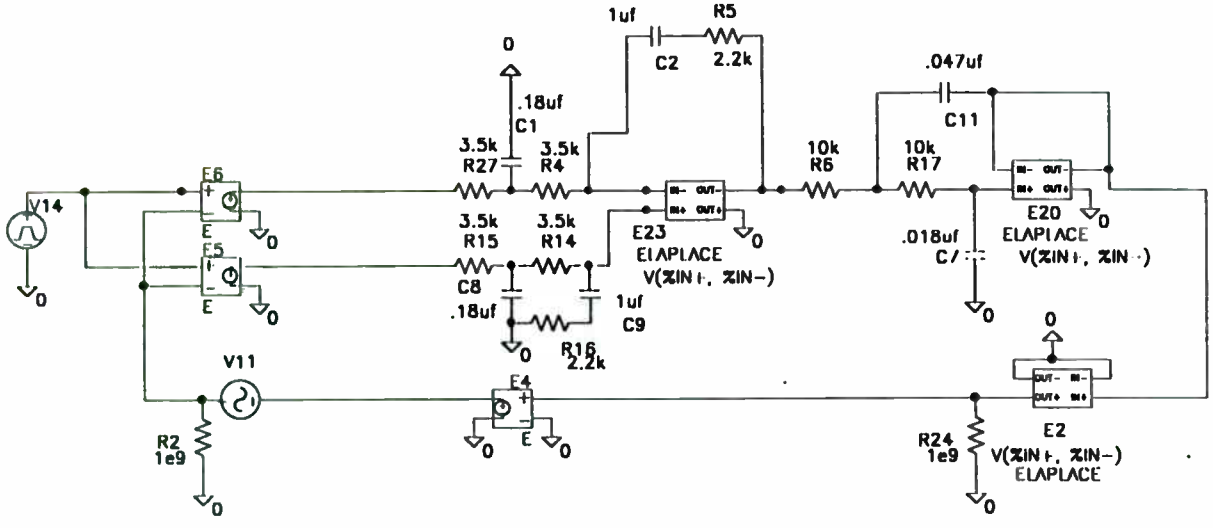

Figure-5A: A Pspice Loop Model. V11 used for Gain and Phase Margin. V14 is used for the Switching Response.

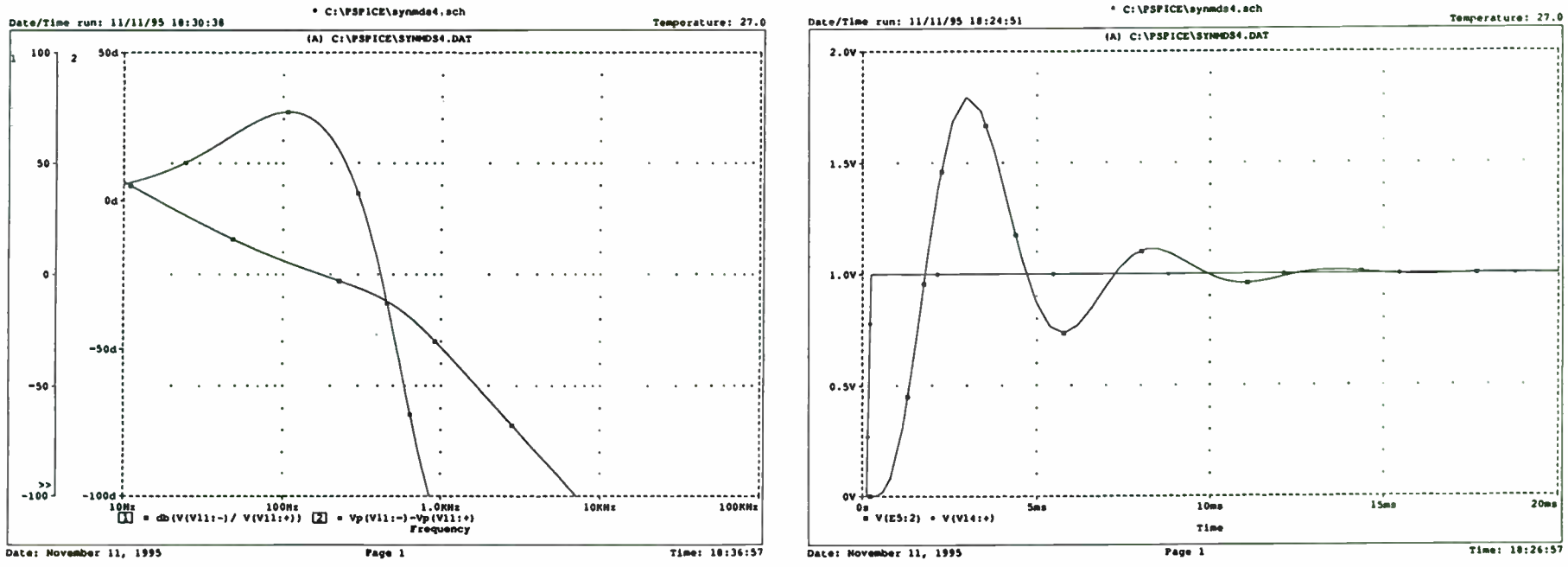

Figure-5B: Phase/Gain Response (Left), Switching response (Right).

$F_{phase\text{-}det} = K_\Phi U(t+1/2\pi F_{ref})$ for $t \geq 0$, where $1/2\pi F_{ref}$ is the time delay and U is the unit step function.

So the phase detector can be modeled by the Laplace of the above time equation with its transfer function given by:

$$H(s)_{phase\text{-}detector} = K_\Phi / \exp(S/2\pi F_{ref}).$$

The Phase and Gain Margin results can be obtained by taking the AC-response ratio of the Loop. The switching time can be viewed by probing the error signal at the output of the Phase detector output. Notice that the gain and phase margins in figure 4B have not satisfied the 45 degrees merit figure commonly used as a Phase margin at the zero dB crossing frequency. Obviously at this point we must go back and redesign the Loop integrators. Or yet simply have the computer do the job by running the optimizer with the condition of Phase Margin is greater or equal to 45 degrees.

VCO Design:

Most VCOs for the Frequency region of 400-4 GHz tend to be a BJT type devices with common base is the most common configuration. FETs which are highly desirable at VHF are of no use in this band [9]. So a common Base transistor Oscillator was utilized here. The oscillation is controlled by a combination of LC-type resonator. The inductor will be implemented by the use of a Shorted piece of Microstrip Transmission Line. The Varactor can be any of the common devices from Loral or Metalics. The design of the Resonator is fairly simple at the start, but then the Microstrip line in practice has to be trimmed experimentally to over come the parasitic and effects of the ground vias. The design of the inductor is derived from the theory of the input impedance of a transmission line given by:

$$Zin/Z_o = \frac{Z_L + jZ_o \tan \beta d}{Z_o + jZ_L \tan \beta d} \qquad \text{Equation-14}$$

where βd is $2\pi d/\lambda_g$ is the electrical length of the line and λ_g is the wavelength in the Microstrip line and $\lambda_g = \lambda_o / \sqrt{\varepsilon_{reff}}$,

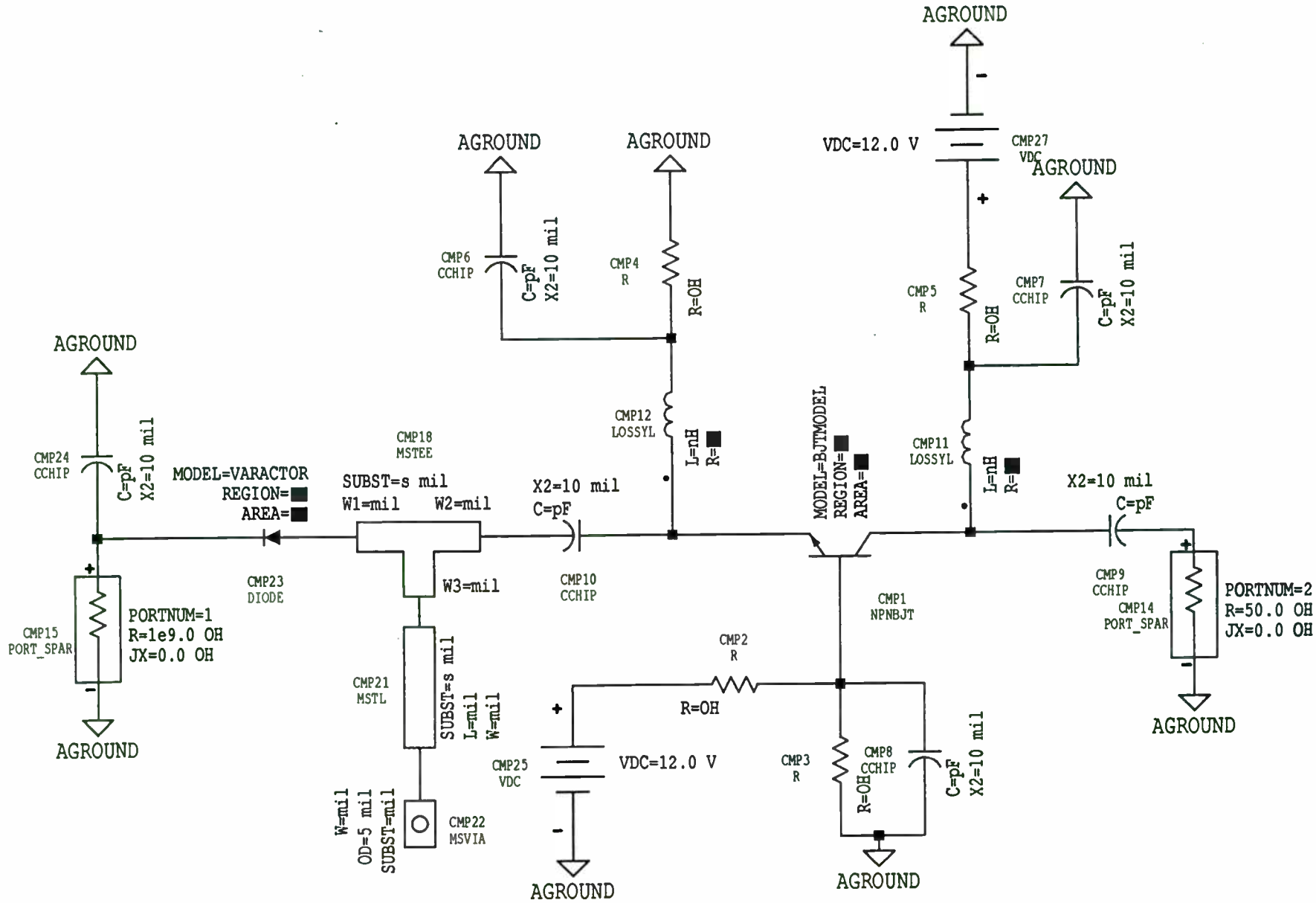

Figure-6: The VCO Model using HP-MDS.

ε_{reff} is the effective electrical permitivity of the board material.

$$\varepsilon_{reff} = \frac{\varepsilon_{r+1}}{2} + \frac{\varepsilon_{r-1}}{2} \left[((1+12h)/ W_e)^{-1/2} + 0.04(1-W_e/h)^2\right]$$

d is the physical length of the printed microstrip inductor and λ_o is the wavelength of the frequency in free space [3]. Z_o is the characteristics impedance of the transmission line. For microstrip lines it can be found by

$$Z_o = \frac{120\pi/\sqrt{\varepsilon_{reff}}}{[(W_e/h) + 1.393 + 0.667\ \mathrm{Ln}((W_e/h) + 1.444)]} \qquad \text{Equation 15}$$

$$W_e = W+(t/\pi)[\mathrm{Ln}(2h_e/t) +1]$$

$$h_e = h-2t$$

W/h is the width to height ratio of the Microstrip line. Equation-15 is only valid for impedance's where W/h ≥ 1. Since an inductors impedance is of the form +jx Then equation 14 has to have Z_L zero (short terminated stub) in order to implement an inductor equivalence. equation 14 becomes

$$Zin= + jZ_o\tan \beta d = +jX = j2\pi FL \qquad \text{Equation-16}$$

Now given the capacitance of the Varactor at the geometrical mean of the frequency band whose wave length in the board materiel is known also. The frequency of oscillation will be

$F_{oscil} = 1/2\pi \sqrt{LC}$. The length of the resonator Microstrip inductor can be found from the relation $+j2\pi FL= jZ_o\tan \beta d$.

Phase Noise performance:

The Phase noise of a free running oscillator had been analyzed by Lessons [2]. and given by

$$\pounds(F) = \qquad \text{Equation-17}$$
$$10\,Log_{10}\{[1+F_o^2/(2FQ)^2](1+F_c/F)\digamma KT/2P_s+2KTRK_o^2/F^2\}\ dBc/Hz$$

Where:

$\digamma$=Noise Figure of the active device

K_o= Oscillator voltage gain

P_s = Average power at the Oscillator input.

R= Equivalent Noise Resistance of the Varactor diode.

F= Noise Factor

F = Frequency offset .

F_o = Carrier Frequency.

F_c = Flicker Frequency of the BJT Device.

Q = Loaded Q of the tuned LC-Resonator.

KT= 4.1×10^{-21}

By inspection of Equation-17 it may be seen that the phase noise is proportional to Q^{-2} and F^{-2} , which means that for every octave decrease in the offset F the phase noise power will increase by 4-times or at 6 dB/Octave. Another factor in the phase noise contribution is the Noise figure of the device, the Flicker noise or 1/F for close-in offsets, the AC swing of the signal on the LC-resonator. But by far the most improvement in the oscillator's control over phase noise can be done through a careful design of the loaded Q of the resonator circuit. Varactors usually can be obtained with Q of 1000-4000 which is enough. But to obtain a high Q from the Microstrip Inductor we must design the printed inductor carefully or use a Ceramic or Dielectric resonators which for our current application is too expensive. The unloaded Q of a microstrip line is given by:

$$1/Q_{unloaded} = 1/Q_{dilectric}+1/Q_{radiated} +1/Q_{Conductor} \qquad \text{Equation-18}$$

$$Q_{radiated} = \frac{Z_o(F)}{480\pi(h/\lambda_o)^2\{((\varepsilon_{reff}(F)+1)/\varepsilon_{reff} - [(\varepsilon_{reff}(F)-1)^2/2\varepsilon_{reff}(F)^{3/2}(Ln(\sqrt{\varepsilon_{reff}}+1)/(\sqrt{\varepsilon_{reff}}-1))])\}}$$

where $Z_o(F) = Z_o[(\varepsilon_{reff}/\varepsilon_{reff}(F)]^{1/2}$

and $\varepsilon_{reff}(F) = \varepsilon_r - \frac{\varepsilon_r - \varepsilon_{reff}}{1+G(F/F_p)^2}$

$F_p = Z_o/8\pi h_e$

$G = 0.6 + 0.009\, Z_o$

Where F_p is the cut-off frequency of the next higher order propagation mode.

$$Q_{dilectric} = \frac{27.3}{\alpha_{dilectric}}$$

$$\alpha_{dilectric} = 27.3\{(\varepsilon_{reff} - 1)/(\varepsilon_r - 1)\}(\varepsilon_r/\varepsilon_{reff})(\tan\delta/\lambda_g)$$

Where tan δ is the tangential loss of the Microstrip substrate and usually specified by the manufacturer.

$$Q_{Conductor} = 4780\, h\sqrt{F}$$

Where h is the substrate height in cm and F given in GHz. By inspecting the above equations for the unloaded Q of the Resonator Inductor which is a main contributor to the Phase Noise power as seen in Equation-17, to maximize the Q of the Inductor we need to have less radiation loss, less dielectric loss, and less conductor loss. After one comes with the required length d and width of the Microstrip line needed for the center frequency, a process of optimized by HP-EESOF MDS may improve the speed of the design.

VCO Computer Model:

The way to simulate the Oscillator is described in [6]. Basically the Active device is a negative resistance device. by shunting the Resonator with the active device and looking at the Input Scattering parameters S11 of the combined parallel combination of the Resonator and the Active device. The value of the Resonator's impedance cancels the input impedance of the device and results in oscillations or S11 greater than 1 . After the first few cycles of oscillation the process can no longer be assumed linear and the MDS analysis of the Oscillator can no longer apply. Usually Harmonic balanced analysis is valid after that. MDS-HP (Palo Alto, CA) simulations are excellent at least to optimize the Microstrip inductor and the load matching. For the varactor, substituting a capacitor with values corresponding to the upper and lower Varactor values and with the inductor at the length and width found from Equation-16 and then sweeping the Oscillator and looking at S11 [6]. The frequency where S11 is maximum and where the reactive impedance crosses the zero ohms is the frequency of oscillation. The value of the fixed cap across the Inductor can be swept in range to emulate the varactor capacitance curve. A process which should be able to tell the gain and range of the VCO design. The optimize program can also be used to optimize the Active circuit's matching for a given varactor. Some flexibility has to still be there to able the designer to trim the length of the Microstrip line.

Phase Noise Measurements:

The phase noise of the PLL synthesizer can be divided to three regions. The first is the Phase Noise for offsets less than the closed loop bandwidth, for frequency offsets greater than the closed loop bandwidth and up to several 100 kHz, and offsets larger than several 100 kHz to greater offsets away from the carrier. Inside the loop bandwidth the phase noise is simply that of the Crystal reference reduced by the Phase noise contribution of the Phase detector, the voltage regulators, loop filter opamps, and the prescalers and given by:

£(F)= Equation-17

$$20\ \mathrm{Log}_{10}(N_{Total}) + £(\mathrm{Reference}) \pm 3\mathrm{dB} \quad \mathrm{dBc/Hz}$$

However the phase noise for offsets outside the loop bandwidth and up to several 100 kHz, is simply that of a free running VCO.

£(F)= Equation-18

$$10\ Log_{10}\{[1+F_o^2/(2FQ)^2](1+F_c/F)FKT/2P_s+ 2KTRK_o^2/F^2\}\ dBc/Hz$$

Notice that for these offsets the Phase noise of the PLL synthesizer can not be improved or affected by the performance of any part of the Synthesizer for offsets frequencies greater than the loop bandwidth, since it is completely controlled by the VCO. For frequency offsets far away from the loop bandwidth, the phase noise is basically the noise floor of he system and very flat (clearly can be seen if we let the frequency offset term F in equation-18 goes to infinity).

£(F)= **zero** **zero** **zero**

$$10\ Log_{10}\{[1+F_o^2/(2FQ)^2](1+F_c/F)FKT/2P_s+2KTRK_o^2/F^2\}\ dBc/Hz$$

or just $£(F)=10\ Log_{10}[FKT/2P_s]\ dBc/Hz$

The only thing that could improve the PLL's Phase noise at these offsets is by choosing an oscillating device with low noise figure F. And by increasing the average power at the Active device input there by increasing the signal to noise ratio effectively. This can be done by having minimum loss in the Resonator and maximum reactive impedance in the resonator. Or in other words, we are back to mandating a very high Q for the resonator.

Practically, and after building the PLL, there are two methods in which we can test the Phase noise performance. We can use a dedicated HP-3048 test gear, or simply with a Spectrum Analyzer. Figure-5 shows the spectrum of

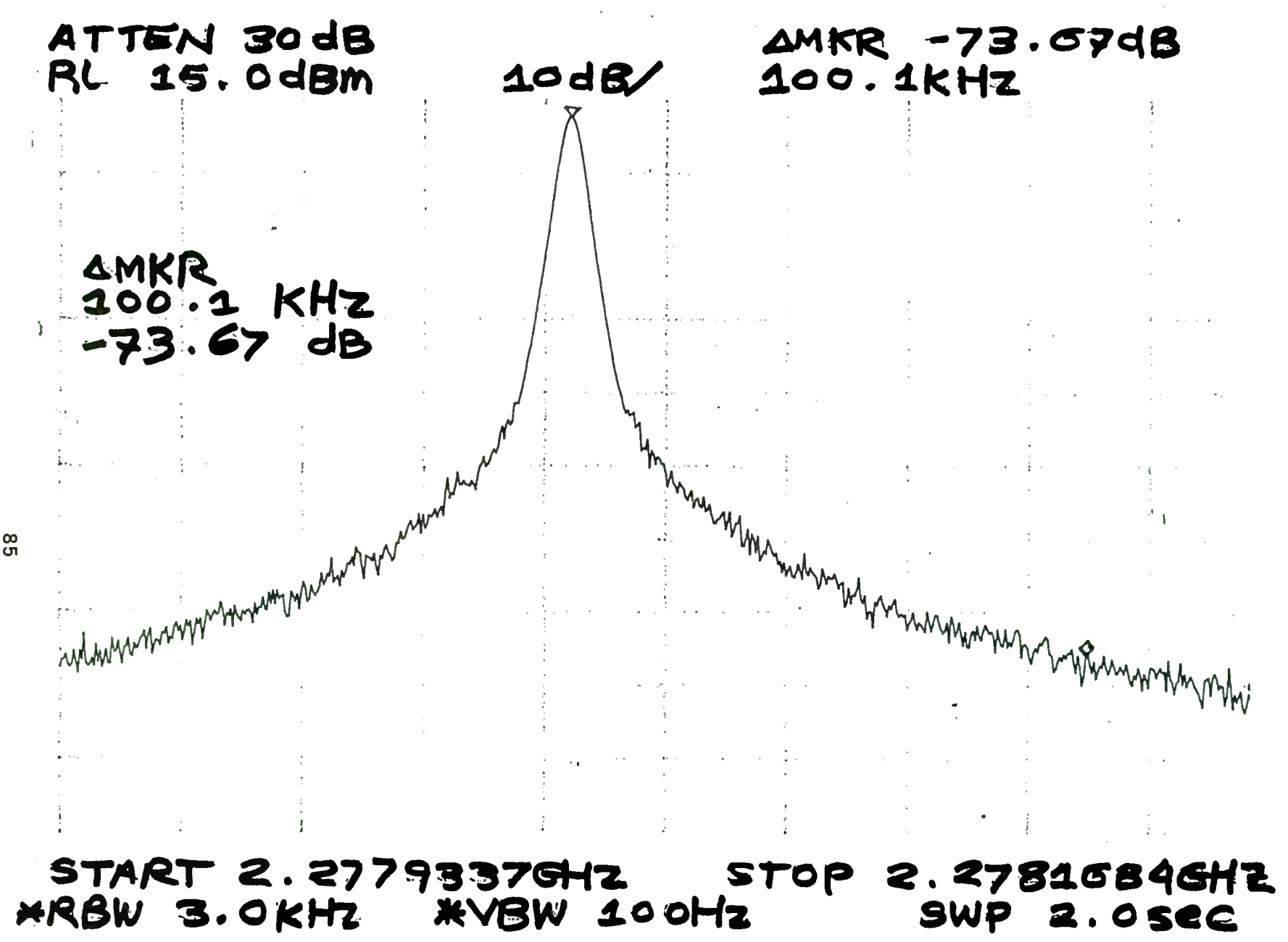

Figure-7: A spectrum Analyzer of the Synthesizer output. The Δ Marker is used to compute the Phase Noise.

the signal at 2278 MHZ. To measure the phase noise center the Span of the spectrum analyzer on the carrier. Adjust the span so the appropriate offset frequency can be viewed. The difference between the levels of the carrier and the noise level at the offset minus $10Log_{10}$(Resolution bandwidth of the Spectrum analyzer) is simply equal to the Phase Noise in dBc/Hz. As an example the delta marker on figure-6 shows a
-73.67 dBc at an offset of 100 kHz from the carrier. The Resolution Bandwidth is 3 kHz. So the Phase noise at an offset of 100 kHz is -73.67-10Log10(3000) = -108 dBc/Hz.

The article should serve as a novel starting point to designers who are new to the design of Frequency synthesizer and as a review to those who are experienced in this field. The CAD model for simulating the Phase and gain margins as well as the transient response had proven to be a powerful method. It is easy, no math involved, and the software is very conveniently available.

Note: *This work has been conducted by the author prior to joining Allied-Signal Aerospace.*

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Bibliography: *Mohammed Nezami was born in Jordan, he has a BSEE (1988) and MSEE (1992) from the university of Colorado. Currently he is pursuing a PhDEE at Florida Atlantic University, Boca Raton Florida.*

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SAW Devices for Digital Mobile Communication Systems

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ABSTRACT

One of the major focuses of all modern systems is to optimally utilize the allocated frequency band for maximum subscriber capacity and fastest data transfer. SAW filters are already established as the key technology for channel selection in almost every digital communication system due to their high stopband transition, low amplitude and delay variation in the passband and a high temperature stability.

The paper focuses on high-performance SAW components developed for IF filtering in CDMA and TDMA basestation and subscriber units. System requirements, full-custom design methods and the filter performance will be discussed. Finally, the trends in SAW technology will be highlighted.

I. INTRODUCTION

Recently, a number of new digital mobile communications systems have been introduced on the market. The systems provide digital radio quality, higher subscriber density and numerous functional features serving personal computers, pagers and faxes.

Regarding the subscriber access modus, digital mobile communication systems can be classified into two groups: a) the Code Division Multiple Access (CDMA) systems and b) the Time Division Multiple Access (TDMA) systems. In the case of CDMA, the digital information is modulated by a particular digital code. By using different orthogonal functions for the digital code for every particular subscriber, a large number of these spread-spectrum signals can occupy the same radio band for transmission. In the receiver the spread signals are separated from each other without interference by applying the same digital code used for the modulation. In TDMA systems the subscribers are separated in the time domain by using different time slots. Accordingly, every physical channel contains a number of subscriber signals.

Meanwhile, several different CDMA and TDMA systems are already established or will start operation soon. The common CDMA systems are:

- cellular CDMA occupying a radio band at 800 MHz and
- PCS-CDMA at 1900 MHz.

The TDMA systems are:

- GSM at 900 MHz,
- PCN/DCS1800 at 1.8 GHz and
- PCN/DCS1900 at 1.9 GHz.

System	cellular CDMA	GSM
Frequency range	935-960 MHz 890-915 MHz	824-849 MHz 869-894 MHz
radio bandwidth	25 MHz	25 MHz
number of physical channels	10	125
subscribers per channel	118	8
channel spacing	1.23 MHz	200 kHz
data rate	1.228 Mbit/s	270.8 kbit/s

Table I: Digital mobile communication systems: system characteristics

Table I gives a brief comparison between two representative systems, namely cellular CDMA and GSM. Both systems accommodate several subscribers in one physical channel. In the case of CDMA, the spreading of the signal frequency spectrum leads to rather wide physical channels. However, due to the orthogonality of the spreading codes, up to 118 subscribers can be served in the same spectrum. With 10 physical channels, the cellular CDMA has a capacity of

1,180 subscribers per cell cluster.

In GSM the channel spectrum is significantly narrower. Every channel serves 8 subscribers, by using different time slots. However, 125 physical channels are accommodated in the 25 MHz radio band giving a total capacity of 1000 subscribers per cell cluster.

The PCS-CDMA system uses the same modulation and channel spacing as the cellular CDMA. The main difference is a wider RF frequency band at 1.9 GHz leading to a much higher subscriber capacity.

The PCN/DCS1800 and the PCS/DCS1900 systems are similar to GSM. They use the same channel spectrum and channel spacing. The main difference is that they occupy a significantly wider RF band at 1.8 GHz and 1.9 GHz respectively, allowing a capacity of up to 3000 subscribers per cell cluster.

SAW technology can provide appropriate IF filtering in both CDMA and TDMA mobile communication systems. Section II of this paper deals with the system requirements for IF filters in digital mobile communication systems. Section III introduces the main SAW design techniques and the fabrication technology. Finally, sections IV and V give some filter examples for CDMA and TDMA systems.

II. SYSTEM REQUIREMENTS

There are several receiver architectures for CDMA and TDMA phones resulting in different requirements for the center frequency, the passband flatness and the stopband rejection of the filter.

The choice of the receiver's 1st IF frequency depends on the front-end concept, on the synthesizer and oscillator architecture and finally on the demodulation method. Therefore, about every basestation or subscriber model uses a different IF frequency. Generally, systems with an RF below 1 GHz use a 1st IF around 100 MHz. This simplifies the next down-conversion and the demodulation. Systems with an RF at 1.8 GHz and 1.9 GHz are designed with an IF frequency around 200 MHz and above to simplify the filtering and the down conversion in the RF stage.

system	1st IF	fractional bandwidth
cellular CDMA	45 to 110 MHz	1.1 to 2.8%
PCS CDMA	> 200 MHz	< 0.6 %
GSM	70 to 300 MHz	0.3 to 0.07%
PCN/DCS1800	> 160 MHz	< 0.1 %
PCS/DCS1900	> 160 MHz	< 0.1 %

Table II: IF frequencies of CDMA and TDMA mobile communication systems.

Table II gives an overview of the current IF frequencies used on the market. Most GSM IF frequencies are around 100 MHz, however, there is a trend to use frequencies above 200 MHz in order to have uniform receiver platforms for GSM and PCS/DCS1800. The required fractional bandwidths vary between 0.07% and 2.8%.

The system requirements of the IF filter passband are generally different for CDMA and TDMA systems. The performance of CDMA systems is sensitive to amplitude and phase variation in the passband. In order to get an acceptable bit-error rate, an amplitude ripple around 1 dB and a phase linearity of 5°rms are specified within the passband.

In TDMA systems the channel spectrum has a gaussian shape with a 6 dB bandwidth of 200 kHz. However, since the information is concentrated in the center of the channel, the required filter bandwidths are between 145 kHz and 180 kHz. The bit-error rate primarily depends upon the group delay ripple. Depending on the receiver's architecture, the group delay ripple is required to be in the range of 500 ns to 1 µs.

The system requirements on the filter's stopband rejection are primarily given by:

- the receiver's blocking performance since strong, adjacent channels have to be suppressed to allow the linear operation of the receiver,
- the frequency of the 2nd IF since the image frequency has to be suppressed before the next conversion.

- the channel selection since the adjacent channels have to be suppressed to avoid co-channel interference in the demodulator.

Filters required for blocking and image frequency suppression are usually wider than the channel bandwidth and are known as roofing filters. Filters contributing primarily to channel selection have a sharp passband transition and are usually called channel filters. In many cases, the channel selectivity is distributed between several IF stages and in the analog and the digital part of the baseband.

For CDMA the requirements for stopband rejection start at ±900 kHz from the center frequency and call for relative attenuation between 30 dB and 50 dB. Due to the demands for a very flat and wide passband, the resulting shape factor for CDMA filters is in the range of 1.2. For TDMA filters the requirements on stopband rejection start at ±200 kHz and depend on the additional filtering in other IF stages and at baseband.

III. SAW TECHNIQUES

The function of SAW filters is based on the piezoelectric behavior of non-isotropic materials. By applying a voltage on the surface of a substrate, a surface acoustic wave (SAW) propagates on the top of the crystal. Due to reciprocity, a propagating wave can also induce a current on electrodes placed on the surface.

In order to get a bandpass characteristic, interdigital transducers (IDTs) are deposited on highly-polished piezoelectric substrates. The IDTs consist of thin electrodes alternately connected to the two bus bars. If an input voltage is applied on the one transducer, it excites an acoustic wave propagating on the top of the surface. As it travels under a second transducer, the wave induces a voltage at the output of the filter. The center frequency is given by the acoustic wave velocity and the periodicity of the electrodes. Since the SAW velocity is 10^{-5} slower than an electromagnetic wave, the resulting wavelength and hence the dimensions of SAW components are very small compared EM counterparts for a given impulse response lentgh.

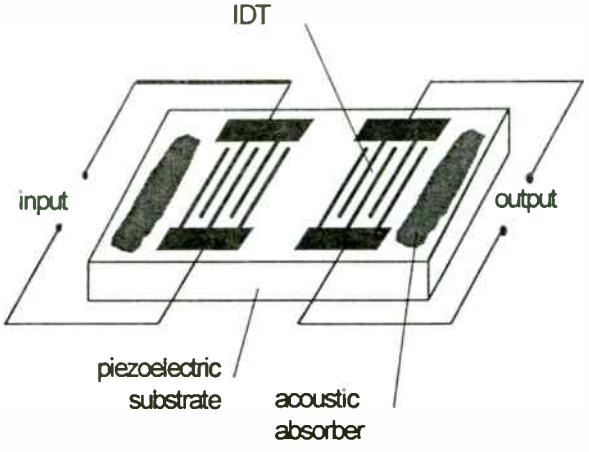


Fig. 1: SAW filter schematic

Fig. 1 shows schematically a SAW bandpass filter with two IDTs. Since every IDT launches waves in both directions perpendicular to the electrodes, some absorbing material is added on the end of the substrate to suppress acoustic waves reflected by the edges of the substrate.

The frequency response of the filter shown in Fig. 1 can be easily described by means of the Fourier transform: the impulse is given by the convolution of the impulse response of the two IDTs. Furthermore, the impulse response of each IDT is given by the geometry of its electrodes. By varying the length of the electrodes it is possible to weight the impulse response and hence shape the frequency response of the filter.

For example, an IDT consisting of constant electrode length will give a $\sin x/x$ response in the frequency domain. This response is not sufficient for IF filtering, since most applications require a steeper shape factor and a better stopband rejection. Actually, a filter with a rectangular frequency response is usally optimal.

Based to the Fourier transform, however, a rectangular characteristic in the frequency domain corresponds to a $\sin x/x$ function in the time domain and hence to an IDT with infinite length. Therefore, several design methods have been developed to optimize the frequency response for a given IDT length. Nevertheless,

the steepness of the passband skirts, the flatness of the passband and the stopband rejection are primarily proportional to the length of the IDTs.

The temperature dependence of the frequency response is an important parameter of the receiver's performance. Due to the tight requirements on the transition bandwidth, a quartz substrate is the most commonly used material for narrowband IF filters. It has a parabolic temperature dependence of frequency given by

$$\frac{\Delta f}{f} = \left(\frac{T - T_o}{5.4}\right)^2 ppm,$$

where $\Delta f / f$ is the frequency drift in ppm, T the ambient temperature and T_o the turnover temperature. By choosing an appropriate crystal cut, the turnover temperature point can be optimally selected. In this case the frequency drift of a filter operating, for example, in a range between -20 °C and +70 °C will be 70 ppm.

Due to the considerably low electromechanical coupling of quartz, the insertion loss of filters consisting on two IDTs is considerably high. In addition, in order to avoid acoustic echoes due to regeneration, input and output IDT have to be electrically mismatched to the source and load. The resulting insertion loss depends on the fractional bandwidth and the requested passband ripple and is in a range between 20 dB and 25 dB.

Some new IDT patterns have been developed to reduce the insertion loss. These patterns use reflective electrodes distributed within the IDTs, allowing the waves to be launched in only one direction. In this case it is possible to electrically match the filter to the source and load without an increase of acoustic echoes. This IDT technique is called the single phase unidirectional transducer (SPUDT) /1/. SPUDT filters have 10 to 15 dB better insertion loss. Usually, their passband ripple is slightly higher than in the case of conventional 2 IDT filters.

A major reason for the high reliability and reproducibility of SAW devices is their advanced process technology. Highly polished wafers and the photolithographic patterning process employed in the semiconductor industry lead to precise and reproducible fabrication of the electrode structures. Exposure, developing and etching are critical parameters for the frequency accuracy of the filters.

For the final assembly of the die, various packages are in use. Long dies for high-performance applications are housed in dual in-line metal packages. For subscriber applications however, size and surface mount capability are as important as the frequency response. SMP ceramic packages, available in different sizes, are used in this case. Advanced packaging technology can reduce the thickness of SMP packages to less than 70 mils.

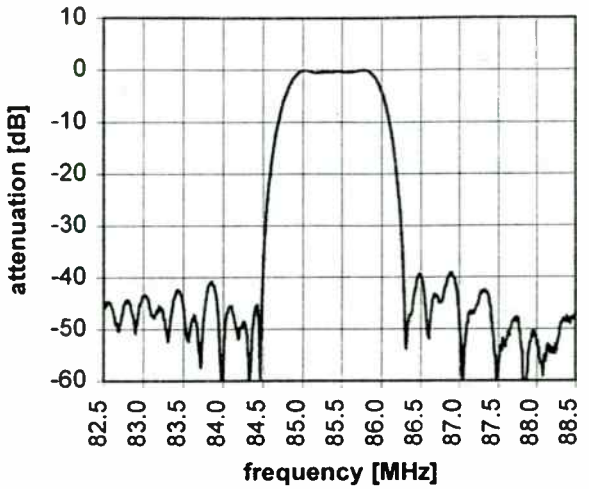
IV. IF filters for CDMA

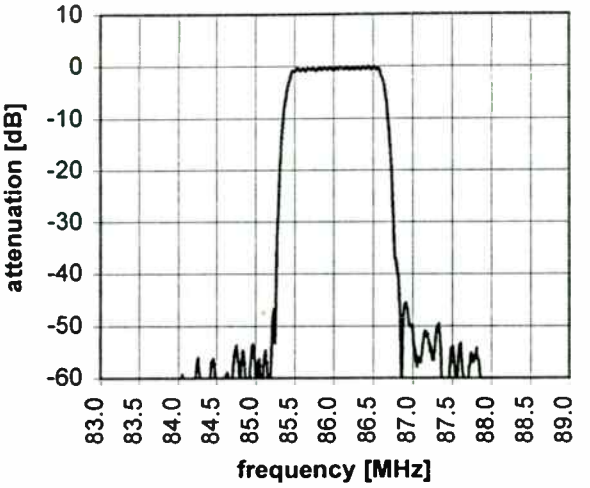
For IF applications in subscriber cellular-CDMA phones, filters have been developed at 85.38 MHz. The SPUDT technique has been applied to reduce the insertion loss and hence to increase the system's signal-to-noise ratio.

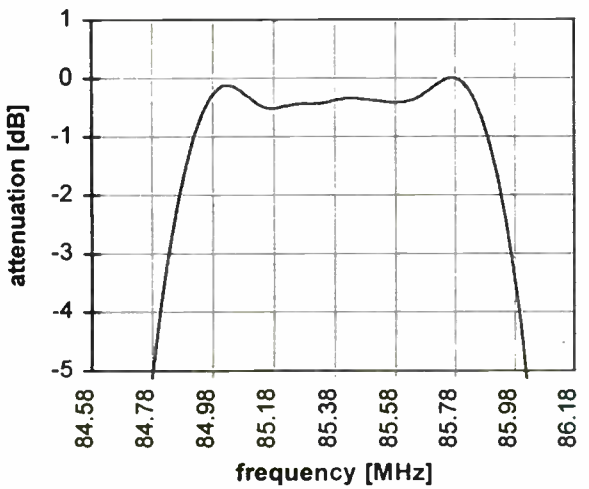
Fig. 2 shows the frequency response of the filter. A simple network consisting of a parallel inductor and a series capacitance matches the filter to a 1000 Ω source and a 500 Ω load. By changing the matching network, the filter can be matched to virtually any impedance. Depending on the circuitry, the filter can be connected for single ended, balanced operation or mixed operation.

Table III summarizes the typical characteristics of the filter. The filter is mounted in a 10 pin SMP with a dimension of .75" x .26" x .07" and can operate in a temperature range from -30°C to +80°C without any degradation of the performance.

For basestation applications the passband and stopband requirements are significantly tighter, resulting in a longer SAW structure. Fig. 3 gives an example of an 86.01 MHz filter developed for cellular CDMA basestations. Table IV summarizes the filter characteristics.







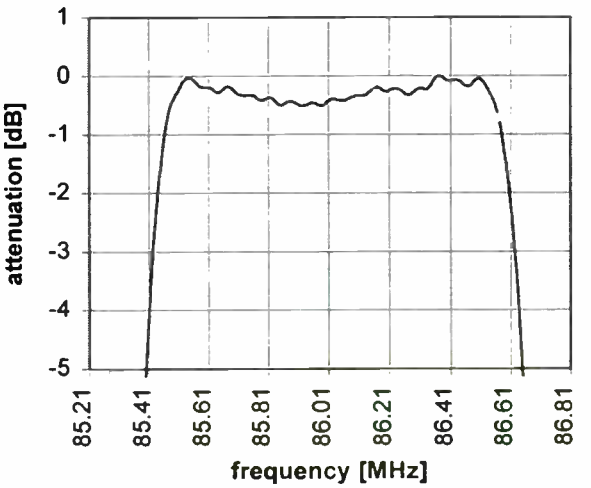


Fig 2: IF filter for CDMA subscriber phones: frequency response.

Fig 3: IF filter for CDMA basestations: frequency response.

Parameter	Typ. Value
Center Frequency fo	85.38MHz
Insertion Loss	15.0 dB
Passband Variation at fo ± 300 kHz	0.3 dB
Phase Linearity at fo ± 630 kHz	2.0 °rms
Attenuation at fo ± 900 kHz	35.0 dB
Attenuation at fo ± 1.23 MHz	38.0 dB
Ultimate Rejection	40.0 dB

Table III: IF filter for CDMA subscriber phones: filter characteristics

Parameter	Typ. Value
Center Frequency fo	86.01MHz
Insertion Loss	15.0 dB
passband Variation at fo ± 450 kHz	0.5 dB
Phase Linearity at fo ± 630 kHz	2.0 °rms
Attenuation at fo ± 900 kHz	48.0 dB
Attenuation at fo ± 1.23 MHz	50.0 dB
Ultimate Rejection	58.0 dB

Table IV: IF filter for CDMA basestations: filter characteristics

The required 1.5 dB-to-35 dB shape factor of 1.2 led to a die length of 2.8" fitting into a 2.9" bathtub metal DIP package. The operating temperature range is -5°C to +65°C.

V. IF filters for TDMA

For TDMA applications below 200 MHz, SPUDT filters are the appropriate technique to achieve the system specifications. Fig 5 shows the frequency response of a 71 MHz channel filter developed for GSM basestations.

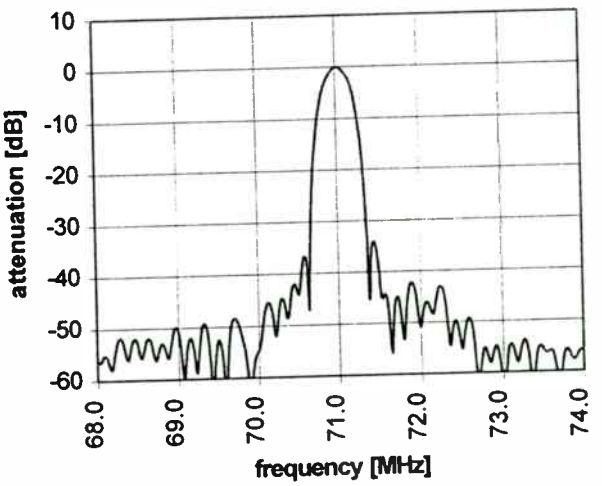


Fig 5: SPUDT filter for TDMA basestations: frequency response

The insertion loss is typically 6 dB and the group delay ripple in the passband better than 750 ns. The 2nd and 3rd adjacent channels at ±400 kHz and ±600 kHz are suppressed by more than 32 dB and 42 dB respectively. The ultimate rejection is typically more than 50 dB. The die fits into a 14-pin DIP metal package with the dimensions of .87" x .50" x .21".

CONCLUSION

SAW filters offer substantial advantages for IF filtering in digital mobile communication systems. There are various SAW techniques offering an optimum solution in every particular receiver architecture. By using simple LC networks, the filters can be matched to virtually every single ended or balanced load giving a high degree of flexibility in the circuit design.

Furthermore, the SAW filters have influenced the receiver's architecture itself. In some cases SAW filters with high stopband rejection allow a simplification of the demodulation and the digital circuitry.

Finally, in subscriber phones, the use of compact SMP packages has led to a further miniaturization of the PCB.

The rapid progress of communication systems will continue to present a great challenge to the component engineer. SAW filters will gain more importance in miniaturized equipment, simplifying circuitry and reducing manufacturing cost in future digital mobile communication systems.

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Multipath fading emulator

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Sofimation has developed a multipath fading emulator that exceeds current test standards for evaluating the RF channel characteristics of cellular communications systems. Is it necessary to have a fading emulator with over 300 signal paths and a signal bandwidth of 35 MHZ?

This paper will explain the necessity of using advanced simulation instruments when making developments for current and future wireless communications systems, including the development of microcells and equipment for Digital European Cordless Telephone (DECT) systems, low-earth-orbit (LEO) satellite systems, and spread-spectrum-based systems. The paper will also offer a brief history of fading simulator development.

DIGITAL WIRELESS COMMUNICATIONS

Digital Wireless Communications

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Hewlett-Packard Co., Lake Stevens Division (Everett, WA)

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SYSTEM CONSIDERATIONS FOR UNLICENSED DIGITAL TRANSMISSION BELOW VHF

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ABSTRACT

There has been a surge in the development of Federal Communications Commission (FCC) Part 15 (unlicensed) devices for the UHF and microwave region precipitated by the recent FCC regulation changes for unlicensed spread spectrum operation in these bands. Many digital applications, such as wireless Local Area Networks and real time telemetry, require high data rates. But, many low data rate applications do not require the wide bandwidth available at microwave frequencies. In the press to develop unlicensed digital transmission devices of all types, little consideration is being given to operation at frequencies below the VHF region (< 30 MHz).

This paper reviews the various FCC allocations for unlicensed operation below 30 MHz, discusses their advantages and disadvantages, recommends various design architectures to maximize their usefulness for digital communication, discusses technologies that can be optimized to improve digital link performance, presents some selected test data demonstrating some design possibilities, and makes some general conclusions.

I. INTRODUCTION

For those digital applications not requiring high data rates (< 2400 BPS), there are several spectrum allocations below 30 MHz that were made available in the past by the FCC for various applications. Although many of the original applications were analog (wireless microphones, Citizens Band, etc.), in many cases the regulations do not limit the modulation to analog waveforms.

Of course, all of these allocations follow the same restrictions regarding interference to and susceptibility from licensed users. That is, the transmissions must not interfere with and must tolerate interference from licensed users of the spectrum. In addition, the transmission paths at frequencies below 30 MHz are limited to a great degree by atmospheric noise. Also, ionospheric reflections and day-to-night/seasonal noise variation can be very troublesome for some applications operating at certain frequencies. Fig. 1 [1] shows the noise level in a 10 kHz band as a function of receiver frequency. It is readily apparent that atmospheric noise is much higher below 30 MHz. Also, note the wide variation in noise level between day and night. Despite the highly variable noise level, these frequencies offer some benefits that microwave spectrum cannot offer. These include low signal path loss through non- and partially-conductive obstacles, reduced multi-path interference, very low component cost, and simple construction practices.

Various transmit receive architectures can be designed to overcome the spectrum-related problems. Many of these architectures in some way allow the link to respond and correct for interference and propagation degradation. With the availability of low-cost processors and special-purpose digital circuits, propagation problems below 30 MHz can be overcome or at least minimized. Recognizing these considerations may pave the way for many new and useful unlicensed digital wireless applications making use of spectrum currently underutilized for digital communication.

II. REGULATIONS

Unlicensed intentional radiation below 30 MHz is allowed by existing FCC regulations. In fact, many of the unlicensed bands allocated have been in force for a

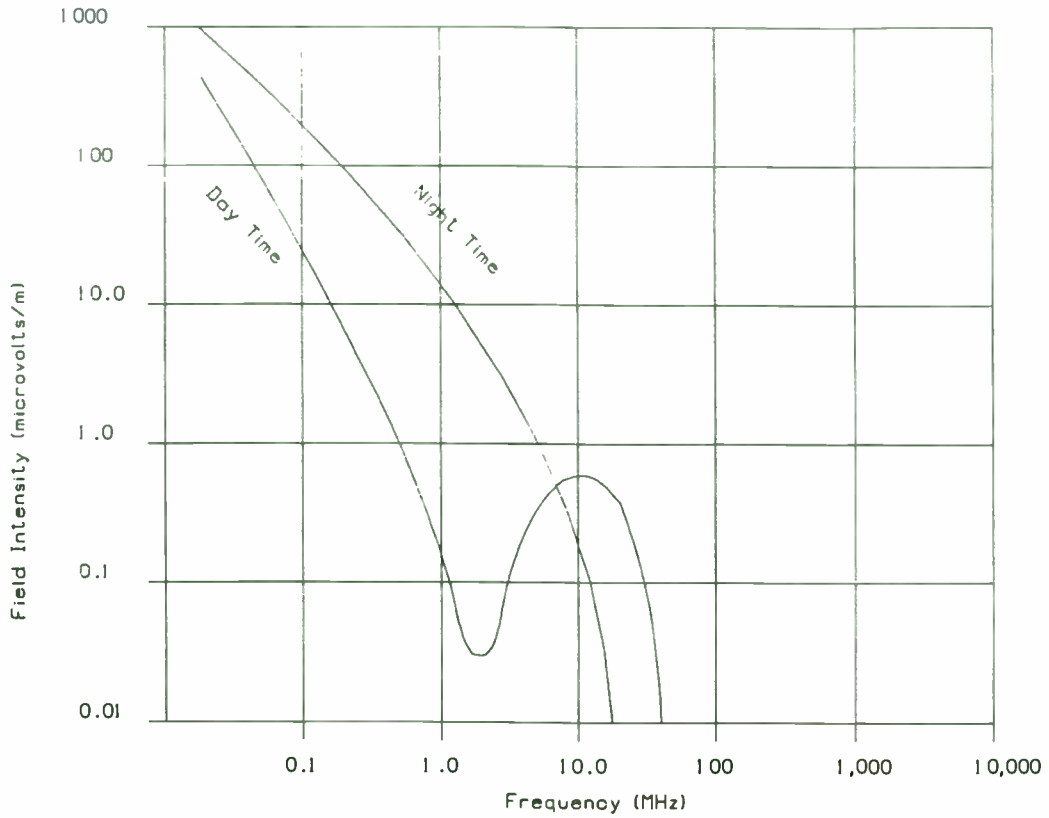

Fig. 1. Atmospheric Noise in a 10 kHz Band Versus Frequency

very long time. This is evident even in the wording of the regulations that exempt "heater current" from the input power limitations. It has been at least thirty years since vacuum tubes were necessary to generate the limited signal strengths required for unlicensed operation below 30 MHz. Despite the mention of heater current, the specifications have changed over the years. For example, the 100 milliwatt limitation for unlicensed operation in the Citizens Band has been reduced to a much lower level. Most of the low-power citizen-band applications have been moved to the 49.82 to 49.90 MHz band. Also, Section 15.223 covering the 1.705 to 10 MHz band encourages the use of frequency hopping and other spread spectrum modulations.

Table 1 lists the bands presently allocated by the FCC for unlicensed operation below 30 MHz. Table 2 describes some modifications to Table 1. Notice that there appears to be no regulated frequencies (frequencies below 9 kHz are not regulated) that are not available for unlicensed use. With the exception of certain restricted frequencies, this is essentially correct. Table 3 lists restricted frequencies together with their primary application. As can be seen by the applications, there is good reason for restrictions on these frequencies. But, also note that the total restricted bandwidth is only 0.2047 MHz, which is less than 1 percent of the .009 to 30 MHz range.

In addition to the general unlicensed transmit power limitations shown in Table 1, the FCC has provided some sub-bands with modifications of the general power/field strength restrictions (Table 2). These sub-bands have no restrictions on modulation type or application. but their technical characteristics are generally specified differently than the restrictions exemplified by Table 1. For example, the radiation limitations for the 160 to 190 kHz and .535 to 1.705 MHz bands are specified in terms of input power to the final amplifier versus field strength at a given distance from the transmit antenna. In any case, unlicensed operation in many of these sub-bands is allowed at higher levels than the general limitations specified for 0.009 to 30 MHz operation in Table 1.

TABLE 1.
FCC PART 15 BASIC BANDS OF OPERATION BELOW 30 MHZ
NOT DESIGNATION FOR SPECIFIC APPLICATIONS

FREQUENCY RANGE	MAXIMUM FIELD STRENGTH	MAXIMUM POWER	MAJOR TECHNICAL RESTRICTIONS	PROPAGATION AND DESIGN CONSIDERATIONS
9 - 490 kHz	2,400/Freq.(kHz) - micro-volts/meter at 300 meters	Approximately equivalent to -47 dBm into a dipole at the lowest frequency.	Efficient antennas are not physically small and high noise level.	Atmospheric noise is high restricting most applications to near field distances only.
490 - 1705 kHz	24,000/Freq.(kHz) - micro-volts/meter at 300 meters	0.1 Watts allowed at certain frequencies	Variable noise conditions.	The broadcast station interference can be minimized by operation at channel overlap. Ranges on the order of 1 mile are easily possible for low data rates.
1.705 - 30.0 MHz	30 micro-volts/ meter at 30 meters	Approximately equivalent to -47 dBm into a dipole.	Variable propagation characteristics.	Atmospheric noise varies greatly across this range of frequencies.

TABLE 2.
MODIFICATIONS OF THE BASIC FCC PART 15 BANDS OF OPERATION BELOW 30 MHZ
THAT ARE NOT DESIGNATION FOR SPECIFIC APPLICATIONS

FREQUENCY RANGE	MAXIMUM FIELD STRENGTH	MAXIMUM POWER	REGULATORY TECHNICAL RESTRICTIONS	PROPAGATION AND DESIGN CONSIDERATIONS
160 -190 Khz	NA	1 Watt input to the final stage	Total antenna length less than 15 meters.	Antenna size restrictions limit the radiation efficiency of antennas. All links at this legal power level would be near field designs with a maximum useful range of approximately 300 feet.
510 - 1705 kHz	NA	0.1 Watts input to the final stage	Total antenna length less than 3 meters.	The broadcast station interference can be minimized by operation at channel overlap. Ranges on the order of 1 mile are easily possible for low data rates.
1.705 - 10.0 MHz	100 micro-volts/ meter at 30 meters	Approximately equivalent to -37 dBm into a dipole.	None	Atmospheric noise varies greatly across this range of frequencies.
13.553 - 13.567 MHz	10,000 micro-volts/meter at 30 meters	Approximately equivalent to +3 dBm into a dipole.	None	Industrial Scientific and Medical applications produce can produce high noise levels.
26.96 - 27.28 MHz	10,000 micro-volts/meter at 3 meters	Approximately equivalent to -17 dBm into a dipole.	Primarily used for "citizens band," but not restricted to that use.	Multiple coherent signals with variable frequency and amplitude.

TABLE 3.
FCC PART 15 RESTRICTED BANDS OF OPERATION BELOW 30 MHZ

FREQUENCY RANGE	TOTAL BANDWIDTH RESTRICTED	PRESENT BAND USE
90 - 110 kHz	20 kHz	LORAN C (navigation system) transmissions.
495 - 505 kHz	20 kHz	International distress transmissions
2.1735 - 2.1905 MHz	17 kHz	International distress transmissions
4.125 - 4.128 MHz	3 kHz	International agreement
4.17725 - 4.17775 MHz	0.5 kHz	International distress direct printing
4.20725 - 4.20775 MHz	0.5 kHz	International distress digital selective calling
6.215 - 6.218 MHz	3 kHz	International agreement
6.26775 - 6.26825 MHz	0.5 kHz	International distress direct printing
6.31175 - 6.31225 MHz	0.5 kHz	International distress digital selective calling
8.291 - 8.294 MHz	3 kHz	International agreement
8.362 - 8.366 MHz	4 kHz	Search and rescue of manned space vehicles
8.37625 - 8.38675 MHz	0.5 kHz	International distress direct printing
8.41425 - 8.41475 MHz	0.5 kHz	International distress digital selective calling
12.29 - 12.293 MHz	3 kHz	International agreement
12.51975 - 12.52025 MHz	0.5 kHz	International distress direct printing
12.57675 - 12.57725 MHz	0.5 kHz	International distress digital selective calling
13.36 - 13.41 MHz	5 kHz	Radio astronomy
16.42 - 16.423 MHz	3 kHz	International agreement
16.69475 - 16.69525 MHz	0.5 kHz	International distress direct printing
16.80425 - 16.80475 MHz	0.5 kHz	International distress digital selective calling
25.5 - 25.67 MHz	170 kHz	Radio astronomy

A. Special Bands of Interest

Although the band regulations listed in Table 2 confer additional signal strength under certain restrictions, the additional strength does not necessarily provide longer range. But, greater range can be obtained if the Part 15 transmitter is optimized to the limits of Table 2. For example, the 160 to 190 kHz band allows transmit final amplifier input power of up to 1 Watt. This seems rather generous until the implications of the antenna restrictions are recognized. The total antenna length in this band is limited to 15 meters. Fifteen meters is only 0.088 wavelengths at 175 kHz. An antenna of this length can be expected to be rather inefficient. Also, the atmospheric noise at this frequency is very high (see Fig. 1). Still, this band is rather underutilized since it is normally assigned to certain obsolete broadcasting and ground aeronautical navigation stations. A spectrum analyzer plot of signals during a summer day was taken on this band using a 1 meter diameter loop antenna followed by a low-noise preamplifier to the spectrum analyzer input. No coherent signals were present.

The 13.553 to 13.567 MHz band looks promising for long-range communication until it is realized that this frequency band is reserved for Industrial, Scientific and Medical (ISM) applications. Depending on ionospheric propagation, these frequencies can be very noisy. Industrial heating and welding at high RF levels are typical applications found in this band. Still, for narrowband signals (< 100 Hz), a fairly quiet frequency can often be found somewhere in the 14 kHz wide allocation.

The "Citizens Band" allocation from 26.96 to 27.28 MHz also offers the potential for long-range communications, but the "noise" sources in that band are well known. Modern microcontrollers in conjunction with conventional Citizens Band RF transceivers could be designed to provide digital packet communications. How well the microcontroller software copes with the signals, noise, and propagation characteristics of this band would be the limiting factor on data throughput.

Possibly the most useful band for low data rate digital communications listed in Table 3 is the 510 to 1705 kHz band. This band is normally assigned to AM broadcast stations throughout the world. Although there are many AM broadcast stations, their frequencies of operation are rigidly fixed. In the United States, the FCC requires that the stations be assigned carrier frequencies at 10 kHz spacing. No guard bands are allocated, but the modulation energy components are normally down quite a few dB at the center points between assignments (see Fig. 3). This is especially true for narrow bandwidths. In Europe and elsewhere, the frequency assignments are not spaced as in the United States, but those signals rarely reach this country at levels sufficiently above the atmospheric noise level, even at night. Atmospheric noise in this band is very low during the day (see Fig. 1) but rises greatly at night. This noise variation may present problems for some applications, but should be investigated for each potential application.

III. DIGITAL LINK ARCHITECTURES FOR LOW DATA RATES

Although high data rates are usually desired, there is a need and a place for low data rate wireless links. The signal limitations due to Part 15 regulations do not necessarily restrict the data rates for these links, but they reinforce the design tradeoff between link range and data rate. For a given signal-to-noise ratio, the data rate is restricted to a value determined by the channel bandwidth. This limitation is a well-known result of Claude Shannon's early work [2]. Slow data can still be of great value especially if the cost is lower or the data cannot be gotten by any other means. Fig. 3 shows a rough estimate of the approximate range that might be expected for "reliable" data transfer through Part 15 compliant links below 30 MHz. Note that very significant ranges (> 10 km) can be expected if the data rate is very slow (<10 BPS).

Part 15 frequencies below 30 MHz are appropriate for short (< 200 ft) and moderate (< 2 miles) range transmission at data rates less than about 2400 bits per second. Of course higher rates are possible, but the dynamic characteristics of these frequencies make it difficult to maintain equal signal quality over wide bandwidths (> 100 kHz).

A. Low Digital Data Rate History

During August of 1858, on the sixth day of communications through the new Atlantic cable, the received message log consisted of about 50 words, mostly short phrases. This was for the entire day. The previous five days were allowed for setting up receiving and transmitting equipment [3]. Assuming 32 bits per word and a 24-hour day, this would be equivalent to 0.0185 bits per second, or 67 bits per hour. This was typical operation until the cable went dead less than one month after completion. The cost for this cable was equivalent to several hundred million in today's dollars. Along with being possibly the slowest, this must have been among the most expensive digital data transmissions of all time. In a way this demonstrates that the data rate or data content is not necessarily a direct measure of the worth of a digital message. If there is no alternative way of getting the data, then the data rate may not be very important no matter how high the cost.

B. Latency

For low data rate links, the message speed may be much slower than normally encountered when using links with high transmission power budgets and normal bandwidths. Part 15 transmissions can overcome the low transmit power by narrowing the link bandwidth. This requires longer transmission times for any given message and, therefore, introduces some latency. For many applications, this is not a problem. A good example is a wireless restaurant waiter call button, a rather new wireless application using FCC Part 15 signals. These are placed on each restaurant table.

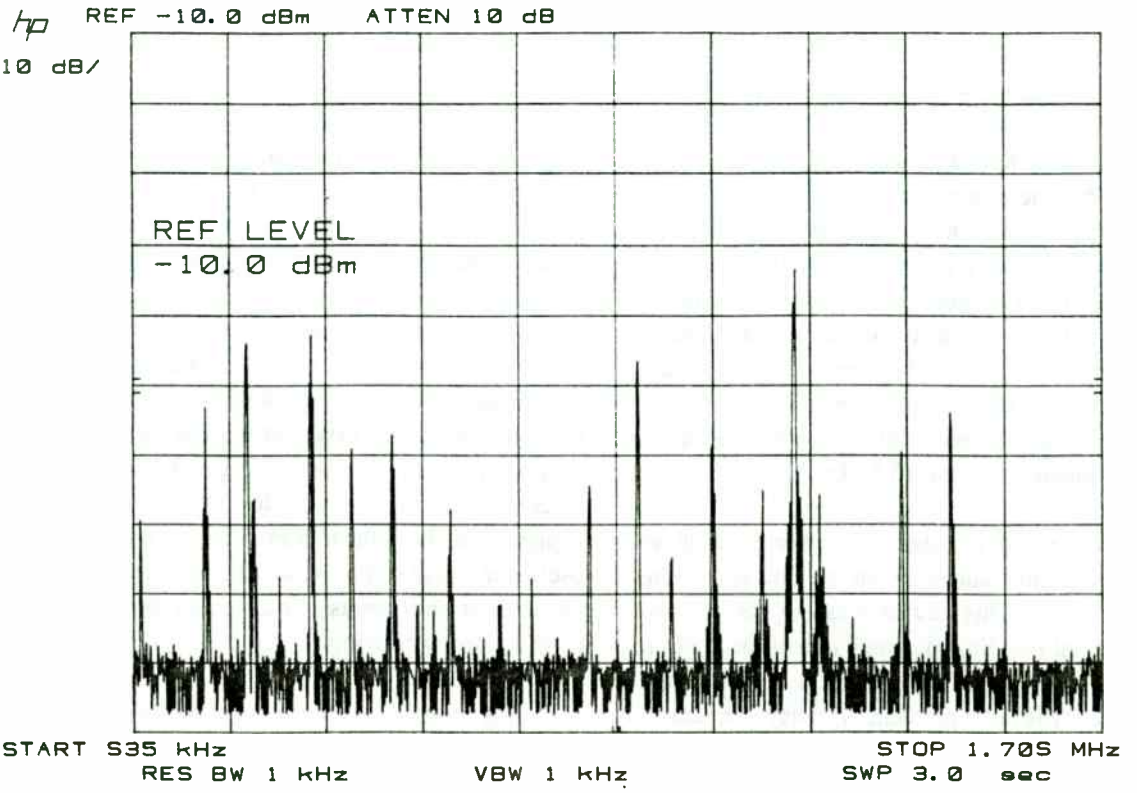

Fig. 2. AM Broadcast Spectrum, San Antonio, TX

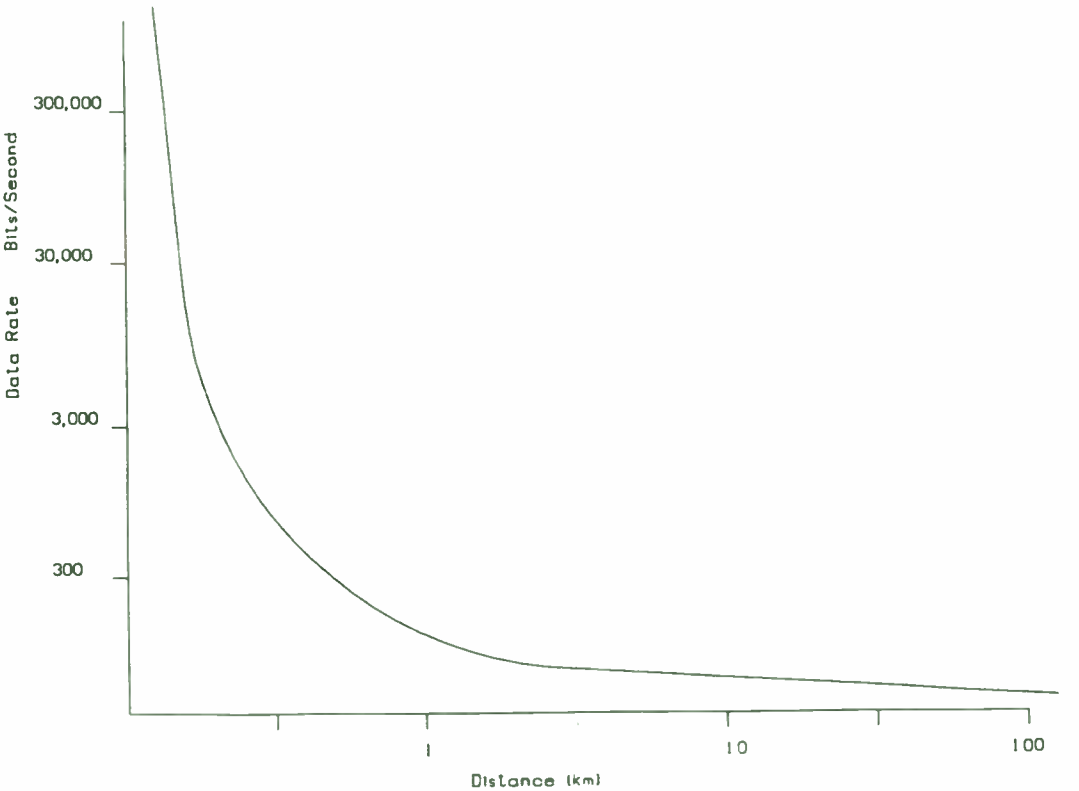

Fig. 3. Estimate of "Reliable" Data Transfer Rates vs. Distance for Existing Part 15 Regulations

1) Wireless Waiter Call Button: Such a call button should be designed to operate in a wide variety of locations, not all of which can be line of sight (a VHF and higher frequency limitation). The signal from the call button may have to reach a distance of several hundred feet but the data rate can be very low. Data is limited to either the presence of a signal or its absence. Signal delay is also not a problem, since the restaurant patron has no way of determining the receive time of the waiter's call. Of course a delay of several minutes would be unacceptable for even the speediest waiter. Nevertheless, with seconds or even minutes of time margin, much can be done with narrowband Part 15 signals at frequencies below 30 MHz.

2) Wireless Doorbell: Another good under 30 MHz application currently on the market is the wireless doorbell. This device must be designed to penetrate normal building materials to a distance of up to several hundred feet. The data rate is very low and moderate latency is not a problem. A delay of a second or so would not make the device any less useful. But, the wireless doorbell link must have good error rejection. A combination of high-level coding, clear dynamic frequency selection, and link feedback should be used to ensure that the doorbell only rings when the button is pushed.

C. Modulation Structure

Part 15 regulations usually do not restrict the type of link modulation. For frequencies that are atmospherically noise limited, modulation techniques requiring the minimum bandwidth for a given signal bit rate are usually more advantageous. This is not a result of the inherent improvement in modulation efficiency due to the narrower bandwidth, but is related to the ability of narrowband signals to be placed in "quiet" spots on a crowded spectrum. For this reason, Single Sideband (SSB) and On Off Keying (OOK) are usually the modulation modes of choice below 30 MHz. Of course there can be many variations of SSB and OOK modulation, including pulse width, amplitude, frequency, and phase variation. Normal AM, FM, FSK and other modulations are also used to some extent below 30 MHz. But, the various design tradeoffs for a noise-limited channel is beyond the scope of this discussion.

D. Frequency Generation and Stability

One of the most significant problems in the design of very narrowband communications links is the frequency stability of the transmitter and receiver. At frequencies up to a few MHz, crystal oscillators can be designed to provide stabilities on the order of one part in 10^6. This is adequate for maintaining transmit and receive frequencies for a receive filter bandwidth of 10 or 20 Hz, but is not adequate for narrower bandwidth signals and signals at higher operating frequencies. Automatic frequency control will work once communication is established; but without initial frequency stability sufficient to get the signal into the receiver bandpass, it is of little value. An alternative is signal reuse. Both the transmit carrier and receive local oscillator signal can be generated by receiving a signal common at both points. The signal can be stripped of modulation by filtering.

Depending on the short-term stability and the separation distance between the Part 15 transmitter and receiver, such a technique should be usable to communicate over bandwidths of less than 1 Hz. Fig. 4 shows an approach for obtaining a carrier frequency from a received signal, in this case the 10 MHz time standard station. The main feature of this scheme is that both the Part 15 transmitter and receiver at the remote location will operate using the same coherent frequency reference. Relative transmitter to receiver stability can easily be maintained to within a few Hz. The received carrier should not be amplified directly because of the potential for oscillatory feedback. By self-conversion or other means, the carrier can be translated to another frequency with less potential for positive feedback as shown in Fig. 4.

E. Automatic Link Establishment (ALE)

For conventional high-power LF through HF military communications, the need to accommodate the noise and signal path variation has resulted in the acceptance of a technique called Automatic Link Establishment (ALE). This is a signal protocol defined by MIL-STD-188-141A and Federal Standard 1045 (FS-1045). The protocol is rather specific for ALE compatible equipment. Part 15 devices need not meet the letter of these requirements, but their design architecture can benefit from the ALE concept. The basic ALE concept requires compliance with certain

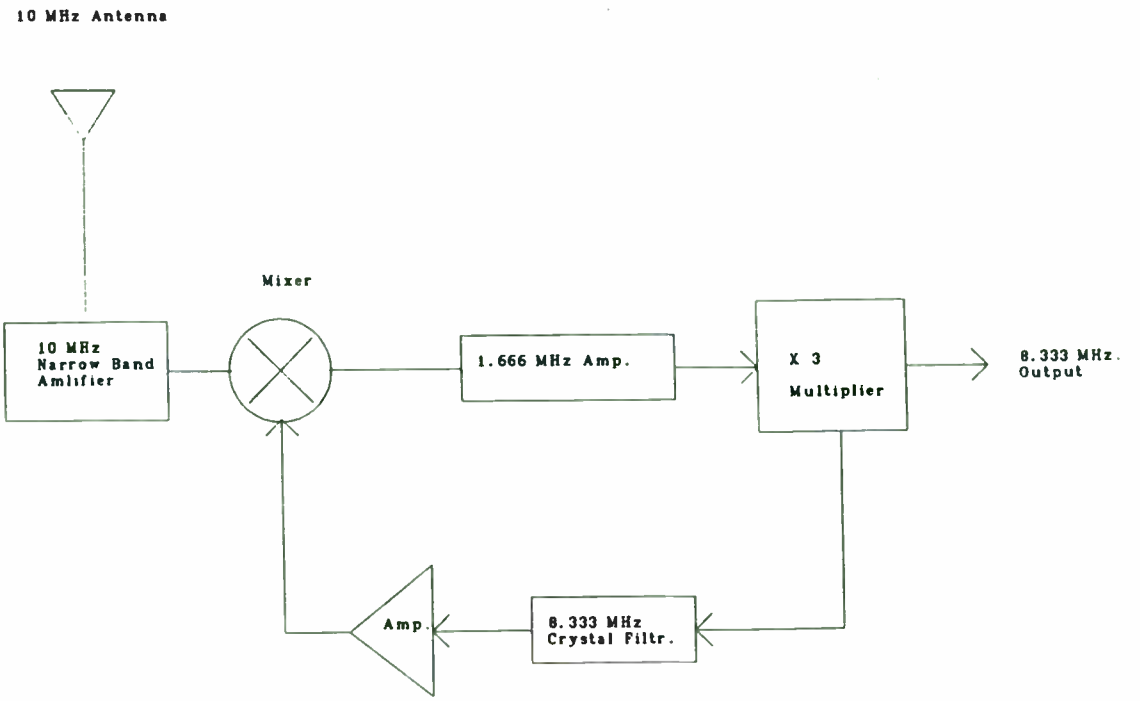

Fig. 4. Possible Carrier Generation Approach

operational rules that make sense for any link established over a path with highly variable characteristics. Some of the most important of these rules are:

1. An ALE system must operate in parallel with the primary receiver.
2. An ALE system must always scan and listen for ALE signals.
3. An ALE system must always respond unless inhibited.
4. An ALE system must always scan if not otherwise in use.
5. An ALE system must never interfere with an active ALE link (or other signals).
6. An ALE system must always exchange link quality data.
7. An ALE system must maintain time synchronization.
8. An ALE system must maintain track of link connectivity .
9. An ALE system must minimize transmit signal power.
10. An ALE system must minimize time on channel.
11. An ALE system must use the highest level of mutual ALE capability.

1) Duplex Error Correction: It has been recognized by the ALE community that full duplex link optimization can overcome both the errors introduced by the signal path noise and correct for path failure (insufficient path loss margin). By continuous interchange between the source of the information and the information receiver, it is possible to correct errors that are recognized by "echoing" the message, i.e., repeating it back to the transmit site or acknowledging correct receipt of the message by some coded means (point 6 above). This is a fundamental requirement for ALE systems and can be as simple or as complex as cost-effective Part 15 communications application will allow or require. This ALE feature is possibly the most useful to modern Part 15 link architecture.

A Part 15 transceiver architecture that could easily apply many of the ALE characteristics is shown in Fig. 5. This transceiver makes use of a single Voltage Controlled Oscillator (VCO) for the transmit carrier and the receive local oscillator. It can be tuned to a frequency within its design band and switched between transmit and receive at that frequency. A simpler

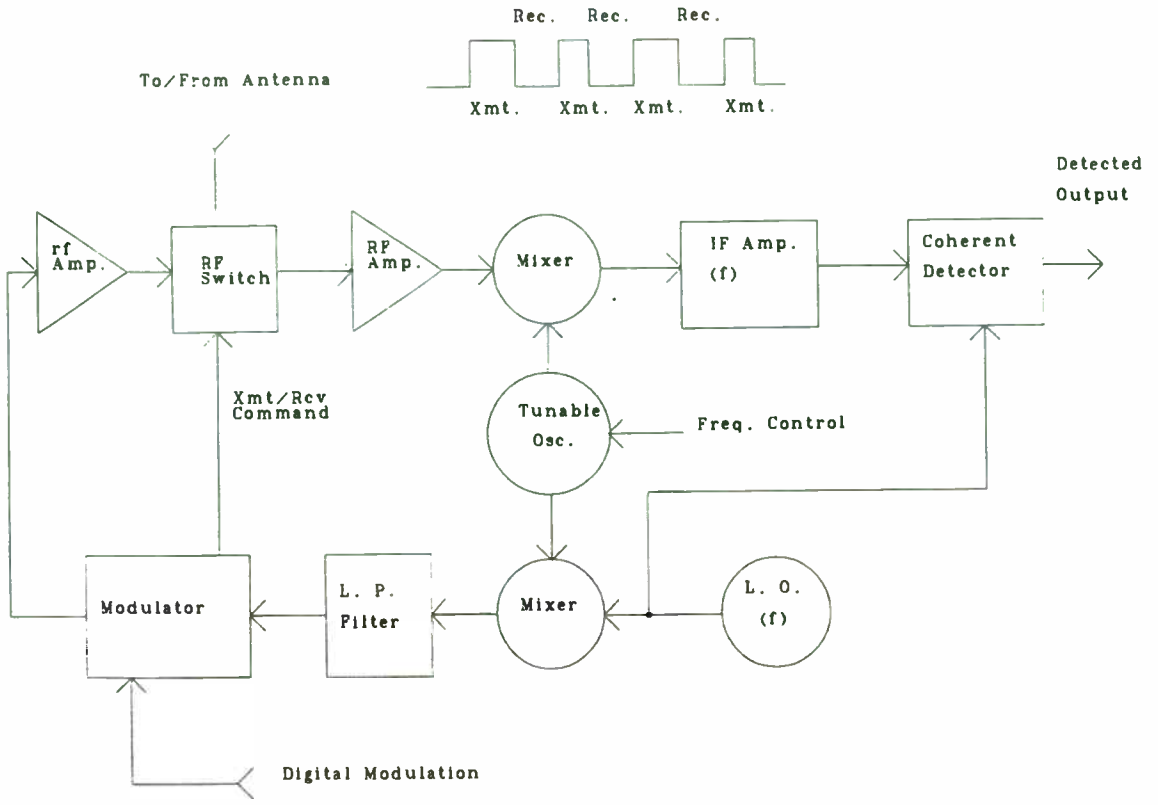

Fig. 5. Single Frequency Single Conversion Transceiver

transceiver architecture suitable for low frequencies (< 1 MHz) is shown in Fig. 6. This direct conversion architecture combines the coherent demodulation with the receive chain amplification.

IV. TECHNOLOGIES FOR MAXIMIZING WIRELESS BITS PER WATT OF SIGNAL POWER

A. Antennas

One of the key elements in the design of an unlicensed communications system is the antenna design. For bands regulated by field intensity restrictions, the transmit antenna can be quite simple and fairly inefficient. For these bands, the primary function of the transmit antenna is to produce a field strength as near as practical to the regulated level in all directions (omni-directional). Omni-directional antennas are usually quite simple. A fundamental example would be an electrically short monopole mounted above a ground plane.

Transmitting antennas providing gain at field strength restricted frequencies (see Tables 1 and 2) are of little value since the field strength in the direction of maximum gain must still be less than the field strength limit at the given distance. By transmitting through a simple omni-directional antenna, it may be possible to recover energy radiated in directions (reflections, conducted signal, etc.) other than that radiated directly to the receive site. Also, these antennas are simple to design and interface to the low-level drive required. Unless efficiency is a concern, matching to the drive circuit can often be ignored. This is because there is no great concern to have all available output power radiated. The only factor that is important is the field strength at the specified (per regulation) distance.

On the other hand, receiving antennas for unlicensed systems are where much of the system design effort should be expended. There are no restrictions on receive antenna gain. For operation at these ambient noise limited frequencies. this is doubly important. Not only will the antenna gain increase receive signal strength, it has the potential for drastically reducing the received signal noise. The potential is only realized if the noise source is not in the same direction as the unlicensed transmitter. This is a system design factor often neglected by designers of unlicensed equipment.

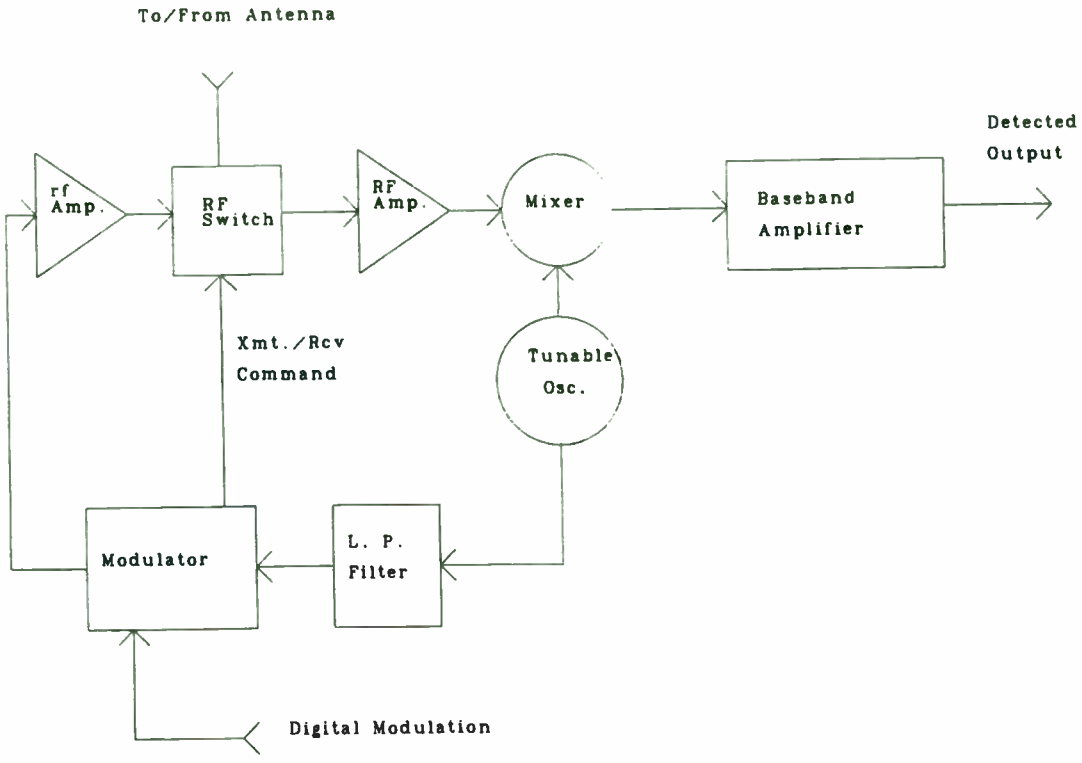

Fig. 6. Single Frequency Direct Conversion Transceiver

1) Beam Forming: Antenna gain at frequencies below 30 MHz is not an easy proposition if the antenna must be of a limited size. To obtain significant gain (> 10 dB), the antenna must on the same order of size or larger than the wavelength of interest. If the space is available, a steerable array such as a yagi, cubical quad, or multi-element phased arrays could provide both signal gain and noise rejection.

If a steerable antenna is not an option, antenna diversity can also be of great value especially for noise reduction. Simple antennas oriented orthogonally or in different angles in the same plane can be electrically switched at the receiver to produce the optimum receive signal-to-noise ratio from the unlicensed transmitter signal.

Although compact antennas seldom offer much gain, simple antennas such as dipoles and loops can provide a deep null usable against directional noise sources. In some cases, it is even possible to combine the phased signals from diversity antennas to reject the noise source signal. For ambient noise limited signals, noise rejection can be just as effective as antenna gain. Multiple ferrite loop antennas, also electrically short loop and dipole antennas, are prime candidates for design of a compact noise rejection antenna system suitable for Part 15 signals below 30 MHz.

2) Steering: If a beam-forming antenna is used for the receiver, it may often be an advantage to the link if the beam can be steered. Manual steering may be acceptable for some fixed location applications where personnel are available to steer the beam for optimum link operation. For design situations where link operation cannot be attended, some form of automatic beam steering may be appropriate. Automatic steering may be as simple as a circuit to select between various antennas aimed in different directions. This is very similar to spacial diversity situations being different only in that the steered antennas are all at the same location. It is also possible to electrically switch the elements of an antenna to change the maximum gain or null direction. Again, the actual use of antenna steering will be determined by many link factors and may not be possible or desirable for some.

3) Antenna Loss Reduction: For those Part 15 bands that specify a maximum input power to the final stage (160 to 190 kHz and 535 to 1705 kHz), the transmit antenna efficiency is of high importance. The regulations specify a maximum antenna size for these bands, but do not define the antenna configuration. Size is specified as a limitation on the total length of antenna elements, lead in, and ground lines. The total length specified is about 1 percent of the wavelength

for these bands. That means that the antenna must be very short electrically, which generally means low radiation efficiency. Although the efficiency can be very low for such short antennas, it can be mathematically shown that the reduction in antenna gain for an electrically short antenna can be very small (for example, < 0.4 dB for an antenna 0.03 wavelengths long), but this assumes optimum antenna matching and ignores conduction losses. Loss reduction through low-loss matching of electrically short antennas is not difficult, but is often overlooked when designing Part 15 transmitters for these bands.

B. Noise Reduction

Noise is one of the major problems at frequencies less than 30 MHz. Any technique that reduces the ambient noise or recognizes, rejects, or corrects for it can yield very significant increases in reliable range.

1) Filtering: The frequencies below 30 MHz are usually considered ambient noise limited. Noise external to the receive circuits (atmospheric noise) limits the ultimate sensitivity. For many situations, this is true; but the noise sources are quite varied with diverse spectral distributions. For the most part, the noise is not "white" noise, i.e., non-coherent signals with energy equally distributed in frequency. For example, ignition noise is a very common type of noise prevalent at frequencies below about 3 MHz. This noise is characterized by a repetition rate dependent on the speed and type of engine. It may vary in intensity with vehicle motion and velocity. If recognized, this type of noise can be reduced through appropriate filtering and/or synchronization. Noise related to the 60 Hz line frequency, rotating machine noise, and other periodic noise is also amenable to filtering.

2) Noise Recognition: Frequencies below 30 MHz include not only noise but may also include noise-like signals, and even signals that appear close to the expected modulation. Consequently, noise recognition may be necessary before appropriate noise correction or reduction circuits can be applied. As Lily Tomlin's telephone operator Ernestine would say, "Is this the party to whom I am speaking?" It very necessary to determine if the "party," i.e., the signal, is the correct "party." This can be accomplished by various recognition algorithms, but one of the best methods may be by closed-loop acknowledgement of the signal. Since the transmitter power level is so low and the cost of the circuitry minimal, it makes sense to provide a complete dupiex (i.e., transceive) capability at each end of the link. even if data is only sent in one direction.

C. Coding

Coding is a sophisticated and potentially complicated method of dealing with error producing noise. It has not seen much application is Part 15 designs, which in the past have been fairly simple. Trellis coding, Viterbi coding, and other codes can be added to the basic digital protocol encoding to provide error correction. Coding often adds latency to the signal. Time is required to code the signal at the transmitter and to decode it at the receiver. But, for low data rates signals. this additional latency should rarely be a problem.

1) Spreading Codes: By spreading the signal over a wide band, interference from narrowband sources can be reduced by the so called processing gain provided by the spreading. There are essentially two spread spectrum techniques, direct sequence and frequency hopping. Direct sequence spreads the signal over a wide band of frequencies by modulating the carrier with a high-rate spreading signal in addition to the normal modulation. Frequency hopping is just like it sounds. In frequency hopping, the modulation is applied normally and the carrier frequency is "hopped" from frequency to frequency in a coded pattern. Direct sequence spread spectrum has not had much use at frequencies below 30 MHz, because of the problems inherent in maintaining phase and amplitude coherency over wide spreading bands. Frequency hopping on the other hand does work fairly well in overcoming such a signal environment especially if the hopping code is dynamically optimized. That is, the hopping signals are steered to frequencies that provide the best link bit error rate (BER) as in ALE.

With many things under processor control, there are many spreading and de-spreading techniques that might be used. Implementation of any of the possible techniques for Part 15 transmitters and receivers has not been very popular for low data rate links. This was because the cost for the spreading hardware and software was too high to justify for low data rates. As the cost for dedicated spectrum rises, this can be expected to change in the near future.

2) Modulation Codes and Data Rate: Coding can be used as a form of software automatic data rate control. By such means, the data rate can be reduced to overcome transitory link noise or increased if the link noise is lessens. If a link bandwidth is fixed by hardware constraints, the data throughput can be varied by changing the levels of coding complexity. Shannon has shown that the channel capacity is a function of not just channel bandwidth, but also the modulation complexity (see Fig. 7). Although the more complex modulation allows higher data rates for a given bandwidth, this is at the expense of a higher signal-to-noise requirement. So, if the link has an inherent method of sensing BER, the data rate can be automatically reduced or increased by changing the level of the code complexity. No hardware changes or hardware state changes would be necessary. The code rate can stay the same, but the transmitting levels and receiving level decoding will have finer graduations. This might mean more phase states beyond Quadrature Phase Shift Keying (QPSK), i.e., 8 level PSK instead of QPSK, 64 level Quadrature Amplitude Modulation (64QAM) instead of 32QAM, etc. This is a form of link adaptation to compensate for the varying link characteristics, which is essential for maximum range using low-power transmissions.

D. Adaption

On January 19, 1992, two amateur radio operators established a confirmed one-way link over a path distance of 1,500 miles from Massachusetts to Texas using a transmitter power level of 0.72 microwatts (-31.4 dBm) [4]. No esoteric equipment or processing was used. The transmission was on a frequency of 28.636 MHz using a Hewlett Packard model 608D signal generator as the signal source. Modulation was conventional On Off Keying (OOK) in international Morse code at five words per minute. The transmitter output went to three element beams 43 feet above ground. The receive site equipment was a conventional communications receiver with a narrowband filter (approximately 100 Hz). Signal recognition was done manually.

As spectacular as this may seem, it fits within what could be expected from the path loss calculations for free-space conditions (Path Loss = $P_t/P_r = A_rA_t/d^2\lambda$.. where P_t = power transmitted, P_r = power received, A_r = effective receive antenna area, A_t = effective transmit antenna area, λ = the signal wavelength, and d = the distance between the transmit and receive antennas) to a noise-free receiver of about 100 Hz bandwidth. The receiver was not noise free, and it was not a free space situation. But, the path conditions were almost as ideal as that expected from free space. Considerable effort went into selection of the optimum time, frequency, noise conditions, and link path. By adapting the link parameters to the path, it is apparent that a low-power link can be established and maintained in the face of almost any obstacle.

1) Signal Path Selection: Propagation path selection is probably a fixed design consideration for most simple Part 15 links. Once the transmitting and receiving situations are defined, only a number of propagation paths may be possible for a given operating frequency. But, if the operating frequency is flexible, many paths may be possible. For example, if the link is completely within a building, some frequencies may penetrate the building material, but be susceptible to power line noise. Other frequencies may not penetrate the building material, but may be conducted by the building structure from transmission to reception point. Another frequency may be reflected from point to point to complete the link path. By supplying frequency agility to the Part 15 link, much of the spectrum available for unlicensed operation can be used to overcome the path loss limitations in each application.

2) Clear Channel Determination: One of the underutilized techniques for noise minimization is clear channel recognition. Part 15 links are unencumbered by frequency assignments. Any clear channel is "fair game" as long as it is not a restricted channel (see Table 3) or in use by a licensed station. A simple scanning receiver can be used to determine a clear channel frequency. With a duplex link, this information can be shared at both ends of the link. The link can then be moved to this frequency and move as necessary to other frequencies where noise is less. Again, the cost of this capability will be low because of the low cost of components for these frequencies. But, the need for channel determination may still not be worth the effort in some cases.

A simpler approach to clear channel determination may be to design for operation on frequencies unlicensed for operation in a given area. This feature can be made part of the design. The user can select a particular operating frequency simply by setting a switch corresponding to the geographic location of the

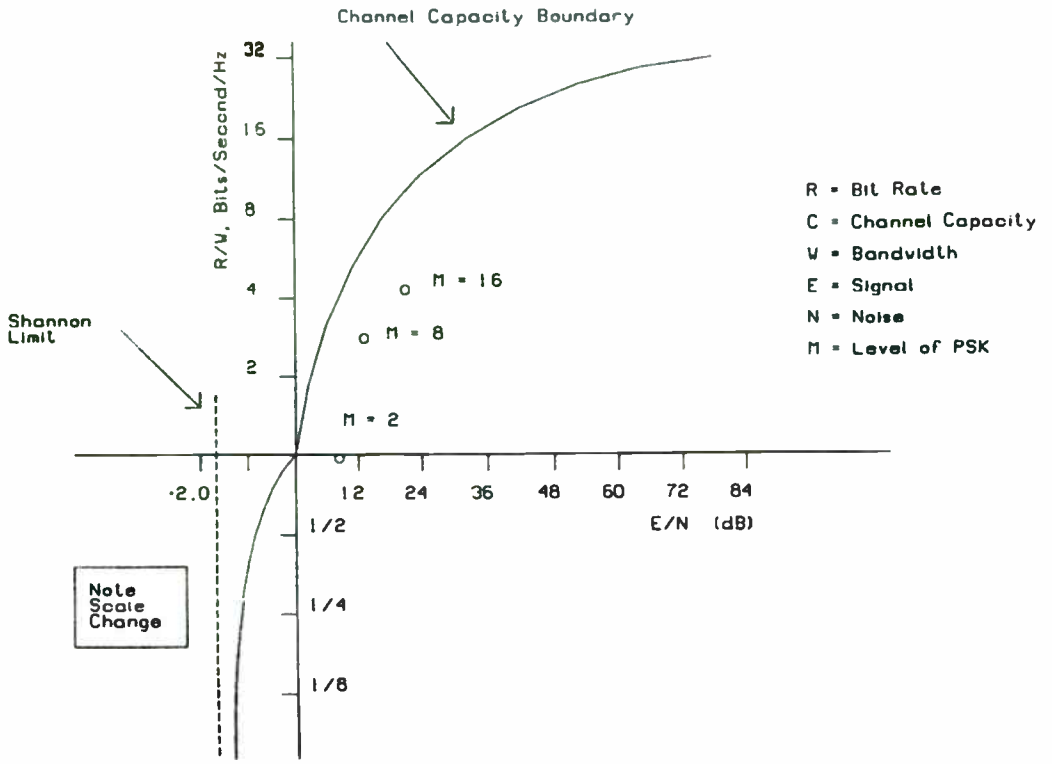

Fig. 7. The Bandwidth - Efficiency

link. The complexity of such an arrangement can be fairly simple for operation in the AM broadcast band, but may be impractical for other bands such as the international (short wave) bands near 9 MHz.

E. Path Loss Reduction

Design features that reduce the path loss are not easy to implement at these frequencies because the signal path is often not a direct line-of-sight path. The actual path may be by conduction or reflection from objects out of sight to the link user. Knowledge of low frequency propagation characteristics is often essential for minimizing the path loss. For example, the receive and transmit antennas should be removed as far as possible from the vicinity of most objects. The near field (inductive) field range is inversely proportional to frequency. At 1 MHz, the near field energy is still significant hundreds of meters from the antenna. This can become a problem or a benefit depending on how that near field energy is coupled between the transmitter and receiver locations.

1) Path Maximizing: It is always possible to extend the range of a Part 15 link by use of relays. Since the power level is low, a full duplex Part 15 repeater can be built at low cost. Also, since there is no limit on the number of Part 15 repeaters or limits on the amount of spectrum used, it would be possible to establish a two-way Part 15 link over almost any path distance.

V. TESTS OF SOME DESIGN POSSIBILITIES

A narrowband link was designed as a simple test of what might be done with a Part 15 narrowband AM broadcast band link. It was designed to transmit OOK signals at a maximum bit rate of approximately 15 bits per second. The transmitter was a crystal-controlled transmitter operating at a carrier frequency of 1.17175 MHz. This is 1.75 kHz above the U.S. assigned AM broadcast frequency of 1.17 MHz and so was still within the 10 kHz bandwidth of the normal AM frequency assignment. In this area of the country (San Antonio. TX), it was not assigned.

The receiver made use of extreme front-end filtering provided by a simple crystal filter centered at the frequency of interest. This was an attempt to reduce the front-end intermodulation noise, which can easily be the limiting factor for noise at this frequency (see Fig. 8).

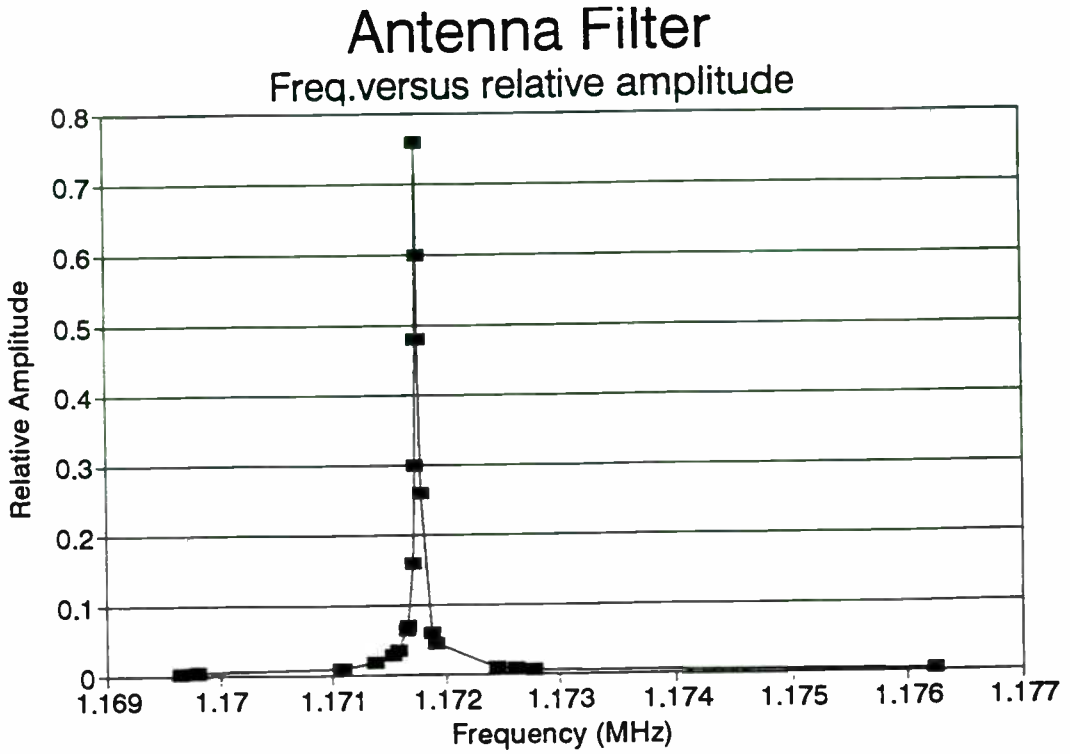

Fig. 8. Narrowband OOK Receiver Input Filter Response

A. Antenna Design

Many antenna configurations were considered that would make the most efficient use of the total 3 meters allowed by Part 15 regulations. The eventual design was a variant of the small loop. Small loops are inherently efficient if the matching network can match the extremely low radiation resistance (approximately 0.2 Ohms for this antenna) efficiently. That problem was overcome somewhat by making the matching network part of the antenna. Fig. 9 shows the transmitter and 3 meter antenna designed and built for the test. Unloaded Q was measured at 300. Of course, this results in a very narrow resonant bandwidth, but this was not a problem when transmitting at a 1 Hz rate.

B. Transmitter Design

The transmitter consisted of a loop antenna fed by a Class C single-stage amplifier limited to an input power of 100 milliwatts. The drive to the amplifier was supplied by a crystal oscillator at 1.17175 MHz with output controlled by an RF switch. The switch was keyed on and off by a square wave generator at a rate of approximately 1 Hz (see Fig. 10). Power to the transmitter was supplied by a 12-Volt battery. No connections to an external power source or ground were made.

C. Receiver Design

Fig. 11 shows the receiver designed and assembled for this test. The receiver was basically an automobile AM broadcast radio with input filtering between the antenna and the receiver input. The size of the shielded loop antenna was increased empirically until the receiver sensitivity was limited by the input noise passing through the crystal filter. The crystal filter 3 dB bandwidth was measured at 15 Hz. Output from the receiver was supplied to a tone decoder (National Semiconductor LM567) which detected a particular tone (coherent beat) and changed states for a signal-to-noise level as low as -3 dB.

D. Test Results

The transmitter/antenna shown in Fig. 9 was placed approximately 1 meter off the ground and the receiver shown in Fig. 11 moved from point to point until the received signal-to-noise ratio dropped to about 6 dB. With the transmitter final amplifier input power measured at 0.075 Watts, a 6 dB SN signal was received over 1.6 kms away. This test was performed in a rural environment at mid-day during the summer. Receiver noise at night did not increase appreciably, but nearby summer thunderstorms did produce transient filter ringing 20 dB higher than the normal receive noise level.

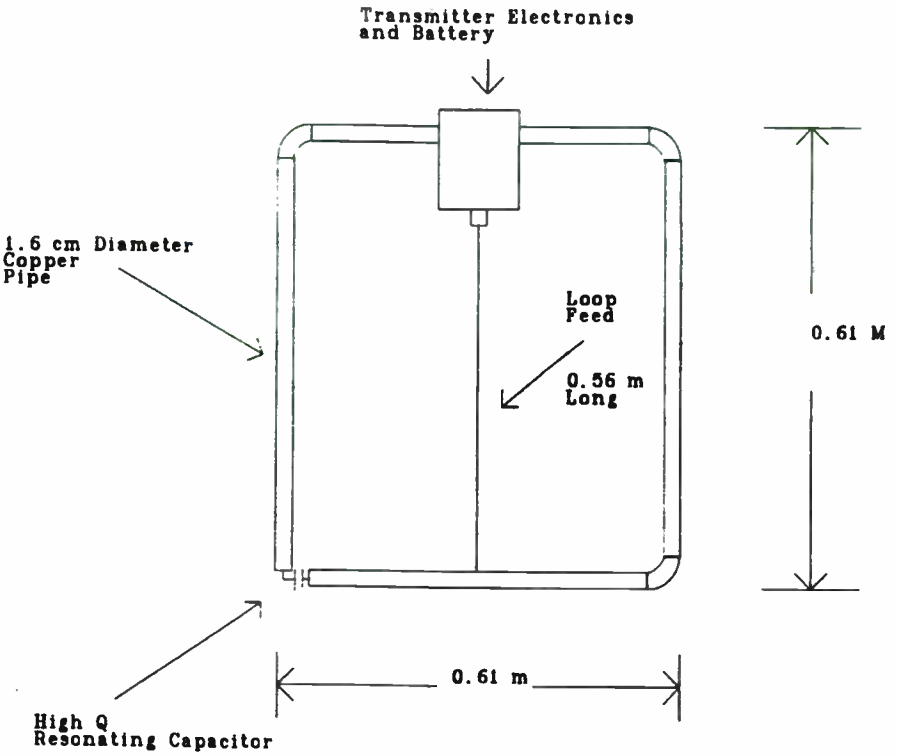

Fig. 9. Broadcast Band Test Transmitter and Loop Antenna

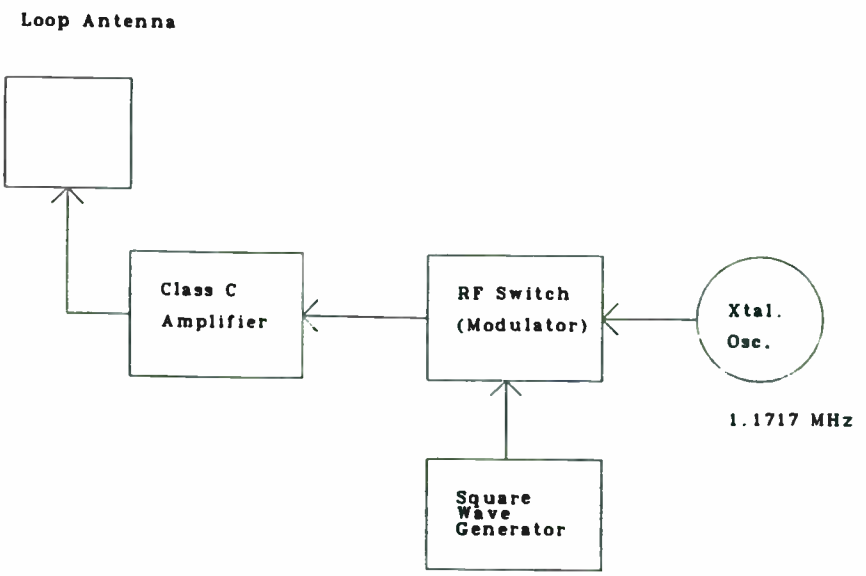

Fig. 10. Broadcast Band OOK Test Transmitter

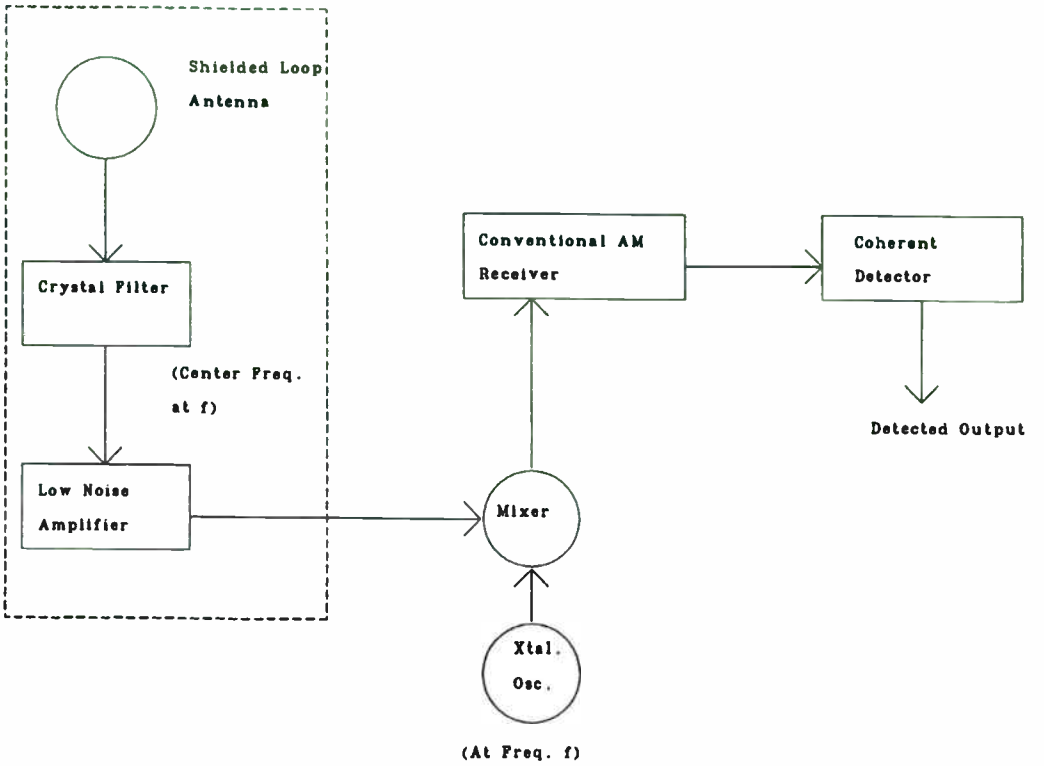

Fig. 11. Narrowband OOK Test Receiver

VI. CONCLUSIONS

Part 15 of the FCC regulations provides many frequencies below 30 MHz that can be used to design low-cost communications links. These frequencies provide superior non-line-of-sight operation, but are susceptible to interference from variable ambient noise as well as the signal normally licensed to these frequencies. The variable nature of the characteristics of these frequencies over wide bandwidths (> 100 kHz) makes design of wideband links difficult, but not impossible. Narrowband low data rate links can be designed to make use of the long distance potential of these frequencies.

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Personal Area Networks (PAN): Near-Field Intra-Body Communication

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ABSTRACT

A Personal Area Network (PAN) has been developed to allow wearable electronic devices to exchange data by capacitively coupling modulated picoamp currents through the body. Cellular phones, personal digital assistants (PDA), pocket video games, and pagers are examples of wearable devices that provide personal communication and entertainment. Networking these devices reduces I/O redundancies and allows new conveniences and services. A low frequency carrier (< 1 MHz) is used so no energy is propagated, minimizing remote eavesdropping and interference. A prototype PAN system allows people to exchange electronic business cards by shaking hands.

1. INTRODUCTION

A. Why A Personal Area Network?

Cellular phones and laptops have liberated people from offices, providing mobile workers instant access to customers, vendors, and databases. However, the inability of wearable electronic devices to exchange data leads to inefficiencies and limits their usefulness. For example a mobile computer user should not have to carry a cellular phone *and* a cellular LAN; phone numbers retrieved from a PDA should not have to be manually typed into a cellular phone; and a message watch should not have to be programmed by four micro switches when a full sized QWERTY keyboard is nearby. Networking these devices would alleviate these inconveniences and allow new features; a watch is too small to contain a multimedia computer, but is large enough to contain a microphone, display, and camera. An I/O rich watch could be networked to a fast powerful computer located in a waist pack or pocket.

A network is commonly divided into layers [1]. The work presented here concerns the physical layer of the PAN; examining the electrical properties of the communication channel. PAN devices communicate by electrostatically coupling picoamp currents through the body. The PAN uses the salty blood-filled body as a "wet wire" to conduct the modulated currents. The body internally has a resistance of about 200 ohms from head to toe [2]. A low frequency carrier (100 kHz to 1 MHz) is used to capacitively couple the current into the body, eliminating the need for direct (resistive) contact with the skin.

B. Comparison to Infrared and Far-Field

Near-field coupling is superior to infrared and far-field methods for PAN applications. Infrared requires line-of-sight which is not practical for devices located inside wallets, purses, and pockets. Far-field (radio) propagation falls off with distance squared (isotropic transmitter), while near-field falls off with distance cubed, making near-field coupling less susceptible to eavesdropping and interference. Far-field transmission is subject to regulations and licensing that vary from country to country. Near-field communication avoids these complications. The PAN prototype which is slightly larger and thicker than a credit card, has a field strength of 350 pV/m at 300 meters, 86 dB below the FCC allowable field strength.

Near-field communication may be more energy efficient than far-field since power consumption generally increases with frequency. Any increase in the carrier frequency above that required to contain the information represents wasted energy. The PAN prototype operates at 330 kHz at 30 volts with 10 pf electrode capacitance, consuming 1.5 mW to charge and discharge the electrode capacitance. A majority of this energy is conserved (recycled) by using a resonant LC tank circuit.

Near-field communication lends itself to greater integration than far-field since the carrier can be generated directly by an inexpensive microcontroller. The PAN demonstration transceiver uses a Microchip Technology PIC16C71 ($3.50 quantity 10K).

3. PAN COMMUNICATION CHANNEL

Figure 1 shows a PAN transmitter communicating with a PAN receiver. Each device has a pair of electrodes (**tb** and **te**, **rb** and **re**) that can be incorporated into shoes, watches, credit cards, and

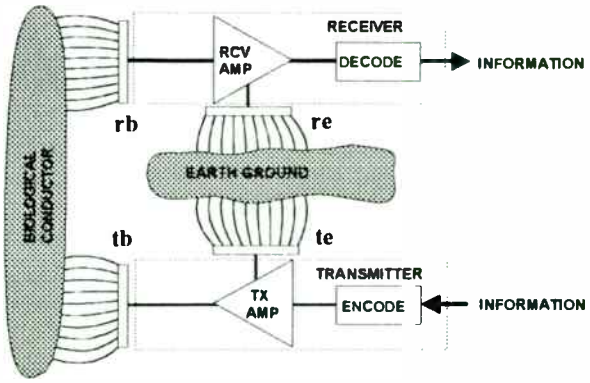

Figure 1. Block diagram of a PAN system. Information is encoded by modulating an electric field which capacitively couples to the body. The body conducts the picoamp current to a receiver which demodulated the signal. The earth ground provides a return path for the signal.

wallets. The PAN transmitter capacitively couples a modulated picoamp displacement current through the human body to the receiver. The return path is provided by the "earth ground" which includes all conductors and dielectrics in close proximity to the PAN devices. The earth ground needs to be electrically isolated from the body to prevent shorting of the communication circuit. For example, in one experiment standing barefoot reduced communication between wrist mounted devices 12 dB.

In Figure 2 the PAN transmitter and receiver are modeled as an oscillator and a differential amplifier, respectively. The basic principle of a PAN communication channel is to break the impedance symmetry among the transmitter electrodes (**tb** and **te**) and receiver electrodes (**rb** and **re**). The intra-electrode

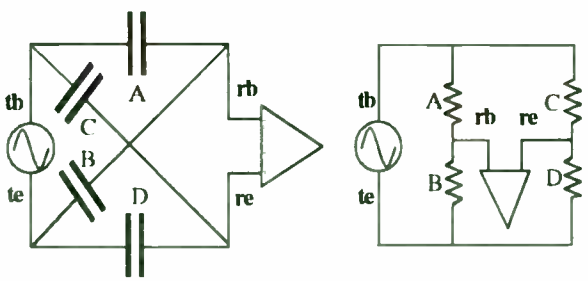

Figure 2. Electrical lumped model of PAN transmitter (oscillator) and receiver (differential amp). The impedances are rearranged to reveal a Wheatstone bridge configuration. Any imbalance of the bridge causes a potential across the receiver.

impedance of the devices are ignored since the oscillator is a load on an ideal voltage source and the differential amplifier is modeled as an open circuit. The four remaining impedances are labeled A, B, C, and D.

The circuit is rearranged to show that PAN device communication works by breaking the impedance symmetry between the four electrodes. The circuit is a Wheatstone bridge where any imbalance of the relationship

$$A/B = C/D \qquad (1)$$

causes a potential across the receiver. Since the ratios must be *exactly* equal to null the circuit, and body-based PAN devices are constantly in motion, there will always be an electrical communication path, as long as the receiver is sensitive enough to detect the imbalance.

The concept of a body and environment electrode is introduced to identify the impedance asymmetry. The body electrode (**tb** and **rb**) is the electrode in closer proximity (lower impedance) to the body. Correspondingly, the environment electrode (**te** and **re**) is the electrode in closer proximity to the environment. For a watch, the face is the environment electrode and the backplate (near the skin) is the body electrode. For a shoe insert, the top is an excellent body electrode due to its large area and close proximity to the body (a sweaty foot is event better!) and the bottom is an excellent environment electrode due to it's large area and proximity to the earth. For a credit card placed in a pocket, the body electrode is the side that faces the body, and the environment electrode is that which faces outward (away from the body).

4. PAN LOCATIONS AND APPLICATIONS

Figure 3 shows typical locations for PAN devices. Head mounted devices can include headphones, hearing aids, microphones, and head mounted displays. Shirt pocket devices can serve as identification badges. The wrist watch is a natural location for a display, microphone, camera, and speaker. A waist pouch can carry a PDA, cellular phone, keypad, or other large devices. PAN medical sensors can provide EKG, blood pressure, and respiratory rate monitoring. Pants pockets are a natural location for wallet based devices. Shoe inserts can be self-powered, capturing energy from walking [2], and provide a data link to remote PAN devices located in

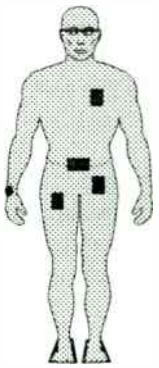

Figure 3. Locations and applications for PAN devices include head mounted display, headphones, identification badge, cellular phone (waist pack), credit and phone cards (wallet), watch with display, microphone, and speaker, and power sneakers (self powering computer shoe inserts).

the environment, such as workstations and floor transponders that detect the location and identity of people.

5. PAN PROTOTYPE

A PAN prototype, shown in Figure 4, has been developed to demonstrate the digital exchange of data through the human body using battery-powered low-cost electronic circuitry. The receiver is a current amp (TLO84, gain=10^6) followed by an analog bipolar chopper (4066, TLO84) controlled by a digital microcontroller (PIC16C71). The detector synchronously integrates the tiny received displacement current (e.g., 50 pA, 330 kHz) into a voltage that can be measured by the microcontroller's analog-to-digital converter (50 kHz, 8 bits, +5 volts full scale). The analog components and microcontroller may be combined into a single CMOS integrated circuit, providing a low-cost integrated PAN transceiver.

The transmitter is an LC tank (Q=6) made from a surface-mount inductor and the inherent electrode capacitance. The tank circuit produces a clean sine wave output from a square wave input, minimizing RF harmonics, and boosts the output voltage in proportion to the Q of the tank. The transmit voltage can also be digitally programmed by varying the pulse width of the tank driver. The integrator is discharged after every message bit (integrate-and-dump filtering) to minimize inter-symbol interference [3].

6. CHANNEL CAPACITY

A communication network is judged primarily by channel capacity, with a theoretical limit defined by the Hartley-Shannon law

$$C=B\log(1+S/N) \qquad (2)$$

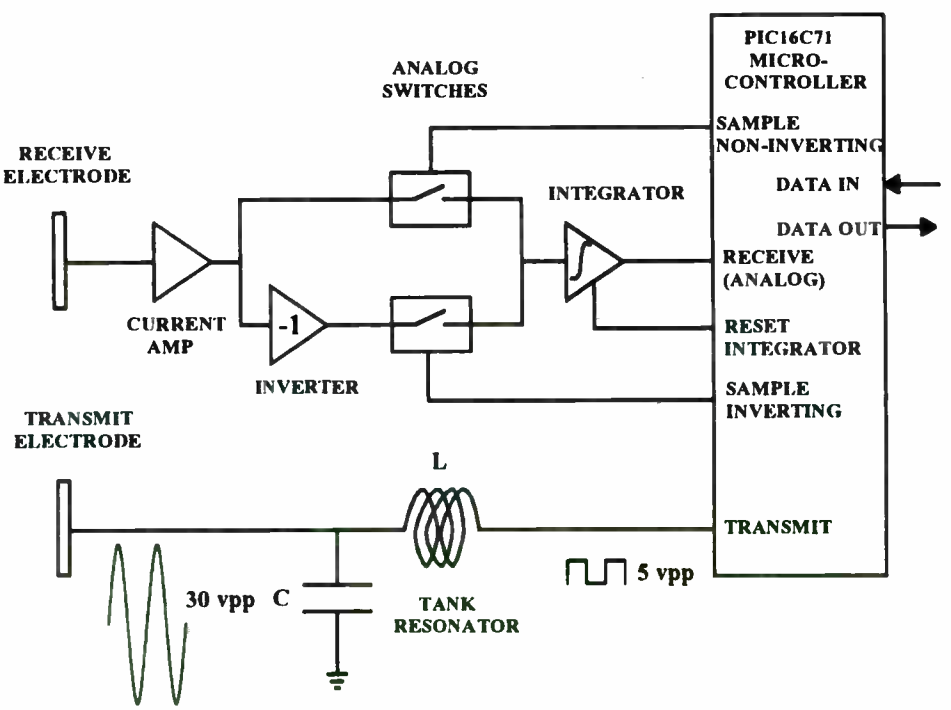

Figure 4. Block diagram of half-duplex PAN transceiver. Microcontroller controls analog switches to synchronously rectify and integrate amplified signal picked up by receive electrode.

where C is channel capacity in bits/second, B is bandwidth, S is signal, and N is noise. The 3 dB bandwidth of the prototype PAN receiver is 400 kHz (100 kHz to 500 kHz), resulting in a maximum theoretical channel capacity of 417 kbits per second, assuming a robust signal-to-noise ratio of 10. The PAN transceiver prototype implements a modest 2400 bit per second half-duplex modem.

7. MODULATION STRATEGIES

Two modulation strategies were examined for PAN communication; on-off keying and direct sequence spread spectrum. On-off keying turns the carrier on to represent a message bit one, and turns the carrier off for a message bit zero. The signal-to-noise performance is improved by increasing the transmit voltage. Direct sequence spread spectrum modulates the carrier with a pseudo-noise (PN) sequence, producing a broadband transmission much greater than the message bandwidth. Symbol-synchronous PN modulation is used where a message bit one is represented by transmitting the entire PN sequence, and a message bit zero is represented by transmitting the inverted PN sequence. The signal-to-noise performance increases with the length of the PN sequence.

The prototype hardware detects both on-off keying and direct sequence spread spectrum, determined by microcontroller coding. For on-off keying the bipolar chopper switches are driven at the carrier frequency and the integrated result is compared to a fixed threshold to determine the value of the message bit. Quadrature detection is implemented by performing two sequential integrations at 90 degrees phase per message bit. For spread spectrum the switches are driven by the PN sequence (100 elements long) and the integrated result (the correlation) is compared to two thresholds. If the correlation is greater than a positive threshold, the message bit is one. If the correlation is less than a negative threshold, the message bit is zero. If the correlation is between these thresholds (the dead zone) no message bit is received.

Once the message has been successfully received and demodulated, the microcontroller transmits the message to a host computer over an optical link (not shown), which electrically isolates the transceiver allowing evaluation and debugging independent of an electrical ground reference.

8. THE BUSINESS CARD HANDSHAKE

The demonstration prototype consists of a battery powered transmitter and receiver, and a host computer running a terminal program. The PAN prototypes are mounted in aluminum cases measuring 94 mm x 120 mm x 37 mm. The lids are electrically isolated from the cases and serve as electrodes. The transmitter contains a microcontroller that continuously transmits stored ASCII characters representing an electronic business card. The devices are located near the feet of two participants, simulating PAN shoe inserts.

When the participants are in close proximity, particularly when they shake hands, an electric circuit is completed, allowing picoamp signals to pass from the transmitter to the receiver through the participants bodies, and back through the earth ground. ASCII characters are sent to the receiver, demodulated and sent via optical link to the host computer where they are displayed.

9. CONCLUSION

A novel means to perform digital communication between wearable electronic devices using electric fields has been demonstrated. The trade-offs among cost, speed, size, power, and operating range must be further studied and quantified in order to engineer practical PAN devices.

The sensitivity and bit rate must be increased in order to realize a watch-sized PAN transceiver. The application of modem digital communication techniques may deliver PAN channel capacities of 100 kbits per second, which can be further enhanced with data compression. The low frequency carrier of near-field communication makes direct sequence spread spectrum both practical and desirable.

The concept of power sneakers is intriguing. Shoes are something that we always carry with us, are unlike to lose, and are hard to steal. Networked shoes could keep track of who we've met, where we've been, and what we've done. When we walk by a store, advertisements could upload, sticking like digital chewing gum to our shoes. Homework assignments, grades, shopping lists, errands, and reminders could be automatically exchanged among family members during meals. Privacy issues are raised when personal data can effortlessly be exchanged. Near-field networking does offer some inherent security over far-field methods. However, as with any data communication system, there are trade-offs among access, convenience, and security.

Ultimately PAN devices will be judged a success

when they appear as common objects that perform magic; from picture telephone "Dick Tracy" watches to self-powered smart sneakers that seamlessly interconnect us to a world-wide network of information and communication.

ACKNOWLEDGMENT

This research was sponsored in part by Hewlett-Packard and the Festo Didactic Corporation and was conducted at the Physics and Media Group of the MIT Media Laboratory in collaboration with Professor Neil Gershenfeld.

PATENT PENDING NOTIFICATION

This paper reports on work that is part of the US Patent Application, "Non-Contact System For Sensing and Signaling by Externally Induced Intra-Body Currents" by Gershenfeld, N., Zimmerman, T.G., Allport, D., filed May 8, 1995, and assigned to MIT.

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Accurate and Reliable Adjacent Channel Power and Burst Power Measurements on Digital Wireless Transmitters

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Richardson, Texas

Abstract: Accurate measurements of today's digital wireless transmitter characteristics require special equipment and measurement techniques. Adjacent channel power due to transients and burst power versus time measurements are not required for older analog systems such as the Advanced Mobile Phone System (AMPS). Spectral splatter, or adjacent channel interference, outside the defined communication channel is of particular concern to RF frequency planners since it affects overall system capacity and performance. Users should be able to communicate on their assigned channels without adjacent channel interference from other transmitters. Interference degrades the bit error rate (BER) of a digital communication system and thus the voice quality to the user. Transients generated by bursting the TDMA carrier on and off during its assigned time slot increases the adjacent channel interference. Accurate measurements of both adjacent channel power and burst rising/falling edges are critical to understanding and minimizing these important parameters.

This paper will discuss the measurement techniques used in a typical spectrum analyzer and the Anritsu MS8604A Digital Mobile Radio Transmitter Tester. A detailed example will be presented based on the NADC standard IS-55-A titled, "Recommended Minimum Performance Standards of 800 MHz Dual Mode Mobile Stations." A summary of the relevant specifications from IS-55-A is presented in Figures 1 and 2. The relative merits of each measurement technique for adjacent channel power (ACP) and burst rise/fall time will be discussed. Certain inherent limitations in the spectrum analyzer test methods will be detailed in this paper.

Burst Power Measurements

TDMA systems require good transmission power versus time characteristics in order to minimize interference with other channels . This interference can be either in the time domain or the frequency domain. In the time domain, interference may result from bursts overlapping into adjacent time slots. In the frequency domain, spectral sidelobes from both the modulation characteristics and bursting of the signal may cause power to fall into adjacent channels. Measurements used to characterize a wireless transmitter's

IS-55-A Digital Specifications

- Frequency Stability: +/- 200 Hz
- Carrier Switching Time: +4/-20 dB of the Mean Output Power within 3 symbol periods
- RF Output Power: 28 dBm (0.6 watts) Nominal and Within +2/-4 dB of Mean Burst Power Over Symbols 6 Through 162 (at least 140 symbols)
- Modulation Accuracy:
  - RMS Vector Error: 12.5% Maximum
  - EVM (first 10 symbols): 25% Maximum
  - Origin Offset:-20 dBc Maximum

Figure 1

IS-55-A Digital Specifications Cont.

- Occupied Bandwidth: 30 KHz Maximum
- Adjacent Channel Power Due to Modulation and Out of Band Power (ACP) Due to Transients:
  - -26 dB at 30 KHz Offset
  - -45 dB at 60 KHz Offset
  - -45 dB or -13 dBm (lower) at 90 KHz Offset
- Conducted Harmonic and Spurious Emissions:
  - -13 dBm in the 824-849 MHz TX Band
  - -80 dBm in the 869-894 MHz RX Band

Figure 2

power versus time characteristics include carrier power, burst rise time, burst fall time, and carrier off power. Figure 3 shows a typical transmitter burst power measurement for half of a frame since the pattern repeats (time slots 1/4, 2/5 and 3/6 are used in pairs for a full rate vocoder).

RF power output or carrier power is defined to be the mean power transmitted during the active part of the burst (after the rise time) as specified by each system standard. Some standards specify the start and stop symbols for the power measurement. IS-55-A specifies that the mean power is to be measured using symbols 6 through 162 as shown in Figure 4.

Carrier off or leakage power is defined as the mean power in all inactive time slots in a TDMA frame. The carrier on/off ratio is important since it sets the background interference level through which the base station receiver must receive transmissions on other channels.

Burst rise and fall times are usually displayed with a burst mask showing the specification limits which provide a "pass" or "fail" criteria. The burst power measurement with a rising edge view is shown in Figure 5. The display time axis is in symbol periods rather than μsec for convenience since the standard is specified in symbols.

Adjacent Channel Power Measurements

Frequency domain interference must be minimized in digital communication systems so that strong signals in adjacent channels do not mask weaker signals in the assigned frequency channel. ACP is affected by the digital modulation scheme chosen, the frame repetition rate, and the burst rising/falling characteristics of the transmitter. Many wireless system standards require separate ACP measurements for the mean power due to modulation and the peak power due to transients. Mean power due to modulation measures the spectral sideband levels of the continuous spectra generated by both the digital modulation method ($\pi/4$ DQPSK, GMSK, GFSK, etc.) and the sin(x)/x pulse spectrum. Peak power due to transients measures the transient spectra generated by the rising and falling edges of the burst. Figure 6 shows the spectrum of a $\pi/4$ DQPSK modulated signal with its spectral sidelobes spilling into adjacent channels.

Interference close to the carrier is defined as adjacent or alternate channel interference. Interference far from the carrier frequency is defined as spurious emissions which are measured separately. ACP is defined as the ratio of the amount of leakage power in an adjacent channel to the total carrier power in the assigned channel. ACP is usually specified in dBc relative to the carrier power, although some standards do specify ACP in absolute power levels (dBm).

Spectrum Analyzer Methods

Spectrum analyzers have recently added a limited capability to make burst power and ACP measurements by adding time-gated analysis. Downloadable software is used to control the spectrum analyzer and perform measurements according to the various existing international wireless standards. There are, however, certain

RF Power vs. Time - Frame View

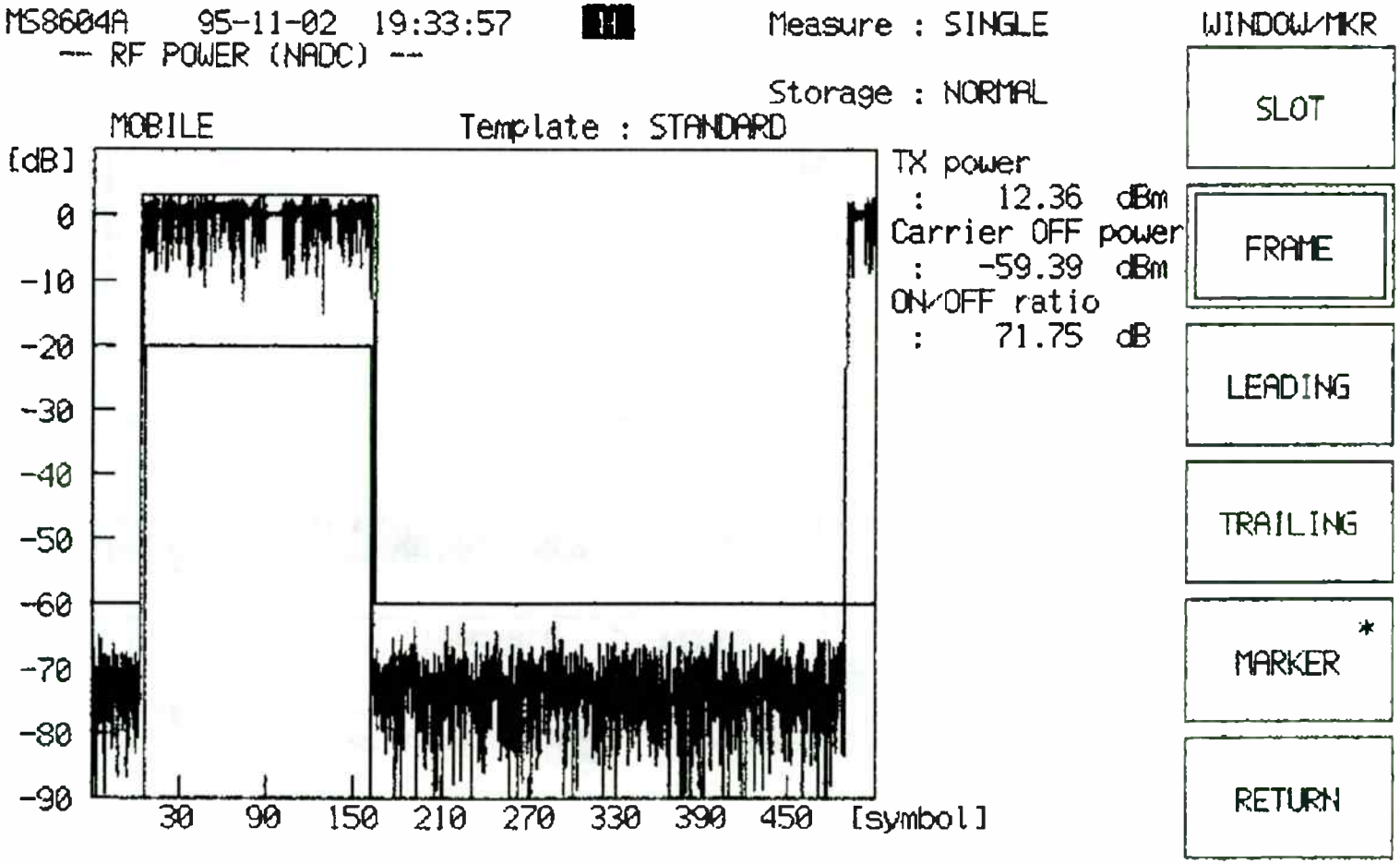

Figure 3

RF Power vs. Time - Slot View

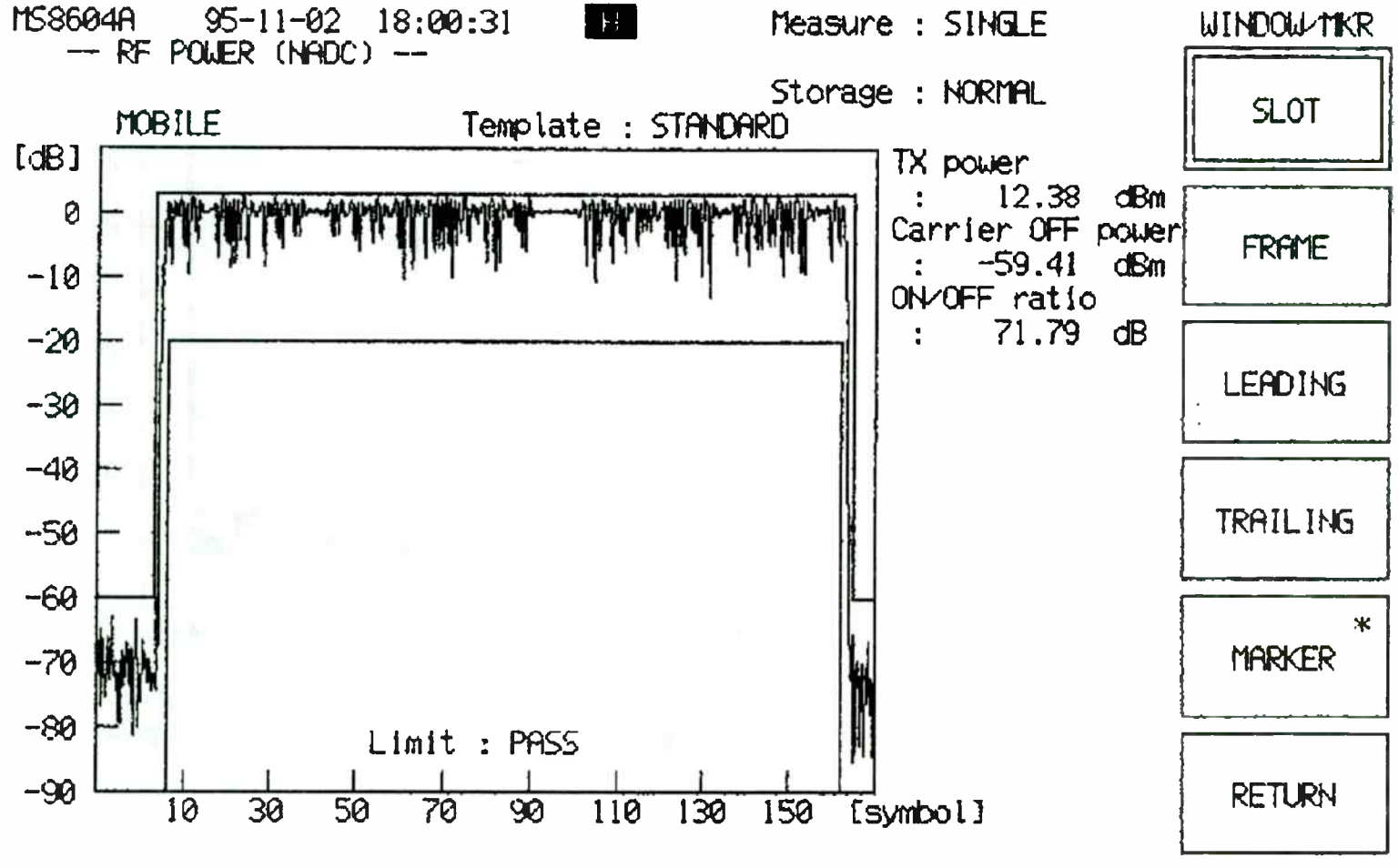

Figure 4

RF Power vs. Time - Rising Edge

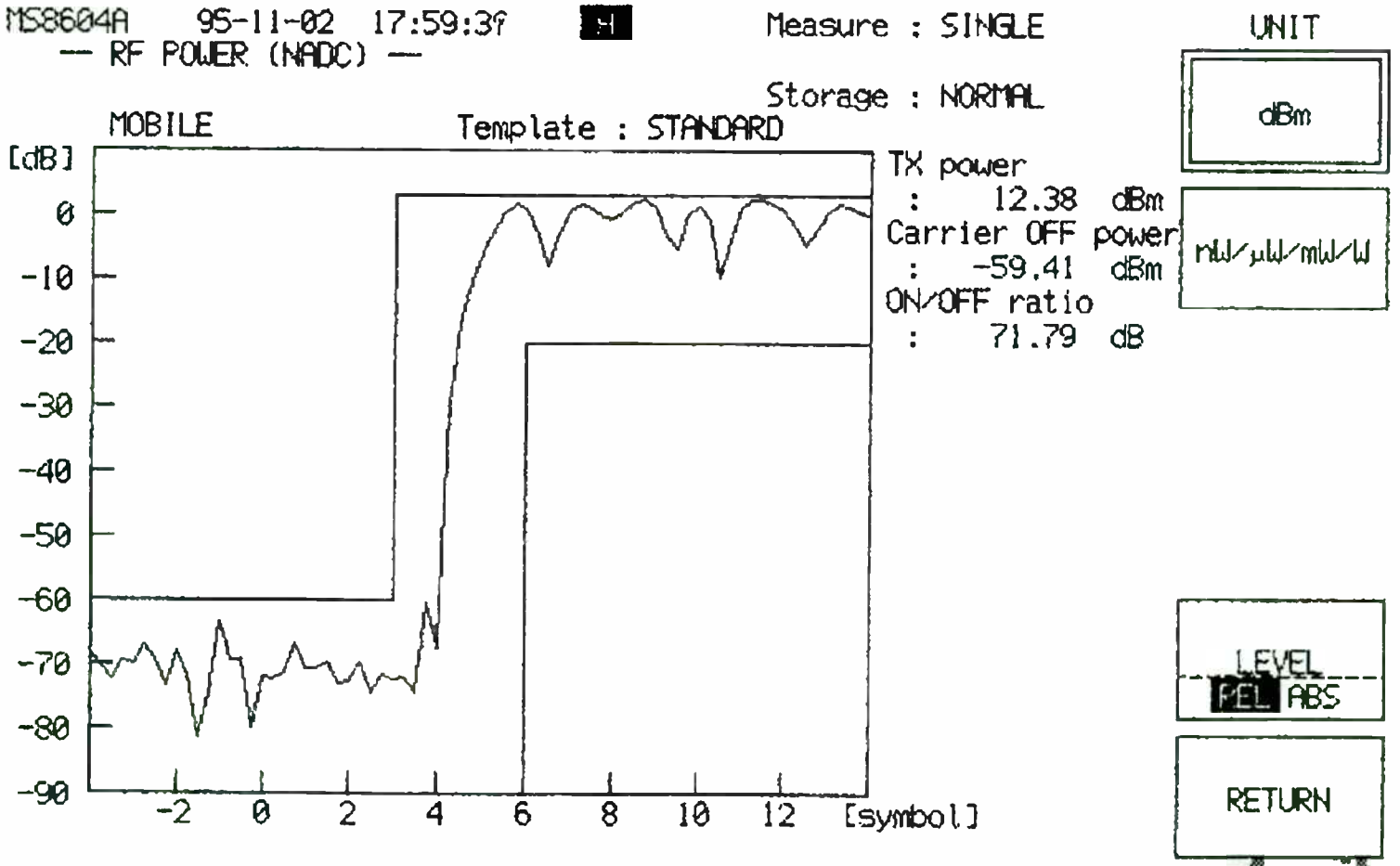

Figure 5

Adjacent Channel Power (ACP)

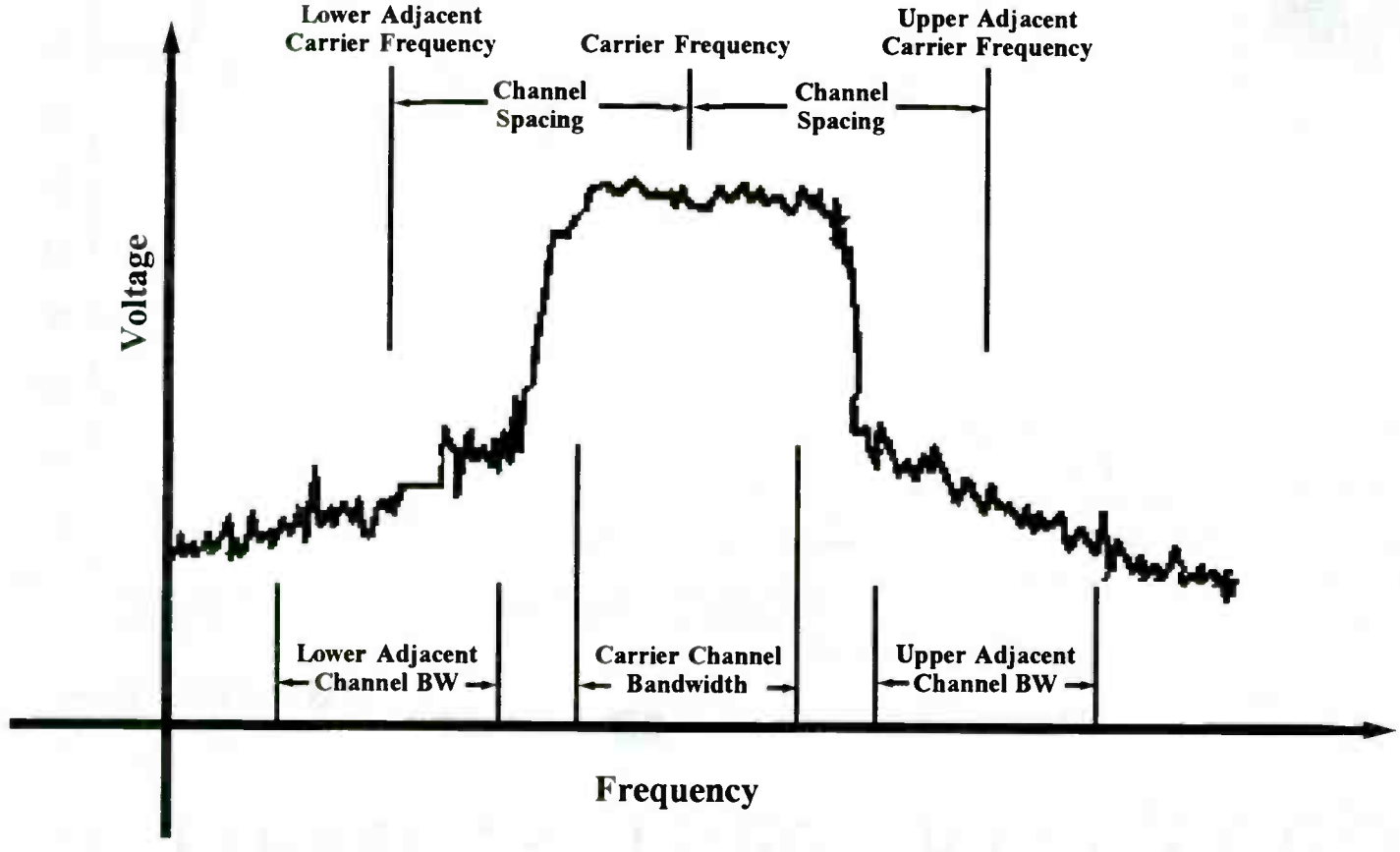

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Figure 6

limitations to the spectrum analyzer test methods which will be described below.

The spectrum analyzer is a swept tuned receiver which peak detects the signal in the resolution bandwidth as it is swept across a specified frequency range. A simplified block diagram of a spectrum analyzer is shown in Figure 7. The detected voltage is converted to power. Incoming RF signals are downconverted to an IF by a swept tuned local oscillator (LO), filtered by the resolution bandwidth filter, amplified by a log amplifier, and peak detected by an envelope detector. The demodulated video signal is filtered by the video bandwidth filter where it is integrated by the filter's time constant. The resulting signal is sampled by an analog-to-digital converter (A/D), quantized, stored in memory, and displayed as points on the video display CRT. Each point in the swept trace is the total power in the resolution bandwidth.

Time domain measurements on TDMA carriers may be performed by setting the spectrum analyzer to zero span mode. Zero span mode implements a fixed tuned receiver tuned to the carrier frequency which results in an output similar to an oscilloscope. The envelope of the carrier may be viewed directly on the display. Time measurements using the traditional spectrum analyzer are poor, and the burst shape of each particular time slot cannot be measured using this method.

Time-gated spectral analysis is required for power versus time and ACP measurements on TDMA signals since the carrier is only on for short periods of time. An analog switch is inserted between the envelope detector and the video filter. The switch is closed by a TTL level trigger signal (the GATE) which is synchronous with the frame rate of the TDMA carrier. The spectrum analyzer can be triggered anywhere within the frame by delaying the trigger signal with respect to the beginning of the frame as shown in Figure 8. Each slot within the frame may be measured by selecting the appropriate delay value. Figure 9 shows how the instantaneous spectrum of the burst varies with time over the burst period.

The resolution bandwidth, video bandwidth, and sweep time are key parameters which must be carefully selected when performing gated measurements. Resolution bandwidth determines the frequency resolution which is the ability to separate two signals into distinct responses. Video bandwidth determines the amount of smoothing of the noise on the signal. Sweep time should be chosen to show the desired time interval with the maximum time resolution.

Total power detection is required is required to make ACP measurements on signals that contain both the signal and noise. A narrow video bandwidth will cause erroneous total power measurements due to noise peak compression. The video bandwidth should be much wider (theoretically > 10 times) than the resolution bandwidth for total power detection.

The combination of the resolution and video bandwidths determines the pulse response of the spectrum analyzer. Good pulse response is critical to the time resolution and amplitude accuracy

Spectrum Analyzer Block Diagram

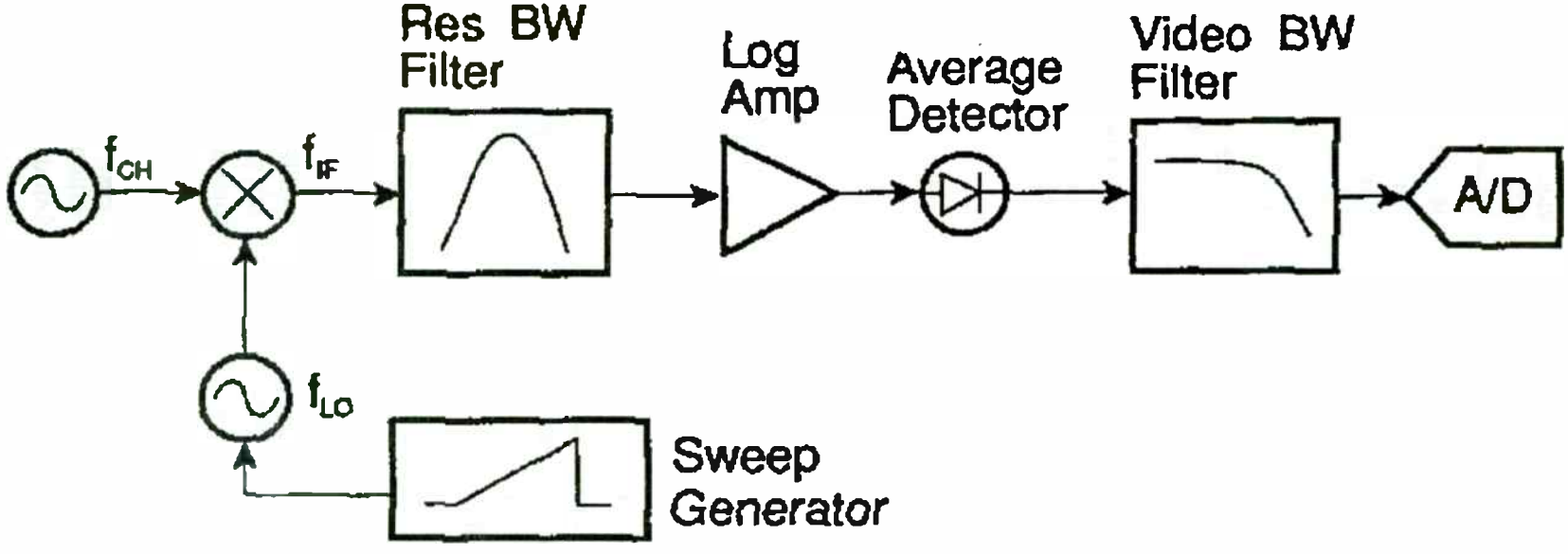

Figure 7

Time-Gated Spectrum Analyzer Measurements

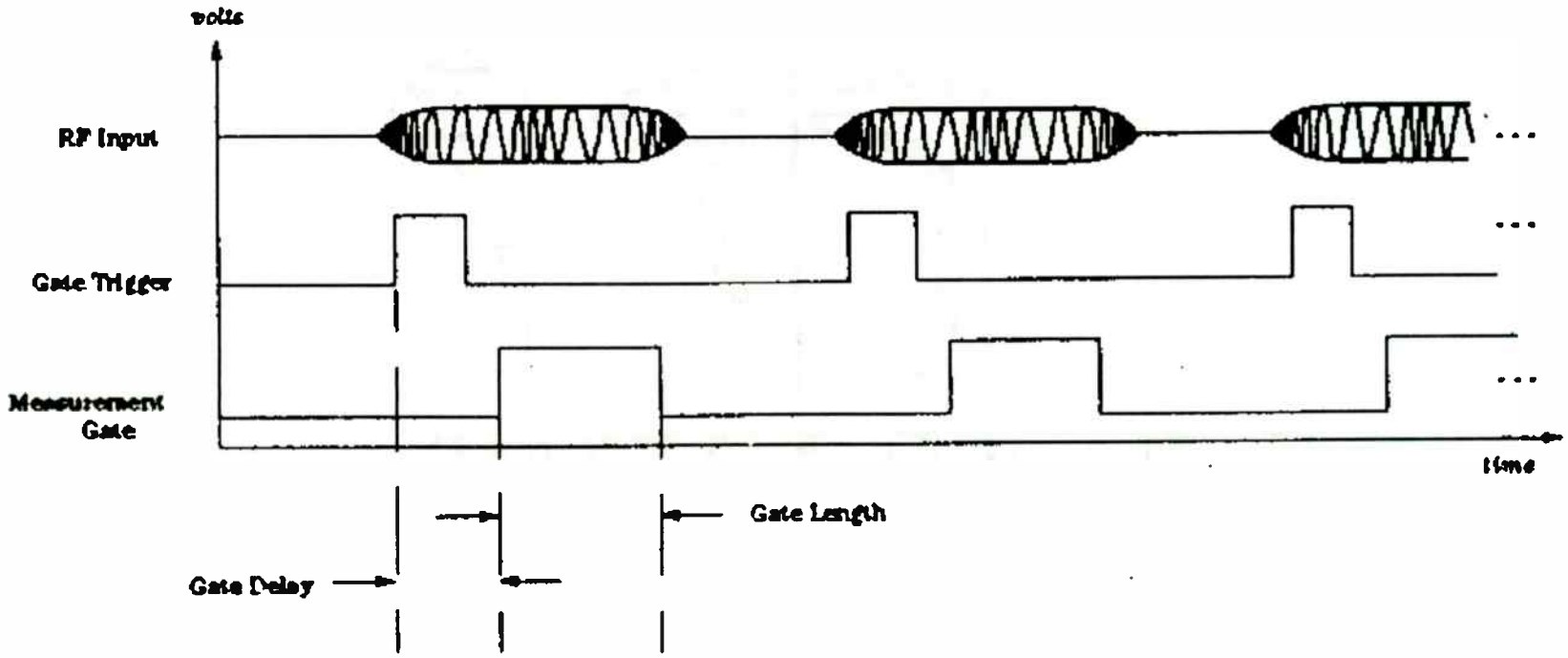

Figure 8

Time Selective Spectrum Measurements

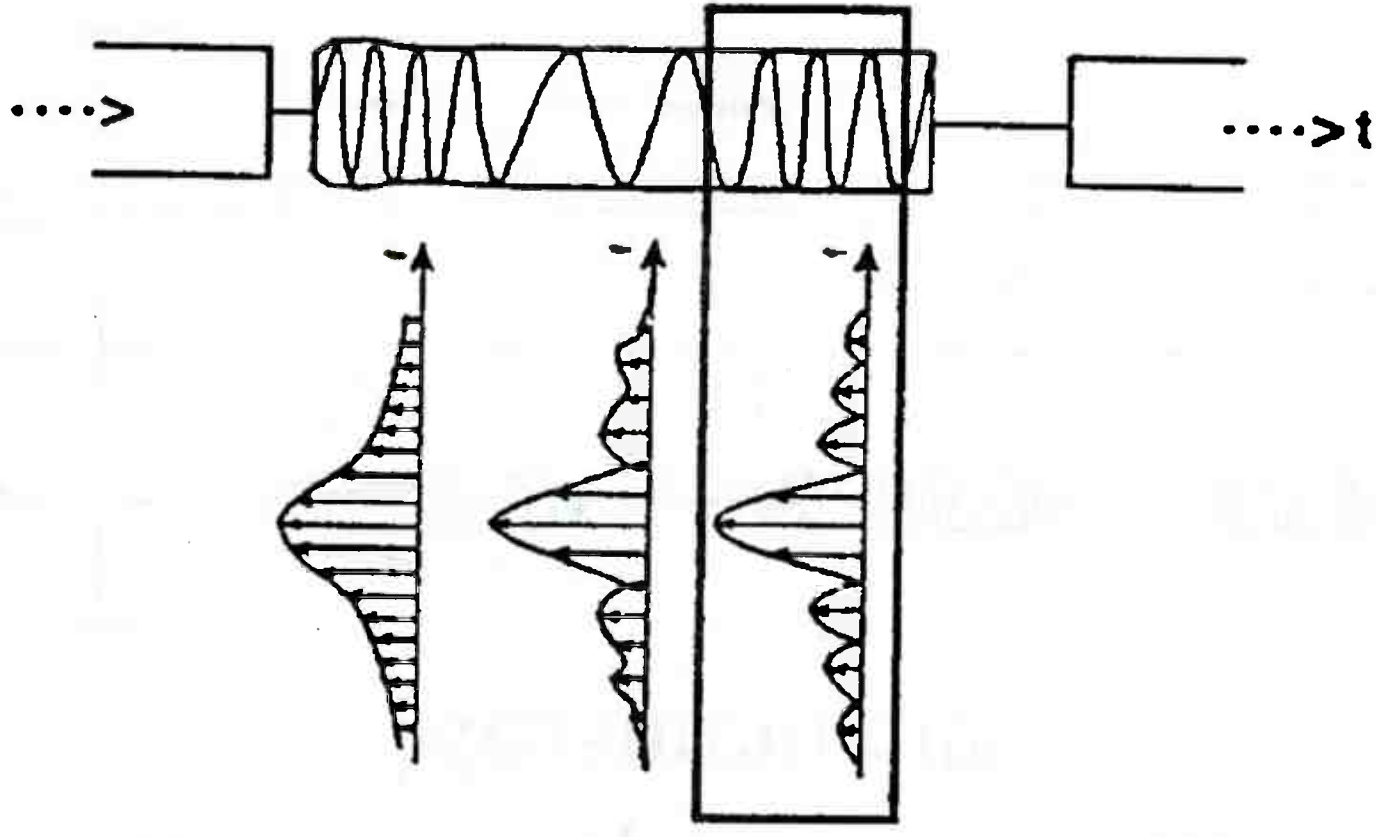

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Figure 9

of the analyzer. A resolution bandwidth which is too narrow will distort the pulse shape and increase the sweep time of the analyzer. A resolution bandwidth which is too wide will add excess noise and degrade the dynamic range of the analyzer. Figure 10 illustrates the effect of resolution bandwidth on the pulse response. The choice of resolution bandwidth must take the system data rate into account since the data rate of the digital modulation is much faster than the frame and burst repetition rate.

Anritsu MS8604A Digital Mobile Radio Transmitter Tester Methods

The MS8604A Digital Mobile Radio Transmitter Tester is really three instruments in one: a spectrum analyzer, a power meter, and a modulation analyzer. Figure 11 shows a block diagram of the MS8604A. Accurate measurements can be made on transmitters for the following systems: PHS, PDC, NADC, GSM, DCS1800, PCS1900, DECT, PACS, WCPE, TETRA, and CT2. The MS8604A has the flexibility to support all of these standards at the touch of a button. Measurements made by the MS8604A include: frequency accuracy, data rate accuracy, modulation accuracy, phase error, RF power output, burst power versus time characteristics, occupied bandwidth, FM deviation, adjacent channel power due to modulation/transients, and spurious emissions. All measurements conform to the appropriate EIA/TIA, RCR, MKK, or ETSI standard. Measurement displays include an I/Q diagram, trellis diagram, eye pattern, and phase/amplitude error. High speed DSP based measurements can be selected to greatly reduce the test time required for manufacturing and servicing transmitters. Automated test software may be written to support custom test procedures and executed by the microprocessor inside the MS8604A.

Figure 12 shows a block diagram of the digital demodulator inside the MS8604A. The 21.4 MHz IF output of the spectrum analyzer is downconverted to baseband (at 1.4 MHz) to be sampled by an A/D converter. The quadrature demodulator section consists of a coherent quadrature demodulator and a decimating digital filter. By changing the decimating ratio to suit the bit rate of the signal to be measured, measurements may be made on any signal having a bit rate from 100 bps to 1.25 Mbps. The decimated I/Q data is stored in waveform memory for further processing.

A block diagram of the DSP measurements performed in the digital demodulator is shown in Figure 13. A baseband digital filter (root-Nyquist) is then applied to the data if required by the standard. The demodulator recovers the signal amplitude and phase on a symbol-by-symbol basis for the DSP based power measurements. Re-sampling of the data stored in memory occurs after symbol timing detection. The display resolution of the signal to be measured is set at either 1/4 or 1/10 symbol depending on which measurement option is selected. SYNC word detection is performed on the demodulated data in order to re-assemble the burst symbols.

Frequency and phase error measurements are performed by comparing the phase of the signal to be measured with that of the demodulated ideal signal. Phase

Resolution Bandwidth Effects on Pulse Response

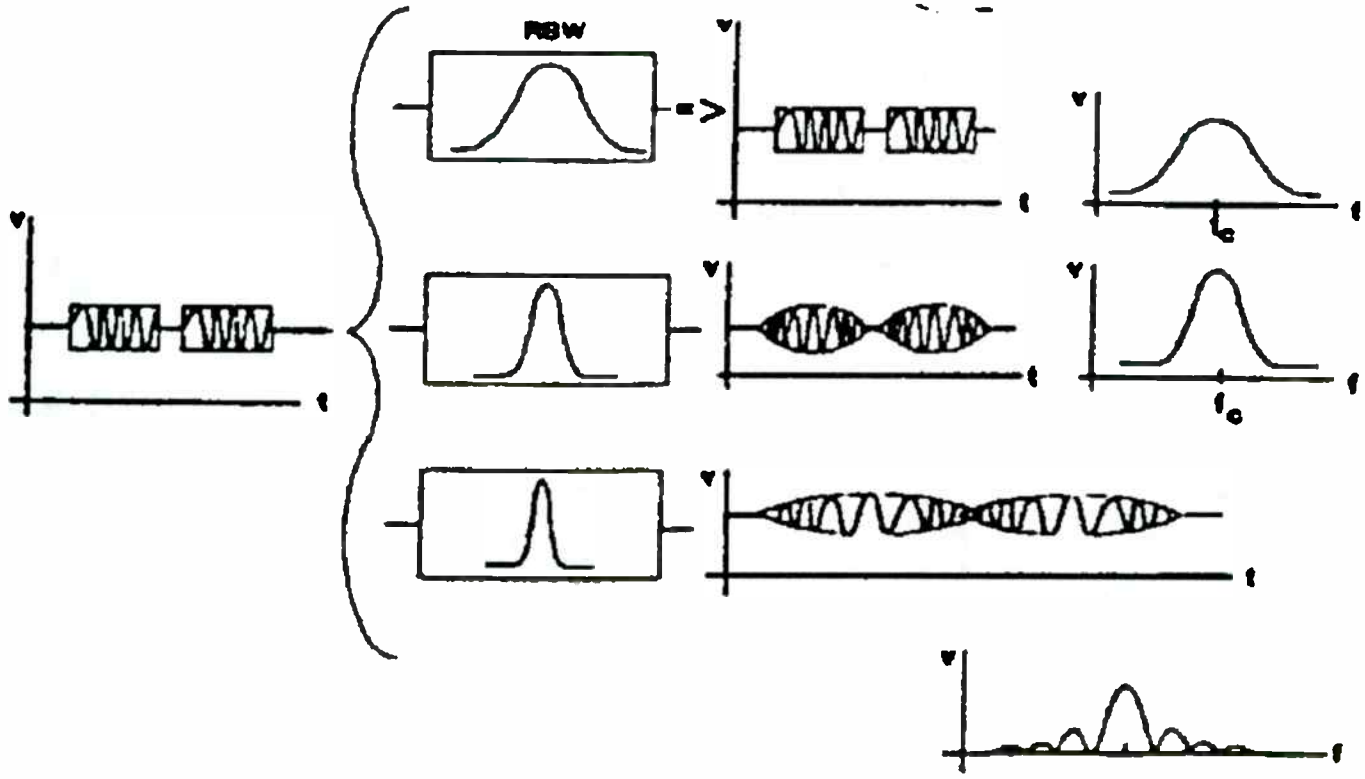

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Figure 10

MS8604A Digital Mobile Radio Transmitter Tester Block Diagram

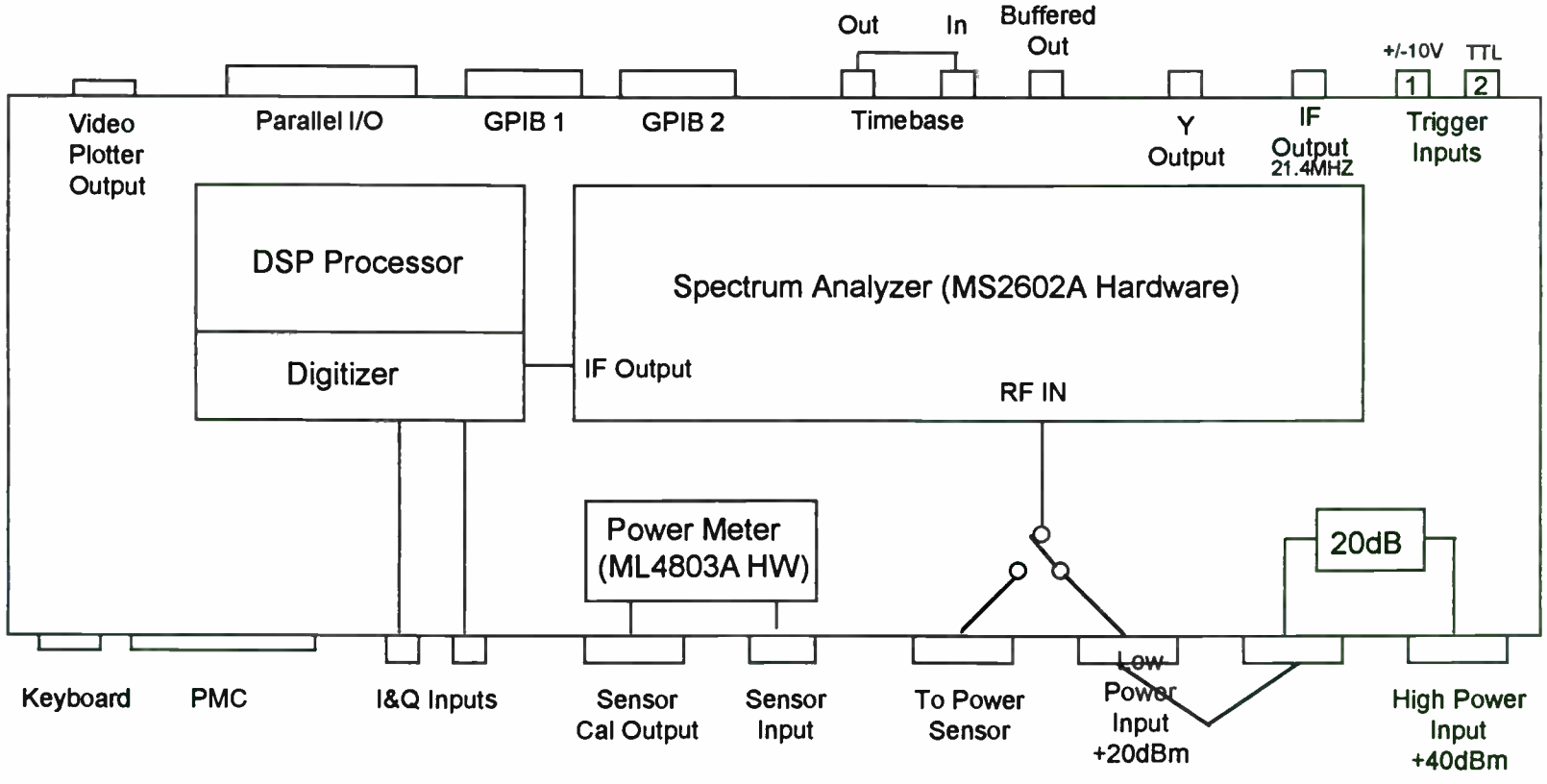

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Figure 11

MS8604A Digital Demodulator Block Diagram

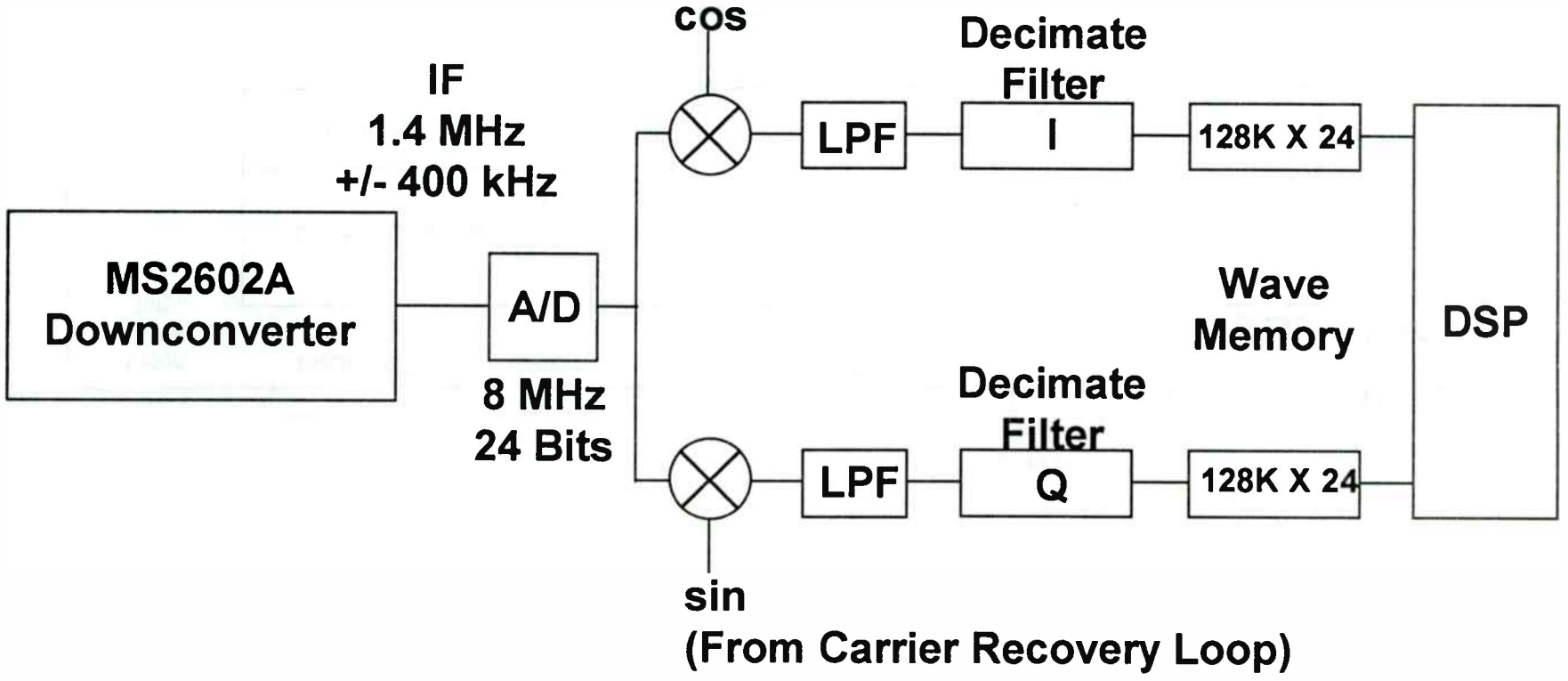

Figure 12

MS8604A DSP Measurements

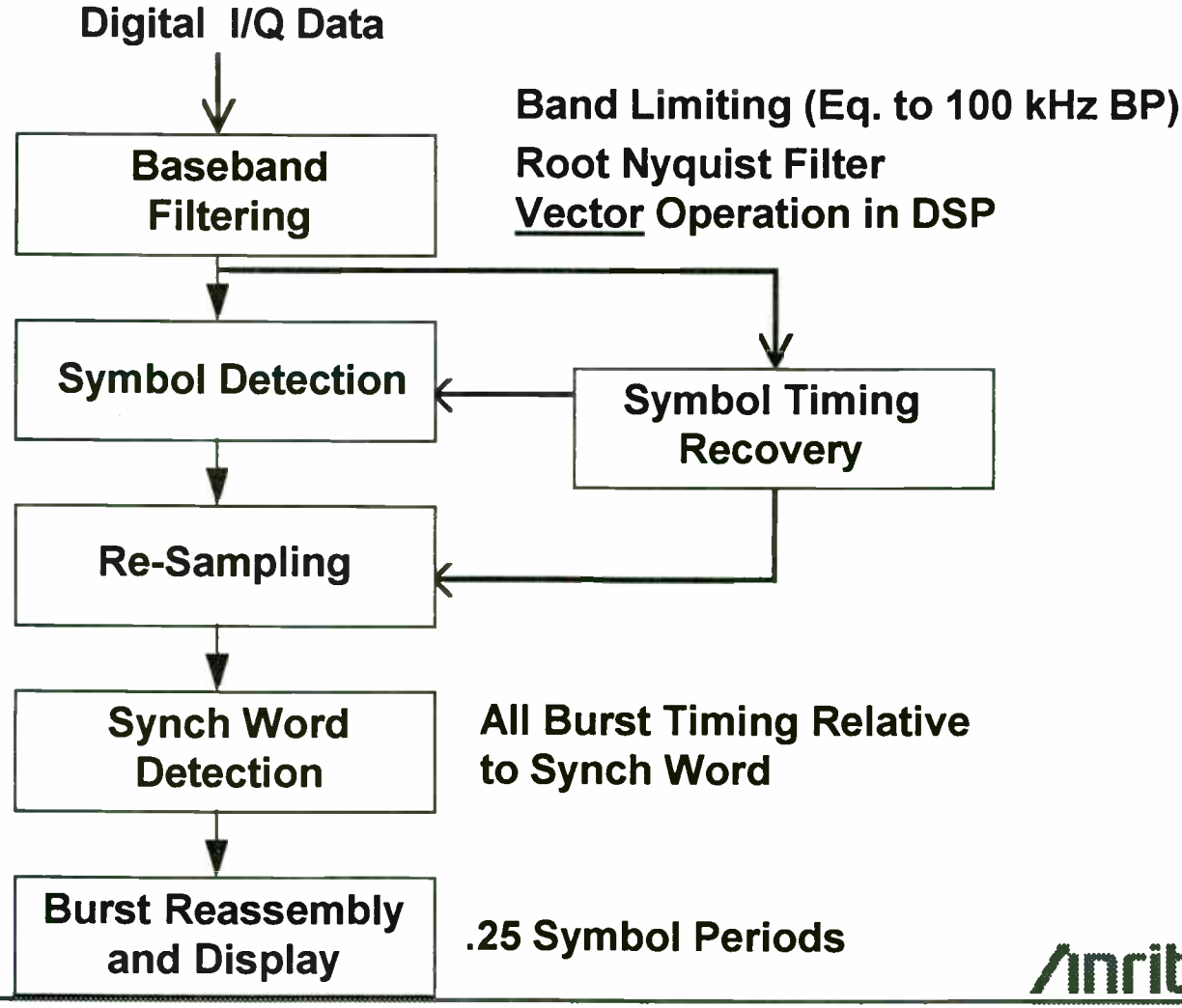

Figure 13

difference is plotted versus time where the slope is the frequency error and the difference from the linear fit is the phase error.

SYNC word detection provides an accurate time reference so that an external trigger signal is not required for burst power and ACP measurements. Power is measured using only the exact symbols in the range specified by the standard. The absolute accuracy of the burst power measurement is 10% (not to be confused with the +/- 0.5% of the power meter) or 0.4 dB maximum for a 40 dBm (10 watt) input. A wide dynamic range mode is also provided to enhance the dynamic range during carrier on/off measurements. In this mode, the power in the ON time and that in the OFF time are measured separately by changing the internal attenuator value and combining their waveforms for display. This method yields about 100 dB dynamic range.

A high speed DSP based ACP measurement method is provided to decrease test time and increase production throughput. The IS-55-A specified ACP measurement shown in Figure 14 is implemented using DSP. Overall, the MS8604A provides a much more flexible solution for transmitter tests since it uses digital signal processing and advanced measurement techniques.

Sources of Power Versus Time Measurement Errors

Precise timing in the measurement process is required to make power versus time measurements. Time-gated spectrum analyzers are susceptible to timing errors since they are designed to make frequency domain measurements. The major sources of measurement error in the time domain for the spectrum analyzer are: the sampling clock error, the sampling clock time resolution error, filter delay error, the trigger generation and jitter, and delay time error. Sampling clock error is defined as the sweep time accuracy. Sampling clock time resolution error is the sweep time divided by the maximum number of points (typically 401) in the trace display. Resolution bandwidth and video bandwidth delay error is caused by the signal being delayed by the filters relative to the amplitude trigger signal. There are also errors in the generation of the trigger as well as jitter on the signal. Sources of time domain measurement error for power versus time measurements as defined by the IS-55-A NADC standard are given as a detailed example in this section.

A. Spectrum Analyzer

The data sheet for a typical spectrum analyzer lists the following major sources of error:

1. Sweep time accuracy
   = sweep time x +/- 0.02%
   = 640 µsec x .02%
   = 128 nsec for rising edge display

   = 8 msec x .02%
   = +/-1.6 µsec for slot display

2. Sampling clock time resolution error
   = +/-1.6 µsec for rising edge display

Adjacent Channel Power
DSP Method

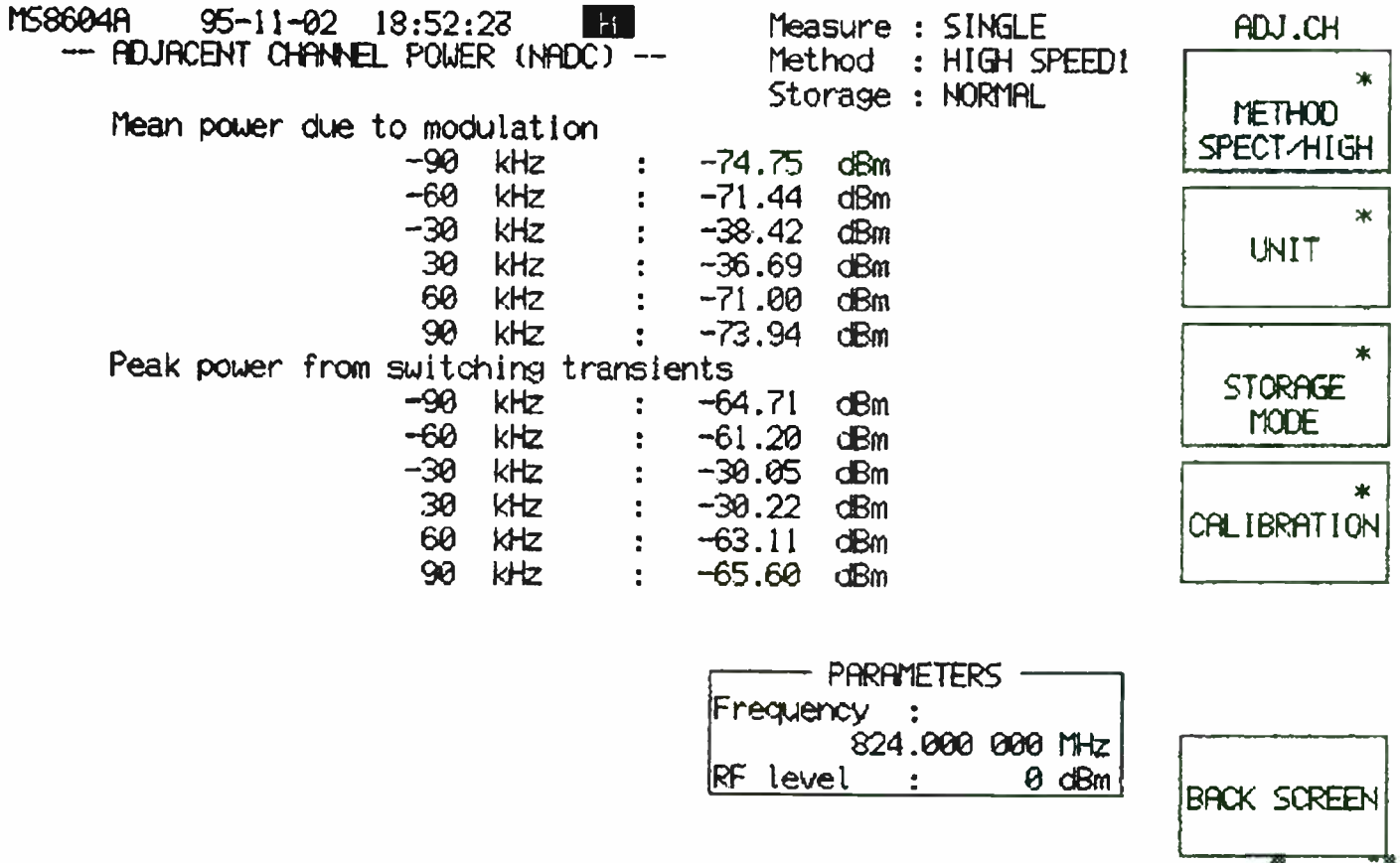

Figure 14

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= +/- 20 µsec for slot display

3. Resolution bandwidth and video bandwidth time delay = 4.5 µsec

4. Amplitude trigger jitter = 1.3 µsec

5. The trigger generation error is not specified and is unknown.

The total measurement error is then for burst display:

1.6 µsec + 20 µsec + 4.5 + 1.3 µsec = 27.4 µsec or about 2/3rds of one symbol

The total measurement error for the burst rising/falling display:

1.6 µsec + 4.5 µsec + 1.3 µsec = 7.4 µsec or about 1/5th of a symbol

B. MS8604A Digital Mobile Radio Transmitter Tester

The major sources of error in the MS8604A include only the sampling clock error and the SYNC word detection error.

1. Sampling clock error = +/- 0.1 ppm

Burst display = 7.407 msec x 0.1 ppm
= +/- 740 psec

Rising edge display
= 740.7 µsec x 0.1 ppm
= +/- 74 psec

2. SYNC word detection error
= +/- 0.4 µsec

Since all measurement timing is relative to the SYNC word, the total measurement error is about 0.4 µsec or 1/100th of a symbol. Therefore, the Anritsu MS8604A is 20-68 times more accurate than the typical spectrum analyzer. The difference in accuracy can be very significant when displaying the burst ramp up with respect to the specification mask. A fraction of a symbol can be the difference between meeting the specification and failing the test.

Figures 15 and 16 show the measured data taken on two commercially available NADC mobile stations using the MS8604A. The first mobile passes the test and the second mobile fails by a fraction of a symbol. The second mobile passes the test when measured with a typical spectrum analyzer.

Sources of Adjacent Channel Power Measurement Errors

The IS-55-A standard specifies two measurements of adjacent and alternate channel power. The average (mean) power due to modulation, and the out of band (peak) power arising from switching transients. The spectrum due to modulation uses time-gated average power measurement through a root-Nyquist filter over at least 50% of the symbols in a slot. Mean carrier power is compared with the average power measured at frequency offsets of +/- 30, +/- 60, and +/- 90 KHz.

The spectrum due to transients uses a peak power measurement through a root-Nyquist filter. The peak carrier power is measured by adjusting the center frequency of the measuring

Mobile Station Which Passes Test

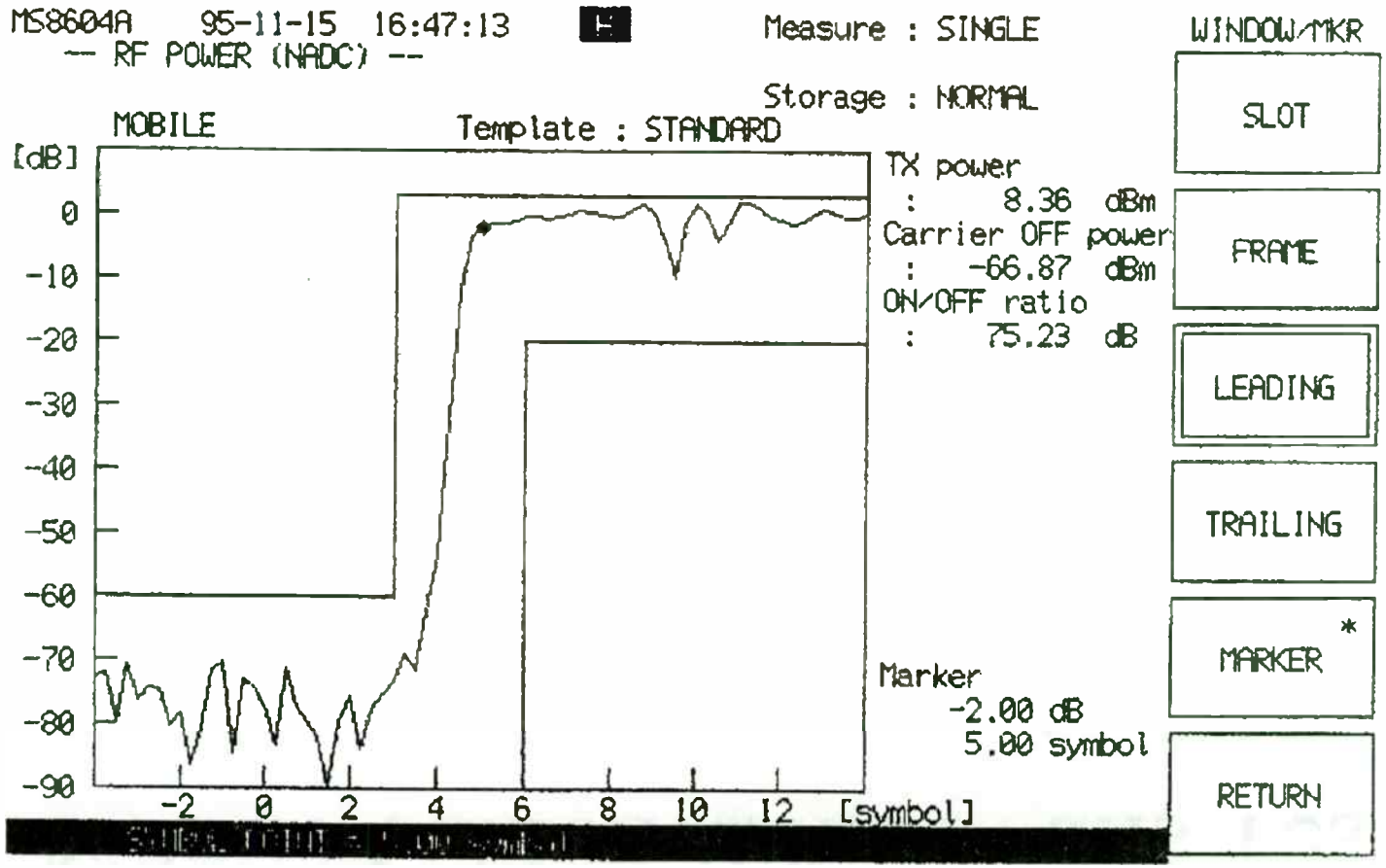

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Figure 15

Mobile Station Which Fails Test

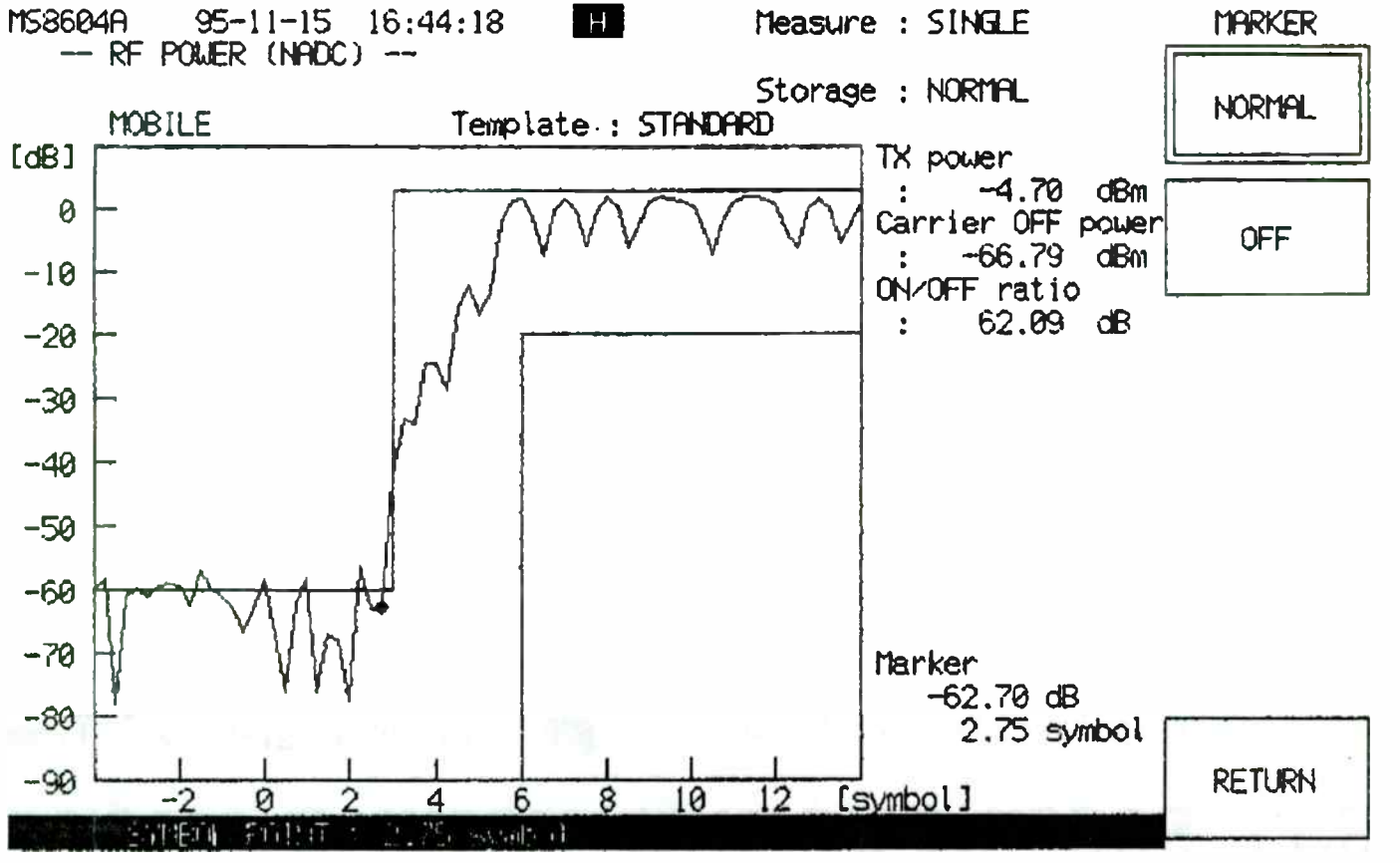

Figure 16

receiver to the center frequency of the transmitter under test. Peak ACP is measured by sweeping the frequency range with the spectrum analyzer peak detector selected. The test criteria is given below:

Frequency Offset (Khz)	ACP Level
+/- 30	-26 dBc
+/- 60	-45 dBc
+/- 90	-45 dBc or -13 dBm whichever is lower

The typical spectrum analyzer implements these ACP measurements by performing two sweeps: one normal sweep and one time-gated sweep. The normal sweep measures both the ACP due to modulation and transients. The second sweep measures the ACP due to modulation only by time- gating the rising and falling edges of the burst out of the measurement. The ACP due to transients is derived by subtracting the two sweeps. Both sweeps are performed using a peak detector, and each sweep takes about 8-14 seconds.

The typical spectrum analyzer uses a four-pole Gaussian resolution bandwidth filter in the IF section. A root-Nyquist filter is required by IS-55-A prior to the average or peak power detection. A spectrum analyzer has no way to properly implement this filter since phase and amplitude data is required. The spectrum analyzer attempts to compensate for the difference in filtering by using a correction factor. The correction factor does not correct for phase.

An amplitude trigger signal synchronous to the burst rate must be provided to the spectrum analyzer. The leading edge of the burst is detected using an RF amplitude detector, sometimes called a burst carrier trigger. The accuracy of this trigger signal is unknown and an important factor that cannot be overlooked.

An additional correction factor is necessary to account for the fact that a positive peak detector is used for both sweeps, and during the time-gated sweep the measurement time is cut in half (part of the burst between 40 and 90% points is gated out). This is inadequate since the response of the detector depends on the characteristics of the input signal. The spectrum due to noise component is somehow increased to account for the shorter measurement time before the spectrum subtraction operation.

The MS8604A uses a digital demodulator which includes a pre-detection digital root-Nyquist filter. The carrier power can be measured simultaneously with the adjacent and alternate channel power since the entire 1 MHz IF bandwidth is digitized and stored in wave memory for post processing. The correct detection method (average or peak) is applied to the data to properly measure each ACP noise component. No correction factors are needed!

There is a large difference in measurement speed between the two techniques. The spectrum analyzer

method of measuring ACP typically requires about 20-25 seconds. The Anritsu MS8604A can make the ACP measurement in about 1.5 seconds by using advanced DSP based methods.

DSP based measurements are much more reliable and accurate since precise measurement timing is maintained. No correction factors are necessary since the correct digital filter response is applied. Measurement comparisons for ACP between the MS8604A and a spectrum analyzer show that the spectrum analyzer measurement results are 6-10 dB lower than the correct ACP value measured by the MS8604A for the IS-55-A standard.

Summary and Conclusions

Reliable and accurate measurements of power versus time and ACP are necessary to characterize today's digital TDMA wireless communication systems. This paper has shown how limitations in the time-gated spectrum analyzer measurement techniques result in erroneous measurements of burst power versus time and adjacent channel power. A detailed example based on the IS-55-A standard was presented in order to show the magnitude of the measurement errors for a typical spectrum analyzer. Correction factors inadequately compensate for the shortcomings of the spectrum analyzer methods. The MS8604A Digital Mobile Radio Transmitter Tester, from Anritsu Wiltron Co., uses advanced DSP based measurements which improve the speed, accuracy, and reliability of wireless transmitter tests.

Nonlinearity Effects of Power Amplifiers on CDMA Communication Systems

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Abstract

The AM-AM and AM-PM distortions of a high power amplifier have significant influence on the bit error probability performance of a CDMA system. This paper presents two efficient methods to explore the nonlinear effects. The constellation distortions and the E_b/N_o ratios, both for SSPA and TWTA with different back-off points, are given as function of the number of the simultaneous users.

I. Introduction

The AM-AM and AM-PM nonlinear characteristics of the power amplifiers have significant effects on communication systems. Especially, for high power amplifiers operating in CDMA base stations, this problem must be considered. Multiple users signals in CDMA are permitted to be modulated at the same carrier frequency, to share the same entire system bandwidth, and to occupy the same time slot. Therefore, a single transmitter supports multiple traffic channels which share one radio channel. The average power and the instantaneous power fed to the power amplifier vary with the number of simultaneous users. A large dynamic linearization range is required for a power amplifier in the base-station transmitter [1]. If the transmitted signal is distorted by the AM-AM and AM-PM nonlinear behavior of the high gain power amplifier, the bit error rate (BER) of the CDMA receiver will increase. However, for general nonlinear channels, it is extremely difficult to calculate the AM-AM and AM-PM effects on the degradation of the CDMA system performance [2]. Therefore, many papers have evaluated the BER or E_b/N_o (bit energy-to-noise density ratio) for the different number of users limited to linear channels only. Using a commercial software SPW (Signal Processing Worksystem) [3], this paper presents estimation of power amplifier nonlinearity effects on the performance of a CDMA system for multiple simultaneous users. The constellation distortion is introduced first. Then the E_b/N_o degradation is revealed.

II. Constellation Distortion

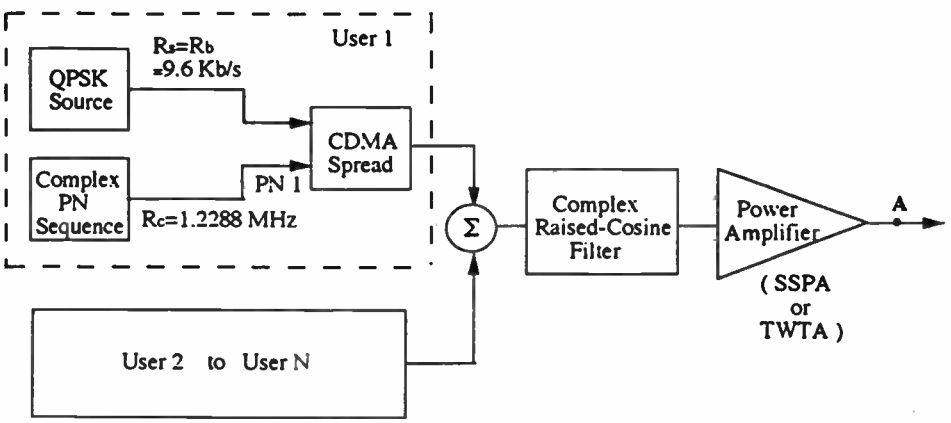
As shown in Fig.1, a QPSK source is modulated by a complex pseudo-noise sequence PN1 to generate a QPSK direct sequence spread spectrum (DS-SS) signal for a CDMA user 1. The information rate and the chip rate are set as R_b = 9.6 kb/s and R_c=1.2288 MHz, respectively. It means that the radio channel bandwidth of the spread wideband spectrum W_{spread} is 1.2288 MHz after the raised-cosine filter. Similarly, multiple QPSK

DS-SS signals of user 2 to user N are generated, wherein the Walsh function numbers for different users are different.

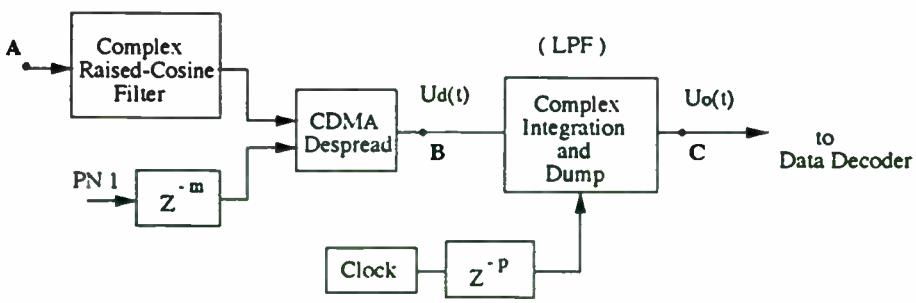
The receiver for user 1 is supposed to be ideally synchronized. It means that the desired signal is cross-correlated with a reference signal which has the same code as PN1, except having m samples delay (where m depends on the two filters in Fig.1). Assuming the additive white Gaussian noise is ignored, other unwanted users signals are considered as interference. The resulting signal $u_d(t)$ at point B after de-spreading is

$$\begin{aligned} u_d(t) &= C_1(t)\,[\sum_{j=1}^{M} C_j(t)B_j(t)] \\ &= C_1^2(t)B_1(t) + C_1(t)\,[\sum_{j=2}^{M} C_j(t)B_j(t)] \\ &= KB_1(t) + jamming \end{aligned} \tag{1}$$

where $B_1(t)$ is the desired signal for user 1, $C_1(t)$ is the specified code PN1, while $B_j(t)$ and $C_j(t)$ ($j \neq 1$) correspond to other users.



(a) Base Station Transmitter



(b) User 1 Receiver

Fig.1 CDMA System Simulation Block Diagram

The integration and dump block in Fig.1 act as a narrow band low pass filter (LPF). Therefore, $u_0(t)$ at point C includes the despread desired signal which does not change after the LPF, while the power of the jamming component decreases by a factor, i.e., the bandwidth expansion factor of the CDMA system. Finally, $u_0(t)$ is treated with a data decoder and the transmitted QPSK signal of user 1 is recovered.

In order to investigate the nonlinear channel effect on the performance of the CDMA system, two nonlinear amplifier models (TWTA and SSPA) are inserted into the transmission channel, shown in Fig.1, independently. The AM-AM and AM-PM characteristics of each amplifier [4] are interpreted by two look-up tables. Assuming that each user has an identical power, the operation point of the amplifier of a given number (N) of simultaneous users is determined by the sum of the total users. It vary from back-off 0 dB to -12 dB.

The constellations of the signals $u_0(t)$ after LPF are then obtained for different cases. It is shown in Fig.2, as an example, N = 40. Obviously, the constellation is more divergent if the back-off is less. Also, the constellation divergence of the TWTA is more serious than that of the SSPA (the normalized 0 dB back-off to saturation for these two amplifiers are identical). These plots reveal the AM-AM and AM-PM nonlinear distortions that result in the constellation distortions, from which the data decoder in the receiver is easier to have the error bit decision.

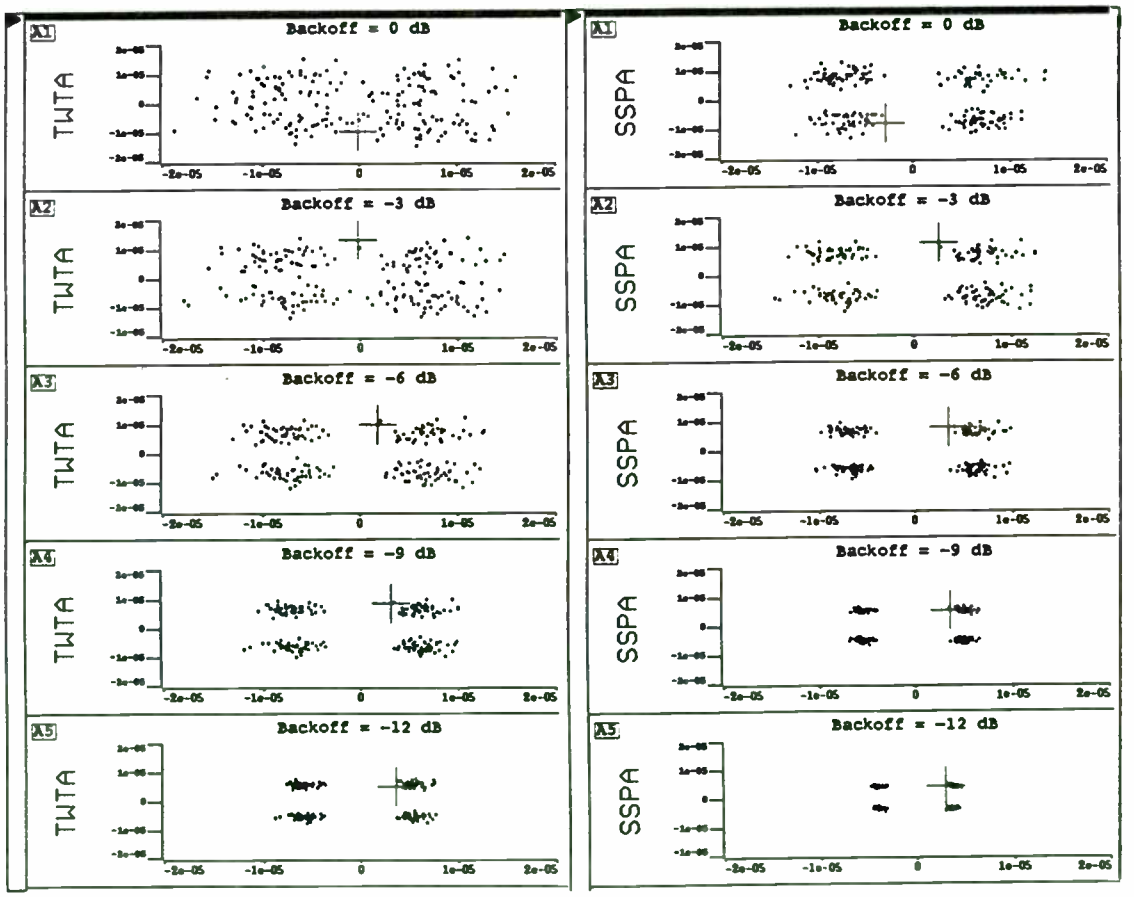


Fig.2 Costellation Distortions for TWTA and SSPA (N = 40)

III. E_b/N_o DEGRADATION

The BER is the most important specification to characterize the digital communication system performance. However, to estimate the BER for a CDMA system needs a large amount of data, either in experiment, or in simulation. For system illustrated in Fig.1, even for obtain a BER at the order of 10^{-3}, at least 10^5 QPSK symbols are necessary. Note that a QPSK-DSSS symbol corresponds to 128 PN chip symbols. Each chip symbol is sampled by 8 samples in the simulation. Therefore, about 10^8 iteration points are needed. Instead, the E_b/N_o after the LPF at point C in Fig.1 is calculated by the average power as follows:

$$\frac{P_{S+I} - P_I}{P_I} = \frac{E_b/T_b}{N_o W_{spread}} = \frac{E_b R_b}{N_o R_b} = \frac{E_b}{N_o} \tag{2}$$

where P_{S+I} is obtained if all the signals $\sum_{j=1}^{N} S_j$ (including the desired signal S_1) are injected to the power amplifier; P_I is obtained if only the interference signals $\sum_{j=2}^{N} S_j$ are injected to the power amplifier at the same operation point; E_b is the signal energy per bit; T_b is the bit interval; R_b is the bit rate; N_0 is interference power density; and W_{spread} is equal to the bandwidth of the LPF.

For different number of simultaneous users and different operation point, the simulation results for both SSPA and TWTA are given in Fig.3. The iteration points taken are 2×10^5.

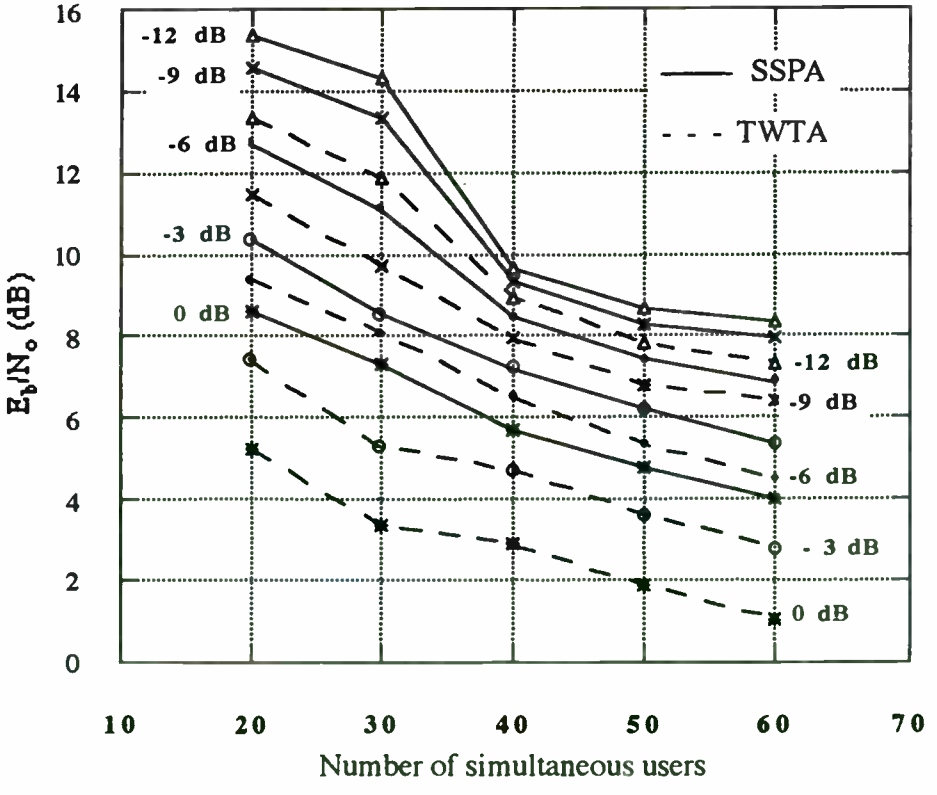


Fig.3 E_b/N_o as Functions of N and Operation Point of Power Amplifier

It can be seen apparently: (1) for a given power amplifier, the more back-off, the higher E_b/N_o; (2) for a fixed operation point, E_b/N_o degrades if the number of simultaneous users increases; (3)the lower the AM-AM and AM-PM distortions, the better the E_b/N_o performance (e.g., SSPA is better than TWTA).

For a forward link, BER$\leq 10^{-3}$ can be achieved at $E_b/N_o = 5\,dB$ with powerful code [5]. Consequently, if the required E_b/N_o is 6 dB for N = 60, the simulated SSPA and TWTA should operate at back-off -6 dB and -9 dB, respectively. Those two operation points correspond to the third-order intermodulation product about -35$\sim$ -30 dBc [4]. Although these values are device-dependent, the estimation approach is appropriate to a general case.

IV. Conclusion

For a CDMA system, the envelope of the combined multi-users signal varies within a large dynamic range. Therefore, the AM-AM and the AM-PM distortions cause constellation distortion, which can be examined at the point before the decision in the receiver. This is a useful tool to qualitatively investigate the nonlinear channel effects. The E_b/N_o ratio also can be calculated by two average power at the same point. This is more convenient and realistic for microwave amplifier designers, rather than the BER calculation for a CDMA system with nonlinear channel.

The proposed estimation approaches of the effects of nonlinear amplifiers on CDMA communication systems can be applied to any power amplifier, providing that its AM-AM and AM-PM characteristics are known in advance.

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High-Speed CMOS Direct Digital Frequency Synthesizer Including D/A Converter

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Abstract

In this paper, the phase accumulator that limits the maximum synthesized frequency of direct digital frequency synthesizer (DDFS) is improved with new design of pipelined adder dynamic D-F/F. Using the proposed method of sine amplitude difference algorithm in coarse/fine ROM, the data is compressed approximately 6.4:1 (2048 bit to 320 bit), where the address and data are set to 8 bit.

It is also designed and added the high speed 8 bit D/A converter at the end of digital amplitude data output stage.

To design and verify the aimed operation of logic circuit, the existing standard cell library and a specific design system of FPGA, QuickLogic and GEX layout tool are used.

The maximum operating frequency of phase accumulator in DDFS is estimated to be 526.6MHz in the consideration of the propagation delay time of D-F/F and 1-bit full adder, which is verified via SPICE simulation.

I. Introduction

Direct Digital Frequency synthesizer produces various frequencies applicable to many digital communication systems, CDMA digital cellular telephone, spread spectrum equipment and wireless LAN(Local Area Network). Resolution, band-width, and frequency switching speed of the synthesis are especially important in modern mobile communication. The phase of the synthesizer used in those systems is in need for the precise calculation con-verting to amplitude of sine function.

In this study, the DDFS is designed using the pipeline method, coarse/fine ROM, sine amplitude-difference algorithm, and fast D/A converter. Adopting pipeline algo-rithm, time delay of a phase accumulator is the same as that of a 1 bit full adder, regardless of the number of accumulator bits.

The ROM data compression ratio by coarse/fine and sine amplitude-phase difference algorithm is compared with that of conventional ROM, and the ROM can change with combinational circuit for real speed. The speed of the phase accumulator

is estimated by simulating adder and the dynamic D-F/F.

Ⅱ. Pipeline phase accumulator

A conventional structure of a phase accumulator is not fit for getting UHF frequencies. An addition of one digit can be performed only after accepting the carry of the previous digit. In the case of the 1-bit adder of which delay time is t_d, the total delay time of conventional N-bit adder is $N \times t_d$. The problem can be solved by rearranging delivery path of each carry.

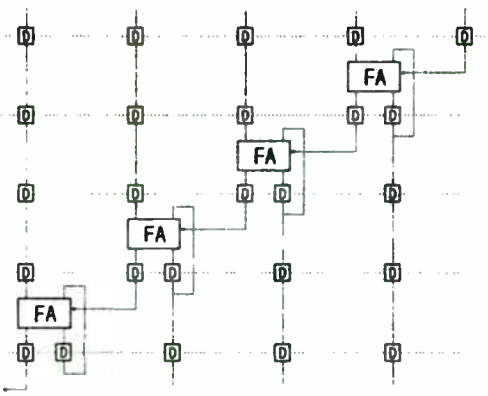

Fig. 1. Pipeline phase-accumulator

In non-pipeline phase accumulator, a high speed phase accumulator as a carry-lookahe ad method, requires so many logic gates an d long critical path. Consequently, total dela y time of carry-lookahead method is much longer than 1-bit full adder.

In the case of pipelined N-bit adder, the total delay time is t_d. Because, in spite of the length of bits, the pipelined phase accu mulator is just one delay time(t_d), the phas e accumulator can run faster N times than conventional phase accumulator.

Ⅲ. ROM data compressions

The data length of sine function can be reduced by using coarse ROM and fine ROM. The assignment of look-up table samples in this architecture is based upon several trigonometric approximations. First, the bits representing the phase argument, θ, of one quarter period of the sine function are decomposed into the sum of three functions ;

$$a < \frac{\pi}{2},$$

$$b < \frac{\pi}{2}(2^{-A}),$$

$$c < \frac{\pi}{2}(2^{-(A+B)})$$

such that θ = a+b+c.

$$\sin(A+B+C) \cong \sin(A+B)\cos C + \cos A\cos B\sin C - \sin A\sin B\sin C \quad \cdots\cdots\cdots (1)$$

$$\sin(A+B+C) \cong \sin(A+B) + \cos A\sin C \quad \cdots\cdots (2)$$

Using trigonometric identity, eq. (1), and its approximation, eq. (2), the function is given by

$$\sin(A+B+C) \cong \sin(A+B) + \cos A\sin C.$$

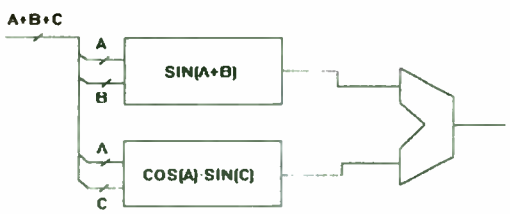

Fig. 2 Coarse/fine ROM block diagram.

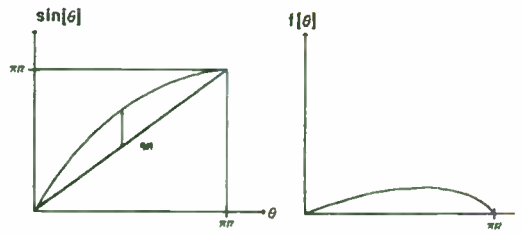

Fig. 3 Amplitude-phase difference algorithm

For example, lower 9-bit of phase accumulator except higher 2 bits are assigned to A, B, and C each 3 bits respectively. When data are 10 bits, equation (1) requires $5120(=10\times2^{3+3+3}=10\times2^{9})$ bits. On the other hand, equation (2) needs just $960(=10\times2^{3+3}+5\times2^{3+3}=10\times64+5\times64)$ bits. Therefore, ROM area of equation (2) is less 5.1 times than that of equation (1).

A quarter period of a sine function can be represented by $f(\theta)=\sin(\theta)-2\theta/\pi$ to improve the compression ratio. The maximum value of $[\sin(\theta)-2\theta/\pi]$ is less than a quarter of a sine function. Using this method, 2 bits of ROM address is able to be saved. $f(\theta)$ is shown by Fig.3.

IV. D/A Converter Design

A 8-bit weighted-current-sink digital-to-analog converter with 10-90 percent rise/fall time of 2ns, integrated with a 0.8μm technology. The D/A Converter designed by GEX design tool, and simulated by HSPICE. Designed D/A Converter layout shown by Fig. 4.

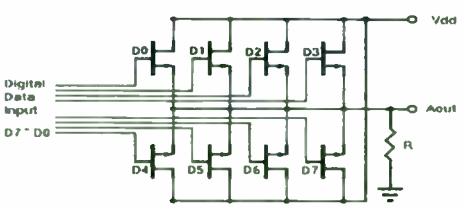

Fig. 4. A MOS-based 10 bit weighted current DAC design

V. D-F/F design

In conventional CMOS circuits both static and dynamic CMOS logic are used. For the purpose of system timing a clocking strategy is always involved except for a self-timed system.

The most popular clocking strategy is clocked CMOS logic(C^2MOS), which uses a nonoverlapping pseudo two phase clock. Clock skew in the system will cause serious problems and result in difficulties in increasing circuit speed. New clocking method, known as TSPC, which fits not only dynamic but also static CMOS circuits and in most cases cam replace the NORA CMOS technique, doesn't require more than one clock phase. But this flip-flop has a hazardous discharge when its output should remain stable.

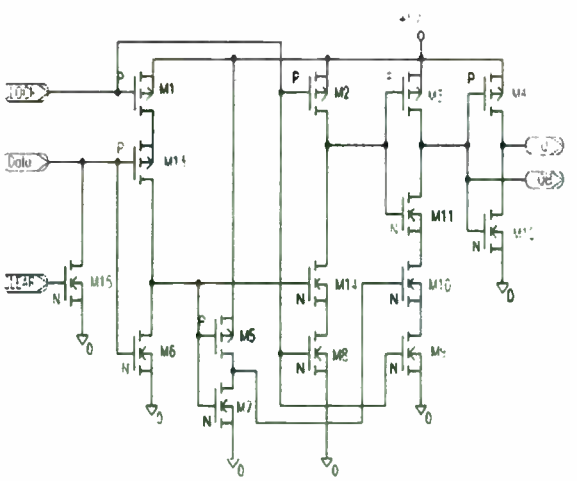

Fig. 5 Final version of dynamic D-F/F with CLEAR

The structure[3], which another transistor is inserted into, prevents the output QB from discharging when it should remain stable. However, this circuit which has unnecessary transistors is modified as above figure shows. Also CLEAR of D-F/F is added.

VI. DDFS design and logic simulation

Frequency controller consists of 16-bit D-Flip/Flop and phase accumulator is composed of pipeline adder which uses 272 D-F/Fs. Total 16 bits of pipeline phase accumulator consist of 8-bit address of sine ROM, 2 bits of phase control, and the other bits are not used.

In a 12-bit address of phase accumulator, 2 bits are used for phase control, 8 bits for address of coarse/fine ROM, and the other bits are truncated. When an address consists of a=2, b=3, c=3, respectively, and 8 data bits, it is possible to design fine ROM with 5 bits. Two coarse/fine ROM data generation equation of is given by

$$F_c(a,b) = \sin\left(\frac{\pi}{2} \times \frac{a \times 2^{B+b}}{2^{(A+B)}}\right) \quad \cdots\cdots\cdots\cdots\cdots (3)$$

$$F_f(a,c) = \sin\left(\frac{\pi}{2} \times \frac{a \times 2^{(B+C)} + b \times 2^{c} + c}{2^{(A+B+C)}}\right) - F_c(a,b) \quad \cdots (4)$$

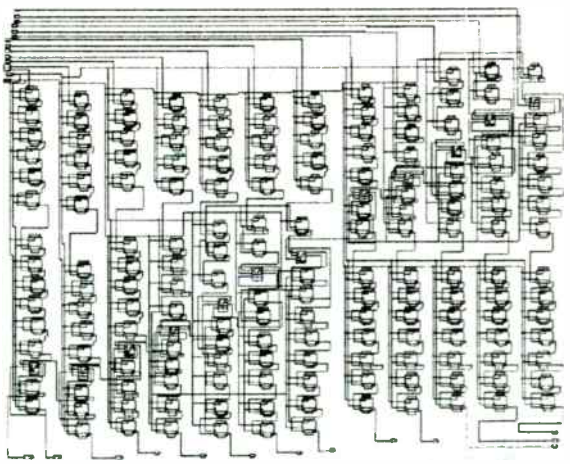

Fig. 6. FPGA design of pipeline phase-accumulator

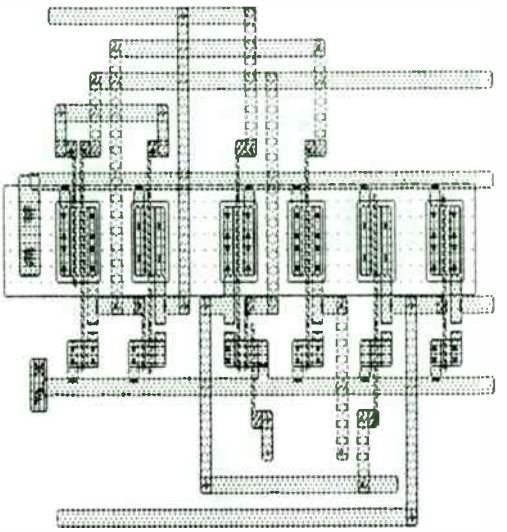

Fig. 7. GEX design of D-F/F with CLEAR

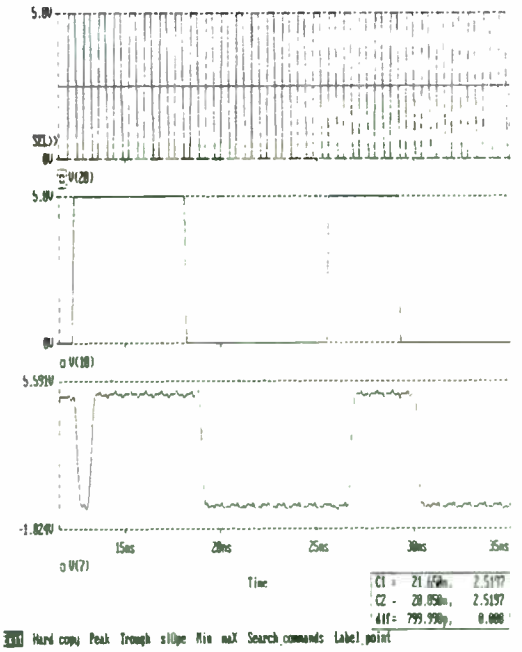

Fig. 8. SPICE simulation result of D-F/F with CLEAR

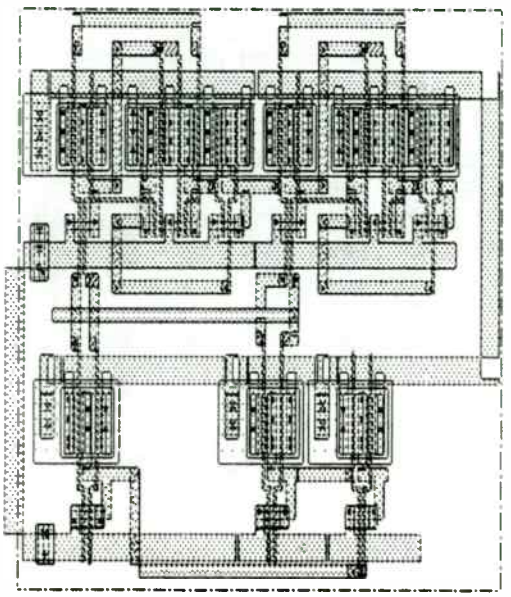

Fig. 9. GEX design of 1 bit full-adder

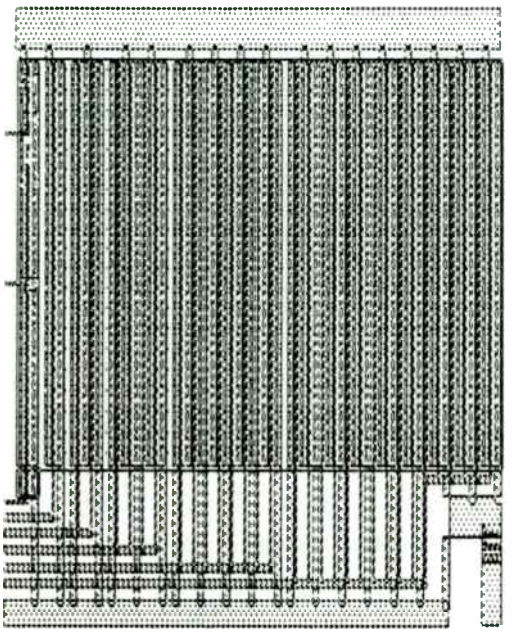

Fig. 11. GEX design of 8bit DAC

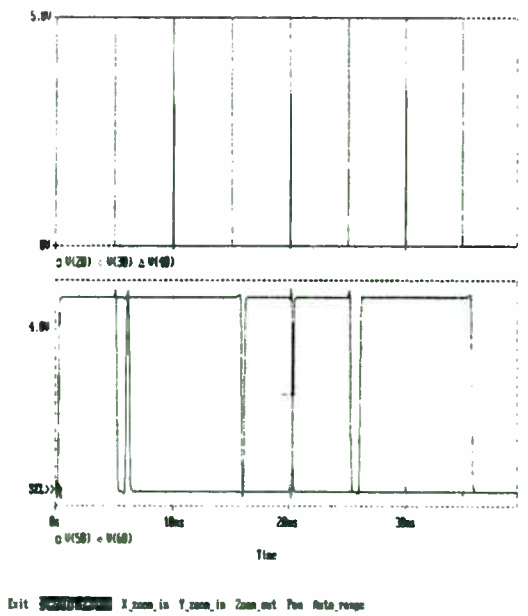

Fig. 10. Simulation result of 1-bit full-adder

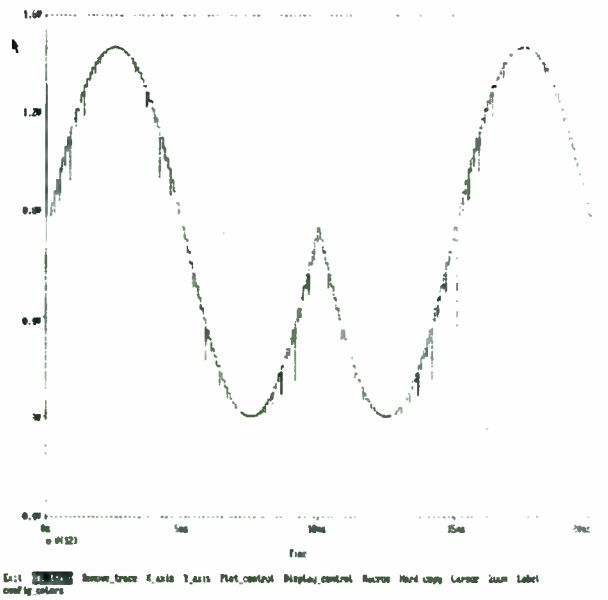

Fig. 12. SPICE simulation result of 8 bit DAC design

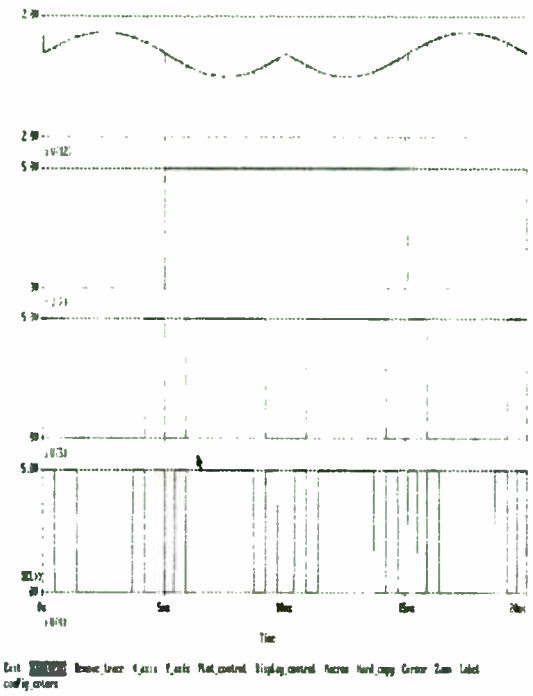

Fig. 13. Simulation result of 8bit DAC with simple PSK signal

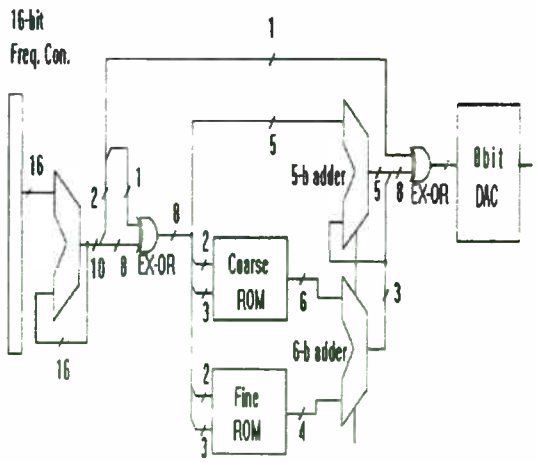

Fig. 14. Overall direct frequency synthesizer block diagram

VII. Conclusions

In this paper, the DDFS is designed using the pipeline method, coarse/fine ROM, and sine amplitude-difference algorithm.

Adopting pipeline algorithm, the time delay of a phase accumulator is the same as that of a 1 bit full adder, regardless of the number of accumulator bits. If address and data bits are set to 8 bits with existing ROM table, the used bits are 2048 bits, but using the data compression algorithm, the used bits are reduced to 320 bits. It shows that the data compression ratio of novelly presented frequency synthesizer is roughly 6.4:1 in contrast with existing products.

We design the phase accumulator deciding the maximum frequency of the digital frequency synthesizer, and D/A converter too. After drawing up the layout with GEX, as a design tool, we extract SPICE files and make simulation.

The operating frequency of D-F/F is accurately 1.25GHz, and that of 1-bit full adder 925MHz. The maximum operating frequency of phase accumulator in DDFS is estimated to be 526.6MHz in the consideration of the propagation delay times of D-F/F and 1-bit full adder.

Since the generation frequency of DDFS is maximally about the half of the system clock frequency, our designed DDFS is expected to have the maximum frequency of 263MHz, which is about 10 times of Qualcom's Q2230 DDFS chip.

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UNDERSTANDING AND APPLYING ERROR VECTOR MEASUREMENTS IN DIGITAL RF COMMUNICATIONS DESIGN

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Hewlett-Packard Company, Everett, WA

The diverse technologies that comprise today's digital RF communications systems share in common one overarching goal: placing digital bitsteams onto RF carriers and then recovering them with accuracy, reliability and efficiency. Achieving this goal demands engineering time and expertise, coupled with keen insights into RF system performance such as those provided by the most up-to-date test and measurement technologies.

Recently, many design and test engineers have begun to rely on a new category of test instrumentation to help them meet their performance and schedule goals. Known as vector signal analyzers, these tools perform time, frequency and modulation domain analysis on a wide variety of signals. Because they process signals in full vector (magnitude and phase) form, they easily accommodate the complex modulation formats commonly used for digital RF communications. Perhaps most importantly, these analyzers contribute a new type of measurement called "error vector magnitude", or EVM.

Primarily a measure of signal quality, EVM provides both a simple, quantitative figure-of-merit for a digitally modulated signal, along with a far-reaching methodology for uncovering and attacking the underlying causes of signal impairments and distortion. EVM measurements are growing rapidly in acceptance, having already been written into such important system standards as GSM, NADC and PHS, and they are poised to appear in several upcoming standards, including those for digital video transmission. This article will define error vector magnitude and related measurements, discussing how they are implemented and explaining how they are practically applied in digital RF communications design.

Error Vector Measurements -- an Overview

EVM Defined

In order to understand error vector magnitude, recall first that vector modulation transfers digital bits onto an RF carrier by varying the carrier's magnitude and phase such that, at each data clock transition, the carrier occupies any one of several unique locations on the I vs. Q plane. Each location encodes a specific data symbol, consisting of one or more data bits. A constellation diagram shows the valid locations (i.e., the magnitude and phase) for all permitted symbols, of which there must be 2^N, given N bits transmitted per symbol. To demodulate the incoming data one must thus accurately determine the exact magnitude and phase of the received signal for each clock transition.

The layout of the constellation diagram and its ideal symbol locations is determined generically by the modulation format chosen (BPSK, 16QAM, pi/4DQPSK, etc.). The trajectory taken by

the signal from one symbol location to another is a function of the specific system implementation, and is readily calculated.

At any moment in time, the signal's magnitude and phase can be measured (relative to the carrier), the values for which define its actual or "measured" phasor. At the same time, the ideal or "reference" phasor can be determined by calculation, given some knowledge of the transmitted data stream, the system clock rate, baseband filtering parameters, etc. Simply put, error vector magnitude is the unsigned, scalar distance between the endpoints of these two phasors.

Figure 1 defines EVM and several related terms. By convention, it is reported as a percentage of the peak signal level, usually defined by the constellation's corner states. While the error vector has a phase value associated with it, this angle generally turns out to be random, because it is a function of both the error itself (which may or may not be random) and the position of the data symbol on the constellation (which, for all practical purposes, is random). A more useful angle is measured between the actual and ideal phasors (I-Q phase error), which will be shown later to contains information useful in troubleshooting a wide variety of problems. Likewise, I-Q magnitude error shows the magnitude difference between the actual and ideal signals.

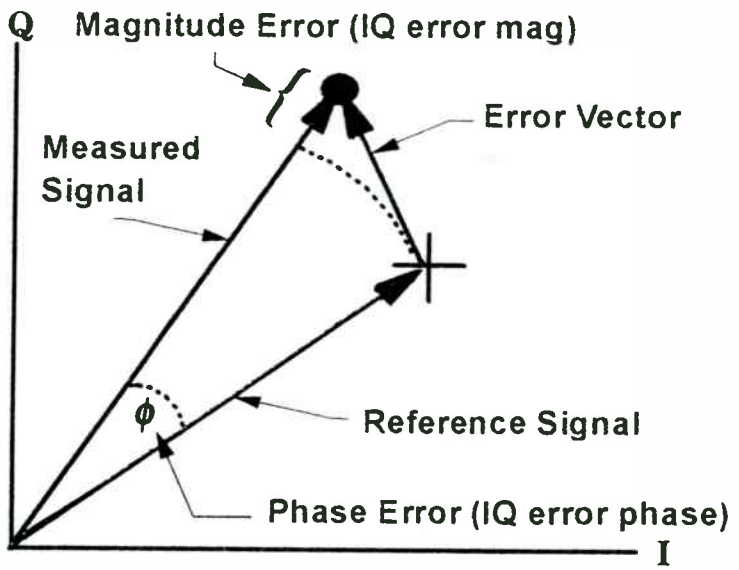


Figure 1 -- Error vector magnitude (EVM) measurements are based on the instantaneous difference between a vector-modulated signal and an ideal, noise-free "reference" version of itself.

Displaying EVM

The most common display of EVM is a simple plot its value as a function of symbol time, as shown in figure 2. Vertical bars may be positioned along the x-axis at the actual symbol clock transitions, with a height proportional to the EVM percentage. The display also shows the instantaneous EVM (continuous line), which portrays the accuracy of the signal's trajectory

from one symbol state to another. This provides useful insights into the time domain performance of system baseband filtering, and can be helpful in troubleshooting ISI problems.

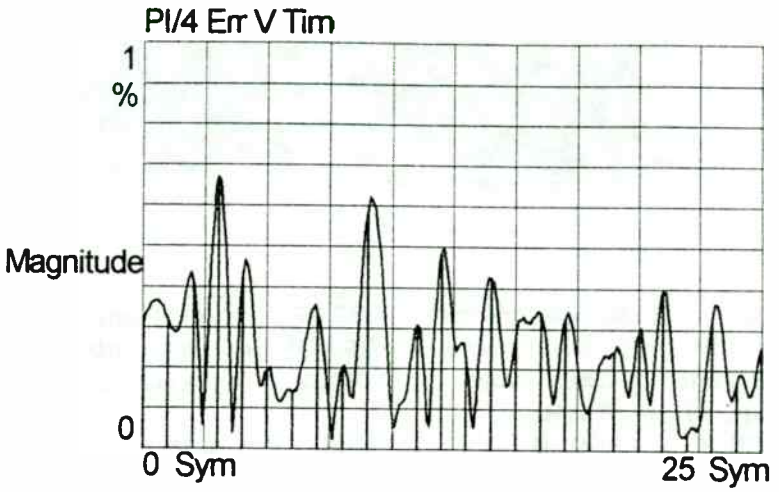
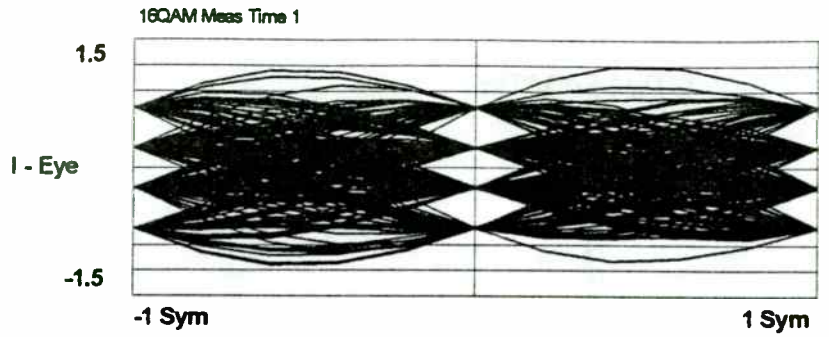


Figure 2 EVM plot taken on an HP89441A vector signal analyzer, shows the error magnitude both at the symbol clock times (vertical bars) and in-between (continuous line).

When qualifying a system against a specific performance standard, a detailed EVM plot may not be the best answer, as compared with a single average value. This is readily calculated from the rms average of the individual EVM percentages, taken across a user-specified block of symbols (perhaps a single TDMA burst). The data table display in figure 3 provides this average value, as well as the location and value of peak magnitude and phase errors within the data block.



EVM	= 248.7475	m%rms	732.2379	m% pk at symbol	73
Mag Error	= 166.8398	m%rms	-729.4476	m% pk at symbol	73
Phase Error	= 251.9865	mdeg	1.043872	deg pk at symbol	168
Freq Error	= -384.55 Hz				
IQ Offset	= -67.543 dB		SNR	= 40.58	dB

0	1110011010	0110011100	0110011010	0100101001
40	0010100110	1000010101	0010010001	0110011110
80	1001101101	0110011001	1010101011	0110111010
120	1000101111	1101011001	1001011010	1000011001

Figure 3 Data table summary shows peak and average EVM, SNR, along with I-Q phase and magnitude errors.

It should come as no surprise that EVM may also be expressed as a signal to noise ratio (SNR). Recalling its fundamental definition -- the residual between an actual signal and an ideal version of itself -- one discovers a good basic definition for noise in general. Comparing the equations for EVM and SNR (figure 4), the only difference (other than the fact that one is reported as a percentage while the other is given in dB) is that the percentage form of EVM normalizes errors to the peak signal state, while SNR form normalizes them to the average signal state. The difference is simply the peak-to-average ratio of the signal.

$$\text{Error Vector Magnitude} = \frac{\text{average error magnitude}}{\text{peak signal magnitude}} \times 100\%$$

$$\text{Signal to Noise Ratio} = -20 \log \frac{\text{average error magnitude}}{\text{average signal magnitude}}$$

Figure 4 Definitions for EVM and SNR are closely related, differing only by the peak-to-average ratio of the signal.

How EVM Measurements are Made

To most effectively use EVM as an analysis and troubleshooting tool, it's useful to have at least a passing familiarity with the underlying measurement methodology, as discussed in the following section.

The need for an ideal reference signal creates a challenging task for an EVM measurement tool. This signal must be of the same modulation type and carry the same data stream as the input signal, but have no noise or waveform degradation of any kind. In practice, generating this signal comprises a good portion of the EVM measurement task. The block diagram of figure 5 shows how this is accomplished.

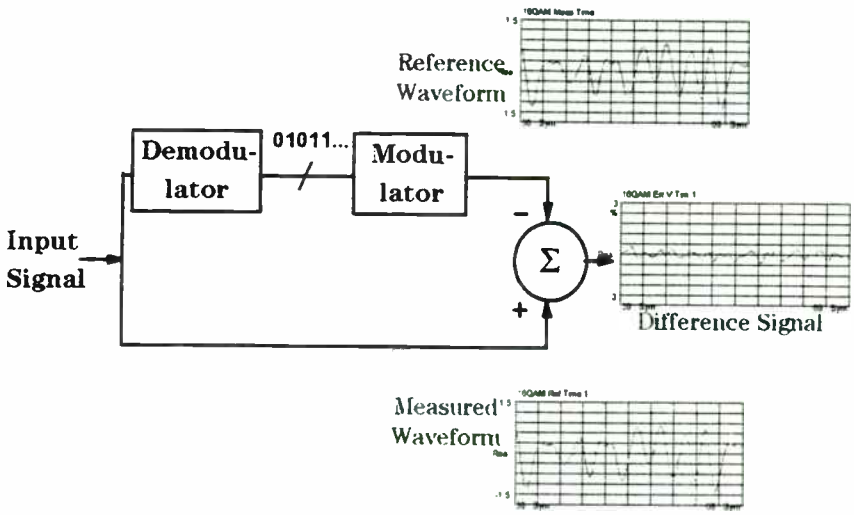


Figure 5 Error vector measurements involve regenerating an ideal, noise-free version of the input signal and subtracting it from the original, in order to obtain the residual noise and distortion signal.

Step 1 - Precision Demodulation

The first step is to recover the incoming digital data stream. In cases where only a single modulation format will ever be analyzed, this could actually be reasonably easy to accomplish, particularly if LSI or other system-specific demodulation hardware was available to be "borrowed".

In a more general implementation, such as in a piece of commercial test equipment, one would expect to be able to demodulate signal formats ranging from simple BPSK to 256 level QAM, at rates from a few hundred to several megasymbols per second. Such implementations are based today on ultra-linear analog-to-digital conversion coupled with powerful DSP, and are user-configurable for most common communications formats. Demodulation algorithms

automatically recover and lock to the carrier and data symbol clocks, and ultimately output the demodulated data as blocks of binary digits.

The accuracy of the flexible DSP demodulator will usually be as good as that of a dedicated demodulator, although it will lack system-specific features such as adaptive equalization and/or error correcting codes to aid under very marginal signal conditions. In addition, its general architecture carries a certain speed penalty -- enough to preclude fully continuous, real-time operation. Thus, demodulation and measurement will take place on individual blocks of data, sampled periodically from the incoming symbol stream.

Step 2 - Regenerating the Reference Waveform

The recovered data bits are next used to create the ideal reference version of the input signal. Assuming flexibility to again be at a premium, this is best accomplished in DSP, taking the recovered data and a predefined modulation algorithm, and calculating the reference signal as individual I and Q waveforms. Being digitally realized, the reference signal can be calculated to any degree of accuracy desired, constrained only by the accuracy of the modulation algorithm and the precision of the math used.

Step 3 - The Complex Comparison

With valid reference and measured waveforms in hand, the two need only be subtracted, sample by sample, to obtain the error vector values. This is only slightly complicated by the fact that both waveforms consist of I and Q components, requiring complex math operations throughout. Fortunately, the DSP engine has more than enough horsepower to handle this, and the resulting vector differences provide the sought-for measurement data.

An interesting sidelight on the flexibly-configurable DSP demodulator: in real-world implementations, it is impractical to vary the ADC's sampling clock to line up precisely with the incoming signal's symbol clock. As a result, we will rarely have actual measured data points at the exact symbol times. This, unfortunately, is the precise time at which we most wish to have data! The answer to this difficulty lies in a special "resampling" algorithm, applied to the incoming ADC samples, which creates an entirely new set of "virtual samples", whose sample rate and timing are precisely in sync with the received symbols.

Applying Error Vector Measurements

Putting a Number on Modulation Quality

The first value of an EVM measurement lies in the single, quantitative figure of merit it provides for a vector-modulated signal. Like THD or SINAD measurements on analog modulated signals, EVM relates the total noise to the overall signal power. Like traditional bit error rate measurements, it is sensitive -- enough to quantify the slightest differences in signal quality, even those occurring across a single stage of the system. However, unlike both types of measurements, it creates its own reference from the transmitted data stream, and requires absolutely no interruption of traffic in order for a measurement to be made.

Figure 6 shows EVM measurements taken at successive test points in a digital RF communications transmitter, proceeding from the modulator to the antenna output. In this case, the largest SNR loss clearly occurs in the final power amplifier, presumably due to various linear and/or non-linear distortion mechanisms. Optimizing this amplifier design will be greatly simplified by the ability to re-measure its EVM after each design iteration, making comparison to this baseline measurement, and seeing precisely the positive or negative effects of each change.

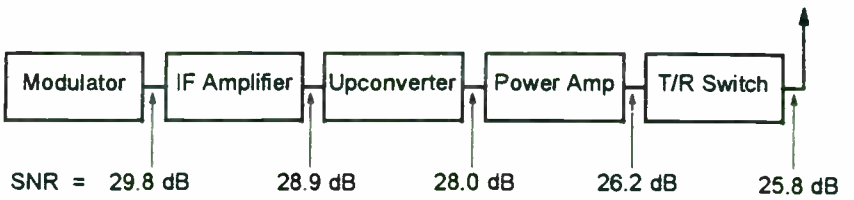


Figure 6 Measurements taken at various points in a digital RF communications transmitter profile the system's SNR "budget", revealing and quantifying possible areas for further design work.

Troubleshooting Signal-to-Noise Problems

Whether a system is completely noise-ridden or simply in need of a few more dB of performance margin, EVM techniques are invaluable for optimizing and/or troubleshooting signal-to-noise ratio problems. By examining the measurement results in the various formats available, the user can gain significant insights into types and causes of noise. The following paragraphs suggest an orderly process for viewing and interpreting the test results.

Step 1 - Compare magnitude error vs. phase error

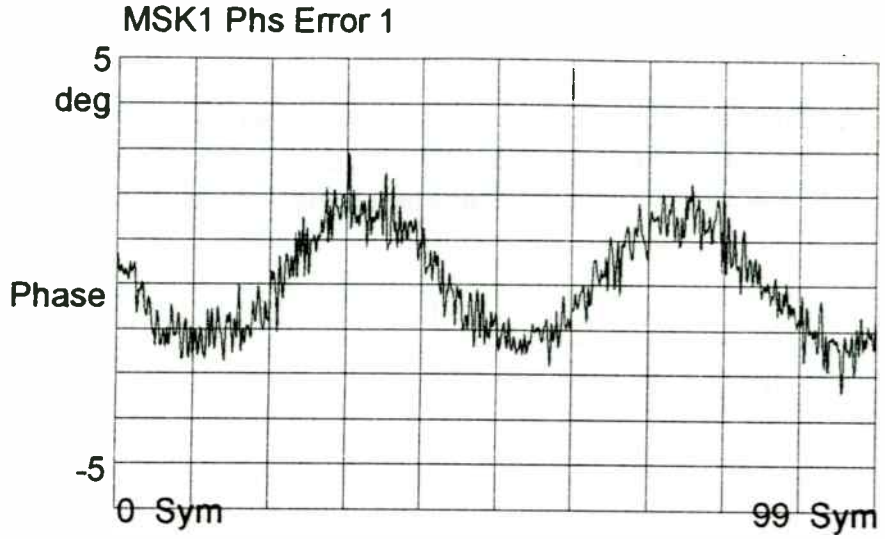
Different noise mechanisms will affect a signal in different ways, whether magnitude only, or phase only, or both simultaneously. Knowing the relative amounts of each can quickly confirm or rule out certain types of problems. Thus, the first diagnostic step is to resolve EVM into its magnitude and phase error components (see figure 3) and compare the relative sizes of each.

When the average phase error (in degrees) is larger than the average magnitude error (in percent) by a factor of perhaps five or more, this indicates some sort of unwanted phase modulation as the dominant noise mode. Look for noise, spurious or cross-coupling problems in the frequency reference, phase-locked loops or other frequency-generating stages. Likewise, residual AM is evidenced by magnitude errors that are significantly larger than the phase angle errors.

In many cases, the magnitude and phase errors will be roughly equal. This indicates a broad category of potential noise types, which can be further isolated with the following steps.

Step 2 - View the error waveforms

Displaying the actual waveform of the error signal can easily distinguish between random noise and steady-state spurious. Figure 7 shows a phase error waveform where the offending signal is



clearly sinusoidal. Because the display calibration is absolute, the actual peak-to-peak phase deviation in degrees can be recorded and tracked throughout the troubleshooting process.

Figure 7 I-Q phase error plot shows waveshape of error-causing signal, in this case a continuous sinusoid of about 3 degrees pk-pk.

Irregular noise may be truly random (thermal or phase noise), or it may be a function of the data waveforms which, for all practical purposes, are also random. In the latter case, symbol domain displays (error versus symbol clock) can be helpful. In figure 8, the significant error "peaks" between symbols indicate that the signal trajectory is not following its optimum path between symbols. This is most likely related to poorly shaped baseband filters, and is probably accompanied by unsatisfactory spectral shaping.

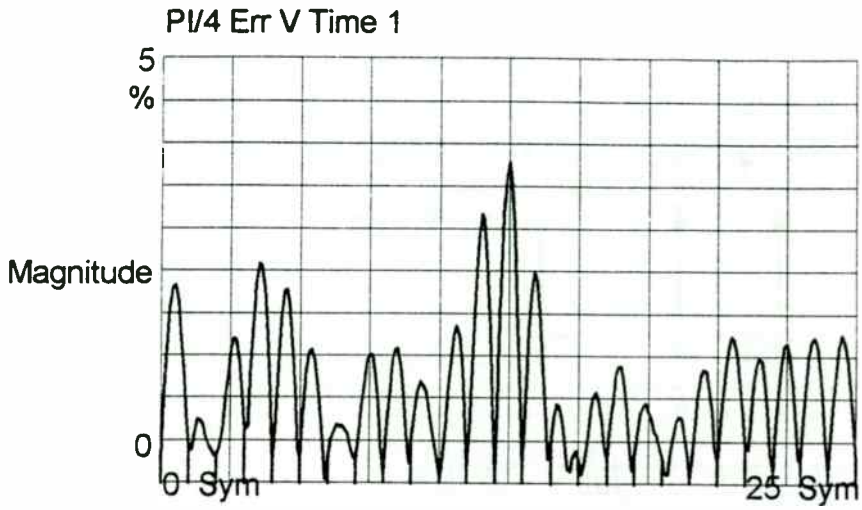


Figure 8 Error peaks between symbols indicate that the magnitude/phase "trajectory" is non-ideal, possibly due to baseband filtering problems.

Finally, try correlating errors to the actual signal waveform itself. Figure 9 displays error magnitude versus signal magnitude, showing a clear relationship between maximum error and signal peaks. In this case the diagnosis is amplitude non-linearities, perhaps in a DAC or amplifier stage. Other useful displays include error magnitude versus I or Q magnitude for locating gain imbalance problems, and error phase versus any of the above.

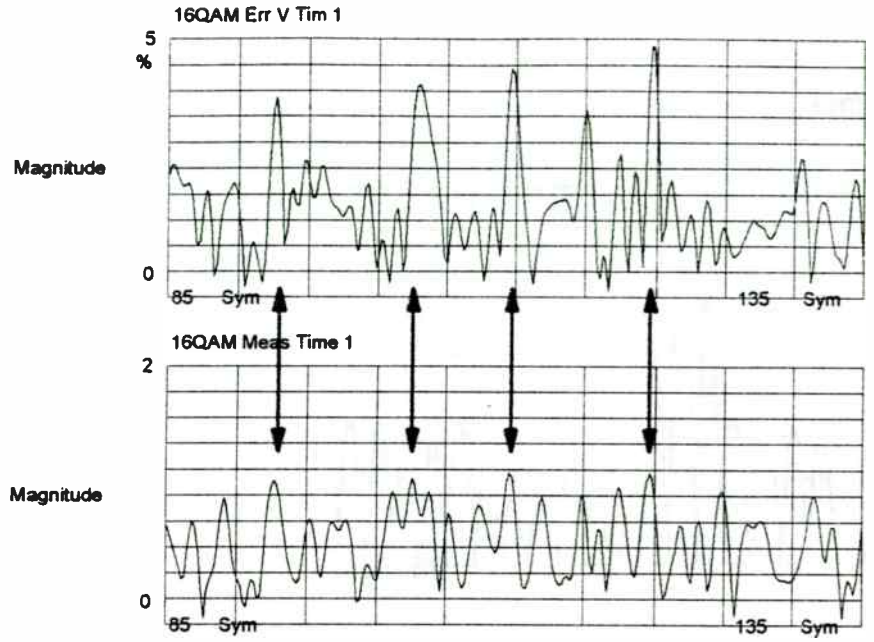


Figure 9 Correlating the error (upper trace) and signal magnitude (lower trace) shows that error peaks occur with each signal peak, indicating an amplitude compression or clipping problem.

Step 3 - View the error spectrum

A final view of the error signal utilizes a Fourier transform of the error waveform to create an error spectrum display (figure 10). In many cases this will confirm that the noise is truly random (i.e. flat across the signal bandpass), but it may also indicate the presence of discrete signals. Identifying the precise frequency of these spurs will often conclusively prove their source, such as power supply ripple, specific isolation problems, etc.

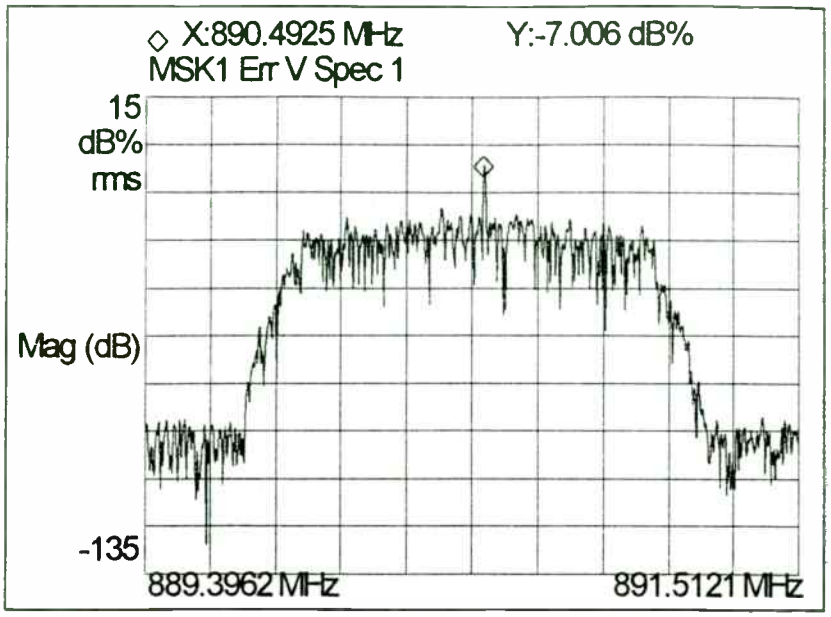


Figure 10 Spectrum of error vector signal clearly shows a spur offset 40 kHz from the carrier, due to crosstalk from the unit's switch-mode power supply.

Evaluating Modulator Frequency Response

The ideal reference waveform created and used in error vector measurements can also give rise to an extremely powerful measurement of channel frequency response. In fact, this measurement, showing gain and phase flatness from the complex (I and Q) baseband input through to the IF or RF output is virtually impossible to achieve outside of this technique.

To understand the measurement, consider first the reference waveform. While existing only as an array of mathematical values it is, in effect, an image of the modulator's baseband input as it would look if it were: a) an analog waveform; b) perfectly noise- and distortion-free; c) a single complex signal rather than separate I and Q waveforms. Thus, without any physical connection to the modulator, we have a picture of the "virtual stimulus" that already exists at its input.

Calculating the ratio of the measured spectrum to the reference spectrum, we easily create a transfer function measurement of the modulated channel (figure 11). With it, one can see the composite response of I and Q baseband filtering, compensation networks, bandpass filters, amplifier frequency response, etc. This calculation is done using trace or register math, or perhaps externally in a computer-based math package. For best readability, the results are viewed in the frequency domain, using traditional gain, phase and group delay plots.

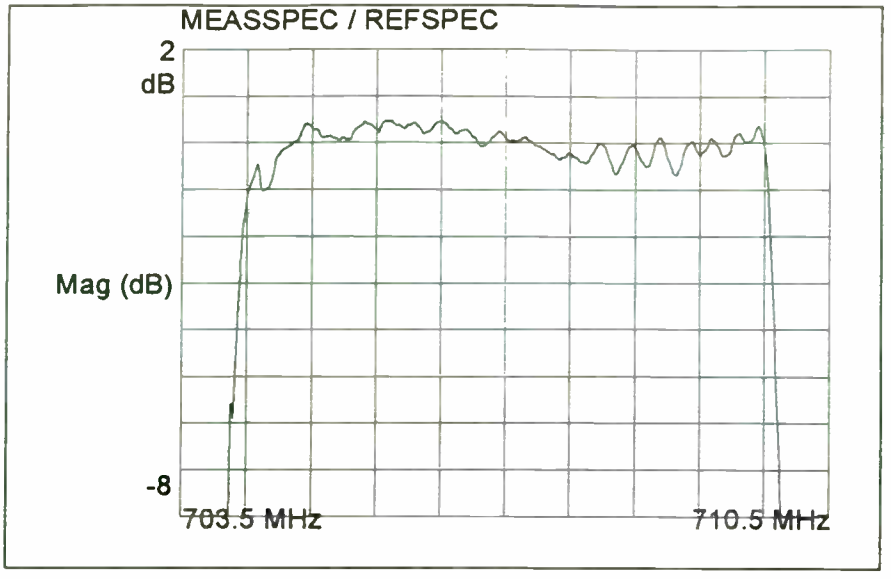


Figure 11 Dividing the actual measured spectrum by the spectrum of the reference signal yields the frequency response of this digital television transmitter. The technique requires no physical access to the modulator's I-Q inputs.

Estimating Bit Error Rate

Given an accurate signal-to-noise measurement for the system, a natural question might be whether this can be used to estimate system bit error rate (BER), using the BER vs. SNR charts found in practically every digital communications textbook. The answer is both no and yes.

On the negative side, bear in mind that textbook analyses invariably assume only white Gaussian noise as the interfering signal, in order to keep the math manageable. In real-world error vector measurements, the definition of "noise" includes white noise, spurious signals, intersymbol interference and all other effects causing imperfect waveshapes. Each of these noise types has its own unique effect on actual BER, which in practice is difficult to calculate (particularly with multiple noise types interacting). It is, however, safe to say that the BER derived from the measured SNR will be a limiting value, i.e. the actual BER will be at least as good, but never poorer than that calculated in this way.

Additionally, in some systems it will be possible to say with relative certainty that white Gaussian noise far outweighs all other noise processes, thus allowing BER to be calculated from SNR with reasonable accuracy. A prime example of this might be a system implemented in DSP throughout its modulator, upconverter and IF stages. Such a design would be fairly immune from the typical distortion mechanisms induced by analog circuits, including harmonic and intermodulation distortion, stray coupling, imperfect filter shapes, mismatch effects, etc.

Offering these and other powerful insights into RF system performance, error vector magnitude measurements are rapidly becoming the signal analysis tool of choice for the digital communications designer. Driven more and more by time-to-market pressures, many are

finding them to furnish an indispensable edge for meeting their goals for both performance and scheduling.

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WIRELESS DEVICE TECHNOLOGIES

Wireless Device Technologies

Session Chairperson: Victor Perrote,
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RF/Microwave Surface-Mount Plastic Package Modeling and Characterization: 16-Lead SOIC Package Outline. **Sedki Riad, Wansheng Su, Iman Salama, James Purdue,** and **Aicha Elshabini-Riad,** Virginia Polytechnic Institute (Blacksburg, VA); **Michael Rachlin** and **Walter (Greg) Baker,** ITT GaAs Technology Center (Roanoke, VA) **167**

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RF/Microwave Surface Mount Plastic Package Modeling And Characterization: 16 Lead SOIC Package Outline

Sedki M. Riad, Wansheng Su, Iman Salama, James Perdue, and Aicha Elshabini-Riad*
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Abstract - This paper presents the effort performed in the areas of package modeling and packaging material characterization at RF/microwave frequencies. Several commercially available plastic molding compounds were characterized in the frequency range up to 14 GHz. The obtained data was used in a subsequent electrical modeling to assess the influence of the dielectric materials involved. Electrical modeling was performed on a 16 lead SOIC plastic package using time domain approach. The developed models have been successfully used by ITT GTC in developing a new generation of power amplifier RFIC's.

I. INTRODUCTION

Consumer expectations for new wireless communication products to be lightweight, compact, and inexpensive have provided an unavoidable and predetermined incentive for RFIC component suppliers to use already established and mature packaging technologies. Surface Mount Plastic Packaging technology is widely used for packaging ICs in industrial, consumer, and automotive electronics. Widespread commercial acceptance of this technology has become a cost effective reality at low frequencies, though the use of plastic packages at RF/microwave frequencies is still limited. Plastic packages provide benefits such as lower cost and weight, and reduced size and board footprint. However, they also introduce performance and functionality limitations. Plastic packages were not originally designed to handle such high frequencies, and the extension of their frequency limits is taking place only in recent years. Packages slated for RF/microwave applications are more demanding than those intended for low frequency analog or digital use. Package modeling and characterization represent one of the key success factors in extending the frequency limits of existing plastic IC packages.

The paper presents the effort performed in the areas of package modeling, and package and material (molding compound) characterization at RF/microwave frequencies. At high frequencies material properties and properties of signal lines/interconnects are equally important. As such, the presented effort dealt with material (molding compound) characterization and modeling and characterization of lead frames and bond wires. While the microwave characterization of the molding compounds performed in this study over a wideband of frequencies can be utilized in a variety of the plastic package structures, the objective of the model development was to develop an electrical model of 16 lead SOIC plastic package, that gained lately a great popularity for packaging wireless RFIC's. The models developed and used will be discussed along with experimental results. Discussion of technique validation, accuracy, repeatability, and variability will be held.

II. MATERIAL CHARACTERIZATION

For dielectric materials, like plastic molding compounds used in RF/microwave packages, their electrical properties can be described by their relative dielectric constant and loss tangent. To measure these properties at microwave frequencies, the two most commonly used techniques are the resonant technique and transmission line technique [2]. The resonant technique relates the measured resonant frequency and quality factor of a resonator to the characteristics of the material from which it was constructed. On the other hand, the transmission line technique uses an assumed model for the response of a dielectric filled transmission line section and then uses either time or frequency domain measurement techniques to match the response of a real transmission line to the model. In this paper, both techniques are used to characterize the dielectric properties of the plastic molding compounds. Two measurement techniques, the HP coaxial probe [1] and the stripline resonator [2], were used to characterize the material properties. Several issues related to the methods are described in the following subsections.

A. Sample Preparation

For the HP probe approach, the sample preparation is relatively simple. Only a flat surface and sufficient thickness are required for the sample. This is usually

* *Currently with ITT-GTC*

the case for plastic molding compounds. Choosing the compounds with a flat surface is the only work for sample preparation. No mechanical work is required.

The test sample for resonant structures is shown in Fig. 1. To separate the dielectric loss from the conductor loss [2], four resonant structures are chosen as test samples. For a stripline resonator, the basic design parameters are the length of the resonator section, the width of the resonator section, the thickness of the conductor line, and the substrate thickness. The design considerations on choosing these parameters are explained as follows.

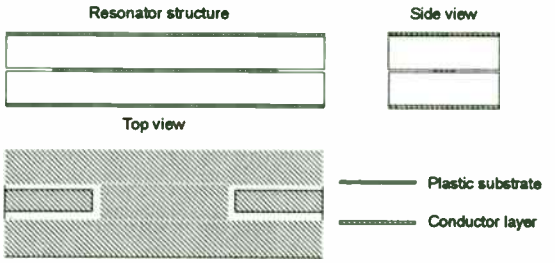

Figure 1. Test Sample for Resonator Structure.

1) Length of the Resonator Section

Since the resonant techniques can give the material properties only at base resonant frequency and its harmonic frequencies, it is desirable that the first resonant frequency be low. In other words, the resonant section should have enough length. The size of the substrate available was 2"x0.5", the length of the resonator section was chosen as 1.5 inches. The quater inches on both sides were reserved for the launchers. The coplanar waveguide/stripline overlap was chosen as 100 mils and can be adjusted during the measurement. For a dielectric constant of around 4, the first resonant frequency is about 2 GHz.

2) Electrical Coupling

Electrical coupling is a critical issue to the resonant techniques. If the coupling is too weak, the signal will be too small to enable an accurate measurement. If the coupling is too strong, however, the loading effects from the system will lower the measured quality factor of the resonator. In practice, -40 dB coupling is desired for neglecting the loading effects. The desired coupling can be obtained through choosing proper distances between the launchers and the resonator section. This can be easily realized at a single frequency or in a narrow frequency band. In this study, the frequency band of interest is from a few GHz up to 10 GHz. The traditional coupling approach simply cannot cover such wide frequency band. A new design (patent-pending) using coplanar line to stripline transition, as shown in Fig. 1, is used to solve this problem. The center conductor of the coplanar line is designed to overlap the center resonator line (100 mils) to provide enough coupling at low frequency. Since the coplanar line is built on the top surface, the overlap length can be trimmed to satisfy the coupling requirements at high frequencies.

3) Stripline Configuration

In order to separate the dielectric loss from the conductor loss, we can vary the dimensions of the striplines, thickness of the conductor strip, width of the stripline and thickness of the substrate. The thickness of the copper strip for building stripline is chosen as 1 mil. The other two design parameters which can be changed are the width of the stripline and the thickness of the substrate. Variations in substrate thickness and stripline width are used to insure adequate distribution of g(t,w,b) values.

B. Measurement Results

Measurement results using the two methods are presented in the following sections.

1) HP coaxial probe

The plastic molding compounds were measured using the HP coaxial probe. Several experiments were performed to validate the approach. First, the sample thickness was determined by measuring the samples with different layers of the plastic molding compounds. This experiment has been performed up to three layers of the compounds. Due to the tiny size of the coaxial open end, no significant difference has been found. Based on this experiment, all the measurements were performed using only one layer of the compounds. Second, three samples were measured for each material to check the repeatability of the probe approach. As seen from the following graphs, the repeatability is in the order of 1%. Third, the calibration scheme was investigated using different calibration standards. To perform the full one port calibration, three standards are required. Two of them, the open and short standards, are relatively good. The third standard is a coaxial load. Since the load is not a mechanical match with the probe end, it is actually connected before the probe. This degrades the effectiveness of the calibration process. The alternative approach is to use other standards whose material's properties are well known. Two such materials, water and Teflon, were used as the standards. From the measurement results, the measurements of using Teflon standard gave much better results. This is reasonable because Teflon has a

closer dielectric constant to the compounds and offers better sensitivity. The measurement results are shown in Figs. 2 and 3.

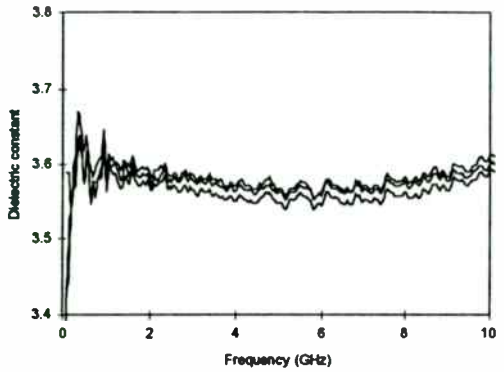

Figure 2. Dielectric Constant Results Using the HP Probe.

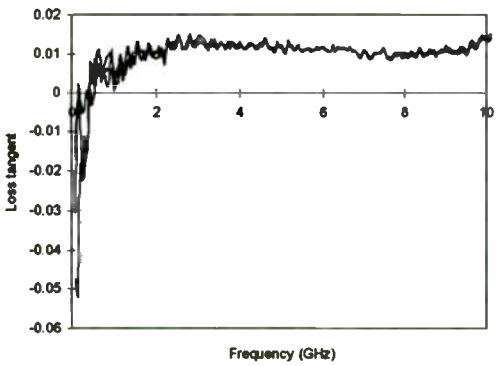

Figure 3. Loss Tangent Results Using the HP Probe.

2) Stripline resonator

The stripline resonator method was also used to characterize the two compounds. Based on the design considerations, four samples with different geometrical structures were used to characterize its dielectric properties, dielectric constant, and loss tangent. Measurement results are shown in Figs. 4 and 5.

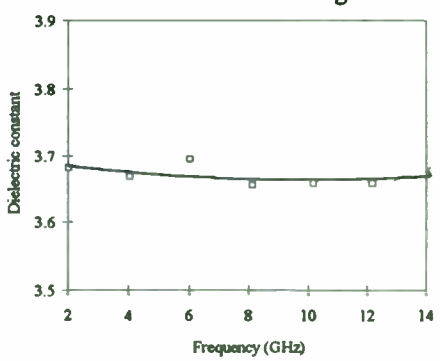

Figure 4. Dielectric Constant Results Using the Stripline Resonator Method.

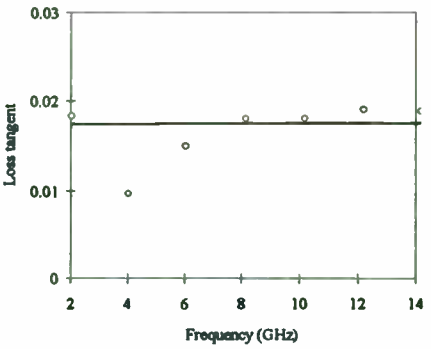

Figure 5. Loss Tangent Results Using the Stripline Resonator Method.

C. Error Analysis

Based on the HP specifications, the HP probe's accuracy is ±5% for measuring dielectric constant and ±0.05 for measuring the loss tangent. In this section, the measurement accuracy for the stripline resonator approach is addressed.

1) Source of Errors

The main error terms using stripline resonator to characterize dielectric materials are as follows.

Error from electrical measurements:

- ➢ Frequency measurement error 0.1%
- ➢ S11 amplitude precision 0.05 dB
- ➢ S11 phase precision 0.5 degree

Error from mechanical measurements:

- ➢ Dimensional measurement error 0.5%±1mil

Error from resonator model:

- ➢ End effects +2%
- ➢ Gap between the substrates -1.5%

Environmental conditions:

- ➢ Temperature change 3oF
- ➢ Humidity change 5%

Error from numerical calculation:

- ➢ Truncation error 10e-5
- ➢ Computation error 10e-5

2) Estimated Measurement Accuracy

Based on the source of errors listed above, the estimated measurement accuracy is as follows.

- ➢ Dielectric constant 3%
- ➢ Loss tangent 0.01

D. Discussion

From the typical measured S21 waveform shown in Fig. 6, it is clear that the resonant peaks are distorted

above 14 GHz. This is because the unwanted resonances from the resonator structure itself, not the central resonant section, corrupt the waveform. It shows the upper frequency limit of the structure. From the data, it appears that the materials will perform well at even higher frequency range. In order to characterize the performance at frequencies above 14 GHz, the resonator structure needs to be redesigned.

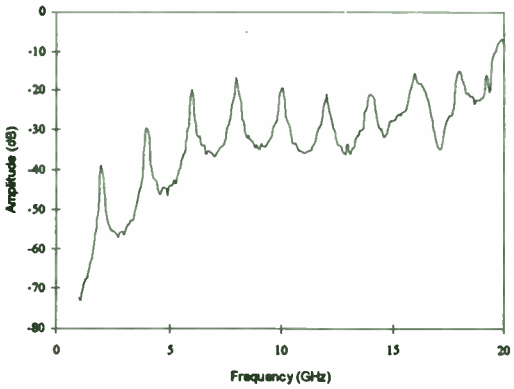

Figure 6. Typical S21 measurement results of stripline resonators.

III. ELECTRICAL MODELING

In order to model the lead frame, there are two main approaches commonly used, the analytical approach and experimental approach. For the analytical approach, a field solver is used to obtain the circuit parameters by solving Maxwell equations. Many commercial field solvers are available in the market, such as Ansoft, HFSS, Sonet and Zeland. For the experimental approach, the circuit parameters are extracted from the measured circuit responses. The experimental approach can be performed in both frequency domain or time domain. However, the time domain approach has some important advantages which make it necessary to use in this modeling. The advantages are the ability to identify directly the various contributions (reflections) from the different discontinuities of the structure under test and its high spatial resolution.

A. Time Domain Techniques for Package Modeling

Time domain techniques have been used by many investigators to model transmission line structures. The approach is based on TDR measurements to construct an initial model for the circuit under test. Starting with this approximate model, and using a transient circuit analysis computer program such as MTCAP [3], a simulation of the TDR measurement is performed. Both measured and simulated TDR waveforms are compared, and the values of the different components in the model are adjusted until a reasonable fit between the two waveforms is achieved.

B. Time Domain Measurement System

Fig. 7 shows the TDR setup used for the measurement and waveform acquisition. The measurement system consists of an HP-54124 sampling oscilloscope, a Picosecond Pulse Labs PSPL-4015 pulse generator, a custom made microwave test fixture and a data acquisition computer. The HP oscilloscope has 7 ps transition time or 50 GHz equivalent frequency bandwidth. The oscilloscope also has an internal pulse generator in the TDR channel. However, the transition of the internal pulser has slower transition which is about 40 ps. So, an external PSPL pulse generator with 15 ps transient time is used to substitute the internal pulse generator. The resultant transient time of the measurement system under this configuration is less than 20 ps. The intercontinental test fixture is used to provide both electrical and mechanical connection for an SOIC package.

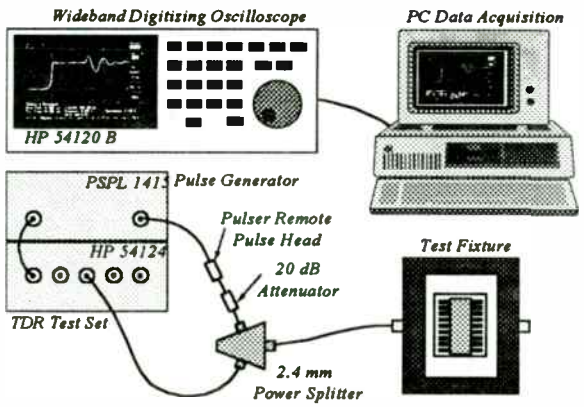

Figure 7. Time Domain Measurement System Setup.

The test fixture with the SOIC package under test is attached at the end of a 50-Ohm reference transmission line. A reference waveform is acquired as the negative of the reflection of a short circuit located at the test fixture interface to the reference line. The TDR response waveform for the fixture and package under test is also acquired. Both the reference and response waveforms are stored in a form suitable for later use in the computer simulation program.

C. Establishing an Electrical Circuit Model

A typical TDR response from an SOIC package is shown in Figure 8. Examining the TDR response of the package structure, the waveform dips and peaks are recognized as reflections caused by distributed or

lumped discontinuities in the transmission path. Typically, these discontinuities can be modeled by one or more ideal components connected in series or in shunt with the circuit network model. In order to determine the proper model for these discontinuities, one has to become familiar with typical reflection responses of ideal component discontinuities, e.g., resistors, inductors, and capacitors. The behavior of various nonideal components and/or combinations of ideal components needs to be studied as well.

It is important to recognize that during the modeling process, the discontinuities are dealt with one at a time, in order of their physical existence away form the launch end. This is a unique feature of performing the modeling in the time-domain reflectometry approach. The reason can be attributed to the following: once the model component for a discontinuity is fixed, changing the model components of later discontinuities does not affect the response waveform of earlier time epochs. As a result, the modeling process involves dealing with only one discontinuity at a time.

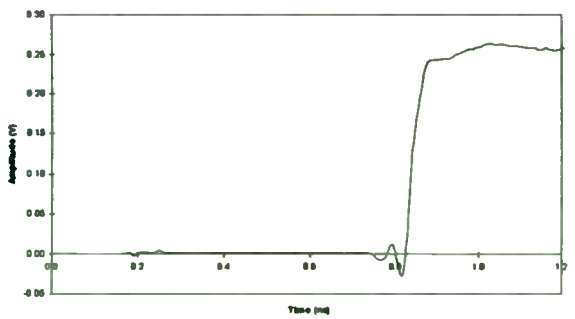

Figure 8. A Typical TDR Response of an SOIC Package.

D. Modeling Procedure

To illustrate the modeling process, the modeling of the lead frame with a TDR response shown in Fig. 8 will be presented as an example. Both the TDR reference and response waveforms for the package were experimentally acquired and the reference waveform is illustrated in Fig. 9. Utilizing the results of the TDR study on ideal components, as well as the physical nature of the structure, an initial model (physically based) for the structure can be determined. The first reflection seen in the response waveform of Fig. 8 can be attributed to an inductor connected in series with the line. The second reflection can be modeled as a capacitor connected in shunt with the line, the third a inductor in series with the line and the fourth a capacitor in shunt with the line. The complete model based on these observations is thus put together, shown in Fig. 10.

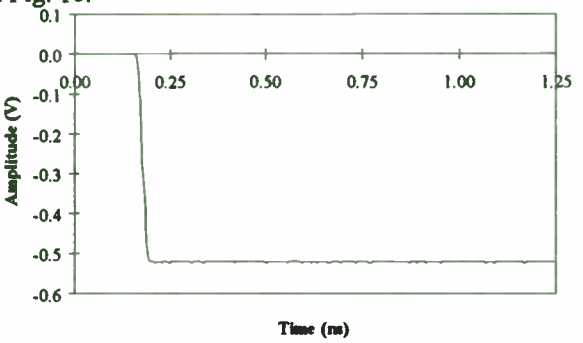

Figure 9. A Typical TDR Reference Waveform.

The next step is to assign initial estimates to every component. This is usually done through try and error approach. However, some approximate relationships have been also developed to determine the inductance and/or capacitance, for small reactive discontinuities, provided that the test pulse can be approximated by a simple ramp, discontinuity component values are small.

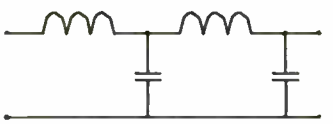

Figure 10. A Simplified Model for the SOIC Package.

As shown in Fig. 10, each small discontinuity is modeled by one element, making the available relations very rough approximations. However, more than one element may be needed to model a complicated discontinuity. Also, in the case of multiple discontinuities, the leading edge of the test pulse is modified by successive reflections, thereby degrading the accuracy of modeling the later discontinuities. Therefore, in the case where a discontinuity is modeled by two or more elements, as well as in the case of too closely spaced discontinuities, the task of separating the various component contributions will be a very difficult one.

Another method that can be used to assign initial values for the model of components is to use other measurement approaches to obtain more information about the structure being modeled. Information such as electrical properties, mechanical properties and material properties: dc resistance, low frequency inductance, capacitance, dimensions and dielectric properties of the material are also important. The more we know about the component, the better model we can obtain.

With the availability of the initial, physically based electrical network model, and the reference waveform, the computer simulation can be started. The initial network model is used in the MTCAP to simulate the component under test. Using the acquired reference waveform as the excitation, a simulated TDR response waveform is computed as the reflected transient response of the network as its input port. The simulated response is then compared with the measured TDR waveform, and the value of the different components in the model are adjusted iteratively until the simulated reflection matches the measured one.

This computer simulation and iterative adjustment procedure was applied to the SOIC package under test. Fig. 11 illustrates the close match achieved between the experimental and simulated response waveforms.

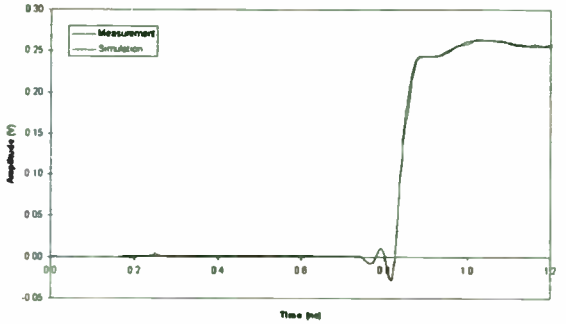

Figure 11. Comparison of Simulated and Measured TDR Responses.

The MTCAP is a software package developed at Virginia Tech. Basically, the package is a custom tailored SPICE package. The package has a very convenient feature of using the real measurement waveform as the input source and comparing the measurement response with the simulated circuit response. Based on the network theory, if the two networks with the same input exciting signal and obtain the same response output, the two networks are equivalent. Clearly, the two network structures are not necessary the same. In other words, the network is not unique.

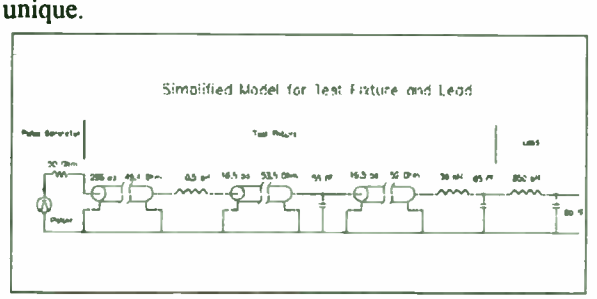

Figure 12. Test Fixture and the Circuit Model for the SOIC Lead.

E. Obtained Models for SOIC Leads

Using the approach explained above, the circuit model for the SOIC lead is obtained as shown in Fig. 12. A sample of the obtained MTCAP circuit file is given in Table 2. The model shows adequate fit between the measured TDR response and simulated TDR response. The actual fit was illustrated in Fig. 11.

```
C*************************************************************
C        MTCAP Model for ITT Commercial SOIC Package
C                  (Lead Frame)
C*************************************************************
  B1, N(1,0), VXTS1=1, NINPTS=500, NAME=SHREF.DAT
  B2, N(1,2), RRS=50.00
C*************************************************************
C          ***** Model for Test Fixture *****
C*************************************************************
  B3, N(2,0), TLINDEL0=288.0E-12, R0=49.4, N<3,0>
  B4, N(3,4), LL1=0.50E-12, L0=0.0
  B5, N(4,0), TLINDEL1=16.5E-12, R0=53.5, N<5,0>
  B6, N(5,0), CC1=55.0E-15, C0=0.0
  B7, N(5,0), TLINDEL2=10.5E-12, R0=52.0, N<6,0>
  B8, N(6,7), LL2=30.0E-12, L0=0.0
  B9, N(7,0), CC2=55.0E-15, C0=0.0
C*************************************************************
C            ***** Model for Lead *****
C*************************************************************
  B10, N(7,8), LL3=30.0E-12, L0=0.0
  B11, N(8,0), CC3=55.0E-15, C0=0.0
C*************************************************************
C          ***** Model for Short Circuit *****
C*************************************************************
  B12, N(8,0), TLINDEL01=65.0E-12, R0=1.4, N<9,0>
  B13, N(9,0), RRL=0.4
C*************************************************************
    TMAX=1.250E-9
    TMIN=0.000E-9
    NUMPTS=500
    PRINT NODE VOLTAGES=1:2
 WAVEFORM COMP=2, WINDOW=0,2,1,500, WAVEFORM
NAME=SHT1.DAT
END
C*************************************************************
```

Table 2. A Sample MTCAP Circuit File.

F. Bondwire Model

Since wire bonds are extensively used in SOIC packages for providing connection among the IC chips and package leads, a model for bondwires is desirable to designers to consider their effects, especially at RF and microwave frequency range. A custom made SOIC package with a long bondwire is used to perform the model. Examining the bondwire structure reveals that it can be approximated as a straight wire above a ground plane for a small bondwire segment. Cascade of the all segments of the bondwire enables us to obtain a model for the bondwire as shown in Fig. 13. Fig. 14 illustrates the corresponding time domain fit between

the simulation from the model and the actual measurement.

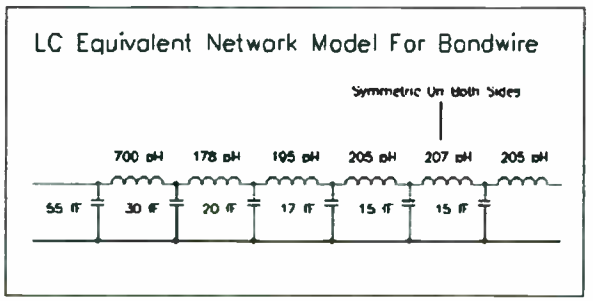

Figure 13. Lump LC Equivalent Network Model for Bondwire.

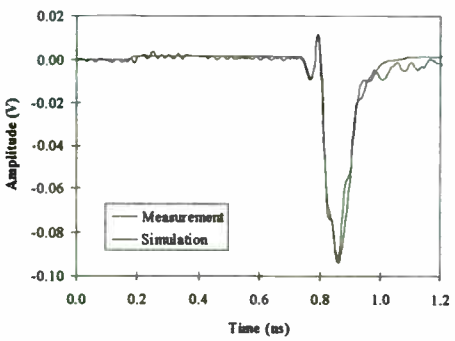

Figure 14. Comparison of Simulated and Measured TDR Responses for Bondwire Structure.

G. Verification of The Obtained Model

For verification purposes, the S-parameters of the measured experimentally using the HP 8510 Network Analyzer and the simulated one from the time domain model are compared. This measurement was conducted for the frequency range 1-20 GHz, with a frequency step of 50MHz. Using the system's built-in full 2-port calibration process, the S-parameters were determined. In the meantime the S-parameters of the obtained model was computed using SPICE circuit analysis software package. The results of both the SOIC package's measured S-parameters and that computed from the estimated model are compared to each other, and are illustrated in Fig. 15. The figure shows a reasonably good agreement between the measured S-parameters and that calculated from the estimated model. The discrepancies can be attributed to the inaccuracy of the measurement, and to the mismatch between the measured response waveform and the model's response waveform.

H. Validity of the Modeling Approach

If the insertion impulse response of two networks are equal, then the S_{21} scattering parameters of the two

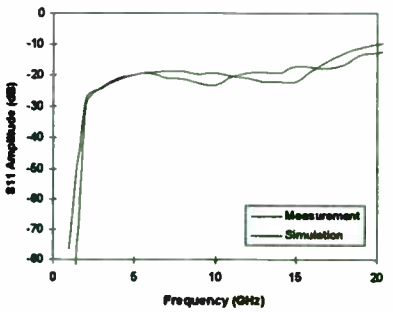

Figure 15. Comparison of Results From the Measurement and Simulation Using the Obtained Circuit Model.

networks are equal. Note here that the driving source waveform is the ideal impulse. In practice, the driving source waveform is never an ideal impulse or step. Thus in the epoch near t=0+ (which corresponds to |s|-->infinity) information will be lost, i.e., some waveform variations will not appear due to the slowness of the leading edge of the applied signal. Consequently, any model based upon an observed physical waveform (as in Fig. 11) will not contain information extending endlessly to higher frequencies. Also, a similar argument can be made for low frequencies if it cannot be said "that for all practical purposes, the waveform has reached its final value at the end of the chosen time window (t=1.2 ns in Fig. 11). Therefore, there could be more than one model that will perform satisfactorily over the frequency band of interest. In other words, this technique (or any other in the time or frequency domains) will not yield a unique model nor will it provide information for all times and frequencies [4]. Also, its quality will depend on the individual performing the modeling. An experiment designed to study the nonuniqueness of the model and its dependence on the human factor is needed and proposed for a future research.

The accuracy of the obtained model depends on two main factors. The first factor is the adequacy of modeling distributed discontinuities by a suitable number of lumped components, and the second factor involves the accuracy of the computer simulation for the network identification problem, e.g., the transient analysis time interval, iteration accuracy, and computation errors. The frequency responses of the different models showed that the human factor is of second order and should not be critical for this modeling technique.

I. Variability Analysis for Bondwire Model

A variability analysis has been performed as shown in Fig. 16. Based on the bondwire model obtained, a

10% increment on inductance and a 10% reduction on capacitance was simulated and denoted as L Values +10% in the attached graph. The other simulation with a 10% inductance reduction and 10% capacitance increment was performed and denoted as L Values -10%. Comparing the results shown in the graph, it can be concluded that the error of the bondwire model is within the error bounds of a few percent.

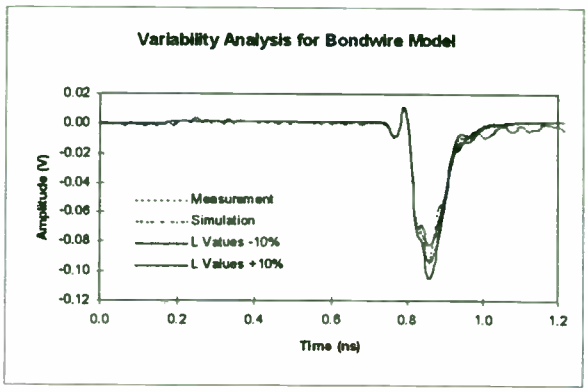

Figure 16. Variability Analysis for the Bondwire Model.

J. Repeatability of the Samples

Three custom made bondwire samples are measured to investigate the repeatability of the wire bonding process. The good agreement shown in Fig. 17 demonstrate the repeatability of the wire bonding process.

IV. CONCLUSION

Characterizing the plastic molding compounds reveals that the dielectric constant of the compounds is almost constant and loss tangent is less than 0.02 for frequencies up to 14 GHz. This discovery demonstrates the potential of the plastic compounds as packaging material for devices working at microwave frequencies. Using the plastic compounds to substitute the traditional ceramic material for the microwave packaging will lead to a significant cost savings over the cost of ceramics.

The electrical modeling enables the designers to improve the circuit performance by considering the

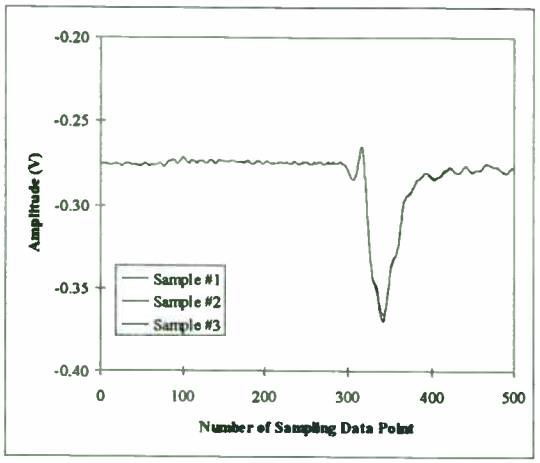

Figure 17. Repeatability of the Wirebond Samples.

packaging effects including both interconnections and packaging materials. The results presented herein provide a better understanding of the frequency behavior of molded plastic packages and demonstrate the feasibility of using time domain and EM simulators to design such electronic packages. The developed models have been successfully used by ITT GTC in developing a new generation of power amplifier RF IC's.

References

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[3] S. M. Riad and K. M. Fidanboylu, *The Modified Transient Circuit Analysis Package (MTCAP)*, User's Manual, Virginia Tech, VA, 1988.

[4] S. T. Salvage, A. A. Riad, and S. M. Riad, "*Wideband Device Modeling Using Time Domain Reflectometry*," IEEE Trans. Instrum. Meas., Vol. IM-32, No. 1, March 1983, pp.134-136.

The Zero Bias Schottky Diode Detector at Temperature Extremes - Problems and Solutions

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Abstract - **The zero bias Schottky diode detector is ideal for RF/ID tag applications where it can be used to fabricate a receiver which consumes no primary power. However, its performance is heavily dependent upon its saturation current, which is a strong function of temperature. At both low and high temperature extremes, this dependence can lead to degradation in performance. The behavior of zero bias Schottky diodes is analyzed, experimental data is given, and a solution to the loss of performance at cold temperatures is presented.**

I. INTRODUCTION

The zero bias Schottky diode detector [1], [2] is widely used in RF/ID and other applications where no primary (DC) power is available in the standby or "listen" mode. When combined with a simple antenna to form a receiver, it lacks the sensitivity of the superheterodyne receiver, but offers the advantages of very low cost and zero power consumption. The single diode detector is shown in Figure 1.

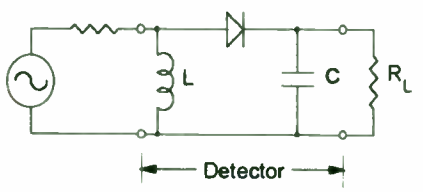

Figure 1: Diode detector

R_L is the video load resistance. L, the shunt inductance, provides a current return path for the diode, and is chosen to be large (compared to the diode's impedance) at the input or RF frequency. C, the bypass capacitance, is chosen to be sufficiently large that its capacitive reactance is small compared to the diode's impedance but small enough to avoid having its reactance load the video circuit [3].

Such detector circuits display a characteristic transfer curve of output voltage vs. input power as shown in Figure 2.

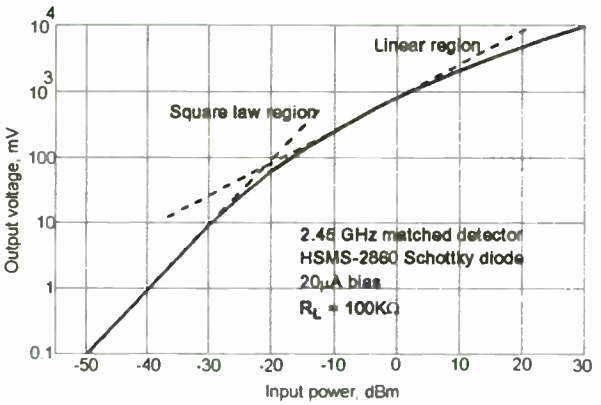

Figure 2: Detector transfer curve

P_{in} is the RF input power applied to the detector circuit and V_o is the output voltage appearing across R_L. As can be seen from Figure 2, the transfer curve follows a square law (output voltage proportional to the square of input voltage) at low levels of input power and displays quasi-linear behavior (output voltage proportional to input voltage) at higher levels.

A key performance criterion for a diode detector is the slope of the transfer curve, γ, generally expressed in mV/μW. One can plot γ vs. P_{in} as shown in Figure 3.

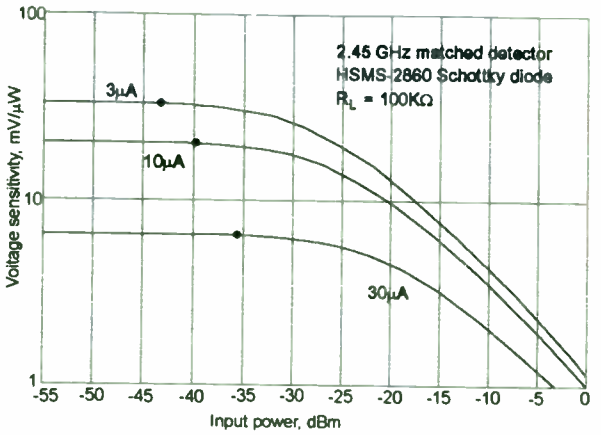

Figure 3: γ vs. input power

Such a plot is a more sensitive indicator of detector performance than the transfer plot of Figure 2. Note that γ is a function of externally applied bias (among other parameters) in conventional (DC biased) detectors. It can be noted from Figure 3 that external bias can be adjusted to trade sensitivity for a wider dynamic range of square law response.

A Schottky diode can be represented by the linear equivalent circuit shown in Figure 4.

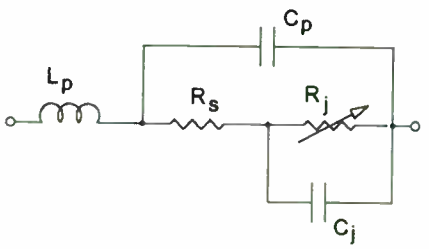

Figure 4: Diode equivalent circuit

L_p is package parasitic inductance, C_p is package parasitic capacitance, R_s is the diode's parasitic series resistance, C_j is junction parasitic capacitance and R_j is the diode's junction resistance.

Figures 1 and 4 can be combined to create both an RF and video equivalent circuit of the Schottky diode detector. The RF equivalent circuit is given in Figure 5.

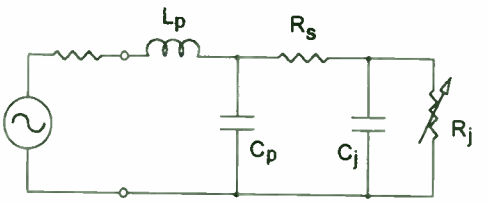

Figure 5: RF equivalent circuit of a detector

Note that this equivalent circuit does not include the RF impedance matching network which is normally found between the diode and the 50Ω source.

Figure 6 shows the video equivalent circuit for the diode detector.

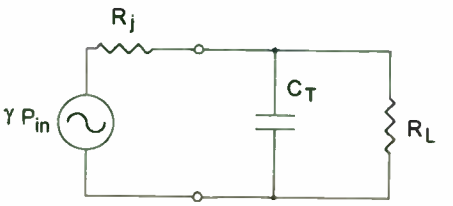

Figure 6: Video equivalent circuit of a detector

where C_T is the sum of bypass capacitance and input capacitance of the video circuit.

L_p, C_p, and R_L are constants. R_s has some small variation with temperature, but that variation is not a significant parameter in this analysis. C_j is a function of both temperature and DC bias, but this analysis concerns itself with the zero bias detector and the variation with temperature is not significant. R_j is a key element in both equivalent circuits - its behavior clearly will affect the performance of the detector circuit.

While many commercial applications cover a narrower temperature range, the analysis which follows will include the 140° from -55° to +85°C.

II. JUNCTION RESISTANCE

Three different currents affect the junction resistance of a Schottky diode. The first is the diode's own saturation current, I_s. The second is extemally applied bias current, I_o. The third is $I_c = V_o/R_L$, the circulating current produced by rectification in the diode. In the small signal region of interest in this discussion, where $I_c < I_s$, the equation for junction resistance is

$$R_j = \frac{n\,k\,T}{q\,I_s + I_o} \qquad (1)$$

where n is the diode ideality factor (emission coefficient), k is Boltzmann's constant, q is the electronic charge, and T is temperature in degrees Kelvin.

The equation for saturation current is given by

$$I_s = I_{so}\left(\frac{T}{T_o}\right)^{\frac{2}{n}} e^{\frac{-q\psi}{k}\left(\frac{1}{T}-\frac{1}{T_o}\right)} \qquad (2)$$

where T_o is 273°K (room temperature), I_{so} is saturation current measured at room temperature and ψ is the metal-semiconductor Schottky barrier height (energy gap).

Combining these two equations produces a relation for R_j as a function of temperature.

For a high performance zero bias Schottky detector, such as the Hewlett-Packard HSMS-2850, I_{so} = 3mA, n = 1.2 and ψ = 0.35 eV. Using these values in (1) and (2) results in the computed junction resistance shown in Figure 7.

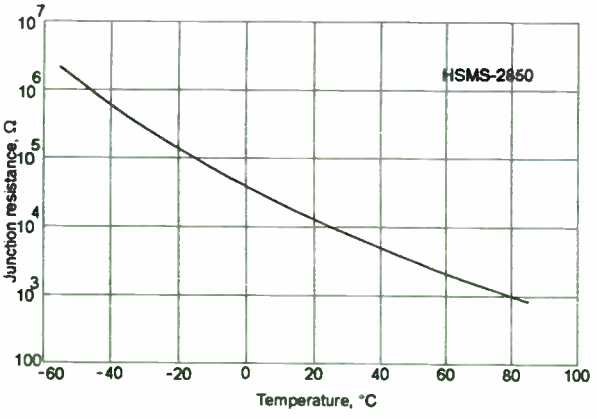

Figure 7: R_j vs. temperature for the HSMS-2850

As can be seen from this figure, R_j varies by three and a half decades over the 140°C temperature range.

This variation in R_j will affect two performance parameters of vital interest to the detector circuit designer.

III. PERFORMANCE OVER TEMPERATURE

Schottky diode

The two performance parameters of interest to the circuit designer are the video bandwidth and voltage sensitivity of the detector. The analysis of video bandwidth as a function of temperature is straightforward [3] and will be shown first.

The video equivalent circuit shown in Figure 6 has a low pass filter response, with a 3dB cutoff frequency defined by

$$f_c = \frac{1}{2\,\pi\,C_T\,R_T} \qquad (3)$$

where

$$R_T = \frac{R_j\,R_L}{R_j + R_L} \qquad (4)$$

Using the variation in R_j given in Figure 7, the variation in video bandwidth can be computed. Typical values of R_L = 100KΩ and C_T = 50pF were used to compute the curve of cutoff frequency vs. temperature shown in Figure 8.

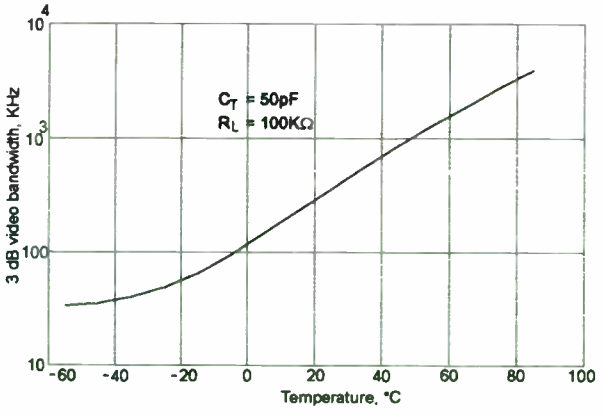

Figure 8: f_c vs. temperature for the HSMS-2850

As can be seen from this plot, video bandwidth can shrink to a value as low as 30 KHz at -55°C. Many RF/ID systems [4] use data rates which are higher than 30 KHz. Of course, a reduction in C_T will improve bandwidth, but there are practical limits to how low total capacitance can be made. Similarly, a reduction in R_L will increase video bandwidth, but at the expense of voltage sensitivity, according to the following relationship.

$$\gamma = \gamma_{oc} \frac{R_L}{R_L + R_j} \qquad (5)$$

where γ_{oc} is the detector's voltage sensitivity for R_L = infinity.

The analysis of voltage sensitivity as a function of temperature for a Schottky diode detector is complex. Harrison and Le Polozec [5] have provided an exact analysis for zero frequency, as follows:

$$I_o\left(\frac{\Lambda}{n}\sqrt{8 R_g P_{inc}}\right) = \left(1 + \frac{I_o}{I_s} + \frac{V_o}{R_L I_s}\right) e^{\left[\left(1 + \frac{R_g + R_s}{R_L}\right)\frac{\Lambda}{n} V_o + \frac{\Lambda}{n} R_s I_o\right]} \qquad (6)$$

where I_o is the zero-order modified Bessel function of the first kind, P_{inc} is the incident RF power, R_g is the generator or source resistance, $\Lambda = q/kT$. This equation can be solved for P_{inc} as a function of V_o using Mathcad[1] and the worksheet shown in [6].

An examination of (6) will reveal that only Λ and I_s are functions of temperature, aside from the small variation of R_s mentioned earlier. This equation can be applied to a zero bias Schottky diode, such as the HSMS-2850, terminating a 50Ω source as shown in Figure 1. Curves of voltage sensitivity vs. input power and temperature can then be calculated as shown in Figure 9.

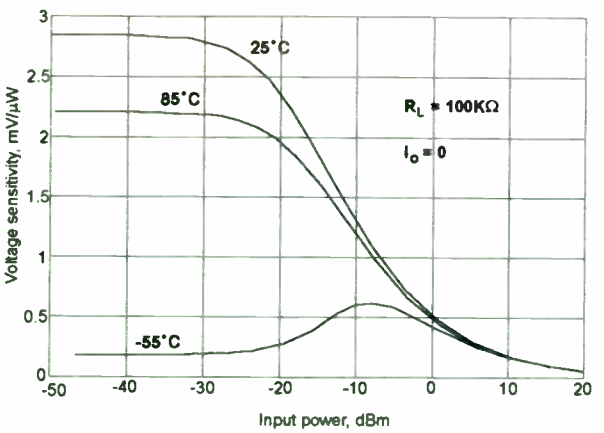

Figure 9: γ vs. P_{in} and temperature for the HSMS-2850 at zero frequency

[1] Product of MathSoft, Inc., 201 Broadway, Cambridge, Massachusetts

Due to the choice of the optimum value for I_{so} [2], the diode shows reasonable sensitivity at 25°C (despite the lack of an RF impedance matching network) and good square law response (flat γ) almost to -30 dBm. At 85°C, I_s has increased beyond the optimum, and sensitivity suffers slightly. However, behavior at -55°C does not follow traditional models; sensitivity peaks at -8 dBm, and drops off to less than half the peak value at small signal levels where detectors are most often used. This anomalous effect is the consequence of the very low value of I_s at -55°C.

While a powerful and convenient tool, (6) neglects the effects of diode junction capacitance, package parasitics and RF input matching network, all of which are part of practical diode detectors.

Detector diode and circuit

In [1], several detector designs with RF impedance matching networks are presented, along with test data obtained at 25°C. The 2.45 GHz single-diode detector designed around the 25°C characteristics of the HSMS-2850 device was chosen for further analysis and test over temperature.

An analysis tool [7] was created to add the effects of frequency and reactive circuit elements to (6). This tool was applied to the 2.45 GHz detector and the resulting data were compared to performance measured on a prototype circuit. Calculated and measured data are shown in Figure 10.

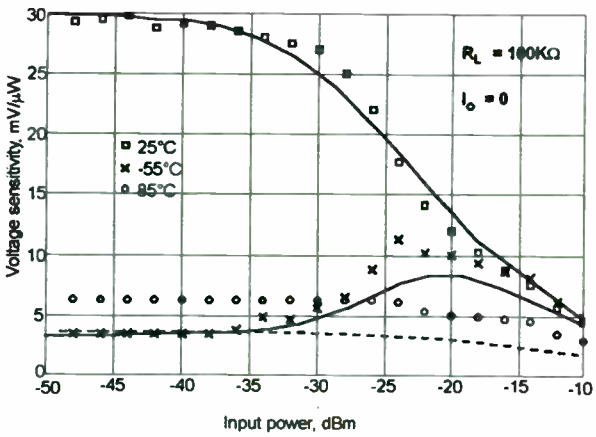

Figure 10: γ vs. Pin, 2.45 GHz detector

In this figure, the top curve is the calculated sensitivity at 25°C, which is compared to the measured data (indicated by boxes). The middle curve and "X" marks compare calculated and measured at -55°C. The bottom curve and circles compare calculated and measured at 85°C. Note that in this case, where a RF input impedance transformer has been placed between source and diode, voltage sensitivity is ten times greater at 25°C. However, sensitivity drops rapidly at 85°C, compared to the unmatched case shown in Figure 9. Agreement between calculated and measured is good except for the data at 85°C. As in the zero frequency case shown in Figure 9, performance at -55° is anomalous, except that the effect of the RF input matching network was to shift the peak value of γ from -8 dBm down to -22 dBm.

A more common diode detector measurement is output voltage vs. temperature at some fixed value of input power. Such data were obtained for the experimental circuit with P_{in} = -30 dBm, and are compared to a calculated curve in Figure 11.

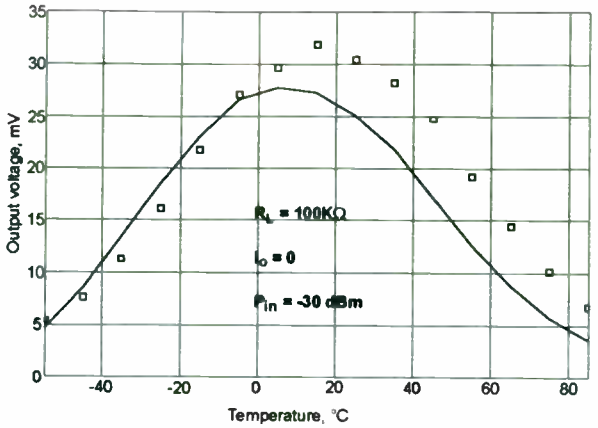

Figure 11: Output voltage vs. temperature, 2.45 GHz detector

As was the case in Figure 10, agreement between predicted performance and experimental data is good except at higher temperatures.

An examination of (2) and (6) will show that variation in I_s with temperature is larger and more significant than the variation in Λ. Not only does the temperature sensitivity of I_s directly affect γ as given in (6), but it results in wide swings in R_j, as was seen in Figure 7. This, in turn, can change the input impedance match and result in substantial impedance mismatch losses at temperature extremes. Calculated input match for the 2.45 GHz detector under discussion is given in Figure 12. Circles on the Smith Chart are impedances given at 10° increments.

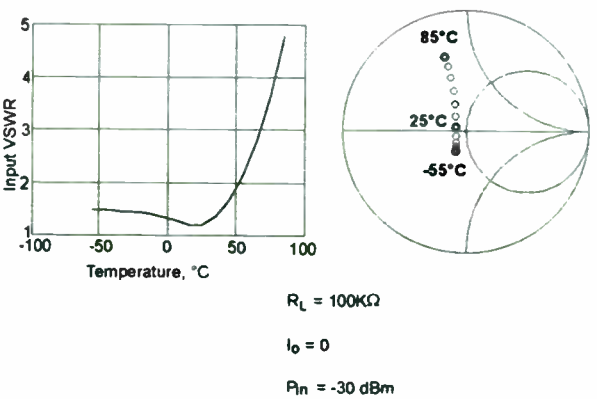

Figure 12: Calculated Z_{in} vs. temperature, 2.45 GHz detector

The design of the input impedance matching transformer was done at 25°C. From this figure, it can be seen that the input match is fairly good until temperature exceeds 50°, after which it

degrades quickly. Severe mismatch losses at the input to the detector are the result, lowering the power delivered to the diode's junction.

Because the impedance at high temperatures swings out from the origin of the Smith Chart so rapidly, a small error in modeling the impedance matching network can lead to errors in the prediction of high temperature sensitivity. This accounts for the difference between measured and predicted in Figure 11. However, a sensitivity analysis of the matching network is beyond the scope of this paper.

It can be seen that loss of video bandwidth and voltage sensitivity at cold temperatures is due to very low values of saturation current, leading to a drop in performance as predicted by (3) and (6). At high temperatures, RF impedance mismatch losses at the input to the detector lead to loss of sensitivity. These two different problems suggest two different solutions.

IV. COMPENSATION METHODS

Low temperature compensation:

Conventional DC biased detectors generally operate from a continuous current of 10 to 30μA, and offer greater temperature stability than the zero bias Schottky detector. However, these are devices with saturation currents in the nanoamp range. Nevertheless, the use of supplemental DC bias current suggests itself as a solution to poor video bandwidth and low sensitivity at low temperatures.

The 2.45 GHz detector described in Figures 10, 11 and 12 was tested with small amounts of supplemental DC bias, as shown in Figure 13.

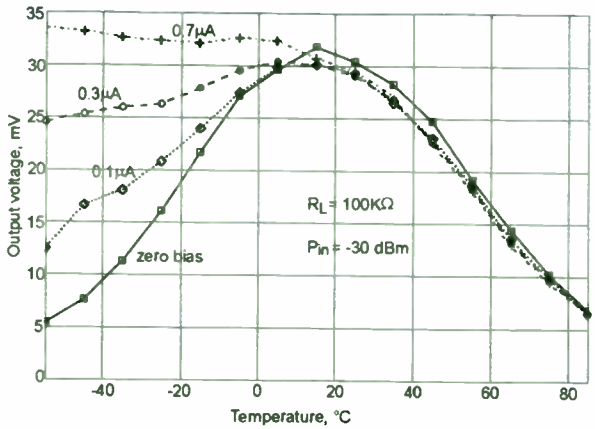

Figure 13: Measured V_o vs. temperature, 2.45 GHz detector

It can be seen that less than 1μA of current can compensate for loss of sensitivity at cold temperatures. An examination of Figure 13 suggests that 0.5μA of supplemental bias current would produce a flat output voltage from -55° to 15°C.

At temperatures above 20°C, these small amounts of external bias current have virtually no effect on output voltage.

An analysis was performed of the small signal transfer curve of this detector at -55°C as a function of external DC bias, as shown in Figure 14.

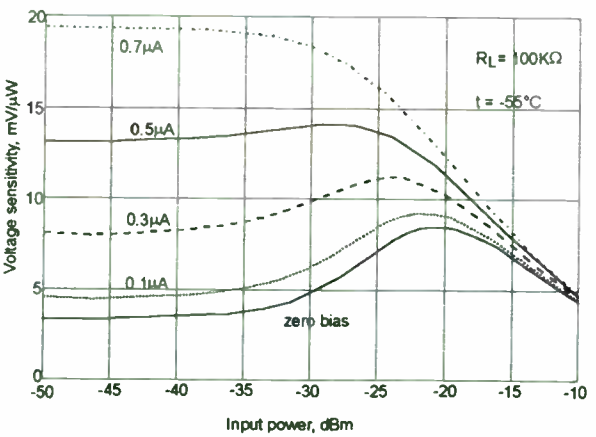

Figure 14: Calculated transfer curve, 2.45 GHz detector

It can be seen that a supplemental DC bias of 0.5μA dramatically brings up the voltage sensitivity in the small signal region, nearly eliminating the anomalous behavior observed at zero bias.

In addition, this small DC bias prevents junction resistance from exceeding 43KΩ at temperatures below -20°C, raising the 3 dB video bandwidth below this temperature to a minimum of 100 KHz (refer to Figure 8).

High temperature compensation:

As was seen in Figure 12 and from comparing Figures 9 and 10, RF impedance mismatch is the major cause for poor voltage sensitivity at 85°C.

To compensate for poor sensitivity at 85°C, the input matching network for the 2.45 GHz detector under discussion was redesigned. Calculated input parameters for this high temperature detector are shown in Figure 15.

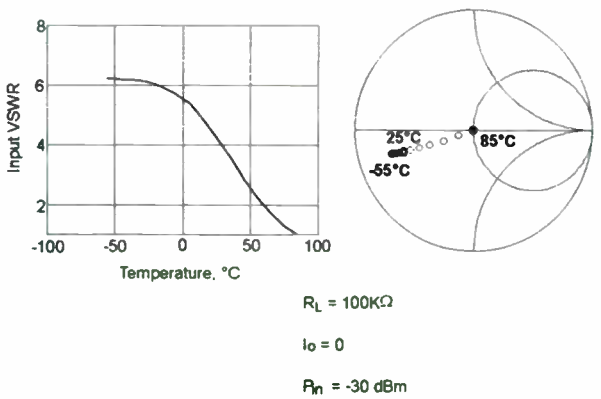

Figure 15: Calculated Z_{in} vs. temperature, redesigned 2.45 GHz detector

In this case, care was taken to provide a perfect match at 85°C, allowing the match at other temperatures to degrade. This approach contrasts sharply to the impedance behavior given in Figure 12. Output voltage vs. temperature was then calculated for this new design, as shown in Figure 16.

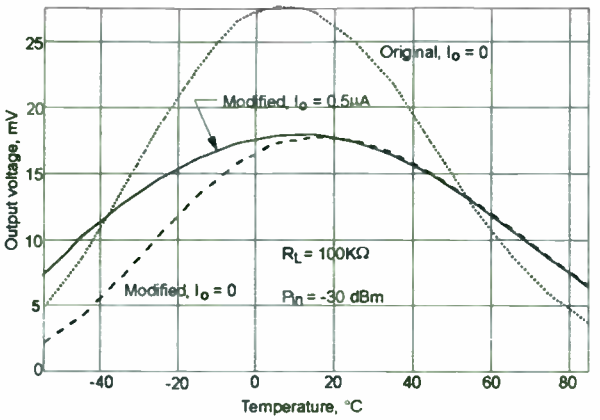

Figure 16: Output voltage vs. temperature, redesigned 2.45 GHz detector

Three plots are given in this figure. The first (dotted line) is the output voltage at zero bias for the original design (a copy of the data from Figure 11). The second (dashed line) is the zero bias output voltage for the redesigned matching network described in Figure 15. The third (solid line) is that same matching network, but with 0.5μA of supplemental bias added. It can be seen from comparing the dashed and dotted plots that changing the RF impedance transformer raised the output voltage at 85°C and reduced it at temperatures under 55°C. The tradeoff for this temperature compensation is lower output voltage at room temperature.

The addition of 0.5μA of supplemental bias had no practical effect on output voltage for temperatures over 20°C, but brought it up at -55°C. Because the RF impedance mismatch is so poor at -55° in this revised design, additional supplemental bias would be required to completely compensate output voltage at cold temperatures.

The ratio of output voltage at 25°C to that at 85°C went from 6.9 (dotted line, Figure 16) to 2.7 (solid line) because of the design change. That ratio can be further reduced, but at the expense of sensitivity at room temperature. Referring to Figure 15, this can be done by moving the impedance match at 85°C to the left along the real axis (towards the zero resistance point).

This approach to the temperature compensation of the Schottky diode detector works as well at any other RF frequency. The remaining discussion will focus on methods of controlling or limiting the supplemental bias current.

V. BIAS CONTROL

A simple way to obtain a supplemental bias current is with a DC voltage source and a resistor. This is similar to conventional DC biased detector diodes except with a lower bias current level, as shown in Figure 17.

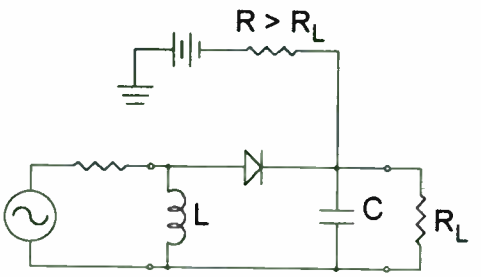

Figure 17: DC biased detector

If a 5 V battery is used in series with a 10 MΩ resistor, a bias current of 0.5μA will be supplied, increasing the output voltage at low temperatures as shown in Figure 16. In many tag designs with READ/WRITE capability, a 5 volt power source is readily available. The 10 MΩ resistor value does not load down the video circuit whose load resistor R_L is typically 1 KΩ - 100 KΩ. However, this current flow will be continuous and would shorten the battery (and tag) life. In addition, bias current has no practical effect at temperatures greater than 20°C. Thus, bias control that is temperature dependent is needed.

Thermistor with Positive Temperature Coefficient

By replacing the 10 MΩ resistor in Figure 17 with a thermistor that has a positive temperature coefficient (PTC), the supplemental bias current would decrease at higher temperatures where it is not needed (to save battery life) and increase at lower temperatures to improve performance.

The AIRPAX Series 5024 Thermistors have a PTC characteristic as depicted in Figure 18.

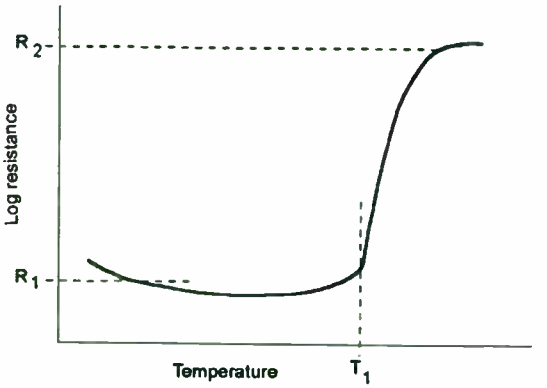

Figure 18: Typical PTC Thermistor

By specifying that R_1 = 10 MΩ, R_2 = 100 MΩ, and T_1 = 10°C, the 0.5μA of bias current would flow when T < 10°C , and only 50nA would flow when T > 10°C . Other values of R_1, R_2, and T_1 can be selected to achieve optimum tag performance at specific temperature ranges.

Power Supply with Thermostat

Using a thermistor, some current still flows even though it is not needed. Replacing the thermistor with a thermostat whose ON/OFF state is dependent on temperature, the bias current can be completely shut off so that no primary power is consumed at the higher temperatures (Figure 19). Note that the use of a low resistance thermostat requires the use of the 10MΩ resistor seen in Figure 17.

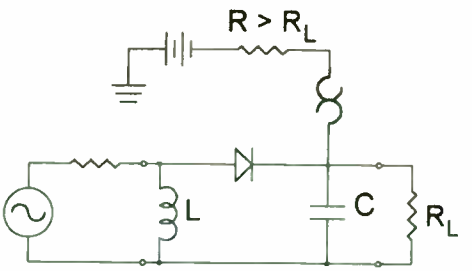

Figure 19: Detector with Thermostat

A snap action, bimetal disc switch such as the AIRPAX Series 5003 Thermostat can be used to turn the bias current on or off at different temperature set points. These switches are very reliable whose contact operation can be designed to close (open) when the temperature is decreasing (increasing) through a specified setpoint. This supplies the bias current only when needed so that no current is flowing at higher temperatures. Although these thermostats add cost to the circuit,

the user may find that the performance and maintenance benefits outweigh the these costs.

IC switches are also available that are temperature dependent. However, most require a supply voltage to operate and may have significant current levels even in the OFF position.

VI. CONCLUSION

The effects of temperature upon the performance of the zero bias Schottky diode detector have been analyzed and compared to experimental data. Two methods of compensation, for low and high temperature extremes, have been described..

VII. ACKNOWLEDGMENTS

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Noise and gain performance of PSA transistors based LNA vs. emitter number and operating conditions for personal communication systems

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Abstract

Properly down-scaled silicon bipolar transistors for high performance digital and microwave circuit applications have gained great benefits from the adoption of ion-implanted polysilicon emitter contacts.

In this work, the results of an extensive characterization activity carried out on several advanced double polysilicon bipolar transistors to the aim of deriving their effectiveness in low-noise amplifiers are presented.

Introduction

In portable communication systems operating over the low microwave range, devices and circuits must be designed to meet their best performance at very low current and voltage levels. The industry's trend is for developing advanced silicon bipolar processes to realize low cost components, size and performance competitive with solution using GaAs. Among the most advanced bipolar processes for the realization of high speed silicon transistors, double-polysilicon self-aligned (PSA) schemes have definitively emerged as the most effective technique.

In this work, we report noise and gain performance of low-noise amplifiers (LNAs) based on PSA transistors vs. emitter number and operating conditions, starting from an extensive characterization activity carried out on several advanced polysilicon bipolar transistors.

To the aim of exploring the features and performance of a commercially competitive PSA bipolar process, the manufacturer (CoRiMMe, an SGS-Thomson Research Centre, Italy) has supplied us with several devices characterised by different emitter configurations. We have characterised a total of 29 PSA transistors supporting 5 different chip topologies to gain a better insight on those effects related to emitter geometry which affect device operation. The features of the measured families (named Qi) are the following:

-Q2 4 emitters, 5 base contacts, 8 μm emitter length, with 4.6 μm pitch

-Q3 8 emitters, 9 base contacts, 8 μm emitter length, with 4.6 μm pitch

-Q4 16 emitters, 17 base contacts, 8 μm emitter length

-Q6 same of Q2, with 3.8 μm pitch

-Q7 same of Q3, with 3.8 μm pitch

The emitter finger pitch may be a critical parameter in improving the RF performance of BJT's since the transition frequency f_T can be increased by reducing its size.

We performed the characterization of the transistor series in terms of noise, gain, and scattering parameters by means of an automatic system whose measuring procedure has been developed in our Lab, over the 2-6 GHz frequency range at the bias conditions suggested by the manufacturer which consisted of the fixed low voltage of 2.8 V and two Ic current values proportional to the emitter finger number. Starting from an accurate model including noise sources, the behaviour of these transistors has been analysed from the point of view of the device suitability in CAD applications of low-noise amplifier. To accomplish that, the trade-off performance in terms of noise figure and operating power gain has been investigated as a function of emitter number and operating conditions.

Devices characterization and modeling

By means of an automatic system whose measuring procedure has been developed in our Lab, we performed measurements of the noise figure at the system output for either some properly selected values of Γ_S and, at each Γ_S value, for different values of the *receiver* noise figure realised by a high repeatability step

attenuator. From these noise data we derived both the noise and the gain parameter sets of the device by an accurate deembedding of the various stage contributions and by applying appropriate data processing techniques [2].
For all device series, we first performed a d.c. characterization and *screening* microwave measurements of the scattering parameters, the available gain G_a and the noise figure F_{50} in input matched conditions (i.e. @ Γ_S =0) as a function of bias voltage and current in the 1-4 GHz frequency range [3].
As a second step, the transistors were completely characterised in the 1-6 GHz range at the following bias conditions:
- Q_2 @ V_{CE} = 2.8 V, I_C = 2 and 8 mA;
- Q_3 @ V_{CE} = 2.8 V, I_C = 4 and 16 mA;
- Q_4 @ V_{CE} = 2.8 V, I_C = 16 and 64 mA;
- Q_6 same as Q_2;
- Q_7 same as Q_3;

Since all the measured data for each group exhibited reduced spread, a Q_i *typical* device (bold line in the reported diagrams) has been determined by simple statistic functions for representing each transistor series.
By deembedding the effects of the package (70-mil type) from the measured parameter values, we obtained scattering and noise parameter sets which refer directly to the chip device performance. The optimisation procedure was then applied to the chip model network to determine the circuit element values by minimizing the scattering parameter error functions.
The values of the equivalent noise sources were first derived on the basis of the noise theory for bipolar transistors, then optimized by fitting the noise parameters. The adopted noise model is represented by a couple of correlated noise current sources at the input and the output port of the transistor plus the thermal contribution arising from each of the physical resistors. The complete model structure is shown in Fig. 1; the element values, including noise generators, are reported in Tab.1.

Performance evaluation and results

Starting from the noisy models, fitted to the measured data, the noise and gain performance of the transistor families Q_i have been evaluated vs. bias current level and vs. emitter number (n_e) by means of a graphical tool developed in our lab and defined as trade-off chart [4].

Some interesting differences have been noted in the performance among the PSA transistor families Q_2, Q_3 and Q_4. No appreciate variations could be attributable to the different emitter finger pitch between Q_2 and Q_6, as well as between Q_3 and Q_7.
Reffering to Q_2, Q_3 and Q_4, some interesting remarks can be made:
- the minimum noise figure decreases with increasing bias current and markedly with increasing n_e
- the slope of the minimum noise figure vs. frequency increase proportionally with increasing n_e;
- the operating power gain decreases with increasing n_e and is less affected by the bias current level than the emitter number.

Besides, as a decreasing of the equivalent noise resistance with increasing the emitter number has been noted, a more stable behaviour is expected to.
The performance of noise figure and operating power gain vs. bias current level and vs. emitter number are reported in Figg. 2 and 3, respectively.

Suitable low-noise applications of PSA transistors are in the field of wireless communication systems in the low microwave range where the low-cost and high reliability characteristics of the silicon technology are preferred over GaAs.

Conclusions

We have here presented the results of an extensive characterization activity performed on several PSA bipolar transistors.
The devices were characterized by a different emitter finger number n_e and were tested over the 2-6 Ghz frequency range in terms of noise, gain and scattering parameters at different values proportionally n_e for each device series. Starting from a bias-dependent model including noise performance, a comparative analysis among the measured families has then carried out in terms of noise and gain performance vs. bias current level and emitter number.
Outstanding performance for this bipolar process suitable for low.power application up to 4-6 Ghz has been evidenced.

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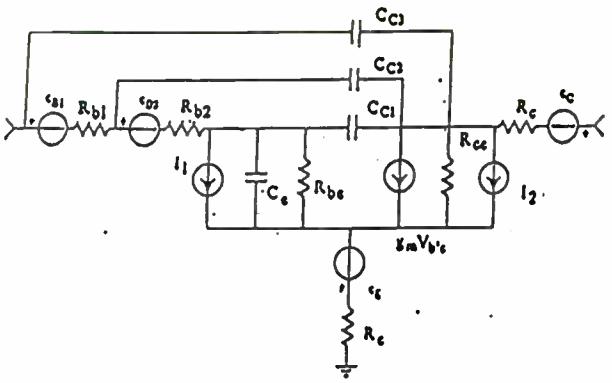

Fig.1. Equivalent circuit model including noise sources

	Q_1 A	Q_1 B	Q_1 A	Q_1 B	Q_1 A	Q_1 B
R_{b1} (Ω)	6	6	10	9	6	6
R_{b2} (Ω)	35	35	16	16	9	7
R_e (Ω)	3.3	3.3	1.8	1.8	0.8	0.5
R_c (Ω)	6	6	6	6	7	10
R_{ce} (Ω)	10000	10000	10000	10000	10000	10000
R_{be} (Ω)	1000	1000	1000	1000	1000	1000
C_e (pF)	0.5	0.4	1.6	3	6	20
C_{c1} (pF)	0.015	0.015	0.017	0.017	0.03	0.03
C_{c2} (pF)	0.09	0.1	0.13	0.13	0.3	0.36
C_{c3} (pF)	0.09	0.1	0.11	0.125	0.35	0.4
$\|I_1\|^2$ (pA²/Hz)	10	35	14	45	20	80
$\|I_2\|^2$ (pA²/Hz)	300	503	450	750	400	4000
$Re\{Y_{b'e}\}$	0.8	0.8	0.6	0.6	0.15	0.8
$Im\{I_1 I_2^*\}$	0.3	0.76	0.4	0.3	0.85	0.3
T_{LC} (K)	297	297	297	297	1100	1000

Tab.1. Model element values.

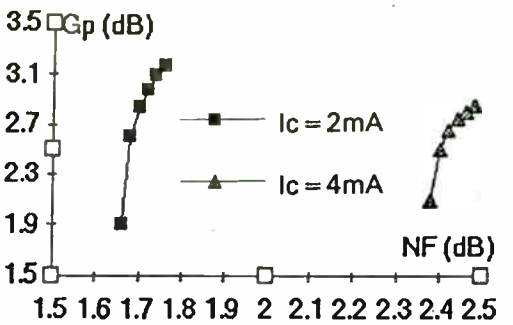

Fig.2. Performance of noise figure and operating power gain vs. bias current level of Q_2 typical device @ 6 GHz.

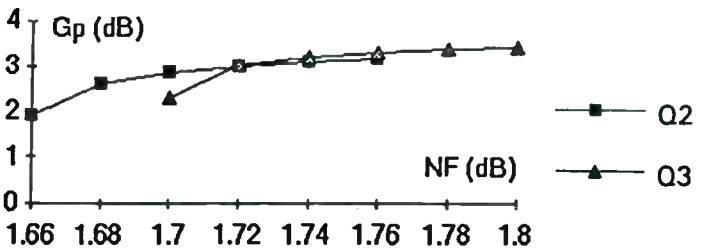

Fig.3. Performance of noise figure and operating power gain vs. emitter number of Q_2 and Q_3 typical devices @ 6 GHz.

RF power amplifiers for portable radio equipment built with discrete bipolar SMD transistors.

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I INTRODUCTION AND SUMMARY. In this article examples will be given for the realization of power amplifiers for handheld radio equipment with discrete SMD components. The radio systems could be either the analog or the digital systems operating at 900 and 1800 MHz. Other solutions are available these days in the form of hybrid modules and integrated circuits which both have their own advantages over the other. This article shows that low cost power amplifiers with excellent performance can be built with bipolar transistors in a plastic SMD package.

In the development department. of Philips semiconductors last year a new plastic SMD package has been developed for power RF transistors up to 4W of pulsed power. On the outside the package is a standard SO8. The high performance is achieved by the pin configuration and the use of an internal input matching. An application with this transistor has been built which realizes a complete power amplifier for class 4 GSM with special attention to the reproducibility.

Finally an overview of the available lineups will be given.

II RF POWER AMPLIFIER DESIGN

Today a lot of different solutions exist for power amplifiers which differ in the technology used. Examples of these are integrated solutions (often GaAs), hybrid modules (GaAs, MOS or Si-bipolar technology) and discrete components. One of these solutions can have specific advantages over the other. PA's built up with discrete transistors distinguish from the other solutions on:

- Complexity. built with a lot of components. The discrete PA design seems complicated.
- Amplifier performance. The overall performance depends on both component performance and the design (solution).
- PRICE. Discrete component solutions are cheaper than other solutions.
- Flexibility. Customer specific solutions are possible. The solutions can perfectly fit to what the customer needs
- Size, more board space needed than for the other solutions
- Height, often lower than other solutions.
- Performance, because different technologies can be mixed, discrete PA's can have excellent performances.

III RF POWER TRANSISTORS

Theory. Good RF power transistors are the basis for a good and efficient working power amplifier. RF power transistors are normally used in a non linear mode of operation, like class AB, B or C. The most important specifications for power transistors are gain and power added efficiency. These can only be achieved with a good transistor in combination with a good package. Figure 1 shows the most important transistor parameters, responsible for the RF performance. In practice for RF transistors operating under low

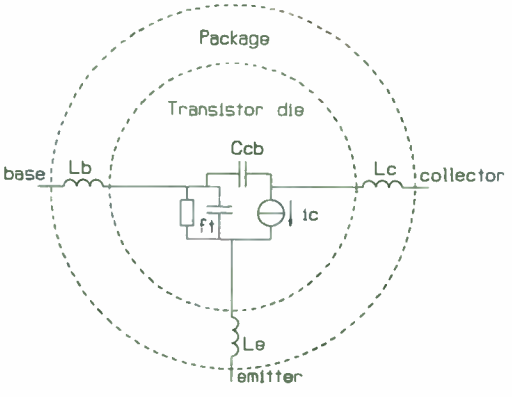


Fig.1 Important parameters for RF power transistor performance

voltage conditions, the f_T at low supply voltage, and emitter inductance *Le* are having the largest impact on transistor performance.

This is shown by an approximation for the gain of an RF transistor in common emitter configuration is given by the formula in figure 2.

$$Gain = \frac{|uce|}{\omega^2 \cdot Le} \cdot \left(\frac{1}{\frac{2 \cdot Pl}{\omega_T \cdot |uce|} + Ccb \cdot |ucb|} \right) + 1$$

Fig.2 Formula describing the gain of a RF power transistor in class AB.,

In this formula the symbols represent:

- uce: amplitude of the signal between the internal collector and emitter in Volt.
- ω: the angle velocity in rad/sec.
- Le: the total emitter inductance ($L_{package}+L_{via\ holes}$) in Henry.
- Ccb: the average of the feedback capacitance between collector and base in Farad.
- ucb: amplitude of the signal between collector and base in Volt.
- Pl: the power generated by the intrinsic transistor in Watt.
- ω_T: The angle velocity at which the current gain of the transistor reaches 1, in rad/sec.

In case of a low voltage transistor, operating in class AB and with low series resistance in base, emitter and collector the following estimation can be made:

- uce = Uce (DC voltage on the collector supply)
- Ccb = Ccb @ the nominal supply voltage
- ucb = Uce (DC voltage on the collector supply)
- ω_T = $\omega_T/2$ (measured in class A, @ the nominal supply voltage and average collector current).

A lot of transistor parameters are highly supply voltage and current dependent. Therefore transistors should be optimized for each supply voltage and output power.

Because the gain of a bipolar transistor is inverse proportional to the emitter inductance, effort has been spent to reduce this value in our new packages. One of these packages is the plastic SO8, in which 4 pins are used for emitter grounding. The shape of the pins and pin configuration is optimized for a good RF performance. Fig. 3 shows the inside of a 6V, 900 MHz transistor for GSM. In this transistor pre-matching is included to transform the input impedance. This makes the input impedance frequency dependent, so the transistor can be used for one specific frequency band only.

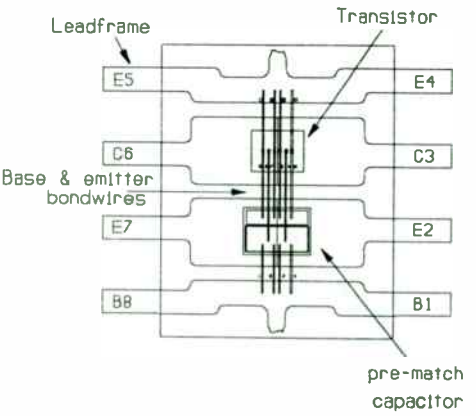


Fig.3 Internal configuration of a transistor in the plastic SO8 package.

An equivalent electrical diagram is shown in figure 4, which shows the internal transistor, pre-matching and the number of emitter pins and bondwires placed in parallel. With this package, in combination with our low voltage transistors, high gains (9 to 14 dB) at 900 & 1800 MHz can be achieved with at the same time very high *power added efficiencies* ranging from 60 to 68%. The input impedance is transformed to a level between 6Ω and 20Ω.

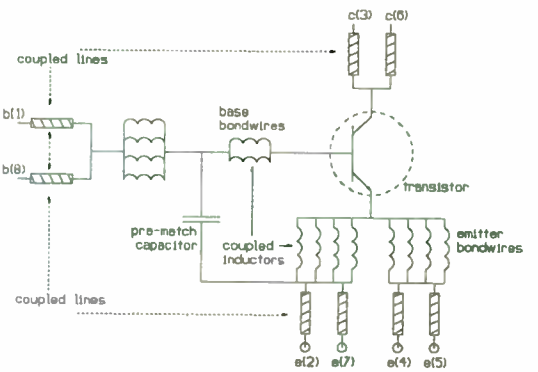


Fig.4 Equivalent electrical model of a transistor in the plastic SO8 package,

In fig 5. some measured gain and efficiency curves where given for a 900 MHz transistor, operating from a 5 cell supply (nominal. 6.0V). Fig. 6 gives an overview of the specifications for this transistor.

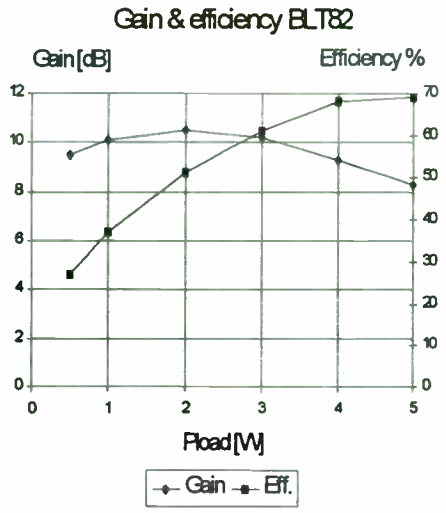


Fig.5 RF performance BLT82, 3.5 Watt transistor @ 6.0V, 900 MHz

Specification BLT82:

Gain	> 8dB (10dB typ.)
Efficiency	> 50% (65% typ.)
Supply voltage:	6.0V (8.6V max)
Frequency:	900 MHz
Input impedance	7+j4
input return loss	>14 dB
Rth	< 32 K/W
Bvceo	> 10 V
Bvcbo	> 20 V

Fig.6 Specifications RF power transistor for 900 MHz, 3.5W @ 6.0V

Spread of amplifier performance.

When making a design with discrete transistors, spread in performance due to parameter spread of the transistors and passive components is a critical issue. Data sheets normally give typical and minimum performance figures. (gain and efficiency). The input and load impedance are expressed in typical figures only. Most of these parameters depend on transistor parameters which are correlated with DC parameters. Gain and efficiency figures are guaranteed values, and will be within +/- 1dB resp. +/- 5% worst case. Fig 7 & 8 show the spread in performance on these parameters, measured on a large number of devices.

The optimum load impedance will depend most on the passive matching network, which can be optimized by the PA designer. The input impedance of the transistors depends on the transistor parameters like f_T and Ccb (feedback capacitance) and the internal pre-match, built up with bondwires and MOS capacitor. This configuration is very consistent as shown in fig. 9. This picture shows the input return loss measured in a fixed tuned circuit on a large number of samples. The guaranteed return loss at the input is better than 15 dB, with typ. values of 30 dB. These spread values should be taken into account in power amplifier design.

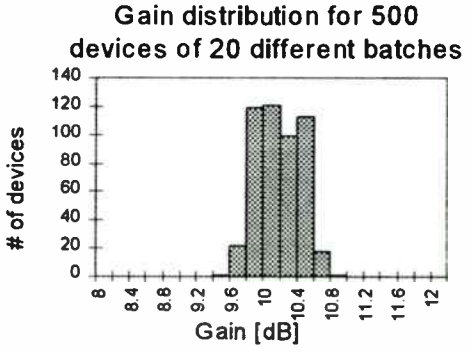


Fig.7 Gain distribution

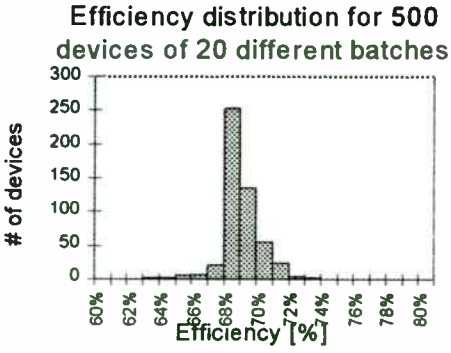


Fig.8 Efficiency distribution

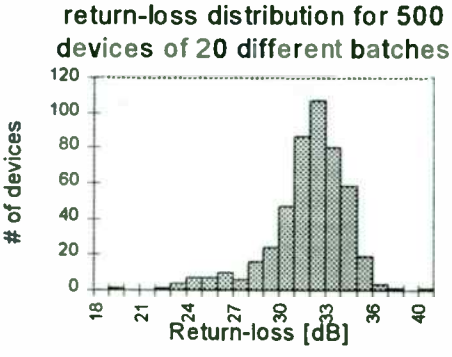


Fig.9 Return loss distribution

Thermal characteristics

In discrete transistor technology, the dissipated heat will be transported through the collector pins. Care should be taken in the PCB board design that the maximum junction temperature of the device and the maximum solder point temperature will not be exceeded. The sum of the thermal resistances of the transistor (Rth_{j-s}) and printed circuit board (Rth_{s-a}) in combination with the maximum ambient temperature must be taken into account when calculating the maximum junction temperature (175°C). In power amplifiers used for TDMA systems the maximum allowed dissipation is not critical because of the low average dissipation. For pulsed operation with short period times (<5ms) the peak junction temperature can be found by the following equation:

$$Tj\_peak = Zth_{package} * Pdiss_{peak} + Rth_{PCB} * Pdiss_{avg} + Tamb$$

Fig.10 Calculation of the peak junction temperature

Figure 11 will illustrate the junction temperature as function of the on and off switching.

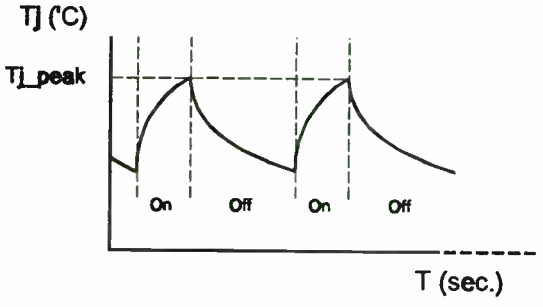


Fig.11 Junction temperature as function of time for pulsed operation.

In the formula (fig. 10)

Tj_peak	peak junction temperature
$Zth_{package}$	Thermal impedance from junction to collector solder point. This value can be found in the transistor data sheet and is a function of pulse time and duty cycle.
$Pdiss_{peak}$	Dissipated power during the "on" state of the transistor
Rth_{PCB}	Thermal resistance of the PCB from collector solder point to ambient
$Pdiss_{avg}$	The average dissipated power in the transistor (with duty cycle taken into account)
Tamb	Ambient temperature

Practical values for the $Zth_{package}$ are 7 K/W and for the Rth_{PCB} 60 K/W.

For CW operation the maximum dissipation in the plastic SO8 transistors can be a problem and is limited to 1.5 to 2.0W dependent on the application and your PCB design. When dissipation is critical the thermal resistance of the PCB can be decreased by the methods stated in fig.12. With these methods the thermal resistance of a 0.3 mm thick PCB can become as low as 40 K/W.

- Thermal conducting glue between transistor and PCB
- large (wide!) pads on the PCB for the collector
- Thick copper on top and bottom side of PCB (>60µm)
- alloyed PCB
- thin PCB material

Fig.12 Methods for decreasing the thermal resistance of a PCB.

IV MATCHING CIRCUITS

General

Matching circuits in power amplifiers are used for transforming the input impedance of a power transistor to the desired load impedance for the driver stage. For RF power transistors this optimum load impedance is not the conjugate of the output impedance, but an impedance dependent on loadpower and available voltage swing, cancelling package parasitics and output capacitance.

Good matching circuits perform the correct impedance transformations, with low losses over the complete frequency band. In a PCB design several components like capacitors & inductors (lumped element) and microstrip and stripline (distributed) are available. Because of cost, microstrips instead of SMD inductors are preferred.

When designing matching networks for a complete amplifier, most effort is usually spend on matching the final stage to the output (50Ω). Losses in the PA output matching have a big impact on the total PA performance as gain, maximum load power & efficiency will be affected. The matching network at the output of a PA can also be used to perform harmonic filtering.

Spread in matching networks

Fig. 13 shows a typical configuration with matching networks. In these matching networks, spread of component placement, line widths

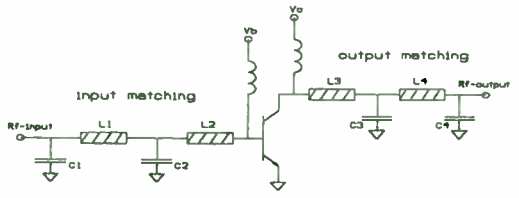


Fig.13 Typical matching network configuration

(PCB etching), material specifications (ε_r, height and tan δ) and values can take place. For networks, matching low impedances, in general it can be said that the length of microstrip(or stripline) inductors (L2 & L3) and capacitor values (C2 & C3) causes most of the spread of the total matching network. For a capacitor the spread in value can be translated to a spread in impedance. The parasitic series inductance of a capacitor can cause the relative error to explode. This will happen if you come close to series resonance.

Fig 14 shows the result of a Monte Carlo analysis

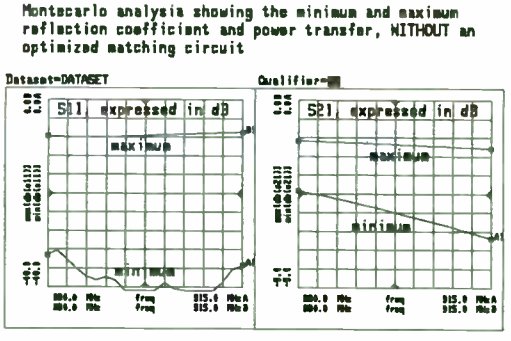


Fig.14 Spread in matching circuits caused by capacitor tolerance and component placement accuracy.

done on an input matching network, which matches 50Ω to 1Ω in 2 steps. C2 is simulated with a spread in component value of +/- 5%, for the length of L1 & L2 a spread of 0.5mm is taken into account.

From these figures it can be seen that the reflection coefficient at the input can vary between -40 dB and -8dB, which are not acceptable values. The losses of this matching network are between 1 and 3.5dB, which can be called high.

Improvement for reducing the spread

Improvement on this matching circuit to reduce the variations in input reflection coefficient and losses can be made by building large capacitor values (close to series resonance) up from 2 capacitors in parallel, and by a smart connection of the capacitors as shown in fig. 15 With this configuration spread can be reduced at lot.

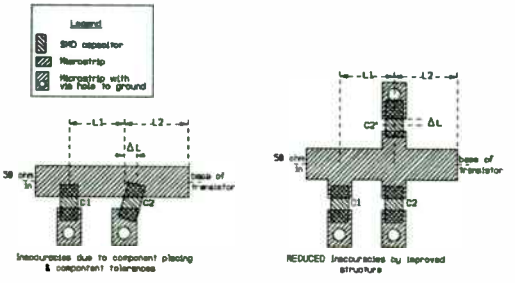


Fig.15 Methods for minimizing the sensitivity to spread

Figure 16 shows the result of a simulation for the improved matching network. Again the effect of +/-5% tolerance for the capacitor, and +/- 0.5mm placement accuracy for the capacitor is shown. The maximum reflection coefficient is under -20dB, which is an acceptable value. The losses are reduced to 1dB. This is a significant improvement over the previous solution.

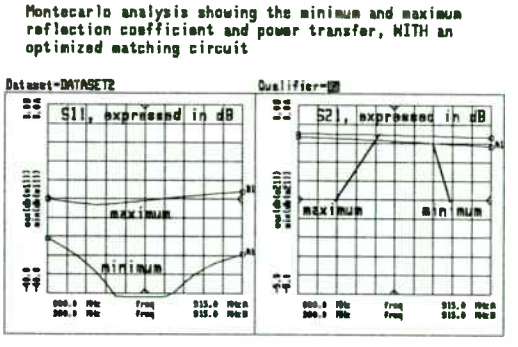


Fig.16 Spread in matching circuits caused by capacitor tolerance and component placement accuracy, improved version.

V Power control and standby switching

Most communication systems require a PA with a power control and a method to switch it off. When a PA is switched off it's current consumption should become less than 100µA. Because of efficiency reasons and power control over a large range it is preferred to bias bipolar RF transistors in class AB. A Class AB bias voltage should be temperature dependent voltage source with the same temperature coefficient as the RF transistor base-emitter knee voltage. (≈ -2mV/°C). This can be realized with a resistor (R1) and a diode for stabilization as shown on the left hand side of fig. 17. The current through the diode (Iref) should be about 2 times the maximum base current. The maximum base current depends on the loadpower, minimum efficiency and minimum Hfe

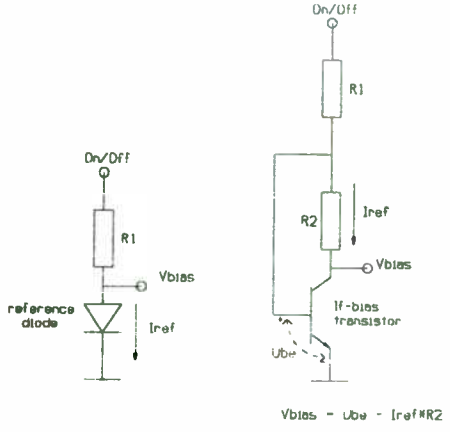


Fig.17 Realization of Class AB bias.

(DC current gain). The same can also be achieved with a transistor (picture on the right of fig. 17). This configuration gives you the freedom of realizing low bias voltages (<0.65V) with a temperature coefficient of -2mV/°C. The actual voltage can be chosen with resistor value R2.

The power control in a bipolar PA is performed with the first stage, of which the DC collector current is controlled. When the PA is switched off, the bases of all 3 transistors are biased at 0V, and the collector is connected directly to the supply voltage. This gives a very good isolation from input to output.

VI EXAMPLE OF A POWER AMPLIFIER FOR 900MHZ REALIZED WITH DISCRETE TRANSISTORS

The first transistor in our new SO8 package for RF was designed to operate as a final stage in a class 4 GSM power amplifier. It will be driven with a small RF power transistor with an excellent performance at 900 MHz. (>13 dB of gain). These 2 transistors in cascade have an overall gain of about 24 dB, which means that only 1 extra stage is needed to fulfill the total gain specification. A summary of the specification for the total amplifier is shown in fig. 18.

Class 4, GSM power amplifier.	
Frequency	880-915 MHz
Gain:	> 35.5 dB (40 dB typ.)
Output power	> 3.5W (4.0W typ.)
Efficiency	>45% (53 % typ.)
Nominal supply voltage:	6.0 (8.6V max.)
Input VSWR	<2:1
Noise	<-85 dBm, bandwidth=30 khz
Stability	<-60 dBc, VSWR≤6:1
Harmonics	<-40 dBc
Isolation	<-36 dBm

Fig.18 Specification for class 4 GSM power amplifier.

The main features of the amplifier are

- low cost
- 100% SMD components
- high performance
- operates from a single supply
- no tuning required.

The amplifier is based on a three stage lineup, which consists the input stage BFG540W/x, a driver stage BFG10W/x and the final stage BLT82, all bipolar transistors. The input and output are matched to 50Ω. The amplifier is built on a low cost printed circuit board and included bias circuitry for load power control and fast on/off switching.

The total PA contains the functions shown fig. 19. The attenuator at the input is used to keep the input VSWR below 2:1 when the power is controlled. The attenuation is 2dB.

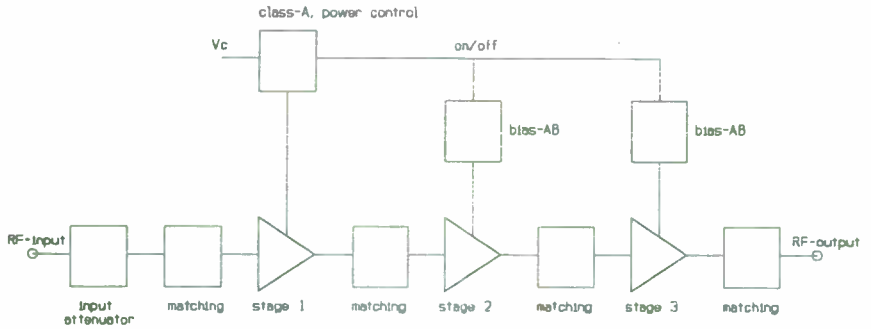


Fig.19 Functional block diagram power amplifier

The measured performance for each separate stage is:

Stage #	Transistor	Load power	Gain typ.	Eff. typ
1	BFG540W/x	65 mW	17 dB	20%
2	BFG10W/x	0.65 W	15 dB	60%
3	BLT82	3.5 W	10 dB	65 %

Optimum impedance values for the BLT82 were derived from impedance measurements. Impedance values for BFG10W/x and BFG540W/x were derived from large signal simulations with MDS (microwave design system from HP). The amplifier is built on standard FR4 PCB board, all matching circuits are low pass networks. The total schematic and circuit layout are shown in fig. 22 & 23.

Measured results:

In the next figures the performance is shown for this amplifier. In fig. 20 the harmonics and efficiency produced by this amplifier are shown as a function frequency. The output power of the amplifier is set to 3.5W (35.5 dBm). The specifications for harmonics (<-40dBc) are easily met, and the efficiency is over 50% for the complete frequency band. Efficiency vs. loadpower is shown in fig. 21 It shows the advantage of the class AB biased RF power transistors; the efficiency is over 40% for load powers ranging from 1.6W to 4W. Because mobile phones are often used at a power level lower than the maximum power level, this will result in a longer talktime.

All other specifications, mentioned earlier in this article are met with this amplifier.

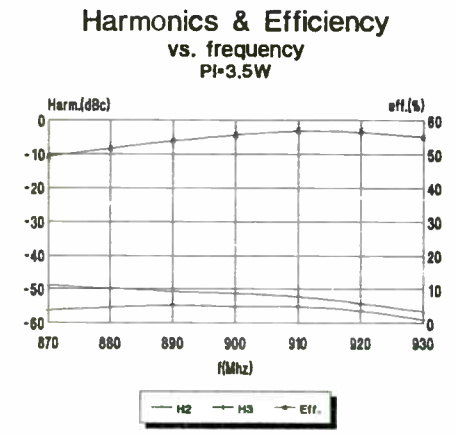


Fig.20 Efficiency of 900 MHz power amplifier.

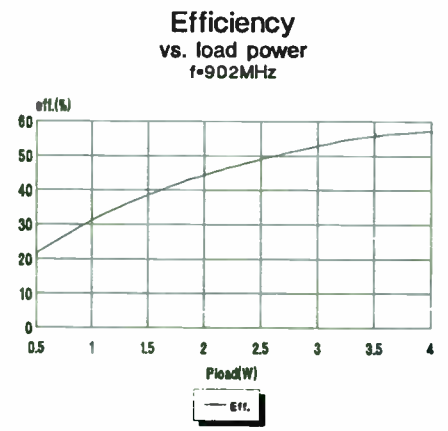


Fig.21 Efficiency vs. loadpower of 900 Mhz power amplifier.

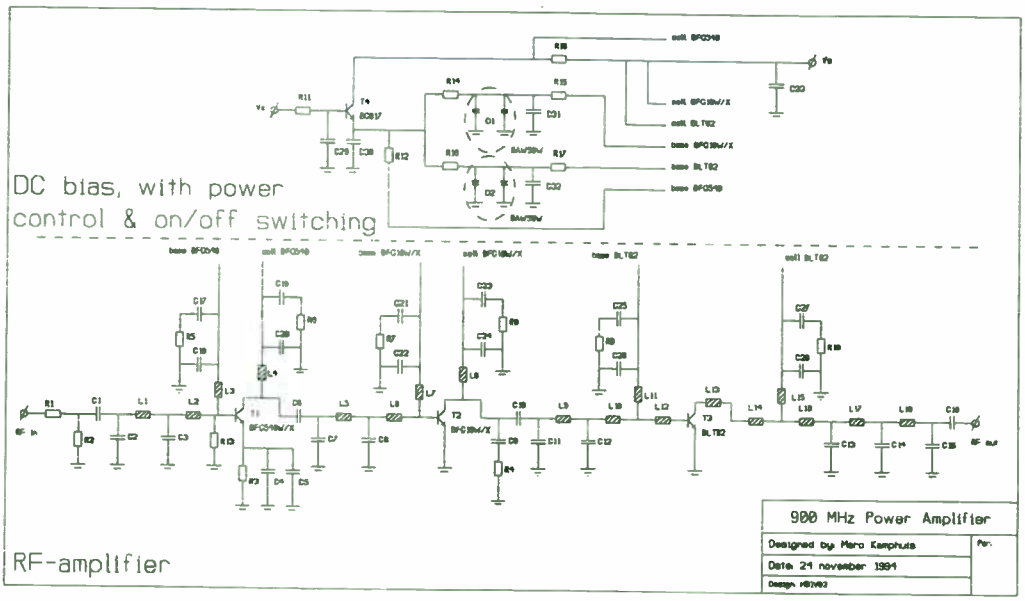


Fig.22 Schematic of 900 Mhz, 3.5W power amplifier

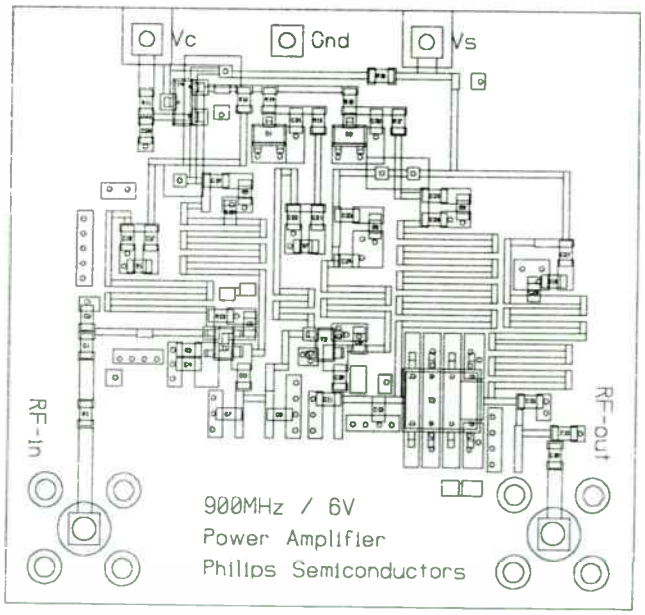


Fig.23 Layout of 900 Mhz, 3.5W power amplifier

NEW TRANSISTORS IN DEVELOPMENT

Based on previous described transistor in the plastic SO8 package, new types of transistors are in development. With these transistors a big part of the frequency band from 900 to 1.9 GHz will be covered, from supply voltages as low as 3.6 to 6V.

The table shows the possible lineup configurations, with suggestions for the different communication systems.

Characteristics			Transistor types (package)			
Communication system	Supply voltage	Frequency band	STAGE 1 (in SOT343)	STAGE 2 (in SOT343)	STAGE 3 (in SO8)	Overall Gain
AMPS/ETACS/NMT Pload = 1.2W	6.0V	825-905 MHz	n.a.	BFG10W/x	BLT81/8	28 dB
	4.8V		n.a.	BFG10W/x	BLT71/8	28 dB
	3.6V		n.a.	BFG10W/x	BLT61	26 dB
GSM Class 4, Pload=3.0/3.5W	6.0V	890-915 MHz	BFG540W/x	BFG10W/x	BLT82	40 dB
	4.8V		BFG540W/x	BFG10W/x	BLT72	40 dB
	3.6V		BFG540W/x	BFG10W/x	BLT62	37 dB
PCN/PCS Pload=1.6/2.0W	6.0V	1710-1900 MHz	BFG540W/x	BFG11W/x	BLT13	30 dB
	4.8V		BFG540W/x	BFG11W/x	BLT14	29 dB

Surface Mount PHEMTs Offer Low Noise Solutions in Direct Broadcast Satellite Service

Al Ward
Hewlett-Packard Communications Components Division
Richardson, Texas

The recent boom in the Direct Broadcast Satellite Service is putting price pressure on low noise blockconverter designs. Improvements in manufacturability as well as lower cost active components are needed. Pseudomorphic High Electron Mobility Transistors (PHEMTs) in miniature surface mount plastic packages provide a solution, offering 1 dB noise figures at 12 GHz to replace conventional MESFETs in relatively expensive ceramic packages.

This paper will cover the design techniques associated with using plastic-packaged surface mount PHEMTs. Both single stage and multistage 12 GHz broad band low noise amplifier circuits will be presented along with measured performance. The effects of out-of-band gain and cavity resonances will be examined. The importance of using a device with a low noise resistance to meet the broad bandwidth requirement of the 12 GHz satellite market will also be addressed.

INTRODUCTION

The Direct Broadcast Satellite service is growing at an enormous rate. Although it has just been recently introduced to the general market in the US, it has been in place in Europe and the Far East where cable TV has a lesser hold on the TV viewing market. For the reception of present analog and future Astra satellites in Europe, the Universal band from 10.7 to 12.75 GHz has been proposed. System noise figure is specified as less than 1.5 dB maximum between 10.7 and 11.7 GHz and less than 1.3 dB noise figure from 11.7 to 12.75 GHz. In the US, the Digital Satellite System, DSS, has been set up from 12.2 to 12.7 GHz. System noise figure requirement is 1.1 dB maximum.

System noise figure is set by the Low Noise Block Downconverter (LNB) that is placed at the feed of the parabolic reflector (dish). The LNB consists of a Low Noise Amplifier (LNA) followed by a converter that converts the Ku Band signals down to L Band for further signal processing. The LNA sets the LNB noise figure and usually consists of 3 stages of amplification.

The first stage of the LNA is the primary device that drives the noise figure and the second and third stages provide good gain at reasonable noise figure so as to not add appreciable noise to the first stage. Usually the second and third stage contributions are desired to be less than 0.2 dB. The requirements for the combined second and third stage are about 18 to 20 dB gain with a noise figure of 1.5 to 1.8 dB. The second and third stages should also be very low cost and surface mount compatible.

This paper describes the use of the Hewlett-Packard ATF-36163 in several low noise amplifiers suitable for the Direct Broadcast Satellite service at 12 GHz. The ATF-36163 device provides a nominal 1.2 dB noise figure and a minimum of 9 dB of associated gain at 12 GHz. The ATF-36163 is housed in a plastic surface mount SOT-363 (SC-70) package offering low noise performance in a low cost package. For most applications, the ATF-36163 is ideal for second and third stages of the LNA. However, for some applications, the noise figure may be adequate for the first stage.

The first two amplifiers are designed for use in the DSS service from 12.2 to 12.7 GHz. A single stage ATF-36163 amplifier

provides a typical 1.25 dB noise figure and 9 to 10 dB of associated gain over the 12.2 to 12.7 GHz frequency range. A 2 stage amplifier is described which has comparable noise figure and an associated gain of 18 to 20 dB gain from 12.2 to 12.7 GHz. The third amplifier has been optimized for the Universal 10.7 to 12.7 GHz band. As with any wide band width amplifier , a small amount of gain and noise figure must be sacrificed in order to obtain the broadband performance necessary for DBS applications. The addition of a low noise device such as the ATF-36077 as a first stage will decrease the overall noise figure to less than 0.8 dB over the band.

LNA Design

The LNAs were designed using EESOF's Touchstone for Windows and published S and Noise parameters.

The reference plane for both the S and Noise parameters is shown in Figure 1.

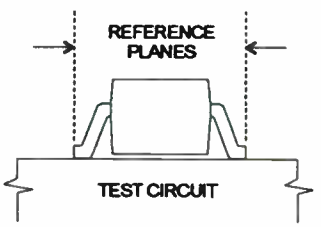


Figure 1. Reference plane for S and Noise Parameters.

Unlike the customary ceramic microwave type package, the plastic SC-70 package has its reference plane for both S and Noise parameters at the end of the device leads and not at the package to lead interface.

The ATF-36163 has 4 source leads, all of which, need to be grounded for proper RF performance. The S Parameters were measured in a test fixture designed specifically for the SOT-363 package. The effects of source grounding in the fixture have been de-embedded so that the designer can add circuit grounds including plated through holes and any associated source lead length. All LNAs are designed for 0.015 inch thick dielectric material with a dielectric constant of 2.5. The use of 0.015 inch thick material as opposed to 0.031 inch thick material minimizes radiation losses which can raise noise figure and create stability problems.

Single Stage 12.2 to 12.7 GHz Amplifier

Although the ATF-36163 is specified with the customary maximum noise figure and minimum gain specification at 12 GHz, the desired operation is from 12.2 to 12.7 GHz, slightly higher than where the device is tested. Close examination of the data sheet indicates a 0.8 dB drop in gain from 12 to 13 GHz. Therefore both the output and input matching networks presented to the device must be designed with greater emphasize on gain and bandwidth with noise figure secondary. Fortunately, the ATF-36163 has a fairly low noise resistance, Rn, which allows greater bandwidth to be achieved as compared to other devices.

A Smith Chart with Noise Figure and Available Gain Circles for the ATF-36163 at 12 GHz is shown in Figure 2.

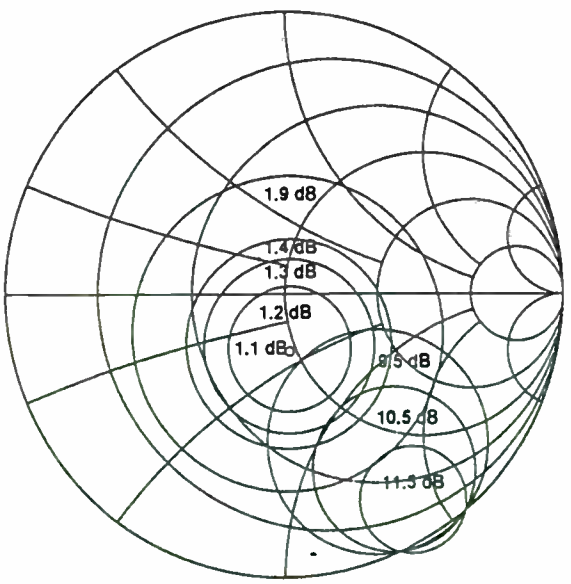


Figure 2. Smith Chart with Noise Figure and Available Gain Circles at 12 GHz, Vds=1.5V, Id=10 mA

An input match optimized only for noise figure would consist of a shunt capacitance at the gate of the device. However, the curves suggest a compromise input match that would

only sacrifice noise figure by 0.2 dB while simultaneously increasing gain by 1 dB. Adding a high impedance microstripline in series with the shunt capacitance will provide the optimum match. The output was conjugately matched to provide good gain over the same bandwidth. The resultant circuit board artwork is shown in Figure 3.

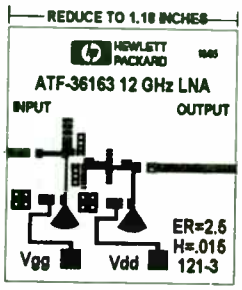


Figure 3. Artwork for 1 stage ATF-36163 LNA

Component placement is shown in Figure 4 and a schematic diagram is shown in Figure 5

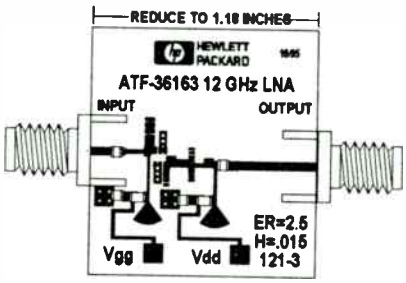
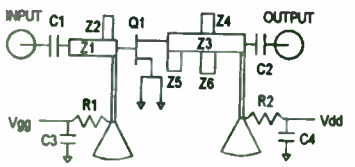


Figure 4 Component Layout for 1 stage ATF-36163 LNA



C1 -2.7 pF chip capacitor
C2 -1 pF chip capacitor
C3,C4 - 1000 pF chip capacitor
Q1 - Hewlett-Packard ATF-36163 PHEMT
R1, R2 - 50 ohm chip resistor
Z1,Z2 - Input Matching Network
Z3, Z4, Z5, Z6 - Output Matching Network

Figure 5 Schematic Diagram of 1 stage ATF-36163 amplifier.

The input matching network consists of a 2.7 pF blocking capacitor along with a series transmission line Z1 and a shunt capacitor in the form of an open circuit stub at Z2. Increasing the impedance of Z1 or using a capacitor at C1 with greater parasitic inductance will tend to increase gain and sacrifice noise figure. The output circuitry consisting of transmission lines Z3 through Z6 has been optimized to enhance gain in the 12.2 to 12.7 GHz frequency range. The output blocking capacitor is 1 pF.

50 Ω chip resistors bypassed to ground with 1000 pF bypass capacitors are used to provide a VHF termination for the device. They are located at the junction of the radial stubs and the high impedance transmission lines attached to the input and output RF matching networks.

The graph in Figure 6 shows gain versus frequency and bias point of the completed amplifier. At the data sheet bias point of Vds of 1.5 volts and Id of 10 mA, the gain is typically 9 dB in mid band. Increasing the bias to a Vds of 2 volts and Id of 15 mA increases the midband gain to 10 dB. Noise figure varies from 1.25 to 1.3 dB over the band and is actually about 0.05 dB lower at the higher bias point.

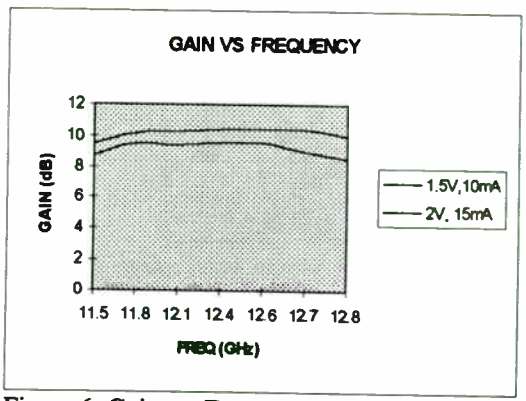


Figure 6. Gain vs. Frequency of 1 stage LNA

The losses of the input and output matching networks were then measured so that the performance of the device by itself could be compared to the specifications on the data sheet. The loss of the output matching network was measured at a nominal 0.6 dB at 12 GHz increasing to 0.7 dB at 12.7 GHz. Based on this measurement, the input matching network will have approximately 0.2 dB of loss at 12 GHz. Subtracting the 0.2 dB loss due to the input matching network projects a device noise figure of about 1.1 dB maximum at 12 GHz. Adding both the 0.2 dB loss for the input network and

0.6 dB of loss for the output matching suggests a device gain of about 9.6 dB at 12 GHz.

2 STAGE 12.2 to 12.7 GHz AMPLIFIER

A 2 stage amplifier using a pair of the ATF-36163 devices is described in this section. The 2 stage amplifier provides a high performance yet low cost solution for the last 2 stages of a typical 3 stage sub 1 dB noise figure LNA. The artwork and component layout for a 2 stage ATF-36163 amplifier is shown in Figures 7 and 8.

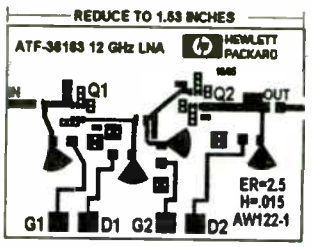


Figure 7. Artwork for 2 stage ATF-36163 LNA

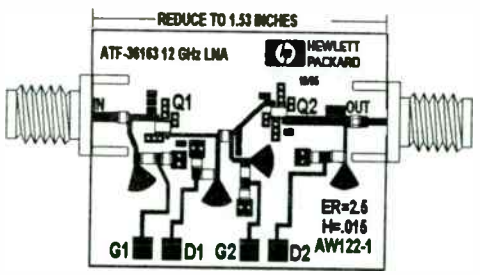


Figure 8. Component Layout for 2 stage ATF-36163 LNA

A schematic diagram is shown in Figure 9. The input matching network consisting of Z1 and Z2 plus C1 provide a compromise noise figure / gain match to Q1. The interstage matching network consisting of Z3 through Z6 and C2 provides gain equalization in the 12.2 to 12.7 GHz frequency range while Z7, Z8, and C3 provide an output match to 50 Ω.

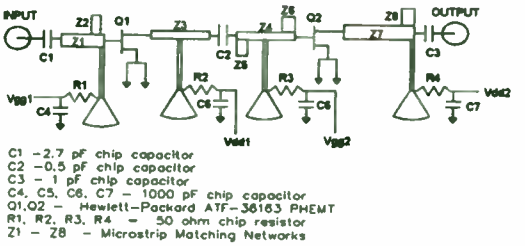


Figure 9. Schematic Diagram for 2 stage ATF-36163 LNA

The graph in Figure 10 shows swept gain of the completed 2 stage LNA. The plots suggest that an additional 1 to 1.5 dB of gain can be achieved by using the higher bias point described in the preceding section on the single stage LNA. Noise figure was measured at 1.23 to 1.28 dB from 12.2 to 12.7 GHz.

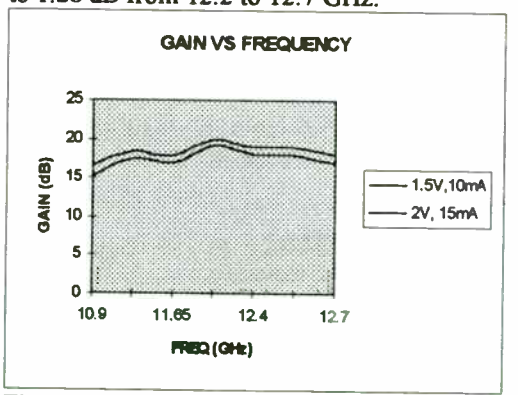


Figure 10. Gain vs. Frequency of 2 stage ATF-36163 LNA

Single Stage 10.7 to 12.7 GHz Amplifier

A single stage amplifier is described using the ATF-36163 which has been optimized for maximum gain from 10.7 to 12.7 GHz. The resultant noise figure varies from 1.1 dB at 10.7 GHz rising to 1.8 dB at 12.7 GHz. Bias condition is 2 volts at a drain current of 15 mA. Noise figure at 12.7 GHz was sacrificed in order to get additional gain at 12.7 GHz. With a first stage device with a 0.7 dB noise figure and 12 dB gain, the overall LNA noise figure has only degraded 0.1 dB at 12.7 GHz due to the 2 stage noise figure of 1.8 dB. For most applications where the ATF-36163 will be used as a second or third stage, gain is of primary importance.

The broad band LNA input matching network uses a single open circuited stub placed at the gate of the device. The output series transmission line has been widened based on bench tests to enhance gain in the 10.7 to 12.7 GHz frequency range. The artwork shown in Figure 3 was modified to provide best broad band performance. The resultant circuit board artwork is shown in Figure 11.

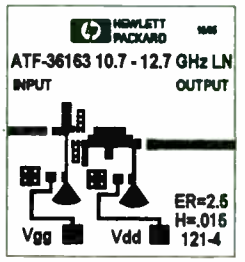


Figure 11. Artwork for 1 stage ATF-36163 10.7 to 12.7 GHz LNA.

Component placement for the broadband amplifier is similar to that shown in Figure 4.

The graph in Figure 12 shows gain versus frequency of the completed amplifier. The amplifier is biased at a Vds of 2 volts and Id of 15 mA for optimum gain performance. The amplifier exhibits between 10.5 and 12 dB gain over the entire 10.7 to 12.7 GHz frequency range. Noise figure varies from 1.1 to 1.8 dB over the band as shown in Figure 13.

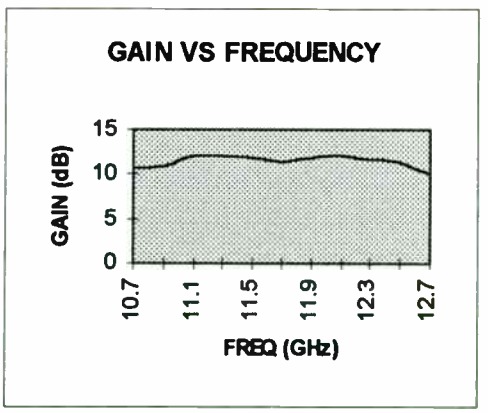


Figure 12. Gain vs. Frequency of 1 stage 10.7 to 12.7 GHz LNA.

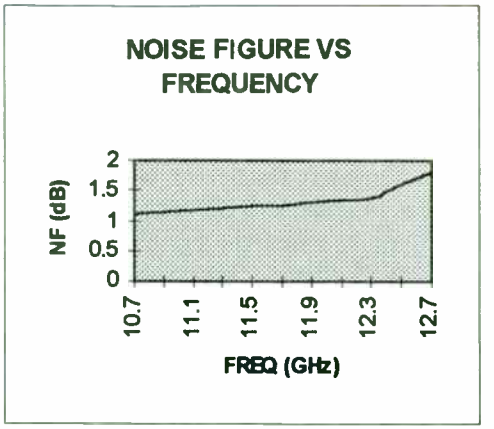


Figure 13. Noise Figure vs Frequency for 1 stage LNA

General Design Considerations

SOT-363 PCB Layout

A PCB pad layout for the miniature SOT-363 (SC-70) package is shown in Figure 14. Dimensions are in inches. The layout is shown with a nominal SOT-363 package footprint superimposed on the PCB pads.

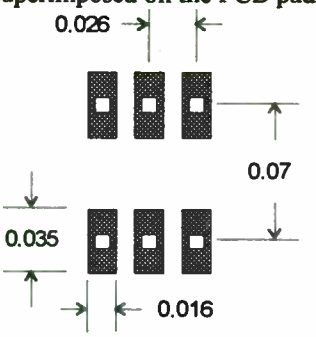


Figure 14. PCB Pad Layout (dimensions in inches)

It is important to properly model the PCB pad layout when doing the design to get best correlation between simulation and actual performance. The pads add shunt capacitance at the drain and gate leads of the device. It is also best to add plated through holes as close as possible to the 4 source lead pads. Excessive source lead length, i.e.. 0.050" can cause gain peaking in the 13 GHz range which can ultimately produce instabilities.

Biasing

For best performance, the ATF-36163 should be operated with the source leads dc grounded. This requires a negative voltage on the gate to "bias-up" the device. Nominal gate voltage is a (negative) -0.20 volts for 10 mA drain current and somewhat less negative for a drain current of 15 mA. Typical operation for best gain performance would be at a Vds of 2.0 volts and an Id of 15 mA. With a 50 Ω resistor in the drain bias decoupling network, a supply voltage of 2.75 volts will be required.

Enclosures

The LNA is usually installed in some sort of conductive or RF "reflective" enclosure or housing. The housing has various effects on the overall performance. The addition of walls and a cover can actually reduce radiation losses with the "good" result of lowering noise figure by 0.1 dB and raising gain by a dB or so. Now for the "bad" effect. Depending on the height and width of the enclosure, as viewed from the end of the LNA, a waveguide effect can occur. Depending on the width of the cavity versus operating frequency and the ability of any component on the circuit board to launch a wave into the "waveguide", various other undesired phenomena can occur. The most obvious is instability resulting in oscillations. The ability of the LNA plus enclosure to oscillate is generally determined by the frequency where maximum gain occurs and this may even occur at a frequency lower than the desired operating frequency. A good idea is to measure the swept gain of the LNA just to make sure that there is no excessive gain peaking out-of-band which could potentially cause trouble. The use of the lowest possible value blocking capacitors helps provide a highpass response to roll-off low frequency gain. Adjusting the impedance of the inductors used for bias decoupling can also be another means of providing a more highpass gain response.

Off Isolation

The dual polarity Universal LNB requires 2 LNAs, each driven separately from the feedhorn. This allows the viewer to receive 2 channels on the same frequency and to pick the program desired by turning on the appropriate LNA. This requires a certain amount of isolation by the LNA that is non-energized. The ATF-36163 LNA was tested for "off" isolation by leaving the normal gate voltage intact and removing the drain voltage. This condition produced a loss of about 12 dB in band resulting in an "on to off" isolation of between 20 and 22 dB.

Conclusion

PHEMT devices packaged in state-of-the-art low cost surface mount packaging can still provide near 1 dB noise figure and 9 to 10 dB gain at 12 GHz. The devices provide excellent performance for use in second and third stages of LNAs and depending on the application , the device could be used as a first stage.

Testing Multi-Branch Diversity Receivers

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Abstract

Developers of wireless systems are continually challenged to find new ways to increase system capacity and improve performance. One method to achieve these goals is to utilize the diversity combining capabilities of wireless communications receivers.

Spatial diversity is one popular technique that utilizes multiple antennas to capture transmission paths subject to different fading statistics. Various combining techniques use these semi-correlated received branches to optimize signal recovery. Telecom Analysis Systems (TAS) has developed a testing method that provides precise control of the fading correlation between transmission branches to facilitate the evaluation of diversity systems.

DESIGN CONCEPTS FOR CELLULAR, PORTABLE, AND CORDLESS APPLICATIONS

Design Concepts for Cellular, Portable, and Cordless Applications

Session Chairperson: Mark Reinhard,
Motorola, Inc. (Schaumburg, IL)

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Offset-Reference PLLs for Fine Resolution or Fast Hopping. **Morris Smith,** Motorola, Inc., MOS Digital-Analog IC Division (Austin, TX) 208

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Dual-Conversion FM Narrowband Receiver for Cellular and Cordless Phones Uses Low-Cost Monolithic IC Chip Set. **Harry J. Swanson,** Motorola, Inc., Analog IC Division (Tempe, AZ) 224

An Integrated Low-Cost, High-Efficiency Power Amplifier for Analog Cellular Applications. **Mark Williams** and **Jeff Ortiz,** Motorola, Inc., Semiconductor Products Sector (Tempe, AZ) 237

Power-Control Considerations for Personal Wireless Systems. **Mike Miceli,** Motorola, Inc., Wireless Market Development Group (Schaumburg, IL) 241

Wireless Systems Improvements Through Innovation and Integration. **Yves LeGrand,** Motorola, Inc., Analog IC Division (Tempe, AZ) 248

An Analog Single-Chip Receiver IC for the 46/49-MHz, 25-Channel Cordless Phone and Application in the 902-to-928-MHz ISM Band, **Ten-Voon Wong,** Motorola, Inc., System Engineering Segment Marketing (Singapore) 254

Dual 1.1 GHz PLL Frequency Synthesizer

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Austin, TX 78721

Motorola recently completed another phase of PLL frequency synthesizer development with volume production being achieved on the MC145220. This dual PLL supports two loops simultaneously using a common reference which feeds two independent reference counters. Packages available are the EIAJ 20-pin surface-mount package with 50-mil lead pitch and TSSOP (thin shrunk small-outline package) with 0.65 mm pitch.

The only additions needed to build two frequency sources are external low-pass filters and VCOs. The chip may be used in applications requiring two UHF loops, such as a 900 MHz cordless phones. Also, the PLL is useful in applications such as cellular phones which may need an 800 MHz loop and a 90 MHz offset loop.

Powerful Features

The MC145220 contains two on-board programmable counters covering a range of 40 to 1100 MHz. Input sensitivity is -16 dBm from 700 to 1100 MHz over a temperature range of -40 to 85° C.

A minimum operating voltage of 2.7 V, an operating current of 6 mA nominal per loop, and two standby modes make this PLL attractive for portable applications. Two phase/frequency detectors are included for each loop; one has a current source/sink output and the second has a double-ended output.

High-Speed Counters

The on-board main counters allow the user to achieve lower loop counter divide ratios than most competitive devices. These counters have independent prescalers with divide ratios of 32/33 and 64/65. The programmable division ratios cover 992 to 262,143. For example, with the minimum divide ratio of 992, the reference frequency at the detector input could be as high as 50 kHz with an input range of 49.6 MHz or higher and as high as 300 kHz with an input of 297.6 MHz or higher. This would be with continuous band coverage, with no gaps. (1 MHz is the maximum operating frequency of the phase/frequency detectors.)

Low Operating Current

Supply current is determined by three modes which are controllable via a serial port. With both loops operating, the supply current is nominally 12 mA. With one loop operating and the other on standby, the current drops to 6.5 mA. Both loops on standby drops the current to a few microamps.

Phase Detectors

The device has two types of phase detectors (actually, phase/frequency detectors).

One detector has a single-ended output which is a current source/sink/float. This detector has

programmable gain. Four levels are available: 100% of available output current (1 mA at 3 V), 80%, 50%, and 5%. An open-drain general-purpose output is available for filter switching, if needed. The "current-source" detector output's working voltage range is to within 0.5 V of either supply rail and it is usually used with an external passive low-pass filter.

The other detector has a double-ended output which is tied to an external combiner and loop filter. This circuit usually includes an op amp.

The unused detector may be shut down via the serial port, thus reducing interference and power line spikes. Also, this allows sharing of one pin by both detectors. Both detectors have a linear transfer function (no dead zone).

More Attributes

The reference counters are programmable for divide ratios of 10, 11, 12, and so on - up to 8,191. In addition, when "1" is programmed for the ratio, direct access to the reference input of the phase detectors is allowed. Direct access is useful for some modulation schemes. The reference counters are independently programmable which allows different step sizes for each loop.

The synchronous serial port, which is SPI compatible, may be operated up to 2 megabits per second. Random access of the five registers is accomplished with a single steering bit due to the patented register logic. A one-byte transfer accesses the C registers which select which detector is used, the polarity of the phase/frequency detectors, engages the standby modes, and controls the gain of the current-source phase detectors. A two-byte transfer accesses the R register which determines the reference counter divide ratio and oscillator/reference circuit. A three-byte transfer accesses the A registers which determine the loop (or VCO frequency) divide value. Ratios up to 262,143 are achievable.

A lock detect signal is provided for each loop. The two outputs are open-drain which facilitates wire-ORing the two signals.

Other attributes of the part include an ability to be cascaded using the Output A pin (configured as Data Out). When cascaded, several devices may be controlled with only three pins from a micro controller. A capability of monitoring the outputs of the A, N, and R counters is another feature. An auxiliary reference divider may be used to divide the reference by 16, 8, 4, 2, or 1. The output of the counter is fed to the REFout pin.

Closed-Loop Performance

A loop was built using a VCO running around 740 MHz. With 100 kHz step size, reference spur suppression of 90 dB was achieved. Lock time was 2 ms.

Obtain More Information

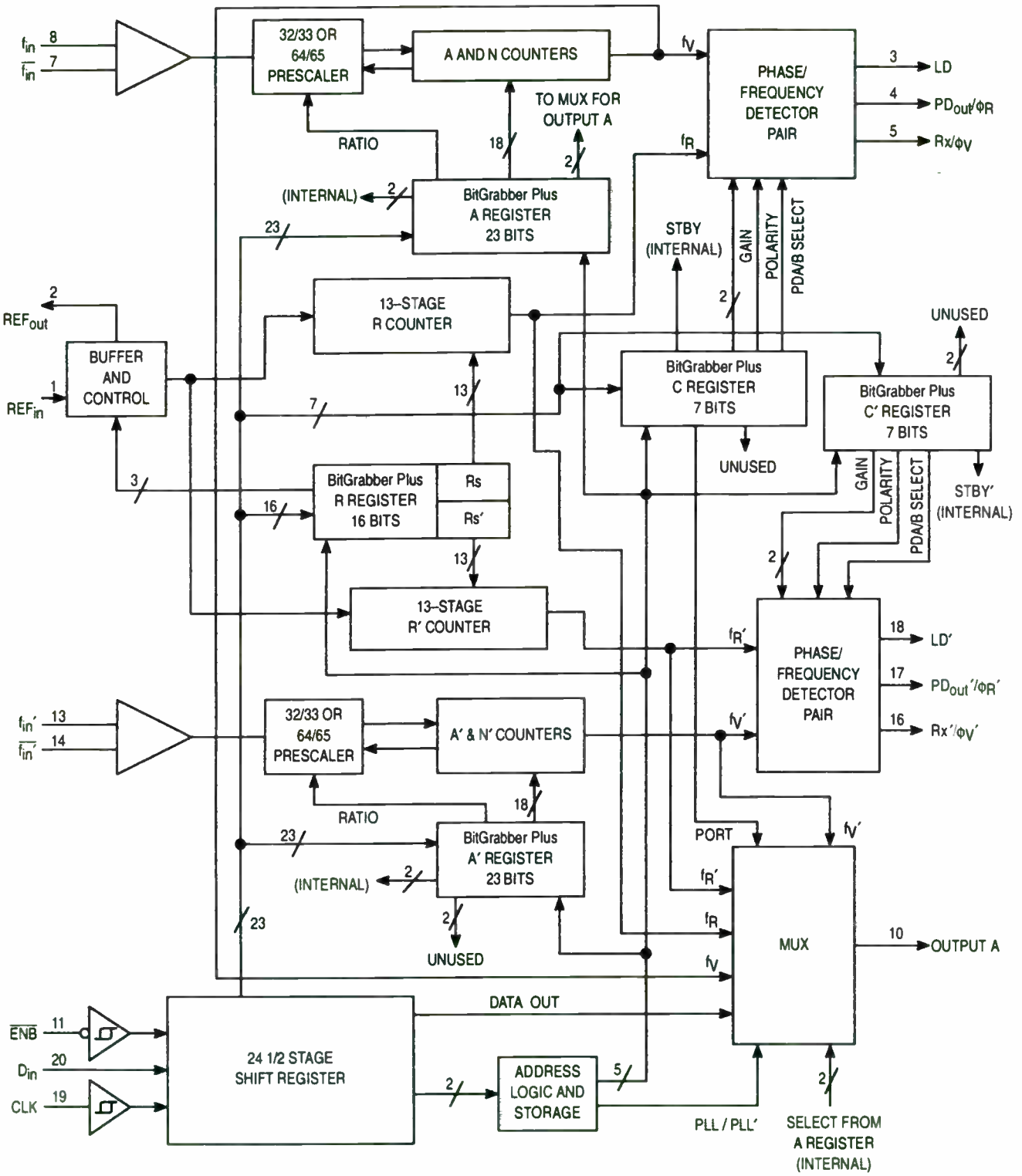
For additional information on this product, call the Motorola fax service at 602-244-6609. Request sheet number MC145220.

The paper in this publication by Morris Smith titled "Offset Reference PLL's for Fine Resolution or Fast Hopping" has information on multi-loop synthesizer applications. The MC145220 is mentioned in the paper.

References

MC145220 Data Sheet, Motorola, 1995

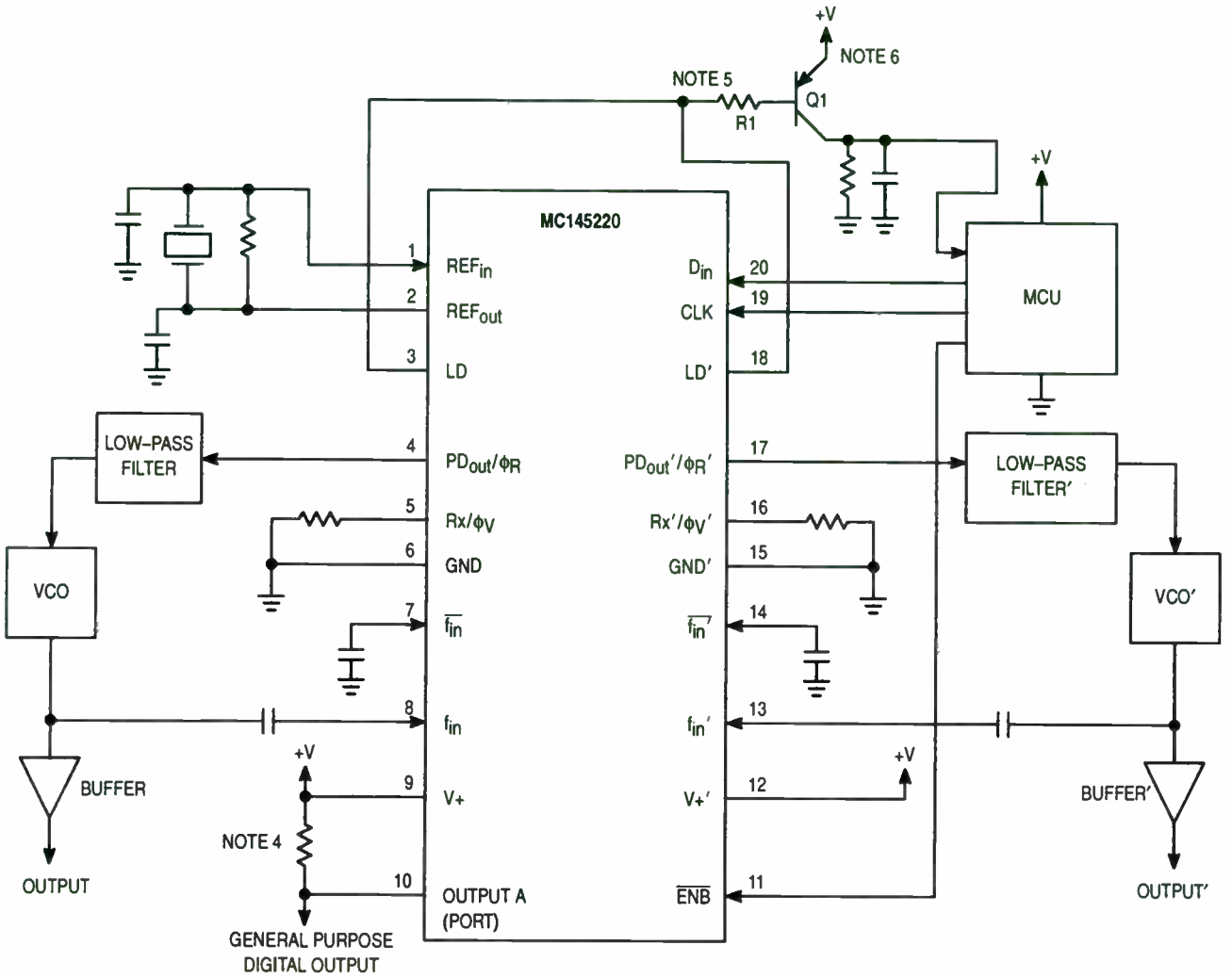
MC145220 Block Diagram



PIN 9 = V+ (Positive Power to the main PLL, Reference Circuit, and a portion of the Serial Port)
PIN 6 = GND (Ground to the main PLL, Reference Circuit, and a portion of the Serial Port)
PIN 12 = V+′ (Positive Power to PLL′ and a portion of the Serial Port)
PIN 15 = GND′ (Ground to PLL′ and a portion of the Serial Port)

BitGrabber is a trademark of Motorola Inc.

Application Showing Use of the Two Single–Ended Phase/Frequency Detectors



NOTES:

1. The PD_{out} output is fed to an external loop filter.
2. For optimum performance, bypass the V+ and V+′ pins to GND and GND′ with low–inductance capacitors.
3. The R counter is programmed for a divide value = REF_{in} /f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \cdot P + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively. P is the lower divide ratio of the dual–modulus prescaler (i.e., 32 or 64).
4. Pull–up voltage must be at the same potential as the V+ pin or less. Pull–up device other than a resistor may be used. (Pull–up device not required when Output A is configured as f_R, f_R', f_V, f_V' DATA OUT.)
5. LD and LD′ are open–drain outputs. This allows the wired–OR configuration shown. Note that R1 and Q1 form the "pull–up device".
6. Use of Q1 is optional and depends on loading.

Offset Reference PLL's for Fine Resolution or Fast Hopping

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Introduction

Frequency Synthesis by use of two loops, with reference frequencies offset from each other, can provide much finer resolution or faster hopping than a single loop. Dual PLL IC's are available to make compact low current synthesizers using the technique.

Alternative techniques will be discussed, the design method described and examples provided. This technique has been used successfully with the Motorola MC145220 dual PLL providing 10 Hz step size, 30 MHz frequency range and switching time of 30 mS.

Alternative Techniques

Direct Digital Synthesis

DDS composes a Sine wave from discrete digitized samples. Sometimes they are called Numerically Controlled Oscillators (NCO's). Samples for one complete Sine wave are stored in read only memory (ROM). A clock outputs a sample every period. At some frequency every Sine wave sample will be used. At a higher frequency every second or third sample might be used. Digital to analog conversion produces analog levels corresponding to sample codes. The output is low pass filtered. Below 1 Hz resolution and micro-second switching are the advantages of DDS.

Spurious signal levels and high current are the weaknesses. Currently available Digital to Analog converters have spurious levels greater than -76 dB in the VHF and higher frequency range. Sometimes manufacturers of DDS devices that don't include a D/A converter will give specs that are computed assuming the D/A is perfect. Spurious of -96 dB could be quoted under these conditions. Spurious signal levels make DDS unsuitable for most receiver and many transmitter applications. Current consumption is greater than 100 mA.

Fractional N

It is possible to have PLL output increments smaller than the step size by use of a fractional N divider in the feedback loop. Available Fractional N IC's cannot achieve 1000 times ratio of loop step size to output increment. The offset reference technique can do it. Fractional N synthesis produces spurious signals at the increment offset from the carrier. Offset reference does not do this.

Triple Loop PLL's

Triple loop PLL's are the most common technique used to obtain an output that increments in steps much smaller than the step size of the individual loops. An example is shown in Figure 1. The output tunes 45-75 MHz in 10 Hz steps to convert the 0-30 MHz HF spectrum onto a 45 MHz IF.

An offset loop operates 44-74 MHz in 100 KHz steps. The fine tune loop covers 1.0-1.1 MHz. A 45-75 MHz VCO is phase locked to the sum frequency of the offset and fine tune PLL's. Fine tune loop frequency range is always equal to the step size of the offset loop.

Phase lock in the output loop depends on phase lock in the two other loops, the mixer output being initially within the filter passband and output loop VCO being at a higher frequency than the offset loop. Two situations can cause the output loop to latch up with the other two loops locked. If the VCO is too high in frequency initially, filter output is not enough to drive the phase detector. Phase Detector output (PD_{out}) goes high and pulls the VCO further from lock. If the VCO initially is below the offset loop, the PD_{out} line tunes it away from lock.

Lock Detect (LD) from the output loop detects latch up. If the loop hasn't locked within a set amount of time, the VCO sweep circuit moves the VCO through it's operating range. During frequency changes all four transient phenomena

can occur. The triple !oop PLL is not simple to design and produce.

Offset Reference PLL Advantages

The offset reference PLL (Figure 2 and Figure 3) use two loops mixed together to produce an output with a smaller step size than the individual loops. The reference frequency difference between the two phase detectors is the output step size. Compared to the triple loop it avoids loop latch-up, uses one less PLL and can be designed with each PLL operating independently.

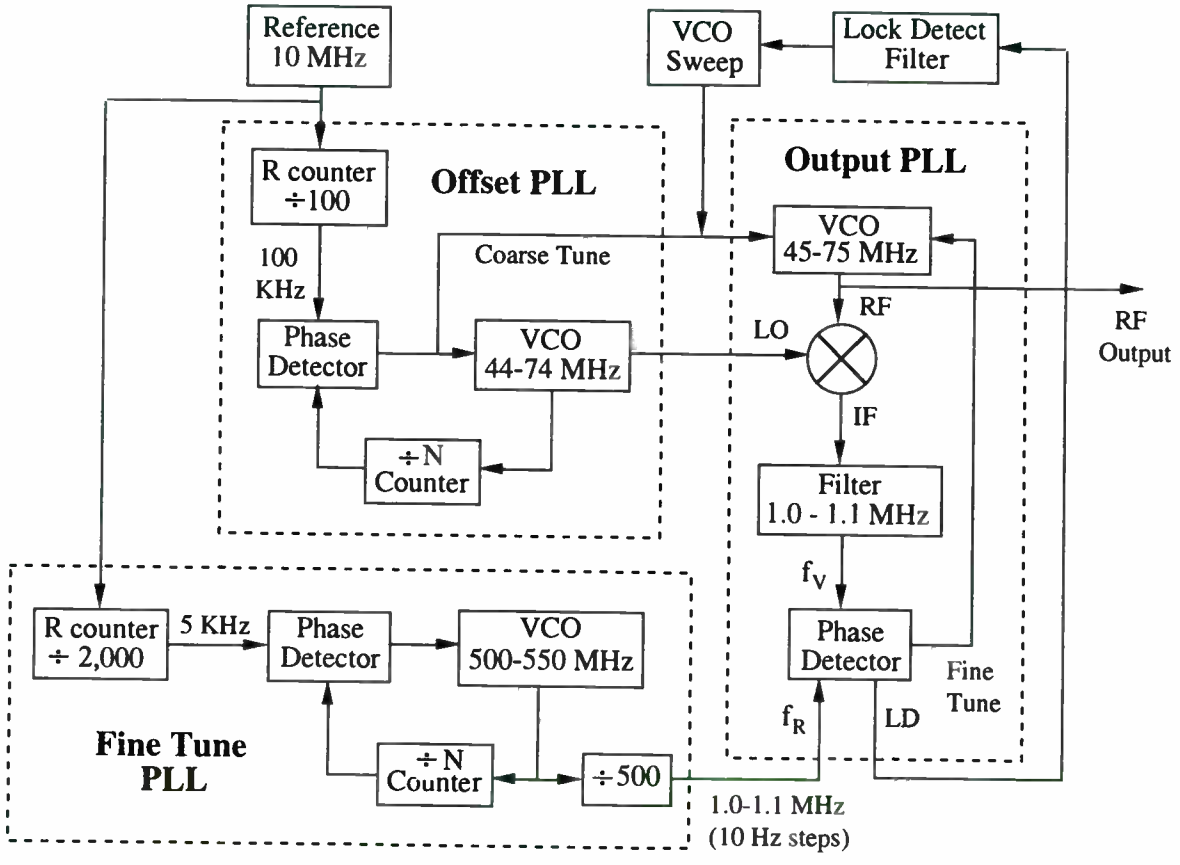

Figure 1. 45-75 MHz Triple PLL Synthesizer

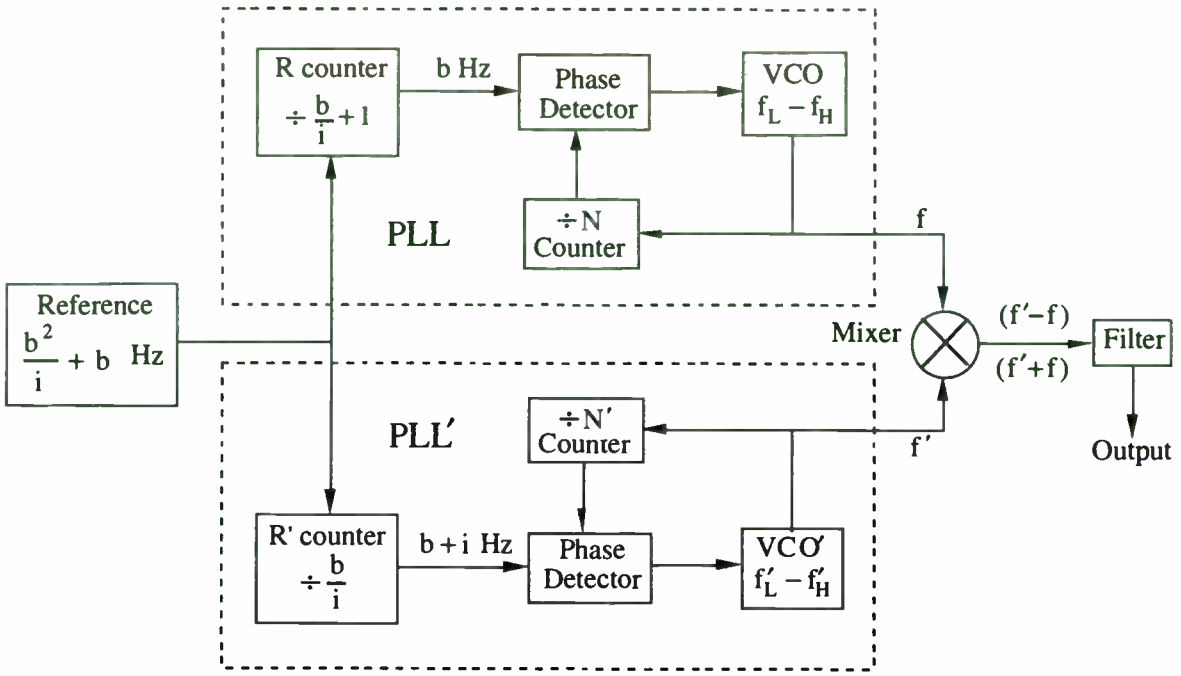

Figure 2. Output Mixed PLL's

Common Characteristics

Variable	Definition
b	Step size of PLL-Base step size
i	Step size of synthesized output $(f'-f)$, $(f'+f)$ or f depending on configuration
b+i	Step size of PLL′
C	Reference Frequency
$(f'-f)$	Mixer difference frequency output
$(f'+f)$	Mixer sum frequency output
$(f'-f)_L$	Low frequency limit of $(f'-f)$
$(f'-f)_H$	High frequency limit of $(f'-f)$
$(f'+f)_L$	Low frequency limit of $(f'+f)$
$(f'+f)_H$	High frequency limit of $(f'+f)$
R, R′	Reference divider values

Variable	Definition
N, N′	PLL, PLL′ feedback divider values
N'_L, N'_H	Lowest and highest N′ divider values
N'_{imax}	Number of N′ divider values used in addition to N'_L
f, f′	VCO, VCO′ frequency
f_L, f'_L	VCO, VCO′ lowest frequency
f_H, f'_H	VCO, VCO′ highest frequency

Table 1. Variable Definitions

N, N′ Count Sequence Except Feedback Sum Configuration

At any output frequency that is an integer multiple of the base step size (b), $f' = f'_L$. As the output is stepped up in frequency by increment (i), the N′ counter is incremented by one in the sequence $N'_L ... N'_H$. N'_H is the counter value one increment (i) below the next output frequency which is an integer multiple of (b).

Through the $N'_L...N'_H$ count sequence, N either increments or decrements by one each time the output frequency is stepped up by (i). The term in the output frequency equation which is multiplied by (b) will be held constant. At the same time the term multiplied by (i) will be increased.

N, N′ Count Sequence Feedback Sum Configuration

At any output frequency that is an integer multiple of the base step size (b), $f' = f'_H$. As the output is stepped up in frequency by increment (i), the N′ counter decrements by one in the sequence $N'_H...N'_L$. N'_L is the counter value one increment (i) below the next output frequency which is an integer multiple of (b).

Through the $N'_H...N'_L$ count sequence, N decrements by one each time the output frequency is stepped up by (i). The term in the output frequency equation which is multiplied by (b) will be held constant. At the same time the term multiplied by (i) will be increased.

Formula Limitations

There are a few restrictions on PLL and PLL′ frequencies which were made only to simplify the formulas.

Both the output and feedback mixed difference frequency configurations require $f'_L > f_H$ so that as the output increases in frequency, the N′ counter value increments.

Output frequency endpoints and either f'_L or f'_H are integer multiples of the base step size (b). This ensures that at the endpoints, VCO′ is at f'_L or f'_H. VCO′ is also at f'_L or f'_H for any output frequency between the endpoints that can be evenly divided by (b). If the conditions were not met N′ could be anywhere in it's count cycle at endpoints. Adding terms to the equations for the two VCO tuning ranges would allow endpoints to be multiples only of the incremental step size (i).

Reference frequency C is given for the lowest frequency that can produce both step sizes by integer division. The R divide value will be one greater than the R′ divider. Any reference frequency can be used that is a multiple of the C value from the table.

Since either f'_L or f'_H and C divide by both step sizes, f'_L or f'_H will be an integer multiple of C.

Variable	Design Equations
C	$C = \frac{b^2}{i} + b$ or $C = \frac{b}{i}(b+i)$
R	$R = \frac{b}{i} + 1$,
R'	$R' = \frac{b}{i}$
N'_{imax}	$N'_{imax} = \frac{b}{i} - 1$
N'_H	$N'_H = N'_L + N'_{imax}$
f′	$f' = N'(b+i)$
$f'_H - f'_L$	$f'_H - f'_L = \frac{b^2}{i} - i$
f'_H	$f'_H = f'_L + \frac{b^2}{i} - i$

Table 2. Formulas for all configurations

Output Mixed PLL's

Variable	Design Equation
$(f'-f)$	$(f'-f)=b(N'-N)+N'i$
$(f'-f)_L$	$(f'-f)_L=f'_L-f_H+N'_{imax}b$
$(f'-f)_H$	$(f'-f)_H=f'_L-f_L$
f'_L	Any frequency for which $f'_L>f_H$ and f'_L is an integer multiple of C
f	$f=Nb$
f_L	$f_L=f'_L-(f'-f)_H$
f_H	$f_H=f'_L-(f'-f)_L+N'_{imax}b$
f_H-f_L	f_H-f_L $=(f'-f)_H-(f'-f)_L+N'_{imax}b$

Table 3 Output Mixed $(f'-f)$ formulas

Output $(f'-f)$ Key Points

a) RF output is $(f'-f)$ with $f'_L>f_H$

b) C and f'_L divide evenly by both step sizes.

c) $(f'-f)_L$, $(f'-f)_H$ divide evenly by b

Output $(f'-f)$ Example

The desired frequency range is 150-154 MHz in 0.5 MHz steps using PLL's with 2.0 MHz and 2.5 MHz step sizes.

Reference Frequency:

$$C=\frac{b^2}{i}+b=\frac{2^2}{0.5}+2=10\text{ MHz}$$

The Reference divider values are:

$$R=\frac{b}{i}+1=\frac{2}{0.5}+1=5$$

$$R'=\frac{b}{i}=\frac{2}{0.5}=4$$

The number of N' counter values used in addition to N'_L is:

$$N'_{imax}=\frac{b}{i}-1=\frac{2}{0.5}-1=3$$

The frequency range of VCO' is:

$$f'_H-f'_L=\frac{b^2}{i}-i=\frac{2^2}{0.5}-0.5=7.5\text{ MHz}$$

The frequency range of VCO is:

$$\begin{aligned}f_H-f_L&=(f'-f)_H-(f'-f)_L+N'_{imax}b\\&=154-150+3(2)\\&=10\text{ MHz}\end{aligned}$$

f'_L and f_H frequencies depend on each other. To select values, the equation for f_H is solved in terms of f'_L:

$$\begin{aligned}f_H&=f'_L-(f'-f)_L+N'_{imax}b\\&=f'_L-150+3(2)\\&=f'_L-144\end{aligned}$$

Frequencies used for f'_L and f_H are a tradeoff between phase noise and ease of filtering the mixer products. As f'_L and f_H increase filtering of mixer products improves. However the VCO noise increases. The same VCO resonator Q at a higher frequency results in higher noise for the same offset frequency. PLL IC's also produce more noise with increasing frequency.

f'_L of 500 MHz is chosen. The frequency range of VCO' is 500-507.5 MHz. The frequency range of VCO is 346-356 MHz

To check results all divide values and frequencies are in table 4.

$(f'-f)$ MHz	N	N'	f MHz	f' MHz
150	175	200	350	500
150.5	176	201	352	502.5
151	177	202	354	505
151.5	178	203	356	507.5
152	174	200	348	500
152.5	175	201	350	502.5
153	176	202	352	505
153.5	177	203	354	507.5
154	173	200	346	500

Table 4. Output Mixed $(f'-f)$ example

Variable	Design Equation
$(f'+f)$	$(f'+f)=b(N'+N)+N'i$
$(f'+f)_L$	$(f'+f)_L=f_L+f'_L+N'_{imax}b$
$(f'+f)_H$	$(f'+f)_H=f_H+f'_L$
f'_L	Any frequency f'_L which is an integer multiple of C
f	$f=Nb$
f_L	$f_L=(f'+f)_L-f'_L-N'_{imax}b$
f_H	$f_H=(f'+f)_H-f'_L$
f_H-f_L	$f_H-f_L=(f'+f)_H-(f'+f)_L+N'_{imax}b$

Table 5. Output Mixed $(f'+f)$ formulas

Output $(f'+f)$ Key Points

a) RF output is $(f'+f)$

b) C and f'_L divide evenly by both step sizes.

c) $(f'+f)_L$, $(f'+f)_H$ divide evenly by b

Output $(f'+f)$ Example

The desired frequency range is 800-801 MHz in 125 KHz steps using PLL's with 500 KHz and 625 KHz step sizes.

Reference Frequency:

$$C=\frac{b^2}{i}+b=\frac{500^2}{125}+500=2.5\text{ MHz}$$

The Reference divider values are:

$$R=\frac{b}{i}+1=\frac{500}{125}+1=5$$

$$R'=\frac{b}{i}=\frac{500}{125}=4$$

The number of N' counter values used in addition to N'_L is:

$$N'_{imax}=\frac{b}{i}-1=\frac{500}{125}-1=3$$

The frequency range of VCO' is:

$$f'_H-f'_L=\frac{b^2}{i}-i=\frac{500^2}{125}-125=1.875\text{ MHz}$$

The frequency range of VCO is:

$$f_H-f_L=(f'+f)_H-(f'+f)_L+N'_{imax}b$$
$$=801-800+3(0.5)$$
$$=2.5\text{ MHz}$$

f'_L and f_H frequencies depend on each other. To select values, the equation for f_H is solved in terms of f'_L:

$$f_H=(f'+f)_H-f'_L \quad \text{or} \quad f_H=801-f'_L$$

Frequencies used for f'_L and f_H are a tradeoff between phase noise and ease of filtering the undesired mixer products. The best filtering of spurious mixer products occurs if both VCO's are operating at about half the desired output frequency. This increases the frequency separation of the sum and difference products. VCO noise increases with frequency. The same VCO resonator Q at a higher frequency results in higher noise for the same offset frequency. PLL IC's also produce more noise with increasing frequency.

f'_L of 400 MHz is chosen. The frequency range of VCO' is 400-401.875 MHz. The frequency range of VCO is 398.5-401 MHz

To check results all divide values and frequencies are in table 6.

$(f'+f)$ MHz	N	N'	f MHz	f' MHz
800	800	640	400	400
800.125	799	641	399.5	400.625
800.25	798	642	399	401.25
800.375	797	643	398.5	401.875
800.5	801	640	400.5	400
800.625	800	641	400	400.625
800.75	799	642	399.5	401.25
800.875	798	643	399	401.875
801	802	640	401	400

Table 6. Output Mixed $(f'+f)$ example

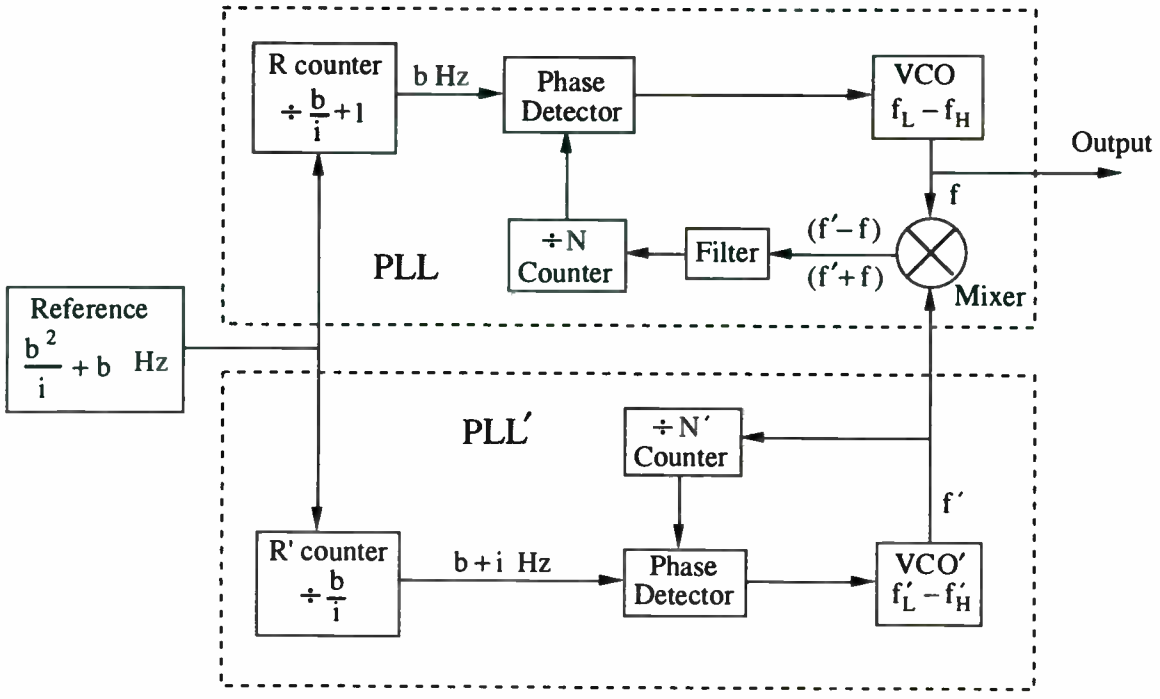

Figure 3. Feedback Mixed PLL's - f output

Feedback Mixed PLL's

Variable	Design Equation
f	$f = b(N' - N) + N'i$
f'_L	Any frequency for which $f'_L > f_H$ and f'_L is an integer multiple of C
$(f'-f)_L$	$(f'-f)_L = f'_L - f_H$
$(f'-f)_H$	$(f'-f)_H = f'_L - f_L + N'_{imax}b$
$(f'-f)_H$ $-(f'-f)_L$	$(f'-f)_H - (f'-f)_L$ $= f_H - f_L + N'_{imax}b$

Table 7 Feedback $(f'-f)$ formulas

Feedback $(f'-f)$ Key Points

a) RF output is f with $f'_L > f_H$

b) C and f'_L divide evenly by both step sizes.

c) f_L, f_H divide evenly by b

d) Feedback mixer output is $(f'-f)$

Feedback $(f'-f)$ Example

The desired frequency range is 63-64 MHz in 100 KHz steps using PLL's with 500 KHz and 600 KHz step sizes.

Reference Frequency:

$$C = \frac{b^2}{i} + b = \frac{500^2}{100} + 500 = 3\,\text{MHz}$$

The Reference divider values are:

$$R = \frac{b}{i} + 1 = \frac{500}{100} + 1 = 6$$

$$R' = \frac{b}{i} = \frac{500}{100} = 5$$

The number of N′ counter values used in addition to N'_L is:

$$N'_{imax} = \frac{b}{i} - 1 = \frac{500}{100} - 1 = 4$$

The frequency range of VCO′ is:

$$f'_H - f'_L = \frac{b^2}{i} - i = \frac{500^2}{100} - 100 = 2.4\ \text{MHz}$$

The frequency range of VCO is the output frequency range which is 63-64 MHz.

f'_L is selected such that $f'_L > f_H$ and f'_L is an integer multiple of C. If the frequency ranges for VCO and VCO′ are close together, sum and difference products from the mixer will be further apart and easier to filter.

If both VCO's operate at close to the output frequency, they might overlap. Mixer output could be $(f - f')$ and VCO would be pulled in the wrong direction.

f'_L of 66 MHz is chosen. The frequency range of VCO′ is 66-68.4 MHz. N counter input frequency range is:

$$(f'-f)_L = f'_L - f_H$$
$$= 66 - 64$$
$$= 2\ \text{MHz}$$
$$(f'-f)_H = f'_L - f_L + N'_{i\max} b$$
$$= 66 - 63 + 4(0.5)$$
$$= 5\ \text{MHz}$$

To check results all divide values and frequencies are in table 8.

$(f'-f)$ MHz	N	N′	f MHz	f′ MHz
3	6	110	63	66
3.5	7	111	63.1	66.6
4	8	112	63.2	67.2
4.5	9	113	63.3	67.8
5	10	114	63.4	68.4
2.5	5	110	63.5	66
3	6	111	63.6	66.6
3.5	7	112	63.7	67.2
4	8	113	63.8	67.8
4.5	9	114	63.9	68.4
2	4	110	64	66

Table 8. Feedback $(f'-f)$ example

Variable	Design Equation
f	$f = b(N - N')i$
f'_H	f'_H is an integer multiple of C
$(f'+f)_L$	$(f'+f)_L = f'_L + f_L + N'_{i\max} i$
$(f'+f)_H$	$(f'+f)_H = f_H + f'_H$
$(f'+f)$	$(f'+f) = Nb$

Table 9. Feedback $(f'+f)$ formulas

Feedback $(f'+f)$ Key Points

a) RF output is f
b) C and f'_H divide evenly by both step sizes.
c) f_L, f_H divide evenly by b
d) Feedback mixer output is $(f'+f)$

Feedback $(f'+f)$ Example

The desired frequency range is 63-64 MHz in 100 KHz steps using PLL's with 500 KHz and 600 KHz step sizes.

Reference Frequency:

$$C = \frac{b^2}{i} + b = \frac{500^2}{100} + 500 = 3\,\text{MHz}$$

The Reference divider values are:

$$R = \frac{b}{i} + 1 = \frac{500}{100} + 1 = 6$$

$$R' = \frac{b}{i} = \frac{500}{100} = 5$$

The number of N′ counter values used in addition to N'_H is:

$$N'_{i\max} = \frac{b}{i} - 1 = \frac{500}{100} - 1 = 4$$

The frequency range of VCO′ is:

$$f'_H - f'_L = \frac{b^2}{i} - i = \frac{500^2}{100} - 100 = 2.4\ \text{MHz}$$

The frequency range of VCO is the output frequency range which is 63-64 MHz.

f'_H is selected to be an integer multiple of C. If the frequency ranges for VCO and VCO′ are close together, sum and difference products from the mixer will be further apart and easier to filter.

f'_H of 66 MHz is chosen. The frequency range of VCO′ is 63.6-66 MHz.

The frequency limits of the input to the N counter are:

$$(f'+f)_L = f'_L + f_L + N'_{i\,max}\,i$$
$$= 63.6 + 63 + 4(0.1)$$
$$= 127\ \text{MHz}$$
$$(f'+f)_H = f_H + f'_H$$
$$= 64 + 66$$
$$= 130\ \text{MHz}$$

To check results all divide values and frequencies are in table 10.

$(f'+f)$ MHz	N	N′	f MHz	f′ MHz
129	258	110	63	66
128.5	257	109	63.1	65.4
128	256	108	63.2	64.8
127.5	255	107	63.3	64.2
127	254	106	63.4	63.6
129.5	259	110	63.5	66
129	258	109	63.6	65.4
128.5	257	108	63.7	64.8
128	256	107	63.8	64.2
127.5	255	106	63.9	63.6
130	260	110	64	66

Table 10. Feedback $(f'+f)$ example

Design Tradeoffs

Limitations of Feedback Sum

Feedback sum output causes the N counter to operate at a higher frequency than the desired output. Phase noise within the loop bandwidth could be up to 8-9 dB worse than the feedback difference circuit. The worst case for phase noise is the best case for spurious product suppression from the mixer (both VCO's operate at about the same frequency).

Output Mixed Difference

At least one VCO will operate at frequencies above the desired output. This is most useful where the output tuning range is a high percentage of the center frequency. Frequencies of DC-100 MHz for example would be simple to implement in this configuration. If the feature is not needed phase noise will be higher than necessary.

Feedback Difference

This technique results in low phase noise and avoids mixer products being in the output. It works well when both VCO's can tune the ranges needed without range switching. Output mixed sum should also be considered.

Output Mixed Sum

If the output is between 400 MHz and 800 MHz it may be better to use two JFET VCO's and sum the outputs. Two bipolar VCO's combined using feedback difference might have higher phase noise. Also the loops function independently.

Output vs. Feedback Mixing

Output mixing allows both PLL's to operate independently. Spurious mixer products will be present on the output. Feedback mixing results in the products being on the PLL input where they will need much less filtering. Also the switching time and damping may depend on both PLL's

The total number of N′ counter values used is:

$$N'_{Total} = \frac{b}{i}$$

Due to N'_{Total}, it is quite likely that the tuning range of VCO′ is much smaller than that of VCO. VCO′ would then frequency hop much more quickly. The frequency switching characteristics of PLL using feedback mixing might not be dependent on PLL′.

Frequency Range Extension

Both the output mixed sum and feedback mixed difference PLL's can extend the frequency range of the PLL IC's they are used with by approximately two times. Both VCO's would need to be on about the same frequency.

Summary

A series of examples and equations has been described to illustrate a technique that though not commonly applied is an elegant way to achieve fine resolution and faster switching.

Offset reference PLL's have become much easier to implement since the introduction of dual loop PLL IC's such as the Motorola MC145220 which operates from DC-1.1 GHz. Phase Detector and Reference divider maximum input frequencies are the major limitation on (b) to (i) ratio.

Shortly a MC145220 EVK (Evaluation Kit) will be released which implements the output mixed difference technique to achieve 30 mS switching from 47.8-77.7 MHz. After the switching time has elapsed, the output is within 1 KHz of final frequency. PLL has 10 KHz steps and PLL′ has 10.01 Khz steps. Output increment size is 10 Hz. 10 KHz sideband levels are -80 dB.

Acknowledgment

[1] Jim Irwin of Motorola, Semiconductor Products Sector provided many examples of alternative multiple loop schemes.

Reference

[1] Communications Device Data (DL136/D Rev.3), Motorola, 1993.

MOTOROLA'S MOSAIC™ V SILICON BIPOLAR RF BUILDING BLOCKS FILL GAPS IN HIGH PERFORMANCE LOW POWER WIRELESS CHIP SETS

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Abstract- **Motorola's MOSAIC™ V RF silicon bipolar process is well suited for low power, cost sensitive wireless applications. The use of a high frequency silicon process technology and novel circuit techniques has resulted in the production of high performance low power RF building blocks. These circuits fill the need for complete RF system configuration with a minimum number of external components. These circuits operate at supply voltages as low as 1.8V and at frequencies up to 2.4GHz. Unique mixer configurations are employed in these circuits to provide superior linearity at very low power consumption. Each linear mixer features a single ended 50Ω input while providing double balanced operation.**

I. INTRODUCTION

Today's portable communication products require circuits that can perform well in a low power environment. This has been brought on by a reduction of power supply voltages (allowing for fewer battery cells, reducing size and weight) and a requirement that circuitry draw less current (extending battery lifetime). These new constraints adversely affect the performance of standard RF circuitry.

Cost is another factor constraining a designer of portable communications products. This typically leads to the use of silicon integrated technology for as much of the high frequency signal processing as possible. Silicon bipolar technology is very cost effective especially when small feature sizes are implemented on a large wafer. Bipolar circuits which can achieve the design goals for noise figure, linearity and power consumption for portable communications products are clearly needed.

II. SILICON PROCESSING

High performance receiver front end circuits were fabricated using Motorola's advanced silicon bipolar MOSAIC V process (Fig. 1). Process characteristics include a 0.4µm effective emitter width, 14GHz f_t, a 1Ω-cm p+ substrate, poly silicon emitter and trench isolation.

A. Signal Isolation

Signal isolation is a critical parameter in RF integrated circuit design. Isolation on the packaged die is greatly aided by the use of a low resistance top side substrate contact.

Isolation measurements between two MOSAIC V epi contacts spaced 12µm apart and separated by a top side substrate contact were made. The results of this measurement are shown in Fig. 2. The data shows that this process is capable of achieving 94dB of isolation at 1GHz. The actual isolation achieved in practice will be limited by the package that the die is placed in.

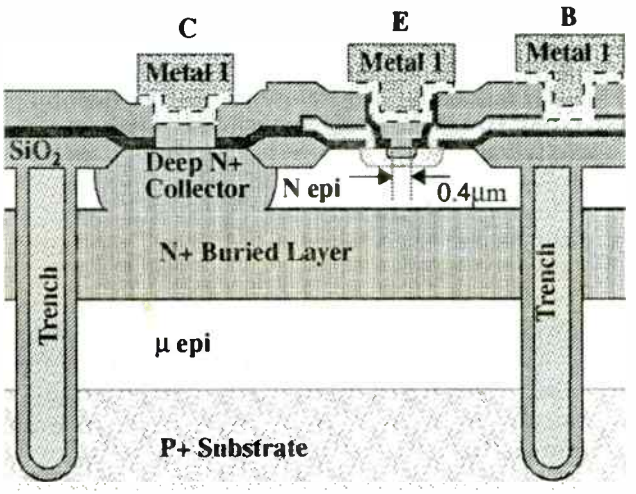

Fig. 1. MOSAIC V NPN transistor cross section

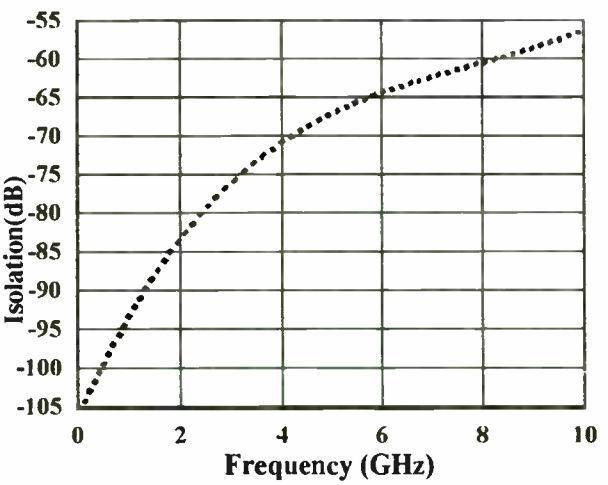

Fig. 2. Epi contact isolation versus frequency

III. PACKAGING

Motorola continues its commitment to wireless integrated circuits by introducing a new plastic 20 pin thin quad flat package (TQFP) customized for RF applications. This plastic package features a 4mm x 4mm body and 0.65mm pin pitch. The leadframe (Fig. 3) is customized for RF signal isolation which is further improved by the connection of two leads directly to the leadframe flag.

MOSAIC is a trademark of Motorola, Inc.

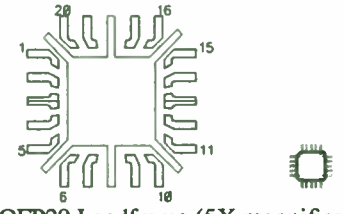

Fig. 3. TQFP20 Leadframe (5X magnification) and package (1X magnification)

The quad arrangement eases external component configuration, allows easy access to ground pins and reduces the need for signal line width tapering.

A. *Characterization and Modeling*

The RF suitability of the package can not be appropriately used in the design and simulation of a circuit without the aid of an accurate package model. Electromagnetic simulation of the package construction in addition to RF package characterization based on measured S-parameters yields a reliable model which uses only lumped elements (Fig. 4.). Additionally, the effects of substrate coupling is minimized due to the top side substrate contact and the low resistivity substrate in the MOSAIC V process. Modeling of the substrate is essential for RF circuits which are processed on moderate to high resistivity substrates or those which do not include a low resistance top side connection to substrate.

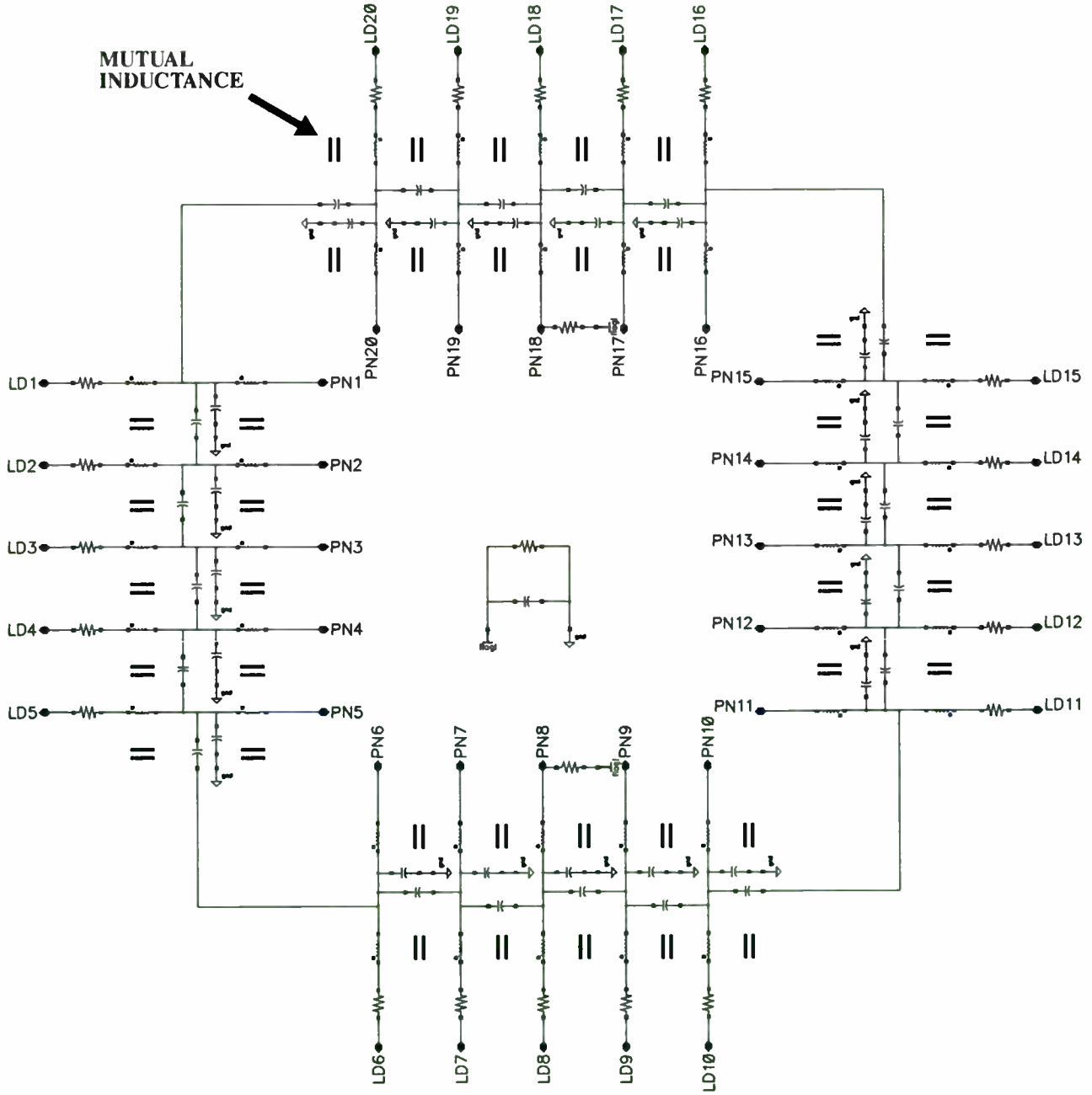

Fig. 4. TQFP20 lumped element model

IV. CIRCUIT TECHNIQUES

The basis for a frequency mixer is typically a transconductor and a switch. It is important to maximize linearity in the transconductor while minimizing transition time in the switch.adfgsdfg

A. Common Approaches

High linearity differential transconverter circuits based on variations of the differential pair typically trade linearity for transconductance and noise. Emitter degeneration resistance is often used to absorb some of the input signal. In doing so, the linear range is improved but the transconductance suffers and the noise increases. Alternatively, cross coupling and area ratioing of differential pairs is also used for linearity expansion [1], [2].

Each of the above mentioned transconductors feature improved linearity but none of them arrive at this without a degradation in noise performance and a reduction in transconductance. The peak output current is limited to the quiescent current in each of these circuits and none of these feature a method of reducing the input impedance which is typically desired to be 50 Ω.

B. Amplifier Distortion Theory

The nonlinearities in the transfer function of an amplifier can be expressed as a power series [3], [4]:

$$y = f(x) \Rightarrow y = \sum_{n=0}^{\infty} C_n x^n \tag{1}$$

$$y = C_0 + C_1 x + C_2 x^2 + C_3 x^3 + C_4 x^4 + \ldots \tag{2}$$

$$C_n = \frac{1}{n!}\left(\frac{d^n}{dx^n} y(x)\right)\Big|_{x=0} \tag{3}$$

Harmonic and intermodulation distortion can be calculated from the power series coefficients. If two tones (4) are applied at the amplifier input then the resulting output will include intermodulation and distortion products.

$$x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \tag{4}$$

If the input signals (4) in a two tone test are assumed to be equal in amplitude, the input referred third order intermodulation intercept point (IP^3_i) can be easily calculated. The time varying third order intermodulation signal is defined in (5). IP^3_i is the input power level at which (6) is satisfied assuming that the third order distortion is the dominant source of the third order intermodulation.

$$IM3(t) = \left(\frac{3}{4}C_3 A_1^2 A_2 + \frac{5}{4}C_5 A_1^4 A_2 + \frac{15}{8}C_5 A_1^2 A_2^3 + \ldots\right)\cos(2\omega_1 t \pm \omega_2 t) + \left(\frac{3}{4}C_3 A_1 A_2^2 + \frac{5}{4}C_5 A_1 A_2^4 + \frac{15}{8}C_5 A_1^3 A_2^2 + \ldots\right)\cos(\omega_1 t \pm 2\omega_2 t) \tag{5}$$

$$IP_i^3 \cong A\Big|_{\left(\frac{3}{4}\right)C_3 A_1^2 A_2 = C_1 A_1\Big|_{A_1 = A_2 = A}} = \sqrt{\frac{4C_1}{3C_3}} \tag{6}$$

C. Linear Transconverter

Fig. 5 shows an improved transconverter cell[1]. The features of this cell include:

- High linearity
- Low noise
- High peak current
- Low quiescent current
- Good transconductance
- Selectable input impedance
- Single ended drive
- Differential output

This circuit utilizes a common base transistor (Q_4) and a current mirror (Q_5, Q_6). When current flows through the input, it adds to the quiescent current going through the mirror thus raising the input voltage. As the input voltage rises, the current flowing through the common base transistor, Q_4, decreases. Current flowing through the input of this cell appears as a difference between two output currents, I_{Q4c} and I_{Q6c}. The cell thus linearly converts a single ended signal into a differential signal.

The purpose of the series resistors, R_7 and R_8, is to increase the linearity of the cell when driven by a voltage.The mathematical analysis which follows shows that there is a single optimum value for these resistors.

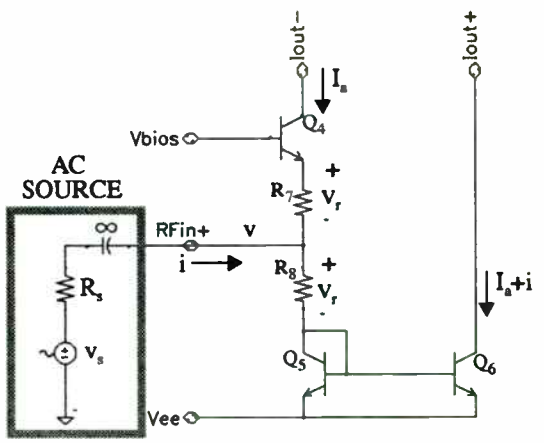

Fig. 5. Linear transconverter

D. Analysis

Define:
- I_q = quiescent current in transistors Q_4, Q_5 and Q_6
- i = delta input current
- I_a = active current in Q_4
- I_a+i = active current in Q_5, Q_6
- R_s = source resistance
- R = R_c=resistance value of R_7 and R_8
- v_s = source voltage before source resistance
- v = delta input voltage
- V_r = quiescent voltage across R_7 and R_8
- Vt = thermal voltage=kT/q

If V_r is biased such that (7) is satisfied then third order nulling is achieved (8). IP^3_i must then be redefined for it will be dominated by fifth order distortion (9). Equation (7) can be satisfied through proper biasing and resistance selection (10).

$$V_r = RI_q = \frac{Vt}{2} \tag{7}$$

1. Patent Pending, Eric Main and Jeff Durec, February 1994.

$$C_3 = \left.\frac{\frac{1}{2} - \frac{1}{3}\left(1 + \frac{RI_q}{Vt}\right)}{\left(1 + \frac{RI_q}{Vt}\right)^5}\right|_{V_r = \frac{Vt}{2}} = 0 \qquad (8)$$

$$IP_i^3 \cong A\left|_{\frac{5}{4}C_3A_1^4A_2 + \frac{15}{8}C_5A_1^2A_2^3 = C_1A_1}\right. = \left(\frac{8}{25}\frac{C_1}{C_5}\right)^{1/4} \qquad (9)$$

$$R = \frac{Vt}{2I_q} \qquad (10)$$

The input resistance of this circuit is calculated in (11). In biasing this circuit, values for I and Re should be chosen such that (12) and (13) are satisfied.

$$R_{in} = (R_7 + re_{Q4}) \| (R_8 + re_{Q5}) \qquad (11)$$

$$R = R_7 = R_8 = \frac{re}{2} = \frac{2}{3}R_S \qquad (12)$$

$$I_q = \frac{Vt}{re} = \frac{3}{4}\frac{Vt}{R_S} \qquad (13)$$

The proper biasing of this circuit will put it into an efficient state maximizing linearity for a given quiescent current.

V. MIXER IMPLEMENTATION

Fig. 6 depicts the block diagram and pin out for a class AB linear mixer (MC13143). The class AB nature of the circuit allows for a low quiescent current while a high power input will cause an increase of the bias.The concept of a class AB mixer has been implemented in the past as a single-balanced architecture but not as a double-balanced architecture. The linearity of single-balanced architectures typically requires increased power consumption. The double balanced architecture provides an improvement in LO to IF and RF to IF isolation when implemented in a down conversion mixer.

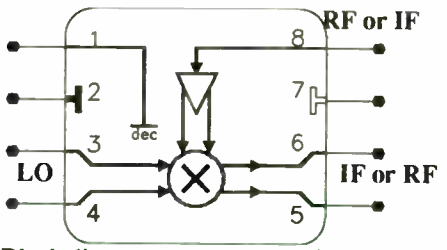

Fig. 6. Block diagram of class AB up/down mixer

The double-balanced class AB mixer has a +3dBm input 1dB compression point, 50Ω single-ended input, and an input third order intermodulation intercept (IP^3_i) which can be externally programed as high as +21dBm. Nominal single sideband mixer noise figure (NF_{SSB}) of less than 12dB and conversion gain of -3dB are achieved at a supply voltage of 2V while consuming under 1mA of supply current. This circuit has wide bandwidth at all three ports and can thus be operated as either an upconversion or a downconversion mixer. The die was packaged in a standard plastic eight pin SOIC package.

Fig. 7 displays the schematic of the class AB mixer based on the linear transconverter core (Fig. 5). The bias voltages for the RF and LO are derived internally with the RF bias point pinned out to allow for increased decoupling and linearity adjustment. This circuit has a die area of 19.8mil x 19.8mil (Fig. 8).

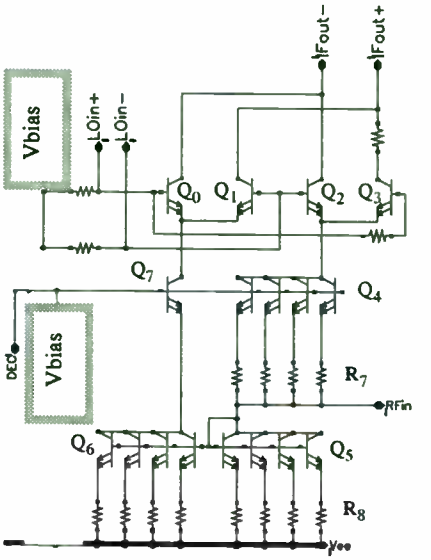

Fig. 7. Schematic of MC13143

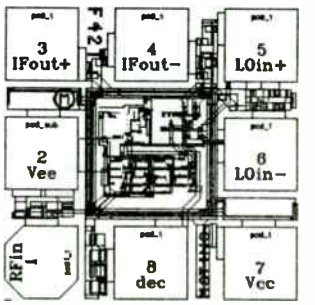

Fig. 8. MC13143 layout (100X magnification)

VI. MC13143 MEASURED DATA

The AC performance of the input impedance is shown in Fig. 9. The 50Ω match requires only a DC blocking capacitor (100pF) with the remaining broadband matching defined by the internal circuitry. Typically amplifier inputs are matched with reactive components which provide only a narrow band match. The new cell has an input return loss in excess of 20dB over a very wide frequency range. This broadband match allows for easy interfacing to an RF filter such as a SAW device. Out of band stability is also aided by the broadband match.

The test conditions for the following data plots include:

Vs = 2V
RF frequency=900MHz
IF frequency=50MHz
LO frequency=950MHz
RF amplitude=-30dBm
LO amplitude=0dBm

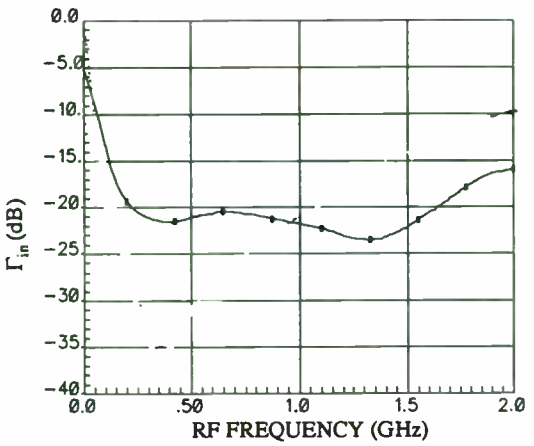

Fig. 9. Input return loss versus frequency

Fig. 10 depicts the power conversion gain and noise figure versus LO frequency. NF_{SSB} at an LO of 950MHz and an IF of 50MHz is just under 12dB. Acceptable performance is achieved through 1.8GHz. Fig. 11 shows the power conversion gain and noise figure versus LO power. A minimum single-sided noise figure of 11.8dB is achieved at an LO power of 0dB with an associated conversion gain of -3.2dB. Fig. 12 depicts power conversion gain and supply current versus RF power. The input -1dB compression point (Pin_{1dB}) is shown to be +3dBm. At an RF power level of -20dBm, the supply current begins to rise as the class AB nature of the circuit exhibits itself. A slight gain increase occurs at 0dBm input. Fig. 13 shows the power conversion gain and the supply current versus supply voltage. This graph shows that the gain and power consumption is very well regulated against supply variations. This circuit can be used in applications requiring between two and five battery cells (1.8V-6.5V).

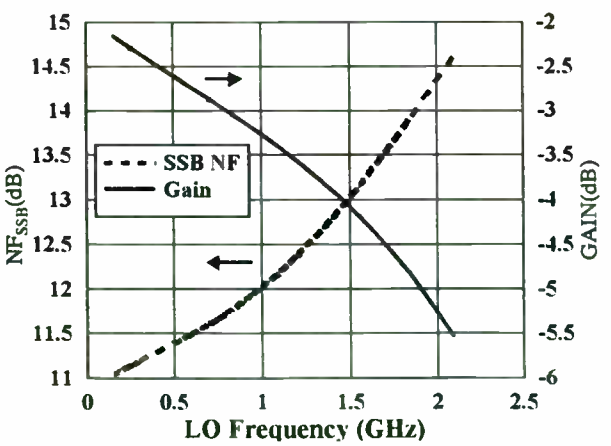

Fig. 10. Noise Figure and Gain versus LO frequency

The effects of the linearity adjustment is shown in Fig. 14 where IP^3_i, conversion gain and supply current are plotted versus adjustment current. The data for this graph included a power supply of 3V and -27.5dBm RF power level. A maximum IP^3_i of +21dBm is achieved at an adjustment current of 3mA with an associated supply current of 8.8mA. The linearity adjustment feature of this circuit is an important facet because it allows for the linearity to be programmed for a particular application. Certain applications favor reduced power consumption over linearity whereas other applications sacrifice power drain for linearity improvements. This circuit can accommodate each of these applications.

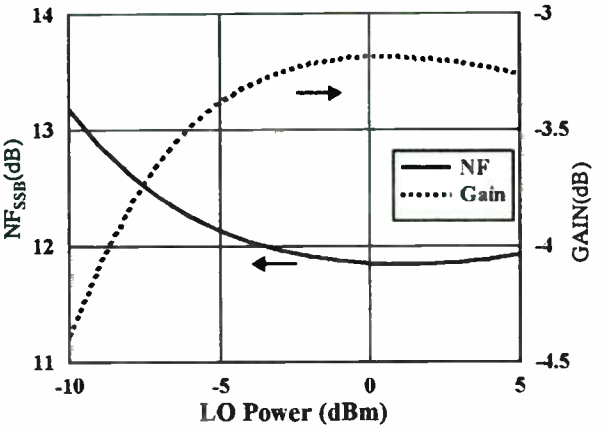

Fig. 11. Noise Figure and Gain versus LO power

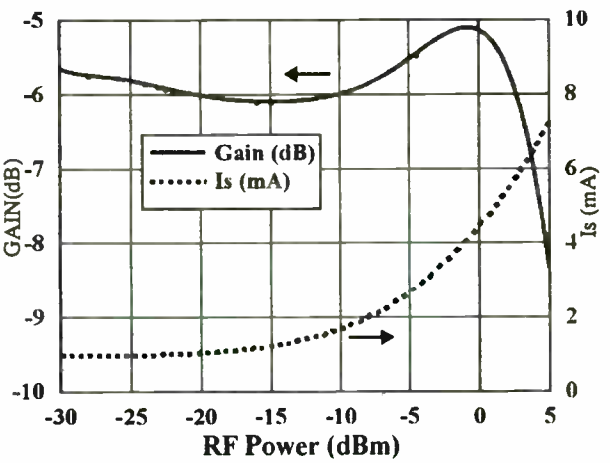

Fig. 12. Power Conversion gain and supply current versus RF power

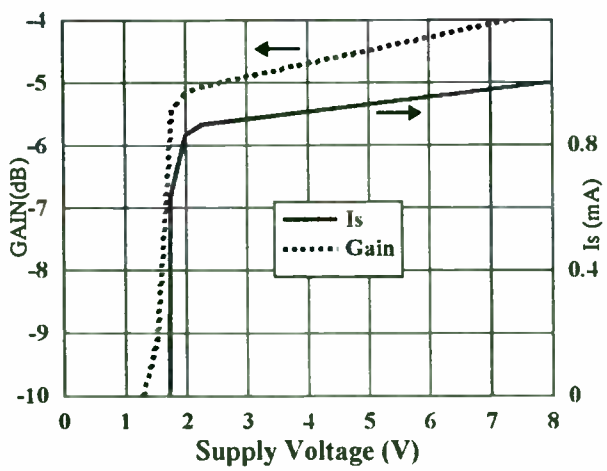

Fig. 13. Power Conversion Gain and supply current versus supply voltage

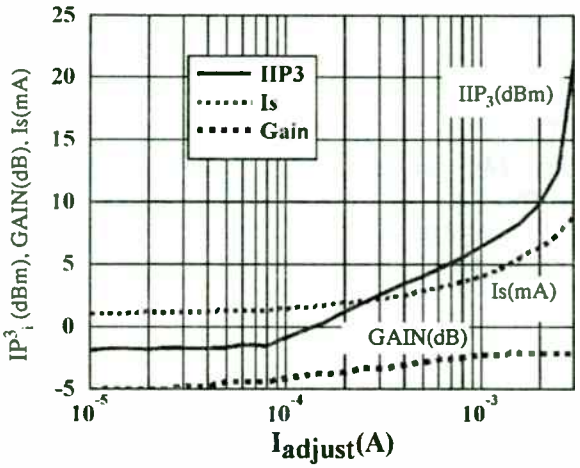

Fig. 14. IP^3_i versus linearity adjustment current

VII. MC13141

The MC13141 is intended to be used as a first amplifier and down converter for RF applications. It features wide band operation, low noise, high gain, and high linearity while maintaining low current consumption. The circuit consists of a Low Noise Amplifier (LNA), a Local Oscillator amplifier (LOamp), a mixer, an Intermediate Frequency amplifier (IFamp) and a DC control section with enable function. This circuit is available in the SOIC8 (Fig. 15), SOIC14 and TQFP20 packages.

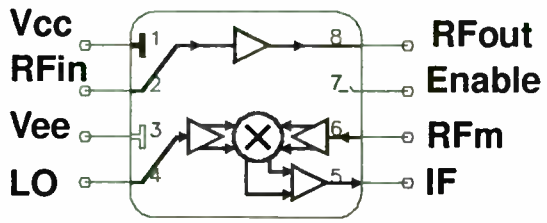

Fig. 15. MC13141 SOIC8 package

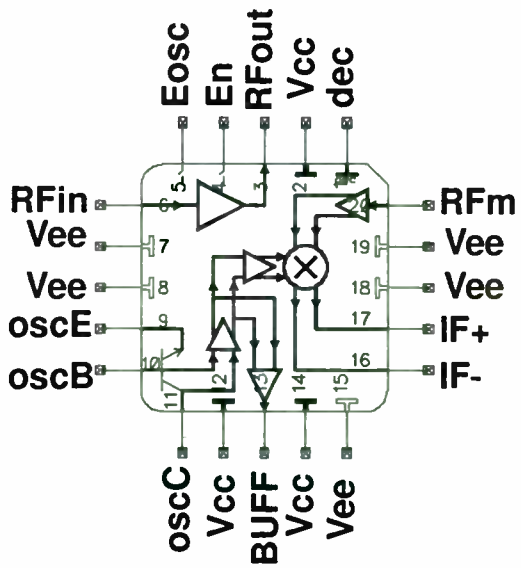

Fig. 16. MC13142 TQFP20 package

VIII. MC13142

The MC13142 adds a voltage controlled oscillator and to the MC13141 circuit. The Mixer and Oscillator can be enabled independently. This circuit is available in the SOIC16 and TQFP20 (Fig. 16) packages.

IX. PERFORMANCE OVERVIEW

The performance data for the RF circuits is summarized in TABLE 1. Linearity adjustment of the mixer is available in each circuit except the SOIC8 version of the MC13141. The availability of the linearity adjustment allows the user to program the circuit for the desired linearity with a minimal change in the gain. The MC13143 data reveals that very high linearity (IP^3_i of +21dBm) is achieved at a quite efficient power dissipation (8.8mA at 3V). These results prove the versatility and high performance nature of the new class AB mixer.

TABLE 1. Performance Data

	Gp(dB)	NF(dB)	IP^3_i
MC13141			
LNA	17	2.5	-5
MIXER	1	17	+3
MC13142			
LNA	17	2.5	-5
MIXER	-3	11.5	-3
MC13143			
MIXER	-3	11.8	-3 ➡+21

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[6] H. Sapotta, "Push-Pull Receiver Input Amplifier Stages -- The Solution to Intermod Problems," *Proceedings of the Second Annual WIRELESS Symposium*, pp. 10-11, Feb. 1994.

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Dual Conversion FM Narrowband Receiver for Cellular and Cordless Phone Uses Low Cost Monolithic IC Chip Set.

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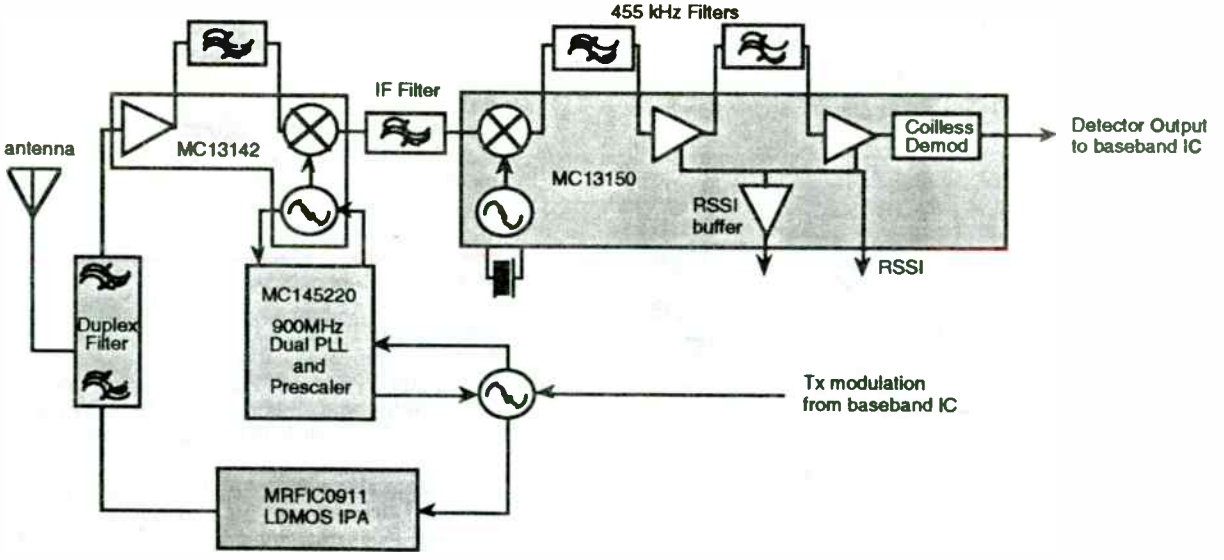
Introduction

This paper describes an analog narrowband FM receiver designed for cellular and 902-928 MHz ISM Band Part 15 cordless phone applications[1]. The receiver is a dual conversion superheterodyne receiver incorporating a low cost silicon monolithic IC chip set which is comprised of an integrated LNA, Mixer and VCO RF front end IC, MC13142 and a single conversion, split IF and coilless detector back end IC, MC13150. Design techniques to optimize the receiver sensitivity and noise performance are analyzed and developed; tradeoffs in signal handling and power management are discussed. Surface mount components, small size PCB layout and few external components allow fabrication of a receiver suitable for cellular and portable applications. Performance is verified in a demonstration receiver.

Figure 1 shows a simplified block diagram of an analog/digital FM narrowband RF section commonly used in low cost, high volume analog cellular services today. The receiver topology may be used to implement popular wireless communications applications such as 100 channel 902 - 928 MHz cordless phones, Cellular packet radio, Special Mobile Radio (SMR), Narrowband PCS (covers messaging and paging services), and the newly proposed Family Radio Services at 462 and 467 MHz for very short distance Two-Way Radio service (FCC 95-261 released Aug 2, 1995).[1]

Figure 1 - Analog/Digital FM Narrowband RF Section



Description of Chip Set

Front End Receiver IC

The MC13142 [2] is intended to be used as the first amplifier, voltage controlled oscillator and down converter. It features wideband operation, low noise, high gain and excellent linearity while maintaining low current consumption. The circuit consists of a low noise amplifier (LNA), a voltage controlled oscillator (VCO), a buffered oscillator output, a doubly balanced mixer, a wideband IF amplifier and a dc control section. The wideband IF amp allows this IC to also be used as an up converter and exciter amplifier.

The IC is offered in two packages: 1) 16 Pin SOIC and 2) 20 Pin thin quad flat package (TQFP). Figures 3 and 4 show the MC13142 pin connections in both packages. In the TQFP package, a pin is provided for linearity adjustment of the mixer; the input intercept point may be increased up to +20 dBm. Other features include:

* Low Power Operation : 13 mA at V_{CC}= 2.7 - 6.5 Vdc
* High Mixer Linearity: Input IP3 = + 3.0 dBm
* Single - Ended 50 Ω Mixer Input
* Double Balanced Mixer Operation
* Open Collector Mixer Output
* Single Transistor oscillator with Collector, Base and Emitter Pinned Out
* Buffered Oscillator Output
* Mixer and Oscillator Can Be Enabled Independently

Figure 2 - MC13142D Pin Connections

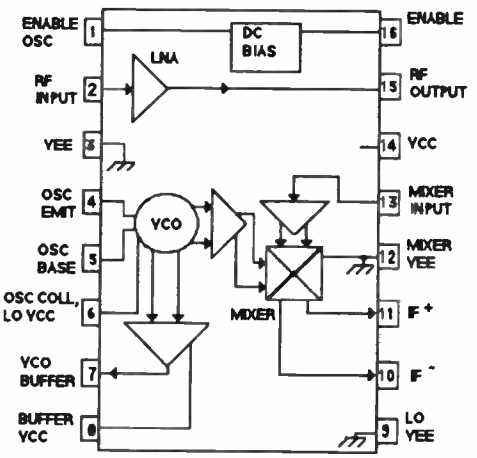
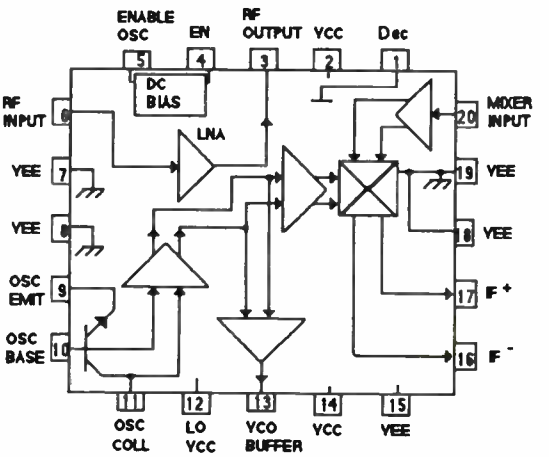


Figure 3 - MC13142FTB Pin Connections



Back end Receiver IC

The MC13150 [3] is designated for use as the back end in analog narrowband FM systems such as cellular, 900 MHz cordless phones and narrowband data links with data rates up to 9.6 kbaud. The MC13150 is a very low power single conversion narrowband FM receiver incorporating a split IF. It is comprised of a doubly balanced mixer, common collector transistor oscillator, extended range received signal strength indicator (RSSI), RSSI buffer, IF amplifier, limiting IF, an unique coilless quadrature detector and a device enable function (Refer to Figure 4, Simplified Block Diagram and Pin Connections). The following are key features of this unique IC:

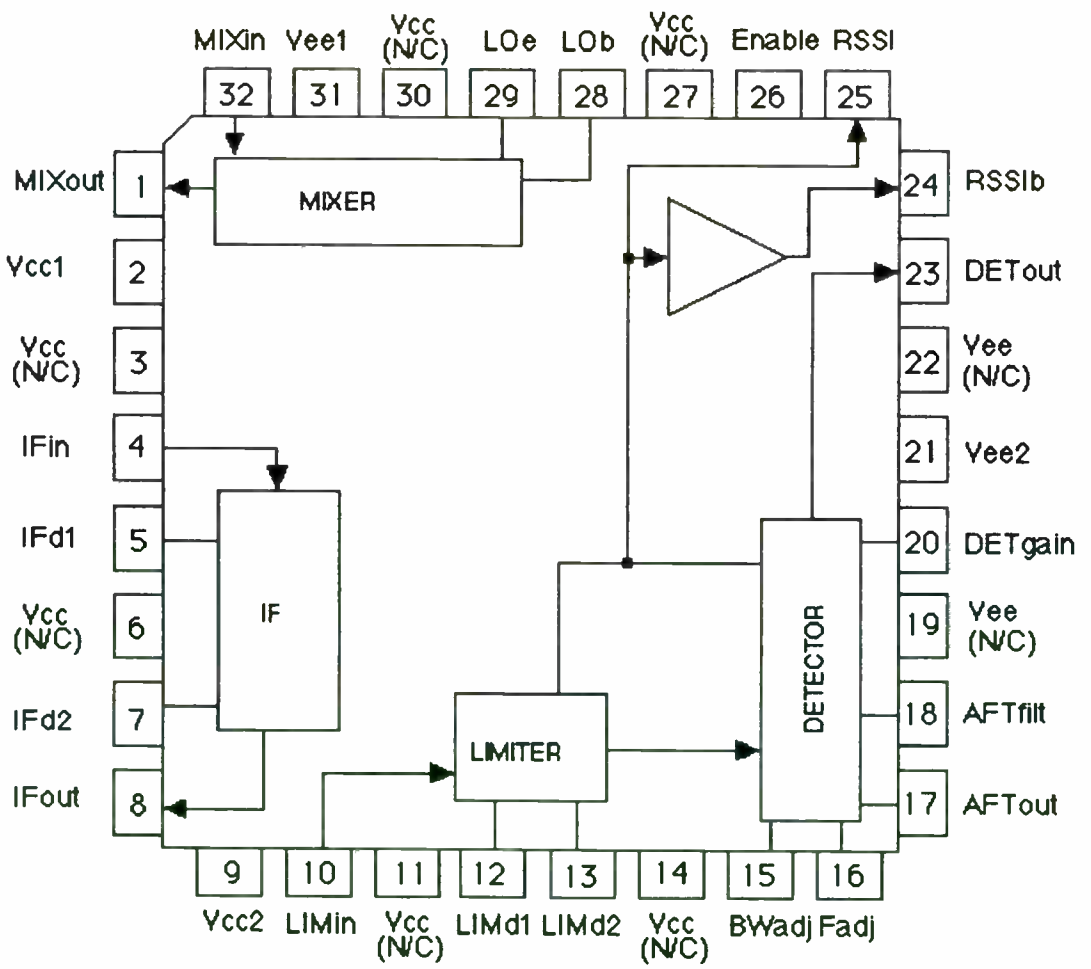
* Low Frequency Corner Adjustable to < 1Hz for Paging and Messaging Applications
* Low Current at 1.7 mAdc at 2.3 to 6.5 Vdc
* 110 dB RSSI Dynamic Range
* 12 dB SINAD Sensistivity = -100 dBm
* Available in 32 and 24 Pin TQFP Packages

The MC13150 Advance Information data sheet contains details on the IC description and applications.

The MC13175D [4] UHF PLL System is used as the 1/8 Prescalar and Phase Detector for the 2nd LO PLL. Other ICs include the MC33111 [5] Compander , MC33269-3 [6] 3.3 V, Low Dropout Reguator (LDO), MC145220 [7] Dual PLL Synthesizer. MRF944L [8], RF Low Noise transistor.

* Unique Coilless Detector

Figure 4 - MC13150FTB Block Diagram and Pin Connections



Receiver System Design

LNA/ 1st Mixer

Figure 5 , Block Diagram of the Receiver System shows the implementation of the front-end and back-end ICs. In this receiver a discrete LNA, MRF9411L is used before the MC13142 to improve sensitivity. A detailed noise analysis follows supporting this conclusion.

Figure 5 - 926.5 MHz Receiver System Block Diagram

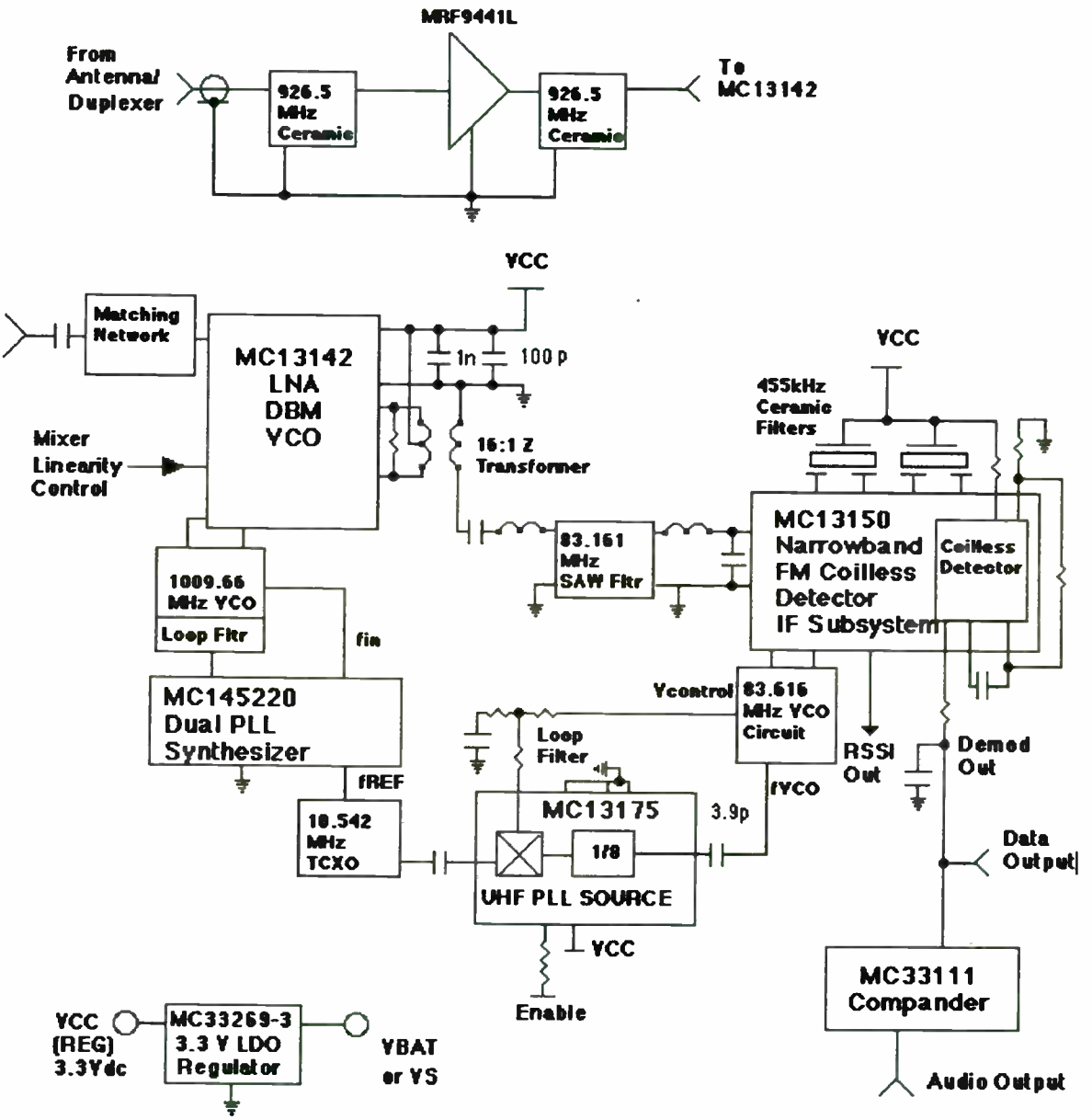
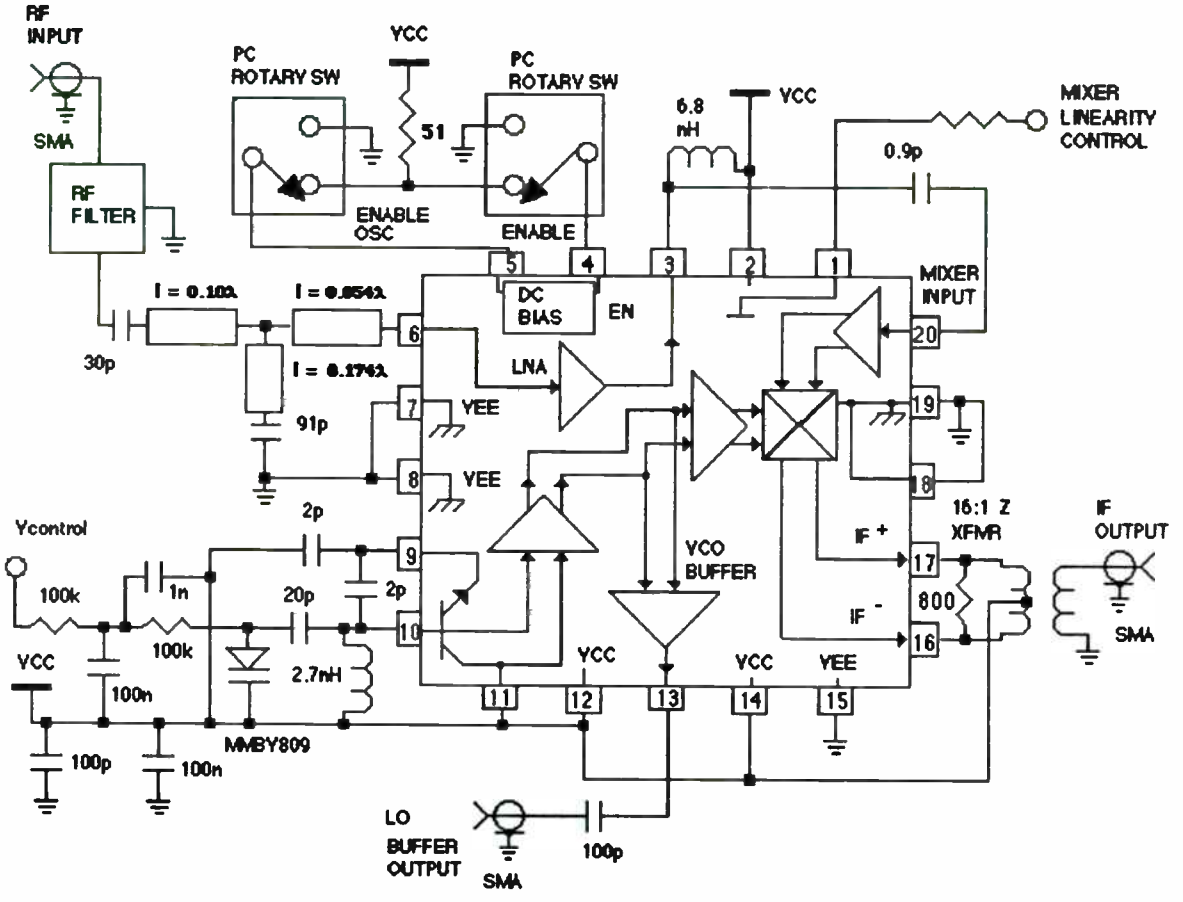


Figure 6 - MC13142FTB Front-End Receiver Circuit



Front End IC

The front end IC circuit is shown in Figure 6. The matching network is optimized for noise figure, gain and input VSWR. Small signal scattering parameters and noise parameters are found in the IC data sheet. An RF filter is used before the LNA and mixer to provide image rejection. A variety of filters - SAW, ceramic and dielectric are offered by many manufacturers such as Toko, Motorola, and Murata. Both Toko (Part # 4DFA-926A-11 at 926.5 MHz & Part # 4DFA-904A-10 at 904.5 MHz) and Motorola (Part # KFF6140A at 906.5 MHz & Part # KFF6141A at 926.5 MHz [9]) make ceramic filters for 902-928 MHz Part 15 applications. The above filters have 3 dB bandwidths of 2 MHz .

IF Output Matching

The IF output is converted to 50 Ω via a 16:1 impedance transformer. The transformer provides dc through its center tap on the high side; 800 Ω is used across the high side to set the impedance for the 16:1 transformation to 50 Ω. Following the mixer IF output is an IF preamplifier which is optional. The IF preamp provides additional gain with low noise figure and is used to lower the secondary noise figure contribution of the back-end portion of the receiver system. A receiver noise analysis is presented later which shows the results with and without the preamp (see Table 1).

The 1st IF is chosen at 83.16 MHz since manufacturers such as Toko (Part # SWS.83GBWA) and Murata (Part # SAFC83.161MA40X) offer surface mounted SAW filters with high attenuation at f_C ±910 kHz. This 1st IF filter is designed to provide at least 60 dB of 2nd image rejection in a typical narrow band FM receiver with a 455 or 450 kHz limiting IF.

1st Local Oscillator

The 1st Local Oscillator is PLL controlled with a MC145220 dual PPL synthesizer. The MC13142 has an on-board transistor with the emitter base and collector pinned out . Figure 8 shows the VCO circuit which uses a common collector configuration. The following equation is used to calculate the center frequency of the varactor controlled oscillator at a nominal 2 volt control voltage:

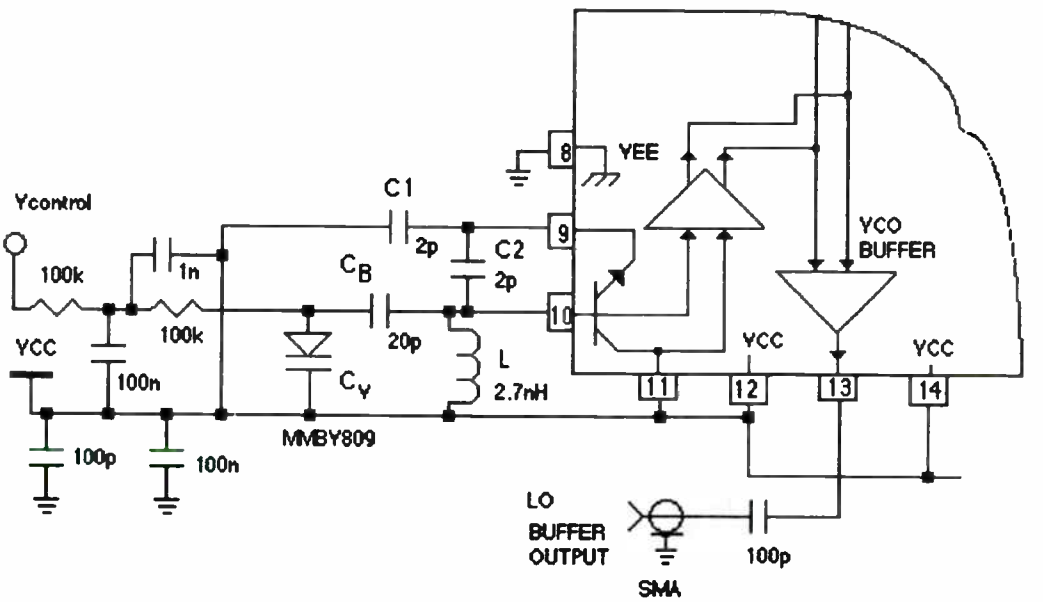
$$f_{osc} = 0.159 \{L [(C1C2/(C1+C2))+ (C_V C_B/(C_V+C_B))+ C_p]\}^{-1/2}$$

where C_p is the parasitic capacitance of the IC and PCB layout; C_p is typically 4 pF.
The sensitivity may be adjusted by changing CB; if CB >> Cv, then Cv dominates and the VCO sensitivity is maximized; thus,

$$C_V C_B / (C_V + C_B) \sim C_V$$

If CB ~ Cv, then the effect of Cv is minimized and the VCO sensitivity is minimized.
The parasitic capacitance , Cp, is minimized by keeping the interconnects short and maintaining small component mounting pads. Components should be chosen that are high Q having minimum parasitics. The Q of the inductor is important to maintain phase noise performance and power developed in the VCO. Also, the varactor should have sufficient Q at the VCO frequency; the MMBV809 offers high Q (150) with 6pF at 2 volts.
Thus, the nominal center frequency of the VCO with 2 volt varactor controlled voltage is calculated to be 1003 MHz; the required LO center frequency is 1009.661 MHz.

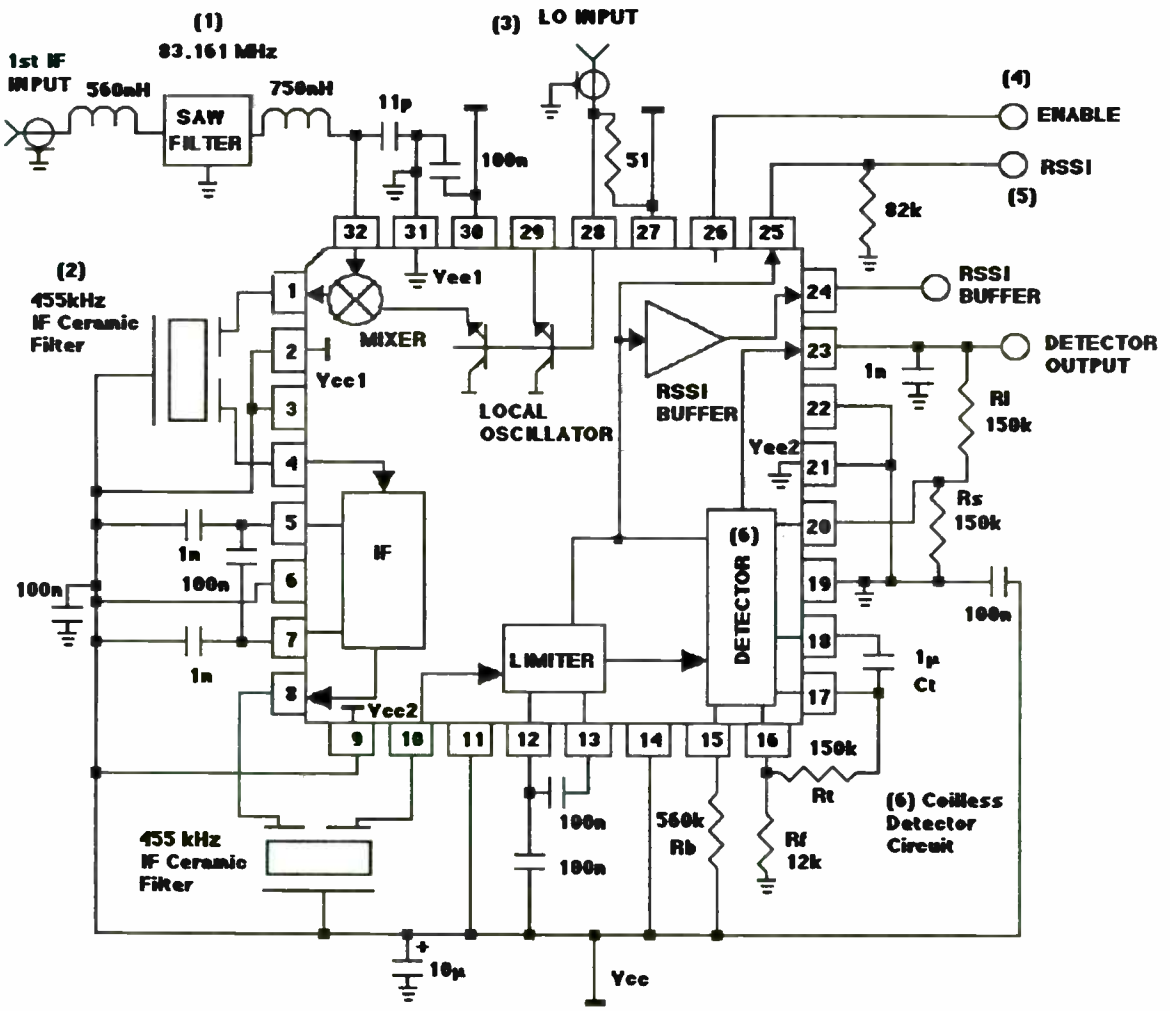
Figure 7 - 1st Local Oscillator "VCO" Circuit



Back end Receiver IC

The backend function of the receiver makes use of the unique coilless detector in the MC13150 (see Figure 8 - Back-end Receiver Circuit). The coilless detector external circuit design (pins 15 to 22) is explained in detail in the IC data sheet. When the external components are properly chosen, no detector tuning is required in production manufacturing.

Figure 8 - Back-end Receiver Circuit



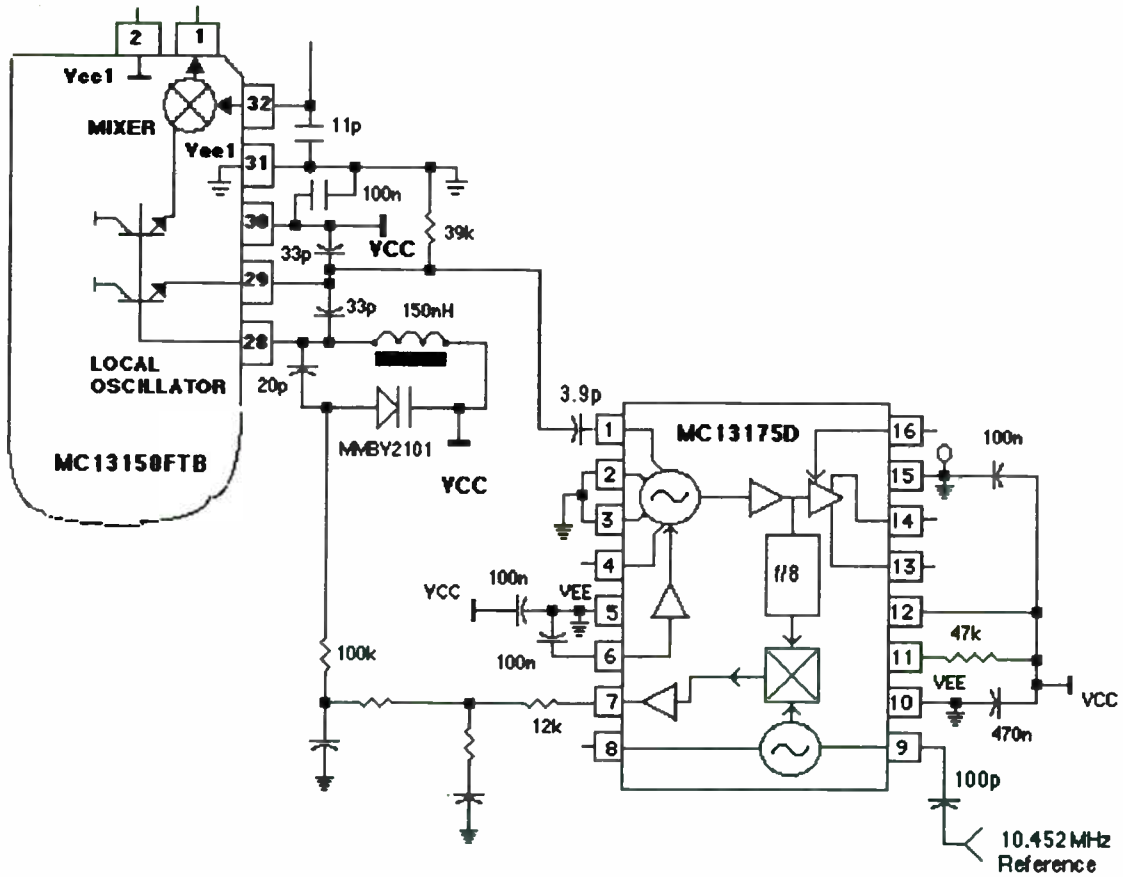
NOTES:
(1) SURFACE MOUNT SAW FILTERS AT 83.16 MHZ IF CENTER FREQUENCY REQUIRED A SERIES INDUCTOR ON THE INPUT AND OUTPUT TO MATCH TO 50 Ω. TOKO AND MURATA ARE EXCELLENT SOURCES FOR THESE FILTERS.
(2) 455kHz CERAMIC FILTERS (SOURCE MURATA CFU455 SERIES WHICH ARE SELECTED FOR VARIOUS BANDWIDTHS).
(3) FOR EXTERNAL LO SOURCE, A 51 OHM PULL-UP RESISTOR IS USED TO BIAS THE BASE OF THE ON-BOARD TRANSISTOR AS SHOWN IN FIGURE 9.
DESIGNER MAY PROVIDE LOCAL OSCILLATOR WITH 3RD, 5TH, OR 7TH OVERTONE CRYSTAL OSCILLATOR CIRCUIT (SEE IC DATA SHEET FOR DETAILS).
(4) ENABLE IC BY SWITCHING THE PIN TO VEE.
(5) THE RESISTOR IS CHOSEN TO SET THE RANGE OF RSSI VOLTAGE OUTPUT SWING.
(6) DETAILS REGARDING THE EXTERNAL COMPONENTS TO SETUP THE COILLESS DETECTOR ARE PROVIDED IN THE APPLICATION SECTION OF THE IC DATA SHEET.

2nd Local Oscillator

The 2nd local oscillator is at 83.616 MHz; it may be either crystal controlled using a 5th overtone crystal as shown in the MC13150 Idata sheet or PLL controlled in which case the master PLL reference oscillator is used. This latter method eliminates an expensive overtone crystal and the required tuning to ensure lockup. Since the master PLL reference oscillator is a narrowband FM system which uses a very stable TCXO having 1-2 ppm frequency tolerance and 1 ppm/year aging, tuning of the reference is not necessary.

The MC13175 may be used to implement the 2nd L.O. by using its fixed divide by 8 prescalar and phase detector. The 10.452 MHz reference is ac coupled at pin 9. The phase detector output at pin 7 is used to drive a passive loop filter which drives an external varactor controlled LC tank circuit at pins 28 and 29, the internal common collector transistor oscillator. The VCO circuit for the 83.616 oscillator is shown in Figure 9. Implementing the 83.616 MHz oscillator in this way offers appreciable savings in material and engineering cost while providing better system frequency stability and performance.

Figure 9 - 83.616 MHz VCO (2nd LO)



System Noise Analysis

The system noise analysis compares several possible configurations using a public domain software application published by HP called AppCAD. A summary of the system noise figure, overall gain, Iinput 3rd order intercept point (IIP3), IMD and SINAD is presented in Tables 1 and 2.

Front-end Noise Analysis

Noise analysis of the front end and back end IC circuits are done separately based on the performance characterization of the ICs. Figure 10 shows the model used for the MC13142. A low noise amplifier (LNA) MRF9411 (Figure 11) is used to improve the front-end noise performance. Design of the matching network is detailed in a paper by Nagaraj Dixit in March 1994 [10]. Noise performance with and without this discrete device is shown in Table 1 (see circuit examples 1 and 2). Although using the discrete transistor requires a few more external components to match and interface with the MC13142, it is preferable for the following reasons:

1) Provides better overall system noise figure and SINAD performance due to added gain and lower noise figure.

2) Improves reverse isolation of the LO at the antenna port. While the TQFP package is excellent and is appreciably better than the SOIC package, it only provides 45 dB maximum isolation between any two pins.

The additional LNA circuit preceeding the MC13142FTB, improves the reverse isolation by the contribution of the discrete transistor and the RF bandpass filters. The RF LNA provides improvement in noise performance while it reduces the IIP3. The RF ceramic or SAW preselector filter contributes to 1.5 to 3.8 dB insertion loss; this adds directly to the system noise figure, but the filter is necessary to provide 1st image frequency rejection.

Figure 10 - Noise Analysis Diagram of MC13142 with/without MRF9411L Preamp

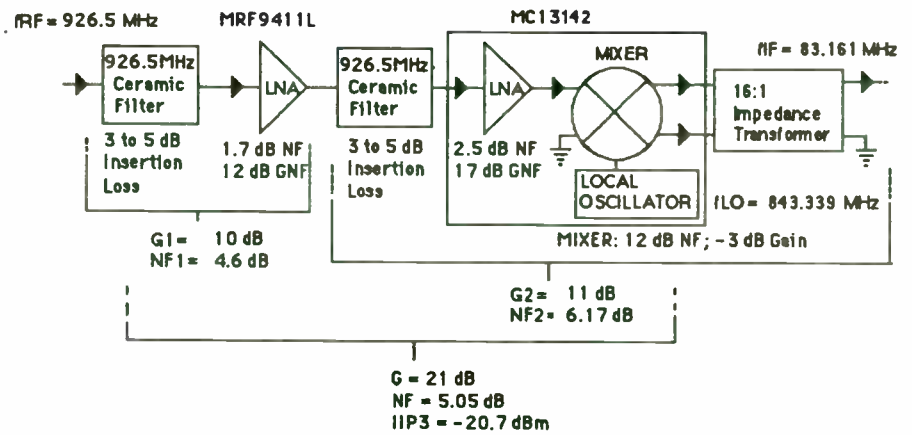
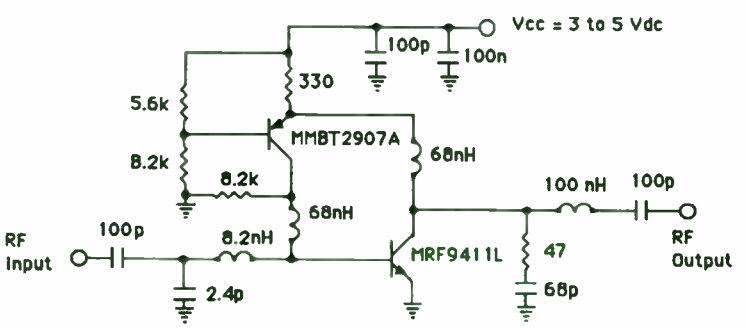


Figure 11 - MRF9411L RF LNA



Back End Noise Analysis

Figure 12 shows the noise model of the MC13150 at 83.16 MHz using the 1st IF SAW filter specified in the application. Performance is shown with and without a preamp as done in the MC13142 analysis. Examination of the data in the Table 1 (Circuits 3 & 4) clearly shows the performance tradeoff with and without an IF preamp. The noise figure improves from 21.8 dB without the preamp to 6.3 dB with the preamp.

Figure 12 - Noise Analysis Diagram of MC13150 Backend with/ without IF Preamp

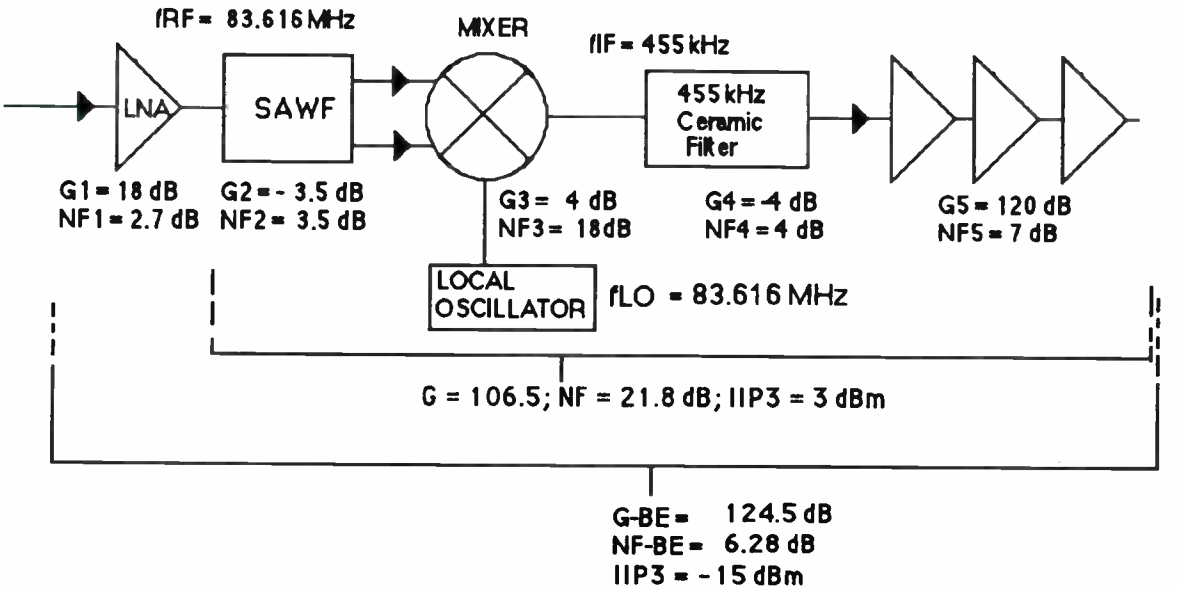


Figure 13 - MRF9411L IF Preamp

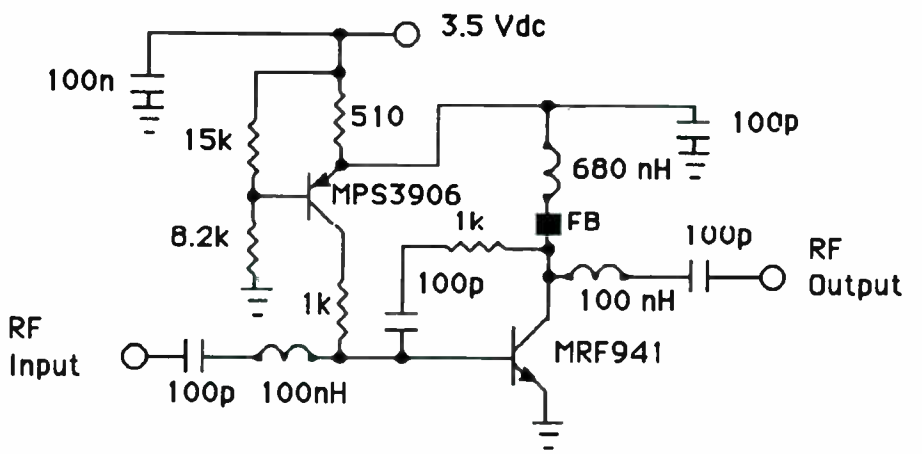


Table 1 - Noise Analysis Front-end and Back-end Circuits

Input Power = -30 dBm

Circuit Reference Number	Circuit Configuration Description	Cascaded Gain (dB)	Cascaded NF (dB)	Input IP3 (dBm)	Minimum Detectable Signal (dBm)	Output IP3 IM3 O/P Level (dBm)
1 (Figure10)	MC13142 w/o Preamp	11.0	6.17	-10.6	-104.8	0.36 -57.7
2 (Figure10)	MC13142 w Preamp	21	5.05	-20.7	-105.9	0.34 -27.7
3 (Figure12)	MC13150 w/o Preamp	106.5	21.8	3.0	-107.4	109.5 10.5
4 (Figure12)	MC13150 w Preamp	124.5	6.28	-15	-122.9	109.5 64.6

Table 2- Noise Analysis of System Receiver Comprised of Front-end and Back-end Combinations

Input Power = -30 dBm

Circuit Reference Number	Circuit Configuration Description	Cascaded Gain (dB)	Cascaded NF (dB)	Input IP3 (dBm)	Minimum Detectable Signal (dBm)	Output IP3 IM3 O/P Level (dBm)
1 + 3	MC13142 w/o Preamp MC13150 w/o Preamp	117.5	12.07	-12.5	-117.1	105 52.56
1 + 4	MC13142 w/o Preamp MC13150 w Preamp	135.5	6.43	-26.1	-122.7	109.4 97.7
2 + 3	MC13142 w Preamp MC13150 w/o Preamp	128	6.42	-22.7	-122.8	105.3 83.4
2 + 4	MC13142 w Preamp MC13150 w Preamp	145.5	5.08	-36.1	-124.1	*109.4 127.7

* Note that intermod products exceed the output intercept point in this example.

Cascaded Receiver System Noise Analysis

The front end and back end circuits in Table 1 are cascaded together in four possible combinations. Table 2 shows the analysis of overall gain and noise figure, receiver sensitivity, intermodulation and intercept point performance. The receiver system comprised of the MC13142 with an external preamp and the MC13150 with no external preamp is chosen over the others because it offers the best overall performance. The cascaded noise figure and sensitivity are optimized while maintaining reasonable third order intercept point and intermod performance. The worst peformances for IIP3 and intermod are when preamps are used with both the front end and back end ICs. At -30 dBm input power level, the output intermod exceeds the output IP3.

Performance Criteria

The receiver outlined in Figure 5 has the following performance:
> System Noise Figure is typically 6.5 to 7 dB
> 12 dB SINAD performance - 116 dBm to -118dBm.
> Input Third Order Intercept Point of -23 dBm
> 2nd Image Rejection > 70 dB
> RSSI Dynamic Range of Typically 100 dB

Other Design Considerations

Component Selection

Component selection is a critical issue in RF circuit design. Components used in these radio and wireless systems must be well characterized and must be consistent from lot to lot. The Q and tolerance of the components used in fixed tuned circuits should be tightly specified . Of the several manufacturers of RF SAW and dielectric bandpass filters for cellular and cordless phone applications, the specifications for maximum insertion loss are somewhat relaxed and varied. If the RF preselector filter has wide and uncertain specification limits, this will adversely affect the receiver system performance since the preselector filter insertion loss adds directly to system noise figure. These filters are optimized for 50 ohm load and source terminations; it is important that the interface matching is implemented correctly and that it can be repeated in a production manufacturing environment .

PCB Layout

In RF circuit design, controlled impedance lines are used to reduce lump component count and to reduce manufacturing cost. Microstrip techniques are successfully used in 900 MHz RF circuit design. The ICs specified in this receiver are all surface mount components; a very compact layout using these ICs and other surface mount passive components is realized. The demonstration receiver PCB is an example of good RF layout and grounding practices. Chapter 8 of the Analog IC data book discusses the criteria for for good RF layout.

FCC Regulation and Approval

The receiver system discussed in this paper is not considered a final product nor is is approved by the FCC. It is the responsibility of the manufacturer to obtain the acceptance and the licenses required by the Code of Federal Regulation (CFR Title 47) to manufacture and market a radio frequency product. The main purpose of this paper is to help the radio designer in his quest with design techniques, application solutions and recommendation of suitable semiconductor and passive components that achieve the performance criteria of the wireless communication system.

References

1 Code of Federal Regulations, Title 47, U.S. Government Printing Office, Washington, 1994, Part 15 & 95.

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3 MC13150/D, Motorola Semiconductor Technical Data, Motorola, Inc., Tempe, AZ, 1995.

4 MC13175/D, Motorola Semicondutor Technical Data, Motorola, Inc., Tempe, AZ,1992.

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6 MC33269/D, Motorola Semiconductor Technical Data, Motorola, Inc., Tempe, AZ, 1994.

7 MC145220/D, Motorola Semiconductor Technical Data, Motorola, Inc., Tempe, AZ, 1994.

8 MRF9411/D, Motorola Semiconductor Technical Data, Motorola, Inc., Tempe, AZ, 1994.

9 KFF6141A Ceramic Bandpass Filters Data, Motorola Components Division, Motorola, Inc., Albuquerque, NM, 1994.

10 Dixit, Nagaraj V., "Design and Performance of a Low Voltage, Low Noise 900 MHz Amplifier", *RF Design,* March, 1994, Argus Business, Skokie, IL, pp. 48-53.

An Integrated Low Cost High Efficiency Power Amplifier for Analog Cellular Applications

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I. Introduction

Cellular radio is by far the most successful example of the wireless revolution. With over 77 million subscribers world wide predicted by the end of 1995, cellular phone service is available on every continent.

While there is much activity in the area of digital cellular technology, 24 million analog cellular handsets are predicted to be produced in 1995 with continued demand over the next few years.

This paper presents one in a class of analog integrated power amplifiers either currently being offered or in design by Motorola's Communications Semiconductor Products Division RFIC Operation, the MRFIC0911.

II. Analog Cellular Power Amplifier Requirements

Table 1 compares the requirements for various analog cellular systems around the world. The main differences from an RF amplifier standpoint are the frequencies.

STANDARD	AMPS	ETACS	NTACS	NMT900
MOBILE RX FREQ (MHz)	869-894	916-949	860-870	935-960
MOBILE TX FREQ (MHz)	824-849	871-904	915-925	890-915
MODULATION	FM	FM	FM	FM
PORTABLE ANT POWER (W)	0.6	0.6	0.6	1
MOBILE ANT POWER (W)	3	3	3	6
PA LINEARITY	N/A	N/A	N/A	N/A
CHANNEL SPACING (kHz)	30	25	12.5	12.5
NUMBER OF CHANNELS	832	1000	400	1999
DUPLEX METHOD	FDD	FDD	FDD	FDD

Table 1. International 900 MHz Analog Cellular Standards

Figure 1 is a block diagram of the analog portion of a typical analog cellular phone. Analog cellular grew out of land mobile radio and, as such, uses constant envelope, narrow band FM modulation and frequency domain duplexing. The handset transmitter is always on during a phone call. Since average and peak transmit power are the same, amplifier efficiency is critical to handset talk time. Fortunately, the constant envelope FM modulation favors operation of amplifiers in saturation thus enhancing amplifier efficiency. Also an artifact of FDD is the need for low noise and signal power in the receive band less the transmitter de-sense the receiver.

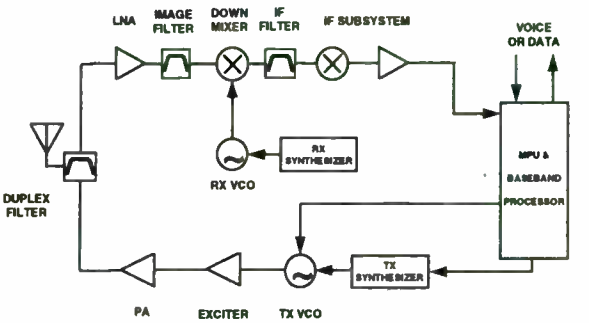

Figure 1 Simplified FDD Radio Block Diagram

GaAs amplifiers offer high efficiency through the improved carrier mobility of the semiconductor material. Integrated GaAs IPAs are offered by several manufacturers including Motorola but have the disadvantages of relatively high cost when compared with discrete solutions and silicon IPA and most require negative gate voltage. Analog cellular is a mature service with low, medium and high tier products. For low and medium tier phones, many manufacturers prefer the cost advantage of silicon solutions over the higher efficiency of GaAs.

DESIRED FEATURES OF AN ANALOG CELLULAR INTEGRATED POWER AMPLIFIER

LOW COST - $3 TO $5
SMALL SIZE
1.4 WATT OUTPUT
HIGH EFFICIENCY - >50%
45 dB DYNAMIC RANGE POWER CONTROL
BIAS AND MATCHING CIRCUITS ON CHIP
RUGGED AND STABLE INTO 10:1 VSWR MISMATCH
LOW RECEIVE BAND NOISE POWER

Figure 2

Depending on how one assesses manufacturing cost, discrete power amplifiers can have a cost advantage over power modules and integrated power amps. But manufacturability can often be an issue. Integrated power amplifiers improve manufactuability through reduced parts count and the repeatability that can be had from monolithic circuit technology.

Features desired in a integrated power amplifier are summarized in Figure 2.

III. Motorola's Lateral MOSFET Process

Silicon MOSFET technology has been employed for several decades in RF applications.[1,2,3] Most of these devices have vertical structures as shown in Figure 3.

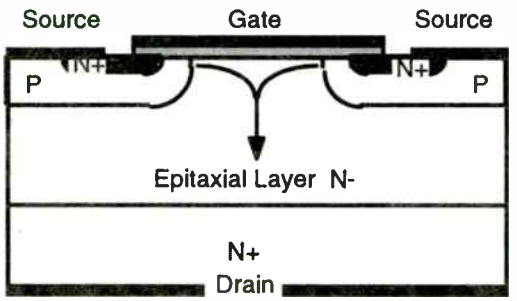

Figure 3. Simplified Vertical RF MOS Structure

More recently, lateral structures, sometimes called LDMOS, which are based on CMOS technology, have been adapted to RF applications.[4,5] As shown in Figure 4, this structure allows for drain, gate and source contacts to be on top of the die. Vertical MOS structures have the drain contact on the back of the die. The source contact, which is usually grounded, can be contacted to the back of the die as shown through a P+ sinker, thus reducing ground inductance. For discrete devices, these features allow the elimination of insulating material under the die thus reducing package costs. For integrated applications, the drains and gates are available on the top of the die allowing for easy cascading of common source stages.

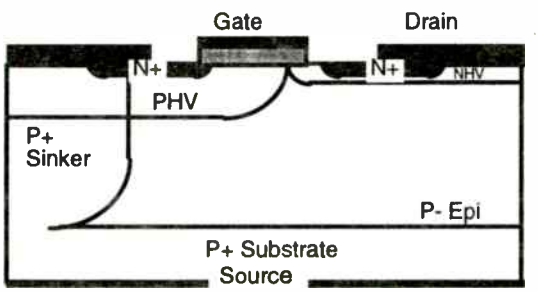

Figure 4. Simplified Lateral RF MOS Structure

The gate length chosen for Motorola's LDMOS IC process is 1.5 micron. From a manufacturing point of view, the LDMOS structure offers the low cost and maturity of silicon MOS technology. Equivalent bipolar IC processes are much more costly due to the increased complexity of the bipolar structure.

IV. Packaging Considerations

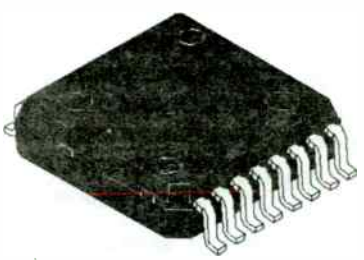

Figure 5. PFP-16 Package - 7 mm X 7 mm

As mentioned earlier, analog cellular transmitters operate at a constant output power. At 31.5 dBm output and, at 50% efficiency, the power amplifier will dissipate 1.4 Watts. This power level must be considered in the IPA design. Standard IC packages are rated at near one Watt dissipation when tooled with special leadframes. To ensure reliability, Motorola has adapted a package currently qualified for automotive use, the QFP-32 with a copper slug, to use for IPAs. Designated the PFP-16, this package has improved thermal performance over standard IC packages because heat is conducted down through the copper slug which is soldered to the printed circuit board instead of simply out through the leads. Additionally, the die is soldered instead of epoxied. The result is a thermal resistance of 4°C/W, junction to case, for the MRFIC0911.

V. Design Philosophy

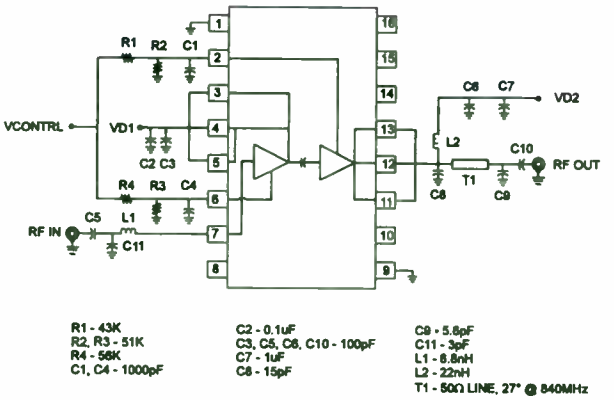

Figure 6. MRFIC0911 Applications Circuit

The MRFIC0911 is a two-stage class AB common source amplifier with interstage matching on chips. The LDMOS structure, as mentioned earlier, employs 1.5 micron gate for the FETs. The device sizes are 6 mm for the input stage and 24 mm for the output stage.

The primary goals for the design of the MRFIC0911 were high performance, minimal cost and maximum flexibility. Tradeoffs exist between these goals and are best illustrated in Figure 6 which shows a schematic of the MTFIC09111 along with its required external components.

All three goals dictate the use of an external load-line match. The most practical embodiment is to use two series-L shunt-C networks. The second inductor is most easily realized through a 50 Ω transmission line with 27° of electrical length at 840 MHz. A higher impedance line can be used to reduce board space.

The input match is done externally with a series 6.8 nH inductor followed by a shunt 3 pF capacitor. A high impedance transmission line can be used instead of a discrete inductor to reduce cost. Alternatively, the input match can be omitted altogether resulting in less than 1 dB on mismatch loss.

The interstage match is implemented on chip with a DC blocking capacitor and a shunt inductor. To save die area, the shunt inductor is realized through the bondwire and lead inductance of the first stage drain bias feed.

All analog cellular PAs require a means of adjusting the output power in a closed loop. There are two main methods; drain control and gate control. Drain control is usually done by varying the drain voltage of the driver stage. Normally, a pass device is used to buffer the loop from the large drain current. Gate control is usually done by varying the gates of both stages through a resistive divider. There are several advantages to using gate control. The efficiency is much higher at lower power levels since the gate bias voltage is being reduced. Additionally, a pass device is not needed since the gates do not draw appreciable current. Since bias currents are controlled by the loop it is not necessary to set quiescent currents. As an added advantage of integration, since both stages are on the same die, there is threshold voltage tracking which negates the need for threshold correction which is commonly needed in discrete solutions.

VI. Performance

The performance of the MRFIC0911 in the circuit configuration shown in Figure 6 is shown in Figures 7 through 9. Since cellular power amps tend to operate at a constant input power, these charts display data taken at an input drive of 13 dBm. Figure 7 shows the dynamic range obtainable with the power control scheme shown in Figure 6. Figure 8 shows the output power and power added efficiency over a narrow range of VCNTRL. Normal "full output" VCNTRL is about 4 V. Figure 9 shows the performance over the AMPS cellular subscriber 824 to 849 MHz band.

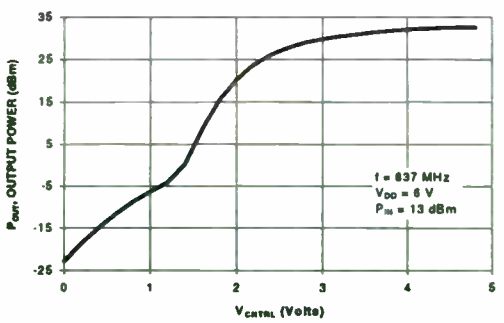

Figure 7. Output Power versus VCNTRL

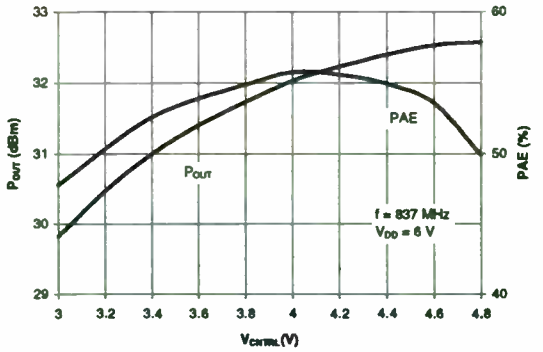

Figure 8. Pout and PAE versus VCNTRL

Operating Frequency	824 - 905 MHz
Supply Voltage	5.5 - 6.5 Volts
Pout at Pin = 13 dBm	31.5 min.
Noise Power at 45 MHz Offset in 30 kHz Bandwidth	-92 dBm max
Total Supply Current at Pout = 31.5 dBm	470 mA max

Table 2. MRFIC0911 Key Performance Parameters

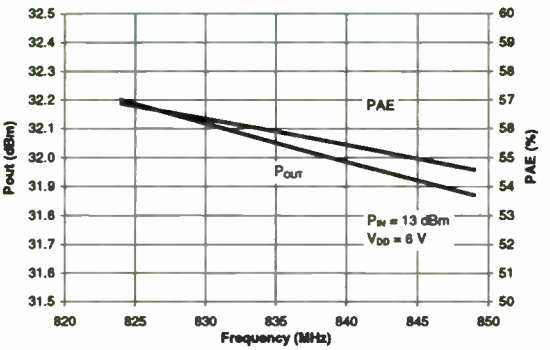

Figure 9. Pout and PAE versus Frequency

VII. Conclusion

A cost effective silicon MOSFET integrated power amplifier has been presented. It displays greater than 50% power added efficiency at 31.5 dBm output power when operated at 6 Volts in the 900 MHz cellular band in FM applications.

The MRFIC0911 is one in a family of silicon and GaAs integrated power amplifiers Motorola is introducing for 900 MHz cellular applications.

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[1] Roy Hejhall, "VHF MOS Power Applications", Motorola Semiconductors Application Note AN-878.

[2] Dick Moss, "ISOFET Evolution Yields High-Power Devices", Microwaves & RF, Feb. 1983, pp. 91-94.

[3] Ed Oxner, "Meet the V-MOSFET Model", RF Design, Jan/Feb 1979, pp. 16-22.

[4] H. Itoh, T. Okabe, M. Nagata, "Extremely High Efficiency UHF Power MOSFET for Handy Transmitter", IEDM Tech. Digest, 1983, pp. 95-98.

[5] N. Camilleri, et al, "Silicon MOSFET'S Wireless Technology for the 90's", Applied Microwaves & Wireless, Vol. 5, No. 4, Fall 1993, pp. 42-57.

Power Control Considerations for Personal Wireless Systems

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Battery operated communications will account for nearly 90% of all personal wireless systems produced by the year 2000. Battery life will be a key product differentiator for personal communication system terminals. There are a variety of techniques that can be used by the system designer to implement an overall power management strategy. This paper will discuss some of the techniques used in the areas of system, silicon and software design.

I. Introduction

Personal Communications Service (PCS) in the United States has been in the planning stages for over 6 years. PCS promises to provide the capability of being able to communicate with anyone, without regard to the person's location or the time of day. This is commonly referred to as "anytime, anywhere, to anyone" communications and is the grand vision for PCS. According to the vision, communications will be accomplished with small, lightweight multi-function portable phones and other subscriber terminals capable of communicating images and other two way data. This increased dependency on portable wireless communications will place greater demands on terminal manufacturers to produce small, light weight units with battery life greater than what is currently available. A key differentiator for manufacturers will be the length of time the terminal can operate between charges, in both standby and active mode, and the amount of charging cycles before the battery must be replaced.

Industry analysts expect that early PCS services, those which might be offered in late 1996, will look very much like, and be in competition with, current cellular services. This class of service is generally referred to as "high-tier". High tier systems are characterized by the following attributes:

1) Macro cell based system providing vehicular corridor coverage.

2) Speech quality that is below "toll" quality. This is due to the low bit rate vocoders that are used in these systems.

It is expected that high-tier subscribers will account for the majority of PCS service revenues in the period up to 2000. Beyond 2000, the largest percentage of revenues will be from hybrid services.[1] Hybrid services are those which allow a single handset to function as a cordless phone within the home and a cellular phone when outside the range of the home base station. In order to accomplish this, some hybrid handsets will incorporate multiple air interface standards, such as GSM/DECT. Most of the digital standards that will be used in PCS terminals share a common element in that they use modulation technologies requiring linear amplification. This requirement necessitates the use of class A or AB

[1] BIS Strategic Decisions

RF amplifiers which are not as efficient as the class C amplifiers used for narrow band analog FM systems. These and other factors create challenges for the designer of battery operated wireless terminals. These factors are summarized below:

1) The use of battery operated wireless terminals will increase as PCS evolves.

2) Our dependence on wireless devices will increase as they become more ubiquitous.

3) Multiple service tiers deployed in the PCS networks will require terminals to be flexible and powerful enough to implement multiple air-interface standards.

4) Demand for additional user features, better voice quality and increased system capacity will necessitate the need for more powerful baseband processing devices.

This paper will discuss techniques that can be used to minimize system power consumption, and therefore maximize battery life in portable wireless terminals. The discussion will be facilitated by presenting a baseband architecture that is flexible enough to accommodate the inevitable changes that will occur in PCS standards.

II. System Architecture

In architecting next generation wireless systems, designers must make tradeoffs between cost, flexibility and power consumption. Cost is the first concern of wireless subscriber handset designers, followed by performance (including flexibility and power consumption). Flexibility is an important attribute for PCS terminals because of the fragmented and dynamic nature of the standards proposed for PCS.
Consider the baseband processing section of a digital wireless terminal as shown in Figure 1. This platform consists of a PCM voice codec, a microcontroller (MCU), a digital signal processor (DSP) and an RF interface device. As shown, this device lineup performs all of the baseband processing required for an IS-136 based PCS terminal. IS-136 is an air-interface standard based on time division multiple access technology (TDMA) that can be used for both digital cellular radio at 800 MHz and PCS at 1900 MHz. As a PCS standard, it is designated as the TIA JTC Tag-4.

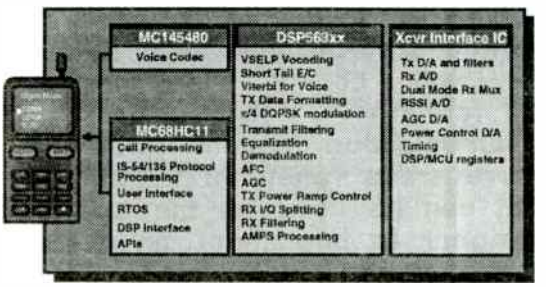

Figure 1: IS-136 Baseband Platform

Baseband processing platforms such as this must be able to execute the complex signal processing algorithms required for voice coding, channel coding and channel equalization in addition to the system control, user interface and call processing functions required in the standard. This requires the execution of many millions of instructions per seconds (MIPS). Unfortunately, higher MIPS rates usually mean higher clocking rates which in turn means higher power consumption.

III. Supply Voltage

A critical factor in the amount of power a system will consume is the supply voltage requirements of each of the devices in the system. In 1984, JEDEC established a standard for 3.3V battery operated systems. The shift from 5V to 3.3V systems has been slow, however, due to the lack of a complete portfolio of 3.3V semiconductor devices. This has changed over the past several years and the number of 3.3V portable systems has increased accordingly. This has several

advantages for the PCS terminal designer. The first major advantage is in power consumption. The power consumed is proportional to the square of the supply voltage. Operating a system at 3.3V results in a 40-50% decrease in power dissipation over a 5V system. The result is a system that will operate about twice as long between battery charges. Devices operating at 2.7V and below are available today so a migration path for even lower power units is evolving.

The second major advantage of lower supply voltage is in the weight of the system. Since the majority of the weight of a handset is typically in the battery pack, manufacturers usually offer a pack with less capacity to trade off talk time for weight. Systems operating at lower voltages can be lighter weight and still retain reasonable talk time.

IV. Device Architecture

As discussed above, semiconductor device supply voltage plays a critical role in the overall system power consumption. There are other gains to be made and these are dependent on hardware and software features of the specific devices used in the system. This discussion will refer specifically to the two main components of the baseband architecture shown in Figure 1. These are the MC68HC11xx microcontroller (MCU) and the DSP563xx digital signal processor (DSP) from Motorola. These two devices form the processing core of the IS-136 baseband processing unit.

A. MC68HC11

The MC68HC11 is an 8 bit MCU Family which includes over 60 different device types with a variety of on-chip peripherals supporting wireless applications. These devices are available in both 5V and 3V versions and have on-chip program memory up to 32K bytes. On-chip peripherals include A/D converters, timers, synchronous and asynchronous communications controllers, real time interrupts, chip selects, general purpose I/O and an external memory expansion bus.

In this example, the HC11 runs a real time operating system to manage the multitude of tasks involved with the call processing and user interface functions in a wireless PCS terminal. These tasks include call establishment, registration/authentication, call operation, call release, channel scanning, transmitter control, call handoff, digital control channel signaling and protocol processing, plus user interface functions such as keypad/button monitoring, menu scrolling, display driver, ringer control, audio path control and battery monitoring. During peak processing loads, like call establishment, the HC11 is running at its full operating speed. During idle time, when the unit is not receiving or placing a call, the HC11 can enter one of two low power operating modes. These modes are software controlled and allow the HC11 to operate at reduced power consumption levels.

1) WAIT Mode: The WAIT mode of operation is entered through the execution of the WAI instruction. This instruction causes the HC11 to prepare for the reception of an interrupt (wait for interrupt). The contents of the core registers are pushed on the system stack and the MCU enters a wait state for an integer number of clock cycles. During this time, the clock oscillator continues to run, but the fetching and execution of instructions stops. This results in fewer gates being clocked and is the reason for the reduction in supply current from the run mode of operation.

If all on-chip peripherals are shut down prior to the execution of the WAI instruction, a reduction in Idd of over 60% compared to the run Idd can be achieved. The actual savings is dependent upon which peripherals are active and the circuitry connected to the external pins. The wait mode is exited

upon the reception of an unmasked interrupt. This interrupt can be caused by an on-chip peripheral or from an external source. Upon exiting wait mode, the HC11 resumes normal instruction stream processing .
Since the clocks continue to run in this mode, the timer is also active and can be used to trigger the HC11 to resume normal processing. This is important for TDMA systems where the terminal needs to maintain a time base in order to synchronize with the system frame structure. The use of this mode requires advanced planning because it is software controlled. If the system requires an active time base, but has an idle period in which the instruction execution can be halted, the WAI instruction can be used to lower the average power consumption of the system. Further reductions can be realized by shutting down peripherals prior to entering the wait mode.

2) STOP Mode: STOP mode is the lowest power operating mode of the HC11. This mode is controlled with software by the execution of the STOP instruction. During the stop mode, all internal clocks are shut down, including the internal oscillator. All instruction processing is stopped as is all peripheral activity on the device. Because of the absence of a clock, the power dissipated in this mode is due entirely to leakage from high impedance CMOS gates. This mode is used when clocks are not required to be maintained and idle time is present. STOP mode is exited by a RESET or the external interrupts XIRQ and IRQ. Since the oscillator is stopped in the STOP mode, a restart delay of 4064 clock cycles may be required to allow oscillator stabilization. If the internal oscillator is being used, this delay is required; however, if a stable external oscillator is being used, a control bit will allow startup in only 4 cycles.

Specified Idd values for RUN (normal operation), WAIT and STOP are given in the table below:

Table 1: MC68L11E9 DC Electricals

Mode	Total Supply Current (Idd)	Comments
RUN	4 mA	
WAIT	1.5 mA	1
STOP	25 μA	

Notes: MC68L11E9 device, Vdd=3V, Single-chip mode

1) All peripherals shut down

The MC68HC11 is a Family of microcontrollers with a migration path to even higher performance. For those systems requiring a 16 bit data path and more sophisticated peripherals, the MC68HC16 Family provides an MCU architecture that is upward source code compatible with the HC11. The HC16 Family includes a library of peripherals such as timers, queued serial modules for autonomous serial transfers, A/D converters, chip selects and PLL clocking systems. The PLL clock system is particularly significant for low power systems since it allows very low power operation at KHz range frequencies while providing clocks necessary for system synchronization.

B. DSP56300

The core of the baseband processing section of the IS-136 terminal is a new digital signal processor from the Motorola DSP56300 Family. This family of 24 bit, fixed-point DSPs is code compatible with the DSP56000 series, but offers several major advantages for battery powered wireless communicators as discussed below.

The major features of the DSP56300 Family are:

- 66/80 MIPS with a 66/80 MHz clock
- 100% Object Code Compatible with the 56K core
- Fully pipelined 24 x 24 Bit Parallel Multiplier-Accumulator
- 56 Bit Barrel Shifter
- 16 Bit Arithmetic Support
- Highly Parallel Instruction Set
- Position Independent Code support
- Unique DSP Addressing Modes
- On-Chip Expandable Hardware Stack
- Nested Hardware Do Loops
- Fast Auto-Return Interrupts
- On-Chip Instruction Cache
- On-Chip Concurrent DMA Controller
- On-Chip PLL
- On-Chip Emulator (OnCE)
- IEEE 1149.1 JTAG Port

The DSP56300 core uses fully static CMOS technology which allows the clock to be shut off completely to save power. Additionally, two low power software modes, STOP and WAIT have been included. The design priorities for this family of DSPs are low cost, low power dissipation, high performance and high integration.

1) Hardware Architecture: The clock system in the DSP56300 core has been optimized for low power applications and uses a distributed power management scheme. The heart of the system is a phase locked loop (PLL) oscillator that allows software controlled dynamic throttling of the system clock frequency. This allows operation at reduced clock frequencies during periods of inactivity and full speed operation during peak processing conditions. There are many small clock generators throughout the chip that provide a clock to each of the on-chip peripherals and memory modules. These clocks can be individually gated off on a per clock cycle basis if the particular logic is not required for the current operation. For example, if a branch instruction is being executed, the data ALU block will not be clocked. The result is a device that consumes only enough power required for the current operation.

2) Software Architecture: Next generation portable wireless systems must have the processing power (MIPS) and flexibility (programmability) to adapt to changing standards and new user features. The DSP56300 Family offers a selection of programmable digital signal processors with a raw performance capability of 80 MIPS at 3.3V and 66 MIPS at 2.7V. This performance level is achieved through the use of a single clock cycle per instruction processing engine. Advanced power saving features designed into the architecture of these devices produce a family of digital signal processors that have one of the lowest mA/MIPS figure of merit in the industry. For the DSP56300 Family this figure is 1.4 mA/MIPS at 3.3V. The MIPS rating alone is not sufficient for determining a power vs performance figure of merit, however. This is due to the differences in the instruction set efficiency from one processor to the next. A processor Family, such as the DSP56300 ,which has been optimized for wireless applications, will be able to perform required algorithms with less power consumption than devices having less efficient instruction sets.

a) WAIT Mode: The DSP56300 core has a wait mode that is very similar to the wait mode on the HC11 MCU. This mode is entered upon execution of the WAIT instruction. During WAIT, the internal clocks to the processor core and memories are gated off and all activity in the processor is suspended until an unmasked interrupt occurs. The clock oscillator and the internal I/O peripheral clocks remain active. When an unmasked interrupt or external (hardware) processor RESET occurs, the processor leaves the WAIT state and begins exception processing of the unmasked interrupt or RESET condition

b) STOP Mode: The STOP mode is the lowest power operating mode of the DSP56300 core. When the DSP executes a STOP instruction, all clocks in the system are gated off. All activity in the processor is suspended until the device receives a RESET, DMA request or an IRQA interrupt. At that time, the DSP wakes up and begins processing according to the particular signal that caused the exit from STOP. If the IRQA interrupt caused the DSP to wake up, processing of the interrupt service routine will begin after an oscillator stabilization delay is executed.

The DSP56300 Family of DSPs provides the performance and power saving features for portable wireless applications. The 24-bit data path allows processing algorithms with minimal round off errors. Certain algorithms, such as the GSM vocoder, require bit-exact computations based on a 16 bit word size. These algorithms are executed using the 16 bit mode available on the DSP56300 core. Future Family members will offer a 16 bit data path. These devices will be based on the DSP56300 core architecture, but will have a reduced data bus width of 16 bits and deliver 66 MIPS of processing performance at 2.7V. The expected power/performance ratio for this device Family is below 1 mA/MIPS.

V. Power Management with MOSFET Switches

Some of the devices used in portable systems have a pin dedicated for power control. Applying the correct logic level causes the device to enter a low power "standby" mode. For those devices that do not have "standby" capability, external power MOSFETs can be used to control the voltage source to the device. Figure 2 shows an example using a P-channel MOSFET controlling the power amplifier in a portable system.

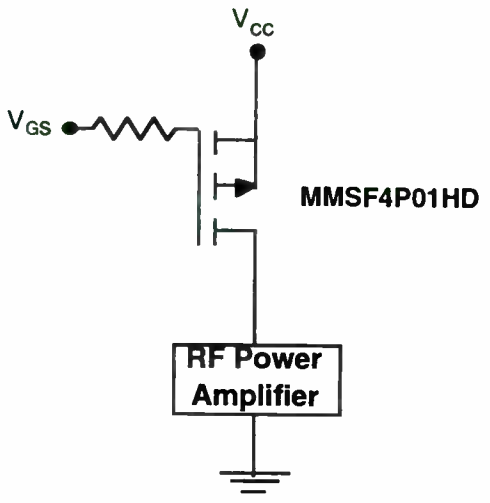

Figure 2: P-channel MOSFET used as a High Side Driver

During active periods when the terminal is in use, a control voltage is applied to the gate of the MOSFET. This logic level control voltage is typically provided by the control processor or other supervisory circuit. The gate voltage causes the MOSFET to turn on and provide a low resistance path between the power amplifier and V_{CC}. Since the total supply current for the power amplifier flows through the MOSFET RDS_{on}, it is imperative that this resistance be extremely low for power efficient operation. In this example, the Motorola MMSF4P01HD MOSFET is used. This device has a RDS_{on} of 110 mΩ at a gate voltage of V_{GS} = 2.7V. Increasing the gate voltage to 4.5V decreases RDS_{on} to 100 mΩ. If the power amplifier has a collector efficiency of 50%, it will require 2W of DC input power to deliver 1W of RF power to the load. At a supply voltage of 6V, the total supply current will be 333 mA and the power dissipated in the MOSFET will be 11 mW. The amount of power wasted in the MOSFET is directly proportional to RDS_{on}, so this becomes a critical parameter in device selection.

VI. Summary

This paper has presented some areas to consider when designing portable wireless systems for minimum power consumption:

• System supply voltage was shown to be a critical factor in system power consumption. The challenge lies in selecting devices that have the required performance at low voltage.

• Software power saving modes, such as WAIT and STOP, offer reduced power dissipation and must be exploited during periods of system inactivity.

• Advanced device architectures, such as the DSP56300 digital signal processor Family, employ sophisticated on chip PLL clocking systems . These systems allow full speed device operation with KHz speed oscillators and supply clocks only to those functional blocks that are required during a given instruction cycle.

• Power MOSFETs can be used to control supply voltage to the various functional blocks in the system. These functional blocks can be placed in standby mode, under control of the system microcontroller or power management circuit, when their use is not required for the current system operation.

As PCS evolves, our dependency on portable wireless devices will continue to increase. Battery life will be a key performance factor for portable PCS terminals and a differentiator for subscriber terminal manufacturers. System designers will be faced with designing subscriber terminals that are more complex while minimizing power consumption. Techniques such as those presented in this paper, must be applied to these future systems in order to meet the rising battery life expectations of the consumer.

Wireless Systems Improvements through Innovation and Integration

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Abstract

For successful wireless system cost improvements, innovative and integrated design are necessary. Managing a good balance of the two, along with a clever partitioning of the different system function blocks, is the challenge facing the wireless system designer. Examples of innovative and integrated designs are presented in this paper, along with some guidelines on system partitioning for Time and Frequency Division Duplex wireless systems.

I. Introduction

As cellular and PCS systems become consumer oriented, the price pressure on wireless terminals keeps increasing. The same quest for cost reduction is already well known by cordless phone manufacturers who have been serving a consumer type market for some time now. In this kind of market a 10 to 20% cost improvement per year is needed to stay competitive. Unlicensed frequency band cordless phones in the 50 and 900 MHz bands throughout the world have created the necessary critical mass market to allow IC suppliers to offer cost effective RF solutions.

The licensed band wireless services (cellular, land mobile radio, paging,...) at first did not feel the same kind of terminal price pressure. Often if not always, the real cost of a cellular phone is hidden to the end consumer by the service provider marketing strategy. But the fact that the cellular market is now consumer driven puts the same kind of pressure on continuing wireless terminal cost reduction. IC suppliers already serving the consumer wireless terminal type market will have an edge over other competitors because of their consumer market learning curve experience.

II. The I cube Formula

The I^3 formula is simple, and stands for Improvements through Innovation and Integration. As cost, cost, and cost are the three main drivers of any new or re-design of a radio subsystem, improvements here can indeed be read cost improvements.

Adequate performance is a prerequisite, but not a winning factor over price. Second order improvements which will still help win a design slot are power savings (the war on current drain in any portable equipment is just starting). Power savings could also translate into cost savings if there are significant enough to allow battery type changes or cell capacity reduction. A smaller form factor will also be a second order type improvement. It will allow the wireless terminal industrial designer to be more creative, by inventing new terminal shapes. For instance stand up cordless phones will benefit greatly from a compact electronic design, allowing the handset to come through the base station printed circuit board area. The electronics will then reside on the peripheral area of the base PCB.

So how to cut costs ? Integration almost always comes to mind first. The whole electronic industry is driven by greater and greater levels of integration, and wireless terminals are no exception. High performance and cost effective semiconductor technology is a must to

provide high level of integration. A mixed mode BiCMOS process will allow integration of analog, digital and RF functions on a single IC, while GaAs or high performance bipolar process will help integrating the most difficult part of the radio subsystem. These capabilities will usually be found in large companies with enough resources to invest in leading edge semiconductor processes, but smaller companies can still compete. There is another way to cut costs; through innovative design techniques. Changing the architecture, eliminating expensive passive components, reducing manufacturing tuning processes and test times will also greatly help. Talented and experienced engineers are needed for this, but are hard to find.

Innovative designs, along with the appropriate integration levels will allow wireless terminal manufacturers to reduce their bill of material count and costs, as well as speeding up their manufacturing process and improving their yields. Innovation and Integration for cost Improvement is the formula for success in the consumer wireless electronics industry. Managing a good balance of the two is the challenge facing the RF IC system designer.

III. Integrated Design

Whether it is a high performance sub-micron microprocessor, or a mixed-mode analog and digital system, the use of an advanced semiconductor process potentially offers cost improvements through higher integration levels. Cutting down the number of ICs, discretes, and passive components will usually, but not always, reduce system cost. There are two paths for the radio designer to cut costs with integrated design: improve the RF front end, and integrate the analog, digital, and eventually low/high frequency signals.

The RF integration creates several challenges to the IC designer. One of them being a packaging problem. Traditional and low cost surface mount packages like TSSOP or TQFP, can severely limit the performance of an integrated RF IC. The package parasitic inductance and capacitance of these packages are much worse than discrete type packages. In addition, isolation between different active elements on the chip is likely to be package-limited. These parasitic and isolation problems are much easier to deal with when using discrete components, but there is a great payoff for those who can overcome these obstacles. With an acceptable performance level and even with a similar price compared to a discrete solutions, an integrated solution will always win as it offers a lower bill of material part count, and a faster and more reliable manufacturing process.

The three basic cost components of an integrated circuit are die, package and test. The IC package, for instance a good RF performance QFP with 24 pins, and its associated testing account for a fixed starting cost which will make it difficult to compete against low complexity discrete solutions. A cheaper package like an SOIC with 8 pins could help reduce the package cost, but with its low pin count will limit the integration potential. But when the integration level of the IC increases, the package and test overhead cost becomes more and more acceptable and even competitive. As illustrated in Figure 1, the integrated solution becomes cheaper if it integrates enough equivalent discrete transistors. The die cost delta to integrate another RF transistor equivalent function on chip is rather small compared to the discrete transistor cost. Therefore the incentive is to integrate as much as possible of the radio functionality on a single chip, keeping in mind the performance and isolation problems as previously mentioned.

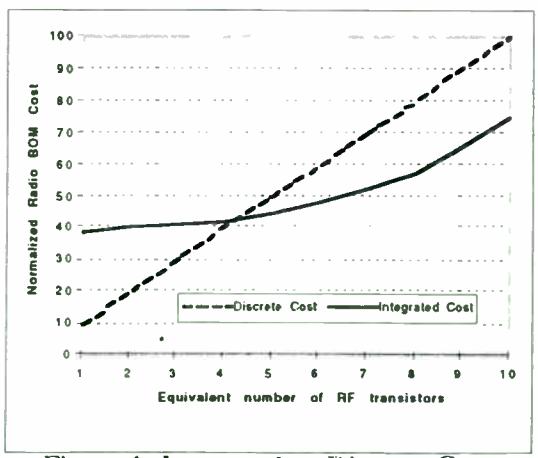

Figure 1: Integrated vs Discrete Cost

The BiCMOS process also offers great integration potential. Analog, digital, and RF functions have already been combined on the same chip. Depending on the BiCMOS RF process capabilities, higher RF integration can be accomplished. But even with a medium RF performance BiCMOS, integration of VHF systems like a 50MHz cordless phone can be achieved. The Motorola MC13109 or MC13111 Universal Cordless Phone Subsystem ICs, integrate all the analog voice processing, the dual conversion FM receiver, the CMOS universal dual PLL frequency synthesizer, low battery detect and more miscellaneous functions. The MC13110 also incorporates a voice scrambler to provide call privacy. At first look, the new ICs cost more or almost the same when compared to the three or four older ICs that they replace. Still, it proves to be very successful. Why? Simply because they offer substantial cost savings which can't be directly accounted in the selling price. First, they eliminate a number of manufacturing tunings; second, they reduce the number of passive components; and third, they increase production reliability.

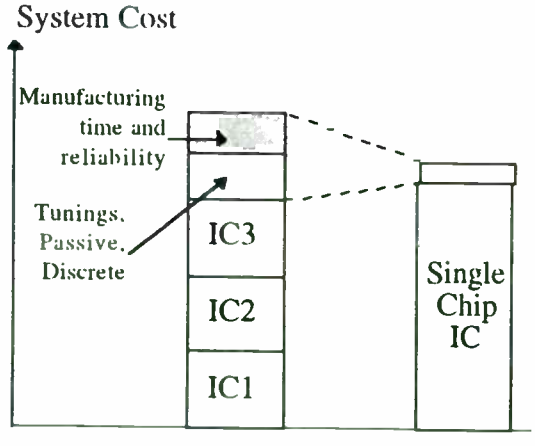

Figure 2: System Cost Comparison between an Integrated vs Multi Chip Solution

From Figure 2 the cost benefit of the integrated one-chip solution becomes obvious. In the case of the MC13109 Cordless Subsystem IC, another important benefit includes reduced current consumption down to one-third of the multi chip solution, and a significant PCB real estate reduction.

A similar system cost improvement could be illustrated with an integrated power amplifier (IPA). Whether in GaAs for maximum efficiency or LDMOS for lowest cost, IPAs are gaining an increasing market share in transmitter design for the same economic reason, lower overall system cost.

IV. Innovative Design

Innovative design improves overall system cost through reduction of external components count and price, as well as improvements in manufacturing cycle time and reliability. They can also allow an IC to be more versatile, therefore opening a greater potential market size, which would translate again into lower IC cost through increased production volume.

Let us for instance look at the original coilless detector found on the Motorola MC13150 Narrowband FM Coilless Detector IF Subsystem. The first obvious benefit of this detector is to eliminate the bulky traditional quadrature coil usually needed to perform the FM demodulation. This provides a direct savings on the system bill of material; and a tremendous advantage for space-starved applications such as wireless PCMCIA modems. There is also a second advantage,. the detector autotunes itself on the IF frequency, so there is no manufacturing adjustment needed. The radio manufacturing process is therefore simpler, quicker, and more reliable. Thirdly, the detector is highly flexible. The IF frequency can be chosen freely within the detector operating bandwidth. Also, the demodulated signal bandwidth can be easily adjusted with a couple of external resistors and capacitors. All this is done without sacrificing any linearity or distortion performance. This detector even delivers a rail-to-rail demodulated signal output under 2.5 to 6 volts operation, incredibly better than the usual hundred millivolts or so of traditional quadrature detector. This IF Subsystem IC can therefore easily be implemented in various analog or low speed digital FM wireless systems.

Innovative low power, highly linear, double balanced RF mixers like the MC13143 or integrated into the MC13142 LNA, mixer, and VCO, also help the radio designer. Fully operational from DC to 2 GHz, these new kinds of mixers offer an outstanding 1 dB compression point at +3.0 dBm and input IP3 at -3.0 dBm. Another nice feature is the linearity adjustment input pin which can be used to extend the input IP3 up to +20 dBm at the expense of a slightly higher current drain. The high performance over a wide frequency range and programmability of this mixer will allow a radio designer to use it in various system design applications. He will save time and design effort by re-using the same part over and over. Also, through higher total volume purchase he will be able to negotiate a better price. This is another example of an innovative design which has the potential to reduce a radio system cost.

V. Partitioning of New Radio Design

Keeping in mind our I^3 formula for a successful design implementation, how should you partition a new radio chip set? There are so many different systems and standards that one architecture will not fit them all. We could first classify radio systems into two categories: Frequency Division Duplex (FDD) and Time Division Duplex (TDD) systems. Also, the transmitting power of the radio would dictate different system partitioning. The transmitter stages in a low power system (typically cordless phones) could be integrated in silicon with other functions while high power terminals like cellular or PCS will need separate power amplifiers, integrated or not.

Once this basic system requirement is understood (TDD vs FDD, low or high power), and the radio architecture is chosen (single, dual conversion, direct conversion, direct VCO modulation, etc...), the system designer must carefully make the best use of the different IC technologies that are available to him. Some functions will be more cost effective in one process than another. But there is a last trade-off between the best possible cost effective cut and a platform concept. With scarce RF design expertise available, it is very desirable that one particular radio design could be re-used as is done on other terminals with different feature set. This way, one RF subsystem design can be dropped entirely into a new terminal without re-design, possibly even eliminating re-qualification, significantly speeding up the wireless terminal design cycle time. A slightly more expensive chip set at first could prove to be very economical if applied over several different end products.

A. FDD Analog System

Let us illustrate these few principles with a tremendously price sensitive wireless terminal such as a 50MHz analog cordless phone. With a retail price as low as $30 there is no room for error in the cordless phone system cost budget. The main functional blocks of this system are (Figure 3) the FM dual conversion receiver, the universal dual PLL, the FM transmitter, the voice processing (compander, scrambler, gain adjustment), the audio interface, and the microcontroller.

This system is FDD and low power. The baseband processing does not require DSP processing but relies on proven analog design techniques. A maximum system integration seems therefore possible. Because it is FDD, it is wise to leave at least the last transmitter stage outside of the IC. The best system partitioning is achieved by integrating together the receiver, DPLL, voice processing and audio interface in a 0.8µm BiCMOS process. The FM transmitter is already available as a low cost standard component. The extra cost implied for its integration on-chip versus its low selling price makes its integration questionable.

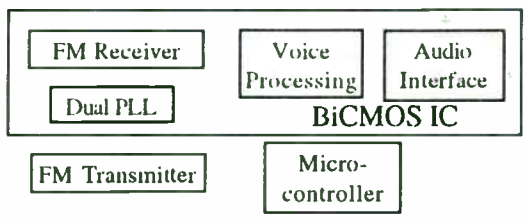

Figure 3: Optimum Integration of a 50MHz Cordless Phone Terminal

Keeping the MCU separate leaves flexibility to the phone designer. All its RF and analog processing is done by the integrated receiver and the transmitter IC. The phone functionality and man-machine interface is under the MCU control. By upgrading the MCU, a new and different phone can be designed without changing the RF and analog sections. To extend this platform concept, Motorola proposes a set of pin-compatible ICs, one offering a voice scrambler (MC13110), the other not (MC13111). Once the non-scrambler phone design is done using the MC13111, the designer can drop in the MC13110 and have a phone with scrambler!

B. FDD Digital System

There is now a tremendous market growth opportunity in the USA for good quality digital cordless phones. In contrast to Europe or Japan, where standards have been established (CT2, DECT, PHS) to serve that market, the US *laissez faire* approach has left the cordless phone designer with a wide range of design options. A cordless system can be low power, or spread spectrum high power, and does not necessary needs to be digital. Analog voice is also possible. All it needs to do is to conform with the Part 15, 902-928 MHz ISM band rules.

The winner in this new market is likely to be a low power, cost effective, digital phone. If it is an FDD system, it would not need data framing and burst mode control logic. Same as for 50MHz cordless phone, the receiver and transmitter function will be better being separated to avoid Tx to Rx interference. A high frequency bipolar process like MOSAIC™ V is chosen for the front end radio design. With Ft at 14 GHz, this process offers optimum performance versus cost for a 900 MHz system. Having now defined a receive and transmit front end IC, it will be to our advantage to integrate all functional blocks of the system which will have optimum performance in this process. For the receiver; that includes the low noise amplifier, down mixer, prescaler, VCO, IF amplifier stages and a coilless demodulator. The transmitter IC should integrate a VCO, prescaler, and amplification stages to drive the antenna. Standard surface mount TSSOP or TQFP packages can be used and still provide acceptable RF performance. (Figure 4).

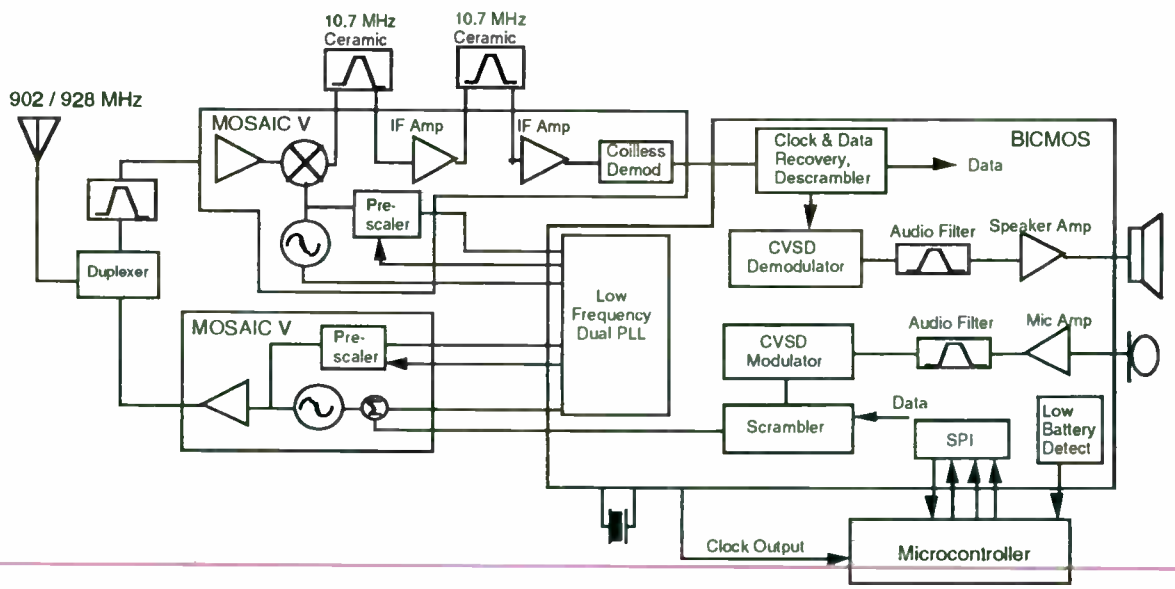

Figure 4: A Digital CVSD 900 MHz Cordless Phone

What is left outside of these two front end ICs is the dual PLL frequency synthesizer, and the baseband processing. Several standard options exist to digitize the voice: PCM, ADPCM, or CVSD codec. ADPCM codec has a lot of momentum since it was adopted as the voice coding standard for CT2, DECT, and PHS. It seems therefore a natural choice for a US digital cordless phone. However, a much older voice coding technique known as Continuously Variable Slope Delta (CVSD), has been recently used in a 900MHz cordless phone. CVSD offers significant cost savings over ADPCM because of its relative simplicity. New CVSD design development would also help integrate more functions and improve voice quality over the existing fairly old devices. A BiCMOS process here will help integrate the CMOS DPLL, the bipolar CVSD and audio interface circuitry, and CMOS switched capacitor filters. This yields the system partition shown in Figure 4.

C. TDD Digital System

Several new wireless systems use a Time Division Duplex (TDD) method. This duplex method potentially can reduce the radio cost by simplifying the RF filtering and making the Tx to Rx isolation easy to implement. DECT is a good example of a TDD system using a simple FM modulation technique. A cost effective FM coilless detector can be used in this case. Thanks to the TDD method, transmit and receive signals can be integrated on the same chip. As many high frequency functions as possible should be integrated in a one-chip front-end transceiver. A high frequency bipolar process like MOSAIC V would be ideal for this transceiver. The remaining functions of the radio subsystem then include the lower frequency IF receiver, CMOS PLL frequency synthesizers, and other miscellaneous functions. These functions can be integrated into a cost effective BiCMOS IC which does not require extremely high RF performance. This partitioning would ensure maximum performance, while using the most cost effective processes available. Figure 5 illustrates this partitioning with the popular single conversion, open-loop modulation type DECT radio architecture.

(MOSAIC is a trademark of Motorola inc)

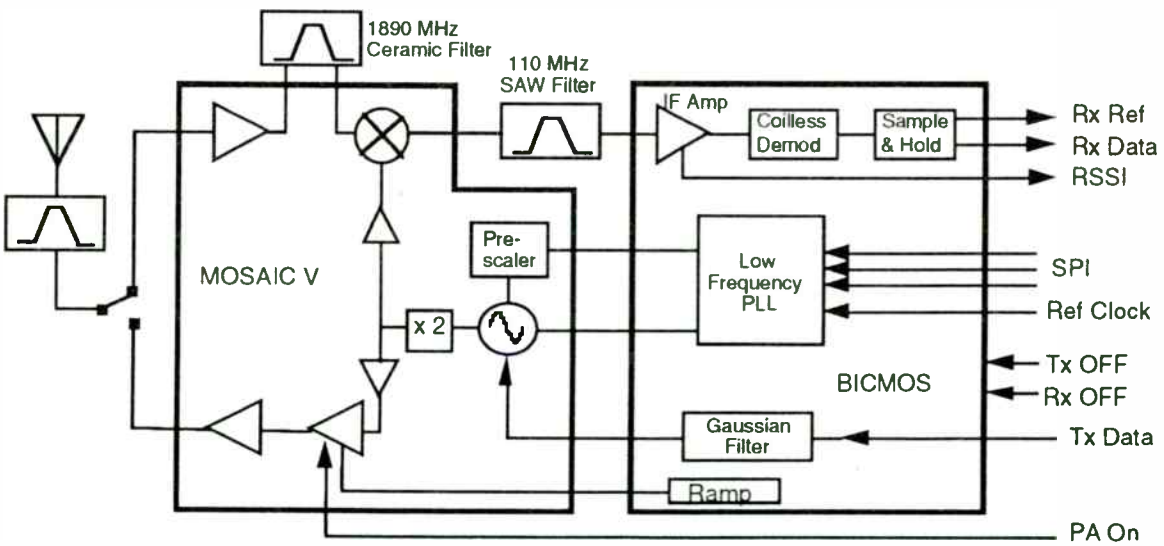

Figure 5: An example of a DECT Radio Partitioning

An Analog Single Chip Receiver IC for the 46/49MHz 25 channels Cordless phone and Application in the 902 to 928MHz ISM band

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Introduction

This paper describes a Motorola single chip that implements the RF circuits and audio baseband processing blocks of a typical 46/49MHz 25 channels cordless phone. The IC includes a dual conversion superheterodyne receiver, a fully programmable dual synthesizer, a fully integrated and programmable baseband audio processor consisting of a spectral inversion voice scrambler, a compandor, a speaker amp driver, and amplifiers with programmable gain.

The paper will start with a quick overview of the various RF design consideration in the new 25 channels 46/49MHz spectrum, followed by a discussion on the MC13110 single chip Cordless phone IC (nicknamed the "combo chip") and its application; and lastly the application of the combo chip as an IF stage for an ISM band (902 to 928 MHz) low power cordless phone.

46/49MHz 25 channels Spectrum

The FCC has released on April 10 1995 the additional 15 channels per each frequency block to increase the total number of available channels to 25. The Base transmitter frequencies are from 43.72MHz to 46.97MHz - a total span of 3.25 MHz; and the Handset transmitter frequencies from 48.76MHz to 49.99MHz - a span of 1.23 MHz. The minimum channel spacing is at 20KHz with its channel number ordering not in a contiguous manner. Examining this allocation of spectrum, several observation can be made :

- the base transmitter & hence the handset receiver has to operate over 3.25 MHz of spectrum - an equivalent bandwidth of about 7%; while that of the handset transmitter & base receiver of about 2.5%;

- in the base, if a conventional second intermediate frequency (IF) of 455KHz is used in a dual conversion receiver, the image frequencies of the second IF in certain channels are exactly those assigned in some other channels. For example, channel 1 (48.76MHz) is exactly the second image frequency of channel 16 (49.67MHz); channel 1 frequency is exactly 2 times 455KHz down from channel 16. So is the case for channel 3 and 19; 4 and 21; 5 and 23; 6 and 24;

- there are possible interferences from the existing private land mobile radio services user which shares the 15 channels frequencies allocated in the handset spectrum. Since these are simplex operated; the base receiver is subjected to such interference.

To take the above observations into the design consideration, one has to decide what kind of system performance required to meet its design needs. In the application example, the wider passband in both the transmitter and receiver front end will need double tuned amplifier, good performance duplexer, and multiple tuned circuit to achieve good receiver signal and transmitter signal separation. Some other choice of IFs such as 12.455MHz and 450KHz for the 1st and 2nd IF may be a better choice. The image channel rejection ratio for either the 1st IF or the 2nd IF may need to be as high as 60dB; and some kind of channel scanning capability will be required to overcome possible interference from the land mobile user.

Description of the Combo Chip

Dual conversion Receiver

A dual conversion superheterodyne receiver is integrated on board with the following performance :

1st mixer :	Gain	= 10 dB
	NF	= 17 dB
	Input TOI	= -10 dBm
2nd mixer :	Gain	= -27 dB
	Input TOI	= -27 dBm
IF Demod :	3dB Sense	= 55uVrms

The 1st mixer can have an IF of up to about 21MHz without losing conversion gain, and the 2nd mixer up to about 1MHz with constant gain. The 1st mixer output impedance is matched to typical ceramic filter; some matching may be needed when using crystal filter so not to degrade the crystal filter's attenuation performance. The second mixer input requires a 330 ohm resistor to match to a ceramic filter and no matching for a crystal filter. Its output is matched to typical ceramic filter at 455KHz and 450KHz. Isolation between the 1st mixer to the 2nd mixer is typically 40dB on the MC13110 without any external connection.

Dual Phase Lock Loop (PLL)

The combo chip has on board two programmable counters that allow full control of two frequency synthesizers, usable up to 80MHz. Furthermore, there is an on board differential voltage controlled oscillator (VCO) serving as a Local oscillator to the 1st mixer of the receiver. The output of the oscillator feeds the receive PLL internally, the error voltage connected through pin 4 may be filtered by a suitable loop filter and controls the on board varactor through pin 42. This VCO has a varactor and a bank of capacitor which can be selected to achieve a wide range of VCO frequencies including the LO frequencies required by the 25 channels. The receiver PLL usually needs to lock in a very short time to allows the receiver to be powered on quickly during the standby mode of operation in the handset. The other PLL controls an external VCO intended for the transmitter. The modulating signals are usually directly injected into the VCO; hence the loop filter needs to have narrow bandwidth to allow modulation [1]. The two PLL are single divide PLL with a 14 bits divider programmable serially through the serial

programmable port. Full details are available in the datasheet of the device. The reference divider consist of a 12 bit programmable divider and optional divide by 4 and 25 options intended for the UK cordless phone standard. The reference crystal doubles up as a 2nd LO for the receiver and also provide the clock signal to the other digital circuits on board.

Voice Scrambler

The analog spectral inversion scrambler use an scrambling carrier of about 4KHz. The voice spectrum is thus flipped at this frequency. The carrier is derived from the 2nd LO through a 6 bit programmable divider followed by a divide by two followed by a divide by 40 counter. The scrambler has built-in multi-pole switch capacitor filter as its anti-aliasing filter. The filter passband thus limits the possible choice of the scrambler carrier frequency controllable through the 6 bit divider. Both of the receive and transmit scramblers have bypass switches which allow the functionality be bypassed.

Compandor and Audio amplifiers

Further programmability is provided through the use of programmable gain amplifiers in both of the receive and transmit path. In the receive path, the amplifier can be adjusted over a range of 30dB through serial programming. A mute switch is also incorporated. The receive path then provides an expandor, a volume control amplifier of 30dB adjustable gain, and a speaker amplifier driver with a mute switch capable driving speaker of down to 32 ohm in load. In the transmit path, there is an uncommitted inverting amplifier as an microphone amplifier , a compressor with ALC, a mute switch and a limiter before sending the signal into the scrambler. After the scrambler, an adjustable gain amplifier of 30dB provides flexibility to signal waveshaping before going into the modulator.

Data Amplifier and Comparator

There is an on board data amplifier with hysteresis which squares up the incoming FSK data to a CMOS compatible signal for the microcontroller to read. In order to access received signal strength information, there is an on board comparator which compares the RSSI voltage to a programmable reference level. This comparator allows the user to vary the reference level and the comparator output a logic signal to the microcontroller to indicate its relative signal strength. This feature is of particular importance to interference avoidance. There are two other comparators which compares two external voltage sources to the on board bandgap reference and they can readily be made into a low battery detector and a dead battery indicator.

All of the programmable blocks are serially controlled through the 3 wire bus. The IC also provide a clock signal for a typical 8 bit microcontroller. The entire IC can be powered to several states including an inactive, a standby, a receive, and an active state through the serial bus. To further improve the integrity of the digital circuit, there is also a hardware interrupt function to reset the circuit to some defined state [2].

The MC13110 combo chip together with a microcontroller IC such as the Motorola HC05 MCU provides full system solution to a cordless phone product. Other similar devices in the Combo family are the MC13109 IC with 2 Volt Vcc capability and is without the scrambler, and the MC13111 which is pin to pin compatible IC to the MC13110 but without the scrambler function on board.

Application in a 46/49MHz System

The targeted system performance for this example of implementing a handset for the US 25 channels phone is similar to or exceed those found on the existing 10 channels set. These targeted requirements are :

- a board level sensitivity of -110dBm with a 3KHz peak frequency deviated signal of 1KHz modulating tone;
- an image rejection ratio performance of more than 60dB;
- an adjacent channel rejection ratio performance of more than 40 dB;
- a received audio distortion of less than 3%;
- a transmitter board level power of 0dBm;
- a transmitter modulation of 1KHz unscrambled tone of 1.8KHz and 1500bps data of +/- 4.5KHz; and
- using off the shelf parts with the least number of external components.

Receiver Design

To meet the requirements, the system needs a preamplifier with a lowest possible noise figure (NF). A problem with intermodulation distortion problem in the handset receiver is serious when the transmitter RF gets through the duplexer and get amplified also by the preamplifier and get mixed with the LO and produce either the upper or lower IF components for the 2nd mixer. This problem is commonly known in the 46.610MHz/49.670MHz frequency pair. While the preamplifier has to have the wider 3.25MHz passband it also needs to have a notch at the transmitter frequency to attenuate the signal. Two ways are being considered to eliminate this problem ; firstly, use an IF such that the spurious intermodulation product does not fall at or near the IF passband, (e.g. a 12.455MHz 1st IF and a 2nd LO of 12MHz.) The choice of the 1st IF is limited by the availability of common ceramic IF filter and crystal value for low cost consideration; alternatively, a preamplifier with a notch filter may be used. Figure 1 shows the preamplifier with a notch filter consisting of inductor Lxx and Cxx , this preamplifier provides about 10 to 12 dB of gain over the 3.25MHz passband and has a 1.5dB attenuation at the 48/49MHz frequency, tested with the MC13109 IC. In this example, the 12.455KHz IF option is chosen since there are commercially available parts for both the 12.455 ceramic filters and 12.00MHz crystal. Figure 2 shows the preamplifier with the coil construction details. In the base receiver in which the 2nd IF image frequency are exactly the other channels with a 2nd IF of 455KHz, a second IF of 450KHz may be helpful to achieve better second IF image rejection. This can be done easily using the same 12.455MHz ceramic filter and 12.00MHz second LO provided that the frequency

modulation of both voice and data are kept under 5KHz of peak deviation.

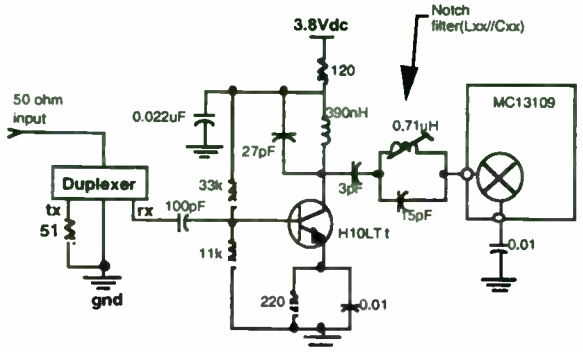

Figure 1.0. Preamplifier with notch filter in the receiver.

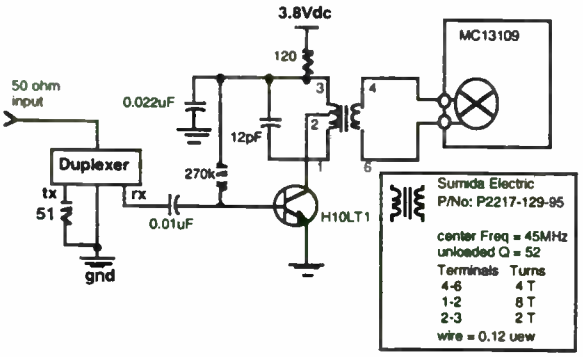

Figure 2.0. Preamplifier with transformer for the Handset receiver front end.

The overall receiver circuits with its internal LO circuits are shown in page 1 of the schematic drawing attached. A list of the vendor part numbers are also provided for the ceramic filters and coils. With these design parameters, the overall receiver performance on the demoboard with a duplexer and the transmitter powered on were measured and tabulated in table 1.

Channel #	12dB Sense. (dBm)	TX Power (dBm)	comment
1	-111.5	0.3	
2	-112.5	0.7	
3	-114.0	0.8	
4	-95.0	1.1	TX desense RX
5	-114.0	1.3	
6	-111.0	1.4	
7	-113.0	1.5	
8	-112.5	1.5	
9	-112.5	1.5	
10	-112.0	1.5	
11	-110.5	1.5	
12	-111.0	1.5	
13	-111.0	1.5	
14	-111.0	1.5	
15	-111.0	1.4	
16	-111.0	1.4	
17	-110.5	1.4	
18	-110.0	1.0	
19	-111.0	1.3	
20	-110.5	1.0	
21	-110.0	1.0	
22	-110.0	1.1	
23	-110.0	0.9	
24	-109.0	0.8	
25	-109.0	0.6	

Table 1(a). 12dB sensitivity of the Handset board; measured in full duplex mode with the transmitter power measured. The desense is typically less than 3dB except in channel 4. The sensitivity is measured with a 1KHz tone modulated carrier of 3KHz frequency deviation.

Receivers Test :

(RF = 46.610MHz, deviation = 3KHz, fm=1KHz) (Image or Adjacent : fm= 400Hz , deviation= 3KHz)	
1st Image rejection Ratio	69dB
2nd Image Rejection Ratio	40dB
Adjacent Channel Rejection Ratio	44dB
Recovered Audio level	138mVrms
Max SINAD (RF@ 1mVrms) (No filter)	37dB
Max THD	1.5 %

Table 1(b). Receiver performance with the preamplifier, 12.455MHz IF1 and 455KHz IF2.

Receiver LO and PLL design

The receiver LO needs to have fast startup time, fast lock and switching time, good spectral purity, low phase

noise, and good tunable range. A high side injection scheme is a better choice here. The IC needs a tank circuit across its differential VCO's terminal as a resonating structure. The lossy element in the tank circuit is the inductor and it is critical to use an inductor of good Q factor, typically of over 60 is adequate. Fixed inductor may be used provided that the Q is high enough. The values of the inductor and capacitor in the tank can simply be calculated taken into consideration of the varactor diodes capacitance and the internal capacitor values (which is programmable [2]). Always using the lowest capacitance values to ensure the highest tuning range and fastest lock time [3]. Loop filter design method can be found in [4] and [5]. The receiver loop is capable of locking from powered up in less than 12 mS; and a lock to lock time of less than 10 mS at the most. The single sideband phase noise is about -65dBc at an offset frequency of 10KHz. Figure 3 to 7 are the PLL component values and the simulated results of the receiver loop using the MathCad software of MathSoft.

A Frequency Table of the handset receiver is shown in Table 2 with the receive divide ratio calculated. The LO frequency is simply the sum of the 1st IF of 12.455MHz and the RF frequency; while the 2nd LO being a 12 MHz crystal with a PLL reference frequency of 5KHz. The divide ratio is then the ratio of the LO frequency over the reference frequency.

Channel No	RX Freq (MHz)	RX LO (MHz)	RX Divide Ratio
1	43.720	56.175	11235
2	43.740	56.195	11239
3	43.820	56.275	11255
4	43.840	56.295	11259
5	43.920	56.375	11275
6	43.960	56.415	11283
7	44.120	56.575	11315
8	44.160	56.615	11323
9	44.180	56.635	11327
10	44.200	56.655	11331
11	44.320	56.775	11355
12	44.360	56.815	11363
13	44.400	56.855	11371
14	44.460	56.915	11383
15	44.480	56.935	11387
16	46.610	59.065	11813
17	46.630	59.085	11817
18	46.670	59.125	11825
19	46.710	59.165	11833
20	46.730	59.185	11837
21	46.770	59.225	11845
22	46.830	59.285	11857
23	46.870	59.325	11865
24	46.930	59.385	11877
25	46.970	59.425	11885

Table 2.0. Handset Receiver Frequency Table for high side injection LO with a 1st LO of 12.455MHz.

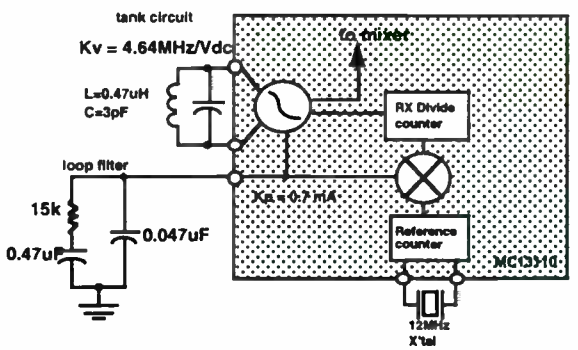

Figure 3. Receiver LO PLL component values.

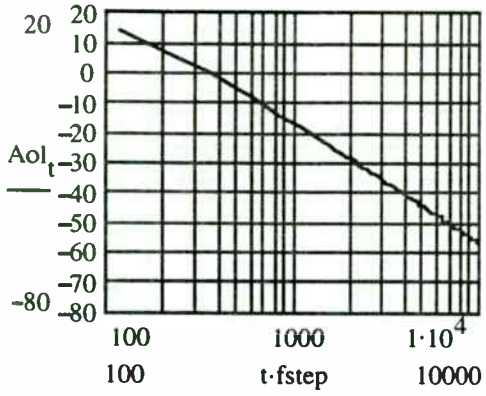

Figure 4(a). The Open Loop magnitude response of the receiver PLL Loop.

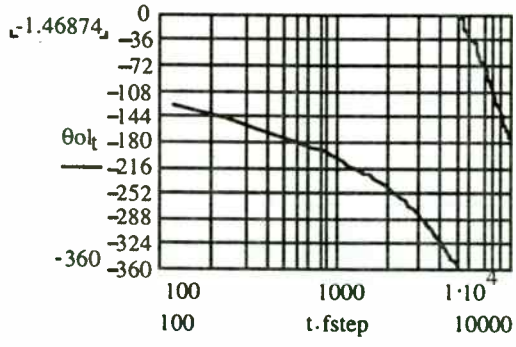

Figure 4(b). The Open Loop Phase response of the Receiver LO PLL loop.

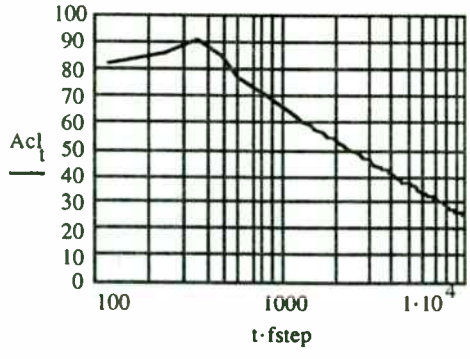

Figure 5 (a). The Closed loop Magnitude response of the receiver LO PLL loop.

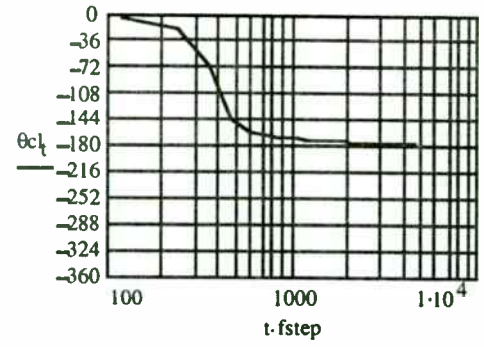

Table 5 (b). The Closed loop phase response of the receiver LO PLL loop.

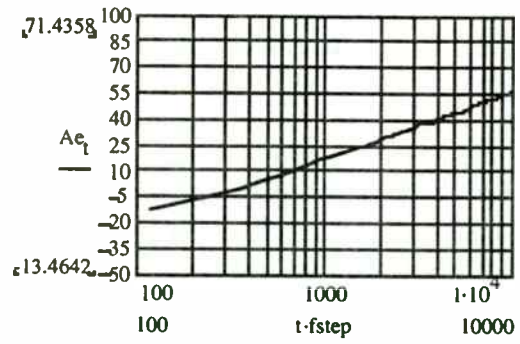

Figure 6(a). The error transfer function magnitude response plot of the receiver LO PLL loop.

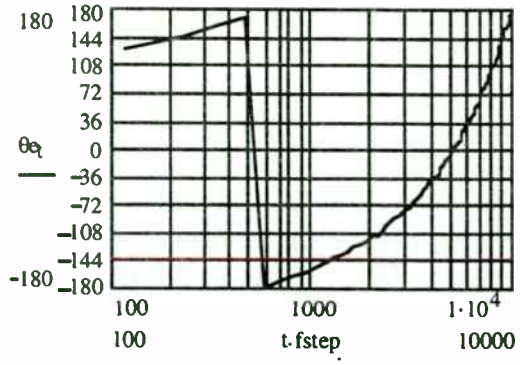

Figure 6(b). The error transfer function phase response plot of the receiver LO PLL loop.

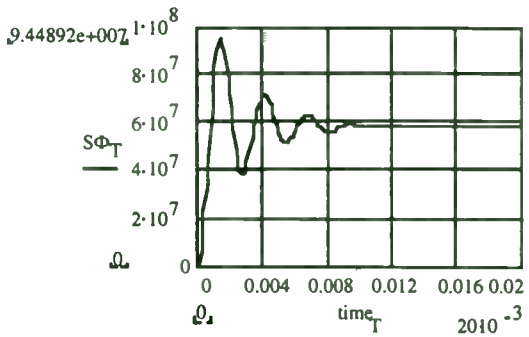

Figure 7. The simulated time domain PLL power on to lock time plot. The simulated time of about 12mS roughly agrees with the measured result of between 12 to 15mS (in many trials).

Transmitter, Modulator and TX PLL

The handset transmitter operates from 48.76MHz to 49.99MHz. With frequency modulation of audio and signalling signal inside the transmit PLL; the PLL bandwidth will need to be lower than its lowest modulating frequency. A typical colpitt oscillator is suitable. A shortest power on to lock time is also desired. The modulator must conform to the FCC requirements of spectrum confinement and spurious emission. The maximum power of the intended carrier is limited to be at 0dBm measured at the 50 ohm antenna port. This level should be sufficiently high to overcome any loss in the antenna circuit and meet the FCC part 15 requirement. The transmit VCO is buffered by an emitter follower before driving a class C amplifier. The amplifier having a collector transformer load drives the duplexer and antenna. The secondary winding of the transformer is double-tuned to widen the passband for the 25 channels. The transmitter circuits are shown in figure 8 and 9. At the modulator input, the modulation sensitivity is about 300Hz/mVrms.

The modulator filter circuit shown in figure 10 provides some preemphasis to the audio signal and "rounding" of the signaling data from the microcontroller (MCU). The transmitter and modulator performance is tabulated in table 3; and the PLL component values and its performance are shown in figure 11 to 15.

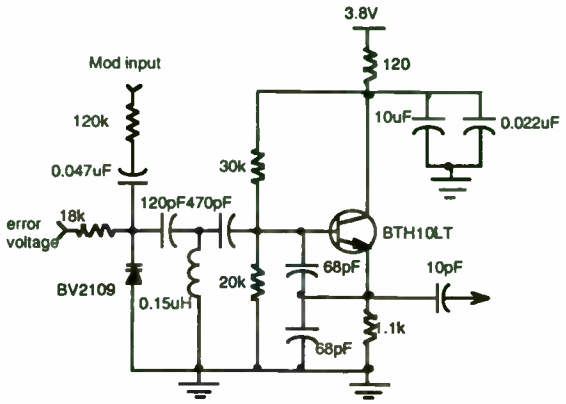

Figure 8. Handset Transmitter VCO circuit; the inductor is tuned so that the DC error voltage is at 1.0Vdc when the VCO frequency is at 48.76MHz. The VCO gain is 1.8 MHz/volt.

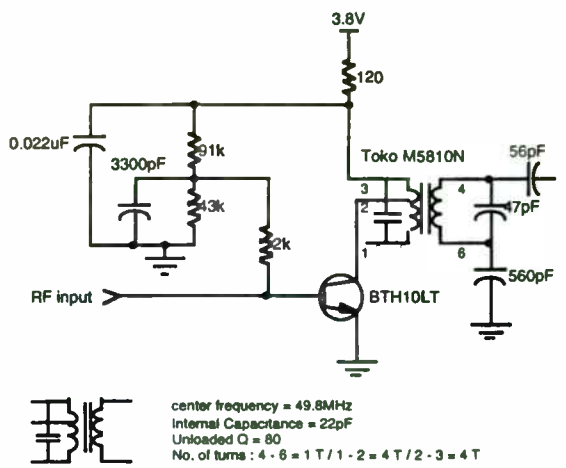

Figure 9. The Handset class c amplifier with double tuning at the transformer secondary. The output drives the duplexer TX terminal. The power level at the 25 channels are given in table 1 in the previous page. The coil construction is also enclosed.

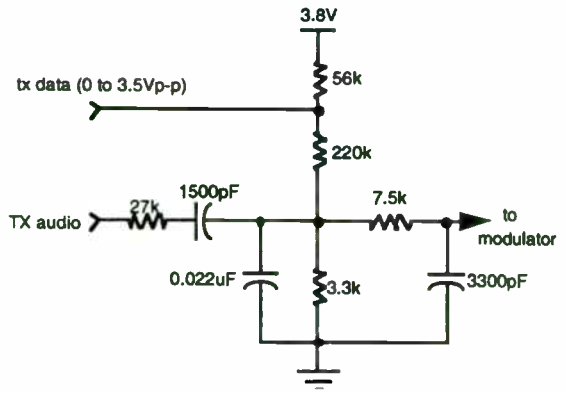

Figure 10(a). Modulator filter for transmit audio and signaling data.

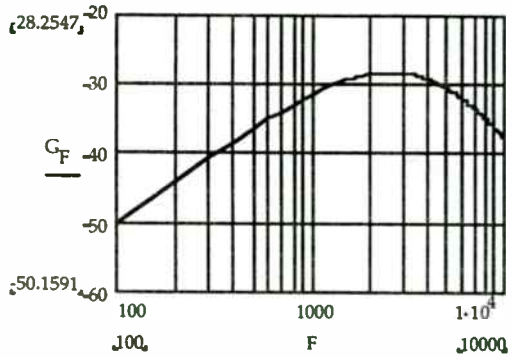

Figure 10(b). The Modulator filter frequency response. The input level of the audio signal to the filter is at -10dBV, and the signaling data at 0 to 3.5Vp-p .

Transmitter Performance :

Vcc	: 3.8Vdc
RF output power	: 0.5 +/- 1 dBm
Spurious Emission	: < -40dBc over all band

Modulation Performance :

Audio Frequency(Hz)	Peak Deviation (No filter)	Modulation Distortion (%)	Mod spectrum at 10KHz offset
	(A) No Scrambler		
300	0.8KHz	8%	
1000	2.0KHz	4%	-38dBc
3000	2.72KHz	1.30%	
	(B) with scrambler		
300	2.8KHz	6%	
1000	2.76KHz	3%	-36dBc
3000	2.1KHz	1.70%	
	(C) 1500bps NRZ data		
Mark	+4.9KHz		-30dBc
space	-4.9KHz		

Table 3. Transmitter Performance and Modulator Performance of the handset transmitter on the demo board.

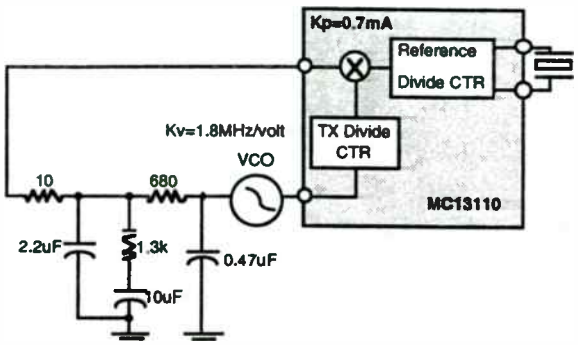

Figure 11. The PLL component values of the transmitter loop. The reference frequency is 5KHz; the frequency table and their associated divide ratio can be found in the data sheet.

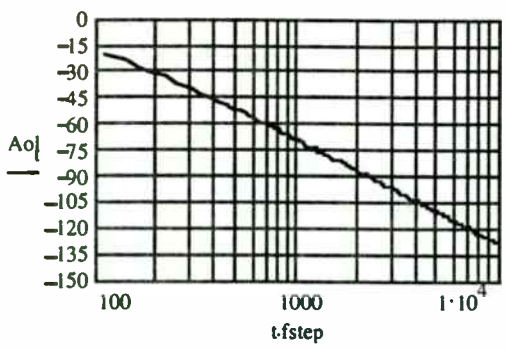

Figure 12(a). The Open Loop Magnitude response of the transmitter PLL.

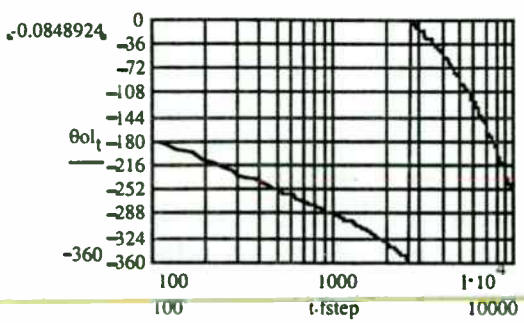

Figure 12(b). The open loop phase response of the transmitter PLL.

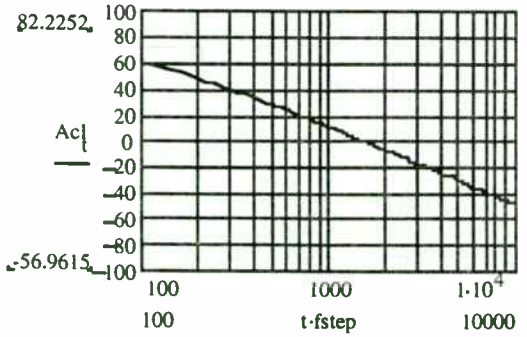

Figure 13 (a). The closed loop Magnitude response of the transmitter PLL.

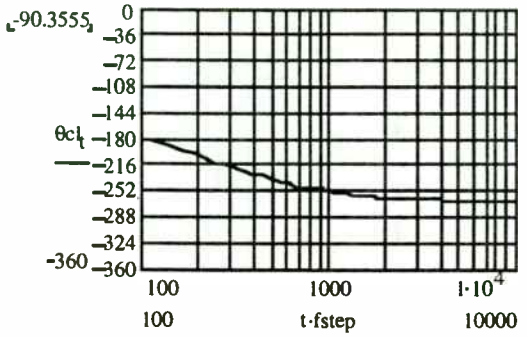

Figure 13 (b). The closed loop phase response of the transmitter PLL.

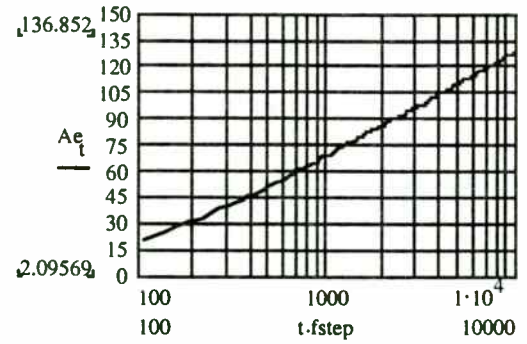

Figure 14 (a). The error transfer function magnitude plot of the transmitter PLL.

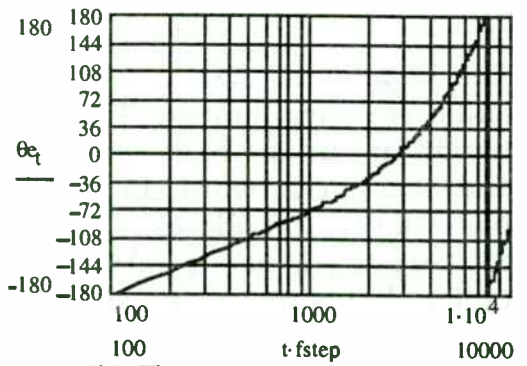

Figure 14(b). The error transfer function phase response plot of the transmitter PLL.

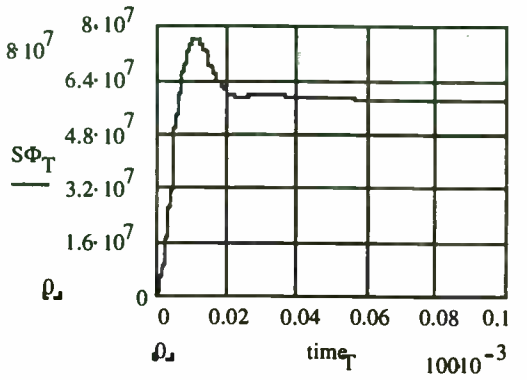

Figure 15. The simulated power on to lock time of the transmitter PLL; the lock time is about 60mSec. The measured time is typically less than 80 mSec. For signaling data modulation, a delay of 80 to 100mSec is recommended before sending the data to the modulator from the time of power up.

The transmitter frequency spectrum was measured with and without the scrambler, all were below the FCC requirement by a margin of 10dB. The modulator is designed with the assumption that the scrambler will also be used to achieve the best performance in a real cordless phone.

Receive Audio Design

The Combo IC has very structured audio circuitry built in. Therefore the design of audio circuit is very simple and straight forward. In the receive path, the final audio level required at the earpiece is about -90dBspl. Using typical 150 ohm coil type speaker, the electrical equivalent is about -32dBV over the toll quality speech spectrum of 300Hz to 3KHz. The nominal level of the recovered audio out of the receiver at the rated deviation is about 100mVrms. Hence the intermediate stages need to be adjusted to meet the earpiece level requirement. Figure 16 demonstrates the receive path and the required signal levels at each stage and its settings under scrambler enable and disable mode.

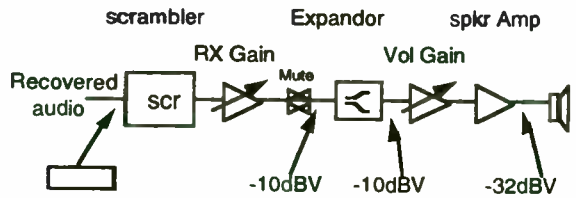

Figure 16. The receive audio path and the desired signal level.

The last stage - the speaker amplifier can be a waveshaping amplifier to enhance the frequency response of the speaker. An example with its frequency response plot are given in figure 17. This amplifier will also provides the 22dB plus of attenuation required; this will allow the nominal "Vol Gain" to be at 0dB and volume increase or decrease controlled through this programmable gain stage.

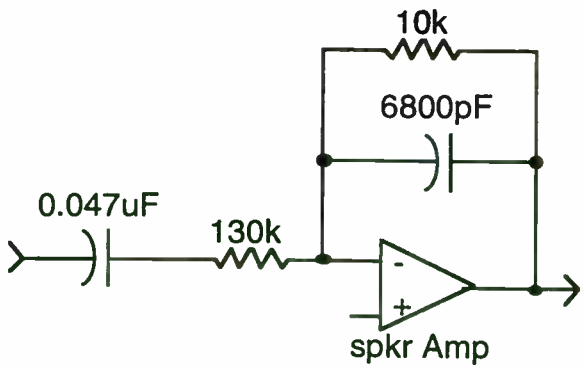

Figure 17 (a). The speaker amplifier configure as a waveshaping driver amplifier.

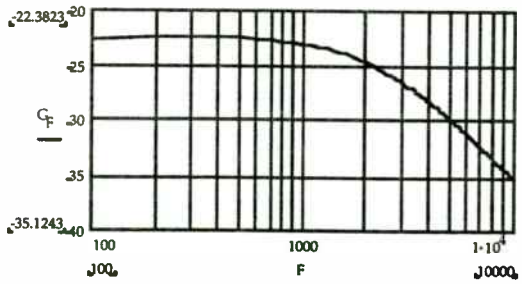

Figure 17(b). The frequency response. of the speaker amplifier shown above.

The transmitter in the base will have modulation performance identical to the handset transmitter as shown earlier. Therefore, the frequency vs modulation characteristic is as follow:

Modulating Freq.	Freq Deviation
300 Hz	0.8 KHz
1000 Hz	2.0 KHz
3000 Hz	2.8 KHz

When the scrambler is enable, the voice spectrum is centred at the scrambling carrier around 3.9KHz and hence at a higher frequency deviation will give the receiver a larger recovered audio level. Since the assumption is the scrambler is always used, this design makes this the nominal level - i.e. both "RX Gain" and "Vol Gain" is at 0dB. However

when the scrambler is disabled, the recovered audio will have a lower level, to make up for this, the RX Gain should be set to +4dB, and Vol Gain at 0dB. In both case, the nominal -32dBV required at the earpiece can be maintained. The measured result is tabulated in Table 4.

Receive Audio Signal Level
Vol Gain : 0 dB

(A) Without Scrambler

Mod freq (Hz)	Frequency Deviation	RXGain (dB)	Level at SPKR Amp output
300	0.8KHz	+4	-37 dBV
1000	2KHz	+4	-32 dBV
3000	2.8KHz	+4	-32 dBV

(B) With Scrambler

Mod freq (Hz)	Frequency Deviation	RXGain (dB)	Level at SPKR Amp output
300	2.8KHz	0	-35 dBV
1000	2.8KHz	0	-33 dBV
3000	2.1KHz	0	-39 dBV

Table 4. The Receive Audio level on the demo board.

Transmit Audio design

The MIC Amp is accessible and should be used to provide waveshaping and amplification of the MIC signal. Since there are ALC and limiting in the compressor block, the MIC input level can be amplified to the -10dBV of the 0dB gain level of the compressor. Excessive MIC input will be hard limited and should not saturate the scrambler stage. The "TX Gain" amplifier then drives the modulator filter at a nominal value with 0dB gain. Hence, the design task is in designing the MIC amplifier only. Figure 18 shows the MIC amplifier circuit and its frequency response. The entire audio to modulation performance is tabulated in Table 3.

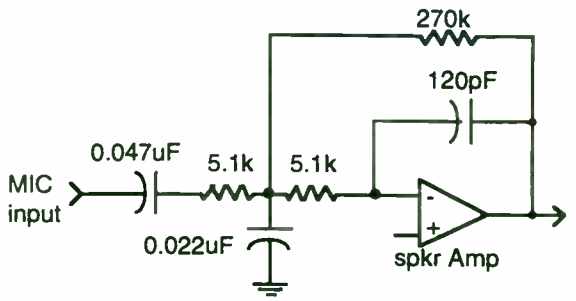

Figure 18(a). MIC amplifier circuit configured as an VCVS amplifier.

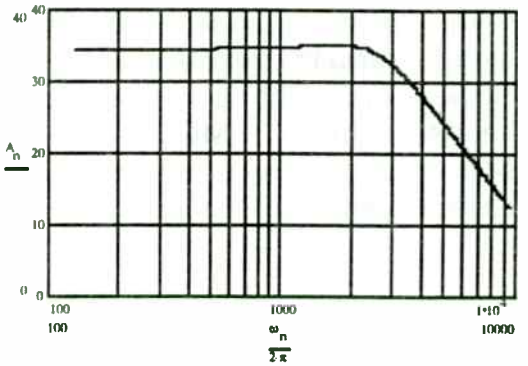

Figure 18(b). The frequency response curve of the MIC amplifier.

Data Amplifier

The data amplifier may have a passive filter before its input for best performance. In the demoboard, the recovered data at 1500bps (NRZ) has a duty cycle of close to 50%. Data rate is limited by the IF bandwidth of the receiver, particularly the passband of the 455KHz IF filter and the bandwidth of the quadrature detector. To allow higher data rate reception, a wider band 455KHz filter may be used together with a larger demodulator bandwidth which can be achieved by loading the quadrature coil with a lower value resistor. However, this passband increase also increase the noise bandwidth and hence the

sensitivity of the receiver will drop accordingly.

Logic Functions

The two comparators may be set up as the low battery detector by a voltage divider of 62K // 62K , and a battery dead detector by a voltage divider of 75k // 62k. The two trip points are 3.6Vdc and 3.3Vdc respectively.

The "CLK OUT" can be selected to be at 4MHz with a divide by 3 option by using a 12MHz crystal, ideal for a MCU clock source. The Carrier detector can be used through MCU control as a scanning receiver to detect busy channels and avoid these channels.

The design steps for the base set using this IC will be identical and straight forward.

Application in a 902 - 928MHz ISM band Receiver

The MC13109, MC13110, MC13111 can also be used as an IF stage in an ISM band device such as a 902-928MHz narrowband unlicensed cordless phone. To keep the cost down, this application example eliminates the use of crystal filter and experiments a triple conversion receiver platform. As a simple exercise, the first IF is chosen to be 45MHz. This choice is based on the predicted achievable image channel rejection by using standard inexpensive ceramic filters in the front end. The second and third IF remain at 12.455MHz and 455KHz respectively. The extra circuits required is a low noise amplifier (LNA) and a down mixer. Two discrete transistors are chosen to implement these circuits. The Motorola RF transistors MRF9331LT1 and BFR93A are chosen for the LNA and mixer. The ceramic filter used are Motorola's KFF6140 single pole filter. To replace a typical narrowband crystal filter at the 1st IF, an additional narrowband IF amplifier is used. The test circuits are shown in figure 19 to 21. The LNA has a small signal gain of 7dB and a NF of 3.5dB, the mixer has a small gain of 5dB with a -6dBm LO drive and a NF of 8dB, the IF amp has about 12dB gain and a 3dB passband of about +/- 180KHz. The 900MHz receiver test circuits are shown in page 2 of the attached schematic, and its result tabulated in table 5.

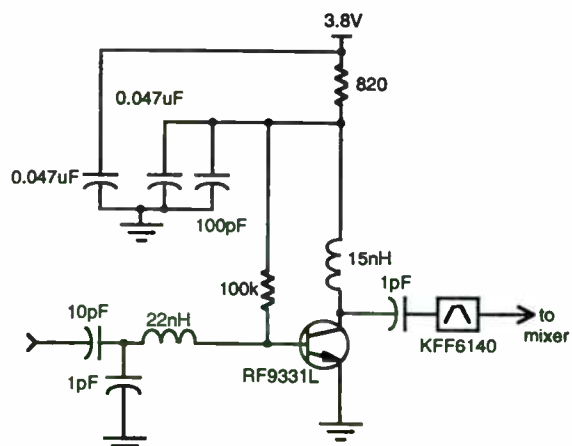

Figure 19. The LNA circuit with a center frequency at 906.5MHz intended for a ISM band cordless phone with a typical receiver bandwidth of 905.5 to 907.5 MHz - allowing a total of 100 channels of 20KHz channel spacing.

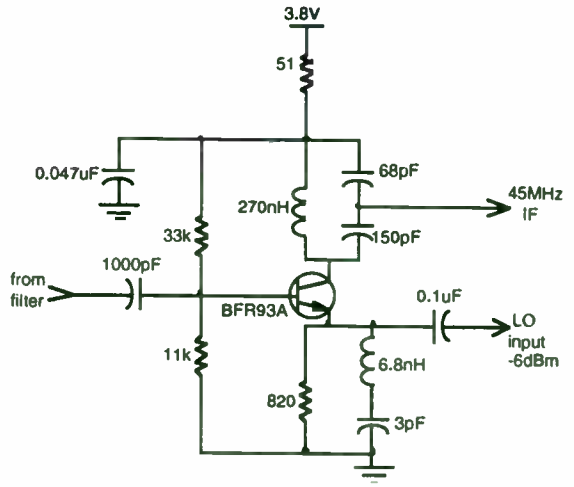

Figure 20. The down mixer circuit with a tuned circuit collector load at 45MHz. The 270nH inductor has a Q of about 60 at 45MHz.

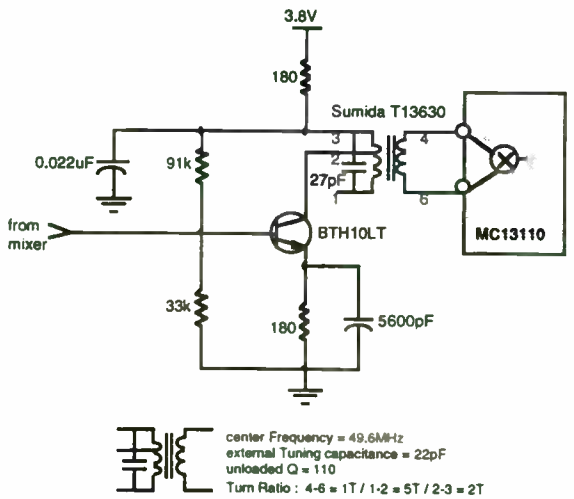

Figure 21. The IF amplifier with a centre frequency of 45MHz.

The test result shows that the 1st IF image rejection could be improved with the addition of an adequate duplexer. The gain distribution may also need to be re-evaluated to improve the sensitivity in a real system with transmitter desense and duplexer loss. The circuit without crystal filter does exhibit sufficient rejection to the image frequency and its adjacent channels.

906.5MHz Receiver Performance :

Vcc = 3.8Vdc, fm = 1.0KHz, fDev = 3KHz
RF = 906.5 MHz, LO = 861.50 MHz at -6dBm
No duplexer / No Transmitter Desense

12dB SINAD Sensitivity	-110 dBm
1st Image Channel rejection Ratio (IM freq = 816.50MHz)	30 dB
2nd IF Image Channel rejection Ratio (IM freq = 791.59 MHz)	62.5 dB
3rd IF Image Channel rejection Ratio (IM freq = 895.41MHz)	85 dB
Adjacent channel rejection Ratio (AC Freq = 906.52MHz) (AC Freq = 906.48MHz)	51.3 dB 50 dB

Table 5. The Receiver performance of the ISM band receiver.

Conclusion

The MC13109, MC13110, and MC13111 provide consumer electronic designers the high level of integration required for a low component count design, programmability, and allow fast prototype turnaround due to the simplicity of the system design. An application in the 46/49 MHz 25 channels demonstrated the ease of their application; and extend the ICs usable range as a IF stage with minimum external components in the 900MHz ISM band.

Reference

[1] F.M. Gardner, Phase Lock Techniques, John Wiley & Sons, New York, 1979, 2nd edition.

[2] Motorola's MC13110 data sheet.
[3] TenVoon Wong, " Designing with the MC13109 Universal Cordless

Telephone System IC.", Motorola forecoming Application note in 1996.

[4] F.M. Gardner, " ICs for radio equipment. Charge pump phase lock loops." IEEE Trans. on Comm. vol. COM-28, No-11,1980.

[5] Andrzej Przedpelski, "Analyse, don't estimate phase lock loop", Motorola Communication data book.

The author wish to thank the following component vendors for their support of components :

1. KDS Crystal.

2. Sumida Electric.

3. Toko coils.

4. Coicraft.

5. Motorola Ceramic Products.

SPREAD-SPECTRUM TECHNIQUES

Spread-Spectrum Techniques

Session Chairperson: Mark Sturza,
3C Systems Company (Encino, CA)

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AN OPTIMUM NETWORK FOR SPREAD SPECTRUM AND DIGITAL HDTV

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Gaithersburg, MD. 20879

INTRODUCTION

There are five fundamental properties which identify biological behavior in humans, animals and plants. This is true in all levels, molecules, cells, neurons etc. These are [1-3]:

1.Minimum energy state-maximum efficiency.
2.Self-regulating and self-limiting properties.
3.Increase of efficiency when internal dissipation and external stimulus are reduced.
4.Existence of Clock.
5.synchronization.

All elements search for a position which is comfortable, in order to perform their best. This is also the minimum energy state and the most stable state. for the biological world In general, the thermal equilibrium state may not be always the minimum enegy state, but in biological world it is the minimum energy state, which is almost imposible to realize otherwise.

Sound and cool thinking occurs when the human mind is at rest. At this state, the energy dissipation is also minimal. Jittery body and uneasy mind result in poor thinking. A good example, for efficient operation, are the fire-flies, when flashing operate at 96-98% efficiency, compared to the efficiency of incandescent lamps of 6%. The nature provides the best and the most efficient technology. The molecules, cells and the neurons, in the human body, orient themselves in the environment, in order to be comfortable. Most proteins fold into roughly globular shapes, with water-loving amino acids on the surface and the oil-loving ones inside. For every protein chain, there is theoretically, some combination of twists, bends and turns that puts it in a minimum energy state, that is the most comfortable and stable position.

A distortionless network is a dissipationless network. Therefore, in order to produce an energy efficient network, it must have minimum distortion.

The self-regulating properties in humans, animals, plants and nature are observed everywhere. No human can grow to be 10 feet tall, nor trees can reach the skies. Everything must have a self-limiting or self-regulating property, so that life can exist, without being destroyed. Likewise, in a lake, the fish population reaches a steady state level, the big fish eating the small ones simultaneously, limiting the birth rate and the population growth. Self-limiting effect is also observed on oscillators. Continuous positive feedback should destroy eventually the oscillator. But, this does't happen. In this case, the limiting property is provided by the expression "Regeneration Gain x Amplitude of Oscillations" remains always constant. That is, when regeneration gain increases the amplitude of oscillations decrease by the same amount to prevent its self-destruction. This functional property provides also thermal equilibrium for the Synchronous Oscillator(SO), which is the main topic of this paper.

Clock exists in almost every organism, from humans to other mamals down to insects and plants. Evidence exists also that a given organism may contain more than one independent clock, each containing a different function. The ability of a human to be able to get synchronized to the outside world makes him very flexible. Also, bees use their arcadian rhythms as a chronometer to make navigation possible.. The fertility cycle of many coastal marine animals(Grunion) lay eggs when the tide pulls out. Likewise, the tides are phase-locked to the moon's cycle about the earth. Humain brain contains a number of frequencies around 10 Hz, and they are attracted to each other or synchronized by internal or external stimulation, such as body chemistry, food consumed or the condition of the heart. For

example, many people drink coffee in the morning to help organize the synchronization of brain waves.

Reassuring ourselves that God would not permit sluggish, inefficient and ineffective biological existence, it would be appropriate to design electronic networks, similar to the biological behavior.

The Synchronous Oscillator(SO) circuit, shown in Fig.1, has the essential functional properties of biological organism, that is, it is energy efficient and the efficiency goes up as the input energy and the internal dissipation are reduced. It has self-regulating properties, clock and can be synchronized.

WHAT IS A SYNCHRONOUS OSCILLATOR

A Synchronous Oscillator(SO)[4-6] is a universal, multifunctional network which synchronizes, tracks amplifies, filters, divides, modulates and samples in a single process, using the least amount of energy. It has no frequency limitation, except those imposed by the circuit components. Its input signal sensitivity is a function of the thermal or Johnson noise of the individual circuit elements. The SO can detect very low input signals and input signal-to-noise ratios, several order of magnitude lower than any classical network can. The limitation comes from the thermal or Johnson noise, which is also substantially limited in a SO, because it is a function of the bandwidth. The SO has two independent internal filters, namely the noise rejection bandwidth and the data bandwidth or the tracking range. The noise rejection bandwidth can be few hundred Hz, while it enjoys, at the same time, several MHz tracking range. The SO operates similar to a spectrum analyzer, where noise bandwidth corresponds to the resolution bandwidth of the spectrum analyzer.

The SO is not optimum only in regard to biological behavior, but optimum or ideal also in regard to classical network theorems. The LC linear oscillator is the fundamental circuit of the SO. The SO uses the fundamental functional properties of the LC oscillators to provide the optimum performance. For example, the SO operates in class "C" mode. This implies that the positive feedback in an LC linear oscillator is not continuous, but occurs in bursts, which are identified as time domain windows. The gain and phase-synchronization curves are shown in Fig.2. The tracking range is flat with steep and abrupt transition corners, while the phase is linear. According to Paley-Wiener criteria and Bode's Integral theorem, such gain curve is not realizable and the phase of such a gain curve can not be linear. Although the Paley-Wiener criteria requires that the gain curve has zero output outside the synchronization area, it is very difficult if not impossible to realize such a gain curve. from practical considerations.

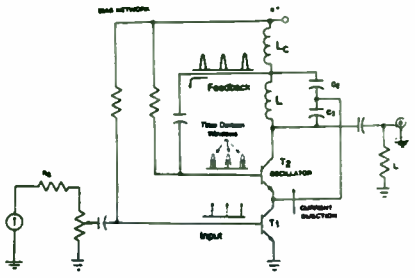


Fig.1

The gain of a SO is inversely proportional to the input signal level, as shown in Figure 3. This implies that the gain goes to infinity as the input signal level tends to zero. This means that the SO has higher regeneration gain when the input signal is reduced

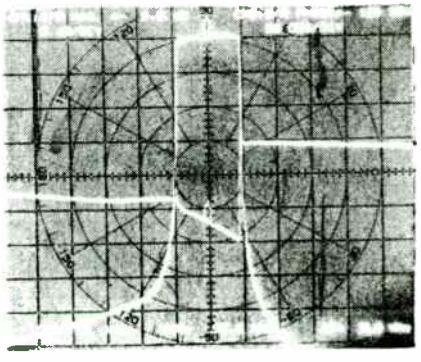


Fig.2.

The two independent internal filters of the SO, namely, the low-pass filter due to the sampling process and the high "Q", LC tank circuit filter, under regeneration, combined, generate an effective "Q_e"=3×10^6, while at the same time, the SO enjoys several MHz tracking range. This is a unique functional property, not shared by any other network. The SO is an ideal filter, an ideal divider, an ideal amplifier and modulator. Fig.4 displays

the block diagram of a SO. where the virtual sampling process combines the input signal with the time domain window and together they enter the SO. The level of the input signal to the SO is very important. It should not exceed 0 dBm for the circuit shown in Fig.1. The input signal should not disturb the regeneration process. The performance of the SO relies highly on the intensity of the regeneration gain. High regeneration gain means higher noise rejection, wider tracking range and faster acquisition.

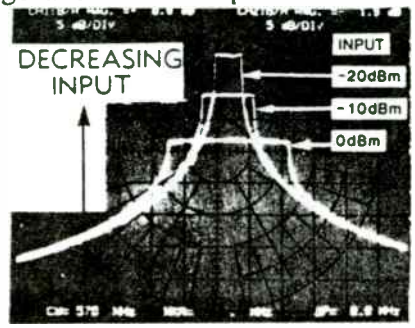


Fig.3

The SO operates similar to a spectrum analyzer, where the noise bandwidth corresponds to the resolution bandwidth of the spectrum analyzer..

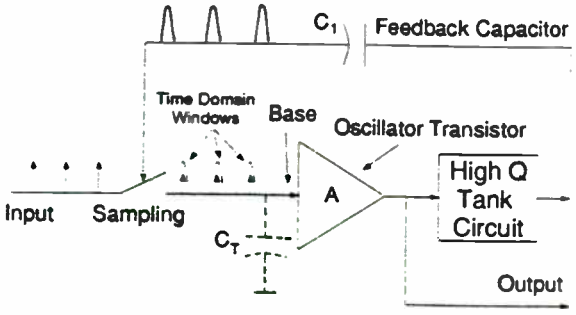


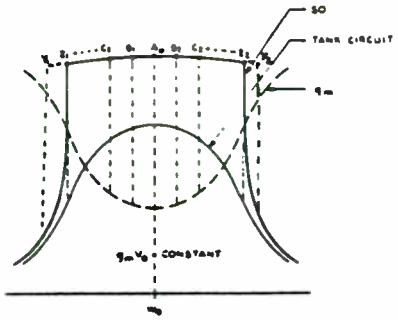
Fig.4

The SO can detect and process input signals at -100 dBm and signals with signal-to-noise ratio as low as -38 dB. These numbers correspond to the circuit in Fig.1.

The SO can divide also by integer and rational integer numbers, such as 7/8, 3/4, 2/3 in a single process, without any frequency limitation.The SO is also an ideal modulator, an ideal filter and an ideal amplifier. No other network can have higher amplification and higher noise rejection. because of the regeneration process. No other network has two independent filters. because of the sampling and the tank circuit "Q". This is why the SO is considered an optimum filter. Its proximity to biologial behavior and its ideal network characteristics generate an optimum network.

FLAT TRACKING RANGE [4,5]

Amplitude-frequency synchronization curve of a SO is shown in Fig.5. along with the tank circuit "Q" curve and the Regeneration gain curve G_R. The amplitude "A" varies according to the "Q" curve. It should be noticed that the "Q" curve and the regeneration gain curve are equal. but inverse of each other. The center frequency is identified by A_O. When the input frequency moves away from the center frequency, the product G_RxA generates points B_1 and B_2 and in turn points C_1 and C_2 and at the end generates points Z_1 and Z_2. At this point the regeneration gain is not sufficient to overcome the circuit losses and the synchronization curve collapses at a very fast rate, because regeneration for the input signal does not exist.



FILTERING PROCESS

There are two filters inherent to the SO. the sampling filter and the tank circuit filter. One way to realize a sampling filter is by using tapped delay lines or transversal filters. A sampling filter is a correlation filter and it is an optimum filter. Correlation gain is realized by sampling signals imbedded in noise. Signals at the individual tapes add directly, whereas noise adds only rms-wise. The ratio of the peak outputsignal to rms noise level is expressed as

$$R = 10 \log N \qquad (1)$$

According to expression (1), the sampling improves the S/N by as much as 30 dB after 1000 samples. Figure 6a shows on a spectrum analyzer, a direct display of an input carrier with S/N ratio of 0 dB and Figure 6b shows the display when the same signal is applied through the SO. The improvement of the S/N ratio indicates the noise rejection capability of the SO. In order for the spectrum analyzer not to interfere with the noise rejection performance of the SO, its resolution bandwidth was set at 3 MHz. The tracking range of the SO was adjusted to 1 MHz by the inputt signal level. Figure 6b shows 40 dB improvement in the S/N ratio. We may approximate the S/N enhancement by

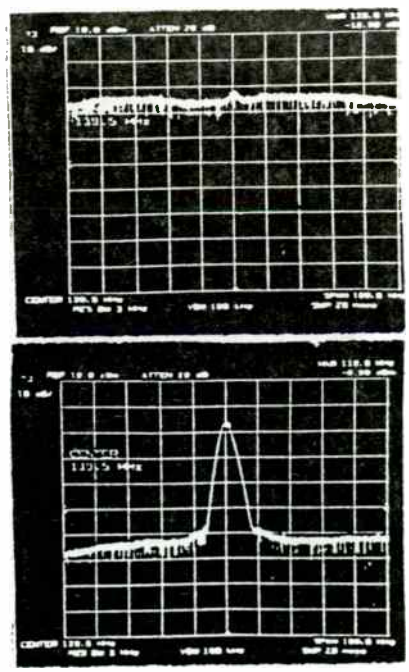
$$S/N=40\ dB= 10\ \log(3\ MHz/Noise\ BW) \quad (2)$$

Solution of (2) yields 300 Hz noise bandwidth, while the SO enjoys, at the same time, 1 MHz tracking range.

The effective "Q_e" of the SO can be determined by using expression (3).

$$Q_e = \omega_0 / \text{ 3dB BW} \quad (3)$$

For ω_0=140 MHz we have an effective "Q_e" equal to 2.9×10^6.



a

b

Fig.6

THE SO AS A FIRST ORDER LOOP[3]

The optimization of a SO is enhanced because the acquisition time, the tracking range and the phase act as first order loops [3], while the noise filtering process is of very high order, The designer has the freedom to choose the noise rejection filtering and the tracking range independently. In classical networks, such as a PLL, the loop filter and the tracking range are fully dependent, improving the noise filtering deteriorates the tracking range and vice versa.

ACQUISITION TIME

The SO acts as a first order loop in acquisition, which implies that it acquires very fast, usually within a cycle or so. The SO acquisition is only a function of the tracking range and it is independent of the noise bandwidth. Figure 7 shows the acquisition of a SO, near the center frequency.

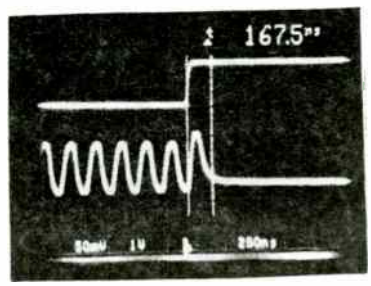


Fig.7

THE INPUT SIGNAL SENSITIVITY

The input signal sensitivity is defined as

$$S = dA/dE \quad (4)$$

where A is given as

$$A = (4\omega_0 E_m)^{1/3} \quad (5)$$

or $A = KE_m^{1/3}$

where K is a constant.

S becomes

$$S = KE_m^{-2/3} \quad (6)$$

input signal sensitivity is a direct function of the internal regeneration gain. Expression (6) implies that the input signal sensitivity tends to infinity as the input signal level tends to zero. The input signal sensitivity is a direct function of the internal regeneration gain. Figure 3 shows three gain curves, where the input varies between 0 dBm and -20 dBm. At -20 dBm the gain has increased by almost 20 dB.

BODE'S INTEGRAL THEOREM

Bode's integral theorem derives the phase from the gain or attenuation curves and vice versa. K in expression (7) corresponds to the number of poles.

$$\phi = -K\Pi/2 \qquad (7)$$

For one pole network the phase is -90° and for two pole network, it is -180°. According to Bode, for the gain curve of Fig.2, the ϕ should change also abruptly, as shown in Fig.10. But in a SO the phase remains always 180°, independent of the gain curve. The ϕ is independent of the gain characteristics. It is a function of the tank circuit.

PALEY-WIENER CRITERIA

Paley-Wiener Criteria sets the rules for the realizability of classical networks. The necessary and sufficient condition for the gain function to be realizable, the following must be true:

1. The gain curve can not fall-off faster than an exponential order, and 2., the gain can have infinite rejection for discrete set of frequencies, but it can not have infinite rejection over a band of frequencies. The gain curve of Fig.8 can not be realized, because it has infinite rejection over a band of frequencies. Also, the network of Fig.9 can not be realized, because the curve falls off faster than exponential. The gain curve of Fig. 10 can be realized, because it never reaches the zero level (finite ε) and the gain is finite outside the tracking range. From practical considerations, the gain curve of Fig.10 is very difficult to be realized, if not impossible. The gain curve of Fig.10 is similar to the SO gain curve in Fig.2. Note the ϕ in Fig.10, from classical considerations. For the SO the ϕ-curve is always 180°

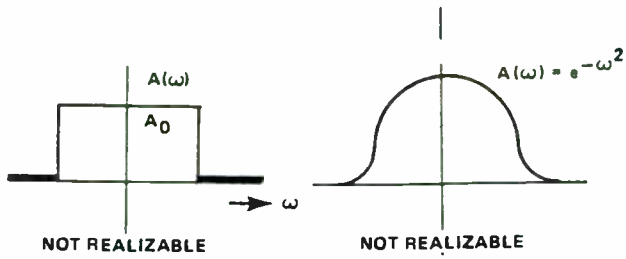


Fig.8 Fig.9

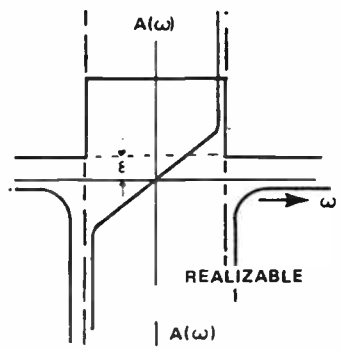


Fig.10

Lyapunov's stability criteria nor any classical network theorem can be applied to the SO, because , according to classical network theories an oscillating system is unstable. But, interestingly the SO performs its functions while in oscillations and performs them in a superior way. Based on the biological phenomenon and the results on classical networks, optimum performance can be achieved only by networks which adhere to biological behavior.

COHERENT PHASE-LOCKED SO [7]

The Coherent phase-Locked Synchronous Oscillator(CPSO) retains all the functional properties of the SO, while providing coherency, throughout the tracking range. Figure 11 shows a detailed block diagram for a 120 MHz CPSO. The input phase is compared to the output phase and the error is used to correct for the bias, which makes the CPSO frequency equal to the input frequency. Thus, the CPSO operates always under optimum conditions. Similar to the SO, the frequency acquisition is very fast, while phase follows it, becuse of the integration process in the loop. The CPSO is very usefull in digital communications.

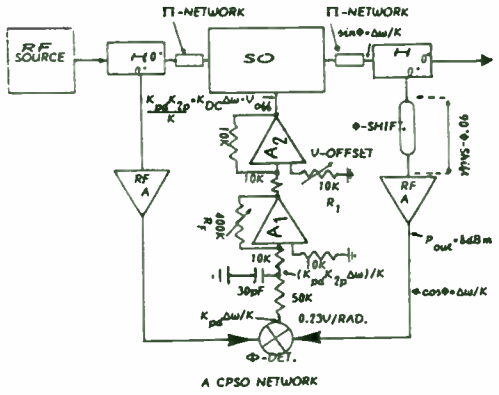


Fig.11

The gain and phase synchronization curves of a CPSO are shown in Figure 12. Note that the phase is almost zero throughout the tracking range, campared to a SO, which is +90-0--90° totalling to 180°.

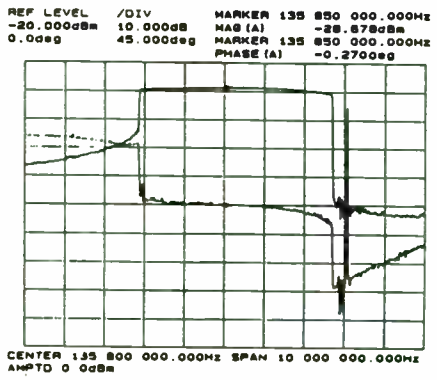


Fig.12

SPREAD SPECTRUM SYSTEMS [8]

Block diagram of the practical direct-sequence spread-spectrum link is shown in Figure 13. The success of this arrangement lies in the use of the SO to recover the transmitter carrier and clock at the receiver. In the transmitter, a spread spectrum signal is generated by mixing carrier oscillator and pseudo-noise(PN) signals in a double balanced mixer (DBM). The energy of the resultant bi-phase modulated suppressed carrier signal is spread over a wide bandwidth. In the link receiver, the spread-spectrum signal is despread by mixing it with a PN signal identical to that used in the transmitter. In practice, the most difficult aspect of making this system work is that of synchronizing the PN-generator clocks at the transmitter and receiver sites.

Envelope of the unfiltered biphase-modulated spread spectrum signal as viewed on a spectrum analyzer, in Fig.14A. At the receiver end of the link, the filtered spread spectrum signal is apparent only as a 10 dB hump in the noise floor. Despread signal at the output of the receiver DBM. The original carrier-and any modulation components, that accompany it, has been recovered. The peak carrier is about 45 dB above the noise floor, more than 30 dB above the hump, shown at 14B.

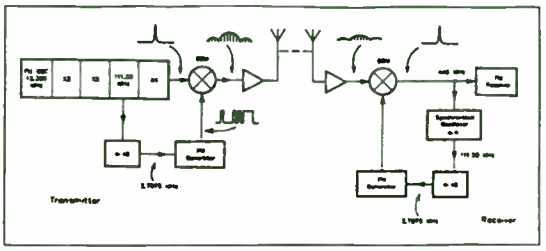
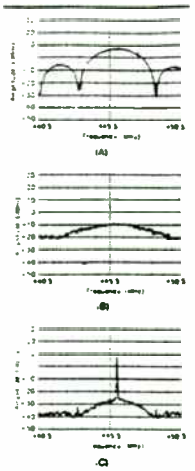


Fig.13



Envelope of the bi-phase modulated spread spectrum signal at the transmitter.

Spread Spectrum at the receiver end.

RF signal after carrier recovery.

Fig.14

The circuit used for the carrier recovery is shown in Fig.15. The additional Π-tuned circuit is for the purpose of reducing further the noise bandwidth. The Π-network is within the regeneration process. The receiver stays locked for hours without needing readjust ment. The SO requires around 30 minutes warm-up. No special components were used in the design.

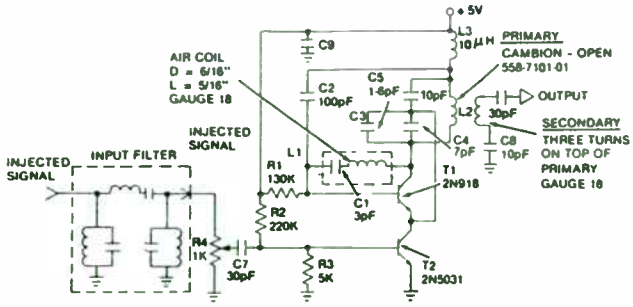


Fig.15

DIGITAL HDTV

Networks with two bit rates are discussed to cover the entire area of digital HDTV. The first network is 120 Mbits and the second one 1.4 Gbits. For the 120 Mbit case, the IF frequency is 140 MHz and it is QPSK modulated. This implies that the carrier recovery network operates at 560 MHz. For the second case the modulating frequency is 4.3 GHz and it is BPSK modulated. The main purpose of the discussions is to show the quality of performance. The 560 MHz carrier recovery circuit is shown in Fig.16.

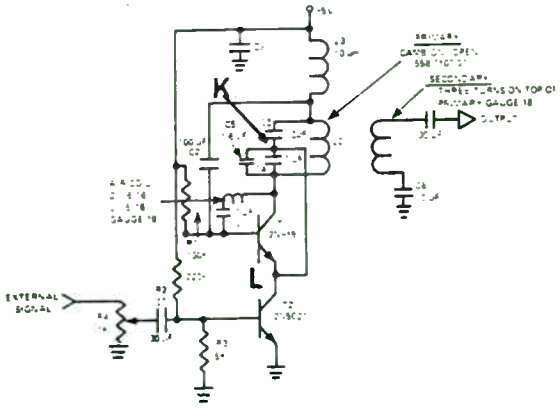


Fig.16

This circuit has an additional feedback between the collector of the oscillator transistor and the base, to enhance the noise rejection and the tracking range. The driver transistor 2N5031, has relatively low noise and high gain The output is transformer isolated to reduce the effect of the output variations to the input. Fig.17 show the BER curves. Fig.17a compares the back-to-back operation to the recovered clock and carrier, while Fig.17b compares the standard operation, with no offset, to the operation with ±30 KHz offsets. The superior performance of the SO is evident in both cases. The operation, with clock and carrier recoverings, is almost equal to those to back-to-back operation. Likewise, the BER curves with offsets are equal to those with no offsets. Fig. 18 shows a clock recovery circuit diagram for the 120 Mbit case. The circuit has only one transistor, because the noise level for the clock recovery is lower than that of the carrier recovery and the input signal level is higher.

The carrier recovery network for the 1.4 Gbit system is shown in Fig.19., while the spectrum of the receiver before and after the carrier recovery is shown in Figures 20a and 20b, respectively. There is over 30 dB improvement in the signal-to-noise ratio.

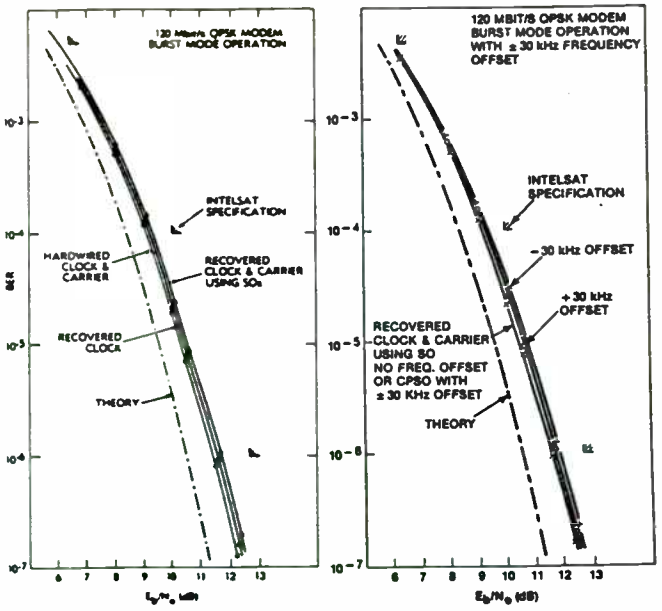


Fig.17

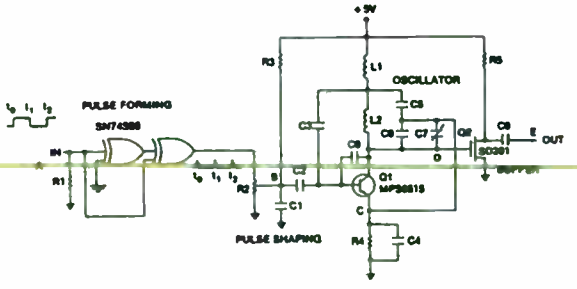


Fig.18

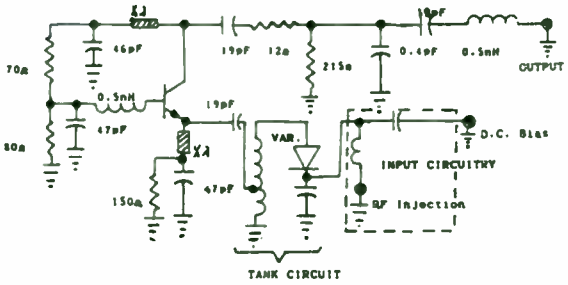


Fig.19

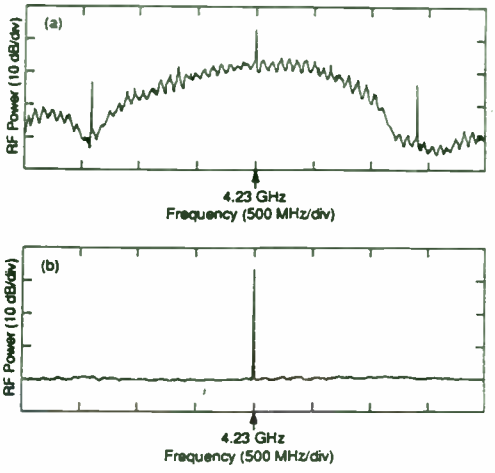


Fig 20

CONCLUSION

This paper has shown the link between the biological behavior and electronics networks. Based on the biological criteria and analytical and experimental results, and its succesful and optimal performance in circuits, such as high noise wide bandwidth systems, the following rules were established:

°No other network has higher amplification without distortion than a SO.

°No other network has two independent internal filters.

°No other network has higher noise rejection, for a given tracking range, than the SO

°No other network has an ideal gain function than the SO, while its phase remains linear.

°The SO has no frequency limitation. The same circuit concept can be used at any frequency.

°No other network can detect signals and signal-to-noise ratios lower than the SO.

The detection is limited only by the thermal noise of the circuit elements. As the thermal noise is a function of the bandwidth and the SO looks, at any time, to the instanteneous input data frequency, and not to the total data, as it happens in classical networks, its effect is reduced.

°No other network has an internal sampling process.

°No other network can divide by rational integer number, such as 7/8,3/4,3/5 and 5/3, in a single process and without any frequency limitation.

°The product of any two functions, such as noise bandwidth and tracking range in a SO, can be optimized. Likewise, the products of noise bandwidth and acquisition time can be optimized. No classical network can be optimized.

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SPREAD SPECTRUM TECHNIQUES FOR VIDEO TRANSMISSION

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ABSTRACT

A number of analog video transmission systems have recently become available for short-range, non-licensed applications in the 900-MHz and 2.4-GHz ISM bands. Because these systems use conventional analog transmission techniques and operate without license, their maximum transmitter output power is limited by FCC regulations to a field strength of 50mV/m at 3 meters (equivalent to 0.7 mW on a dipole antenna), providing ranges less than 1000 feet.

The severe range limitation as well as the susceptibility to interference on those systems can be overcome by the use of spread spectrum techniques. FCC regulations allow unlicensed spread spectrum systems to transmit at considerably higher power than conventional narrow-band systems, up to 4 W effective radiated power (ERP). With appropriate video compression techniques, a spread spectrum system can transmit near-live video at ranges up to 100 miles, without the requirement of an FCC license.

This presentation describes a system designed to provide high reliability video transmission, through the use of advanced video compression coupled with spread spectrum interference suppression and avoidance techniques, for surveillance applications in the security, vehicle traffic management and other markets.

INTRODUCTION

This presentation will commence with an overview of the basic principles and advantages of spread spectrum technology, including a discussion of spreading techniques allowed by the FCC and other important performance parameters. This will be followed by a brief discussion of the most common video

compression techniques and standards. Finally, the combination of spread spectrum technology with video compression to form a fully integrated wireless video transmission system, will be described. The performance of such a system will be evaluated and examples of potential applications will be examined.

AN OVERVIEW ON THE ADVANTAGES OF SPREAD SPECTRUM TECHNOLOGY

BACKGROUND

It is characteristic of conventional modulation schemes that they attempt to minimize the occupied bandwidth for a given data rate transmission. A spread spectrum system takes the opposite approach, spreading the signal out over a bandwidth much wider than the data rate. Various methods are used to spread the signal, but common to all spreading schemes is the use of a reciprocal process at the receiving end to "despread" the signal.

Since the spread spectrum system distributes transmitted energy over a wide band, the signal-to-noise ratio at the receiver input is low - in many cases below the noise floor of a conventional receiver and thus invisible to it. However, by despreading, the spread spectrum receiver restores the level of the desired spread signal, it has the opposite effect on narrow-band interferers - it spreads and thereby suppresses them. Thus the despreading process can recover the desired signal even in the presence of narrowband interferers with a much greater power density than that of the desired signal.

This characteristic makes spread spectrum systems useful for secure communications: they suppress interference while making it difficult for any unintentional receiver to detect their own transmissions, extract messages, or jam the intended receiver.

TECHNIQUES OF SPREAD SPECTRUM MODULATION

Two basic techniques are allowed by the FCC for bandwidth spreading, direct sequence and frequency hopping. The FCC also allows the combining of both techniques in a hybrid scheme.

DIRECT SEQUENCE

In a direct sequence system, the baseband data is directly modulated by a much higher frequency spreading signal, referred to as a pseudonoise (P/N) code. The P/N code is a very fast binary bit stream designed to appear random, i.e., a mix

of approximately equal numbers of zeroes and ones. Each P/N code bit is called a chip.

Spreading signal bandwidth should be large relative to the data bandwidth to ensure that signal bandwidth is dominated by the spreading signal and therefore nearly independent of the data signal.

At the receiving end, the P/N code is duplicated and synchronized for signal despreading and is selected to have properties that facilitate the despreading process at the intended receiver while making demodulation by unintended receivers difficult. These properties also allow the intended receiver to discriminate between the signal and interferes or jammers.

Modulation is usually achieved by a form of digital phase modulation such as binary phase-shift keying (BPSK) or quadrature phase-shift keying (QPSK). Other methods, such as amplitude or frequency modulation, are less immune to interference and compromise privacy, since amplitude modulation can be recovered by an envelope detector and frequency modulation by a squaring device and frequency discriminator.

The interference immunity of a properly implemented direct sequence system is indicated by processing gain which is defined and discussed in a later section.

FREQUENCY HOPPING

In a frequency hopping spread spectrum system, the bandwidth of a data-modulated carrier is spread by periodic changes in the carrier frequency. The amount of time the carrier remains on a single frequency (channel) is called the dwell time; to avoid interfering with conventional users and achieve immunity to interference from conventional user, the dwell time must be very short.

Although not essential to the frequency hopping technique, frequencies are chosen from a set of 2^K frequencies spaced approximately at the width of the data modulation spectrum. The frequency hopping sequence is fixed and is replicated at the receiver where it is mixed with the received signal for despreading.

As presently implemented in commercial systems, frequency hopping offers no processing gain. These systems rely on interference avoidance rather than interference suppression.

HYBRID

A hybrid spread spectrum system is a direct sequence system in which the carrier frequency changes periodically. This offers four advantages:

1) Because it can frequency-hop over a much greater band than it can occupy with practical direct sequence techniques, the hybrid system can use available bandwidth more effectively.
2) By combining direct sequence and frequency hopping techniques, the hybrid system combats interference in two ways: hopping avoids the interference signal part of the time, and when the system hops into the interference band, the interference is spread and filtered by direct sequence techniques.
3) A hybrid system offers the multipath rejection of a direct sequence system. (Multipath rejection is not available in commercial frequency hoppers.)
4) A hybrid system can use the available band with fewer hopping channels than a pure frequency hopper.

Thus by taking advantage of the best features of both techniques, a hybrid system can provide very robust performance.

A system that meets FCC requirements for direct sequence spread spectrum can employ a variant of the hybrid design by hopping selectively. Such a system seeks the channel with the lowest noise and interference and operates on that channel without further frequency hopping as long as interference remains low enough to be combated by direct sequence techniques. When interference exceeds this level, the system will sequence through the hopping channels until it finds the next low-interference channel.

This technique has been selected by Utilicom for the video system implementation which will be described in a later section.

PROCESSING GAIN

Processing gain is the most important parameter of spread spectrum systems since it determines the level of interference suppression that a given system can provide.

Processing gain is a consequence of the reciprocal spreading/despreading process in a direct sequence spread spectrum system. The receiver correlates the signal with its locally generated P/N code; when the two signals are matched, the data signal is despread to its original bandwidth, while unmatched signals are spread to the P/N code bandwidth. In other words, the receiver enhances the desired signal while suppressing noise and interference, thereby increasing the signal-to-noise ratio of the output signal over that of the input signal. The ratio of the output and input signal-to-noise ratios is defined as processing gain.

In a properly implemented direct sequence spread spectrum system, processing gain can be estimated by the equation

$$\text{processing gain} = G_P = \frac{BW_{RF}}{\text{data rate}}$$

where BW_{RF} is the bandwidth of the transmitted spread spectrum signal.

ADVANTAGES OF SPREAD SPECTRUM SYSTEM

The performance characteristics just described give spread spectrum systems a number of advantages over conventional systems. These include:

* interference immunity
  Spread spectrum systems can operate reliably in the presence of high-power jamming signals. In addition direct sequence spreading techniques offer effective rejection of multipath signals.
* low interference production
  Spread spectrum signals appear as low-level noise to conventional receivers and may be well below receiver threshold.
* high data rates
  Allowed bandwidth for spread spectrum makes relatively high data rates attainable.
* non-licensed operation at practical power levels
  The FCC licensing process is avoided, and there is now a practical alternative in metropolitan areas where licenses may be unobtainable.

INTRODUCTION TO VIDEO COMPRESSION TECHNIQUES

Spread spectrum is a digital modulation technique and therefore it requires digital data to interface with. In order to accommodate video transmission the analog signals from a video camera have to be digitized. The resulting digital data rates for a broadcast quality live video are typically in excess of 200 Mbits/sec. Those extremely high data rates can not be supported by spread spectrum transmission within the limited bandwidths allocated by the FCC.

Fortunately, advanced and well proven video compression techniques currently available can substantially reduce the data rate requirements thus making spread spectrum a viable video transmission technique. Compression ratios in

the range of 200:1 are common today and compression ratios as high as 500:1 have recently been reported claiming insignificant picture quality degradation.

Taking into account those high compression ratios, live video could be transmitted at less than 500 Kbits data rate.

Furthermore, considering that live video is not necessary for many surveillance applications, additional data rate reductions are possible. For example, video security surveillance at 5 to 10 frames per second could be quite an acceptable rate making it feasible to use transmission data rates in the order of 100 Kbits/sec. Those data rates can be accommodated quite well with spread spectrum equipment and, as it will be shown in a later section, reliable communication ranges up to 100 miles can be achieved.

Therefore, since we have established the strong viability of spread spectrum technology for video transmission we will next briefly discuss the various video compression/decompression techniques and standards.

COMPRESSION/DECOMPRESSION CHOICES

The numerous available techniques are discussed below:

SOFTWARE-ONLY VS. HARDWARE ASSISTED

Software-only compression uses a computers' CPU to deliver low quality, windowed (usually 1/16 to 1/4 screen) and less than full motion (about 15 to 30 frames per second) video on fast Intel 486 or pentium platforms.

Hardware assisted compression uses add-on hardware boards with dedicated and extremely fast video DSP chips in order to improve picture quality or reduce data rate requirements for the same picture quality over software-only techniques.

INTERFRAME VS. INTRAFRAME

The interframe technique uses combinations of key, motion-predicted and interpolated frames to achieve high compression ratios and low data rates.

Intraframe systems compress every frame and, sometimes, every field of video individually. These algorithms provide quality video at the cost of higher data rates.

SYMMETRIC VS. ASYMMETRIC

In addition to algorithm types, another issue of compression is the symmetry of the process. With symmetric algorithms, the compression process requires the

same amount of clock time as the decompression. On the other hand, the asymmetric compression process requires considerably more clock time than decompression. Because most of the horsepower is required for compression, asymmetric decompression can be done on low-cost computer equipment.

LOSSLESS VS. LOSSY

Lossless compression is easily understood. If we wish to transmit the four-character string "XXXX," it's sufficient to send the two-character string "4X." As long as the recipient knows to decode these characters as "four X's," no information whatsoever is lost.

Lossy compression involves permanently discarding information during encoding such that it cannot be recovered during decoding.

The goal is to eliminate data undetectable by the human eye or data that can not be reproduced because of limitations of the equipment involved.

Lossless compression can reduce bandwidth requirements for encoding constant color backgrounds, or for video images that change little from frame to frame. Lossy compression eliminates the transmission of indistinguishable pixel-to-pixel differences within one frame or successive frames (that is, it eliminates data that couldn't be reproduced because of the resolution or frame-rate limits of the equipment), and it eliminates color and intensity information that the eye could not detect.

Unnecessary visual information can be identified and deleted by means of the discrete cosine transform (DCT), which pinpoints light-dark-light spatial-frequency variations and helps to determine whether these variations are so closely spaced as to be indistinguishable, either because of limitations of the human eye or the display device.

COMPRESSION STANDARDS

There is a variety of compression standards. The most common ones are JPEG (Joint Photographic Experts Group), MPEG (Motion Picture Experts Group), Wavelet, and Intel Indeo.

MOTION JPEG

This is the most widely used compression technique for video editing even though it does not support audio. It was originally developed for encoding still images, but because video is actually a series of 30 still images per second, JPEG can be used to digitize each frame, then play them back to simulate full-motion video.

MPEG-1 AND 2

With MPEG, audio and video can be compressed through hardware or software. MPEG eliminates the redundant information between frames over time (temporary redundancy), and encodes only the differences (incremental encoding). As a result, each frame is not saved as a single element; to reconstruct a single frame, MPEG must have information from previous frames. Capable of compressing video much more efficiently than JPEG, MPEG uses a lot less bandwidth. Usually, compression is lossy, which is another way of saying that image quality is lost. Also, MPEG is still very expensive although prices are starting to come down.

MPEG-1 uses video transfer rates of 150 Kbytes/s to 600 Kbytes/s and provides compression ratios as high as 200:1, but reasonable image quality is maintained at ratios up to 100:1. It delivers 30 frames/s at a resolution of 352 x 240 NTSC (comparable to VHS image quality) and is used primarily for low-scale video or animation.

MPEG-2 conforms to broadcast quality standards and uses a large amount of bandwidth at (main profile/main level) data rates of 0.5 Mb/s to 2 Mb/s.

WAVELET TECHNOLOGY

Like JPEG, this technique saves each frame individually. However, Wavelet differs from JPEG in that it quantifies information for each frame as a single unit instead of dividing the image into pixel blocks. The artifacts typically found in Wavelet differ from the blocky effects sometimes seen in JPEG when high compression ratios are used. Wavelet suffers from some noticeable image degradation around the edges of objects, which introduce artifacts into details.

INTEL INDEO

This is a software technique that can deliver full-screen, 30 frames/s video playback on standard PCs (Pentium or 486 DX4/100). Indeo compression is relatively inexpensive compared with most other technologies allowing compression to be done in-house. It is not a high-quality image, but the savings when video quality isn't the key factor are usually worth it.

UTILICOM'S "VideoRanger 2000" SYSTEM

GENERAL DESCRIPTION

By utilizing spread spectrum technology, along with advanced compression techniques, Utilicom has developed a fully integrated video system for turnkey installation.

The spread spectrum transceiver utilizes a combination of direct sequence modulation, along with adaptive frequency hopping, to provide a high level of interference suppression. It is capable of handling data rates of 128 Kbits/sec which coincides with the resulting video data rate after compression.

Compression is accommodated by an Intel 486 DX2 platform running at 66 MHz and utilizing 8 MB of RAM. The compression is hardware-assisted by the use of highly integrated VLSIs developed by C-cube Microsystems.

For this first generation system, a lossless symmetric compression technique was selected. However, lossy schemes such as "Wavelet" are currently being investigated for use in the next generation system, in order to provide higher compression ratios.

Utilicom's "VideoRanger 2000" is a two-way system, offering video transmission from the remote site to be monitored to the security station, and command transmission from the security station to the remote site. The command link allows remote camera selection and control.

The image resolution is user selectable from 96 x 64 to 384 x 288 pixels. Frame rate is also selectable and can be traded for picture quality. The standard system has inputs for 4 cameras and can be easily upgraded to service up to 32 cameras by the addition of a plug-in board. A user friendly icon-based interface is provided.

To further enhance the reliability and robustness of the "VideoRanger 2000", Utilicom has developed and incorporated on this system certain unique interference suppression and avoidance technique described in the next section.

INTERFERENCE SUPPRESSION AND AVOIDANCE TECHNIQUES

Spread spectrum systems must share the bands assigned by the FCC with a number of other services which have the potential to produce high interference levels. Furthermore, the ever increasing use of those bands would require robust spread spectrum equipment that will continue to perform reliably as band congestion increases in the future. The primary interference suppression

technique is the processing gain of the system; however, under severe interference conditions, a system with a fixed processing gain may not be adequate in overcoming such levels of interference.

Therefore, Utilicom has developed certain additional techniques to successfully resolve high interference problems. Those techniques described below provide significant interference suppression and avoidance and can be implemented primarily in software, thus reducing the recurring-cost burden to the commercial user.

ADAPTIVE CHANNEL SELECTION

Adaptive channel selection is a means of adding "frequency hopping" to a direct sequence system, allowing the system to select automatically and dynamically the best communication channel at any time.

A manual implementation of this technique is widely recommended by spread spectrum manufacturers, who suggest that the user examine the ISM band with a spectrum analyzer in order to select the channel with least interference. The problem with the manual technique, though it is better than blind channel selection, is that interference conditions are dynamic. There is no assurance that a quiet channel will remain quiet in the long term, or even in the sort term, since conditions can change moment by moment.

The solution, of course, is to automate channel selection. The process works as follows: The system initially selects a quiet channel and continues to operate in that channel as long as the bit error rate (BER) is within acceptable limits. If BER limits are exceeded, the system automatically seeks another channel.

Coordination of channel selection among all radios in a network imposes some burden on data rate, but efficient algorithms can minimize the overhead. However, this overhead is already minimized for point to point communications, which are typical in video surveillance applications.

ADAPTIVE PROCESSING GAIN SELECTION

Adaptive processing gain provides software control of processing gain, optimizing data throughput while providing the required interference suppression. This technique operates as follows: Before transmitting data, the receiving station measures the interference level in the selected channel and determines the processing gain required for successful data transfer. The station then transmits a code specifying the selected processing gain to the transmitting station, which adjusts itself accordingly. Since processing gain is inversely proportional to data rate, this technique maximizes data rate by reducing processing gain to the minimum required level.

IMPLEMENTATION OF ADAPTIVE CHANNEL AND PROCESSING GAIN SELECTION FOR THE " VideoRanger 2000"

The I.F. (Intermediate Frequency) bandwidth of the video receiver is approximately 1 MHz. Therefore, there are 83 non overlapping channels available in the 2.4 GHz band, to be selectively used depending on interference conditions.

At power turn on, the system automatically tunes to a preset channel and will remain on this channel until interference exceeds the jamming margin of the receiver.

Interference is detected by a bit error detector with presentable threshold. If the bit error rate exceeds the threshold setting, the system automatically searches for a quieter channel.

Channel search is fast enough so that switching to a nearby channel is imperceptible, and maximum search time is less than 1 second. If interference across all channels reaches levels that cannot be suppressed with the preset processing gain, processing gain is automatically increased at the expense of data rate. However, the system will still remain operational even if the full band is jammed. The penalty paid will be a reduction in the frames per second being transmitted. Therefore, the implementation of those techniques yields a very reliable system capable of surviving the most adverse interference conditions.

COMMUNICATION DISTANCES OF THE "VideoRanger 2000"

The "VideoRanger 2000" can provide respectable communication distances despite the fact that it is a non-licensed system.

To maximize the communication distance capability, Utilicom utilizes a technique that totally eliminates the coaxial cable losses affecting neither the maximum power output allowed by the FCC nor degrading receiver sensitivity.

Antenna feed line losses can be eliminated by including the transmitter's power amplifier and a low-noise receiver amplifier as part of the antenna assembly. Any line losses between the amplifiers in the antenna and the remainder of the radio system are easily compensated by a bi-directional automatic gain control circuit. Thus the full power output of 36 dbm is transmitted.

The receiver's sensitivity is -100 dbm at 10^{-6} BER. This respectable sensitivity is attributed to a very low noise GaAs FET integrated with the antenna.

The antenna utilized is a combination of patch, Yagi, backfire yielding a compact light weight, and low cost assembly with an 18 dbi gain at 2.4 GHz.

With those parameters we will calculate the overall system gain.

System gain = transmitted ERP + Receiving antenna gain + receiver sensitivity

System gain = 36 dbm + 18 dbi + 100 db = 154 db

Allowing a 20 db fade margin yields a 134 db practical system gain.

Free space attenuation is calculated as:

$A = 20 \log D + 20 \log F + 96.6$

where A- attenuation in db
D-distance in miles
F-frequency in GHz

or $134 = 20\log D + 20\log 2.45 + 96.6$

$D = 30.2$ miles

Therefore, a 30 mile range can be accommodated with a 20 db fade margin.

The distance can be further increased by using parabolic antennas. A 4 foot dish will provide a 27 dbi gain at 2.4 GHz. Of course, with the higher antenna gain the transmitter power will have to be reduced to 9 dbm in order not to exceed the 36 dbm FCC limit.

Repeating the above calculations, the maximum communication distance with 20 db fade margin will be 85 miles.

Communication distance can be further increased by lowering the data rate, if a lower frame rate can be acceptable. At a data rate of 64 Kbits the receiver sensitivity will be -103 dbm. With this additional receiver sensitivity and utilizing a 27 dbi dish the maximum communication distance will be 120 miles.

Therefore, the limiting factor in accommodating long range communications is not the system gain but rather the capability to erect high enough towers to overcome the radio horizon limitation to attain line of sight conditions.

APPLICATIONS OF THE "VideoRanger 2000"

The "VideoRanger 2000" can efficiently service several applications where wireless video surveillance requirements exist. It can be extremely useful in two major markets, Security Systems and Traffic Control Management. It can provide essential services in applications where ISDN lines are not available or where the user wishes to avoid ISDN lease costs.

The "VideoRanger 2000" can either be used in a wireless point to point stand alone configuration or it can be interfaced with an ISDN line to provide "last mile" connectivity to a remote location.

For security surveillance applications it can be interfaced with motion sensors to provide an alarm when motion is detected, thus alleviating the burden of continuously watching a video monitor.

For traffic surveillance applications it can be interfaced with specialized hardware/software to count the number of vehicles crossing an intersection, thus replacing conventional traffic counters. Furthermore, it can also be used as a vehicle license number reader.

These are a few examples of the potential of this system. Its applicability is only limited by the users imagination.

CONCLUSION

By taking advantage of the latest video compression and spread spectrum techniques, Utilicom Inc. has developed a wireless video transmission system offering the capability of long range (up to 100 miles) reliable video transmission, without requiring an FCC license.

The "VideoRanger 2000" offers excellent jamming resistance capabilities. It outperforms all other non-licensed wireless analog video transmission systems which only offer up to 1000 feet of range and suffer from susceptibility to interference as well as deliberate jamming.

It is expected that this system will be widely used in numerous applications where reliable wireless connectivity is mandatory and in applications where it is desirable to avoid fees for leased lines.

Digital Direct-Sequence Spread-Spectrum Receiver Design Considerations

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Digital direct-sequence spread-spectrum receivers have application in a variety of wireless systems including cellular, PCS, cordless phones, wireless LANs, and GPS. The three key receiver design trades are bandlimiting, sampling, and quantization. This paper provides a tutorial discussion of each trade and establishes the relationships between the design parameters and correlation loss, which is the figure of merit for a spread-spectrum receiver.

Functional block diagrams are included for digital receivers implementing lowpass, integer-band, and quadrature bandpass sampling. Detailed descriptions and spectrum diagrams are provided for each technique.

The relevant design parameters are bandlimiting bandwidth, sampling rate, number of quantization levels, and AGC setting. Design curves are provided for correlation loss as a function of sampling rate for various bandlimiting bandwidths, and as a function of AGC setting for various numbers of quantization levels.

Real world component specifications that effect correlation loss are discussed. These include non-rectangular filters, filter passband ripple and phase non-linearity, finite sampler aperture, and quantizer non-symmetry and hysteresis. Both theoretical and simulation results are presented.

Time Division and Spread Spectrum Access Methods for PCS

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Multiple access methods should efficiently use the limited bandwidth of the digital microcellular personal communication networks. Minimum cost and maximum performance are among the major concerns in cellular/microcellular network design. Time Division Multiple Access (TDMA) method is the classic approach and Code Division Multiple Access (CDMA) method is the new spread spectrum solution. Frequency Division Multiple Access (FDMA) is not a proper choice for PCS. TDMA is used in digital cellular systems such as GSM (Europe), IS-54 (North America), PDC (Japan), DECT (Europe), PHS (Japan), WACS and PACS. Characteristics of TDMA and CDMA are compared in this paper and advantages and disadvantages of each method are discussed.

Comparisons of TDMA and CDMA systems are usually done based on different assumptions and different systems in different evolutionary stages. If we were able to have optimized and ideal systems, we would come up with the conclusion that these methods have almost similar capacities. However, the capacity can have two meanings. Cell capacity is defined by radio link performance and its carrier-to-interference ration (C/I) for a given quality. Two factors that affect the cell capacity are modulation efficiency and frequency reuse. System capacity talks about the capacity of group of cells and relates to the cell size. When cell size decreases, the system capacity increases. The number of users supported for a given bandwith is another capacity measurement factor.

Since different cell sizes are needed to cover different capacity demands, the Hierarchical Cell Structure (HCS) is introduced. The Adaptive Channel Allocation (ACA), Frequency Hopping (FH), or Random FH (Slow or Fast FH) are used to increase the cell capacity. These methods have their own benefits and problems. Another issue is Mobile Assisted Hand-Off (MAHO) which is used to enable the mobile to work with different RF-Carriers.

Each approach has its solutions for delay spread and time dispersion resulted from multipath propagation. Multipath delay spread can be solved by adaptive equalization. Decision Feedback Equalization (DFE) or Maximum Likelihood Sequence Estimation (MLSE) are methods used to solve this problem. Antenna diversity reception and channel coding are other issues involved in the design of these multiple access systems.

Some of the modulation schemes used in these systems are QPSK, Differential QPSK (used in IS-54, PDC and PHS), DAPSK, star QAM, Gaussian Minimum Shift Keying or GMSK (used in GSM and DECT).

Some of the important characteristics of Direct Sequence CDMA are frequency reuse, power control, soft handoff, coding, Multiple Access Interference (MAI), and Antenna gain. Issues involved in frequency hopping of CDMA are total interference, reverse link, near-far problem, external jamming, and frequency agility. IS-95 standard and Broadband CDMA address the standards in this area. Interoperation of terrestrial and satellite based PCS systems is another issue of concern.

A Direct Sequence Spread Spectrum Chip

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Abstract

This paper presents a direct sequence spread spectrum baseband chip, implemented in CMOS. It includes both the transmitter and the receiver digital parts.

The chip is made for homodyne radio architecture and it has a simplified switching detection scheme which takes care of the error frequency between the transmitter and the receiver oscillators. The circuit is designed for a maximum sampling speed of 51.2 MHz and a maximum bit rate of 2 Mbit/s.

1 Introduction

The design of flexible and efficient future high data rate mobile communication systems such as e.g. the Walkstation concept [4], is a major challenge due to the inherent complexity of underlying algorithms and to the harsh radio environment in which these systems will operate. Even though VLSI technology continuously allows increasingly complex systems to be integrated into single chip solutions, simplifications of the existing communication algorithms are needed to allow implementation.

In this work, we present our CMOS standard cell design of a digital transceiver for a direct sequence spread spectrum (DS SS) radio targeted for 2 Mbit/s cellular data communication. Most of the design which now has been implemented in an ASIC is based on our earlier work, which is reported in references 5 to 8. The receiver architecture is thoroughly tested both with simulations and an FPGA based prototype [8]. The circuit architecture presented in this paper is for a digital baseband modem for a direct sequence spread spectrum (DS SS) [1 - 3] radio link for high data rates. In figure 1, a simplified block diagram of a DS SS link is shown. The binary information sequence *b(t)* is multiplied with a code sequence *c(t)* and a radio frequency (RF) carrier signal. The binary code sequence is a pseudo random noise (PN) sequence with a rate R_c which is usually much larger than the rate R_b of *b(t)*. The quota $L_c = R_c/R_b$, which often is referred to as the spreading gain or spreading factor, can also be seen as the bandwidth expansion factor - that is, L_c times more bandwidth than necessary is employed to transmit the data sequence *b(t)*. In the receiver, the down-converted signal is decorrelated in a filter matched to the PN-sequence *c(t)* (in the following abbreviated MF), and after that a binary decision is made.

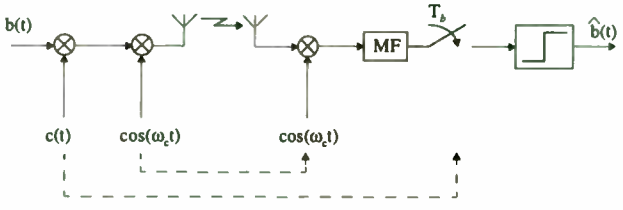

Figure 1. A simple direct sequence spread spectrum system, where the dashed arrows symbolize some kind of synchronization.

2 System overview

The radio system

In figure 2, the radio including the analog frontend is shown as it is targeted in this work. On both the transmitter (Tx) and receiver (Rx) side, homodyne mixing is used, meaning that the conversion to/from RF is done directly from/to baseband. Furthermore, the local oscillators (LO) of a communicating transmitter and receiver are not locked to each other in the targeted system; thus, this frequency incoherence must be handled by the digital transceiver. We propose differentially encoded binary phase shift keying together with so called switching BPSK (SBPSK) [7] detection as a solution to this problem due to its inherently limited complexity.

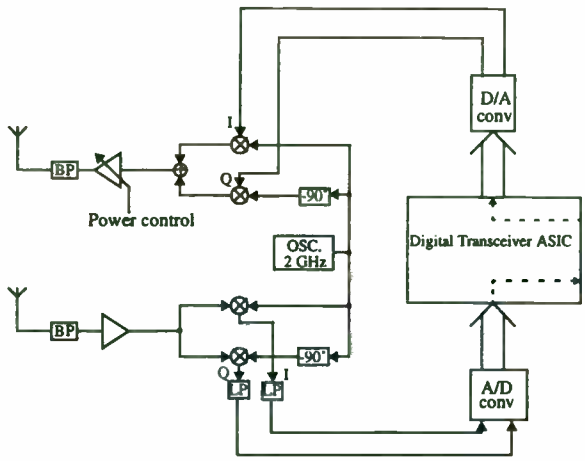

Figure 2. The radio with its analog frontend.

The transceiver circuit has at the top hierarchical level three main entities: the transmitter and receiver, which form two independently operating units driven by different system clocks. They are described in more detail below. The third part is a slow speed control block, which handles reading and writing from/to the circuit, and this is done via an 8-bit in/out bus. This enables reconfiguration of e.g. the PN-sequence (currently any sequence of length between 5 and 128 PN-bits/bit can be used).

The baseband transmitter

The transmitter's overall task is to differentially encode information symbols and to do PN-sequence modulation. Its structure is shown in figure 3. First, the incoming information bits $b^{(k)}$ are mapped to BPSK symbols $u^{(k)}$ according to table 1.

After differential encoding according to

$$d^{(k)} = u^{(k)} \cdot d^{(k-1)} \qquad \text{Eq (1)}$$

the signal is multiplied with the PN-sequence $c(t)$ and with a constant A which results in

$$s(t) = A \cdot d^{(k)} \cdot c(t) \text{ , for } k \cdot T_b \le t < (k+1)\, T_b \qquad \text{Eq (2)}$$

This signal is then fed to the I and Q off-chip D/A converters as shown previously in figure 2.

Table 1: BPSK

$b^{(k)}$	$u^{(k)}$
'0'	1
'1'	−1

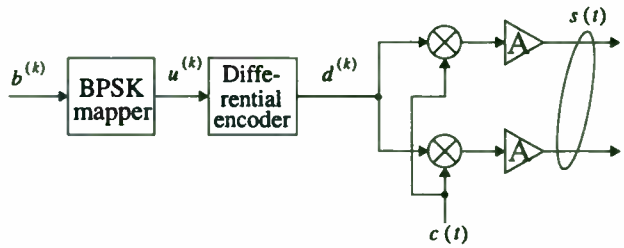

Figure 3. The baseband transmitter.

The baseband receiver

The received signal which is seen at the output of the A/D converters in figure 2 may be modelled as

$$r(t) = \alpha \cdot e^{j\theta(t)} \cdot s(t) + n(t) \qquad \text{Eq (3)}$$

where α is the channel attenuation factor, $\theta(t)$ an unknown phase, which is due to system imperfections such as a difference frequency between the transmitter and receiver LOs, and $s(t)$ the transmitted signal (eq. 2). The noise $n(t)$ is here modelled as complex-valued WGN. In the receiver, $r(t)$ first needs to be demodulated, in e.g. a matched filter, after which detection of the transmitted symbols can be done. In figure 4 we see how a partitioning of the receiver into a "matched-filter-equivalent" part and a detector is done on our receiver architecture..

Synchronization

One of the non-trivial problems one must face with a DS CDMA system is the synchronization of the PN sequence in the receiver[1]. Different solutions have been studied and proposed. A matched filter is one way of doing this, the filter will output a pulse as the PN sequence matches the PN sequence stored in the filter constants. A delay locked loop [2] is another way of doing this, the received signal is multiplied with three

1. Each bit is modulated with exactly one cycle of the PN-sequence; this means that having PN-sequence synchronization implies having bit synchronization.

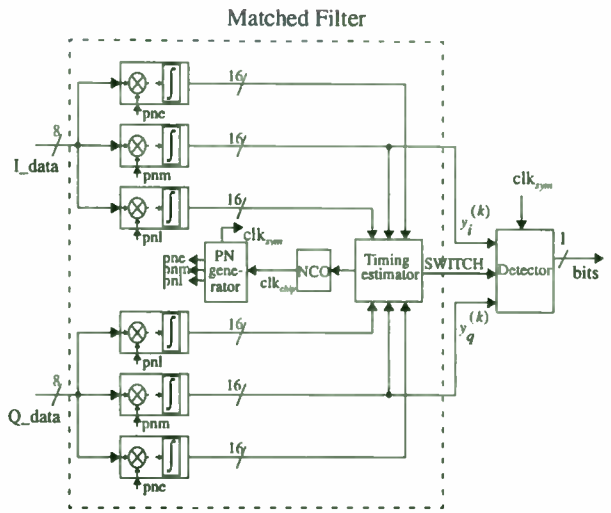

Figure 4. The baseband receiver.

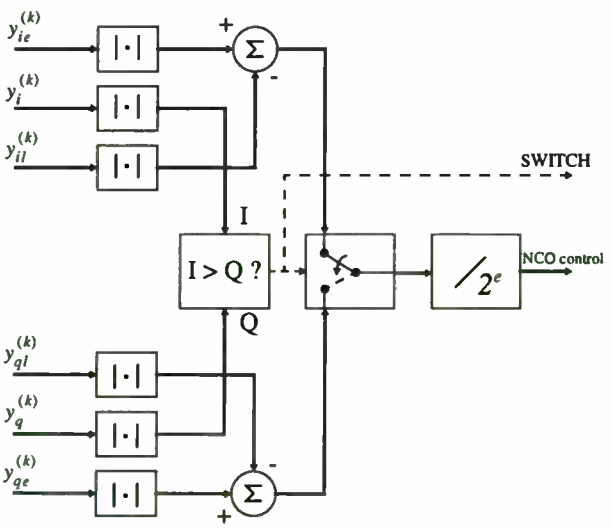

Figure 5. Block diagram of the timing estimator.

replicas of the PN sequence, which are shifted by half a chip in time from each other. We have selected this method due to its inherent simplicity for VLSI realization.

As shown in figure 4, the data is extracted from the incoming samples correlated with the middle PN sequence. The incoming samples are also correlated with a late and a early variant of the PN sequence, and by taking the difference of those we get an estimate of the timing error (see fig. 5). This signal is fed back to a numerical controlled oscillator (NCO) which generates the chip clock for the PN generator. The NCO is the digital variant of the Voltage Controlled Oscillator (VCO). It consists of a phase accumulator where the output frequency is $f_{out} = f_c \left(a/2^m \right)$ where m is the number of bits of the NCO and f_c is the clock frequency. The output frequency is controlled by the parameter a.

Detection

With the receiver partitioned as in fig. 4, the detection can be treated as a an independent problem. Therefore, the discussion which follows below is applicable to other D-PSK modulated systems, not depending on the MF structure. Let us denote the I and Q outputs of the matched filters $y_i^{(k)}$ and $y_q^{(k)}$ respectively. We now form the complex symbol sample $y^{(k)}$ as

$$y^{(k)} = y_i^{(k)} + jy_q^{(k)} \qquad \text{Eq (4)}$$

With the input to the MF described by (3), $y^{(k)}$ can after some straight forward calculations be shown to be

$$y^{(k)} = \alpha \cdot A \cdot d^{(k)} e^{j\hat{\theta}_k} + n^{(k)} \qquad \text{Eq (5)}$$

where the index k implies that the variables now are time discrete. If $\hat{\theta}_k = 0$, which would imply coherent demodulation, we see that $y^{(k)}$ is just a scaled and noisy version of the transmitted symbol $d^{(k)}$, and it could therefore easily be decoded. However, $\hat{\theta}_k$ can not be assumed to be zero, and it can not even be assumed to be constant in time due to the fact that the local oscillator of the receiving radio is not locked to the local oscillator of the transmitting radio.

This phase error changes with the difference between the transmitter and the receiver oscillator frequency. Since we have differentially encoded all data, we can use a simple scheme of simply selecting the channel which has the highest amplitude. This will work as long as the difference in frequencies is much lower then the bit-rate.

If ω_{diff} is equal to the frequency difference of the transmitter and receiver local oscillator, then, $\hat{\theta}_k$ can be expressed as

$$\hat{\theta}_k = \omega_{diff} \cdot T_b \cdot k \qquad \text{Eq (6)}$$

where T_b is the bit-time.

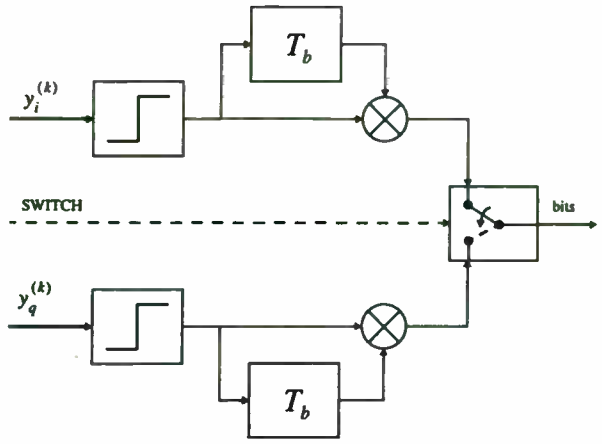

Figure 6. Block diagram of the detector.

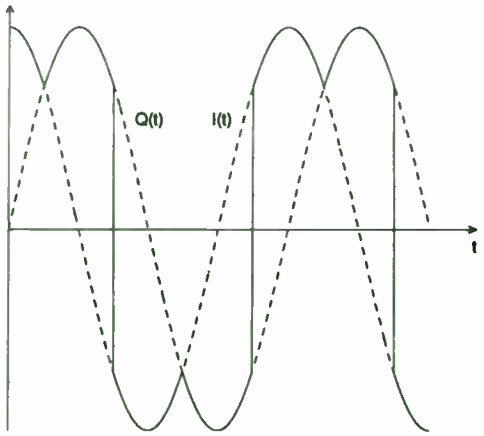

Figure 7. The thick line shows the received signal after the selection between the two branches.

The I and Q outputs from the matched filter will then be

$$y_i^{(k)} = d^{(k)} \cdot \cos(\omega_{diff} \cdot T_{bit} \cdot k) \qquad \text{Eq (7)}$$

$$y_q^{(k)} = d^{(k)} \cdot \sin(\omega_{diff} \cdot T_{bit} \cdot k) \qquad \text{Eq (8)}$$

Based on which of these has the largest magnitude we choose to extract the information from that branch. The decision process is shown in figure 7. The drawback of this algorithm is that since we use only the I **or** Q branch and not a combination of I **and** Q branch, some information which could be used to decrease the error rate is lost.

The performance of this detection scheme, which we call SBPSK (Switching BPSK), in a WGN (White Gaussian Noise) channel has been evaluated, and it can be shown that the noise margin decreases more than 3 dB compared to ordinary BPSK modulation. This is illustrated in figure 8, where the BER's for coherent BPSK, coherent SBPSK, and SBPSK with an error frequency of 4% of the bit rate are shown. With a bit rate of 2 Mbit/s, this frequency corresponds to an error frequency of 80 kHz, which corresponds to 40 ppm of a carrier frequency at 2 GHz. This is a realistic demand on the precision of the crystals.

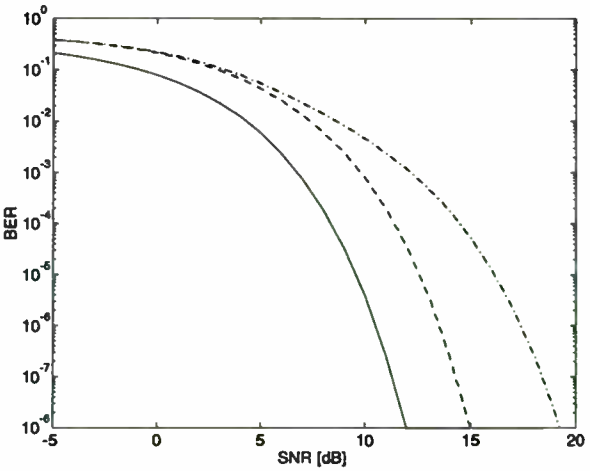

Figure 8. Theoretical BER curves for coherent BPSK (solid), coherent SBPSK (dashed) and SBPSK with an error frequency of 4% of the bit rate (dashed-dotted). The SNR is after despreading.

3 VLSI implementation

The transceiver was implemented in a 0.8 µm CMOS process as a standard cell implementation. The dye size was 16 mm^2 including the bonding pads (see fig. 9).

The most time critical components in the circuit are the accumulators in the integrate-and-dump units. They need to be 16 bit wide to allow addition of as many as 256 8-bit consecutive samples without overflowing, and they must be faster than 20 ns to tolerate a targeted system clock frequency of more than 50 MHz. We could only achieve such performance by using fast carry-look-ahead adders.

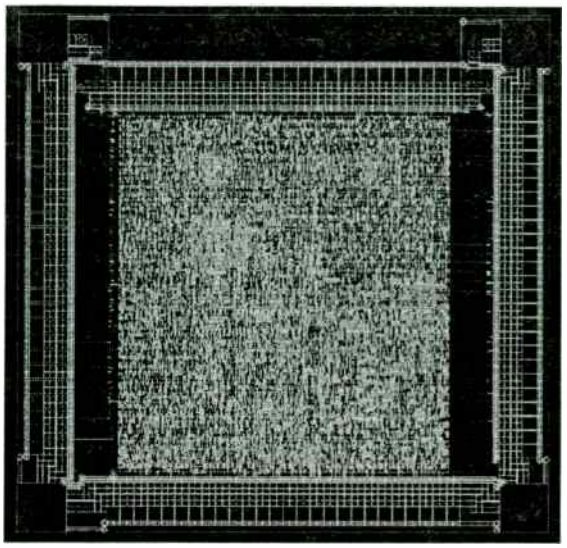

Figure 9. Chip layout of the spread spectrum transceiver.

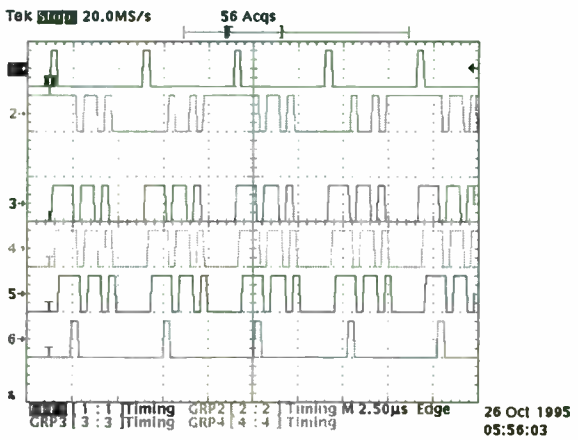

Figure 10. Measurement data. The figure above was obtained from measurements on circuit v0. In the experiment the transmitter data input was tied to logic one. Since the data is differentially encoded the output phase changes 180 degrees at every bit interval, which can be seen in curve two. In the test setup this signal is connected directly to the receiver input. Curves three, four and five are the locally generated replicas of the same PN code used in the transmitter. As can be seen in the figure, they are correctly synchronized to the incoming data and are interspaced by half a chip period.

4 Results and Measurements

After processing, the chip was packaged in a 120 pin PGA package. In order to test the circuit without an ASIC-tester the chip was set up for measurement in such way that the MSB of the inphase output of the transmitter was connected to the MSB of the inphase input of the receiver. The slowspeed interface was connected to the parallel port of a PC and the chip was programmed from the PC after power up. As can be seen in figure 9 the three replicas of the PN-code generated in the receiver are tracking the incoming MSB of the inphase data. The circuit was run on 3.3 V supply voltage and the current consumption was approximately 40 mA at the maximum clock frequency which was measured to 70 MHz.

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A Mobile Spread-Spectrum System for Reliable Indoor Communications

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Abstract:

A need exists for reliable indoor data transmissions in industrial environments. These correspond to low to medium data rate applications (10-500KBps), such as industrial or medical data communications, demanding reliable data transmission in electromagnetically harsh environments. Measurements of radio propagation were made at different industrial sites such as administrative buildings, airport terminals, hospital sites, and gas station areas. Results showed that reliable transmissions through partitions and walls, as well as through reinforced concrete were possible with the use of spread-spectrum.

Based on this, a prototype of a direct-sequence spread-spectrum transceiver was studied and implemented in the ISM band of 2.4-2.5 GHz using differential QPSK modulation, a flexible chip rate up to 11 Mchips per second, and a data rate up to 2 Mbits per second.

Measurements were made in a modern office building at different locations. The results of transmission without automatic repeat request (ARQ) show a BER of 10-5 or less in the majority of the cases, and 10-3 in harsh transmission conditions.

A fully bi-directional protocol was designed with ARQ. To demonstrate the system's capabilities, two transceiver prototypes were built for an indoor multi-media demonstration comprising the transmission of a digital picture of about 1.3 Mbits through a wall from one station to another in less that 8 seconds. Based on measured error profiles, an appropriate forward error correction scheme was selected.

The possibility of use of the upper layers of the DECT protocol in conjunction with the aforementioned spread-spectrum system has been studied. This will allow mobility functions on top of a physical layer which is more resistant to fading than the DECT physical layer. Although no spectral gains are made, the increased reliability due to spread-spectrum coupled with the network capabilities of DECT render this system attractive.

From Chips to Handheld - Designing a GSM Telephone

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Abstract

Motivated by the worldwide popularity of GSM, PCN and associated standards, ever more electronic equipment manufacturers are considering how to enter this fast growing segment of the digital cellular radio market. This paper describes the essentials elements of handheld design and the support tools available in the design process based on the SIEMENS GOLDplus chip set. Off-the-shelf software modules accelerate the development process, as described with reference to the Optimay GSM Global protocol stack. Finally, an insight into project and resource planning for a GSM handheld project is given.

I. INTRODUCTION

Of all the current standards for digital cellular telephony, the European GSM has without doubt gained the most widespread acceptance. The current growth in existing GSM markets and the opening up of new markets such as PCS in the US, presents tremendous opportunities as well as challenges for the handheld manufacturer. The design of a new GSM (or PCS/PCN) handheld for these markets must meet exacting demands for features, reliability, cost and time-to-market. The latter can be met by careful selection of components, support tools and design partners, thus enabling even new entrants into the GSM handheld arena to come to market on-time with competitive products.

The design and development of a GSM handheld may be divided into development of GSM hardware, GSM software and the integration of the two. Up to a certain stage development runs in parallel, converging prior to GSM type approval. Details of this integration process are discussed in later sections. Hardware development itself may also divided between the development of the baseband and the radio-frequency parts. The latter in particular requires considerable depth of experience and know-how. Evaluation boards and reference designs enable software development to begin ahead of hardware design, thereby reducing development timescales. On the other hand, the complexity of and development time required for GSM software must not be underestimated.

The following sections describe the issues involved in handheld design. Section II describes the factors affecting handheld cost. Selection of a standard chip set both speeds development and lowers costs. Section III presents the SIEMENS GOLDplus chip set, a state-of-the-art standard solution for baseband and RF design. The development of a GSM handheld requires both optimum hardware and software development tools to meet time scales in a rapidly evolving market. Section IV discusses such development tools essential in hardware design based on the GOLDplus platform and Section V addresses the issue of software development.The latter may be accelerated by using off-the-shelf software modules. Munich-based OPTIMAY GmbH offers type-approved GSM software specifically for the GOLDplus chip set with an easily customizable MMI. The Optimay protocol GSM software closes the discussion on software. Finally in Section VI a typical design flow is presented, from component selection through to conformance testing.

II. OPTIMISING HANDHELD COST

The manufacturing costs of a GSM handheld can be broken down approximately as shown in figure 1.

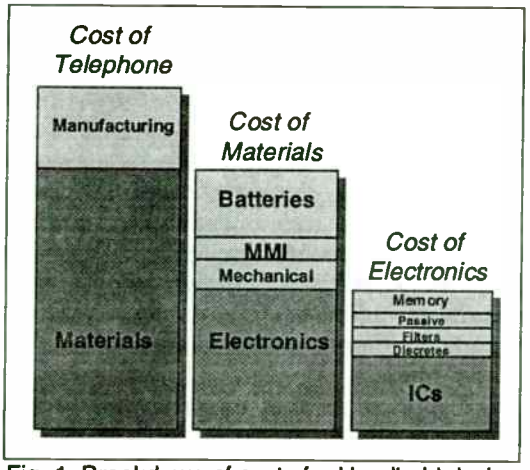

Fig. 1. Breakdown of costs for Handheld design

Manufacturing costs are minimised by a robust, high yield design concept and ease of fast testability. The materials costs of a handheld are detemined to a large extent by the electronics cost. The latter is in turn heavily influenced by the IC cost. Consequently the choice of the IC solution is critical to the optimisation of overall costs of the handheld. However correct choice of the ICs themselves affects systems costs in other ways:

- the level of integration both in the baseband and RF parts, saves on discretes and simplifies the design process.
- battery costs form the second most important constituent in materials costs. A real 3V IC solution contributes to a reduction in cost.
- in the memory part of the electronics cost, flash memory can be saved by employing a code efficient micocontroller in the IC baseband solution.
- Filter costs also can be minimised by selection of a high intermediate frequency, low-pole image filters and relocating as much filtering as possible in the CMOS baseband.

In conclusion, with chip set costs under $50, high feature telephones costing in the range of $150-200 are realistically achievable. One standard chip set exists, which addresses the issues raised above, the SIEMENS GOLDplus chip set discussed in the next section.

III. GOLDplus CHIP SET

SIEMENS Semiconductor has been been active in standard GSM chip sets, since the introduction of the GOLD (GSM One-chip Logic Device) chip set in 1993 and has gained considerable experience through successive generations. A standard chip set proven in design and manufacture, provides an ideal platform for manufacturers requiring rapid entry into the GSM market, whilst meeting the cost issues raised in the previous section. The GOLDplus chip set is the latest generation of standard solutions for mobile communications from Siemens.

GOLDplus shown in figure 2 is a complete IC solution for GSM, PCN and PCS-1900 handhelds. It comprises six chips: 3 baseband ICs and 3 radio frequency ICs. An optional co-processor supports additional functionality such as the half-rate vocoder. The complete chip set operates down to a minimum supply voltage of 2.7V, leading to a significant reduction in battery costs. In addition, the high level of integration reduces the need for external components and optimized interfaces simplify the design process. All components are packaged in state-of-the-art TQFP packages, making them ideal for compact designs or PC-Cards (PCMCIA).

A. GOLDplus Baseband

For a full-rate handset only three chips are required to perform all baseband processing in the GOLDplus chip set: the GOLD-SP signal processor, GOLD-µC system controller and the GAIM. The GOLD-SP (PMB 2707) is a powerful digital signal processor and contains all the necessary algorithms in firmware and implements the channel and speech coding/decoding, equalisation and GMSK modulation. Salient features of the GOLD-SP include the soft-decision decoding and the complex Viterbi equalizer with soft output and the security encryption according to the A51 and A52 ciphering algorithm. Moreover, all digital filtering needed for the baseband and voiceband processing is performed on chip. All data services set down in the GSM specifications are supported by the GOLDplus chip set, which is also prepared for the future GSM developments, such as the extended GSM bands and the half-rate algorithm.

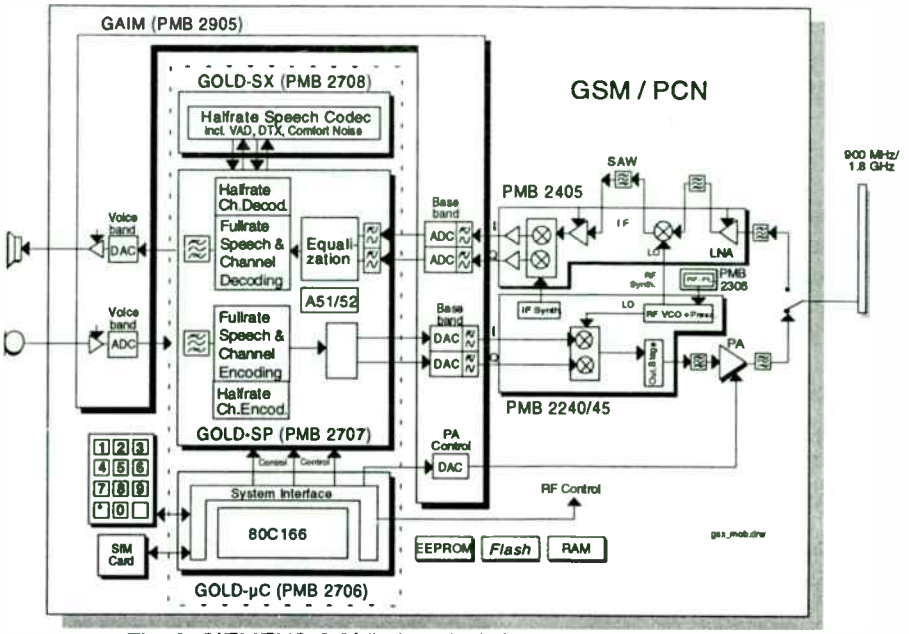

Fig. 2. SIEMENS GOLDplus 3V Solution for GSM Handhelds

At the heart of the GOLD-µC (PMB 2706) lies a powerful 16-bit microcontroller (80C166) enabling the GOLDplus chip set to deal with tremendous complexity of the GSM/PCN protocol stack and attain the high-processing speed required in real-time operation. In addition its highly efficient instruction set, allow very high code densities to be achieved, thus reducing memory requirement, as discussed in Section II. The controller is identical to that used in the present SIEMENS GOLD solution ensuring code compatibility with existing systems. Additional flexible power saving features for minimizing current consumption have been added to the controller functionality. A 2 MByte address space for code and data facilitates the implementation of high-end man machine interfaces (MMIs) and added value. Finally, the system interface block incorporates the complete system control including all timing functions and RF control as well as the control of peripheral modules, such as the SIM card and the keypad.

The GSM Analog Interface Module (GAIM) (PMB2905), the third chip in the GOLDplus chipset baseband solution, implements all the baseband and voiceband analog-to-digital and digital-to-analog converters. An additional converter is provided on the GAIM for conversion of the RF power control signal. The baseband A/D-converters can be optionally used for battery supervision. This cost-saving feature removes the need of an additional ASIC for this particular function.

GOLDplus is intended as a flexible platform, with which extensions to the GSM specifications can easily and quickly be addressed. For this purpose a co-processor, the GOLD-SX (PMB2708), which communicates directly with the GOLD-SP, provides the necessary power. The GOLD-SX is currently supplied with firmware required for half-rate voice coding and an implementation of the enhanced full-rate algorithm for PCS is also in development.

B. GOLDplus RF

In the GOLDplus chipset, all the required RF functions for a GSM telephone are integrated in 3 RF IC's: a transmitter, a receiver and a phase-locked loop. The transmit and receive functions are implemented in Siemens' world class B6HF high-frequency bipolar process technology. Devices manufactured in B6HF technology (with f_T >26GHz) offer significant advantages with respect to noise figure, gain, linearity, input sensitivity and power consumption. Furthermore, the use of B6HF allows for true 3V (+/- 10%) operation in the RF front-end. GOLDplus RF solutions are not only available for GSM (PMB 2240, 2405), but also for DCS-1800 (PMB2245, 2407) and DCS-1900 (PMB 2247, 2407).

The transmitter circuit PMB2240 integrates the complete transmit path of a GSM phone as well as part of the frequency synthesis. It includes a direct modulation vector modulator with high output-level and on-chip phase-shifting circuitry. This modulator builts upon the highly successful PMB 2200, which was used in many of the 1st and 2nd generation GSM telephones.
Off-set frequency synthesis is used in GOLDplus to reduce the filter-cost and limit on-chip interference. To support the frequency synthesis, the PMB 2240 integrates an off-set mixer, the IF-PLL, an RF VCO and the RF prescaler.

The 2.7V high performance CMOS PLL, PMB 2307, completes the RF synthesizer functions of the PMB 2240. This PLL, designed with the demands of mobile telephony in mind, offers state-of-the-art phase-noise performance and is used in many GSM telephones.

The receiver PMB 2405 implements a complete single heterodyne receiver . It includes a gain-switchable LNA, the 1st mixer, programmable IF gain stages with 80 dB of digitally programmable gain in 2dB steps, the IF VCO, a vector demodulator and sample-and-hold interface to the A/D converter. The architecture has been chosen to keep external component count to a minimum and support high IF values to enable the use of smaller and cheaper filters.

III. HARDWARE DEVELOPMENT

Use of evaluation boards and development tools are an indispensable part of the development process. In this section the evaluation boards for the SIEMENS GOLDplus chip set are presented, together with hardware and software development tools.

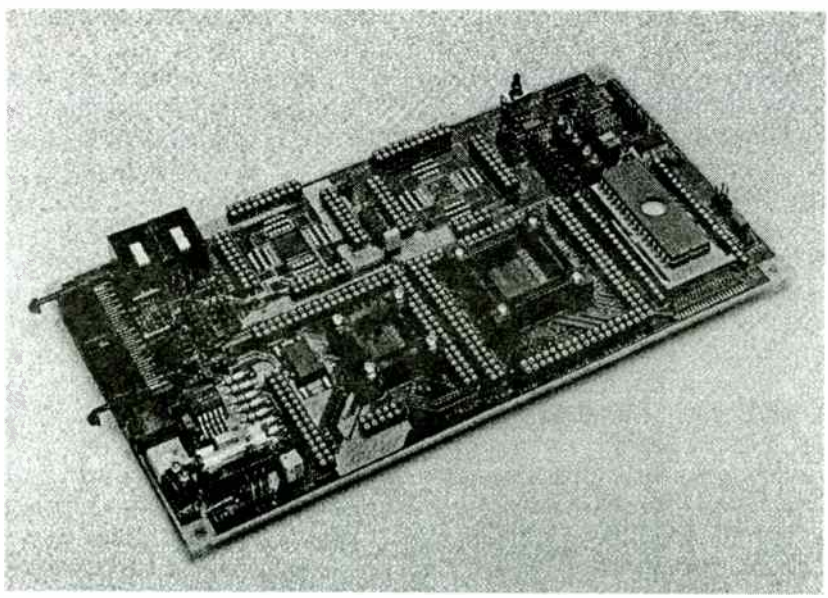

Fig. 3. GOLDplusX GSM Baseband Evaluation Board

A. GOLDplus Evaluation System

The GOLDplus chip set is supported by an evaluation system comprises all parts of a GSM full rate and half rate handset. It consists mainly of the GOLDplusX GSM Baseband Board and the GOLDplus GSM RF Board.

The GOLDplus Demo System permits evaluation of all features of the GOLDplus chip set, both for the baseband as well as the RF part. By adding the PMB 2708 half-rate coprocessor the baseband may be upgraded optionally to half-rate operation. Critical parameters like power consumption or equalizer performance can be measured. Cost estimations for a customer handset can be based upon the bill of materials of the boards.

Furthermore the evaluation system serves as a starting point for customer hardware design by giving a guideline for connectivity and layout and by providing valuable application hints.

1) GOLDplusX Baseband Board

a) Description

The GOLDplusX board (figure 3) has been designed to give maximum flexiblity to customer requirements without sacrificing performance. It combines a compact near-prototype design with the flexibility to alter the board to meet different customer periphery configurations. A wide variety of memory devices e.g. FLASH memories can be adapted to the available headers.

All serial interfaces including the GSM specific DAI are easily accessable for debugging, data transfer or type approval respectively. Furthermore the GOLDplusX board gives access to all chip set pin signals thereby permitting efficient in-depth debugging and problem diagnosis.

No external passive components are required for connection of the keypad and chip card. Interfacing to an intelligent display is straightforward. Only very few passive components are required on the audio interface.

b) GOLDplusX as a Software Development Platform

GOLDplusX board permits the handheld designer to start GSM software development rapidly without having to wait for his own board prototypes. It provides an optimum debugging platform not only for the GOLD-µC C166 system controller but also for the GOLD-SP, if additional customer specific features have to be implemented in DSP firmware. For debugging of customer prototype boards and first software version it can serve as a reference. Furthermore it usually offers valuable additional debugging features compared to the more production oriented customer prototype board.

Besides getting acquainted quickly with the baseband functionality the board permits easy and complete control of RF chip set using the GOLD-µC controller functions. This is especially useful for evaluation and fine-tuning of the RF board functionality.

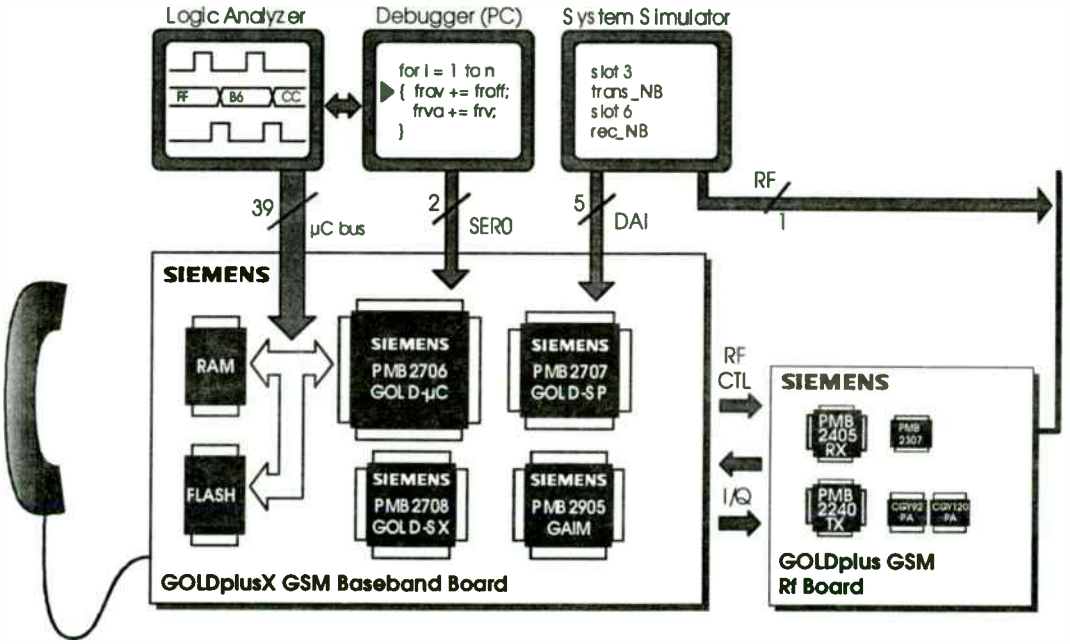

Fig. 4. GOLDplusX Board and GOLDplus RF Boards with Debugging Interfaces

A *Getting started* software package containing basic routines for all hardware and firmware functions is available with the GOLDplusX board. Basic routines for RF control are also part of this package.

2) GOLDplus RF Board

The GOLDplus RF board (figure 4) provides an evaluation platform for IC's, filters, power

amplifier, filter performances. Designed to match closely the RF parameters specified by the GSM 05 series (ETS 300 57x), its quality will be sufficient for first phase baseband integration and tests.
Using the GOLDplus RF board, the time consuming and costly task of investigating all the RF sections (transmitter, receiver, power amplifier) separately, before integration in a single layout, is removed from the development process.

a) Board Design
The complete RF board design is packed onto a 4 layer FR4 printed circuit board the size of a credit card that fits into commercially available handies. This near-optimized size has been chosen to still allow visually distinguishing of the power-, transmit- and receive-blocks. Further optimization can be done according to the individual needs of the manufacturer.

b) Transmitter Section
The GOLDplus GAIM (PMB2905) converts the digital I /Q baseband signals from the GOLD-SP into an analog signal, which is fed into the modulator inputs of the PMB 2240, where it is directly modulated onto the end-frequency. The use of balanced structures throughout the PMB 2240, optimize for high LO-rejection, intermodulation products of even order and common-mode noise. The direct modulation has the advantage of saving filtering at the IF-frequency.

c) Receiver Section
The signal received from the antenna directly enters the on-chip low noise amplifier, which is the first gain block in the receive path of the mobile radio. After external filtering the double balanced RF signal is down-converted to an intermediate frequency (IF) by the first mixer. The IF signal is then filtered externally in a low loss SAW filter B4579 to perform rough channel selection with 40dB adjacent channel rejection 400 kHz away from the carrier. After filtering, the signal is fed into the digitally programmable gain control block (PGC), that allows for 80 dB gain programmable in 2 dB steps. Finally the amplified IF signal is demodulated and passed to the GAIM. Active on-chip baseband filtering before the AD converters provides additional adjacent channel rejection 200 kHz away from the carrier.

d) Frequency synthesis
The use of the on-chip RF VCO and RF-prescaler of the PMB 2240 requires only one external PLL (PMB 2307) to realise the offset RF frequency, whereas the IF-frequency can be realised using the IF-VCO (PMB 2405), the IF-PLL (PMB 2240) and IF-prescaler (PMB 2240) This solution provides a balance of cost and performance.

e) Power Down Modes
All IC's have complete and partial power down modes, allowing for optimal battery life and simplifying the software design of the control software.

6) Antenna
On the GOLDplus RF Board, a duplexer (passing 890-915 Mhz in transmit and 935-960 Mhz in receive direction) provides the interface to the antenna.

B. Software development tools

For the C166 controller software development proven standard development tools provide high density code (e.g. from BSO/Tasking). All tools offer C-compiler, assembler, linker and locator and are available for all powerful PC and workstation (SUN) platforms. For the development of additional DSP firmware efficient and reliable software development tools are offered based upon Microsoft Windows.

The C166 controller on GOLD-µC may be replaced by an emulator. The emulator adaptor is plugged onto headers located on the board thereby ensuring reliable operation.

C. Real-time debugging

Efficient real-time debugging is one of the key factors for time-to-market. Testing in real-time environments permits early recognition of potentially time-critical event-chains and avoids later software redesigns. It is equally required for fine-tuning of hardware and software to meet GSM Technical Specifications.

The most important debugging interfaces are shown in figure 4 along with the appropriate debugging tools. For watching program flow a logic analyzer may be used to trace the GOLD-µC bus, a debugger on a PC linked to a memory-resident monitor on the target system permits control of GOLD-µC activity by a simple

two-wire interface. The system simulator Digital Audio Interface (DAI) may be served by GOLD-SP for GSM type approval tests.

A highly-efficient software debugging tool optimized for GSM applications is provided along with the GOLDplusX board. This software-monitor running on a PC enables a tight coupling with a logic analyzer.

This combination allows near-emulator performance to be achieved without incurring typical drawbacks related to emulators such as contact reliability of the emulator adaptor and high cost. Qualified breakpoints can be defined at source level in the PC debug window for the logic analyzer permitting breaks at specific code lines depending on values on the data bus. Another outstanding feature is the possibility of tracing selected memory locations at predefined code lines (watchpoints) thereby greatly easing trapping of rarely occuring error conditions. Several debug features only require the 2-wire serial debug interface to GOLD-µC even when FLASH program memory is used. The latter enables debugging even in the initial production versions of the handset.

Further options for this debugging environment include tools for simultaneous debugging of SP firmware and µC controller software.

VI. GSM Software

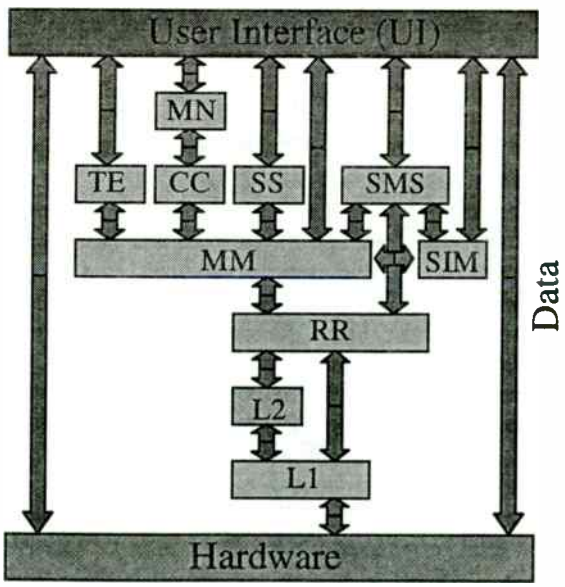

Fig. 5. GSM Software Protocol Stack

Siemens Semiconductors has cooperated closely with Optimay GmbH to develop software for the GOLD chip set. This software is available for purchase and is currently designed into many leading handsets. This long-standing relationship is continued in the case of GOLDplus, for which Optimay is transfering the Optimay Global™ GSM System Software on to the GOLD-µC.

The Optimay Global™ GSM System Software consists of a number of software modules, which together are sufficient for the development of a GSM handheld (Fig.5). The software modules are available as seperate products, so that the customer can choose only those modules which are relevant to the application area.

At the core of the Optimay Global™ GSM Protocol Stack (figure 5) is the software for Layers 1, 2 and 3 of the GSM software. As seperate but related products, Optimay provides GSM Data Services software, GSM Short Message Services software, a GSM mobile User-Interface Framework and a PC-based GSM User-Interface development environment. These products have been designed to function seamlessly with the GSM Protocol Stack. They are however available seperately from the Protocol Stack.

Product differentiation is achieved by customisation of the mobile telephone User-Interface. Standard Man-Machine Interaces (MMIs) have become very advanced in GSM, where full featured MMIs include several languages, Short Message and Supplementary Services. Typical sizes of MMIs are about 200-500K of code. The Optimay User-Interface Framework (UIF) is a library of routines, that allow a developer of an MMI to specify an MMI and code it in a matter of months. It provides a solid foundation for user-specific product differentiation and is implemented to meet the GSM 02.30 requirements. Such a User-Interface can be enhanced and extended in a PC development environment using the UI development tools supplied by Optimay - WinWise and M^{3}I.

Optimay is commited to supporting GSM by implementing additional features such as Phase 2 Supplementary Services, Phase 2 Short Message Services, Non-Transparent Data Services and Phase 2+ modifications to the protocol stack as the market requires them.

In addition to supplying software modules, Optimay may provide hardware integration services, support with interfaces and RF control issues, MMI integration and type-approval.

VI. PROJECT FLOW

Having focused on the GSM chip set, the development tools and the off-the-shelf hardware and software modules available, it is now possible to present these elements in the entire development process. A typical project flow for a GSM handheld based is shown in figure 6. This plan assumes the selection of the SIEMENS GOLDplus chip set, development tools and software from Optimay GmbH. Typical project flows vary from 12 to 15 months.

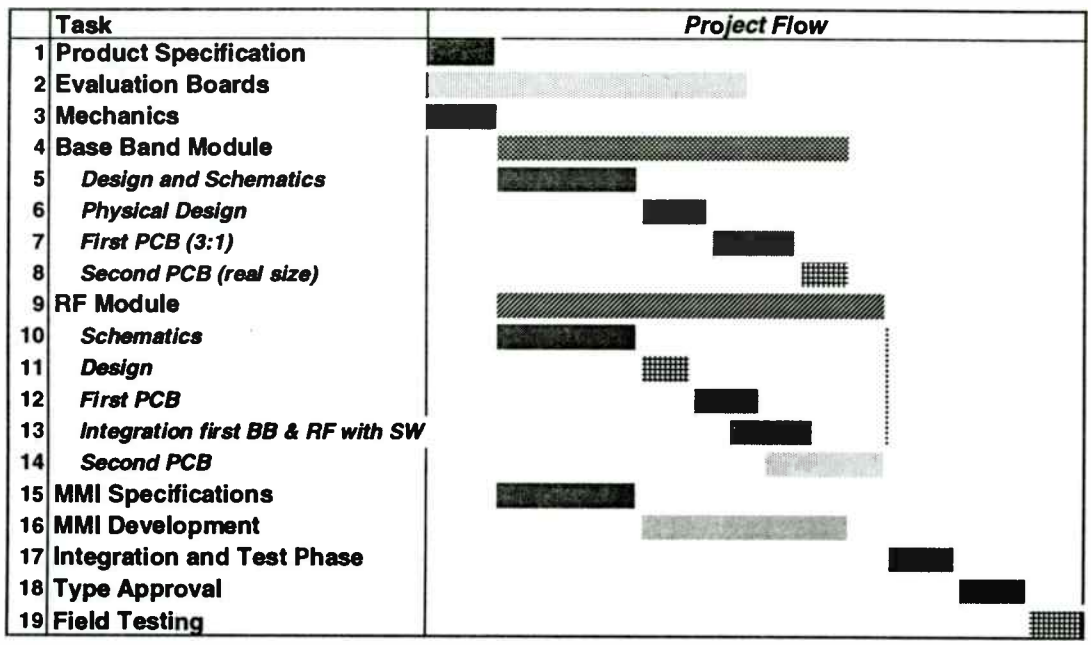

Fig. 6. Typical Design Flow for GSM Handheld

In order to start a handheld project following investment in hardware and software must be made:

- GOLDplusX Base Band Evaluation Board
- GOLDplus RF Evaluation Board
- GSM Protocol Stack (from Optimay GmbH)
- RF Test Program (from Optimay GmbH)
- Tools for User Interface (UI) development
- R&D tools such as:
  - GSM tester
  - Logic Analyser
  - complete set of RF singal generators and singal analyzers eg. spectrum analysers
  - EPROM simulator (optional)
  - Software tool chain

Beyond this initial material investment, development resources must also be planned.

At the outset of the project, in the *Product Specification* phase, decision are made on the features which the handheld is required to have. This includes the outward form and feel of the handheld, thereby setting goals for the entire development process. Mechanical features are also decided upon here, such as battery type, LCD, key pad, SIM card-type and connectors. It is at this stage that important decisions are made, based on marketing requirements, concerning the service features to implement, for example Short Message Service (SMS), Supplementary Services (SS), data services or fax. Indeed, more fundamental is the selection of the phase of GSM (I, II or II+) the handheld should support, once again determined by

marketing input. Finally, of importance for handheld design is the specification of power saving features, since these have a profound influence on the complexity and cost of design as well as the handheld's performance. Included in these considerations is the battery management specification.

Concurrent to the specification is an evaluation phase, where initial evaluation and development work is conducted on the GOLDplusX and GOLDplus RF evaluation boards. This stage enables experience to be gained with the chip sets and first integration of the software with hardware. Use of the evaluation boards considerably accelerates the design process and provides a reference for successive design cycles.

Once the specifications have been finalised the *Schematics and Design phase* begins, followed by the physical *Design* of the *First PCB*, which is in the case of the baseband board typically ratio 3:1 to the final product usually containing the core sections with near final dimensions and layout surrounded by debugging periphery. Here much can be taken from the evaluation board as a basis for design. The first RF board in contrast is already dimensioned as the final product, with additional debugging interfaces. Baseband and RF development flows can be treated as independent processes, punctuated by integration phases with software. Development of the two boards proceed at different paces and development milestones reached at varying times. It should be noted that the First PCB phase actually refers to number of development cycles, of design, test, debug and optimisation. Once a satisfactory stage has been attained, the baseband board is shrunk yielding *Second PCB* with the geometry of the final product.

Having finalised the overall specification, the *MMI Specification* phase is entered, followed by *MMI Development*, which runs parallel to hardware development. The minimum requirements of the user inferface is set down in the GSM specification. However a considerable freedom for customisation exists and decisions must be made which again influence the complexity of design and the resource allocation for the project. Such features as language choice, ringing tone selection and customised text. Supported by a User Interface development tool, such as the Optimay M^3I, a User Interface of moderate complexity can be designed by 2-3 software engineers in six months.

The prototype boards then pass through the phase of *Integration and Test*, where the final RF and baseband boards are integrated. In addition User Inteface is integrated into the final baseband board and the features such as data services included and tested. Finally customized hardware is integrated with the boards including memory devices, key pad and display.
Mid-way through integration, the handheld will already pass to some form of *Field Testing*, where the performance is tested under real conditions, where such issues User Interface as flexibility are addressed. A stage is reached in the development process, when the handheld is ready for Type Approval (TA), arguably the main milestone in the entire flow. The process of approval takes place in an accredited Type Approval test house, where the handheld is submitted to rigorous tests in a GSM simulator. Here the RF design comes under scrutiny, the software is tested according to ETSI 11.10 and finally the User Interface. It should be noted that Optimay GmbH provides a warranty that the software as delivered will fulfil the GSM specification.

Final Field Testing involves testing of the initial production of the handheld to verify behaviour in different situations and on different networks.

VII. CONCLUSION

The market for GSM handhelds is increasingly demonstrating the same features as other consumer markets, with associated shortening design cycles and increasing cost pressures. Time-to-market and design-to-cost are critical in such situations. Siemens Semiconductor's GOLDplus chip set, with its focus on systems solution, and the related development support tools enable the handheld designer to leap-frog the earlier stages of the development cycle. Off-the-shelf software from Optimay further accelerates the development flow.

Future generations of Siemens GSM solutions will ensure the competitiveness of handhelds based on the GOLD concept. As a next step, the High Integration GOLD (HiGOLD) will combine all logic baseband functionality on one device. In the coming years, developments in semiconductor and packaging technologies will bring ever higher levels of integration, enabling

handheld manufacturers to simplify designs, reducing component count and exploit increased processing capability, whilst reducing the cost, power consumption and weight of the final product. This in turn will drive the cellular market, ultimately making digital mobile telephones as ubiquitous an item as the digital watch is today.

RFID SYSTEMS AND STRATEGIES

RFID Systems and Strategies

Session Chairperson: James Eagleson,
RF Technologies, Inc. (Milwaukee, WI)

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RF/ID: Spectrum, Applications, & Techniques

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Abstract

Radio Frequency Identification (RF/ID) has matured considerably since its conceptual start as IFF transponders used in World War II to identify friendly aircraft. Systems have been developed for a wide variety of applications including animal tracking, asset tagging, security products, access control, assembly line management, and various transportation uses. Most systems, numerically, are in the VLF and HF frequency bands. Others have been implemented at VHF, UHF and Microwave frequencies. This paper attempts to give an overall view of applications, available spectrum and characteristics, plus techniques appropriate for RF/ID.

I. A BRIEF HISTORY: Cows to Cowcatchers

I've presented a similar paper in the past by introducing it as "From Cows to Cowcatchers". Two important characters in this scenario were Ms Blue and Ms Green, two dairy cows at a private high school sandwiched between the sand dunes along the coast near Watsonville, California.

RF/ID Pioneers Matt Lezin and Tom Wilson Installing a Cow Tag

An odd alliance was formed between Los Alamos Scientific Laboratories (LASL), the University of Chicago, and Saltz Tannery in Santa Cruz, California.

Transponders were placed beneath the skin of Blue and Green to provide both the identification and temperature of the animals. With this information it was felt that dairy farmers could tell whether an animal was sick or well, when it was ovulating, and so forth.

Later, the ID portion of the system was used to allow automatic feeding of the animals without risk of overfeeding them.

LASL, of course, was making an effort to transfer some its research technology into the private sector, as it had been instructed to do by the government.

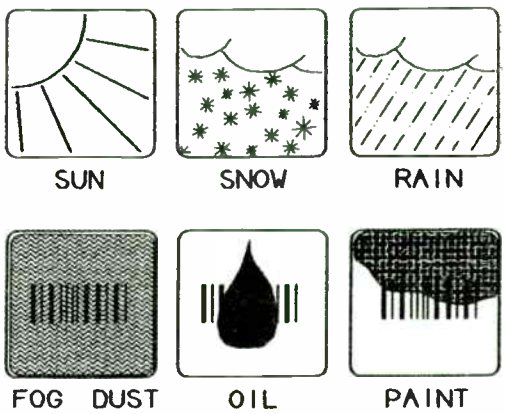
The University of Chicago had a long standing relationship with many New Mexico labs dating from nuclear research efforts during World War II. Additionally, they had a close alliance with midwestern farmers, many of whom are dairymen.

The Santa Cruz tanner, who would seem the oddest addition to this group, was interested in promoting a method of "branding" cows which would not destroy up to one quarter of the animal's hide in the process. For his purposes.. the traditional branding practice was a waste of valuable leather.

At this point a fourth party, General Railway and Signal (GRS) of Rochester, New York enters the picture.

Railroads had attempted to use a modified form of Bar Code technology to keep track of rolling stock during the late 1970's. Unfortunately, due to the harsh, often very dirty environment found along railroad lines, this technology did not prove to be very effective.

GRS saw that RF tagging techniques would be much more tolerant of rain, snow, ice, dirt, dust, fog and even such things as the rising or setting of the sun, all of which can negatively impact reliability of almost any visual or infrared technology.



GRS came to Identronix Research to find out if the "cow" tracking technology could be re-applied to "cowcatchers", that is, train cars and engines. This completed the otherwise obscure link between "cows and cowcatchers".

II. COMPETITIVE FIT: RF/ID vs Other Forms of Auto ID.

In our mass market world it is tempting to try to develop the "universal" RF/ID system in order to cash in on the economies of scale. There are certainly many applications where this can be done.

It is likely, however, that the cost of *any* electronic circuit will always exceed most forms of bar code labeling. RF/ID tag cost is more often measured in *dollars* rather than *cents*. More sophisticated units often cost tens of dollars. Some Read / Write tags, in fact, can cost upwards of $150.

This tends to restrict the use of RF/ID to that subset of all Automatic Identification opportunities we could call "items which cannot be identified with cheaper, more familiar Bar Code labels"(1).

It also reduces potential mass market numbers from tens or hundreds of millions to millions or hundreds of thousands of units.. placing RF/ID somewhere between a niche and a commodity market. It is a "chicken and egg" situation where costs can't come down without a huge market and the huge market can't develop because of higher costs.

One mass market now seeing some activity is the pet identification business. Here VLF based transponders are implanted subdermally in dogs or cats to allow veterinarians to identify them should they become lost or stolen. The tags can also be applied towards computerized call up of health records for individual animals.

Tagging of clothing and other retail items is sometimes referred to as RF/ID though these so called "single bit" systems are probably better described as "presence detectors" than a true RF/ID system. It is a very large market, however.

A few companies, like Texas Instruments with their TIRIS line, are targeting mass market applications. Most of these systems operate at VLF frequencies although some HF versions are also offered.

Other approaches, such as the so-called "Super Tag" (2) developed in South Africa, operate at low microwave frequencies.. in this case at 915 MHz. Micron Communications (Boise, ID) offers another RF/ID system designed for the mass market. It operates at 2400 MHz (3).

The "Super Tag" is supposed to compete with supermarket bar coding by providing automatic checkout of a cart full of groceries without removing anything from the cart. The developers think that ultimate cost per tag will be under a dollar given a sufficiently large market.

The Micron system uses an integrated MMIC / Lithium Battery combination and is small in size due to the 2400 MHz frequency. It is also supposed to be producible at relatively low cost.

Neither of these UHF / Microwave systems have seen widespread application as yet, but since UHF and Microwave systems generally provide longer range and higher data rates, the potential is certainly there. These systems are also useable in environments where VLF systems would be impossible to use due to electrical noise or other interference sources.

III. WHEN THE GOING GETS TOUGH, THE TOUGH GET RF/ID.

Just about any item which needs to be identified could be a candidate for RF/ID(1). Typically, however, the higher cost of RF/ID restricts its use to those applications where other, more familiar and less expensive approaches have already failed or been ruled out for one reason or another.

These include identifying items which are used in extreme environments such as auto assembly plants, paint ovens, chemical storage facilities, paper plants, railroads, tollways, and assembly plants where dust, dirt, oil, stray light, fog, rain, snow, chemical pollutants, or extreme temperatures often make Bar Codes or Infra Red systems unreliable.

RF/ID tends to be more flexible for many applications than Bar Code tagging, human readable labeling, or other competing forms of ID.

Most RF/ID techniques *do not need line-of-site* between the reader and tag, for example.

Tags are usually *reusable*. This often brings down the initial higher cost of RF/ID tags into a *per use* cost competitive with other technologies.

Many RF/ID tags *can be specifically programmed* with the number or description of the item being tagged. They can also be *re*-programmed for a different item or use later on.

RF/ID tags can be made *interactive*, that is, "Read / Write" providing two way communications for applications requiring constant updating of data or distribution of intelligence throughout a system.

High Frequency and Microwave RF/ID tags can operate at distances from *a few feet to several yards.* Some can operate from 30-300 feet (10-100 meters).

Some systems can even provide identification of *individual items in a group of mixed items* without moving either the reader or the items.

IV. GENERAL CLASSES OF RF/ID TAGS

Active Tag: Any tag which has its own internal power source, usually a battery, are referred to as "active". Active tags may be continuously transmitting at some preset interval or they may only power up when they receive a poll or interrogation from a reader.

Passive Tag: Tags not having internal power are considered passive. They may have a small battery to keep their memory active, but receive all (or most) of their operating power from the reader's interrogation signal.

Transponder: Tags which are passive are usually transponders, that is, they receive energy from the reader and use part of that energy both to power up their circuitry and return a signal to the reader. Some also shift their response to a different frequency than the one used by the reader to power up the tag.

The exact mix of active/passive, data length, tag size, working distance, and so forth for given applications depends on the nature of those uses.

V. APPLICATIONS VERSUS SYSTEM REQUIREMENTS

Some of the major RF/ID uses now in common use are:

1. **Animal ID**
2. **Personal ID**
3. **Inventory Control**
4. **Process Control**
5. **Access Control**
6. **Proximity Detection**
7. **Toll Collection**
8. **Vehicle ID**
9. **Automatic Guided Vehicle Control**
10. **Hazardous Material ID**
11. **Asset Tracking & Location**
12. **Patient ID & Security**

Just as there are limitations to the use of Bar Codes in certain environments and for certain applications, there are characteristics of RF based systems which must be taken into account when designing for RF/ID. Cows may require one technique while Cowcatchers may require a totally different approach.

Each application has a different set of constraints, goals, and environmental conditions. Among these are:

1. **Working Distance**
2. **Tag-to-Tag Spacing**
3. **Power Source**
4. **Data Length**
5. **Data Integrity**
6. **Tag Size**
7. **Tag Shape**
8. **Tag Cost**
9. **Ruggedness**
10. **Overall Reliability**

Often these factors are in direct conflict, particularly when it comes to size versus working distance or ruggedness and reliability versus cost.

This provides the design engineer with his most favorite and least favorite of all things: multiple challenges.

Anti-Theft

An anti-theft tag, for example, often uses a "one bit" system to identify the presence or absence of an object at a point of egress from the store. Some of these systems exhibit only 90 to 95% detection rates but are still widely used because they provide sufficient economic benefit to the end user.

Wanderer Monitoring

A wanderer monitoring device worn by an Alzheimer's patient, however, had better approach 100% detection rate due to serious impact this kind of application of RF/ID might have on the health and safety of the patient. Detection of presence is, again, the primary requirement though many systems also identify and display the number or name of the specific patient.

Animal ID

Animal ID can be broken down into three basic sub-categories:

1. Small Animals like cats and dogs
2. Farm Animals like cows, pigs, and sheep
3. Wild Animals such as bears, deer, whales, and trout

Pet Identification

The primary issue with smaller animals is to have a very small, implantable device which is inexpensive enough to penetrate a cost sensitive consumer market.

Generally there is no need to read the ID tag at a long or even moderate distance. Tag-to-tag spacing is not an issue since only one animal at a time needs to be identified.

ID tags used for this purpose are roughly the size of a large grain of rice or somewhat larger and are permanently implanted under the skin of the animal.

As with any transplantable tag, small animal tags must use a passive transponder so that no internal battery is required. Almost all batteries contain toxic substances so that implantation of battery operated tags is not acceptable.

Data length needs to be long enough to allow identification of several million individual animals out of a nationwide data base. Data length will also be impacted by the desire to include other information as well as by the need for data integrity bits for checksums or hamming codes.

Cost is an issue for pet identification products. The lower the price, including implantation by the vet, the more likely the product is to gain widespread acceptance. Price must be dollars, not tens of dollars if reasonable market penetration is to be expected.

While such tags do not need to meet a strict ruggedness requirement, biologically compatible, hermetically sealed, non-toxic materials must be used which are resistant to biological fluids.

Separating the Sheep from the Goats

For larger animals, both implantable and non-implantable tags are used, depending on the application. Generally the tag for domestic animals such as cows and sheep consists of an ID collar or an ear tag. Usually these are VHF or UHF tags to provide tracking the animals at a distance.

Some ranchers use VLF tags and even implantables to allow automatic feeding systems to dispense food to a particular animal while not allowing the same animal to obtain food again before a certain period of time has expired.

Tracking on the Wild Side

UHF is used whenever moderate to long distances are required. Examples of this would be tags used for tracking bears, elk, or other wild animals as well as tags used for domestic range animals such as cattle or sheep.

Close range UHF tracking is done using a handheld directional antenna, typically a three element yagi. Animals can be tracked out to several miles by using antennas mounted on low flying aircraft.

One system even uses a combination data recorder and data link transmitter which uplinks a record of sub-surface activities of a migratory whale during its surface activity periods.

Smaller fish, on the other hand, are usually tagged with VLF implantables since these can be made passive (no batteries) and very small in size.

When a fish so tagged returns to its "spawning grounds", in this case a commercial hatchery, it is made to swim single file through a pipe which is only 14 inches in diameter. The reader's antenna coil surrounds a non-metallic portion of the pipe so that the implanted ID tag is never more than seven inches from the antenna coil which allows it to both power up and read the tag as the fish passes by the site.

There is even one recorded case where a poacher was caught by using the implanted tag in a fish.

Some UHF tags provide long range communications through orbiting satellites by using very low speed data. This allows use of very narrow receive bandwidths so that the signal can be picked up from Low Earth Orbit (LEO) satellites passing a couple of hundred miles above the animal.

The system can provide both the animal's identification and calculate its precise location by using the Doppler Shift signature of the transmitter's carrier. This technique was first demonstrated using the OSCAR 6 Amateur Radio satellite and is also used to locate Emergency Locator Transmitters (ELTs) from downed aircraft or lost wilderness hikers.

VI. FREQUENCY SELECTION FOR RF/ID

RF/ID tags have been built at just about every frequency between **50 KHz** and **10 GHz**. The most common frequencies are 50-150KHz, 260-470 MHz, 902-928 MHz, and 2450 MHz.

Selection is based on several factors:

1. **Desired Pattern Control**
2. **Range Requirements**
3. **Required Data Rate**
4. **FCC/DOT/International Regulations**
5. **Size Requirements**
6. **Power Requirements**
7. **Interference Environment**
8. **Noise Environment**
9. **Cost / Performance Tradeoffs**

SPECTRUM CHARACTERISTICS

Band:	VLF	HF	VHF	UHF	uWave
Data Rate:	Low	Med	Med	High	Very High
Noise:	High	Med	Low	Lower	Negligible
"Skip" Interference*	None	High	Tropo	Tropo	None
Absorption	Low	Low	Med	Med	High
Reflection	None	Low	Med	Higher	High
License Required	No**	Y/N**	Y/N**	Y/N**	No**

* "Skip" is external interference from distant sources either by atmospheric propagation below 100 MHz or tropospheric propagation in roughly the 100 - 500 MHz region.

** "No" means Part 15 or other license free operation options are available. "Y/N" means that Part 15 operation options are available in some portions of these bands but licensing is required for other frequencies and kinds of operation.

It is best to consult the FCC Regulations *before* spending much time developing an application at any

given frequency. There are certain restrictions in place with regard to allowed functions and modulation types in addition to the regulations concerning power, bandwidth, and field intensity levels allowed.

VII. VLF SPECTRUM CHARACTERISTICS

VLF is the spectrum between 30 - 300 Khz. Most commonly, VLF systems operate on subharmonics of typical microprocessor crystals, such as:

4.194 KHz / 64 = 65.531 KHz
4.194 KHz / 32 = 131.063 KHz
4.194 KHz / 16 = 262.125 KHz
4.194 KHz / 8 = 524.250 KHz

4.000 KHz / 64 = 62.500 KHz
4.000 KHz / 32 = 125.000 KHz
etc.

Many RF/ID systems, therefore, operate on or near these frequencies depending on the crystal frequency used for their microprocessor.

Some typical frequencies are:

TI TIRIS	**134.2 KHz**
Omron V660-Hxx	**530.0 KHz**
IDTAG	**125.0 KHz**
Deister Electronic	**125.0 KHz**
Cotag (Amtech)	**R66.1 / T132.2 KHz**
Indala (Motorola)	**T125.0 / R62.5 KHz**

First, the Bad News

Frequency selection for VLF can be critical in certain environments. Locations having Televisions or Computer Monitors, for example, will have significant levels of energy at the fundamental and harmonics of the Horizontal Scan frequency. This is a common problem in Nursing Homes, Hospitals, and other environments having significant TV or Computer usage.

This common interference source can obviously impact both frequency selection and bandwidth availability. For example, operation at 65.535 KHz is less than 2.5 KHz above the second harmonic of a VGA Monitor or a Standard TV Screen. Attempting to use this frequency for data rates much above 1,200 baud (1 Kb/s) would require a receiver bandwidth which would be wide open to interference from these sources.

Video Monitor Radiations:

Mode	Fund	2nd	3rd	4th	5th	6th	7th
VGA	31.5	62.9	94.4	125.9	157.3	188.8	220.3
XGA	35.5	71.0	106.6	142.1	177.6	213.1	248.6
VGA VESA	37.9	75.7	113.6	151.4	189.3	227.2	265.0
SVGA VESA	37.9	75.8	113.6	151.5	189.4	227.3	265.2
SVGA	35.2	70.3	105.5	140.6	175.8	210.9	246.1
TV	31.5	63.0	94.5	126.0	157.5	189.0	220.5
	KHz	KHz	KHz	KHz	KHz	KHz	KHz

Systems operating on 125 KHz, another common frequency choice, must contend with the 4th harmonic of both VGA Monitors and Standard TV Screens. In this case the interference is centered only 0.9 to 1.0 KHz from the carrier. This would suggest a data rate of under 600 baud (0.6 Kb/s) to allow for appropriate selectivity.

At 131 or 132 KHz, on the other hand, the closest interference is more than 4 KHz away which would allow a data rate of about 2400 baud (2-3 Kb/s) with adequate selectivity to reduce the adjacent interference source.

(Tip of the day: Digital oscilloscopes having VGA screen displays can be a source of frustration for the developer of VLF RF/ID systems. DVMs and oscilloscopes have sometime proven to be the *real* source of inexplicable "instability", "noise", or "oscillations" !)

VLF Impulse Noise versus Data Integrity

Just about everything which generates a spark, whether vacuum cleaners, hair dryers, or large industrial welding equipment, radiates significant energy in the VLF, HF, and even lower VHF regions.

Motor noise is particularly problematical for many VLF systems because brush noise often occurs at a repetition rate similar to the data rates of many Pulse Position Modulated (PPM), On/Off Keyed (OOK), and Amplitude Shift Keyed (ASK) systems.

Unless care is taken to optimize receiver sensitivity and/or gain to just the level required for a given application, bogus identification based on ambient noise sources may occur. Judicious use of data checksums, CRC, or hamming code structures will

also help prevent false decoding of "data" out of noise or interference.

Some have gone to FSK or QPSK to work around the noise problem, but these techniques increase power drain and occupied bandwidth which can impact battery life (active tags) and maximum useable data rate.

This problem is not as critical in industrial applications where a "no read" is better than a "bad read". We merely make the data so secure that an incorrect identification is highly unlikely. The added overhead of CRC or hamming code bits is warranted by the need for precision.

Even here, though, there is a trade off between required data length and such variables as transaction time, available memory, and battery life. Thus use of higher bit overhead for data integrity is not always an acceptable solution.

The noise handling issue becomes a major design problem in longer range systems like wanderer monitoring where an alarm needs to sound whether or not the system was able to achieve perfect identification of the specific wanderer. We certainly would like to know *who* is trying to leave the facility, but even if we can't correctly identify the individual, we still want to know that *someone* being monitored has left or is attempting to leave the building.

For this application we want to set up a minimal, but adequate data integrity check. We want any error to be on the side of safety, not accuracy.

On the other hand, we don't want to create a "boy who called wolf" situation by having too many nuisance alarms whenever the maintenance person vacuums or some other noise source creates semi-organized noise in the receiver.

Welder noise in the industrial setting can be an overwhelming problem at VLF. Often a few milliwatts from an ID tag must compete with several hundred watts of broadband arc noise.

Fortunately this noise source is not generally continuous so that readings can be made during "quiet" periods between welds. System planning becomes as important as system capability, in this case. The system should avoid making a read attempt during the middle of a weld operation.

Similar, but generally less severe problems can occur with elevators in hospitals or assisted living facilities. Often we have a high current motor attached to a long, trailing wire "antenna" (i.e., the power cable). Care must be taken to minimize noise pickup from this kind of "unintentional radiator" to prevent nuisance alarms and avoid masking of desired signals when the elevator is in use.

Interference between co-located RF/ID or Data Communication Systems

Occasionally a VLF RF/ID system must contend with interference from a competing VLF system. A number of RF/ID and access control systems radiate significant energy in order to power up their passive tags.

As an example, COTAG (Amtech) energizes their tags at 132 KHz while receiving the response at 66 KHz. RF Technologies 'Smart Guard' system, on the other hand, uses an active tag which transmits at 132 KHz.

If a facility has both a COTAG system and a Smart Guard system, the COTAG energizing signal, which is several *Watts*, may interfere with reception of the Smart Guard tag, depending on system separation and other installation parameters.

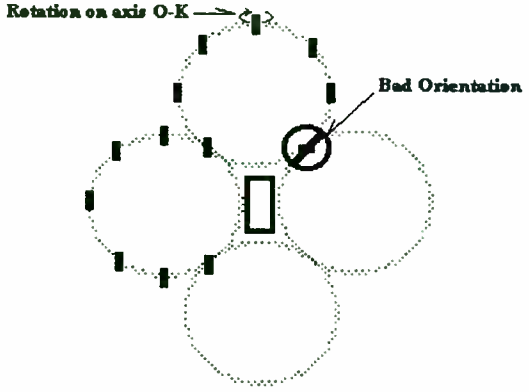
This is not really a problem for RF Technologies since the "Smart Guard" is only one of several systems offered. When it is known that potential interference exists, other options including a unit identical to the COTAG system can be offered.

What this points out, however, is the need in RF/ID (or *any* RF based system) to have more than one option. Just as the users of wireless LAN equipment are finding out, *no one RF/ID system will cover all possible applications, conditions, or environments!* This is a case where 'diversity' is not only 'politically correct', it is also smart business.

Orientation Sensitivity

A lot of hype was made in the early days of RF/ID about the orientation insensitivity of VLF tags when compared to UHF tags. Certainly the typical VLF tag can rotate 360 degrees on its axis without much impact on coupling between it and the tag reader, but

this rotation still can only be around one, coplanar axis.



VLF Tag Orientation Problems

If a VLF tag is rotated around the other axis, it will show a null just as deep (probably deeper) than a UHF tag.

Some VLF companies, RF Technologies being one of them, have gotten around this by using two, orthogonal antenna coils in their tags.

A more recent effort at controlling this problem was described in an article in Wireless Systems Design (4) and uses *three* orthogonal coils to create a truly omni-directional, omni-polarized tag. This is probably overkill but is practical when tag size is not a critical issue.

Multiple coil tags generally switch between coils rather than having them all active at once. This reduces mutual coupling and provides a diversity effect.

An alternative to the multiple coil approach in the tag is to use two or three orientations for the RF/ID reader's antennas. This allows use of a single coil in the tag which is important where minimal tag size is required.

Use of multiple coils may not be very practical for passive tag systems, however, due to the larger coils often needed to transfer energy to these tags. The use of three large coils is not likely to have wide acceptance with customers already desiring very small RF/ID tags for their application.

The use of multiple reader antennas has one other potential drawback. Omni-polarized antennas may be more likely to receive noise and interference. It is quite common to use antenna orientation in a VLF system to null out or reduce interference and noise sources.

The Good News

Even gravity doesn't make it impossible to go to the moon.

In spite of the noise, interference, and bandwidth limitations associated with VLF frequencies, hundreds of thousands of VLF tags are in use throughout the world and are providing excellent service.

While VLF RF/ID may not be appropriate for some applications, many others could not be met using any other technique.

In almost all cases, VLF tags can be made smaller than UHF alternatives. VLF tags have been made which are roughly the size of a large grain of rice and most are only an inch or two across.

In some regulatory environments, UHF and Microwave alternatives are not readily available for RF/ID use... especially at the power levels required for *passive* UHF or Microwave tags.

For imbedded applications, such as placing a tag in a machine tool, under a floor, or implanting a tag in an animal, VLF generally works best and UHF or Microwave may not be practical due to size and signal constraints.

VLF, within its distance limitations, has the best 'penetration' of all RF/ID tags.

"Path Loss"

One characteristic of VLF which provides some relief from the noise and interference problem is its very long wavelength. At 100 KHz, a wavelength is 3000 meters long (300,000 meters per second / 100 KHz). Since near field boundary is defined as $\lambda / 2\pi$, *all* VLF systems operate well within the *near field* region.

This means that the signal strength of a VLF tag falls off very rapidly with distance. Magnetically coupled tag signals drop about 12 dB every time the distance between the tag and the antenna coil doubles.

This also means that noise and interference influence falls off 12 dB for every doubling of distance between the source and the RF/ID receiver.

VLF "Path Loss"
40 LOG (D1 / D2)

Distance	Reference Level
2"	0 dB
4"	-12 dB
8"	-24 dB
16"	-36 dB
32"	-48 dB
64"	-60 dB
128"	-72 dB
256"	-84 dB

Transponder signals (ie, from passive tags) will fall off even more rapidly than active tags. Signal strength in the case of a transponder is lost both *going to* the tag (i.e., the energizing signal) and *returning from* the tag. A figure of 60 LOG (D1 / D2) has been used for the transponder situation but I have not, personally, confirmed this.

The Bottom Line: VLF Effective Range

I have seen articles suggesting VLF tag ranges up to 10 feet (3m) but my experience suggests that the range which can be relied upon is really only about five to seven feet. Totally passive transponders, those having no battery at all, generally have less range than active tags.

For their TIRIS system, for example, TI gives the following specs for expected range:

23mm Transponders	**60cm (23.5")**
32mm Transponders	**100cm (39.4")**
Disk Transponders	**60cm (23.5")**
Card Transponders	**100cm (39.4")**
Vehicle Transponders	**200cm (78.7")**

As a rule, I would use these specs as a guide to what can be expected at VLF frequencies.

Fabrication Advantages of VLF

VLF is well within the frequency range of all common integrated circuit technologies. Producing mixed mode RF/ID chips, even some with complex modulator/demodulator schemes, is easily achievable.

VLF is quite easy to hermetically seal. With the deep penetration characteristic to VLF frequencies, normal potting or sealing techniques can be used. Dielectric variation and absorption factors are not usually critical.

VLF is not layout critical. Where at UHF or Microwaves the printed circuit board is actually *part of the circuit*, at VLF the circuit board layout is not significant in most cases. Some, in fact, use no circuit board at all.

A VLF tag using an integrated mixed mode chip might be configured with a very small solenoid coil, a flat, credit card sized, printed circuit coil, or a large, ferrite core coil, depending on the desired application. None of these variations will make much difference to the operation of the ID tag except for the range variation caused by the coupling efficiencies of the coils being used.

VLF System Development Cost

Another advantage of VLF is that simple test equipment can be used both for development and servicing of these systems. A good Digital Volt Meter (DVM), a reasonably good Oscilloscope and a handful of test jigs are sufficient for most development and service. "The rest is just software".

Many VLF RF/ID companies got their start as "garage" operations because of this.

Of course, this assumes that the developer is using off-the-shelf chips, ASICs, or one of the specialized RF/ID chips from the several vendors which offer them, rather than trying to develop his own, proprietary integrated circuits.

VIII. UHF/MICROWAVE CHARACTERISTICS

When very high data rates or longer working distances are required for an RF/ID system, UHF or Microwave tags are the best candidate.

At VHF and higher frequencies we can rely on the much more gradual path loss found in the Far Field. This is the familiar 20LOG(D1/D2) path loss compared to the 40LOG(D1/ D2) or higher loss experienced with VLF tags. It is not uncommon for

UHF tags to achieve distances up to 300 feet in applications where size is not limited, and almost all such tags are able to deliver 5 to 10 feet with no problem.

At UHF we can use data rates of hundreds of Kilobits per Second. For short range applications, even higher data rates can be achieved. For longer range requirements, data rate can be reduced to extend receiver sensitivity through reduced noise bandwidth.

U.S. Low Power Device Bands

The primary frequencies for UHF tags are between 260-470 MHz and in the 902-928 MHz "ISM" band.

Allowable uses of these bands are defined in FCC Part 15.xxx, 15.yyy, and 15.zzz.

Commonly used frequencies in the 260-470 MHz band are 303.825, 315.000, 318.000, 418.000, and in Europe 433.920 MHz. This is because of widespread availability of SAW resonators for these frequencies.

In this band, however, there is a caution. The FCC has restricted frequency bands at:

Part 15.205a
Protected Bands

240.000 - 285.000 MHz
322.000 - 335.400 MHz
399.900 - 410.000 MHz
960.000-1240.000 MHz

"..only spurious emissions are permitted in any of the frequency bands listed.. "

260-470 MHz Interference Sources

The major problem with the 260-470 MHz band is interference. This can be from high powered FM broadcast transmitters (88-108 MHz x 3 = 264 - 324 MHz), garage door openers (303 & 315 MHz are both common), and fire and security devices (315 and 318 MHz are common).

For short range applications, under 10 feet or so, interference from other Part 15 devices is not too likely unless located in the immediate vicinity of the RF/ID equipment.

Generally, for example, a home garage door opener will not be in the same area as an industrial RF/ID system.. at least not within hundreds of feet of it. The reverse is also true.

On the other hand, security and fire alarm devices may very well be in use within the same facility as an RF/ID system. Furthermore, keyless entry systems for cars and vans, are also on these frequencies and could see regular use in industrial plant parking lots.

Another problem which can exist is interference from the superregenerative receivers often used for many of the UHF based systems. Receivers should not have much influence beyond 5 or 10 feet, but their relatively broadband noise may cause problems when co-located with the RF/ID equipment. This would have the most effect on longer range, higher sensitivity systems.

260-470 MHz Noise

Man made noise, particularly ignition noise from cars, is one limiting factor in this band.

The level of such noise is inversely proportional to the frequency so that its effect is 6 dB higher at 260 MHz than at 470 MHz. This means that all else being equal (and in RF we all know that isn't usually the case), one should achieve *twice* the distance in a given noise environment at 470 MHz than we can at 260 MHz.

This kind of interference will be strongest in urban environments or near highways and busy streets.

SAW Devices

The least expensive transmitter for UHF use is one using a SAW resonator, two capacitors, an inductor, and a transistor. Total cost: about $3. For about $5 at least one manufacturer offers a complete surface mount transmitter module which is about the size of an eight pin integrated circuit.

The advantage of SAW resonators is low cost and on-channel operation. Since there is no need for multiplier stages, this leaves suppressing harmonics as the only concern of the designer. There are no power hungry multipliers with their potential for spurious radiations, filtering requirements, and extra "real estate".

The problem with SAWs is their frequency stability. Typically calibration tolerance for these devices is

only about +/-100 KHz. Furthermore, they are available only on a limited number of frequencies unless usage is high enough to amortize the required NRE to develop a custom frequency.

Obviously a system using a SAW oscillator will require a receiver with a bandwidth of at least 200 KHz to allow for resonator calibration and temperature tolerances. Higher data rates would probably raise this to 300 or 500 KHz if sideband clipping of the incoming signal is to be avoided.

Given a Noise Figure of 6dB for a typical low cost receiver, 270 KHz Noise Bandwidth for the usual 10.7 MHz ceramic IF filter, and a 12 dB Carrier to Noise Ratio (CNR) requirement, we can calculate the following receiver sensitivity:

RX Sens = -174dBm+10LOG(BW)+NF+CNR
= -174+10LOG(270000)+6+12
= -174+54+6+16 =-174+72
= **-102 dBm**

Of course we can improve on this a bit more by use of a Gaussian Low Pass Filter after the detector. For lower data rates like 4800 Baud our noise bandwidth might be reduced to 15 or 20 KHz rather than 270 KHz. Thus we might achieve a sensitivity of -114 dBm or so.

RF Monolithics, a long time supplier of SAW devices for various wireless applications, also produces a very small, surface mount integrated circuit receiver based on SAW technology (5). This unit has sensitivity in the -90 to -100 dBm region depending on data rate and frequency band. Data rates are available from 1 to 20 Kb/s.

RFM calls their unit the ASH receiver and sell it for about $17 in moderate production quantities. ASH, by the way, is an abbreviation for Amplifier Sequenced Hybrid. It is probably is not completely coincidental, however, that Darrell Ash, RFM's VP of Engineering, designed the ASH receiver.

By using the inherent delay through SAW filters to allow sequencing two low noise RF amplifier stages, gain is never turned on for both at the same time. This sequenced amplification provides very high, single frequency gain without the instability one would expect from a Tuned Radio Frequency (TRF) receiver.

An intentional by product of switching on only one amplifier at a time is an average drain of only 1.4 mA at 3.3 VDC which includes the output driver current.

Since selectivity is also provided by two SAW filters, bandwidth is quite reasonable and no tuning of the circuit is required. Receiver bandwidth is +/-200 KHz centered on the desired channel and better than 20 dB down at +/-1 MHz. This is far better than the 1-3 MHz achieved by the super-regenerative receivers often used for RF/ID and Keyless Entry applications.

Spurious responses of the ASH receiver are better than -85 dB outside of +/-7.5 MHz or so. Since there are no oscillators in the receiver, there is no requirement to certify the receiver for incidental radiation.

Unfortunately, the ASH receiver is presently only available for the really highly used frequencies of 303.825, 418.000, 433.920 MHz, and 916.5 MHz. There has been some discussion of making 315 MHz available, but the critical usage numbers have not quite coaxed RFM into providing this frequency.

A drawback to the ASH receiver is that it is *not* very tolerant of *on channel* carrier interference. It will go into hard limiting with a very low cw input level.

This is not a problem when using the On Off Keying (OOK) modulation around which the ASH was designed, but it makes the unit less useful for other possible amplitude modulation schemes where the "off" condition may only be suppressed 20 or 30 dB, or for those situations where other carrier signals might be present within the passband of the receiver.

A second drawback, of course, is that this receiver does not receive FM, FSK, PSK, or QPSK.

Other Candidate Receivers

There are, of course, other candidate receivers for the 260-470 MHz band.

One, already mentioned, is the superregenerative (SRG) receiver. In spite of its *many* drawbacks, the SRG still is used in all kinds of remote control, RF/ID, keyless entry, and alarm systems. Whether it is used in the $9.95 "wireless" door chime or an industrial fire alarm system, the SRG provides:

1. **Low Cost: Usually less than $3**
2. **Fair Sensitivity: -90 to -100 dBm**
3. **Low Current: 0.5 - 2.0mA common**

A variety of special integrated circuits have been developed for Two-Way Radio applications (though now cited for "wireless" or "cellular" use) which provide a mixer, an oscillator, an IF Amplifier, a signal strength output, and an FM detector.

Typical of these is the Phillips NE615 which provides operation up to about 500 MHz, RSSI (Received Signal Strength Indicator) output, and oscillator good to 100 MHz with a crystal and higher using LC oscillators, and will detect Pulse modulation (using the RSSI output) or FSK and FM.

Operating voltage for this class of parts is now from about 3 Volts to 12 Volts. Current draw is rarely below 6-8 mA, however, making them less competitive than SRG or ASH receivers in some long life battery applications.

More recently, driven by the PCS and Digital Cellular markets, several IC's for QPSK, and other digital modes have also become available. While these tend to be more expensive than the NE615 kind of parts, they are certainly much less expensive than they were a few years ago.

There are even chip sets aimed at the "wireless" handheld market which provide digital, spread spectrum operation. These are not really applicable for most RF/ID operations, however, because they are relatively expensive and draw tens of milliamps, not microamps. I would imagine that they will see service in those RF/ID applications which can operate from AC power or which can "freeload' power from the equipment to which they are attached, however.

FCC Allowed Levels vs Distance

If we have a sensitivity of -110 dBm to work with, just how far can we expect to receive useful signals from an ID tag?

If the device falls under the broadest FCC category as defined by Part 15.209 of the rules, between 216 and 960 MHz we are allowed a maximum field strength of 200 uV per meter. For *intentional* radiators, however, we cannot place our *fundamental* frequency between 470 and 806 MHz.

A level of 200 uV/m calculates to:

dBuV/m = 20*LOG(uV/m)
= 20*LOG(200)
= 46 dBuV/m

To calculate the power received by a receiver in a field of a given field strength:

dBuV/m = 107 + LC + AF + PR

where LC = Loss of Cable
AF = Antenna Factor
PR = Power Received (dBm)

We will assume zero cable loss for the typical RF/ID tag reader since the antenna is generally integrated into the unit. We will also assume dipole gain for the antenna though this could be more or less depending on the type of antenna used.

thus,

PR = dBuV/m - (107 + AF + LC)

and,

AF = 20*LOG(FR) - GA - 30

where FR = Frequency
GA = Gain of Antenna (dBi)

AF = 20*LOG(303.825) - 2.15 - 30
= 17.5 dB

so,

PR = 46 - (107 + 17.5 + 0) = -78.5 dBm

Given the minimum FCC limit, then, we can easily receive a return signal from at tag at three meters. In fact, we have more than 20 dB to go before we will drop in level to the previously calculated -114 dBm sensitivity we can achieve when using SAW stabilized transmitters.

If the application is in free space, we can apply the general formula:

Distance Multiplier = 10^(dB/20)
= 10^(20dB/20)
= 10^(1)
= 10 times

This means that given a receiver sensitivity of -114 dBm, we should be able to receive an FCC legal transmitter at a free space distance of about 30 meters, or 100 feet.

But...

There always seems to be a "but..." when it comes to RF.

UHF and Microwave Nulling

One of the reasons we use RF instead of just wiring things together is that RF gets to everywhere in general whereas wires only connect from Point A to Point B. This means that RF both affects all of its environment and *is affected by* all of its environment.

RF tags are not generally located in "free space". In fact, they are frequently located in terrible locations.. under something, behind something, next to something, between 'somethings'. "Free space" hardly ever applies.

At the very least, one should plan for 10 dB of path variations due to nulling, blockage, and noise. When using SAW transmitters and 300 KHz receiver bandwidths, ignition and other electrical noise will certainly impact range at the lower UHF frequencies. Reflections will create nulls, some approaching 20 or 30 dB. Blockage due to obstructions will also reduce signal levels.

The 100 foot (30 meter) range we calculated before now drops back to 1/3rd of 100 feet to about 30 feet (10^(10/20) = 0.316) if we are to maintain reliable coverage.

In the case of keyless entry to a car or garage door, the user just presses the button again until he or she leaves a null (or finds a peak). This is similar to the Bar Code Scanner in your supermarket where the label is often passed over the unit several times before it reads correctly.

For RF/ID, however, we are more closely related to the wireless microphone situation where we dare not lose the signal. We might only get one chance at receiving the signal or the tagged object might stop in a poor location.

This is one of the most serious problems for UHF and Microwave RF/ID systems.. handling signal nulls.

It is one reason so many VLF systems are used in spite of their inherent limitations of lower data rate, range, and noise immunity.

Spread spectrum reduces nulling effects but is generally too expensive and power hungry for RF/ID use.

Diversity reception can help (and is used in the wireless microphone case), but superregenerative receivers do not lend themselves to this technique due to their receiver radiation problems. Mutual interference will occur.

Diversity using an ASH receiver would work well, but at $17 per unit the ASH might be too costly for some applications.

Receivers based on one of the mixer, oscillator, IF, detector integrated circuits will still run $7 to $10 once all support components are in place. This is in a more acceptable region, but still expensive for some of the more cost sensitive applications.

Multiple antennas have one other drawback: size. At 303 MHz, and even at 915 MHz, antennas are 3 to 20 inches long, depending on frequency and type. This may take up too much space for many applications when two (or more) such antennas are mounted orthogonally to each other or physically spaced apart sufficiently to provide true diversity.

Pattern Control

Another problem at VHF, UHF, and Microwaves is that of pattern control. At VLF we basically have only one pattern: omnidirectional. At higher frequencies we can use multiple element arrays to achieve unidirectional patterns, but (there's that word again) there also are reflections and nulls to contend with.

As we suggested earlier, due to nulls and peaks in the field intensity from or to an RF/ID tag at higher frequencies, we experience at least +6 dB and -10 dB even with diversity techniques.

This means that while we may have set up a range limit of 10 feet for our system, the enhanced range for the +6 dB case could increase this by two times (10^(6/20) = 2) or it might drop it down as low as 1/3rd of the desired range (10^(-10/20) = 0.32). Thus our desired 10 foot coverage zone might be as high as 20 feet in certain locations where the signal is

enhanced by reflections, and it might be reduced to only about 3 feet in areas experiencing nulling.

Clearly, then, use of UHF for door monitoring in nursing homes or similar five to eight foot proximity applications becomes problematical. VLF provides a much more reliable, controllable coverage zone whenever VLF range restrictions are acceptable.

One technique which has been used to get around this problem is to use a VLF signal to trigger the UHF tag signal only when it is in a tightly controlled VLF field. This localizes the signal sufficiently, but still may cause an adjacent reader to report the same tag number where multiple readers are in close proximity.

Blockage, Absorption, and Penetration

Higher frequencies are more easily blocked or absorbed than VLF signals. While wrapping a VLF tag in tin foil or submerging it in water will not greatly attenuate its signal, UHF and Microwave tags can show great attenuation under similar circumstances and may not work at all.

It was for this reason along with the pattern control issue just discussed which caused RF Technologies to produce a dual frequency, VLF/UHF identification bracelet for infant/child security applications.

While we needed wide area coverage should someone attempt to remove or cut the bracelet from the child, we also didn't want the signal to set off an alarm every time someone carried a baby past an alarmed exit door or elevator.

The "tin foil" attenuation problem was addressed by using a multitude of close spaced receivers with overlapping coverage to assure reception of even very weak signals. It is nearly impossible to both remove a band and keep a tight enough shield around the bracelet given the receiver "overkill".

The exit door problem was addressed by using VLF for the exit alarm signal since this allows tight control of pickup coverage yet prevents shielding of the VLF signal without a great deal of effort.

Other schemes such as trying to keep in continuous contact with up to 250 bracelets were considered, but given the interference, blocking, and nulling environment of the average hospital, these approaches were considered to cause as many problems as they solved. We feel that the method selected serves the application better.

Additionally, most hospitals desire to *reduce* the number of active VHF and UHF signals present in their facilities since they already contain broadband, interactive cable TV systems, a variety of VHF and UHF telemetry and patient monitoring systems, and wireless data, personnel monitoring and paging systems.

VHF, UHF, and Microwave systems have varying penetration capability. Of the three, VHF (30 - 300 MHz) penetrates walls and ceiling best, UHF penetrates adequately, and Microwaves penetrate less adequately.

Compared to competitive technologies such as infrared, which has *no* penetration through walls and ceilings, even Microwave RF has "good" penetration.

Penetration ability is either a strength or a weakness depending on whether you are trying to cover only a single room or if you are trying to cover a larger, multiple room area.

Defining Coverage Area

One common problem with RF based systems is the inability to define coverage area succinctly. An example is trying to receive an RF/ID signal up to the edge of a piece of property *but no further*. This is similar in nature to the exit door monitoring where we want to cover all of a doorway but not have coverage into hallways or rooms on either side of the door.

At VLF, with its ominidirectional coverage, this is difficult enough since the reader will pick up signals 5-6 feet in *all* directions. With VHF, UHF, or Microwave systems, clearly defined coverage is even more difficult because of reflections and nulling. There is no "brick wall"surrounding a coverage zone when using the higher frequencies for RF/ID.

Perimeter alarms using microwave beams at 10 GHz have seen military and industrial use since the 1960's. Buried VLF wire loops have seen use in pet control. (Cross this wire, pet, and you'll get the shock of your life!) Monitoring of the FM Broadcast spectrum as received by a buried wire has been used to detect crossing of that wire by larger mammals (ie, human beings). It appears that the spectral balance between

stations is sufficiently disturbed by such a crossing to allow determination of an alarm condition.

In all of these cases, however, we are really looking at field disturbance sensing, not specific identification of a given individual who is leaving or attempting to leave a monitored zone or area. The system which is able to monitor everything inside a zone yet alarm at a well defined perimeter remains elusive.

Totally Passive Transponders

Most UHF and Microwave tags are active. A few, for various reasons, are passive and contain *no* battery. These are generally tags used on objects which cannot use batteries due to safety concerns such as using such tags in high temperature environments where batteries might explode or cease to work.

These transponders must receive all of their energy from the tag reader.

What range can we achieve with such a transponder?

At 300 MHz we are allowed 67 dBuV/m for an automatically keyed RF/ID systems. Depending on the duty factor of the transmission averaged over a 100 millisecond period, we may be able to increase this to a maximum FCC *peak* field strength limit 20 dB higher at 87 dBuV/m.

The formula for calculating FCC duty factor allowance is:

FCC Allowance = 20 Log (Time On / 100)

where Time On is in mS

thus, for a 10mS out of 100 mS transmission,

Allowance = 20 * LOG (10/100)
= -20 dB

In other words, if we have a 10% duty factor, we can take our measured Field Strength in dBuV/m and subtract 20 dB from it. This is then considered the average field strength so that 87 dBuV/m *peak* would be allowable under the 67 dBuV/m FCC *average* limit.

To put this into perspective, if we were to use a 200Kb/s data rate, we can transmit up to 2000 bits of raw data (ie, ID code) in 10 milliseconds.

So how much power can we achieve if our tag receives this field strength?

PR = dBuV/m - (-107 + AF + LC)
= 87 - (107 + 17.5 + 0)
= 87 - 117.5 = -30.5 dBm

Well, this isn't too much to work with.

Even if we boost the voltage by transforming the impedance to 500 Ohms instead of 50 Ohms, we still only get a terminal voltage of 0.06 Volts. This is hardly enough to detect in a diode let alone fully rectify and run both the digital encoder and modulator circuits.

The received power level comes up a bit shy, too. A level of -30.5 dBm is only about 1 *micro*watt. Even if we had enough voltage, we'd still be looking for more power.

If we came 20 dB closer, which is 1/10th the distance, we still only have -10.5 dBm yielding a voltage of about 0.67 Volt and power of about 90 *micro*watts. We still fall far short of useful energy transfer even at a distance of only 0.3 meters (about 12 inches).

Fortunately the FCC provided one band with a specified field strength sufficient to provide us with a workable solution. At 915 MHz we are allowed a 3 meter field strength of 94 dBuV/m average for a peak allowance of 124 dBuV/m. This falls under Part 15.249 of the FCC regulations.

Substituting this into our earlier formula provides:

for a dipole antenna...

AF = 20*LOG(915)-2.15-30 = 27.1

PR = 124 - (107 + 27.1 + 0)
= 124 - 134.1 = -10.1 dBm

Cutting our distance in half to about 1.5 meters (about 5 feet) doubles the voltage produced by increasing field strength 6 dB. Thus we obtain -4.1 dBm which translates to a 500 Ohm terminal voltage of 1.4 volts, just sufficient to run some of the lower voltage integrated circuits.

Power is increased by four times to about a 1/2 milliwatt which is adequate for more efficient ICs.

At 0.75 meters (30 inches), we are far better off with 2.8 Volts at two milliwatts.. well within a useful voltage and power range. If in addition to transforming the input to the higher, 500 Ohm impedance, we also use a voltage doubler rectification scheme, it is quite possible to improve performance further.

At 915 MHz one can also provide extra antenna gain, if the application allows space for it, by using the surface on which the tag is mounted as a passive reflector. As much as 6 dB gain can be achieved in this way without increasing the tag's footprint, but this assumes that the tag is mounted to a metal surface and that the tag's antenna can be spaced as much as 1.5 inches from that surface.

Tags produced by IDX, Inc. in 1982-83 for transportation applications were actually able to achieve a sensitivity with under 130 dBuV/m using this technique. Since these tag were used in a higher powered, Automatic Vehicle Monitoring system under FCC AVM rules, we were able to achieve a 25 to 50 foot range reliably with about 30 Watts EIRP.

Generally speaking, however, totally passive tags in the 915 MHz band are going to be restricted to a reliable range of about 1-3 feet for FCC Part 15 applications.

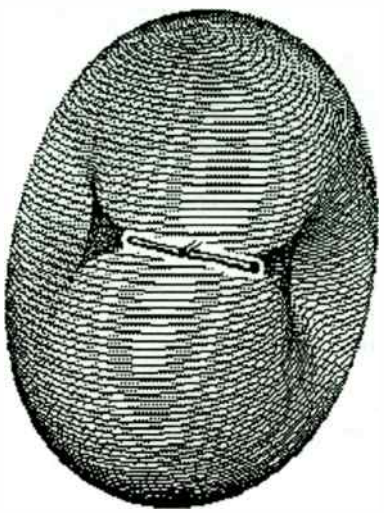
UHF Antennas

There are probably as many approaches to antennas for UHF and Microwave tags as there are applications. Several types are typical, however.

The most straight forward approach is to use a dipole or monopole antenna. This generally provides the most gain with the widest bandwidth but also may be too long for a given application. A half wave dipole at 915 MHz, for example, is about 154 mm long (6.3 inches) once length-to-diameter effects are taken into account. At 300 MHz, a dipole is about 475 mm long (19.4 inches).

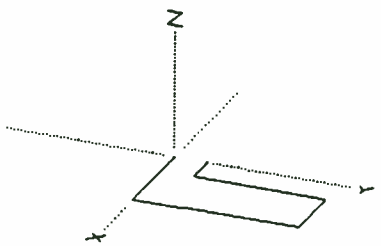
Various techniques like implementing linear loading on the printed circuit or using series inductors can shorten these lengths. There will always be a gain, efficiency, and / or bandwidth penalty, however (6). Furthermore, clearance needs to be maintained around this kind of antenna if full efficiency is to be expected.

The pattern, in these cases, is that of a dipole. It is omnidirectional if the dipole (or monopole) is vertically mounted, but is a figure eight pattern with deep nulls if mounted horizontally.



Basic Dipole Antenna Pattern

An alternative antenna developed most recently for pocket pager applications is the small loop antenna (see illustration). This antenna provides a much more spherical coverage pattern than the dipole but also has clear bandwidth, gain, and efficiency problems (7).

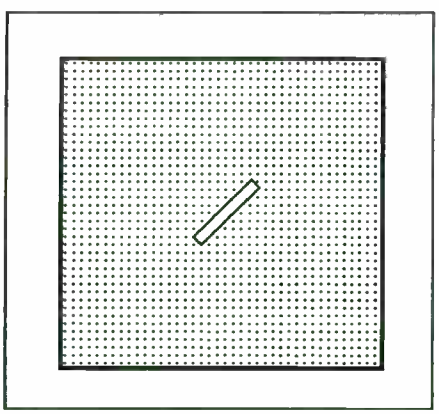


Small 303 MHz Loop Antenna

Small 303 MHz Loop Antenna Pattern

Microstrip Patch antennas are quite popular at Microwave frequencies because they can provide a very low profile(8). At 2GHz and up the patch can be quite effective. At 915 MHz, however, patch size starts to become more problematical (over 3 inches on a side) and at 300 MHz there are many better choices.

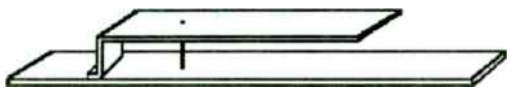
Single element patch antennas generally provide narrower bandwidth and less gain than a dipole. While they can be bi-directional, they are generally hemispherical in coverage.



Circularly Polarized Patch Antenna

Multi-element patch arrays are not very practical for frequencies under 5 GHz except for applications where antenna area is not important. A typical patch antenna at 2.4 GHz is more than an inch by an inch square and should probably be mounted on something at least two inches on a side.

A narrow, "half patch" has seen some use, especially in high temperature applications where it uses air dielectric and is constructed of sheet metal stampings. This provides a compact assembly though it is narrow in bandwidth and low in gain.



Half Patch Antenna

VIII. Conclusion

RF/ID has broad potential use but often tends to require customized approaches and application.

VLF provides the best opportunity for "mass market" approaches which are finally becoming available to potential end users as well as system integrators from several suppliers. It is limited in range, data rate, and may not work in electrically noisy environments, but is relatively low in cost, has a well defined pickup pattern, and allows batteryless operation for those applications requiring it.

VHF, UHF, and Microwave tags, on the other hand, can support very high data rates, much longer range, and provide much more immunity to the noise and interference often found in many environments.

Higher frequency tags can be made without batteries, but most require battery operation.

Development of RF/ID tags requires an integrated approach balancing mechanical, electrical, and software techniques against a variety of application requirements.

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Other Resources

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ID Systems, The Magazine of Automated Data Collection, (603) 924-9631

RF Monolithics, 1995 Products Data Book, (214) 387-8148 (has good reference info on both SAW based circuits and wireless regulations).

Texas Instruments, TIRIS Automatic Radio Frequency Identification Systems, 12501 Research Blvd MS2243, Austin, TX 78759 (512) 250-6617

Indala / Motorola, 3041 Orchard Parkway, San Jose, CA 95134-2017 (408) 383-4000

Data Logic, Inc, 104 Whispering Pines Drive, Scotts Valley, CA 95066 (408) 438-7000

ID Tag, LTD, Unit 1, Forest Park Business Centre, 18-25 Horndean Road, Forest Park, Bracknell, Berkshire RG12 3XQ 44 (0) 1344 482958

Cotag / Amtech, 17304 Preston Road, Dallas, TX 75252, (214) 733-6000

INTEGRAL BACKSCATTERING TRANSPONDERS FOR LOW COST RFID APPLICATIONS

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ABSTRACT

The article considers theoretical and practical aspects of low cost, long read range RFID transponder design, and compares different approaches in transponder reply and modulation techniques.

An overview of the harmonic, anharmonic, transmitting, sequential amplifier re-transmitting, and backscattering types of RFID tags is presented, with the most inexpensive type, the backsacttering tag, being considered in greater detail. The advantages of Schottky barrier diodes as backscatter elements for long read range microwave tags are shown. ASK and PSK modulation types with Schottky diodes as backscatter elements are described, and their advantages in passive and active tags are indicated.

Techniques for simplification of transponder design and improvement of transponder performance through integration of the backscatter element into the transponder antenna are described. A number of quasi-optical antennae, including loops, small electric dipoles, and patches, suitable for such integration in both passive and battery assisted tags, are presented. Experience of using a hybrid integrated circuit as a universal component for passive and battery assisted tags at different frequencies is illustrated. Such a standard component allows a significant reduction in both cost and time to market for new RFID products.

A description of a variety of the Company's RFID tags, based on the ISD6408 code generator chip and designed for the UHF and microwave bands of 434MHz (Europe), 902-928MHz (USA, Australia, South Africa, etc.) and 2.45GHz (world-wide) is included.

I. INTRODUCTION

Rapid growth of the area of wireless communications has given a new impetus to the radio frequency identification (RFID) industry, which is now growing faster than the most popular wireless consumer markets. World-wide unit sales of semiconductors for RFID applications were almost 10 times larger than for digital cordless phones in 1993, and are expected to continue to run well ahead of other wireless product categories, including cellular and cordless phones, WLANs and GPS. Kenneth W.Taylor & Associates (Redding, CA), a research and consulting organisation specialising in the global digital wireless communications industry, projects the world-wide market for RFID to grow from US$88 million in 1994 to US$1 billion in the year 2000, a growth of a healthy 34%annually [1].

Explosive growth in integral solutions for cellular phones and wireless LANs gives an excellent opportunity for a designer to apply standard RF ICs to RFID system development, with the result that RFID equipment will become much smaller and cheaper. Nowadays ASICs, designed specifically for RFID transponders (tags), are available off the shelf and significantly reduce cost of entry into this marketplace.

Over the history of RFID much experience has been accumulated and a variety of technologies developed [2]. However, because of the lack of standards in the industry, the task of selecting an appropriate approach to an automatic identification task can be quite confusing. While many RFID techniques are now available, the optimum solution to an RFID problem is influenced by many subtle aspects of each real application, and a user has to make a

decision on a particular way of implementation. As the user in this case may be either a system integrator or an OEM moving into RFID area, the selection may be difficult. To aid in this process, in the following sections the issue of operating frequency for RFID applications is discussed, and a brief description of major RFID tagging technologies is provided.

II. TRANSPONDER TYPES

RFID tags may be classified in frequency range as follows:

I 10-400kHz - low frequency tags;
II 3-30 MHz - medium frequency tags;
III from 300 MHz upwards - UHF and microwave tags.

The tags in classes I and II operate in the near field of the interrogator's antenna and read range usually does not exceed 5 ft. In order to achieve longer distances a far field communication link between the tag and the interrogator has to be established. Thus the class III frequency band gives the best opportunity to increase the distance between the RFID reader and a labelled object.

Like wireless LANs, RFID systems tend to occupy the Industrial, Scientific and Medical (ISM) *unlicensed* frequency bands. As the Federal Communications Commission's (FCC) Part 15 specified ISM bands are:

902 - 928 MHz
2.435 - 2.465 GHz
5.785 - 5.815 GHz
10.500 - 10.550 GHz
24.075 - 24.175 GHz

In order to meet the strong demand from the market for a low cost RFID systems, the first two bands should be considered seriously, e.g. around 915 MHz and 2.45 GHz. The latter band is attractive because it is internationally accepted (in Europe and Japan as well). Some European countries allow to use 434/458 MHz for RFID. Systems operating in any of these three frequency bands are excellent candidates for long read range electronic tagging applications.

In order to achieve the best performance of the transponder, the method of reply generation should be considered carefully. The most important of the reply generation techniques are discussed below.

1) In the *harmonic tags* [3, 4, 5], illustrated in Fig. 1, the reply code is superimposed as a modulation upon a deliberately created harmonic, usually the second, of the interrogation signal. This technique provides a good isolation between the down link (from the interrogator to the tag) and unlink (from the tag back to interrogator), but it suffers from the low efficiency of the frequency doubler (0.9% in [3]) and the need for a double-frequency antenna or even two antennae [4] for the tag. Moreover, there are no frequency bands allocated for unlicensed use at both frequencies.

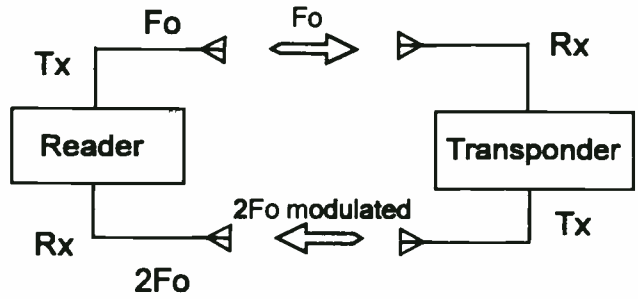

Fig. 1. Harmonic tag RF system.

2) Actively *transmitting tags* produce their own code-modulated RF carrier in response to interrogation [6]. These systems demonstrate very long read range capability even in a very limited radiated power environment, but can not compete with passive tags in cost as they require a battery and a stable microwave frequency source.

3) *Backscatter tags*, illustrated in Fig. 2, do not generate RF energy, but act as field disturbance devices by reflecting in a coded manner the incident RF signal. A generalised structure of this type of RFID tag is shown in Fig. 2. The tag can be significantly simplified if a Schottky barrier diode is firstly used to provide, by means of rectifying of the incident RF energy, a DC power source for the code generator, and secondly is used as a key element in the receiver, mixer and transmitter of the reply circuit. The realisation of several tag functions in one component makes this type of reply generation attractive for use in economical RFID systems and is described in this paper.

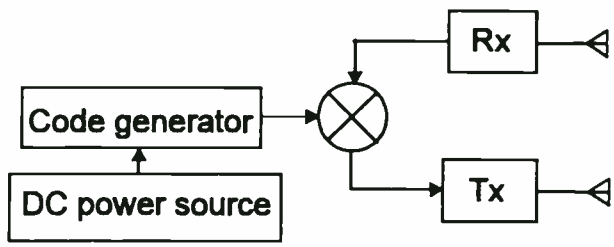

Fig. 2. Backscatter RFID tag structure.

4) Carrier frequency conversion (or *anharmonic*) types of tags [7, 8], illustrated in Fig. 3, consist of a receiving antenna at frequency F1, self-oscillating mixer at F2, an IF filter and amplifier at frequency (F1-F2) and a transmitting antenna at the IF. The frequency translation separates the reply signal from the interrogation. Both the IF amplifier and the LO in this tag may be modulated to generate a digitally coded reply. This arrangement eliminates one disadvantage of the harmonic tags through providing freedom in the location of the tag reply frequency, but it still possesses the weaknesses of the actively transmitting tag in terms of its complexity, requirement for frequency stability, and for a DC power source.

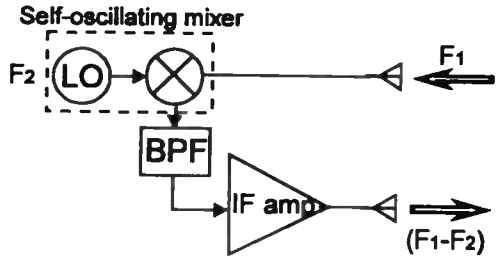

Fig. 3. Anharmonic tag.

5) RFID tags employing a *sequenced amplifier* [9], illustrated in Fig. 4, can achieve a read range comparable with that of a transmitting tag without actually generating an RF signal within the tag. The incoming signal from the interrogator is applied to the first RF amplifier (amp 1), which is turned on by the pulse generator. The amplified signal then goes through a narrow band SAW delay line. As is illustrated in the diagram, the second RF amplifier (amp 2) is turned off when the RF amp 1 is on and vice versa. When the signal is emerging from the delay line, amp 1 is turned off the amp 2 is turned on, and the amplified signal is transmitted back to the interrogator via a second antenna. The RF signal re-transmitted in this fashion is modulated by switching on and off amp 2 to provide an amplitude modulated output signal from the tag. The data rate of this tag has to be much lower than the pulse generator "sampling" frequency. In practice the data rate does not exceed a few kBaud. Avoidance of instability of the amplifiers caused by positive feedback via two antennas can be achieved by careful design of the amplifiers and ensuring good broad band isolation between the input and output of the amplifier when it is switched off.

Tag systems using sequential RF amplifiers have two advantages over transmitting tags, in that no strict requirements are placed on the tag frequency stability, and that the interrogator receiver can be of a simple homodyne type.

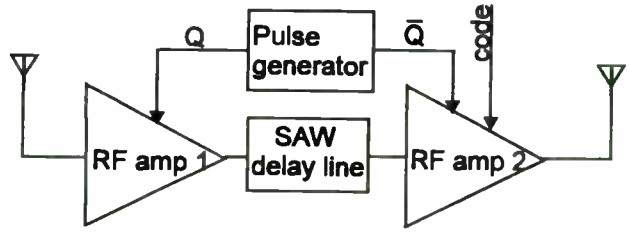

Fig. 4. Sequenced amplifier tag.

III. PASSIVE BACKSCATTER TAGS

A. Scatter methods

Analysis shows that backscatter type tags give the best performance-to-cost ratio and appear to be the most attractive solution for the majority of long read range automatic tagging applications.

There are three main functions to be realised by the tag:

- code generation
- RF signal receiving, modulation and sending back
- DC voltage generation.

To provide for the tag the most reliable endurance with respect to time and temperature, DC voltage may be derived from the incident RF signal of the interrogator via a rectifying process. A zero bias detector diode or a low barrier Schottky diode provides a high sensitivity and efficiency for the rectifier. As shown in Fig. 2, the rectified DC voltage supplies the electronic circuit generating the reply code and the modulation waveform, which in turn is applied to a modulator circuit.

The backscatter technique employs the principle of scattering of the incoming RF signal in a controlled manner. As shown in Fig. 5, for example, the tag antenna reflects the incident RF signal when the control data bit is "1" and absorbs RF energy when it is "0". In general, the scattered RF signal can be modulated by any means that alters the RF current flowing in the antenna, i.e. by changing the impedance with which the antenna is terminated. Any method that dynamically varies the resistance or reactance placed across the antenna terminals in

accordance with the desired modulation pattern can be used.

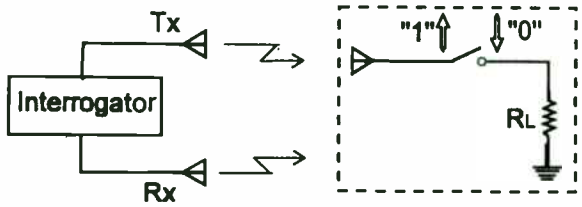

Fig.5. Simplified backscatter communication.

A variety of different approaches and phenomena can be employed to realise a modulated scattering [10]. For instance, as shown in Fig. 6a, a PIN diode may serve as a variable RF resistance and thereby modulate the signal scattered from the antenna. The resistance is controlled by varying a bias current through the diode. For a digital code re-transmission, the diode has two possible states: "on" (low resistance r , a few Ω) and "off" (high resistance R, a few kΩ). Thus the ideal impedance across the diode terminals will appear as in Figure 6b. The Smith chart shows that the impedance changes its state from open to short circuit and the magnitude of reflection coefficient remains constant, but its phase alters by 180°.

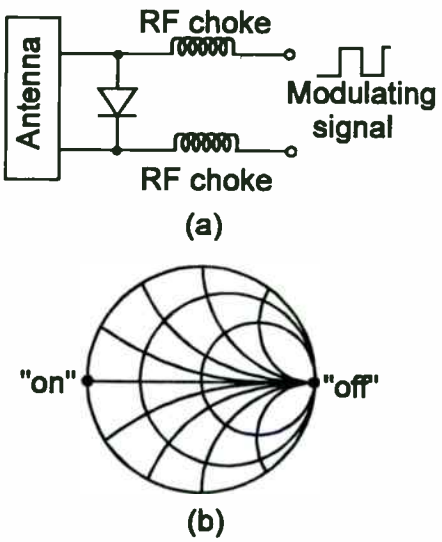

Fig. 6. PIN diode backscattering.

Therefore, by varying the forward bias on a PIN diode, bi-phase PSK modulation can be achieved, provided the antenna is self resonant and its radiation resistance satisfies:

$$r << R_{rad} << R, \qquad (1)$$

i.e., the antenna is well mismatched with the diode impedance in both states.

It has to be mentioned that a major disadvantage of the PIN diode backscatter method is the relatively high current to be applied to the diode (a few mA) to obtain its low resistance state.

Another method of modulating the scattered signal is shown in Fig. 7. The load current I_L of the rectifier is modulated by a combination of a switched FET and a resistor. The rectifier capacitor C is a low impedance bypass at the excitation frequency and a high impedance at the modulation rate. The modulation process, as in the case with PIN diode, is based on altering, relative to the radiation resistance of the antenna, the impedance of the diode which forms the antenna load impedance.

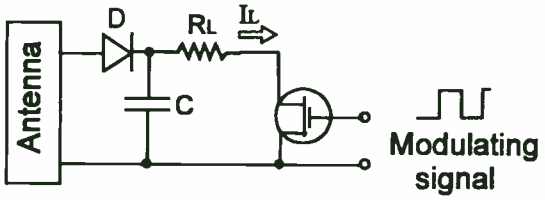

Fig. 7. Switchable diode load backscatter.

Depending on the state of the antenna load, the incoming RF signal is either absorbed or re-radiated by the antenna. The absorption of RF energy in one of the states may be achieved by matching the antenna impedance to the diode impedance at that state. Through this basic process, the incident interrogation signal is effectively amplitude modulated and for a digital modulating signal, ASK is implemented.

We can see now that the same Schottky diode can comprise several functions in the tag: a rectifier as a DC supply, and the modulator, transmitter and receiver of the backscatter process.

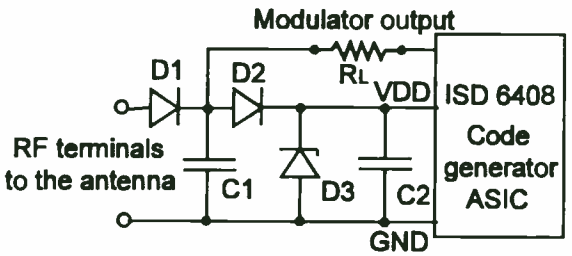

Fig. 8. Passive tag electronics.

A schematic circuit of the passive tag is presented in Fig. 8. The code generator of the tag is ISD's proprietary CMOS low threshold voltage ASIC ISD6408 [11], which generates a 200kHz sub-carrier and the tag's unique 64-bit code at rate of 50kbit/s, and superimposes it on the sub-carrier by means of a DPSK modulation technique.

The output modulator of the IC is a large FET serving as a switchable load for the rectifier circuit D1-C1. The second Schottky diode D2 with a low forward voltage drop together with a reservoir capacitor C2 across the supply rail provides isolation of the ASIC's power supply rail from the strong pull-down of the modulator. A Zener diode D3 in the circuit is used to safeguard the ASIC against excessive voltage which may be supplied by the rectifier. The circuit shown in Fig. 8 is implemented in a hybrid microcircuit OM1690 with dimensions 0.49" x 0.29" x 0.1" (12.5 x 7.5 x 2.5mm). This small footprint integrated backscatter device is a universal component for an RFID tag and can be used by a designer with considerable flexibility in conjunction with a variety of tag antennae.

B. Passive Tag Antenna Design

In order to meet the requirements of different applications the antennae shown in Figure 9 have been designed. The general requirements for the tag antenna are:

- small size
- high efficiency
- broad beamwidth for reduction of orientation sensitivity
- simplicity and low manufacturing cost.

The ASK backscattering technique requires that the input terminals of the hybrid OM1690 be well matched to the tag antenna in one of the modulation states and mismatched in the other. During the matched period of the cycle the modulator output is in a high resistance state and the rectifying diode D1 is loaded only with the ISD6408 voltage supply rail. The input impedance of the hybrid at 915MHz, in this operation mode is

$$Z_{hybrid} = 15 - j95\ \Omega \qquad (2)$$

A simple antenna which achieves that required match and allows a minimum of components in the tag will have an impedance conjugate to Z_{hybrid}.

Antenna 1 shown in Fig. 9 is a metal strip loop, printed on alumina substrate with dimensions 1.2" x 0.8" x 0.02" (30 x 20 x 0.5mm). The hybrid microcircuit terminals are connected to the antenna at the points A and B.

Antenna 2 has superior performance when the tag is mounted on a metal surface or even partly surrounded by metal. It is a small loop made of a piece of standard brass tube Ø0.83"x0.83" (Ø21x21 mm) with a slot. The width of the loop provides an increase in loop diameter for a given inductance, and thus an increase in radiation resistance, achieving a value suitable for matching to the hybrid. The loop antenna gain can, with the aid of its image, be increased up to 5dBi if it is, as shown in Fig. 9, mounted next to a conductive surface [12].

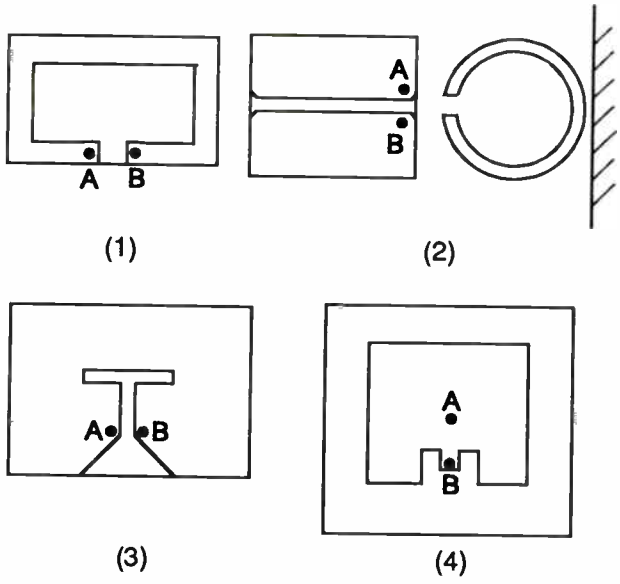

Fig. 9. Antennae for passive tags.

Antenna 3 is a combination of an open-mouth planar slot antenna and a small flat folded dipole with dimensions of a credit card [13]. To achieve these dimensions an ordinary resonant dipole antenna cannot be used at this frequency as half a wave length is 6.45" (164mm) which is double that of credit card size. A small electric dipole is not suitable because of its capacitive impedance; we need the inductive antenna to conjugate match the backscatter hybrid. So by shorting inductively the wings of a small dipole and adjusting the slot size the required impedance of the antenna is achieved.

Characteristics of the above described antennas are presented in Table 1.

Table 1. Backscatter tags characteristics with different antennae at 915 MHz.

Antenna type in Fig. 9	1	2	3
Q factor	40	40	15
Gain, dBi	0	2...5	2
Read range[1], m	3	5	>6
Application specific features	-very small size -high temperature applications	-compact, easy to use on metal surface -high temperature applications	-convenient credit card size -long read range

[1] *Typical read range measured above ground plane with interrogator power specified by FCC Part 15.*

C. Quasi-optical patch antenna for a passive tag at 2.45GHz

The hybrid microcircuit with microwave and low-frequency components on board can be successfully employed in tags at frequencies below 1GHz, but at higher frequencies the presence of parasitic components and loss in the hybrid lead to separate RF and LF sections of the backscattering system. A circuit diagram of the passive backscatter is shown in Fig. 10, wherein D1 is rectifying/backscattering diode HSMS2820 in a low cost SOT-23 package and OM1690S is a special version, no rectifier on board, of the tag hybrid used at frequencies higher than 1GHz.

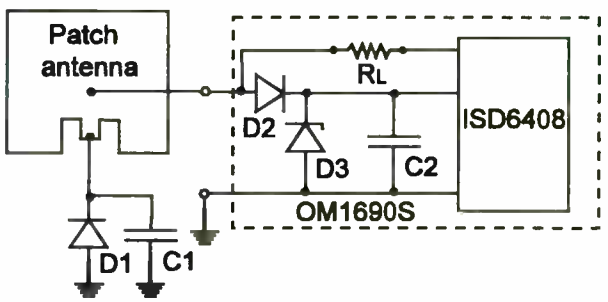

Fig. 10. Passive backscatter tag schematic at 2.45 GHz.

A half a wavelength patch antenna of the tag is printed as shown in Fig. 9(4) on a credit card size woven teflon substrate with ε_r = 2.55 and thickness 0.062" (1.6mm). It has gain about 6dBi and is non-sensitive to proximity of any objects behind its ground plane.

For a conjugate match between the antenna and the diode an antenna impedance of Z_{ant} = 5 + j50 Ω is required. A half a wavelength patch has impedance measured at the edge of the patch [14]

$$R_{in} = 60\,\lambda / W,\ \Omega \qquad (3)$$

where: λ - wavelength in free space
W - width of the patch.

For a square patch antenna this impedance is relatively high at

$$R_{in} = 60\lambda/(\lambda/2)=120\ \Omega \qquad (4)$$

In order to obtain much lower real part for the patch impedance, a cut out in the patch towards its centre has been made. An appropriate inductive impedance has been achieved by means of a narrow strip through the middle of this cut out.

Thus the antenna is matched to the diode impedance and a low frequency connection between the diode and the hybrid circuit is implemented at the centre of the patch, where RF voltage is at its minimum [14]. So all the backscatter functions of the tag are realised without lossy RF chokes and matching networks. This quasi-optical approach [8] improves the tag efficiency. With interrogator eirp of 500mW[2] the tag showed over 1m read range.

IV. ACTIVE BACKSCATTER TAG

As EMC regulations in the world tend to move even in ISM bands in the direction of lower radiated power, the problem of achieving a desirable read range for RFID tags becomes crucial.

[2] *In accordance with European regulations.*

The range of established microwave links can be significantly increased if a long life lithium battery is utilised to supply the code generator IC in the tag. In order to save the battery life a wake-up (tum-on) circuit should be included into the tag. This circuit turns on the code generator and the backscatter circuit only when an RF pulse of known frequency is received from the interrogator.

The active tag usually consists, as shown in Fig. 11, of a receiving antenna, detector diode, tum-on circuit with a battery, code generator, backscatter diode and backscatter antenna. Separate receiver and backscatter channels are chosen deliberately in order to provide optimum performance of each of them to achieve maximum read range of active tag. Thus, the envelope detector diode is optimally matched to the receive antenna for maximum sensitivity of the tag, and the backscatter diode is deliberately mismatched, in both of its states, to its antenna for both maximum reflection from the backscatter antenna and for high resolution between two states of the digital modulation.

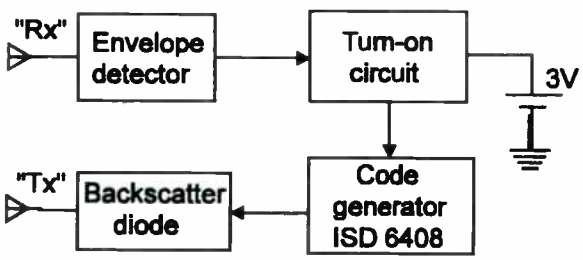

Fig. 11. Active tag block diagram.

To satisfy the latter condition the PSK type of modulation of the RF signal, which allows up to 6dB improvement over ASK in terms of net probability of error performance, should be employed.

This function can be economically implemented utilising, instead of resistance in a PIN diode, the modulation of a reverse biased Schottky diode reactance. For instance, HP5082-2800 diode has the depletion region (or transition) capacitance C_{T1} = 2.0pF at no applied voltage (V=0) and C_{T2} = 1.0pF at negative bias of 2V. Ideally for bi-phase shift keying the impedance of the backscatter diode would appear as shown in Fig. 12. At frequency f_o = 434MHz[3] the diode reactances are:

$$X_{d1} = 1/(2\pi FC_{T1}) = -183\ \Omega \text{ at } Vd = 0V$$
$$\text{or} \qquad (5)$$
$$X_{d2} = 1/(2\pi FC_{T2}) = -367\ \Omega \text{ at } Vd = -2V$$

To make these impedances symmetrical on a Smith chart, a series inductance should be added. The value of this inductor is

$$XL=(Xc1+Xc2)/2 = 275\ \Omega$$

$$L=XL/(2\pi F) = 101nH \qquad (6)$$

The input impedance of the diode with the series inductor are then:

$$+92\ \Omega \text{ at } Vd = 0V$$
$$(7)$$
$$-92\ \Omega \text{ at } Vd = -2V$$

To yield a high value of modulation index and obtain desirable impedances +/-j on the normalised Smith chart the antenna active impedance should be 92 Ω. This is easily achievable by a careful choice of a feed point in a resonant patch antenna.

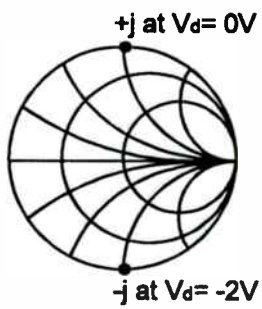

Fig. 12. Input impedance of reactively modulated backscatter element.

Figure 13 shows a schematic diagram of the battery assisted tag at 434MHz which demonstrated read range capability up to 10m with eirp=500mW. The quarter wavelength patch antenna for the tag is printed on a polyguide substrate with thickness t=0.125" (3.2mm) and ε_r = 2.32 (Polyflon Company, Norwalk, CT).

[3] *Available band in Europe*

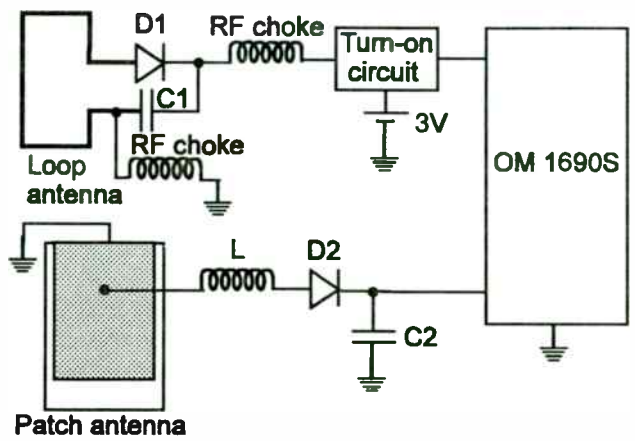

Fig. 13. Battery assisted tag at 434 MHz.

Similar calculations at 2.45GHz with lower capacitance diode HSMS2820 will give the following values:

$$\text{with } C_{T1} = 0.8\text{ pF} \quad \text{at Vd} = 0\text{V}$$
$$C_{T2} = 0.5\text{ pF} \quad \text{at Vd} = -2\text{V}$$

$$\Rightarrow \quad L = 6.6\text{nH} \text{ and } Z_o = 22\,\Omega \qquad (8)$$

The system environment of 22 Ω could be implemented by the appropriate feed point in the patch antenna or a quarter wavelength microstrip transformer from 50Ω into 22Ω with $Z_o = \sqrt{50 \cdot 22} = 33\ \Omega$. A narrow microstrip line could be used as an inductor L as well.

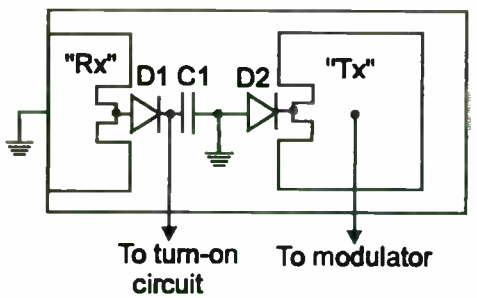

Fig. 14. Antenna structure of a battery assisted backscatter tag at 2.45 GHz.

A higher integration of the battery assisted backscatter tag is implemented using quasi-optical approach eliminating the need of any matching networks on board and hence reducing loss. Figure 14 shows the antenna structure of the tag at 2.45GHz, demonstrating read range up to 8m at eirp = 500mW radiated by the interrogator. Two patch antennas are printed on a credit card size polyguide substrate (t=0.062"=1.6mm): a quarter wavelength patch as a receiver antenna and a half a wavelength patch as a backscatter antenna. The cut-outs in the patches serve to provide appropriate matching between the HSMS2820 diode and the antenna. The receiver antenna has 2dB gain, lower than 6dB of the backscatter antenna. This has been done to match the communication ranges capability for the downlink (from the interrogator to the tag) and the uplink (from the tag to the interrogator).

V. CONCLUSION

A variety of small sized and low cost antennae has been developed for use with RFID tags in different ISM bands. The quasi-optical approach offers significant performance benefits as well as reduced size and complexity to microwave backscattering transponders. Combining circuit and antenna functions into compact processing structures and using a universal integrated backscatter IC reduces the cost of the tag and gives great flexibility for a user at the same time.

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RFID Systems Design

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Time-to-market issues can be managed by using off-the-shelf integrated circuits (ICs) designed for RFID. Several single-chip transponders are available which allow the user to place them in different operating modes thereby allowing a unique product to be developed with standard programmable parts.

Various applications using different interrogation methodologies will be discussed and various transponder chips will be shown to have certain strengths for specific applications.

The relationships between modulation methods and return data frequencies will be examined and optimization of the channels will be explored.

Radio Frequency Identification - Traffic Management Assistance

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Abstract: Key words; electronic tolls, commercial vehicle operations, vehicle roadside communications, RF/ID, Radio Frequency Identification.

Radio Frequency Identification (RF/ID) has found many applications in security, time and attendance accounting, manufacturing process control, inventory control, personal identification, animal identification, and medical identification and control. Most of the systems used for these applications are represented by low frequency, low speed, read only, and close proximity technologies.

A second tier of RF/ID technology is currently making great inroads into the highway systems around the world, with major projects in progress in the United States and Canada. This level of technology generally has operational parameters that include high frequency, high speed, long distance communications, and on-the-fly read/write capabilities. Because of these enhanced operational characteristics, RF/ID is finding excellent acceptance in such operations as electronic tolling (road-ways, bridges, and tunnels), commercial vehicle operations, and vehicle to roadside communications applications.

This paper will examine some of the current programs in progress, such as Advantage I-75, HELP, Highway 407, Oklahoma, Kansas, Illinois and Maine Turnpikes, and others. In each example, the technology of choice and the characteristics that drove its selection will be discussed.

The final portion of the paper will address possible future applications, where the new application may be able to take advantage of the technology already in place for other uses.

Advantage I-75

The Advantage I-75 program is a Federal Highways Administration (FHWA) operational test program, with the primary investigation being Commercial Vehicle Operations (CVO). In this particular project, the objective is to examine the benefits, and costs, of providing weigh station bypass to certain participating trucking firms.

The concept of the program is to enable a truck approaching a weigh station to be weighed by high-speed scales at highway speeds, commonly referred to as weigh-in-motion (WIM). While not as accurate as a static scale, the WIM equipment provides a reasonable screening for the trucks approaching the weigh station. Once the weight is obtained, it is passed to a Vehicle Roadside Communications (VRC) system, which then checks the truck for a transponder. If the truck is so equipped, a number of other items such as safety record, credentials, axle weights, gross weights, and enforcement officer overrides are examined. If all checks are within acceptable values, the truck is signaled, via a green light on the transponder, that the truck is authorized to bypass the upcoming weigh station. If any of the parameters do not meet specified criteria, the driver is signaled with a red light on the trans-ponder, indicating that the truck is to pull into the weigh station for normal processing.

The intent of the system is to enable certain authorized truckers the opportunity to bypass weigh stations, thus saving the trucking firm time, providing better fuel economy, less tire and brake wear, and an added public safety factor, as the trucks do not have to slow to enter the station nor accelerate into high speed traffic upon exit.

The RF/ID technology selected for this particular project was that of Hughes Transportation Management Systems, Fullerton, California. The system was required to provide read and write communications between the truck and the weigh station. It was also required, in Phase 2, that an off-transponder communications interface be supported. The Hughes technology met both the Phase 1 and Phase 2 requirements with their initial offering. That particular aspect of the technology offering was essential in the selection of the Hughes offering.

The Advantage-75 program is currently entering a two year test phase, with some thirty sites scattered between Florida and Ontario, Canada. When it is fully operational, truckers may enter the corridor in Florida, and not stop at another weigh station along the entire route. In its initial acceptance and test, the system has received good reviews from the trucking industry.

Oklahoma Turnpike

The Oklahoma Turnpike Authority had an interest in providing a more efficient manner in processing people through the toll plazas across their tollroads. The system selected had to provide central control, yet allow users to travel any of the

roads, using a common technology.

In this case, the Authority selected the technology offering of Amtech Corporation, Dallas, Texas. The technology offers a 128 bit identification for each transponder, and is read only. In this manner, the transponder is used to identify a particular user of the roadway, and all account information is handled in a central office. When a user passes a toll plaza, the identification number from the transponder is read, and the account balance verified. The user will then be signaled, via an external lighting fixture, to continue, stop and pay a toll (account balance zero), or be given a warning signal that the account balance is below some pre-defined minimum and it is time to replenish it.

The system selected is simple and rugged, and has found a number of applications in other areas, especially where the operational environment is harsh.

Illinois Thruway

In a manner similar to that of the Oklahoma Turnpike Authority, the Illinois Thruway Authority decided to implement an electronic tolling system. However, the requirements in this case included the ability for in-car signaling of account information to the patron. Because of the direct signal capability requirement, the technology selected was provided by AT/Comm, Marblehead, Massachusetts. The AT/Comm technology not only provides direct patron signalling on the transponder, it also provides account balance information directly for multiple accounts on the transponder.

The latter feature, multiple account balance, is a design feature which allows AT/Comm to suggest that different Agencies could use a common technology for applications that are similar, i.e., road tolls, bridge tolls, tunnel tolls, and so forth. AT/Comm supports up to ten different account balances in their transponder.

Kansas Turnpike Authority

The original Kansas Turnpike Au-thority system was a ticket system, where the patron was given a ticket upon entry and was billed for distance traveled upon surrendering the ticket at exit. Again, for better patron service during peak traffic hours, the Turnpike Authority searched for an RF/ID technology which could be used to replace the paper ticket with an "electronic" ticket.

In their original request for quotes, one stipulation that weighed heavily was the need for the selected technology to be "compatible" with existing systems in use in Oklahoma and Texas. This, for

practical purposes, forced the selection of an Amtech Corporation system. In this particular case, a recent joint venture between Motorola and Amtech Corporation, Intellitag, Inc., was selected.

The technology selected provides read/write operation, and a transponder signal light system which can be used to signal the patron on account status. No account information is maintained on the transponder.

Inter Agency Group

One of the more significant groups looking to RF/ID for assistance in patron service is a conglomerate formed by New York, New Jersey, Pennsylvania, and Massachusetts. The group consists of turnpike authorities, bridge authorities, tunnel authorities, etc., all with a common solution as their goal.

Based on some early project testing, two companies were selected to continue to the second test phase, Amtech Corporation, Dallas, Texas, and Mark IV Industries, Missasauga, Ontario, Canada. This competition has recently been reduced to the Mark IV technology being selected as the system to be implemented. An interesting note, Mark IV has provided as their technology growth path, the architecture and implementation of the Hughes Transportation Management Systems technology.

Canada 407

The Ministry of Transportation - Ontario has recently proposed Highway 407, a new highway north of Toronto. While the idea of another highway is not new, the idea of the highway being paid for by tolls is somewhat different. As a result, the Ministry sought a technology solution which could provide an all electronic toll system (note the word all) as the system had to provide a mechanism for capturing use of the road by "casual" users as well as pre-paying patrons.

The technology selected was that offered by Hughes Transportation Management Systems, Fullerton, California. In this case, the RF/ID technology was augmented with the use of a video image capture and processor for use with the casual user processing.

The video will also be used to process billings for anyone attempting to use the roadway with the intent of not paying the required toll.

The Future

The applications discussed to this point are here today. They have been, or are being, implemented and proving their usefulness on a daily basis. Other agencies will decide to select one of the already discussed suppliers for their technology, or some new, emerging supplier and

implement their particular application. The biggest drawback to the general rollout of the technology is the lack of an industry standard or standards for the technologists. Most of the current systems are proprietary.

Let us, for the sake of argument, assume that the lack of a standard will be solved by industry pressure, and that a standard emerges which permits multiple suppliers to read, write, and otherwise process transponders from other suppliers.

When such standards emerge, a number of additional applications can occur. For example, if a trucking firm has transponders on its vehicles which are used for toll applicaitons, why can't those same transponders be used to track the vehicle into and out of the trucking firm yards, thus providing simple inventory tracking of the firm's valuable assets - their trucks and trailers.

In a second case, why not enable users of toll roads to use the same transponder in parking garages or airport parking facilities? With common interfaces and communications, the same transponder could be used for both.

One might also say, that with the spread of such devices, government could place tracking stations around and begin to track citizens, thus knowing where they are and have been. While such things could occur, are they any different than the trail left by credit card purchases, bank drafts, telephone calls, and the like? No, it is not.

RF/ID applications will continue to evolve as more systems are installed and industry standards are finally implemented. The RF/ID technology has many of the same traits that Bar Codes employ, with the major differences being the remote detection and harsh environment operation that RF/ID offers over bar codes. Just as in bar codes which were once thought to end with their use for product marking, RF/ID will continue to find new and more complex applications in the future.

A Combined High Security Remote Keyless Entry and Immobilization System

by

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I. ABSTRACT

Crime and vehicle theft are on the increase and with the high cost of cars and insurance today; the need for sophisticated vehicle anti-theft devices are in demand.

This paper focuses on the architecture, design development, breadboarding, and packaging of a combined high security Remote Keyless Entry and Immobilization (RKE/I) system for automotive applications to deter vehicle theft and enhance recovery; discussing problems and trade-off solutions necessary for the system's wireless low and ultra-high frequency mixed signal implementation in silicon. The full system's mixed signal implementation incorporates SMARTMOS™ having CMOS logic, bipolar/MOS analog circuitry, DMOS drivers, and MOSAIC™ technologies.

II. INTRODUCTION

Remote Keyless Entry (RKE) systems were first introduced a few years back by U.S. automotive aftermarket suppliers and touted as a convenience feature. The convenience of RKE was many times incorporated with anti-theft alarm systems. As the public's acceptance for this "nifty" feature increased in popularity along with the ever increasing demand for alarm systems; vehicle manufacturers (OEMs) themselves got into the act where now most manufacturers offer RKE as an option, if not standard, on many models.

Europe on the other hand was having it's own vehicle theft problems. With the eastern block countries opening up, cars were being stolen and transported to other countries making recovery very difficult. Insurance companies imposed stiff insurance premiums on owners of cars that did not have a secure anti-theft immobilization feature which would rendered the vehicle inoperable by anyone not authorized for it's operation. The insurance companies in Germany were successful in getting legislation passed, mandating some form of Immobilization to be incorporated on all 1997 and later vehicles to deter such thefts.

European manufactures did not buy into RKE initially for the reason that most European cars had mechanical locks whereas most U.S. vehicle models had already adopted some form of electric locks. The European automotive manufacturers are rapidly incorporating electric locks making possible both RKE and Immobilization. Conversely, U.S. manufacturers are adopting the Immobilization feature for much the same reasons as did Europe. Insurance companies in several states mandate discounts be given to vehicle owners having anti-theft devices installed. The U.S. leads the world by having almost two million cars stolen each year. In addition to stolen cars, there are nearly three million that are broken into each year and have contents stolen. Japanese auto manufacturers are also adopting the features to meet their export market needs.

III. SECURITY PHILOSOPHY

First it should be pointed out that if a thief wants your car bad enough, he'll get it and no security system can stop him. A thief can load a car into a shielded truck and drive away and no detection system can track it for retrieval purposes. All vehicle anti-theft systems reduce to one of being a deterrent to theft rather than an absolute guarantee where by the thief is forced, by a good system, to go to great lengths to steal a car and in the process runs a very high risk of being caught in the attempt. Most cars are stolen by individuals under the age of 21 using relatively cheap and unsophisticated hand tools; such as a slim-jim or a screwdriver.

ARCHITECTURE

A. System Requirements

Aside from the intended purpose of security, the system should be low cost. OEMs are facing product pricing resistance by their customers and will not tolerate costly systems, regardless of their performance. System cost is a major issue and it has been said "the first nine rules of system design are cost, and the tenth is performance". Reliability and low power consumption are also important, both in the vehicle and the key. OEMs would like the system to be trouble free for the life of the vehicle; ten years or more in most cases.

Having cost, security, and performance as dominate guidelines; system versatility, flexibility, and small physical size are of importance to both the silicon supplier and the OEMs.

B. General System Description

1. Vehicle-Side

It was decided early that the vehicular side of the system should be Micro-Controller Unit (MCU) based so as to provide a cost reduction, along with higher levels of security, versatility and flexibility for automotive OEMs.

The security function can be performed by using only a small amount of a modern MCU's capability. By including this function in an MCU that is performing other needed functions in the vehicle, a dedicated single-purpose IC is eliminated.

There is added security in this approach as all the validation would be contained in an MCU which could also control vital engine functions. If the validation were performed externally a thief could override the system by knowing which logic line tells the controller a valid key response has been obtained. With the validation function contained in the MCU along with some vital functions of the vehicle, no such simple override would be available.

An MCU based system would allow a vehicle's feature set to be easily adopted via software modification, leaving only the feature's specific hardware to be added to the vehicle. For instance, if remote immobilization capability were desired to be implemented by an OEM to cover the event of a thief stealing a valid key with which he then uses to steal the car; the OEM could add a pager or cell phone to have the capability of initiating a software programmed remote shutdown procedure.

Where a pager or cell phone is installed, the vehicle owner alone could remotely initiate the programmed shutdown procedure and not require police assistance in doing so.

Another possibility is for the police to have the capability of broadcasting a wide area Ultra-High Frequency (UHF) signal gaining access to the vehicle's UHF receiver and MCU calling for a priority shutdown procedure to commence, specific to the stolen vehicle. So as to prevent governmental abuse, the police's wide area UHF broadcast system could require the owner to produce a valid spare key in order to transmit the priority shutdown signal to the stolen vehicle; the code information contained within the spare key being essential in sending a recognizable priority signal to the specific vehicle. Any of these approaches would preserve the owner's civil rights and prevent governmental abuse.

One can envision a car thief driving the stolen car down a freeway, thinking he has gotten away, only to have the car start mis-firing and get progressively worse with time, to the point where the thief is forced to pull over to the side of the road and stop. At this time the stolen car could go into full immobilization; shutting off the vehicle's fuel pump, fuel injectors, ignition, and starter while locking the transmission and steering, and causing the vehicle's horn to honk and lights to flash.

To carry the scenario further; if a Global Position Satellite (GPS) receiver were on-board the vehicle in addition to a cell phone, or some other suitable transmitter; the vehicle's position could be broadcasted to authorities making for easy retrieval. In any event, it is doubtful the thief would hang around for roadside assistance to appear on the scene and the owner's car would be readily identifiable.

The point to realize is that by having the system MCU based; many feature scenarios can be accommodated with relative ease through software implementation.

2. Key Side

The portable half of the system (key side) is shown in Figure 1 and is envisioned as being a conventional key, within which there is an embedded integrated circuit (IC), field coil, capacitor, battery, and keypad switches. The blade of the key serves as an antenna to provide better radiation than would be the case where the IC is within a key fob with it's contained loop antenna shielded by the person's hand during operation.

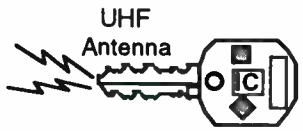

Figure 1. Combined Electronic/Mechanical Key

Having a conventional key available is handy for back-up purposes in the event the car's battery fails and the owner needs to gain entry into the vehicle; if for no other reason than to replace the cars dead battery, which is usually located in the secured engine compartment area. The conventional key is also worthwhile as a back-up in the event the RKE feature itself fails allowing the owner manual entry into the vehicle. Though the system could eliminate the conventional serrated mechanical key and be totally electronic, it is felt the mechanical key still has a place and purpose, particularly in areas requiring less than maximum security.

Content security of the vehicle might be considered as being of lesser security as opposed to the operational security of the vehicle itself, nevertheless the same high level of code security is provided by the system for both access and operation of the vehicle.

The key side IC incorporates a UHF transmitter, Low Frequency (LF) transponder, messaging algorithm, and battery charger. There are no MCU or EEPROM requirements on the key side. They are not necessary and we chose to eliminate them in the interest of reducing the key cost. The key provides both RKE functions (unlock driver door, unlock all doors, lock doors, panic/alarm, etc.) as well as validating the vehicle's operation.

Figure 2 shows a simplified block diagram of the internal key.

3. Communications

The vehicle side incorporates an MCU, UHF Receiver, and LF read-write inductive circuit. The LF read-write inductive coupling serves as a two-way communication between the key and vehicle side MCU whenever the key is in the ignition lock. The LF communication link also supplies energy to the key with which the key is able to power itself up, process data, and communicate back to the MCU.

As a fail-safe feature, the transpond process is not dependent on the key's battery but does report the key's battery status to the MCU every time the key communicates to the MCU. If the key's battery is deficient, the MCU causes energy to be transferred from the vehicle's energy source to the key via the inductive link to recharge the key's on-board battery. The key's battery is used only for RKE functions and the preserving of essential code information passed to the key by the vehicle's MCU when last used in the ignition lock. This information is required by the key in order for the key to generate a different RKE validation code (rolling code) and transmit it to the vehicle MCU every time the key is used to perform some remote function. Figure 3 shows a simplified block diagram of the vehicle side of the system.

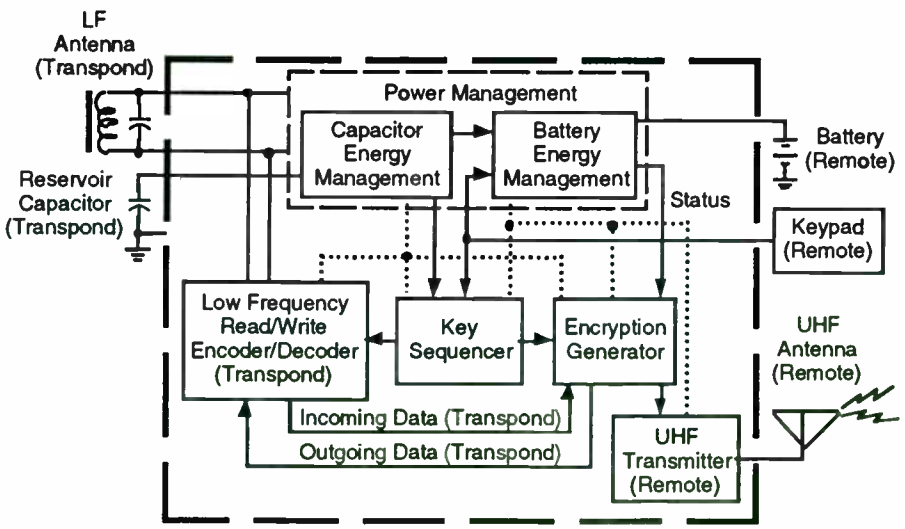

Figure 2. Key Block Diagram

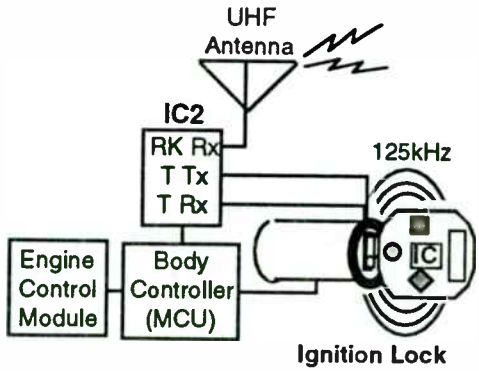

Figure 3. Vehicle Side MCU Based System

As pointed out earlier, many cars already have an on-board MCU to perform vehicle body control functions; a second vehicle side MCU being unnecessary. Normally the vehicle's Body Control MCU is able to talk to the Engine Control's MCU to support any disabling functions associated with the vehicle's drive train. Door locks, windows, lights, horn, etc. are body control module functions and have direct access to the security system.

A simplified block diagram of the vehicle side IC is shown in Figure 4 that incorporates the active elements of a UHF Receiver, an LF Transponder/Driver and a Control Sequencer.

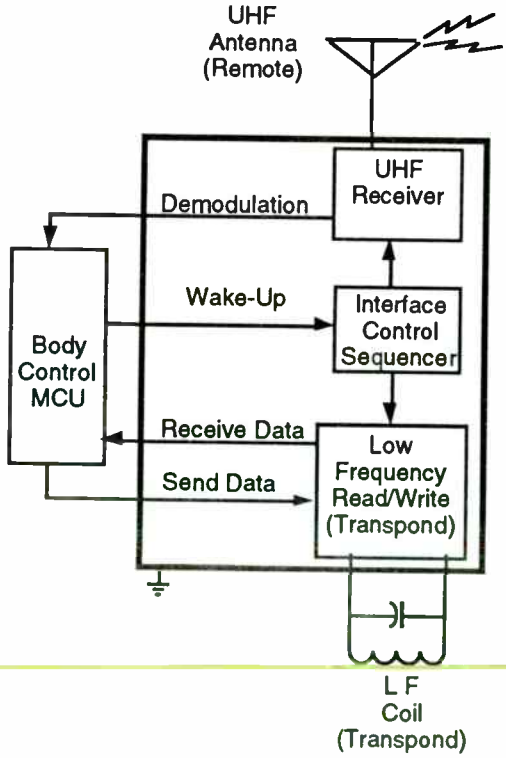

Figure 4. Vehicle-Side IC

C. Operation

1. Immobilization

In this system, the vehicle MCU knows each and every valid key outstanding. When a key is inserted in the ignition lock, it is sensed by the vehicle's "key-in" switch. This signals the MCU to send the key energy with which to power itself up and a "packet" of newly generated data by way of the LF (125kHz) inductive coupling asking the key to transpond back it's identification (ID) and results of processing the received packet of data.

The key responds by switching a load across the inductor in the key, resulting in more energy being extracted from the field. This is sensed on the vehicle side as a fluctuation of the voltage across the coil around the ignition switch. The switching is modulated off-and-on by a sequence of 40 bits of data containing the key's ID and the data processing results embedded within the message frame.

Since the vehicle's MCU knows all outstanding keys; the MCU compares the transponded results with what should be transponded back for that specific key's ID. If a data match is obtained, validation is obtained and the ignition start function is allowed to progress.

The start time delay as a result of the electronic validation process would occur in less than 75 milli-seconds and would not be perceptible to the cars driver at engine start up. If validation were not obtained, the software programming of the vehicle side MCU by the OEM would dictate the action to be taken.

The software may first allow an immediate retry with a new packet of data sent to the key; if validation were again denied, the software may ignore another retry until a specific time had lapsed. The vehicle would remain in a full immobilization state until successfully validation of the key was obtained.

2. Keyless Entry

For remote operations; The key uses the encrypted data sent by the vehicle's MCU when last used in the ignition lock. This data is used to generate a new rolling code for validation. Every time the key is used remotely, a different code is transmitted to gain validation by the vehicle's MCU. A unique encryption technique is employed to maintain message synchronization between the key and the vehicle's MCU.

3. Password Generation

The key's processing (encryption) of data sent it by the MCU is modulo-2 serial stream processed using a number of maximal length polynomials so as to assure that with the change of even a single bit in the seed value, the output will change completely and bear no resemblance to the previous value.

4. Modulation Coding

FM0 coding is used for both the UHF RKE and LF Immobilization. This is a modified Manchester coding that has the property of an average output of 0 (no DC component) regardless of data and will decode correctly even if the data is inverted. The tolerance of data inversion is most important for a Frequency Modulated (FM) system where the sense of positive transitions can be changed by a high-side mix in the receiver.

5. Technology Choices

Stringent size requirements are placed on the key side of the system. It is important to minimize the component size and count in order to keep the key head size from growing. This must be done without forgetting the major overall design factor of cost. A classic method would result in a two-chip set in the key; one for the RF/Analog requirements and one for the Digital requirements. It is possible to combine both of these functions into a single mixed-signal IC but, will only make sense if it is cost effective.

IV. DESIGN DEVELOPMENT

A. Key Logic

The key logic can be performed by a state sequenced logic device. The overall size and cost of this type of approach is less than would be obtained by using an MCU. The function of the logic on the key side of the system is well defined and will not impact the overall system flexibility. This is not the case on the automobile side of the system where many features will be added and changed by the manufacturer. The logic on the automobile side will be performed by an MCU which may already exist in the vehicle.

In order to smooth the transition of the logic from breadboard to production, the design was modeled at a high level using Verilog-HDL. This textual description was converted to actual gate design by using Synopsys. The breadboard uses a Xilinx FPGA as the target for the logic. This allows verification of the logic description and affords any necessary logic changes to be implemented relatively easily. The ease of making changes during the breadboard testing and field evaluation is very important in order to arrive at the best logic solution.

The transition of the logic to the final production device can be made with a high degree of confidence by using the same high-level description that was arrived at during the initial design and breadboard/field test activity. Again, Synopsys will still be used but the target will be the dedicated key logic device instead of the FPGA.

B. RF/Analog

The RF/Analog development follows the relatively standard approach of using available components to breadboard the design for field testing and the transition of the tested design into the IC device.

C. System Considerations

In order to minimize the cost and size of the key side of the system while maximizing performance, a system approach must be used. The following requirements were arrived at for the IC, based on a reduced cost and size of the finished key even though the cost of the IC would be increased.

Phase-Locked-Loop (PLL) UHF Generator using the low frequency logic clock oscillator. This reduces the need of requiring only one resonator and the need for tuning a LC oscillator.

Use of frequency steering in the PLL. This eliminates the need for tuning the free-running frequency of the PLL tank circuit to get it close enough for the PLL to pull-in. A standard chip inductor and capacitor can be used in the LC tank.

FM generation through pulling of the reference oscillator. This allows the use of a fast PLL loop to clean up the noise resulting from the use of small low-cost oscillator components and microphonics due to physical handling. It also reduces the size of some of the loop capacitors and eliminates the need for more costly precision components to be used.

Push-Pull RF Output. This reduces even order harmonics and reduces the need for output filtering. A combined inductive pickup/UHF matching transformer will

reduce parts count and take advantage of the push-pull output.

Automatic Level Control (ALC) using output level sensing. This will reduce output variation caused by how the person holds the key and status of the battery's charge. This allows more consistent range performance while keeping the output below the allowed level under best case conditions.

1. Modulation

Current systems use Amplitude Modulation (AM) in the form of On-Off Keying (OOK). This allows the use of simple regenerative type receivers. When RKE systems were only occasionally found, interference between systems was not a major problem; this is now changing.

Regenerative receivers generate signals that are on the received frequency. This can result in the jamming of receivers by other receivers in nearby cars. This problem of on-channel radiation has brought the use of regenerative receivers under scrutiny and legislation may eventually preclude the use of these receivers in many countries of the world.

Moving into a super-heterodyne type of receiver opens the possibility of using FM. The most attractive thing about using FM is the consistency of operation due to the "capture effect" of wide-band FM. The rapid establishment of a high post detection signal-to-noise ratio (SNR) as the pre-detection SNR climbs above 9 dB makes the use of error-detection and correction unnecessary. In large parking lots where simultaneous transmissions will occur, the "capture-effect" of FM will reduce the possibility interference will be a problem as long as the desired key is closer to the correct vehicle than an interfering key (an expected situation).

The attractiveness of a simple LC OOK transmitter from a cost standpoint begins to diminish when it's need for adjustment is addressed. There is also a desire to make the key water-proof so that it will survive inadvertent trips through a clothes washer or accidentally getting water in it (heavy rain, forgetful swimmer, etc.). This will most economically be achieved by encapsulation.

The tuning and holding of frequency by the tunable elements in a simple LC oscillator could be a problem for encapsulation. The use of a Surface Acoustic Wave (SAW) device to set the frequency could solve this problem but, the cost of the SAW device could exceed that of an IC which uses the logic clock resonator (needed for data rate stability) to derive an accurate, no-tuning-needed, frequency.

V. BREADBOARD

A. Automobile Side Breadboard

The Automobile breadboard consisted of a UHF receiver (320 Mhz), LF Coil Driver (125 KHz) and MCU. The MCU contains an Analog-to-Digital Converter (ADC) which was used to demodulate the data from both the UHF receiver and the LF response from the key. The block diagram is shown in Figure 5.

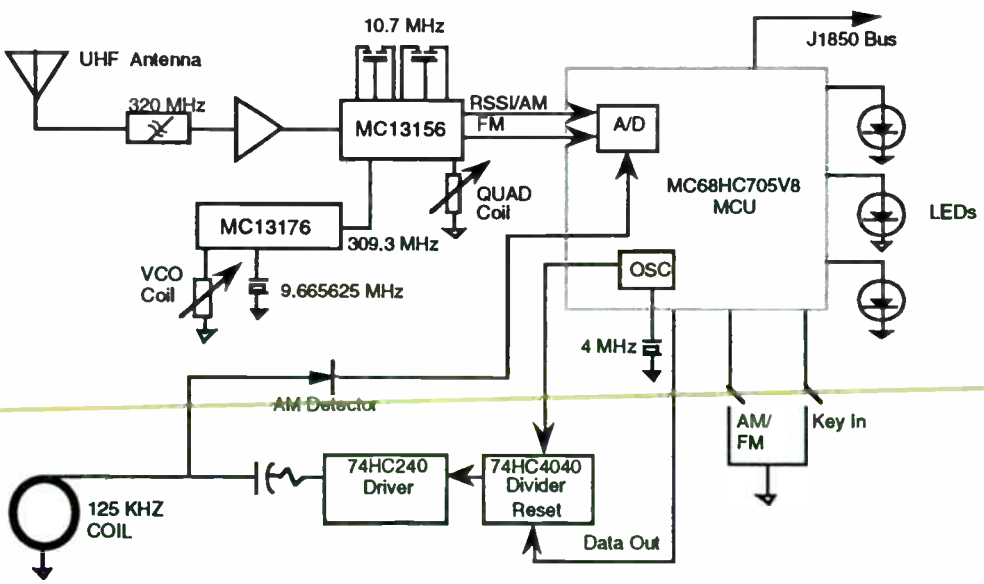

Figure 5. Automobile Breadboard Block Diagram

1. UHF Receiver

The UHF Receiver uses a helical front-end filter and a front-end amplifier to establish a reasonable noise figure. The front-end amplifier's signal is sent to the MC13156 receiver IC for filtering and demodulation. A low-side mixer Local Oscillator (LO) signal is provided by an MC13176 PLL. This IC uses a Colpitts crystal oscillator at 9.665625 Mhz and a Voltage Controlled Oscillator (VCO) tuned to 32 times this frequency (309.3 Mhz). The on-board fixed divide-by-32 and PLL phase-locks the output signal to the reference. AM output is provided by the Received Signal Strength Indicator (RSSI) signal available from the MC13156. This output is logarithmic and while no good for analog AM, provides the signal-present/signal-absent indication needed to demodulate OOK.

2. LF Coil Driver

The Low Frequency circuit derives it's frequency from the clock oscillator in the MCU. This 4 Mhz signal is divided by 32 using a 74HC4040 device. The signal is passed to a 74HC240 Buffer/Driver. All of the outputs of the IC (8) are connected in parallel and used to drive the coil. A series capacitor is used to resonate the coil and a series resistor reduces the circuit Q. The Field-Strength developed at the coil must be sufficient to power the key circuitry as well as communicate with it. The output is On-Off-Keyed by a reset signal applied to the divider by the MCU. A capacitor in the key stores enough energy to keep it's internal circuitry functioning between signal-on pulses. A simple diode detector is connected across the coil and it's output is sent to the MCU Analog inputs.

3. MCU

The MCU is an MC68HC705V8. This device is very popular in automotive applications. It has a Message Data Link Controller (MDLC) which conforms to the SAE J1850-Class B Data Communications Network Interface. This allows communications within a vehicle with other systems compatible with this standard. The MCU also contains an analog multiplexer and an 8 bit A-to-D converter. The MCU can select between UHF AM, UHF FM, or LF AM. When the key is in the ignition, only the LF AM signal is used. When it is not, either UHF AM or FM is used depending on which is desired.

B. Key Side Breadboard

The Key side breadboard was broken into two parts. The logic was built on a wire wrapped grid board. The RF portion was built on a small Printed Wire Board (PWB) with a key blade antenna. The two were interconnected with a ribbon cable.

A block diagram of the Key breadboard is shown in Figure 6. The XILINX XC4010 is loaded (following power-up) with a pattern stored in the EPROM. This pattern controls the internal interconnection of logic gates. Changes in the logic operation are made in a high-level behavioral description (Verilog-HDL), compiled by a silicon compiler (Synopsys) and burned into the EPROM.

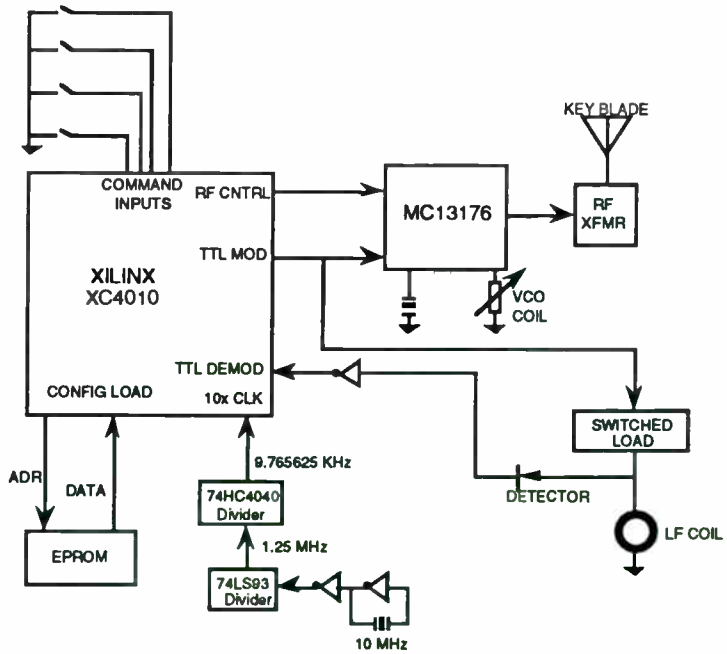

Figure 6. Key Side Breadboard Block Diagram

The clock for the logic and data I/O is derived from a 10 Mhz crystal using a logic oscillator. This is divided by 16 in the 74LS93 and then by 64 in the 74HC4040. The resulting frequency of 9.765625 KHz is 10 times the data rate.

The MC13176 IC uses an internal Colpitts oscillator and a crystal at 10 Mhz as a reference for a PLL. A VCO in the IC is phase-locked after going through a divide by 32 (inside the IC) resulting in an output of 320 Mhz. In the production key , a single resonator will be used for both the logic clock and the frequency reference. The breadboard used one for each sub-assembly. The LF coil, switched load, and detector are located on the key. The coil provides only communications on the breadboard.

VI. PACKAGING

A. Vehicle Side

The vehicle side will use conventional techniques for the main circuitry. The UHF antenna and LF Coil require special attention. The coil has to be around the ignition switch in order for the key to receive power and communicate with the vehicle-side of the system. This creates the opportunity to include both the UHF and LF circuits into the steering column. A dipole or loop type antenna can be integrated into the package for UHF reception and could result in a very good location for reception of the key signal.

The logic would be located in the body controller, engine controller or some other vehicle module area away from the steering column. By imbedding it in the vehicle's control modules, replacement of these modules by a would be thief could be made impractical. The response from the key could be sent to more than one controller preventing them from functioning without a valid key response. Since the key password would be set to each of the modules, simply overriding bus commands or driving simple logic levels on module's inputs would not work to bypass the system.

B. Key Side

The key side of the system has a significant size limitation. The intent is to fit all active and passive elements along with a battery into the head of the key. The use of chip-scale packaging techniques are most attractive in this area so as to end up with a reasonably sized key head. Furthermore, the packaging should be water-proof and able to survive trips through a clothes washer and dryer.

A vehicle owner's inability to start the car after getting the key wet would present a serious customer relations problem. The inclusion of a long life rechargeable battery (such as a re-chargeable Lithium Ion) allows the entire assembly to be molded as a single piece. The push-button switches could then be attached or, better yet, implemented with switches that could be imbedded in the molded package.

WIRELESS DATA SYSTEMS DESIGN

Wireless Data Systems Design

Session Chairperson: Ken Thompson,
Hewlett-Packard Co., Spokane Division (Liberty Lake, WA)

Digital Cordless Telephone For WLAN/Telephone/Videophone Service.
Harold Walker, Pegasus Data Systems, Inc. (Middlesex, NJ) 352

U-PCS Band Wireless PBX/LAN is ISDN and Multimedia Ready.
Bohdan Stryzak and **Harold Walker,** Pegasus Data Systems, Inc.
(Middlesex, NJ) 358

Wireless Data Communications. **Donald Burtis,** Pacific Communication
Sciences, Inc. (San Diego, CA) 362

New Capabilities in Digital Test Equipment for Wireless Products.
Michael Lauterbach, LeCroy Corp. (Chestnut Ridge, NY) 363

DS-SS High-Capacity (1.544-to-10-Mb/s) Power-Efficient Modem/Radio.
Andrew Denis, David Bayendor, and **Tony Defries,** IOTA, Inc.
(Berryville, VA) 370

Digital Cordless Telephone For WLAN/Telephone/Videophone Service

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562 Lincoln Blvd
Middlesex, N.J. 08846

ABSTRACT:

Data transmission at 320 Kb/s in the bandwidth allowed for 46/49 MHz cordless telephones makes it possible to provide H320 videoconferencing, two separate 2B+D channels, or 5 "B" channels over a cordless telephone/wireless link using the presently assigned band. Provision is made for analog or 2B+D service (U Interface) at 160 Kb/s to connect to the external telephone lines. Within the users facility, data can be transferred at 320 Kb/s for WLAN service, or for videoconferencing using the H320 standard. 2B+D video can also be used.

This paper will discuss only the radio portion of the link, as prototyped, assuming that all level conversions, protocols etc. are taken care of elsewhere and that normal CMOS level NRZ signals are available from the phone line equipment to the radio equipment.

VPSK modulation is used to compress the RF bandwidth 15.3/1 (15.3 bits/Hz). VPSK is a modified form of BPSK modulation that does not lose signal power as a result of compression. 15.3/1 compression is the equivalent of QAM 40,342 - which is impossible to achieve. The power and BER relationship is given in the Figure 8. VPSK modulation does not follow the powers of two rule applicable to QAM. See references.

FCC REGULATIONS:

FCC regulations for cordless telephone service in the 46/49 MHz bands allow 20 Khz of bandwidth using a crystal stability of 100 ppm. Crystal drift either way could thus result in a bandwidth of 30 Khz. The FCC allows for this by requiring any radiation +- 10 Khz outside the nominal 20 Khz center to be at least -26 dB below the peak value after allowing for crystal accuracy and frequency drift. Signal strength is limited to 10 millivolts per meter at 3 meters from the transmitter, which rules out the use of any other compression method..

By using crystal oscillators with a stability of better than 10 ppm and with VPSK 15.3 to 1 compression, the radiation can be confined to the permitted FCC limits while transmitting data at 320 Kb/s. 10VPSK encoding is used. Actually, 6VPSK with 10/1 compression would occupy 32 Khz at -26 dB, which would comply with a liberal interpretation of the rules. If 2B+D is used, compressing 10/1 uses only 16 Khz of bandwidth. VPSK can compress 7.4/1, 10/1, 12.6/1 or 15.3/1. Tests have been made at 18.6/1.

TRANSMITTER-ENCODING:

Figure 1 shows a block diagram of the VPSK encoder. A crystal oscillator with compensation to better than 10 ppm supplies a clock frequency to the data source, a modulation IF frequency to the balanced

BPSK modulator and a clock frequency to the synthesizer to select the channel.

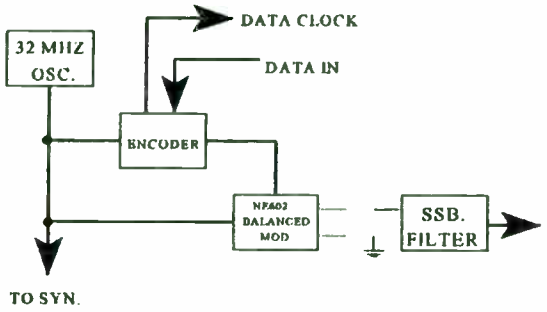

Figure 1. The Data Encoder and Modulator.

VPSK encoded data is end to end pulse width encoded prior to the BPSK modulator. In the case of 10VPSK, the bits supplied to the BPSK modulator are stretched 1/10 and 2/10 bit width. The Fourier frequencies resulting cover a band 1/15.3 the data rate, or 20.9 KHz. See the references for articles on VPSK modulation.

The upper sideband filter is a simple two pole LC filter followed by a locked oscillator to further narrow the bandwidth as shown in Fig. 2. The spectrum transmitted, which is -26 dB at the +-10 Khz points, is shown in Fig.3.

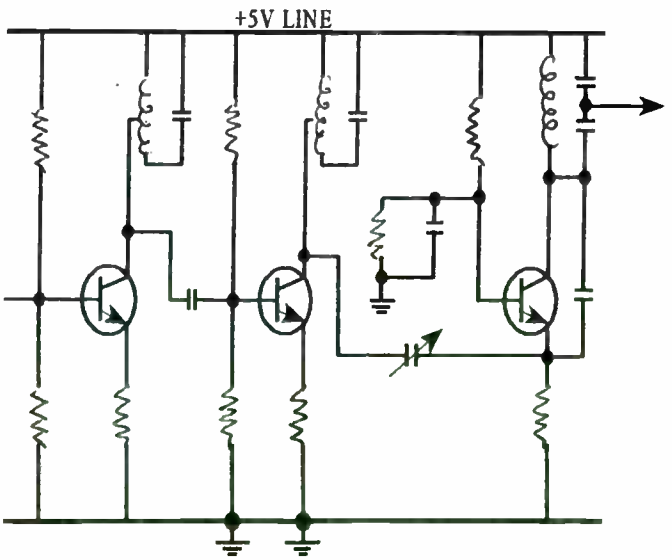

Figure 2. The Transmitter IF filter.

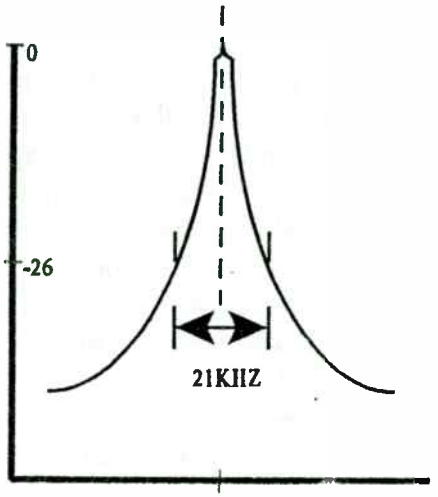

Figure 3. The Spectrum for 320 Kb/s Digital Modulation Using VPSK.

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The upper sideband of the modulated IF signal is mixed with a local oscillator signal to provide the 46 or 49 MHz output. A second locked oscillator at the mixer output passes only the desired signal, rejecting the two mixer input signals. This oscillator also drives the diplexer. Because of the strong drive signal to this oscillator, it comes under the regenerative IF amplifier category and is not to be considered a free running oscillator, which the FCC would not permit. Figure 4 shows the mixer and output amplifier along with the diplexer. See the references regarding Regenerative IF Amplifiers.

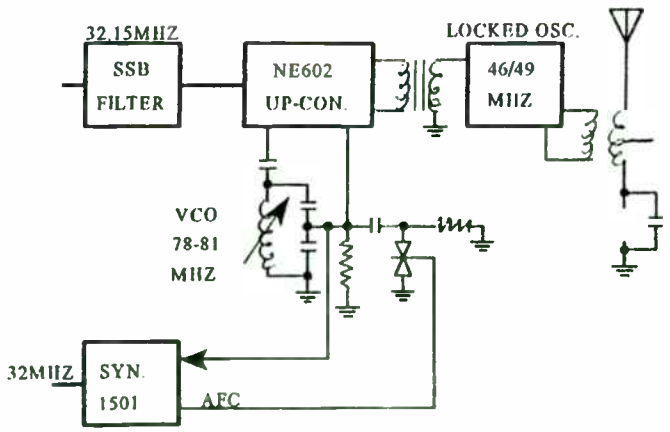


Figure 4. Mixer and Output Amplier.

DIPLEXING:

The diplexer is a typical Hybrid transformer circuit. If the antenna and the dummy load at the ends of the hybrid are balanced, the output to the receiver tap is a null at the transmitter frequency. Additional trapping can be used. This circuit requires a fixed antenna length shorter than 1/4 wavelength (36"). The antenna represents a resistive/capacitive load of approximately 1800 ohms and 10 pf of capacity, which is balanced by the dummy capacitor and ferrite bead to provide the null. The ferrite bead has a resistive component of 1800 ohms with little or no inductance at 49 MHz.

The oscillator output level is nearly +20 dBm. This must be padded down to comply with the power output regulations. The necessary reduction is accomplished by varying the coupling distance between the coils. 3 dB of power or more is lost in the hybrid.

RECEIVER-DECODING

Figure 5 shows the RF input circuit. Low noise FET amplifiers are used to raise the signal above the background noise of the following stages as much as possible to prevent additional losses in the mixer and IF amplifier.

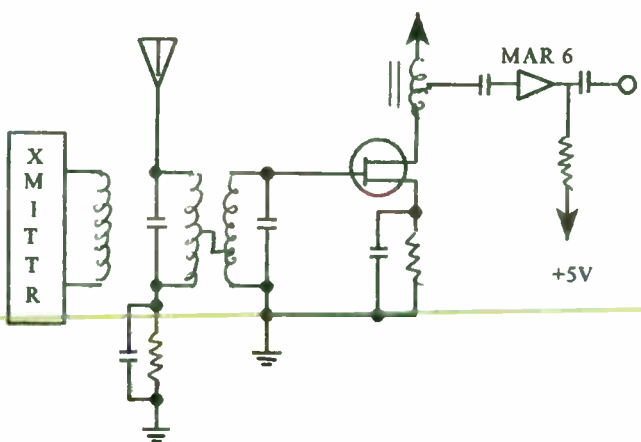


Figure 5. Receiver Input Circuit.

The resistive noise (background noise) is approximately -128 dBm for a bandwidth of 30 Khz. Assuming a receiver noise figure of 8 dB, a noise level of -120 dBm remains.The signal must be above this level by a sufficient margin to give an error free response. The theoretical signal to noise for 1 in 1 million BER for VPSK at all levels of compression is 7.4 dB, which is 3 dB better than QPSK. In practice, filter non linearity and detector uncertainty result in a value of 14-15 dB. Add to this the expected losses and input noise of the receiver and data should be recoverable at the -95/-100 dBm input level.

Substituting a signal generator for the antenna, with impedances matched, the measured input signal level required for 20 dB S/N was -85 dBm. Obviously the losses in the hybrid and the input NF were not as low as expected. The VPSK modulated signal was close to error free at -90 dBm.

The same two pole LC filter as used in the transmitter IF is used in the receiver, except that an NE605 limiter is used ahead of the locked oscillator. A interesting feature of the locked oscillator in this circuit is that it offers processing gain, typically more than 6 dB. The noise bandwidth of the locked oscillator is less than 10 Khz, while the tracking range is approximately 100 Khz. See the references for "Regenerative IF amplifiers"

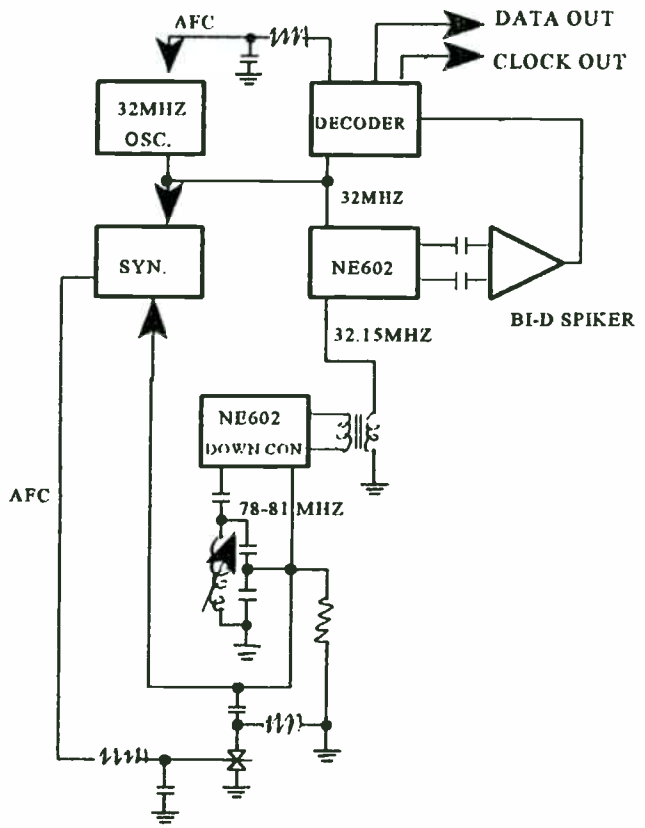


Figure 6. Receiver IF and VPSK Detector.

Figure 6 shows the receiving circuit following the down conversion. The 1X clock and the data are restored at the decoder output. VPSK modulation is single sideband FM with a coherent carrier reinsertion required. The AFC circuitry in the decoder chip makes it possible to lock the 100X oscillator exactly in phase and frequency with that of the originating transmitter.

BPSK modulation (and VPSK) can be detected as either AM or FM. The circuit used here is that of a SSB AM product detector with the reinserted carrier exactly the same as the transmitter carrier, which is eliminated or suppressed at the transmitter.

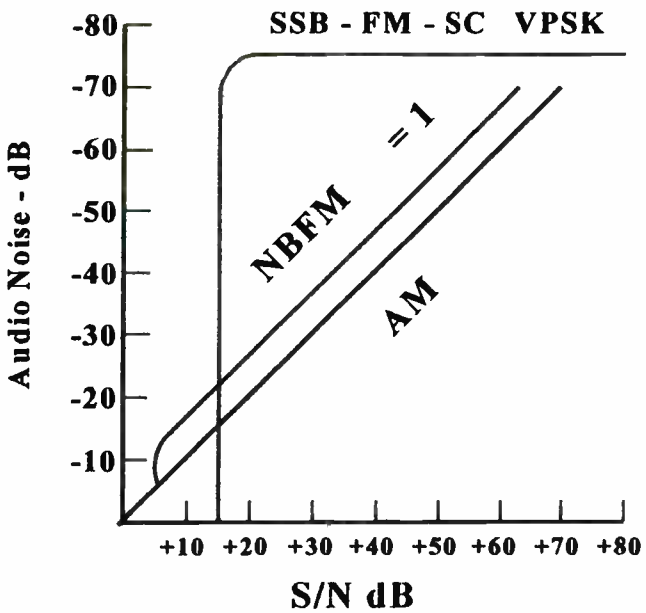
The output of the detector is a series of square waves of varying widths. A zero crossing detector is required to produce a spike at each zero crossing for use by the decoder chip. A Bidirectional one shot is used for this purpose.

QAM vs VPSK

The only other modulation method that can compress data more than 5 or 6 to one is QAM. To compress 10 to 1, QAM requires 35 dB Eb/n. 6VPSK compresses 10 to 1 with Eb/n values of 14-15 dB for the same BER. The reason for the difference is in Shannons' Limit. VPSK is BPSK modulation, with 1 bit per symbol, not 10 bits per symbol as would be required for 1024 QAM. Shannons' limit for VPSK is the same as that for BPSK - 0 dB. Shannons' Limit for 1024QAM is 20 dB. This is an immediate power gain improvement of 20 dB for VPSK. 1024QAM is not a reality at this time. VPSK as used here compresses 15.3/1, hence is the equivalent of 40,342 QAM, which is an impossibility. If it were possible, the Eb/n required would be 50 dB or more. See Figure 8. Add this to the input noise plus losses and the signal level required for 1 in 1 million BER would be greater than - 60 dBm, which is more than 30 times the signal level required for a cordless analog phone. The range of such an impossible system would obviously be less than 1/30 that of an analog phone.

VPSK on the other hand, has been demonstrated to offer better post detection signal to noise than analog FM at the same signal strength. Those unfamiliar with the concept will say this cannot be. You cannot compress without losing signal power. VPSK equipment in the field has repeatedly proven that you can compress with post detection S/N better than or comparable to analog FM.

Figure 7 showns the performance of a VPSK receiver using 10/1 compression, compared to analog FM using the same receiver, which could be operated in a dual mode.



Figiure 7. Performance of VPSK vs FM.

The measurements given here offer further proof. This Cordless Telephone prototype is being used to demonstrate VPSK at trade shows to convince the skeptical.

One thing should be obvious to all from the graph in the appendix, this equipment is operating well below Shannons' limit for the equivalent QAM, yet it does not violate Shannons' Limit. Shannons' limit rises as the number of bits/symbol rise. 1024 QAM uses 10 bits/symbol. VPSK is always 1 bit per symbol regardless of compression, hence has the same characteristics as other 1 bit/symbol methods (Unencoded BPSK). See References.

The frequency synthesizer method used is shown in the figures above, where it will be noted that the synthesizer clock and data clock are the same. The IF frequency from the modulation section of the transmitter and to the receiver detector is 32 MHz. This must be mixed to provide a signal at 46 or 49 MHz.

Since a frequency of 14 or 17 MHz cannot be used, (lower than the IF frequency) the local oscillator frequency is 32 plus 46/49, or 78/81 MHz. The synthesizer uses the 32 MHz as a reference and locks a VCO at 78/81 MHz as required.

This synthesizer has spurs and phase noise that would be unacceptable for FCC use on licensed frequencies, but which can be permitted under part 15.

The VCO is a part of the NE602 up or down converter, so a separate VCO is not required for the mixers.

Operating under Part 15 of the FCC regulations has many advantages and some disadvantages. The advantage is the need to suppress unwanted signals by only 26 dB, thus simplifying filtering. The disadvantage is the low power permitted, which limits range. In this narrow band service at 46/49 MHz, VPSK modulation offers the only acceptable means of passing a higher data rate within the allowed bandwidth and at satisfactory in office distances.

Figure 8 shows the Eb/n values required for 10-6 BER when using VPSK modulation for various degrees of compression. Unlike the other compression methods, the power required does not increase with compression. Various degrees of compression from 4/1 to 15.3/1 are shown.

Like all compression methods, the required power for VPSK rises with compression, but the decrease in bandwidth results in cancellation of the power increase. As a result, the required signal strength for VPSK stays the same regardless of the compression ratio.

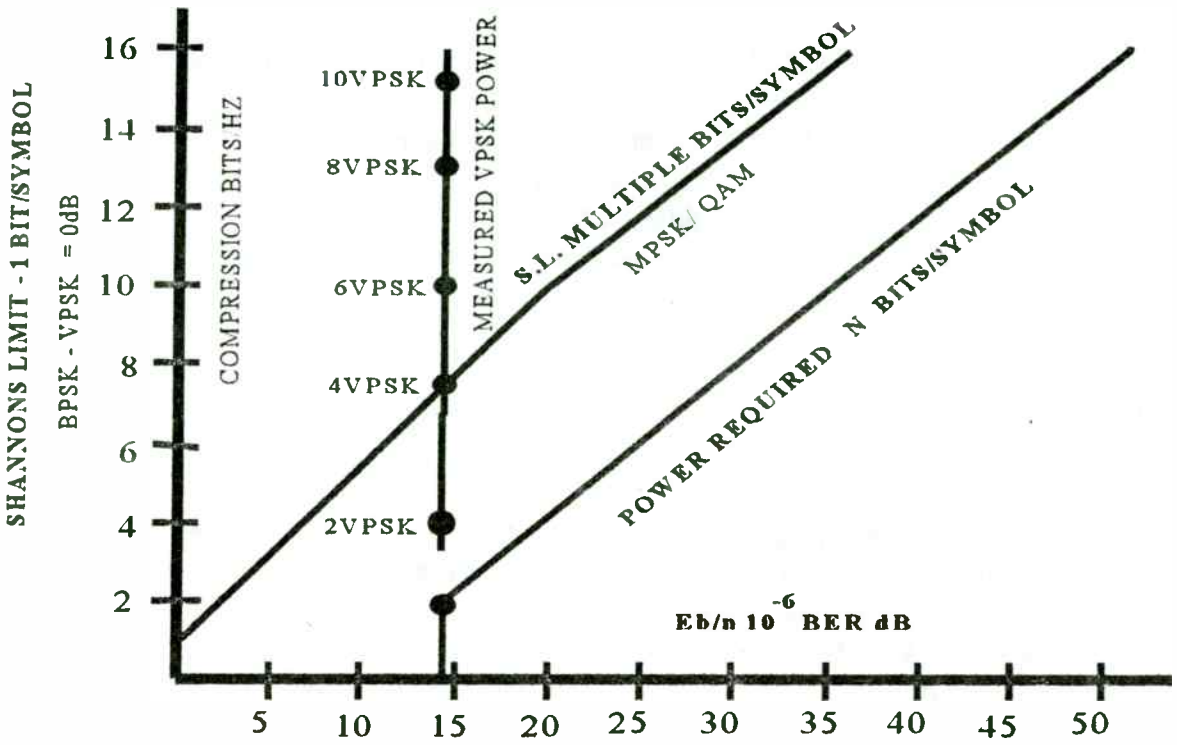


Figure 8. VPSK Eb/n for 10-6 BER.

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5. B. Stryzack and H.R. Walker " Improve Data Transmission Using Single Sideband FM with Suppressed Carrier", Microwaves and RF Magazine, Nov. 1994 (Wireless Systems Design Supplement)

6. H.R. Walker, "Regenerative IF Amplifiers Improve Noise Bandwidth". Microwaves and RF Magazine, Dec. 1995.

7. Kamilo Feher, " Understanding The Limits of Digital Cellular Formats" Microwaves and RF Magazine. July, 1995..

8. H.R. Walker, " The Advantages of VPSK Modulation", Transactions -IEEE Wescon, Communications Technology, Part 1., San Francisco, Cal., Nov. 1995.

9. B.Stryzak and H.R. Walker, " U-PCS Band Wireless PBX / LAN is Multimedia Ready" Fourth Wireless Symposium, Santa Clara Cal., Feb. 1996.

The author can be contacted at **908-356-9200**

U-PCS Band Wireless PBX/LAN is ISDN and Multimedia Ready

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908-356-9200

ABSTRACT:

The new Isosynchronous U-PCS band at 1900 MHZ makes it possible to provide Wireless ISDN service at T1 or E1 rates in a local area PBX/LAN connection (WLAN), or to provide ISDN telephone line connections to the outside world. In the user facility, the dial up connection can be used for LAN service at T1 or E1 rates between terminals , or for video conferencing. The S interface can be connected by switching to the telephone network where ISDN services (T1 or E1) are available. RF compression utilizing VPSK modulation that compresses to 10 bits per Hz without loss of signal power is employed to make the maximum use of the available RF spectrum. Channel widths of 200 Khz or less are used.

FCC Regulations:

The regulations for U-PCS service under part 15 of the Code are rather voluminous and will not be repeated here except in summary. For service in the Isosynchronous band (1920-1930 MHZ), the minimum allowed bandwidth is 50 Khz. Using VPSK modulation, this corresponds to a 500 Kb/s data rate. For lower data rates, the 900 MHZ or the 46/49 MHZ band should be considered. For T1 or E1, (160 and 200 Khz of bandwidth using 6 VPSK , or 100 Khz and 133 Khz of bandwidth using 10VPSK) the U-PCS band offers some promise. Actually, 10 Mb/s can be transmitted using 6VPSK in the 1.25 MHZ allowed for the Isosynchrous band maximum.

The conditions imposed by the regulations on channel switching, protocol and the allowed spectrum will probably result in this band being used only for wireless PBX service and not for wireless LANs in general where the 900 MHZ and 2400 MHZ bands are less restrictive.

This paper will not cover the data handling using T1 or E1, but only the prototyped RF transmission part. For testing, an Intraplex T1 audio digitizer was used to generate the T1 framed data chain that was transmitted. Data to and from the Intraplex equipment was by 4 wire S interface using HDB3 or AMI coding on the lines. This was converted to and from NRZ digital at both ends to interface the radio.

The encoder and decoder chips for VPSK radio operate with a clock frequency of 46.32 MHZ. This is doubled to 92.64 MHZ for the RF modulation. VPSK is single Sideband FM with the upper sideband at approximately 690 Khz above the carrier, or 93.33 MHZ. The clock oscillator and RF Modulator/Demodulator is shown in Fig. 1.

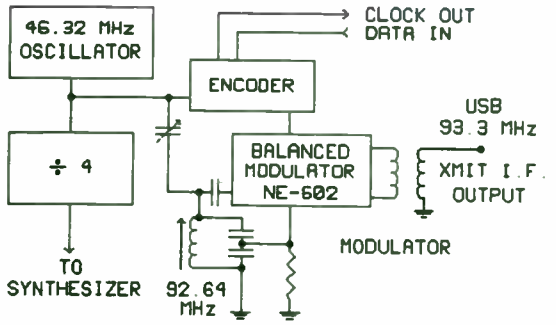

Figure 1. The Encoder and Modulator.

To obtain a signal which could be up converted and away from the 93 MHZ region, The scheme shown in Fig 2 Is used. The 46 MHZ clock has strong harmonics, enabling the first locked oscillator to lock at 138.96 MHZ. This is used as a first local oscillator frequency to mix the 93.33 MHZ signal up to 232.29 MHZ. The second locked oscillator at 232 MHZ removes any vestiges of the lower frequencies so that the requirements for spurious frequencies at the final output can be met.

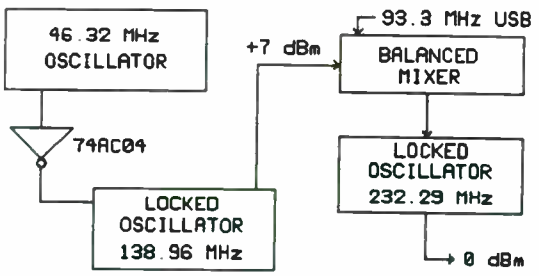

Figure 2. The First Mixer.

Locked oscillators are a throwback to early radio days, but they are very effective when used as regenerative IF filters. They are much narrower than ordinary LC or Helical filters. See References.

Figure 3 shows the up converter sequence. When used in reverse it becomes the down converter sequence. The synthesizer makes it possible to shift frequencies as required by the protocol.

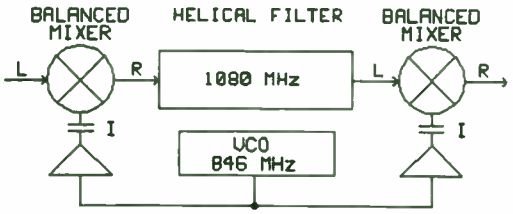

Figure 3. Up Conversion.

The up converter uses Minicircuits RMS30 mixers, which are passive and require 7 dBm of drive. Each has its own driver, a Minicircuits MAR4. The down converter uses Avantek IAM81008 active mixers to obtain some gain as will as to perform the mixing. The mixer drivers are not required.

Note that the mixers have the L.O. drive on the IF terminals, not the LO terminals. The maximum quoted IF frequency is 1 Ghz, but if the IF terminals are used as a signal input instead of an output, the LO and RF terminals maintain their upper limit freq. specification - although with slightly more loss than normal.

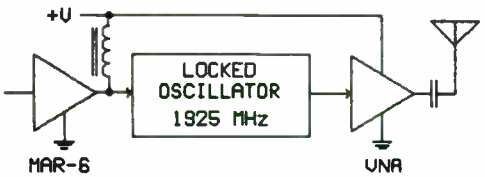

Figure 4. Output Circuit.

The transmitter output is a Minicircuits VNA driven by a locked oscillator operating at 1925 MHZ. The locked oscillator uses a ½ wavelength strip line resonator as its frequency determining element. This oscillator can be pulled approximately +- 20 MHZ by the drive signal at the emitter so that it does not require retuning to shift frequency within the 10 MHZ band.

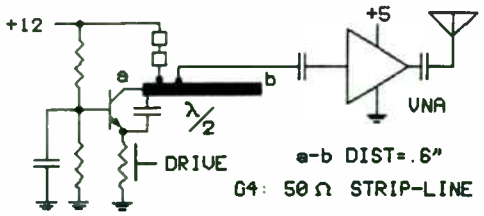

Figure 5. The Locked Oscillator.

The schematic of the locked oscillator is shown in Fig. 5. The mechanical details are shown in Figure 6.

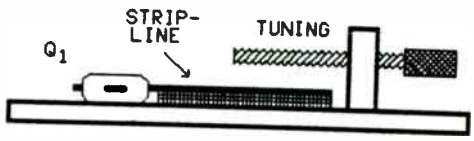

Figure 6. Locked Oscillator tuning.

The emitter resistor is a carbon film 1/8 W resistor that normally would not be used at these frequencies. It has an inductive component that helps with the oscillation feedback. The PC board below this resistor has a small plate that capacitively couples the drive or lock signal to the oscillator via this resistor.

Tuning to band center is by means of a screw that represents a section of coupled line that alters the equivalent LC of the resonant line. Initial tuning is by cutting the strip line to length.

The locked oscillator, which is really a Regenerative RF Amplifier, is an excellent substitute for a Helical or Coaxial resonator filter, which is not always available at the desired frequency. See references.

The down converter is the reverse of the up converter, using active mixers instead of passive mixers. The input is a MAR6 operated broadband, thus depending on the Helical filter and the IF filter that follows for bandwidth limiting (selectivity). The very short antenna used almost eliminates any concern about outside RF signals being picked up, and the low power used by other stations in the building will not cause any overload of the MAR6.

The receiver input is shown in figure 7.

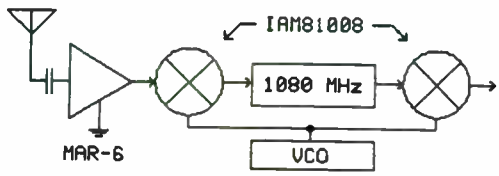

Figure 7. The Receiver Input.

Separate antennas are used with the receiver antenna being shielded from the transmit antenna to reduce pickup. Reflectors cannot be used legally to increase transmitter power, but they can be used to increase received signal level and to cancel or reduce the local transmitter signal level. A diplexer for a band this narrow at 1900 MHZ would be almost impossible to build, making full duplex operation difficult..

It is best to have the input and output MMICs right at the antenna base to avoid loss of power due to standing waves and the resulting mismatch in a cable.

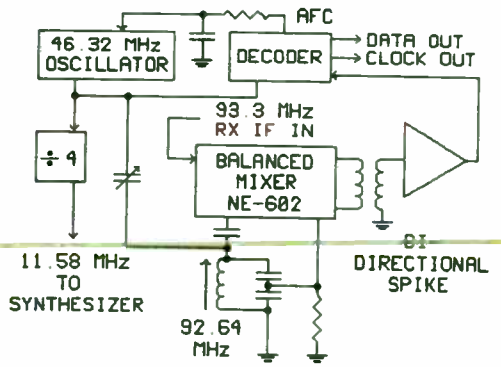

Figure 8. The Decoder Section.

The decoder section is shown in Fig. 8. The decoder chip has a built in AFC circuit to lock the receiver IF frequency to the transmitter frequency (coherent carrier reinsertion). This AFC circuit and the decoding circuits are dependent upon the received signal, which is detected as a sequence of square waves of varying widths. These square waves are then passed through a bidirectional one shot to obtain spikes that are used in the decoder for AFC and data decoding.

Figure 9 shows the S/N ratio required for VPSK modulation vs FM. FM offers no compression, but great simplicity. VPSK is more complex, but requires much less bandwidth. The most probable users of the U-PCS band will be Wireless PBXs. In an office with 25 -100 lines or more the amount of bandwidth available to each individual line will be limited, therefor the system designer cannot afford to waste it. VPSK modulation offers the most lines for a given spectral space.

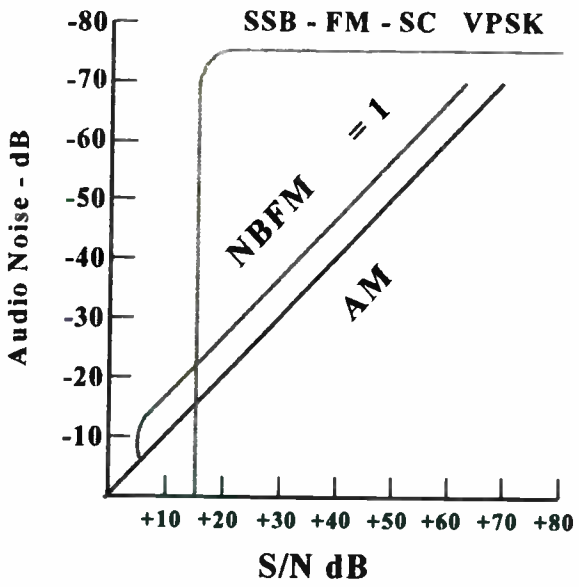

Figure 9. Performance of VPSK vs FM

Conclusions:

By using VPSK modulation, the maximum number of users in the U-PCS band can be accommodated. The modulation method is not complex compared to QAM and offers much better Eb/n values. The cost is much lower in comparison. VPSK is therefor the logical choice for a wireless PBX in the U-PCS band.

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Wireless Data Communications

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Currently, there exists an array of innovative, cost-effective wireless data communications technologies. This presentation discusses the future of wireless data communications, focusing on the availability and benefits of wireless data applications to the end-user. Existing wireless data applications and emerging Personal Communications Services (PCS), such as two-way messaging and telemetry, will be discussed:

- Evaluation and implementation of existing wireless data technologies and applications;
- How companies and mobile professionals can benefit from the use of wireless data technologies;
- Cellular Digital Packet Data (CDPD), the Japanese Personal Handyphone System (PHS), and time-division multiple access (TDMA) technologies.

New Capabilities in Digital Test Equipment for Wireless Products

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Abstract

There are new design and test tools for wireless circuits. Digital instruments have new memory capabilities, trigger features, measurement techniques, processing algorithms and documentation possibilities which can be extremely helpful in getting wireless products to market. Specific tools include automated measurement of worst case circuit performance, histograms for failure analysis and new troubleshooting tools for intermittent failures and signal dropouts.

I. New Memory Capabilities

A digital oscilloscope can be considered to consist of two sections. The front end consists of an amplifier, analog to digital converter and fast data acquisition memory. The rest of the instrument is a computer—including processor, processing RAM, math co-processor, display, floppy drive, serial/parallel ports and newer instruments

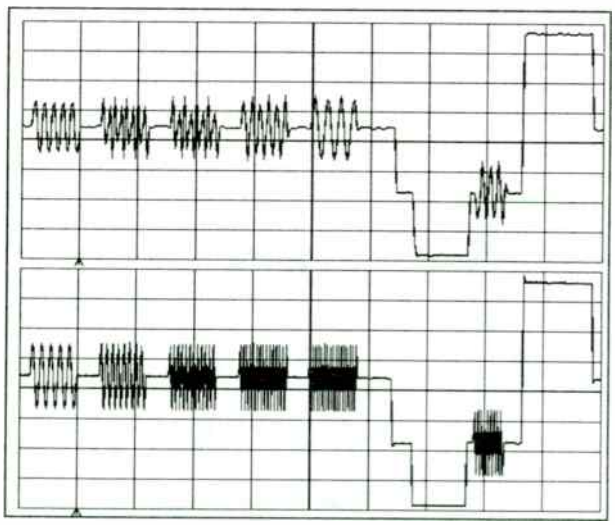

Figure 1. Zoom Details of a video signal captured first using 50k points of memory and then with 2M points

have PCMCIA type II and type III slots for IC memory cards and portable hard drives. The use of the data acquisition memory and processing RAM is key to productivity for the digital scope user. Data acquisition memory is used to capture the signal of interest. More bytes in the data acquisition memory translates to seeing finer signal details and better accuracy in both timing and amplitude.

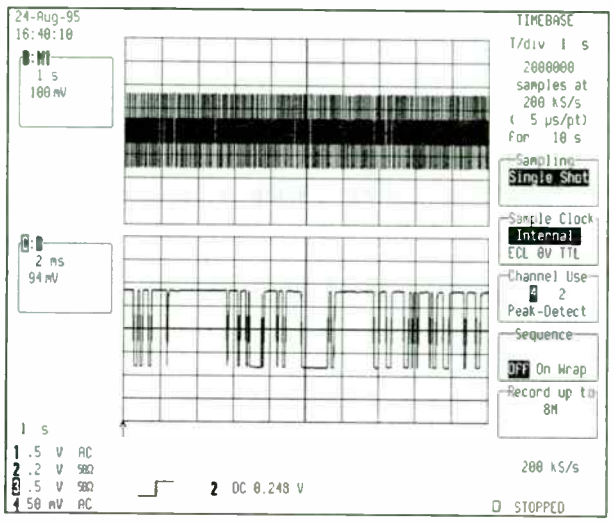

Figure 2a. Ten seconds of data from a pager is shown on the top trace. A zoom detail of 20 ms portion is on the bottom.

An example of a video signal is shown in Figure 1. A short data acquisition memory of only 50k bytes (upper trace) lacks the ability to characterize the signal adequately. A 2Mbyte memory (lower trace) performs much better. An example of applying long acquisition to obtain more accurate measurements in shown is Figure 2a, 2b and 2c. Ten seconds of data from a pager is captured into 2 Mbytes of acquisition memory. The data is then zoomed horizontally and vertically in order to isolate the tops of pulses. The noise on the top of the pulse can be analyzed for its peak to peak amplitude. The user can also measure the base and top of the noise to see if it is within tolerance. This type of measurement would not be possible using smaller memory with fewer data samples.

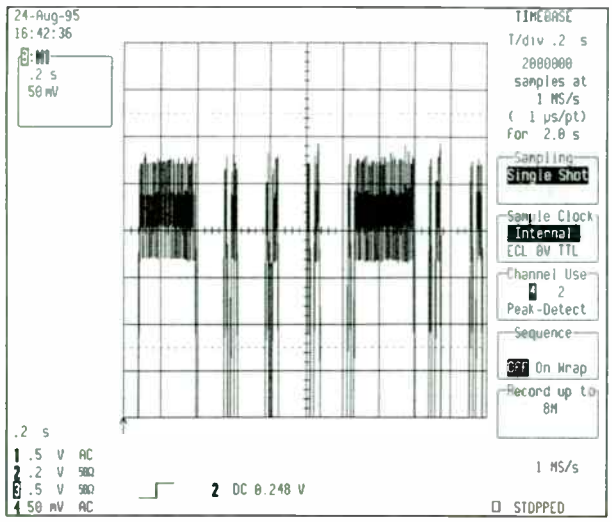

Figure 2b. Vertical and horizontal zooming of pager data reveals noise on the top of the pulses.

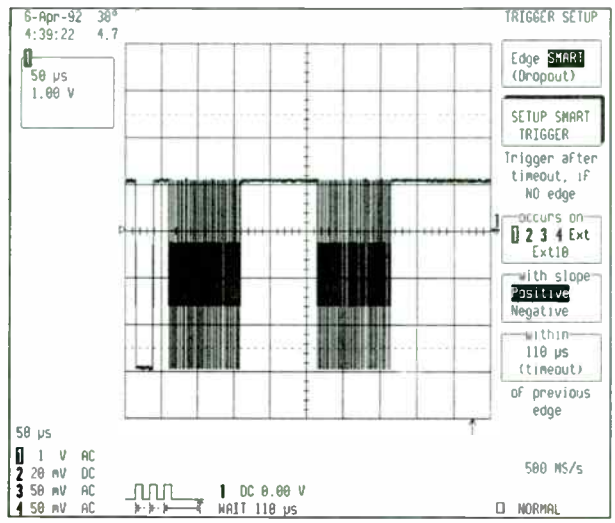

Figure 3. A DSO triggers on a "dropout". Note the scope is set to trigger if there is a gap of longer than 110 µsec. Two data packets occur, but when a network collision causes the third packet to disappear the scope triggers.

In general, the amount of signal time which can be captured by a digital oscilloscope, T_C, is:

$$T_C = \text{Sample Period} \times \text{Memory Length} \quad (1)$$

where "Sample Period" is the ADC's sampling period and "Memory Length" is the data acquisition memory.

A scope whose memory is too short will expand the time between samples in order to capture the amount of time set by the time per division knob. Moving the samples farther apart leads to loss of signal fidelity as previously shown in Figure 1. Current state of the art in digital oscilloscopes is 2 Mbytes of data acquisition memory on each of four channels which can be combined to 4 Mbytes on two channels or 8 Mbytes on one channel.

II. Triggering

The trigger in a digital scope is the user's way of telling the DSO that an event of interest has occurred. The scope will move the data from the acquisition memory to the processor for viewing, measurement and storage. There are many kinds of triggers available. Most high

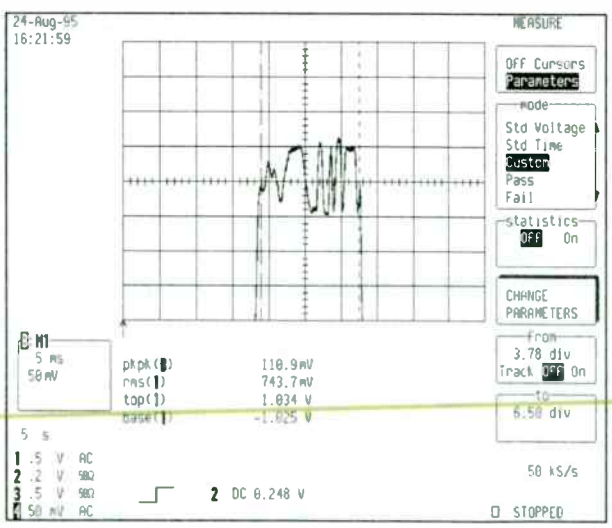

Figure 2c. The noise on a single pulse from the original ten seconds of data in Figure 2a is analyzed.

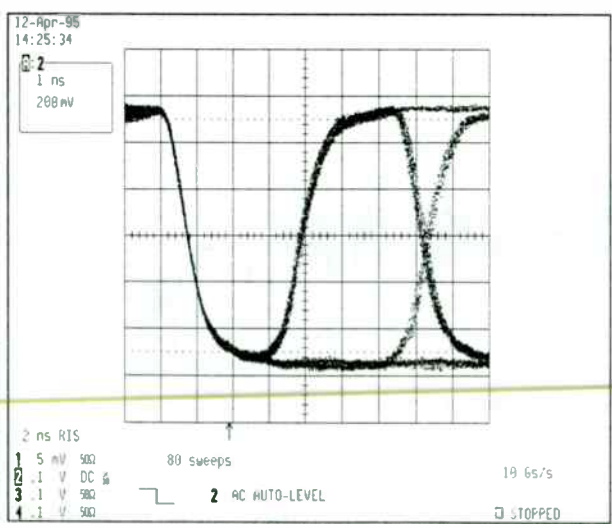

Figure 4a. Overlapping patterns due to the lack of adequate triggering.

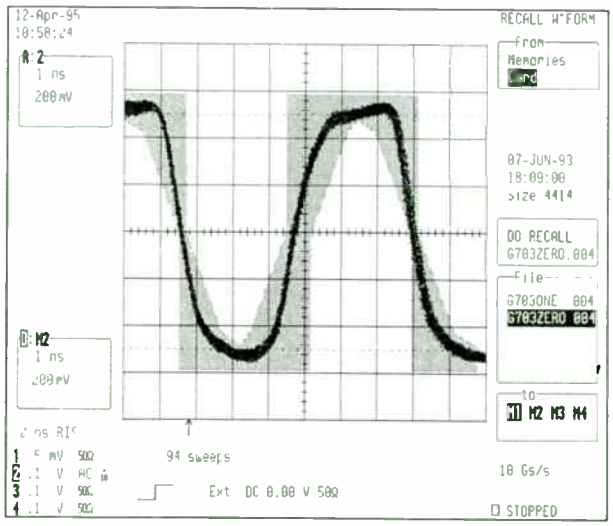

Figure 4b. Mask test of a binary 0. Notice the jitter at the trailing edge of the pulse.

performance digital scopes can trigger on signal edges, pulses widths, glitches, logic patterns of up to five inputs and other signal characteristics. One type of trigger useful for wireless design is called "Interval" trigger. This allows the user to specify the correct interval between two consecutive edges on a signal. If the interval becomes too long or too short the DSO can trigger. This is a good way to check for timing problems causing bit jitter. Another very important task for circuit designers is to track down problems causing data interruptions. This could be due to a packet collision, microprocessor hang-up, faulty connection or any other event that causes a signal to become quiescent when data should have been present. An example of a "Dropout" trigger finding a delayed data packet is shown in Figure 3. A trigger

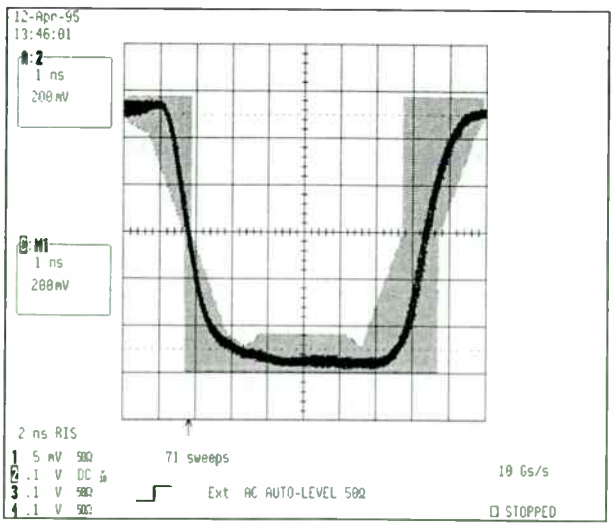

Figure 4c. Mask test of a binary 1.

enhancement for testing 155 Mbps SDH and SONET signals is shown in Figure 4a, 4b and 4c. Normally, engineers see a stream of 1's and 0's in persistence mode display as shown in Figure 4a. New triggering tools sensitive to serial data allow the user to capture just the 1's or just the 0's and compare them to standard test templates.

III. Data Analysis Techniques

Sometimes it is sufficient to view the data. An older style analog scope or a digital scope with long acquisition memory and dedicated hardware to maintain a fast display but little processing power can be used for these types of applications. All LeCroy scopes contain a (patented) hardware set which sorts the data in a long memory to find all minimums/maximums and display them quickly. This allows the user to acquire data sets megabytes in length and see short signal artifacts even if they are only one sample wide. If measurements of the data are required then the oscilloscope's processing power is important. A high speed processor, math co-

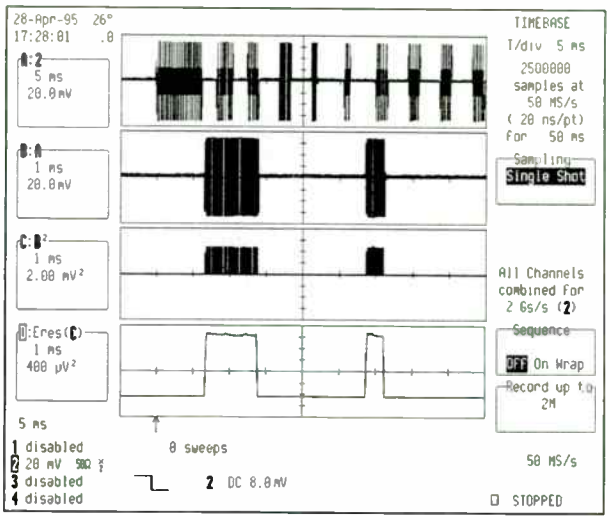

Figure 5a. The top trace is data from a automotive keyless entry system. Trace 2 is a zoom of the data and Trace 3 is a square of the zoom. The final Trace allows packets to be measured for proper width.

processor and adequate RAM are required. Current state of the art is use of a 32 MHz 68030 processor with 68882 co-processor and 64 Mbytes of RAM. An example of using long data acquisition memory coupled to strong processing is shown in Figures 5a and 5b. The signal shown is from a keyless entry system for an automobile. These systems operate using gated oscillators at 315 MHz in the USA and 434 MHz in Europe. Data is encoded by pulse width modulation. A wide pulse from the oscillator is a "1" and a narrow pulse is a "0". An

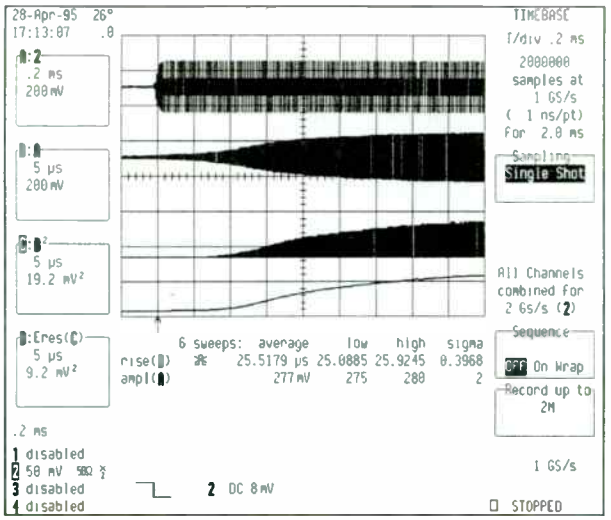

Figure 5b. Startup characteristics of an automotive keyless entry system are measured to verify FCC compliance. Risetime and amplitude must be verified.

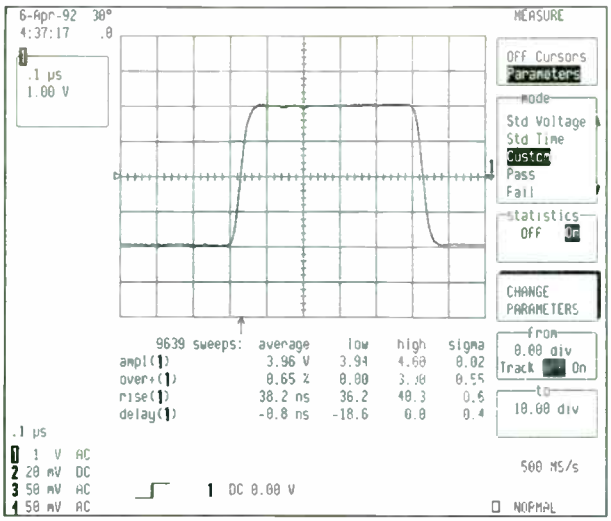

Figure 6. A DSO measures best and worst case shape of a data bit. In this case the maximum and minimum values are shown for pulse amplitude, positive overshoot, risetime and delay (timing jitter).

extra wide pulse is used as a "wake up" at the start of data. The pattern is repeated twice and lasts for a total of 500 msec. The top trace of Figure 5a shows 50 msec of data. The trace below it is a zoom detail of the beginning of the packet. Note the extra wide pulse at the beginning of data. In order to check that width of each oscillator packet is correct, the data is squared (in the third trace) and then filtered to eliminate high frequency components. The bottom trace allows the engineer to measure the widths of the oscillator packets and see the data content in an NRZ format. In addition to verifying the widths of data packets the designers of such systems must measure the ramp up characteristics of the oscillator as it is gated on. If the signal rises to quickly, the fast edge contains frequency components which are too high and run counter to FCC guidelines. Figure 5b shows the rising edge of a gated packet which has been zoomed, squared and filtered. At the bottom of the screen are measurements of the risetime and amplitude. Note that the average, lowest value and highest value of these parameters based on 6 sweeps of the oscilloscope are displayed. The DSO is using its processing power in two ways to help the user make this measurement:

A. It can daisy chain math functions (i.e. zoom the data, square the zoom and apply a digital filter to the square of the zoom).

B. It can remember worst case circuit performance.

Another example of analyzing worst case circuit performance is shown in Figure 6. Here 9,639 data bits have been captured and analyzed for amplitude, positive overshoot, risetime and jitter (delay compared to the trigger). Although all DSO's can measure standard pulse parameters, it is very useful to be able to have the scope monitor a signal and track worst case characteristics. A final example of combining the power of long acquisition memory with a strong processing engine is shown in Figure 7a and 7b. Spectrum analysis can be a very important tool for wireless design and it is one of the most popular options for digital oscilloscopes. The resolution of the FFT in a scope is proportional to the number of points analyzed by the FFT algorithm and to the

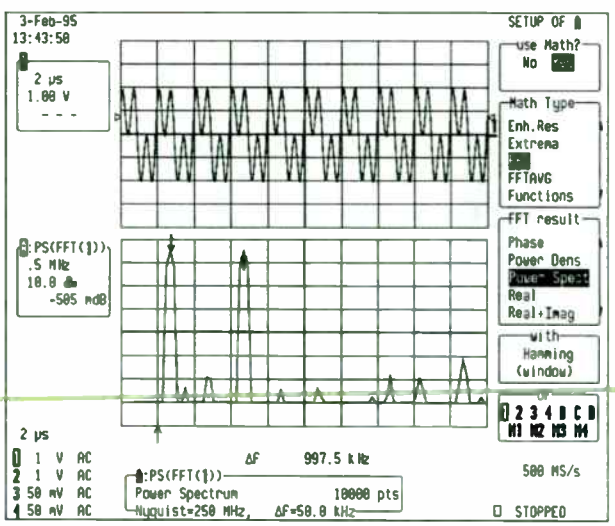

Figure 7a. An FFT of 10,000 points captured at 500 MS/s. Δf is 50kHz.

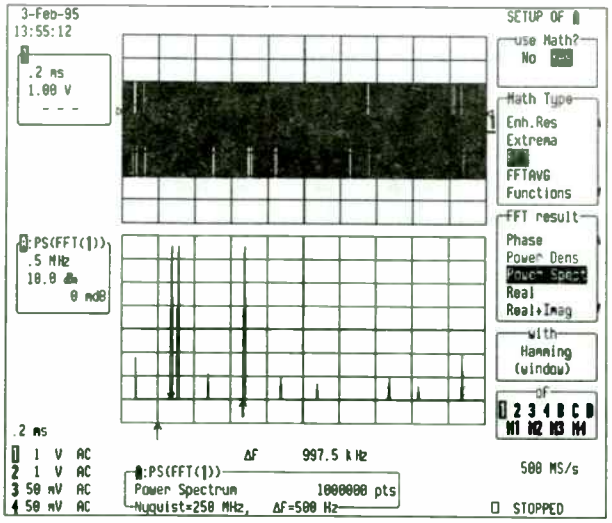

Figure 7b. An FFT of the same signal from Figure 7a with 1,000,000 points captured and analyzed. Now Δf is 500 Hz and the initial peak of Figure 7a is resolved into 2 peaks.

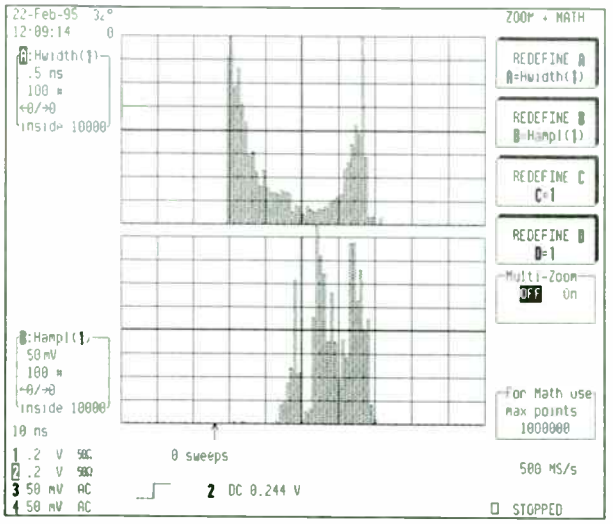

Figure 9. The pulse widths and amplitudes of a data stream are analyzed to verify performance is within specifications.

sampling rate at which those points were acquired. In general,

$$\Delta f = \frac{\text{sampling rate}}{\text{FFT length}} \qquad (2)$$

In this case long acquisition memory helps in two ways. It allows the scope to maintain a high sample rate over a long period of time and it allows the availability of more points to input into the FFT algorithm.

FFT computations can be optimized for speed or for usage of computational RAM. A typical algorithm optimized for speed can use 10 bytes of RAM for each byte of time domain data input. Thus, and FFT of 1 Mpoint of data requires 10 Mbytes of RAM. An FFT of 10 Kpoints of data would only need 100 Kbytes of RAM but it would have a resolution 100 times worse. Figure 7 shows the difference between a 1 Mpoint and 10 Kpoint FFT. Note that the presence of long data acquisition memory is not by itself sufficient to achieve good performance. There are some scopes on the market that can acquire 500 Kpoints of data but are limited to using 10 Kpoints in the FFT. The result is very poor performance in the frequency domain.

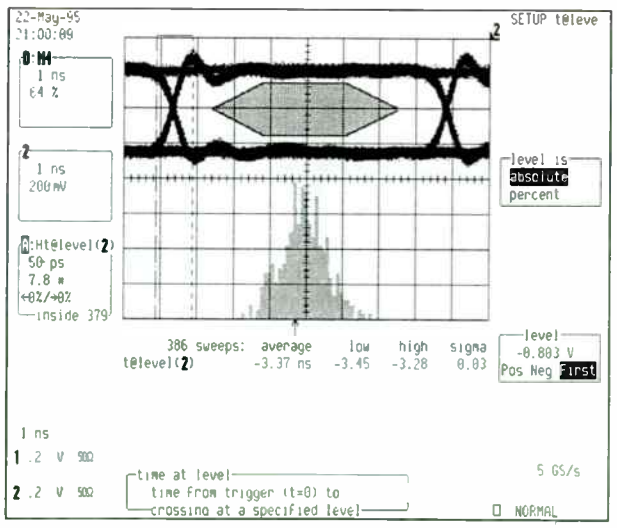

Figure 8.

Eye patterns are a traditional way of viewing communication signals. Figure 8 shows an eye pattern along with a histogram which allows numerical measurement of signal jitter. Histograms can also be useful for verifying signal quality or monitoring signal drift. Up to four simultaneous histograms can be displayed. Figure 9 shows the results of monitoring the stability of pulse amplitudes and pulse widths in a signal.

IV. Capturing Intermittents

Intermittent faults are the most time consuming for either design engineers or manufacturing to troubleshoot. Also, they have a chance of being missed and passed on to the customer. If the shape of an intermittent fault is not known the scope user has difficulty in selecting among the available trigger types to choose the one which will trigger on the fault. A traditional method to look for intermittent signal aberrations is to use persis-

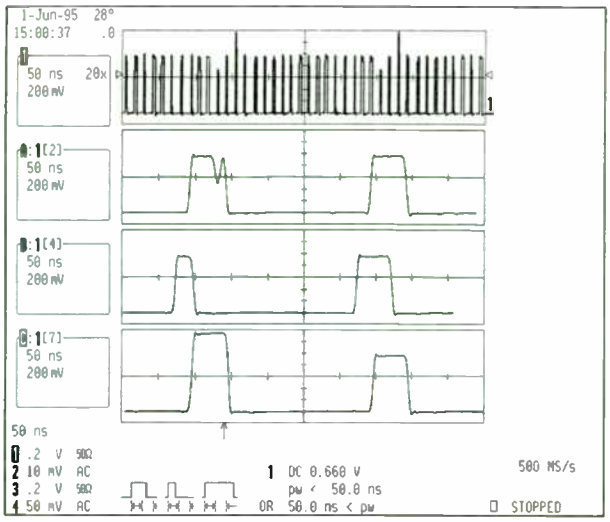

Figure 10. The compacted display of 20 events is on the top trace. On the other traces the zoomed detail of the 2nd, 4th and 7th event are shown.

tence display. Many signal acquisitions are displayed on the screen and the user looks for deviations from the normal shape. LeCroy's 7200 series and some scopes from other vendors offer color graded persistence. In this method the most common signal shapes are red and least common are violet. Signals with medium probabilities occupy spectral colors between red and violet. A year ago one vendor introduced a new chip set that could acquire a color graded persistence display faster through rapid triggering but with the weakness that all data acquisitions were limited to 500 points. Unfortunately, many real world signals cannot be adequately described by 500 points. A new tool called "Exclusion Trigger" was introduced late in 1995. It is intended for protocols where data bits should have a standard width or period. The scope can be set to exclude triggering on the normal signal and only trigger on aberrations. Previous methods of triggering a DSO or analog scope only allowed the scope to be actively monitoring a signal less than 25% of the time. The rest of the time was deadtime between triggers during which the scope was rearming itself and getting ready for the next trace. Exclusion Trigger avoids triggering the scope on signal shapes which have no useful information (the normal shape) thereby allowing the scope to monitor the signal 100% of the time until an intermittent aberration occurs. The faulty signal is captured, displayed, its properties can be measured by cursors/FFT/advanced math and it can be saved. A sequence of faulty signals can be captured and stored for comparison or for histogram analysis which reveals which failure modes are most common. The time of each failure and the time between failures can also be recorded. This gives the engineer more troubleshooting tools than previously available for solving intermittent problems and also provides a better way of proving that such problems have been solved. Suppose an intermittent fault occurs once per hour. In the traditional method, the user might watch the scope for 4 fours and see the fault once (since the scope has 25% active time). On a color graded persistence display he might have 10 seconds to stop the scope to save that one failure on the screen. But using Exclusion Trigger, the engineer can walk away from the scope and come back 4 hours later to find that all four faults have been captured and stored for view/analysis. Figure 10 shows an example where 20 intermittent faulty pulses were captured.

V. Documenting Results

Most DSO's offer a floppy drive for saving data. Newer scopes offer fast internal graphics printers, slots for SRAM memory cards (PCMCIA type II devices) and portable hard drives (PCMCIA type III). The memory cards and hard drives are much faster than the floppy. In manufacturing test the memory card has the greatest speed advantage for recalling test templates and oscilloscope setups. It can also contain stored "golden" waveforms which can be compared to the device under test. The hard drive is also much faster than a floppy but its key difference lies in the amount of data that can be saved. PCMCIA portable hard drives of 270 Mbytes are available. In storing data from a DSO that has 2 Mbytes of data per channel the 1.44 Mbyte floppy is inadequate. Even for scopes with only 500 Kpoints of data it is cumbersome to store data onto floppies.

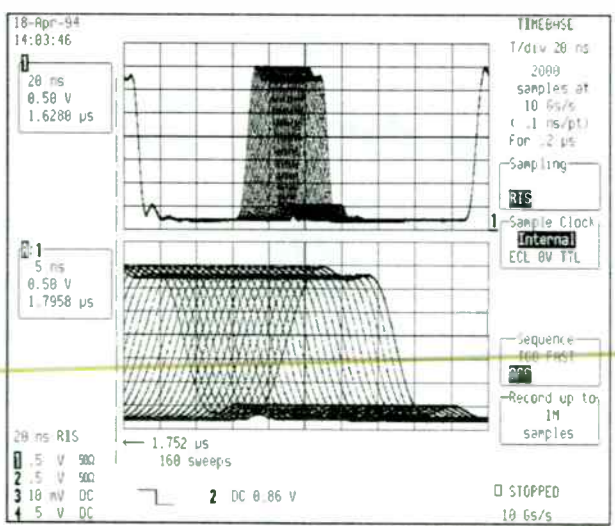

Figure 11. Bit jitter simulated by an AWG.

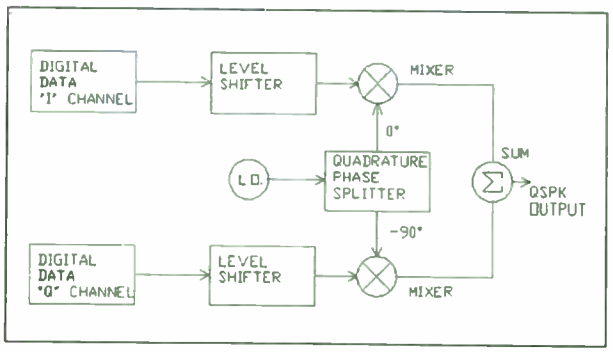

Figure 12. Block diagram of Quadrature Signal Generation.

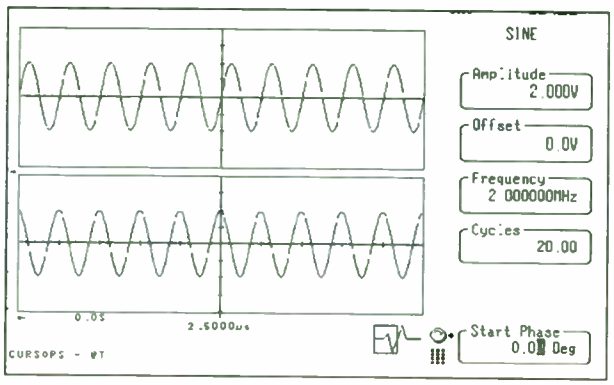

Figure 13. Phase control in an AWG.

VI. Using Digital Instruments to Generate Test Signals

Arbitrary Waveform Generators (AWG's) can be very useful instruments at both the design and manufacturing stage of wireless products. The effects of bit jitter in either amplitude or time can be easily simulated. Figure 11 shows one bit in a data stream being moved relative to the others to test the robustness of a design against timing jitter. Pulse edges or larger pieces of a waveform can be moved in 100 psec increments by simply turning

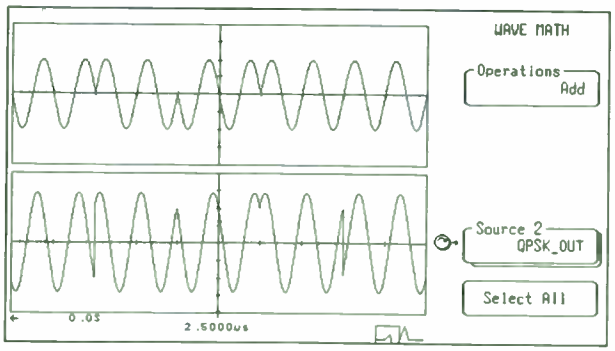

Figure 14. QPSK signal from an AWG.

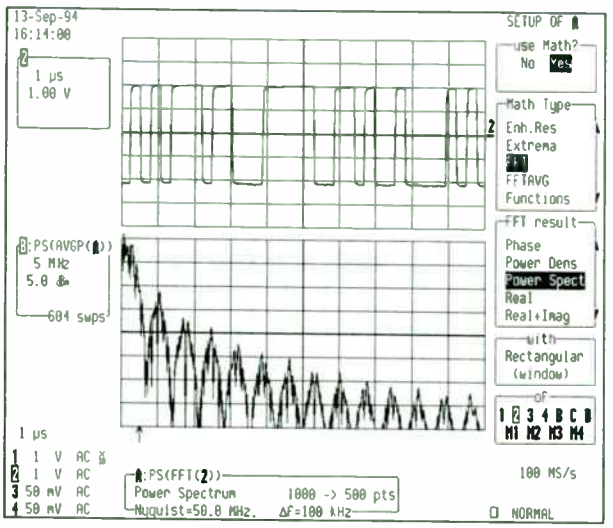

Figure 15. The top portion shows an AWG output of a spread spectrum communications "chipping" sequence. The lower portion shows a frequency analysis of the signal.

a knob on the AWG. Another practical example of the use of an AWG for wireless design comes in quadrature signal generation. Figure 12 shows a block diagram of the circuit which will be simulated. "I" and "Q" data can be created and their phase shift controlled in 0.01° increments as shown in Figure 13. Binary Phase Shift Keyed (BPSK) waveforms can be added to create the QPSK waveform shown in Figure 14.

A final example of the use of AWG's is shown in Figure 15. Here, the AWG is creating a data sequence and simultaneous encoding sequence for the data from a spread spectrum home security system. Because the AWG has two channels driven by the same timebase the data and the "chipping" sequence which encodes it can be kept exactly in time. The two signals are mixed together to produce the final output which can be used to test the receiver. The spreading sequence, and its spectral analysis are shown in Figure 15.

VII. Conclusion

The new tools available in digital instruments can be of considerable help in getting new products to market. New features can also help troubleshoot problems at the manufacturing test stage or to document proper performance. There are significant differences in basic features available in instruments so the best advice is to consult several vendors and try a "test drive" before investing in a new instrument.

DS-SS High-Capacity (1.544 Mb/s to 10 Mb/s)

Power-Efficient Modem/Radio

Andrew Denis ***David Bayendor*** ***Tony Defries***

IOTA, Inc.

Berryville, VA 22611

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New direct sequence spread spectrum (DS-SS) architectures and system developments for FCC-15 high-capacity and power-efficient RF component solutions are described. To attain robust performance, including significant link margins for distances in the 50km to 80km range, the chosen transceiver design has to transmit maximal power within the regulatory limits and provide robust bit-error-rate (BER) performance in an interference polluted environment.

Research by IOTA led to the development of nonlinearly amplified (C-class) 2.4 GHz and 5.7 GHz spread spectrum architectures which use integrated patented FQPSK modulation RF amplification techniques. To maximize the capacity in the authorized ISM bands by DS-SS access methods, it is essential that the combined modulation and radio subsystems be bandlimited, that is spectrally efficient, and simultaneously RF power/DC power efficient. The combination of powerful baseband direct sequence processors and of integrated IF and RF components led to a spread spectrum design which outperforms in power efficiency conventional DQPSK standardized spread spectrum systems by 400% and has a BER performance which is 7 dB more robust that that of alternative GFSK-based Frequency Hopped spread spectrum systems.

System design parameters, architectures and experimental results are presented. The synergistic advantage of power and spectral efficiency combined with robust BER performance maximizes the capacity of interference and noise limited systems. The first generation of products is for 1.544 Mb/s applications and the same architectures could be applied for higher bit rates in the 6 Mb/s to 10 Mb/s range.

SATELLITE COMMUNICATIONS AND TELEMETRY

Satellite Communications and Telemetry

Session Chairperson: David Sprague,
InMark—The Independent Marketing Group (Walnut Creek, CA)

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Economic and Performance Advantages of a Digital, Ready-to-Use VSAT Receiver Board Assembly

by James D. McVey
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Very small aperture terminal (VSAT) satellite networks are extremely popular for transmitting information in applications including digitized audio, data, and video broadcast networks. While the small size of the VSAT antenna dish is an important advantage, it also creates challenges for VSAT system designers. The antenna's low gain requires a high-performance binary phase-shift keying (BPSK) or quaternary phase-shift keying (QPSK) demodulator, with forward error correction (FEC). This paper will describe how Stanford Telecom's STEL–9236A line of products provides system designers a ready-to-use, digital PSK satellite receiver that not only provides the performance and reliability of digital technology, but also helps reduce the engineering expense required to develop satellite systems.

I. Receiver Block is Key Element in VSAT System Design

No matter what the VSAT application may be — MPEG video, digitally compressed music, rural telephony, or stock market data — the receiver block is a common element in all satellite systems. Unless systems integrators require so many nodes that it pays to retain the engineering expertise needed to develop and manufacture a custom receiver, it makes economic sense to incorporate a standard, ready-to-use receiver that is already being produced in high volume.

A primary attraction of current VSAT technology is the small size of the antenna. This is because the antenna and mount are less expensive than earlier systems, and the cost of installing them is lower. For example, the antenna is easier to lift into position and presents less wind-loading, therefore requiring fewer structural modifications to the mounting location. In addition, its reduced visual cross-section often results in fewer regulatory issues having to do with building codes and architectural limitations.

The penalty for the small antenna is reduced gain which — for any given data rate, modulation, and coding technique — requires a corresponding increase in satellite power. Thus, systems designers always have to consider the trade-off of one-time costs versus recurring costs. One-time costs include providing and installing the antenna and receiver. The recurring, "space segment" cost is tallied in terms of satellite power and bandwidth. However, this recurring cost can be reduced by incorporating more sophisticated receivers that use efficient modulation and FEC techniques.

In the past, the cost differential between a less power-efficient FM^2 receiver and a sophisticated BPSK or QPSK receiver with Viterbi decoder was quite significant. Now the cost of a digitally implemented BPSK or QPSK Single Channel Per Carrier (SCPC) receiver is on a par with an FM^2 receiver, so the economic trade-offs need to be reevaluated. Lower one-time and recurring VSAT costs allow operators to field systems that meet the price expectations of an expanded customer pool. Also, since the cost of the space segment is reduced, it is practical to implement networks with smaller numbers of nodes focused on niche markets. These factors are all accelerating a move toward PSK receivers.

II. Stanford Telecom's Digital STEL–9236A

The STEL–9236A from Stanford Telecom is a ready-to-use, board-level digital receiver assembly that provides BPSK or QPSK demodulation for ranges of data rates from 19.2 to 2048 kbps. Reduced phase noise in the STEL–9236A makes possible QPSK demodulation at data rates as low as 64 kbps. Bit error rate (BER) performance is typically within 0.4 dB of theoretical. The receiver includes onboard K=7, Rate 1/2 Viterbi forward error correction. The STEL–9236A accepts a 950 to 1450 MHz signal from a Low Noise Blockconverter (LNB) and gives HCMOS-compatible serial data and clock signals as outputs. It also can be provided without a downconverter for direct 70 MHz IF (intermediate frequency) input. (Figure 1) The assembly is a low profile configuration measuring, 6.0 in. x 4.0 in. x 1.45 in. (152 mm x 102 mm x 37 mm) with the tuner assembly mounted flat on the back side of the receiver board.

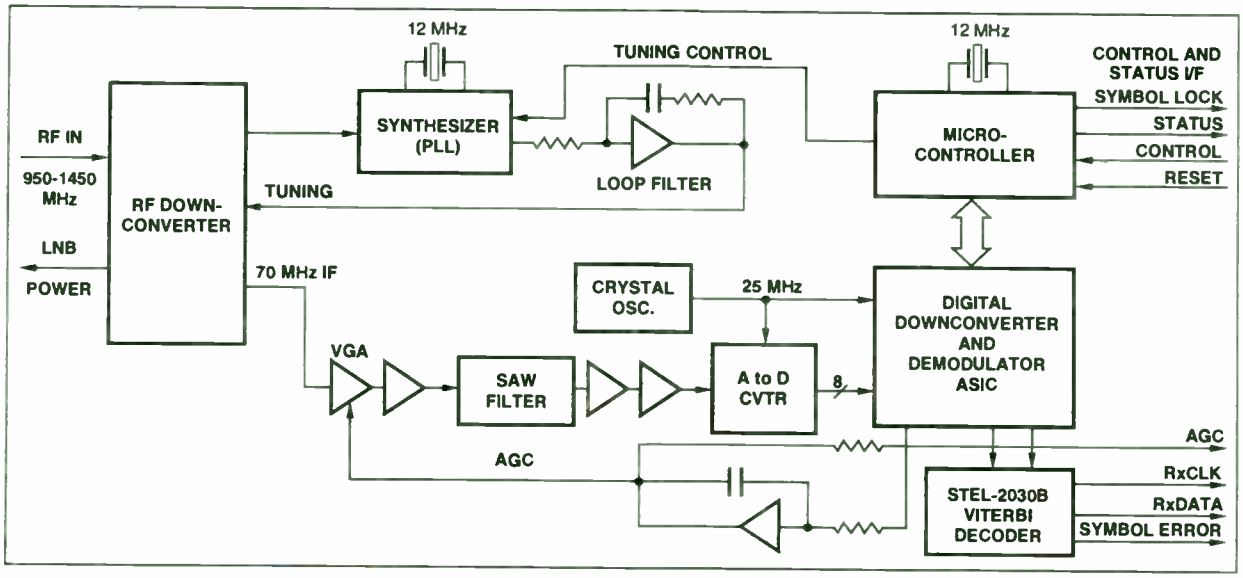

Figure 1. Stanford Telecom STEL–9236A Block Diagram

III. Advantages of IF Analog to Digital Conversion and Demodulation

Performing demodulation with digital technology gives a number of advantages: no adjustments, repeatable performance, no drift, small size, low part-count, low power consumption, and high reliability. In fact, the STEL–9236A uses only one analog phase-lock loop, which controls the L-band tuner voltage-controlled oscillator. Stanford Telecom has optimized the performance of this analog circuit for reduced phase noise and microphonic sensitivity. Carrier-recovery and symbol-timing phase-lock loops are fully digital, and thus fully programmable. Their digital implementation also eliminates the need for any screwdriver adjustments during assembly.

The receiver's digital technology improves system performance by eliminating two sources of error common to analog downconversion: quadrature error and DC offset. Quadrature error occurs in analog systems when the local oscillator signal is split into two parts that are not precisely 90° apart. In analog circuits, the split will never be precisely 90°. However, in the STEL–9236A the local oscillator is a digital circuit (the numerically controlled oscillator, or NCO) that generates sine and cosine values mathematically, so they are exactly 90° apart. The sine and cosine values always are in perfect quadrature for all frequencies. This is significant for QPSK since it ensures that the BER will be the same for all lock states even if the transmitter has imperfect quadrature. Another disadvantage of analog implementations is that analog circuits can produce DC offsets resulting in the signal not being centered around the DC voltage "decision threshold" — this translates into degraded system's BER. The STEL–9236A, on the other hand, contains digital multipliers with no DC offsets.

IV. Signal Processing for High Performance

Signal processing in the STEL–9236A begins with a synthesizer-controlled RF downconverter that tunes the desired signal to a 70 MHz intermediate frequency and reduces the system bandwidth to about 30 MHz. The IF signal is amplified and bandpass-filtered with a surface acoustic wave (SAW) filter that further reduces signal bandwidth. The SAW bandwidth required is related to the symbol rate and is chosen to minimize adjacent channel interference and yet avoid intersymbol interference (ISI) caused by amplitude and phase distortions [1]. After filtering, the IF signal is amplified and then sampled and digitized with a single analog-to-digital converter (ADC). The sampling rate is 25 MHz. This sub-samples the 70 MHz carrier but over-samples the modulation bandwidth. The 70 MHz IF is essentially mixed with the third harmonic of 25 MHz (3×25 MHz = 75 MHz) to give a 5 MHz digital waveform. The digitized signal is fed into the Stanford Telecom ASIC (application-specific integrated circuit) that serves as the digital demodulator .

A numerically controlled oscillator in the ASIC produces quadrature (sine and cosine) values

corresponding to a nominal 5 MHz frequency. The exact frequency is controlled by the carrier recovery loop. The digitized input signal is multiplied by sine and cosine values to yield I and Q channel products. These product terms are filtered with digital integrate-and-dump filters which, in turn, produce baseband I and Q signals.

The baseband signals branch into two control paths and one output path. One control branch is fed to a symbol timing discriminator. The discriminator is the starting point for a second order phase-lock loop (PLL). The PLL controls an NCO that is used to produce the dump clock for the integrate-and-dump filters. Since the recovered symbol timing is dependent on data transitions, data streams with long runs of 1's or 0's need to be "whitened" or scrambled at the modulator. The STEL–9236A demodulator includes a selectable V.35 descrambler.

The second control branch feeds the carrier tracking discriminator. This discriminator can be set to function as a frequency discriminator or as a phase discriminator. The frequency discriminator provides wide capture range and so is used in AFC mode for rapid acquisition of the signal. The phase discriminator is used in PLL mode to allow coherent demodulation for optimum BER.

The output of the Stanford Telecom digital demodulator ASIC is three-bit soft decision I (and, for QPSK, Q) data. These values are fed to the Stanford Telecom STEL–2030B Viterbi decoder, which operates at rate 1/2 with a constraint length (K) of 7, using the industry standard polynomials G1 = 171_8 and G2 = 133_8. The Viterbi decoder automatically resolves the time ambiguity in BPSK and two of the four phase ambiguities in QPSK. The remaining ambiguities effect the polarity of the data bit-stream; a selectable differential decoder can be enabled if desired.

The STEL–9236A can be externally programmed on a PC via a two-wire asynchronous (RS–232-like) port. This feature makes it possible to control center frequency, set acquisition sweep width, and turn the differential decoder and V.35 descrambler on and off. Operational status can be read back. In addition to these simple functions, the asynchronous port can also control more esoteric parameters like carrier and symbol timing recovery loop bandwidths.

These loop parameters can be adjusted from the nominal settings to optimize total system performance for actual phase noise and timing jitter in the complete system. In the case of the carrier loop, there is a trade-off between a wide carrier-loop bandwidth that is superior for tracking out system phase noise and a narrow carrier-loop bandwidth that is superior for rejecting additive white Gaussian noise (AWGN). For any given phase noise and AWGN situation, there is a carrier-loop bandwidth that will give optimum bit error rate (BER) performance [2]. In this way, an economic trade-off on LNB cost and phase noise performance can be accommodated with minimum impact on BER or space segment cost.

The port can also be used to download complete parameter sets (a parameter set consists of a 33-byte string of values) for different data rates and modulations. This allows the STEL–9236A to function as a multi-rate demodulator that can be used instead of a more expensive variable-rate demodulator for many applications.

V. STEL–9236A Functions as a Multi-Rate Demodulator Over an Octave Range of Symbol Rate or More

The STEL–9236 product family spans 19.2 kbps to 2.048 Mbps with only one hardware difference — the IF bandpass filter, which customers can specify to accommodate their desired data rates.

The IF bandpass filter provides some adjacent channel selectivity. The primary limitation on the ratio of highest to lowest data rate for a given filter is the adjacent channel selectivity required at the lowest data rate. The IF filter is chosen to be as narrow as possible for the highest data rate, then for lower data rates, the filter is somewhat wider than needed. System adjacent channel selectivity is the combination of the SAW IF filter and the digital baseband filters, which have a low pass response on a dB scale is given by equation 1 [3].

$$H(f) = 10\log_{10}\left(\frac{\sin(\pi fT)}{\pi fT}\right)^2 \qquad (1)$$

f = the frequency of interest in Hz. T = the symbol time in seconds. This filter function is steeper for lower symbol rates. As a result, the receiver provides a 2:1 range of symbol rate for any application, thus allowing slower, more cost-effective data rates to be transmitted with optimum performance. The adjacent channel carrier-to-interference ratio (C/I) can be estimated using numerical integration. It is important to note that, due to receive-frequency uncertainty such

as LNB drift, the desired carrier and the adjacent carriers may not be centered in the IF SAW filter. This will somewhat reduce the effectiveness of the IF filter.

A typical case can be examined to illustrate the technique. Figure 2 represents the power spectral density of a typical 512 ksymbol per second signal centered near (but not exactly) 70 MHz and two adjacent carriers of a similar symbol rate but each 10 dB higher in power.

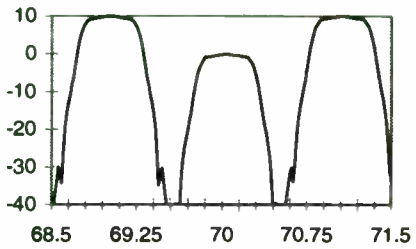

Figure 2. Receive IF Power Spectral Density Before Filtering.

The frequency response of a typical SAW IF filter which might be used for a 1024 ksymbol per second rate is shown Figure 3. This data is derived from specifications for the SAW filter.

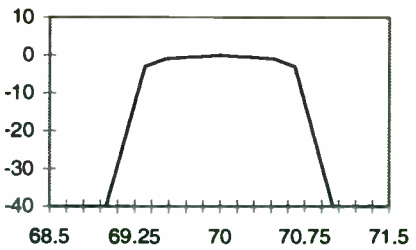

Figure 3. Receive IF SAW Filter Response

Figure 4 below represents the $(\sin(x)/x)^2$ response of the digital filters transformed to a bandpass response centered around the desired carrier.

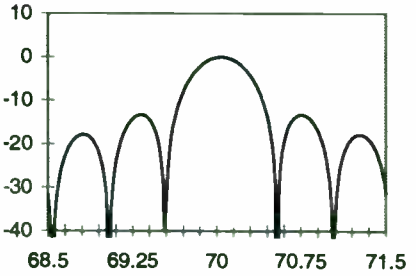

Figure 4. Receive Digital Filter Response

The combined frequency response of the SAW filter and the digital filters is shown in Figure 5. Note that because the desired carrier was chosen to be off-center from the IF filter, and since the digital filters always track the desired signal, the combined response is not symmetrical in this example. Note in Figure 5 below that the lower frequency side lobe is higher than the other side lobe. This situation is chosen for analysis since there will be more adjacent channel interference in this case than if the desired signal were centered in the SAW filter pass band.

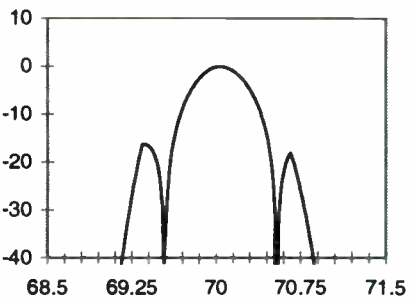

Figure 5. Combined Receive Filter Response

The final received power spectral density is computed by multiplying in linear units the received IF power spectral density by the combined receive filter response (Figure 6). The carrier to interference ratio is computed by integrating (again in linear power units) under the center lobe to obtain the carrier power, and integrating under the two side lobes to find the interference power.

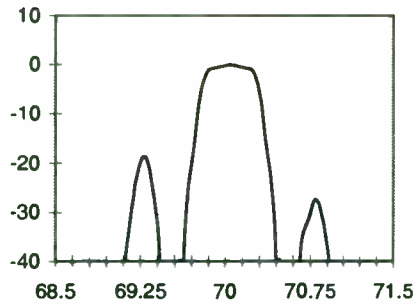

Figure 6. Receive Power Spectral Density After Filtering

The degradation due to adjacent signals is commonly expressed in dB at a particular Eb/No, and can be evaluated by comparing carrier-to-noise versus carrier-to-noise plus interference as given in equation 2. D is the degradation in dB's.

$$D = \left(10\log_{10}\left(\frac{C}{N}\right)\right) - \left(10\log_{10}\left(\frac{C}{N+I}\right)\right) \quad (2)$$

Care must be used when converting from Eb/No to C/N to account for BPSK or QPSK, rate 1/2 convolutional encoding, and receiver noise bandwidth. In this example, the degradation is less than 0.25 dB at an Eb/No of 10 dB for BPSK with no FEC.

V. Typical Applications of the STEL–9236A

The STEL–9236A is incorporated into satellite systems that provide a large variety of data applications. (Figure 7) Some examples:

- A complete "L-band to data stream" receiver board to provide digitized audio for background music in shopping malls, plus other data to businesses around the world.
- A multi-rate demodulator to provide six data rates — from 512 to 2048 kbps using both BPSK and QPSK — to a worldwide radio network for transmission of broadcast audio and control data.
- A receiver subsystem to provide telephone service in rural areas.

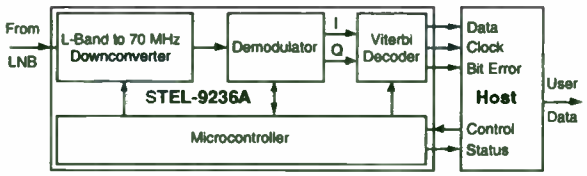

Figure 7. Typical Application Block Diagram

Other applications include inventory, stock market, sales transaction, banking, and nationwide paging services, electronic newspaper transmission, and differential correction information for global positioning systems.

VI. Conclusion

Since the cost of a digital BPSK or QPSK satellite receiver is already on a par with analog FM² receivers, it makes even more economic sense for system designers to employ ready-to-use PSK receiver boards in their VSAT systems. Stanford Telecom's STEL–9236A receiver board offers cost and performance advantages through digital technology. The board is provided ready to use, with a range of data rates from 19.2 to 2048 kbps.

References

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Personal Communications Services Based on Satellite Systems

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Personal Communication Services (PCS) or in other words Universal Personal Telecommunication (UPT) is defined by standard bodies (ITU and others) as a universal service based on a personal, unique and network independent number. In this concept a logical address is assigned to the user which enables him to access the services independent of the access method, and available network/terminal. Thus, the PCS covers all concepts of terminal/personal mobility, wired/wireless access, and call management. Universal Mobile Telecommunication Systems (UMTS) is the ultimate standard for third generation mobile services which is supposed to be implemented by the end of this decade or early next century.

A wide range of applications can be supported by Satellite PCS, e.g paging, electronic mail, fax, positioning systems, hand-held or portable terminals for data communication applications such as Point of Sale (POS), Electronic Data Interchange (EDI), etc. Many issues are involved in implementation of satellite-based PCS such as the choice of a modulation technique, power control, multiple access techniques, channel allocation and isolation of users, delivery time, encoding, and quality of service. Regarding the frequency allocation and related regulatory issues, the FCC and its Negotiated Rule Making (NRM) committee have set and are in the process of setting the required regulations.

There are two possible approaches to implementation of mobile satellite systems. In the first approach, the satellite communication system can work independent of the terrestrial cellular networks and compete with the cellular network services. In the second approach, the satellite system can cooperate with the cellular networks. In the second approach, integration of the two systems offers a uniform service to mobile users. For the emerging wireless communication services, the proper internetworking procedures are a necessity. The satellite system should be able to interact with the two multiple access techniques of the terrestrial wireless networks, which are Time Division Multiple Access (TDMA) and Code Division Multiple Access (CDMA).

This papers discusses the issues of PCS satellite systems such as the integration of satellite systems with cellular networks, Low Earth Orbit (LEO) and Intermediate Circular Orbit (ICO) satellites, Packet Reservation Multiple Access (PRMA), Dynamic Channel Allocation (DCA) and frequency hopping, signalling, multipath fading, Adaptive Power Control, delivery time analysis, modem architecture, synchronization and handover in TDMA and CDMA techniques.

A Spread Spectrum Satellite Tracking System

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This presentation will describe a joint project by National Semiconductor Corporation and SpaceQuest Ltd. to design, develop and deploy a Satellite Ranging and Tracking System that will track miniature, inexpensive ground transponders, called "tags." Each ground transponder will detect a unique code sent specifically to it from a low Earth orbit satellite (LeoSat), and respond within a fixed time interval with a "squawk" to indicate its presence. The LeoSat will measure and record the round trip time delay to the transponder and determine a circular locus of points on the ground from which the signal could have emanated. A second interrogation of the transponder shortly afterwards will allow the location of the transponder to be determined as one of two points on the ground.

The proposed system will be based on a direct sequence spread spectrum technology which offers several advantages over a narrowband system. These advantages include: (1) the ability to coexist with other users in the frequency band with minimal interference, (2) low probability of detection, (3) resistance to interference and jamming, and (4) excellent resolution of transit time.

Both government and commercial applications are envisioned for the satellite-based tracking system. Government users are interested in keeping track of high value assets, including personnel, trucks, containers, and high-priority shipments. Commercial user are interested in tracking the location of trailers, intermodal containers, fishing vessels, and high-value cargo. The projected low price for the tracking services is made possible by the lightweight LeoSat and low-cost tags which use high production volume, single chip transceivers and microprocessor devices.

At a projected cost of less than $100, the low cost tags being developed by National Semiconductor can be considered disposable for many applications. The high-performance, frequency-controlled, single-chip transceivers using BiCMOS technology have extremely low power consumption. High levels of silicon integration are used to achieve a low manufacturing cost at high production volumes. Computer-controlled circuits and functions keep the power consumption of the unit at extremely low levels so that a small, integrated battery can be used effectively for many of the intended applications.

The satellite-based tracking system should achieve its initial operational capability sometime during 1997, following on-orbit checkout of the LeoSats and field testing of the electronic tags.

A Telemetry System for Selected Grain Post-Harvest Operation

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I. Introduction

Grain Post-harvest operation consists of grain storage and grain drying operations. In addition to this, post-harvest operation would also include grain transport and trading activities. After the harvest of grain (i.e. rice, corn), these newly harvested grains are transported from the harvest site to different strategically located drying and storage facilities. Old stocks of grains which were dried and stored earlier are released to grain dealers and distributors. These processess constitute Grain post harvesting operation.

Drying plants and storage silos are used for drying and storage operations. To operate them, micro-environment (environment within the silo) conditions such as temperature, moisture, pressure and relative humidity of these facilities are controlled. Existing micro-environment conditions as well as macro-environment (environment outside the silo) are gathered, and these data in conjunction with past data are used to calculate present settings for the micro-environment conditions. These conditions must be controlled in real time for optimum grain production (minimum wastage during the drying and storage operations).

II. Telemetry System Applications

For gathering data and controlling the micro-environment in real-time, an automated data gathering system can be used in each facility. And since there is a number of these drying and storage facilities, a wireless telemetry system would centralize the operations. Meteorological data gathered (precipitation history, daily sunshine records, geographic location and/or physical characteristics of the structure) are centrally stored.

These data are processed and used in the following applications:

1) A computer simulation software may be developed to predict the state of the grains over a period of time given different assumptions and using the meteorological data gathered. This would greatly change existing policies of product movement. Specifically the "First-in-first-out" policy of grain stocks for drying or storage, where decisions are based on the predictable states of the product. In this policy, newly harvested stocks replaces stocks in storage which in turn are transported to dealers and distributors. By predicting the state of the grains, new stocks may not necessarily replace the old stocks but can be directly transported from the harvest site to the dealers and distributors. This would greatly reduce operation cost without reduction in grain quality.

2) Meteorological data can be used through computer simulation to determine the suitability of the site in drying and storage of certain grains in a given time of the year. Some sites may well be suited to accept other crops or grains at a higher moisture content compared to other storage site locations. This in a way optimizes operation and yield.

3) An automated drying and storage system can be developed where aeration can be fully automated to respond to, and take advantage of transient characteristics of weather on a daily basis. The fan may operate upon detection of a drop in relative humidity or when the wet-bulb temperature of the day is lower than that of the inter-granular atmosphere. The sensors can be made to actuate cooling or aeration systems based on predicted micro-climactic environment as affected by the current state of the grain and physical environment. This system would greatly minimize maintenance cost and greatly improve accuracy and efficiency of the drying and storage operation. The present systems require maintenance personnel in each drying and storage facility. Gathering of data is done by measuring the sensors and storing them in a

portable data logger. Data from the logger is downloaded into a PC terminal in the warehouse and processed to determine if aeration or other actions are required for effective storage and drying. It is clear that the new automated system would greatly improve operation and reduce manpower costs since the drying and storage facilities does not need to be manned.

4) A computer siftware can use the data gathered to determine the besr drying method for particular site. There are different drying methods already developed. And these different methods suit certain grain production sites better than the others. In some areas for example, grain storage using a plastic envelope may prove sufficient to maintain commodities for a certain length of time while other storage structures may be less efficient. With the data gathered using the telemetry system and computer software modelling of the different drying structures, a prediction can be made on the effects of the environment on the grain products.

III. Description of the Telemetry System

The system consist of a main station (MS) and several satellite processing stations (SPS), as shown in Figures 1 and 2. Each satellite processing station consist of a Drying Plant with Storage Silos and warehouse. The storage silos are equipped with aerators and sensing equipment vital for drying and storage operation. A control and data acquisition equipment is connected to a PC terminal which in turn is connected to a radio-modem set-up. The MS is also equiped with a PC or workstation and radio-modem and polls the SPSs to acquire data as well as send control commands. Signals received by the radio-modem is interpretted by the PC and in turn performs the required corresponding action. Data from the sensing instruments are stored in the PC ready to be sent to the main station through the radio-modem. Data gathered by the main station is processed to determine appropriate control commands for the SPSs to effect an optimum post-harvest operation.

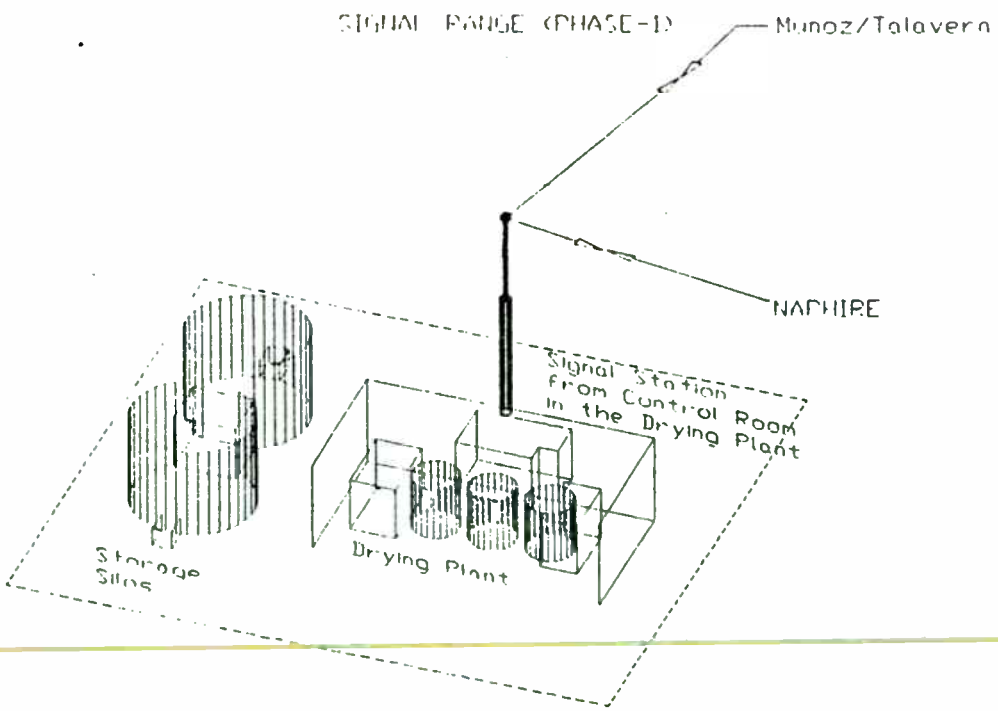

Figure 1. Drying and Storage Facility

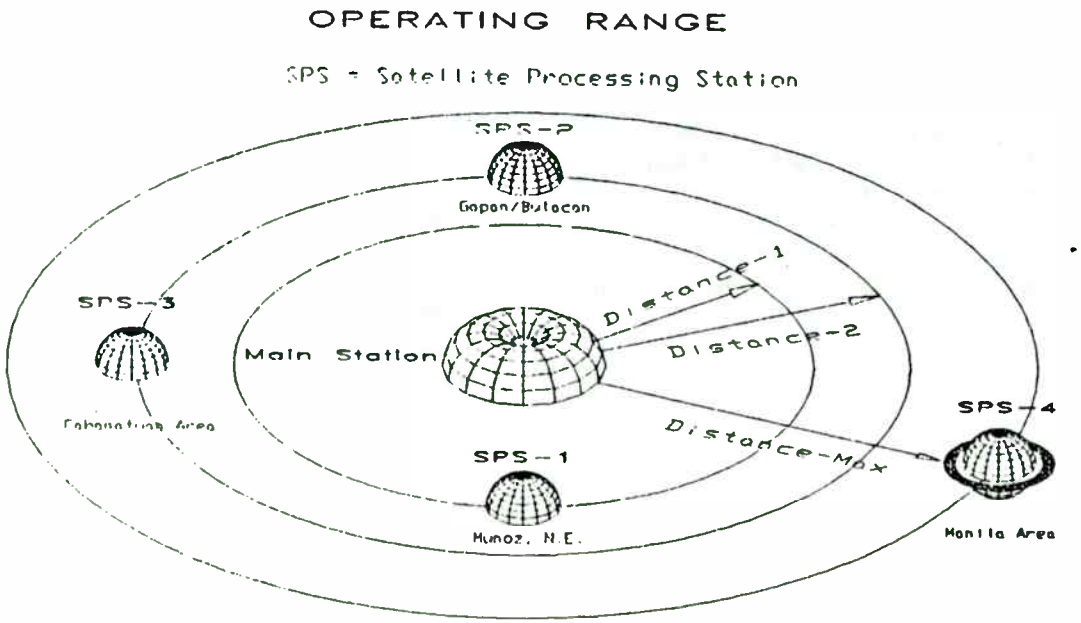

Figure 2. Telemetry System Operating Range

A. Radio Equpment

The radios are UHF radios in the frequency range of 380-500 MHz since this range is suitable for long distance communication in such a rural setting. Power output will be determined by the required distance of transmission. The radios are crystallized with sensitivity of -115 dBm at 20 dB quietting. Receiver ICs from Philips, the NE602 and NE604 are used. Channel bandwidth of 25 kHz is used. Spurious transmissions are low, <60 dBc. Different power modules are designed to easily operate the system at different distances. Different transmission powers of 2W, 5W, 7W, 10W and 30W are available. A combination of Motorola and Philips discrete and hybrid amplifier modules are used for power amplification. A voice service channel is provided for voice communication between SPS and MS. Directional antennas are used in the SPS radios for efficient use of transmitted power since transmission is just directed towards the main station. The main station, on the other hand, makes use of an omni antenna with transmission power of 30W, which is strong enough to communicate with the farthest SPS.

B. SCC/Modem

The SCC or serial communications controller, which has a RS-232 interface to the PC, converts serial data from the PC to serial packet data, processed by a GMSK modem at a speed of 9600. Packets received by the modem on the other hand are converted back to RS-232 serial data format. The SCC design uses a serial communications controller IC and a microprocessor IC from Zilog.

C. Communications Control Software

The communication control software is responsible for passing data from the serial port

to the application software and vice versa. In the main station, the control software send commands and receives data or acknowledgements. While in the SPSs, the control software receives control commands and send data or acknowledgements. Each SPS is polled by the MS to gather meteorological data. Data is stored in a database in primary or secondary storage of the PC or workstation at the MS. The database is accessed by the application software for its use. On the other hand, the SPS communications controller software monitors for packets addressed to him from the MS. These data are stored also in memory to be used by the SPS application software.

D. Application Software

The application software for the MS accesses the data gathered from the different storage/drying facilities and simulates grain status and generates parameters for optimum conditions given the present data and past data. Decision algorithms are implemented to decide on aeration control, suitability of the site, drying method to be used and stock movement.

On the other hand, in the SPSs, the application software controls the data acquisition processess and aeration control plus other special controls for monitoring.

Shown in figure 3 and 4 are the simplified block diagram of the main station and satellite processing station systems.

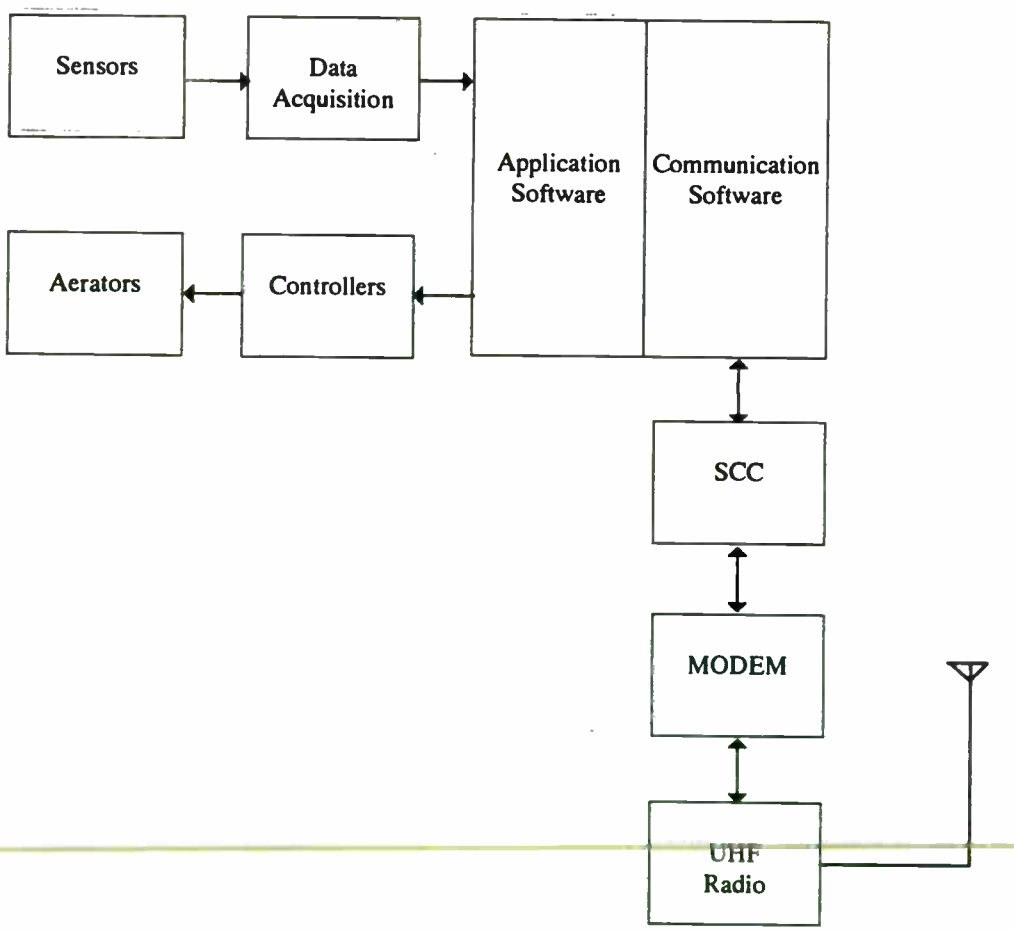

Figure 3. Simplified Block Diagram of Satellite Processing Station System

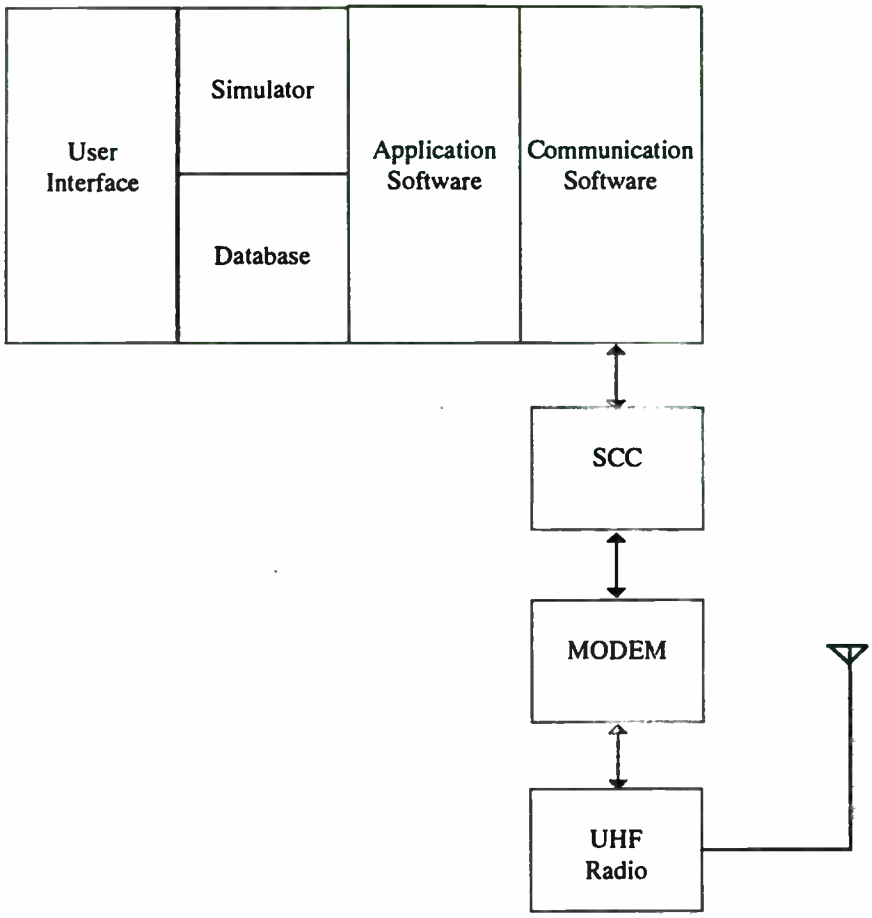

Figure 4. Simplified Block Diagram of Main Station System

IV. Conclusion

A telemetry system has been presented and this shows that with advanced systems for drying and storage (i.e. remote control, computer simulation), it can provide farmers with indicators that will determine the aftermath of their produce much ahead of the harvesting seasons. Drying and storage operation activities can easily be interlinked with the transport and trading activities which is considered to be the lifeline of any agricultural cooperative business. The drying and storage operation has been optimized resulting in high grain yield with less grain losses. Also transport and trading has been optimized greatly reducing operations costs which in effect increases profit.

Acknowledgements

I would like to acknowledge Dr. Ricardo L. Cachuela and the National Post Harvest Institute For Research and Extension (NAPHIRE) .

Reference

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Model and Experiment of A Up-link Power Control Loop for Satellite Communication Systems

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Abstract

This paper presents the model and experiment of the up-link power control loop for the point to multipoint VSAT satellite communication system that broadcasts paging signals to paging base stations. The up-link power control loop is the amplitude locked-loop (ALL) which is dual of the phase locked loop (PLL), or an automatic gain control (AGC) loop. The up-link rain attenuation for the transmitting power control of the hub station is estimated by the attenuation on the self-transmitted signal and received beacon signal and returned signal level from the satellite. The result of up-link power control experiments using the INTELSAT VII is also described and compared with the estimated value.

Architecture of DBS MPEG-2 Satellite Receiver for Consumer Application

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C a n a d a

Abstract

Recently, there have been an increasing number of MPEG-2 video / audio decoder chips but only a few MPEG-2 Transport Layer Demultiplexer devices are available. In this paper architecture and features of our first generation digital consumer satellite receiver with C-Cube Microsystem's chipset are presented.

As a smart adaptive system built around MC68306 32-bit microcontroller this receiver will support various MPEG-2 DTH multistream, point-to-multipoint, multi-carrier DBS (direct broadcasting satellite) networks, especially Canadian ExpressVu and US AlphaStar digital television services.

This paper outlines main HW functional building blocks and basic software applications for receiver setup, MPEG-2 PSI and DVB SI table processing in DRAM and flash memory and ours 7 days TV GUIDE.

Key Words

MPEG-2, video compression digital video, digital audio, QPSK demodulation, RISC and CISC microcontrollers, conditional access, MPEG-2 PSI and DVB SI tables.

Wireless 96
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Slide #1

Architecture of DBS MPEG-2 Satellite Receiver for Consumer Application

WIRELESS '96

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Microwaves & RF

Slide #2

- **Part 1: Satellite Networking**
- **Part 2: RF Front End Subsystem**
- **Part 3: CPU, Transport, Video & Audio**
- **Part 4: Achieved Results and Conclusion**

In this paper major functional building blocks of MPEG-2 digital set top box are described. We will explore capabilities of MPEG-2 transport streams for transfer, synchronization, decoding and presentation of the video, audio and private data in the packet oriented multiplexes. We will study main MPEG-2 multiplex organization and satellite delivery system for digital broadcast application. Main hardware layers of our satellite receiver are:

- Transmission Layer for 27/ 54MHz transponder with QPSK demodulator and Forward Error Correction (FEC) supported by variable symbol rate from 8 to 90 Mbit/s.
- MPEG-2 Transport Layer supported by CL9110 Transport Layer Demultiplexer.
- Conditional Access Layer organized around CL9110, on board descrambler, smart card and 2400 bit/s V22.bis telephone upstream modem.
- Video Compression Layer supported by CL9100 MPEG-2 Video Decoder.
- Audio Compression Layer decoded by CS4920A MPEG-2 Audio Decoder.
- MPEG-2 PSI and DVB SI Network Data Layer supported by CL9110, DRAM & flash memory.
- MPEG-2 Private Data Layer extracted by CL9110 and supported by DRAM and async 38.4 Kbit/s serial UART.
- On Screen Display GUI Layer built around CL9100, main CPU and on board DRAM.

Direct Broadcast Satellite Systems offer new and exciting potential in consumer and business (commercial) areas :

- Ability to receive a few hundred channels.
- Video-on-demand.
- Interactive television.
- High-rate data service.
- Digital ad insertion.
- Video telephony.
- Satellite news gathering.
- Impulse pay-per-view.
- Electronic TV guide and animations.
- Possibility for gambling-on-demand.

All of these services lead toward convergence of Interactive Computing, Newspapers, Television and High-Speed Networks. All of this multimedia services has been predicted (ref1. - ref3). It was a metter of video-audio compression / decompression theory and VLSI integrated circuits technology in last 10 years which enables practical development and deployment of home entertainment products in reasonably low cost (below $1000). Another reason for digital set top box revolution is effective satellite transponder usage. Up to 8 video / audio channels could be packetized in one multiplex to best fit available transponder bandwidth, lowering its cost up to 8 times.

Slide #3

Part 1: MPEG-2 Systems

- Comparison of video compressions
- Main MPEG-2 layers
- MPEG-2 levels and profiles
- Typical DTH satellite delivery system
- Satellite and cable link

Slide #4

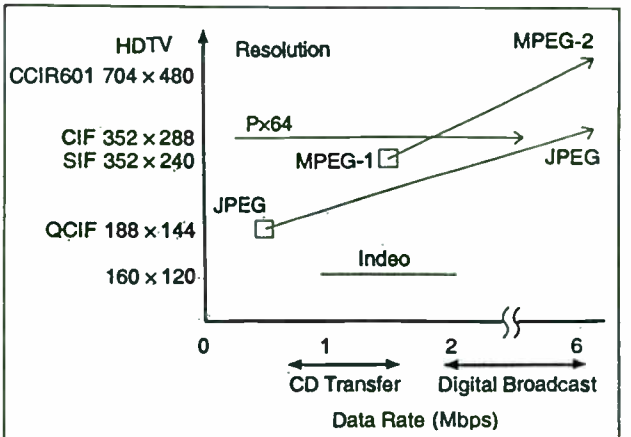


Fig 1: Video compression standards

Bringing digitized multimedia to desktop PC or digital set-top box is a big challenge due to dense stream of moving images and background audio. Typically, this requires high bandwidth. For example reproduction of uncompressed full motion video on 640 x 480 VGA display requires 640 x 480 x 30 x 16 bits / pixel = 140 Mbit/s at video data rate of 30 frames per second.

Even in modern Pentium computer systems it is difficult to overcome physical limitations of its internal buses. Another problem is high storage requirement for video data. One minute of digital video in uncompressed form would require about a Gigabyte - unpractical even for CD storage media.

Finally, third problem exists during video-on-demand data transfers via commonly available Ethernet or Token-Ring LANs. Usually, CPU data base systems are insensitive to infrequent timing errors and usually there is ability to repeat data transfers. But in case of video / audio transmission delays badly affect quality of motion video and sometimes cause serious and random loss of synchronization between audio and video (lip-sync problem).

On the encoding side real-time processing of broadcast or VHS tape quality of video requires enormous CPU power and compression ratio of 100:1 or better. All today hardware compression systems use a series of lossy compression methods which are based on certain characteristics of human vision or eye characteristics.

Due to less eye sensitivity to change in color than to change in intensity color information could be compressed with higher ration. Because of that at the beginning of every compression system we have translation from RGB to YUV color space where Y is intensity and U,V are color values. Also, fine picture detail is less noticeable to the eye. In that case there conversion from bit map spatial domain to frequency domain exists. Transformation could be done by using one of next basic methods:

- DCT (discrete cosine transform)
- VQ (vector quantization)
- DWT (discrete wavelet transform)
- Fractal compression

All of this transformation work on YUV pixel blocks and generate isolated frequency components of the color values and intensity. Later uses frequency dependent quantization of intensity and color values coefficients with controllable loss of image information. This process results in array of numbers with many adjacent same values. Due to that fact we are using zigzag organization of color values and intensity arrays before applying RLA or run-length-amplitude with run-length count and amplitude of the next value. More compression is achieved by Huffman variable length encoding. This is known as single image *intraframe compression.* This is common to Indeo, Px64 & JPEG standards. In case of moving pictures further compression is achieved with *interframe techniques* with predictive coding which compares current and previous image to encode the difference (P frames) & interpolative coding which creates intervening frames between two non-adjacent images (B - bidirectional frames).

Slide #5

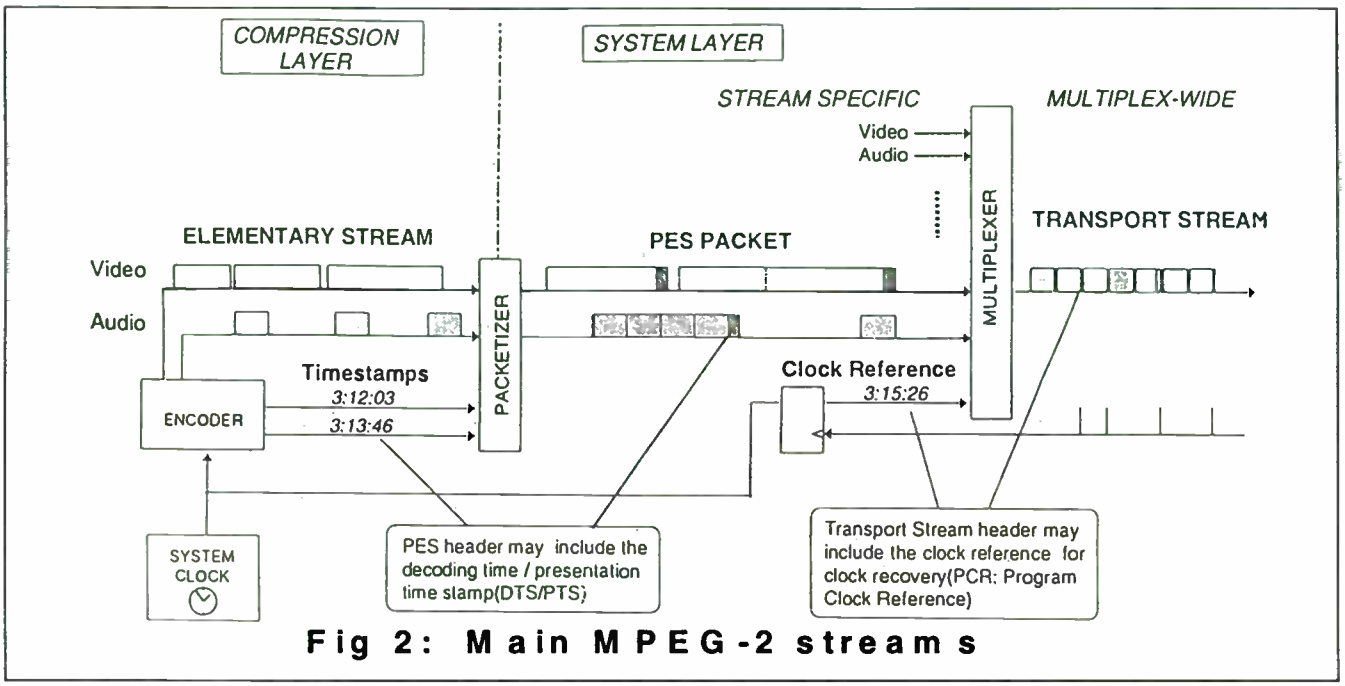


Fig 2: Main MPEG-2 streams

After video, audio & data compression and encoding has been done output of encoder is in a form of pure elementary stream form. ISO/IEC 13818-1 standard specifies 3 basic layers:

- Compression layer with *Elementary Streams*
- System layer with *Packetized Elementary Streams*
- Multiplex-wide layer with *Transport or Program Streams.*

To be quite useful Elementary Streams have to be supported by decoding and presentation time stamps (DTS & PTS). They are included in a PES header. They have to be retrieved by related audio / video decoders. Usually, PES packets are much larger than transport packets and they may form PES streams. In that case they contain Elementary Stream Clock Reference (ESCR) and Elementary Stream Rate fields. PES header also may contains a number of flags opening up a broad range of optional fields. Always PES packets made up of Elementary Streams form a program channel with a common (same) timebase and are intended to be used in a form of Program Streams intended for multimedia applications on CD-ROM and Transport Streams for environments with significant errors. Transport Stream System Layer is divided into Transport Packet Layer for so called multiplex wide operations and Individual Elementary Streams (PES packet layer for stream specific operations in a transport demultiplexer chip). Second layer is Transport Stream Compression Layer for audio and video decoders.

Transport packets with 188 bytes in length begin with 32 bit prefix. Prefix contains one synch byte (47H), 13 bit long packet ID (PID) and optional adaptation field which may carries sample of 27MHz encoder clock (Program Clock Reference or PCR) and a group of flag indicating private data or MPEG-2 Program Specific Information (PSI) tables.

MPEG-2 defines four PSI tables:

- *Program Association Table (PAT).*
- *Program Map Table (PMT).*
- *Network Information Table (NIT).*
- *Conditional Access Table (CAT).*

Slide #6

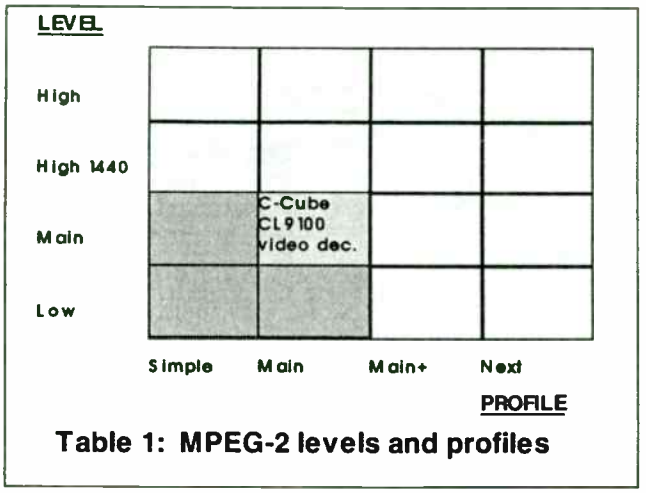


Table 1: MPEG-2 levels and profiles

MPEG-2 profile specifies applied type of compression in spatial and frequency domain. It could be *Simple, Main, Main+ and Next.* Level specifies achieved picture resolution, video data rate, clock speed, I/O bandwidth and size of memory for frame buffer.

- *High Level* usually means HDTV resolution of 1920 x 1152 pixels and video rate < 90Mbit/s.
- *High 1440 Level* specifies resolution less than 1440 x 1152 and video rate less than 60Mbit/s.
- *Main Level* is commonly used nowadays for resolution of 720x576 and video rate <15Mbit/s.
- *Low Level* is for resolution less than 352 x 288 pixels and video data rate less than 4Mbit/s.

Slide #7

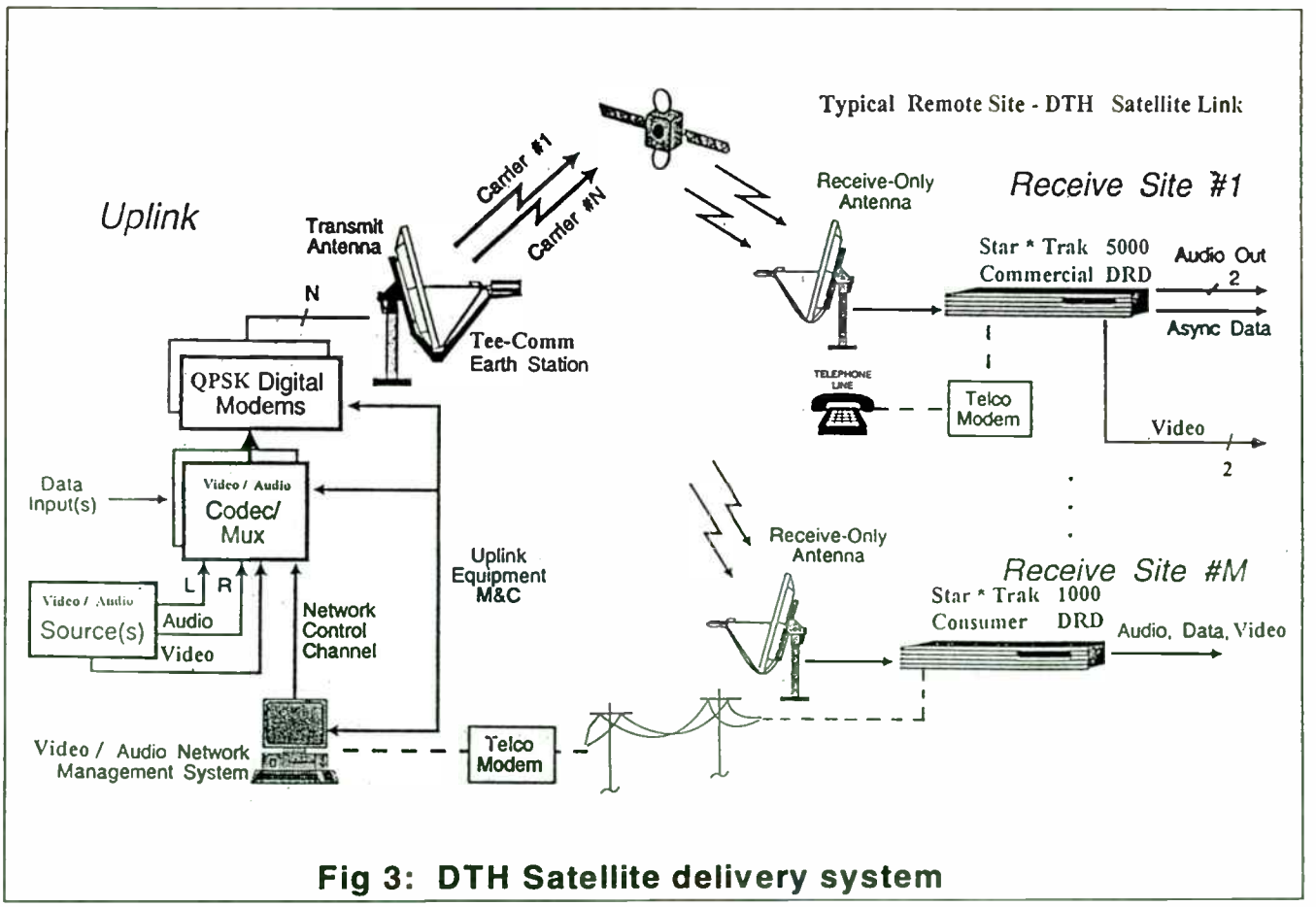
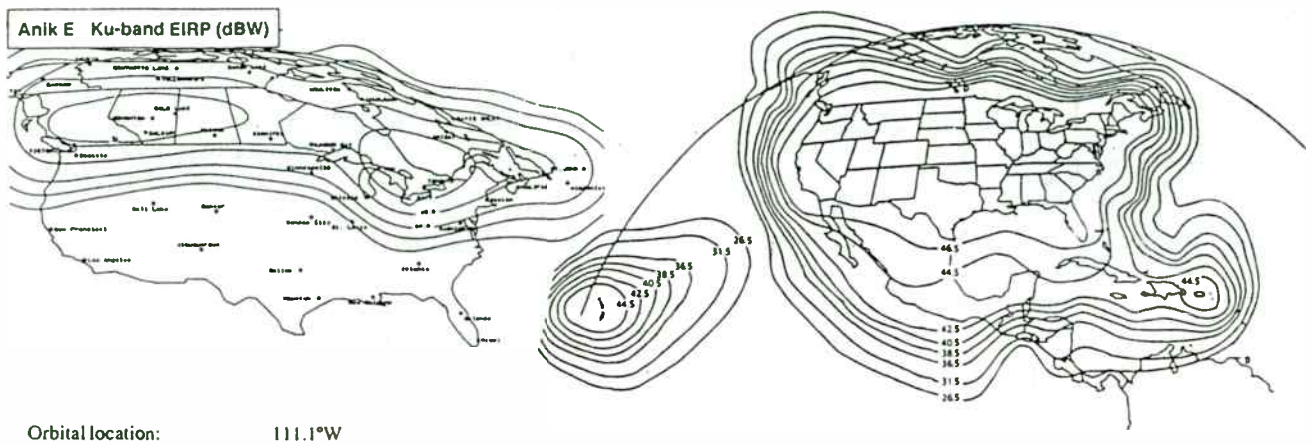


Fig 3: DTH Satellite delivery system

Slide #8



Orbital location:	111.1°W
Launch:	September 1991, Ariane
Expected lifetime:	10 years
Expected end of life:	2003
Ku-band:	Canada and Northern
C-band:	Canada and Conus USA

The AlphaStar system will digitally beam its programming services across the continental U.S., Alaska, Hawaii, and Puerto Rico. From initial system launch the signal will be transmitted directly to consumer households everywhere via AT&T's Telstar 402R satellite. In 1997 AlphaStar will be able to expand this programming offering to well over 200 services on the planned Telstar 5 satellite.

Fig 4: ExpressVu & AlphaStar satellite footprints

In Canada, digital MPEG-2 satellite television distribution is growing rapidly, from theoretical study and planning phases to practical network implementation. Canadian ExpressVu service will be organized as multi-station network, each center will have one transponder in Anik E1 satellite and organize 6 to 8 channels in 1 multiplex Fig. 3 shows typical uplink system which provides:

- ***Physical Network Layer***
- ***Transport Network Layer***
- ***Presentation Network Layer***

Multichannel encoders are organized around *Compression NetWorks System*, originally developed by TV/Com International, San Diego, CA. This will deliver TV signals in various formats: analog,digital, clear or encrypted. Process of format conversion, compression encryption and actual uplinking take place in earth or ground station, using 9m antennas. Encoders and QPSKmodulators are linked by using 270 Mbit/s serial D1 T-link. Total network control is achieved by:

- *Main Encoding and Encryption System (MEES)*
- *Subscriber Management System (SMS)*
- *Network Management System (NMS)*
- *Conditional Access Control System (CACS)*

Cable distribution system will use 64 QAM or 256 QAM modulator in a cable head-end where local insertion of programs & local conditional access information is possible. Remote nodes will be linked by using fiber / coax network or wireless microwave (MMDS, 2.5 GHz). This will effectively reuse existing cable network and subscribers in rural areas will have cable set-top box and 90 cm pizza-size satellite dish.

Networks organized on this way will insure open standard, multiple (global & local) conditional access systems and a broad range of proprietary technologies on equal and fair base. That will affect and drop cost of set-top box.

Physical Network Layer is created by using QPSK satellite modulator and demodulator for very low bit error rate (less than 10 -10) over satellite link. This requires appropriate receive dish size error protection technique at transmit side.

Before modulation we use concatenated error protection coding based on convolutional inner code (Viterbi) and [204, 188] Reed Solomon outer code with framing and convolutional interleaving. This code will relate Reed Solomon (RS) code words directly to MPEG-2 Transport Packets, so in case of uncorrectable but detected errors only one 188 bytes Transport Packet will be affected but flagged. Also, this type of mapping is very good in low satellite power operating conditions (margins). Before RS encoding data is randomized according to IESS-309 standard for low satellite interference and possible timing recovery. Viterbi code rates are 1/2, 2/3, 3/4 5/6 and 7/8. In the case of 27 MHz available satellite transponder bandwidth optimum symbol rate is 22Msym/s and Viterbi rate of 3/4. For Anik E1 or Telstar 402R 54MHz transponders optimum symbol rate is 45 Msym/s and Viterbi rate of 2/3. This will give rate of 90Mbps at the input of QPSK receiver and 60Mbps at its parallel output (7.5MHz which is maximum clocking frequency of CCube's CL9110 Transport Demultiplexer chip).

Adopted satellite modulation system is QPSK with coherent demodulation due to power efficiency and robustness in the case of transponder nonlinearity's. Applied modulators have variable Nyquist roll-off filtering, selectable between 20, 27, 35 and 40%.

Cable modulation system uses 256 or 64 QAM with 15% Nyquist roll-off filtering. For low error rates adaptive frequency equalization at QAM receiver will be adopted.

Transport Network Layer is ISO / IEC 13818-1 MPEG-2 System Layer. System multiplex will use *Statistical Multiplexing or Joint Bit Rate Control* to achieve constant overall bit rate in a group of video encoders and variable output bit rate at each individual video encoder within defined range. This feature is based on human eye characteristic that different complexity of video material could have variable bit rate (low in case of static pictures - opera or drama as example and higher in case of dynamic pictures - sport events or action movies) and still achieve very good visual or image quality. This changes in video bit rate could be done dynamically per frame or in a simpler form dynamically per program. In later case video rate control is under software control and is done by using DVB EIT (Event Information Table) which contains category descriptor for each TV program. Conducted theoretical analyses show that about 20% of compression efficiency can be achieved.

Presentation Network Layer for video decoding is fully compliant with MPEG-2 Main Level @ Main Profile. Supported video rates are from 1 to 12 Mbit/s with automatic 3:2 pull-down detection for 24Hz film video. Encoder can generate or skip B frames and may have various length of Group Of Pictures (GOP). It also supports a few resolution levels. Audio encoder supports ISO / IEC 13818-3 MPEG-2 standard for Layer 1 or 2 audio compression from 32 to 384 Kbit/s bit rates. This selection is supported via *UspLite* control software. In a transport stream we could have up to 6 audio streams per each video stream (multilingual channels). Audio / Video synchronization is done by means of MPEG-2 time-stamp mechanism or by streams alignment.

Closed captioning and teletext is supported by means of VBI information data extracted from the input NTSC / PAL signal at the encoder and transported in a User Data Field of Video Picture Layer (2 bytes per frame). At the set-top box side this information is extracted from CL9100 video decoder chip on interrupt base per frame. It may be:

- *Inserted locally* in IRD (integrated receiver decoder) by using YUV - PAL/NTSC video encoder integrated circuit which supports closed captioning at line 21. This is the case of our Star * Trak 1000 consumer receiver.

- *Reinserted as VBI information* in the VBI of the baseband NTSC composite video and channel 3 or channel 4 in RF modulator. This is the case of our Star * Trak 5000 commercial receiver.

On-Screen-Displays (OSD) for multilingual bitmapped graphics, graphical overlays or program provider logos are supported with graphical overlay feature of CL9100 video decoder chip. Also, this is the base of our TV-Guide. MPEG-2 private data are supported by async RS-232 low rate (up to 38.4Kb/s) auxiliary data port for consumer receiver Commercial set-top box supports RS-232 / RS485 or RS422 interface for data rates up to 115.2 Kbit/s.

Slide #9

Part 2: RF Front End Subsystem

- Transponder Usage
- Analog vs. Digital Comparison
- Multichannel, Multicarrier Transponder
- RS Performance Curves
- Structural Diagram of QPSK Receiver
- Achieved Results

Slide #10

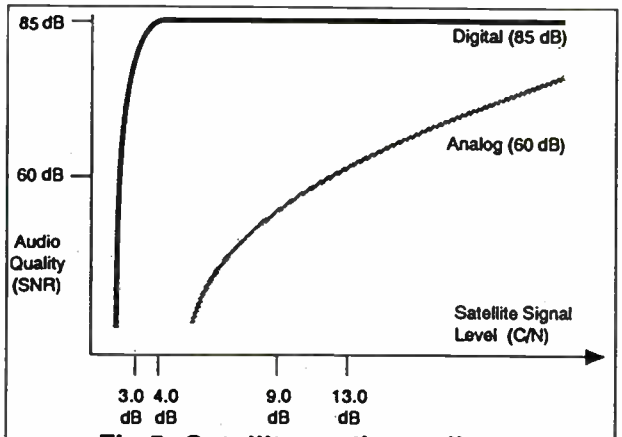


Fig 5: Satellite audio quality

Since the introduction of compact disc more than ten years ago home entertainment industry is less accepting lower fidelity and higher noise mediums for audio / video storage such as cassetes, Lps and video tapes, shown at figure 5. There are a few adventages of digitization of analog sources:

- Mixed video / voice / data networks very useful for teleconferencing.
- Application of forward error correction based on redundancy coding for low bit error rates.
- Superior signal-to-noise ratio in digital transmission systems over analog techniques based on repeaters where SN ratio always degrades. This is especcialy true in the case of cable distribution networks where picture quality depends on end-user location in network chain.
- Digital tecniques allow one to easily encrypt the signal to maintain privacy of information, which is important in business comm. networks.

Digital QPSK modulation is based on phase modulation of the carrier [see ref. 4, 5, 7] according to the data state. It is the most efficient modulation technique in terms of required minimum energy for a given bit error rate. Normalized S/N ratio is a quantity called Eb/No, where Eb is energy per bit and No is the spectral density of the noise. Energy per bit power times time i.e. carrier power C times period T. So we have that Eb/ No = C T / No equals C / T No. Because T is bit period (interval) then 1/T equals R or bit rate. So, one end ups with Eb / No as C / NoR = C / N because No R is noise power in a bit rate bandwidth. By modulating the phase of a carrier we have :

- *BPSK or Biphase Modulation* where we take each information bit and modulate the carrier into two phase states.
- *QPSK or Quadraphase Modulation* where every two data bits or dibits modulate the carrier into four states.

We can think about QPSK as modulationg two quadrature carriers at half the data rate, so we use half of the RF power for each data stream. But, the bit period for each data stream is twice as long. This ends up with the same Eb / No on each carrier as one originally used for a BPSK carrier so we can achieve an overall error rate for each quadrature carrier that is the same as the original BPSK BER.

Due to the transponder limitations in their available bandwidth and power (typical saturated EIRP in 36MHz transponder is around 36dBW and to achieve linear operation with multiple carriers there is 4dB output backoff giving us effective EIRP of 32dBW. The spectrum for NRZ (non-return to zero) signal is non bandlimited. The nulls of the spectrum are centered at the symbol rate (for BPSK that is bit rate and for QPSK the symbol or baud rate (rate of changes of modulation characteristics) is at one-half of the bit rate. Adjacent spectrums and spectrum roll-off has a (sin(x) / x) shape.

Slide #11

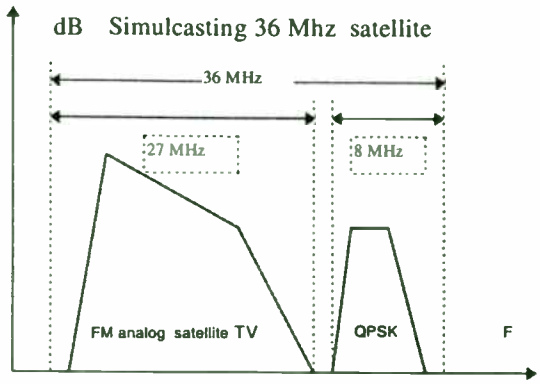


Fig 6: FM / QPSK dual-mode

In that case the power of adjacent leaps and adjacent carriers in transponder acts like noise for the current channel and it is known as *Adjacent Channel Interference (ACI).* Usually, digital filters in QPSK modulators / receivers must eliminate the power from the adjacent channels / leaps and minimize the effect of ACI by minimizing inter-symbols interference (Nyquist Filtering) and also maximizing SNR.

By using *Forward Error Correction (FEC)* coding which means adding a controlled redudancy in information bits one could achieve a lower power level for a given BER performance curve.

Figure 6 shows example of simultaneous transfer of analog and digital TV over one 36MHz transponder. Multiple FM analog audio channels combined by digital QPSK satellite TV are shown at figure 7.

Slide #12

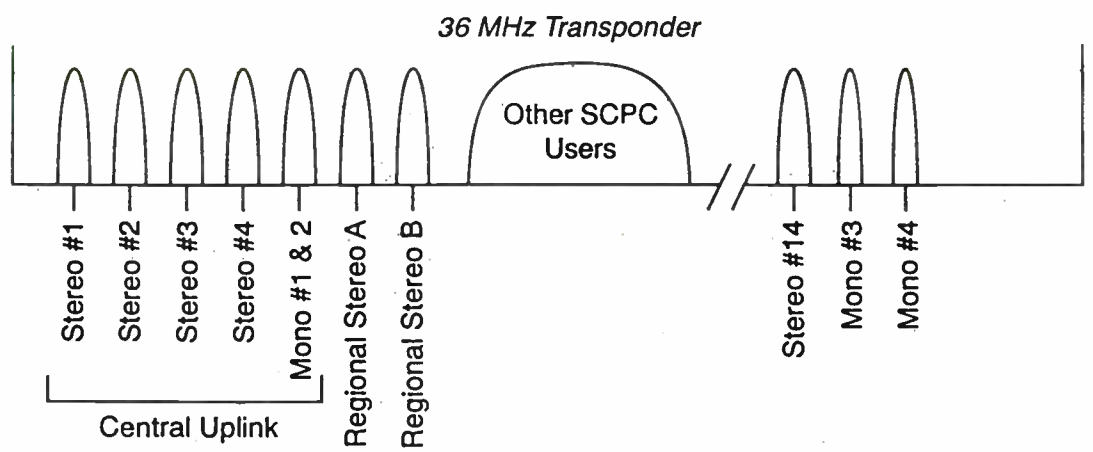


Fig 7: Multichannel 36MHz Transponder

Typical considerations in design of QPSK uplink systems are:

- *Single Carrier per Transponder* for eperation in saturated Hub Power Amplifiers to achieve max. transponder output power and acceptance of uplink signals from single site.
- *For Two Polarized Carriers per Transponder* may require 3dB back-off for each carrier to minimize no-linearities. Also receivers need polarization control and each uplink carrier may come from different sites.
- *Multiple Carriers per Transponder* requires back-off hub power amplifiers to minimize non-linear conferences of multi-carriers but waste guard-band between adjacent carriers.
- *Analog FM / Digital QPSK Simulcasting*

Slide #13

Key System Technologies

Critical Receiver Conditions

- Eb/No = 4~8dB for 11-12GHz 30" dish
- 2" increase in dish size can improve Eb / No up to 6dB.
- Ku band needs 3dB min "rain margin"
- For video rate of 4Mb/s and error rate of 10^{-9} video errors every 10 min.
- Viterbi / RS / Interleaving FEC codes
- Error Concealment and MPEG-2 motion compensation reduce artifacts

Slide #14

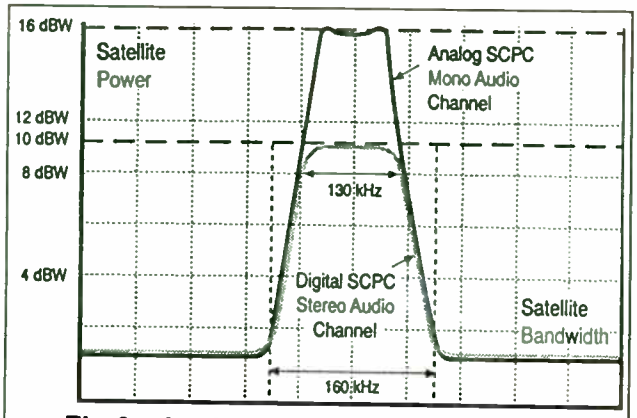


Fig 8: Analog and Digital Spectrums

Typical characteristic curves for RS code with 16 bytes redundant code are shown at figure 9. Figure 9. shows probability of uncorrectable error Pue vs. channel symbol error rate Pse in the case of independent symbol errors. MPEG-2 via QPSK uses (204, 188) code.

Typical Viterbi outer code rate curves are shown at figure 10. Here we can see that it is feasible to achieve very low BER by using more redundant coding (lower value of Viterbi code rate). This means less information (data) bits over single communication channel (transponder).

Slide #15

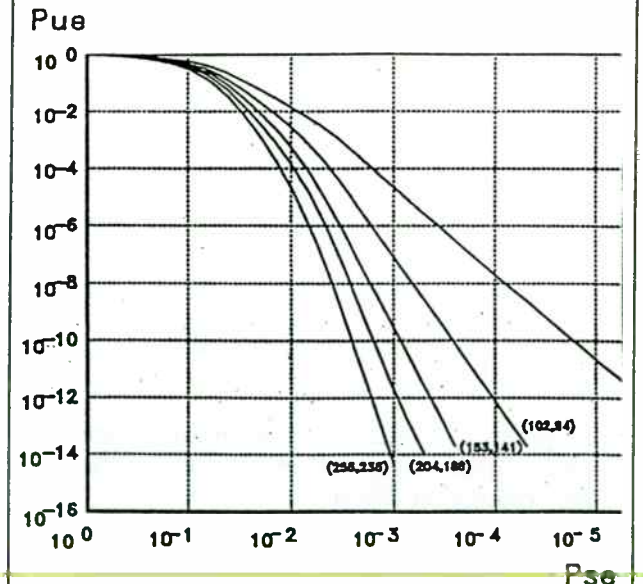


Fig 9: RS Codes of Rates 0.92

Slide #16

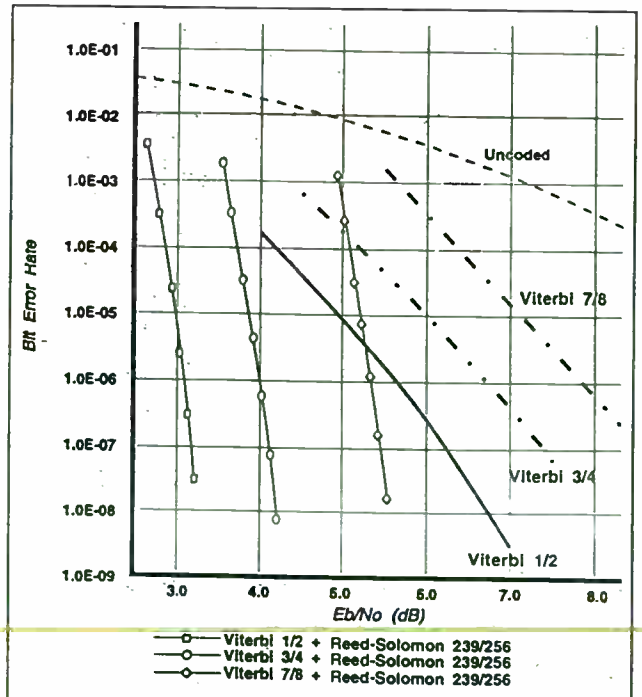


Fig 10: Viterbi Performance Curves

Slide #17

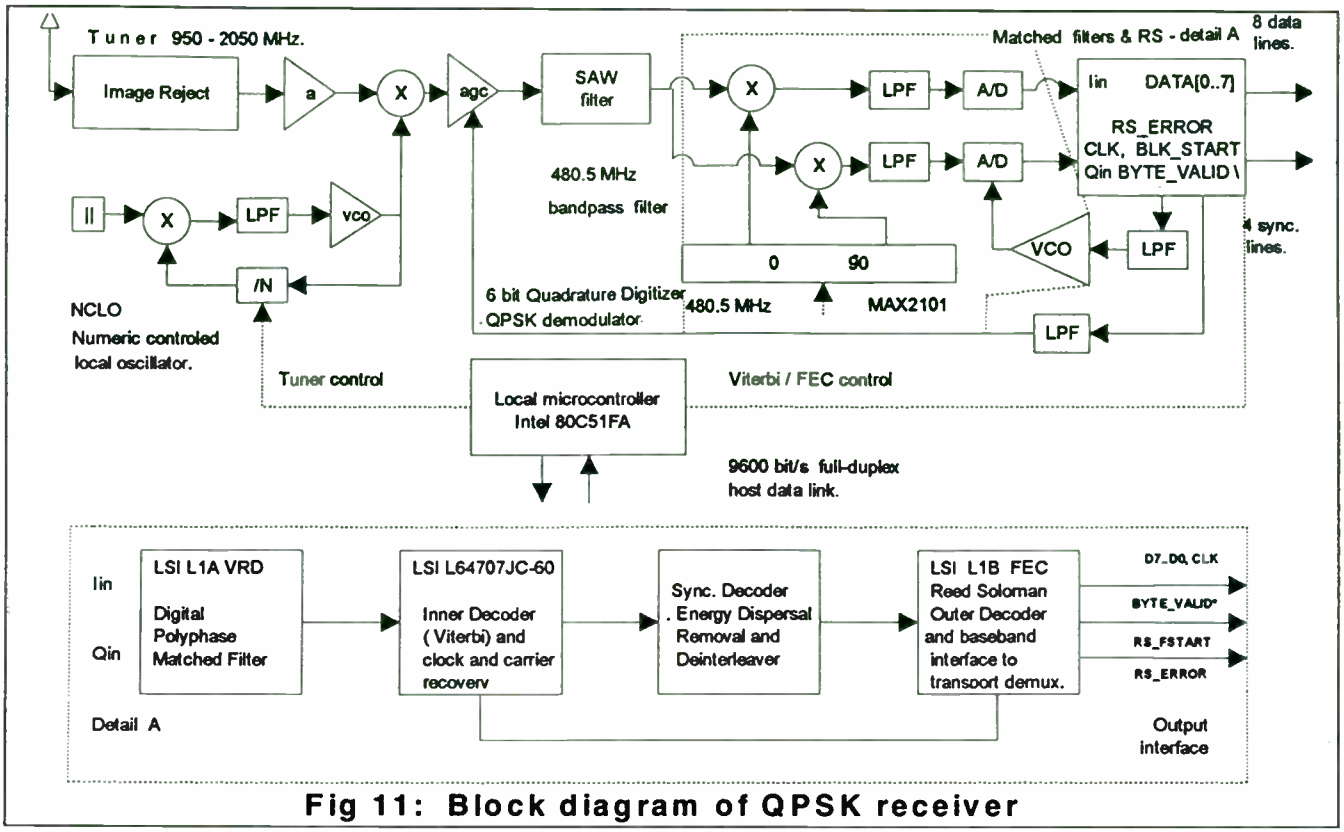


Fig 11: Block diagram of QPSK receiver

The system block diagram of QPSK receiver is shown at Figure 11. The downconverted Ku band input signal by the satellite dish LNB fits L band from 950 to 2050 MHz. L band local oscillator in the tuner synthesizes frequency band from 1.44 to 2.54 GHz by using crystal reference and PLL with the programmable divider (divide by N) in the feedback Due to the large tuning range (greater than twice the intermediate frequency of 480.5 MHz a tunable image reject filter is used.

Filtering of 54 MHz satellite transponder signal is done with a surface acoustics wave filter (SAW). As a passband filter it has very narrow transition band and it also reject adjacent channel interference. External closed loop provides AGC Automatic Gain Control.

Downconversion of 480.5 MHz IF signal in quadrature to baseband is done by fixed LO. Dual 60 Msym/s analog to digital A/D converters sample the quadrature baseband signals. Sample rate is controlled by 3 digital outputs from on board local microcontroller (INTEL 80C51FA).

Extrapolation to 90 MHz signal is done in ASIC. Also antialiasing low pass filters for I and Q baseband signals have externally variable bandwidth from 10 to 30 MHz and are under CPU control of CPU. The digital downconverter performs decimation to twice the baud rate, removes the residual frequency offset & performs the root-raised cosine filtering. The coefficient set of p olyphase root-raised cosine filters are downloadable, so PMF filters could have 20, 27, 35 and 40 % roll-off.

The symbol synchronizer closes quadrature data transition tracking loop. The demodulated I and Q data streams are passed to the deinterleaver before being decoded by the inner Viterbi decoder. Next step is Reed-Solomon outer decoding. Byte wide data with clock and RS error signaling are passed to C-CUBE CL9110 MPEG-2 transport layer demultiplexer. Measured BER erformance are shown at Fig. 12. For bandwidth calculation we use equation:

$$ActBW = Ri * 1/RS * 1/FEC * 1/2 * ALPHA \quad (1)$$

Slide #18

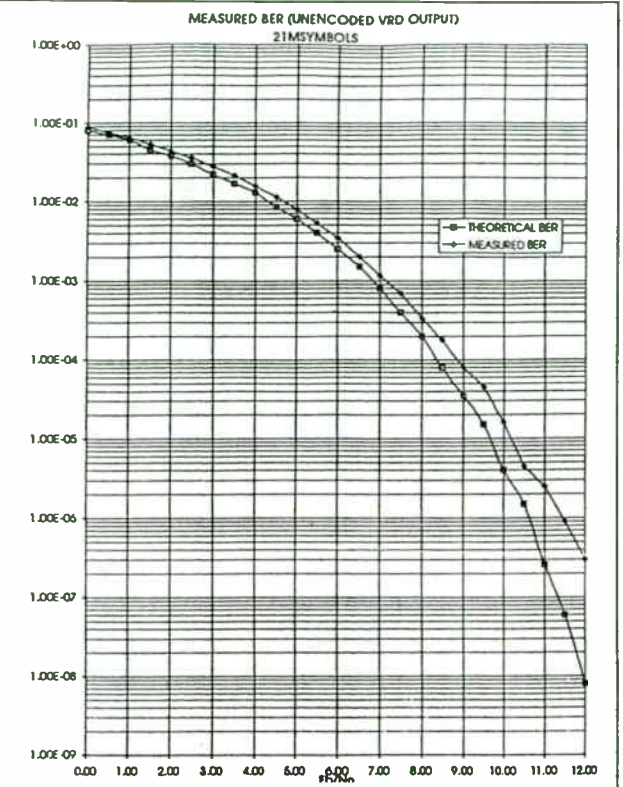


Fig 12. Measured QPSK performance @ 21 Msym/s

Slide #19

Main features of QPSK receiver:

- DVB V4 ModB compatible
- QPSK, BPSK & OQPSK support
- Raised Cosine spectral filter
- Concatenated FEC coding
- Interleaving for burst noise
- Viterbi Inner Code k=7
- Programmable RS Outer Code
- IESS-309 & V.35 / IESS-308 scrambler for energy disperzal
- Symbol Rates from 1 to 45 MHz
- User Data Rates > 55Mbit/s
- Low threshold C/N - Eb/No
- Wide L-band input: 950-2050 MHz
- Carrier offset +- 5MHz
- 9600 bit/s UART SCADA interface
- Power AutoScan for Carriers
- Built-in self-test

In equation (1) ActBW is the actual bandwidth occupied on a satellite transponder, Ri is the average or aggregate bit rate (in Mbps) of actual service programming with transport stream overhead, PSI or Program Specific Information SI or System Information Tables and CA EMM / ECM or Conditional Access Entitlement Management Messages and Entitlement Control Messages. Item RS or Reed Solomon error correction factor equals 204 / 188. Item FEC =1/2, 2/3, 3/4, etc. is Viterbi error correction rate and ALPHA = 1.2 - 1.4 corresponds to filter roll-off factor from 20% - 40%

Note that the factor '2' in '1/2' refers to QPSK's modulation efficiency of 2 bits/Hz. Also, term Ri * 1/RS * 1/ FEC * 1/2 = ActBW / ALPHA is known as the symbol rate (in Msym / s). Consider example from Fig. 12, running 21 Msym / s (constrained by a 27MHz transponder) at 20% roll-off and V = 2/3 yields:

ActBW = SR * ALPHA = 21Msym/s * 1.4 = 25.2MHz
From SR = Ri * 1/RS * 1/ FEC *1/2 we get data rate

Ri=SR * RS * FEC * 2=21Msym/s * 2/3 * 188/204* 2;

This yields aggregate data rate of 25.8 Mb/s By using three video channels with 6 Mbit/s with six audio channels per one video service for multilingual support with 256 Kbit/s one can achieve aggregate date rate of 22. 6 Mbit/s. Remaining 3.2 Mbit/s could be used for PSI / SI data, electronic program guide (EPG) and private data transfers. So, one could packets three video channels of VHS type quality & plenty of audio channels per 27MHz transponder.

At slide 18 typical characteristics of variable rate QPSK receiver used in our Star * Track 1000 and Star * Track 5000 set-top boxes are illustrated.

Conclusion: Variable rate QPSK front - end receiver has one big advantage over fixed rate systems It is able to adopt new uplink conditions by using NIT data (Network Information Table). It creates a great possibility for *Dynamic Satellite Networks,* important feature for traffic change or transponder failure.

Slide #20

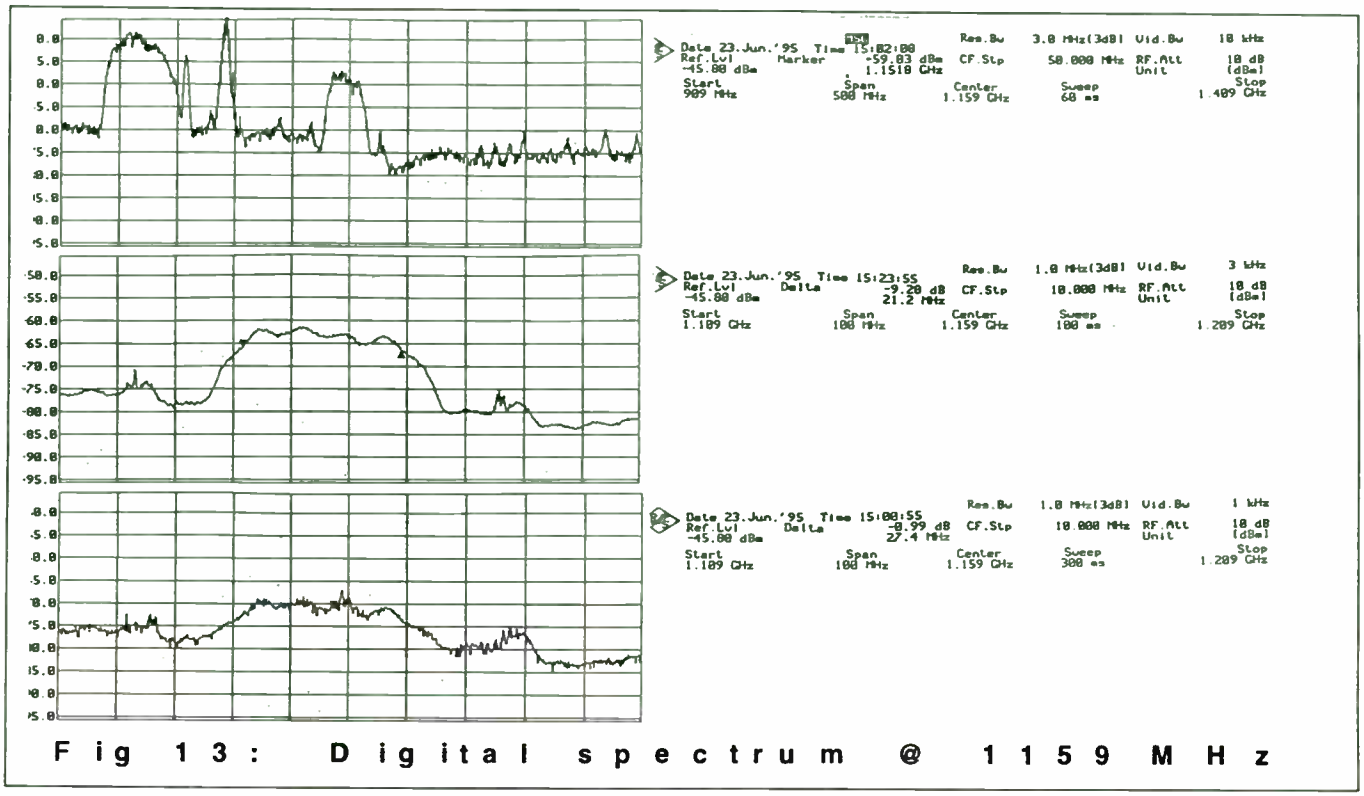


Fig 13: Digital spectrum @ 1159 MHz

Tests conducted in Telesat Canada teleport in Montreal over Anik E1 satellite with 30Msym/s and Viterbi rate of 2/3 shows necessary power level for reliable operation without motion block artifacts.

Rohde & Schwarz spectrum analyser was used in spectrum power level measurement @ L band input of QPSK receiver. Reception was in Milton, Canada. Fig. 13 shows typical spectrum distribution over 500MHz span range. We can see a few analog subcarriers and a digital carrier at 1159MHz.

Experiment was started with teleport station power level which caused -57dBm relative power after downconversion from 11 - 12 GHz Ku band to L band by using 75cm satellite dish. Also, one can see detailed digital spectrum shape caused by QPSK modulation.

By continuous power drop of uplink station we have achieved reliable satellite receiver peration with -70dBm. This is extremely important result for check satellite link budget. QPSK receiver was detected about 400 corrected Reed - Solomon errors at every 3 seconds. Number of uncorrected errors reported by FEC chip was neglictable.

Polling of QPSK receiver was done every 3 seconds by using serial port and main host CPU at our satellite receiver. Data were sent to diagnostic RS-232 port. Uplink parameters were:

- Access Format: FEC Link with RS(188,204) & Viterbi rate of 2/3.
- Information Rate: 36.5 Mbit/s
- Threshold Eb/No: 4.8 dB
- Information Margin: 1dB
- Symbol Rate: 29.7048 Msym/s
- Carrier Occupied Bandwidth: 35.645 MHz
- Threshold C/No Performance: 81.4 dB-Hz
- Satellite Saturated Flux Density: -85 dBW/m^2
- Uplink Carrier EIRP: 77.8 dB
- C/No Uplink Thermal Noise: 103.7 dB-Hz
- Earth Station Antenna Diameter: 9.2m
- Earth Station Antenna Efficiency: 63.0%
- Earth Station Antenna Boresight Gain: 60.7dBi
- Available Uplink EIRP: 91.2 dBW
- Required HPA Power: 101W
- HPA Output Back Off: 13.4 dB
- Uplink Power Density: -57.7 dBW / Hz
- Receive Antenna Diameter: 75 cm.

Slide #21:

Part 3: CPU, Transport, Video & Audio

- Motorola 68306 Microcontroller System
- CL9110 Transport Demultiplexer
- CL9100 MPEG-2 Video Decoder
- CS4920A MPEG-2 Audio Decoder
- Bt9104 YUV / NTSC Video Encoder
- Flash Memory & Telephone Upstream Modem for IPPV applications
- Software Requirements, Achieved Results, Conclusion and Acknowledgements

Slide #22

Motorola 68306 MCU features:

- 32-bit 68000EC 2.4 MIPS , 16.67 Mhz core
- Two channel sync / async 38.4Kbps UART
- Integrated 16 Mbyte DRAM controller
- Integrated Prioritized Interrupt Controller
- Integrated Timer / Couner & Bus Timeout
- Programmable Chip Selects & Wait States
- 24 Address Lines, 16 Data Lines, 132 pin PQFP or 144 pin TQFP package, 5V only

Slide #23

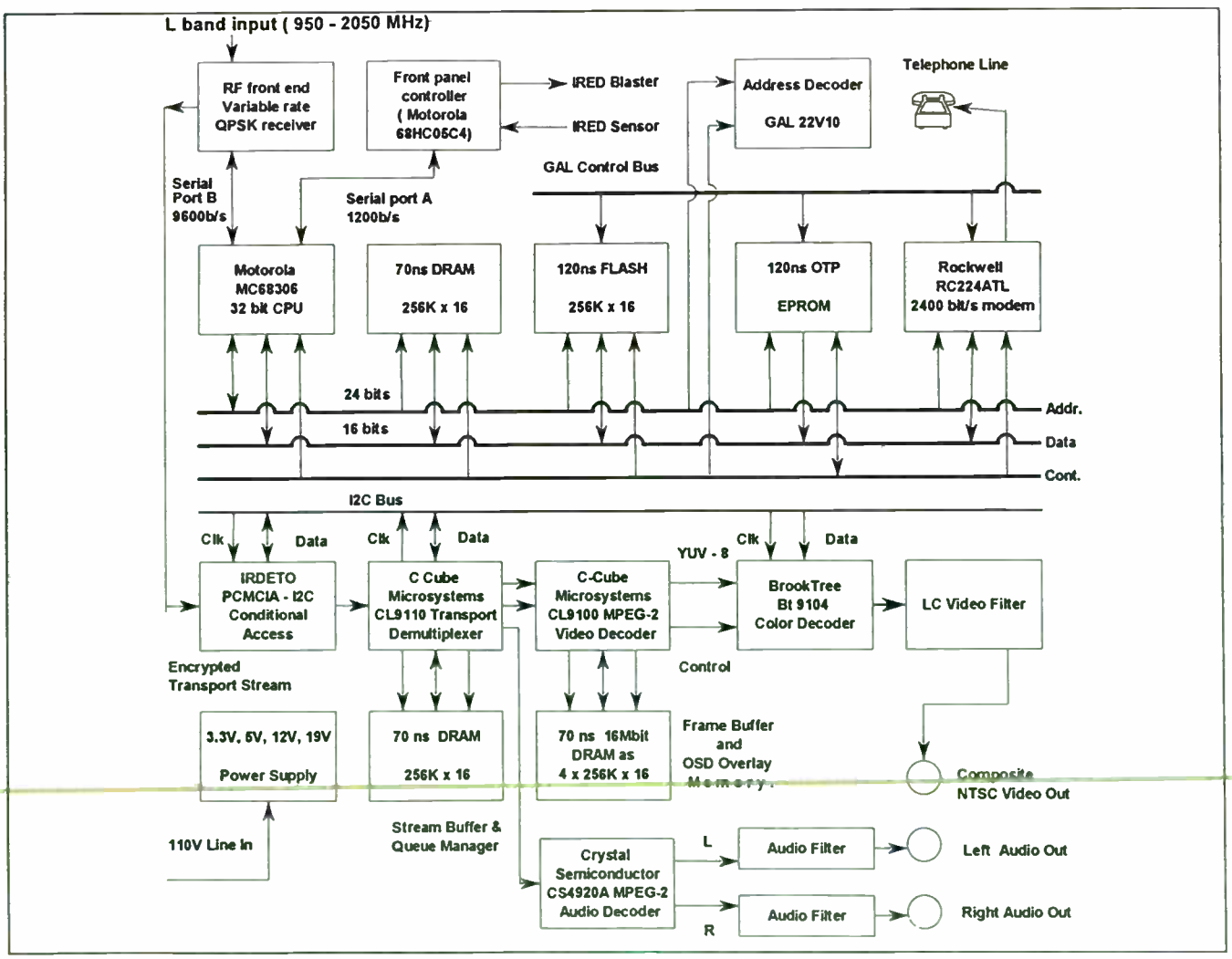


Fig 14: Block Diagram of MPEG-2 Satellite Receiver

Slide #24

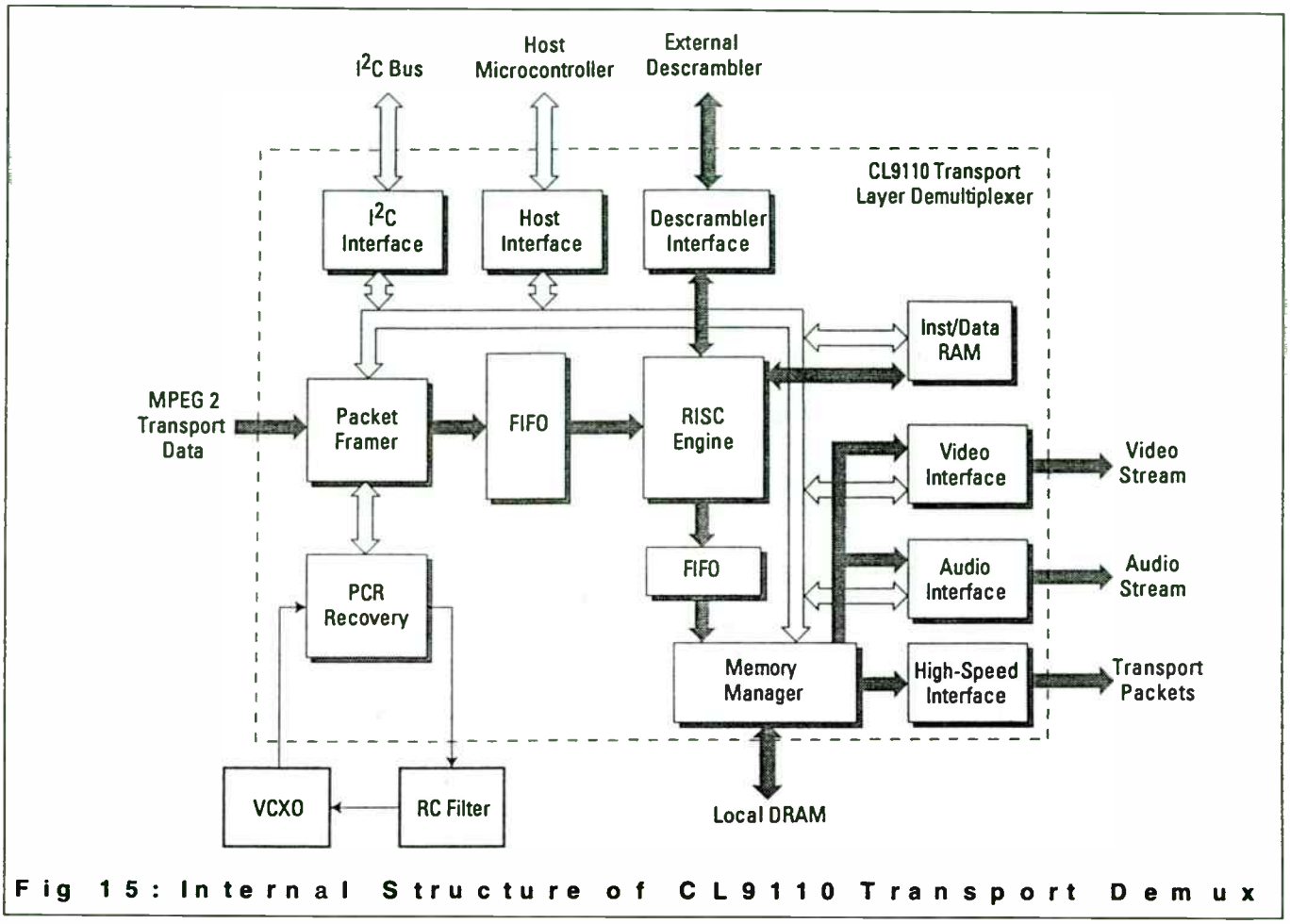


Fig 15: Internal Structure of CL9110 Transport Demux

Block diagram of our satellite receiver at Fig. 14 shows a few separate building block:

- *Motorola 68306 32-bit host microcontroller* with 16 bit data bus and 16 MBytes address space. For device drivers we use 1Mbit OTP (one time programmable) memory organized as 64K x 16 (Atmel 27C1024). This memory stores fixed part of application software. Receiver's channel memory, conditional access system software and GUI interface is stored in 4Mbit flash memory organized as 256K x 16 (INTEL AMD or SGS Thomson memory).

- *9600 bit/s full duplex, multidrop serial link to QPSK receiver* for issuing control messages for frequency, symbol rate and Viterbi rate setup. Internal uart A of 68306 MCU is used and it can operate as remote diagnostic serial port.

With baud rates up to 38.4 Kbit/s it is used as remote, in-system flash memory programming port.

- *9600 bit/s full duplex serial link to front panel controller* organized around Motorola 68C05C4 8 bit MCU. This module is used as scanning & decoding IRED remote and front panel key controller. Also it refreshes 4 digits LED display It has ability to learn foreign remote control keys, send or retrieve them from host CPU and activate IRED blaster @ 38KHz IRED-infra red carrier frequency. This allows control of external devices such as TV or VCR.

- *MPEG-2 subsystem* consists of C-CUBE CL9110 transport demultiplexer whose structure is shown at Fig. 15, CL9100 video decoder, Crystal Semiconductor CS4920A audio decoder and Brooktree Bt9104 color decoder (video encoder).

- *I²C serial link* integrated in CL9110 is used for initialization of Bt9104 color decoder and for audio decoder microcode downloading.

- *Rockwell ATL224 2400 bps telephone modem* is used as upstream link to remote subscriber management center for PPV applications.

- *Conditional access system*, currently under development is based on IRDETO EURO-I descrambler chip embedded in PCMCIA style control subsystem. Modified ACCESS BUS ™ control channel is used for message exchange between host CPU and ST-9 MCU embedded in a CAM (conditional access module). As block diagram shows another types of descrambling devices (Philips SAA7206, Sony CXD1954) could be used in a similar approach where CAM is placed between QPSK or QAM receiver and transport demultiplexer. Acquisition of ECM & EMM messages has to be done by transport demultiplexer and host CPU in the case of descrambling device only. Another possible location for descrambler device is @ descrambler port of CL9110 and DVCOM device could be used. Decryption of control messages in a CAM is done by ISO-7816 smart card. Also, working key for descrambler is retrieved from smart card at approximately every 10 seconds. IPPV or Impulse Pay Per View records are stored in smart card and once per month are retrieved from the card for the billing purpose. By using RSA or DES encryption / decryption algorithm smart card system offers a few main services:

  * Peer Entity Authentication
  * Data Origin Authentication
  * Access Control and Audit
  * Confidentiality
  * Integrity and Non Repudiation
  * Access Key Management
  * Screen Blackout Control
  * IPPV Management
  * Region Blackout
  * Parental Control
  * Home Shopping
  * Macrovision Control
  * Pre-View and Event Recording

- *Analog active LC video and RC audio filters* to RCA back panel connectors for external audio / video home theatre system.

Main part of our satellite receiver is CL9110 MPEG-2 transport demultiplexer whose internal structure is shown at Fig. 15. It has DRAM memory manager for 2 banks from 32 to 256K x 16. This is used in shared memory CPU bus systems. Also our main 68306 CPU controller has integrated DRAM controller, so practically this DBS receiver could support to 4 DRAM memory banks. Two memory banks of 256K x 16 are implemented: one at CPU side and another at CL9110 side. All read / write access operations to this memory, to CL9100 video decoder and it's OSD and video frame memory are through memory manager of CL9110. DTACK signal (Data Transfer ACKnowledge) with external wait state logic is used for synchronization between host microcontroller and transport demultiplexer.

CL9110 whose internal system structure is illustrated at Fig. 15 is RISC CPU based transport demultiplexer. RISC engine requires downloading of 1KByte microcode from host CPU and performs next functions:

- PES and PSI MPEG-2 transport parsing
- Stream demultiplexing and filtering
- Control of external stream descrambler
- PCR, video and audio PTS extraction
- Video & audio channel data buffering
- Extended channel rate buffering
- Video decoder interface (to CL9100)
- Audio decoder interface (to CS4920A)
- HSO or High Speed Output interface for outputting transport packets based on PID matches in real time
- I²C interface for sending data and control messages to audio and color decoder

CL9110 performs *Program Clock Reference or PCR recovery* by using PCR samples embedded in an MPEG-2 transport packet. In our receiver recovery loop is built around Bt9104 color decoder 27MHz local oscillator. VCO or Voltage Controlled Oscillator action is derived from varactor diodes built around 27MHz LO instead of real VCO. This configuration costs less than $1 instead of $10 price range for VCO. Delta range of 27MHz frequency is +/- 1KHz. Control loop is closed at host CPU. After power up or channel change host CPU performs PI (proportional-integral) digital tracking algorithm which is fast enough to drop start up '27 MHz' LO close to uplink encoder 27MHz frequency. In order to minimize fast frequency transitions later we use Moving Average algorithm based on last 4 samples.

Slide #25

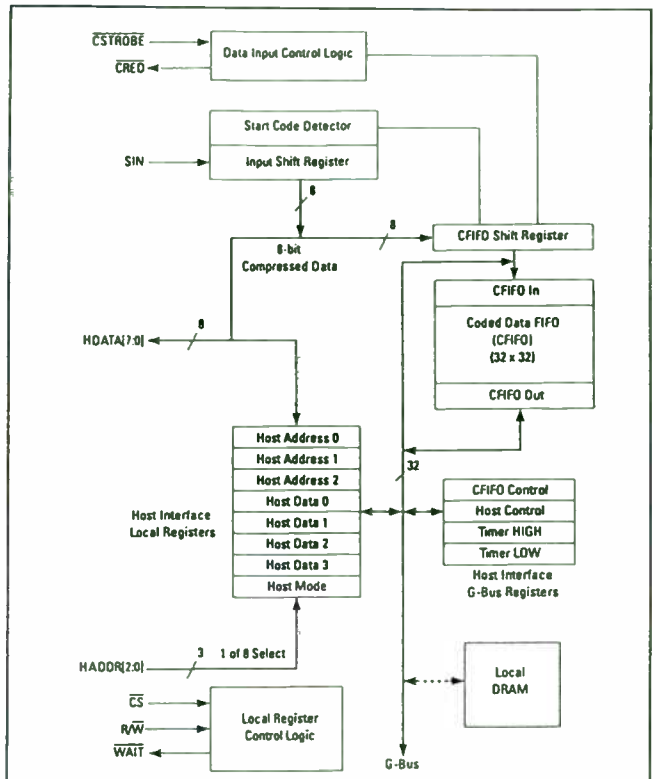


Fig 16: Structure and Host Interface of CL9100 MPEG-2 Video Decoder

Slide #26

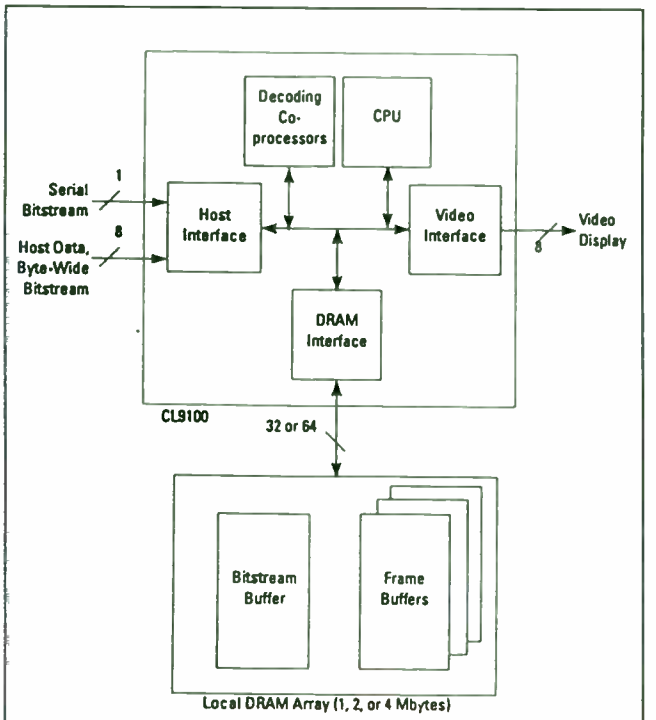


Fig 17: Video Memory Interface of CL9100 MPEG-2 Video Decoder

Internal structure of CL9100 video decoder is shown at Fig. 16. Fig. 17 shows interface to 16 Mbit DRAM used as video buffer and OSD overlay. Main features are:

- MPEG-2 Main Level @ Main Profile decoding
- MPEG-2 Main Level @ Simple Profile with dual prime mode
- ISO/IEC 11172 & ISO/IEC 13818 compatible
- Error detection and concealment
- Closed Captioning User-Data Field extraction
- Audio / Video synchronization using PTS embedded in an FIFO buffer or in an user-data field of picture header
- Internal 90KHz System Time Clock (STC)
- Decodes MPEG-1 & MPEG-2 bitstreams up to CCIR 601 resolution of 720x480 @ 30Hz for NTSC or 720 x 576 @ 25Hz for PAL.
- Horizontal resampling and vertical resampling
- Pan-and-scan for 16:9 video source
- Supports conversion of 24Hz film rate

Sustained video data rate of 16 Mb/s @ serial mode 25 Mbit/s peak rate or 80 Mbit/s parallel peak rate.

- On chip DRAM controller supports 16 or 32 Mbit DRAM organized as 256K x 16
- Eight-bit interface to host CPU
- 27MHz input clock frequency for main clock and video pixel clock.
- Supports MPEG2 high-level command interface (Reset, Play, Pause, Freeze, New Channel,Scan, Fast Forward, Single Step, Slow Motion and Block Write commands for simple operation).

As a RISC based video decoder CL9100 requires a downloading of approximately 47KBytes microcode for executing inputting, decoding and displaying processes. Inputting process transfers data from on-chip FIFO to the bitstream buffer in the DRAM MPEG-2 decoding process includes VLC decoding, dequantization, inverse DCT, motion compensation, error concealment and picture storing in frame buffers. Displaying process sends data to the video interface in YUV format towards color decoder.

Slide #27

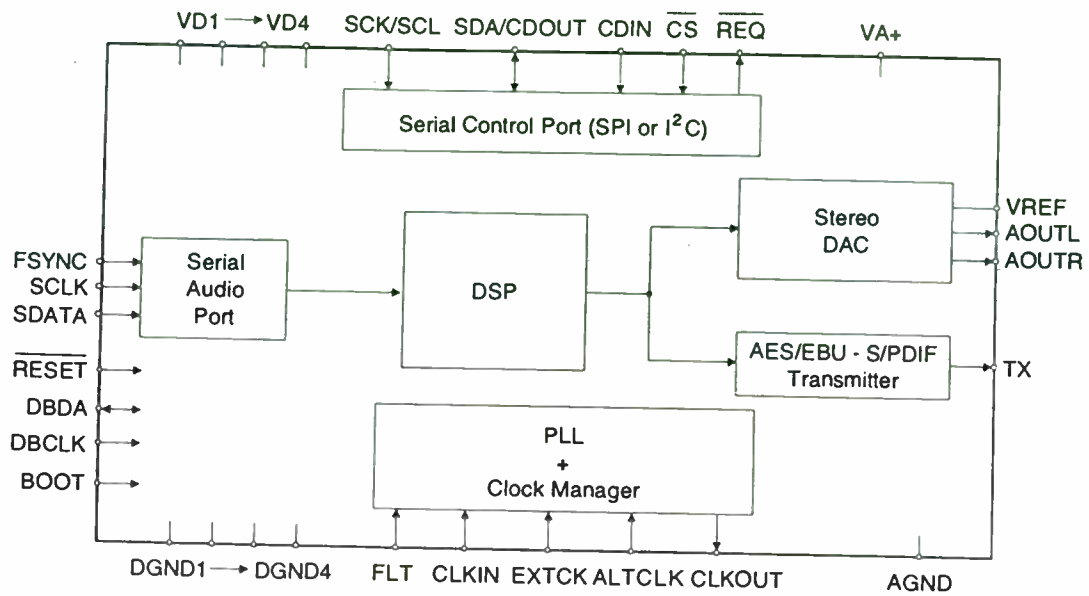


Fig 18: Structure of audio decoder

As the block diagram at Fig. 18 shows Crystal Semiconductor CS4920A audio decoder is DSP based audio subsystem with integrated CD quality stereo Digital-to-Analog Converter, programmable PLL clock multiplier, an audio serial input port, SPI or I²C serial control port and an AES-EBU - S/PDIF compatible digital audio transmitter.

The DSP core requires downloading of approximately 18KBytes microcode for MPEG layers 1 & 2 and Dolby AC-2 algorithms. The DSP engine has a 24-bit fixed point data path 4K words of program RAM and 2K words of data RAM. The execution unit has a 48-bit accumulator only. On-chip ALU typically reads instructions from program memory, operands from data memory and returns results back to data memory. For 44.1 KHz sample rate DSP engine has up to 16.9 MIPS. During playback synchronization of audio and video could be achieved by using a few methods:

- *Retrieving audio PTS* from CS4920A to the host, comparison with internal STC and forcing video decoder to skip or repeat a frame.
- *Video slaved to audio* requires initialization of STC counters in audio & video decoders with a first PCR value from transport stream. At every frame (every second VSYNC interrupt) host has to read CS4920A internal PCR counter & write this value to video decoder PTS FIFO buffer. Simultaneously CS4920A will self-synchronize by using MPEG1 Packet stream or MPEG2 PES
- *Independent Audio / Video Synchronization* requires initialization of STC counters in audio and video decoder from a common time-base, usually first PCR from a transport stream, extraction of video PTS samples from transport packet by transport demultiplexer and write of this value to the video decoder FIFO buffer by host CPU. CS4920A extracts audio PTS from MPEG-2 PES stream and synchronize itself.

Bt9104 NTSC color decoder generates and outputs HSYNC (horizontal sync) and FSYNC or frame sync control strobes to video decoder and reads 8-bit YCrCb pixels. The 4:2:2 YCrCb data is demultiplexed & 2x upsampled to 27MHz. Chroma and Luma data are lowpass filtered and modulated. NTSC analog composite video, luminance (Y) and chrominance (C) are outputs from color decoder.

For data transfer from receiver to subscriber management system (SMS) we use Rockwell ATL224 2400bps telephone modem. It supports V22.bis standard and contains 8-bit parallel bus interface to host microcontroller. Internally, it has 16C450 PC uart compatible register set.

Software requirements for satellite receiver:

1. Physical interface to the hardware consists of:

- QPSK interface control via 9600 bit/s async link This achieves tuner control, Low Noise Block-downconverter Horizontal / Vertical Control, Viterbi & FEC initialization and querying.
- Serial async 9600 bit/s communication link to infrared decoder and LED display (under local control of Motorola 6805C4 microcontroller).
- MPEG-2 transport demultiplexer, video & audio decoder microcode downloading, initialization and polling.
- Flash memory control.
- Telephone line detect and modem control.
- Conditional access system control.
- I^2C communication channel to color decoder.
- Direct read / write access to smart card.
- One milliseconds timer interrupt service processing for housekeeping jobs and interrupt servicing for serial ports, modem transport demultiplexer (for PCR and PTS processing), video & audio decoder interrupt processing.

2) Currently, our software consists of hardware initialization phase, interrupt servicing and main loop, written in C and assembler. Channel memory of our satellite receiver is built in flash memory by acquiring subset of MPEG-2 PSI & DVB SI tables:

- MPEG-2 Program Association Table (PAT)
- MPEG-2 Conditional Access Table (CAT)
- MPEG-2 Program Map Table (PMT)
- DVB Network Information Table (NIT)
- DVB Service Description Table (SDT)
- DVB Bouquet Association Table (BAT)
- DVB Time and Date Table (TDT)
- DVB Running Status Table (RST)
- DVB Stuffing Table (ST)

System software supports next subset of MPEG-2 and DVB descriptors:

- MPEG-2 Conditional Access Descriptor
- MPEG-2 ISO 639 language Descriptor
- MPEG-2 Private Data Indicator Descriptor
- DVB Stream Identifier Descriptor
- DVB Network Name Descriptor
- DVB Satellite Delivery System Descriptor
- DVB Country Availability Descriptor
- DVB Linkage Descriptor
- DVB Service Descriptor
- DVB Service List Descriptor
- DVB CA Identifier Descriptor
- DVB Telephone Descriptor
- DVB Bouquet Name Descriptor

For total definition of 150 channels receiver memory organized in flash memory we need about 28 Kbytes. PAT, CAT, PMT and NIT tables are acquired every 30 seconds. If there is a change of version number host CPU starts new & complete acquisition process to fill flash memory with new data. Tee-Comm's EPG is organized as proprietary service scheduler and descriptor and has format of private data table with long section syntax. It describes current network services and programs in a near future (next 7 days). Complete operational interface and GUI is based on this EPG-Electronic Program Guide. It is transferred and stored in RAM memory in compressed form. It typically needs about 350KBytes of storage RAM space. Refreshment of EPG data is once per day.

3) Very convenient Operational and Graphical User Interface enables volume control, channel change by UP / DOWN keys, channel change by direct access, channel change by GUI menu system and by EPG on screen display and IPPV channel change.

During channel change alpha blending feature of CL9100 OSD overlay is used for transparent on-screen display of current program (short description). During installation of satellite dish OSD system graphically shows signal strength. *Three Carrier Automatic Search Algorithm* is used in order to get first transport stream. After that receiver starts self-programming cycle to complete channel memory.

Part 4: Achieved Results and Conclusion

To obtain synchronization between audio and video proper presentation time stamp software handling is necessary. To keep this synchronization for long time and to prevent video buffer overflows and underflows in video decoder DRAM memory it is important to have proper control of 27MHz PCR transport stream samples. Software on host CPU executes next PI digital tracking algorithm:

```
delta_pcr(k) = Kp * ( delta(k) - delta(k-1) ) +
                Ki *  delta(k) ;                    (2)

pcr_control(k) =pcr_control(k-1) + delta_pcr(k) ; (3)
PWM = pcr_control(k) ;                              (4)
delta(k-1) = delta(k) ;                             (5)
pcr_control(k-1) = pcr_control(k) ;                 (6)
```

where:

delta(k) is current difference between PCR value and STC value in CL9110 demultiplexer.
delta(k-1) has same meanings but for previous iteration.
delta_pcr(k) is current delta in control value of applied control quantity.
pcr_control(k) is control quantity.

PWM is pulse width modulation register in CL9110 whose output is used to set up output PWM pulse. After lowpass filtering it creates DC control voltage which is applied to 27MHz VCO (voltage controlled oscillator). In equations (5) and (6) we save control parameters for next iteration. Kp is coefficient of proportional action and Ki is coefficient of integral action which supposes to eliminate long term offset. This algorithm is executed every PCR interrupt (depends of PCR samples frequency, in case of our uplink encoder approximately 30 times per seconds)

For Moving Average Algorithm we use:

```
for (i=0; delta_average=0; i<LOOP_LEN-1;  i++)
 {
  delta_array[i] = delta_array[i+1] ;
  delta_average += delta_array[i] ;
 }

delta_array[LOOP_LEN - 1] = delta;
delta_average += delta ;
delta_average >>= LOOP_LEN;
PWM = delta_average;
```

where:

delta is current difference between PCR and STC of CL9110 transport demultiplexer chip.

LOOP_LEN = 4; Number of samples for averaging.
delta_array[LOOP_LEN] is global array.
delta_average is control value stored in variable.
PWM is control register in CL9110 whose value generates pulse width modulated control signal used for VCO correction.

In previous algorithm we first shift the global array and apply current delta to the last element of the array. Right shifts corresponds to the division by LOOP_LEN (i.e. 4, or 8 etc.). By this method we calculate average value of last LOOP_LEN = 4 PCR samples and generate appropriate PWM signal and after lowpass filtering DC voltage for voltage controlled LO.

Figure 19 shows long term frame jitters and burst frequency error. Frame jitters are very low and satisfy our need for smooth frequency transitions. Burst frequency error could be better (it has to be less than 10Hz). This could be accomplished by more precise tracking. This measurement was done by Hewlett Packard VM700 Video Measurement Set.

Slide #28

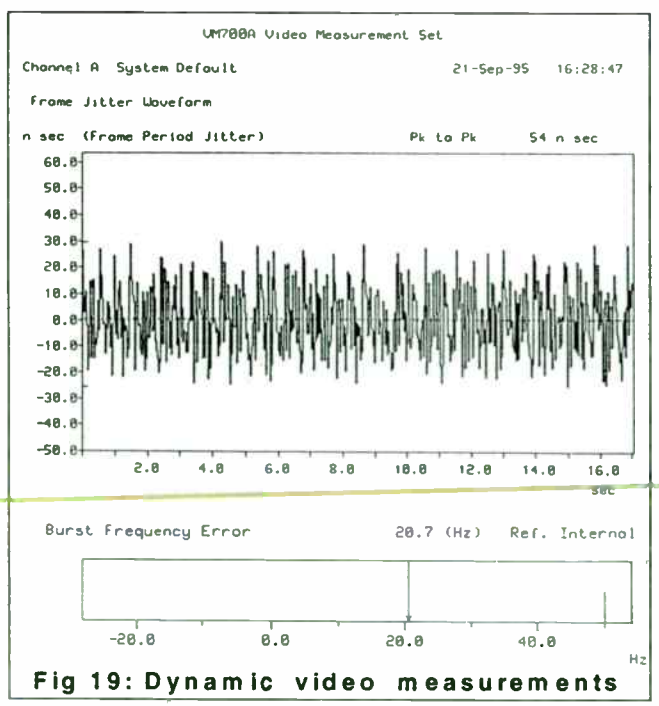


Fig 19: Dynamic video measurements

Slide #29

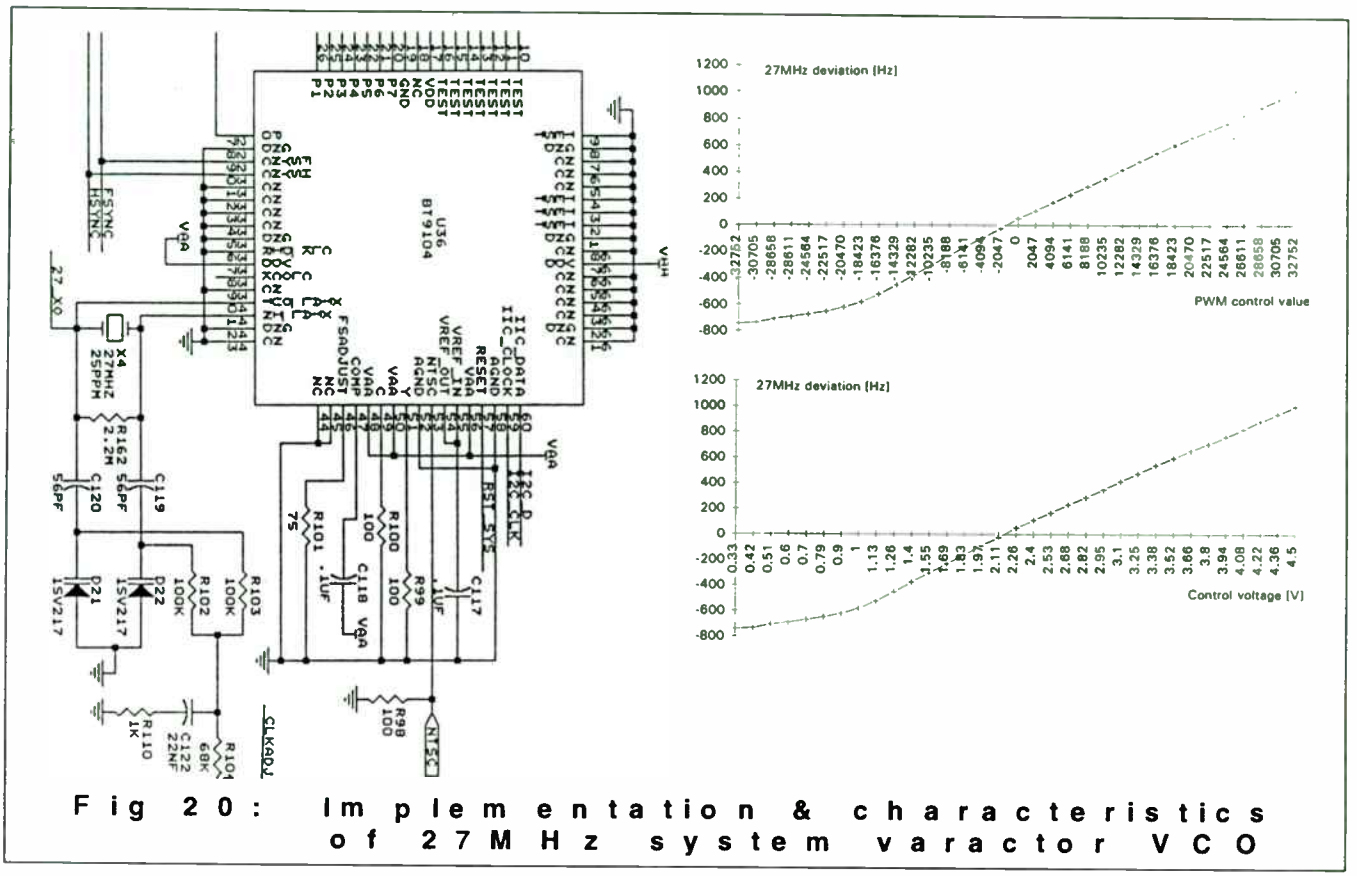


Fig 20: Implementation & characteristics of 27MHz system varactor VCO

At fig. 20 typical characteristic of system 27MHz voltage controlled oscillator (VCO) built around Bt9104 color decoder is shown. As we can see function of frequency change vs. PWM control value (or control voltage) is linear in range from -600Hz to +1000Hz around -2047 which correlates to 2.2 V.

When the control value drops below -20470 which is 0.93V applied voltage to varactor diodes is not enough to produce linear change of its capacitance. Still, even in the range of small control voltages delta of frequency can be modeled by two segment linear approximation.

Graphical User Interface (GUI) is composed of linked lists of submenus. Selection is made via IRED remote controller for audio volume control, or channel change, Electronic Program Guide or EPG channel selections and Impulse Pay Per View selection. EPG program choice is shown at Fig 21.

Slide #30

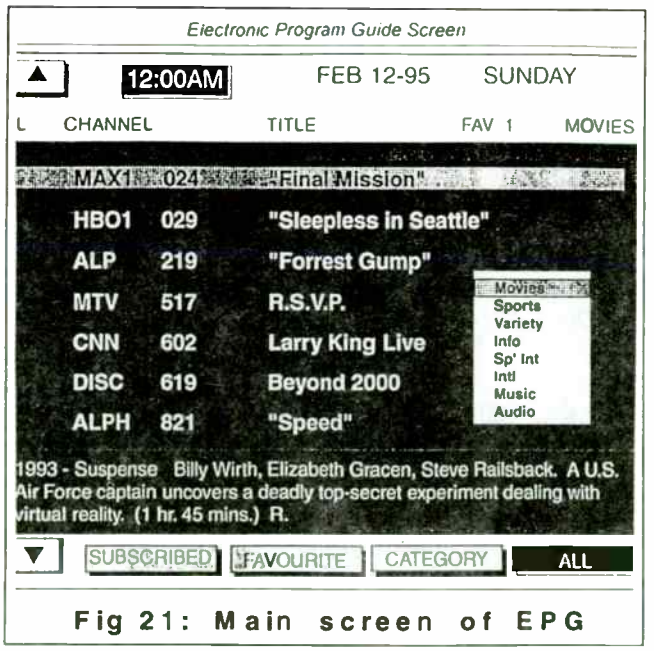


Fig 21: Main screen of EPG

Conclusion:

In this article typical organization and common building blocks for all digital, MPEG-2 DVB compatible satellite receiver with variable rate QPSK RF front-end were illustrated & studied. Future in home entertainment systems is in MPEG-2 open standard systems. Also, due to compatibility with ATM networks we believe that MPEG-2 could play major role in multimedia and computer markets during next 10 years. Fact that our DBS satellite receiver uses variable rate QPSK front-end creates new opportunity in comparison with currently available fixed rate systems. It could adopts new reality (frequencies, symbol rates, etc.) in various satellite networks. Currently, it supports four networks and 150 channels. Deployment on North American market we expect during 1996.

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Acknowledgments:

I would like to thank Mr. David Lester, director of engineering at Tee-Comm Electronics for his continuous help during 1994 - 1995. Also special thanks to other team members: Rudy Heidebrecht for PCB design, Leo Dalupan for receiver prototype construction, Dragan Milanovic and Ljiljana Lazic for OSD software development, Simpson Lam for telephone modem hardware & software design, Shao Zhan for power supply and video filter design, Goran Kundacina for in-receiver selftest software design and test workbench design, Sam Sayyah and Mirjana Matijevic for PSI / SI table fetching & processing software design, Nabil Kanaan and Shawn Saleem for system integration of uplink video & audio compression equipment and Martin Schuman for CA control system development. Very special thanks to James Chan & Benjamin Tsai of C-Cube Microsystems for CL9110 / CL9100 system support and Dan DeHaan & Glen Roberts from TV/COM International for CAM integration.

Biography:

From July '93 Branko Kovacevic works for Tee-Comm Electronics . As Senior R&D Engineer he is in charge of development of *Star * Track* generation of analog and DTH all digital consumer satellite receivers. In the area of analog receiver design his main achievement is *Star * Track 850* PAL / NTSC international, multipurpose receiver for European and Far East market. In the field of digital receiver design his main research interests are applications of MPEG integrated circuits.

Branko Kovacevic received MSEE & BSEE degree in electronics from the University of Belgrade, Yugoslavia, in 1994 & 1988, respectively. From September 1988 until June 1993 he worked in Institute "Mihailo Pupin" in Robotics and Mehatronics departments. As R&D Eng. he was involved in design of PUMA-560 robot controller & a few microprocessor based control mechatronics systems. He has extensive experience in PL/M , C and assembly languages. He is the author of three articles about SCADA embedded systems published in ETAN conferences in Yugoslavia.

A New Audio DSP Processor for Consumer Analog Satellite Receivers

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Abstract

Nowadays market of analog satellite set-top boxes contains an increasing number of various types of home entertainment and professional satellite receivers but only a few of these devices are built in a fully integrated form. Cost reduction usually means usage of transistors and OPAMPs as active elements for video and audio sections. In this paper architecture and features of our new satellite receiver with low cost all digital audio section are presented.

Our receiver is built around Intel 8097BH 16-bit microcontroller and ITT - Intermetal MSP3410 satellite audio subcarrier DSP. EPROM based channel memory contains description of video and audio frequencies for 600 channels and 42 satellites.

This paper outlines main hardware functional building blocks and basic software applications for audio processing via I^2C interface.

Key Words

TV-sound-processing, automatic gain control, demodulation of FM mono TV sound, two carrier FM systems, digital NICAM standard, Automatic Search For Audio (ASFA), high deviation mono FM.

Wireless 96
Fourth Wireless International Symposium

Slide #1

A New Audio DSP Processor for Consumer Analog Satellite Receivers

WIRELESS
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Microwaves & RF

Slide #2

- **Part 1: System Block Diagram**
- **Part 2: Structure of Audio DSP**
- **Part 3: Software Requirements**
- **Part 4: Implementation and Conclusion**

1. 1 Introduction

MSP3410 as a single-chip Multistandard Sound Processor developed by ITT Semiconductors can be used in satellite receivers, analog and digital TV sets and video recorders. It accepts analog audio signals in baseband and at intercarrier positions. It is fabricated in 1.0 micron technology and we use it in 68 pin PLCC package.

MSP3410 has ability to simultaneously perform digital demodulation and decoding of NICAM coded TV stereo sound and demodulation of FM mono TV sound or German or (and) Korean two carrier FM TV sound. Demodulation of AM sound carriers is seldom used but for FM carrier detection is used for calculation of carrier strength in ***automatic search algorithm***. Total control of the device is achieved by software emulated I^2C bus at two I/O pins of INTEL 8097BF (8096 family) host microcontroller.

1.2. Basic Features

- Three analog baseband stereo SCART inputs, one analog mono input for AM sound and stereo satellite audio subcarrier IF inputs.
- Stereo loudspeaker, headphone and two SCART outputs with I/O switching matrix (20Hz - 20kKHz SCART to SCART bandwidth).
- Automatic Gain Control (AGC) in the range from 0.14V to 3V for analog inputs.
- On-chip stereo A/D converter for satellite IF inputs, S/N ratio > 85dB
- On-chip programmable demodulation and filtering.
- One crystal source of 18.432MHz.
- Pay-TV for NICAM receivers.
- +/- 360 KHz high deviation FM mono mode.
- digital I/O for DSP section via S-bus.
- 50us, 75us, J17 and Wegener Panda 1 all deemphasis system software selectable.
- Digital baseband processing of volume, bass. treble, loudness, pseudostereo and basewidth enlargement under host CPU control.
- Wide audio bandwidth for FM audio signals (20Hz - 15kHz, +/- 1dB).
- Two pairs of 4-fold oversampled D/A converters for loudspeaker and headphones outputs with 1.4 Vrms max.
- One pair of four-fold oversampled D/A outs for two selectable pairs of SCART outputs with 2 Vrms max. output level.

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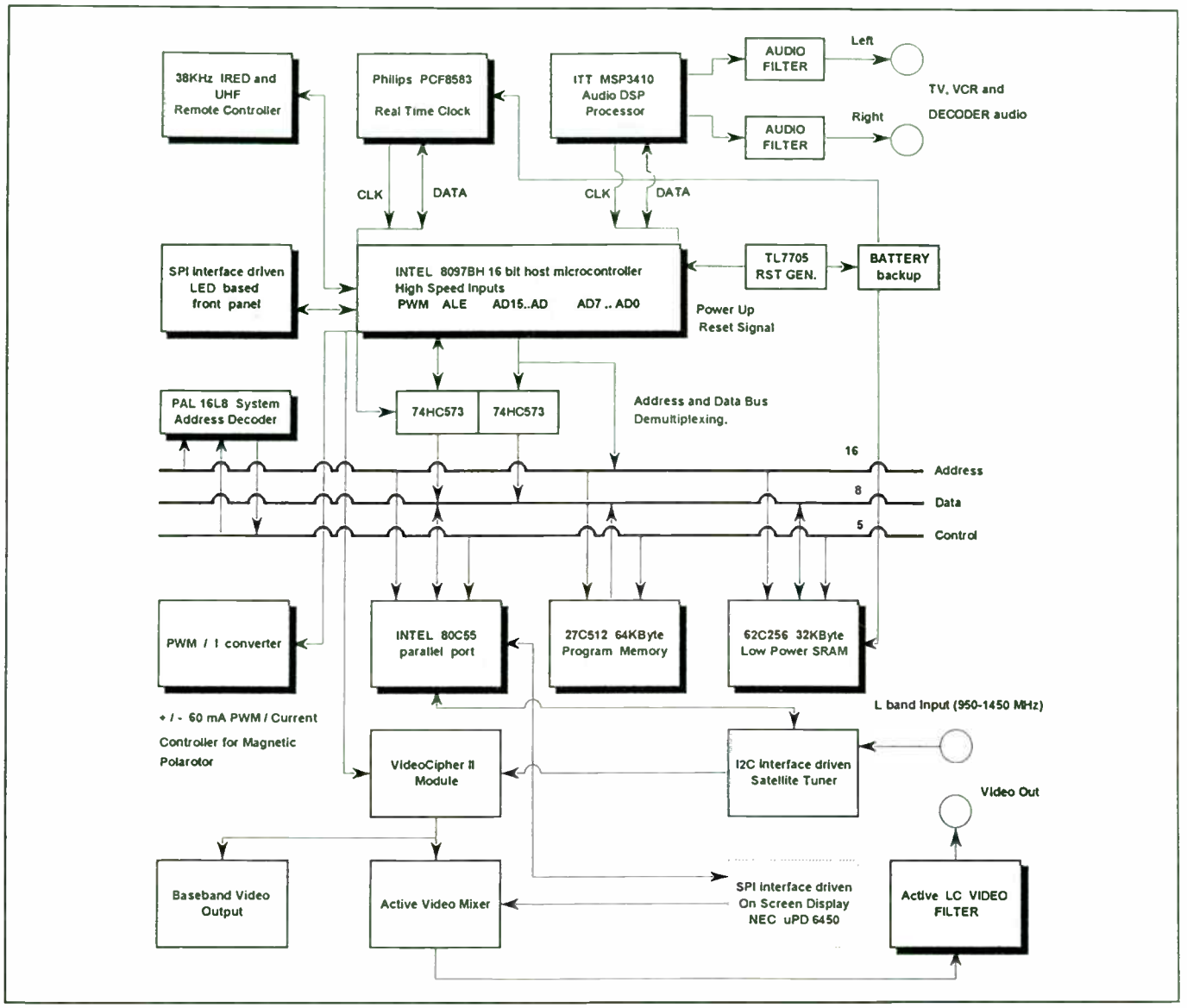

1.3. Main Block Diagram

Fig 1: System Block Diagram

Block diagram of ***Star*Trak 850E*** satellite receiver is shown at fig. 1. There are two separated software emulated I^2C buses in a system. One is used for real time clock / calendar with battery backup and for control of satellite tuner. Another is for multibyte I/O transfers for MSP3410. Host microcontroller is 16-bit INTEL 8097BH used in 8-bit bus interface mode. Run time application code is stored in 64KBytes EPROM (27C512). From total 64KB address range of host MCU 56 KBytes are used for application program, 2 KBytes are used for system RAM, 2 KBytes are allocated for I/O page and 4 KBytes for 32 KBytes low power SRAM with battery backup and paging control from system PAL 16L8 which also performs address decoding. This SRAM contains 600 channels receiver memory and table description of satellites. In system parallel I/O ports extension is done via INTEL 80C55 parallel bus I/O device.

Host CPU controls 4 digits LED display via SIPO shift register. Decoding of incoming IRED and UHF remote pulse train is also done by host CPU. Receiver SRAM memory to memory transfer is available via 19.2 Kbit/s RS-232 async serial port.

2.1. Typical application of MSP3410

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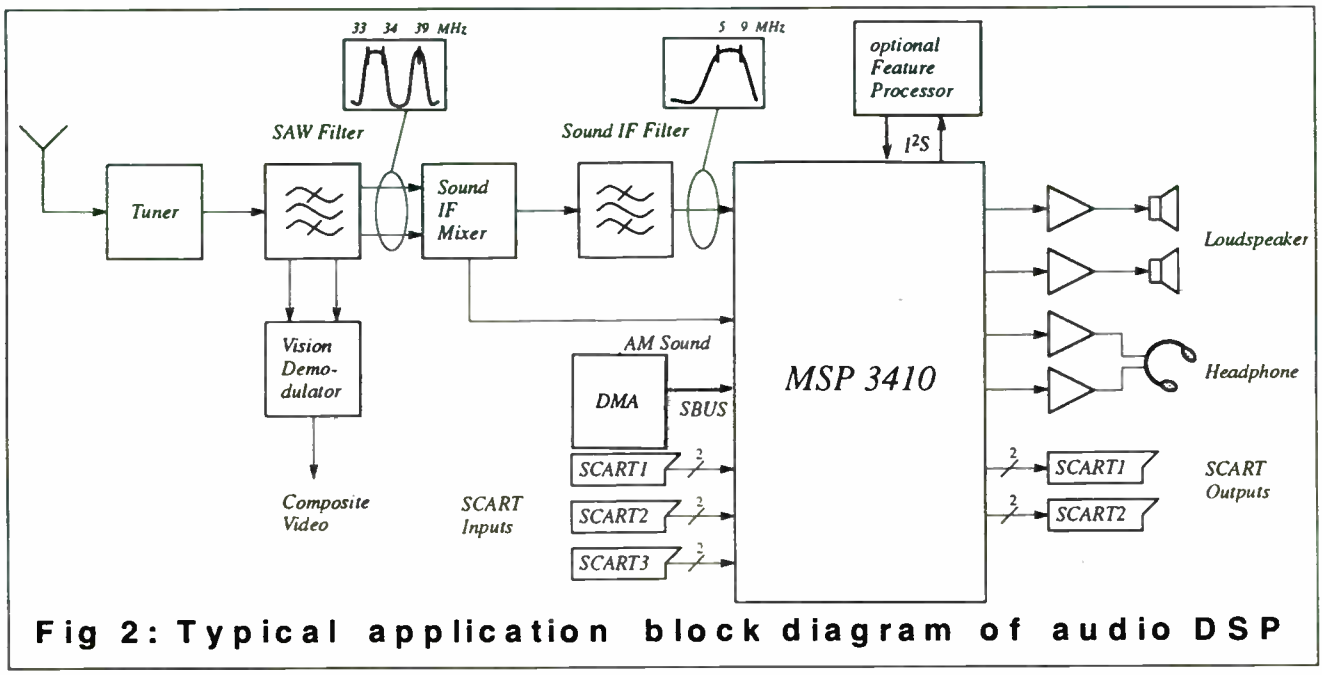

Fig 2: Typical application block diagram of audio DSP

There are a few TV systems where two high quality digital sound channels can be added to one existing FM channel. So called *Near Instantaneous Companding System (NICAM 728)* is used with ***Differential Quadrature Phase Shift Keying*** (DQPSK). In that case there are three channels available:

- Digital NICAM A and NICAM B which are typically used for stereo or dual language transmission
- Analog FM mono sound may contain same or different audio service.

Typical European TV standards are:

- **B/G** with sound carriers at 5.5 / 5.74 MHz and FM stereo sound modulation for PAL used in Germany.
- **B/G** with sound carriers at 5.5 / 5.85 MHz with FM mono / NICAM sound modulation for PAL in Spain and Scandinavia.
- **L** with sound carriers at 6.5 / 5.85 MHz and AM mono / NICAM for SECAM in FRANCE.
- **I** with sound carriers at 6.0 / 6.55 MHz with FM-mono / NICAM for PAL used in UK.
- **M** with sound carrier at 4.5MHz and FM mono for NTSC used in USA and Canada.
- **D & K** with FM-mono sound carrier at 6.5 MHz for SECAM used in Russia.
- **Satellite audio** with FM mono sound carrier at 6.5MHz or FM stereo sound with carriers at 7.02 / 7.2 or 5.58 / 5.76 or 7.38 / 7.56 MHz used in Europe and North America, supported by our ***Star * Track 850E*** satellite receiver.

Typical NICAM 728 audio coding method uses 32KHz sampling frequency for 2 channels with 14 bit / sample initial resolution and near instantaneous companding with compression to 10 bits/sample in 32 samples (1ms) blocks. Used preemphasis is J17. Transmission rate is 728Kbit/s.

2.2. Internal structure of DSP CPU

Slide #5

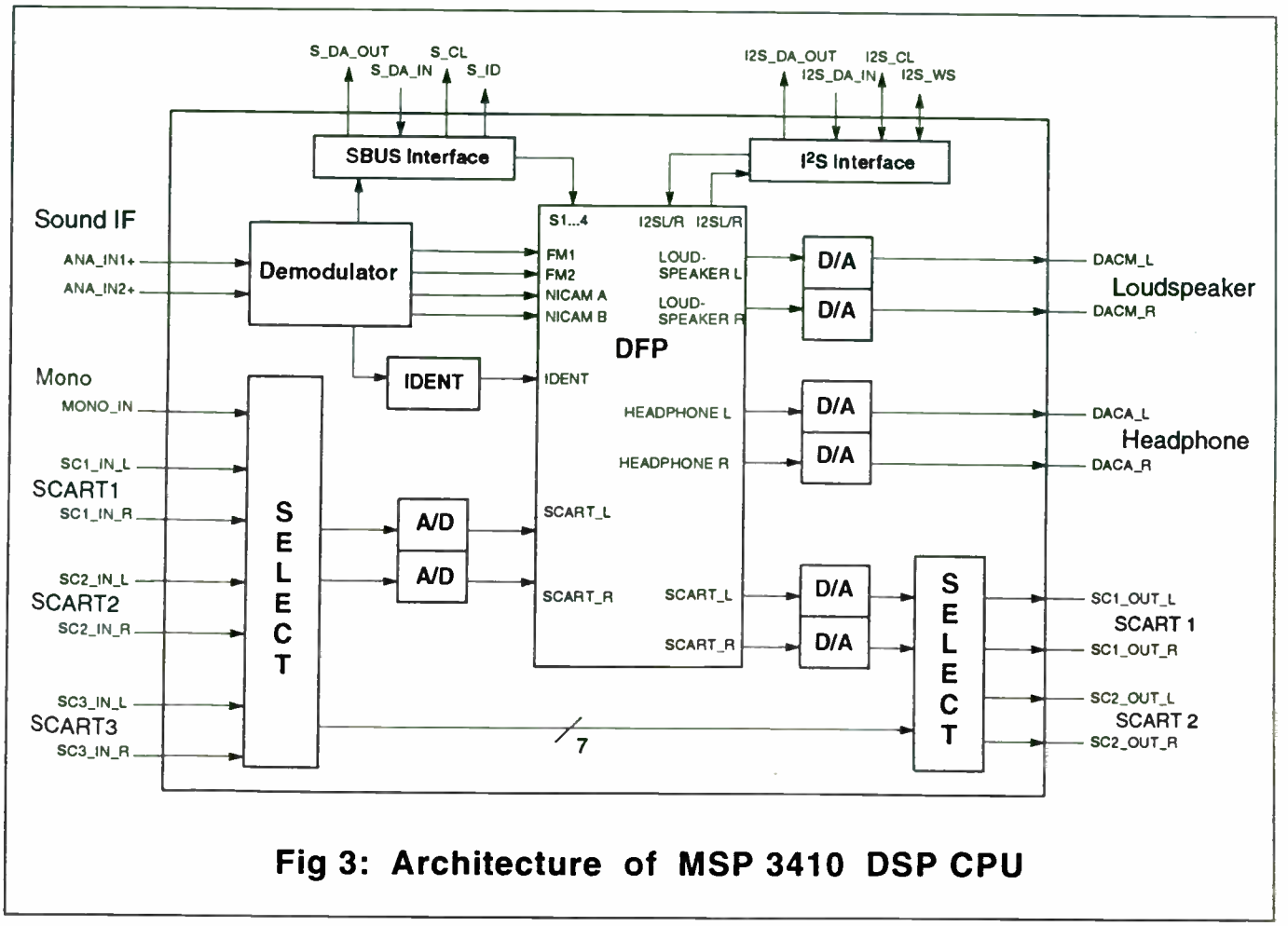

Fig 3: Architecture of MSP 3410 DSP CPU

MSP3410 audio subcarrier processor whose internal structure is shown at Fig. 3 consists of:

- Analog section with stereo A/D converter, input multiplexer for channel selection and six D/A converters.
- Demodulator and decoder section.
- Digital sound processing unit (DSP) for audio baseband processing.

Integrated A/D converter for satellite IF signals is flash converter whose output can be used for analog AGC. Also, there is possibility to use fix but setable gain. AGC provides optimum level for A/D for a wide range of input signals.

Analog I/O section offers a wide range of switching facilities for 3 pairs of SCART inputs and 2 pairs of SCART outputs.

The switches are directly mapped into one of internal registers of MSP3410 and are under software control of host CPU.

During the initialization sequence of MSP3410 host microcontroller may select non default I/O switch configuration.

Slide #6

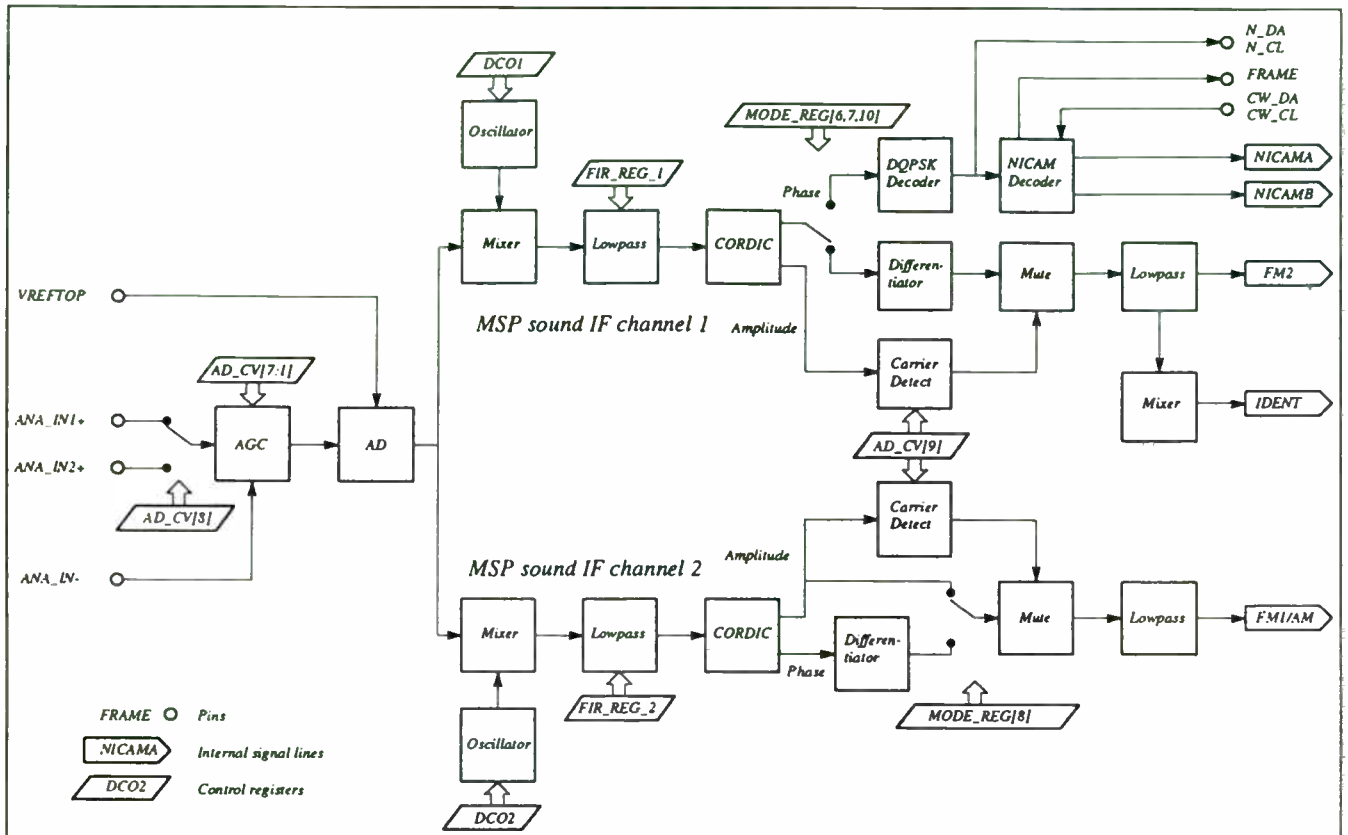

Fig 4: Structure of internal demodulator

Internal demodulator is used to process digital audio stream coming from A/D converter at a frequency range from 0 to 9 MHz or to support two different audio sources:

1. NICAM for channel 1 or FM mono for channel 2

2. FM2 for channel 1 and FM1 for channel 2

which may be shifted into baseband position. Numeric controlled oscillator is under CPU control which can select the frequency of wanted carrier. Linear digital FIR filters with programmable filter coefficients are lowpass decimation filters.

CORDIC processor block transforms filtered IF sound signals from Cartesian into polar format to generate phase and amplitude of audio signals.

Amplitude information is used for AM signal processing and the phase I nformation for FM and NICAM (DQPSK) demodulation. FM demodulation is performed by differentiating the phase output of CORDIC block. Demodulated FM and AM signals are lowpass filtered and decimated to a 32 KHz sampling frequency. At the output DSP processed signals have bandwidth of 15 KHz.

Original NICAM bitstream is available at the output of DQPSK decoder. This block uses Frame Alignment Words to synchronize and lock to the NICAM frame structure. Also this block is used to descramble, deinterlive & rescale. Specific error correction and error concealment is done within this block. NICAM mode and bit error rate can be monitored by host CPU via I^2C bus. NICAM block decoder is not used in satellite receiver application.

Slide #7

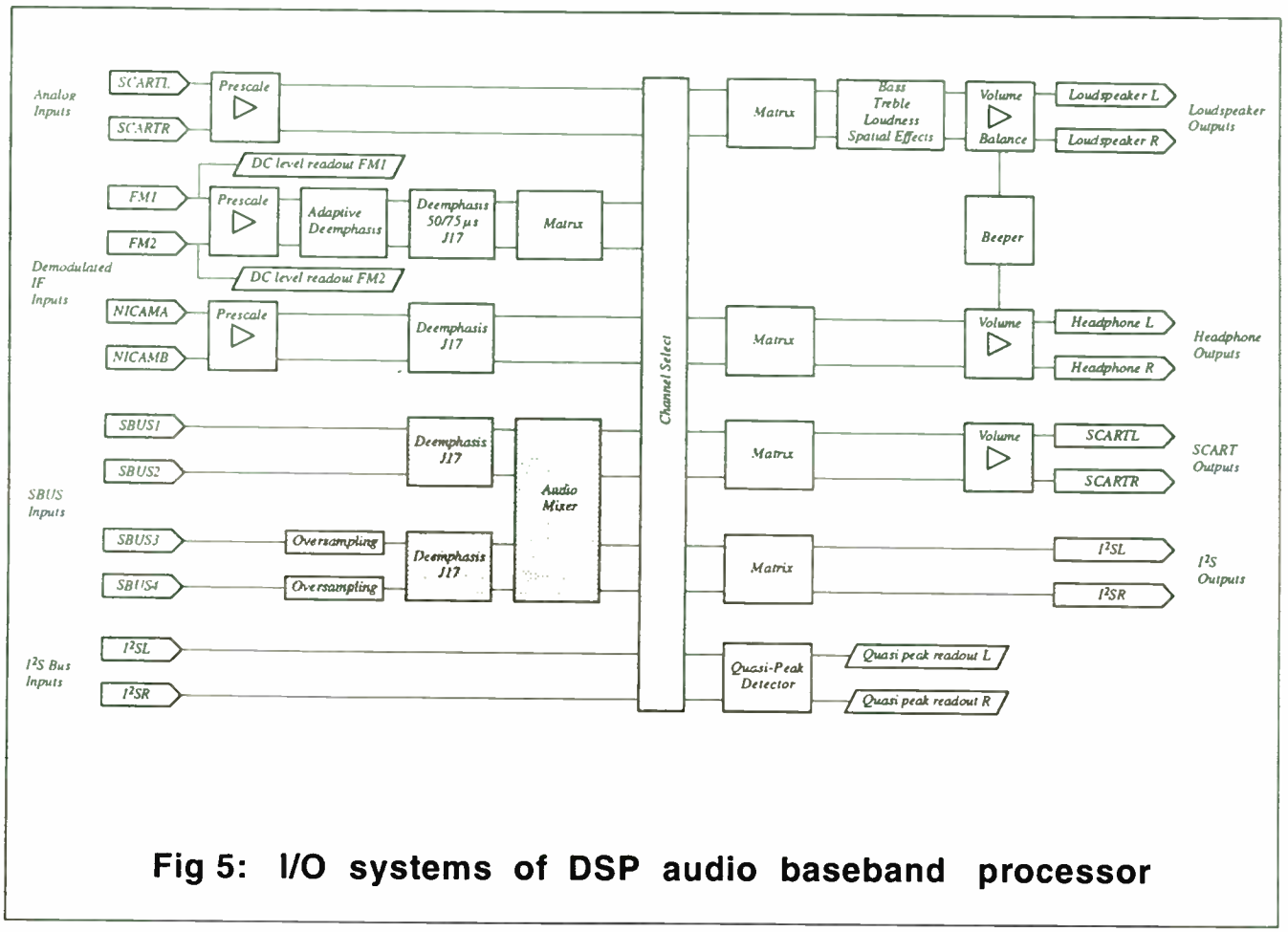

Fig 5: I/O systems of DSP audio baseband processor

Internal DSP processor is used for:

- ***Input preprocessing*** to prepare all input source signals in a form of standardized signals. This means volume and deemphasis adjustment and dematrixing.

- ***Channel selection*** for I/O distribution of all possible source signals to output channels and signal routing to external coprocessor for special effects by using ***I²S I/O***. External audio devices such as sound field processors, surround processors and graphic equalizers could be used.

- ***Channel postprocessing*** for volume control of main loudspeaker channel in the range from -94 to +12 dB, balance control between left and right channel in the range from 0.8 to 100%, individual bass and treble control of left and right channels in the range of +/- 12 dB, loudness control in the range from 0 to +12 dB and spatial effects over loudspeaker channel for *Stereo Basewidth Enlargement (SBE) or Pseudo Stereo Effect (PSE).*

Also DSP controls volume of headphone channel in the range from -77dB to +12dB and volume of SCART channel in the range from 0 to +6 dB. All of these functions are under CPU control, which has direct access to various registers inside DSP module. FM volume prescale, FM matrix mode selection, FM fixed or adaptive deemphasis selection, I/O switch selector NICAM volume and deemphasis selection is under host CPU control.

MSP3410 has a squarewave beeper with CPU programmable frequency from 31 Hz to 1KHz for loudspeaker and headphone channels.

2.3. CPU Bus and Pay TV Interfaces

Slide #8

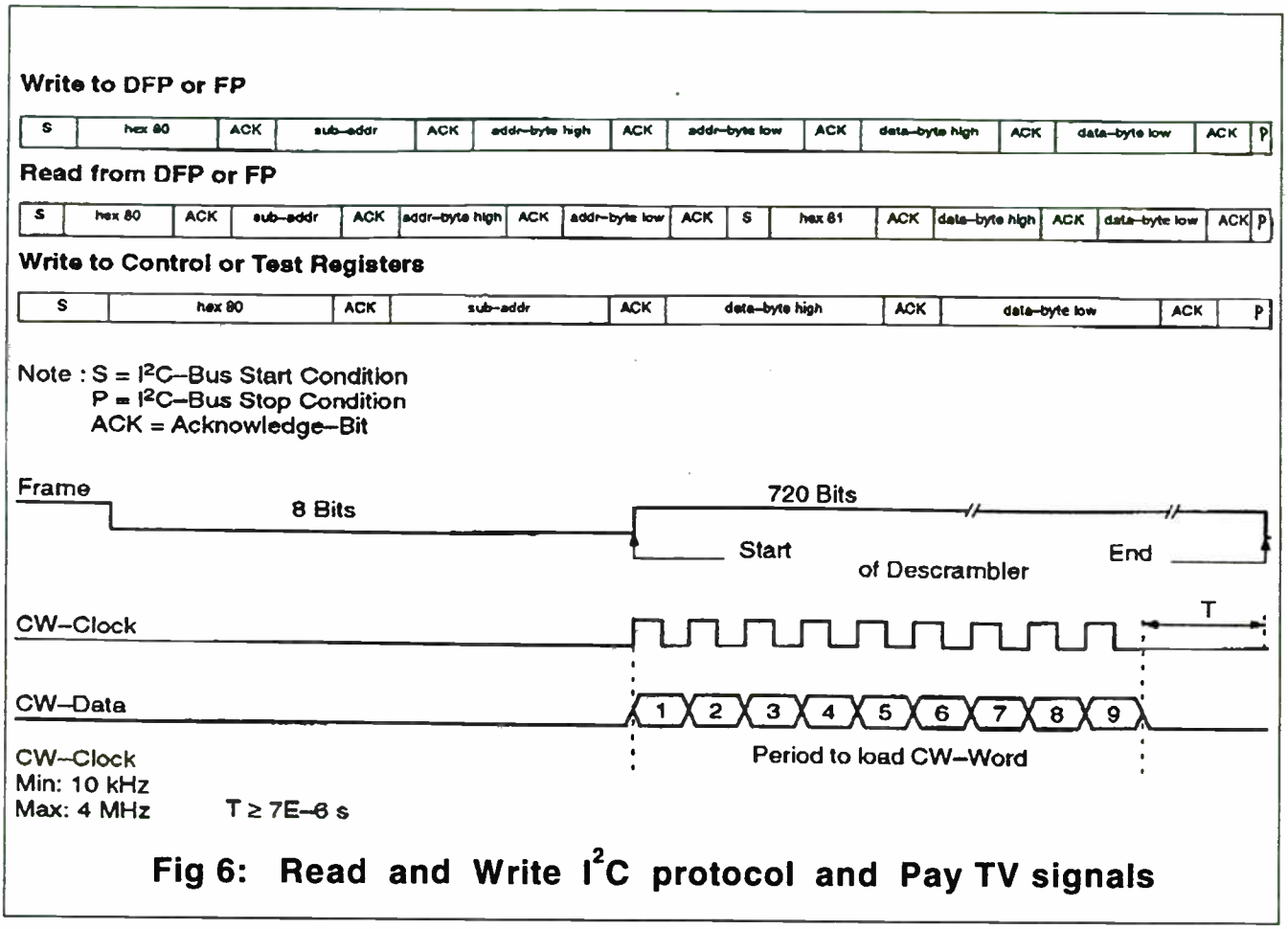

Fig 6: Read and Write I²C protocol and Pay TV signals

Host control of MSP3410 is possible by ***I²C Interface.*** Access to internal registers of MSP3410 is possible by subaddressing of FP (demodulator) or DFP (DSP unit) parts. I²C write addresses are 80 or 84H and 81 or 85H for reading, which are main addresses. Control register has subaddress zero, Test Mode uses subaddress 01H, FP module has write subaddress 10H and 11H as read subaddress, DFP module uses subaddresses 12H or 13H for I/O write or read operations.

One typical write cycle contains 4 or 6 bytes and read cycle contains 4 or 7 bytes.

Digital N Bus Interface has data and clock lines. Fix frequency of clock signal is 728KHz.

Input of digital NICAM sound can is via N Bus Interface, but NICAM stream is encrypted in typical PAY TV application. In that case external device loads 9-bit start sequence (descrambling key) via the two pins: ***CW_Clock and CW_Data*** at the beginning of high level of **Frame Signal.** This three lines interface could be used for one or multiple audio frames to initialize internal pseudo random sequence generator used for descrambling of system encrypted NICAM digital stream.

Three lines ***S Bus Interface*** enables input of digital data from other ITT family members (DMA2381). It consists of S_DA_IN for four channels per sampling cycle, 4.608 MHz S_CL clock and S_ID as end of sample marker.

Slide #9

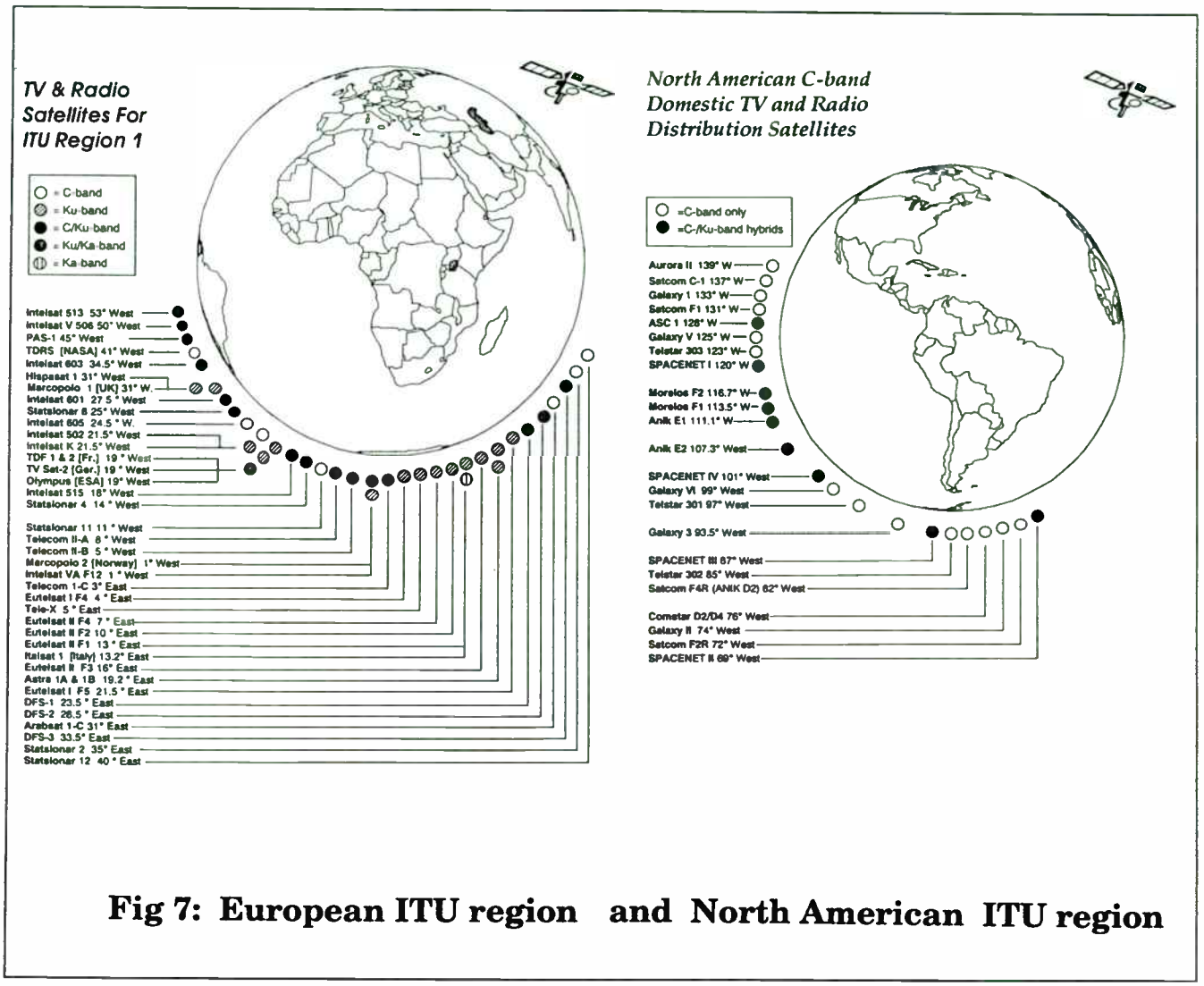

Fig 7: European ITU region and North American ITU region

Automatic Search For Audio (ASFA) is narowband FM carrier search method achieved by using AM demodulator for calculation of field strength of currently available FM carrier. After each incrementation of FM sound carrier frequency a field signal strength value is available at the DC level register. During this incremental scan CPU examines this local maximum and stops search algorithm at current maximum or performs a frequency sweep and memorizes frequencies of local maxima.

For the CD quality audio products delivered via satellite the race is still on. Most of the valuable udio services are based on ***Direct To Home***.Usage of audio DSP based processors in analog receivers and noise reduction techniques allows new and extended life of currently available analog satellite radio systems in competition against DOLBY AC-2 DOLBY AC-3, MUSICAM or DAB digital systems. With THD from analog input to SCART output of 0.01% , SNR of 96dB and crosstalk between left and right channels of -80dB max MSP3410 in our satellite receiver can compite against these new digital audio systems.

3. 1 Software requirements

Complete system software of our satellite receiver was written in PL/M - 96. This high level language is well optimized for 8096 family and it was developed by INTEL to support this family of 16-bit RISC like microcontrollers. We found very useful ability to allocate global or module variables in local in-chip RAM. This method uses 8 bit direct addressing thus saving program memory space and speeding run time execution of application code.

Embedded software is segmented in a few basic layers:

* ***Interrupt Response Drivers*** for high speed VideoCipher II Communication port, high speed input for UHF and IRED pulse trains from remote controllers, 1ms timer tick used for LED refresh and front panel key scan, high speed input for satellite dish actuator process and high speed output for mechanical polarotor or magnerotor control.

* ***Device drivers*** for system hardware resources.

* ***SRAM Data Base I/O drivers*** for satellite and channel memory.

* ***Menu Driven On Screen Display (OSD) System***

* ***IRED and UHV Remote Decoder Driver.***

* ***Satellite Dish Actuator Driver.***

* ***Men Machine Interface*** for satellite and channel selection and adjustment of various audio or parameters via front panel keys and infrared or UHF remote controller.

* ***Automatic Search for Audio*** at user request.

* ***Satellite and Channel Memory Data XFER*** via 19.2 Kbit/s async RS-232 data link.

* ***One Year Ten Events VCR Timer Driver*** based on Real Time Clock (PCF8583) Interrupt Signal.

Our software is based on initialization and main loop, interrupt and device drivers, text OSD navigator and synchronization via semaphores and mail boxes.

4. 1 Implementation

Figure 8. shows implementation circuitry around MSP3410 subcarrier audio processor and implementation detail of European SCART based back panel connections. For North American model we use only RCA connectors. All circuitry was done in two layer PCB board.

4. 2 Conclusion

In this article organization and specific building blocks for our Star * Track 850E analog satellite receiver were studied and illustrated. Special attention was emphesized on DSP based satellite audio processor for delivery of high quality audio channel over DTH satellite link.

Deployment on European and Middle East market started in second quarter of 1995. We expect delivery on North American market during 1996.

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Slide #10

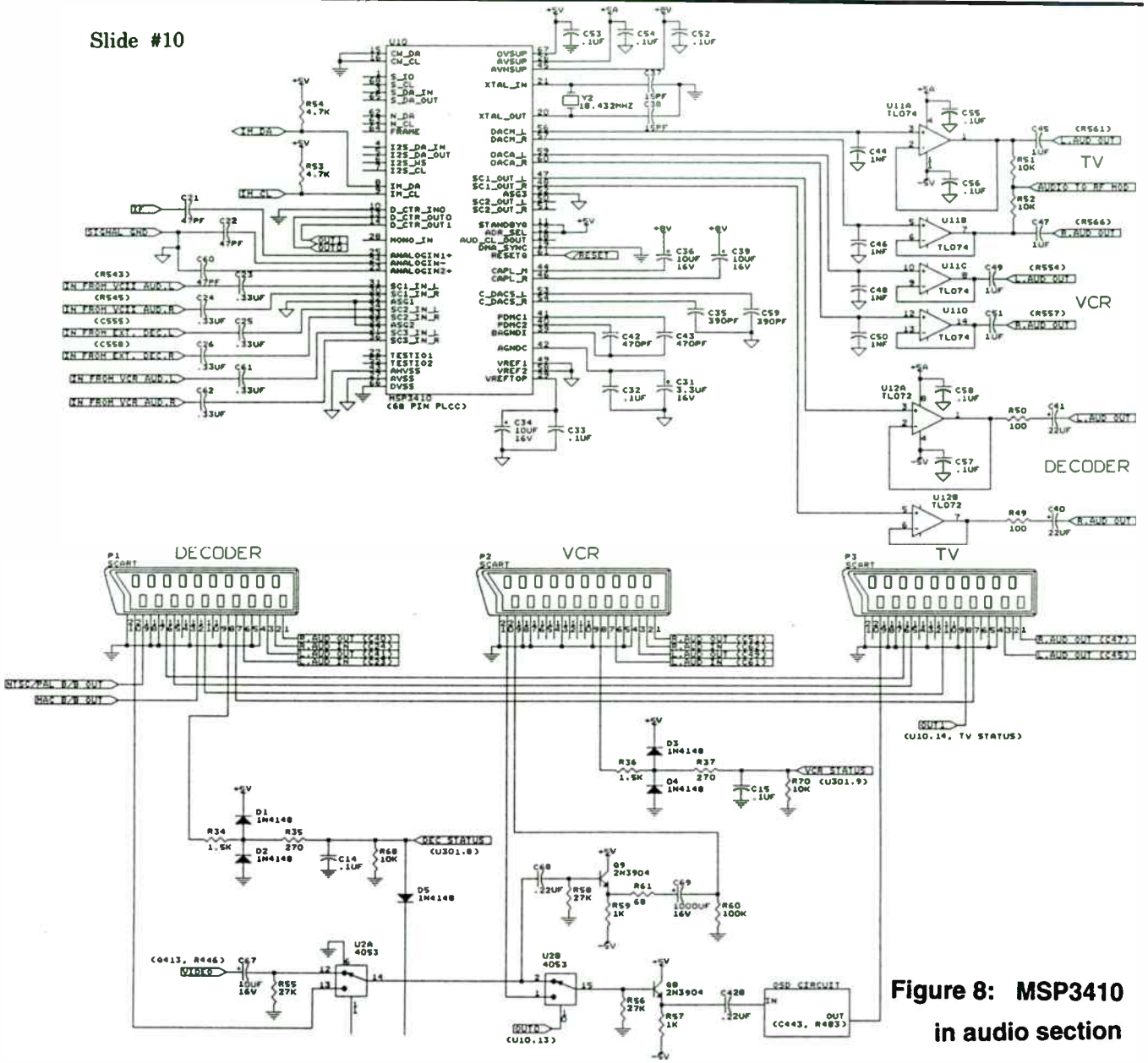

Figure 8: MSP3410 in audio section

Acknowledgments:

Very special thanks to Mr. David Lester, director of engineering at Tee-Comm Electronics for his continuous help during 1994. Also, I would like to thank to Mr. Rudy Heidebrecht and Mr. Volter Wan for receiver prototype construction and Mrs. Mirjana Matijevic for her cooperation in software development. Also, many thanks to Mr. Bogdan Dumitrache of ENCOM, Paris, France for testing of our Star * Trak 850E analog satellite receiver in European site during 1995.

Biography:

From July '93 Branko Kovacevic works for Tee-Comm Electronics . As Senior R&D Engineer he is in charge of development of *Star * Trak* generation of analog and DTH all digital consumer satellite receivers.

Branko Kovacevic received MSEE & BSEE degree in electronics from the University of Belgrade, Yugoslavia, in 1994 & 1988, respectively. From September 1988 until June 1993 he worked in Institute "Mihailo Pupin", Belgrade, Yugoslavia.

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AUTOMATIC FUNCTIONAL TEST (TYPE APPROVAL) OF PCS 1900-BASE STATIONS

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[Abstract] Within the ETSI Technical Specifications GSM 11.21 (Radio Aspects) and GSM 11.23 (Signalling Aspects) of the Base Station Systems (BSS) a number of test cases are defined as conformance requirements. The most important test cases which focus on the air interface and the A-bis interface of the Base Transceiver Station (BTS) are selected as essential conformance requirements. Based on these requirements the system architecture of the Base Station Tester was systematically developed. This paper presents the results of the design considerations and gives a survey of the appertaining application. The application can be divided into RF tests, which prove the transmitter and receiver characteristics, Radio-Link Management tests, which prove the timing tolerance, and Signalling tests, which prove the selected layer-2 and layer-3 signalling functions. In conclusion the presented test architecture fully meets the comprehensive requirements of BTS Type Approval.

I. Introduction

In a Digital Cellular Radio Communication Network like GSM 900 or PCS 1900 where thousands of base stations share the scarce resources of frequency, time and space very strict adherence to the relevant specifications is required [1]. As far as mobile telephones are concerned type approval test systems for GSM and PCN are already in operation [7], [8], for the functional test of base stations a test solution can now be presented. The GSM Radio Network (including the extended frequency band) is operating in the 900-MHz band with carrier frequencies between 925 and 960 MHz (downlink) respectively 880 and 915 MHz (uplink) for 174 channels. The PCS 1900 Radio Network is operating with carrier frequencies between 1930 and 1990 MHz (downlink) respectively 1850 and 1910 MHz (uplink) for 299 channels. For sufficient coverage a great number of Base Station Systems (BSS) are required which consist of Base Station Controllers (BSC) and typically a bigger number of Base Station Transceiver Stations (BTS). The maximum output power of a normal BTS-Transmitter is in the order of 320 W (GSM 900) resp. 20 W (PCS 1900), several types of micro- BTS are of lower power classes down to a maximum output power of 9 dBm. The BSSs support 6 steps of Static Power control with respect to the declared output power, in addition to the Static Power Control levels the BSS may utilise up to 15 steps of Dynamic Power control. This results in a measurement range of 88 dB, which the Base Station Testsystem has principally to cover. On the other hand for the BTS-Receiver a sensitivity level of -104 dBm is required in the presence of interfering signals with levels 50 dB above. Such challenging requirements for the BTSs cause also hard requirements for the Signal/Noise-ratio for the test signals to meet.

II. The relevant Test Specifications

Within the ETSI Technical Specification GSM 11.21 [2] and GSM 11.23 [3] regarding the Radio

and Signalling Aspects more than 1000 test cases on more than five BSS interfaces are defined. From these standards, national standards were derived, e.g. BAPT 222 ZV 6 for Germany and MPT 1378 for United Kingdom. The type-approval specifications in these standards are related to GSM 900 and DCS 1800 networks and a true subset of the test cases defined in the GSM specifications. It is assumed that for the PCS 1900 network similar requirements are applicable. The test cases deal with tests on the air interface and the A-bis interface of a Base Transceiver Station [4], [5]. A-bis is a digital interface with a data rate of 2048 kbit/s, allowing up to 120 16 kbit/s traffic channels to be handled. The GSM 11.21 specifies the RF- and Link Management tests and GSM 11.23, the signalling tests for the BTS. Essential conformance requirements are those, which are necessary:

-to ensure compatibility between the radio channels in the same cell
-to ensure compatibility between cells, both co-ordinated and unco-ordinated
-to ensure compatibility with existing systems in the same or adjacent frequency bands
-to verify the important aspects of the transmission quality of the system.

These conformance requirements will be proven by the following tests.

III. The relevant Test Cases

Transmitter Tests

The test **Static Layer 1 transmitter functions** verifies the interleaving, channel encoding and enciphering functions on the transmit site. The test **Phase error and mean frequency error** verifies the correct implementation of the GMSK pulse shaping filtering and the limitation of the phase and frequency error during the active part of the time slot. The test **Mean transmitted RF carrier power** verifies the accuracy of the mean transmitted RF carrier power across the frequency range and various power steps. The test **Transmitted RF carrier power versus time** verifies the transmitted power envelope within the useful part of the time slot and between the time slots. The tests **Adjacent Channel Power** verify the spectra of the RF output power due to the continuous modulation, wide band noise and power level switching, which can produce significant interference in the GSM 900, PCS 1900 and adjacent bands. The test **Spurious emissions from the transmitter antenna connector** measures the spurious emissions inside and outside the BTS transmit band, while the transmitters are in operation. The test **Intermodulation attenuation** verifies that the RF transmitter is able to restrict the generation of intermodulation signals caused by an external interfering signal. The test **Intra Base Station System intermodulation attenuation** verifies that the level of intermodulation products generated inside the relevant RX and TX band due to leakage of the various carriers into the transmitters do not exceed the specified limits.

Receiver Tests

The test **Static Layer 1 receiver functions** verifies the multiplexing and multiple access capability and the deciphering, de-interleaving and channel decoding functions on the receive side. The test **Erroneous Frame Indication Performance** verifies the reliability of the overall Bad Frame Indication (BFI) presented to the full-rate speech decoder and the Frame Erasure Indication (FEI) used on control channels. The test **Static Reference Sensitivity Level** verifies that the receiver will produce after demodulation and channel decoding data with a Frame Erasure Ratio (FER), Residual Bit Error Ratio (RBER) or Bit Error Ratio (BER) better than or equal to those specified for a specific channel type under static propagation conditions. The test **Multipath Reference Sensitivity Level** verifies that the receiver will produce after demodulation and channel decoding data with a FER, RBER or BER better than or equal to those specified for a specific channel type under multipath propagation conditions. The test **Reference interference level** measures the capability of the receiver to receive a wanted modulated signal

without exceeding a given degradation due to the presence of an unwanted modulated signal at the same carrier frequency (co-channel interference) or at any adjacent carrier frequencies (adjacent channel interference). The test **Blocking Characteristics (Blocking and Spurious Response Rejection)** measures the ability of the receiver to receive a wanted GMSK modulated signal in the presence of an interfering signal, whereby the level of the interfering signal in the test of blocking is higher than in the test for spurious response. The test **Intermodulation Characteristics (Intermodulation Rejection)** measures the linearity of the receiver RF parts. It expresses the capability of the receiver to receive a wanted modulated signal without exceeding a given degradation due to the presence of two or more unwanted signals with a specific relationship to the wanted signal frequency. The test **Spurious emissions from the receiver antenna connector** measures the emissions of the receiver at frequencies other than those of the BTS transmitter carriers and adjacent frequencies.

Radio Link Management Tests check the correct timing of the bits and the frames, prove the capability of the Frequency Correction Channel (FCCH) and the Synchronisation Channel (SCH), verify the structure of the TDMA frame, measure the signal strength and signal quality as a criterion for the RF power control and handover process.

In the OSI reference model, the layer above the physical layer (layer 1) is called the data-link layer (layer 2). This layer exchanges data blocks with the next higher layer and ensures correct reception by the Base Station by an acknowledgement procedure. When **Layer-2 Tests** are made, the message contents are modified, data blocks omitted and time limits not met or exceeded, i.e. the rules are deliberately violated to test the Base Station's reaction.

The Layer-3 Tests constitute the major part of all test cases. Numerous tests check the efficiency of link set-up and the associated messages, handover detection, basic measurement reporting, MS power control and error reporting.

IV. Analysis of the test requirements

The Test requirements have been analysed carefully and for each test case a test set up was theoretically developed which contained the measuring equipment, the switching and the connections to the Unit under Test. In order to minimize the number of different instruments, the measuring equipment was selected by the criteria of the required maximum technical characteristics and multiple utilisation.
By this method a complete optimized list of instruments was found and the baseline for all necessary switching paths could be defined. The result can be demonstrated by the **GSM-PCS-Base Station Tester.**

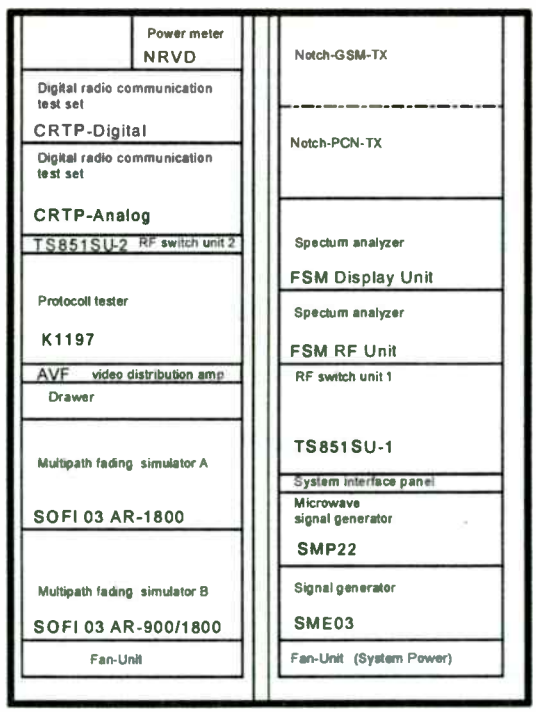

Fig.1 GSM-PCS-Base Station Tester

V. System architecture of the GSM-PCS-Base Station Tester

The Base Station Tester is linked to the base station via two interfaces: the air interface and the A-bis interface. For transmitter measurements the base station is set to the desired transmit mode via the A-bis interface by the **Protocol Tester K1197**. RF parameters such as frequency, phase and spurious emissions are measured at the air interface. For receiver measurements the test system sends the wanted signal along with the required interference signals to the air interface of the base station. The data are received by a Protocol Tester at the A-bis interface of the base station, converted and sent back to the test system, where the bit-error rate is determined by the CRTP.
The **Digital Radiocommunication Test Set CRTP 04** [6] is the heart of the Base Station Tester. As a signalling unit, CRTP 04 simulates the Mobile Station and sets up calls with the base station. The traffic channel and the interfering channel are simulated by the two signal sources of the instrument. After call set-up, CRTP 04 determines the power versus time template, the frequency and the phase error, the bit-error rate, and performs all signalling tests at the air interface. The instrument also acts as the system controller.

Besides the tests in the GSM 900-, PCS 1900 - and adjacent bands, other RF tests have to be carried out to determine spurious emissions from the base station in the range 100 kHz to 12.75 GHz. These tests are performed by **Spectrum Analyzer FSM,** which has extremely high input sensitivity and extremely low phase noise.

As described above further tests are carried out to determine the base station's immunity to interference. **Two RF generators** are selected for these tests: Signal Generator **SME** (5 kHz to 3 GHz), which has highly versatile modulation facilities, extremely high spectral purity and frequency-hopping capability, generates a GMSK-modulated interference signal in the receiver test cases covering Intermodulation Characteristics and Reference interference level. Broadband Signal Generator **SMP** (10 MHz to 20 GHz) supplies interference signals up to 12.75 GHz in the test cases covering the Blocking Characteristics.
The **Fading Simulator SOFI 03 AR** degrades the wanted signal to simulate realistic transmission conditions for the traffic channel in the uplink band. A total of twelve paths are available for channel simulation. Attenuation, delay and doppler spectrum can be selected individually for each channel. The fading simulator can be operated as a single-channel 12-path simulator or as a dual-channel 6-path simulator. In dual-channel mode, two uncorrelated fading signals are generated. The fading simulator not only generates all channel models stipulated by GSM Technical Spec. 05.05. but also virtually any type of user specific channel model.

All transmit and receive signals are routed via the comprehensive RF-Switch-Unit. The extremely high requirements with respect to accuracy and
dynamic range caused an appropriate high effort in the development of the Switch Unit. Thus this test system component contains apart from circulators, isolators and amplifiers roughly 50 relays, 3 customized diplexers and 12 customized filters. The tuneable notch filters support the testing of the intermodulation products of the transmitter stages at any frequency in the GSM 900- and PCS 1900- receive and transmit band.
It can be seen in Fig.2 that the normal signal path for a standard link set-up between the Base Station Tester and a base station (Device Under Test DUT) is quite straight through. The CRTP sends a simulated uplink signal directly to the Base Station or via attenuators. The downlink signal sent by the base station is applied to the receiver section of CRTP via a power combiner and via a selectable amplifier. Signal traffic is displayed on a spectrum analyzer. The analyzer also measures the output spectrum and spurious emissions from the Base Station. To do this, the downlink signal is passed through complex filter banks to suppress the wanted signal, which under normal circumstances would prevent a suitable measurement sensitivity.

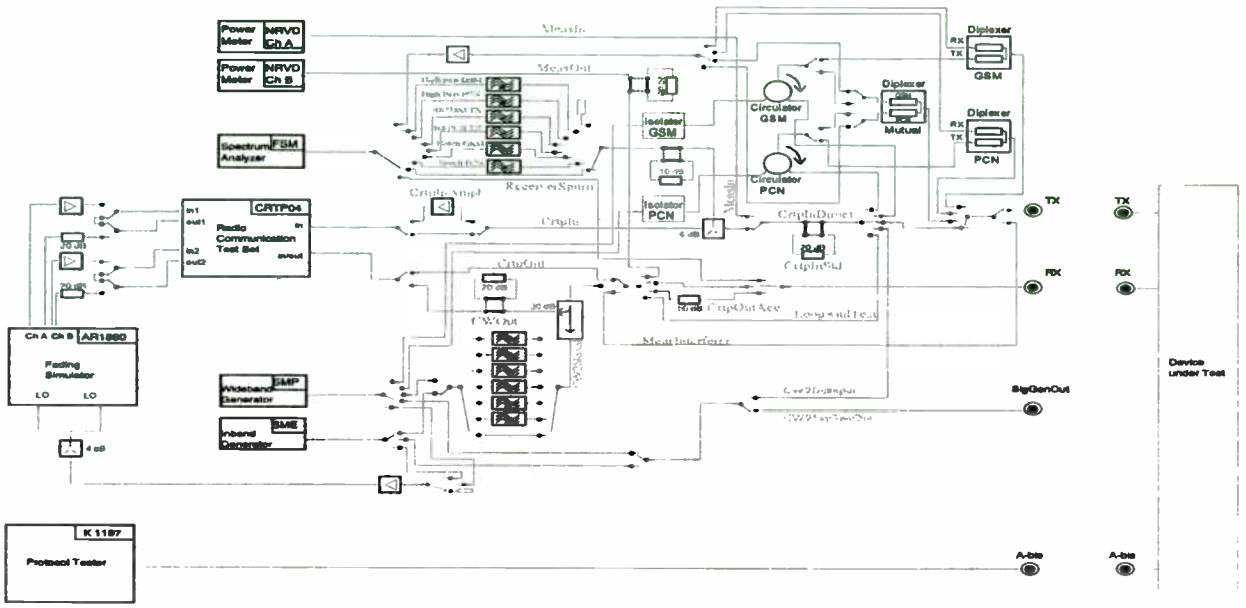

Fig.2 RF-Functional-Block diagram of the GSM-PCS-Base Station Tester

The mutual duplex filter will be used when spurious in the complementary frequency band compared to the active one, GSM 900 or PCS 1900, will be determined. The two duplex filter for the receive band and the transmit band are in use during the tests of the transmitter intermodulation attenuation.

Generators SME and SMP are used as local oscillators for the fading simulator and also as interference sources for immunity and intermodulation tests. Depending on the required frequency and modulation, an interference signal from SME or SMP is added via the circulators to the downlink signal (intermodulation attenuation test) or via the lower filter banks and the directional coupler to the uplink signal (blocking test) and applied to the base station.

RF measurements require extremely high level accuracy. However, given the wide frequency range of up to 12.75 GHz, even the most carefully designed RF switching units are prone to unpredictable frequency response. To minimize this dependence on frequency, two RF probes of a RF Power Meter are incorporated in the RF switching unit at strategic points of the switching matrix. The levels of the Base Station Tester generated signals are monitored via channel B and the levels of the received signals via channel A. With the aid of these RF probes, reference values are determined and used for automatic level compensation in RF measurements.

VI. Application of the GSM-PCS-Base Station Tester

Two examples of test application will give an indication of the required capability which the Base Station Tester has to meet.

During the test of the **Blocking Characteristics** two combined RF signals will be fed into the receiver antenna connector of the base station. The wanted signal modulated with normal GSM modulation

shall be at the operating frequency of the receiver and shall have a level of -101 dBm. Simultaneously an unmodulated interfering signal with a very high level of +8dBm shall be applied in the frequency range between 600 kHz and 12.75 GHz. Considering the measuring bandwidth of 200 kHz the required Signal/Noise Ratio of the interfering signal can be calculated to more than 170 dB. This extremely high S/N figure is only achievable by insertion of filters, even if high quality generators are used. Because of the wide frequency range three filters are necessary, a low pass filter and a high pass filter out of the receiving band and an in band notch filter. Due to the variable receiving frequencies the notch filter has to be tuneable in the range of the receiving band. In order to achieve the required level accuracy of 1 dB of the small wanted signal this signal will be generated at an higher level which is monitorable by the RF probe of the precise RF Power Meter. Having the level appropriately adjusted the signal will be attenuated by the previously measured attenuator down to the required level of -101 dBm.

During the test of **Conducted spurious emissions from the transmitter antenna connector: outside the BTS transmit band** the spurious emissions in the frequency range between 100 kHz and 12.75 GHz are to be determined. The maximum power should not exceed -30 dBm for frequencies up to 1 GHz and -36 dBm for frequencies above 1 GHz. All base station transmitters are active at their maximum output power on all time slots. Assuming a maximum power of 43 dBm a measurement dynamic range of greater than 79 dB is required. Apart from this a resolution bandwidth of up to 3 MHz is also specified. These requirements can also only be met if filters are inserted. Three filters per frequency band (GSM and PCS) are in operation during this test. The spurious emissions within the BTS receive band shall not exceed a maximum power of -98 dBm which results in a measurement dynamic range of greater than 140 dB. The specific mutual duplex filter supports this requirement.

VII. Conclusion

Measurements as described above need a lot of effort if they were performed by manual test set up. The individual physical test preparation, collecting instruments and connecting the correct links and cables is prone to human errors. The manual performance of the thousands of measurements regarding the RF path compensation and regarding the main test case contents is very time consuming and only with difficulty reproducible. Furthermore for the purpose of Design Verification/Type Approval a well documented package of test results has to be produced.

Automatic Test Systems which perform the measurements by using a fixed set of standard instruments and a signal adapting RF switching unit as presented in this paper perform the major part of the testing task automatically. The testing effort is reduced, the tests are performed within a short and computable period of time, the test results are automatically well documented.

The Test Capabilities for Automatic Design Verification of the Base Station are implemented in the described Base Station Tester which fully meets the comprehensive requirements of BTS Type Approval. All measurements are reproducible under the same conditions and can be repeated at any time and in various laboratories.

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No More Debate

PCS In the Local Loop Leaves Cable Plant in the Dust

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The communications industry embraced hybrid fiber coax (HFC) when faced with the challenge to offer broadband services. Communications companies thought HFC would enable them to implement high-speed, high-bandwidth fiber cabling from the central office to a hub in the field. From that hub, coax cabling would take communications services to the curb and into the home. Then came the debate as to whether HFC was really worth the effort since the price of fiber to the curb started to decline.

But now there's a new debate. Is a cable plant — any cable plant — necessary? In some circles the question is, "Who'd want it?" As personal communications services begin to take shape, carriers just now are beginning to explore the uses they envision for their billion-dollar investments. Encouraged by a recently passed federal bill that relaxes rules governing crossover services provided by telecommunications and cable television companies, PCS has the potential to become the be-all, end-all communications pipeline for practically any application.

With an antenna mounted on top of their houses, occupants could have access to a broad range of digital services including voice, fax, e-mail, cable, video-on-demand, radio-on-demand, the Internet and applications that haven't even been invented yet. And service would be guided by competition in a free market.

A radio-based infrastructure would cost far less to install than physical connections. Radio in the local loop would merely require the deployment of antennas on existing buildings. No lines would be have to be buried and no dirt would have to be turned as required with land lines. Furthermore, an antenna infrastructure would be more cost-effective to operate and maintain.

Koopmans will examine the advantages and disadvantages of radio in the local loop and how these compare to the advantages and disadvantages of cabling. He will explain the technologies behind PCS that will make radio in the local loop a reality and discuss a feasible time frame for implementing these new services.

I. Wireless Local Loop: What is it?

The world is getting smaller. Through advances in communications technology, people, countries and cultures from different parts of the globe are drawing closer together. The telephone system is perhaps the most pervasive and personal example of how technology diminishes the distance among earth's inhabitants.

Although conceptually unaltered for more than 100 years, innovations in technology have transformed telecommunications dramatically, bringing about the invention of new information services. The Internet is the latest development, but certainly not the last. Despite the widespread availability of telecommunications, particularly in industrialized nations, there still remain access issues in developing nations, where, at times, geography plays a role equal to economics.

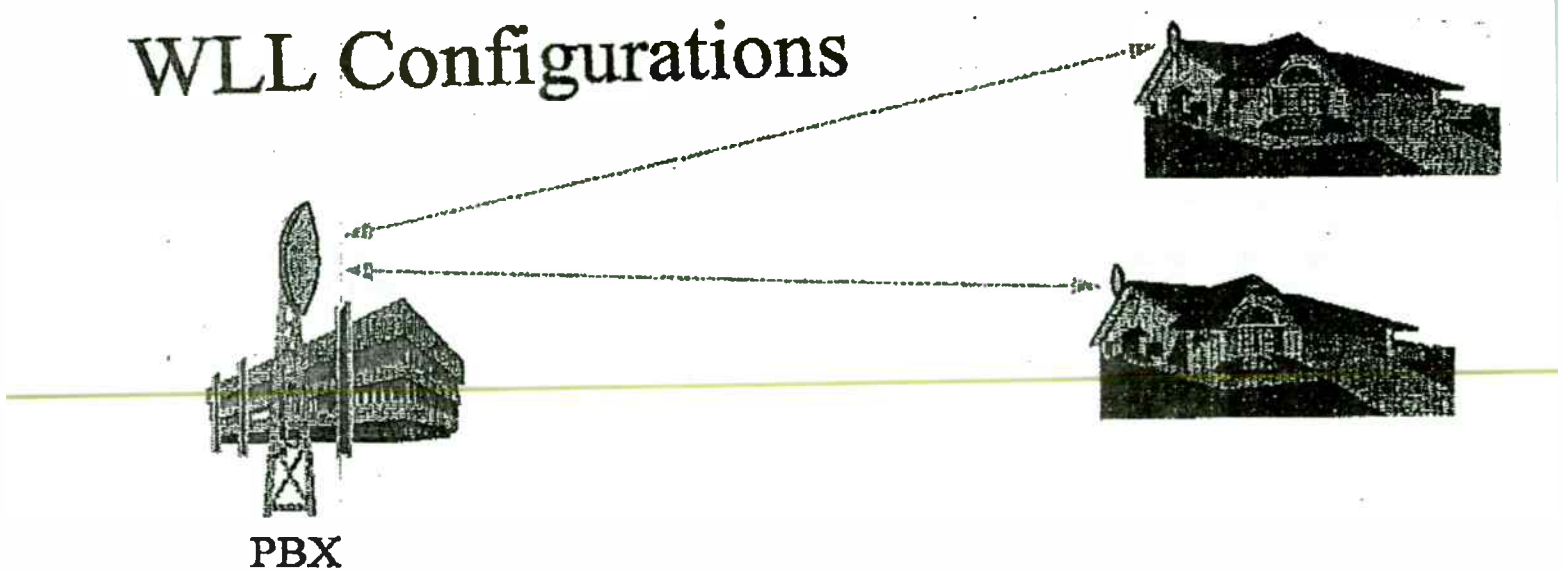
Providing wired telecommunications access for every person is a vast undertaking, involving huge capital investments, and is beyond the economic resources of the developing world. New technologies have emerged to provide access, including coax, fiber terrestrial radio and satellite. Fiber and coax have concentrated on providing higher bandwidths while radio offers lower connection costs.

Digital radio technologies hold the most promise in creating universal access for in emerging countries that have no infrastructure. Cellular telephones have been available for years, but only to an elite portion of the population and have been viewed generally as more expensive than the incumbent wired network

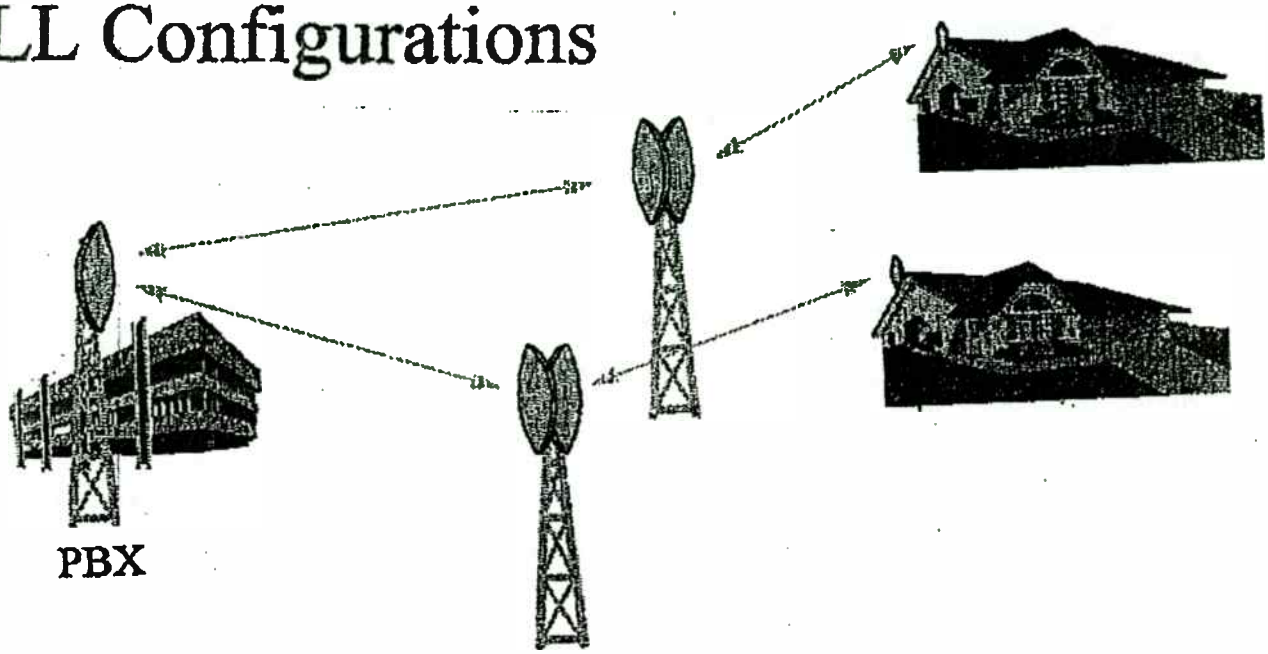
The wireless local loop (WLL) is a new look at network access using radio technology. With this technique the services of the network can be offered faster, easier and cheaper, addressing areas where no access exists.

WLL bypasses the wireline connection between the service subscriber's premises and the central office switch in the public network. Using this definition, WLL is a 'fixed' wireless installation that typically does not provide mobility. By defining WLL as a 'fixed' wireless service, multiple system configurations are possible.

In a general configuration, the distance between the subscriber unit and network access point can be bridged using just two transceivers. An alternate configuration is the relay technique where more than two transceivers are employed. Another variation includes some cabling along a pipeline. For a new service provider with no wired infrastructure, the cost of connecting radio base stations into the network can be the dominate economic factor.



WLL Configurations



Choosing between a network with two transceivers as a bridge or a network with the relay technique depends on the existing network infrastructure and the topography of the country in which the system will be installed.

Even within a single country geography varies. The United States will be an interesting testing ground for WLL architecture because of the combination of rural and high density urban areas. In many respects these unique geographical considerations immediately raise the issue of technology. Although the choice of technology plays a role, such choices must be put in proper perspective: commercial benefits.

II. Wireless Local Loop: Why Bother?

In the developed world, the main driver behind WLL is the comparative cost advantage. With the deregulation of the telecommunication markets globally, prevailing public telephone network service providers already are encountering competition from other operators also using landline systems. WLL operators economically will undercut both the established wired service providers and emerging competitors.

For wired networks, the cost of network access is calculated primarily using parameters such as cost per subscriber house or revenue lost per nonsubscriber house. WLL access methods have significant cost advantages over cable installations, and the parameters used in calculating costs in wired environments take on a different meaning.

For example, in the United Kingdom the copper penetration level of telecommunications is close to 100 percent. The service provider loses money if a household does not accept the service because the infrastructure already is in place. Competitors entering the market via WLL will not have that problem because there are no fixed landlines to install. The U.K. government

has issued only three licenses to companies that could offer WLL access to telephony services.

In developing countries with little access to telephony services, the primary advantage WLL holds over cable is that wireless technology is much easier to install and is likely to be cheaper than copper wire. A classic example is India, a country where some 400,000 villages do not have access to any telephone network. Vast distances need to be covered and installation of cable is hardly an option because of the costs compounded by the potential for vandalism and theft.

Beyond the commercial and financial aspects of WLL, legislative changes in some countries make wireless network access the most attractive option in emerging markets. Furthermore, in some countries, the lay of the land make wireless the only option.

III. Wireless Local Loop: How Does It Work?

Selecting a configuration for a wireless local loop is determined on a case-by-case basis. There are too many factors involved in each application, and it is virtually impossible to develop a magic calculation for every situation.

For example, systems designers must decide what level of service quality should be provided. In the example of India, the quality must be acceptable for most telephone applications, but the No. 1 priority is to get a telephony service to remote areas. Therefore digital technology is not necessarily a requirement. In the developed world the quality must be better than that offered by copper wire. New digital personal communications services technologies are an essential part of the picture.

In the example of the United States, the wireless coverage area is important. When choosing a long-range technology the cost of technology sharply increases, but fewer base stations are required. Short-range technology can be cheaper and can accommodate a higher traffic capacity than long-range technology. However, more base stations are required, increasing infrastructure costs. Calculations that show the cost of technology are important, but are ultimately less dominant in the final analysis. Therefore, an economic model of any system must be tuned carefully before technology decisions are made.

This point is illustrated with a practical example. In the United Kingdom, Ionica, a new operator has based its entire business strategy on the WLL concept. The company developed this decision by creating different cost models. Systems planners then discovered that no existing technology fits into their concepts. Consequently, the company developed a proprietary air interface technology. Although the company cannot benefit immediately from cheap equipment components, planners discovered that technology cost of is not the overriding factor once the system configuration is established.

While Ionica discovered its economic model required proprietary technology, that does not mean that WLL operators in other countries will draw the same conclusions. Existing technologies may be suitable in certain situations. More likely, a combination of technologies will be used to address different topographies, particularly in North America where population spread is so diverse.

IV. Conclusion

Wireless in the local loop can provide new providers of telecommunications service quick, easy and inexpensive access to existing markets where a wired infrastructure already is established. Introducing wireless in a wired environment gives consumers more choices in service, fostering competition. Wireless capabilities also provide an economical way to bring widespread telecommunications where no network exists, such as in most developing nations or in topographical areas where wires are difficult to deploy.

Wireless in the local loop won't change the reasons why people want to communicate, but it can change the way they do it. WLL can increase telecommunications access in parts of the world historically excluded from everyday use of this voice technology. In this sense, WLL can be seen as another step in drawing people, countries and cultures from around the world a little closer together.

Achieving Gain Enhancement in PCS handset systems with New Antenna Designs in Free Space and near Human

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Abstract

The proposed antenna systems on a handset have the merits of shaping the antenna pattern and enhancing the antenna horizontal gain of 5 dB in free space, 2 dB near a operator. Because of high flexibility of the systems, any antennas (whip antennas or built-in antennas) can be adopted for the systems. In addition, adaptive antenna pattern can be achieved by choosing the system conditions.

For the systems being designed, Electromagnetic Field Simulator is essential because it is difficult to determine the optimum conditions of the systems by measurement. Then efficient computation of the electromagnetic field of the system is required. The method of the efficient computation procedure in the method of moments is shown below.

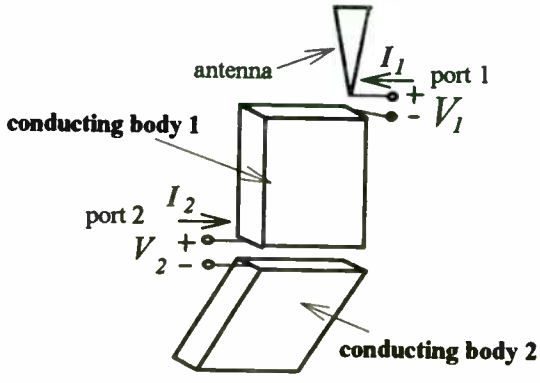

Fig. 1. A new structure of antenna system in a handset. An antenna is excited at port 1 and a load is attached to port 2.

I. Introduction

In mobile communications, portable cellular phone market is rapidly expanding world-wide. Therefore high performance and good tractability of the handset are required to compete in the market. Design of antenna is surely one of the key technology to achieve the object. Almost all the handsets use whip antennas because of the simplicity. In addition, the whip antennas have higher gain than the built-in antennas and are nearly omnidirectional in the horizontal plane when there is nothing near the handsets as in free space. As a whip antenna, $\lambda/4$ monopole antenna is often used. The main drawback is that its antenna pattern deflects more than 30° downwards when the size of the handset is of about a wavelength which condition is often met at 1.9 GHz band. This causes the decrease of the horizontal plane gain about 6 dB compared with the gain of a dipole antenna in free space [1,2]. The same drawback is occurred as for PIFA (Planar Inverted F antenna) [3]. The decrease of the gain is a major problem on designing a portable handset because the communication range and the battery life time depend on the gain.

Overcoming these difficulties, we developed new antenna systems on a handset for PCS, PHS or DECT operating 1.9 GHz band as in Fig. 1 [3-5].

One example of the new antenna system consists of a antenna, two conducting boxes (which make a housing of the handset) , and a passive load. Using a monopole antenna or a PIFA as an antenna on the handset, the new antenna system improves the antenna gains from 2 dB to 5 dB. Even at the very proximity to human head and hand, the improvement is also attained. In addition, changing the value of the passive load makes the antenna pattern variable in desirable forms.

The merits of the systems are ascertained by the calculations based on the method of moments using surface patching modeling and the measurements both in free space and very close to the head and hand.

Because the new developed antenna system has great flexibility, that is, the system can be applicable to any kind of antennas and structures of the handset, the new antenna system is very promising.

The paper is organized as follows. In Section II we explain the efficient method used in the calculation of the method of moments where the surface integral equations are used. In Section III we show the new structure of antenna system to enhance the antenna gain. A $\lambda/4$ monopole antenna and a PIFA on conducting boxes are considered in free space and near the head and hand.

II. Efficient computation in the method of moments in the EFIE and the MFIE

In calculation, efficient and accurate computation was done by the method developed in [6] as follows. The typical geometry to be considered here is shown in Fig. 2.

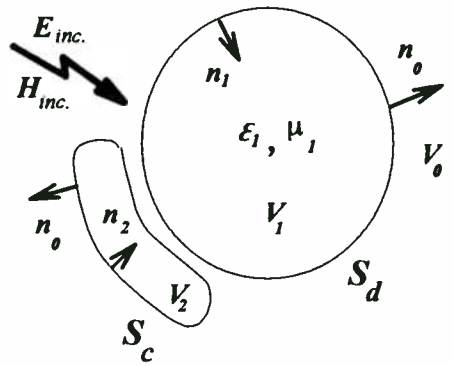

Fig. 2 Geometry of a homogeneous lossy object V_1 and a conducting body V_2 in free space V_0.

This is the problem of electromagnetic scattering from 3D arbitrary shaped homogeneous lossy dielectric objects (human head and hand) and antenna systems formed by 3D arbitrary shaped conducting bodies. The surface integral equations of the EFIE (Electric Field Integral Equation) and the MFIE (Magnetic Field Integral Equation) are used and are reduced to the matrix equation by MoM (the method of moments) following [7,8]. The objects and bodies can be modeled by triangles and some of them by rectangles.

Recently, by using FDTD (Finite Difference Time Domain) method, many papers about the problem concerning the portable phone near human head (and hand) have been published[9-11]. Whereas FDTD makes easily the calculation of the portable phone near real human head and hand with complex material constitutions, FDTD requires a powerful computer and needs the repeated computation at the beginning even as one parameter are slightly changed.

In contrast, MoM makes the repeated calculation more faster than the first calculation because the calculation is repeated only in the changed matrix elements, although MoM cannot treat the complex problems like real human head. Since the detailed structures of human head don't affect the characteristics of the handset near human head[11,12], MoM is useful for the repeated computation as a few parameters are changed. Therefore MoM is used in this computation.

The calculation of the matrix elements are performed by the surface integrals of the uniform and linearly varying currents on the triangle and the rectangle. The integrands of the surface integrals have the singularities of the order R^{-1}, R^{-2}, and R^{-3}. In particular, the strongest singularity R^{-3} causes the jump discontinuity in the values of the integrals of the self terms. Thus, the accurate numerical integration of the terms is very difficult. It is known that the accuracy of the result of the moment method critically depends on the one of the self terms. Therefore the efficient and accurate calculation of the self terms is crucial to the moment method.

In static problem, the closed form expressions of the corresponding surface integrals have been given [13],[14]. For time-harmonic electromagnetic problem, say, dynamic problem, some surface integrals are converted into the line integrals [15].

We extend the results and show that all the surface integrals of uniform and linearly varying currents on the triangle and the rectangle are converted into the line integrals by using the three new integral identities.

The line integrals have merits with regard to numerical calculation:

1) Numerical integration is easily done even at the observation points very close to the source region.

2) The numerical integration converges more rapidly than the one of the corresponding surface integrals in any case.

In the following, we show the new integral identities and discuss efficiency of the line integrals converted from the corresponding surface integrals.

A. The surface integral equations of the EFIE and the MFIE [6]

The geometry in Fig. 2 is one of antenna systems consisting of a human head and a portable telephone set. V_1 is the domain representing the head and hand bounded by S_d. It is modeled by the lossy dielectric object characterized by the constitutive parameters ε_1, μ_1. V_2 is the domain modeling the portable telephone set formed by the antenna and the perfect conductor whose boundary is denoted by S_c. V_0 is free space. $\boldsymbol{n}_i$ is the unit surface normal on S_i and pointing into V_i.

Following the notations of [16], the boundary conditions are expressed as

$$\boldsymbol{E}_{inc.}|_{tan} = \left\{ L^0_{S_c} \boldsymbol{J}_c + L^0_{S_d} \boldsymbol{J}_d - K^0_{S_d} \boldsymbol{M}_d \right\}|_{tan} \quad \text{on } S_c \tag{1}$$

$$\boldsymbol{E}_{inc.}|_{tan} = \{ L^0_{S_c} \boldsymbol{J}_c + (L^0_{S_d} + L^1_{S_d}) \boldsymbol{J}_d - (K^0_{S_d} + K^1_{S_d}) \boldsymbol{M}_d \}|_{tan} \quad \text{on } S_d \tag{2}$$

$$\boldsymbol{H}_{inc.}|_{tan} = \{ K^0_{S_c} \boldsymbol{J}_c + (K^0_{S_d} + K^1_{S_d}) \boldsymbol{J}_d + (\frac{L^0_{S_d}}{\eta_0^2} + \frac{L^1_{S_d}}{\eta_1^2}) \boldsymbol{M}_d \}|_{tan} \quad \text{on } S_d \tag{3}$$

where η_i is the intrinsic impedance in V_i,

$$J_i = n_0 \times H_i \quad \text{on} \quad S_i \tag{4}$$

$$M_i = E_i \times n_0 \quad \text{on} \quad S_i \tag{5}$$

$$L_i^t C(r') = j\omega\mu_i \int_s \left[C(r') - \frac{\nabla' \cdot C(r')}{k_i^2} \nabla' \right] \Phi_i(|r - r'|)\, dS' \tag{6}$$

$$K_i^t C(r') = -\int_s C(r') \times \nabla' \Phi_i(|r - r'|)\, dS' \tag{7}$$

$$\Phi_i(|r - r'|) = \frac{e^{-jk_i|r-r'|}}{4\pi|r - r'|} \tag{8}$$

and k_i is the wavenumber in V_i.

The electric current J_i and the magnetic current M_i on S_i are expanded by basis functions which represent uniform and linearly varying currents on triangles and rectangles. Testing both sides of (1)- (3) with the same basis functions and approximating the inner products, these equations are reduced to the matrix equation [7,8].

B. New integral identities

The calculation of the matrix elements and the electromagnetic fields are reduced to the calculation of three kinds of the surface integrals on S_i which are converted into the line integrals by the new integral identities.

The new integral identities are derived from the natural extension of the previously known ones in static field [13] into the ones in electromagnetic field. Therefore the new integral identities shrink the ones in static field as frequency goes to 0, say, static case. The new integral identities are

$$\int_s \frac{e^{-jk_i R}}{R} dS' = \frac{j}{k_i} \int_{\partial S} \frac{m \cdot \rho'}{\rho'^2} (e^{-jk_i R} - e^{-jk_i h}) dl' \tag{9}$$

$$\int_s \frac{\rho' e^{-jk_i R}}{R} dS' = \frac{j}{k_i} \int_{\partial S} m (e^{-jk_i R} - e^{-jk_i h}) dl' \tag{10}$$

$$\frac{\partial}{\partial z} \int_s \frac{e^{-jk_i R}}{R} dS' = z \int_{\partial S} \frac{m \cdot \rho'}{\rho'^2} \left\{ \frac{e^{-jk_i R} - e^{-jk_i h}}{R} \right\} dl' + z e^{-jk_i h} \int_{\partial S} \frac{m \cdot \rho'}{\rho'^2} \left\{ \frac{1}{R} - \frac{1}{h} \right\} dl' \tag{11}$$

where ρ' is the surface component of the position vector r' on S, m is the unit normal to ∂S and in S, $z = n \cdot r'$, $h = |z|$, n is the unit normal of S, and R is the absolute value of r' as in Fig. 3. In (11), only the first term must be numerically integrated because the second term is analytically integrated [13,14] and have difficulty in the case of the observation points being on the boundary. The difficulty can be avoided by extracting the terms which can be expressed in the closed forms.

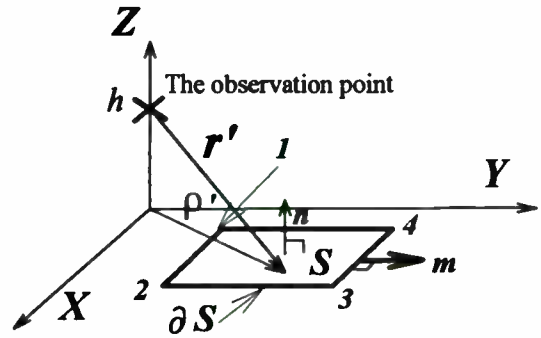

Fig. 3 Geometrical quantities associated with a rectangular basis S in the XY plane.

C. Comparison of convergence

In this section, we discuss convergence of numerical integration of the line integrals and the surface integrals for the rectangular region S of $0.1\lambda_0 \times 0.1\lambda_0$ in Fig. 3 where λ_0 is wavelength in free space. Following discussion, unit of length is normalized by λ_0.

Showing superiority of the line integrals and making the surface integrals tractable often used in practice, we subtracted some kinds of singularities from the integrands in the surface integrals. That is, we used

$$\int_s \frac{e^{-jk_i R} - e^{-jk_i h}}{R} dS' \tag{12}$$

$$\int_s \frac{\rho'(e^{-jk_i R} - e^{-jk_i h})}{R} dS' \tag{13}$$

$$-z \int_s \frac{(1 + jk_i R)}{R} (e^{-jk_i R} - e^{-jk_i h})\, dS' \tag{14}$$

in the numerical integration for (9)-(11).

The reference values of the integrals were obtained using the line integrals by Romberg integration whose convergence criteria were relative error of 1.0e-15 and highest extrapolation order of 20. The line integrals were performed by 1D Gauss integration of degrees from 2 to 16 and the surface integrals by 2D Gauss integration of degrees from 2×2 to 16×16.

Fig. 4 shows relative error vs. number of integration points for scalar potential of (9) at the observation points of z=1.0e-2 and three (x, y) pairs which are typical and correspond to the quasi self term, the adjacent terms, and the neighboring terms in the method of moments. The term very close to S by the line integrals converge more rapidly than the ones by the surface integrals. However the higher h or the more far x=y is, the faster both the line and surface integrals converge. In these cases, the surface integrals can be used as efficient numerical integration.

Fig. 5 was calculated as almost the same conditions of Fig. 4 for vector potential of (10). The results for the derivative of scalar potential of (11) are shown in Fig. 6. The conclusions are the same as ones for Fig. 3.

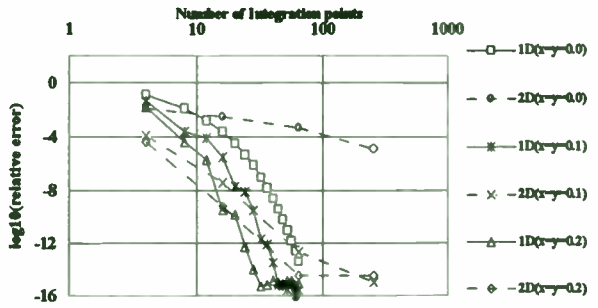

Fig. 4 Relative error vs. number of integration points in static potential of (12) for z=1.0e-2 where x=y are 0, 0.1, and 0.2 with $\Delta_x = \Delta_y = 0.1$.

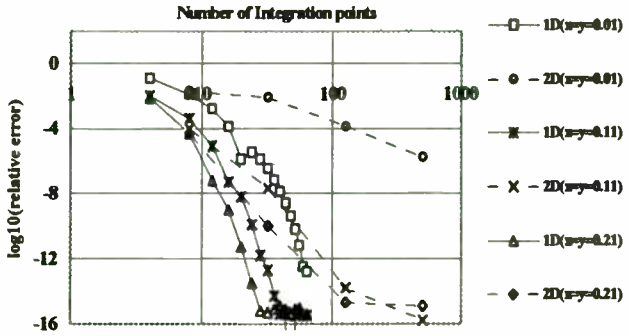

Fig. 5 Relative error vs. number of integration points in vector potential of (13) for z=1.0e-2 where x=y are 0.01, 0.11, and 0.21 with $\Delta_x = \Delta_y = 0.1$.

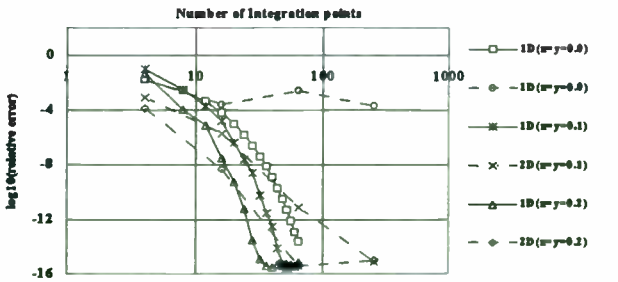

Fig. 6 Relative error vs. number of integration points in the normal derivative of static potential of (14) for z=1.0e-2 where x=y are 0.0, 0.1, and 0.2 with $\Delta_x = \Delta_y = 0.1$.

From the results, the line integrals are more efficient and accurate than the surface integrals, especially for the nearly self terms.

III. New structure of antenna system

It is known that the gain decrease in the horizontal plane becomes small as the conducting body becomes small[1-2]. However it is very difficult to make the conducting body smaller than one wavelength considering the tractable size of the handset at 1.9 GHz.

To recover this gain reduction, we propose the method that enhance the antenna gain by passive loading, in the horizontal plane.

As one example, a new structure of antenna system using our method is shown in Fig. 1. The two conducting bodies subdivided from an original conducting body are connected by a passive load at port 2 and the antenna is fed at port 1.

A. Theory of operation [5]

The principle of our method is explained through the effective complex length[17] as

$$\mathbf{h}(V_1,V_2,\theta,\phi) = \frac{\int_S (\hat{\mathbf{r}}\hat{\mathbf{r}} - \mathbf{I}) \bullet \mathbf{J}(\mathbf{r}', V_1, V_2) e^{jk_0\hat{\mathbf{r}}\bullet\mathbf{r}'} dS'}{Y_{in} V_1} \quad (15)$$

where J is the current distribution on the antenna and the conducting body, $\hat{r}$ is the unit vector directing the observation point(θ,ϕ), I is the identity dyadic, k_0 is the wavenumber of free space, V_1 is a voltage fed to the antenna, Y_{in} is the input admittance of the antenna at port 1 and V_2 is a voltage at the load Z_L. Using the Eq.(15), we get the gain of θ component as

$$G_\theta(\theta,\phi) = \frac{\eta_0 |Y_{in}|^2 k_0^2 \left|\mathbf{h}(V_1,V_2,\theta,\phi)\bullet\hat{\theta}\right|^2}{4\pi\, Re(Y_{in})} \quad (16)$$

where η_0, $\bullet$ and $\hat{\theta}$ denote the intrinsic impedance of free space, inner product and the θ -directing unit vector respectively.

When the antenna is excited by V_1 and the load Z_L is connected, V_2 is given by

$$V_2 = -\frac{Z_L Y_{21}}{1 + Z_L Y_{22}} V_1 \quad (17)$$

and the input admittance Y_{in} is given by

$$Y_{in} = Y_{11} - \frac{Z_L Y_{21} Y_{12}}{1 + Z_L Y_{22}} \quad (18)$$

using the admittance matrix Y_{ij}.

From the Eq. (15),(17), the effective complex length is decomposed into

$$h(V_1,V_2,\theta,\phi) = \frac{Y_{11}}{Y_{in}} h(V_1,0,\theta,\phi) - \frac{Y_{12}}{Y_{in}} \frac{Z_L Y_{21}}{1+Z_L Y_{22}} h(0,V_1,\theta,\phi) \quad (19)$$

where $h(V_1,0,\theta,\phi)$ denotes the effective complex length when the load sets short and $h(0,V_1,\theta,\phi)$ denotes the one when the antenna feed point sets short and the load terminal is excited by V_1 .

Owing to this equation, we can change the antenna pattern by changing the load Z_L ,that is, we can control the antenna pattern by the load. We have found the optimum loads in which the antenna patterns have desirable characteristics.

Therefore our method has the easiness of construction and consumes no power when using the purely reactive load. Moreover our method is applicable to many kinds of antenna on a handset.

B. λ/4 monopole antenna on a handset

To show the usefulness of our proposed method, we first examine the characteristics of the antenna characteristics of a $\lambda/4$.

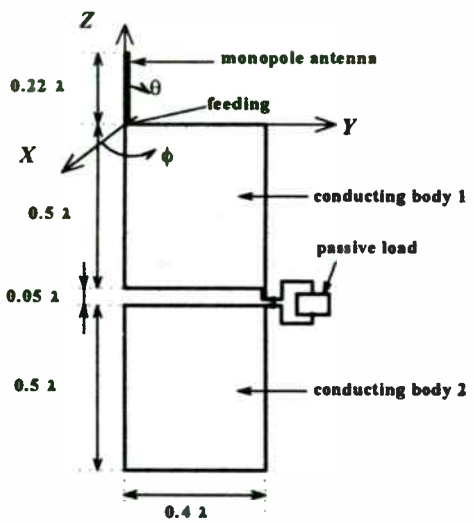

Fig. 7. A new structure of $\lambda/4$ monopole antenna system in a handset.

The geometry of one model using our method is shown in Fig. 4. Two plates of the same size are separated by 0.05 λ (this separation distance is unimportant) and connected at the opposite sides of the antenna by a passive load(this connection point is important). To calculate the antenna gain pattern for arbitrary passive load, we have used the decomposition of the effective complex length by the two effective complex lengths of the open case (Z_L= infinite) and short case (Z_L= 0).

We have searched the nearly omnidirectional and relatively high gain pattern in the XY plane by changing the passive load value in calculation. The ranges of the value are from 0 to 10KΩ in real part and from -10KΩ to +10KΩ in imaginary part. We have found that the best characteristics are obtained when Z_L is purely reactive.

To measure the antenna system performance, the maximum gain and average gain in the horizontal plane are used here. The maximum gain is defined as follows.

$$G_{\theta.max.} = \max\left[G_\theta(\theta = \pi/2,\phi)\right]_{\phi=0}^{\phi=2\pi} \quad (20)$$

The average gain in the horizontal plane is defined as

$$G_{\theta.avg.} = \frac{1}{2\pi}\int_0^{2\pi} G_\theta(\theta = \pi/2,\phi)\,d\phi \quad (21)$$

This is MEG(mean effective gain)[18,19] when all electromagnetic waves are incoming from the horizontal plane and vertically polarized. They are shown in Fig. 8 where the calculated average gains (solid line) and the maximum gains (dotted line) are depicted with the measured ones for the new structure and the conventional one. The maximum of the average gain and the maximum gain are obtained when Z_L equals -j516Ω.

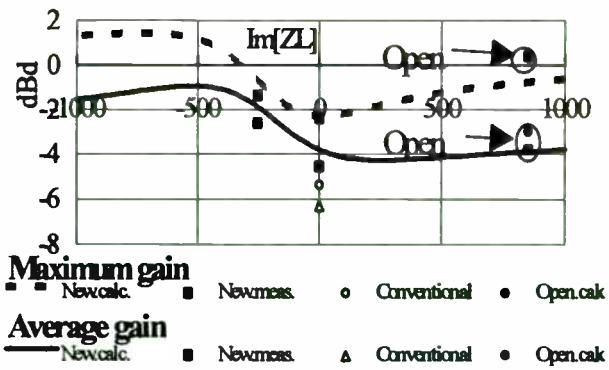

Fig. 8. The maximum and average gains of the new structure and the conventional one for the passive load that is purely reactive, in free space.

G_θ antenna patterns of capacitive loads Z_L=-j116Ω (broken line), -j250Ω (solid line) and -j516Ω (dotted line) are plotted in Fig. 9.

From Fig. 8, the antenna gain in the XY plane is found to increase to the maximum of 1.1 dBd and the average of -0.9 dBd when Z_L=-j516Ω. Therefore the

gain improvement of 5 dB from -5.9 dBd has been attained.

From Fig. 9, the antenna patterns changes as the value of the load is changing from -j116Ω to -j516Ω. This indicates that the antenna pattern can be controlled by the passive load.

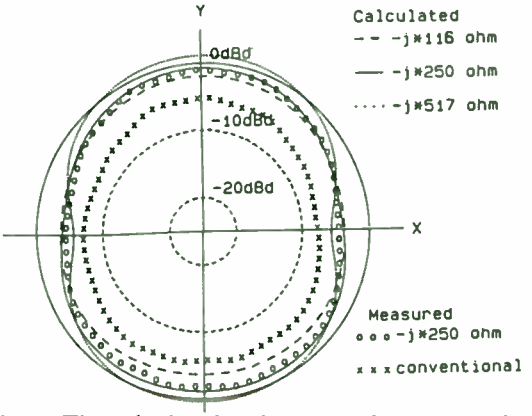

Fig. 9. The calculated and measured antenna gain pattern of the new structure and the conventional one in the XY plane, in free space.

C. New PIFA system on a handset in free space [3]

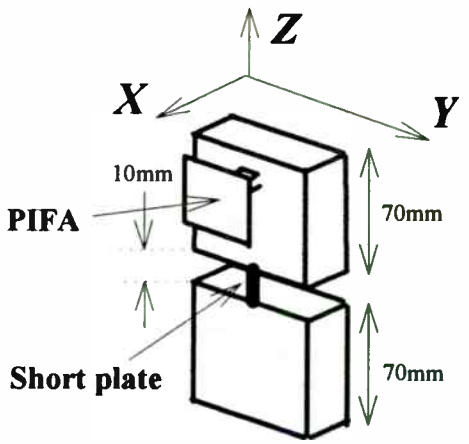

Fig. 10. New PIFA system on the handset.

As the same as $\lambda/4$ monopole antenna, the new structure for PIFA is shown in Fig. 10. The new one consists of two conducting boxes and a short plate as a passive load connecting two boxes divided from the one box of the conventional structure. The passive load is placed between the lower side center of the upper box and the upper side center of the lower box. The values of the passive load Z_L can also change the antenna patterns. The short plate width and the separation distance between two boxes are not important.

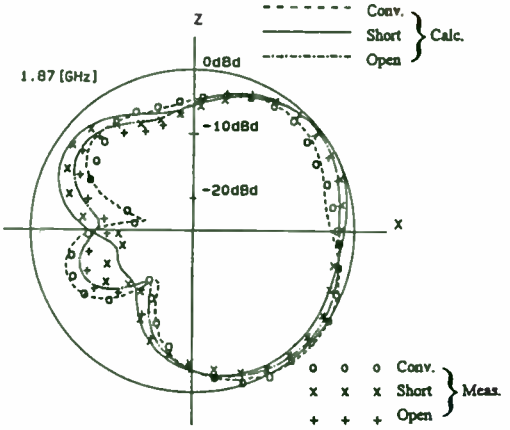

Fig. 11. The calculated and measured antenna gain pattern of the new structure and the conventional one in the ZX plane, in free space.

In Fig. 11, the calculated and measured G_θs in the ZX plane are plotted for the conventional structure, the open ($Z_L = \infty$) and short states ($Z_L = 0$) of the new structure. The short state improves the maximum gain 2.2 dB and the average gain increases by 1.0 dB in the horizontal (XY) plane. Also the antenna patterns are changed according to the values of the passive load.

Whereas the maximum gains and the average gains in the ZX plane are almost the same irrespective of the structures, G_θ of the short state has no null, or smooth variation, and becomes higher above the upper half plane ($Z \geq 0$). This characteristic is a great advantage because the incoming electromagnetic waves are expected to be from the upper hemisphere (the most base stations for PCS and PHS are expected to be higher than the handsets).

The average and maximum gain to reactive load is shown in Fig. 12.

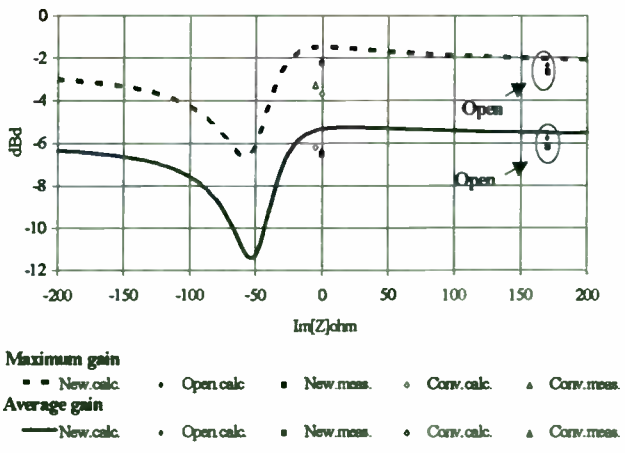

Fig. 12. The maximum and average gains of the new structure and the conventional one for the passive load that is purely reactive, in free space.

From the figure, the maxima of the average gain and the maximum gain are obtained at ZL=0.

D. New PIFA system on a handset near human head and hand

To examine the effect of human on the antenna gains, we consider the PIFA system near human head and hand modeled in Fig. 13. The distance between hand and handset is 6.5 mm apart.

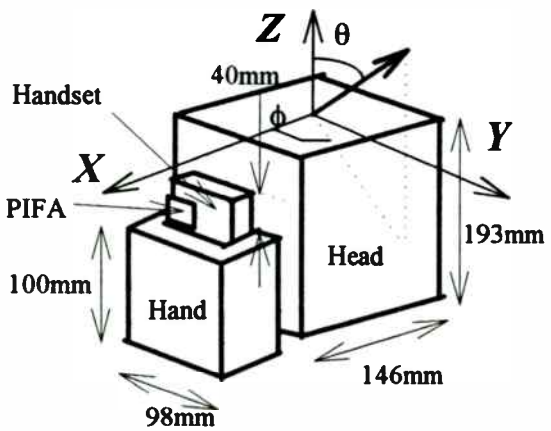

Fig. 13. Geometry of PIFA on the handset near head model and hand model.

From Fig. 14, the maxima of the average gain and the maximum gain are attained at ZL=0 even near the head and hand.

To compare the average and maximum gains of the new system and the conventional one, we calculated the gains vs. the shortest distance between the handset and hand as in Fig. 15. The figure shows the average and maximum gains for both cases and also shows the gains near only the head and in free space. The new PIFA

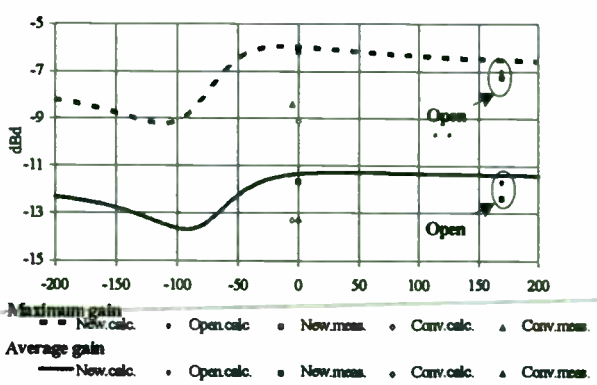

Fig. 14. The maximum and average gains of the new structure and the conventional one for the passive load that is purely reactive, near head and hand.

system is always superior to the conventional system irrespective of the distance, or surroundings.

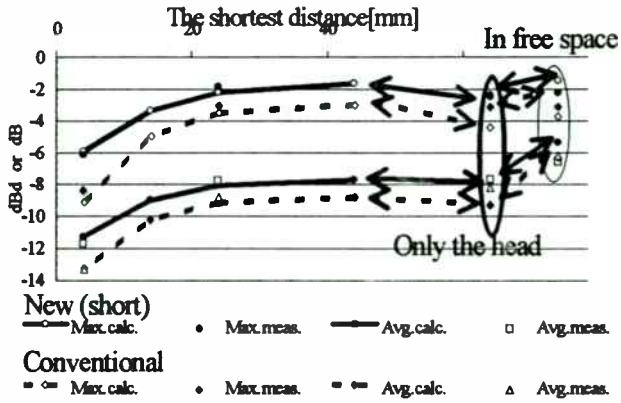

Fig. 15. The measured and calculated average and maximum gains vs. the shortest distance between the handset and the hand for the new PIFA system and the conventional system. The gains in free space and near only the head are also plotted.

IV. Summary

We have derived the line integrals converted from the surface integrals appearing in the problems of electromagnetic scattering and antenna. By the newly derived line integrals, efficient and accurate calculation of electromagnetic field and the method of moments can be done. The line integrals are most efficient at the observation point very close to the source region compared to the corresponding surface integrals even with extracted singularities in the integrands.

Using the new line integrals in the moment method, we have proposed a new built-in antenna system on a handset for PCS or PHS at 1.9 GHz band. The λ/4 monopole antenna and the PIFA system on the handset successfully enhance the horizontal plane gain and control the antenna pattern.

Compared with the conventional antenna systems, the new ones have the merits of

1. the improvements of 2.2 dB for the maximum gain and 1.0 dB for the average gain of the PIFA in the horizontal (XY) plane, in free space,
2. the 5 dB gain improvement of the λ/4 monopole antenna in the XY plane, in free space,
3. changing the pattern according to the values of the passive load, and
4. the improvements from 1 dB to 3 dB in close proximity to the head and hand (decreasing the distance between the hand and the PIFA makes the improvement larger).

We will also apply the new structure to other antennas like microstrip antenna, loop antenna, and etc.

Acknowledgment

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Front end concepts for 3V GSM, PCN and PCS handies

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Introduction

Cellular telephones, 15 years ago nobody knew what they were. Today they are almost a way of life. The ever decreasing cost, size and phone tarifs of these handy phones or handies as they are called have proved to be the two key elements in reaching this position. Further reductions in cost and size can be achieved by moving away from the 5-6V supply voltage use in most handies to a 3 cell, ie 3.0-3.6V supply. At least at first glance this poses some problems to the handy developer; how to offer the same high level of performance at this low supply voltage. The rf front end is especially critical here. 3V designs must offer equal or better performance than their 5V predecessors. Thus a new range of low cost, high performance 3V front end devices and concepts are needed. In this paper new parts are presented for the three typical front end applications; power amplifier, low noise amplifier and transmit/receive switch.
When looking for parts for these applications cost of the particular part together with the cost of the surrounding subsystem and system are of utmost importance. But one musn't forget other crutial aspects such as design flexibility, ease of design, and availability of low cost SMD packaging when deciding which parts and which concepts to use.

Low noise amplifier

Handy user swear by their handy because they can ideally be reached "anywhere". Handies must have a very high input sensitivity to offer this kind of service. The performance of the low noise amplifier defines the sensitivity. Performance sacfrificed here costs a multiple of the front end to recover in the backend if at all possible. Thus for devices for future LNA applications must not only be capable of working a 3V supply, they must also offer even lower noise figure and higher gain at 3V than the devices used now in 5V handies. This sort of performance can only be achieved by choosing a totally different silicon technology or looking towards GaAs devices. Now Siemens offers both of the above with the new SIEGET rf biploar transistors series and CGY60 respectively.
The SIEGET transistors offer unsurpassed performance for bipolar transistors [1]. These transitors with a typical transition frequency of 25GHz are designed for use as low cost high performance LNA's. At 1.8GHz they have a noise figure of 1.1dB and an associated gain of 15dB, all at 2V supply as shown in figure 1.

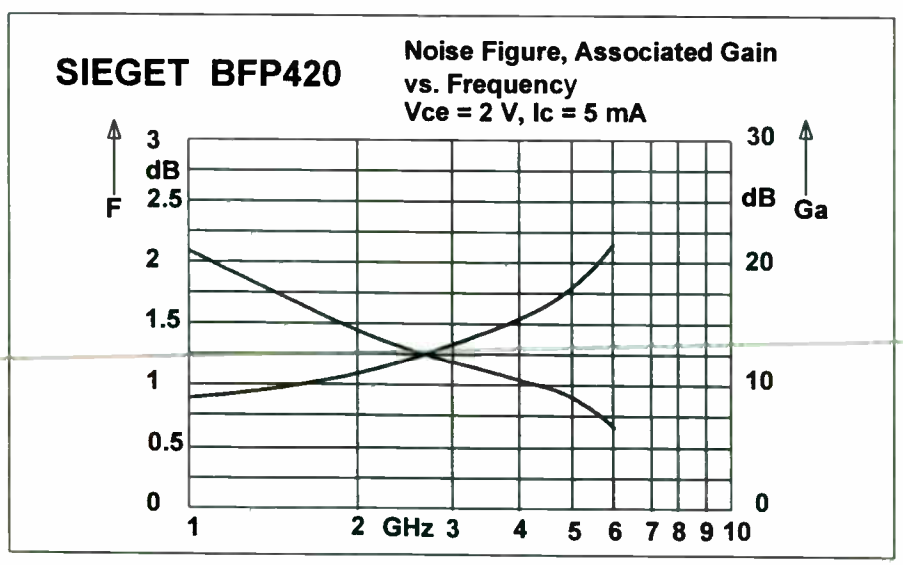

Figure 1 : Performance of BFP420 as LNA

Table 1 gives an overview of the performance available. Because they are silicon bipolar transistors they are easy to match. SIEGET transistors are available in the super miniature SOT343 package.

Part	f_T	IC_{max}	F_{min}	G_{ma}/G_{ms}	IP3	P_{-1dB}
BFP405	25GHz	12mA	1.15dB	22dB	15dBm	5dBm
BFP420	25GHz	35mA	1.05dB	20dB	22dBm	12dBm

Table 1 : Performance of SIEGET rf bipolar transistors at 1.8GHz and 3V supply

CGY60 is a GaAs MMIC for low noise amplifier applications. It offers outstanding rf performance coupled with 50Ω input and output matching thus reducing design times. At 3V supply CGY60 has a noise figure of 1.85dB and offers 12.5dB associated gain. With more than 25dB of reverse isolation, the CGY60 is also excellent for use in buffer applications. CGY60 is available in the MW6 package, a 6 pin derivate of the SOT143 package.

Power amplifier and transmit receive switch

The electrical as well as the economical feasability of a 3V power amplifier (PA) depends not only on the PA itself but also on critical parameters of components before and after the PA. In particular we need to look at noise produced by the RF VCO and modulator, and at the losses incurred between PA and antenna. As will be shown these two are very closely related.
Modulator and VCO dispertion noise are inherent products of rf signal modulation. They can be thought of as a noise floor in the transmit band. In DCS systems such as GSM and PCN, intermodulation and mixing between the modulated carrier and this transmitter noise in a non-linear PA will transform a part of this transmit noise floor into the receive band as shown in figure 2. The GSM specification clearly defines the maximum values for this transmitter noise in the receive band ie. max -79dBm. Should this value be exceeded then the excess noise **must** be filtered out with highly selective and expensive duplex filters between PA and antenna. This is a solution but not the ideal solution since these filters incur high losses between the PA and the antenna. This means that extra output power must be produced, ie we need a larger PA chip which in turn leads to a higher current consumption. This leads to higher cost and reduced talk time.

f_T
carrier

f_N
noise in transmit band

$2f_T-f_N$
shifted noise in receive band

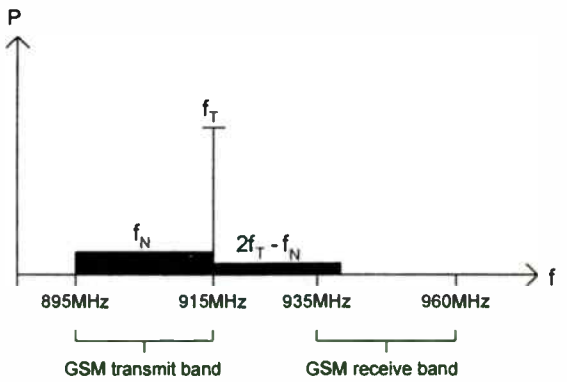

Figure 2 : Transmitter noise in the receice band (GSM)

Unlike FM systems (eg. AMPS and ETACS), TDMA systems such as GSM, PCN and PCS1900 do not require duplex filters. So why use them! Under ideal circumstance the duplexing can be done using a transmit/receive switch. These switches offer insertion losses well under 0.5dB (depending on frequency) in comparison to the >2dB for the duplex filters. If a transmit/receive switch can be utilised then we have achieved one of our goal, ie reducing losses between PA and antenna to an absolute minimum. Prerequesite for this is a low noise modulator. So here we see why the performance of component before and after the power amplifier must be considered. It is also obvious that transmitter

optimisation not only aids the realisation of an ecomical 3V PA, we have also paved the way for considerable cost savings and increased talk time.

The first priority when chosing a pin diode switch is hence finding diodes which offer lowest possible insertion loss. Second priority is selecting a diode configuration such that the signal from the PA is not distorted. The best configuration for this case is the series shunt configuration shown in figure 3 [2].

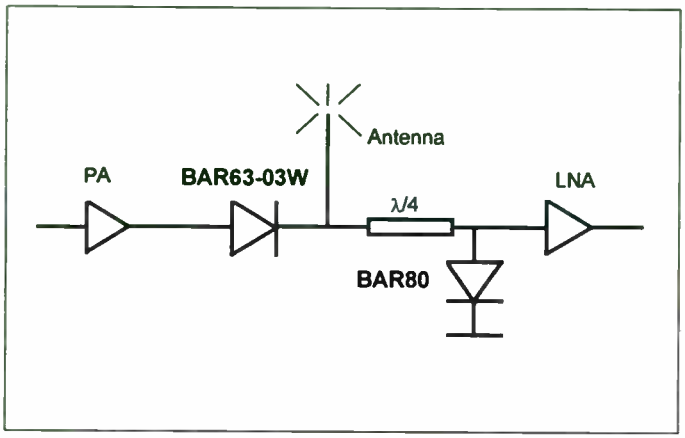

Figure 3 : Series shunt antenna switch with BAR63-3W and BAR80

The λ/4 stripline can alternatively be replaced by an L C combinations shown in figure 4 saving valuable board space.

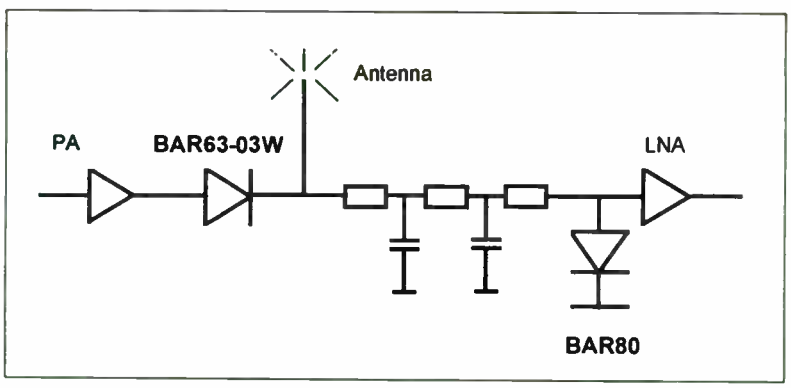

Figure 4 : Series shunt antenna switch with λ/4 stripline replaced by shortened striplines and discrete capacitances

The advantages of the series-shunt configuration is that it consumes no current in receive mode, it requires no negative voltage, and also requires only one switching voltage of <3V. Both diodes shown in figure 3 and figure 4 have been optimised specifically for use in their respective applications, ie the BAR63 has been designed specifically for use in series configuration and the BAR80 for use in shunt configuration. The typical performance of such a switch at 1.9GHz is shown in table 2.

Transmit			**Receive**	
Insertion loss	Isolation	Harmonics	Insertion loss	Isolation
0,4dB	24dB	-87dB (2^{nd})	0,45dB	19dB

Table 2 : Performance of PIN diode switch with BAR63 and BAR80 at 1.9GHz

Assuming that all above mentioned criteria for a 3 cell handy are now fulfilled we can now move on to the power amplifier itself. The requirements for the PA are fairly simple at first glance; high power and high efficiency, ideally at or below 3.6V supply . This is exactly the domain where GaAs has an

inherent advantage over silicon. GaAs transistors may be more expensive than their silicon counterpart when comparing transistor for transistor, the situation in the handy however must be reviewed from a system perspective. If, as will be shown, GaAs can offer the necessary power at or below 3.6V supply where silicon requires 5V or more to offer similar performance, then GaAs can offer substantial savings.
3V power amplifier are already available for systems such as DECT and PHS. There the Siemens 3-stage GaAs MMIC CGY180 has already shown that GaAs MMIC technology is ideal for these low voltage, high performance PA applications [2]. The above mentioned systems specify output powers less than 1W. For GSM, PCN, and PCS systems required output power levels at the PA output are well over 1 W, for GSM over 2W. It can now be shown that the afore mentioned GaAs MMIC technology is equally ideal for these high output powers.
For GSM 2W of rf power are required at the antenna. The best transmitter designs have losses as low as 0.5dB between PA and antenna. Thus the ideal GSM power amplifier should be capable of an output power of 33.5dBm. With the CGY94 Siemens offers the first PA capable of delivering more than 2W of rf output power at 3,6V. Together with the variable gain amplifier CGY120 as driver, more than 40dB gain is available. The CGY94 works in the near linear A/B mode and still offers over 45% efficiency. The input is matched to 50Ω, at the output there is a prematch giving the developer flexibility whether he wants to match for optimum output power, maximum gain or maximum efficiency. Contrary to silicon PA modules, CGY94 is available in a plastic MW12 package (12-pin derivate of SOT223 package). Table 3 gives a complete overview of the performance of the GSM PA line up.

Application	Test Results @ 3.6V					Device Selection	
	Pi dBm	PO dBm	PAE %	VGA	f MHz	1. Stage	2. Stage
GSM	-11	33.5	46	Yes	890 -915	CGY 120	CGY 94
DECT/PHS	0	27	35*	No	1880-1900	CGY 180	
PCN/PCS	-8	32	40	Yes	1710-1785	CGY 120	CGY 181

* lower than other PA's since 3 stage MMIC

Table 3 : Performance of GaAs power MMIC's at 3.6V

Similar criteria are valid for PCN and the 1W PCS systems in North America. A minimum of 31.0dBm (accounting for higher losses at higher frequencies) output power are required at or below 3.6V supply. Again Siemens offers a GaAs MMIC capable of delivering the required rf power at these low supply voltages. The CGY181 delivers 31.5dBm output power at 40% efficiency at 3.6V supply. The input and output matching are as with the CGY94. The package is identical to that of the CGY94. Again the CGY120 is ideal for use as a driver for the CGY181. Table 3 also gives a complete overview of the electrical characteristics of the CGY181.

Conclusion

With the availability of of SIEGET rf bipolar transistors, low loss PIN diodes such as BAR63-03W and BAR80, and GaAs MMIC for PA applications, 3cell GSM, PCN and PCS handies are very realistic. The above mentioned devices are the ideal building blocks for low cost high performance 3 cell applications.

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Personal Satellite Communications and Cellular Interworking

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Introduction

As the world becomes more reliant on mobile personal communications systems, users will need to have the assurance that communications will always be available, no matter where the caller or correspondent roams. Cellular systems, because of their essentially local - and sometimes - incompatible, nature cannot provide this assurance on a global, or even regional, basis. Total, anywhere, anytime, anyplace reliability can only be provided by a satellite system. COMSAT, the world's only global mobile satellite operator, is a natural choice.

Already a leader in the global Inmarsat system, COMSAT is launching a daring initiative to bring a new generation of Personal Satellite Communications to people worldwide. The core of this new personal satellite communications revolution is the integration of high quality wireless communications, personal mobility management and global coverage - into one new technology that will offer digital voice, data and enhanced calling capabilities to international business travelers on a regional, national and global basis.

When fully developed, Personal Satellite Communications will enable individuals who live or travel in remote areas to call anywhere in the world, from anywhere in the world, on a portable phone that is inexpensive, compact and easy to use.

The target is to provide global hand-held Personal Satellite Communications service by the year 2000. Studies in support of a global Personal Satellite Communications service have shown that a conservative estimate of the world wide demand from business travelers or anyone whose work takes them beyond the reach of fixed or compatible cellular systems - will exceed several million users by the year 2005.

To prepare for handheld, COMSAT has put together a management team to develop the world's first Personal Satellite Communications service, Planet 1. Introduction of Planet 1 service is planned for introduction by the third quarter of 1996 and will operate with the Inmarsat-3 satellites. The Inmarsat-3 satellites are a new generation of more powerful satellites incorporating spot beams to achieve enhanced EIRP and G/T permitting higher traffic density and the use of smaller and lower cost user terminal. With ten times the power and six times the capacity of the current Inmarsat satellites, the Inmarsat-3 satellites will enable COMSAT to serve the needs of business professionals well in advance of competing satellite systems. Construction of Inmarsat's third generation satellite system is well underway, with the first launch scheduled for February 1996.

The Planet 1 services currently under development are being planned to incorporate a number of advanced features.

- **Voice service quality as good as cellular**

Based on low bit rate, high quality AMBE digital voice encoding, the Planet 1 service will provide voice quality similar to that of digital cellular systems.

- **Global roaming with single number regardless of location**
  Planet 1 service supports the use of subscriber identity modules (SIMs), Personal 500 numbers and location databases. Personal mobility is the capability to route a call to a mobile user regardless of their location.

- **Cellular network integration**
  The Planet 1 mobile satellite switching center (MSSC) supports the same signaling standards used by cellular and PCS operators throughout the world.

- **Voicemail, paging and short message service**
  Optional messaging services enable business travelers to keep in touch across time zones thereby increasing the productivity of mobile communications.

- **Call management services**
  Advanced call management services will enable the mobile user to control whose calls are forwarded, who pays and or which calls are diverted to voicemail.

Planet 1 System Overview

The current Inmarsat-M system is designed for operation with Inmarsat's first, second and third generation space segment, thus operating to both global and spot beams. An evolved system, "Planet 1", is planned for introduction by mid-1996 with operation limited to Inmarsat-3 spot beams so as to minimize size, weight and power consumption characteristics in the mobile earth stations.

The Inmarsat 3 satellites will have a total of 1,800 voice channels, compared to the current generation Inmarsat 2 fleet.

Construction on a third generation Inmarsat 3 satellite is already underway and will launch in early 1996. The Inmarsat 3 fleet will provide global beams for signaling and high power 48dBw spot beams for traffic channels. The additional gain available with Inmarsat 3 spot beams enables the Planet 1 terminal to operate with lower transmit EIRP. For land-based terminals, the combined spot beam coverage assuming four operational satellites is almost total, with back-up between spot beams of adjacent satellites.

The Planet 1 terminal will be designed to operate in the Inmarsat-3 spot beams for traffic channels (voice, facsimile and data), and in the global beam for signalling channels. The additional gain available with Inmarsat-3 spot beams enables the Planet 1 terminal to operate with lower transmit EIRP. For land-based terminals, the combined spot beam coverage assuming four operational satellites is almost total, with back-up between spot beams of adjacent satellites.

Products and Services

The basic Planet 1 service objective is to provide full, two-way digital voice communications to and from notebook sized terminals. The LESs, in turn, provide the connection to the worldwide public switched telephone networks. Voice quality will be similar to that of digital cellular phones.

The COMSAT Planet 1 terminal will be the smallest, lightest personal satellite terminal in the world. In addition to providing digital voice, Planet 1 will support group 3 facsimile and circuit-switched data services. Value added services such as voice mail, paging and short message service for displaying the number of a caller or for voice mail alerting and ISDN supplementary calling services.

The Planet 1 terminal is expected to be available in mid-1996 with the end user price targeted for sale to end-user's at $2,995. The Planet 1 terminal includes a corded handset and cradle, battery pack and AC charger and power cord.

A summary of the Planet 1 basic and value-added services are summarized below.

Basic Services

- 4.8kb digital voice, 2.4kb fax and data
- Authentication of Subscriber Identity Modules (SIM)
- Call Forwarding from cellular networks
- Emergency speed dial number
- Inmarsat number plan (76 dual T-digit)
- Mobility management
- Operator assistance (directory inquiries and call extension)
- Personal identity for SIMs

Value Added Services

- Carrier presubscription
- Cellular Integration Function (CIF) for SIMs
- Debit card
- Voice mail/ Fax mail
- ISDN supplementary services
- PCS 500 number services
- Secure communications
- Short message service (SMS)

Personal Mobility Management

To enable personal mobility management and authentication, Comsat shall implement a location database of the mobile user at each LES. On the terminal side, a SIM card similar to that used in the GSM system, shall be applied as the enabling technology of Comsat's personal mobility

management and authentication functions.

When the mobile user roams to a different ocean region, their personal id is forwarded in the ocean region registration message. In addition to the personal id, each subscriber has their own Inmarsat Mobile Number (IMN). This method allows the SIM card holder to use any terminal, for example, a rental terminal or lease terminal.

In addition to personal mobility SIM cards will enable streamlined access and dialing.

The SIM improves security for the mobile user in two ways.

- Passive authentication utilizing a personal identification number (PIN). If the PIN code presented corresponds with the one stored on the SIM card, then the authentication is successful.

- Active authentication utilizing a random number passed-on by the LES and an algorithm with a unique key stored on the SIM, to calculate a result. The same calculation is performed by the LES. If the results correspond, the authentication is successful.

Cellular Interworking

The Planet 1 network will be able to interwork at different levels of integration: call forwarding and location registration, i.e., roaming. Call forwarding between the cellular networks and Planet 1 requires user cooperation. The user must manually forward the fixed-originated calls placed to the cellular number to the Planet 1 subscriber's satellite telephone number.

The Cellular Interworking Function (CIF) will be implemented in COMSAT's land earth station (LES) and Planet 1 terminal. The goal of CIF is to allow seamless interworking between COMSAT's Planet 1 network and the GSM/PCS networks, by making the satellite network seem to appear just as another cellular or personal communications network that a GSM/PCS subscriber has the option of "roaming" into. The implementation of this function will allow a GSM or PCS subscriber with a standard GSM SIM card to insert the card in the Planet 1 terminal which implements this option, and thereafter be reachable internationally via the Inmarsat Mobile Subscriber Identity (IMSI) number available on the SIM card. The GSM customer will be billed directly by the GSM/PCS service provider for "air-time" on calls made/ received by the Planet 1 terminal.

The design of the Inmarsat systems in the past, have traditionally focused on the radio access subsystem without specifying the supporting network infrastructure. Specifications were developed principally to handle the communications access over the satellite air interface. Given the small market size and the limited mobility of terminals, the need for location and service information databases and network infrastructure was not justified. However, the evolution towards Planet 1, and beyond, will greatly change the past service matrix. In addition to the potentially much larger market, the use of new generation spot beam satellites and mobile terminals of sufficiently reduce size and costs will greatly expand mobility and service

management requirements.

To address the emerging requirements for the support of mobility and service management, since one of the central elements of mobile communications is mobility management, COMSAT Mobile Communications (CMC) is taking the lead over other Inmarsat Land Earth Station Operator's (LESO's) in expanding its network infrastructure capabilities. The GSM network and switching subsystem will be adopted by CMC to support the necessary mobility and services management and allow for integration with the Planet 1 satellite radio access system. The GSM system provides the best solution today for supporting international interconnectivity among mobile networks.

Efficient and seamless provision of a range of enhanced and value added services is one of the goals of CMC's network. GSM provides a rich and diverse set of mobile network features and communications service capabilities. Many of the features desired for the COMSAT Planet 1 service are being offered today with GSM. With this in mind, CMC intends to model its own network architecture after the GSM standard to take advantage of the existing proven technology and equipment. The interworking of the GSM Network, switching subsystem and Inmarsat satellite radio access subsystem will also allow the various capabilities of global satellite communications to be offered in conjunction with an array of standard and value added mobile network service features.

In addition, adoption of the GSM network technology will create the opportunity to develop global roaming services across compatible network systems service features. The integrated network will serve to establish the presence of the CMC satellite system in the wider arena of standard communications networks and will facilitate standard service offerings and signaling system connectivity to national and international mobile and fixed terrestrial networks.

The GSM standard for mobile cellular communications is truly emerging as a global standard for personal communications. network operators are already established in Europe and are emerging in developing countries as well. These network operators are already established in Europe and are emerging in developing countries as well. These operators already have a large base of customers to whom they have issued GSM SIM cards. These cards allow for personal mobility of GSM cellular customers well beyond their own home Public Land Mobile Networks (PLMN's) through well defined interworking schemes and agreements between network operators. It is envisaged that CMC will have the opportunity to provide service to members of this large subscriber base that wish to have convenience of total global mobility using the Planet 1 system as a seamless expansion of the terrestrial PLMN's.

The GSM SIM interworking function developed by COMSAT is an optional function that may be implemented by any Inmarsat LES operator and an mobile equipment manufacturer. The goal of this function is to allow seamless interworking between the Inmarsat satellite network and GSM networks, by making the Inmarsat satellite network appear as just another GSM network that the GSM user has the option of roaming into. The implementation of this function will allow a GSM subscriber with a standard GSM SIM card to insert this card into a mobile satellite terminal (which implements this option), and thereafter be reachable (globally) via the subscribers standard

GSM directory number (MSISDN) associated with the SIM card. The GSM customer will be billed directly by the GSM service provider for 'air time' on calls made/received by the Inmarsat mobile equipment.

Conceptually, a GSM subscriber of XYZ Telecom in country A would be able to insert the GSM SIM card issued by their service provider into an Inmarsat mobile satellite terminal and be allowed to make and receive calls through any Inmarsat LES that had executed an intercarrier agreement with XYZ Telecom. The LES operator would then not deal directly with the individual subscriber, but instead execute settlement agreements with XYZ Telecom for their subscribers use of the LES and satellite network. The subscriber would see the mobile satellite calls itemized on their cellular telecom invoice, in much the same way as calls made to/from the user when roaming in a foreign PLMN.

Mobile Station Test Using the HP 8924C

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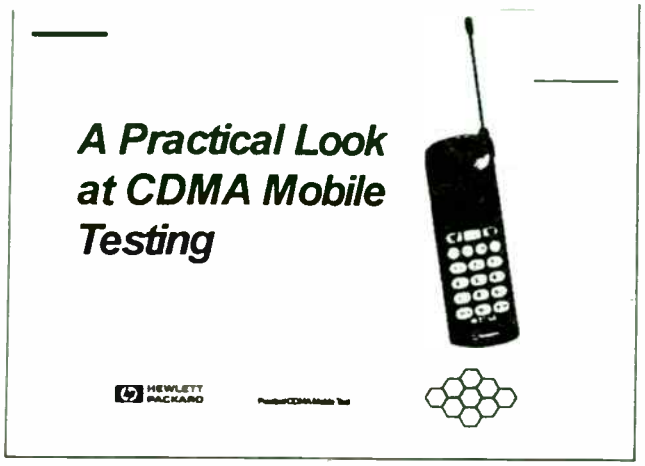
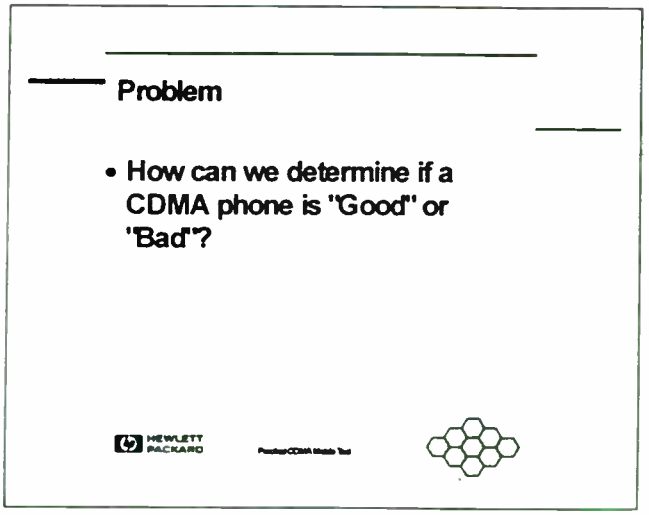


Welcome to "A Practical Look at CDMA Mobile Testing." IS-95 CDMA is about to go commercial. Based on the CDMA system developed by Qualcomm Inc., this new standard for cellular phones provides an alternative digital system for the cellular market. This new technology brings with it not only promises of much higher capacity and improved service, but also challenges for those who must install, maintain and service the system. This paper will not try to explain the CDMA system and its workings (see reference list in the Appendix), but will rather try to take a practical look at the question of "How can we determine if a CDMA phone is working properly or is broken?"

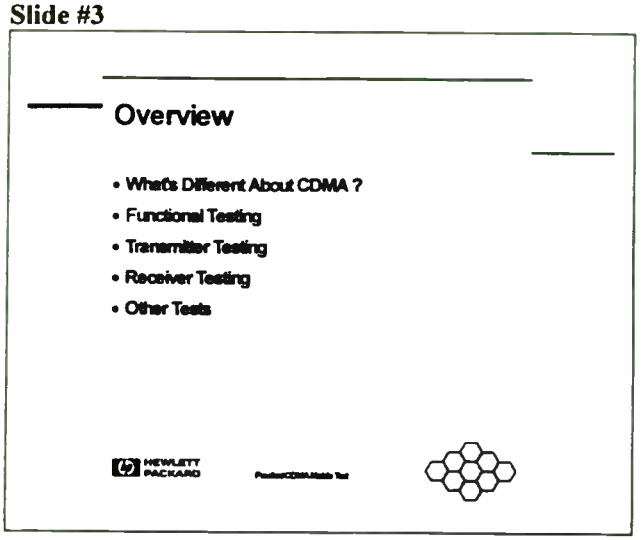
Slide #2



Lets assume that CDMA has gone commercial, and we have been given the task to figure out how to test these new phones. This testing could be for incoming inspection, to make certain the phones are in good working order before we give them to our top customers, or it may be to determine if a phone is truly "broken" when a customer brings it into a service center. Our problem is to determine if the phone is "Good" or "Bad".

Lets define what we mean by "Good" and "Bad". A "Good" phone is pretty self-explanatory – it functions properly and meets its specifications. A "Bad" phone can come in a couple of flavors – it may not work at all, or it may function at nominal signal levels, but have problems with power, noise or interference making it "broken".

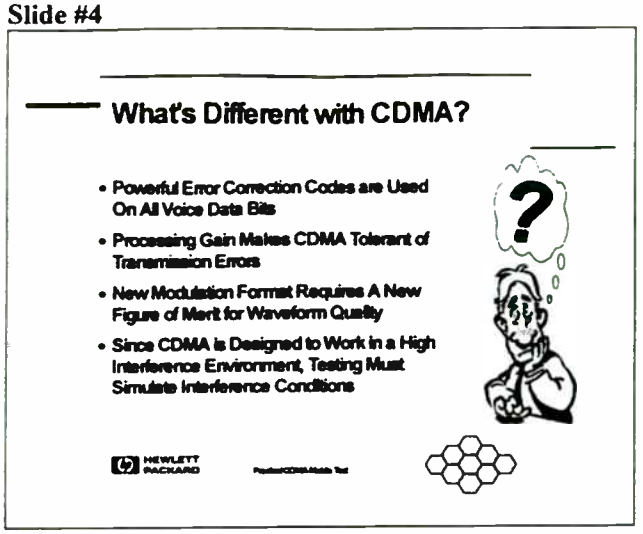
Slide #3



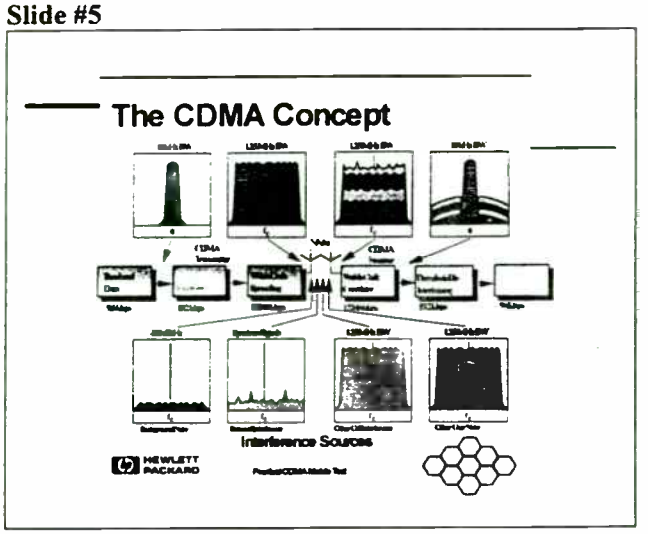
Before we delve into the testing of CDMA phones, lets remind ourselves of what makes CDMA different from analog or TDMA as well as what is required to actually get a CDMA phone up on a link. After we lay this foundation, we will explore how to determine if the phone is working or if it is broken and needs to be repaired.

Practical CDMA Mobile Test

Slide #4



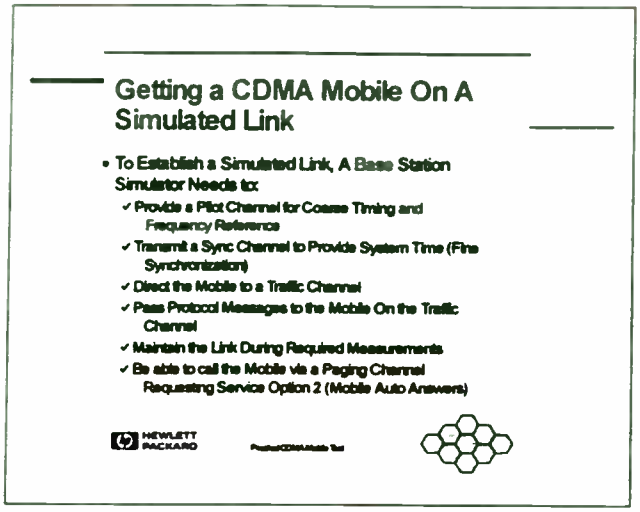
Slide #5



CDMA - Code Division Multiple Access - is a variant of direct sequence spread spectrum communications that was originally developed for military communications. This wideband transmission system allows powerful error correction codes to be applied to all of the encoded voice data bits. In addition, the processing gain of CDMA's error correction codes and spreading codes makes the system very tolerant of transmission errors. What would appear a gross errors in the transmitted signal of any other cellular system are normal for a properly operating CDMA mobile. Tradition tests that examine modulation quality (global phase error - GSM, and error vector magnitude - TDMA) and receiver performance (bit-error-rate) do not provide meaningful insight in to a CDMA mobile's performance. Finally, CDMA technology was designed for military communications and was specifically developed to operate with high levels of interference, so testing must duplicate the normal interference levels experienced by a CDMA mobile.

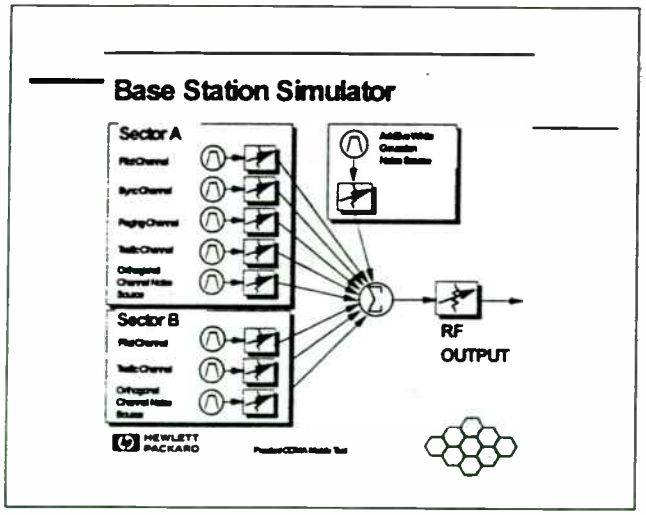
CDMA starts with a narrowband signal, shown here at the full speech data rate of 9600 bps. This is spread with the use of specialized codes to a bandwidth of 1.23 MHz. The ratio of the spread data rate to the initial data rated is called the processing gain. For IS-95 CDMA the processing gain is 21 dB (at 9600 bps). When transmitted, a CDMA signal experiences high levels of interference, dominated by the coded signals of other CDMA users. This takes two forms: interference from other users in the same cell and interference from adjacent cells. The total interference also includes background noise and other spurious signals. When the signal is received, the correlator recovers the desired signal and rejects the interference. The correlators use the processing gain to pull the desired signal out of the noise. Since a signal to noise ratio of about 7 dB is required for acceptable voice quality, this leaves 14 dB of extra processing gain to extract the desired signal from the noise. This is possible because the interference sources are uncorrelated (orthogonal in the case of the forward link) to the desired signal.

Slide #6



In order to test a CDMA mobile, we must establish a link on a traffic channel. To do this the base station simulator must provide specific signals and protocol messages to establish and maintain a CDMA link. The simulator must provide a Pilot Channel to allow the mobile to get its timing and frequency alignment, and a Sync Channel that broadcasts the state of the Long Code to establish exact system time. To create a link, the simulator must call the mobile via a paging channel and direct the mobile to a Traffic Channel. To maintain the link, the base station simulator must pass any required protocol message and respond correctly.

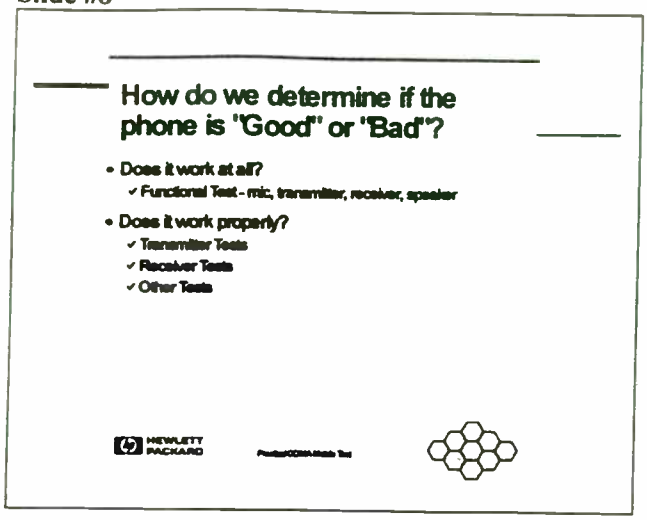
Slide # 7



In Addition to supporting a Pilot, Sync, Paging, and Traffic channels, the base station simulator must provide other channels to simulated the nominal interference presented to a CDMA mobile. Two noise sources are required: an OCNS source to simulate the interference from other users in the same cell, and an AWGN source to simulate the noise from users in adjacent cells, OCNS stands for Orthogonal Channel Noise Source. Since other users in the same cell are encoded with orthogonal Walsh codes, OCNS noise must use a different Walsh code than the one used for the traffic channel link. AWGN stands for Additive White Gaussian Noise. The interference for users in adjacent cells is not orthogonal, but is uncorrelated since they are encoded with the sort sequence (2E15 PRBS) that is offset in time. All of these sources must be accurately calibrated and support relative amplitude resolution and accuracy of +/- 0.1 dB.

For other testing, such as checking a mobile's ability to hand-off to another sector (softer-handoff), a partial sector consisting of Pilot, Traffic and OCNS may be needed as well.

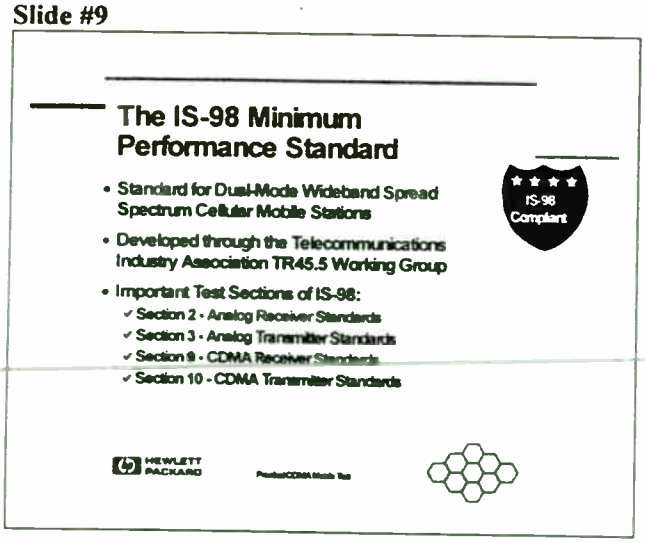
Slide #8



How can we determine if a CDMA mobile is "Good" or is broken and needs to be sent for repairs?

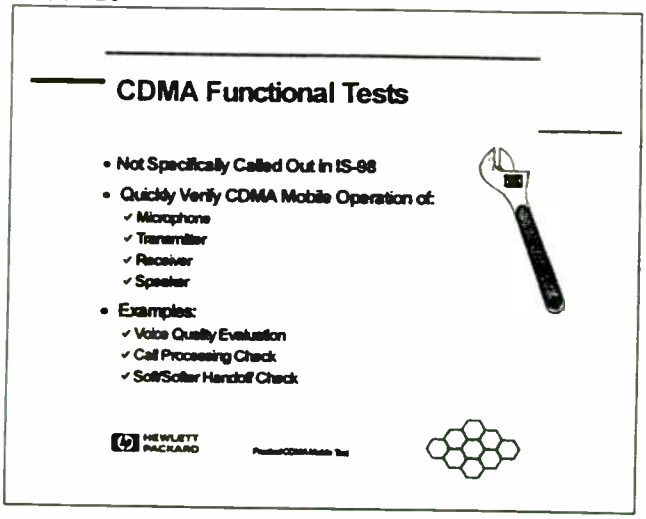
The first step is to determine if it works at all – that is will it function? Once we determine that the phone is functional, we need to ask the questions: "Does it work properly?" "Does the transmitter output a clean, high quality signal?" "Can the receiver process the desired signal at low/high levels as well as reject other unwanted signals?" We may also want to check that the mobile can work properly during the soft hand-off transition between two base stations or sectors.

Slide #9



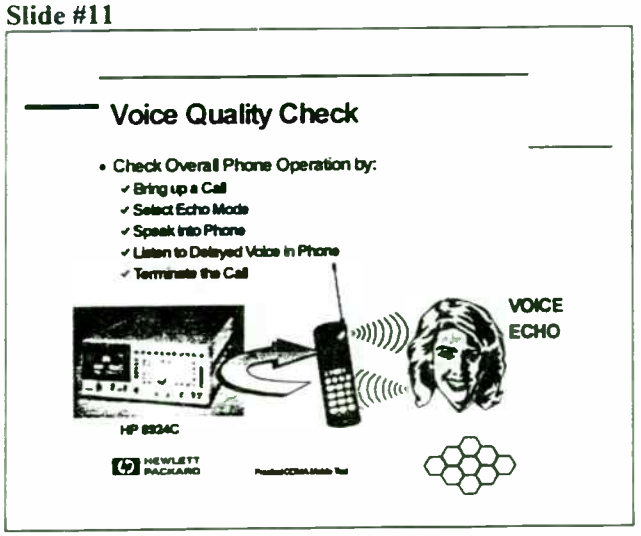
Developed by industry members of the TIA, IS-98 is designed to be an open industry standard to promoted interoperability of equipment (one manufacturer's mobile will work with another manufacturer's base stations). This document specifies minimum standards of performance of environmental, protocol, transmitter, and receiver characteristics for both the AMPS analog and CDMA digital modes. Many of these tests, while important for initial type acceptance and interoperability, will not be performed regularly in typical manufacturing, incoming inspection, or service applications. Accordingly, this paper will refer to this standard for those tests that will be done in manufacturing, incoming inspection, and service applications.

Slide #10



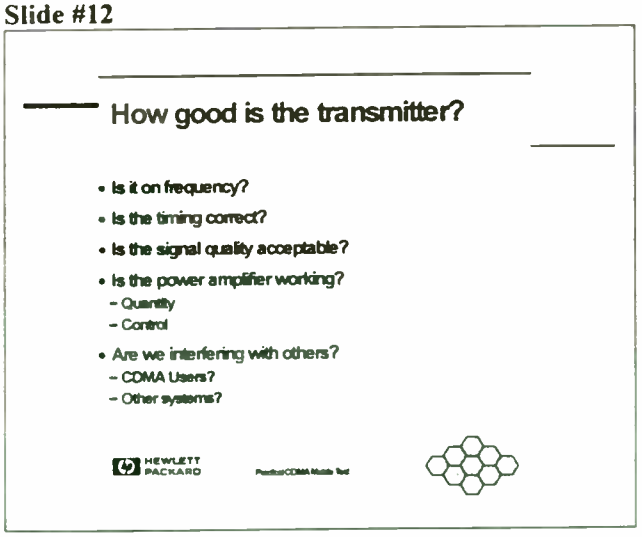
Function testing can quickly evaluate the overall operation of a CDMA mobile with reduced test equipment cost and complexity. Some possible application areas for functional testing include manufacturing final check-out, incoming inspection of mobiles for service providers, or for repair verification in service shops. This testing can give a good indication of a major failure (microphone, transmitter, receiver, or speaker) but may not locate performance problems in the mobile.

Slide #11



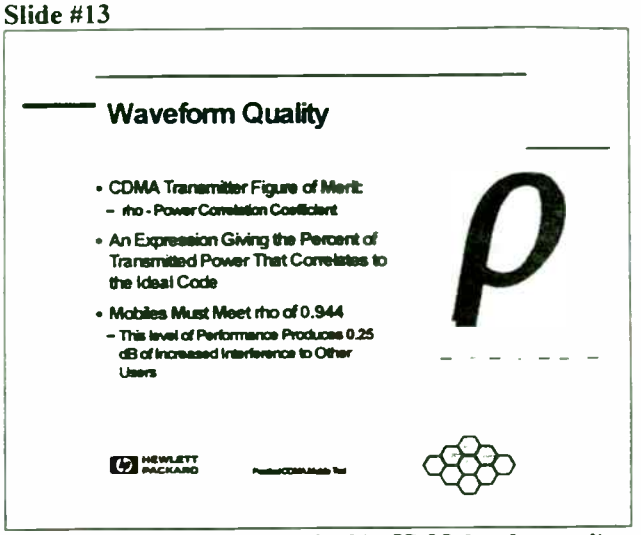
One of the best functional tests of a mobile is the Voice Quality Check. To perform this test, the CDMA base station simulator must be able to bring the mobile up on a Traffic Channel link and then echoes the voice data it receives back to the CDMA mobile. This test check the operation/connections of the microphone, modulator, power amplifier, receiver front-end, rake receivers, audio circuits, and speaker with one simple test set-up.

Slide #12



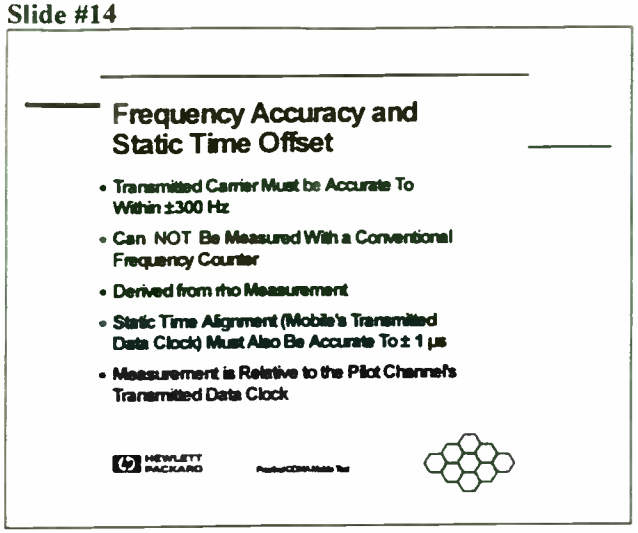
These are some of the questions that we need to answer to evaluate the CDMA mobile's transmitter. The first four check to see that it is generating a signal that the Base Station can receive. The last two really are to ensure that we are not generating unwanted signals that may interfere with other users and/ or systems.

Slide #13

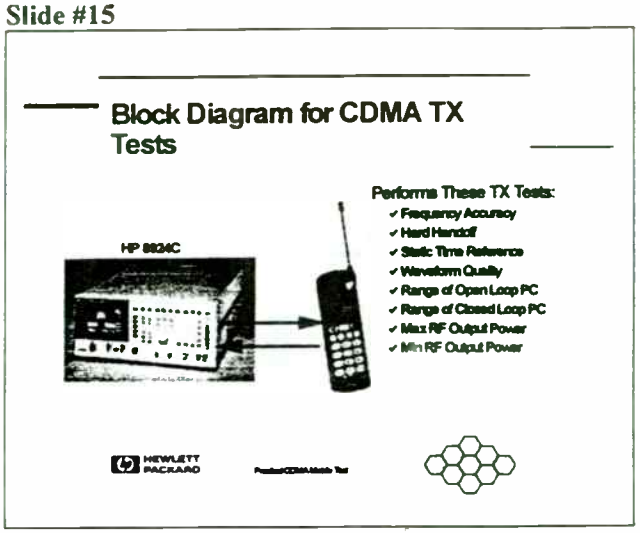


The figure of merit specified in IS-98 for the quality of a OQPSK modulated transmission form a CDMA mobile is called "ρ" (Greek letter rho). The ρ measurement is also referred to as the power correlation coefficient. The concept of the ρ measurement is fairly simple. Although the CDMA system is designed to operate with high levels of interference, the ultimate capacity of any given cell is limited by the total interference (number of active users). For adjacent cells that are equally loaded this limit is about 32 callers per cell or sector. If any mobile's transmitter is not properly encoding each user's data into the required code, some of the transmitted power will appear as increased noise to other users. The ρ measurement computes the power of a CDMA transmitted signal that correlates to the desired code. Thus ρ gives an indication of the increased interference that will be caused by modulation errors in a CDMA transmitter. A ρ value of 1.00 indicates that all of the transmitted power correlates with the ideal transmission code. The specified performance level that a CDMA mobile must meet is 0.944 indicating that 94.4% of the transmitted energy correctly correlates into the ideal code. At this level of ρ performance, the increased noise to other users will be an additional 0.25 dB.

Slide #14



Slide #15

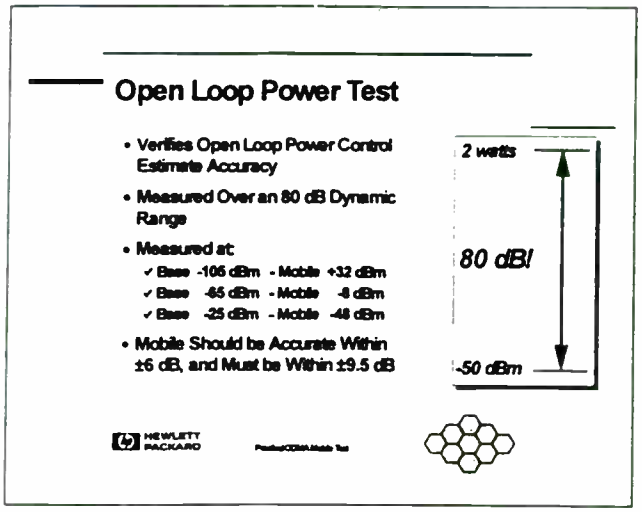


Two other important mobile station parameters derived from the ρ measurement are transmitted frequency error and static time alignment. Since the transmitted CDMA waveform is spread using pseudo-random codes, the resulting RF waveform appears as a block of random noise. A conventional frequency counter cannot accurately measure the center frequency of an OQPSK modulated signal. The value of the frequency error used to maximize the measured value of ρ provides the estimate of the carrier frequency error. In a similar manner, during calculation of ρ, the DSP must derive an estimate for the static time offset. This is a measure of how accurately the CDMA mobile has aligned its timing to the reference signal broadcast by a CDMA base station. Any test equipment that measures mobile station must therefore provide an RF signal emulating the pilot channel transmission of a CDMA base station.

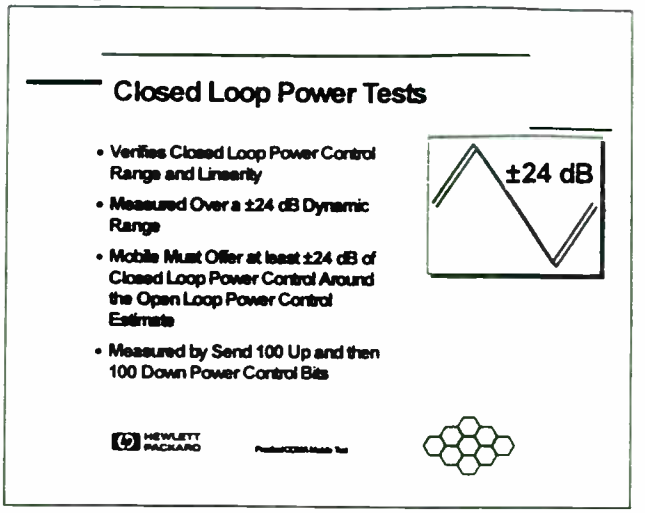
The basic transmitter tests can be performed with the typical block diagram above. The cell simulator is set up at the specified total cell power with each individual code channel at its proper relative power. A call is placed to the mobile (or from the mobile) and maintained while the measurement of interest is performed. The waveform quality measurement reports back the Frequency Accuracy, Static Time Reference, and Correlation Coefficient, ρ, with a single measurement.

Practical CDMA Mobile Test

Slide #16



Slide #17



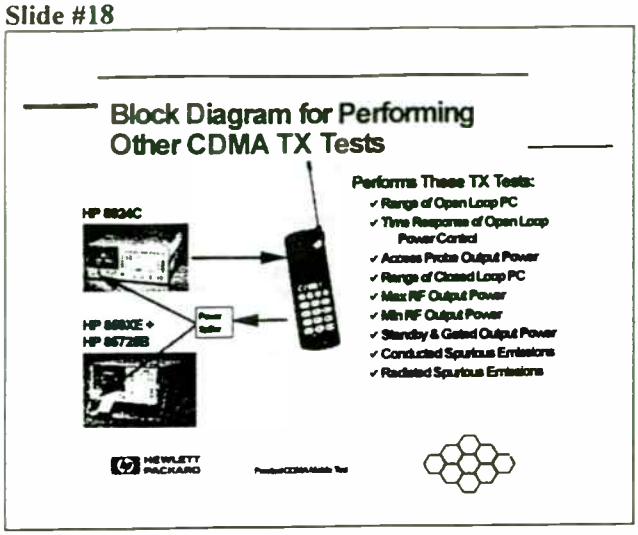
Open loop power control causes a CDMA mobile to monitor the received power from the base station and continuously adjust it output power accordingly. Ideally the mobile must raise or lower its output power linearly for every change in the received power from the base station. Open loop power control follows the following equation with the powers in terms of dBm

Mobile TX Power = -73 - Received Base Power

To measure the accuracy with which a CDMA mobile performs open loop power control, a mobile must first be actively transmitting and monitoring the signal level from a CDMA base station simulator. By then changing the output level of the pilot channel and measuring the response of the CDMA mobile, the open loop power control performance of the mobile can be verified.

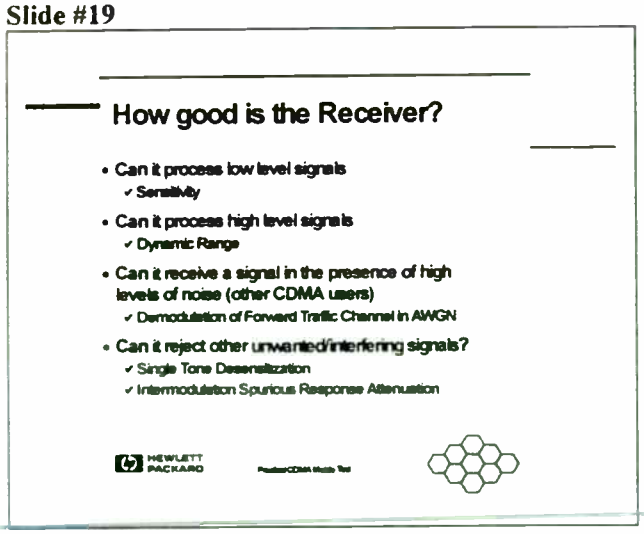
For closed loop power control, the base station directs the mobile to fine tune its output level. Based on the received level, the base station commands the mobile to increase or decrease its output power by 1 dB every 1.25 milliseconds (800 times per second). The standard method of testing closed loop power performance involves verifying the overall range and linearity of the closed loop power dynamic range. A CDMA mobile must demonstrate a +/-24 dB closed loop power dynamic range as well as have a well defined slew rate as it changes power. To verify performance, the test equipment must first establish a call with the CDMA mobile, then command the mobile to increase its power by over 24 dB and measure that the mobile has increased power at least 24 dB. The mobile must also be commanded to lower its power by at least 24 dB to verify that the mobile can decrease its power by at least 24 dB.

Slide #18



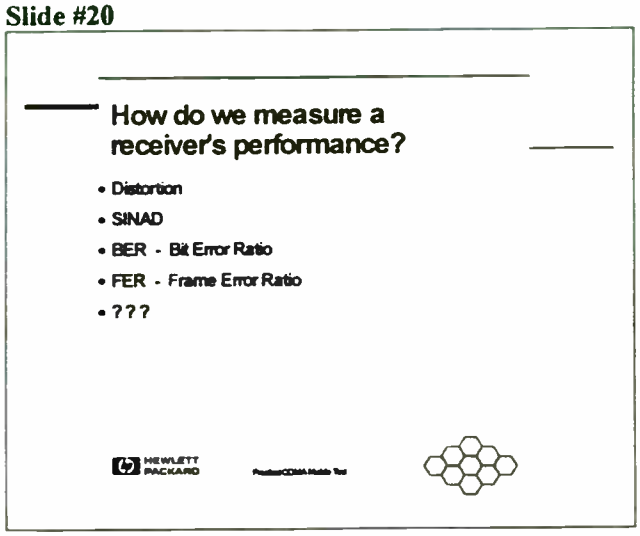
Other transmitter tests can be performed by adding a CDMA spectrum analyzer to our basic transmitter test set-up. The cell simulator (HP 8924C) still is used to establish and maintain the link with the mobile under test, while the spectrum analyzer (with CDMA personality) can make additional measurements of the mobile's transmitter. Many of these tests insure that the mobile is not interfering with other CDMA users and other systems.

Slide #19



We have progressed to the point that we know that the phone was functional and we have determined that the transmitter is in good working order. Now we need to check the operation of the receiver. We know that it functions, now the question is "How well?"

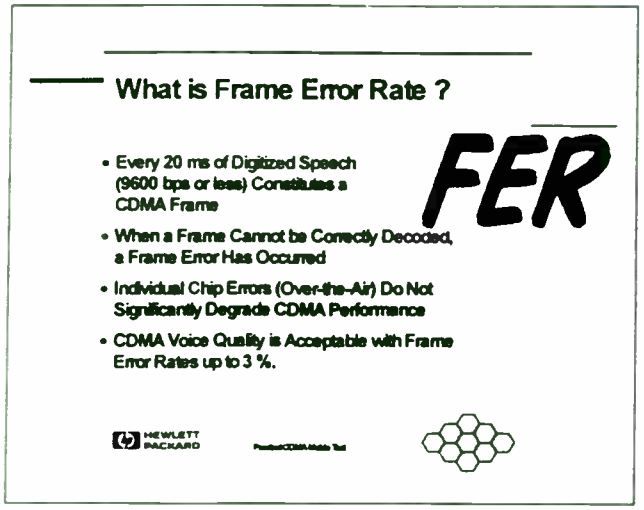
Slide #20



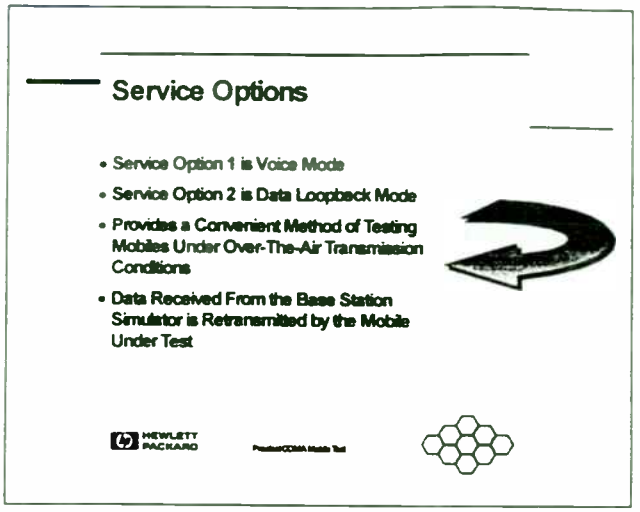
How do we measure the receiver's performance? Remember, a CDMA phone transmits and received digital data to represent the speech. This digital data is a very close approximation, but may differ slightly from the original speech. Analog measurements like distortion and SINAD will not work. Other digital systems, such as TDMA and GSM, use bit error rate measurements to evaluate receiver performance.

Practical CDMA Mobile Test

Slide #21



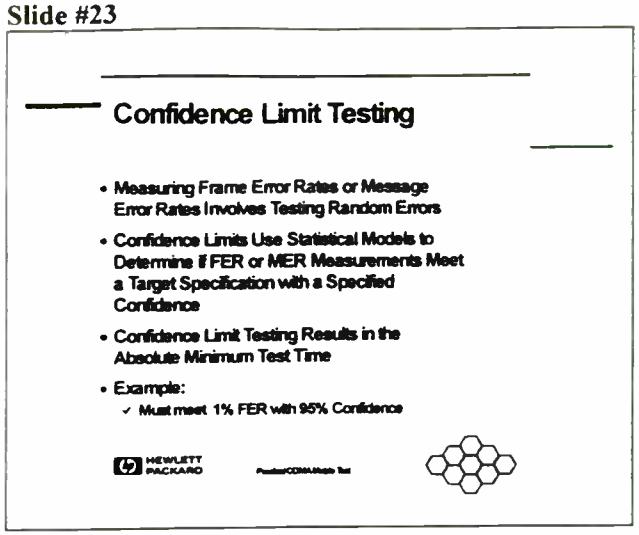
Slide #22



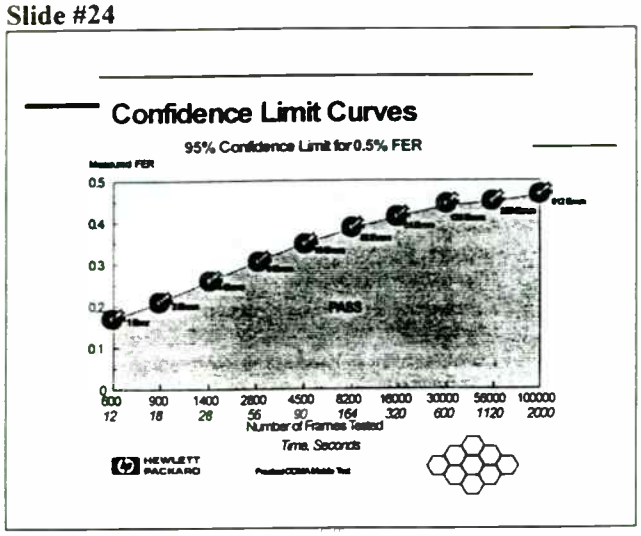
Each CDMA frame contains the digitized voice bits for 2 milliseconds of speech. When a frame has been so corrupted that error correction cannot fix all the errors, a frame error has occurred. Because of the processing gain of the CDMA system, individual bit errors in the received waveform are of little consequence. Bit errors on the physically received signal are usually repaired by the error correcting action of the CDMA codes. Because of this, the traditional test of digital receiver performance, bit-error-rate, does not have any usefulness in CDMA applications. A more meaningful test for CDMA is Frame Error Rate. FER is the true measure of CDMA receiver performance. Corrupted frames in CDMA are not retransmitted and the voice decoder must either interpolate the missing data or mute the audio output. The acceptable level of frame error rate for poor signal conditions is about 3%.

To simplify testing, IS-98 specifies that all CDMA mobiles must support a special service option. The CDMA standard allows for multiple service options to handle future requirements such as data services. Service Option 1 is the normal (9600 bps) speech transmission mode for CDMA. Service Option 2 is the data loopback mode called out in the IS-98 standard. Service Option 2 provides a convenient method to test a CDMA mobile under a simulated over-the-air link. In data loopback mode, the CDMA mobile demodulates the signal received from the base station simulator and then retransmits the same data back to the base station. This allows accurate characterization of the CDMA mobile receiver performance.

Slide #23



Slide #24

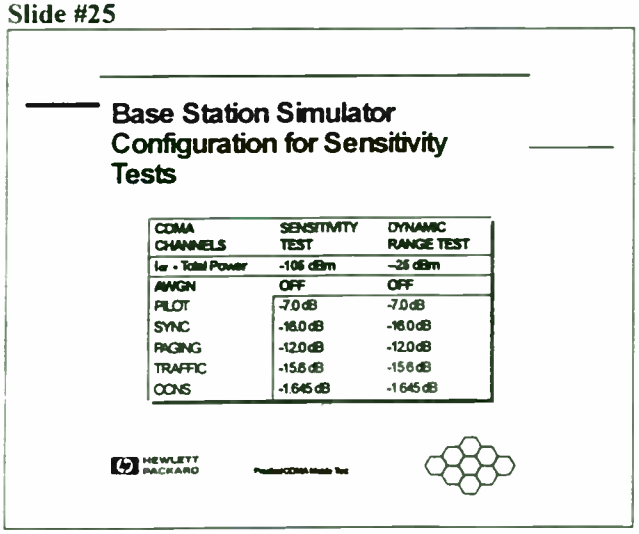


Measuring the error rates of a digital receiver can require lengthy measurements due to the random nature of the errors. Since these errors are random and independent, we must use statistical modeling in order to get a high degree of accuracy when measuring them. In the past, the common solution was to verify the error rate performance by testing a large number of frames or bits. This did provide adequate accuracy, but resulted in excessive test times for FER testing. In order to provide high accuracy without long test time, the TIA committee has specified the use of confidence limit testing when measurement error rate performance of CDMA receivers.

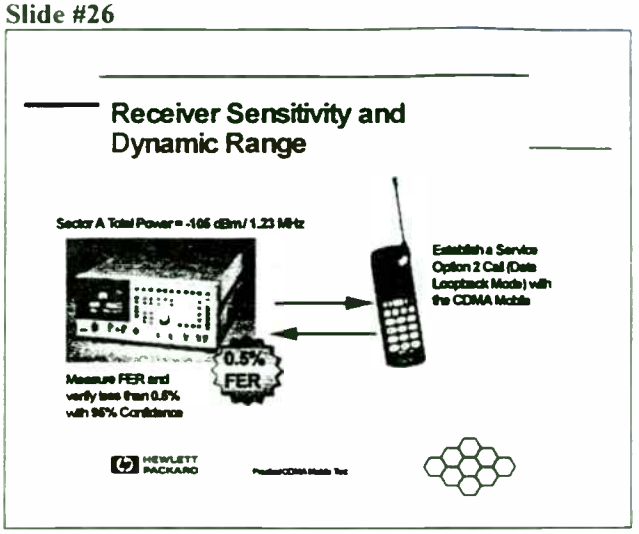
Confidence limit testing uses a specific statistical distribution to model the random nature of the errors (CDMA uses a Poisson distribution). Each test is given a specified error rate that must be met with a specified level of confidence. Typically, the confidence level is 95%. As an error rate test proceeds, the measured error rate is compared to the confidence level using the statistical model. If the test meets the confidence level criteria, the test stops. This results in the absolute minimum test time possible. In other words, if few errors are measured in a given number of frames tested, then the test will meet the specified FER level with high confidence. Conversely, if a large number of errors are measured, the test must measure more frames to determine if the actual error rate will meet the specified error rate with 95% confidence.

If we look at an example FER test, we can see the benefits of confidence limit testing. This example is for measuring the FER of a CDMA mobile receiver that must meet a specified FER of 0.5% with 95% confidence. The graph shows the number of frames tested along the X axis and the actual measured FER on the Y axis. The curve displays the points where the measured FER just meets the 95% confidence limit for 0.5% FER. If the test measures 600 frames with 1 frame error, then the test has demonstrated that the true FER will be less than or equal to 0.5% with 95% confidence. Notice at this point that the measured FER is only 0.167%. We can stop the test at this point because we have 95% confidence that the true FER performance of the CDMA receiver will meet the specified level of 0.5%. If more errors are measured, then the test will continue until the confidence limit is met. As more frames are measured, the measured FER approaches the specified level of 0.5%. This points out the statistical nature of the measurement. If you measure more frames, you have more confidence in the result.

Slide #25



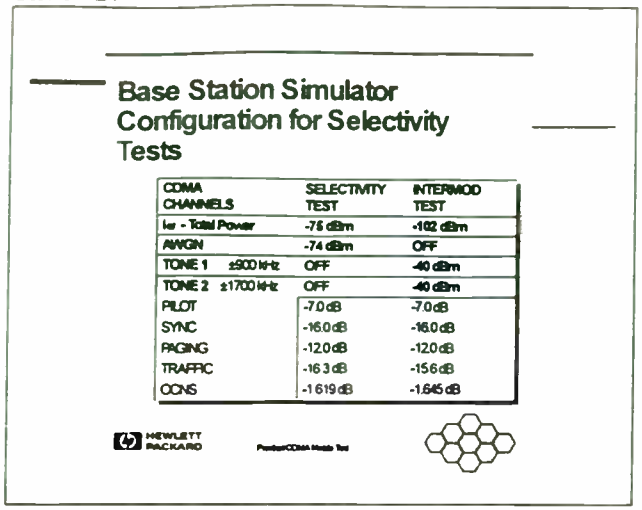
Slide #26



The CDMA receiver sensitivity test is performed without any AWGN interference. Only OCNS noise is required to simulate other users in the same cell. This slide shows the specified setup for a sensitivity test for all of the required channels. The total cell power I_{or} is specified at -105 dBm in a 1.23 MHz bandwidth. The power in each channel is specified in terms of dB below the total cell power. For example, the pilot channel always has the most power and is specified to be -7 dB below the total cell power. Since the total power must add up to the total cell power, the OCNS source is set to produce the remaining power. Although this places a large amount of power in OCNS, this accurately simulates real conditions where up to thirty other users may be active in a cell. The test is repeated with a total cell power of -25 dBm per 1.23 MHz bandwidth to ensure that the receiver does not overload with strong signals.

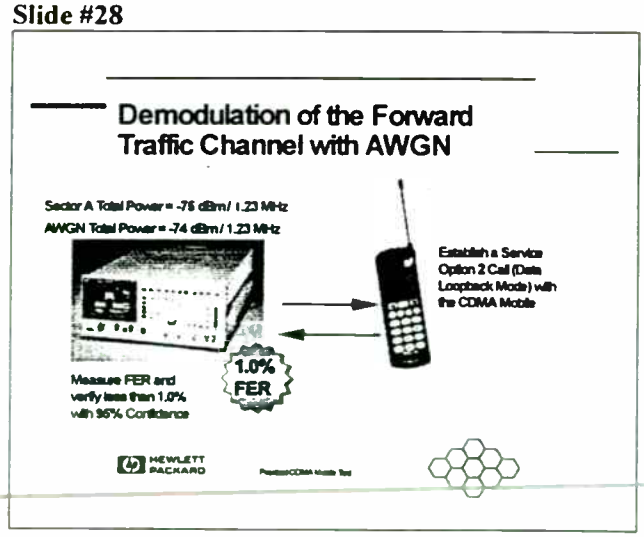
Slide 26 shows a typical block diagram for performing the CDMA receiver sensitivity and dynamic range test. The cell simulator is setup at the specified total cell power with each individual channel at its proper relative power. A call is placed to the mobile, and the cell simulator then requests a service option 2 connection. The cell simulator then transmits a PRBS data pattern to the CDMA mobile. The mobile demodulates the signal and then retransmits the data to the cell simulator. The cell simulator then compares the returned data to the transmitted data to calculate the frame error rate. Since the mobile retransmits the data to the cell simulator at a high level, any returned frames that have errors are considered bad frames. For the receiver sensitivity test, the minimum performance level is 0.5% FER. The sensitivity test is only performed on full rate traffic channels.

Slide #27



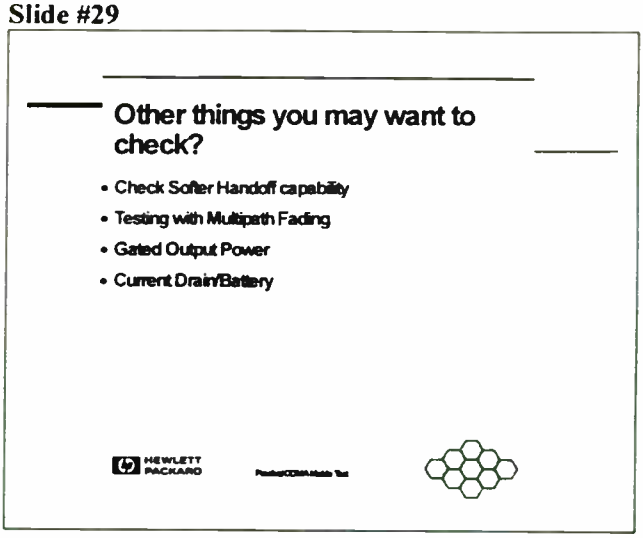
The selectivity test for CDMA, called demodulation of the forward traffic channel in AWGN, is similar to the sensitivity test, but adds the AWGN noise source. The AWGN noise source is set to -74 dBm in a 1.23 MHz bandwidth, while the total cell power is set to -75 dBm in a 1.23 MHz bandwidth. The intermodulation spurious response attenuation test and the single tone desensitization test measure FER performance in the presence of CW tone interference sources rather than using an AWGN noise source.

Slide #28



Like the sensitivity test, the demodulation of the forward traffic channel in AWGN test cannot be performed without a simulated CDMA link with the mobile under test. Service option 2 is required to measure the FER performance accurately. This test is performed at all four possible traffic channel data rates: 9600 bps, 4800 bps, 2400 bps, and 1200 bps. For the 9600 bps case, three traffic channel relative levels are called out with the minimum FER performance ranging from 0.5% to 3%. These three test setups correspond to three different signal-to-noise ratio conditions presented to the mobile's receiver. Similar test conditions are specified for the other three traffic channel data rates.

Slide #29



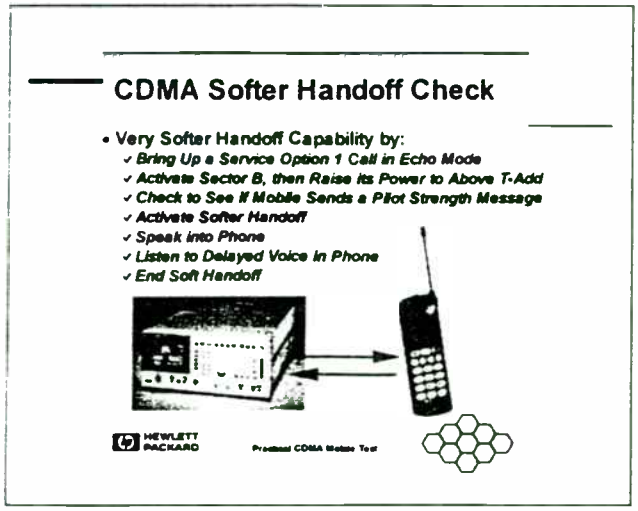
Other characteristics of the mobile may also need to be evaluated.

A mobile's ability to successful operate during the transition state of a soft/softer hand-off can be checked if the cell simulator has the capability to generate at least a partial second sector (Pilot, Traffic, and OCNS).

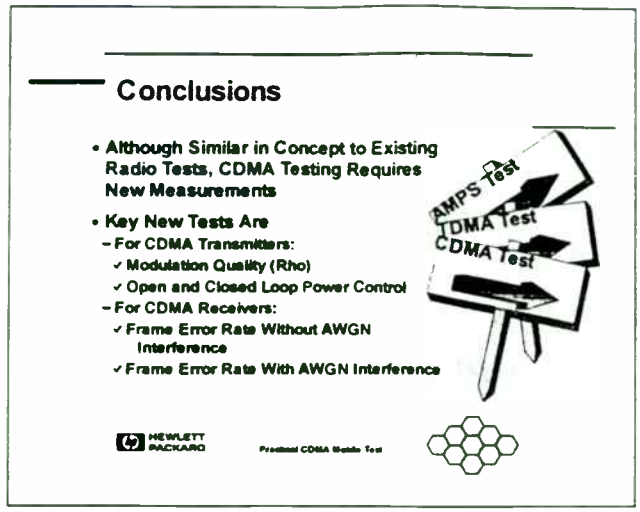
A mobile operates in a real world environment that include multipath signals and fading. Testing that duplicates this environment can be done, but the complexity, expense, and test time go up considerably. Many times this functionality is check indirectly or is felt to be firware based.

Other test include gated output power, current draw, hot/cold testing, . . .

Slide #30



Slide #31



If the base station simulator can support two CDMA cells or sectors, both the phone call functional test and the soft hand-off functional check can be combined into a single test. For this test, a phone call is originated either by the mobile or by the base station simulator. Once the link is established, the base simulator is set so that its second cell or sector presents an attractive level to the mobile for soft or softer hand-off. After the mobile detects the second cell and requests soft hand-off, the base simulator directs the second cell to transmit to the mobile and directs the CDMA mobile to listen to the second cell. If these actions are completed successfully, the hand-off capabilities of the mobile have been verified.

As has been shown, the tests required for CDMA cellular telephones are similar in their basic concepts to tests already in use. However, new tests and test conditions are required along with a new generation of test equipment to perform them. Testing must be performed under precisely controlled interfering conditions when operating on a simulated CDMA link in service option 2. These new tests, along with tests covering the AMPS analog mode of operation of these phones are outlined in TIA standard IS-98. The key new tests for CDMA transmitters are waveform quality (ρ), along with open and closed loop power control verification. For CDMA receivers, the key tests are frame error rate measurements with and without Additive White Gaussian Noise interference. Functional tests, such as voice quality checks, provide a useful and lower cost alternative to full testing for cost sensitive applications like service and incoming inspection.

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APPENDIX

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IS-98 TX Test Capabilities

CDMA Transmitter Tests	HP 85725A	HP 8924C
10.1.1 Frequency Accuracy	◐	●
10.2.1 CDMA Hard Handoff		◐
10.3.1 Time Reference		●
10.3.2 Waveform Quality (rho)		●
10.4.1 Range of Open Loop Power	◐*	●
10.4.2 Time Response of Open Loop Power	●*	
10.4.3 Access Probe Ouput Power	●*	
10.4.4 Range of Closed Loop Power	●*	●
10.4.5 Maximum RF Output Power	◐*	●
10.4.6 Minimum Controlled Output Power	●*	◐
10.4.7 Standby and Gated Output Power	●*	
10.5.1 Conducted Spurious Emissions	●*	
10.5.2 Radiated Spurious Emissions	●	

* Must be used with the HP 8924C to make this measurement

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IS-98 RX Test Capabilities

CDMA Receiver Tests	HP 85725A	HP 8924C
9.1.1 Frequency Requirements	●	●
9.2.2 Idle Handoff in Non-Slotted Mode		○**
9.2.3 Idle Handoff in Slotted Mode		○**
9.2.4 Neighbor Set Pilot Detection in Soft Handoff		○**
9.2.5 Candidate Set Pilot Detection in Soft Handoff		○**
9.2.6 Active Set Pilot Loss Detection in Soft Handoff		○**
9.3.1 Demod of Non-Slotted Paging Channel with AWGN		◐
9.3.2 Demod of Slotted Paging Channel with AWGN		◐
9.3.3 Demod of Forward Traffic Channel with AWGN		●
9.3.4 Demod of Forward Traffic Channel with Fading		◐*
9.4.1 Receiver Sensitivity and Dynamic Range		●
9.4.2 Single Tone Desensitization		◐*
9.4.3 Intermodulation Spurious Response Attenuation		◐*
9.5.1 Conducted Spurious Emissions	●	
9.6.1 Radiated Spurious Emissions	●	

* HP 8924C requires extra external equipment to make this measurement
** HP 8924C has the capability to perform portions of this measurement

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References

- CDMA Technical Seminar - Hewlett-Packard
- IS-98 - Recommended Minimum Performance Standards for Dual-Mode Wideband Spread Spectrum Cellular Mobile Stations - TIA
- Concepts of CDMA - Ken Thompson/Dave Whipple - Hewlet-Packard
- CDMA Mobile Testing - Ken Thompson - Hewlett-Packard

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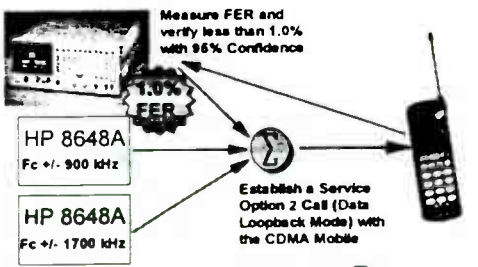
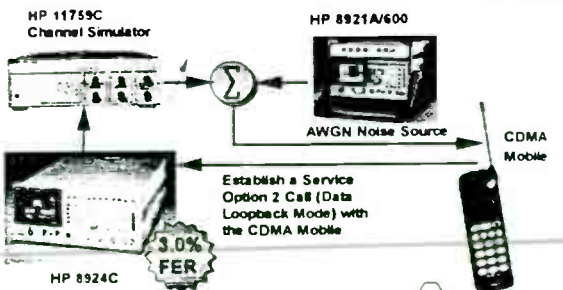
Intermodulation Spurious Response Attenuation



Slide #37

Demodulation of Forward Traffic Channel in Multipath Fading



INTEGRATED CIRCUITS FOR WIRELESS COMMUNICATIONS

Integrated Circuits for Wireless Communications

Session Chairperson: Mark McDonald,
Linear Technology (Milpitas, CA)

Silicon RF ICs for Frequency-Conversion Applications. **Jim Wholey, Detlef Daniel,** and **Kevin J. Negus,** Hewlett-Packard Co., Communications Components Division (Newark, CA) **465**

CDMA and TDMA Standards-Compatible Modem Developments Improve Power Efficiency and Performance of Wireless RF ICs. **Earl McCune,** RF Communications Consulting (Santa Clara, CA); **Kamilo Feher,** Digcom, Inc. (El Macero, CA) and University of California at Davis (Davis, CA) **472**

A Fully-Integrated 290-to-460-MHz ASK Receiver. **Gordon A. Wilson** and **Philip J. Knights,** GEC Plessey Semiconductors (Swindon, Wiltshire, England) **480**

New Package and Silicon Technology for RF Front Ends. **B.N. Balm,** Philips Semiconductors (Nijmegen, The Netherlands) **489**

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Silicon RFICs for Frequency Conversion Applications

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Abstract

Three silicon transmit ICs for RF frequency conversion applications are discussed.The primary applications of these circuits are for wireless communication systems and are compatible with vector modulation and frequency conversion to 4GHz. In order to optimize power efficiency, all three converters operate from 2.7 to 5.5 volt supplies and include full power down circuitry. They are manufactured using HP's bipolar ISOSAT process and are housed in 16 lead SSOP (Shrink-Small Outline Package) plastic packages.

I. Introduction

Figures 1 through 3 illustrate the three frequency converters. The dual conversion modulator (figure1) and the offset loop modulator (figure 2) incorporate vector modulators. In both cases, signal isolation requirements (transmit signal to LO sources) are minimized due to the LO/transmit frequency differences.[1] The upconverter (figure 3) is comprised of a double balanced mixer followed by a single-ended postamplifier.

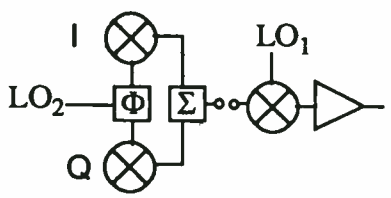

Figure 1.
Dual Conversion Modulator

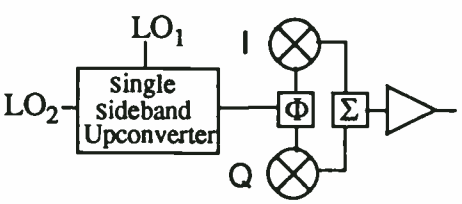

Figure 2.
Offset Loop Modulator

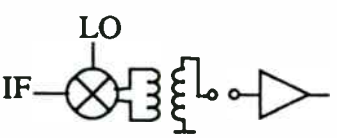

Figure 3.
Upconverter

II. Dual Conversion Vector Modulator

An overview of the dual conversion vector modulator is shown in figure 4.There an IF LO_2 signal (40 MHz to 400 MHz) is passed through a quadrature phase splitter and used to drive a vector modulator. The IF modulated signal is available for user filtering, and can also be upconverted with a LO_1 signal through an on chip double balanced mixer to produce transmit signals up to

4.0 GHz. Optionally, the latter frequency upconversion stage can be separately powered down, leaving the user with a wide band IF vector modulator. Open collector output structures are used in the dual conversion modulator to allow optimization at various frequencies and to set loadings to establish the trade-off between power and linearity.

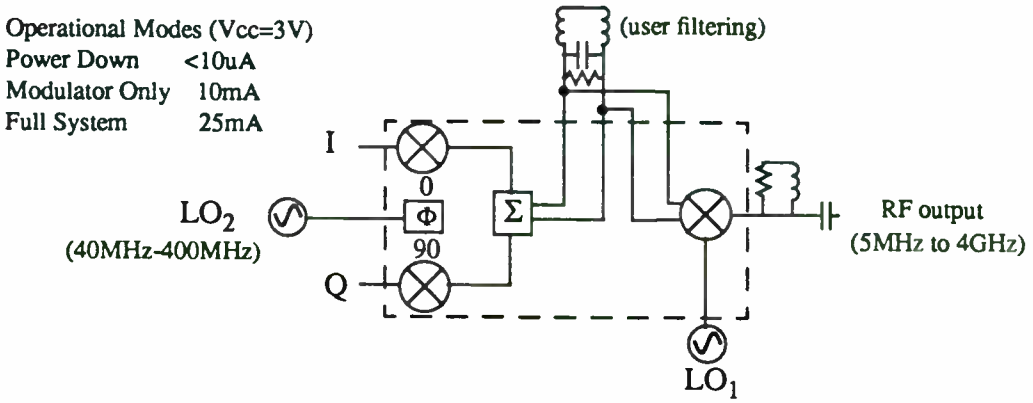

Figure 4. Dual Conversion Vector Modulator

Characterization of the dual conversion vector modulator (and in general any vector modulator) is based on the upconversion of a pair of low frequency sinusoidal signals applied to the IQ inputs. With quadrature IQ signals (I=Vamp $\sin(\omega_m t)$, Q=Vamp $\cos(\omega_m t)$), a single side band (SSB) upconverted spectrum will be observed. The transmit carrier frequency (LO_2 from the modulator only, LO_1+LO_2 or LO_1-LO_2 from the full system) and the image signal of the modulation will be suppressed.[2,3] Figure 5 shows the performance of the vector modulator section vs. frequency. Here the modulator output is taken single-ended, into an effective load of 43Ω. Output powers can be increased with higher impedances or the use of baluns to combine the differential outputs, although carrier leakages and image suppressions (in dBc) would remain the same. It is seen that excellent suppression of undesired signals is obtained over a 40MHz to 400MHz bandwidth.

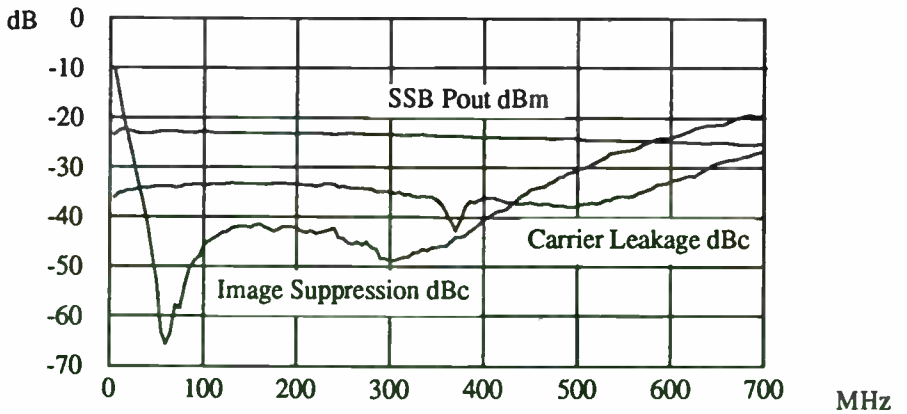

Figure 5. Vector Modulator Performance

Distortion characteristics of vector modulators are evaluated by applying in phase IQ signals, with the resulting output being a pair of signals similar to a double sideband mixer (DSB) (at f_carrier + f_mod and f_carrier - f_mod) and their corresponding third order intermodulation distortion products (IMD) (at f_carrier + 3*f_mod and f_carrier - 3*f_mod). Figures 6a and 6b illustrate output powers and linearity for the dual conversion vector modulator vs. IQ drive level. Figure 6a shows output powers from the modulator only (LO2 = 150MHz) and 6b shows powers for the full system at 1900MHz(LO1=1750MHz, LO2=150MHz). The modulator is designed to provide a high degree of linearity at nominal IQ drives(Vamp = 150mV), as the intermodulation products are suppressed 47dBc. The upconverter can be optimized for linearity or power. This is most easily done by altering the loading of the modulator output open collectors to set the drive level into the upconverter. Figure 6b shows the power/linearity trade-off for an effective loading of 215Ω per modulator output.

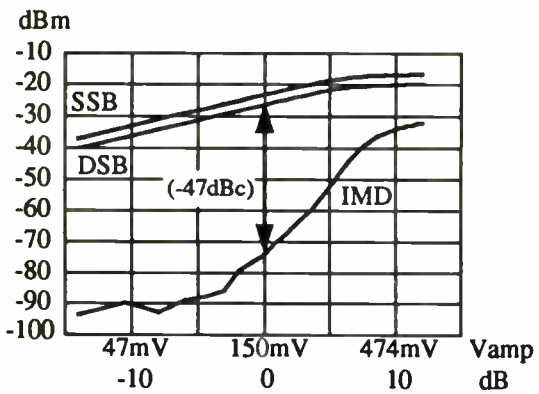

Figure 6a. Modulator Output only (LO2=150MHz)

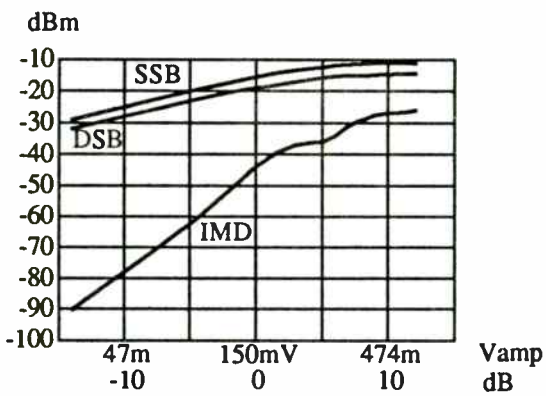

Figure 6b. Dual Conversion Output 1900MHz (LO2=150MHz, LO1=1750MHz)

III. Offset Loop Vector Modulator

A separate approach to generating a vector modulated signal is that of an offset loop modulator. There a rf LO_1 signal is combined with (or offset by) a lower frequency LO_2 signal (70 MHz to 250 MHz) to produce an 800 MHz to 1000 MHz carrier frequency at LO_1-LO_2. This carrier frequency is then used to drive a direct conversion vector modulator. Since the rf carrier signal is fully differential and exists only on a small portion of the ic chip, its required shielding from the full output is minimized. Likewise should the output signal interfere with the LO sources, normal frequency translations from this modulator (and well as in the previous dual conversion modulator) would place unwanted signals at frequencies easily amenable to filtering.

Figure 7 presents an overview of the offset loop modulator. The LO_1 and LO_2 signals are combined by generating quadrature pairs of each signal and processing them through a separate vector modulator, much as quadrature IQ signals are used to generate a single sideband upconversion. This mechanism avoids the off chip filtering which would be necessary if LO signals were combined with only a simple double balanced mixer. After the carrier is modulated through the IQ vector modulator it is amplified in a buffer and output stage. By use of an external resistor, the

user can configure the modulator to optimize the power or linearity. The output amplifier supplies a single ended output that is reactively tuned with an on chip inductor and capacitor to 50Ω in the 800MHz to 1000MHz frequency band.[4] This gives an output return loss of greater than 15dB over any of the common 900MHz transmit bands.

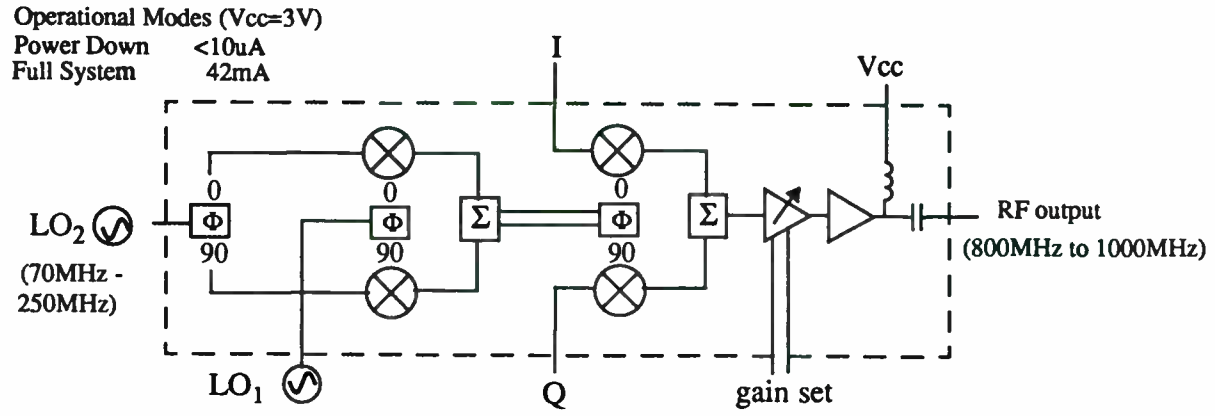

Figure 7. Offset Loop Vector Modulator

Figure 8 shows the frequency performance of the offset loop vector modulator. A carrier frequency of 800MHz is generated from a differential high side LO_1 frequency and an offset LO_2 signal, i.e. f_carrier = f_LO_1-f_LO_2. A pair of quadrature sinusoidal signals are input into the IQ ports of the vector modulator, generating a single sideband fundamental signal (SSB) and a suppressed carrier and image signals.

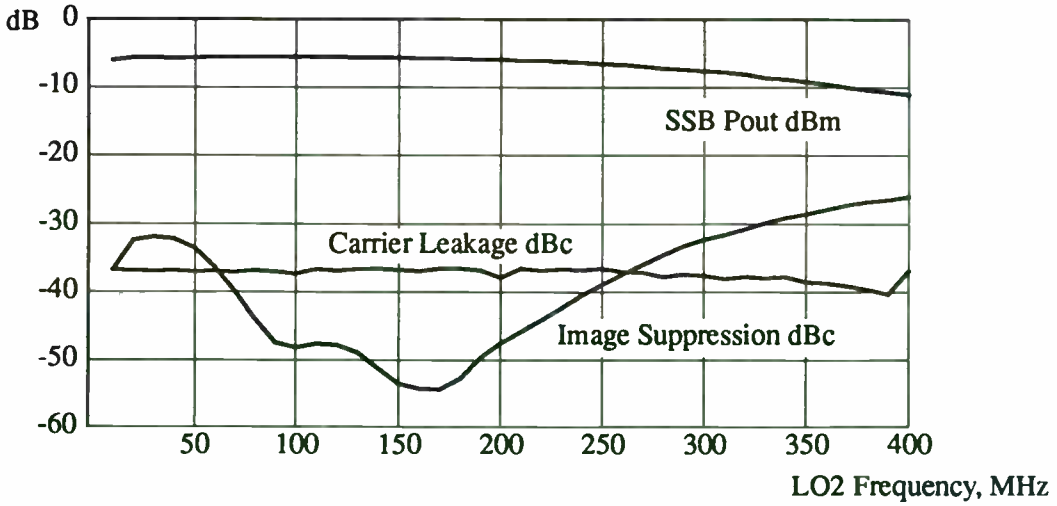

Figure 8. Frequency Response of Offset Loop Vector Modulator with Rgain set = 640Ω (linear configuration).

Power and linearity characteristics of the offset loop vector modulator are shown in figures 9a and 9b. Here a 900MHz carrier is generated using a pair of 1040MHz and 140MHz signals. The single sideband power results from quadrature IQ signals, whereas the double sideband signals and their associated intermodulation distortion result from in phase IQ signals. By varying the resistor at the 'gain set' location of the offset loop modulator (fig. 7) one can significantly alter the power/linearity trade-off of this part. Figure 9a represents a 640Ω resistor for linear applications and figure 9b shows the higher power levels and deteriorated linearity when the gain set pins are shorted (R=0Ω).

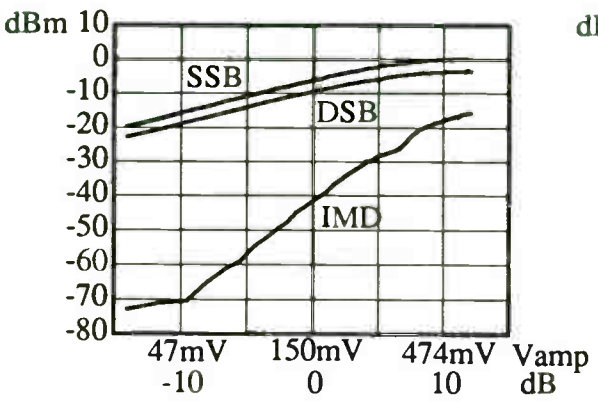

Figure 9a. Offset loop power output
R gain set = 640Ω

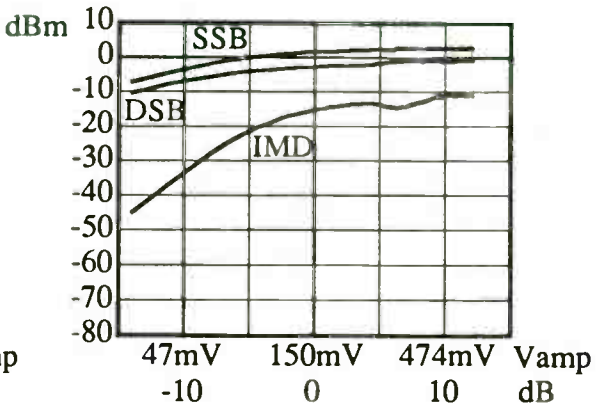

Figure 9b. Offset loop power output
R gain set = 0Ω

IV. Upconverter

The upconverter circuit shown in figure 10 mixes IF and LO signals in a double sideband fashion to produce lower and upper frequency terms. An on-chip transformer then combines the differential outputs of the Gilbert cell mixer to produce a single ended output available for user filtering. Removing the undesired sideband will enable a more efficient use of the following amplifier. The upconverter is compatible for output frequencies of 800MHz to 2500MHz and can be used in place of the upconverter of the dual conversion vector modulator when higher power is desired.

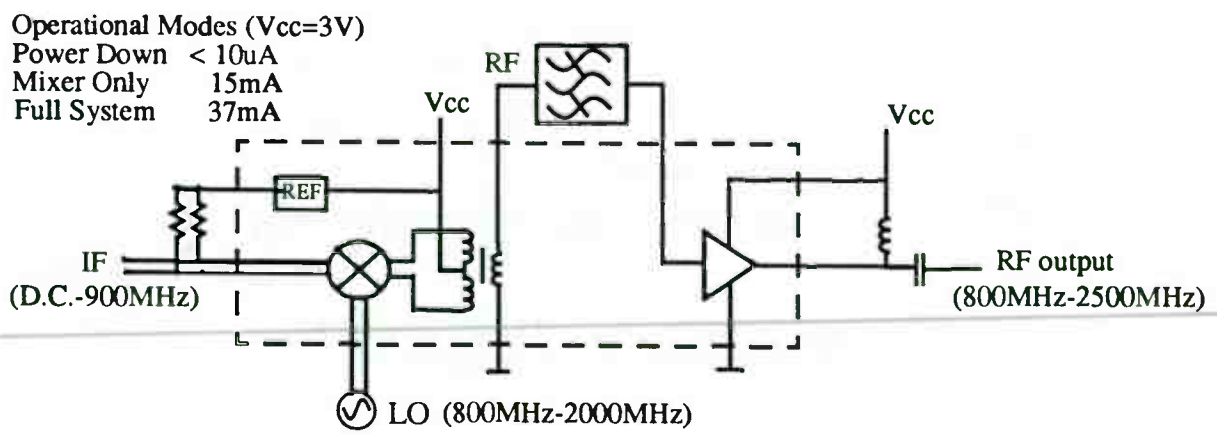

Figure 10. Upconverter Circuit

The IF port of the upconverter is set at a high impedance to allow the mixer to be directly connected to baseband circuits as in a BPSK modulator. However the IF port normally will be a.c. coupled and input impedances can be set by external resistors. Impedances of the LO and RF mixer ports are internally set to provide a return loss of better than 10dB at 1900 MHz. Figures 11a and 11b show the mixer output characteristics as the IF and LO frequencies are swept from single ended sources. Figure 11a keeps the transmit frequency at 1900MHz (LO=1900MHz-IF) and figure 11b keeps the IF frequency at 150MHz (transmit=150MHz+LO). The LO power level was -3dBm, and the device voltage was 3V. The noise floor of the mixer output is -136dBc/Hz referred to P-1dB signal levels and the corresponding output third order intercept point (IP3) of the mixer is +2dBm.

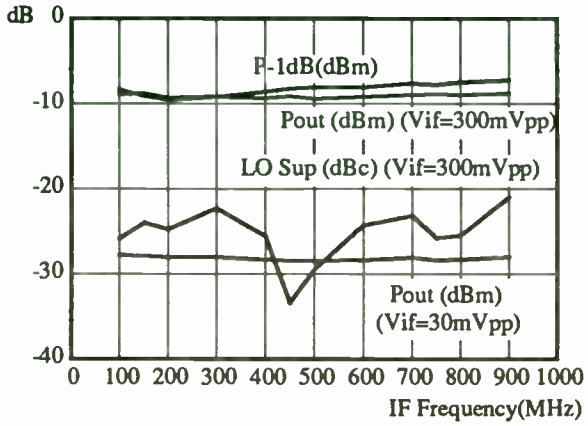

Figure 11a.Mixer Output vs. IF sweep.

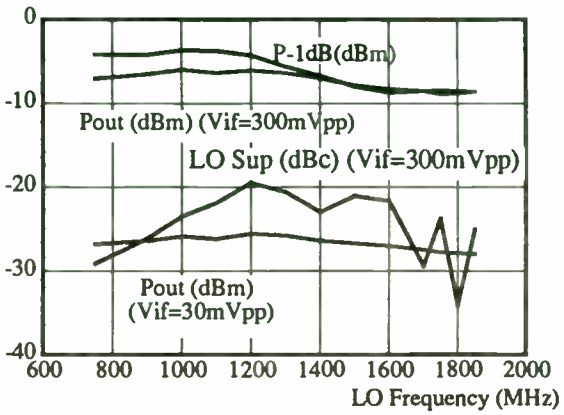

Figure 11b. Mixer Output vs. LO sweep

The postamplifier is configured as a wide-band gain block with a 50Ω match at the input. The output is an open collector and can be externally matched to 50Ω by the LC network shown in figure 10. The amplifier typically provides 14dB gain at 1900MHz with a noise figure of 8.5dB. The output power at P-1 is +4dBm and the output IP3 is +15dBm.

V. Packaging

The three frequency converter IC's are each housed in the plastic 'Shrink Small Outline Package' (SSOP-16). The small size (0.154" by 0.193") enables optimum use of critical board space for compact hand held systems. Figure 12 is a photograph of the dual conversion upconverter placed on a typical FR4 test board.

VI. Conclusion

Three silicon based IC's for RF frequency conversion have been presented. Their small size, low voltage operation, and low current consumption with power down capability make them appropriate for handset applications. User flexibility is maintained with these circuits since simple external components are used to determine trade-offs between gain and linearity or optimization of operation at various frequencies when appropriate.

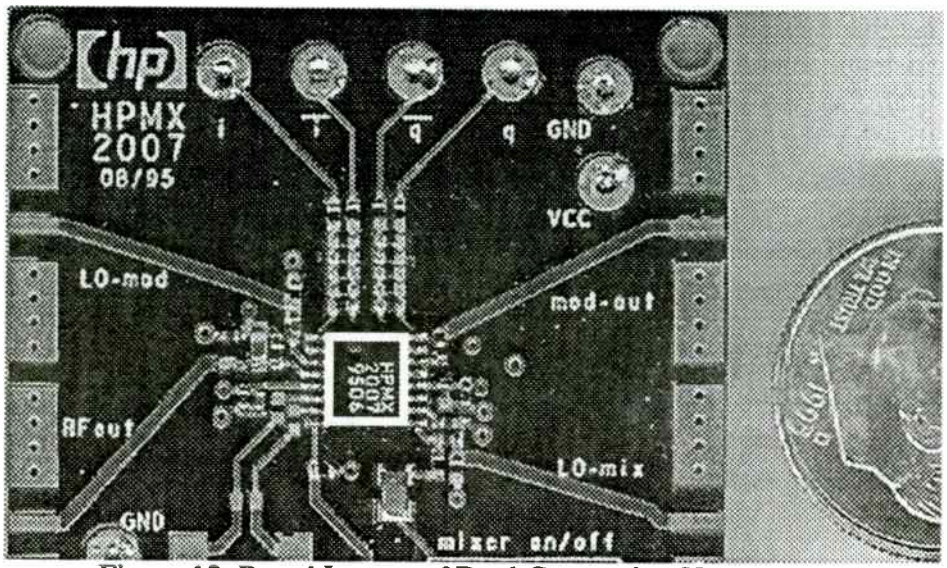

Figure 12. Board Layout of Dual Conversion Upconverter

References

[1] Rehorst M., "Direct vs. Dual Conversion Quadrature (Vector) Modulation", Proceedings of the First Annual WIRELESS Symposium, Jan 1993, pp109-116

[2] Nguyen N., Wholey J., Avasarala.M., "Silicon Bipolar RF Integrated Circuits for Cellular Radio and Wireless Applications", Proceedings of the First Annual WIRELESS Symposium, Jan 1993, pp117-131

[3] Wholey J., "Vector Modulator IC's for Use in Wireless Communications", Conference Proceedings RFexpo West, March 1993, pp232-240.

[4] Negus K., et al,"A Highly Integrated Transmitter IC with Monolithic Narrowband Tuning for Digital Cellular Handsets", Digest of Technical Papers, 1994 International Solid-State Circuits Conference, San Francisco, CA February, 1994

CDMA and TDMA Standards Compatible Modem Developments Improve Power Efficiency and Performance of Wireless RFICs

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Abstract

For handheld wireless communication products to be successful, it is essential that each electron from the battery performs useful work. Choice of modulation, and also the method of implementation of the defined modulation, can have a significant impact on overall product power efficiency. Implementation options to several standard modulations are presented that allow significant improvement in product power efficiency with no change in RFIC choices.

I. Primary Standards In Use

Significant product development activity is currently happening in compliance with established CDMA and TDMA standards, including GSM, IS-54/136, IS-95, DECT, and CDPD. Relative market activity in the first three standards [1] is shown in Figure 1.

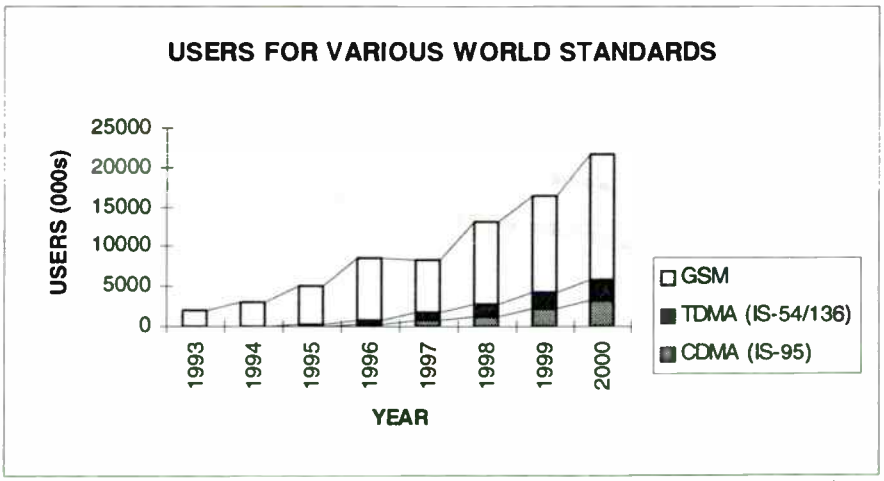


Figure 1. Relative user counts, with future growth estimates, for three RF communication standards, from [1].

From this figure it is clear that the GSM system, and its GMSK modulation, widely dominates in that it has more users than other digital cellular standards combined. The TDMA system is currently in second, with its $\pi/4$-DQPSK modulation. The CDMA system is just now being brought on-line, with its QPSK modulation.

II. Product DC Power Efficiency

Motivation and Definitions

'Talk time' is a major performance measure for any successful product in the wireless communication marketplace. With small and finite batteries in these products, it is therefore essential that each and every electron taken from the battery be put to effective use. For a radio product, this means that efficiency in the generation and reception of the radio signal becomes paramount. Such DC-to-RF (DCRF) efficiency is affected by more than just circuit design: how the modulations are chosen and implemented has a major effect.

Appendix A shows that the DCRF efficiency of an RF stage, such as a power amplifier, is

$$\eta_{stage} = \frac{P_{added}}{P_{supplied}} = \frac{P_{out} - P_{in}}{V_{supply} I_{supply}} = \frac{P_{out}(1 - \frac{1}{G})}{DC_{in}} \qquad (1)$$

This stage efficiency is often called the power added efficiency, PAE. In the presence of a large power gain G, this can be approximated by

$$\eta_{stage} \approx \frac{P_{out}}{DC_{in}} \qquad (2)$$

Clearly, for a specified RF power output we want a minimum amount of DC input.

Signal Effects at Higher PAE Operation

Figure 2 shows a typical power transfer relationship for an RFIC designed for class-A operation. It shows both the output compression characteristic, and the power added efficiency. The PAE is at or below 10%, and is well below 10% for linear operation. This means that over 90% of the DC power being applied to this amplifier is being converted to heat. This is not good for a high 'talk time' product.

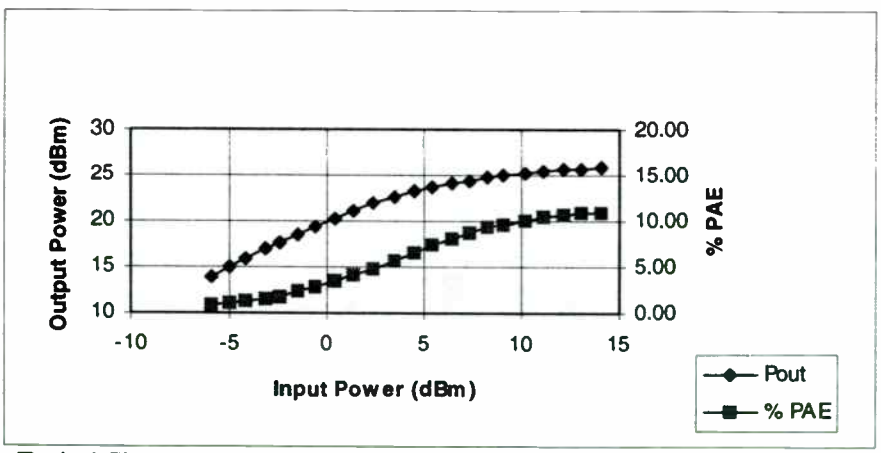
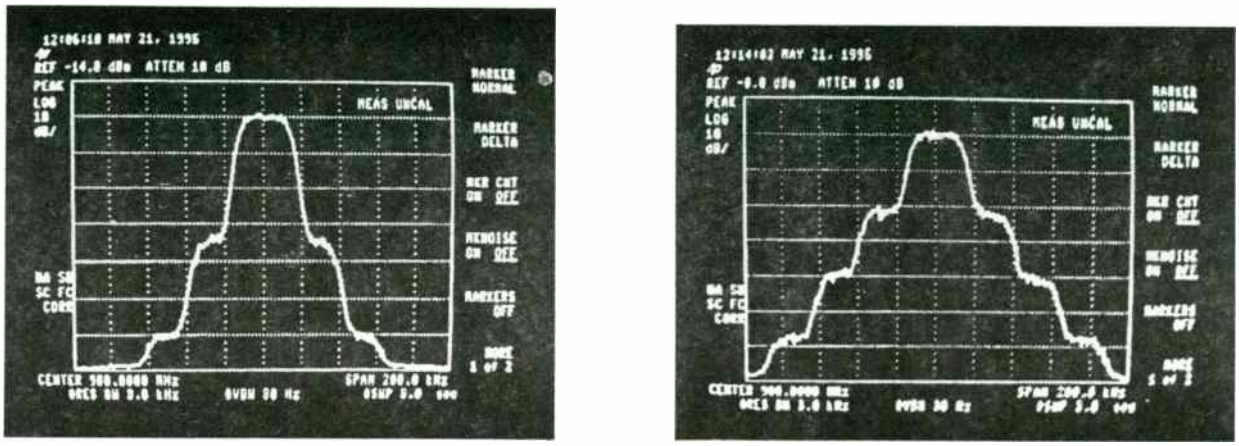


Figure 2. Typical Class-A RFIC amplifier power transfer relationship, with power added efficiency. (from Muhonen)

To see how standard signals perform in amplifiers operating at higher PAEs, the following measurements have been taken. Figure 3b shows how π/4-DQPSK performs at 3dB compression, about 9%PAE. Significant spectral regrowth is clearly evident. Backoff to linear operation is definitely required to maintain the spectral

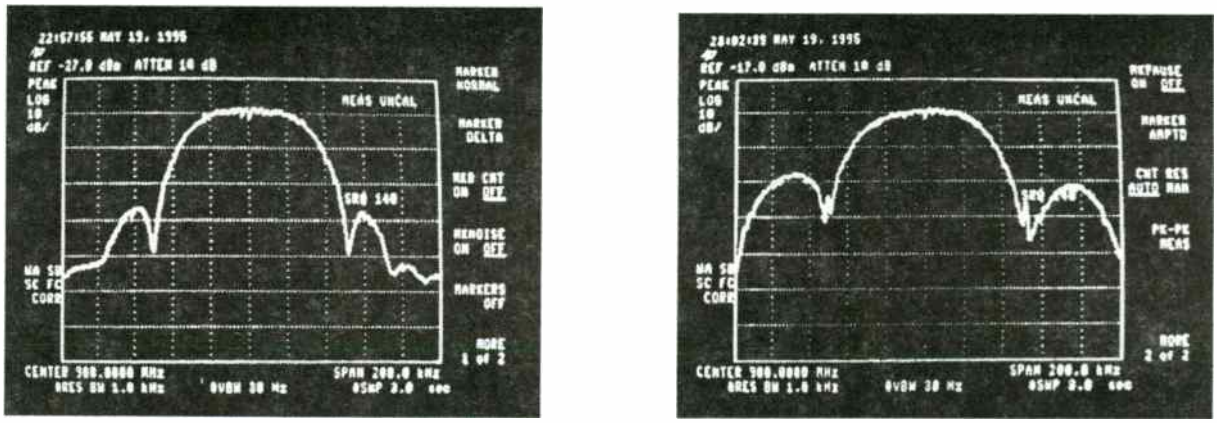
efficiency of this signal. At this backoff, the operating PAE of the amplifier becomes less than 5%. The amplifier is putting out 1 part useful RF and 19 parts waste heat from the DC power supplied to it.



(a) (b)

Figure 3. $\pi/4$_DQPSK performance through this amplifier: a) linear, and b) 3dB compressed. Experimental data from UC Davis, by Kathy Muhonen

Similar sideband regrowth is evident in Figure 4 for BPSK. Even though these signals are considered only phase modulated, clearly a significant amplitude component exists.

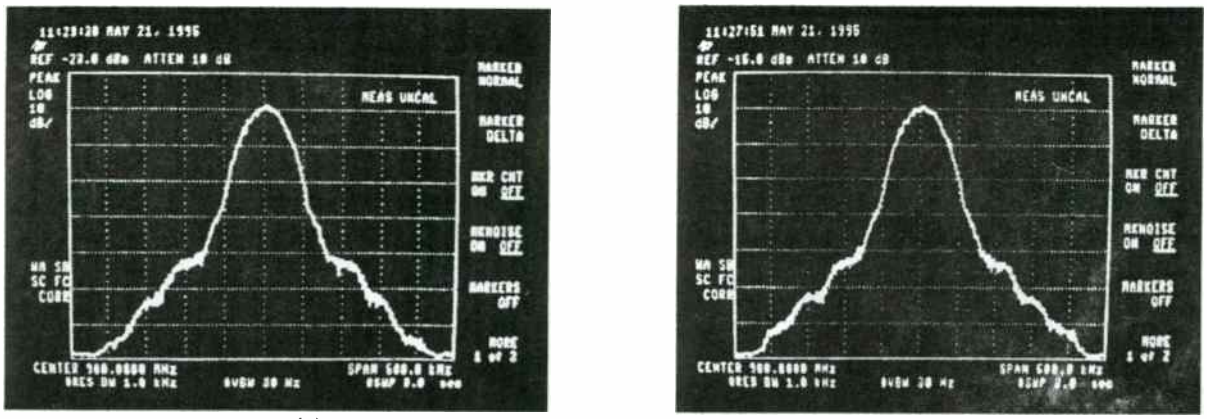


(a) (b)

Figure 4. BPSK performance through this amplifier: a) linear, and b) 3dB compressed. Experimental data from UC Davis, by Kathy Muhonen

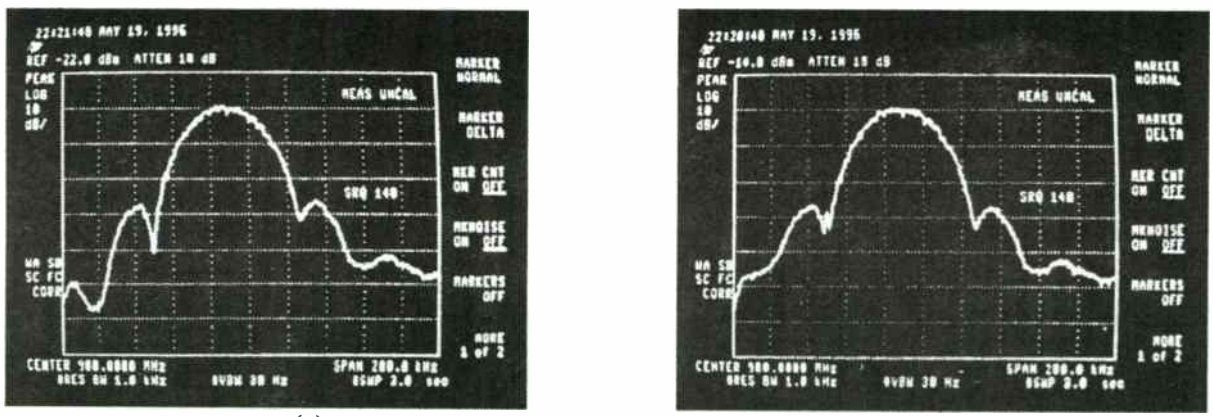
Characteristics of High PAE (NLA) Tolerant Signals

Compatible modulations do exist that perform significantly better at high PAEs. Figure 5 shows the performance of FQPSK-KF in both linear and 3dB compressed modes. Only minimal differences can be seen, and even these are over 60dB down from the center. This type of filtering strategy, pioneered and patented by Feher [2;3], clearly contributes significantly to higher PAE capability in PSK modulated products. Similar tolerance is exhibited by the FBPSK signal, as shown in Figure 6.



(a) (b)

Figure 5. FQPSK-KF (Feher's patented QPSK) performance through this amplifier: a) linear, and b) 3dB compressed. Experimental data from UC Davis, by Kathy Muhonen



(a) (b)

Figure 6. FBPSK (Feher's patented BPSK) performance through this amplifier: a) linear, and b) 3dB compressed. Experimental data from UC Davis, by Kathy Muhonen

Examination of the signal constellations for all of these signals shows a particular feature that leads to tolerance of operation through a compressed amplifier. That is a minimization of amplitude variations in the signal envelope. The GMSK signal from GSM has a naturally low envelope fluctuation when implemanted properly, and so it is also tolerant of operation through a compressed or saturated amplifier.

III. Conventional Modulation Implemantations

All of these digital modulations are conventionally implemented with the quadrature AM (QAM) structure[2]. The baseband is converted into two streams, which separately linearly modulate two RF carriers in phase quadrature. The resulting AM signals are phase combined into the final modulated output signal.

GMSK

The constant amplitude GMSK signal is implemented with quadrature modulation as shown in Figure 7. The baseband signal shaping filters in a sense make a pseudo-quadrature signal out of the gaussian filtered baseband signal, which then gets applied to the quadrature modulator.

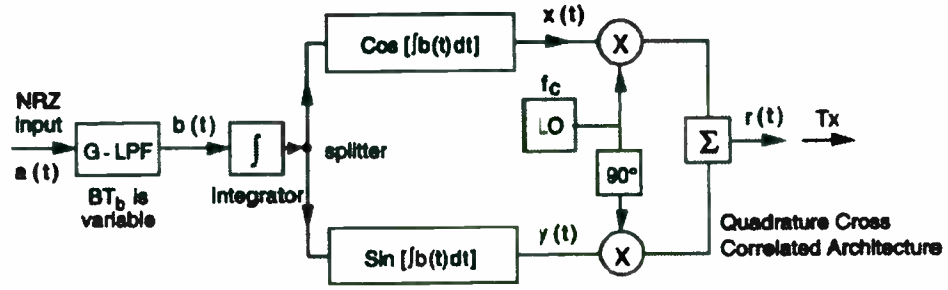


Figure 7. An implementation of a GMSK modulator based on quadrature crosscorellated modulation [2;3].

π/4-DQPSK

Unlike GMSK, the baseband bandlimiting filters in π/4-DQPSK quadrature modulators are not designed to generate a pseudo-quadrature signal. The I and Q channels therefore operate independently, and the resultant output signal displays a significant envelope fluctuation. Envelope power variations of 6dB (4:1) are not uncommon.

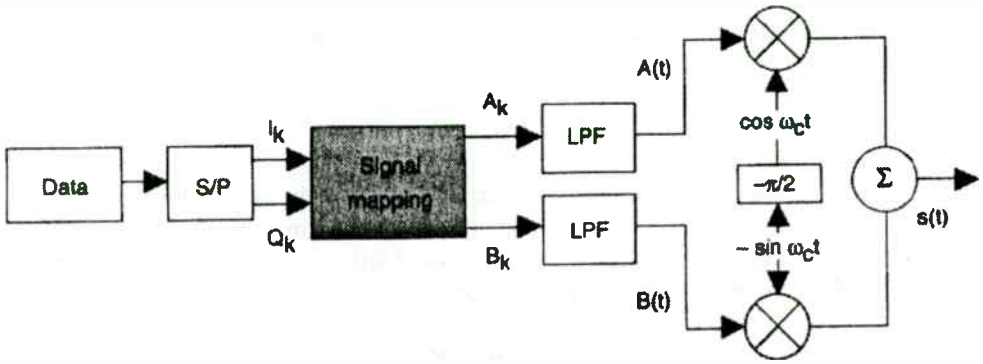


Figure 8. Conventional implementation of a π/4-DQPSK modulator.

AM Limited PSKs: FQPSK

The amplitude variation of a QPSK signal can be completely removed by using a cross correlator [3;2]. Such a signal does show a complete tolerance of operation through a compressed amplifier. Generation of these signals could follow a block diagram like that of Figure 9.

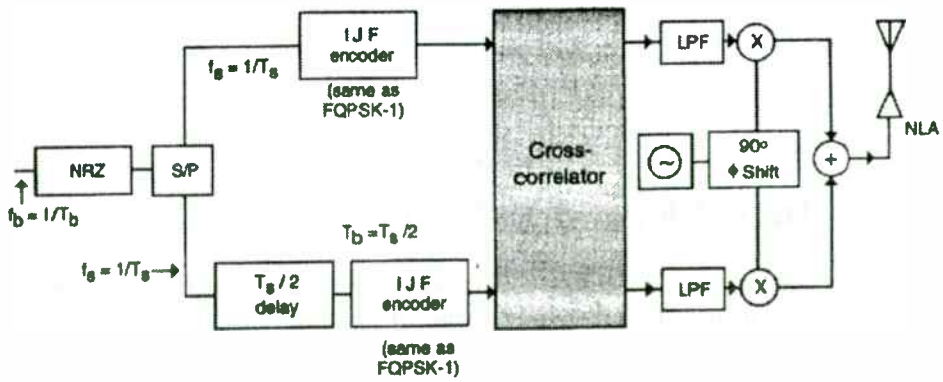


Figure 9. Implementation of a cross-corellated FQPSK and/or GMSK modulator. [2]

IV. Alternative Modulation Implementations

More recent work has shown that the quadrature modulator is not necessary to implement any of these signals[4,5]. By eliminating the linear modulator stages of the quadrature modulator, and replacing them with nonlinear and much more power efficient digital circuits, even higher product power conversion efficiencies can be achieved. Two possibilities are shown in Figure 10. These proposed alternative implementations derive from viewing any signal, and particularly these constant amplitude signals, in polar coordinates rather than cartesian coordinates. Any constant amplitude signal then reduces to a single modulation dimension, the signal angle ϕ.

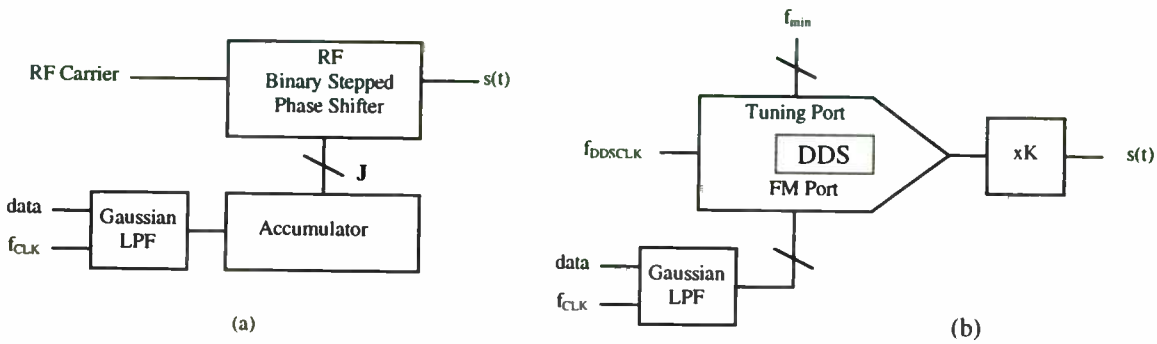


Figure 10. Nonlinear implementation options for GMSK: a) serrodyne, and b) multiplied DDS

V. Conclusions

Power efficiency is a vital product performance parameter for handheld and other battery operated wireless communication devices. Choice of modulation, and certainly the choice of modulation implementation, has a dramatic impact on the overall product power efficiency. Options exist on standardized modulations that provide designers access to this enhanced performance without compromising compatibility with any other compliant unit.

Acknowledgements

The authors would like to thank Kathleen Muhonen for her amplifier performance measurements.

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APPENDIX
DC to RF Power Efficiency Definitions

To any market, the total DC to RF conversion efficiency is all that really matters. As engineers we seldom have access to the entire design of a product. It therefore becomes important to relate the overall product DCRF efficiency to the efficiency of any particular block in the product design. For these individual blocks, this introduces the concept of power added efficiency, PAE.

The overall product is viewed as shown in Figure A.1. The product itself is some black-box B. It draws DC power from its associated battery, and provides an RF communication signal. The overall product DCRF efficiency is

$$\eta_{DCRF} = \frac{P_{RF,\,out}}{DC_{in}} \tag{A.1}$$

where DC_{in} is the total supplied power to the product.

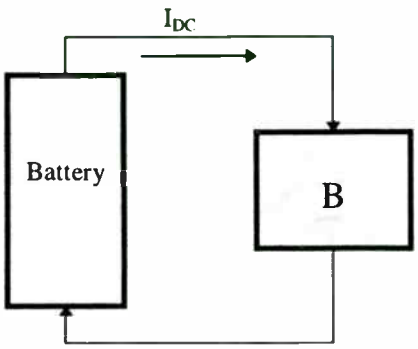

Figure A.1 DC to RF power efficiency of a product

To the engineering staff designing such a product, there is a cascade of circuitry blocks such as that shown in Figure A.2. Each block in the cascade has an input RF power, and provides an output RF power, except the first one. This is the oscillator block, which by definition provides output RF power without any input RF power.

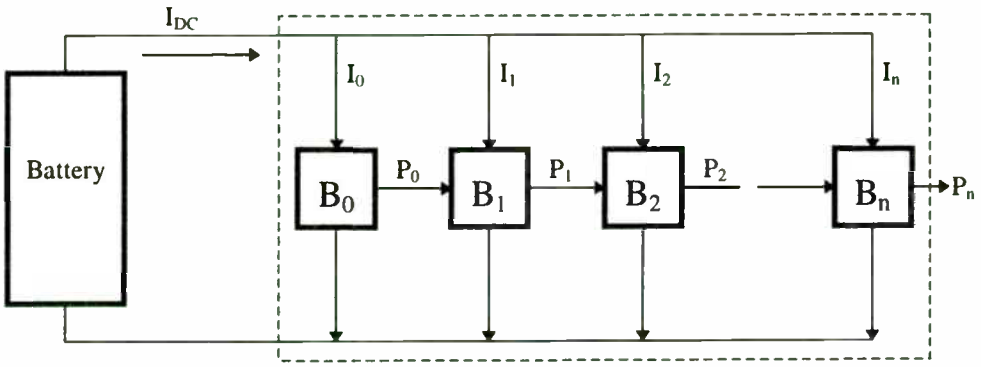

Figure A.2. The RF cascade within a product.

With input powers present, the definition of power efficiency for the individual blocks needs to change slightly. The blocks now add power to the signal, so power added efficiency is now appropriate

$$\eta_{stage} = PAE = \frac{P_{out,stage} - P_{in,stage}}{DC_{stage}} \tag{A.2}$$

For the effective stage gain G, (A.2) can be written as

$$PAE = \frac{P_{in}(G-1)}{DC_{stage}} = \frac{P_{out}\left(1 - \frac{1}{G}\right)}{DC_{stage}} \tag{A.3}$$

For G>>1, (A.3) can be approximated by

$$PAE \approx \frac{P_{out}}{DC_{in}} \tag{A.4}$$

Note that for the conventional engineering approximation of <10% is negligible, G > 10 is necessary for the approximation of (A.4) to be valid. In dB, this equates to $G(dB) > 10\log_{10}10 = 10dB$.

As a check, the combination of RF and DC powers for each stage must result in (A.1). Efficiencies do not add directly, so the RF and DC terms must be combined separately:

$$\eta_{DCRF} = \frac{\sum_{i}^{n}\left(P_i - P_{i-1}\right)}{\sum_{i}^{n} DC_i} \tag{A.5}$$

$$0 \le i \le n$$

Performing the summations and canceling like terms yields

$$\eta_{DCRF} = \frac{P_n - P_{-1}}{DC_{in}} \tag{A.6}$$

Now, since $P_{-1} = 0$, and knowing that $P_n = P_{RF,out}$, (A.6) becomes

$$\eta_{DCRF} = \frac{P_{RF,\,out}}{DC_{in}} \tag{A.7}$$

which matches (A.1) and the check passes.

A Fully Integrated 290MHz to 460MHz ASK Receiver

by

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Recent years have seen the proliferation of simple, low power, short range wireless data transceiver applications operating in the unlicensed portion of the lower UHF band. GEC Plessey Semiconductors has produced a single chip super-heterodyne ASK receiver, the KESRX01, for use in applications from 290MHz to 460MHz . This high sensitivity receiver offers radio engineers the opportunity to implement their Keyless Entry and RFID systems at low cost, with the minimum component count and with very low supply current (~2mA or less). Integrated are all the functions required to implement a single-conversion super-heterodyne receiver : LNA, double balanced active mixer, VCO, IF filter, PLL, Logarithmic amplifier, RSSI detector, data filter and comparator thus providing a complete RF to Data solution in a single, plastic, 24 pin surface mount package. A quartz crystal oscillator, 4 to 7MHz, determines the frequency and accuracy of the local oscillator. The aim of this paper is to describe the features of the KESRX01 receiver from an IC designer's perspective(Section I) together with a typical application example from an RF engineer's perspective(Section II).

I KESRX01 Receiver Design

A. Super heterodyne Receiver

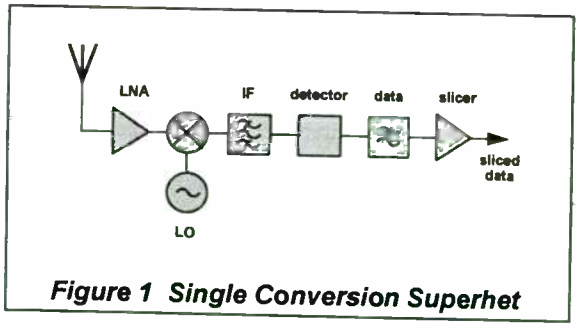

Figure 1 Single Conversion Superhet

The single conversion super-heterodyne receiver, Fig 1, uses the mixer and local oscillator (LO) to down convert the rf signal to a very low IF where it is filtered, and demodulated. The data-slicer optimally slices the baseband signal and presents a clean signal to the data decoder and µcontroller. The overall objective of the receiver is to achieve an acceptable bit-error-rate (BER) at the data-slicer output. This is dependent on the signal-to-noise ratio(SNR) at the output of the data filter.

B. Design

The design of the device was targeted at the FTZ (Germany) and ETSI (Europe) specifications for unlicensed, short range (high sensitivity) applications. Of course this does not preclude its use in USA or the rest of the world. In order to be very system price competitive with existing methods its main features include a very low supply current, ~2mA, a low external parts count, and a crystal referenced local oscillator. This has been achieved by integrating all the functions of the super heterodyne receiver and using a low cost quartz crystal as described below. A block diagram of the complete receiver is shown in Fig 2.

In very low cost applications no image rejection filter is used prior to the mixer. However by using a low IF of 300kHz say the image channel comes from within, or very close to, the accepted unlicensed band e.g. for a wanted signal at 433.92MHz and a VCO at 433.62MHz (300kHz IF) the image frequency occurs at 433.32MHz - unlicensed band of 433.05 to 434.79MHz (FTZ, ETSI). A second benefit of a low IF is that a fairly narrow band IF filter can be achieved with integrated components and no alignment.

1) Low Noise Amplifier (LNA): The RF amplifier consists of a low noise transistor operated in cascode and is provided with separate supply pins from the rest of the receiver to reduce sensitivity to common impedances and LO breakthrough to the RF input. The output collector is open circuit so that gain is set by an externally tuned load.

2) RF Mixer: The output of the LNA is matched into the mixer. The nominal voltage gain of the RF amplifier and mixer combination is 38dB with a noise figure of 17dB.

3) LO and PLL: For other low cost receivers various methods of defining the frequency have been used from adjusted LC oscillators to SAW resonators. The approach used here is to phase lock an LC VCO to a low cost, low tolerance, quartz crystal in the range 4.7 to 7.2MHz. The VCO frequency is divided down by 64 to the phase detector comparison frequency of the crystal. For the generally accepted frequency tolerances, of say 433.92MHz ±90kHz, a low cost 200ppm 6.7839MHz crystal can be used. Conversely if channel accuracy is important low ppm crystals can be used.

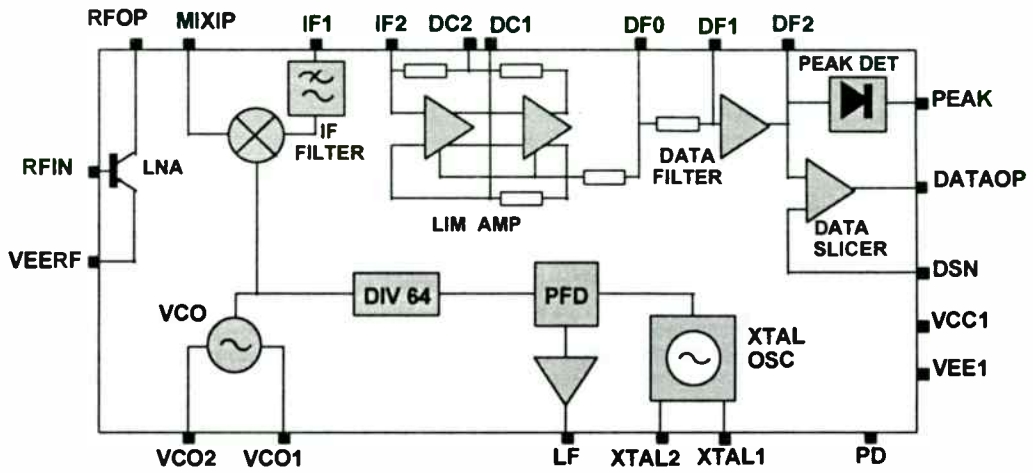

Figure 2 KESRX01 Schematic

Alternatively, if a suitable external reference at the right frequency is available this can be used instead of the crystal. For example, the µcontroller and chip could use the same frequency reference.

The phase detector is a phase frequency detector (PFD) with a current charge pump output. This will always achieve lock for any initial VCO frequency. The PLL loop characteristics such as lock-up time, capture range, and VCO reference sideband suppression are controlled by the external loop filter.

4) IF Filter: This is generated from separate high pass and low pass sections. The low pass section is a 4 pole Butterworth active filter, fully integrated, and un-tuned and is designed to meet the critical selectivity requirements of 'adjacent' channel rejection. The high pass pole is a simple RC using an external capacitor and an on-chip resistor. The nominal overall response is 25kHz to 650kHz 3dB bandwidth. This bandwidth takes into account all tolerances coming from the transmit and LO frequencies and from the spreads of the on chip and external components which define the poles.

5) IF amplifier & demodulator: This is in the form of an IF limiting strip and combines a Received Signal Strength Indicator (RSSI) function. With ASK modulation the RSSI output, which is linear for a logarithmic change on its input, gives the demodulated data.

6) Data Filter: This is an integrated 2nd order Sallen-Key section but using external capacitors to set the actual cut-off frequency. The cut-off frequency can therefore be customised to the application with regard to data rate and sensitivity.

7) Data Slicer: An external slice reference level input is provided. This level can be generated in one of 2 ways i) an average data

slice level generated from the demodulated data signal, using an external RC, or ii) from an on chip peak detector operating on the same signal. The peak detector output represents the peak level at the data filter output. The slice level can be optimised in a number of ways to improve performance dependent on the signal mark/space, and provision of a squelch circuit.

It would normally be the case to use the average data level for grey coded signals and peak detected level for pwm codes.

II. Typical Application Example

The block diagram of the KESRX01 receiver is shown in Fig.3. All the basic functions necessary to implement a single-conversion super-heterodyne ASK receiver are provided on chip.

A brief specification for this receiver is:
Sensitivity: typically -103dBm, average power (source impedance = 50ohm)
Maximum input signal : -20dBm
Supply current : 2.16mA;
Supply Voltage = 5V

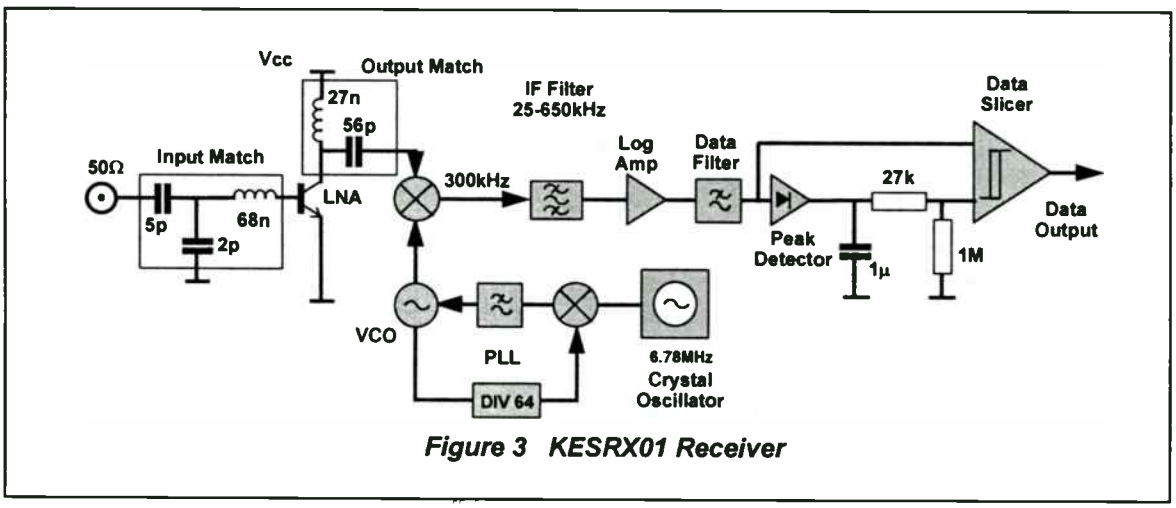

Figure 3 KESRX01 Receiver

The complete schematic of a typical 434MHz application is shown in Fig 4. External components have been kept to a bare minimum to allow for application specific tuning - such as setting the local oscillator frequency and optimising the post-detection filter response - or, are simply coupling/de-coupling capacitors that are too large to be integrated. The performance and design of this receiver is discussed further in sections A to F below

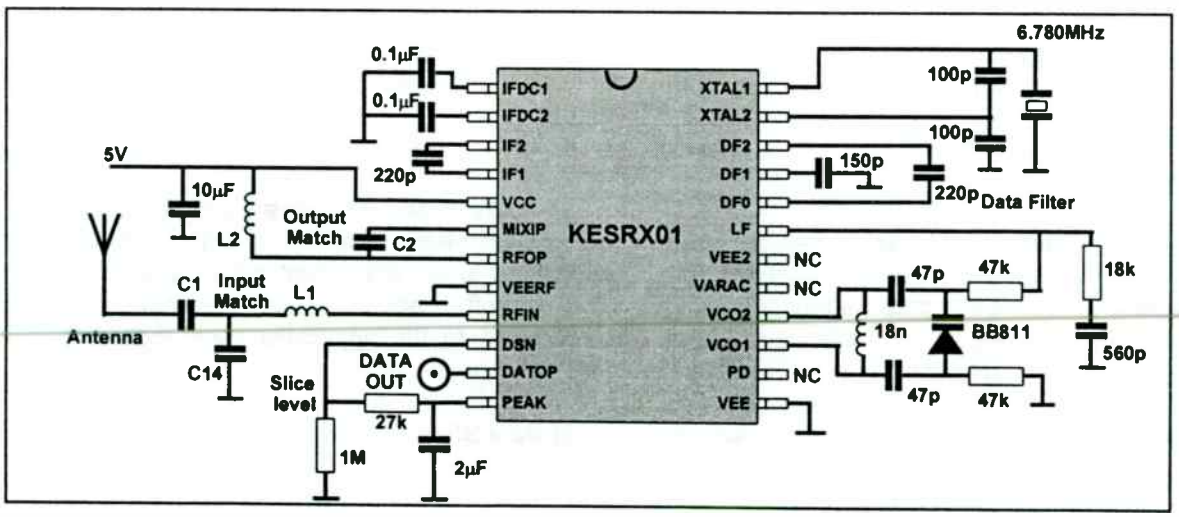

Figure 4 A 434MHz ASK receiver

A. Small signal RF performance

The KESRX01 receiver is specified for 290MHz to 460MHz operation thus making it suitable for applications in North America, Europe and the Far East. Since the device will generally be used at a fixed frequency it is advantageous to make full use of this fact and tune the LNA input match and LNA-to-mixer match to the desired frequency and optimise the Gain, Noise Figure and Selectivity for a specific frequency. The example receiver was tuned for 434MHz operation and matched to a 50ohm signal source. The RF front-end(LNA and Mixer) voltage gain is 38dB and the NF is 17dB.

1)Sensitivity : Sensitivity is the smallest signal that can be detected whilst providing an acceptable SNR at the demodulated output or, more suitable in data systems, an acceptable BER at the data output. The test set-up used to evaluate the KESRX01 receiver sensitivity is shown in Fig. 5. The typical sensitivity of this example circuit is -103dBm average power (modulating frequency is 2kHz ON/OFF keying) for 1 in 100 BER.

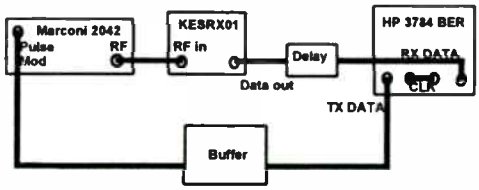

Figure 5 Sensitivity measurement

2) Selectivity : The receiver is intended for operation with the IF centred on 300kHz nominally. The IF bandwidth extends from 25kHz to 650kHz much wider than the proposed data rates thus allowing inexpensive, low tolerance frequency stabilising components to be used in both the transmitter and receiver. The actual overall selectivity is shared between the RF tuning and the on-chip IF filter. Overall selectivity of our example receiver was measured by noting the level of a CW signal that is required to raise the DC level at the RSSI output 50mV above the DC condition for no signal present. This was repeated at a number of offsets above the local oscillator (LO). Note that a 434MHz -103dBm CW signal converted to a 300kHz IF raised the DC level at the RSSI output by 50mV and is the reference level for this measurement. Fig.6 is a plot of the difference between the reference signal level and the level of a CW signal, offset in frequency above the LO, that produces the same RSSI DC output.

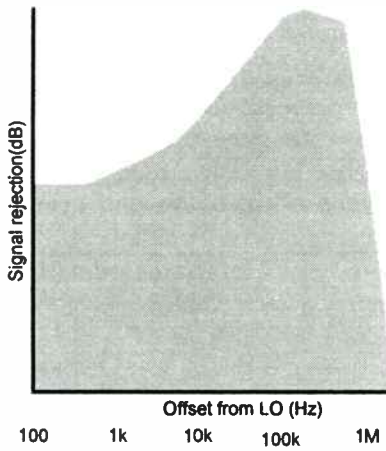

Figure 6 Selectivity

B. Large signal RF performance

Clearly with a single-conversion low IF receiver that uses standard Ls and Cs to determine the selectivity, and takes only 2mA total from the supply, a radio engineer would rightly want to consider its performance in the presence of strong interference signals. Given that the KESRX01 receiver is intended for fixed frequency operation and is intended for use in a number of different countries and applications then the typical "adjacent channel" spectrum is not known. It is difficult to determine in this situation what might constitute a fair test and what is acceptable. It is hoped that the following standard tests on

the example 434MHz receiver provide a good general indication of what can be achieved.

1) Spurious Free Dynamic range: This is a standard test of receiver linearity. Two interference tones, f1 and f2, are selected which are offset from the wanted signal such that the 3rd order inter-modulation product, 2f1-f2, falls on the wanted signal. The level of the two-interference tones is increased until the 3rd order product is detected in-band. Measurements at offsets from +1MHz to +100MHz were taken using the example receiver and the results are shown in Table 1. The recorded level was taken by monitoring the wanted signal at the RSSI output and noting the point at which the interference product increases the RSSI output noise floor by 25mV DC(As a reference a -103dBm CW wanted signal would raise the RSSI output by 50mV).

Offset from wanted	two-tone frequencies	two-tone power level
+1MHz	435 and 436	-85dBm
+5MHz	439 and 444	-46dBm
+10MHz	444 and 454	-44dBm
+25MHz	459 and 484	-36dBm
+100MHz	534 and 634	-27dBm

Table 1

2) Desensitisation and AM cross-modulation: This measurement is done in the same way as the Spurious Free Dynamic range test but in this case with one interference tone offset above and below the wanted signal. The point at which the interferer causes a 25mV DC rise in the RSSI noise is noted both for a CW interferer and a 1kHz, 50% AM modulated interferer. The results are shown in Table 2.

	Interferer level (dBm)			
Frequency offset	+ offset CW	+ offset AM Modulated	- offset CW	- offset AM Modulated
1MHz	-78	-84	-98	-101
2MHz	-57	-63	-69	-76
10MHz	-38	-46	-44	-49
20MHz	-37	-42	-46	-50
50MHz	-34	-40	-40	-42
100MHz	-21	-30	-27	-32
200MHz	-16	-22	-16	-22
500MHz	-10	-16	NA	NA
1GHz	-4	-9	NA	NA

Table 2

C. PLL Design

The base and emitter of a single transistor are bonded out to XTAL1 and XTAL2 pins to allow the user to implement a quartz crystal reference oscillator. If preferred an external reference signal can be used to drive the buffer amplifier. All the functions required to implement a PLL are included. The local oscillator (LO) frequency is stabilised by phase-locking it to the reference signal. The feedback divider ratio is fixed at 64 so that the reference frequency (Fref) is related to the LO frequency(Flo) by :

$$Fref = Flo / 64 \qquad (1)$$

An external inductor and varactor make up the LO resonant tank (see Fig 3 and 4) and the

free-running LO frequency (ωo rads/s) is given by :

$$\omega_o = 1 / \sqrt{LC} \qquad (2)$$

where C is the total capacitance across the inductor.

The passive loop filter voltage swing is limited to 0.5V to Vcc-0.5V and care should be taken to ensure that the control voltage is in the centre of this range when the loop is locked for nominal component values and typical conditions thus allowing for component tolerance and temperature variations. It is also important to ensure that losses in the resonator tank are kept to a minimum.

The natural loop frequency(ωn) and damping factor(ξ) of a second order, type II PLL are set using the following formula to calculate the loop filter component values :

$$C = K_{loop} / \omega_n^2 \ \& \ R = 2\xi\omega n / K_{loop} \qquad (3)$$

where K_{loop} is the loop gain :

$$Kloop = KvcoKpd / 64 \qquad (4)$$

(Kvco is the VCO gain in rad/s/V and Kpd is the phase detector gain in A/rad)

D. IF amplifier and AM detector

The KESRX01 receiver is able to handle a wide range of input signals from the sensitivity level up to -20dBm by virtue of the successive detection logarithmic amplifier following the IF filter. ASK demodulation is performed by making use of the integral Received Signal Strength Indicator (RSSI). A typical plot of RSSI DC output voltage versus input power is given in Fig. 7. The slope of the linear portion is typically 20mV/dB

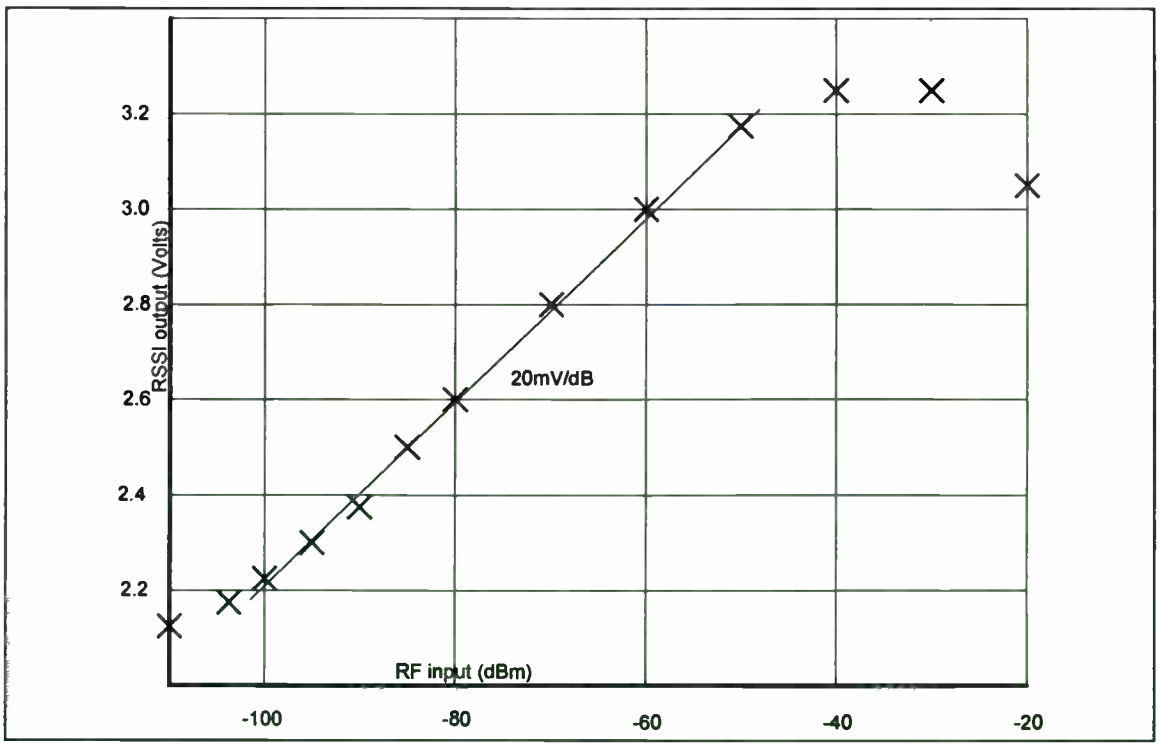

Figure 7

Data Filter and Slicing: Sensitivity can be optimised by filtering the demodulated signal to reduce high frequency noise prior to "slicing"

E. Baseband design

the data at the comparator. An active 2nd order filter can be implemented and the 3dB bandwidth set by two external capacitors. The actual bandwidth that is chosen depends on the data-rate and the extent of mark/space distortion and delays in the data output that can be accepted. In the example circuit a 5kHz Bessel was used and distortion in a 2kHz demodulated is practically negligible whilst still providing some reduction in the noise riding on the RSSI output. The Peak Detector function can be used to determine the threshold level by tapping down from the peak voltage so that the threshold sits just below the noise. In this ways errors will only occur when the tangential sensitivity point is reached.

F. Range and the Antenna Factor

Clearly, as with any radio system, the receiver antenna factor(AF) is critically important in achieving the desired range. The efficiency of the antenna is often constrained in this type of system by the requirement for a small antenna (physical size << wavelength) and in some cases may be totally enclosed. Fig 8 indicates what is theoretically achievable [1] with this receiver (sensitivity = -103dBm and matched to a 50ohm signal source) versus antenna factor for a range of radiated powers : -10dBm to -40dBm.

For Example : Field trials have been carried out to asses the achievable range with a simple, off the shelf, base loaded whip connected directly to a hand-held receiver. The receiver antenna factor for this arrangement was measured and found to be 30dB; this is equivalent to an antenna gain of -7dBi. Data was reliably decoded with this receiver, without error, over 20m for 1μW(-30dBm) e.r.p. (as opposed to 7.8m predicted by the model)

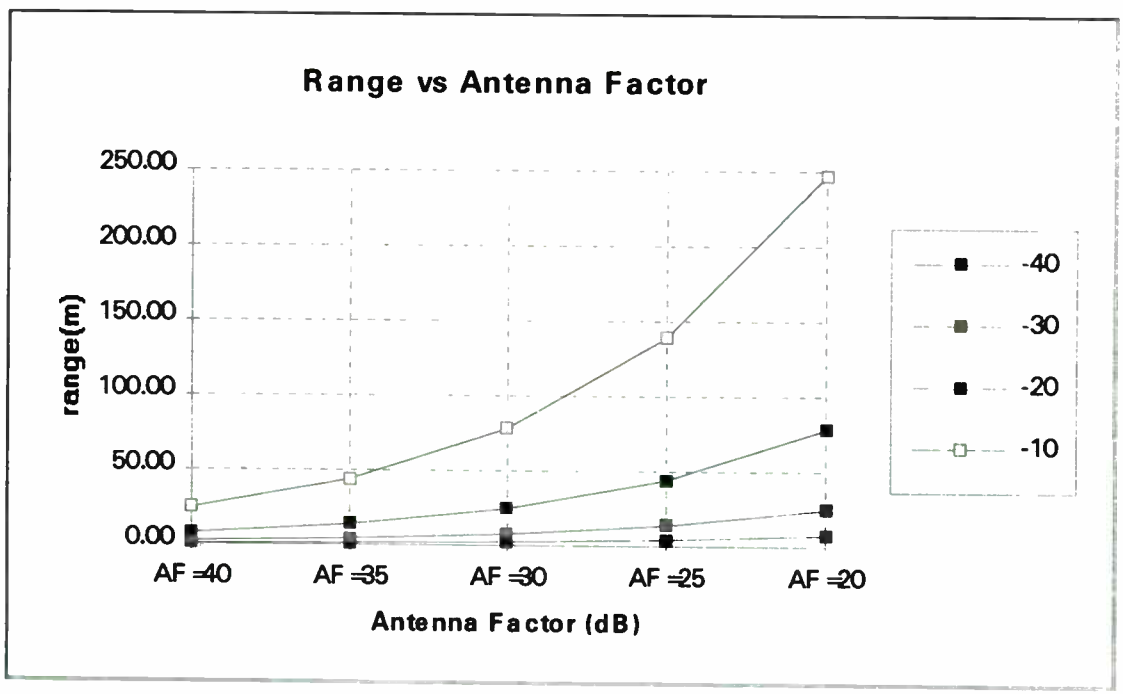

Figure 8

III Conclusion

Advances in Bipolar semiconductor technology have made it possible to fully integrate a 290 to 460MHz ASK receiver for use in the unlicensed, low power applications. Further to this the much proven and reliable superheterodyne technique can be used successfully for this type of application without expensive filters, and with all its inherent

advantages, and is still competitive in both price and power consumption.

Acknowledgements

The authors would like to thank our colleagues at GPS and Mosaic Microsystems Ltd for their invaluable support.

References

[1] F.L.Egenstafer, "Path Loss and Antenna Gain Elementary Calculations", RF Design, February 1995 pp52

NEW PACKAGE & SILICON TECHNOLOGY FOR RF FRONTENDS

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Abstract

1.Dual SMD transistors in a new s-mini SMD package have been developed for RF applications. The SOT353 & SOT363 are 5 & 6 lead packages with a '0805' outline.
The lead pitch is 0.65 mm (25 mil) which is optimal for use in conjunction with 0402 passive components. Combining two matched advanced bipolar technology dies (F_T>9 GHz) in one single package results in a better & smaller RF application for a low price. Three configurations are being released: A cascode connected pair of transistors, a differential pair and dual independent transistors. A few applications will be explained in more detail.

2.A new RF-Silicon technology has been developed, pushing the limits of Silicon further. It is characterized by a FT > 20 GHz (Fmax> 30 GHz) and optimized for low voltage applications. The self-aligned double poly technology has an ultra low noise figure (Fmin< 0.9 dB at 2 GHz!) and extreme low feedback capacitance; resulting in an increased Power Gain.
(a packaged device has a GP> 20 dB at 2 GHz and Gp>10 dB at 6 GHz)
Three complete new transistors are being transferred to production in the near future. They will prove that Silicon can be used for applications at several GHz remaining a superior candidate for low cost wireless applications.

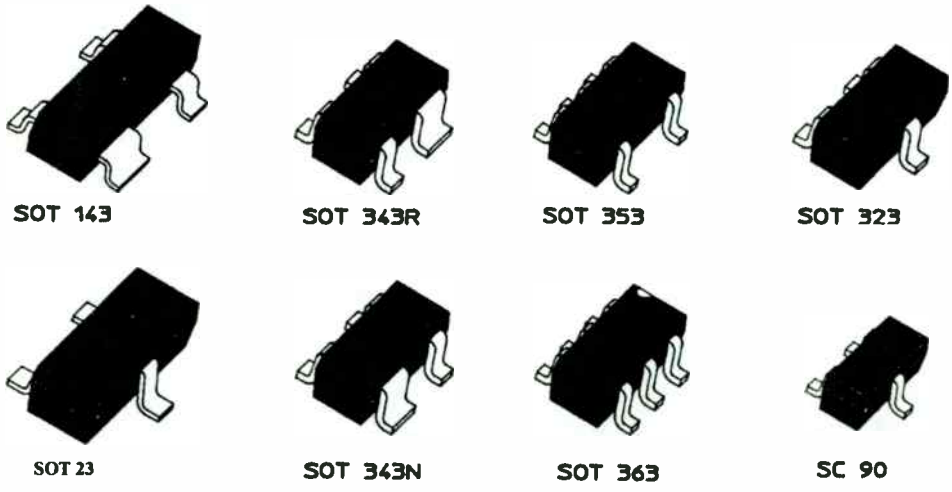

Figure 1: *low cost SMD packages for RF applications (The SOT353/363 were recently introduced)*

1. APPLICATIONS WITH DUAL RF TRANSISTORS

Although Semiconductor Processes with integrated high Q coils and capacitors are still expensive, applications demand for lower cost more integrated solutions.
An intermediate, price attractive solution to this problem, is the combination of RF transistors in one single package. Including external components (which choice are left to the circuit designer) the size can be smaller than fully integrated solutions because the package is very small. Furthermore, due to the low lead inductances a better RF performance can be expected. Target applications for these transistors are: Oscillator, Mixer, Low Noise & Buffer amplifier. Two applications will be explained in more detail: A balanced mixer and an extreme low current low noise amplifier for a pager application.

A. A balanced mixer amplifier.

The BFE505 and BFE520 are emitter coupled transistors in one package.
Advantage for use is the good matching of both DC and RF parameters. The Symmetrical package guarantees a good symmetry of the package related parasitics.(see internal wiring diagram, fig 2)
Balancing signals in RF circuits can result in lower 2nd order intermodulation products, a lower radiation (PCB crosstalk) and enables the use of isolated ports in a mixer because of the resulting virtual ground point. Unfortunately, many RF filters, VCO's and antenna's are still single-ended devices, making a unbalance to balance transformer necessary.

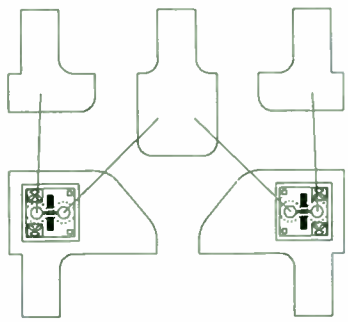

Figure 2 wiring diagram BFE505

Transformer design

Most subscriber applications are narrowband (B/F0 < 10 %) and thus the transformer design can be narrowband also. A coupled transmission line design has a fairly high bandwidth, but the size is a problem. Another way of making balanced signals is the use of a lumped element phase shifter.

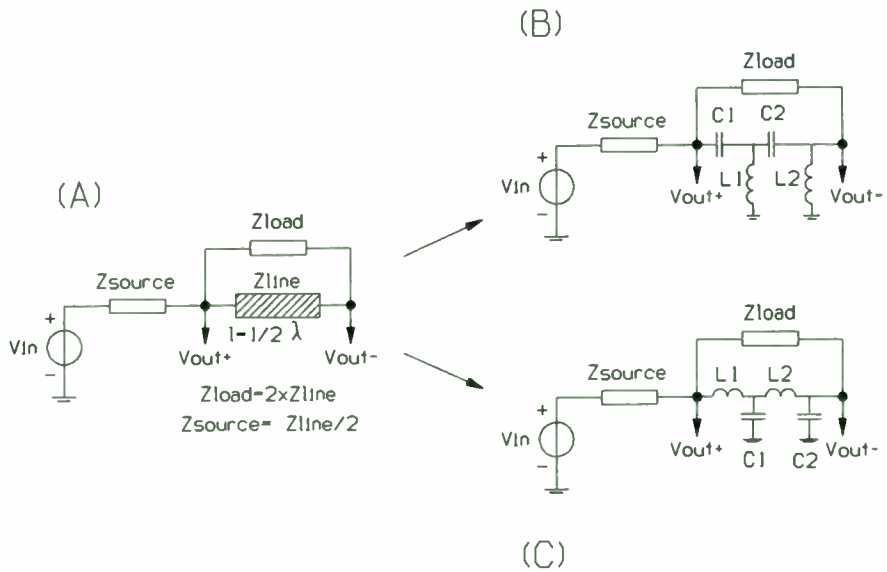

Figure 3 transformer principle

The most simple proposals are shown in fig. 3.
The transformer idea was tested in a 50 ohm environment and it proved to be a feasible design.

The most critical parameter of this kind of transformer might be the reproducability; since tunable designs have to be avoided in any case. A small sensitivity analysis indicated that when a 1:4 transformation factor is used, it is not necessarily a problem.
The basic idea of this transformer is taken from a 1/2 wavelength 1:4 transformer where the transmission line can be replaced by a double LC section (A,figure 3).There is a choice between a high-pass (B) or low-pass (C) solution. The 180 degrees phase shift cannot be obtained from a single LC-section, so a double LC section has to be used.

Practical values of L1, L2, C1, C2 are determined by:

a: The impedance level
b: The bandwidth of the phase shifter
c: The reproducability

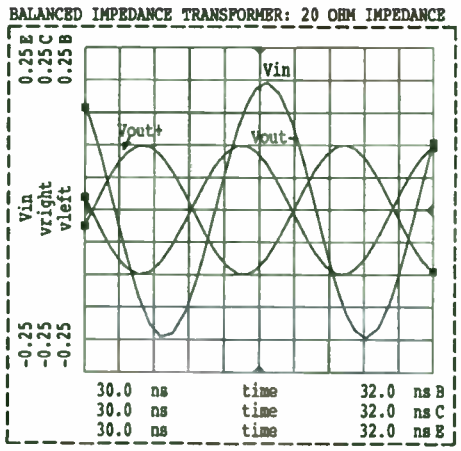

Figure 4 Input &Output voltages of un-bal transformer.

$$C1 = C2$$

$$L1/L2 = 1/2$$

$$L1 = 1/(2 \cdot C2 \cdot \omega^2)$$

Starting values obtained by a simple mathematical analysis are shown. The use of simulation can be a powerful tool to approach the problem. Optimizers are often seen as dangerous simulation tools, since they might cause the designer to loose the right viewpoint on the circuit. However, when carefully managed, they are in fact a very suitable alternative for mathematical analysis and they provide numerical solutions to difficult problems.

In the transformer case, the analysis is focussed on a spread-insensitive design.
This is done by variation of frequency and component values while optimizing.
A nice feature of the optimizers is that an optimization can be carried out at the same time as the component values are varied! In the Microwave Design System of HP so called 'ANALYSIS CONTROLLERS' can be used. (see fig 5)
One of the difficulties is to get the right feeling for weighing factors of the optimization goals since the 'optimal' design depends on the application requirements, which are not always fully clear.
By actually building and measuring circuits one can build up experience. What is of primary importance in optimizations is reduction of the variable elements and correct setting of the optimization boundaries. (starting values) In some complicated cases, a so called Hybrid Optimization can help when the good starting values are not known. The use of Hybrid optimization should not be done with too many variables specified

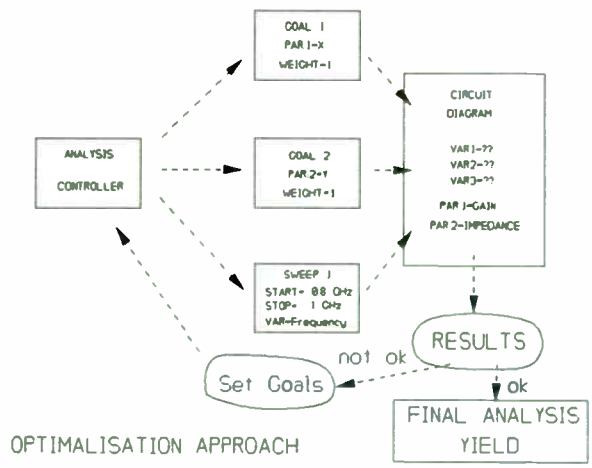

Figure 5 Design approach

Mixer design

In a single balanced mixer; there are some philosophy's which determine the circuit design.
Choice to be made are:

*Balancing of Local Oscillator or RF signal
*Balanced or single-ended IF output match
*Power Level of the Local Oscillator
*Feedpoint of the unbalanced signal at base or emitter

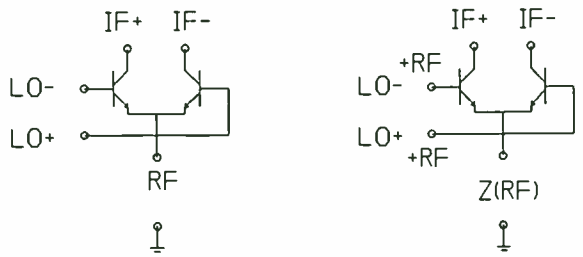

Figure 6 possible signal connections LO/RF and IF.

In fig. 6 the different topologies are shown. (the LO and RF signals can be interchanged) One of the main reasons of using the single balanced mixer is the increased isolation that can be obtained between its RF and LO ports. It also helps the designer; since impedances of the RF source at LO frequency have no influence on the mixer performance. It can be seen as a real 'building block'.

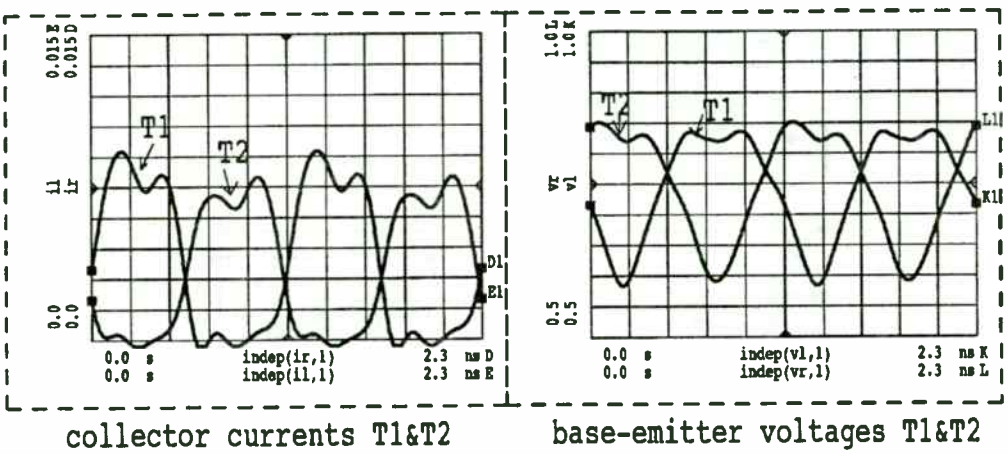

Figure 7 Simulated waveforms in the single balanced mixer

An additional advantage when the RF signal is balanced: A very high IP2 (no second order intermodulation.)
When the LO signal is balanced; the input power can be less than normal possible in a single transistor mixer. This is due to the 'comparator' action of the differential pair: Only a small voltage difference between the two bases is sufficient to get complete current switching (see fig. 7). The comparator action can only be effective when a the emitters are current-sourced. The internal emitter connection of the SOT353 package can provide an internal virtual ground point.

The IF output is taken from only one of the two transistors, since it saves components. When a balanced output is needed, the circuit can be changed accordingly.
Resuming:
The symmetric loading of the differential pair makes it far more easy to get the high isolation.
Furthermore, because of the internal virtual ground for the LO frequency the comparator action of the differential pair assures fast switching and thus a high conversion gain at low LO power.

When the transformer and the differential pair are connected together, an extra coil is necessary to tune out the differential input capacitance of the balanced pair, otherwise the wrong phase shifts are obtained and balanced switching is impossible. Since the impedance level at the unbalance input of the transformer is in the order of 10 Ohm, an additional LC section is necessary to obtain a 50 Ohm LO input impedance (L.O.match)
The same holds for the RF input.(RF match) The total schematic diagram is shown in fig. 8.

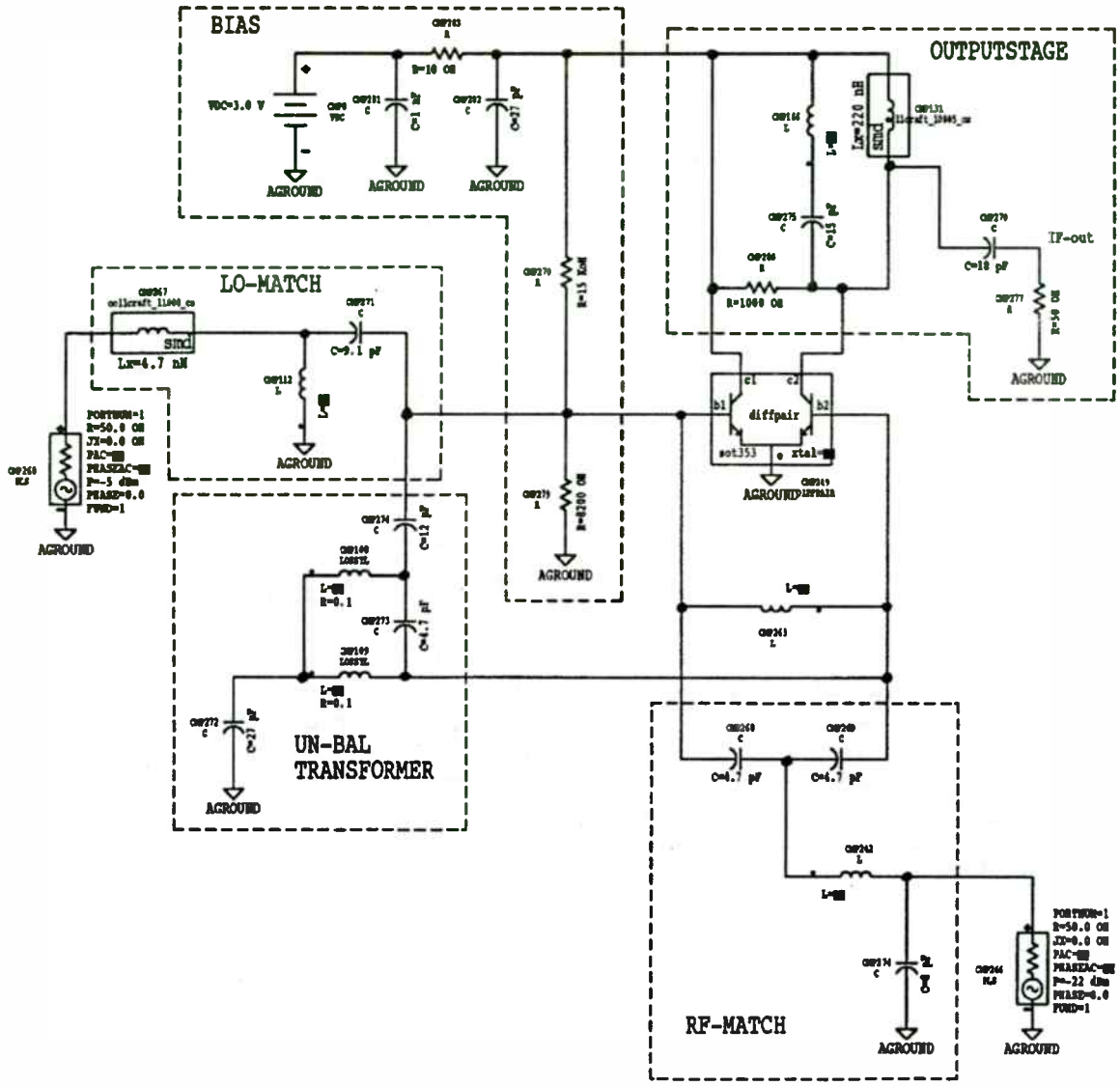

Figure 8 circuit diagram balanced mixer

Building & measuring the circuit

When the circuit diagram is defined, a translation to a PCB can be made.
During lay-out phase one might discover that it is difficult to realize the actual circuit within design rules and available space. It is therefore better, before starting to design the circuit, to already make a proposal drawing for the component placement. The pinning of the BFE505/520 was chosen to fit best to the application. Nevertheless, it might still be useful to compare different topologies, not only on their performance, but also their 'lay-out-ability'.
When finally the lay-out is made, the circuit extraction function of the simulator can be used to convert it back and to perform a 'check' simulation. Small changes to the layout can be made to tune the design.
A sensitivity analysis, finally, can give us an idea of the reproducability.

Now the circuit can be built and measured. When the right models for the chip capacitors, resistors and the SMD coils are used, the measured results should be close to the simulated results.
In the balanced mixer example, the components are placed very close to each other and it cannot be expected that the design is first-time-right. (see the lay-out in fig. 9)

However: The first measurement results were already close to the optimization goals and after changing some capacitor values slightly, the target specifications could be reached.

The final measurement results are:

Supply: 3 volts, 5 mA
L.O. power: -5 dBm
Conversion Gain: > 11 dB
SSB Noise Figure: < 9 dB
RF to LO isolation: > 20 dB
LO to RF isolation: > 20 dB
Intermodulation IP3 input: 0 dBm
Input Impedance LO: 50 Ohm
Input Impedance RF: 50 Ohm
Collector Impedance at IF: 1 kOhm (transf. factor=20)
PCB: epoxy FR4, height 1.0 mm
Size of the PCB (active area): 14 x 8 mm
Number of SMD components: 18

The measurement results show that with the aid of simulation tools and the right models, high performance circuits can be built with low-price components.

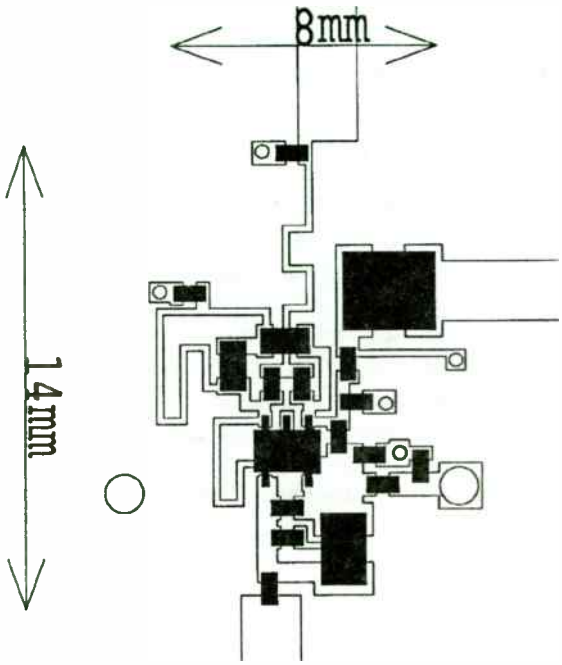

Figure 9 lay-out mixer

B A Pager preamplifier

The same design method was used to design an extreme low current preamplifier. The BFC505 is a cascode transistor with internal connection of collector T1 to emitter of T2.
This assures a lower parasitic loading of the cascode (compared to when two separate transistors are used) and has less chance for oscillations. The main reason of using the cascode amplifier is its extreme low feedback capacitance. The transconductance of a bipolar transistor is quite high, but at low current, the feedback capacitance will become the most dominant gain restriction. A cascode is a solution for this problem. At higher frequencies, the common base transistor in the cascode can become unstable, this is mostly the reason why a cascode is seen as a dangerous potential instable device. With the ultra-small SOT353 package, the base-lead inductance is kept minimal. This brings the resonant frequency of the common base transistor above 4 GHz, were it can be damped easily. The best way to stabilize the transistor is a small series resistor in the output: this will not give a significant gain reduction, but it will suppress possible oscillations. (damping!) It is depending on the actual layout whether this resistor is necessary or not.

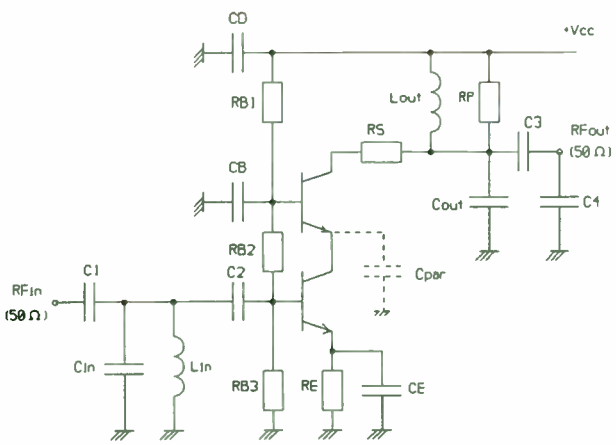

Figure 10 LNA with cascode

The Gain of the cascade amplifier is not limited by the transistor but by the Quality factor of the resonant circuit at the output. The higher the Q, the lower the reproducability, however. In most actual pagers manual tuning of the coils is used and this was applied in our design also. At 1 Volt supply and a current of only 350 micro amp. a Gain of > 17 dB was obtained, with a resonant circuit with Q=30 only. The Noise Figure F= 3 dB at 900 MHz (including circuit losses) is quite low for such a low current device.
In many pager designs, the loop-antenna has a balanced output, a balanced amplifier might be an attractive solution, especially when a balanced mixer is used also. A balanced cascode amplifier can be built up with two cascade transistors. If a normal balanced amplifier is sufficient; the differential pair type could be used.

C. Other applications:

A very small sized VCO can be developed with the BFM or BFC types. When enough supply is available, it is advised to use the cascade configuration for DC , this way the efficiency is better. When the supply voltage and power output requirement conflict to much, the SOT363 dual transistor can be used and it is possible to use the cascade configuration for RF signals, but for DC the parallel configuration can be used.(see fig.11 & 12) This assures the availability of enough supply voltage for the buffer stage. Numerous other configurations can be designed, depending on the application requirements. (Size, Pulling of VCO, Output Power,.....)

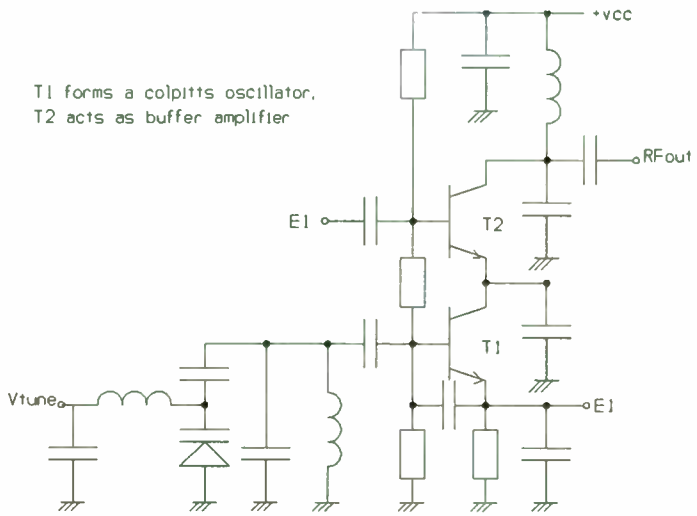

Figure 11 VCO-buffer combination

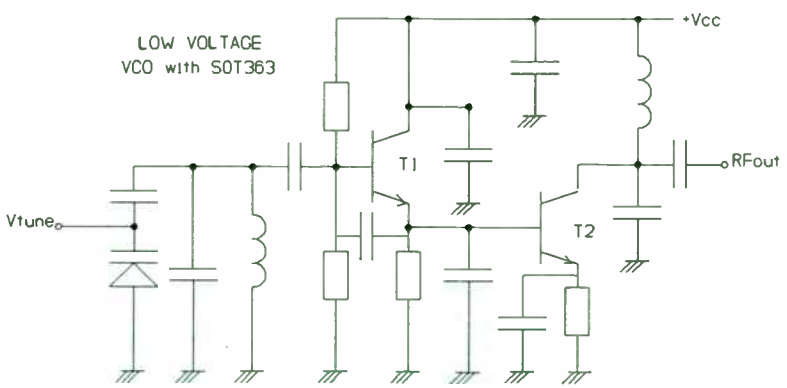

Figure 12 Possible realization of a VCO with BFM505 (SOT363)

2. AN UPGRADE OF SILICON TECHNOLOGY FOR LOW VOLTAGE APPLICATIONS

Performance upgrade of our bipolar processes is (amongst others) obtained by reduction of the emitter finger pitch and this way reducing the feedback capacitance & effective base resistance. These narrow emitter pitch (state of the art: 3 micrometer) in combination with shallow base widths obtained through thin epilayers and direct implanted emitters is a suitable technology for Transition frequencies up to 15-20 GHz and Voltage ratings of 5 Volts and higher. For very low voltage applications, improvements can be found.

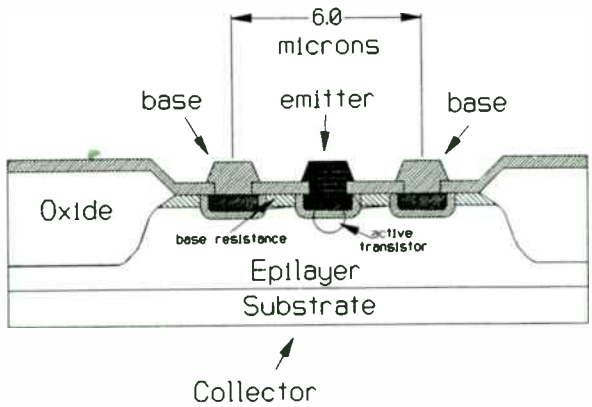

Figure 13 advanced bipolar RF transistor

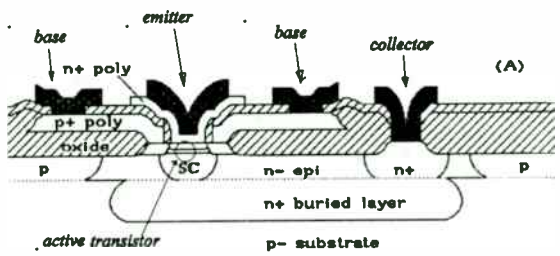

Figure 14 double-poly buried layer transistor

A closer analysis has add some refinements to our standard advanced technology. (where the emitters are implanted and the actual base is formed by means of a thermal anneal step) In the Double-Poly technology the use of poly emitters has resulted in a very steep emitter dope profile, which enables us to produce transistors with Transition Frequencies as high as 25 GHz at Breakdown voltages of 4.5 Volts. (At 3 Volt breakdown, 35 GHz was measured!) The use of poly-base contacts has resulted in a lower Base resistance and the use of a Selective implanted collector has led to a reduction of the non-active base-collector capacitance without the need of reducing the emitter finger pitch further. (see fig 13&14) The result is a submicron-emitter width process (W_E=0.5 micron) in which the emitter finger pitch is no longer the dominant restricting parameter. A 4 micron emitter pitch technology was used for these transistors, and a more narrow pitch is unnecessary.

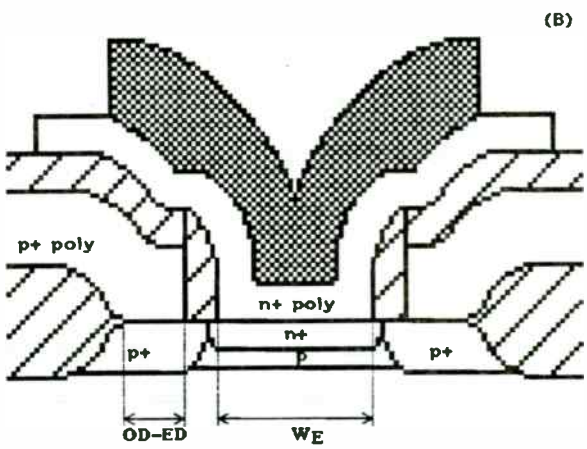

Figure 15 close-up of active transistor (emitter=topmetal)

At GHz frequencies, the gain restriction is a result not only of the diffusion technology, but also of the packaging. Taking a closer look at this problem, we managed to produce transistors with an eliminated package feedback capacitance and a reduced emitter inductance. (see fig. 16)

We are currently tuning this process and the first types to be produced will be released by Q1 1997. (large quantity samples by Q2 1996)
The first measurements on packaged devices have been done already, and ultra low noise Figures in combination with very high gain indicate their suitability for RF frontend applications.

A Gain of **18 dB** with an Associated Noise Figure of **1.2 dB at 2 GHz** and a DC operating point of **2 V; 5 mA** is a real breakthrough for a Silicon based device.

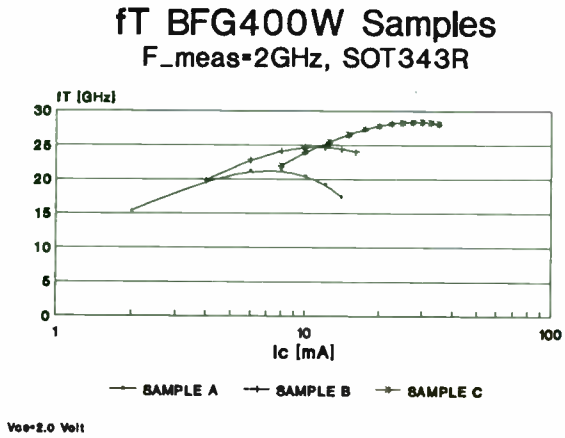

Figure 17 F_T versus current

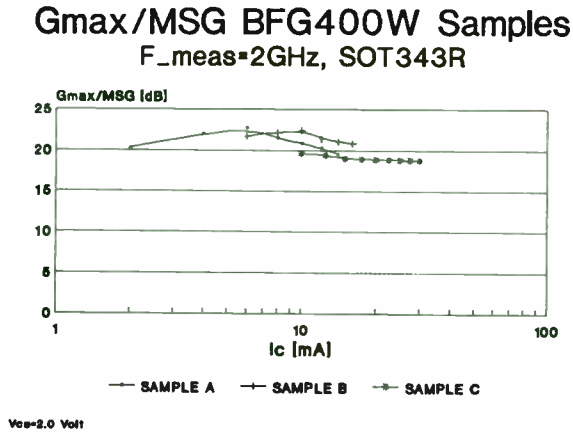

Figure 18 Gain versus current

The first transistors to be produced in this new process will be small signal types: The BFG403W, BFG410W and BFG425W are transistors primarily intended for low noise amplifiers in the frequency range 1-6 GHz.
(see measurement graphs Sample A,B,C in fig 16&17)

A comparison can be made of the main parameters important for these transistors:

1: the ratio of feedback capacitance and nominal current;
2: the Noise Figure (related to R_B and F_T at high frequencies)
3: the Transition Frequency
4: the Breakdown Voltage BVCEO.

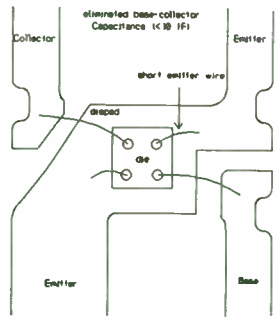

Figure 16 SOT343R wiring diagram

See table 1. This will make it clear where the improvements of these transistors are found.

process version	Cbc/Ietop (fF/mA)	NF 2 Ghz (dB)	top-F_T (GHz)	BVCEO (V)	G_p 2 GHz (dB)	Em.-pitch (microns)	package
existing	14	2.0	9.5	>10	14	5	SOT143
existing*	7	1.6	16	7	17	3	SOT143
doublepoly	5	1.0	25	4	22	4-6	SOT343R

*optimized process with extreme thin epi-layer.

CONCLUSIONS

1:High performance, small size RF subcircuits can be made with dual' RF transistors, for a low price. These semi-discrete solutions remain a very attractive solution for wireless applications.

2 The Double-Poly process, combined with the right RF package results in major improvements in Gain & Noise performance of RF transistors.
The advanced, though not complex process will further improve the strong position of silicon in the wireless market.

Aluminum Thick-Metal-Backed Circuits: Conductive Adhesive Technology

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Thick metal backed (TMB) printed wiring boards are commonly used in high frequency wireless circuit applications requiring significant thermal dissipation, such as power amplifiers. The thick metal backer typically functions as a ground plane as well as a heat sink. When the thick metal backer provides an electrical grounding function as well as thermal and mechanical function, conductivity through the interface between the printed circuit card ground plane and the TMB can be critical. In-plane gaps in the conductive path between the circuit ground and the TMB are typically maintained at less than 1/4 wavelength at operating frequency in order to maintain acceptable localized ground paths for the circuits and devices, minimizing impedance and capacitance between the circuit ground and TMB. Electrical interconnections between RF/Microwave printed wiring boards (PWB's) and TMB's have traditionally been accomplished using sweat soldering, plated through holes, or mechanical interconnections. More recently, conductive adhesive technology has been investigated to mechanically and electrically interconnect the PWB to the thick metal ground plane, due to perceived advantages in terms of cost and performance. However, providing mechanically and electrically stable interfaces between conductive adhesives and large metal conductor structures (ground plane on the printed circuit card and/or thick metal backer) has proven to be a significant challenge, particularly in the case of aluminum backed circuits. Aluminum, while being a cost effective material for these applications, is prone to oxidative and hydrolytic processes induced by moisture and catalyzed by temperature, active ionic species, galvanic effects, and other environmental factors. These corrosion processes at the interface between the conductive adhesive and the adherend can compromise both the electrical and mechanical stability of the bond, and thus the performance and reliability of the packaging structure.
This paper will describe work performed at IBM Microelectronics to understand the interfacial resistance between conductive adhesives and typical metal bonding surfaces for TMB printed circuits, and will discuss how reliable and functional interconnections were achieved for high volume commercial designs using conductive adhesive bonding technology.

WIRELESS LOCAL-AREA NETWORKS (WLANs)

Wireless Local-Area Networks (WLANs)

Session Chairperson: Ron Ruebush,
Celeritek, Inc. (San Jose, CA)

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Standards and Trends in Wireless Local Area Networks

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Wireless Local Area Networks provide the network nodes with mobility that can reduce the wiring cost and time. Different technologies are used for indoor networks based on optical or radio frequencies. In radio frequency field, Standard Radio (RF), Frequency Hopping Spread Spectrum (FHSS), and Direct Sequence Spread Spectrum (DSSS) are three major approaches. In optical range, Directed Beam IR (DBIR), and Diffused IR (DFIR) are two dominant solutions. The FHSS and DSSS use the ISM (industrial, Scientific, and Medical) bands for spread spectrum LANs. RF uses ISM or 18 GHz frequencies. Some of the solutions such as DBIR are not appropriate for mobile applications because of their Line of Sight (LOS) requirement. Regarding the operation distances, DBIR is limited to about 80 feet range while some approaches such as DSSS can cover up to 800 feet. CSMA is the dominant access method used in Wireless LANs. However, reservation slotted ALOHA and token ring are used too.

Code Division Multiple Access (CDMA) method is the best solution for multivendor environments and it lets the heterogeneous systems operate simultaneously. In Time Division Multiple Access (TDMA) approach, all systems sharing a channel should cooperate their access with each other. CDMA has a good anti-multipath characteristic which results in a reliable transmission at higher data rates. CDMA is efficient for ISM band but power control is needed to avoid the near-far problem. CDMA is not appropriate when data bursts are supposed to use the whole channel capacity. Thus many ISM band wireless networks in the market use spread spectrum without CDMA. However, in the spread spectrum without CDMA, transmission reliability requirements result in lower maximum data rate. This problem can be solved by approaches such as multiamplitude, and multiphase modulations. Using several orthogonal codes by each transmitter in a single channel CDMA provides a perfect power control and can have a baud rate in the order of 20 Mb/s in an ISM band.

There are three major standardization activities in wireless LAN field. IEEE 802.11 standard works on DFIR, DSSS, and FHSS in ISM bands. Its focus is on physical and Media Access Control (MAC) layers. The High Performance Radio Local Area Networks (HIPERLAN) uses the recently released 5.12-5.3 and 17.1-17.3 GHz bands for data communication with a minimum bit rate of 20 Mb/s. The WINFORUM introduces the limitation on air time usage. When the frequency time share of a device is restricted, the other devices can use the same band.

A new issue in wireless LAN is implementation of a real-time distributed architecture that allows a process to run on any available processor. In such an approach, the Personal Digital Assistants (PDAs) can be used in a wireless LAN. PDA has limited processing power and can conserve the battery power. The processing power of computers on the wireless LAN is used by PDA when needed.

DESIGN OF A MINIATURE, LOW COST, 2.4 GHz TRANSCEIVER SYSTEM USING A SIMPLE BUILDING BLOCK APPROACH.

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I. Abstract

This paper demonstrates that a straightforward, low cost, miniature transceiver can be built for the 2.4 GHz ISM band using RFIC building blocks (LNAs, mixers, filters, and power amps) in surface mount packages. Detailed information is given on the application and usage of each RFIC function in the transceiver. A complete transceiver is built and performance data is shown.

II. Introduction

The 2.4 GHz Industrial Scientific and Medical (ISM) band is becoming popular for unlicensed transmission of spread spectrum signals. The primary function of the transceiver is to transmit and receive a 2.4 GHz carrier signal and frequency convert it to the intermediate IF frequency. The transceiver usually contains low noise amplifiers, power amplifiers, filters, mixers, a switch, and a local oscillator. The design approaches of the transceiver section ranges from discrete transistors [1] to single chip solutions [2].

One cost effective approach is to utilize general purpose RFIC building blocks to perform all major functions required. By using generic RFIC blocks (LNA, mixer, filter, etc.) the system designer can weigh the cost verses performance issues for each block. As system requirements become firm, the designer can substitute different blocks based on system financial and performance changes. This flexibility is the power of RFIC blocks.

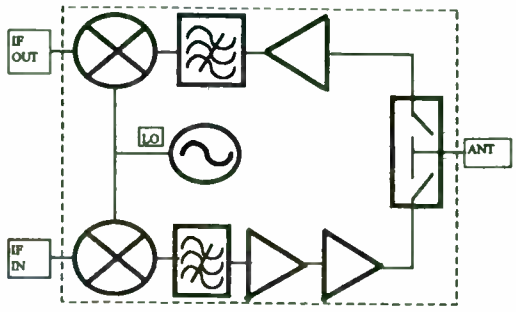

Fig. 1 Transceiver schematic.

Hewlett-Packard offers a variety of both Si and GaAs RFIC building blocks that operate from DC to 6 GHz. The user can select the specific frequency, noise figure, power, voltage, gain, etc. of each block. HP does offer discrete transistors that could be made to perform any of the RFIC block functions. However, many system designers today choose not to deal with the additional complexity and board space that discrete transistors present. Also, the cost and performance gains are incremental at best over an RFIC block solution. A single LSI chip solution may exist, but the system designer is now locked into the chip's compromises with no room to cut cost or increase performance.

III. A 3V(single supply) Transceiver

The transceiver schematic shown in Fig. 1 and the photograph in Fig. 2 was built for demonstrative purposes. It shows that a 2.4 GHz, small , low cost system

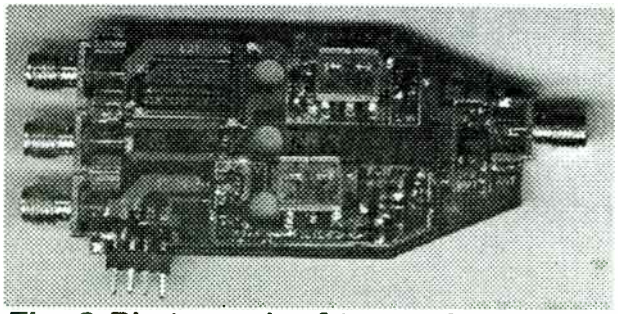

Fig. 2 Photograph of transceiver. Board size is 2.0" x 1.3".

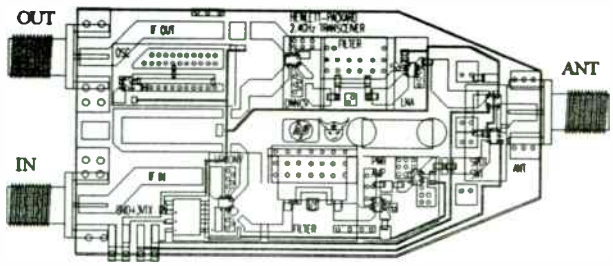

Fig. 3 Drawing of transceiver

can be built. A single 3V DC supply provides power for all functions. The carrier frequency is 2.442 GHz and an IF of 296 MHz was used (any IF from 50 MHz to 500 MHz could have been used). In a complete system the IF would be processed through an I/Q modulator type circuit to base band frequencies. General specification for the transceiver are given in Table 1 below.

Most of the components used are SOT-363 (SC-70) based. This ultra-miniature package only occupies 4 sq. mm. of board space, making it a very efficient and versatile package for a compact design. The MOSFET (used for transmitter power down) and the antenna switch are SO-8 packaged parts. Full transceiver size, including filters, is only 2.0" by 1.3". SMA connectors are used for the IF 296 MHz input and output and the 2.442 GHz antenna. There are four DC connectors; Ground, +3.0 Volts, transmit control (0 or 3 V), and receiver control (0 or 3 V).

Parameter	Value
Voltage	Single 3.0V
RF Transmit/Receive frequency	2.442 GHz
IF frequency	296 MHz
LO frequency	2.738 GHz
Receiver Gain	17 dB
Receiver Noise Figure	4.1 dB
Receiver Input IP3 point	-14 dBm
Receiver current	13 mA
Transmit Gain	30 dB
Transmit Output Power	20 dBm
Transmit efficiency	25 %
Transmit current	125 mA
LO oscillator output power	-5 dBm
LO oscillator current	6 mA

Table 1 Transceiver specifications

IV. Receiver Design

The receiver consists of four blocks. There is a T/R switch, an LNA, a filter and a mixer. The antenna signal passes through a T/R switch (1dB loss) and is amplified by an HP MGA-87563 LNA (1.9 dB NF, 12 dB gain). A Toko 4DFA-2442P-10 image reject filter (1 dB loss) is then used between the LNA and mixer. An HP IAM-91563 active mixer (7 dB gain) downconverts the signal to the 296 MHz IF. Total gain is 17 dB (19 dB - 2 dB) and the total noise figure is 4.1 dB. The mixer has a +4 dBm output intercept point, which translates to a -14 dBm system input third order intercept point. The mixer draws 8 mA current and the LNA 5 mA.

The MGA-87563 LNA requires only three external components. As Fig. 4 shows, a 1.0 nH inductor is used to match the LNA input to 2.4 GHz. A 50 Ω resistor and 100 pF capacitor are used to provide clean DC power. Final performance is demonstrated in Fig. 5.

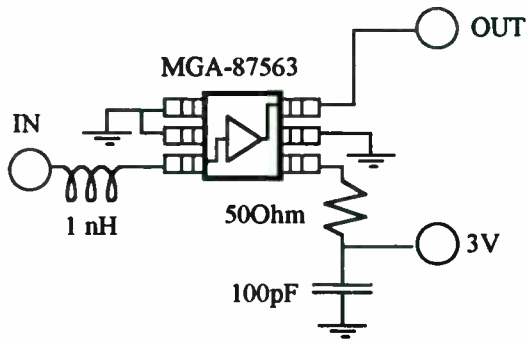

Fig. 4 2.4 GHz LNA design.

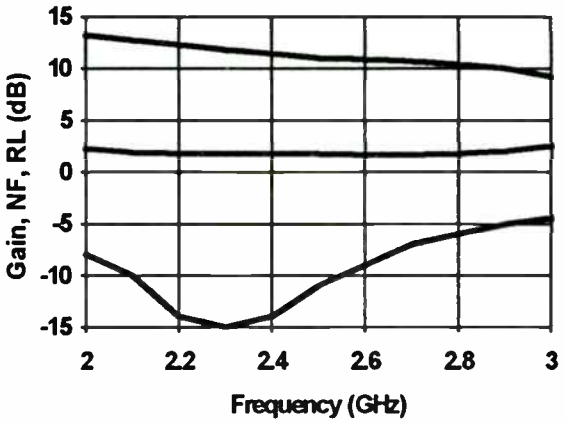

Fig 5. 2.4 GHz LNA performance.

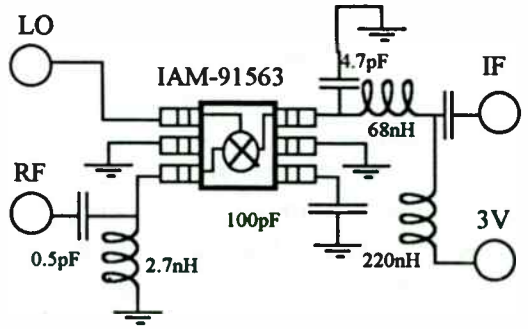

Fig. 6. Downconverter mixer design.

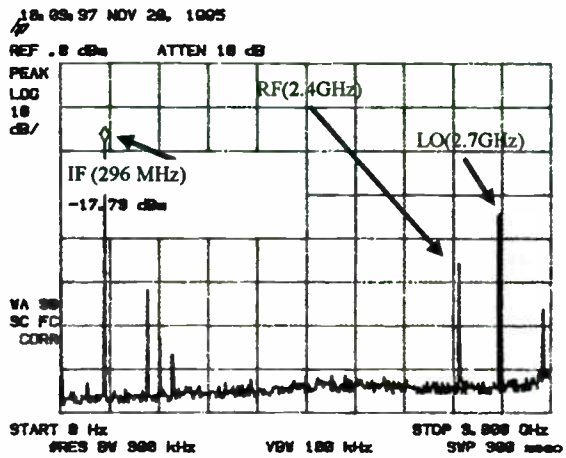

Fig 7. Down mixer performance.

The IAM-91563 is a straightforward design in the application as a downconverting mixer. The IAM-91563 requires 7 external support components. The RF and IF ports must be matched to their respective frequencies. A series capacitor and shunt inductor pair is used for the RF port match. This provides good VSWR while also acting as a high pass filter. A series inductor and shunt capacitor pair provide a IF match while also providing a low pass filter. The LO does not require a match. The last three components are used for DC blocks and choke. Fig. 6 shows the topology used in the transceiver and Fig. 7 the mixer performance. Typical LO drive level is -5 dBm.

IV. Transmitter Design

The transmitter consists of five blocks. There is a mixer, filter, a pre-amp, a power amp, and a T/R switch. The 296 MHz IF is upconverted using the same HP IAM-91563 type mixer used in the receive side. Upconversion gain is 6 dB. A Toko bandpass filter (1 dB loss) is then used to reject the LO on the 2.4 GHz signal. Then a HP MGA-81563 50 Ω gain block (12 dB gain) is used to boost the signal up to +10 dBm power. Next, an HP MGA-82563 is used as a power amplifier (13 dB gain, 20 dBm Pout). The signal is then routed through the T/R switch (1 dB loss) to the antenna. A MOSFET is used to DC power-down the transmit side during receive mode.

The IAM-91563 is not normally recommended as an upconverter, however it's single balanced wide band design allows up mixing applications (There is no LO rejection so a quality filter must be used following the mixer). The HPMX-2007 could be used here as an upconverter block that includes the IQ vector modulator. The IAM-91563 requires 6 external support components. A series inductor and shunt capacitor pair topology is used for the RF (input 296 MHz) port match. A series inductor and shunt capacitor provides an output IF match (2.442 GHz) while also providing a high pass filter. Again, the LO does not require a match. The last three components are used for DC blocks and an RF choke. Fig. 8 shows the topology and Fig. 9 performance.

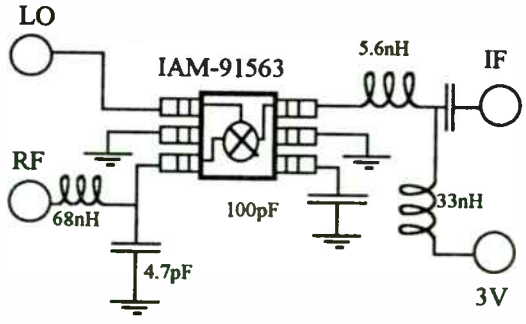

Fig. 8. Upconverter mixer design.

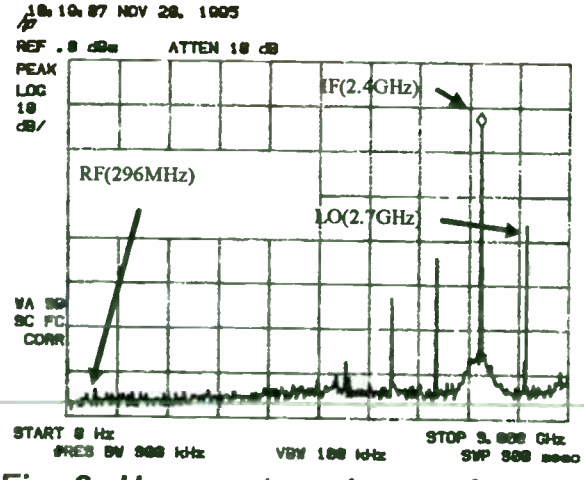

Fig. 9. Upconverter mixer performance including post mixer filter.

The pre-amp and power amp stages are perhaps the simplest to build. An HP MGA-81563 (pre-amp) and MGA-82563 (power amp) are both well matched to 50 Ω internally, no external components are required. The only external components needed are a DC blocking capacitor and RF choke inductor to supply the 3 Volts as shown in Fig 10. The DC line must be clean enough as to not allow RF feedback (potential source of oscillation) and this is done by properly grounding and bypassing. Fig. 11 shows the two stage amplifier performance. More power may be obtained (1 to 2 dB) from the MGA-82563 by power matching it to the antenna load. Also, a harmonic trap may be included to reduce transmitted harmonics and increase efficiency.

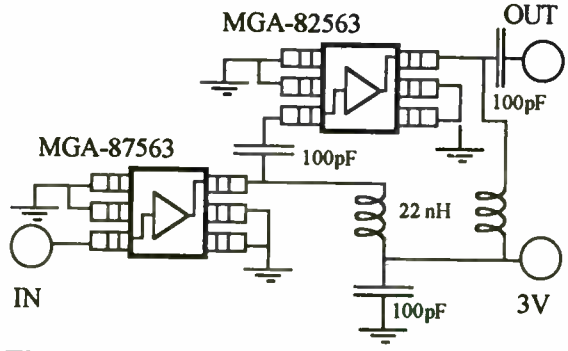

Fig. 10 2 stg. power amp design.

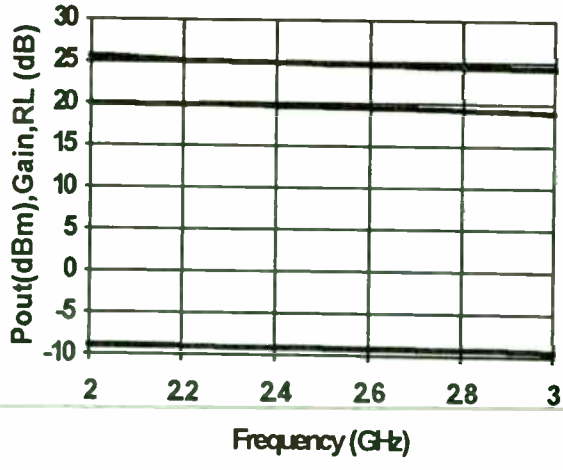

Fig. 11 2 stg.power amp performance.

V. Oscillator Design

The LO is provided by a 2.738 GHz oscillator. An ATF-36163 GaAs FET is used as the negative R generator. A transmission line resonator is used as the frequency-determining element. Seven external components are needed to bias and tune the oscillator. The frequency of oscillation is determined by the length of transmission line and the size of the capacitors. This particular oscillator is sensitive to surrounding elements and bias. Better shielding and a TEM mode high-Q ceramic resonator would give it more stable frequency control. This oscillator could be made into a VCO by adding a varactor as noted in Fig.12 below. A Wilkinson splitter is used to divide LO to the two conversion sections. Output power is -5 dBm to both ports with a single 3 V, 6 mA DC supply.

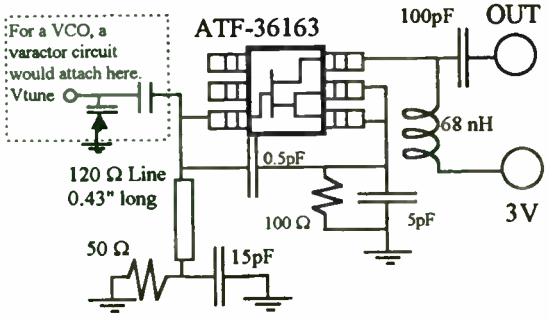

Fig. 12 Oscillator design.

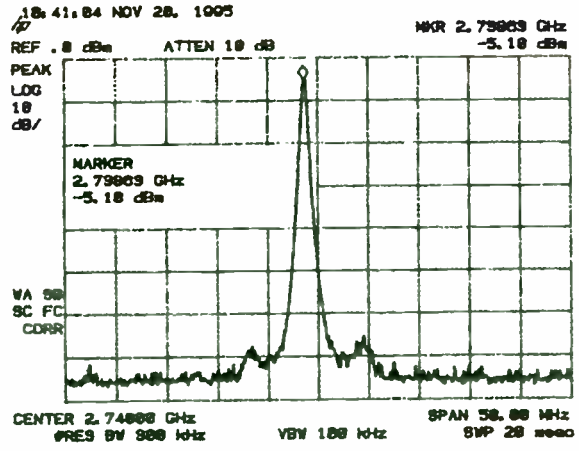

Fig. 13 Oscillator performance.

VI. Transmit/Receive Switch

The transmit/receive function switching is done through the use of the HP MGS-70008 GaAs MMIC switch. This switch is a good choice for this application since it can operate well on 3 volt control and can handle the output power easily.

The switch is normally driven with negative supplies, so the switch ground must be elevated to +3V to allow simple 0V switch drive. This is done by DC isolating the RF ports, pulling all ports (and ground) to +3V, and toggling the control with 0V (off) to +3V (on). The resulting switch requires 5 support components. Typical insertion loss is 0.9 dB and isolation is 18 dB. The switch can handle +24 dBm power and requires a 3 Volt, 1.0 mA supply. C1 and C2 control lines are voltage driven and require less than 0.1 mA.

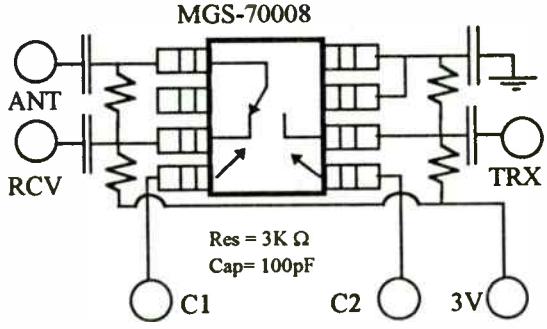

Fig. 14 T/R switch design.

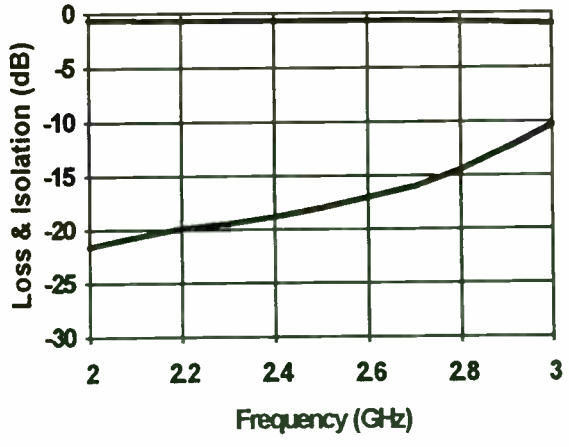

Fig. 15 2 T/R switch performance.

VII. Cost

The cost of a system is highly dependent on volume. The approximate material cost of this 2.4 GHz transceiver system in 10K quantities is shown below in table 2. It should be noted that the RFIC content is only $8.20.

Part # & Description	Section	Cost
MGA-87563 LNA	Rcv	$1.45
IAM-91563 Mixer	Rcv	$1.35
IAM-91563 Mixer	Trx	$1.35
MGA-81563 Amp	Trx	$1.10
MGA-82563 Pwr Amp	Trx	$1.35
MGS-70008 SWT	Both	$1.60
	RFIC Total	$8.20
Toko 4DFA-2442P	Rcv	about $2.00
Toko 4DFA-2442P	Trx	about $2.00
Ind, Res, Cap	Both	about $1.60
Two Layer Board	Both	about $1.00
TOTAL		$14.80

Table 2. Approximate cost of transceiver

VIII. Summary

This paper has demonstrated how a 2.4 GHz transceiver operating on a single 3V supply can be built using RFIC building block. The use of RFIC blocks cuts down the complexity and size from a discrete transistor design while eliminating the cost and inflexibility of a single chip design. RFIC block designs allow quick time to market and the ability to evolve designs to ever changing cost and performance criteria. The transceiver built for this paper shows but one way to apply RFICs to a wireless application. The methodology, however, can be applied to other applications, frequencies, and functions to enable the wireless revolution.

A special thanks is given to John Coward for technician support and Mike Frank for technical assistance.

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Wireless LAN Technology: The Myths and Realities of an Ideal System

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ABSTRACT

Just as the emerging standard for wireless local area networks (LANs) begins to influence the industry, it is becoming clear that wireless data communications is a technology that many users misunderstand. When technology for LANs began to emerge, many industry leaders believed that radio systems eventually would allow wireless connectivity at LAN speeds among portable computers located anywhere in the world.

The impending standard set by the Institute of Electrical and Electronics Engineers (IEEE) 802.11 Committee is the first, but only a small, step in that direction, establishing specifications for interoperability and a minimum level of performance among like systems.

Some people think universal connectivity is just a matter of time. However, portable computer users must realize there are fundamental limitations governing how and where wireless LAN technology can be employed. Efforts are in progress to move this technology forward. Some of this work was brought to the limelight by Apple Computer Inc.'s rule-making petition for a proposed national information infrastructure (NII) submitted to the Federal Communications Commission. HIPERLAN (HIgh PErformance Radio LAN), under development in Europe, is an example of the wireless LAN technology that might be used within this band.

While the IEEE 802.11 standard for wireless LANs in the 2.4 gigahertz (GHz) industrial, scientific and medical (ISM) band is barely off the drawing board, industry groups already are looking to HIPERLAN as newer, faster technology.

In theory, some of that praise seems to be true. HIPERLAN could solve bandwidth problems the emerging 802.11 standard already faces in the 2.4 GHz ISM band. HIPERLAN also promises to offer faster network speeds, up to 24 megabits per second (Mbps) or more. However, even HIPERLAN cannot provide this ubiquitous high-speed access without new spectrum and significant infrastructure investment. Efforts already are being made to improve access to the necessary spectrum.

This paper examines why current wireless LANs have performance limitations, what users can expect in the future and how future network architectures can be constructed to accommodate and exploit wireless LAN capabilities.

I. The Ideal Radio System

Potential users who are not yet educated on the intricacies of wireless LANs may believe that the coming technology is merely a merger of the circuit-switched cellular telephone network and Ethernet functionality. In this mythical scenario, the mobile worker uses a laptop computer with a built-in wireless LAN PC card to communicate wirelessly with another computer or host server located at home, at the office, anywhere in the world. Data rates would be similar to those of the native wired LANs.

While these capabilities are not possible today, many think it is merely a matter of time and technical innovation before such systems become commonplace.

Barriers to implementing the ideal system stem from technical, regulatory, financial and cultural issues. Technically, such a system is possible to build. However, its construction would depend on a huge, expensive supporting wired infrastructure, adequate spectrum and widespread user acceptance. Assuming the industry overcomes these barriers, it may take 10 years of in-building use to reach the point where wireless high-speed data communications is developed for use outside the office environment like cellular phones are used today.

As multimedia technology continues to emerge, the applications for communications will change. The use of the laptop computer as an end terminal no longer may be relevant to the way people work. As the speed of wired LANs increases, the requirements on throughput for wireless LANs will increase. Furthermore, the underlying terrestrial infrastructure is expected to change as asynchronous transfer mode (ATM) technologies and broadband communications become widely available. The ideal system would have to anticipate and accommodate these changes as part of the strategic process of system development.

II. The Facts of Radio Life

Some factors of radio will not change with time:

A. Wireless spectrum is a valuable resource.

Almost all the spectrum below 10 gigahertz (GHz) is assigned or earmarked by the Federal Communications Commission (FCC) for specific purposes. Frequencies above 10 GHz are difficult to use effectively for communications purposes because of atmospheric absorption and the effects of objects in the radio field. Because of these limiting factors, the spectrum set aside for mobile communications must be used with ever-increasing efficiency. As more wireless applications become available, the value of allocated spectrum will continue to rise. Therefore, successful mobile and portable data applications will adopt technology that minimizes the amount of required spectrum.

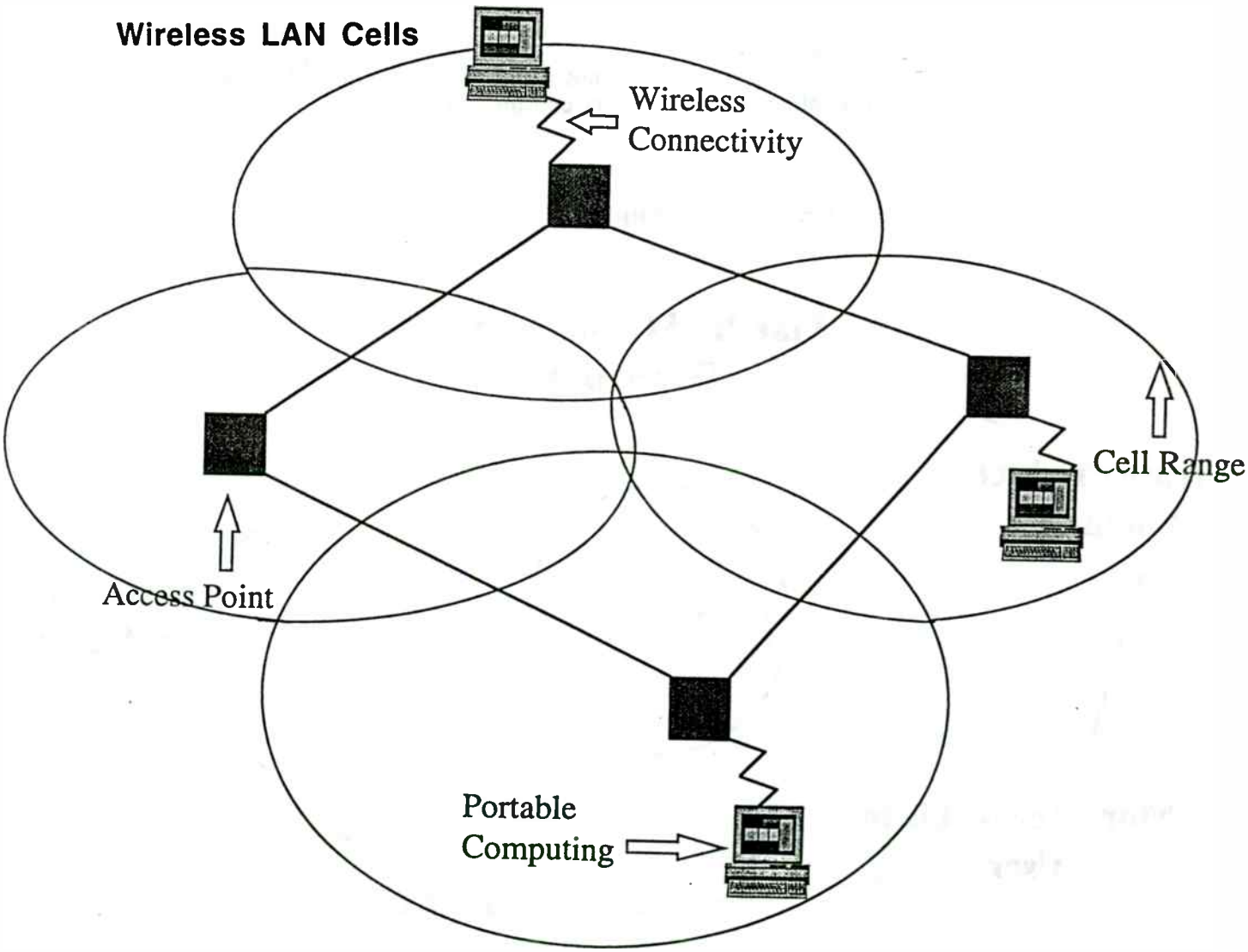
B. Laws of physics limit the ability to increase range through technical innovation.

While there still is some room for improvement in extending range, gains are expected to be small. The science of radio communications already is well developed and has been exploited by military systems for decades. The task of the commercial world is to reduce the size and cost of existing military communications technology from a multimillion dollar, refrigerator-sized box to a PC card that costs $200 or less.

C. HIGH-SPEED LINKS ARE INHERENTLY LIMITED TO SHORT RANGES.

Because fast data rates reduce distance, wide-area coverage at high speeds must be achieved through a secondary backbone system where wireless links are used only for the first hop onto the network. The backbone of a high-speed national system likely will be terrestrial. This is the same principle as the circuit-switched cellular phone system. With a wireless handset, the caller dials a number and presses the send button. Through the wireless pipeline, the signal travels to the first available cell, which then completes the connection through the wired public network.

However, range and hence cell sizes for high-speed data transmission will be much smaller than for cellular phones, meaning more cell sites will be needed for wireless transmission of data. The number of cell sites increases as the range decreases, according to a square law. A wireless data infrastructure requires four times as many cells each time the range is reduced by half. The expected range of high-speed data links may be only 1/10th that of digital cellular, requiring 100 times the number of base stations — obviously a costly infrastructure investment.



III. Wireless LAN Usage Today

Wireless LAN usage in the commercial world is in its infancy. Two factors will make wireless data communications commonplace in the work environment:

A. IEEE 802.11 Standard

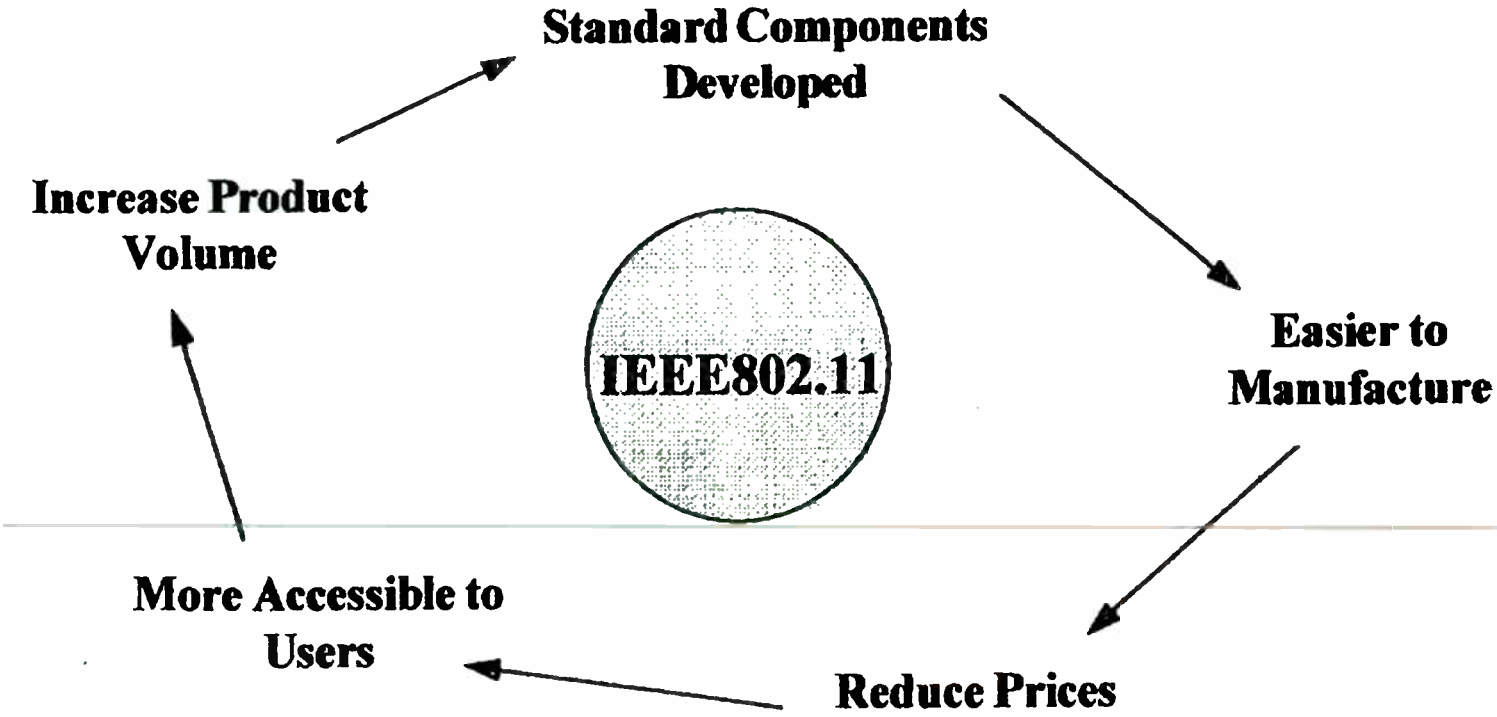
The first factor is the availability of the IEEE 802.11 standard. This standard, under development for several years, is expected to be complete this year. The standard defines the parameters and protocols of wireless LAN systems. These parameters and protocols allow interoperability between systems at speeds up to 2 Mbps. Users can purchase standards-based products from different vendors Furthermore, standards-based products make the decision process easier for users, allowing users to buy products easily and with more confidence.

B. Economic Issues

The second factor in advancing the widespread implementation of wireless LAN technology is the reduction in the cost of the technology. A year ago, a wireless LAN PC card might cost $600-700. This year, the price is expected to drop below $300. At this price, the convenience of the technology is more justifiable.

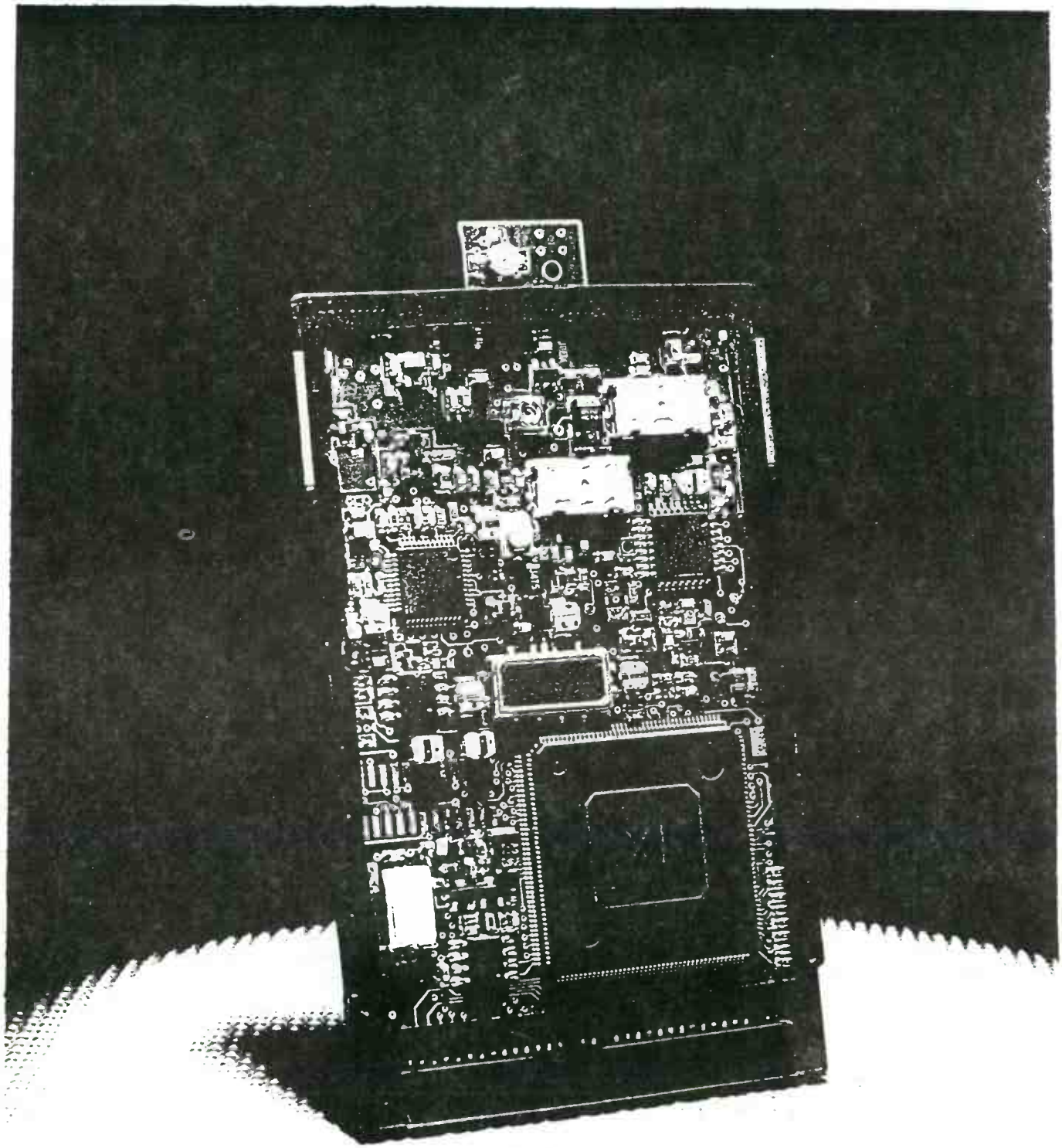
The dramatic price drop stems from the availability of a new silicon bipolar-based radio design pioneered by Symbionics Networks Ltd. and more recently Harris Corp. In addition, large semiconductor companies such as OKI Electric Industry Co. Ltd. and AMD have taken advantage of the emerging standard to make baseband controller chips. Mass production and subsequent availability of such chips reduces the consumers costs.

Indirect Effect of the IEEE 802.11 Standard



With the availability of an industry standard, more companies can enter the market, increasing product diversity and further reducing costs due to competition, fostering extensive implementation of wireless LANs.

Symbionics' PC Card for Wireless LAN Connectivity



IV. How Fast is Fast Enough?

The IEEE 802.11 specification for wireless LANs allows users to transmit data at 2 Mbps with frequency hopping or direct sequence spread spectrum. The specification also calls for back-up operation at 1 Mbps.

While wireless LANs are not — and most likely will not be — fast enough to keep up with wired LANs moving to 100 Mbps, the question becomes, "Why should they?" In the last decade, operating systems and applications have been developed on the assumption that memory and network bandwidth will increase to keep pace with demands. The cost and scale of memory are decreasing while wired network bandwidth is increasing.

However, the capabilities and limitations of emerging wireless communications are raising new questions and concerns. Speed over a wireless link is an expensive commodity because it causes more valuable raw resources in the form of spectrum allocation to be consumed. The amount of spectrum used to accommodate fast speeds cannot be reduced by mere technological advancements.

Meanwhile, the trend toward more mobility and untethered access to information will continue, making greater demands on radio communications. At some point, the priorities of application development must shift to accommodate wireless networks. Under the new scenario, popular applications will be those that make the most efficient use of network bandwidth rather than guzzling megabits on the assumption that there is enough free spectrum to meet the demand.

Even though data rates of 100 Mbps sounds impressive, that kind of speed is not always necessary. With a data rate of 10 Mbps, it is possible to transmit television quality images and sound and to fill a page with text more rapidly than the human eye can read. Therefore, it can be said that the bandwidth of the human senses is limited to about 10 Mbps. Sending 100 Mbps of data to the human interface gains nothing. Since wireless ultimately is about personal communications, 10-20 Mbps is fast enough for human interaction. The technology to deliver this mobility is at hand, but a new paradigm for applications must come with the capability.

V. How Far is Far Enough?

Initially, wireless LAN systems will be limited to use inside an office, where cell ranges of about 200 feet offer comfortable coverage for most environments. But as employees roam farther from the office building, the demand for external wireless LAN coverage will grow. The notion of installing enough base stations to cover all major urban areas with 200-foot wireless LAN cells with 10 Mbps data rates would be too cost prohibitive.

Adjusting the bit range and cell size for different environments will solve some of these dilemmas. In key areas where business applications dominate such as downtown areas, business parks and airports 10 Mbps coverage is feasible to install. In other urban areas where the focus is less business oriented, cell sizes could increase as data rates decrease to 1 Mbps or less.

The concept of continuously variable speed and range has not been implemented, but such an architecture will not be technologically difficult to design. As with many new developments, the barriers are financial and regulatory.

VI. HIPERLAN

Some wireless LAN vendors and users believe the speeds offered by IEEE 802.11 are not sufficient for office applications, especially in view of the accelerating bandwidth of the wired networks — up to 100 Mbps. Using the IEEE 802.11 standard specifications designed for the 2.4 GHz ISM band and require spread spectrum operation, information transmitted at 2 Mbps only has 1 MHz of bandwidth available. Technically, the simplest way to increase bandwidth without reducing range is to allocate more radio spectrum. But because spectrum is so scarce, increased allocation is the most difficult in regulatory terms.

In Europe, the regulatory bodies in charge of spectrum allocation have allocated 100 MHz of spectrum at 5.1 GHz exclusively for wireless LANs. With this amount of spectrum, a standard that will provide a wireless data rate of 24 Mbps already is under development.

This is a demonstration that high speed wireless data communications is possible given enough spectrum. Today the standard is in final public inquiry phase, but unlike IEEE 802.11, no early product developments have been announced.

HIPERLAN not only has high speed operation but also strong built-in support for multimedia services such as video.

VII. HIPERLAN in the United States?

The band used for HIPERLAN in Europe previously was allocated for an international network of microwave landing systems (MLS), the supposedly new generation of automatic aircraft landing systems. However, MLS systems will not be deployed because of technological advances in other navigational systems. This means the dedicated spectrum for MLS is vacant almost worldwide, including in the United States.

The vacant spectrum has drawn new interest from commercial entities. The most notable interest is from Apple Computer. The company petitioned the FCC in May 1995 for the creation of a national information infrastructure (NII) band to allow high speed wireless access to the information superhighway. By the end of the year, no decision was handed down. The petition for unlicensed public use creates an unusual dilemma. The spectrum has a high direct value if auctioned off, but it has a higher indirect value — albeit slower to achieve — if released for unlicensed public use. The indirect value would stem from the increased competitiveness of U.S. companies in developing and marketing technologies, applications and products for a high speed domestic band.

VIII Conclusion

The IEEE 802.11 standard will be the springboard for many new applications for portable computing. The standard will help drive down costs, making the technology more accessible to a wider population. As portable computing becomes more pervasive, people will develop new ways of using the technology and demand more capabilities in terms of speed and range. Furthermore, these demands will be influenced by other emerging technologies.

Still some things about wireless communications will remain constant. Radio spectrum is a valuable, thus well-regulated resource. Radio communications technology is well-established. The greatest remaining task is shrinking the size and cost of this technology so it is a marketable product. And

finally, high speed means less range. That means network providers must sink a considerable investment in building an infrastructure to meet consumer expectations, already established through other existing wireless technologies

And while the IEEE 802.11 standard is the starting point for widespread implementation of wireless LANs, there's room for more evolution. With support for video as well as data, HIPERLAN technology seems to be heir apparent for broader wireless LAN applications. Still the overriding decision in determining how far wireless LANs will go beyond the office building lies with those who will regulate spectrum and those who will build the infrastructure.

ETHERNET COMPATIBLE 24 GHz MMIC WLAN

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Abstract. An Ethernet compatible wireless local area network (WLAN) is being implemented. The design utilizes a transceiver (18 RF functions) that will be integrated on a single GaAs microwave monolithic integrated circuit (MMIC) chip using a 0.18 μm PHEMT process. The chip is being developed under the Advanced Research Program Agency's (ARPA) Dual Use technology reinvestment program (TRP). One of the system cost drivers is the RF transceiver. Northrop Grumman's highly integrated MMIC chip is key to an affordable high speed WLAN. An exhaustive study of medium access control protocols was conducted. Multipath issues were investigated and multi-carrier modulation methods were found to be appropriate for high data rate applications in an office-like environment.

1.0 Introduction

Local Area Networks (LANs) allow multiple computer users to exchange information between other users. With multiple users running multiple applications, the network can easily become loaded to capacity and its data transfer efficiency reduced dramatically. This is increasingly becoming evident as hardware and software capabilities grow, requiring greater amounts of data to complete an application or service. Wired LAN manufacturers addressed this possibility by offering a 100 Mbps wired version of the popular 10 Mbps Ethernet standard. However, the vast majority of wireless LANs offered to date have effective data throughput well below even the 10 Mbps. This paper discusses the design of a millimeter wave frequency Wireless Local Area Network (WLAN), employing a multi-carrier modulation to offer data rates in excess of the 10 Mbps. A multiple access protocol is selected that allows high network efficiency. A WLAN was built and evaluated to demonstrate the feasibility of the technology.

2.0 System Trade-Offs

Our objective was to design an Ethernet compatible WLAN operating at a high data rate (>10 Mbps). The WLAN should support multiple users in an office like environment. To meet these operational requirements, various system parameter trade-offs were investigated including:

- Frequency Band
- RF Channel
- Modulation Schemes
- Multiple Access Protocols
- Antenna Type/Link Budget
- Fixed or Mobile Users
- Cost.

2.1 Frequency Band

For operational reasons one would like to use a compact antenna. Also, for high data rates, a wide RF bandwidth must be utilized. Since our goal was to prove the feasibility of a high data rate WLAN, we employed an FCC unlicensed band. (See Table 1 for a summary of the regulations covering operation in FCC unlicensed bands.) There are many potential interferers in the unlicensed FCC bands. Devices that fall under the category of field disturbance sensors are commonly automatic door openers. Typical industrial, scientific and medical equipment applications are the production of physical, biological, or chemical effects such as heating, ionization of gasses, mechanical vibrations, hair removal, and acceleration of charged particles.

Table 1. FCC Parts 15 and 18 Unlicensed Frequency Band Characteristics [1]

FCC Part	Frequency Bands (MHz)	Radiator Type
15.245	902-928, 2435-2465, 5785-5815, 10500-10550, 24075-24175	Field Disturbance Sensor.
15.247	902-928, 2400-2483.5, 5785-5850	Intentional Radiators.
15.249	902-928, 2400-2483.5, 5725-5875, 24000-24250	Intentional Radiators.
18.301	902-928, 2400-2483.5, 5725-5875, 24000-24250	Industrial, Scientific, Medical (ISM).

We selected the 24 GHz band under Part 15.249. In the lower unlicensed bands (900 MHz, 2400 MHz), there is not sufficient RF bandwidth available to support high data rates. The antenna size in the 24 GHz band is significantly smaller than the 5.8 GHz band. Also, since 250 MHz of RF bandwidth is available in the 24 GHz band, there is growth potential for even higher data rates. The FCC has stated that to the best of its knowledge, (since it is not required to keep records of approved ISM equipment), no commercial ISM equipment exists in this frequency band at present. Therefore, the FCC Part 15.249 24 GHz band has the advantages of unlicensed

operation and suitability for high data rate operation.

2.2 RF Channel

The RF channel in an office-like environment will encounter obstacles in the propagation path, such as metal desks, metal partitions, and metal ceiling light enclosures. Each obstacle will intercept a portion of the transmitted power and reflect or re-radiate the transmitted signal. These multiple transmission paths are referred to as "multipath." The composite signal incident on the receive antenna is a vector sum of all the individual signals. In addition to stationary objects, people and equipment move within the environment in an unpredictable manner. This causes the reflected signals to change with time and space making a deterministic characterization of the RF channel impossible. Thus a statistical model must be used which is derived from many indoor measurements to determine probability distributions of the parameters for the RF channel.

Ideally with no multipath effects, a single impulse launched from the transmit antenna would arrive at the receiver delayed by the arrival time with a change in amplitude and phase. In an actual propagation environment, multiple reflected impulses enter the receiver in addition to the line of sight (LOS) impulse. The "delay spread profile" (amplitude of the individual multipath components as a function of time) characterizes this non-ideal propagation channel. Figure 1 shows a typical delay spread profile for a LOS RF link.

A good measure of a particular multipath delay profile is the RMS delay spread, τ_{rms}. It is defined by:

$$\tau_{rms} = \sqrt{\frac{\sum_k (t_k - \tau_m - t_o)^2}{\sum_k a_k^2}}$$

where t_k is the arrival time of the kth impulse in the profile, t_o is the arrival time of the first impulse in the profile, a_k is the amplitude of the impulses, and τ_m, the mean excess delay defined by:

$$\tau_m = \sqrt{\frac{\sum_k (t_k - t_o)^2 a_k^2}{\sum_k a_k^2}}$$

It has been shown that the performance of a wireless communication system is very sensitive to the value of τ_{rms} [3]. If the value of delay spread is comparable to the symbol length, reduced link performance will result. To recover the data in the presence of the multipath components, adaptive equalizers at the receiver are required to reconstruct the desired signal. The use of an adaptive equalizer is undesirable due to the added system complexity and cost. As a result, *rapid training* in a packet data environment would be difficult.

Since commercial interest in the 24 GHz unlicensed band is only recent, measured delay spread data are not available for the office-like environment in this band. However, measured data are available at 11.5 GHz. Since the delay spread characteristics in the two bands are likely to be similar, it was used to model the 24 GHz propagation channel. Therefore, using the experimental results at 11.5 GHz, the propagation model for the 24 GHz channel was fitted to the data and a channel frequency response generated (as shown in Figure 2). For a fixed receiver in a particular location, the channel frequency response consists of one slice cut in the spatial dimension of the frequency response. The notches in the frequency response will cause distortion of the complex envelope of the transmitted signal, resulting in intersymbol interference.

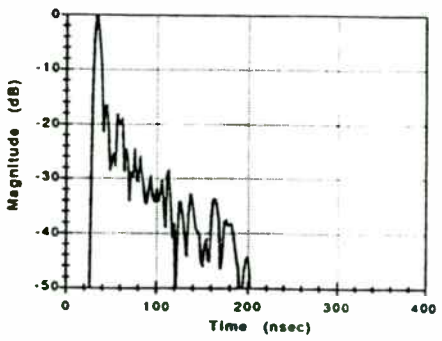

Figure 1. Typical Delay Spread Profile For a LOS (Line of Sight) RF Link [2]

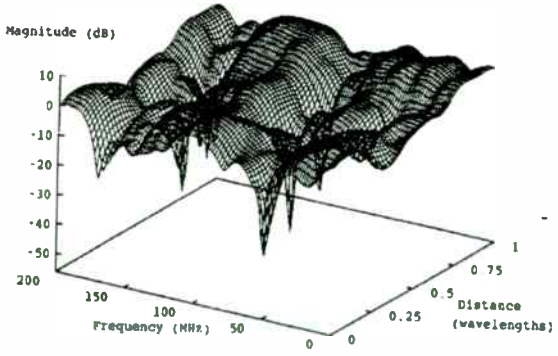

Figure 2. Frequency Response for the Indoor Channel at 24 GHz

2.3 Modulation Schemes

Transmission of data at high rates (>10 Mbps) in a multipath environment requires detailed examination of the modulation scheme trade-offs. We investigated three

modulation schemes from simple to highly complex: linear Quadrature Phase Shift Keying (QPSK), non-linear Gaussian Minimum Shift Keying (GMSK), and multi-carrier Orthogonal Frequency Division Multiplex (OFDM). Simulations were performed using the Comdisco SPW simulator. Simulations of the QPSK and GMSK systems are performed in the time domain whereas OFDM simulations are performed in the frequency domain.

The simulation model for the QPSK system transmitting pseudo random data at a rate of 20 Mbps is shown in Figure 3. The QPSK modulator maps the transmit data into four symbols per bit at a symbol rate of 10 Mbaud. The transmit and receive filters are root raised cosine with 35% excess bandwidth. The QPSK demodulator is assumed to have perfect symbol timing and carrier recovery algorithms. After demodulation, the *eye* is sampled and quantized to +/-1 on each I and Q line. The resultant received data is compared to the transmitted data to determine the bit error rate.

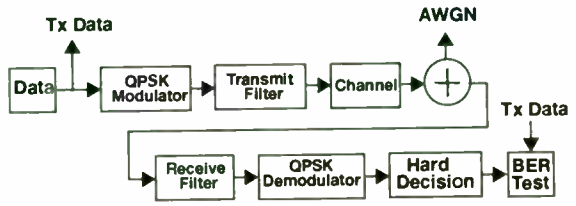

Figure 3. Simulation Model of the QPSK System

The simulation model for the GMSK system (Figure 4) transmits data at 20 Mbps. Since GMSK modulation maps only two symbols per bit, the symbol rate is twice as high, namely 20 Mbaud. The GMSK modulator filters the data with a Gaussian filter with a bandwidth-bit period (BT) product of 0.5. The pre-detection filter is a Butterworth filter of order 4 with a BT product of 1.5. The single-sided noise bandwidth of this filter is approximately equal to its 3-dB cutoff frequency. Limiter-discriminator detection is used with the addition of an integrate and dump (IAD) filter to average out spikes at the discriminator output due to abrupt changes in phase resulting from the interference of multipath components. Perfect symbol timing is assumed, such that the IAD integrates over one complete symbol period.

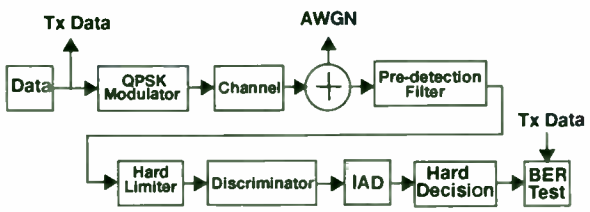

Figure 4. Simulation Model of the GMSK System

The simulation for the OFDM model (Figure 5) is performed in the frequency domain. This is a time-saving measure, as the direct implementation of an OFDM system requires taking the Inverse Fast Fourier Transform (IFFT) of the mapped data, followed by convolving the resulting time domain signal with the channel impulse response, followed by taking the FFT of the received signal. In the frequency domain, it is only necessary to take the FFT of the channel impulse response and multiply the resultant vector, element by element, with vectors of mapped data.

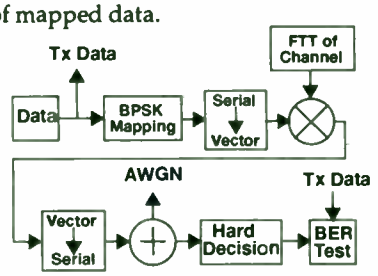

Figure 5. Simulation Model of the OFDM System

The transmitted data is first mapped to a Binary Phase Shift Keying (BPSK) constellation and loaded into vectors of length 155. The channel is sub-divided into 155 sub-channels each carrying a BPSK modulated signal. Each sub-channel has a separation of 200 kHz, and thus the occupied bandwidth of the transmitted signal is 31 MHz. The vectors of the BPSK mapped data are multiplied by the magnitude of the channel frequency response. Since perfect carrier recovery of each sub-carrier is assumed, the phase of the channel frequency response is not used. For a baud period of 5 μs with a 20% guard period totaling 6 μs per block, the symbol rate over the channel is 25.8 Mbaud. Since BPSK modulation bandwidth efficiency is 1 bit/Hz, the OFDM modulator baud rate equals the bit rate, and data transfer is at 25.8 Mbps.

For the ODFM system, a 5 bit Reed-Solomon (RS) code is used which can correct up to 3 RS symbol errors per block length of 155 bits. For the QPSK and GMSK systems, an 8 bit RS code is used which can correct up to 8 RS symbol errors per block length of 528 bits.

Grade-of-Service. The bit error rate of a communication system using coding is a much less important measure of performance than the block, or packet, error rate. A forward error correction (FEC) code can correct a certain number of bits errors within a block. Thus the appropriate measure of performance is the block error rate which is a measure of how often the code could not correct all of the bit errors within a block. A useful metric related to block error rate is grade-of-service (GOS) defined as:

$$GOS\ (\%) = [1 - P] \times 100$$

where P is the ratio of "bad" blocks compared to "good" blocks. A GOS of 100% means that no block errors occur, and a GOS of zero means that the bit error rate is so high that the code cannot correct all of the errors in every block such that every block is in error.

Simulations were run for three different types of RF

channel propagation losses (corresponding to three different locations) in an indoor environment: 1) a typical channel with no "null" in the propagation path, 2) a medium "null" (~ 15 dB) in the propagation path and 3) a deep "null" (>25 dB). The channel frequency response is plotted across a bandwidth of 31 MHz, which is the bandwidth occupied by the OFDM signals (Figure 6). Location 1 is an optimistic expectation of a typical frequency response whereas locations 2 and 3 are more pessimistic.

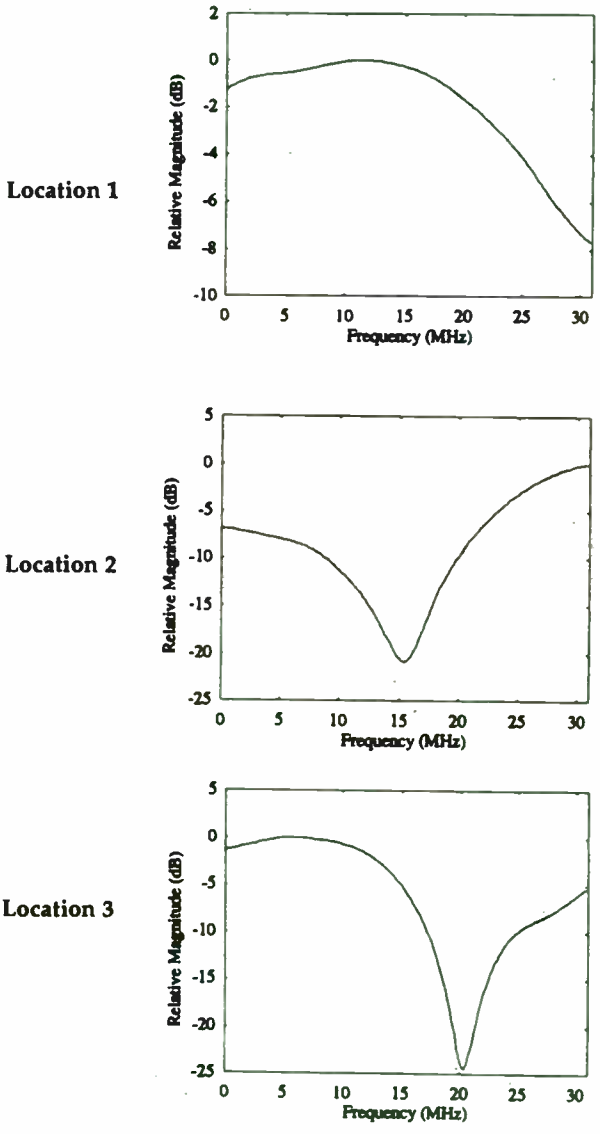

Figure 6. Channel Frequency Response for Three Different Office Locations

The GOS was computed for an appropriate range of energy per bit to thermal noise power (E_b/N_o) for the QPSK, GMSK and OFDM modulation models in the three locations. For GMSK modulation, locations 2 and 3 distorted the received signal to the point of being unusable for data transmission. For QPSK modulation, locations 2 and 3 also yielded an unacceptable grade-of-service. However, for OFDM modulation, a high grade-of-service resulted from an increase in E_b/N_o, independent of the location.

Also, OFDM was found to be effective at combating the effects of delay spread. Even under conditions of deep fades and severe delay spread (locations 2 and 3), an increase in transmission power can reduce the block error rate to an acceptable level. However, increase in transmitted power will increase the system cost. (Also, it may not be feasible to increase the transmitted power due to FCC regulations.) A careful examination of the RF channel model in Figure 2 reveals that considerable spatial decorrelation is available in a single wavelength. As a consequence, a simple antenna diversity scheme would prove beneficial in ensuring a successful link. Coupled with a robust modulation such as OFDM, a highly reliable data link would result.

2.4 Multiple Access Protocols

The operational environment for our WLAN consists of a base (fixed) station and N terminal stations (where N is the number of users and N>1) operating in half-duplex mode. Such a system requires that the base station transmit to all terminal stations on one frequency and then only one of the users (terminal stations) transmits to the base station on that same frequency. The problem is to ensure that only one station transmits at a time on the inbound channel and yet the greatest possible utilization of the channel (commensurate with minimum delay) must be achieved.

A survey of non-deterministic medium access control (MAC) protocols including the ALOHA (pure as well as slotted), the CSMA (Carrier Sense Multiple Access), Ethernet standard protocol CSMA/CD (CSMA with Collision Detect), CSMA/CA (CSMA with Collision Avoidance), the Tree-and-Window Collision Resolution Algorithms (CRA) using control minislots (CMS), and "Reservation System" was performed. It was found that a contention protocol developed at the Illinois Institute of Technology called Distributed Queuing Random Access Protocol (DQRAP) [5] provided the maximum network efficiency when network loading was taken into consideration.

Modeling and simulations indicate that DQRAP using three minislots achieves a performance level that approaches that of a hypothetical perfect scheduling protocol (M/D/1 system) with respect to throughput and delay. The DQRAP would provide immediate access at light loads and then seamlessly move to a "reservation system" at high loads.

2.5 Antenna Type/Link Budget

The physical implementation of the WLAN is heavily influenced by how far the signal will travel and still be received without error. To determine the useful distance between transmitter and receiver, a link budget was developed with the following operational parame-

ters:

- *Receiver Noise Figure:* 6 dB.
- *Data Rate and Signal Bandwidth:* OFDM modulator at 25.8 Mbps data rate (requiring 31 MHz RF bandwidth).
- *Eb/No*: 15 dB to provide an 95% grade-of-service for OFDM modulation.
- *Modem Loss Margin:* 3 dB.
- *Path Loss:* Free space path loss based on line-of-sight transmit and receive antennas.
- *Transmit Power:* 12.6 dBm effective radiated power (ERP) .
- *Transmit Antenna Gain:* Omnidirectional antenna with 2 dBi gain.
- *Receive Antenna Gain:* Omnidirectional antenna with 2 dBi gain or Directional antenna with 17 dBi gain.
- *Shadow Loss:* 8 dB.
- *Co-channel and Adjacent channel Interference:* 6 dB.

Two scenarios were analyzed: a) omnidirectional antennae on both the receive and transmit side of the link and b) an omnidirectional antenna at the transmit side and a directional antenna at the receive side of the link. For case (a), the link would operate up to 39 feet only. For case (b), an operational distance of > 200 feet was calculated. Therefore, to meet the goal of 100 feet operating distance within the maximum permissible transmit power in the 24 GHz unlicensed band, a directional antenna must be used at one end of the link (case b).

2.6 Mobile vs Fixed Users

A WLAN can consist of fixed (terminal station) users, mobile users, or both. In addition, a WLAN that supports mobile users may allow the mobile user to roam between wireless local area networks. A common attribute of mobile users is that the antenna employed is omnidirectional. (An omnidirectional antenna allows the mobile to communicate with the network it is leaving, and listen to the network it is about to enter.) As discussed above (link budget analysis), for an operational WLAN at 24 GHz and high data rate, use of a directional antenna at one end of the link is required. The directional antenna must always be pointed at the other end of the link. In a mobile environment, this cannot always be guaranteed. Therefore, our WLAN design will support a scenario where users must employ terminal stations at fixed locations.

2.7 Cost

The RF transceiver and the OFDM modulator/demodulator (modem) are the two major cost drivers in the 24 GHz high data rate WLAN systems. Cost of the RF transceivers can be lowered by using highly integrated (preferably a single) monolithic microwave integrated circuit (MMIC) chip(s). (See Section 3 for Northrop Grumman's single GaAs MMIC chip details.)

Digital signal processor (DSP) IC chips required to implement the OFDM modems are very expensive at present. However, the cost of the DSP chips is falling at a fast rate (by a factor of two every two years) and will be affordable for WLAN use in very near future.

3. The MMIC WLAN Demonstrator

An Ethernet compatible 24 GHz MMIC-based WLAN at data rates >10 Mbps supporting multiple fixed users at a distance of >100 feet was designed, built and evaluated. (See Figure 7.) To demonstrate the applicability of GaAs MMICs, a 24 GHz transmit and receive module was implemented using discrete MMICs. (An ultimate low cost version will utilize a single 24 GHz transceiver GaAs MMIC chip, as described later.)

The receive chain consists of a MMIC Low Noise Amplifier (LNA), followed by a MMIC amplifier which sets the noise figure of the receiver (< 6 dB). A 6 pole edge-coupled microstrip filter with 3-dB points at approximately 24000 to 24250 MHz limits the image noise incident on the downconverter mixer, and reduces out-of-band spurious. The input signals are downconverted directly to a 140 MHz IF using a MMIC mixer, with built-in LO amplifier. The IF signal is amplified and demodulated by a frequency discriminator.

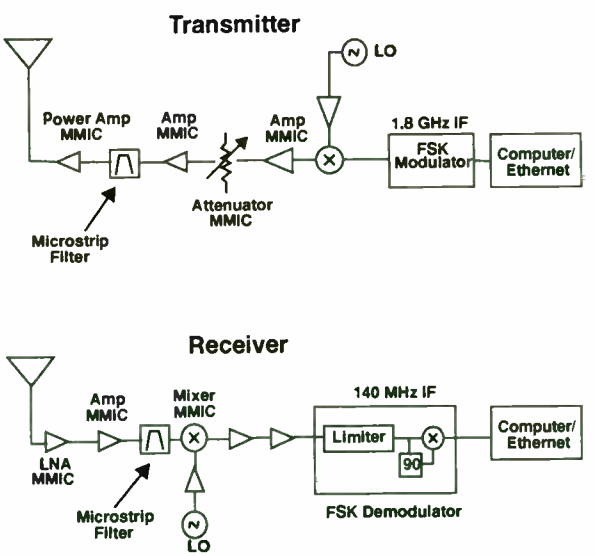

Figure 7. The MMIC Based WLAN Link Demonstrator System

On the transmit side, data packets modulated a carrier at 1.8 GHz. The modulated carrier was upconverted to 24 GHz, preamplified and filtered by a 5-pole edge coupled microstrip filter. A MMIC power amplifier is used to boost the effective radiated output power to +12.6 dBm at the antenna.

A binary Frequency Shift Keying (FSK) modem was substituted for an expensive OFDM modem to implement the modulation and demodulation functions for evaluation of the WLAN link. An OFDM modem would be required to solve a "real" operable scenario whereby an omni-directional antenna would be employed for "base station" and a directional antenna for the "fixed (user) station." This link will perform at low BER with multiple reflection from metal walls and people walking around in the vicinity of the WLAN link. We found that an FSK modem employed under the same conditions but with "directional" antennas at the "base station" and "fixed station," emulated a similar RF link.

The transmitter and receiver were connected to 17 dBi directional antennae. Both antennae were aligned for line-of-sight transmission with no shadow loss or blockage. Ethernet packets were successfully transmitted up to 400 foot distance at 6 Mbps Manchester coded data rate with no errors in data transmitted. (WLAN speed was limited by the bandwidth of the FSK modem .)

The GaAs Transceiver MMIC Chip. A highly integrated single GaAs transceiver MMIC chip (Figure 8) for the 24 GHz band has been designed. It incorporates an LO amplifier with a power divider, a low noise receive chain, a linear transmit chain, and an SPDT transmit-/receive (T/R) switch. It will replace discrete MMICs used in the demonstrator discussed above. Only five external bypass capacitors are required. It contains 18 RF functions and was designed using a 0.18 μm P-HEMT technology which provides low noise and medium power. The chip will provide 14 dBm of transmit power with 18 dB conversion gain in the transmit chain. It has a 5 dB receive noise figure and 20 dB down conversion gain. The transmit and receive chains can be powered independently to conserve power. The T/R switch offers fast switching time and high transmit and receive isolation (>30 dB). The external LO drive required is -5 dBm. The current drain is 320 mA @ 4 V in the transmit mode and 100 mA @ 4 V in the receive mode. The chip size is only 100x150 mils for a total chip area of ~10 mm^2. Use of high density layout techniques maximize chip functionality, provide critical isolation within the chip, and minimize chip size. The chip's small size will provide high-yield and hence lower the system cost.

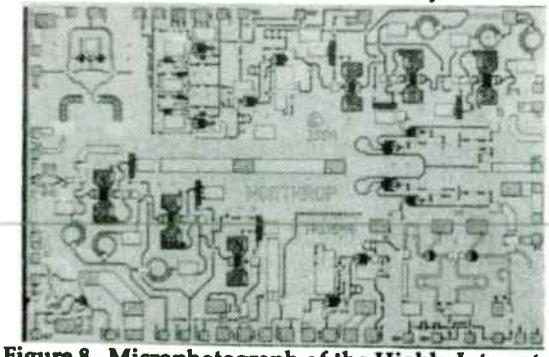

Figure 8. Microphotograph of the Highly Integrated 24 GHz Transceiver GaAs MMIC Chip

4.0 Conclusion

Several technical and practical problems challenge the design of any high-speed wireless network. WLAN system architecture trade studies were performed. Based on these trade-offs, we found the optimum solution to be:

1. *Operate in the unlicensed band.* The 24000-24250 MHz unlicensed FCC Part 15.249 band was chosen because of the lack of interfering sources, wide bandwidth available to support high data rates, future growth potential and unlicensed operation. Also, the antenna sizes are small at these frequencies. Furthermore, WLAN will have small operating cell size due to high propagation losses (at 24 GHz). At first, high propagation loss may appear to hinder the system performance, but it works to the WLAN designer's advantage since it will reduce the interference from adjoining operating cells.

2. *Use multi-carrier complex modulation, such as, orthogonal frequency division multiplex (OFDM).* Computer models were used to determine the best modulation to maintain an acceptable quality of service in the office propagation channel. Results indicated that OFDM modulation will yield a high speed link with minimal errors, even in the presence of severe multipath.

3. *Use directional antennae for users (terminal stations) and an omnidiretional antenna for base station.* To provide reliable data communications over a 100-foot distance and remain FCC compliant, a directional antenna at one end of the link must be employed. Directional antennae are not well suited for mobile scenarios where the user may move from the front lobe to the back lobe of the other user. Consequently the network must consist of fixed users.

4. *Use DQRAP multiple access communication protocol.* A survey of all applicable multiple access protocols was performed and it was determined that Distributed Queuing Random Access Protocol (DQRAP) yielded the greatest throughput and least delay for a wireless LAN system.

5. *Integrate most of the RF functions onto a single multi-function monolithic mirowave integrated circuit (MMIC) GaAs chip to implement an affordable WLAN system.* A significant cost driver is the RF portion of the link. Using packaged discrete devices to implement the transceiver would be cost and size prohibitive. By using a single highly integrated GaAs MMIC chip, a commercially affordable WLAN can be implemented.

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Data Modem/RF Technology for New Wireless PLMR and CDPD Applications

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ABSTRACT[1]

For relatively narrow band FCC part 47 authorized bandwidth including 12.5khz and 25khz as well as for Cellular Digital Packet Data (CDPD), inventions and design led to improved physical layer implementations. In particular for 19.2 kbps data rate in the FCC authorized 25 Khz bandwidth, the implementation of a robust constant envelope modulation technique and non linearly amplified (NLA) mobile link solution was developed by NovaLink USA in joint cooperation with Kb/TEL of Mexico. In this Public Land Mobile Radio (PLMR) system, we implemented FQPSK technology under license of Dr. Feher Associates/Digicom, Inc. The same Feher patented technology is also being developed for new generations of more robust and low cost GMSK based CDPD and other standardized applications.

While previously used GFSK and 4-level digital (4-FM or 4-FSK) system meet the stringiest FCC authorized bandwidth requirements, NovaLink and Kb/TEL developments led to the conclusion that the Feher technology has a 5dB to 10dB radio link budget advantage. This significant advantage leads to a lower BER, higher throughput rate and larger coverage area. Ultimately a higher capacity, better performance and lower cost wireless solution is attained.

[1] For a copy of the complete presentation, please contact NovaLink Technologies, Inc. For technology transfer contact Dr. Feher Digcom, Inc.

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Reliable, 100 kb/s Low-Voltage Powerline Communications

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The AC powerline has long been recognized as a wireless medium offering communications connectivity within a building. Its use, however, until recent developments in semiconductor and communications technologies, has been precluded by the seemingly insurmountable difficulties of receiving data corrupted by powerline noise and attenuation.

Advanced techniques that combine a new spread-spectrum technology and a robust, powerline-specific protocol, enables reliable, high-speed data networking on the electrically-hostile, low-voltage powerline; applications for the new technology include utility Distribution Automation/Demand Side Management (DA/DSM), intraoffice local area networks (LANs), powerline-based telephony, and industrial data networking.

The technology has been implemented as a highly-integrated CMOS chip set, allowing straightforward integration into OEM systems and products.