ONE DOLLAR

FOURTH EDITION

TRANSISTOR MANUAL

CIRCUITS
APPLICATIONS
SPECIFICATIONS

GENERAL ELECTRIC TRANSISTOR MANUAL

fourth edition

CONTRIBUTORS:

E. Gottlieb
F. W. Gutzwiller
D. V. Jones
H. R. Lowry
G. E. Snyder
R. A. Stasior
T. P. Sylvan

APPLICATION ENGINEERING

EDITED BY:

Semiconductor Products Department
Advertising and Sales Promotion
General Electric Company
Charles Building
Liverpool, New York

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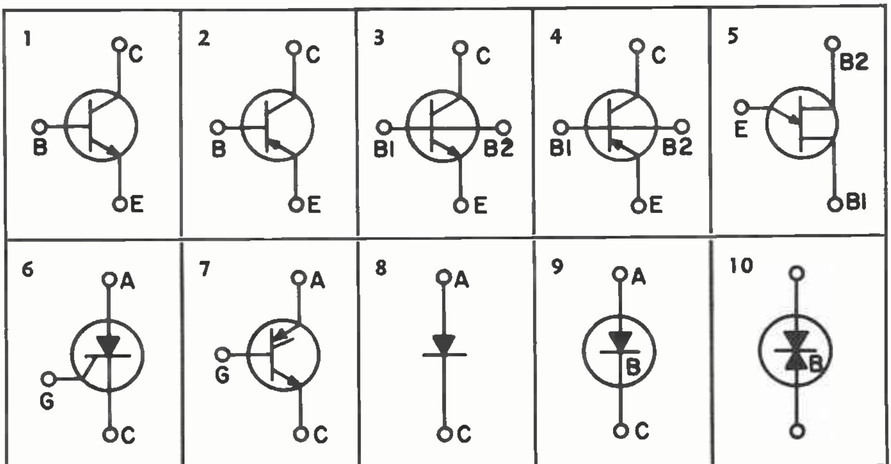
1. BASIC SEMICONDUCTOR THEORY

In the few years since its introduction, the junction transistor has played a steadily increasing part in every branch of electronics. First applied in hearing aids and portable radios, the transistor now sees service in such diverse applications as industrial control systems, digital computers, automatic telephone exchanges, and telemetering transmitters for satellites. The next few years promise an equally spectacular growth since a "second generation" of semiconductor devices is now being introduced which will complement the junction transistor and extend the capabilities of semiconductor electronics. The frequency range of transistors will be extended into the UHF range by such devices as the tetrode transistor and the "mesa" transistor. The power range will be extended by new devices such as the Silicon Controlled Rectifier which will make possible control circuits capable of operating to over 50 amperes, 400 volts, and 20 kilowatts. Devices such as the PNPN diode and the unijunction transistor will make possible simpler and more economical timing and switching circuits. Figure 1.1 lists the names and symbols for most of the semiconductor devices which are commercially available at the present time.



(1) NPN transistor	B = base electrode
(2) PNP transistor	B = breakdown device in (9) and (10)
(3) NPN tetrode transistor	B1 = base-one electrode
(4) PNP tetrode transistor	B2 = base-two electrode
(5) PN unijunction transistor	E = emitter electrode
(6)(7) silicon controlled rectifier (NPNP transistor)	C = collector electrode (symbols 1-5 only)
(8) rectifier or diode	C = cathode electrode (symbols 6-9 only)
(9) zener or breakdown diode	A = anode electrode
(10) symmetrical zener diode	G = gate electrode

STANDARD SYMBOLS FOR SEMICONDUCTOR DEVICES
FIGURE 1.1

A complete understanding of semiconductor physics and the theory of transistor operation is, of course, not necessary for the construction or design of transistor circuits. However, both the electronics engineer and the hobbyist can obtain practical benefits from a general understanding of the basic theory of semiconductors. Such an understanding will often aid in solving special circuit problems and will prove of great assistance in the successful application of the newer semiconductor devices which become available. This chapter is concerned with the terminology and theory of semiconductors as it pertains to rectifiers and junction transistors. The theory and characteristics of other types of semiconductor devices such as the silicon controlled rectifier, the unijunction transistor, and the tetrode transistor are discussed in later chapters of this manual.

The basic materials used in the manufacture of transistors are the *semiconductors* — materials which lie between the metals and the insulators in their ability to conduct electricity. The two semiconductors now being used are germanium and silicon. Both of these materials have four electrons in the outer shell of the atom *(valence electrons)*. Germanium and silicon form crystals in which each atom has four neighboring atoms with which it shares its valence electrons to form four *covalent bonds*. Since all the valence electrons are required to form the covalent bonds there are no electrons free to move in the crystal and the crystal will be a poor electrical conductor. The conductivity can be increased by either heating the crystal or by adding other types of materials *(impurities)* to the crystal when it is formed.

Heating the crystal will cause vibration of the atoms which form the crystal. Occasionally one of the valence electrons will acquire enough energy *(ionization energy)* to break away from its parent atom and move through the crystal. When the parent atom loses an electron it will assume a positive charge equal in magnitude to the charge of the electron. Once an atom has lost an electron it can acquire an electron from one of its neighboring atoms. This neighboring atom may in turn acquire an electron from one of its neighbors. Thus it is evident that each free electron which results from the breaking of a covalent bond will produce an electron deficiency which can move through the crystal as readily as the free electron itself. It is convenient to consider these electron deficiencies as particles which have positive charges and which are called *holes*. Each time an electron is generated by breaking a covalent bond a hole is generated at the same time. This process is known as the *thermal generation* of *hole-electron pairs*. If a hole and a free electron collide, the electron will fill the electron deficiency which the hole represents and both the hole and electron will cease to exist as free charge carriers. This process is known as *recombination*.

The conductivity of a semiconductor material can also be increased by adding impurities to the semiconductor crystal when it is formed. These impurities may either be *donors* such as arsenic which "donate" extra free electrons to the crystal or *acceptors* such as aluminum which "accept" electrons from the crystal and produce free holes. A donor atom, which has five valence electrons, takes the place of a semiconductor atom in the crystal structure. Four of the five valence electrons are used to form covalent bonds with the neighboring semiconductor atoms. The fifth electron is easily freed from the atom and can move through the crystal. The donor atom assumes a positive charge, but remains fixed in the crystal. A semiconductor which contains donor atoms is called an *n-type* semiconductor since conduction occurs by virtue of free electrons (negative charge).

An acceptor atom, which has three valence electrons, can also take the place of a semiconductor atom in the crystal structure. All three of the valence electrons are used to form covalent bonds with the neighboring atoms. The fourth electron which is needed can be acquired from a neighboring atom, thus giving the acceptor atom a negative charge and producing a free hole in the crystal. A semiconductor which contains acceptor atoms is called a *p-type* semiconductor since conduction occurs by virtue of free holes in the crystal (positive charge).

ELEMENT (SYMBOL)	GROUP IN PERIODIC TABLE	NUMBER VALENCE ELECTRONS	APPLICATIONS IN SEMICONDUCTOR DEVICES
boron (B) aluminum (Al) gallium (Ga) indium (In)	III	3	acceptor elements, form p-type semiconductors, each atom substitutes for a Ge or Si atom in the semiconductor crystal and can take on or accept an extra electron thus producing a hole
germanium (Ge) silicon (Si)	IV	4	basic semiconductor materials, used in crystal form with controlled amounts of donor or acceptor impurities
phosphorus (P) arsenic (As) antimony (Sb)	V	5	donor elements, form n-type semiconductors, each atom substitutes for a Ge or Si atom in the semiconductor crystal and can give up or donate an extra electron to the crystal

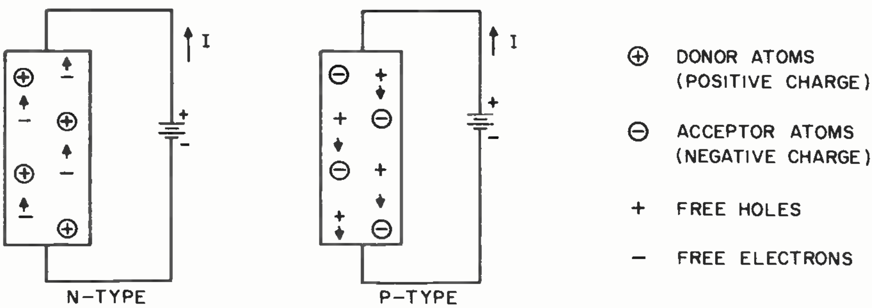
MATERIALS USED IN THE CONSTRUCTION OF TRANSISTORS AND OTHER SEMICONDUCTOR DEVICES

FIGURE 1.2

To summarize, conduction in a semiconductor takes place by means of free holes and free electrons *(carriers)* in the semiconductor crystals. These holes or electrons may originate either from donor or acceptor impurities in the crystal or from the thermal generation of hole-electron pairs. During the manufacture of the crystal, it is possible to control the conductivity and make the crystal either n-type or p-type by adding controlled amounts of donor or acceptor impurities. On the other hand, the thermally generated hole electron pairs cannot be controlled other than by varying the temperature of the crystal.

One of the most important principles involved in the operation of semiconductor devices is the *principle of space charge neutrality.* In simple terms, this principle states that the total number of positive charges (holes plus donor atoms) in any region of a semiconductor must equal the total number of negative charges (electrons plus acceptor atoms) in the same region provided that there are no large differences in voltage within the region. Use of this principle can frequently result in a simpler and more accurate interpretation of the operation of semiconductor devices. For example, in explaining the characteristics of an n-type semiconductor it is usually stated that the function of the donor atoms is to produce free electrons in the crystal. However, using the principle of space charge neutrality it is more accurate to say that the function of the donor atoms is to provide positive charges within the crystal which permit an equal number of free electrons to flow through the crystal.

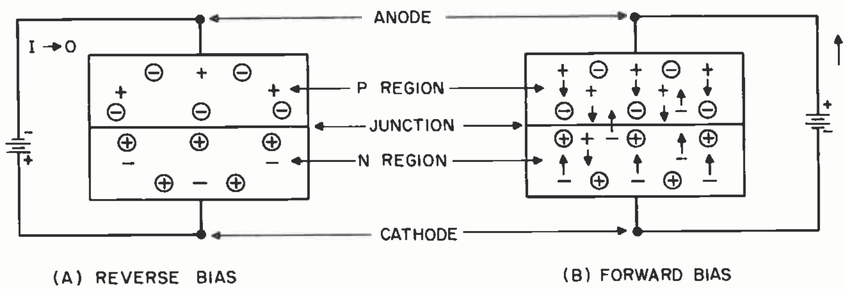
Carriers can move through a semiconductor by two different mechanisms: diffusion or drift. *Diffusion* occurs whenever there is a difference in the concentration of the carriers in any adjacent regions of the crystal. The carriers have a random motion owing to the temperature of the crystal so that carriers will move in a random fashion from one region to another. However, more carriers will move from the region of higher concentration to the region of lower concentration than will move in the opposite direction. *Drift* of carriers occurs whenever there is a difference in voltage between one region of the semiconductor and another. The voltage difference produces a force on the carriers causing the holes to move toward the more negative voltage and the electrons to move toward the more positive voltage. The mechanism of drift is illustrated in Figure 1.3 for both n-type and p-type semiconductors. For the n-type material, the electrons enter the semiconductor at the lower electrode, move upwards through the semiconductor and leave through the upper electrode, passing then through the wire to the positive terminal of the battery. Note that in accordance with the principle of space charge neutrality, the total number of electrons in the semiconductor is determined by the total number of acceptor atoms in the crystal. For the case of the p-type semiconductor, hole-electron pairs are generated at the upper terminal. The electrons flow through the wire to the positive terminal of the battery and the holes move downward through the semiconductor and recombine with electrons at the lower terminal.



CONDUCTION IN N-TYPE AND P-TYPE SEMICONDUCTORS
FIGURE 1.3

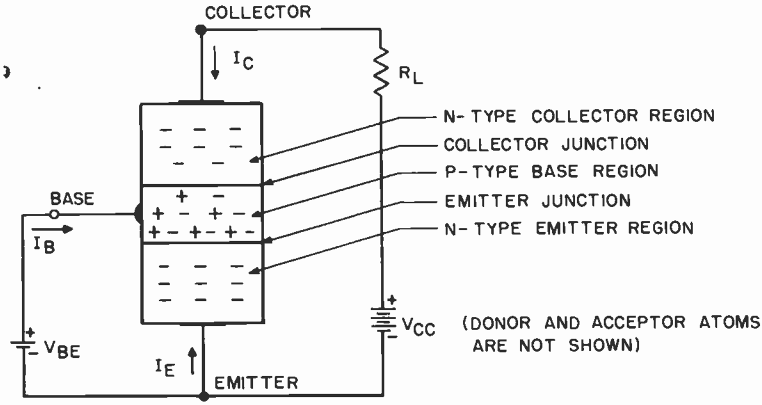
If a p-type region and an n-type region are formed in the same crystal structure, we have a device known as a rectifier or diode. The boundary between the two regions is called a *junction*, the terminal connected to the p-region is called the *anode*, and the terminal connected to the n-region is called the *cathode*. A rectifier is shown in Figure 1.4 for two conditions of applied voltage. In Figure 1.4A the anode is at a negative voltage with respect to the cathode and the rectifier is said to be *reverse biased*. The holes in the p-region are attracted toward the anode terminal (away from the junction) and the electrons in the n-region are attracted toward the cathode terminal (away from the junction). Consequently, no carriers can flow across the junction and no current will flow through the rectifier. Actually a small *leakage current* will flow because of the few hole-electron pairs which are thermally generated in the vicinity of the junction. Note that there is a region near the junction where there are no carriers *(depletion layer).* The charges of the donor and acceptor atoms in the depletion layer generate a voltage which is equal and opposite to the voltage which is applied between the anode and cathode terminals. As the applied voltage is increased, a point will be reached where the electrons crossing the junction (leakage current) can acquire enough energy to produce additional hole-electron pairs on collision with the semiconductor atoms *(avalanche multiplication).* The voltage at which this occurs is called the *avalanche voltage* or *breakdown voltage* of the junction. If the voltage is increased above the breakdown voltage, large currents can flow through the junction and, unless limited by the external circuitry, this current can result in destruction of the rectifier.

In Figure 1.4B the anode of the rectifier is at a positive voltage with respect to the cathode and the rectifier is said to be *forward biased.* In this case, the holes in the p-region will flow across the junction and recombine with electrons in the n-region. Similarly, the electrons in the n-region will flow across the junction and recombine with the holes in the p-region. The net result will be a large current through the rectifier for only a small applied voltage.



CONDUCTION IN A PN JUNCTION RECTIFIER
FIGURE 1.4

An NPN transistor is formed by a thin p-region between two n-regions as indicated in Figure 1.5. The center p-region is called the *base* and in practical transistors is generally less than .001 inch wide. One junction is called the *emitter* junction and the other junction is called the *collector* junction. In most applications the transistor is used in the common emitter configuration as shown in Figure 1.5 where the current through the output or load (R_L) flows between the emitter and collector and the control or input signal (V_{BE}) is applied between the emitter and base. In the normal mode of operation, the collector junction is reverse biased by the supply voltage V_{CC} and the emitter junction is forward biased by the applied base voltage V_{BE}. As in the case of the rectifier, electrons flow across the forward biased emitter junction into the base region. These electrons are said to be emitted or injected by the emitter into the base. They diffuse through the base region and flow across the collector junction and then through the external collector circuit.



CONDUCTION IN A NPN JUNCTION TRANSISTOR
(COMMON EMITTER CONFIGURATION)
FIGURE 1.5

If the principle of space charge neutrality is used in the analysis of the transistor, it is evident that the collector current is controlled by means of the positive charge (hole concentration) in the base region. As the base voltage V_{BE} is increased the positive charge in the base region will be increased, which in turn will permit an equivalent increase in the number of electrons flowing between the emitter and collector across the base region. In an ideal transistor it would only be necessary to allow base current to flow for a short time to establish the desired positive charge. The base circuit could then be opened and the desired collector current would flow indefinitely. The collector current could be stopped by applying a negative voltage to the base and allowing the positive charge to flow out of the base region. In actual transistors, however, this can not be done because of several basic limitations. Some of the holes in the base region will flow across the emitter junction and some will combine with the electrons in the base region. For this reason, it is necessary to supply a current to the base to make up for these losses. The ratio of the collector current to the base current is known as the current gain of the transistor $h_{FE} = I_C/I_B$. For a-c signals the current gain is $\beta = h_{fe} = i_c/i_b$. The ratio of the a-c collector current to a-c emitter current is designated by $\alpha = h_{fb} = i_c/i_e$.

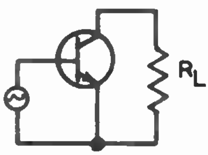
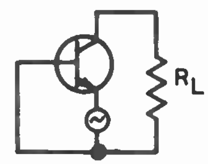
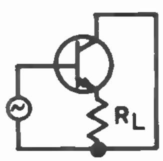
When a transistor is used at higher frequencies, the fundamental limitation is the time it takes for carriers to diffuse across the base region from the emitter to the collector. Obviously, the time can be reduced by decreasing the width of the base region. The frequency capabilities of the transistor are usually expressed in terms of the *alpha cutoff frequency* (f_{ab}). This is defined as the frequency at which α decreases to 0.707 of its low frequency value. The alpha cutoff frequency may be related to the base charge characteristic and the base width by the equations:

$$T_E = \frac{Q_B}{I_E} = \frac{W^2}{2D} = \frac{0.19}{f_{ab}}$$

where T_E is the emitter time constant, Q_B is the base charge required for an emitter current I_E, W is the base width, and D is the diffusion constant which depends on the semiconductor material in the base region.

As evident from Figure 1.5, the NPN transistor has some similarity with the vacuum tube triode. Positive voltage is applied to the collector of the transistor which corresponds to the plate of the tube, electrons are "emitted" by the cathode and are "collected" by the plate of the tube, and the control signal is applied to the base of the transistor which corresponds to the grid of the tube. One important difference between transistors and tubes is that the input impedance of the transistor is generally much lower than that of a tube. It is for this reason that transistors are usually considered as current controlled devices and tubes are usually considered as voltage controlled devices. Another important difference between transistors and tubes is the existence of *complementary* transistors. That is, a PNP transistor will have characteristics similar to a NPN transistor except that in normal operation the polarities of all the voltages and currents will be reversed. This permits many circuits which would not be possible with tubes (since no tube can operate with negative plate voltage). Examples of complementary circuits can be found in other parts of this manual.

The operation of the transistor has been described in terms of the common emitter configuration. The term grounded emitter is frequently used instead of common emitter, but both terms mean only that the emitter is common to both the input circuit and output circuit. It is possible and often advantageous to use transistors in the common base or common collector configuration. The different configurations are shown in Figure 1.6 together with their comparative characteristics in class A amplifiers.

CIRCUIT CONFIGURATION		CHARACTERISTICS*	
COMMON EMITTER (CE)		moderate input impedance moderate output impedance high current gain high voltage gain highest power gain	(1.3 K) (50 K) (35) (—270) (40 db)
COMMON BASE (CB)		lowest input impedance highest output impedance low current gain high voltage gain moderate power gain	(35 Ω) (1 M) (—0.98) (380) (26 db)
COMMON COLLECTOR (CC) (EMITTER FOLLOWER)		highest input impedance lowest output impedance high current gain unity voltage gain lowest power gain	(350 K) (500 Ω) (—36) (1.00) (15 db)

*Numerical values are typical for the 2N525 at audio frequencies with a bias of 5 volts and 1 ma., a load resistance of 10K, and a source (generator) resistance of 1K.

TRANSISTOR CIRCUIT CONFIGURATIONS

FIGURE 1.6

2. TRANSISTOR CONSTRUCTION TECHNIQUES

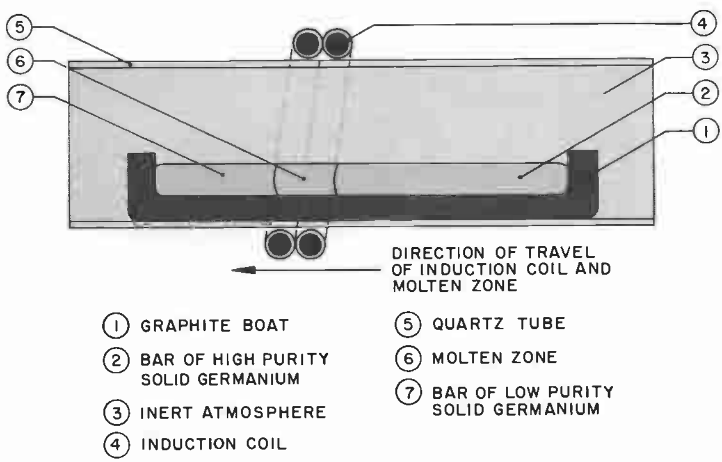
The knowledge of many sciences is required to build transistors. Physicists use the mathematics of atomic physics for design. Metallurgists study semiconductor alloys and crystal characteristics to provide data for the physicist. Chemists contribute in every facet of manufacturing through chemical reactions which etch, clean and stabilize transistor surfaces. Mechanical engineers design intricate machines for precise handling of microminiature parts. Electronic engineers test transistors and develop new uses for them. Statisticians design meaningful life test procedures to determine reliability. Their interpretation of life test and quality control data leads to better manufacturing procedures.

The concerted effort of this sort of group has resulted in many different construction techniques. All these techniques attempt to accomplish the same goal — namely to construct two parallel junctions as close together as possible. Therefore, these techniques have in common the fundamental problems of growing suitable crystals, forming junctions in them, attaching leads to the structure and encapsulating the resulting transistor. The remainder of this chapter discusses these problems and concludes with their bearing on reliability as illustrated by examples.

METAL PREPARATION

Depending on the type of semiconductor device being made, the structure of the semiconductor material varies from highly perfect single crystal to extremely polycrystalline. The theory of transistors and rectifiers, however, is based on the properties of single crystals. Defects in a single crystal produce effects much the same as impurities and are generally undesirable.

Germanium and silicon metal for use in transistor manufacture must be so purified that the impurity concentration ranges from about one part in 10^8 to one part in 10^{11}. Then a dominant impurity concentration is obtained by doping. Finally, the metal must be grown into a single highly perfect crystal.



SIMPLIFIED ZONE REFINING APPARATUS
FIGURE 2.1

The initial purification of germanium and silicon typically involves reactions which produce the chemical compounds germanium and silicon tetrachloride or dioxide. These compounds can be processed to give metallic germanium or silicon of relatively high purity. The metal so prepared is further purified by a process called zone refining. This technique makes use of the fact that many impurities are more soluble when the metal is in its liquid state, thus enabling purification to result by progressive solidification from one end of a bar of metal.

In practical zone refining a narrow molten zone is caused to traverse the length of a bar. A cross-sectional view of a simplified zone refining furnace is shown in Figure 2.1. High purity metal freezes out of the molten zone as the impurities remain in solution. By repeating the process a number of times, the required purity level can be reached. During the process it is important that the metal be protected from the introduction of impurities. This is done by using graphite or quartz parts to hold the metal, and by maintaining an inert atmosphere or vacuum around it. The heating necessary to produce a narrow molten zone is generally accomplished by induction heating, i.e., by coils carrying radio frequency energy and encircling the metal bar in which they generate heat.

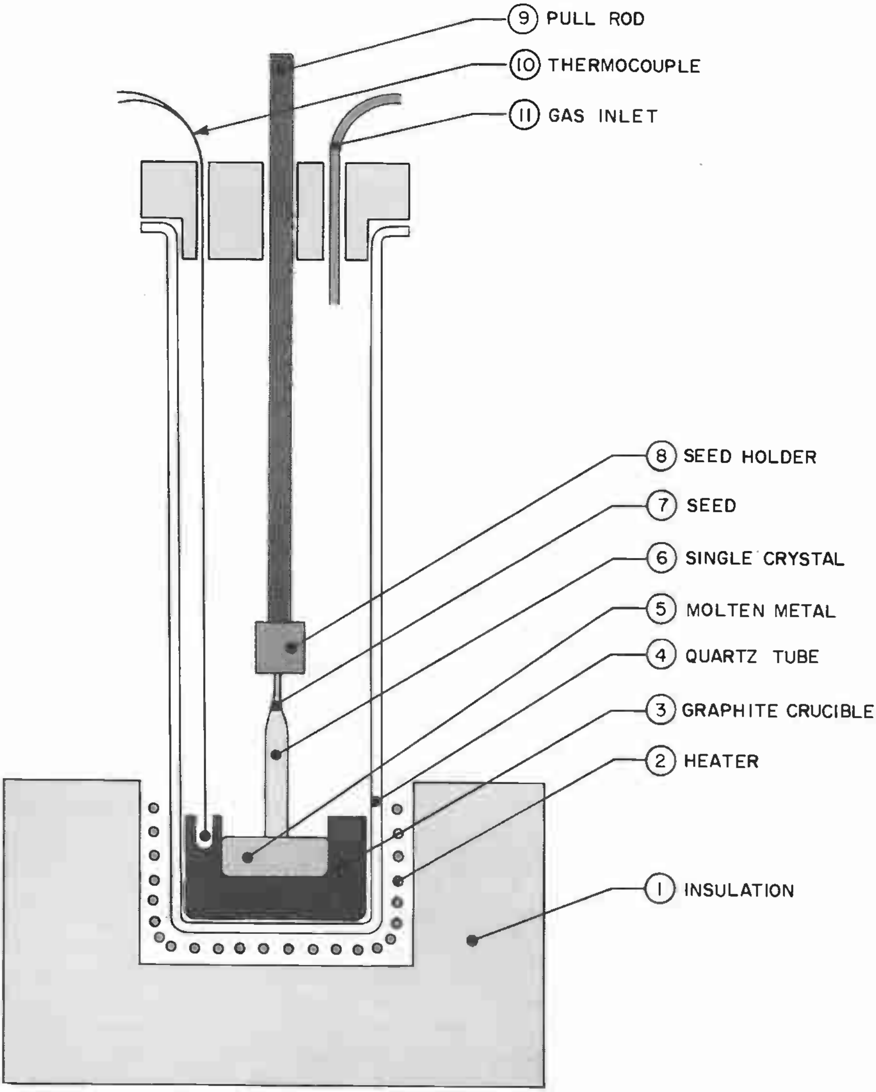
The purified metal is now ready for doping and growing into a single crystal. A common method for growing single crystals is the Czochralski method illustrated in Figure 2.2. In it a crucible maintains molten metal a few degrees above its melting point. A small piece of single crystal called a seed is lowered into the molten metal and then slowly withdrawn. If the temperature conditions are properly maintained a single crystal of the same orientation, i.e., molecular pattern as the seed grows on it until all the metal is grown into the crystal. Doping materials can be added to the molten metal in the crucible to produce appropriate doping. The rate at which doping impurities are transferred from the molten metal to the crystal can be varied by the crystal growing rate, making it possible to grow transistor structures directly into the single crystal. This is discussed in detail in the next section.

The floating zone technique for both refining and growing single crystals has recently been introduced. It is quite similar in principle to zone refining except that the graphite container for the bar is eliminated, reducing the risk of contamination. In place of it, clamps at both ends hold the bar in a vertical position in the quartz tube. The metal in the molten zone is held in place by surface tension. Doping agents added at one end of the bar can be uniformly distributed through the crystal by a single cycle of zone refining. This technique has had much success in producing high quality silicon metal.

JUNCTION FORMATION

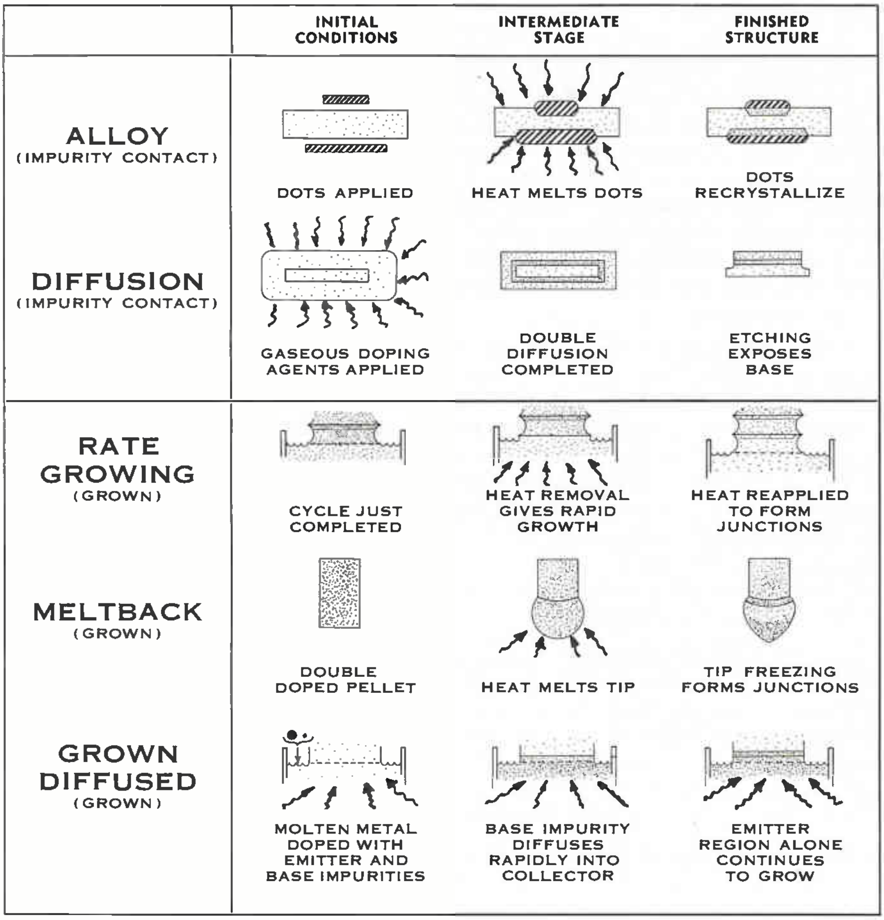
A junction may be defined as the surface separating two parts of a semiconductor with different properties. P-type or N-type doping usually defines the different properties. Transistors generally utilize PN junctions; however, metal to semiconductor junctions are used to manufacture point contact and surface barrier transistors. A transistor can be defined as a structure with two junctions so close together that they interact with one another. For example, the collector junction is close enough to the emitter to collect the current that diffuses into the base region.

Techniques for forming junctions may be subdivided into two basic types, impurity contact or grown junction. The impurity contact method involves treating a homogeneous crystalline wafer with impurities to generate the different properties which form the junction. The grown junction technique involves incorporating into the crystal during its growth the impurities necessary to produce junctions. Alloy transistors, surface barrier transistors, as well as transistors using surface diffusion are examples of



SIMPLIFIED CRYSTAL GROWING FURNACE
FIGURE 2.2

the impurity contact process. Rate grown, meltback and grown diffused transistors are examples of the grown process. These processes, illustrated in Figure 2.3, are discussed below.



IMPURITY CONTACT AND GROWN JUNCTION TECHNIQUES

FIGURE 2.3

The alloy transistor process starts with a wafer of semiconductor material doped to a desired level. Alloying contacts or dots containing impurities are then pressed on either side of the wafer. Heat is applied to the assembly, melting the dots which dissolve some of the wafer, giving an alloy solution. Heat is removed and the solution allowed to freeze. Due to the behavior of impurities during recrystallization, a heavy concentration of donors or acceptors is left at the alloy-semiconductor material boundary. The boundaries are the emitter and collector junctions. The larger dot is the collector. Indium, an acceptor type impurity, when alloyed to antimony doped germanium results in PNP alloy transistors such as the 2N123, 2N396 and 2N525. The final structure of surface barrier and microalloy transistors is similar to that of the alloy transistor. The difference lies in initial etching of the wafer to minimize its thickness followed by plating of the emitter and collector dots. Microalloy transistors melt the dots, generating a recrystallized region which results in normal semiconductor to semiconductor junctions. Surface barrier transistors do not melt the dots and therefore have metal to semiconductor junctions.

In diffusion processes, a wafer of semiconductor material is inserted into a capsule containing one or more impurity elements. The starting material has an impurity concentration suitable for the collector of the transistor. Heat is applied to this system with the result that the impurity elements diffuse into the semiconductor material. If only one impurity element is used, it generates a diffused base region. Subsequently, an emitter region must be added to the structure to form a complete transistor. If two impurity elements are used with germanium wafers, the donor elements will diffuse faster than the acceptor elements and a PNP structure will result. If silicon wafers are used, the acceptor element will diffuse faster than the donor element, resulting in a NPN structure. After the diffusion cycle, proper cutting and etching of the wafer yields transistor structures.

The rate grown process has been applied successfully to germanium yielding transistors such as the 2N78 and 2N167. The molten metal in the crucible contains both donor and acceptor elements. The donor element is sensitive to growth rate so that the amount of this impurity being deposited in the crystal varies as the growing conditions are varied. While a single crystal is being grown from the molten metal, the power is turned off and the crystal is permitted to grow very rapidly. Then excessive power is applied. Growth stops and the crystal starts to remelt. Again the power is turned off. As the metal cools, melting stops and the crystal begins to grow. At the point where the growth rate is zero, the acceptor element predominates and a P region is established across the germanium crystal. Repeating this process, it is possible to grow multiple NPN structures in a single crystal.

In the meltback process, a single crystal doped with both donor and acceptor elements is grown. The crystal is then waferized and diced into small pellets or bars. Each pellet has both donors and acceptors in it. Heat is applied to the tip of the pellet, producing a small drop of molten metal held on by surface tension. Heat is removed and the drop recrystallizes. By taking advantage of the differences in the rate of deposition of the donor and acceptor elements in the drop, a very thin base region is formed. The meltback process yields NPN transistors such as the germanium 2N1289.

The grown diffused process is started by growing a crystal which is doped to the desired collector resistivity. Donor and acceptor elements are added to the molten metal at the same time. Growth continues, but the concentration of impurities has vastly increased. During the growing period, advantage is taken of the different diffusion rates of donor and acceptor elements. In silicon the more rapid acceptors generate diffused base NPN transistors such as the 2N335 and 2N338.

Figure 2.4 lists some of the attributes of junction formation processes. It is seen that the grown processes yield bar shaped transistor structures. Also, all but the now obsolete double-doped process give accelerating base fields to enhance high frequency performance. The rate grown process alone gives more than one wafer from each crystal. Grown diffused and double-doped processes give one wafer per crystal while the meltback process requires melting of each individual bar. Among the limitations of the grown processes is the fact that complimentary types generally are not possible. Also, the bar structure is relatively difficult to heatsink. However, the introduction of the fixed bed construction has resulted in thermal impedances lower than those of many alloy transistors.

Transistors utilizing a surface diffused region have a flat collector surface facilitating heatsink attachment. Because theoretically diffusion can be applied in a variety of ways, great design flexibility is possible. Practically, however, process complexity has limited the number of types being made.

Alloy and microalloy transistors yield two-sided structures which most nearly approximate ideal switches in DC characteristics. Both types have been combined with diffused bases to enhance high frequency performance.

It is seen that many of the structures give similar resistivity profiles and therefore are capable of similar results. For example, both meltback and microalloy diffused transistors have a sharp emitter to base emitter junction, an accelerating field in the base and a low resistivity collector. This results in excellent high frequency characteristics while maintaining relatively high voltage ratings and a moderate saturation resistance. Comparing these with the grown diffused transistor, the latter has the same abrupt emitter junction and graded base resistivity for good high frequency performance, but it does not have a low saturation resistance. Therefore, it is best suited for amplifier applications. On the other hand, the combination of grown diffused bars and fixed bed construction has led to respectable NPN silicon switching transistors such as the G-E 2N338.

The diffused alloy and alloy diffused structures differ in that the former is essentially a conventional alloy transistor with the addition of a diffused base region on the emitter side. The alloy diffused structure, however, has a wafer doped to the required collector resistivity and generates the base region by diffusion out of the emitter dot which has initially been doped with both donor and acceptor impurities.

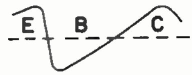
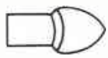
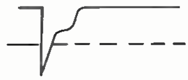
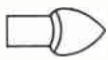
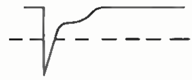
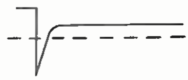
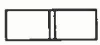
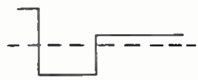
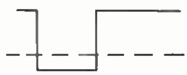
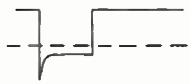
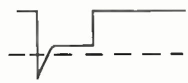
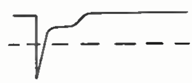
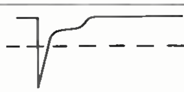
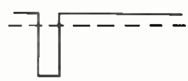
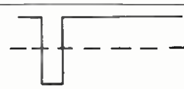
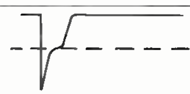
The diffused base and diffused emitter-and-base structures have the same profiles. However, the former has the emitter junction formed by microalloying a semiconductor junction onto the surface of the base; the latter has the emitter already formed by diffusion.

Generally uniformity in transistor characteristics is attributed to processes capable of forming a large number of transistor structures simultaneously, but this uniformity can only be exploited if there is corresponding uniformity in pellet mounting and lead attachment.

LEAD ATTACHMENT

Both ohmic and semiconductor type contacts are required for attaching leads to a transistor structure. Ohmic contacts, i.e., normal non-rectifying contacts, are used to attach leads to exposed regions such as the emitter and collector dots of an alloy transistor or the emitter and collector portions of grown transistor bars. The connection between the mounting base or header leads, and the leads from the transistor structure should also be ohmic. Unless care is taken, leads may form additional PN junctions. If the PN junction is in the collector a PNPN structure results. The same structure is found in the Silicon Controlled Rectifier and therefore it may cause the transistor to turn on regeneratively either at high temperatures or at high collector currents. If the PN junction is in the base lead, it results in a higher base to emitter input voltage, which is a strong function of temperature. This additional junction also affects the base turn off drive in switching circuits and will increase storage time and fall time beyond that of a normal transistor.

On the other hand, semiconductor contacts, i.e., PN junctions, can be useful. They make possible contact with the base region when overlapping the emitter or collector region by the base lead is unavoidable. Grown transistors have extremely narrow base regions so that rugged base leads generally overlap adjacent regions. By doping the base lead heavily with the same impurity as the base, an ohmic type contact is formed

PROCESS DESIGNATION	GEOMETRICAL SHAPE B = Bar D = Double Sided Wafer S = Single Sided Wafer	CROSS-SECTIONAL VIEW SHOWING JUNCTIONS (Not to scale)	RESISTIVITY* PROFILE (Horizontal line is intrinsic resistivity and separates regions. Emitter always on the left.)
RATE GROWN	B		
MELTBACK	B		
MELTBACK — DIFFUSED	B		
GROWN DIFFUSED	B		
DOUBLE DOPED	B		
ALLOY	D		
DIFFUSED ALLOY (DRIFT)	D		 †
ALLOY DIFFUSED	S		 †
DIFFUSED BASE (MESA)	S		
DIFFUSED EMITTER-BASE (MESA)	S		
SURFACE BARRIER	D		
MICRO ALLOY	D		
MICRO ALLOY DIFFUSED	D		

*Profiles are typical and not necessarily to the same scale since processing details can alter profiles considerably.

†Diffused alloy and alloy diffused are capable of identical profiles.

ACCELERATING BASE FIELD	TYPES THEORETICALLY POSSIBLE (Bracketed Types Unavailable Commercially)		NUMBER OF STRUCTURES FORMED SIMULTANEOUSLY	REPRESENTATIVE TRANSISTOR TYPES
	GERMANIUM	SILICON		
YES	NPN	—	MULTIPLE	2N167
YES	NPN	(NPN) (PNP)	INDIVIDUAL	2N1289
YES	PNP	NPN	INDIVIDUAL	—
YES	PNP	NPN	MULTIPLE	2N335
NO	(NPN) (PNP)	NPN (PNP)	MULTIPLE	903
NO	PNP NPN	PNP NPN	INDIVIDUAL	2N525
YES	PNP (NPN)	(PNP) (NPN)	INDIVIDUAL	2N247
YES	PNP	(NPN)	INDIVIDUAL	—
YES	PNP (NPN)	(PNP) (NPN)	MULTIPLE	2N695
YES	(PNP) (NPN)	PNP NPN	MULTIPLE	—
NO	PNP (NPN)	(PNP) (NPN)	INDIVIDUAL	2N344
NO	PNP (NPN)	PNP (NPN)	INDIVIDUAL	2N393
YES	PNP (NPN)	NPN (PNP)	INDIVIDUAL	2N501

JUNCTION PROCESSES AND CHARACTERISTICS FIGURE 2.4

to the base region while semiconductor contacts are simultaneously made to the emitter and collector. With normal transistor biasing, the collector to base PN junction so formed is normally reverse biased. Its primary effect is to increase the collector capacitance. The emitter junction, however, is forward biased, permitting a portion of the base current to be shunted through the overlap diode rather than to be injected into the base region. However, emitter overlap can be completely eliminated by electrolytic etching as in the 2N1289. Mesa-like transistors can also use advantageously heavily doped base leads to permit deep penetration of the base region.

Many materials are suitable for leads, especially if they are doped appropriately. Aluminum, gold, indium, nickel have been used successfully. Gold, which is readily doped P or N-type, is used successfully with both germanium and silicon.

Leads of circular and rectangular cross sections are common. Circular leads offer ease of handling; rectangular, offer a lower base resistance. With rate grown transistors, a circular lead is placed along the full length of the base region to combine the low base resistance of a ribbon contact with the advantages of the circular cross-section.

Alloying, soldering, welding and thermo compression bonding (TCB) are used for attaching leads to header terminals and to the transistor structure. Gold and aluminum are alloyed with germanium and silicon. In some cases, fluxless soldering is the preferred method, for example, in attaching leads to the indium dots on PNP alloy transistors. Welding finds an application primarily in attaching leads to the header terminals. Thermo compression bonding (TCB), which forms contacts by crushing the leads into the transistor structure at elevated temperatures, is of interest since it permits the very shallow surface penetration by the leads which is essential in extremely high frequency transistors. TCB also minimizes potential damage to the junctions because the leads are attached at relatively low temperatures. Close process control is necessary, however, since a precise balance between plastic and elastic deformation must be held to prevent contact failure during thermal cycling.

ENCAPSULATION

The term encapsulation is used here to describe the processing from the completion of the transistor structure to the final sealed unit. The primary purpose of encapsulation is to ensure reliability. This is accomplished by protecting the transistor from mechanical damage and providing a seal against harmful impurities. Encapsulation also governs thermal ratings and the stability of electrical characteristics.

The transistor structure is prepared for encapsulation by etching to dissolve the surface metal which may have acquired impurities during manufacture. Following etching, a controlled atmosphere prevents subsequent surface contamination. The transistor now is raised to a high temperature, is evacuated to eliminate moisture and is refilled with a controlled atmosphere. Then the cap, into which a getter may be placed, is welded on.

In some respects the design of the case, through its contribution to transistor reliability, is as important as that of the transistor structure. Mechanically, users expect to drop transistors, snap them into clips or bend their leads without any damage. Thermally, users expect the header lead seals to withstand the thermal shock of soldering, the junctions to be unaffected by heating during soldering, and the internal contacts to be unchanged by thermal cycling. Considerable design skill and manufacturing cost is necessary to meet the users expectations. Within the transistor structure, coefficients of expansion are matched to prevent strain during thermal cycling. Kovar lead seals withstand the shock of soldering and do not fatigue and lose their effectiveness after thermal cycling. Hard solders and welds maintain constant thermal impedance with time, avoiding possible crystallization of soft solders.

For the stability of electrical characteristics, hermetic seals cannot be overemphasized. They not only preserve the carefully controlled environment in which the transistor is sealed but they exclude moisture which causes instability. While some transistors can tolerate pure water vapor, water makes possible the ionization and migration of other harmful contaminants. Moisture can be responsible for slow reversible drifts in electrical characteristics as operating conditions are changed. Also, while a transistor is warming up after exposure to low temperatures, moisture may precipitate on the transistor surfaces, causing a large temporary increase in I_{CO}. Kovar-hard glass lead seals are used in transistors designed for reliability. Kovar does not have the low thermal impedance or ductility of copper, however, and therefore seal integrity is paid for by a lower dissipation rating and a lower tolerance to lead bending.

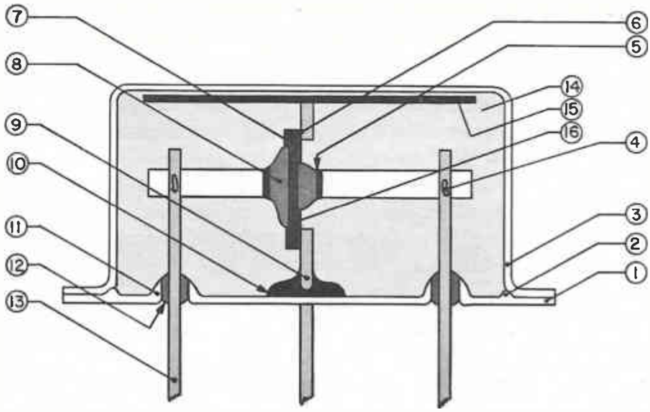
The case design governs the transistor's thermal impedance, which should be as low as possible and consistent from unit to unit. Very small cases minimize the junction to case impedance while increasing the case to air impedance. Larger cases such as the JEDEC 370 mil TO-9 combine a lower case to air impedance, with a lead configuration and indexing tab permitting automatic insertion of transistors into printed circuit boards.

RELIABILITY

Transistors have no known failure mechanism which should limit their life expectancy. Sufficient data has been collected to date to show that with careful construction techniques, transistors are capable of operation in excess of 30,000 hours at maximum ratings without appreciable degradation. Since transistors can perform logical operations at very low dissipation and amplify at high efficiency, the resulting low dissipation reduces the ambient temperature for other components, enhancing their reliability as well. The transistor's small physical size and its sensitivity to small voltage changes at the base, results in low circuit capacitances and low power requirements, permitting large safety factors in design. The variety of manufacturing processes being used by the industry permits choosing the optimum transistor for any circuit requirement. For example, rate grown transistors offer low I_{CO} and low C_C for applications requiring low collector current. Alloy transistors offer high peak power capabilities, great versatility in application, and are available in both PNP and NPN types. Meltback or mesa transistors give high speed at high voltage ratings while microalloy transistors give high speed and good saturation characteristics in lieu of high voltages.

Reliability is a measure of how well a device or a system satisfies a set of electrical requirements for a given period of time under a specified set of operating conditions. Because reliability involves the element of time, only life tests can provide data on reliability. Life tests, however, indicate what the transistor was and how much it has changed during the life test, but they are only a measure of reliability if correlations have been established between the deterioration during life tests and reliability. Life tests alone are inadequate in guaranteeing reliability because they cannot check all potential causes of failure. For example, they will not detect intermittent contacts or the excessive moisture which may cause erratic low temperature performance. Fortunately, other tests detect such conditions, but these problems have led to the adage that reliability cannot be tested in.

While it is true that reliability must be built in, it has seldom proved practical in the past to make an absolute measurement of a specific transistor's reliability. Transistors currently are sufficiently reliable that huge samples and considerable expense in manpower, equipment, and inventory are necessary to get a true measure of their reliability. However, tests can readily show if a transistor falls far short of the required reliability; therefore, they are useful in assigning ratings, in obtaining rate of degradation measurements, and as a measure of quality control or process variability. Figures 2.5, 2.6, 2.7 show some of the considerations in designing reliable transistors.



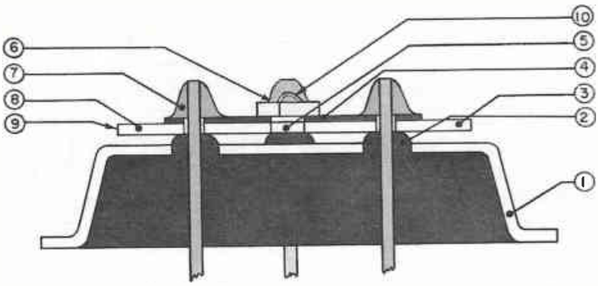
1. KOVAR METAL FOR BEST HERMETIC SEAL
2. RIDGE ASSURES BETTER PRECISION IN WELDING
3. COPPER CLAD STEEL FOR STRAIN FREE FABRICATION, SALT SPRAY RESISTANCE AND MECHANICAL STRENGTH
4. WELDED CONTACTS BETWEEN COLLECTOR AND EMITTER TABS, AND HEADER LEADS
5. SPECIAL ALLOYS AND PROCESSING TO PREVENT POOR WETTING AND CONSEQUENT INTERMITTENT CONTACT
6. SPECIAL ALLOYS BETWEEN WAFER AND SUPPORTING WINDOW TO CONTROL STRESSES DUE TO THERMAL EXPANSION, TO GET GOOD WETTING BETWEEN WINDOW AND WAFER REDUCING THERMAL IMPEDANCE AND SERIES BASE RESISTANCE, TO GET PURELY OHMIC CONTACT
7. CRYSTAL ORIENTATION CHOSEN TO PREVENT DOT SPREADING
8. COLLECTOR DOT CENTERED EXACTLY OPPOSITE EMITTER DOT FOR HIGH CURRENT GAIN
9. THICK WINDOW TO MINIMIZE THERMAL IMPEDANCE TO CASE
10. TWO LARGE WELDS PROVIDE HEAT PATH FROM WINDOW TO CASE
11. SHOULDER ON SEAL FOR STRENGTH
12. KOVAR TO HARD GLASS MATCHED COEFFICIENT SEAL
13. KOVAR LEADS HELP REDUCE JUNCTION HEATING DURING SOLDERING
14. GASEOUS ATMOSPHERE AVOIDS THE MIGRATION OF IONS POSSIBLE WITH FLUID TYPE FILLERS
15. GETTER TABLET TO PERMANENTLY ABSORB ANY MOISTURE DUE TO OUTGASSING
16. SPECIAL ETCHING AND SURFACE TREATMENT RESULTS IN STABLE I_{co} AT ALL TEMPERATURES, VERY LOW NOISE FIGURE, AND SMALL I_{co} VARIATION WITH COLLECTOR VOLTAGE.

DESIGN FOR RELIABILITY
(TYPES 2N43, 2N396, 2N525)
FIGURE 2.5

While a transistor's design must be inherently reliable to yield a reliable product, the design must be coupled with vigorous quality control in manufacturing and accelerated life tests to verify that the process is truly under control.

There are a number of tests which appear to correlate with reliability; however, their significance and applicability to any specific transistor type will vary and must be assessed on this basis.

Storage of transistors at their maximum rated temperature can be a measure of process cleanliness, since chemical activity doubles approximately every ten degrees centigrade. Caution should be used since some organic fillers decompose if the rated temperature is exceeded.



(1) KOVAR METAL HEADER FOR BEST HERMETIC SEAL

(2) RAISED GLASS BEAD TO PREVENT POSSIBLE OCCLUSION OF CONTAMINANTS

(3) CERAMIC DISK WITH COEFFICIENT OF THERMAL EXPANSION MATCHING THAT OF SILICON

(4) GOLD STRIPS BONDED TO CERAMIC BY TECHNIQUES PERFECTED FOR CERAMIC TUBE

(5) SLIT IN DISK CUT TO ±0.001" TOLERANCE

(6) BASE REGION PLACED CLOSE TO COLLECTOR CONTACT FOR LOW THERMAL IMPEDANCE AND LOW SATURATION RESISTANCE

(7) HARD SOLDER PREVENTS THERMAL FATIQUE PROBLEMS

(8) SPECIAL NON-POROUS CERAMIC IS IMPERVIOUS TO PROCESSING CHEMICALS

(9) DISK DIAMETER SMALL ENOUGH TO PREVENT ANY CONTACT WITH CASE

(10) BASE LEAD ATTACHED TO GOLD STRIP

FIXED BED MOUNTING
DESIGN FOR RELIABILITY
(TYPES 2N335, 2N337, 2N491)
FIGURE 2.6

When operating transistors under dissipation, it is preferable to turn the transistors off for approximately ten minutes every hour in order to induce thermal cycling. Thermal cycling will tend to fatigue compression seals, will detect intermittent contacts or poor welds and, by establishing thermal gradients, will accelerate migration of any impurities that may be present.

Some transistors find operation at high voltages and high junction temperatures simultaneously most deleterious. Thermal runaway can be avoided without invalidating the test by applying a collector to base potential and disconnecting the emitter.

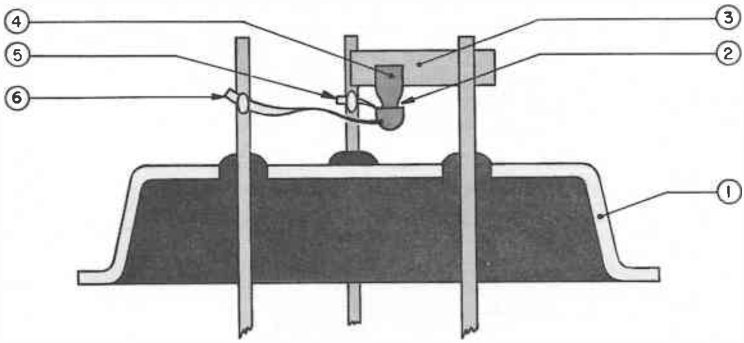
To determine the safety factor in the manufacturer's dissipation rating, life tests at 20% over-rating should detect marginal units. Caution should be exercised with transistors using organic fillers such as greases or oils, since the cases may rupture if the transistors overheat.

With some transistors, a drift in I_{CO} at room temperature is believed to correlate with reliability. In germanium transistors, a drift of more than 1 μa in 15 seconds after power is applied is considered excessive where reliability is of paramount importance.

A transistor may pass the high temperature tests readily even though it will malfunction at low temperatures due to moisture. Moisture can be detected by monitoring I_{CO} while a transistor warms up after being cooled to dry ice temperatures. A significant increase in I_{CO} while the transistor is warming up is indicative of moisture. Care should be taken, however, that vapor condensation on the outside of the transistor case is not responsible for the increase in I_{CO}. Two tests of hermetic seal which are widely used in the industry are the detergent pressure bomb and the Radiflo test. The former involves pressurizing transistors in water to which a small quantity of detergent has been added. On penetrating leaky seals, the detergent contaminates the junctions. To be significant, the test should use a relatively high pressure for a long period of time, particularly if organic fillers are used which might protect the junction temporarily. The Radiflo test forces a gas with a radioactive tracer into the transistor through leaky seals. A Geiger counter detects the presence of the radioactive gas within the leaky transistors.

Another measure of potential reliability are the distribution curves of the major parameters. Except where screening has been done to narrow limits, the distribution curves should be approximately Gaussian, indicating that the transistors represent good process control and statistically will ensure non-critical circuit performance.

The above tests can be made more significant by selecting the samples from several sources over a period of time. This permits a realistic appraisal of the manufacturing process control.



(1) KOVAR HEADER RESEMBLES THAT FOR 2N335
(2) STEP ETCH REVEALS BASE REGION PREVENTING EMITTER OVERLAP
(3) THE HEAT SINK IS A METAL TAB WELDED TO THE HEADER LEAD AND ALLOYED TO THE EMITTER OF MELTBACK BAR
(4) CANTILEVER CONSTRUCTION MINIMIZES MECHANICAL AND THERMAL STRAINS ON BAR
(5) GOLD RIBBON BASE LEAD FOR DUCTILITY, LOW ELECTRICAL RESISTANCE AND LINE CONTACT TO BASE REGION
(6) COLLECTOR LEAD

DESIGN FOR RELIABILITY
(TYPES 2N1289, 3N36, 3N37)
FIGURE 2.7

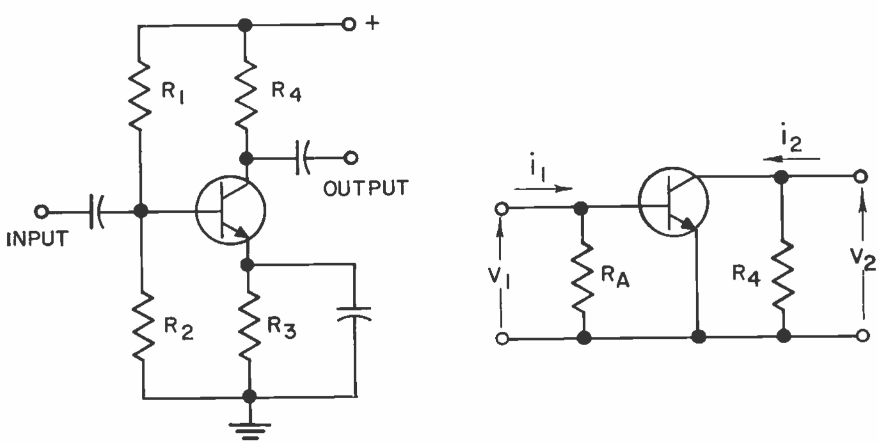
3. SMALL SIGNAL CHARACTERISTICS

A major area of transistor applications is in various types of low level a-c amplifiers. One example is a phonograph preamplifier where the output of a phonograph pickup (generally about 8 millivolts) is amplified to a level suitable for driving a power amplifier (generally 1 volt or more). Other examples of low level or small signal amplifiers include the IF and RF stages of radio and TV receivers and preamplifiers for servo systems.

As described in Chapter 4 on large signal characteristics a transistor can have very nonlinear characteristics when used at low current and voltage levels. For example, if conduction is to take place in an NPN transistor the base must be positive with respect to the emitter. Thus, if an a-c signal were applied to the base of an NPN transistor, conduction would take place only during the positive half cycle of the applied signal and the amplified signal would be highly distorted. To make possible linear or undistorted amplification of small signals, fixed d-c currents and voltages are applied to the transistor simultaneously with the a-c signal. This is called biasing the transistor, and the d-c collector current and d-c collector to emitter voltage are referred to as the bias conditions.

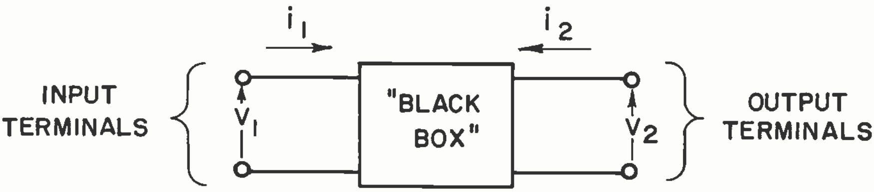
The bias conditions are chosen so that the largest a-c signal to be amplified is small compared to the d-c bias current and voltage. Transistors used in small signal amplifiers are normally biased at currents between 0.5 and 10 ma. and voltages between 2 and 10 volts. Bias currents and voltages below this range can cause problems of distortion, while bias currents and voltages above this range can cause problems of excessive noise and power dissipation.

A typical circuit for a single stage low level a-c amplifier is shown in Figure 3.1. Resistors R_1, R_2, and R_3 form the biasing circuit, the design of which is described in Chapter 5. The capacitors serve to block the d-c voltages, but offer a low impedance path to the a-c signal voltages. Thus, as far as the a-c signals are concerned, the circuit of Figure 3.1 is equivalent to the much simpler circuit of Figure 3.2. Resistor R_A represents the parallel resistance of R_1 and R_2, while v and i designate the values of the a-c voltage and current.



TYPICAL LOW LEVEL A-C AMPLIFIER CIRCUIT AND A-C EQUIVALENT CIRCUIT
FIGURES 3.1 AND 3.2

For the purpose of circuit design any amplifier, whether a single transistor stage or a complete circuit, can be considered as a "black box" which has two input terminals and two output terminals as indicated in Figure 3.3. The circuit designer, knowing the electrical characteristics of the "black box", can calculate the performance of the amplifier when various signal sources are applied to its input and various loads are connected to its output.



BLACK BOX REPRESENTATION OF AN AMPLIFIER CIRCUIT
FIGURE 3.3

Network theory tells us that the complete electrical characteristics of a "black box" such as Figure 3.3 can be specified in terms of four parameters. The parameters which are frequently used for specifying the characteristics of transistors and in the analysis of transistor circuits are the "hybrid" or "h" parameters. The "h" parameters are defined by the equations:

$$v_1 = h_{11}i_1 + h_{12}v_2 = h_i\, i_1 + h_r\, v_2 \qquad (1)$$

$$i_2 = h_{21}i_1 + h_{22}v_2 = h_f\, i_1 + h_o\, v_2 \qquad (2)$$

where

$h_{11} \equiv h_i$ is the input impedance with the output a-c short circuited (ohms)

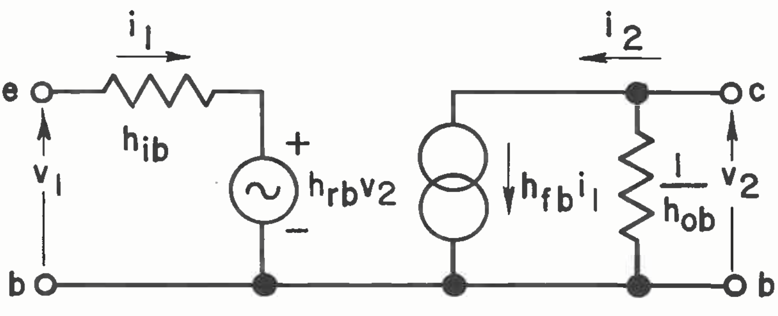
$h_{12} \equiv h_r$ is the reverse voltage transfer ratio with the input a-c open circuited (dimensionless)

$h_{21} \equiv h_f$ is the forward current transfer ratio with the output a-c short circuited (dimensionless)

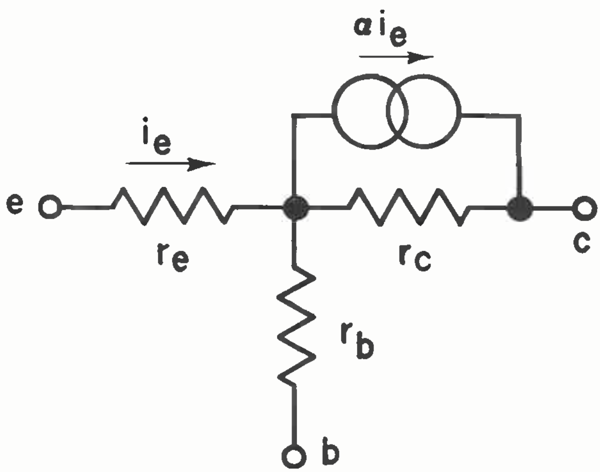
$h_{22} \equiv h_o$ is the output admittance with the input a-c open circuited (mhos)

The letter and numerical subscripts for the "h" parameters are completely equivalent and may be used interchangeably. Common practice is to use the numerical subscripts for general circuit analysis and the letter subscripts for specifying the characteristics of transistors. Since transistors can be measured and used in either the common base, common emitter, or common collector configuration an additional subscript (b, e, or c) is added to the "h" parameters to indicate the particular configuration involved. For example, the forward current transfer ratio in the common emitter configuration is designated by either h_{fe} or h_{21e}.

It is frequently advantageous to use equivalent circuits for transistors to aid in circuit design or to gain understanding of transistor operation. The equivalent circuit for the "h" parameters in the common base configuration is shown in Figure 3.4. In this circuit the voltage transfer ratio, h_{rb}, appears as a voltage generator in the input circuit and the current transfer ratio, h_{fb}, appears as a current generator in the output circuit. Figure 3.5 shows another form of equivalent circuit for the transistor, the "T" equivalent circuit. This equivalent circuit is of interest since it approximates the actual transistor structure. Thus r_e and r_c represent the ohmic resistances of the emitter and collector junction while r_b represents the ohmic resistance between the base contact and the junctions. The current generator αi_e represents the transfer of current from the emitter junction to the collector junction across the base region.



HYBRID EQUIVALENT CIRCUIT (COMMON BASE CONFIGURATION)



"T" EQUIVALENT CIRCUIT

FIGURES 3.4 AND 3.5

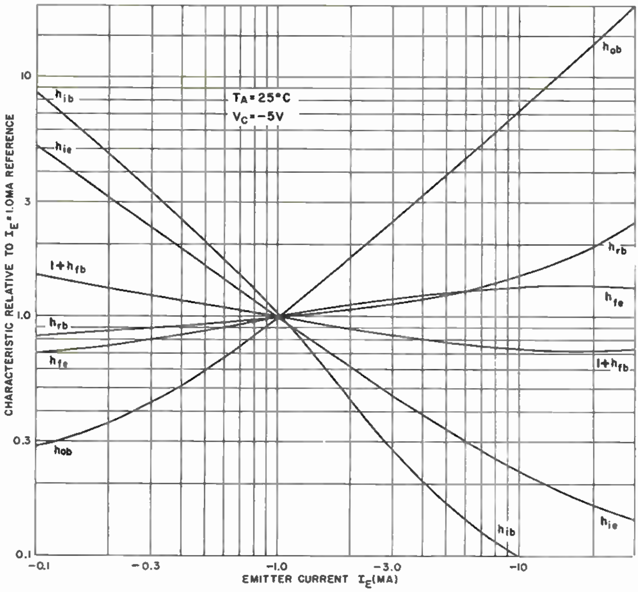
If the "h" parameters are measured or specified for one configuration (e.g., common emitter) the values of the "h" parameters for the other configurations or the values of the parameters in the "T" equivalent circuit may be calculated. Figure 3.6 gives simple conversion equations for all possible cases. Also given in Figure 3.6 are typical values for all the parameters of the 2N525 transistor biased at 1 ma and 5 volts. The "h" parameters are dependent upon the biasing conditions and it is important in circuit design to correct the values of the parameters from the bias conditions under which they are specified to the bias conditions under which the transistors are used. The correction factors can be obtained from a graph such as Figures 3.7 and 3.8.

APPROXIMATE CONVERSION FORMULAE
H PARAMETERS AND T EQUIVALENT CIRCUIT

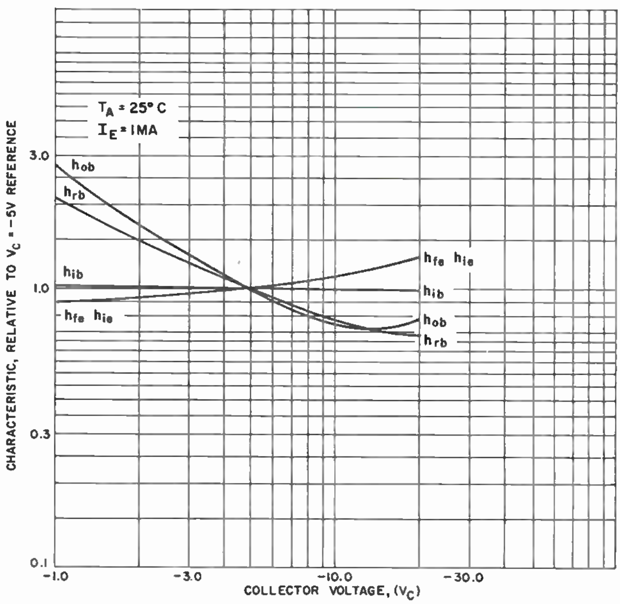
(NUMERICAL VALUES ARE TYPICAL FOR THE 2N525 AT 1 MA, 5V)

SYMBOLS		COMMON EMITTER	COMMON BASE	COMMON COLLECTOR	T EQUIVALENT CIRCUIT
IRE	OTHER				
h_{ie}	$h_{11e}, \frac{1}{Y_{11e}}$	1400 OHMS	$\frac{h_{ib}}{1+h_{fb}}$	h_{ic}	$r_b + \frac{r_e}{1-\alpha}$
h_{re}	h_{12e}, μ_{bc}	3.37×10^{-4}	$\frac{h_{ib} h_{ob}}{1+h_{fb}} - h_{rb}$	$1 - h_{rc}$	$\frac{r_e}{(1-\alpha) r_c}$
h_{fe}	h_{21e}, β	44	$-\frac{h_{fb}}{1+h_{fb}}$	$-(1+h_{fc})$	$\frac{\alpha}{1-\alpha}$
h_{oe}	$h_{22e}, \frac{1}{Z_{22e}}$	27×10^{-6} MHOS	$\frac{h_{ob}}{1+h_{fb}}$	h_{oc}	$\frac{1}{(1-\alpha) r_c}$
h_{ib}	$h_{11}, \frac{1}{Y_{11}}$	$\frac{h_{ie}}{1+h_{fe}}$	31 OHMS	$-\frac{h_{ic}}{h_{fc}}$	$r_b + (1-\alpha) r_b$
h_{rb}	h_{12}, μ_{ec}	$\frac{h_{ie} h_{oe}}{1+h_{fe}} - h_{re}$	5×10^{-4}	$h_{rc} - 1 - \frac{h_{ic} h_{oc}}{h_{fc}}$	$\frac{r_b}{r_c}$
h_{fb}	h_{21}, α	$-\frac{h_{fe}}{1+h_{fe}}$	-0.978	$-\frac{1+h_{fb}}{h_{fb}}$	$-\alpha$
h_{ob}	$h_{22}, \frac{1}{Z_{22}}$	$\frac{h_{oe}}{1+h_{oe}}$	0.60×10^{-6} MHOS	$-\frac{h_{oc}}{h_{fc}}$	$\frac{1}{r_c}$
h_{ic}	$h_{11c}, \frac{1}{Y_{11c}}$	h_{ie}	$\frac{h_{ib}}{1+h_{fb}}$	1400 OHMS	$r_b + \frac{r_e}{1-\alpha}$
h_{rc}	h_{12c}, μ_{be}	$1 - h_{re}$	1	1.00	$1 - \frac{r_e}{(1-\alpha) r_c}$
h_{fc}	h_{21c}, α_{eb}	$-(1+h_{fe})$	$-\frac{1}{1+h_{fb}}$	-45	$-\frac{1}{1-\alpha}$
h_{oc}	$h_{22c}, \frac{1}{Z_{22c}}$	h_{oe}	$\frac{h_{ob}}{1+h_{fb}}$	27×10^{-6} MHOS	$\frac{1}{(1-\alpha) r_c}$
α		$\frac{h_{fe}}{1+h_{fe}}$	$-h_{fb}$	$\frac{1+h_{fc}}{h_{fc}}$	0.978
r_c		$\frac{1+h_{fe}}{h_{oe}}$	$\frac{1-h_{rb}}{h_{ob}}$	$-\frac{h_{fc}}{h_{oc}}$	1.67 MEG
r_e		$\frac{h_{re}}{h_{oe}}$	$h_{ib} - \frac{h_{rb}}{h_{ob}}(1+h_{fb})$	$\frac{1-h_{rc}}{h_{oc}}$	12.5 OHMS
r_b		$h_{ie} - \frac{h_{re}}{h_{oe}}(1+h_{fe})$	$\frac{h_{rb}}{h_{ob}}$	$h_{ic} + \frac{h_{fc}}{h_{oc}}(1-h_{rc})$	840 OHMS

FIGURE 3.6



CHARACTERISTICS VS EMITTER CURRENT



CHARACTERISTICS VS COLLECTOR VOLTAGE

VARIATION OF "H" PARAMETERS WITH BIAS CONDITIONS

FIGURE 3.7 **FIGURE 3.8**

For example, suppose that it is desired to find the typical value of h_{ob} for the 2N525 at 0.5 ma and 10 volts. From Figure 3.6 the typical value of h_{ob} at 1 ma and 5 volts is 0.6×10^{-6} mhos. From Figure 3.7 the correction factor at 0.5 ma is 0.6 and from Figure 3.8 the correction factor at 10 volts is 0.75. The value of h_{ob} is then calculated from:

$$h_{ob}\,(0.5\text{ ma}, 10\text{ v}) = 0.60 \times 10^{-6} \times 0.6 \times 0.75$$
$$= 0.27 \times 10^{-6}\text{ mhos}$$

Once the "h" parameters are known for the particular bias conditions and configuration being used, the performance of the transistor in an amplifier circuit can be found for any value of source or load impedance. Figure 3.9 gives the equations for determining the input and output impedance, as well as the current, voltage, and power gain of a transistor amplifier stage directly from the "h" parameters. The particular "h" parameters used in these equations must correspond to the particular circuit configuration used. For example, if it is desired to calculate the voltage gain of a common emitter amplifier stage the values h_{ie}, h_{re}, h_{fe}, h_{oe} must be used in equation 8.

With the exception of equation 9 all of the equations in Figure 3.9 are valid at any frequency provided that the values of the "h" parameters at that particular frequency are used. At the higher frequencies "h" parameters become complex and the low frequency "h" parameters are no longer valid. The matched power gain given by equation 10 requires that both the input and the output of the amplifier stage be tuned and the input and output resistances be matched to the generator and load resistance respectively. This situation is seldom met exactly in practice, but it is generally met closely enough to permit accurate results from equation 10.

If the voltage feedback ratio, h_r, is very small or is balanced out by external feedback the circuit is said to be unilateral. This means that no signal transmission can take place from the input of the circuit to the output. Under these conditions the input impedance of the circuit will be equal to h_i and the output impedance will be equal to $1/h_o$. The power gain under matched, unilateral conditions is given by equation 11. This power gain is a good figure of merit for the transistor since it is independent of circuit conditions and transistor configuration. It represents the maximum power gain that can be obtained from a transistor under conditions of absolute stability.

As an example of the use of these equations suppose that it is desired to design a tuned amplifier using the 3N37 operating at 150 mc. What power gain can be obtained and what input and output impedances should be used for the matching transformer? From the 3N37 specifications (converting from polar to rectangular form when necessary): $a_{ie} = 80$, $a_{re} = 0.00187$, $a_{fe} = -0.191$, $a_{oe} = 5.5 \times 10^{-4}$, $b_{ie} = -10$, $b_{re} = 0.0179$, $b_{fe} = -1.08$, $b_{oe} = 12.5 \times 10^{-4}$. Putting these numbers into the equations in Figure 3.9 gives:

$$C = -0.062$$
$$D = 0.75$$
$$F = 0.43$$
$$G_m = 8.75$$
$$Z_{im} = 60 - j\,5.0\text{ ohms}$$
$$Y_{om} = (4.15 + j\,12.8) \times 10^{-4}\text{ mhos}$$

In a tuned circuit the reactive part of the output admittance would be tuned out so that:

$$R_i = 60\text{ ohms}$$
$$R_o = 2400\text{ ohms}$$
$$G_m = 10 \log (8.75) = 9.43\text{ db}$$

INPUT IMPEDENCE $$Z_i = \frac{v_i}{i_i} = h_i - \frac{h_f h_r Z_L}{1 + h_o Z_L} \quad (3)$$

MATCHED INPUT IMPEDANCE * $$Z_{im} = a_i \left[D - jC\right] + jb_i \quad (4)$$

OUTPUT ADMITTANCE $$Y_o = \frac{i_o}{v_o} = h_o - \frac{h_f h_r}{h_i + Z_g} \quad (5)$$

MATCHED OUTPUT ADMITTANCE* $$Y_{om} = a_o \left[D - jC\right] + jb_o \quad (6)$$

CURRENT GAIN $$A_i = \frac{i_o}{i_i} = \frac{h_f}{1 + h_o Z_L} \quad (7)$$

VOLTAGE GAIN $$A_v = \frac{v_o}{v_i} = \frac{1}{h_r - \frac{h_i}{Z_L}\left(\frac{1 + h_o Z_L}{h_f}\right)} \quad (8)$$

OPERATING POWER GAIN (LOW FREQUENCY ONLY, $Z_g = R_g, Z_L = R_L$)

$$G = \frac{\text{POWER INTO LOAD}}{\text{POWER INTO TRANSISTOR}} = A_v A_i = \frac{\left(\frac{h_f}{1 + h_o R_L}\right)}{h_r - \frac{h_i}{R_L}\left(\frac{1 + h_o R_L}{h_f}\right)} \quad (9)$$

MATCHED POWER GAIN * $$G_m = \frac{a_f^2 + b_f^2}{a_i a_o \left[(1+D)^2 + C^2\right]} \quad (10)$$

MATCHED UNILATERAL POWER GAIN ($h_r = 0$) $$G_{mu} = \frac{a_f^2 + b_f^2}{4 a_i a_o} = \frac{|h_f|^2}{4 a_i a_o} \quad (11)$$

$Z_g = R_g + jX_g$ = OUTPUT IMPEDANCE OF GENERATOR

$Z_L = R_L + jX_L$ = IMPEDANCE OF LOAD

* FOR MATCHED CONDITIONS

$Z_{im} = R_g - jX_g$

$Z_{om} = R_L - jX_L$

$h_i = a_i + jb_i$

$h_r = a_r + jb_r$

$h_f = a_f + jb_f$

$h_o = a_o + jb_o$

$$C = \frac{a_r b_f + a_f b_r}{2 a_i a_o}$$

$$F = \frac{a_r a_f - b_r b_f}{a_i a_o}$$

$$D = \sqrt{1 - F - C^2}$$

TRANSISTOR CIRCUIT EQUATIONS WITH H-PARAMETERS

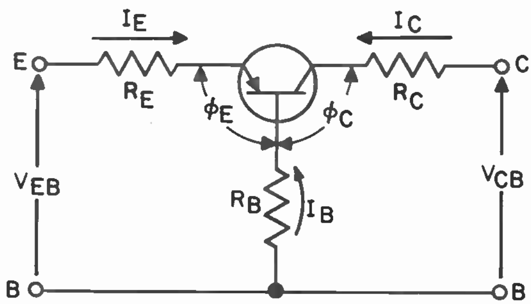
FIGURE 3.9

4. LARGE SIGNAL CHARACTERISTICS

The large signal or d-c characteristics of junction transistors can be described in many cases by the equations derived by Ebers and Moll (Proc. IRE, December, 1954). These equations are useful for predicting the behavior of transistors in bias circuits, switching circuits, choppers, d-c amplifiers, etc. Some of the more useful equations are listed below for reference. They apply with a high degree of accuracy to germanium alloy junction transistors operating at low current and voltage levels, but are also useful for analyzing other types of transistors.

PARAMETERS

The parameters used in the following large signal equations are listed below and indicated in Figure 4.1.



PARAMETERS USED IN LARGE SIGNAL EQUATIONS
FIGURE 4.1

$I_{CO} \equiv I_{CBO}$	Collector leakage current with reverse voltage applied to collector and emitter open circuited (I_{CO} has a positive sign for NPN transistors and a negative sign for PNP transistors)
$I_{EO} \equiv I_{EBO}$	Emitter leakage current with reverse voltage applied to emitter and collector open circuited (I_{EO} has a positive sign for NPN transistors and a negative sign for PNP transistors)
$\alpha_N \equiv \alpha$	Normal alpha, small signal common base forward current transfer ratio from emitter to collector with output a-c short circuited, low current and voltage levels (α has a positive sign for NPN transistors and PNP transistors)
α_I	Inverted alpha, same as α_N but with emitter and collector interchanged
R_B, R_E, R_C	Ohmic resistance internal to transistor in series with base, emitter and collector leads respectively
I_B, I_E, I_C	D-C currents in base, emitter and collector leads respectively, positive sense of current corresponds to current flow into terminals
ϕ_C	Bias voltage across collector junction, collector to base voltage exclusive of ohmic drops (across R_B, R_C), forward bias is positive polarity
ϕ_E	Bias voltage across emitter junction, emitter to base voltage exclusive of ohmic drops (across R_B, R_E), forward bias is positive polarity
V_{EB}, V_{CB}, V_{CE}	Terminal voltages, emitter to base, collector to base, collector to emitter
$\Lambda = \frac{q}{KT}$	$1/\Lambda = 26$ millivolts at 25°C

q	Electronic charge $= 1.60 \times 10^{-19}$ coulomb
K	Boltzmann's constant $= 1.38 \times 10^{-23}$ watt sec/°C
T	Absolute temperature, degrees Kelvin = °C + 273

BASIC EQUATIONS

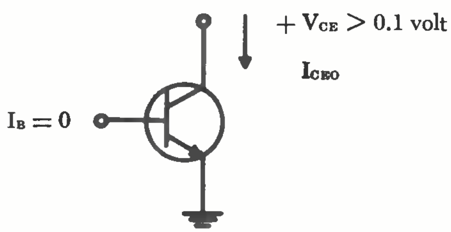
$$\alpha_N I_{EO} = \alpha_I I_{CO} \qquad (4a)$$

$$I_E = -\frac{I_{EO}}{1-\alpha_N\alpha_I}\left(e^{\Lambda\phi_E}-1\right) + \frac{\alpha_I I_{CO}}{1-\alpha_N\alpha_I}\left(e^{\Lambda\phi_C}-1\right) \qquad (4b)$$

$$I_C = +\frac{\alpha_N I_{EO}}{1-\alpha_N\alpha_I}\left(e^{\Lambda\phi_E}-1\right) - \frac{I_{CO}}{1-\alpha_N\alpha_I}\left(e^{\Lambda\phi_C}-1\right) \qquad (4c)$$

Under normal operating conditions, the collector is reverse biased so ϕ_C is negative. If the collector is reverse biased by more than 0.10 volts, then $e^{\Lambda\phi_C} << 1$ and can be eliminated from equations 4b and 4c. The equations given below are derived from equations 4a, 4b and 4c.

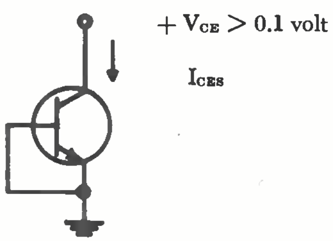
COLLECTOR LEAKAGE CURRENT (I_{CEO})



$$I_{CEO} = \frac{I_{CO}}{1-\alpha_N} \qquad (4d)$$

I_{CEO} is the collector leakage current with the base open circuited and is generally much larger than I_{CO}.

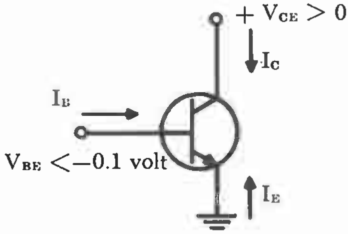
COLLECTOR LEAKAGE CURRENT (I_{CES})



$$I_{CES} = \frac{I_{CO}}{1-\alpha_N\alpha_I} \qquad (4e)$$

I_{CES} is the collector leakage current with the base shorted to the emitter and equals the leakage current the collector diode would have if the emitter junction was not present. Accurate values of α_N and α_I for use in the equations in this section are best obtained by measurement of I_{CO}, I_{CEO} and I_{CES} and calculation of α_N and α_I from equations 4d and 4e. The value of I_{EO} may be calculated from equation 4a.

COLLECTOR AND EMITTER LEAKAGE CURRENT— COLLECTOR AND EMITTER JUNCTIONS REVERSE BIASED

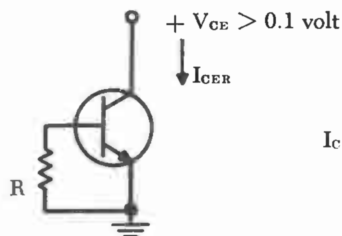


$$I_C = \frac{I_{CO}(1 - \alpha_I)}{1 - \alpha_N \alpha_I} \tag{4f}$$

$$I_E = \frac{I_{EO}(1 - \alpha_N)}{1 - \alpha_N \alpha_I} \tag{4g}$$

Equation 4f indicates that if both the emitter and the collector are reverse biased the collector leakage current will be less than I_{CO} and the emitter leakage current will be less than I_{EO}. The reverse base current will be greater than I_{CO}, but will be less than I_{CO}/α_N. For example, if $\alpha_N = 0.99$ and $\alpha_I = 0.90$ then $I_C = 0.92\ I_{CO}$, $I_E = 0.09\ I_{EO}$ and $I_B = -1.004\ I_{CO}$. This relationship indicates the advantage of using transistors in the inverted connection (collector and emitter interchanged) when a low leakage current is desired in switching circuits.

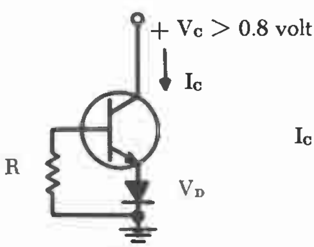
COLLECTOR LEAKAGE CURRENT (I_{CER})



$$I_{CER} = \frac{(1 + AI_{EO}R)\ I_{CO}}{1 - \alpha_N \alpha_I + ARI_{EO}(1 - \alpha_N)} \tag{4h}$$

I_{CER} is the collector leakage current measured with the emitter grounded and a resistor R between base and ground. The size of the resistor is generally about 10K. From equation 4h, it is seen that as R becomes very large I_{CER} approaches I_{CEO} (Equation 4d). Similarly as R approaches zero, I_{CER} approaches I_{CES} (Equation 4e).

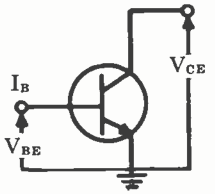
COLLECTOR LEAKAGE CURRENT— SILICON DIODE IN SERIES WITH EMITTER



$$I_C = -\frac{(1 + AI_{EO}R - \alpha_I AV_D)\ I_{CO}}{1 - \alpha_N \alpha_I + ARI_{EO}(1 - \alpha_N)} \tag{4i}$$

This circuit is useful in some switching applications where a low collector leakage current is required and a negative supply voltage is not available for reverse biasing the base of the transistor. The diode voltage V_D used in the equation is measured at a forward current equal to the I_{CO} of the transistor. This equation holds for values of I_C larger than I_{CO}.

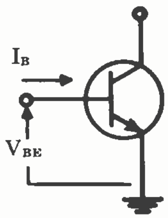
COLLECTOR TO EMITTER VOLTAGE—COLLECTOR OPEN CIRCUITED



$$V_{CE} = I_B R_E + \frac{1}{\Lambda} \ln \frac{1}{\alpha_I} \qquad (4j)$$

The second term in equation 4j indicates that the value of V_{CE} for small values of I_B is determined by the value of α_I. As α_I approaches unity, the second term in equation 4j will approach zero. This indicates the advantage of using a transistor in the inverted connection if a low voltage drop in a switching circuit is desired. Equation 4j also indicates that the series emitter resistance may be obtained by measuring the a-c resistance $R_E = \Delta V_{CE}/\Delta I_B$. The series collector resistance can be measured in the same manner if the transistor is inverted.

BASE INPUT CHARACTERISTICS



for $I_C = 0$:

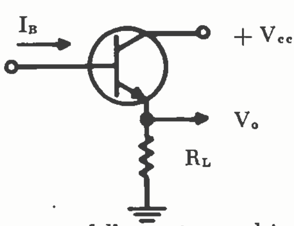
$$V_{BE} = I_B (R_E + R_B) + \frac{1}{\Lambda} \ln \left(\frac{I_B}{I_{EO}} + 1 \right) \qquad (4k)$$

for $V_{CE} > 0.1$ volt:

$$V_{BE} = I_B \left(R_B + \frac{R_E}{1 - \alpha_N} \right) + \frac{1}{\Lambda} \ln \left[\frac{I_B (1-\alpha_N \alpha_I)}{I_{EO} (1-\alpha_N)} + 1 + \frac{\alpha_N (1-\alpha_I)}{\alpha_I (1-\alpha_N)} \right] \qquad (4l)$$

A comparison of equations 4k and 4l indicates that they are approximately equal if R_E is small and α_N is smaller than α_I $(1 - \alpha_N >> 1 - \alpha_I)$. For this condition, the base input characteristic will be the same whether the collector is reverse biased or open circuited.

VOLTAGE COMPARATOR CIRCUIT



for $V_o = V_{cc}$

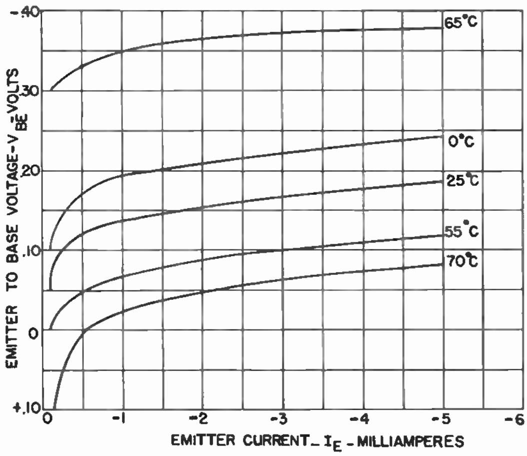
$$I_B = \frac{V_{cc}}{R_L} \left[1 + \left(\frac{\alpha_N}{\alpha_I} \right) \left(\frac{1 - \alpha_I}{1 - \alpha_N} \right) \right] \qquad (4m)$$

If an emitter follower is overdriven such that the base current exceeds the emitter current the emitter voltage can be made exactly equal to the collector voltage. For example, if a square wave with an amplitude greater than V_{cc} is applied to the base of the transistor the output voltage V_o will be a square wave exactly equal to V_{cc}. Equation 4m gives the base current required for this condition and indicates that the transistor should be used in the inverted connection if the required base current is to be minimized. This circuit is useful in voltage comparators and similar circuits where a precise setting of voltage is necessary.

5. BIASING

One of the basic problems involved in the design of transistor amplifiers is establishing and maintaining the proper collector to emitter voltage and emitter current (called the biasing conditions) in the circuit. These biasing conditions must be maintained despite varations in ambient temperature and variations of gain and leakage current between transistors of the same type. The factors which must be taken into account in the design of bias circuits would include:

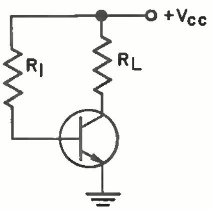
1. The specified maximum and minimum values of current gain (h_{FE}) at the operating point for the type of transistor used.
2. The variation of h_{FE} with temperature. This will determine the maximum and minimum values of h_{FE} over the desired temperature range of operation. The variation of h_{FE} with temperature is shown in Figure 10.7 for the 2N525 transistor.
3. The variation of collector leakage current (I_{CO}) with temperature. For most transistors, I_{CO} increases at approximately 6.5-8%/°C and doubles with a temperature change of 9-11°C. In the design of bias circuits, the minimum value of I_{CO} is assumed to be zero and the maximum value of I_{CO} is obtained from the specifications and from a curve such as Figure 10.6. If silicon transistors are used, it is best to use the specified high temperature I_{CO} for estimating the maximum I_{CO}.
4. The variation of base to emitter voltage drop (V_{BE}) with temperature. Under normal bias conditions, V_{BE} is about 0.2 volts for germanium transistors and 0.7 volts for silicon transistors and has a temperature coefficient of about —2.5 millivolts per °C. Figure 5.1 shows the variation of V_{BE} with collector current at several different temperatures for the 2N525. Note that for some conditions of high temperature it is necessary to reverse bias the base to get a low value of collector current.
5. The tolerance of the resistors used in the bias networks and the tolerance of the supply voltages.

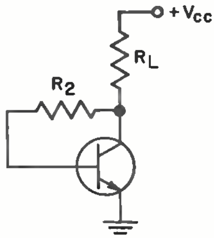


INPUT CHARACTERISTICS OF 2N525 (V_{CE}=1V)

FIGURE 5.1

Two of the simpler types of bias circuits are shown in Figures 5.2 and 5.3. These circuits can be used only in cases where a wide range of collector voltage can be tolerated (for Figure 5.2 at least as great as the specified range of h_{FE}) and where h_{FE}^{max} times I_{CO}^{max} is less than the maximum desired bias current. Neither circuit can be used with transistors which do not have specifications for maximum and minimum h_{FE} unless the bias resistors are selected individually for each transistor. The circuit of Figure 5.3 provides up to twice the stability in collector current with changes in h_{FE} or I_{CO} than the circuit of Figure 5.2. However, the circuit of Figure 5.3 has a-c feedback through the bias network which reduces the gain and input impedance slightly. This feedback can be reduced by using two series resistors in place of R_2 and connecting a capacitor between their common point and ground.

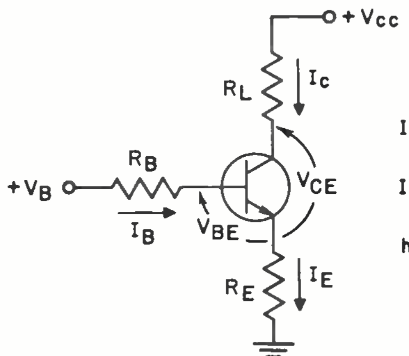




TRANSISTOR BIAS CIRCUITS

FIGURE 5.2 FIGURE 5.3

In cases where more stability is desired than is provided by the circuits of Figure 5.2 or 5.3, it is necessary to use a resistor in series with the emitter of the transistor as shown in Figure 5.4. There are several variations of this circuit, all of which may be obtained by the general design procedure outlined below.



BASIC TRANSISTOR BIAS CIRCUIT
FIGURE 5.4

For the circuit of Figure 5.4, the following equations apply:

$$I_E = (h_{FE} + 1)(I_B + I_{CO}) \quad (5a)$$

$$V_B = \left[\frac{R_B}{(h_{FE} + 1)} + R_E\right] I_E + V_{BE} - I_{CO}R_B \quad (5b)$$

Considering bias conditions at the temperature extremes, at the minimum temperature, I_E will have its minimum value and the worst conditions would occur for $h_{FE} = h_{FE}^{min}$, $V_{BE} = V_{BE}^{max}$, $I_{CO} = 0$ or

$$\text{at lowest temperature:} \quad V_B = \left[\frac{R_B}{h_{FE}^{min}+1} + R_E\right] I_E^{min} + V_{BE}^{max} \qquad (5c)$$

and at the highest temperature of operation I_E will have its maximum value and the worst conditions would occur for $h_{FE} = h_{FE}^{max}$, $V_{BE} = V_{BE}^{min}$, $I_{CO} = I_{CO}^{max}$.

$$\text{at highest temperature:} \quad V_B = \left[\frac{R_B}{h_{FE}^{max}+1} + R_E\right] I_E^{max} + V_{BE}^{min} - I_{CO}^{max} R_B. \qquad (5d)$$

from these two equations the value of R_B can be calculated:

$$R_B = \frac{(I_E^{max} - I_E^{min}) R_E + V_{BE}^{min} - V_{BE}^{max}}{I_{CO}^{max} - \dfrac{I_E^{max}}{h_{FE}^{max}+1} + \dfrac{I_E^{min}}{h_{FE}^{min}+1}} \qquad (5e)$$

As an example, consider the following bias circuit design:

1. Select the transistor type to be used (2N525).
2. Determine the required range of temperature

   0°C to + 55°C
3. Select the supply voltage and load resistance

   $V_{CC} = 20$ volts; $R_L = 7.5K$
4. Determine I_{CO}^{max}:

   From the specifications the upper limit of I_{CO} is 10 μa at 25°C and from Figure 10.6 I_{CO} will increase by a factor of 10 at 55°C, thus $I_{CO}^{max} = 10 \times 10 = 100\ \mu a$.
5. Determine the values of h_{FE}^{min} and h_{FE}^{max}

   From the specifications, the range of h_{FE} at 25°C is 34 to 65. From Figure 10.7 h_{FE} can change by a factor of 0.75 at 0°C and by a factor of 1.3 at +55°C. Thus $h_{FE}^{min} = 0.75 \times 34 = 25$ and $h_{FE}^{max} = 1.3 \times 65 = 85$.
6. Determine the allowable range of I_E:

   In general, the variation of the circuit performance with emitter current determines the allowable range of emitter current. In some cases the allowable range of emitter current is determined by the peak signal voltage required across R_L.

   Assume that the minimum current is .67 ma which gives a minimum voltage of 5 volts across R_L and the maximum emitter current is 1.47 ma which gives a maximum voltage of 11 volts across R_L. The allowable range of emitter current must be modified to take into account the tolerance of the bias resistors. Assuming a bias network using three 5% resistors, then

   $I_E^{min} = (1 + 3 \times .05)(0.67) = 0.77$ ma and

   $I_E^{max} = (1 - 3 \times .05)(1.47) = 1.25$ ma
7. Estimate the values of V_{BE}^{min} and V_{BE}^{max}

   From Figure 5.1 V_{BE}^{min} at 55°C and $I_E = 1.47$ ma is about 0.08 volt, V_{BE}^{max} at 0°C and $I_E = 0.67$ ma is about 0.17 volt.
8. Calculate the value of R_B from equation 5e

   $R_B = 4.15\ R_E - 1.30K$
9. Using the equation trom (8), choose a suitable value of R_B and R_E. This involves a compromise since low values of R_E require a low value of R_B which shunts the

input of the stage and reduces the gain. A high value of R_E reduces the collector to emitter bias voltage which limits the peak signal voltage across R_L.

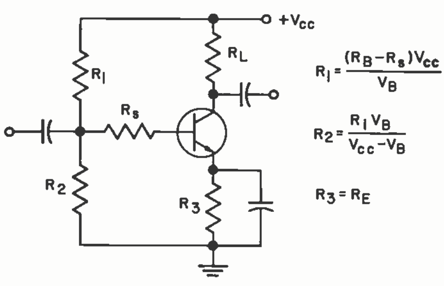
Choose $R_E = 2.7K$ for which $R_B = 9.9K$. This gives a minimum collector to emitter voltage of $20 - (2.7 + 7.5)\ 1.47 = 5$ volts.

10. Calculate V_B using equation 5c

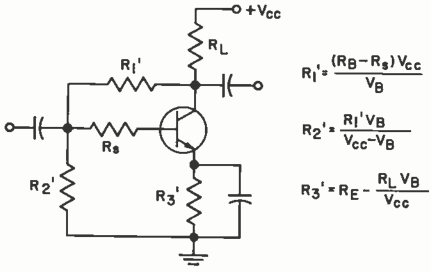
$V_B = 2.56$ volts

11. If the bias circuits of either Figures 5.5 or 5.6 are to be used, the values of the bias resistors can be calculated from the values of R_B, R_E and V_B obtained in the preceding design by the use of the conversion equations which are given. In these figures R_S represents a series resistance which would be present if transformer coupling were used in which case R_S would be the d-c resistance of transformer secondary. In cases where capacitor coupling is used R_S will usually be equal to zero. A comparison of Figures 5.5 and 5.6 indicates that the circuit of Figure 5.6 is superior in that for a given bias stability, it allows a lower value of the emitter resistor or larger values of the base resistors than the circuit of Figure 5.5. On the other hand, the circuit of Figure 5.6 gives a-c feedback through the bias circuits which may be a disadvantage in some cases.

For the circuit of Figure 5.5, assume $R_S = 0$. Then $R_3 = R_E = 2.7K$, $R_1 = 77K$ or, choosing the next lowest standard value, $R_1 = 68K$. Using this value, calculate $R_2 = 10K$. For the circuit of Figure 5.6 as before $R'_1 = 68K$ and $R'_2 = 10K$. Resistor R'_3 is calculated as 1.73K or, using the next highest standard value, $R'_3 = 1.8K$.



VOLTAGE DIVIDER TYPE BIAS CIRCUIT
FIGURE 5.5



VOLTAGE DIVIDER TYPE BIAS CIRCUIT WITH FEEDBACK
FIGURE 5.6

THERMAL RUNAWAY

When a transistor is used at high junction temperatures (high ambient temperatures and/or high power dissipation) it is possible for regenerative heating to occur which will result in thermal run-away and possible destruction of the transistor. In any circuit the junction temperature (T_J) is determined by the total power dissipation in the transistor (P), the ambient temperature (T_A), and the thermal resistance (K).

$$T_J = T_A + KP \tag{5f}$$

If the ambient temperature is increased, the junction temperature would increase an equal amount provided that the power dissipation was constant. However, since both h_{FE} and I_{CO} increase with temperature, the collector current can increase with increasing temperature which in turn can result in increased power dissipation. Thermal run-away will occur when the rate of increase of junction temperature with respect to the power dissipation is greater than the thermal resistance ($\Delta T_J/\Delta P > K$).

Thermal run-away is generally to be avoided since it can result in failure of the circuit and possibly in destruction of the transistor. By suitable circuit design it is possible to ensure either that the transistor can not run away under any conditions or that the transistor can not run away below some specified ambient temperature. A different circuit analysis is required depending on whether the transistor is used in a linear amplifier or in a switching circuit.

In switching circuits such as those described in Chapter 10, it is common to operate the transistor either in saturation (low collector to emitter voltage) or in cutoff (base to emitter reverse biased). The dissipation of a transistor in saturation does not change appreciably with temperature and therefore run-away conditions are not possible. On the other hand, the dissipation of a transistor in cutoff depends on I_{CO} and therefore can increase rapidly at higher temperatures. If the circuit is designed to ensure that the emitter to base junction is reverse biased at all temperatures (as for the circuit of Figure 5.7) the following analysis can be used:

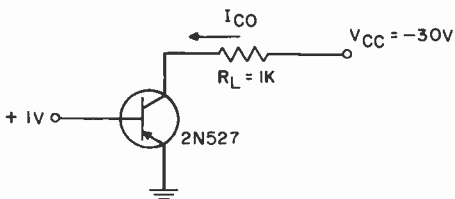


FIGURE 5.7

The transistor power dissipation will be,

$$P = I_{CO}V_{CE} = I_{CO}(V_{CC} - I_{CO}R_L) \tag{5g}$$

The rate of change of power dissipation with temperature will be,

$$\frac{dP}{dT} = (V_{CC} - 2I_{CO}R_L)\,\frac{dI_{CO}}{dT} = (V_{CC} - 2I_{CO}R_L)\,\delta I_{CO} \tag{5h}$$

where $\delta \cong 0.08$ is the fractional increase in I_{CO} with temperature. The condition for run-away occurs when $dP/dT = 1/K$ or,

$$(V_{CC} - 2I_{COM}R_L)\,\delta I_{COM} = 1/K \tag{5i}$$

where I_{COM} is the value of I_{CO} at the run-away point. Solving for I_{COM} gives,

$$I_{COM} = \frac{V_{CC} \pm \sqrt{(V_{CC})^2 - (8R_L)/(\delta K)}}{4R_L} \tag{5j}$$

In this equation the solution using the negative sign gives the value of I_{COM}, while the solution using the positive sign gives the value of I_{CO} after run-away has occurred. It is seen from the equation that the value of I_{CO} after run-away can never be greater than $V_{CC}/2R_L$ so that the collector voltage after run-away can never be less than one half of the supply voltage V_{CC}. If the term under the square root sign in the above equation is zero or negative, thermal run-away cannot occur under any conditions. Also, if thermal run-away does occur it must occur when the collector voltage is greater than $0.75V_{CC}$. Once the value of I_{COM} is determined from Equation (5j) the corresponding junction temperature can be determined from a graph such as Figure 10.6. The heating due to I_{COM} is found by substituting I_{COM} for I_{CO} in Equation (5g). Finally, the ambient temperature at which run-away occurs can be calculated from Equation (5f).

In circuits which have appreciable resistance in the base circuit such as the circuit of Figure 5.8 the base to emitter junction will be reverse biased only over a limited temperature range. When the temperature is increased to the point where the base to emitter junction ceases to be reverse biased emitter current will flow and the dissipation will increase rapidly. The solution for this case is given by:

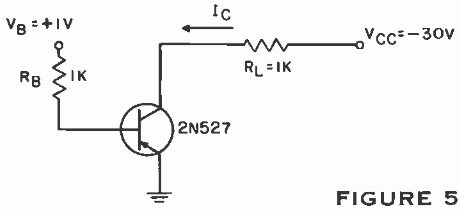


FIGURE 5.8

$$I_{COM} = \frac{(V_{CC} - 2R_L h_{fe} I_x) \pm \sqrt{(V_{CC} - 2R_L h_{fe} I_x)^2 - (8R_L)/(\delta K)}}{4R_L h_{fe}} \quad (5k)$$

where $I_x = V_B/R_B$.

In the analysis of run-away in linear amplifiers it is convenient to classify linear amplifiers into preamplifiers and power amplifiers. Preamplifiers are operated at low signal levels and consequently the bias voltage and current are very low particularly in stages where good noise performance is important. In capacitor coupled stages a large collector resistance is used to increase gain and a large emitter resistance is used to improve bias stability. Accordingly, thermal run-away conditions are seldom met in preamplifier circuits.

In contrast, power amplifiers invariably require transistors to operate at power levels which are near the run-away condition. The conditions are aggravated by the use of biasing networks of marginal stability which are required for power efficiency and by the use of transformer coupling to the load which reduces the effective collector series resistance. Since thermal run-away in power stages is likely to result in destruction of the transistors, it is wise to use worst case design principles to ensure that thermal run-away cannot occur. The worst case conditions are with $h_{fe} \rightarrow \infty$, $V_{BE} = 0$, $R_L = 0$, and $I_{CO} = I_{CO}^{max}$. If these conditions are applied to a transistor in the general bias circuit shown in Figure 5.9 the total transistor dissipation is given by:

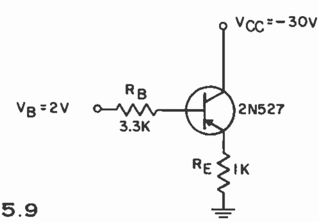


FIGURE 5.9

$$P = V_{CE}I_C = (V_{CC} - V_B - I_{CO}R_B)\left(I_{CO} + \frac{V_B + I_{CO}R_B}{R_E}\right) \tag{5l}$$

Equating dP/dT with 1/K and solving for I_{COM} as before,

$$I_{COM} = \frac{(V_{CC} - R_1V_B) \pm \sqrt{(V_{CC} - R_1V_B)^2 - (R_2)/(\delta K)}}{4R_B} \tag{5m}$$

where

$$R_1 = \frac{R_E + 2R_B}{R_E + R_B} \qquad R_2 = \frac{8R_ER_B}{R_E + R_B}$$

As before, the solution of Equation (5m) using the negative sign gives the value of I_{COM}, while the solution using the positive sign gives the final value of I_C after run-away has occurred. If the quantity under the square root sign is zero or negative, run-away cannot occur under any conditions.

In class-B power amplifiers the maximum transistor power dissipation occurs when the power output is at 40% of its maximum value at which point the power dissipation in each transistor is 20% of the maximum power output. In class-A power amplifiers on the other hand, the maximum transistor dissipation occurs when there is no applied signal. The maximum power dissipation is obtained by substituting I_{COM} in Equation (5l) and the maximum junction temperature is obtained from Equation (5f).

In the design of power amplifiers the usual procedure is to design the circuit to meet the requirements for gain, power output, distortion, and bias stability as described in the other sections of this manual. The circuit is then analyzed to determine the conditions under which run-away can occur to determine if these conditions meet the operating requirements. As a practical example, consider the analysis of the class-A output stage of the receiver shown in Figure 8.16. The transistor is the 2N241A for which K = 250°C/watt and $I_{CO}^{max} = 16\mu a$ at 25°C and 25 volts. Calculating the circuit values corresponding to Figure 5.9 and Equation (5m):

$$V_{CC} = 9 \text{ v}, \quad R_E = 100\ \Omega$$

$$V_B = \frac{(1000)(9)}{1000 + 4700} = 1.58 \text{ v} \qquad R_B = \frac{(1000)(4700)}{1000 + 4700} = 825\ \Omega$$

$$R_1 = \frac{100 + 2(825)}{100 + 825} = 1.89 \qquad R_2 = \frac{8(100)(825)}{100 + 825} = 713\ \Omega$$

Calculating I_{COM} from Equation (5m),

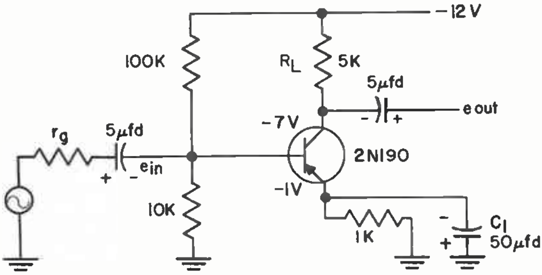
$$I_{COM} = \frac{6 \pm \sqrt{0.47}}{3300} = 1.61 \text{ ma or } 2.02 \text{ ma}$$

Since the quantity under the square root is positive, thermal run-away can occur. The two solutions give the value of I_{COM} (1.61 ma) and the value of I_{CO} after run-away has occurred (2.02 ma). The fact that these two currents are very nearly equal indicates that the change in power dissipation when run-away occurs will not be very large. Using the value $I_{COM}/I_{CO}^{max} = 100$ the junction temperature at run-away from Figure 10.6(A) is about 92°C. The dissipation at run-away, calculated from Equation (51), is about 187 milliwatts. The rise in junction temperature due to this power dissipation is (0.25) (187) = 46.7°C. The ambient temperature at run-away is then calculated to be 92 − 46.7 = 45.3°C. The above value of maximum transistor power dissipation is calculated under the assumption that the series collector resistance is zero. In the circuit under consideration the transformer primary will have a small d-c resistance (R_T) which will reduce the transistor power dissipation by approximately $(I_C)^2R_T$ where I_C is given by the second term in Equation (5l). Assuming that the d-c resistance of the transformer is 20 ohms the reduction in power dissipation for the case just considered will be 18.8 milliwatts and the ambient temperature at run-away will be increased to 50.0°C.

6. AUDIO AMPLIFIERS

SINGLE STAGE AUDIO AMPLIFIER

Figure 6.1 shows a typical single stage audio amplifier using a 2N190 PNP transistor.



SINGLE STAGE AUDIO AMPLIFIER
FIGURE 6.1

With the resistance values shown, the bias conditions on the transistor are 1 ma of collector current and six volts from collector to emitter. At frequencies at which C_1 provides good by-passing, the input resistance is given by the formula: $R_{in} = (1 + h_{fe})\ h_{ib}$. At 1 ma for a design center 2N190, the input resistance would be 43 × 29 or about 1250 ohms.

The a-c voltage gain $\frac{e_{out}}{e_{in}}$ is approximately equal to $\frac{R_L}{h_{ib}}$. For the circuit shown this would be $\frac{5000}{29}$ or approximately 172.

The frequency at which the voltage gain is down 3 db from the 1 Kc value depends on r_g. This frequency is given approximately by the formula:

$$\text{low } f_{3db} \approx \frac{1+h_{fe}}{6.28(r_g C_1)}$$

TWO STAGE R-C COUPLED AMPLIFIER

The circuit of a two stage R-C coupled amplifier is shown by Figure 6.2. The input impedance is the same as the single stage amplifier and would be approximately 1250 ohms.

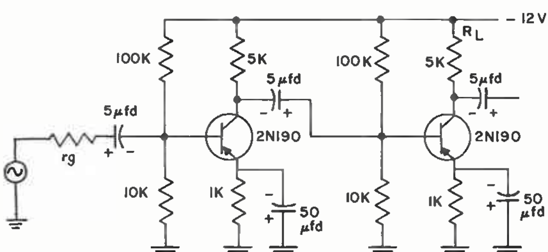


FIGURE 6.2

The load resistance for the first stage is now the input impedance of the second stage. The voltage gain is given approximately by the formula:

$$A_V \approx h_{fe} \frac{R_L}{h_{ib}}$$

More exact formulas for the performance of audio amplifiers may be found in Chapter 3 on small signal characteristics.

CLASS B PUSH-PULL OUTPUT STAGES

In the majority of applications, the output power is specified so a design will usually begin at this point. The circuit of a typical push-pull Class B output stage is shown in Figure 6.3.

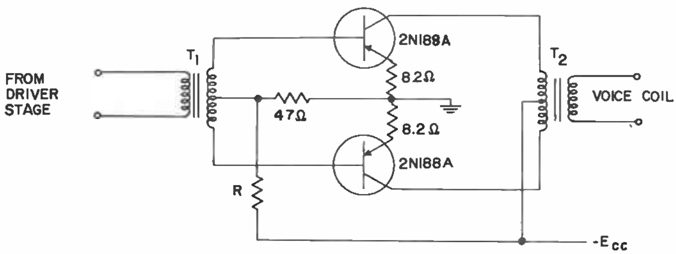


FIGURE 6.3

The voltage divider consisting of resistor, R and the 47 ohm resistor gives a slight forward bias on the transistors to prevent cross-over distortion. Usually about 1/10 of a volt is sufficient to prevent cross-over distortion and under these conditions, the no-signal total collector current is about 3.0 ma. The 8.2 ohm resistors in the emitter leads stabilize the transistors so they will not go into thermal runaway when the junction temperature rises to 60°C. Typical collector characteristics with a load line are shown below:

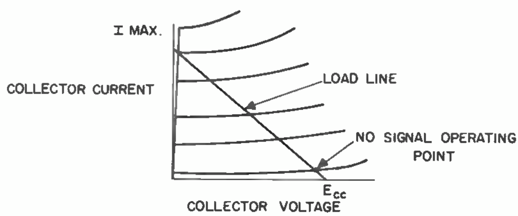


FIGURE 6.4

It can be shown that the maximum a-c output power without clipping using a push-pull stage is given by the formula:

$$P_{out} = \frac{I_{max} \quad V_{CE}}{2}$$

Where V_{CE} = collector to emitter voltage at no signal.

Since the load resistance is equal to

$$R_L = \frac{V_{CE}}{I_{max}}$$

and the collector to collector impedance is four times the load resistance per collector, the output power is given by the formula:

$$P_o = \frac{2 \quad V_{CE}^2}{R_{c-c}} \qquad (6a)$$

Thus, for a specified output power and collector voltage the collector to collector load resistance can be determined. For output powers in the order of 50 mw to 850 mw, the load impedance is so low that it is essentially a short circuit compared to the output impedance of the transistors. Thus, unlike small signal amplifiers, no attempt is made to match the output impedance of transistors in power output stages.

The power gain is given by the formula:

$$\text{Power Gain} = \frac{P_{out}}{P_{in}} = \frac{I_o^2 \quad R_L}{I_{in}^2 \quad R_{in}}$$

Since $\frac{I_o}{I_{in}}$ is equal to the current gain, Beta, for small load resistance, the power gain formula can be written as:

$$P.\,G. = \beta^2 \frac{R_{c-c}}{R_{b-b}} \qquad (6b)$$

where R_{c-c} = collector to collector load resistance.

R_{b-b} = base to base input resistance.

β = grounded emitter current gain.

Since the load resistance is determined by the required maximum undistorted output power, the power gain can be written in terms of the maximum output power by combining equations (6a) and (6b) to give:

$$P.\,G. = \frac{2\beta^2 V_{CE}^2}{R_{b-b} P_{out}} \qquad (6c)$$

CLASS A OUTPUT STAGES

A Class A output stage is biased as shown on the collector characteristics below:

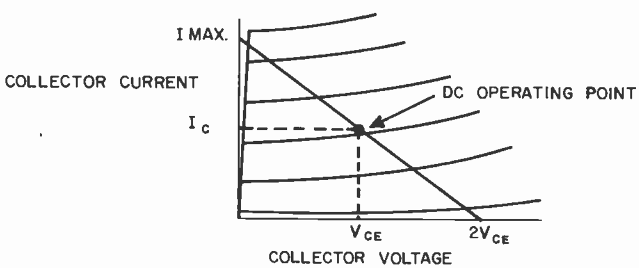


FIGURE 6.5

The operating point is chosen so that the output signal can swing equally in the positive and negative direction. The maximum output power without clipping is equal to:

$$P_{out} = \frac{V_{CE} \quad I_c}{2}$$

The load resistance is then given by the formula:

$$R_L = \frac{V_{CE}}{I_c}$$

Combining these two equations, the load resistance can be expressed in terms of the collector voltage and power output by the formula below:

$$R_L = \frac{V_{CE}^2}{2\,P_o} \qquad (6d)$$

For output powers of 10 mw and above, the load resistance is very small compared to the transistor output impedance and the current gain of the transistor is essentially the short circuit current gain Beta. Thus for a Class A output stage the power gain is given by the formula:

$$\text{P. G.} = \frac{\beta^2 R_L}{R_{in}} = \frac{\beta^2 V_{CE}^2}{2 R_{in} P_o} \qquad (6e)$$

CLASS A DRIVER STAGES

For a required output power of 250 mw, the typical gain for a push-pull output stage would be in the order of 23 db. Thus the input power to the output stage would be about 1 to 2 mw. The load resistance of a Class A driver stage is then determined by the power that must be furnished to the output stage and this load resistance is given by equation (6d). For output powers in the order of a few milliwatts, the load resistance is not negligible in comparison to the output impedance of the transistors, therefore, more exact equations must be used to determine the power gain of a Class A driver stage. From four terminal network theory, after making appropriate approximations, it can be shown that the voltage gain is given by the formula:

$$A_V = \frac{R_L}{h_{ib}} \qquad (6f)$$

where h_{ib} = grounded base input impedance.

The current gain is given by the formula:

$$A_I = \frac{a}{1 - a + R_L h_{ob}} \qquad (6g)$$

where h_{ob} = grounded base output conductance.

The power gain is the product of the current gain and the voltage gain, thus unlike the formula for high power output stages, there is no simple relationship between required output power and power gain for a Class A driver amplifier.

DESIGN CHARTS

Figures 6.6 through 6.16 are design charts for determination of transformer impedances and typical power gains for Class A driver stages, Class A output stages, and Class B push-pull stages. The transformer-power output charts take into account a transformer efficiency of 75% and therefore may be read directly in terms of power delivered to the loudspeaker. Power gain charts show the ratio of output power in the collector circuit to input power in the base circuit and therefore do not include transformer losses. Since the output transformer loss is included in the one chart and the design procedure used below includes the driver transformer loss, it can be seen that the major losses are accounted for.

The charts can best be understood by working through a typical example. Assume a 500 mw output is desired from a 9v amplifier consisting of a driver and push-pull output pair. Also the signal source has an available power output of 156 mμw (156×10^{-9} watts). Overall power gain required then is:

$$\text{P.G.} = \frac{P_{out}}{P_{in}} = \frac{500 \text{ mw}}{156 \text{ m}\mu\text{w}} = \frac{500 \times 10^{-3}}{156 \times 10^{-9}} = 3.2 \times 10^6$$

or approximately 65 db.

To obtain 500 mw in the loudspeaker, the output pair must develop 500 mw plus the transformer loss.

$$P_{collector} = \frac{P_{out}}{\text{transformer eff.}} = \frac{500 \text{ mw}}{.75} = 667 \text{ mw}$$

From Figure 6.10, a pair of 2N321's in Class B push-pull has a power gain of approximately 24.5 db at 667 mw. This is a numerical gain of 280 so the power required by the output stage is:

$$P_{in} = \frac{P_{out}}{\text{Gain}} = \frac{667 \text{ mw}}{280} = 2.38 \text{ mw}$$

If the driver transformer is 75% efficient, the driver must produce:

$$P_{driver} = \frac{\text{P into output stage}}{75\%} = \frac{2.38 \text{ mw}}{.75} = 3.18 \text{ mw}$$

The remaining power gain to be obtained from the driver is 65 db — 24.5 db = 40.5 db. From Figure 6.15 the 2N322 has a power gain of 40.5 db at a power output of 3.18 mw.

The output transformer primary impedance is obtained from Figure 6.6, on the 9 volt supply line at 500 mw output, and is 212 ohms or approximately 200 ohms. The secondary should, of course, match the loudspeaker. From Figure 6.12 the driver transformer primary impedance is 7000 ohms. Therefore, a 7000 ohm or even a 5000 ohm transformer can be used. The secondary must be center-tapped. Typical values of impedance run from 1200 ohms to 4000 ohms. See the specification sheet of the specific output type used for the exact value of input impedance. When this procedure is used for commercial designs it must be remembered that it represents full battery voltage, typical power gain and input impedance, and therefore does not account for end-limit points.

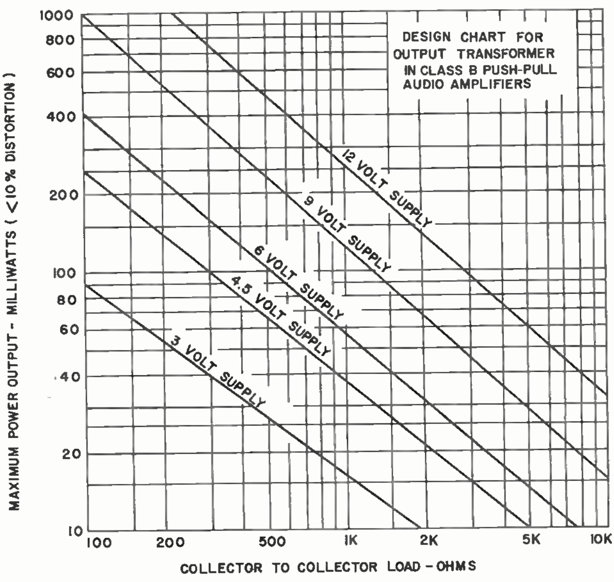


FIGURE 6.6

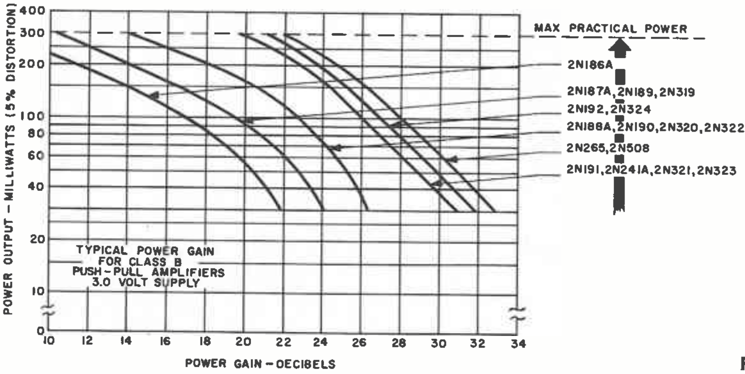


FIGURE 6.7

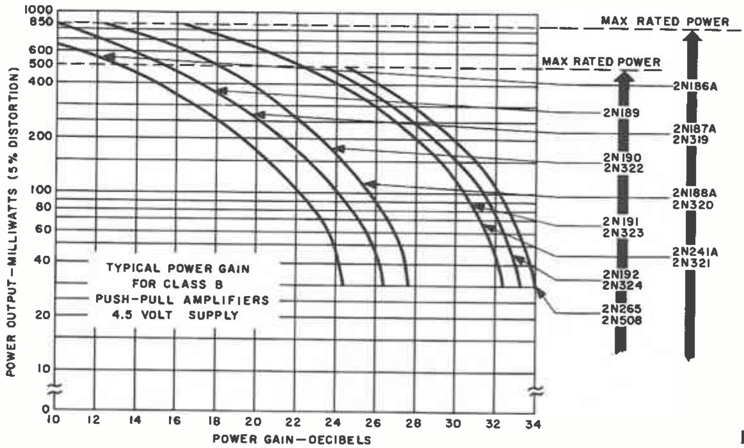


FIGURE 6.8

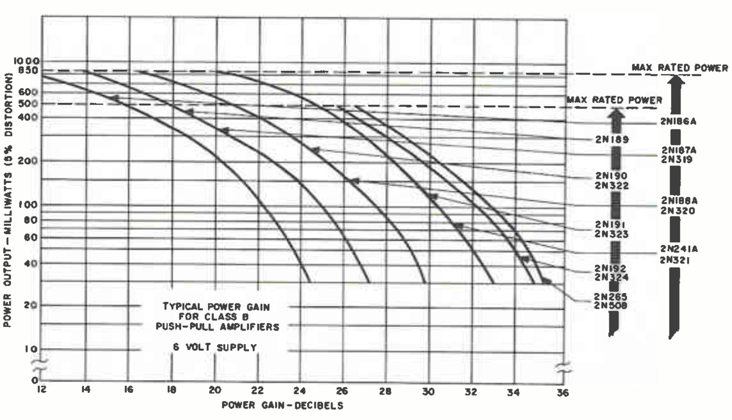


FIGURE 6.9

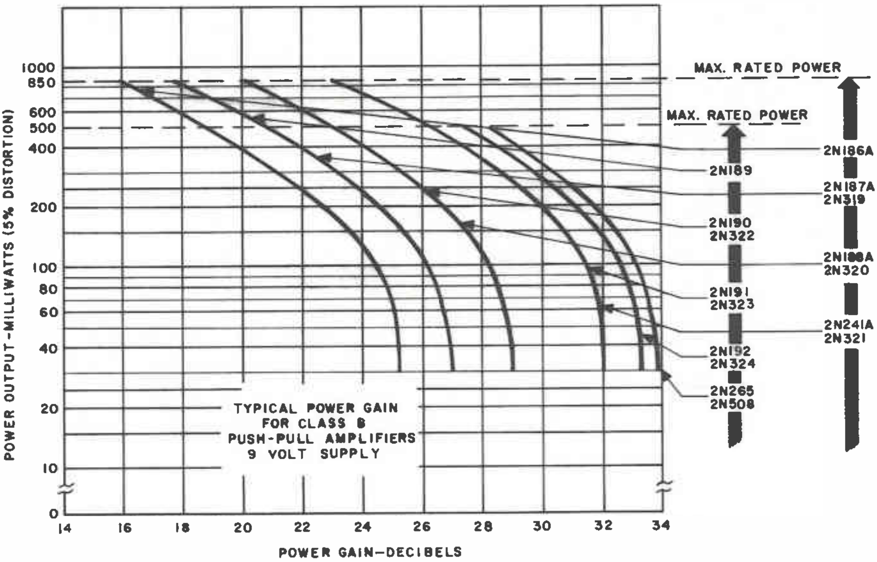


FIGURE 6.10

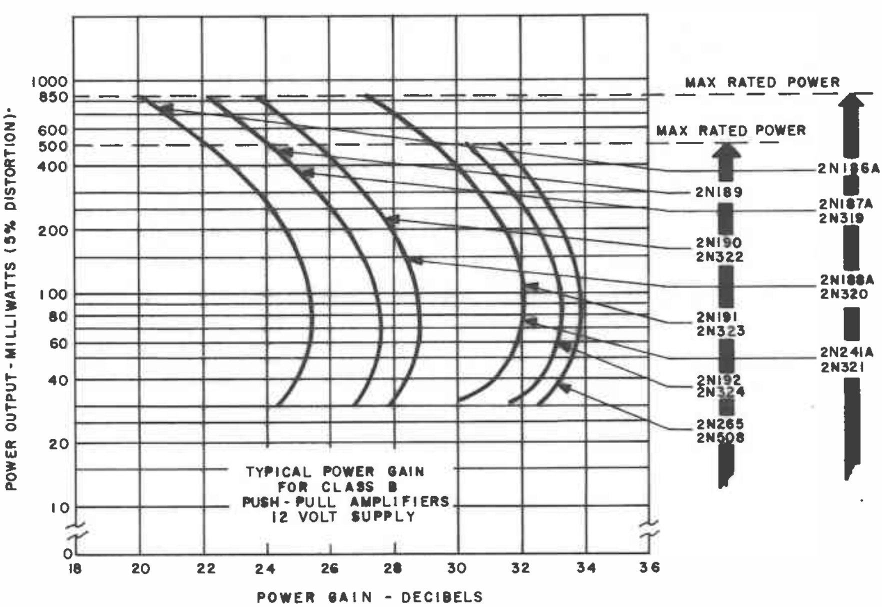


FIGURE 6.11

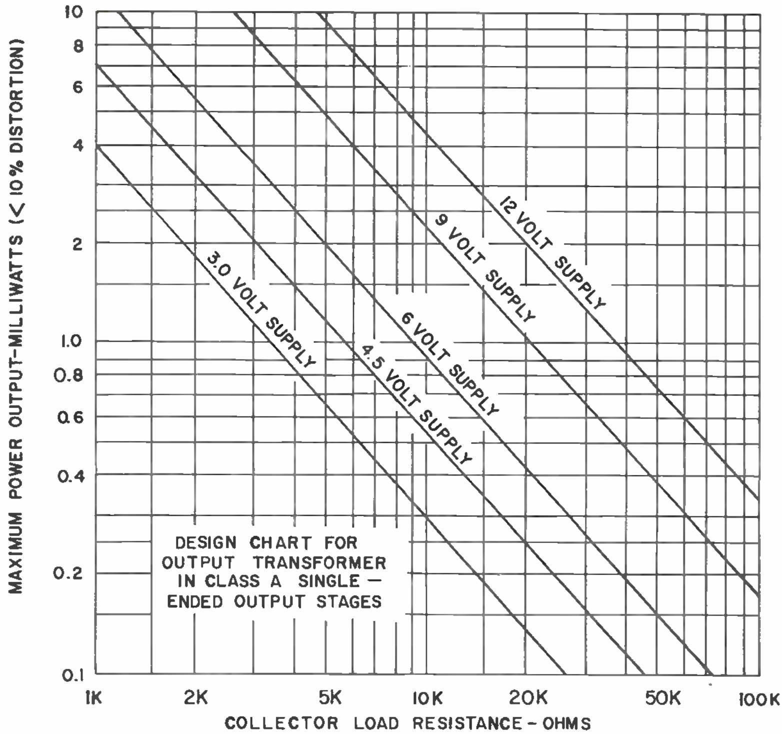


FIGURE 6.12

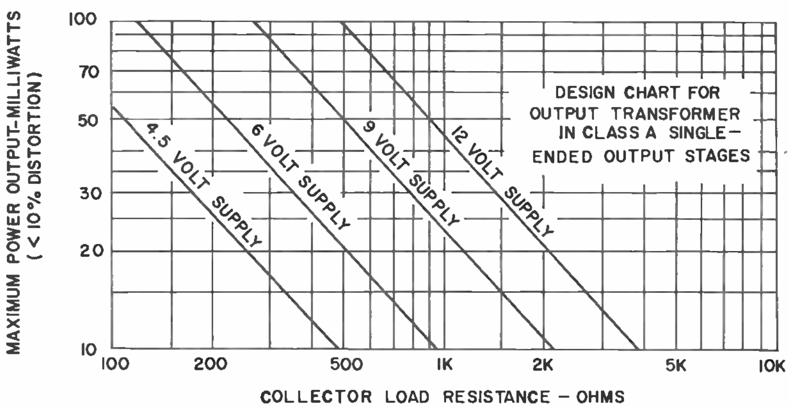


FIGURE 6.13

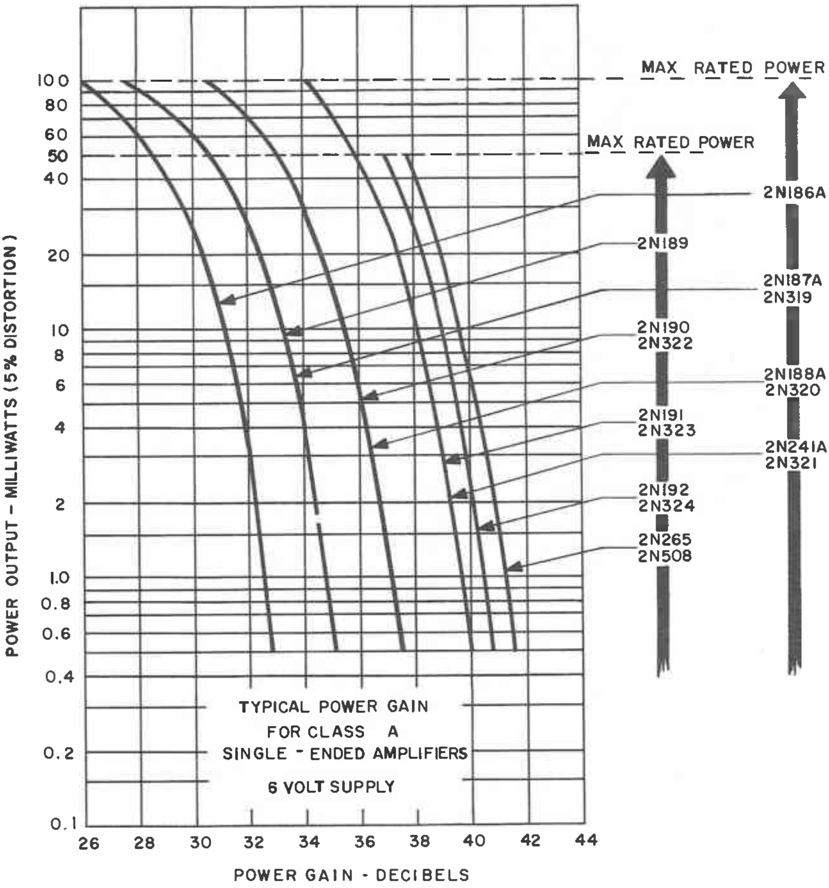

MAX RATED POWER
MAX RATED POWER
2N186A
2N189
2N187A
2N319
2N190
2N322
2N188A
2N320
2N191
2N323
2N241A
2N321
2N192
2N324
2N265
2N508
POWER OUTPUT - MILLIWATTS (5% DISTORTION)
100
80
60
50
40
20
10
8
6
4
2
1.0
0.8
0.6
0.4
0.2
0.1
TYPICAL POWER GAIN
FOR CLASS A
SINGLE - ENDED AMPLIFIERS
6 VOLT SUPPLY
26
28
30
32
34
36
38
40
42
44
POWER GAIN - DECIBELS

FIGURE 6.14

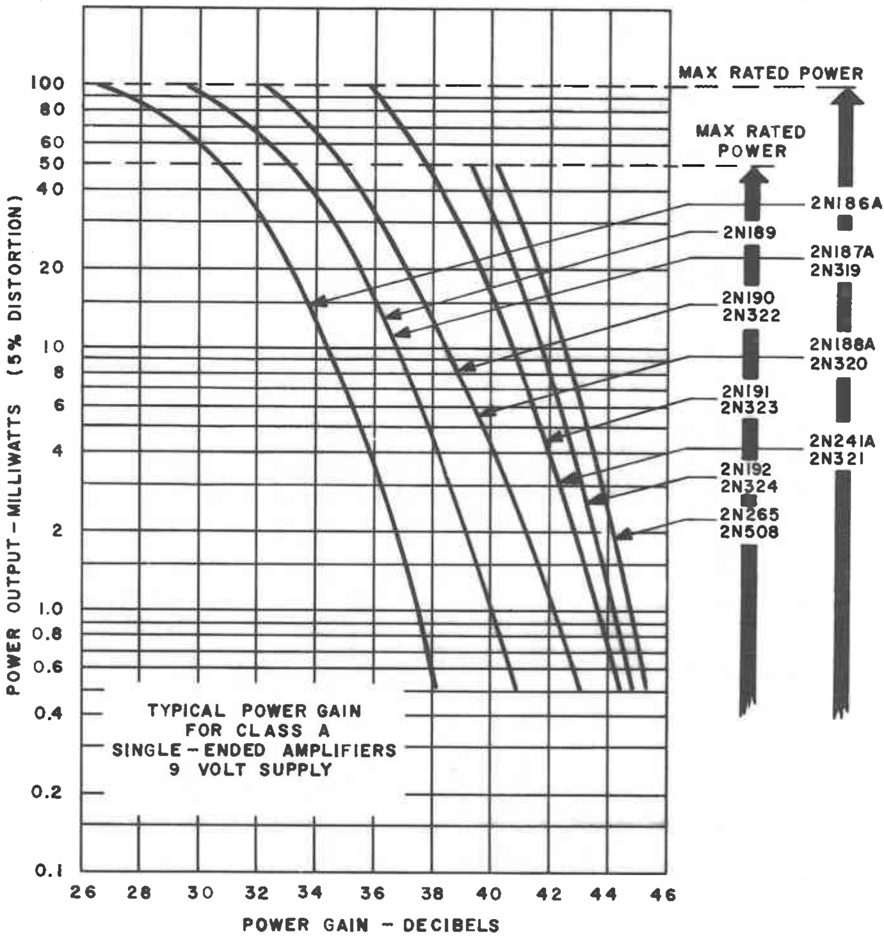
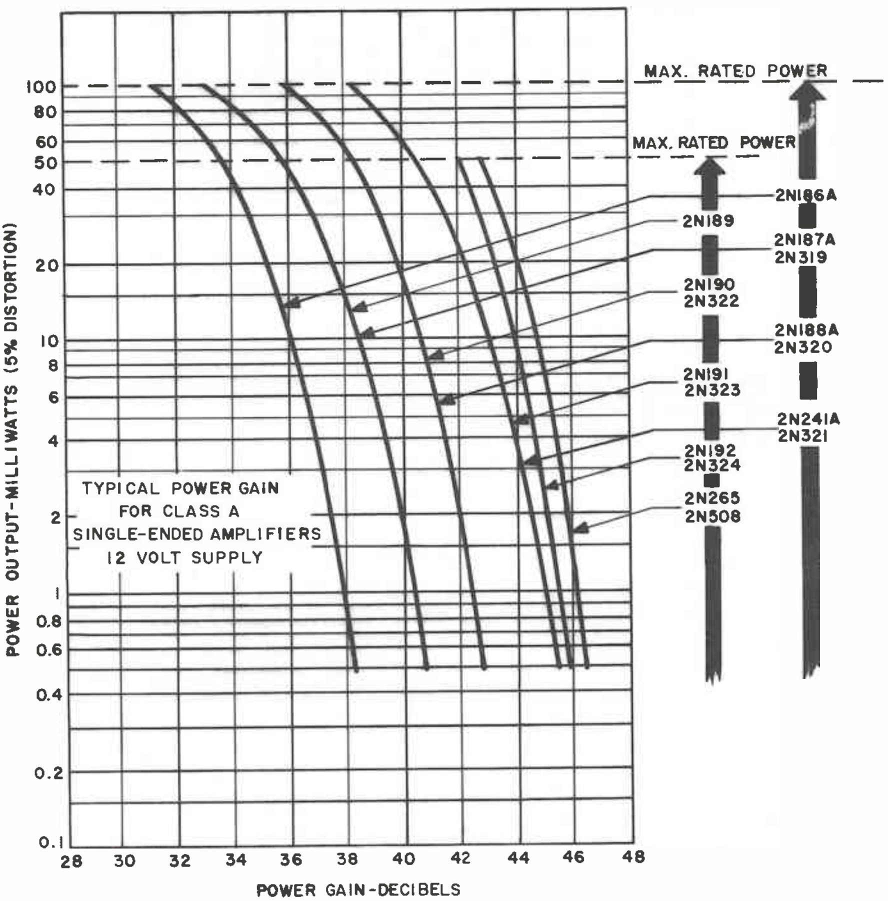

MAX RATED POWER
MAX RATED POWER
2N186A
2N189
2N187A
2N319
2N190
2N322
2N188A
2N320
2N191
2N323
2N241A
2N321
2N192
2N324
2N265
2N508
TYPICAL POWER GAIN FOR CLASS A SINGLE-ENDED AMPLIFIERS 9 VOLT SUPPLY
POWER OUTPUT - MILLIWATTS (5% DISTORTION)
100
80
60
50
40
20
10
8
6
4
2
1.0
0.8
0.6
0.4
0.2
0.1
26
28
30
32
34
36
38
40
42
44
46
POWER GAIN - DECIBELS

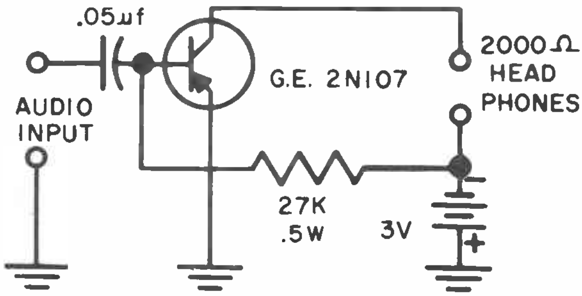
FIGURE 6.15



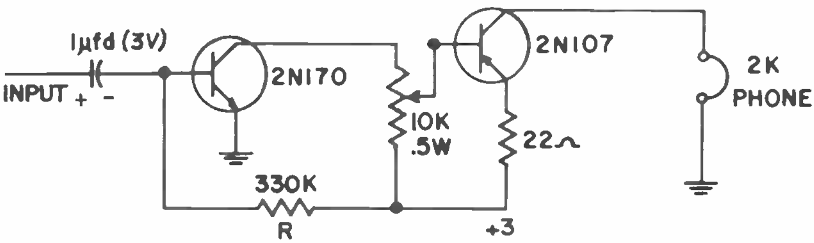
MAX. RATED POWER
MAX. RATED POWER
2N186A
2N189
2N187A
2N319
2N190
2N322
2N188A
2N320
2N191
2N323
2N241A
2N321
2N192
2N324
2N265
2N508
TYPICAL POWER GAIN
FOR CLASS A
SINGLE-ENDED AMPLIFIERS
12 VOLT SUPPLY
POWER OUTPUT-MILLIWATTS (5% DISTORTION)
100
80
60
50
40
20
10
8
6
4
2
1
0.8
0.6
0.4
0.2
0.1
28
30
32
34
36
38
40
42
44
46
48
POWER GAIN-DECIBELS

FIGURE 6.16

AMPLIFIER CIRCUIT DIAGRAMS

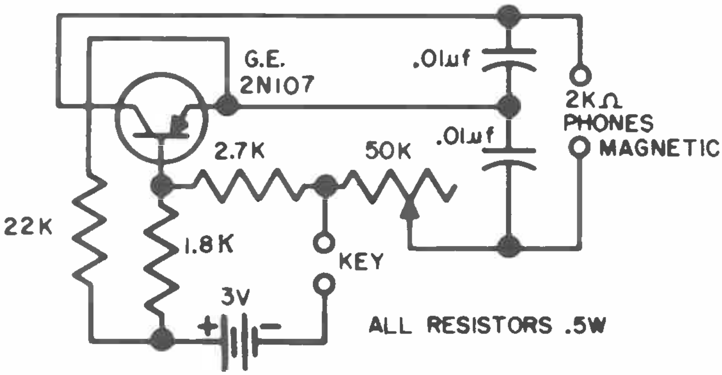


SIMPLE AUDIO AMPLIFIER
FIGURE 6.17

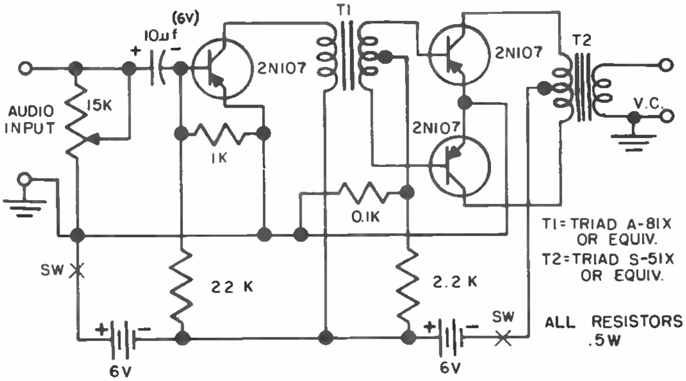


R SHOULD BE ADJUSTED FOR OPTIMUM RESULTS

DIRECT COUPLED "BATTERY SAVER" AMPLIFIER
FIGURE 6.18

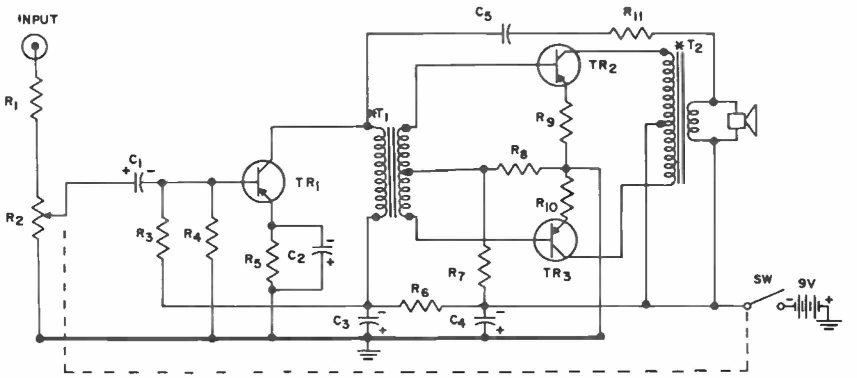


CODE PRACTICE OSCILLATOR
FIGURE 6.19



LOUDSPEAKER AUDIO AMPLIFIER

FIGURE 6.20



R_1,——— 220,000 OHM
R_2,——— VOLUME CONTROL 10,000 OHM 1/2 W AUDIO TAPER
R_3,——— 68,000 OHM
R_4,——— 10,000 OHM
R_5,——— 470 OHM
R_6,——— 220 OHM
R_7,——— 1800 OHM
R_8,——— 33 OHM
R_9,R_{10},— 8.2 OHM
R_{11},——— 4.7K OHM

C_1 ——— 6µfd, 12V
C_2 ——— 100µfd, 3V
C_3, C_4,—50µfd, 12V
C_5,——— .02µfd
TR_1,——— G.E. 2N192 OR 2N265
TR_2,TR_3,–G.E. 2N241A
* T_1 ——— 6KΩ/5KΩ CT
* T_2 ——— 500 Ω CT/ V.C

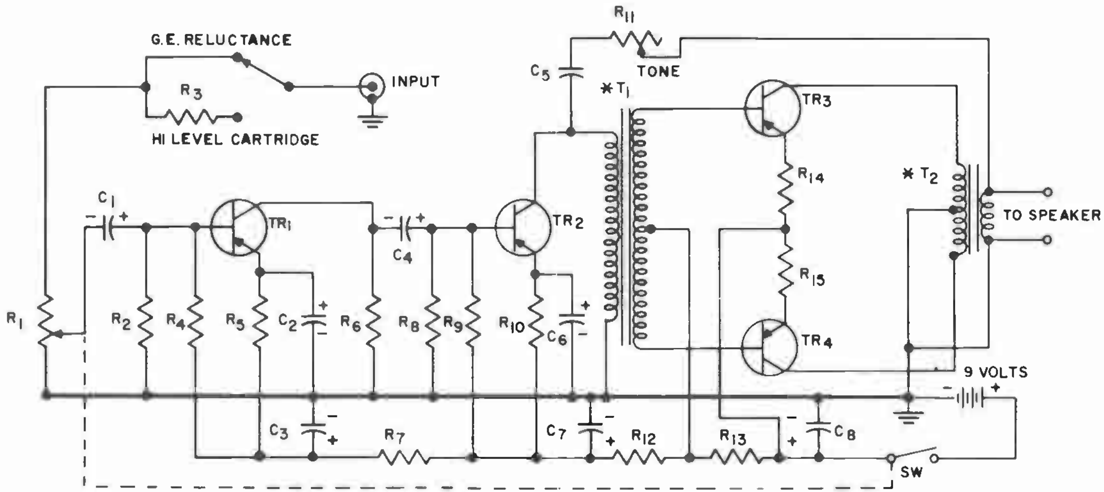
MAXIMUM POWER OUTPUT : .35 WATTS
MAXIMUM POWER OUT AT 10% HARMONIC DISTORTION : .25 WATTS
SENSITIVITY FOR 50 MILLIWATTS REFERENCE POWER OUTPUT : .2 VOLTS
FOR USE WITH MAGNETIC CARTRIDGE OMIT R1, IN THIS CONDITION SENSITIVITY: 5 MILLIVOLTS

ALL RESISTORS .5W

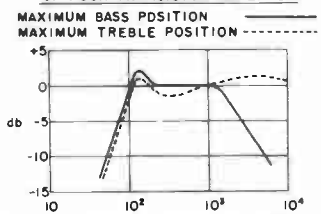
* FOR FURTHER COMPONENT INFORMATION SEE PAGE 226

THREE TRANSISTOR PHONO AMPLIFIER

FIGURE 6.21



FREQUENCY RESPONSE OF FOUR TRANSISTOR AMPLIFIER



AMPLIFIER LOADED WITH 3.2 Ω VOICE COIL SPEAKER RESONANCE @ 130 CPS

- R_1, —5000 OHM VOLUME CONTROL 1/2 W AUDIO TAPER
- R_2, —150,000 OHM
- R_3, —470,000 OHM
- R_4, —10,000 OHM
- R_6, R_9, —4700 OHM
- R_7, —1000 OHM
- R_8, —33,000 OHM
- R_{11}, —25,000 OHM LINEAR
- R_{12}, —220 OHM
- R_5, R_{10}, —470 OHM
- R_{13}, —47 OHM
- R_{14}, R_{15}, —8.2 OHM
- C_1, C_3, C_7, C_8, —50μfd, 12V
- C_2, C_6, —50μfd, 3V
- C_4, —15μfd, 12V
- C_5, —.02μfd
- TR_1, TR_2, —G.E. 2N191 OR 2N323
- TR_3, TR_4, —G.E. 2N188A OR 2N320
- *T_1, —4K/2.6K CT.
- *T_2, —200Ω C.T./V.C.

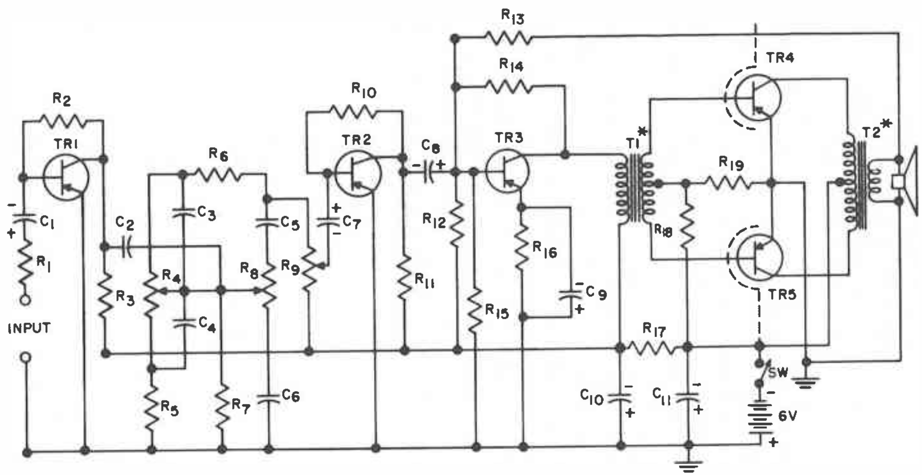
* FOR FURTHER COMPONENT INFORMATION SEE PAGE 226

MAXIMUM POWER OUTPUT : .75 WATTS
MAXIMUM POWER OUT AT 10% HARMONIC DISTORTION : .45 WATTS
DISTORTION AT 100 MILLIWATTS
AT 100 C/S : 5%
AT 1000 C/S : 2%
AT 5000 C/S : 5%
SENSITIVITY FOR 50 MILLIWATTS REFERENCE POWER OUTPUT : CRYSTAL CARTRIDGE : 150 M.V.
MAGNETIC PICK UP : 2 M.V.

ALL RESISTORS .5W

FOUR TRANSISTOR PHONO AMPLIFIER

FIGURE 6.22



R_1 — 10,000 OHMS
R_2 — 150,000 OHMS
R_3 — 6800 OHMS
R_4 — 50,000 OHMS BASS LINEAR
R_5 — 1000 OHMS
R_6 — 10,000 OHMS
R_7 — 100,000 OHMS
R_8 — 50,000 OHMS TREBLE LINEAR
R_9 — 10,000 OHMS TAPER AUDIO V.C.
R_{10} — 220,000 OHMS
TR_1, TR_2, TR_3 — GE 2N323
TR_4, TR_5 — GE 2N321 (WITH CLIP-ON HEATSINK)

R_{11} — 2200 OHMS
R_{12} — 4700 OHMS
R_{13} — 33,000 OHMS
R_{14} — 47,000 OHMS
R_{15} — 1500 OHMS
R_{16} — 330 OHMS
R_{17} — 220 OHMS
R_{18} — 1200 OHMS
R_{19} — 33 OHMS

ALL RESISTORS .5W

C_1 — 8 mfd 6V
C_2 — .50 mfd
C_3 — .02 "
C_4 — .20 "
C_5 — .005 "
C_6 — .10 "
C_7 — 10 mfd 6V
C_8 — 10 mfd "
C_9 — 50 mfd "
C_{10} — 50 mfd "
C_{11} — 50 mfd "
*T_1 — 1K/1K C.T.
*T_2 — 100 Ω C.T/V.C.

PERFORMANCE DATA:
MAXIMUM POWER OUTPUT — 1.00 WATTS
MAXIMUM POWER OUTPUT @ 10% DISTORTION — .75 WATTS
DISTORTION AT 100 MILLIWATTS:
60 c/s — 3.0 %
1000 c/s — 1.5 %
5000 c/s — 3.0 %
SENSITIVITY FOR 50 MILLIWATTS REFERENCE POWER OUTPUT (CRYSTAL CARTRIDGE) — 3.8 mv

* FOR FURTHER INFORMATION SEE PAGE 226

FIVE TRANSISTOR PHONO AMPLIFIER
FIGURE 6.23

7. "HI-FI" CIRCUITS

Transistors are ideally suited for high fidelity amplifiers since there is no problem with microphonics or hum pick-up from filaments as there is with tubes. Transistors are inherently low impedance devices and thus offer better matching to magnetic pick-ups and loudspeakers for more efficient power transfer.

Transistor circuits with negative feedback can give the wide frequency response and low distortion needed in hi-fi equipment. In general, the distortion reduction is about equal to the gain reduction for the circuit to which negative feedback is applied. The input and output impedances of amplifiers with feedback are either increased or decreased, depending on the form of feedback used. Voltage feedback, over one or several transistor stages, from the collector decreases the output impedance of that stage; whereas current feedback from the emitter increases the output impedance of that stage. If either of these networks are fed back to a transistor base the input impedance is decreased, but if the feedback is to the emitter then the impedance is increased. The feedback can be applied to the emitter for effective operation with a low generator impedance, whereas the feedback to the base is effective with a high impedance (constant current) source. If the source impedance was low in the latter case then most of the feedback current would flow into the source and not into the feedback amplifier. The feedback connections must be chosen to give a feedback signal that is out-of-phase with the input for negative feedback.

Care must be used in applying feedback around more than two transistor stages to prevent high frequency instability. This instability results when the phase shift through the transistor amplifiers is sufficient to change the feedback from negative to positive. The frequency response of the feedback loop is sometimes limited to stabilize the circuit. At the present time, the amount of feedback that can be applied to most audio power transistors is limited because of the poor frequency response in the common emitter and common collector connections. The common collector connection offers the advantage of local voltage feedback that is inherent with this connection. Local feedback (one stage only) can be used on high phase shift amplifiers to increase the frequency response and decrease distortion.

PREAMPLIFIERS

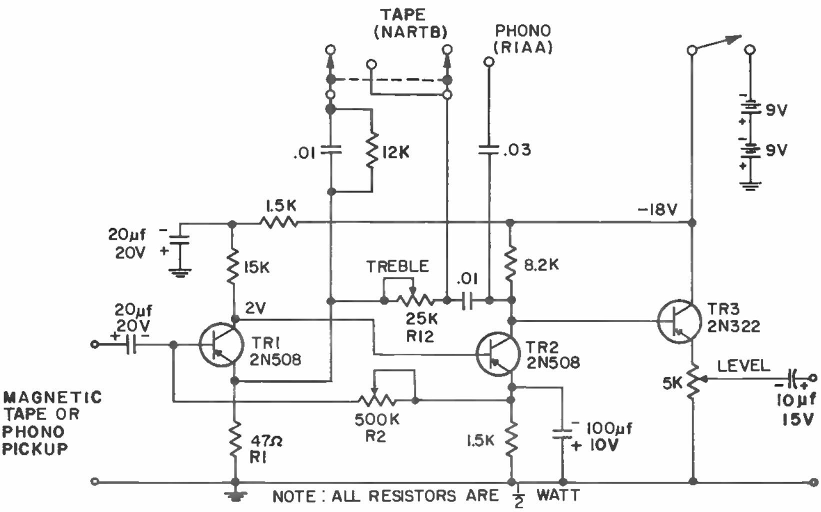
Preamplifiers have two major functions: (1) increasing the signal level from a pick-up device to 1 or 2 volts rms, and (2) providing compensation if required to equalize the input signal for a constant output with frequency.

The circuit of Figure 7.1 meets these requirements when the pick-up device is a magnetic phono cartridge (monaural or stereo), or a tape head. The total harmonic distortion of the preamp is less than ½%.

This preamp will accommodate most magnetic pick-up impedances. The input impedance to the preamp increases with frequency because of the frequency selective negative feedback to the emitter of TR1. The impedance of the magnetic pick-ups will also increase with frequency but are below that of the preamp.

The first two stages of this circuit have a feedback bias arrangement for current stabilization of both stages at ambient temperatures less than 40°C (105°F). R2 from the emitter of TR2 provides this DC current feedback to the base of TR1. R2 should be adjusted to give 2 volts at the collector of TR1. The output stage is well stabilized with a 5K emitter resistance.

The AC negative feedback from the collector of TR2 to the emitter of TR1 is frequency selective to compensate for the standard NARTB recording characteristic



PHONO-TAPE PREAMPLIFIER

FIGURE 7.1

for tape or the standard RIAA for phonograph records. The flat response from a standard NARTB pre-recorded tape occurs with the Treble Control (R12) at mid-position or 12K ohms (see Figure 7.2). There is about 8 db of treble boost with the Control at 25K maximum position, and approximately 20 db of treble cut with R12 = 0. Mid-position of the Treble Control also gives flat response from a standard RIAA recording.

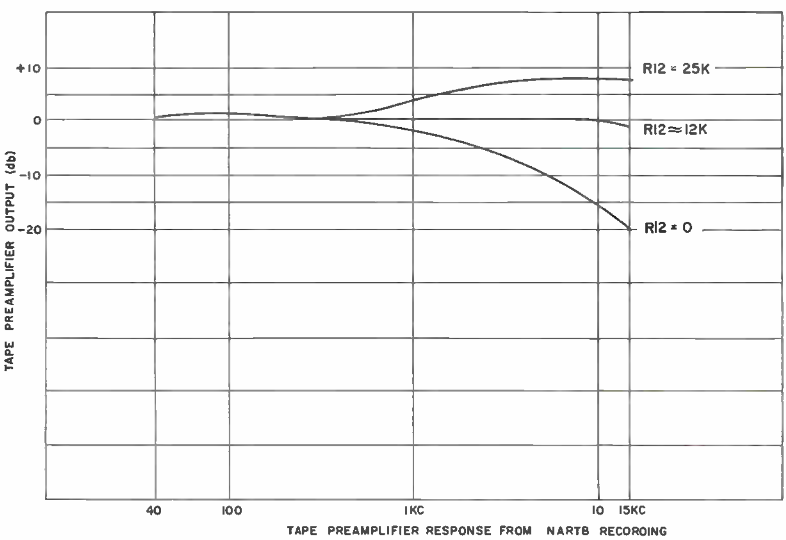


FIGURE 7.2

The voltage feedback from the collector of TR2 decreases at low frequencies because of the increasing reactance of the feedback capacitor in series with the Treble Control. Each of the two feedback networks give the desired increase in gain at the lower frequencies to accomplish the correct compensation. If this feedback capacitor were shunted by an electrolytic capacitor, the preamplifier would give constant gain at all frequencies (in the "Tape" switch position) and the gain will decrease as R12 is decreased. With this flat preamp response a tuner may be connected to the preamp input with a variable attenuator network. This network might consist of a 50K potentiometer in series with a 1K resistor across the tuner output to ground, connect the preamp input across the 1K resistor which has one side on ground.

The RIAA feedback network (with Treble Control at mid-position) has a net feedback resistance of 6K to decrease the gain because of the higher level input. This resistance has a .01 μf capacitor in parallel for decreasing the amplifier gain at the higher frequencies in accordance with RIAA requirements. This eliminates the need to load a reluctance pick-up with the proper resistance for high frequency compensation. If it is desirable to build the preamplifier for phonograph use only, the compensating feedback network would consist only of a .04 μf feedback capacitor in series with a 6K resistor (or a 10K Treble Control) which has a .01 μf capacitor in parallel.

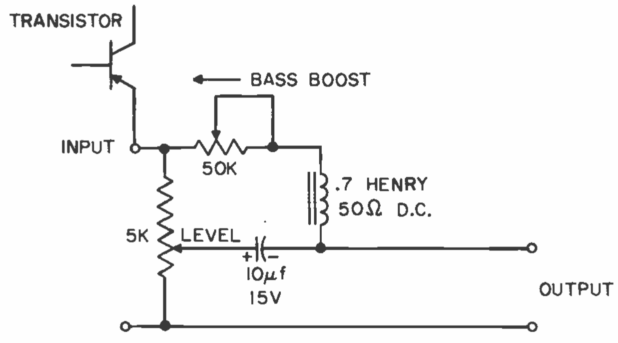
The emitter-follower output stage of the preamp gives a low impedance output for a cable run to a power amplifier (transistor or tube) and acts as a buffer so that any preamp loading will not affect the equalization characteristic.

The Treble Control should have a linear taper and the Level Control an audio taper. Two 9 volt batteries will give good life in this application since the total supply drain is approximately 3.5 ma DC. This 18 volts may also be obtained by suitable decoupling from a higher voltage supply that is available.

The preamplifier of Figure 7.1 may be altered to compensate for tapes recorded at 3¾ inches per second by setting R12 at 25K ohms and making the feedback capacitor .02 μf ± 20%. In addition, the 47 ohm resistor from the emitter of TR1 to ground may be shunted with .5 μf to attain a relatively flat response to 10 Kc. The value needed for this shunt capacitor will depend somewhat on the high frequency response of the tape head that is used, since this capacitor contributes to increased circuit gain above 3 Kc.

BASS BOOST CIRCUIT

The bass boost circuit of Figure 7.3 operates on the output of the preamp (Figure 7.1). With this addition, the operator now has the necessary treble and bass control



BASS BOOST CIRCUIT
FIGURE 7.3

to compensate for listening levels, or deficiencies in program material, pick-up, speakers, etc. This bass boost circuit gives the operator independent control of the level, or amount of bass boost desired, or the level control can be used as a loudness control.

It is usually desirable to have some method of boosting the level of the lower portion of the audio spectrum as the overall sound level is decreased. This is to compensate for the non-linear response of the human ear as shown in the Fletcher-Munson curves that are often referred to in the audio industry. The ear requires a higher level for the low frequency sound to be audible as the frequency is decreased and also as the overall spectrum level is decreased.

Figure 7.4 shows the frequency characteristics of this bass boost circuit. With the level control set for zero attenuation at the output there is no bass boost available, but as the output level is attenuated, the available bass boost increases.

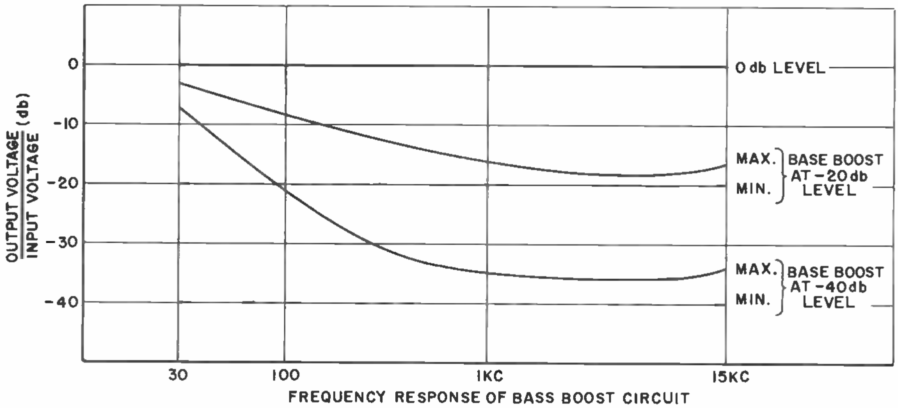


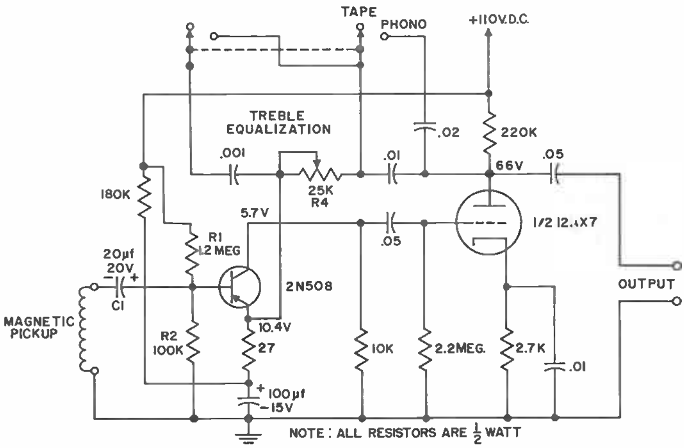
FIGURE 7.4

Figure 7.4 shows the frequency response (lower dashed curve) when the output is attenuated 40 db and the Bass Boost Control is set for minimum (50K ohms). The solid curve immediately above represents the frequency response when the Bass Boost Control is set at maximum (zero ohms). Thus a frequency of 30 cycles can have anything from zero to 27 db of boost with respect to 1 KC, depending on the adjustment of the Bass Boost Control.

The Fletcher-Munson contours of equal loudness level show most of the contour changes involve a boost of the bass frequencies at the lower levels of intensity. Therefore, this circuit combination fulfills the requirements of level control, bass boost and loudness control. This boost circuit operates with the preamp (Figure 7.1) Level Control performing the same function as the Level Control in Figure 7.3. The Bass Boost Control may be a standard 50K potentiometer with a linear taper. The desired inductance may be obtained by using the green and yellow leads on the secondary of Argonne transistor transformer #AR-128.

HYBRID PREAMPLIFIER

The hybrid preamplifier circuit of Figure 7.5 uses a similar feedback equalization technique to that of Figure 7.1 and therefore will accommodate most magnetic pick-up impedances. There is a small amount of treble boost above 10 KC due to the .01 μf capacitor from the 12AX7 cathode to ground. The Treble Control is set near mid-position for a compensated output from a standard RIAA recording or an NARTB recorded tape.



HYBRID PHONO-TAPE PREAMPLIFIER

FIGURE 7.5

The 2N508 transistor is biased at approximately .6 ma from a constant current source for good current stability with temperature and transistor interchangeability. R1 and R2 bias the base for the desired V_{CE}. V_{CE} is in the range of .5 to 5 volts. This voltage varies with leakage current of C1, also with h_{FE} and I_{CO} for different transistors. This range of V_{CE} bias has little effect on the operation of the preamplifier. V_{CE} may reach saturation at ambient temperatures above 55°C.

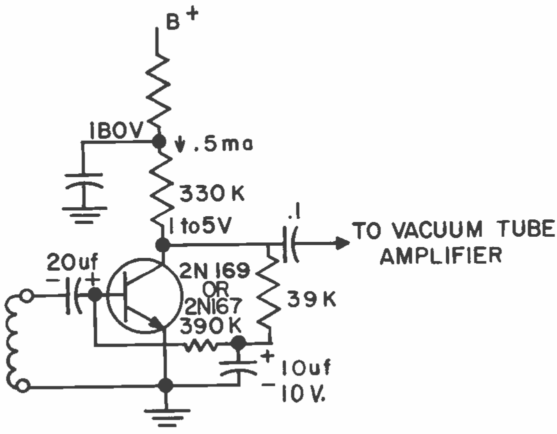
The standard reference level for S/N (signal-to-noise) measurements in tape recording is the maximum level at which a 400 cycle signal can be recorded at 2% harmonic distortion. The hybrid preamplifier of Figure 7.5 is capable of a S/N of 60 db. The signal output from this reference level is approximately 1.5 volts and the total harmonic distortion of the preamp at this level is under 1%.

A dual preamp for a stereophonic disc or tape system could be built with two identical preamps as in Figure 7.5, using only one tube (12AX7) and two transistors (2N508).

In vacuum tube circuitry there is a problem in maintaining high S/N ratio at low audio frequencies because of the lower signal transfer from a magnetic pickup (tape, phono, or microphone) to the tube grid.

The lower input impedance of the transistor more nearly matches the source at low frequencies for a better signal transfer and thus improved S/N ratio. The input signal level at 100 cps has about 40 db of amplification in Figure 7.6 before it reaches the tube grid.

This circuit has a constant collector bias current that is independent of transistor parameters. The collector to emitter voltage, V_{CE}, is biased with a DC feedback network from the collector which helps to stabilize V_{CE}. This circuit should operate to about 50°C ambient temperature with the 2N169 and to 60°C with the 2N167.



NPN PREAMPLIFIER FOR MAGNETIC PICKUPS
FIGURE 7.6

The circuit has an input impedance of about 3K ohms, and frequency compensation of the input signal may be accomplished in a following stage.

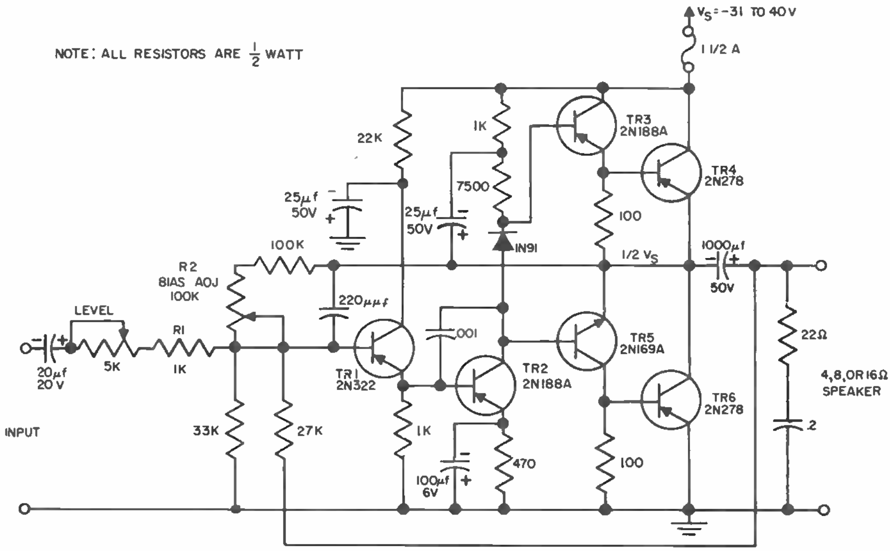
POWER AMPLIFIERS

A great deal of effort has gone into developing transformerless push-pull amplifiers using vacuum tubes. Practical circuits, however, use many power tubes in parallel to provide the high currents necessary for direct driving of low impedance loudspeakers.

The advent of power transistors has given new impetus to the development of transformerless circuits since the transistors are basically low voltage, high current devices. The emitter follower stage, in particular, offers the most interesting possibilities since it has low inherent distortion and low output impedance.

Figure 7.7 is a direct coupled power amplifier with excellent low frequency response, and also has the advantage of a feedback arrangement for current stabilization of all stages. The feedback system also stabilizes the voltage division across the power output transistors TR4 and TR6 which operate in a Class B push-pull arrangement. TR3 and TR5 also operate Class B in the Darlington connection to increase the current gain. Using an NPN for TR5 gives the required phase inversion for driving TR6 and also has the advantage of push-pull emitter follower operation. TR4 and TR6 have a small forward bias to minimize crossover distortion. This bias is set by the voltage drop across the 100 ohm resistors that shunt the input to TR4 and TR6. TR3 and TR5 are biased for the same reason with the voltage drop across the 1N91. A 68 ohm resistor would serve the same function as the 1N91 except there would be no temperature compensation. Thermistors have also been used to compensate for the temperature variation of the emitter-base resistance, but they do not track this variation as well as a germanium junction diode which has temperature characteristics similar to the transistor.

TR2 is a Class A driver requiring a very low impedance drive which is accomplished by an emitter follower TR1. TR1 needs a current source for low distortion, thus R1 and the Level Control supply the desired drive impedance. The Level Control should be set for a value of approximately 2K ohms when this amplifier is driven by the preamplifier of Figure 7.1. This will permit the amplifier to be driven to full output. TR1 has an emitter current of 1 to 1.5 ma, and TR2 has a 2 to 3 ma bias.



SEVEN WATT POWER AMPLIFIER
FIGURE 7.7

The bias adjust R2 is set for one-half the supply voltage across TR6 and can be trimmed for symmetrical clipping at maximum power output. TR4 and TR6 have a beta cut-off at approximately 7 Kc. The phase shift and drop in beta gives rise to a decline in transistor efficiency which causes an elevation of junction temperature. The .001 μfd feedback capacitor from collector to base of TR2 aids in stabilizing this circuit by reducing the phase shift and high frequency gain of this stage. The 220 μμfd capacitor shunting the bias network further aids the stabilization with high frequency negative feedback from output to input. This circuit has approximately 15 db of overall voltage feedback with the 27K resistor from load to input. The speaker system is shunted by 22 ohm in series with .2 μfd to prevent the continued rise of the amplifier load impedance and its accompanying phase shift beyond the audio spectrum.

The overall result, from using direct-coupling, no transformers, and ample degeneration, is an amplifier with output impedance of ½ ohm for good speaker damping, and very low total harmonic distortion. The frequency response at average listening levels is flat over the audio spectrum.

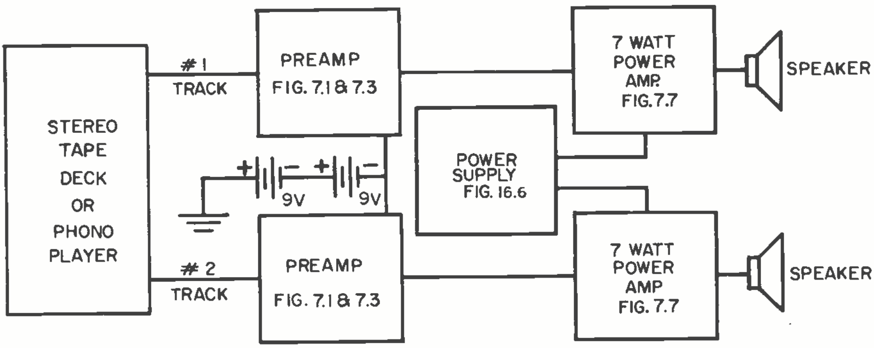
When checking for maximum power out at the higher frequencies, a sinewave can be applied only for a short duration before sufficient heating for runaway results as indicated above. To protect the power transistors, a current meter should be used in series with the voltage supply for quick, visual indication of runaway while checking power output above approximately 2 Kc. There is not sufficient sustained high frequency power in regular program material to precipitate this instability. Thus the actual performance of the amplifier does not suffer since the power level in music and speech declines as the frequency increases beyond about 1 Kc.

This amplifier is capable of a 7 watt output with less than 1% harmonic distortion into a 4, 8 or 16 ohm speaker when used with the power supply of Figure 16.5, page 158.

The power transistors TR4 and TR6 should each be mounted on an adequate heat radiator such as used for transistor output in an automobile radio, or mounted on a 3" x 3" x 3⁄32" aluminum plate that is insulated from the chassis.

STEREOPHONIC SYSTEM

A complete semiconductor, stereophonic playback system may be assembled by using the following circuits in conjunction with a stereophonic tape deck or phono player.



BLOCK DIAGRAM OF STEREOPHONIC SYSTEM
FIGURE 7.8

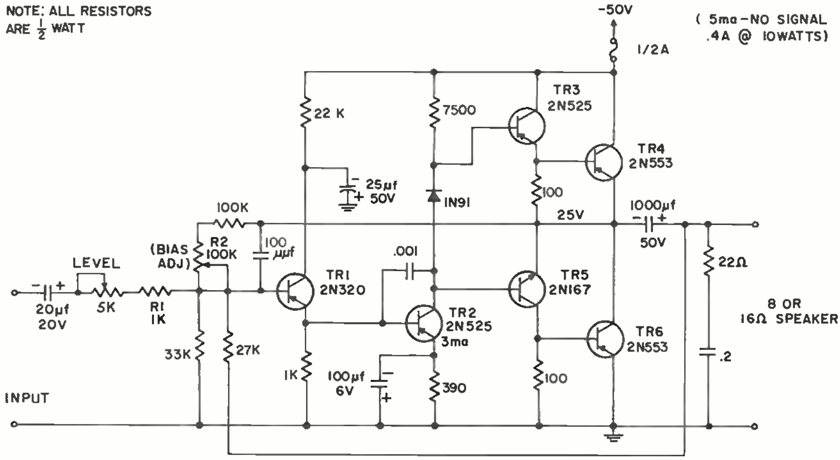
Two identical preamplifier circuits can use a common 18 volt battery supply. The circuitry of Figure 7.1 may be used with the switch and RIAA network eliminated if the preamps are to be used for tape only.

The output of each preamp is fed to a power amplifier as indicated in Figure 7.8. Two identical power amplifiers with circuitry as in Figure 7.7 can use a common power supply as shown in Figure 16.6, page 159. The output of each amplifier fed to its respective speaker completes the stereo system as shown in Figure 7.8.

DUAL 10 WATT STEREO SYSTEM

A dual 10 watt stereo system consists of two identical amplifiers with circuitry of Figure 7.9 using the common power supply of Figure 16.7, page 159. This power supply has separate decoupled outputs for each amplifier. The 1N1115 rectifiers should be mounted on a metal chassis with the electrically insulating mounting kit provided with each unit. The stereo system uses the same preamplifiers as that of Figures 7.1 and 7.3.

The power amplifier of Figure 7.9 is similar to that of Figure 7.7. Figure 7.9 uses transistors with a higher voltage rating, and also the 2N553 transistor has a beta cut-off frequency of approximately 25 Kc. Thus the 2N553's in Figure 7.9 give increased efficiency and thus better stability at the higher frequencies. This amplifier with power supply of Figure 16.7, page 159, is capable of a 10 watt output with less than 1% distortion into an 8 or 16 ohm speaker.

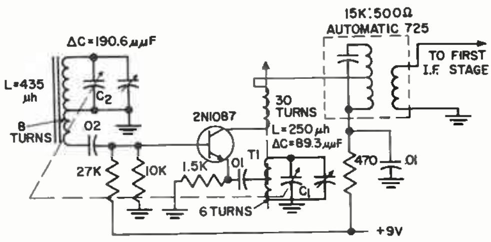


TEN WATT POWER AMPLIFIER
FIGURE 7.9

8. RADIO RECEIVER CIRCUITS

AUTODYNE CONVERTER CIRCUITS

The converter stage of a transistor radio is a combination of a local oscillator, a mixer and an IF amplifier. A typical circuit for this stage is shown in Figure 8.1.



FOR ADDITIONAL INFORMATION SEE PAGE 226

AUTODYNE CONVERTER
FIGURE 8.1

Redrawing the circuit to illustrate the oscillator and mixer sections separately, we obtain Figures 8.2 and 8.3.

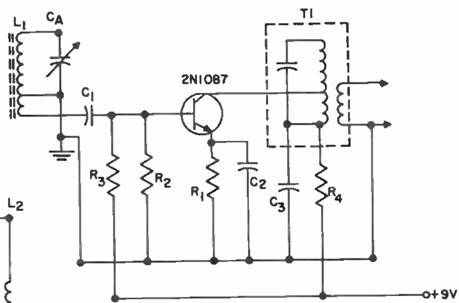


FIGURE 8.3

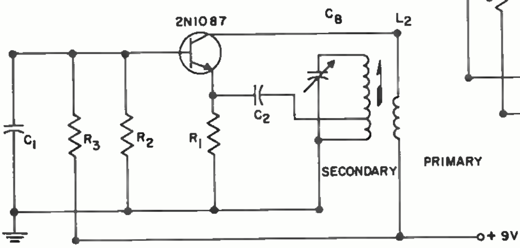


FIGURE 8.2

The operation of the oscillator section (8.2) is as follows:

Random noise produces a slight variation in base current which is subsequently amplified to a larger variation of collector current. This A.C. signal in the primary of L_2 induces an A.C. current into the secondary of L_2 tuned by C_B to the desired oscillator frequency. C_2 then couples the resonant frequency signal back into the emitter circuit. If the feedback (tickler) winding of L_2 is properly phased the feedback will be positive (regenerative) and of proper magnitude to cause sustained oscillations. The secondary of L_2 is an auto-transformer to achieve proper impedance match between the high impedance tank circuit of L_2 and the relatively low impedance of the emitter circuit.

C_1 effectively bypasses the biasing resistors R_2 and R_3 to ground, thus the base is A.C. grounded. In other words, the oscillator section operates essentially in the grounded base configuration.

The operation of the mixer section (8.3) is as follows:

The ferrite rod antenna L_1 exposed to the radiation field of the entire frequency spectrum is tuned by C_A to the desired frequency (broadcast station).

The transistor is biased in a relatively low current region, thus exhibiting quite non-linear characteristics. This enables the incoming signal to mix with the oscillator signal present, creating signals of the following four frequencies:

1. *The local oscillator signal.*
2. *The received incoming signal.*
3. *The sum of the above two.*
4. *The difference between the above two.*

The IF load impedance T_1 is tuned here to the difference between the oscillator and incoming signal frequencies. This frequency is called the intermediate frequency (I.F.) and is conventially 455 KC/S. This frequency will be maintained fixed since C_A and C_B are mechanically geared (ganged) together. R_4 and C_3 make up a filter to prevent undesirable currents flowing through the collector circuit. C_2 essentially bypasses the biasing and stabilizing resistor R_1 to ground. Since the emitter is grounded and the incoming signal injected into the base, the mixer section operates in the "grounded emitter" configuration.

IF AMPLIFIERS

A typical circuit for a transistor IF amplifier is shown by Figure 8.4.

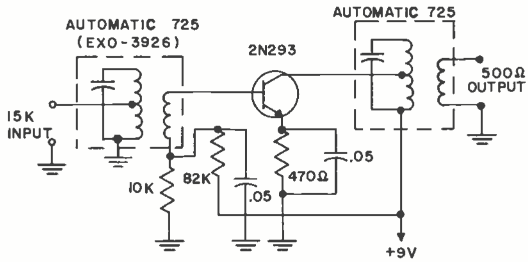


FIGURE 8.4

The collector current is determined by a voltage divider on the base and a large resistance in the emitter. The input and output are coupled by means of tuned IF transformers. The .05 capacitors are used to prevent degeneration by the resistance in the emitter. The collector of the transistor is connected to a tap on the output transformer to provide proper matching for the transistor and also to make the performance of the stage relatively independent of variations between transistors of the same type. With a rate-grown NPN transistor such as the 2N293, it is unnecessary to use neutralization to obtain a stable IF amplifier. With PNP alloy transistors, it is necessary to use neutralization to obtain a stable amplifier and the neutralization capacitor depends on the collector capacitance of the transistor. The gain of a transistor IF amplifier will decrease if the emitter current is decreased. This property of the transistor can be used to control the gain of the IF amplifier so that weak stations and strong stations will produce the same audio output from a radio. Typical circuits for changing the gain of an IF amplifier in accordance with the strength of the received signal are explained in the A.V.C. section of this chapter.

AUTOMATIC VOLUME CONTROL CIRCUITS

A.V.C. is a system which automatically varies the total amplification of the signal in a radio receiver with changing strength of the received signal carrier wave.

From the definition given, it would be correctly inferred that a more exact term to describe the system would be automatic gain control (A.G.C.).

Since broadcast stations are at different distances from a receiver and there is a great deal of variation in transmitted power from station-to-station, the field strength around a receiver can vary by several orders of magnitude. Thus, without some sort of automatic control circuit, the output power of the receiver would vary considerably when tuning through the frequency band. It is the purpose of the A.V.C. or A.G.C. circuit to maintain the output power of the receiver constant for large variations of signal strengths.

Another important purpose of this circuit is its so-called "anti-fading" properties. The received signal strength from a distant station depends on the phase and amplitude relationship of the ground wave and the sky wave. With atmospheric changes this relationship can change, yielding a net variation in signal strength. Since these changes may be of periodic and/or temporary nature, the A.V.C. system will maintain the average output power constant without constantly adjusting the volume control.

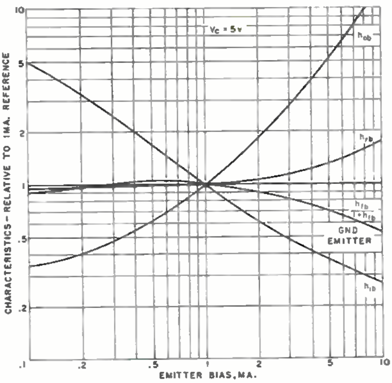
The A.V.C. system consists of taking, at the detector, a voltage proportional to the incoming carrier amplitude and applying it as a negative bias to the controlled amplifier thereby reducing its gain.

In tube circuits the control voltage is a negative going DC grid voltage creating a loss in transconductance (Gm).

In transistor circuits various types of A.V.C. schemes can be used:

EMITTER CURRENT CONTROL

As the emitter current of a transistor is reduced (from 1.0 ma to .1 ma for instance) various parameters change considerably (see Figure 8.5).



CHARACTERISTICS VS. EMITTER CURRENT

FIGURE 8.5

The effect of these changes will be twofold:

1. *A change in maximum available gain and*
2. *A change in impedance matching since it can be seen that both* h_{ob} *and* h_{ib} *vary radically.*

Therefore, a considerable change in power gain can be obtained as shown by Figure 8.6.

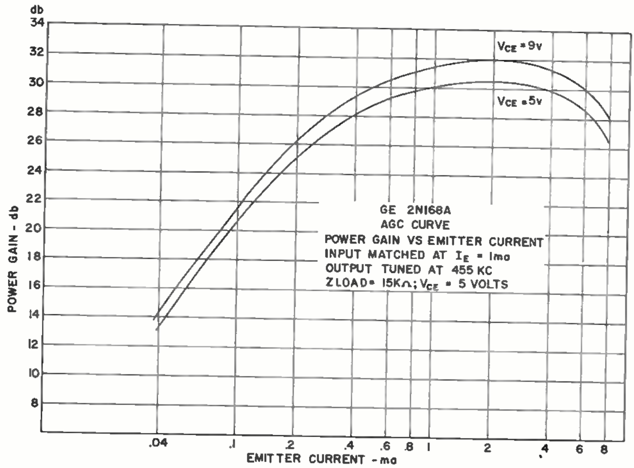


FIGURE 8.6

On the other hand, as a result of I_{co} (collector leakage current) some current always flows, thus a transistor can be controlled only up to a point and cannot be "cut-off" completely. This system yields generally fair control and is, therefore, used more than others. For performance data see Figure 8.7.

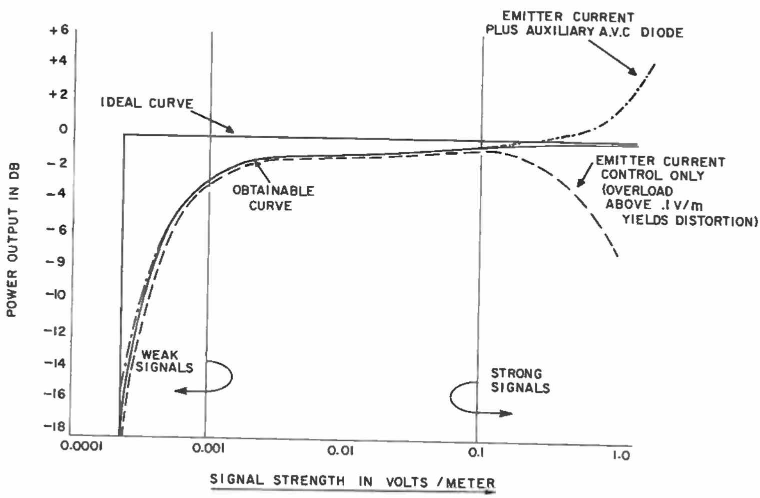


FIGURE 8.7

AUXILIARY A.V.C. SYSTEMS

Since most A.V.C. systems are somewhat limited in performance, to obtain improved control, auxiliary diode A.V.C. is sometimes used. The technique used is to shunt some of the signal to ground when operating at high signal levels, as shown by Figure 8.8.

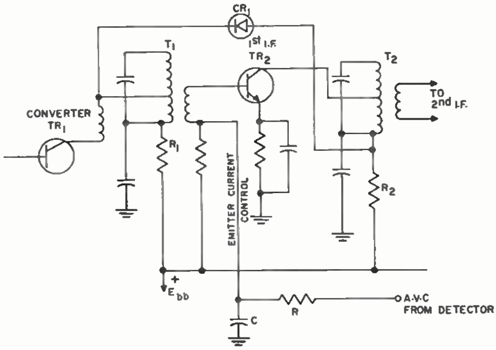


FIGURE 8.8

In the circuit of Figure 8.8 diode CR_1 is back-biased by the voltage drops across R_1 and R_2 and represents a high impedance across T_1 at low signal levels. As the signal strength increases, the conventional emitter current control A.V.C. system creates a bias change reducing the emitter current of the controlled stage. This current reduction coupled with the ensuing impedance mismatch creates a power gain loss in the stage. As the current is further reduced, the voltage drop across R_2 becomes smaller thus changing the bias across CR_1. At a predetermined level CR_1 becomes forward biased, constituting a low impedance shunt across T_1 and creating a great deal of additional A.V.C. action. This system will generally handle high signal strengths as can be seen from Figure 8.7. Hence, almost all radio circuit diagrams in the circuit section of this manual use this system in addition to the conventional emitter current control.

DETECTOR STAGE

In this stage (see Figure 8.9), use is made of a slightly forward biased diode in order to operate out of the square law detection portion of the I-E characteristics. This stage is also used as source of AGC potential derived from the filtered portion of the signal as seen across the volume control (R9). This potential, proportional to the signal level, is then applied through the AGC filter network C4, R7 and C5 to the base of the 1st IF transistor in a manner to decrease collector current at increasing signal levels. R8 is a bias resistor used to fix the quiescent operating points of both the 1st IF and the detector stage, while C6 couples the detected signal to the audio amplifier. (See Chapter 6 on Audio Amplifiers.)

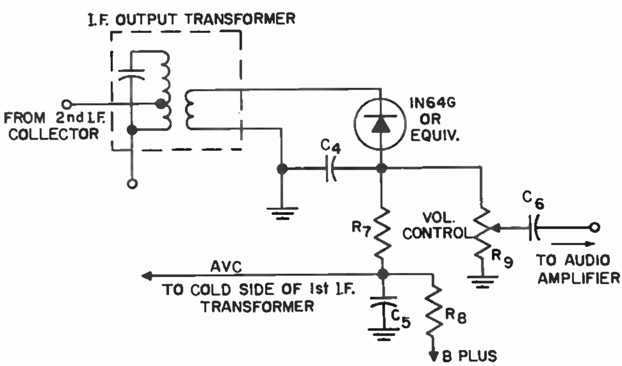
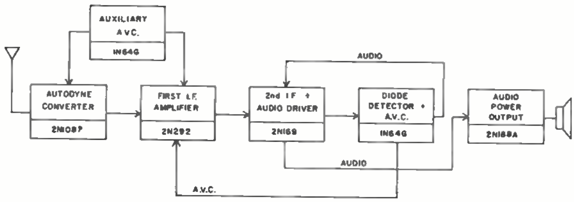


FIGURE 8.9

REFLEX CIRCUITS

"A reflex amplifier is one which is used to amplify at two frequencies – usually intermediate and audio frequencies."*

The system consists of using an I.F. amplifier stage and after detection to return the audio portion to the same stage where it is then amplified again. Since in Figure 8.10,



BLOCK DIAGRAM OF RECEIVER

FIGURE 8.10

two signals of widely different frequencies are amplified, this does not constitute a *"regenerative effect"* and the input and output loads of these stages can be split audio – I.F. loads. In Figure 8.11, the I.F. signal (455 Kc/s) is fed through T2 to the detector circuit CR1, C3 and R5. The detected audio appears across the volume control R5 and is returned through C4 to the cold side of the secondary of T1.

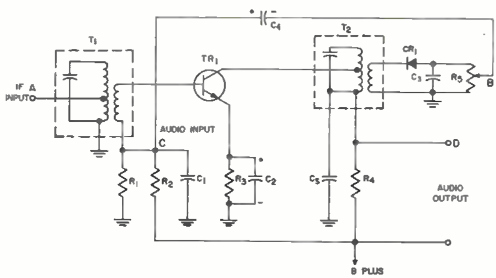


FIGURE 8.11

Since the secondary only consists of a few turns of wire, it is essentially a short circuit at audio frequencies. C1 bypasses the I.F. signal otherwise appearing across the parallel combination of R1 and R2. The emitter resistor R3 is bypassed for both audio and I.F. by the electrolytic condenser C2. After amplification, the audio signal appears across R4 from where it is then fed to the audio output stage. C5 bypasses R4 for I.F. frequencies and the primary of T2 is essentially a short circuit for the audio signal.

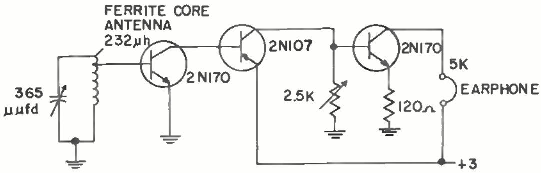
The advantage of "reflex" circuits is that one stage produces gain otherwise requiring two stages with the resulting savings in cost, space, and battery drain. The disadvantages of such circuits are that the design is considerably more difficult, although once a satisfactory receiver has been designed, no outstanding production difficulties should be encountered. Other disadvantages are a somewhat higher amount of playthrough (i.e. signal output with volume control at zero setting), and a minimum volume effect. The latter is the occurrence of minimum volume at a volume control setting slightly higher than zero. At this point, the signal is distorted due to the balancing out of the fundamentals from the normal signal and the out-of-phase playthrough component. Schematics of complete radios are on pages 73 through 83.

* F. Langford-Smith, Radiotron Designers Handbook, Australia, 1953, p. 1140

COMPLETE RADIO RECEIVER CIRCUIT DIAGRAMS

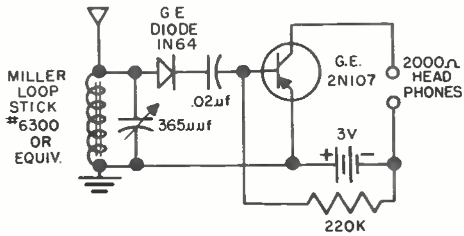
DIRECT COUPLED VEST POCKET RADIO

FIGURE 8.12



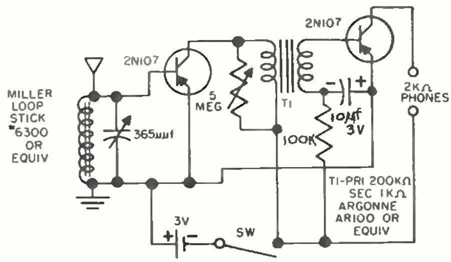
SIMPLE RADIO RECEIVER

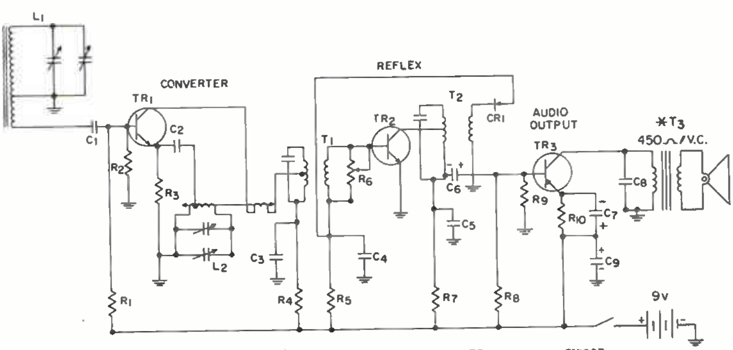
FIGURE 8.13



TWO TRANSISTOR RADIO RECEIVER

FIGURE 8.14





R1 — 47,000 OHMS
R2 — 10,000 OHMS
R3, R7 — 1500 OHMS
R4 — 270 OHMS
R5 — 33,000 OHMS
R6 — 2,000 OHMS VOLUME CONTROL
R8 — 1000 OHMS
R9 — 4700 OHMS
R10 — 100 OHMS

C1 — .02µf
C2 — .01 µf
C3 — 01 µf
C4 — .01 µf
C5 — 002µf
C6 — 5µf - 12V
C7 — 50µf - 3V
C8 — .05µF
C9 — 50µfd-12V

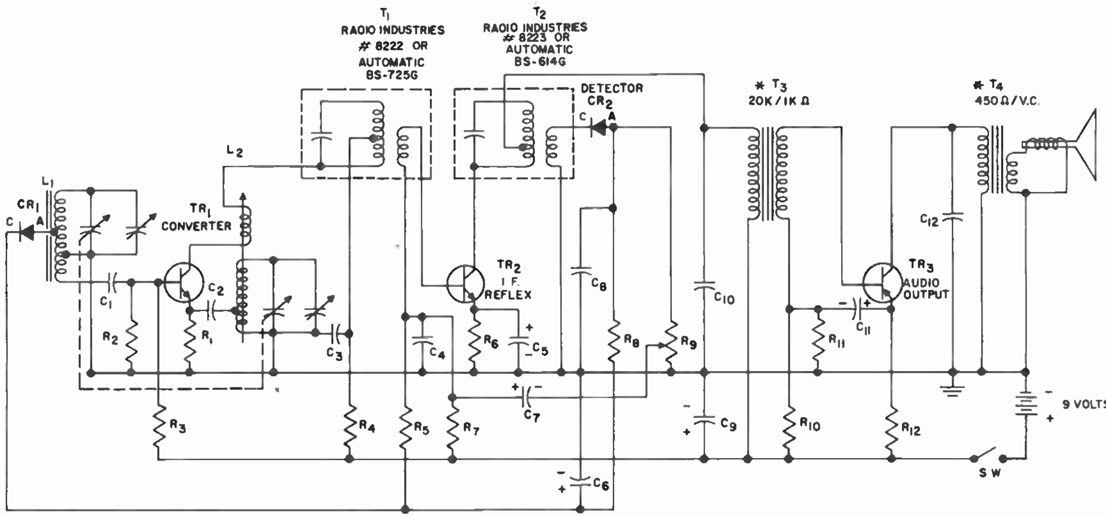
TR1 — 2N1087
TR2 — 2N1121 OR 2N1087 CR1 IN64G OR EQUIV.
TR3 — 2N241A OR 2N321
T1 — AUTOMATIC BS725G OR RADIO INDUSTRIES # 8222
T2 — AUTOMATIC BS614G OR RADIO INDUSTRIES # 8223

NOMINAL SENSITIVITY: 20 MILLIVOLTS/METER
(MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT. 75 MILLIWATTS
SELECTIVITY AT -6db: 10 KC/S
SELECTIVITY AT -60db: 120 KC/S
TOTAL BATTERY DRAIN: 19 MILLIAMPS

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 226

THREE TRANSISTOR REFLEX RECEIVER

FIGURE 8.15



R1, — 1500 OHM
R2, R5, R8, — 10,000 OHM
R3, — 47,000 OHM
R4, — 270 OHM
R6, — 330 OHM
R7, — 330,000 OHM
R9, — VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER
R10, — 1000 OHM
R11, — 4700 OHM
R12 — 100 OHM

C1, C4, C8, — .02 μfd
C2, C3, — .01 μfd
C5, C11, — 50 μfd, 3V
C6, — 15 μfd, 12V
C7, — 6 μfd, 6V
C9, — 50 μfd, 12V
C10, — .002 μfd,
C12, — 0.1 μfd
TR1, — G.E. 2N1087 CONVERTER
TR2, — G.E. 2N1087 OR 2N1121 REFLEX
TR3, — G.E. 2N241A AUDIO OR 2N321

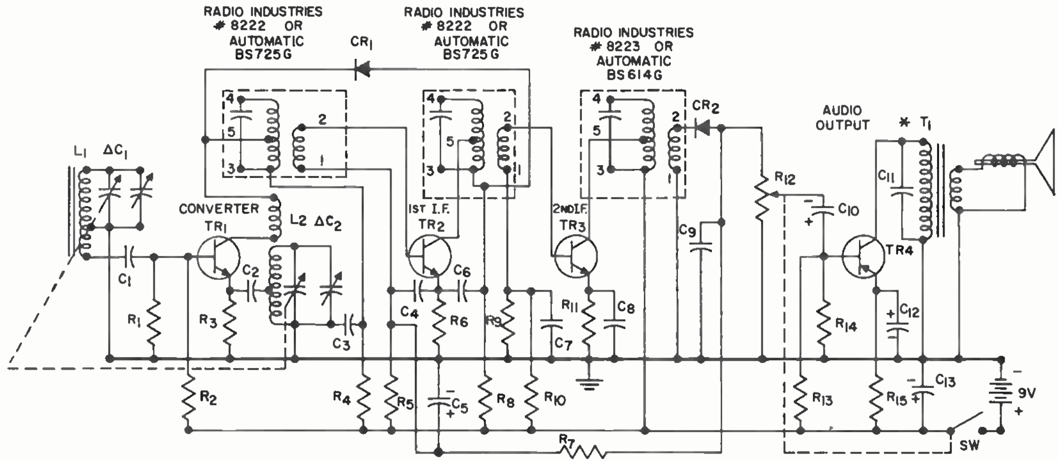
L1, — 435 μh ± 10%
L2, — 250 μh ± 10%
CR1, CR2, — IN64G OR EQUIV.
ΔC1 — 190.6 } R/C MODEL 242
ΔC2 — 69.3 }

NOMINAL SENSITIVITY: 600 MICROVOLTS/METER
(MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT: 75 MILLIWATTS
SELECTIVITY AT -6db : 10 KC/S
SELECTIVITY AT -60db : 120 KC/S
TOTAL BATTERY DRAIN : 17.5 MILLIAMPS

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 226

THREE TRANSISTOR REFLEX RECEIVER

FIGURE 8.16



R_1, R_7, R_9, — 10,000 OHM
R_{12}, — VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER
R_2 — 27,000 OHM
R_3 — 1500 OHM
R_4, R_{11}, — 470 OHM
R_5, — 39,000 OHM
R_6, — 330 OHM
R_8, — 1800 OHM
R_{10}, — 68,000 OHM
R_{13}, — 1000 OHM
* R_{14}, — 5600 OHM
* R_{15}, — 68 OHM
* T_1, — 500 Ω/V.C.
* ΔC_1, — 190.6 } R/C MODEL 242
* ΔC_2, — 89.3 }

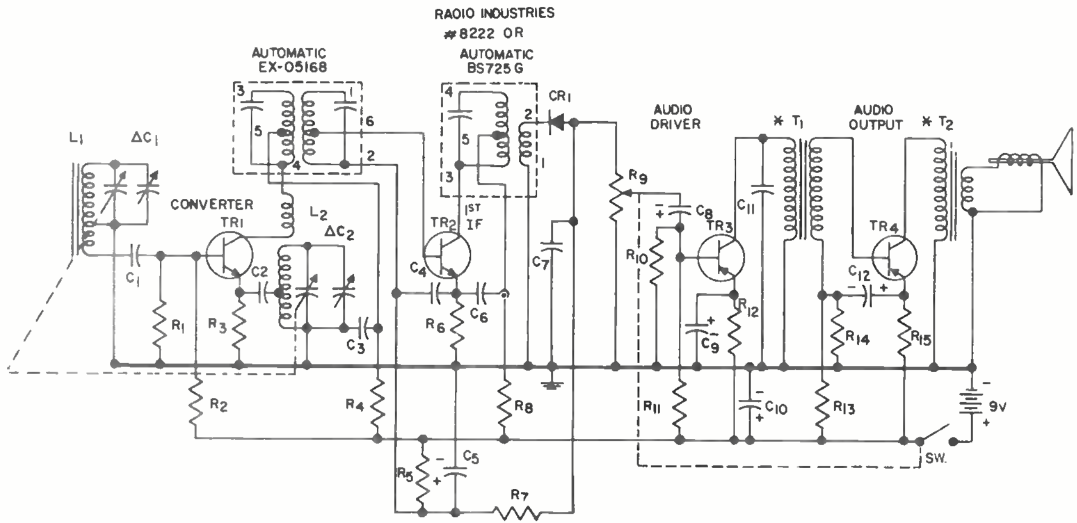
C_1, — .02 μfd
C_2, C_3, — .01 μfd
C_4, C_6, C_7, C_8, C_9, — .05 μfd
C_5, — 15 μfd, 12V
C_{10}, — 6 μfd, 12V
C_{11}, — .1 μfd
C_{12}, — 100 μfd, 12V
C_{13}, — 50 μfd, 12V
TR_1, — G.E. 2N1087 CONVERTER
TR_2, TR_3, — G.E. 2N293 IST & 2ND I.F.
TR_4, — G.E. 2N241A OR 2N321 AUDIO
* L_1, — 435 μh, ±10%
* L_2, — 250 μh, ±10%
CR_1, CR_2, — DR117, IN64G, OR CK706A OR EQUIV.

NOMINAL SENSITIVITY ; 500 MICROVOLTS / METER (MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)	
MAXIMUM POWER OUTPUT	: 75 MILLIWATTS
SELECTIVITY AT -6db	: 8.0 KC/S
SELECTIVITY AT -60db	: 65.0 KC/S
TOTAL BATTERY DRAIN	: 20.0 MILLIAMPS.

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 226

FOUR TRANSISTOR SUPERHETERODYNE BROADCAST RECEIVER

FIGURE 8.17



R_1, ——— 6800 OHM
R_2, ——— 27,000 OHM
R_3, ——— 1500 OHM
R_4, R_8, ——— 470 OHM
R_5, ——— 120,000 OHM
R_6, ——— 330 OHM
R_7, ——— 12,000 OHM
R_{10}, ——— 47,000 OHM
R_{11} ——— 10,000 OHM
R_{12}, R_{13}, ——— 1000 OHM
R_{14}, ——— 5600 OHM
R_{15}, ——— 68 OHM
R_9, ——— VOLUME CONTROL 10,000 Ω 1/2W AUDIO TAPER
* L_1, ——— 435 μh ±10%
* L_2, ——— 250 μh ±10%

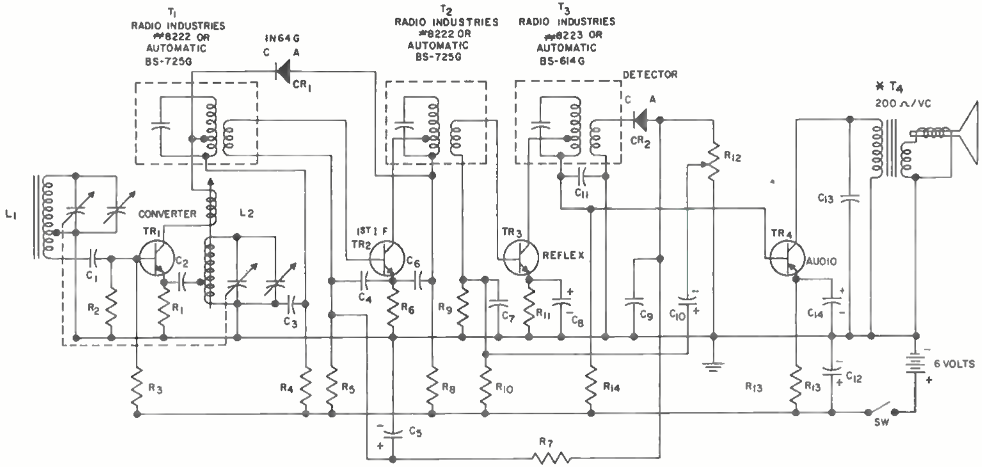
C_1, C_4, C_6, ——— .05μfd
C_2, C_3, ——— .01μfd
C_5, ——— 15μfd, 12V
C_7, C_{11}, ——— .02μfd,
C_8, ——— 6μfd, 12V
C_9, C_{10}, C_{12}, ——— 50μfd, 12V
CR_1, ——— DR117, IN64G, OR CK706A OR EQUIV
TR_1 ——— G.E. 2N1087 CONVERTER
TR_2 ——— G.E. 2N293 I.F.
TR_3 ——— G.E. 2N192 OR 2N324 DRIVER
TR_4 ——— G.E. 2N241A OR 2N321 AUDIO
* T_1 ——— 20KΩ/600Ω
* T_2 ——— 500 Ω/V.C.
* ΔC_1, ——— 190.6 } R/C MODEL 242
* ΔC_2, ——— 89.3 } R/C MODEL 242

NOMINAL SENSITIVITY : 300 MICROVOLTS / METER
(MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT : 75 MILLIWATTS
SELECTIVITY AT -6 db : 8.0 KC/S
SELECTIVITY AT -60 db : 65.0 KC/S
TOTAL BATTERY DRAIN : 18.0 MILLIAMPS

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 226

FOUR TRANSISTOR SUPERHETERODYNE BROADCAST RECEIVER

FIGURE 8.18



R_1	1500 OHM	C_1, C_{11}	.02 μfd
R_2, R_9	10,000 OHM	C_2, C_3, C_7	.01 μfd
R_3	15,000 OHM	C_4, C_6, C_9	.05 μfd
R_4	270 OHM	C_5	15 μfd, 12 V
R_5	56,000 OHM	C_8	50 μfd, 3 V
R_6	330 OHM	C_{10}	6 μfd, 12 V
R_7	3300 OHM	C_{12}	50 μfd, 12 V
R_8	1800 OHM	C_{13}	0.1 μfd
R_{10}	68,000 OHM	C_{14}	100 μfd, 12 V
R_{11}	470 OHM	TR_1	2N1086A, 2N1086 OR 2N1087 CONVERTER
R_{12}	VOLUME CONTROL 10,000 OHM ½ W AUDIO TAPER	TR_2	2N292 IST I.F.
R_{13}	39 OHM	TR_3	2N169 OR 2N1121 REFLEX
R_{14}	1000 OHM	TR_4	2N241A OR 2N321 AUDIO

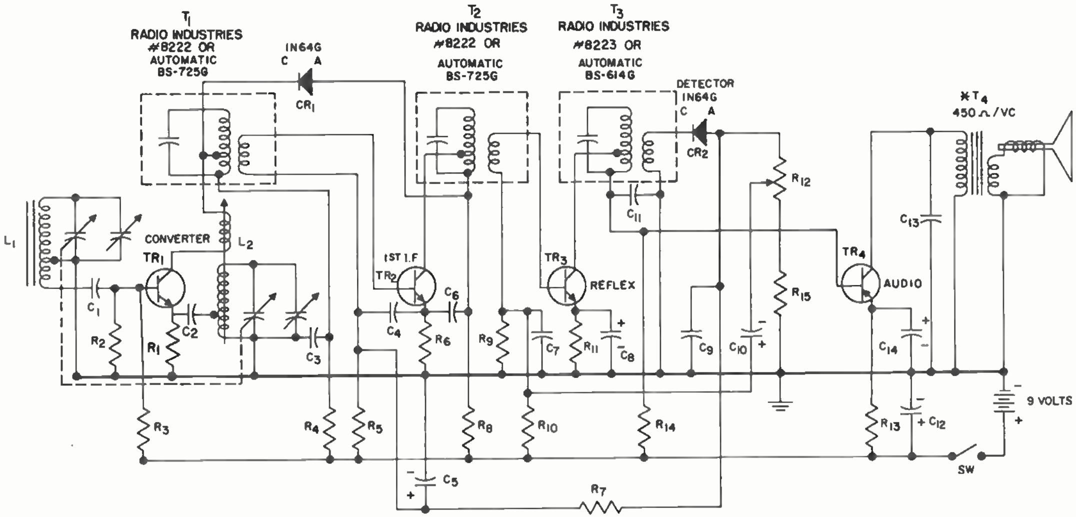
L_1 ——— 435 μh ± 10%
L_2 ——— 250 μh ± 10%
CR_1, CR_2 ——— IN64G OR EQUIV.
ΔC ——— 190.6 } R/C MODEL 242
ΔC ——— 89.3 }

NOMINAL SENSITIVITY: 150 MICROVOLTS/METER
(MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT.)
MAXIMUM POWER OUTPUT: 75 MILLIWATTS
SELECTIVITY AT -6db : 8.0 KC/S
SELECTIVITY AT -60db : 65.0 KC/S
TOTAL BATTERY DRAIN : 25.0 MILLIAMPS

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 226

FOUR TRANSISTOR SIX VOLT REFLEX RECEIVER

FIGURE 8.19



R1, R4, — 1500 OHM
R2, — 6800 OHM
R3, — 27,000 OHM
R4, R11, — 470 OHM
R5, — 82,000 OHM
R6, — 330 OHM
R7, R8 — 3300 OHM
R9, — 10,000 OHM
R10, — 91,000 OHM
R12, — VOLUME CONTROL 10,000 OHM AUDIO TAPER
R13, — 100 OHM
R15, — 120 OHM

C1, C11, — .02 μfd
C2, C3, C7, — .01 μfd
C4, C6, C9, C13 — .05 μfd
C5, — 15 μfd, 12V
C8, — 50 μfd, 3V
C10, — 6 μfd, 12V
C12, — 50 μfd, 12V
C14, — 100 μfd, 12V
TR1, — 2N1086A, 2N1087 CONVERTER OR 2N1086
TR2, — 2N292 1ST I.F.
TR3, — 2N169 REFLEX
TR4, — 2N188A OR 2N320 AUDIO

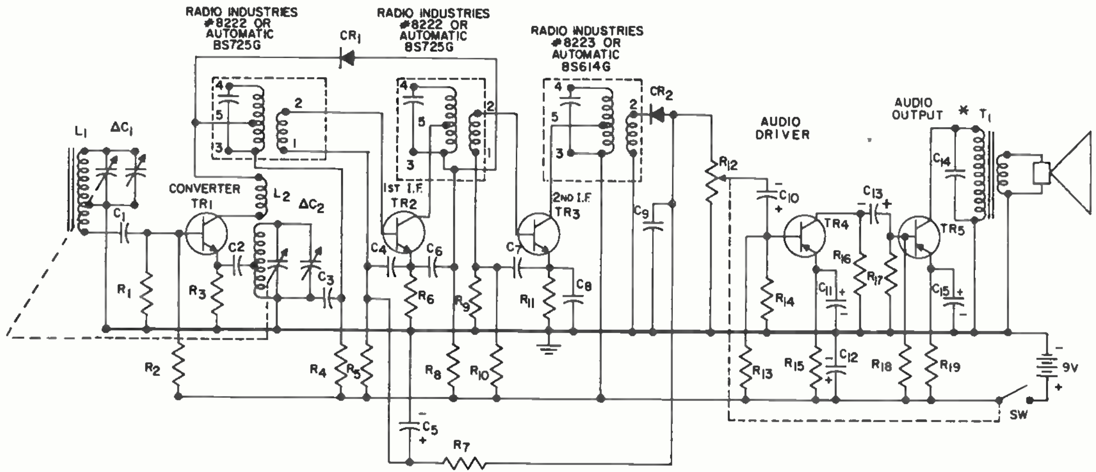
L1, — 435 μh ± 10%
L2, — 250 μh ± 10%
CR1, CR2, — IN64G OR EQUIV.
ΔC1 — 190.6 } R/C MODEL 242
ΔC2 — 89.3 }

NOMINAL SENSITIVITY: 200 MICROVOLTS/METER
(MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT: 75 MILLIWATTS
SELECTIVITY AT -6db : 8.0 KC/S
SELECTIVITY AT -60db : 60.0 KC/S
TOTAL BATTERY DRAIN : 17.0 MILLIAMPS

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 226

FOUR TRANSISTOR NINE VOLT REFLEX RECEIVER

FIGURE 8.20



R1, — 6800 OHM
R2, — 27,000 OHM
R3, — 1500 OHM
R4, R11, R15, — 470 OHM
R5, — 68,000 OHM
R6, — 330 OHM
R7, — 2700 OHM
R8, R16, — 3300 OHM
R9 — 10,000 OHM
R10, — 82,000 OHM
R12, — VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER
R13, — 4700 OHM
R14, — 56,000 OHM
R17, — 5600 OHM
R18, — 1000 OHM
R19, — 68 OHM

C1, — .02 μfd
C2, C3, — .01 μfd
C4, C6, C7, C8, C9, C14, — .05 μfd
C5, — 15 μfd, 12V
C10, C13, — 6 μfd, 12V
C11, C15, — 100 μfd, 12V
C12, — 50 μfd, 12V
TR1, — G.E. 2N1086A, 2N1086 OR 2N1087 CONVERTER
TR2, — G.E. 2N293 1ST I.F.
TR3, — G.E. 2N169 2ND I.F.
TR4, — G.E. 2N265 DRIVER OR 2N508
TR5, — G.E. 2N188A OR 2N320 OUTPUT
* T1, — 500 Ω/VC
L1, — 435 μh ± 10%
L2, — 250 μh ± 10%
CR1, CR2, — DR117, 1N64G OR CK706A

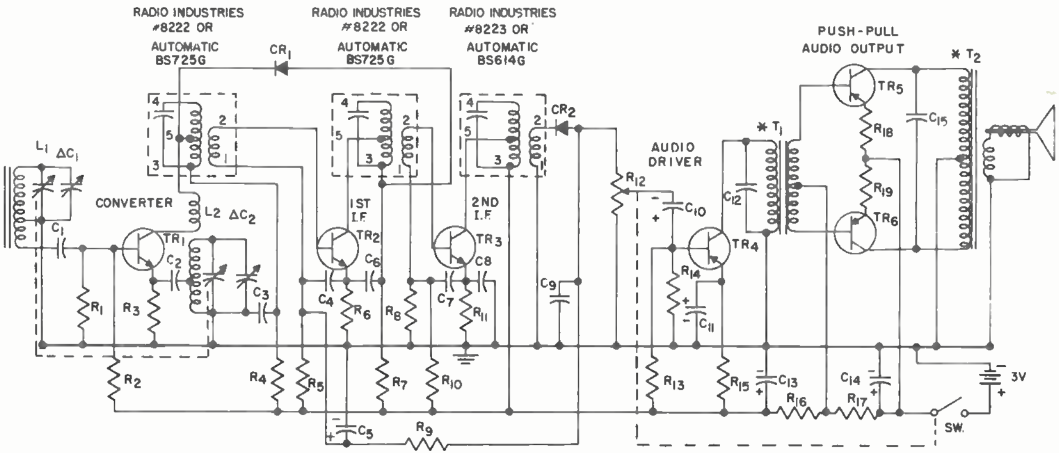
ΔC1, — 190.6
ΔC2, — 89.3
} R/C MODEL 242

NOMINAL SENSITIVITY : 150 MICROVOLTS/METER
(MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT : 75 MILLIWATTS.
SELECTIVITY AT -6db : 8.0 KC/S.
SELECTIVITY AT -60db: 65.0 KC/S.
TOTAL BATTERY DRAIN: 18.0 MILLIAMPS.

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 226

FIVE TRANSISTOR SUPERHETERODYNE BROADCAST RECEIVER

FIGURE 8.21



R1, R8, — 10,000 OHM
R2, — 33,000 OHM
R3, R11, — 470 OHM
R4, — 270 OHM
R5, — 12,000 OHM
R6, — 330 OHM
R7, — 1500 OHM
R9, — 2700 OHM
R10, — 18,000 OHM
R13, — 4700 OHM
R14, — 15,000 OHM
R15, — 390 OHM
R16, — 100 OHM
R17, — 39 OHM
R18, R19, — 5.0 OHM
R12, — VOLUME CONTROL 10,000 OHM 1/2 W AUDIO TAPER

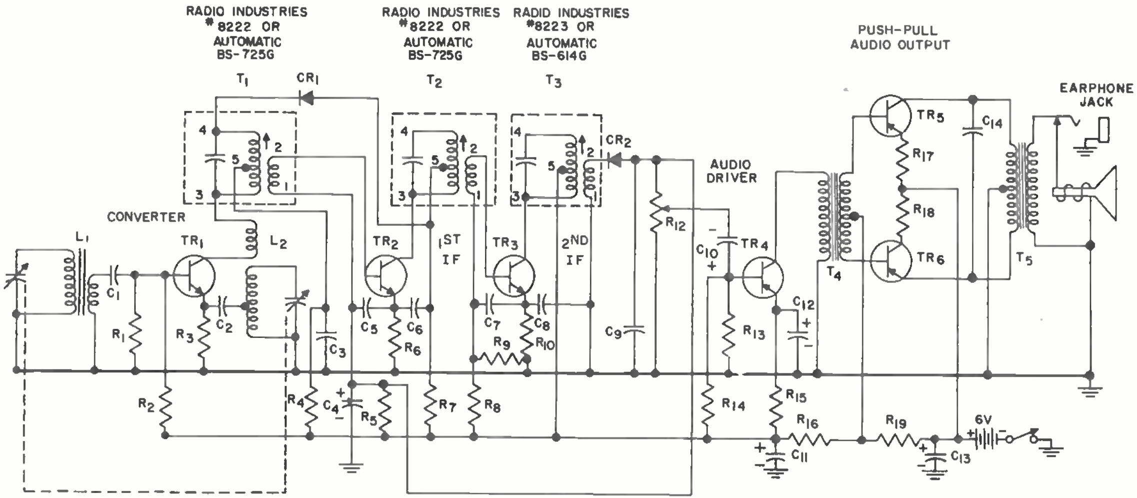
C1, — .02μfd
C12 — .003μfd
C2, C3, — .01μfd
C4, C6, C7, C8, C9, — .05μfd
C5, C10, — 6μfd, 6V
C11, C13, C14, — 50μfd, 6V
C15, — 0.1μfd
TR1 — G.E. 2N1087 CONVERTER
TR2 — G.E. 2N293 1ST I.F.
TR3 — G.E. 2N1121 2ND I.F.
TR4 — G.E. 2N192 2N324 DRIVER
TR5, TR6, — G.E. 2N188A OR 2N320
* T1 — 2600/2600 Ω CT.
* T2 — 300 Ω CT/VC
* L1, — 435μh ± 10%
* L2, — 250μh ± 10%
CR1, CR2, — DR117, IN64G, OR CK706A OR EQUIV.
* ΔC1, — 190.6 } R/C MODEL 242
* ΔC2, — 89.3 }

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 226

NOMINAL SENSITIVITY: 250 MICROVOLTS / METER
(MEASURED WITH 5 MW REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT: 100 MILLIWATTS.
SELECTIVITY AT -6db: 8.0 KC/S
SELECTIVITY AT -60db: 65.0 KC/S
ZERO SIGNAL BATTERY DRAIN: 7.0 MILLIAMPS.

SIX TRANSISTOR THREE VOLT BROADCAST RECEIVER
CAN BE POWERED BY SUN OR FLASHLIGHT BATTERIES

FIGURE 8.22



R_1, R_8,	10,000 OHM
R_2,	15,000 OHM
R_3,	150D OHM
R_4,	270 OHM
R_5,	47,000 OHM
R_6,	220 OHM
R_7, R_9,	2200 OHM
R_{10},	1000 OHM
R_{11}, R_{14},	4700 OHM
R_{12},	VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER
R_{13},	68,000 OHM
R_{15},	470 OHM
R_{16},	100 OHM
R_{17}, R_{18},	8.2 OHM
R_{19},	33 OHM

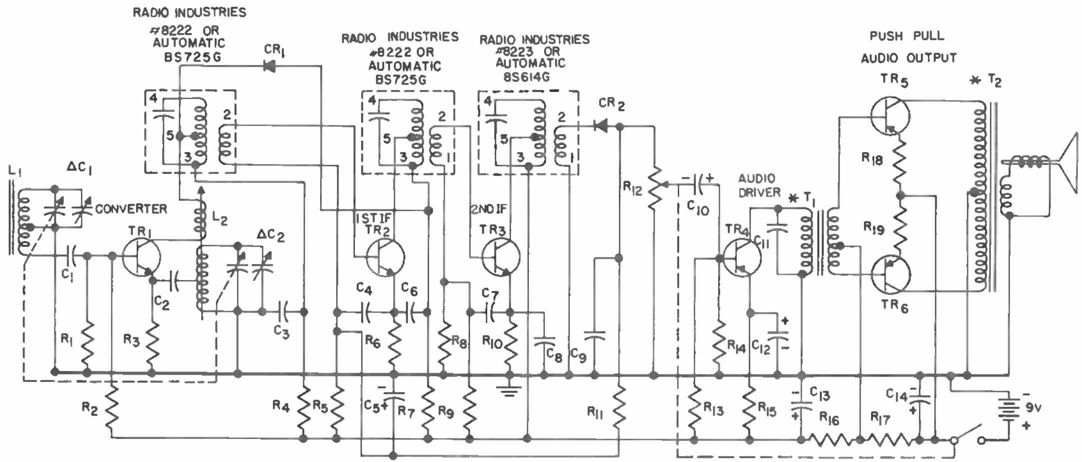
C_1,	.02 μfd.
$C_2, C_3, C_5, C_6, C_7, C_8$,	.01μ fd.
C_4, C_{10},	6μfd. -6V
C_9,	.05μfd.
C_{11}, C_{12}, C_{13},	50μfd.-12V
C_{14},	.2μfd.
CR1, CR2,	IN64G OR EQUIV
TR_1,	G.E. 2N1087
TR_2,	G.E. 2N293
TR_3,	G.E. 2N169 OR 2N1121
TR_4,	G.E. 2N192 OR 2N324
TR_5, TR_6,	G.E. 2N188A OR 2N320

* T_4 = 3600Ω/2000Ω CT
* T_5 = 360Ω CT/VC

* FOR FURTHUR INFORMATION SEE PAGE 226

NOMINAL SENSITIVITY: 200 MICRO VOLTS/METER
(MEASURED WITH 50 MILLIWATTS REFERENCE POWER)
MAXIMUM POWER OUTPUT: 200 MW
SELECTIVITY AT -6 db: 8.0 Kc/S
SELECTIVITY AT -60 db: 60.0 Kc/S
ZERO SIGNAL BATTERY DRAIN: 8 MILLIAMPS

SIX TRANSISTOR SIX VOLT BROADCAST RECEIVER
FIGURE 8.23



R_1, ———— 6800 OHM
R_2, ———— 27,000 OHM
R_3, ———— 1500 OHM
R_4, R_{10}, R_{15}, – 470 OHM
R_5, ———— 68,000 OHM
R_6, ———— 330 OHM
R_7, ———— 3300 OHM
R_8, ———— 10,000 OHM
R_9, ———— 82,000 OHM
R_{11}, ———— 2700 OHM
R_{12}, ———— VOLUME CONTROL
10,000 OHM 1/2W AUDIO TAPER
R_{13}, ———— 4700 OHM
R_{14}, ———— 56,000 OHM
R_{16}, ———— 220 OHM
R_{17}, ———— 33 OHM

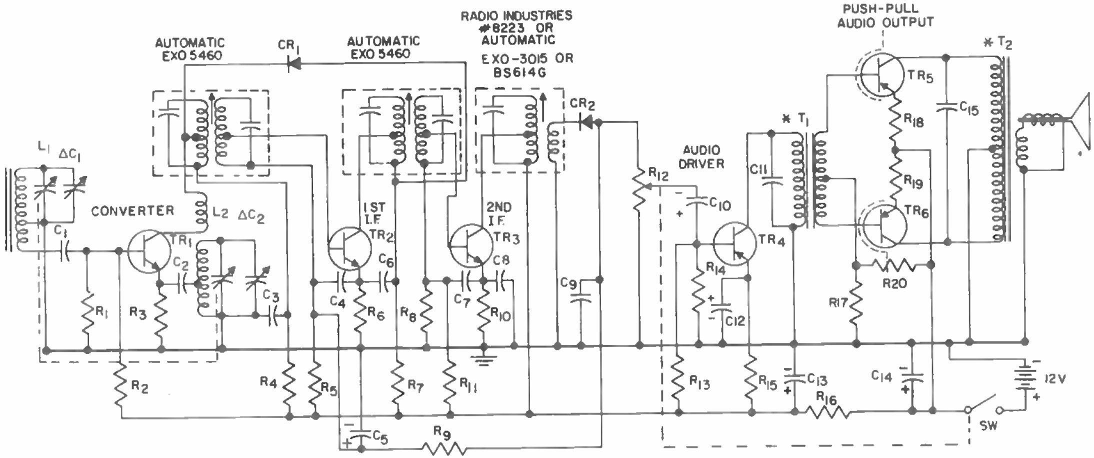
R_{18}, R_{19}, —— 8.2 OHM
C_1, ———— .02 μfd
C_2, C_3, —— .01 μfd
C_4, C_6, C_7, C_8, – .05 μfd
C_5, C_{10}, —— 6 μfd, 12V
C_9, ———— .05 μfd
C_{11}, ———— .003 μfd
C_{12}, C_{13}, C_{14}, – 50 μfd, 12V
TR_1, ———— G.E. 2N1087 CONVERTER
TR_2, ———— G.E. 2N293 1ST I.F.
TR_3, ———— G.E. 2N169 OR 2N1121 2ND IF
TR_4, ———— G.E. 2N192 OR 2N324 DRIVER
TR_5, TR_6, —— G.E. 2N188A OR 2N320 AUDIO
* T_1, ———— 5,000 / 2600Ω CT
* T_2, ———— 250 Ω CT/V.C.

* L_1 ———— 435 μh ±10%
* L_2 ———— 250 μh ±10%
CR_1, CR_2, — DR117, IN64G, OR CK706A OR EQUIV.
* ΔC_1, — 190.6 } R/C MODEL 242
* ΔC_2 — 89.3 }

NOMINAL SENSITIVITY = 200 MICROVOLTS / METER
(MEASURED WITH 50 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT .6 WATTS.
SELECTIVITY AT −6db : 8.0 KC/S
SELECTIVITY AT −60db : 60.0 KC/S
ZERO SIGNAL BATTERY DRAIN 7.0 MILLIAMPS

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 226

SIX TRANSISTOR NINE VOLT SUPERHETERODYNE BROADCAST RECEIVER
FIGURE 8.24



R_1, R_{11} — 6800 OHM
R_2 — 33,000 OHM
R_3 — 1500 OHM
R_4, R_{10}, R_{15} — 470 OHM
R_5 — 100,000 OHM
R_6 — 330 OHM
R_7, R_{13} — 4700 OHM
R_8 — 2200 OHM
R_9 — 27,000 OHM
R_{12} — VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER
R_{14} — 15,000 OHM
R_{16} — 220 OHM
R_{17} — 2700 OHM
R_{18}, R_{19} — 10 OHM
R_{20} — 33 OHM

C_1 — .02 μfd
C_2, C_3 — .01 μfd
C_4, C_6, C_7, C_8 — .1 μfd
C_5 — 6 μfd, 12V
C_9 — .05 μfd
C_{10} — 6 μfd, 6V
C_{11} — .003 μfd
C_{12}, C_{13}, C_{14} — 50 μfd, 12V
C_{15} — .2 μfd
TR_1 — G.E. 2N1087 CONVERTER
TR_2 — G.E. 2N293 1ST I.F.
TR_3 — G.E. 2N169 OR 2N1121 2ND I.F.
TR_4 — G.E. 2N192 OR 2N324 DRIVER
TR_5, TR_6 — G.E. 2N241A AUDIO WITH CLIP-ON HEAT SINK (BIRCHER 3AL635-2R OR EQUIV.)

* T_1 — 2000/2600 CT
* T_2 — 200Ω CT/VC
L_1 — 435 μh ± 10%
L_2 — 250 μh ± 10%
ΔC_1 — 190.6, ΔC_2 — 89.3 } R/C MODEL
CR_1, CR_2 — 1N64 OR 1N295 OR EQUIV.

NOMINAL SENSITIVITY . 150 MICROVOLTS/METER (MEASURED WITH 50 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT : 1 WATT
SELECTIVITY AT -6db : 8.0 KC/S
SELECTIVITY AT -60db . 38.0 KC/S
ZERO SIGNAL BATTERY DRAIN : 10 MILLIAMPS

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 226

SIX TRANSISTOR, 12 VOLT 1 WATT RECEIVER

FIGURE 8.25

9. TRANSISTOR RADIO SERVICING TECHNIQUES

The major function of a radio receiver is to pick up modulated electromagnetic energy and transform its intelligence (modulation) into acoustical energy. Most modern receivers are of the "Superheterodyne" type, and consist of an Autodyne Converter or Oscillator-Mixer, one or two stages of IF Amplification, a Detector (which also provides a source of Automatic Volume Control power), and finally, one or more stages of Audio Amplification.

The components making up the AC circuitry of these stages include the antenna, oscillator coil, IF and audio transformers, tuning, coupling or bypass capacitors, and the speaker. Troubles in these components can usually be spotted by a DC test after the trouble area has been located by using signal tracing techniques.

Since the transistor is probably the most reliable component in the receiver, it should be the last component to be suspected. This is contrary to the long established rule of thumb used in tube radios, where the tubes are normally checked first. This is especially true in personal portable receivers using subminiature components, i.e., coils using extremely fine wire, electrolytics of extremely small dimension with low voltage ratings, etc. Because of their reliability, transistors are generally soldered into the circuit in printed circuit transistor radios. Removing and testing each transistor, as usually done in a tube set, will not only unnecessarily subject the transistor to high peak heating, but will probably damage some other component, particularly the printed circuit board.

Now that the ground rules are laid for a trouble-shooting procedure, proceed with it in a logical sequence.

First determine whether the battery voltage *under load* is high enough to operate the receiver. Although most receivers are designed to operate down to one-half the battery voltage, severe distortion, low sensitivity and reduced power output, as well as possible "motorboating", may result from a low supply voltage. Also make a quick visual inspection to locate possible loose, dirty, or intermittent battery, speaker, or antenna connections. The set can now be analyzed further.

The fastest trouble-shooting technique is to inject an appropriate signal into each transistor base going from speaker to antenna. Starting at the audio stages (the volume control, for instance), apply a 400 or 1000 cycle audio signal. If a clean sine-wave with adequate power output appears at the speaker as indicated by an oscilloscope presentation or listening test, both audio circuits and speaker are in operating condition. In this event take an RF/IF generator and apply a 455 Kc/s signal (30% modulation — 400 or 1000 c/s) to the high frequency section of the receiver. As soon as the applied signal is not passed by a stage of amplification, this stage should be investigated on a DC basis. Note: Care must be taken that the generator's leads have a series DC blocking condenser in order not to change the bias condition in the circuit under investigation.

As a first check, it should be determined that both the magnitude and polarity of the supply voltage are appropriately applied. If NPN transistors are used, the collector will be positive with respect to emitter and base. The latter two will be very close voltage-wise, the base being somewhat more positive than the emitter. The opposite polarity applies to PNP transistors.

Figure 9.1 shows collector current vs. base to emitter bias voltage. Notice that a very small increase in V_{BE} produces a large increase in collector current. Thus, there will generally be from .1 to .2 volts between the base and emitter. Either the positive or negative side of the battery may be grounded, especially in sets using both NPN and PNP transistors.

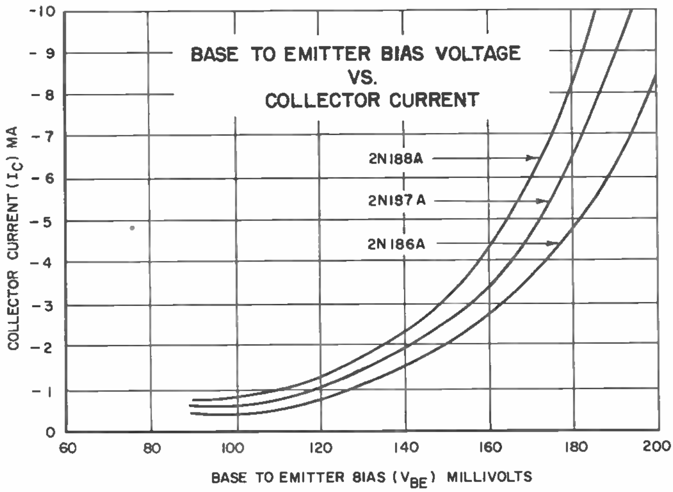


FIGURE 9.1

The next step is to determine bias current. Since base, emitter and collector current are dependent on each other, it generally suffices to measure only one, the collector current for instance. This should be almost equal to the emitter current while the base current, being the difference between the two ($I_B = I_E - I_C$), will generally be very small. Looking at Figure 8.6, it appears that since power gain is maximum between 1.5 and 3.0 ma, most stages will operate in this region. Actually, most RF/IF stages may have operating points down to .5 ma without serious loss of gain. An easy way to measure emitter current in most circuits is to measure to voltage drop across either the emitter resistor or possibly a collector resistor and calculating the current by Ohm's law. For example, if the emitter resistor is 1000 ohms and the measured voltage drop is 1.0 volt then the emitter current is $I = \frac{E}{R} = \frac{1.0}{1000} = .001$ ampere = 1.0 milliamp. The insertion of a milliammeter into the emitter circuit will change the bias in the stage and is not a satisfactory testing technique.

If a stage (with the exception of the output stages) operates considerably below .5 ma or above 3.0 ma, it is fairly certain that the stage is operating improperly. Note: Care should be taken to measure these currents in the absence of signal since in AVC controlled stages, current will vary with signal strength.

In an improperly biased circuit, an ohmmeter check of the resistors and capacitors is in order next. If this fails to isolate the problem, the transistor can be replaced. Since it normally takes highly specialized equipment to test transistors (especially high frequency types) it is more practical to test by substitution.

If the trouble is located in the oscillator section of the converter, an IF signal can be passed through the mixer but an RF signal will not produce the necessary IF to get a signal through. In this case it should be determined at once whether the oscillator is operating at all. In the case of the autodyne converter in Figure 8.1, any AC VTVM, such as the Hewlett-Packard 400C, D, or H, or the Ballantine Models 310-A or 314, is sensitive enough to measure down to 50 mv and can be connected to the emitter of the converter transistor. If these instruments are not available, use a Vacuum Tube Voltmeter such as the Heathkit Model V-7A on the lowest AC-RMS Scale.

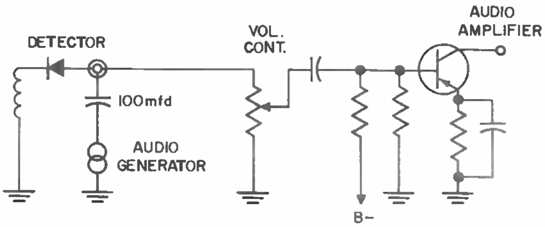
Since the local oscillator operates from .99-2.075 Mc/s, this VTVM should be provided with an RF probe (Heathkit Model 309C or equivalent). The presence or absence of oscillator injection voltage can, however, be determined even without the use of such a probe.

The proper magnitude of oscillation should be somewhere between 50 and 500 mv rms, and oscillation must be present over the entire broadcast band. (This can easily be checked by rotating the variable condenser from end to end.) No voltage at this point indicates the absence of oscillator injection, and an ohmmeter check of the oscillator coil should prove it faulty.

To trouble-shoot or align a transistor radio, it is generally helpful to know how much signal strength should be applied at a given stage in order to evaluate the gain of the receiver. The following is a measurement procedure useable for this purpose.

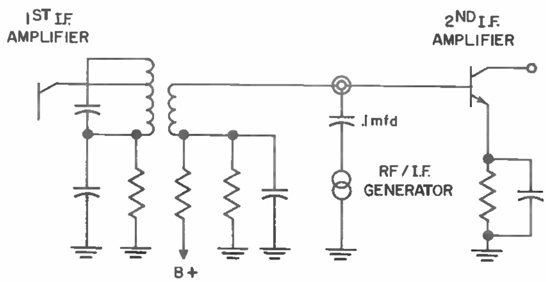
1. An AC VTVM should be connected across the speaker terminals (speaker remaining connected).
2. Applying the signal at any test point, the generator attenuator should be adjusted to get .13 or .4 volts rms reading on the output VTVM. (Since most speaker voice coil impedances are 3.2 ohms, this means that the "reference power output"* is either $P = \frac{V^2}{Z} \cong \frac{.13^2}{3.2} \cong 5$ mw or $P = \frac{.4^2}{3.2} = 50$ mw

   In various subminiature sets, however, the voice coil impedance is about 16 ohms** in which case the reference AC voltage becomes $V = \sqrt{5 \times 10^{-3} \times 16} \approx .28$ volts rms for 5 mw reference and $V = \sqrt{50 \times 10^{-3} \times 16} \approx .89$ volts rms for 50 mw reference.
3. The signal can then be applied to any base as shown in Figures 9.2 and 9.3.



AUDIO STAGE MEASUREMENT

FIGURE 9.2



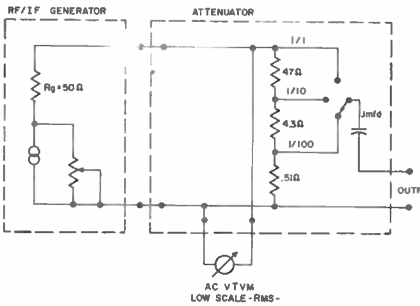
RF/IF STAGE MEASUREMENT

FIGURE 9.3

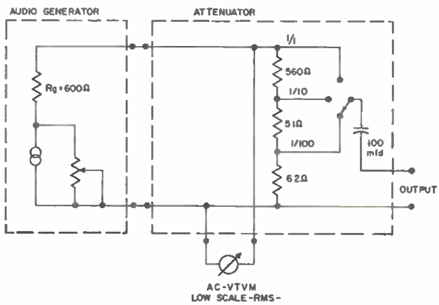
*The "reference power output" is the power output conventionally used to make sensitivity measurements This value is fixed by IRE standard at 5 milliwatts for miniature portable receivers and 50 milliwatts for the larger type portables.

**To determine the voice coil impedance of a speaker, a DC resistance test should yield a value close to the AC impedance of the voice coil, providing the speaker is measured while disconnected from the output transformer. A 3.2 ohm speaker will measure about 2.7 ohms while a 16 ohm speaker measures around 12 ohms in general.

By having a reference power output, it is now possible to read the input voltage at the generator and obtain the receiver sensitivity at this point. The sensitivity, the operational condition, and the quality of the receiver under test can now be assessed. This assumes the use of audio and RF generators having calibrated and metered attenuators (like Heathkit Model LG-1). In the absence of this type of equipment, two very simple attenuators can be built for RF/IF and for audio. See Figures 9.4 and 9.5. The attenuation will permit the injection of small signal into any circuit under test while the relatively unsensitive VTVM measures RMS voltages 10 or 100 times larger.



RF/IF DECADE ATTENUATOR
FIGURE 9.4



AUDIO DECADE ATTENUATOR
FIGURE 9.5

TYPICAL INPUT VOLTAGES FOR REFERENCE OUTPUT

	Audio Output Base	Audio Driver Base	Detector Base	2nd IF Base	1st IF Base	Converter Base
6 Transistor Radio#	150 mv	2.5 mv	50 mv	2.5 mv	50-100 μv	5-10 μv
5 Transistor Radio	20 mv	5.0 mv	50 mv	2.5 mv	50 μv	5-10 μv
4 Transistor Radio	20 mv	.5 mv	5-10 mv	—	200 μv	10-20 μv

#Reference output is 50 mw, all others 5 mw.

It will be found that sensitivitics will vary from set to set because this measurement is only an indication of the order of magnitude of appropriate sensitivities. Even a 5/1 deviation at times can be normal. Deviations larger than 10/1 are strong indications of trouble.

Broadcast Receiver Alignment Procedure:

A conventional set-up procedure is as follows:

a) Connect the output of the IF/RF generator to a radiating loop (Hazeltine #1150 or equivalent).*

*This loop is a calibrated laboratory loop used for accurate sensitivity measurements. Since the purpose here is only to align rather than measure, either an air loop or a ferrite rod antenna may be used as a radiating element. If these are not available either, it often suffices to bring the generator leads close to the receiver's antenna and induce a signal through capacitive coupling.

b) The output meter (AC VTVM) should be connected across the voice coil terminals, the speaker remaining connected.

c) The receiver should be placed one to two feet away from the radiating loop in a plane that optimizes the coupling between the receiving and radiating antennas.

d) Set the volume control of the receiver at maximum volume.

e) Turn the Variable Condenser to the high frequency end of the dial (Gang wide open).

The set is now ready to be aligned.

1. Set the signal generator to 455 Kc/s and at maximum signal output. At this point there should be considerable output from the receiver.

   If the set is operative but does not show enough output, reduce the distance between the receiver antenna and radiating element.

   If the output is much larger than the standard reference value (.4 volts across 3.2 ohms $\approx$ 50 mw), reduce the output of the signal generator.

2. Peak the last IF transformer, then the interstage IF transformer, and finally the 1st IF transformer while maintaining an output voltage close to the reference value by gradually reducing the signal generator output voltage.

3. Repeat the same operation going from the 1st IF to the last IF this time. The IF strip is now aligned.

4. Set the generator frequency to 1630 Kc/s. The variable condenser in the receiver should still be tuned to the high frequency end. Adjust the oscillator "trimmer" for maximum output at this point.

5. Now set the variable condenser to its lowest frequency point (gang fully meshed) and tune the signal generator until output is observed from the set (this should be around 530-540 Kc/s).

   Should the low frequency fall below 520 Kc/s or above 540 Kc/s, the oscillator coil slug should be adjusted to move the low frequency end to 530 Kc/s. If this is done, operation number 4 must be repeated. This means that the set was thoroughly misaligned and it may require repeating operations 4 and 5 two or three times before a full frequency range is obtained.

6. Set the generator to 1400 Kc/s and tune the receiver in very carefully. Now peak the antenna trimmer. The set is now "tracked" *(fully aligned) at 1400 Kc/s.

7. Since it should also be "tracked" at 600 Kc/s,** set the generator to this frequency, tune in the set, and observe whether the sensitivity of the receiver is close to its 1400 Kc/s value. If this is not the case, then peak the oscillator coil slug (providing the coil is slug tuned) while rocking the gang back and forth around 600 Kc/s. Although this procedure will somewhat reduce the frequency range of the set, it will yield the greatest sensitivity at the tracking points.

8. In case the oscillator coil is not tunable, the variable condenser will have to be "knifed", a procedure of bending the plates on the RF section of the air capacitor, plus realignment, that requires a high degree of experience and is not generally recommended.

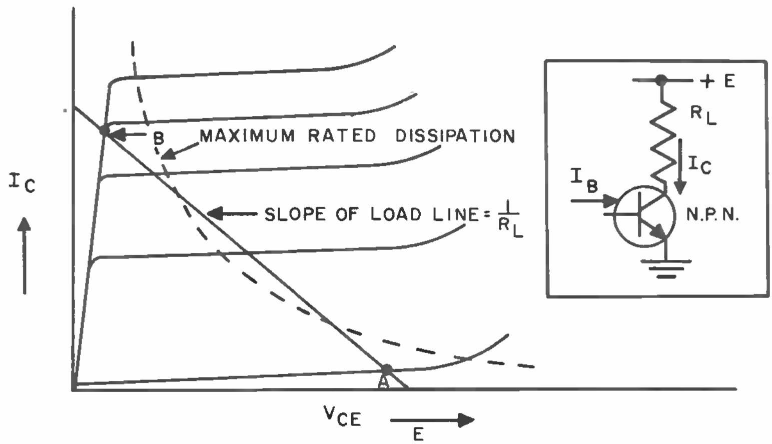
---

*The term "tracking" here applies to the procedure of having the oscillator and antenna circuit tuned to be exactly 455 Kc/s apart, yielding maximum gain at each tracked point.

**Most commercial variable condensers are designed to track at three points along the band, 1400 Kc/s, 1000 Kc/s, and 600 Kc/s.

10. SWITCHING CHARACTERISTICS

A switch is characterized by a high resistance when it is open and a low resistance when it is closed. Transistors can be used as switches. They offer the advantages of no moving or wearing parts and are easily actuated from various electrical inputs. Transistor collector characteristics as applied to a switching application is shown in Figure 10.1. The operating point A at which $I_C = I_{CO}/1-\alpha$ indicates the transistor's high resistance



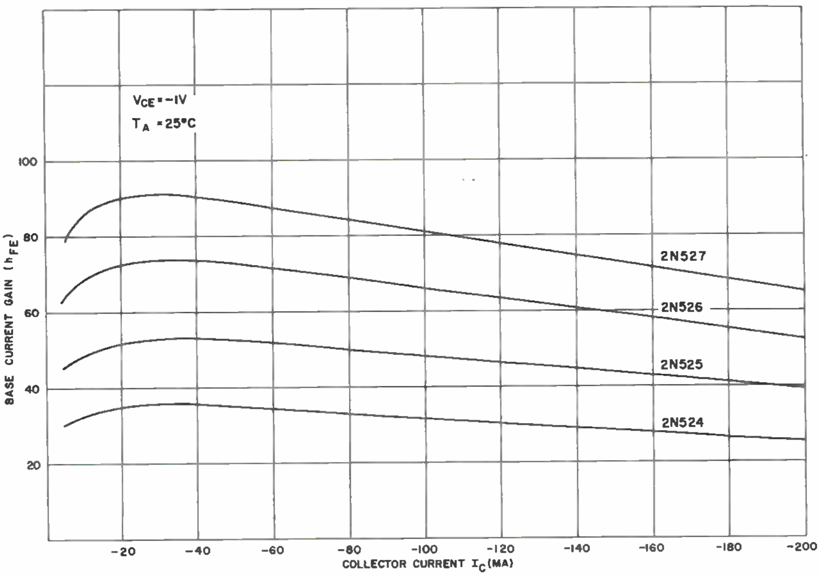
COLLECTOR CHARACTERISTICS

FIGURE 10.1

when $I_B = O$. Since $1-\alpha$ is a small number, I_C may be many times greater than I_{CO}. Shorting the base to the emitter results in a smaller I_C. If the base to emitter junction is reversed biased by more than .2v, I_C will approach I_{CO}. Reverse biasing achieves the highest resistance across an open transistor switch.

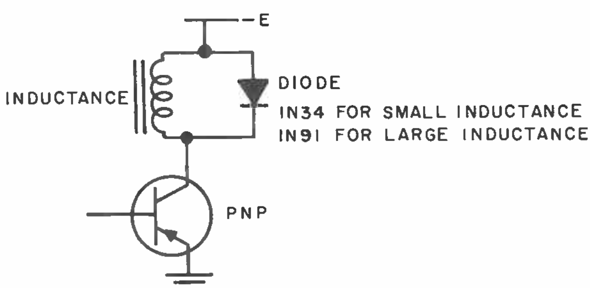
When the transistor switch is turned on, the voltage across it should be a minimum. At operating point B of Figure 10.1, the transistor is a low resistance. Alloy transistors such as the 2N525 have about one ohm resistance when switched on. Grown junction transistors, such as the 2N167 have approximately 80 ohms resistance which makes them less suitable for high power switching although they are well suited for high speed computer applications. In order that a low resistance be achieved, it is necessary that point B lie below the knee of the characteristic curves. The region below the knee is referred to as the saturation region. Enough base current must be supplied to ensure that this point is reached. It is also important that both the on and off operating points lie in the region below the maximum rated dissipation to avoid transistor destruction. It is permissible, however, to pass through the high dissipation region very rapidly since peak dissipations of about one watt can be tolerated for a few microseconds with a transistor rated at 150 mw. In calculating the I_B necessary to reach point B, it is necessary to know how h_{FE} varies with I_C. Curves such as

Figure 10.2 are provided for switching transistors. Knowing h_{FE} from the curve gives $I_{B\,min}$ since $I_{B\,min} = \frac{I_C}{h_{FE}}$. Generally I_B is made two or three times greater than $I_{B\,min}$ to allow for variations in h_{FE} with temperature or aging. The maximum rated collector voltage should never be exceeded since destructive heating may occur once a transistor breaks down. Inductive loads can generate injurious voltage transients. These can be avoided by connecting a diode across the inductance to absorb the transient as shown in Figure 10.3.



D. C. BASE CURRENT GAIN (h_{FE}) VS COLLECTOR CURRENT

FIGURE 10.2

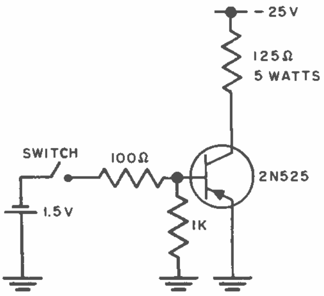


DIODE USED TO PROTECT TRANSISTOR FROM INDUCTIVE VOLTAGE TRANSIENTS.

FIGURE 10.3

Lighted incandescent lamps have about 10 times their off resistance. Consequently, I_B must be increased appreciably to avoid overheating the switching transistor when lighting a lamp.

A typical switching circuit is shown in Figure 10.4. The requirement is to switch a



TYPICAL VALUES

I_c = 80μA SWITCH OPEN

I_c = 0.2A SWITCH CLOSED

I_s = 10mA = CURRENT THROUGH SWITCH

V_{ce} = .19V SWITCH CLOSED

V_{be} = .48V SWITCH CLOSED

INPUT POWER = 15 MILLIWATTS

LOAD POWER = 5 WATTS

Typical transistor switch application
FIGURE 10.4

200 ma current in a 25 volt circuit, delivering 5 watts to the load resistor. The mechanical switch contacts are to carry a low current and be operated at a low voltage to minimize arcing. The circuit shown uses a 2N525. The 1K resistor from the base to ground reduces the leakage current when the switch is open. Typical values are indicated in Figure 10.4.

TEMPERATURE EFFECTS ON SWITCHING CIRCUITS

At high junction temperatures, I_{co} can become a problem. In the off condition, both the emitter and collector junctions are generally reverse-biased. As a rule, the bias source has an appreciable resistance permitting a voltage to be developed across the resistance by I_{co}. The voltage can reduce the reverse bias to a point where the base becomes forward biased and conduction occurs. Conduction can be avoided by reducing the bias source resistance, by increasing the reverse bias voltage or by reducing I_{co} through a heat sink or a lower dissipation circuit design.

The I_{co} of a transistor is generated in three ways. One component originates in the semiconductor material in the base region of the transistor. At any temperature, there are a number of interatomic energy bonds which will spontaneously break into a hole-electron pair. If a voltage is applied, the hole and electron drift in opposite directions and can be seen as the I_{co} current. If no voltage is present, the hole and electron eventually recombine. The number of bonds that will break can be predicted theoretically to double about every 10°C in germanium transistors and every 6°C in silicon. Theory also indicates that the number of bonds broken will not depend on voltage over a considerable voltage range. At low voltages, I_{co} appears to decrease because the drift field is too small to extract all hole-electron pairs before they recombine. At very high voltages, breakdown occurs.

A second component of I_{co} is generated at the surface of the transistor by surface energy states. The energy levels established at the center of a semiconductor junction cannot end abruptly at the surface. The laws of physics demand that the energy levels adjust to compensate for the presence of the surface. By storing charges on the surface, compensation is accomplished. These charges can generate an I_{co} component; in fact, in the processes designed to give the most stable I_{co}, the surface energy levels contribute much I_{co} current. This current behaves much like the base region component with respect to voltage and temperature changes. It is described as the surface thermal component in Figure 10.5.

A third component of I_{CO} is generated at the surface of the transistor by leakage across the junction. This component can be the result of impurities, moisture or surface imperfections. It behaves like a resistor in that it is relatively independent of temperature but varies markedly with voltage. Figure 10.5(A) shows the regions which contribute to the three components. Figure 10.5(B) illustrates how the components vary with voltage. It is seen that while there is no way to measure the base region and surface energy state components separately, a low voltage I_{CO} consists almost entirely of these two components. Thus, the surface leakage contribution to a high voltage I_{CO} can be readily determined by subtracting out the low voltage value of I_{CO}.

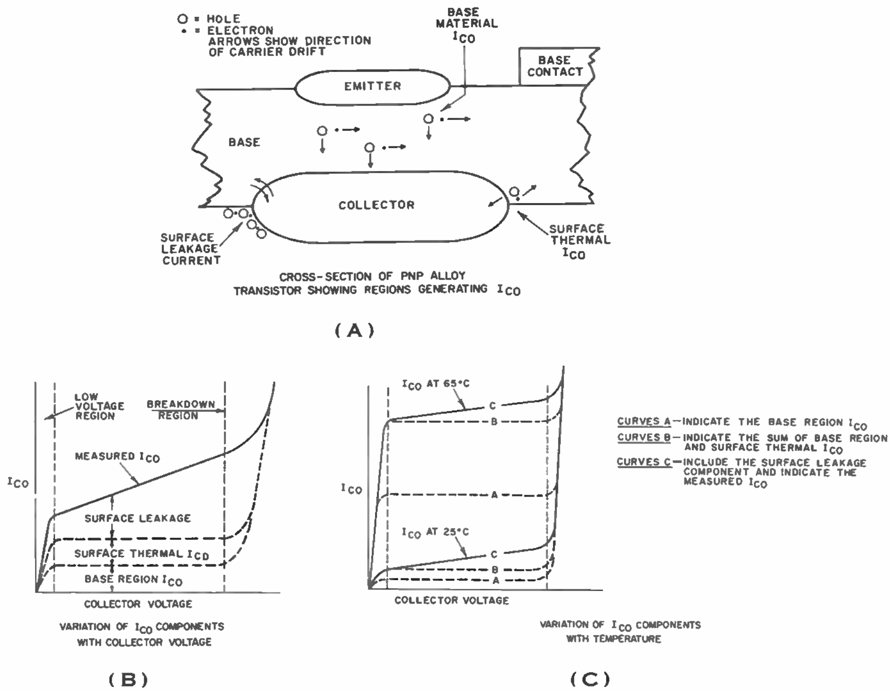


FIGURE 10.5

Figure 10.5(C) shows the variation of I_{CO} with temperature. Note that while the surface thermal and base I_{CO} components have increased markedly, the leakage component is unchanged. For this reason, as temperature is changed the high voltage I_{CO} will change by a smaller percentage than the low voltage I_{CO}.

Figure 10.6 shows the variation of I_{CO} with temperature and voltage for a number of transistor types. Note that the three curves for the 2N396 agree with the principles above and show a leakage current less than one microampere.

The variation of current gain at high temperatures is also significant. Since h_{FE} is defined as I_C/I_B, h_{FE} depends on I_{CO} since $I_C \approx h_{fe}\,(I_B + I_{CO})$. If $I_B = 0$ i.e., if the base is open circuited, a collector current still flows, $I_C = h_{fe}I_{CO}$. Thus h_{FE} is infinite when $I_B = 0$. As base current is applied, the ratio I_C/I_B becomes more meaningful. If h_{FE} is measured for a sufficiently low I_C, then at a high temperature $h_{fe}I_{CO}$ will become equal to I_C. At this temperature h_{FE} becomes infinite since no I_B is required to maintain

I_C. The AC current gain h_{fe}, however, is relatively independent of I_{CO} and generally increases about 2:1 from $-55°C$ to $+85°C$.

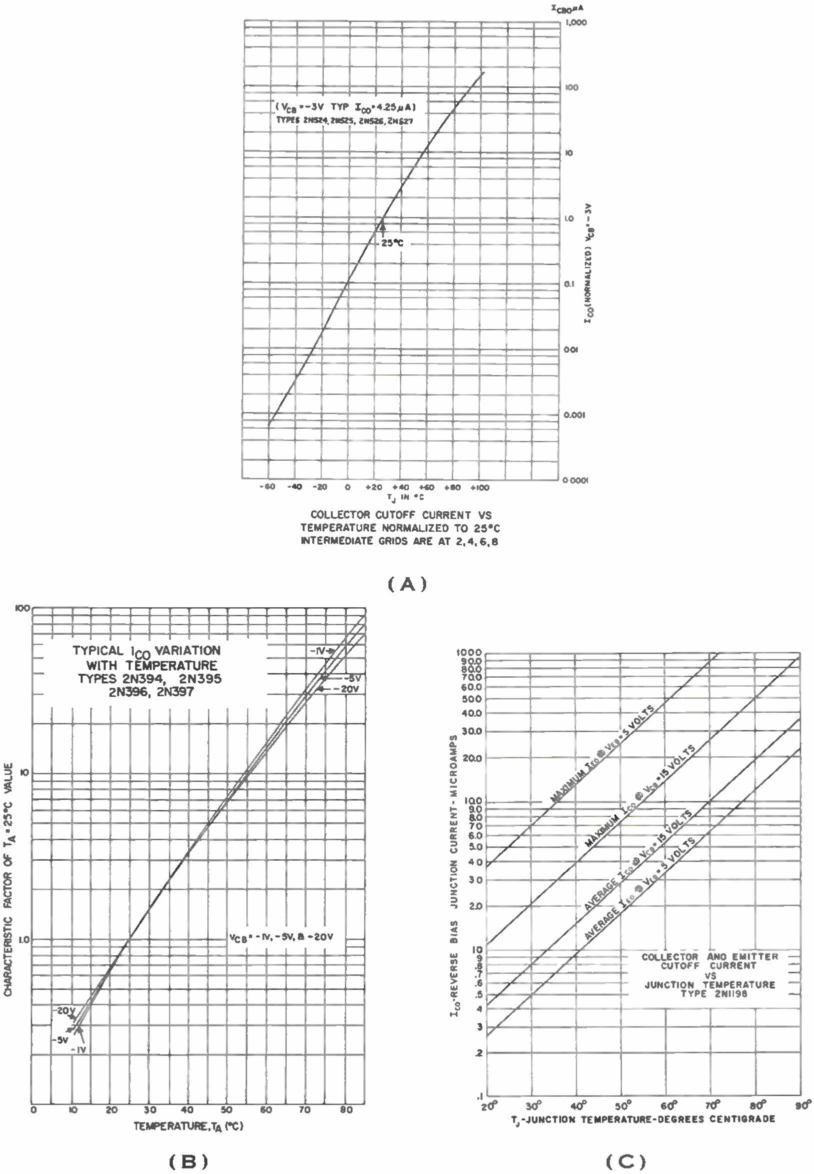


FIGURE 10.6

The different electrical properties of the base, emitter and collector regions tend to disappear at high temperatures with the result that transistor action ceases. This temperature usually exceeds 85°C and 150°C in germanium and silicon transistors respectively.

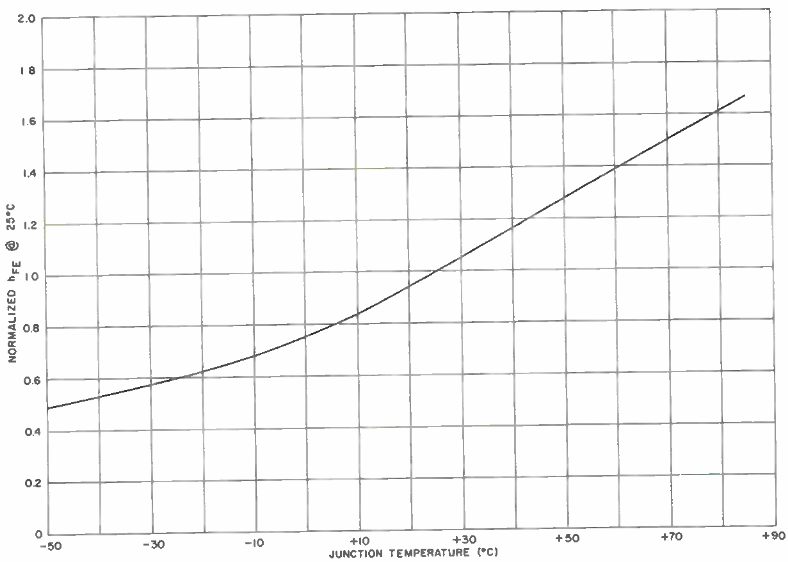
When a transistor is used at high junction temperatures, it is possible for regenerative heating to occur which will result in thermal run-away and possible destruction of the transistor. For the maximum overall reliability, circuits should be designed to preclude the possibility of thermal run-away under the worst operating conditions. The subject of thermal run-away is discussed in detail in Chapter 5.

In accordance with theory the collector saturation voltage, $V_{CE}^{(SAT)}$, decreases linearly with temperature for most transistors. In the case of alloy transistors, this is a result of the increase of I_{CO} with temperature which increases the effective base charge at high temperatures. However, transistors which have an appreciable ohmic resistance in series with the collector or silicon transistors which have a low I_{CO}, generally exhibit a positive temperature coefficient for $V_{CE}^{(SAT)}$.

The base to emitter voltage, V_{BE}, has a negative temperature coefficient which is about 2.0 millivolts per degree Centrigrade for both silicon and germanium transistors. Figure 5.1 shows the emitter to base characteristics of the 2N525 at several different temperatures. The series base resistance and emitter resistance (r_b', r_e') have a positive temperature coefficient so that the IR drops across these resistances can offset the normal variation of V_{BE} at high values of base current.

The increase in $V_{CE}^{(SAT)}$ and the decrease in V_{BE} at high temperatures can lead to instability in DCTL circuits such as shown in Figure 10.9 and result in operation closer to saturation in circuits such as those shown in Figure 10.11.

A major problem encountered in the operation of switching circuits at low temperatures is the reduction in both the a-c and d-c current gain. Figure 10.7 shows the variation of h_{FE} with temperature for the 2N525 and indicates that at −55°C the value of h_{FE} drops to about 50% of its value at 25°C. Most germanium and silicon transistors show approximately this variation of h_{FE} and h_{fe} with temperature. In the design of switching circuits the decrease of h_{FE} and the increase of V_{BE} at the lower temperatures must be taken into account to guarantee reliable circuit operation.



CURRENT GAIN (h_{FE}) VS TEMPERATURE NORMALIZED TO 25°C

FIGURE 10.7

POWER DISSIPATION

As with most electrical components, the transistor's range of operating conditions is limited by the transistor power dissipation.

Because the transistor is capable of a very low V_{CE} when it is in saturation it is possible to use load lines which exceed the maximum rated dissipation during the switching transient, but do not exceed it in the steady state. Such load lines can be used safely if the junction temperature does not rise to the runaway temperature during the switching transient. If the transient is faster than the thermal time constant of the junction, the transistor case may be considered to be an infinite heatsink. The junction temperature rise can then be calculated on the basis of the infinite heatsink derating factor. Since the thermal mass of the junctions is not considered, the calculation is conservative.

In some applications there may be a transient over-voltage applied to transistors when power is turned on or when circuit failure occurs. If the transistor is manufactured to high reliability standards, the maximum voltages may be exceeded provided the dissipation is kept within specifications. While quality alloy transistors and grown junction transistors can tolerate operation in the breakdown region, low quality alloy transistors with irregular junctions should not be used above the maximum voltage ratings.

Quality transistors can withstand much abuse. In experimental work, a 2N43 was operated at a peak power of 15 watts and a peak current of 0.5 amperes with no change in characteristics. 2N396 Transistors in an avalanche mode oscillator were operated at peak currents of one ampere. 3N37 Tetrodes rated at 50 milliwatts and 25 milliamperes maximum were operated at a peak power of one watt and a peak current of 200 milliamperes without change in characteristics. Standard production units however should be operated within ratings to ensure consistent circuit performance and long life.

It is generally desirable to heatsink a transistor to lower its junction temperature since life expectancy as well as performance decreases at high temperatures. Heat sinks also minimize thermal fatigue problems, if any exist.

SATURATION

A transistor is said to be in saturation when both junctions are forward biased. Looking at the common emitter collector characteristics shown in Figure 10.8(A) the saturation region is approximately the region below the knee of the curves, since h_{FE} usually falls rapidly when the collector is forward biased. Since all the characteristic curves tend to become superimposed in the saturation region, the slope of the curves is called the saturation resistance. If the transistor is unsymmetrical electrically – and most transistors are unsymmetrical – then the characteristics will not be directed towards the zero coordinates but will be displaced a few millivolts from zero. For ease of measurement, generally the characteristics are assumed to converge on zero so that the saturation resistance is $r_s = \frac{V_{CE}^{(SAT)}}{I_C}$.

While the characteristic curves appear superimposed, an expanded scale shows that $V_{CE}^{(SAT)}$ depends on I_B for any given I_C. The greater I_B is made, the lower $V_{CE}^{(SAT)}$ becomes until I_B is so large that it develops an appreciable voltage across the ohmic emitter resistance and in this way increases V_{CE}(sat). In most cases the saturation voltage, $V_{CE}^{(SAT)}$, is specified rather than the saturation resistance. Figure 10.8(B) showing the collector characteristics in the saturation region, illustrates the small voltage off-set due to asymmetry and the dependence of r_s on I_B. Note also that r_s is a low resistance to both AC and DC.

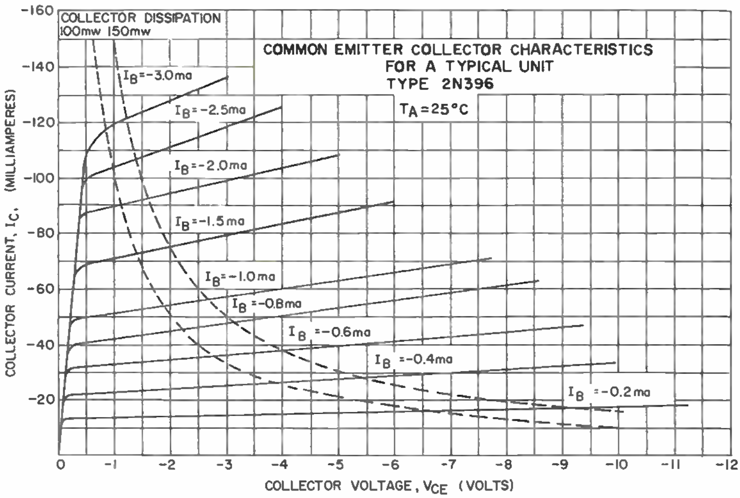


FIGURE 10.8(A)

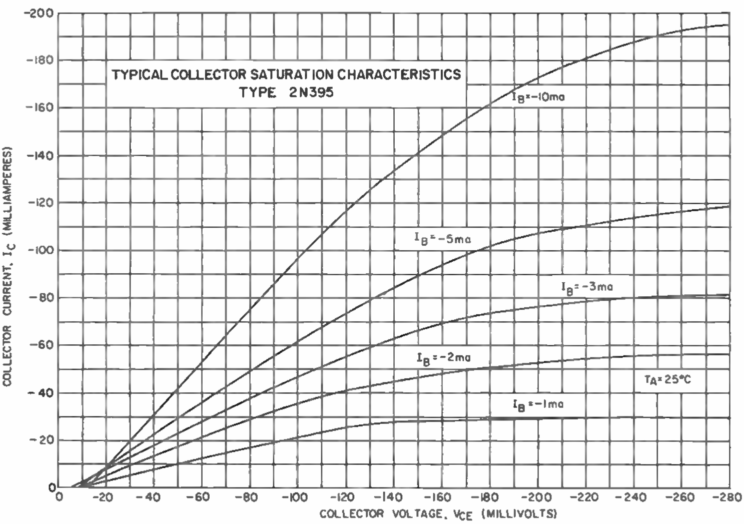
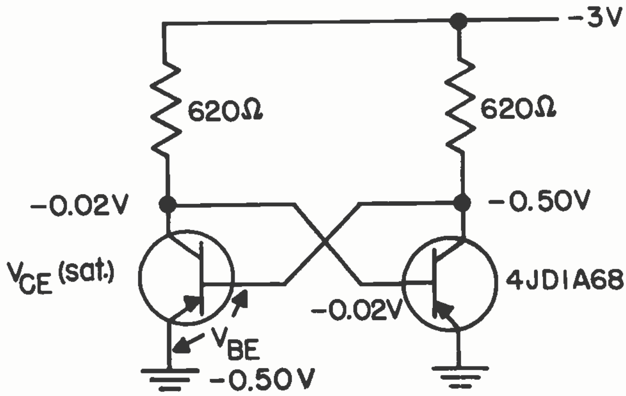


FIGURE 10.8(B)

Some circuits have been designed making specific use of saturation. The direct coupled transistor logic (DCTL) flip-flop shown in Figure 10.9 utilizes saturation. In saturation $V_{CE}^{(SAT)}$ can be so low that if this voltage is applied between the base and emitter of another transistor, as in this flip-flop, there is insufficient forward bias to cause this transistor to conduct appreciably. The extreme simplicity of the circuit



DIRECT COUPLED TRANSISTOR LOGIC (DCTL) FLIP-FLOP

FIGURE 10.9

is self evident and is responsible for its popularity. However, special requirements are placed on the transistors. The following are among the circuit characteristics:

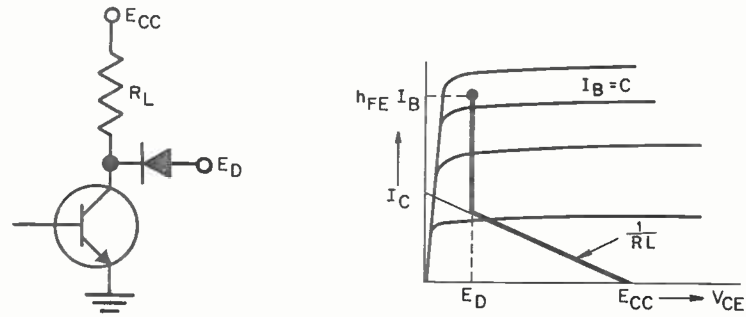
First, the emitter junction is never reverse biased permitting excessive current to flow in the off transistor at temperatures above 40°C in germanium. In silicon, however, operation to 150°C has proved feasible.

Second, saturation is responsible for a storage time delay, slowing up circuit speed. In the section on transient response we see the importance of drawing current out of the base region to increase speed. In DCTL, this current results from the difference between $V_{CE}^{(SAT)}$ and V_{BE} of a conducting transistor. To increase the current, $V_{CE}^{(SAT)}$ should be small and r'_b should be small. However, if one collector is to drive more than one base, r'_b should be relatively large to permit uniform current sharing between bases since large base current unbalance will cause large variations in transient response resulting in circuit design complexity.

Third, since $V_{CE}^{(SAT)}$ and V_{BE} differ by less than ..3 volt, in germanium, stray voltage signals of this amplitude can cause faulty performance. While stray signals can be minimized by careful circuit layout, this leads to equipment design complexity. Silicon transistors with a .7 volt difference between $V_{CE}^{(SAT)}$ and V_{BE} are less prone to being turned on by stray voltages but are still susceptible to turn off signals. This is somewhat compensated for in transistors with long storage time delay since they will remain on by virtue of the stored charge during short turn-off stray signals. This leads to conflicting transistor requirements — long storage time for freedom from noise; short storage time for circuit speed.

Another application of saturation is saturated flip-flops of conventional configuration. Since $V_{CE}^{(SAT)}$ is generally very much less than other circuit voltages, saturating the transistors permits the assumption that all three electrodes are nearly at the same potential making circuit voltages independent of transistor characteristics. This yields good temperature stability, and good interchangeability. The stable voltage levels are useful in generating precise pulse widths with monostable flip-flops. The section on flip-flop design indicates the ease with which saturated circuits can be designed.

In general, the advantages of saturated switch design are: (a) simplicity of circuit design, (b) well defined voltage levels, (c) fewer parts required than in non saturating circuits, (d) low transistor dissipation when conducting, and (e) immunity to short stray voltage signals. Against this must be weighed the reduction in circuit speed. Speed is affected in a number of ways: (a) much higher trigger power is required to turn off a saturated transistor than an unsaturated one, (b) since $V_{CE}^{(SAT)}$, h_{FE} and V_{BE} all vary markedly with temperature, circuit speed also depends on temperature.

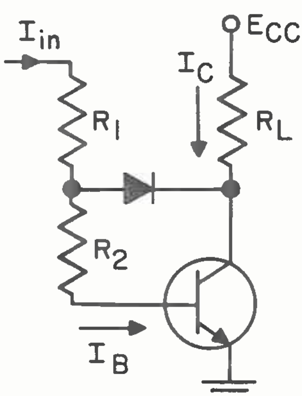


DIODE COLLECTOR CLAMPING CIRCUIT TO AVOID SATURATION

COLLECTOR CHARACTERISTICS SHOWING LOAD LINE AND OPERATING POINTS

Collector voltage clamp
FIGURE 10.10

A number of techniques are used to avoid saturation. The simplest is shown in Figure 10.10. The diode clamps the collector voltage so that it cannot fall below the base voltage to forward bias the collector junction. Response time is not improved appreciably over the saturated case since I_C is not clamped but rises to $h_{FE}I_B$. With typical variations of I_B and h_{FE} with temperature and life for a standard transistor, I_C may vary by as much as 10:1. Care should be taken to ensure that the diode prevents saturation with the highest I_C. When the transistor is turned off, I_C must fall below the value given by $(E_{CC}-E_D)/R_L$ before any change in collector voltage is observed. The time required can be determined from the fall time equations in the section on transient response. The diode can also have a long recovery time from the high currents it has to handle. This can further increase the delay in turning off.

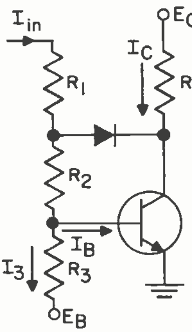


$$V_{CE} \approx \frac{R_2 \; E_{CC}}{R_L h_{FE} + R_2}$$

$$\approx \frac{E_{CC} R_2}{R_L h_{FE}} \quad \text{if } V_{CE} << E_{CC}$$

Collector current clamp without bias supply
FIGURE 10.11 (A)

A much better way of avoiding saturation is to control I_B in such a way that I_C is just short of the saturation level. This can be achieved with the circuit of Figure 10.11(A). The diode is connected between a tap on the base drive resistor and the collector. When the collector falls below the voltage at the tap, the diode conducts diverting base current into the collector, preventing any further increase in I_C. The voltage drop across R_2 is approximately $I_C R_2/h_{FE}$ since the current in R_2 is I_B. Since the voltage drop across the diode is approximately the same as the input voltage to the transistor, V_{CE} is approximately $I_C R_2/h_{FE}$. It is seen that if the load decreases (I_C is reduced) or h_{FE} becomes very high, V_{CE} decreases towards saturation. Where the change in h_{FE} is known and the load is relatively fixed, this circuit prevents saturation.



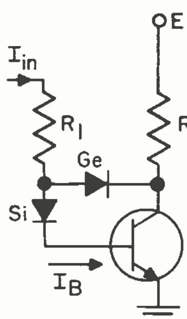
$$V_{CE} \approx \frac{R_2\,(E_{CC} + I_3 R_L h_{FE})}{R_L h_{FE} + R_2}$$

$$\approx R_2\left(\frac{E_{CC}}{R_L h_{FE}} + I_3\right)$$

if $V_{CE} \ll E_{CC}$

Collector current using bias supply
FIGURE 10.11 (B)

To avoid the dependence of V_{CE} on I_C and h_{FE}, R_3 may be added as in Figure 10.11(B). By returning R_3 to a bias voltage, an additional current is drawn through R_2. Now V_{CE} is approximately $(\frac{I_C}{h_{FE}} + I_3)\,R_2$. I_3 can be chosen to give a suitable minimum V_{CE}.



$V_{CE} \approx 0.7\text{V}$ at 25° C.

Collector current clamp using silicon
and germanium diodes
FIGURE 10.11 (C)

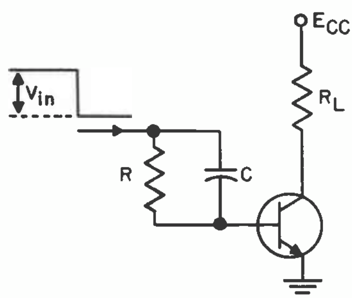
The power consumed by R_3 can be avoided by using the circuit of Figure 10.11(C). The silicon diode replaces R_2. Since the silicon diode has a forward voltage drop of approximately .7 volts over a considerable range of current, it acts as a constant voltage source making V_{CE} approximately .7 volts. If considerable base drive is used, it may be necessary to use a high conductance germanium diode to avoid momentary saturation as the voltage drop across the diode increases to handle the large base drive current.

In applying the same technique to silicon transistors with low saturation resistance, it is possible to use a single germanium diode between the collector and base. While this permits V_{CE} to fall below V_{BE}, the collector diode remains essentially non-conducting since the .7 volt forward voltage necessary for conduction cannot be reached with the germanium diode in the circuit.

The diode requirements are not stringent. The silicon diode need never be back biased, consequently, any diode will be satisfactory. The germanium diode will have to withstand the maximum circuit V_{CE}, conduct the maximum base drive with a low forward voltage and switch rapidly under the conditions imposed by the circuit, but these requirements are generally easily met.

Care should be taken to include the diode leakage currents in designing these circuits for high temperatures. All the circuits of Figure 10.11 permit large base drive currents to enhance switching speed, yet they limit both I_B and I_C just before saturation is reached. In this way, the transistor dissipation is made low and uniform among transistors of differing characteristics.

It is quite possible to design flip-flops which will be non-saturating without the use of clamping diodes by proper choice of components. The resulting flip-flop is simpler than that using diodes but it does not permit as large a load variation before malfunction occurs. The design procedure for an unclamped non-saturating flip-flop can be found in *Transistor Circuit Engineering* by R. F. Shea, et al (Wiley).

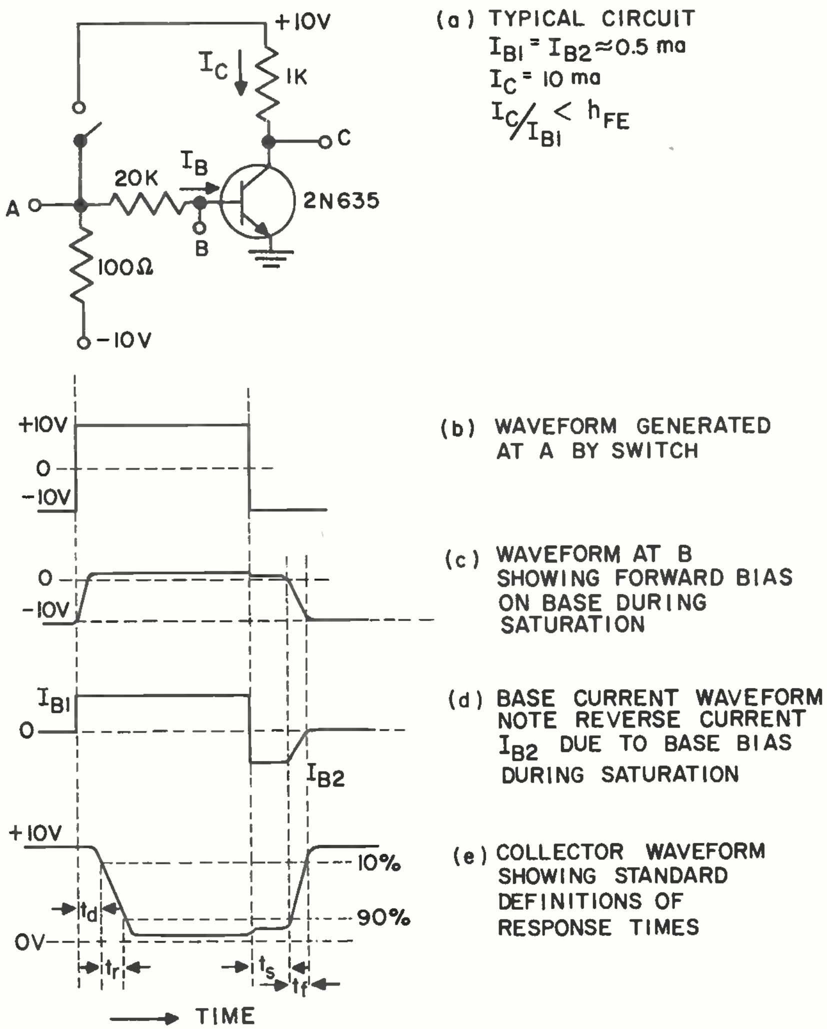


Stored charge neutralization by capacitor
FIGURE 10.12

Another circuit which is successful in minimizing storage time is shown in Figure 10.12. If the input is driven from a voltage source, it is seen that if the input voltage and capacitor are appropriately chosen, the capacitor charge can be used to neutralize the stored charge, in this way avoiding the storage time delay. In practical circuits, the RC time constant in the base necessary for this action limits the maximum pulse repetition rate.

TRANSIENT RESPONSE TIME

The speed with which a transistor switch responds to an input signal depends on the load impedance, the gain expected from the transistor, the operating conditions just prior to the input signal, as well as on the transistor's inherent speed. The following discussion will assume that the collector load resistance is sufficiently small that $2\pi R_L C_c f_\alpha << 1$ where C_c is the collector capacitance. If this is not the case, the rise and fall time equations must be multiplied by the correction factor $(1 + 2\pi R_L C_c f_\alpha)$.



Transient response
FIGURE 10.13

Consider the simple circuit of Figure 10.13(a). Closing and opening the switch to generate a pulse as shown in Figure 10.13(b), gives the other waveforms shown in the figure. When the switch closes, current flows through the 20K resistor to turn on the transistor. However there is a delay before collector current can begin to flow since the 20K must discharge the emitter capacitance which was charged to −10 volts prior to closing the switch. Time must also be allowed for the emitter current to diffuse across the base region. A third factor adding to the delay time is the fact that at low emitter current densities current gain and frequency response decrease. The total delay from all causes is called the "delay time" and is measured conventionally from the beginning of the input pulse to the 10% point on the collector waveform as shown in Figure 10.13(e). Delay time can be decreased by reducing the bias voltage across the emitter capacitance, and by reducing the base drive resistor in order to reduce the charging time constant. At high emitter current densities, delay time becomes negligible. Figure 10.14 shows typical delay times for the 2N396 transistor.

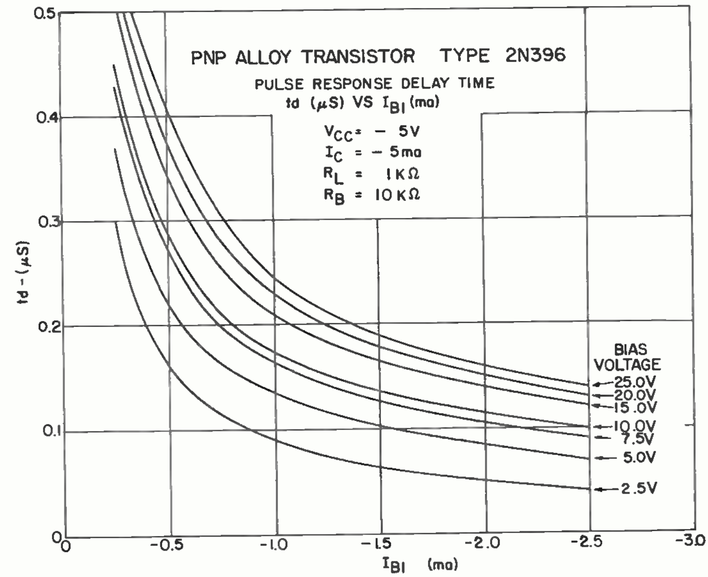
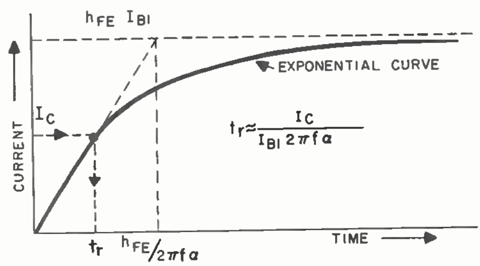


FIGURE 10.14

The rise time refers to the turn-on of collector current. By basing the definition of rise time on current rather than voltage it becomes the same for NPN and PNP transistors. The collector voltage change may be of either polarity depending on the transistor type. However, since the voltage across the collector load resistor is a measure of collector current, it is customary to discuss the response time in terms of the collector voltage. The theoretical analysis of rise time suggests that a single exponential curve as defined in Figure 10.15 fits the experimental results.



GRAPHICAL ANALYSIS OF RISE TIME
SYMBOLS DEFINED IN FIGURE 109
THE INTERCEPT OF I_C AND THE CURVE GIVES t_r.

FIGURE 10.15

If the load resistor R_L in Figure 10.13(a) is small enough that a current, $h_{FE}I_{B1}$, through it will not drive the transistor into saturation, the collector current will rise exponentially to $h_{fe}I_{B1}$ with a time constant, $h_{FE}/2\pi f_\alpha$. However, if R_L limits the current to less than $h_{FE}I_{B1}$, the same exponential response will apply except that the curve will be terminated at $I_C = \frac{V_{CC}}{R_L}$. Figure 10.15 illustrates the case for $I_C \approx h_{FE}I_{B1}/2$. Note that the waveform will no longer appear exponential but rather almost linear. This curve can be used to demonstrate the roles of the circuit and the transistor in determining rise time. For a given h_{FE} and f_α, it is seen that increasing $h_{FE}I_{B1}/I_C$ will decrease rise time by having I_C intersect the curve closer to the origin. On the other hand, for a given I_{B1} and I_C, speed will be proportional to f_α but nearly independent of h_{FE} since its effect on the time constant is balanced by its effect on the curve amplitude. A useful expression for rise time is $t_r = I_C/I_{B1}\ 2\pi f_\alpha$. It is valid for $I_C/I_B < h_{FE}/5$. Since this analysis assumes that h_{FE} and f_α are the same for all operating points the calculated results will not fit experimental data where these assumptions are invalid. Figure 10.16 shows that the rise time halves as the drive current doubles, just as the expression for t_r suggests. However the calculated value for t_r is in error by more than 50%. This shows that even though the calculations may be in error, if the response time is specified for a circuit, it is possible to judge fairly accurately how it will change with circuit modifications using the above equations.

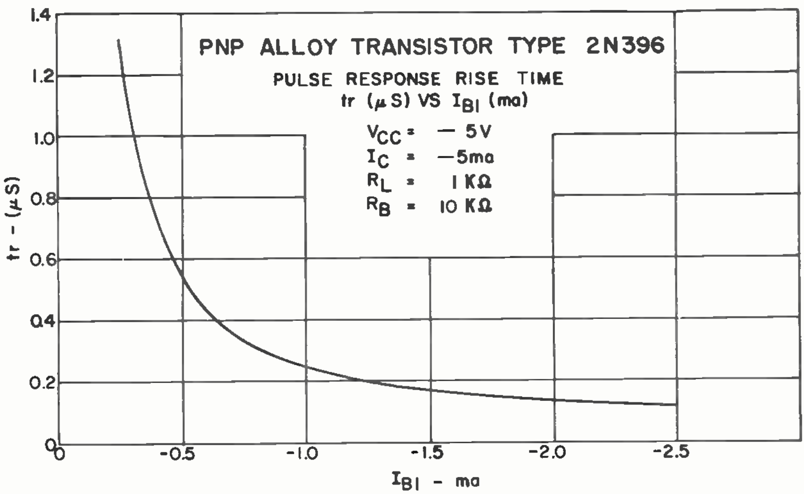
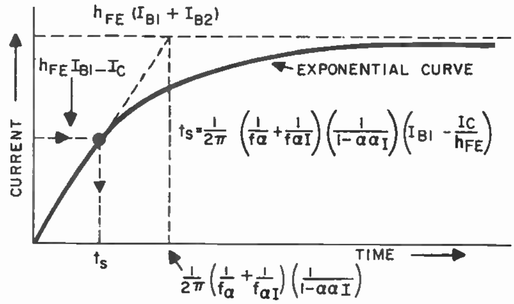


FIGURE 10.16

Storage time is the delay a transistor exhibits before its collector current starts to turn off. In Figure 10.13, R_B and R_L are chosen so that R_L rather than h_{FE} will limit the collector current. The front edge of the collector waveform, Figure 10.13(e), shows the delay time followed by the nearly linear risetime. When the collector voltage falls below the base voltage, the base to collector diode becomes forward biased with the result that the collector begins emitting. By definition, the transistor is said to be in saturation when this occurs. This condition results in a stored charge of carriers in the base region. Since the flow of current is controlled by the carrier distribution in the base, it is impossible to decrease the collector current until the stored carriers are removed. When the switch is open in Figure 10.13, the voltage at A drops immediately to —10 volts. The base voltage at B however cannot go negative since the transistor is kept on by the stored carriers. The resulting voltage across R_B causes the carriers to flow out of the base to produce a current I_{B2}. This is illustrated in Figure 10.13(c) and 10.13(d). As soon as the stored carriers are swept out, the transistor starts to turn off; the base voltage dropping to −10 volts and the base current decreasing to zero. The higher I_{B1} is, the greater the stored charge; the higher I_{B2} is, the faster it is swept out. Since both junctions are forward biased during storage time, the inverse characteristics of the transistor are involved. The inverse characteristics are obtained by interchanging the collector and emitter connections in any test circuit. They are identified by the subscript I following the parameter, e.g., h_{FEI} is the inverse DC beta. Figure 10.17 shows a curve which is useful for calculating storage time graphically. The maximum value is $h_{FE}(I_{B1}+I_{B2})$ where I_{B2} is given the same sign as I_{B1}, ignoring the fact it flows in the opposite direction. The time constant of the curve involves the forward and inverse current gain and frequency cut-off. The storage time corresponds to the time required to reach the current $h_{FE}I_{B1}-I_C$. It can be seen that for a given frequency response, high h_{FE} gives long storage time. The storage time also decreases as I_{B2} is increased or I_{B1} is decreased.



GRAPHICAL ANALYSIS OF STORAGE TIME.
THE INTERCEPT OF $(h_{FE}I_{B1}-I_C)$ AND THE CURVE GIVES t_s

FIGURE 10.17

The time constant for a very unsymmetrical transistor is approximately $\frac{h_{FEI}+1}{2\pi f_{\alpha I}}$. It is seen that the generally specified normal h_{FE} and f_α are of little use in determining storage time. For a symmetrical transistor, the time constant is approximately $\frac{h_{FE}+1}{2\pi f_\alpha}$. It is possible for a symmetrical transistor to have a longer storage time than

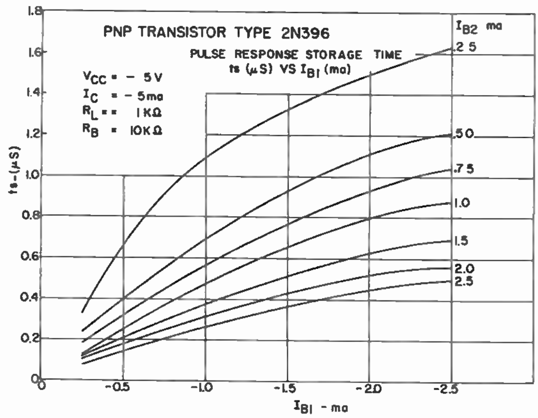
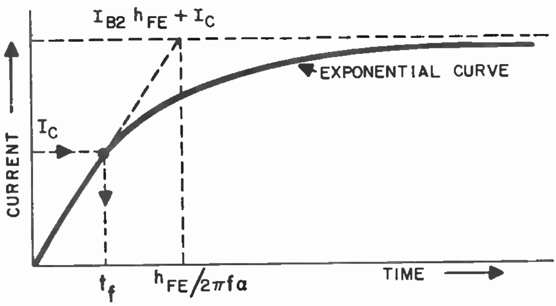


FIGURE 10.18

an unsymmetrical transistor with the same h_{FE} and f_α. Figure 10.18 shows the dependence of storage time on I_{B1} and I_{B2} for the 2N396 transistor.



GRAPHICAL ANALYSIS OF FALL TIME
THE INTERCEPT OF I_C AND THE CURVE GIVES t_f.

FIGURE 10.19

The collector current fall time can be analyzed in much the same manner. Figure 10.19 indicates the exponential curve of amplitude $I_C + h_{FE}I_{B2}$, and a time constant, $h_{FE}/2\pi f_\alpha$. The fall time is given by the time it takes the exponential to reach I_C. If $h_{FE}I_{B2} >> I_C$, fall time is given by the expression,

$$t_F = \frac{1}{2\pi f_\alpha}\,\frac{h_{FE}\,I_C/I_{B2}}{h_{FE} + I_C/I_{B2}}$$

As h_{FE} becomes large, this expression reduces to,

$$t_F = \frac{1}{2\pi f_\alpha}\,\frac{I_C}{I_{B2}}$$

which is identical to the expression for t_r except that I_{B2} replaces I_{B1}. Figure 10.20 shows typical fall time measurements for a 2N396.

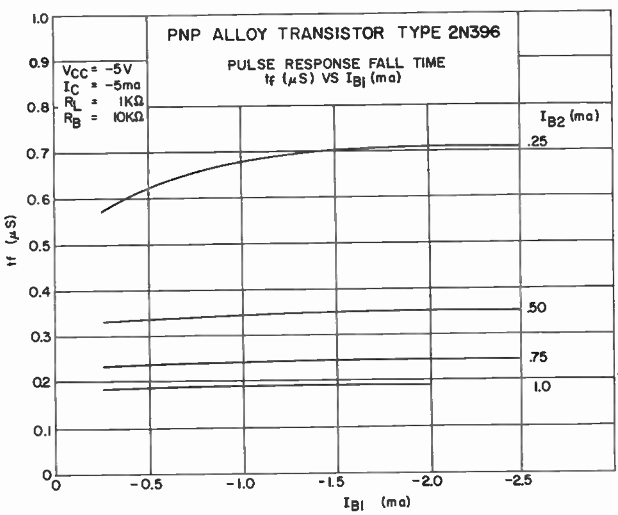


FIGURE 10.20

11. BASIC COMPUTER CIRCUITS

Computers are generally classified as either analog or digital. An example of an analog computer is the slide rule where the numerical values involved in the calculations are represented by the distance along the scales of the slide rule. For the slide rule, distance is the analog of the numerical values. In an electronic analog computer the voltage or current in the circuit is used as the analog of the numerical values involved in the calculation. Analog computers are used primarily in cases where minimum cost is important and high accuracy is not required.

In a digital computer the numerical values change in discrete steps rather than continuously as in an analog computer. An example of a digital computer is the ordinary desk calculator or adding machine. In an electronic digital computer numerical values involved in the calculation are represented by the discrete states of flip-flops and other switching circuits in the computer. Numerical calculations are carried out in digital computers according to the standard rules of addition, subtraction, multiplication and division. Digital computers are used primarily in cases where high accuracy is required such as in standard accounting work. For example, most desk calculators are capable of giving answers correct to one part in one million, but a slide rule (analog computer) would have to be about ⅙ of a mile long to be read to the same accuracy.

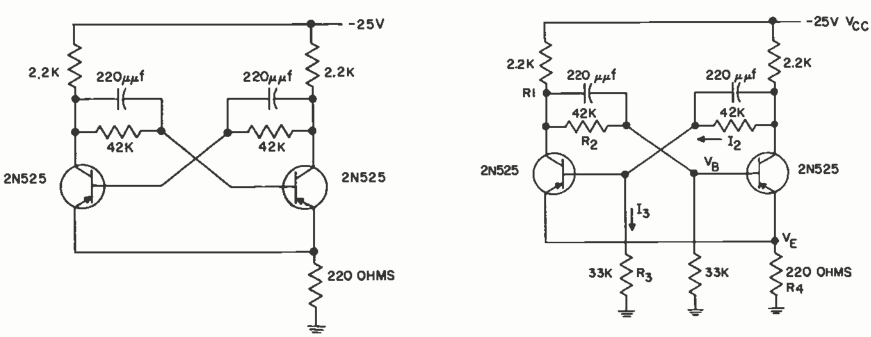
The transistor's small size, low power requirements and inherent reliability have resulted in its extensive use in digital computers. Special characteristics of the transistor such as low saturation resistance, low input impedance, and complementary NPN and PNP types, have permitted new types of digital circuits which are simple, efficient and fast. Computers operating at speeds of 5 megacycles are a commercial reality, and digital circuits have been proved feasible at 160 megacycles.

This chapter offers the design engineer practical basic circuits and design procedures based on proven techniques and components. Flip-flops are discussed in detail because of their extensive use in digital circuits.

FLIP-FLOP DESIGN PROCEDURES

SATURATING FLIP-FLOPS

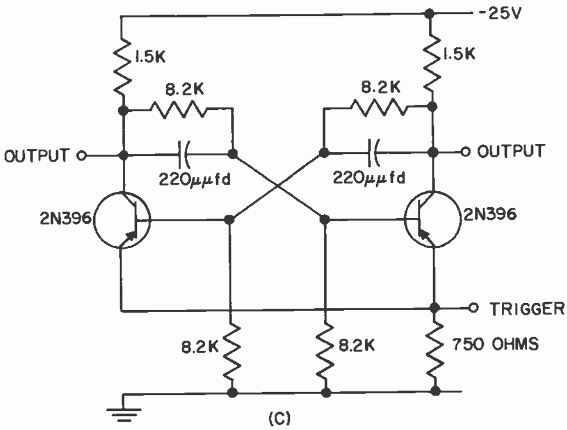
The simplest flip-flop possible is shown in Figure 10.9, however, for standard transistor types the circuit in Figure 11.1(A) is preferable at moderate temperatures. We shall refer to the conducting and non-conducting transistors as the on and off



SATURATED FLIP-FLOPS

FIGURE 11.1 (A) FIGURE 11.1 (B)

transistors respectively. For stability, the circuit depends on the low collector to emitter voltage of the saturated on transistor to reduce the base current of the off transistor to a point where the circuit gain is too low for regeneration. The 220Ω emitter resistor can be removed if emitter triggering is not used. By adding resistors from base to ground as in Figure 11.1(B), the off transistor has both junctions reverse biased for greater stability. While the 33K resistors divert some of the formerly available base current, operation no longer depends on a very low saturation voltage consequently less base current may be used. Adding the two resistors permits stable operation beyond 50°C ambient temperature.



SATURATED FLIP-FLOP
FIGURE 11.1 (C)

The circuit in Figure 11.1(C) is stabilized to 100°C. The price that is paid for the stability is (1) smaller voltage change at the collector, (2) more battery power consumed, (3) more trigger power required, (4) a low I_{CO} transistor must be used. The capacitor values depend on the trigger characteristics and the maximum trigger repetition rate as well as on the flip-flop design.

By far, the fastest way to design saturating flip-flops is to define the collector and emitter resistors by the current and voltage levels generally specified as load requirements. Then assume a tentative cross-coupling network. With all components specified, it is easy to calculate the on base current and the off base voltage. For example, the circuit in Figure 11.1(B) can be analyzed as follows. Assume $V_{BE} = .3$ volt and $V_{CE} = .2$ volt when the transistor is on. Also assume that $V_{EB} = .2$ volts will maintain the off transistor reliably cut-off. Transistor specifications are used to validate the assumptions.

I. Check for the maximum temperature of stability.

$$V_E = \frac{R_4 V_{CC}}{R_1 + R_4} = \frac{220}{2200 + 220}(25) = 2.3 \text{ volts}$$

$$V_{C\,on} = V_E + V_{CE\,on} = 2.3 + .2 = 2.5 \text{ volts}$$

Assuming no I_{CO}, the base of the off transistor can be considered connected to a potential,

$$V'_B = V_{C\,on}\frac{R_3}{R_2 + R_3} \text{ through a resistor } R'_B = \frac{R_2 R_3}{R_2 + R_3}$$

$$V'_B = \frac{(2.5)(33K)}{(42K + 33K)} = 1.1 \text{ volts}$$

$$R'_B = \frac{(33K)(42K)}{75K} = 18.5K$$

The I_{CO} of the off transistor will flow through R'_B reducing the base to emitter potential. If the I_{CO} is high enough, it can forward bias the emitter to base junction causing the off transistor to conduct. In our example, $V_E = 2.3$ volts and $V_{EB} = .2$ volts will maintain off conditions. Therefore, the base potential can rise from 1.1 volts to 2.1 volts (2.3 — .2) without circuit malfunction. This potential is developed across R'_B by $I_{CO} = \frac{2.1 - 1.1}{18.5K} = 54\ \mu a$. A germanium transistor with $I_{CO} = 10\ \mu a$ at 25°C will not exceed 54 μa at 50°C. If a higher operating temperature is required, R_2 and R_3 may be decreased and/or R_4 may be increased.

II. Check for sufficient base current to saturate the on transistor.

$$V_{B\ on} = V_E + V_{BE\ on} = 2.3 + .3 = 2.6 \text{ volts}$$

The current through $R_3 = I_3 = \frac{2.6v}{33K} = .079$ ma

The current through R_1 and R_2 in series is $I_2 = \frac{V_{CC} - V_{B\ on}}{R_1 + R_2} = \frac{25 - 2.6}{42K + 2.2K} = .506$ ma

The available base current is $I_B = I_2 - I_3 = .43$ ma

The collector current is $I_C = \frac{V_{CC} - V_{C\ on}}{R_1} = \frac{25 - 2.5}{2.2K} = 10.25$ ma

The transistor will be in saturation if h_{FE} at 10 ma is greater than

$$\frac{I_C}{I_B} = \frac{10.25}{.43} = 24$$

If this circuit were required to operate to —55°C, allowance must be made for the reduction of h_{FE} at low temperatures. The minimum allowable room temperature h_{FE} should be 50% higher or $h_{FE\ min} = 36$.

Generally it is not necessary to include the effect of I_{CO} flowing through R_1 when calculating I_2 since at temperatures where I_{CO} subtracts from the base drive it simultaneously increases h_{FE}. If more base drive is required, R_2 and R_3 may be decreased. If their ratio is kept constant, the off condition will not deteriorate, and so need not be rechecked.

III. Check transistor dissipation to determine the maximum junction temperature.

The dissipation in the on transistor is

$$V_{BE\ on} I_B + V_{CE\ on} I_C = \frac{(.3)(.43)}{1000} + \frac{(.2)(10.25)}{1000} = 2.18 \text{ mw}$$

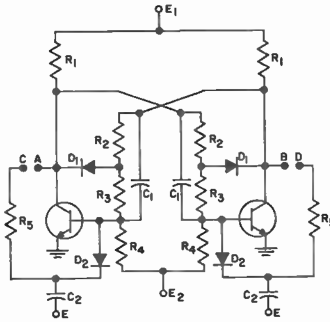
The dissipation in the off transistor resulting from the maximum I_{CO} is

$$V_{CB} I_{CO} \approx \frac{(25)(55)}{10^6} = 1.4 \text{ mw}$$

Generally the dissipation during the switching transient can be ignored at speeds justifying saturated circuitry. In both transistors the junction temperature is within 1°C of the ambient temperature if transistors in the 2N394-97 or 2N524-27 series are used.

NON-SATURATED FLIP-FLOP DESIGN

The abundance of techniques to prevent saturation makes a general design procedure impractical if not impossible. While it is a simple matter to design a flip-flop as shown above, it becomes quite tedious to check all the worst possible combinations of component change to ensure manufacturability and long term reliability. Often the job is assigned to a computer which calculates the optimum component values and tolerances. While a number of flip-flop design procedures have been published, they generally make simplifying assumptions concerning leakage currents and the voltages developed across the conducting transistors.



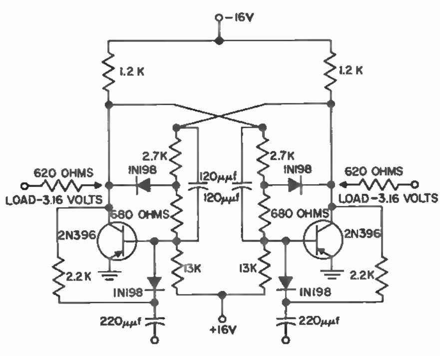
CIRCUIT CONFIGURATION FOR NON-SATURATING FLIP-FLOP DESIGN PROCEDURE

Characteristics:

- Trigger input at points E
- Trigger steering by D_2 and R_5
- Collector clamping by D_1 and R_3
- Connect points A, B, C, D, E as shown in Figure 11.3 to get counter or shift register operation
- C1 and C2 chosen on basis of speed requirements

FIGURE 11.2 (A)

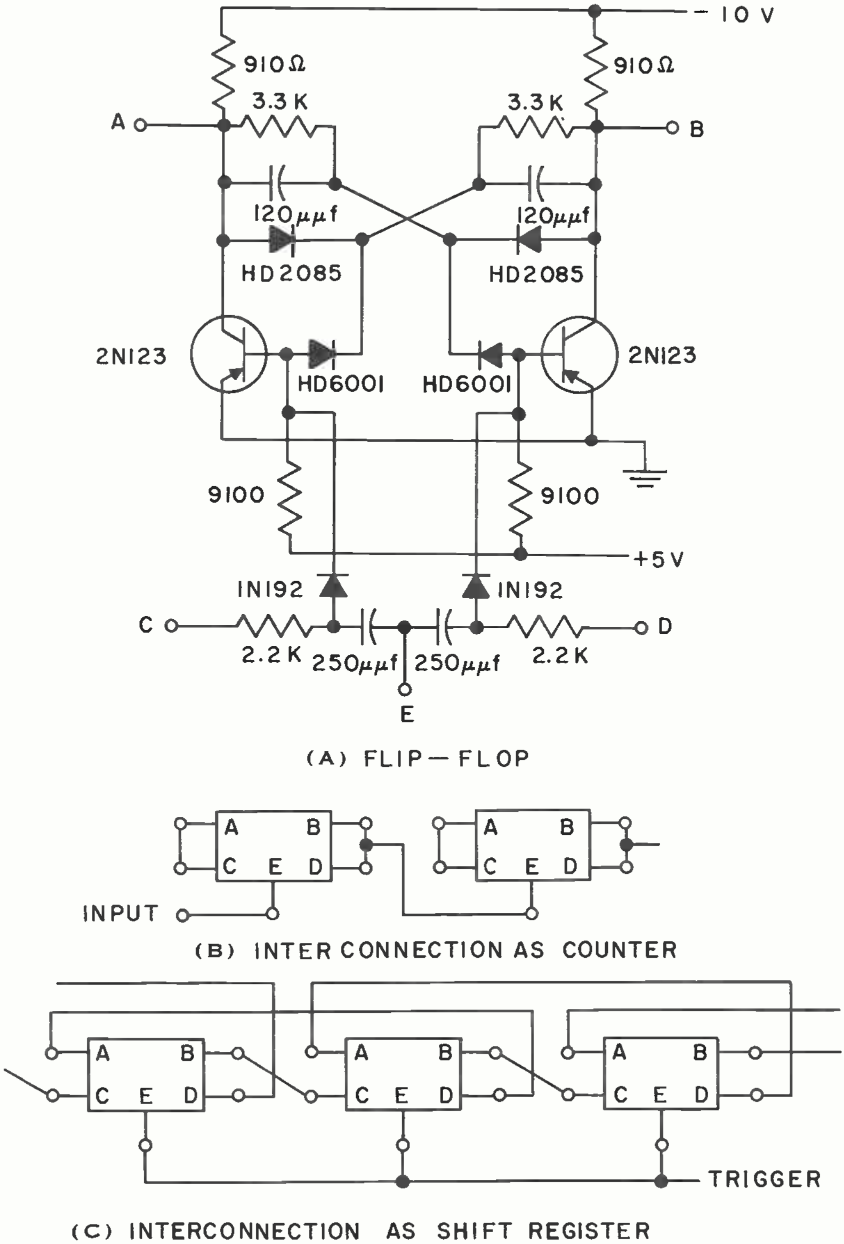
The design procedure described here is for the configuration in Figure 11.2(A). No simplifying assumptions are made but all the leakage currents and all the potentials are considered. The design makes full allowance for component tolerances, voltage fluctuations, and collector output loading. The anti-saturation scheme using one resistor (R3) and one diode (D1) was chosen because of its effectiveness, low cost and simplicity. The trigger gating resistors (R5) may be returned to different collectors to get different circuit functions as shown in Figure 11.3. This method of triggering offers the trigger sensitivity of base triggering and the wide range of trigger amplitude permissible in collector triggering. The derivation of the design procedure would require much space, therefore for conciseness, the procedure is shown without any substantiation. The procedure involves defining the circuit requirements explicitly then determining the transistor and diode characteristics at the anticipated operating points. A few astute guesses of key parameters yield a fast solution. However, since the procedure deals with only one section of the circuit at a time, a solution is readily reached by cut and try methods without recourse to good fortune. A checking procedure permits verification of the calculations. The symbols used refer to Figure 11.2(A) or in some cases are used only to simplify calculations. A bar over a symbol denotes its maximum value; a bar under it, its minimum. The example is based on polarities associated with NPN transistors for clarity. The result is that only E_2 is negative. While the procedure is lengthly, its straightforward steps lend themselves to computation by technically unskilled personnel and the freedom from restricting assumptions guarantees a working circuit when a solution is reached. The circuit designed by this procedure is shown in Figure 11.2(B).



NON-SATURATED FLIP-FLOP

FIGURE 11.2 (B)

The same procedure can be used to analyze existing flip-flops of this configuration by using the design check steps.



500 KC COUNTER-SHIFT REGISTER FLIP-FLOP
FIGURE 11.3

NON-SATURATING FLIP-FLOP DESIGN PROCEDURE

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
(A)	*Circuit Requirements and Device Characteristics*		
1	Assume maximum voltage design tolerance	Δe	Let $\Delta e = \pm 5\%$
2	Assume maximum resistor design tolerance	Δr	Let $\Delta r = \pm 7\%$ (assuming $\pm$ 5% resistors)
3	Assume maximum ambient temperature	T_A	Let $T_A = 40°C$
4	Assume maximum load current out of the off side	I_0	Let $I_0 = 1$ ma
5	Assume maximum load current into the on side	I_l	Let $I_l = 0.2$ ma
6	Estimate the maximum required collector current in the on transistor	I_1	Let $I_1 \leq 17.5$ ma
7	Assume maximum design I_{CO} at 25°C		From spec sheet $I_{CO} < 6\ \mu a$
8	Estimate the maximum junction temperature	T_J	Let $T_J = 60°C$
9	Calculate I_{CO} at T_J assuming I_{CO} doubles every 10°C or $I_{COT_J} = I_{CO25}\, e^{.07(T_J-25)}$	I_2	$I_2 = 6e^{.07T_J} = 71\ \mu a$; Let $I_2 = 100\ \mu a$
10	Assume the maximum base leakage current is equal to the maximum I_{CO}	I_3	Let $I_3 = 100\ \mu a$
11	Calculate the allowable transistor dissipation		2N396 is derated at 3.3 mw/°C. The junction temperature rise is estimated at 20°C therefore 67 mw can be allowed. Let $P_C = 67$ mw
12	Estimate h_{FE} minimum taking into account low temperature degradation and specific assumed operating point	β_{min}	Let $\alpha_{min} = 0.94$ or $\beta_{min} = 15.67$
13	Estimate the maximum design base to emitter voltage of the "on" transistor	V_1	Let $V_1 = 0.35$ volts
14	Assume voltage logic levels for the outputs		Let the level separation be ≥ 7 volts

NON-SATURATING FLIP-FLOP DESIGN PROCEDURE (CONTINUED)

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
15	Choose the maximum collector voltage permissible for the "on" transistor	V_2	Let $V_2 \leq 2.0$ volts
16	Choose suitable diode types		Let all diodes be 1N198
17	Estimate the maximum leakage current of any diode	I_4	Maximum leakage estimated as ≤ 25 μa. Let $I_4 = 40$ μa at end of life
18	Calculate $I_5 = I_3 + I_4$	I_5	$40 + 100 = 140$ μa
19a	Choose the minimum collector voltage for the "off" transistor keeping in mind 14 and 15 above	V_3	Let $V_3 \geq 9.0$ volts
19b	Choose the maximum collector voltage for the "off" transistor	V_4	Let $V_4 \leq 13.0$ volts
20	Choose the minimum design base to emitter reverse bias to assure off conditions	V_5	Let $V_5 = 0.5$ volt
21a	Estimate the maximum forward voltage across the diodes	V_6	Let $V_6 = 0.8$ volt
21b	Estimate the minimum forward voltage	V_7	Let $V_7 = 0.2$ volt
22	Estimate the worst saturation conditions that can be tolerated.		
22a	Estimate the minimum collector voltage that can be tolerated	V_8	Let $V_8 = 0.1$ volt
22b	Estimate the maximum base to collector forward bias voltage that can be tolerated	V_9	Let $V_9 = 0.1$ volt
23a	Calculate $V_2 + V_7$	V_{10}	$2 + 0.2 = 2.2$ volts
23b	Calculate $V_2 + V_6$	V_{11}	$2 + 0.8 = 2.8$ volts
24a	Calculate $V_8 + V_7$	V_{12}	$0.1 + 0.2 = 0.3$ volt

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
24b	Calculate $V_8 + V_6$	V_{13}	$0.1 + 0.8 = 0.9$ volt
25	Calculate $V_8 + V_9$	V_{14}	$0.1 + 0.1 = 0.2$ volt
(B)	*Cut and Try Circuit Design*		
1	Assume E_2	E_2	Let $E_2 = -16$ volts $\pm 5\%$; $\overline{E_2} = -15.2$ v; $\underline{E_2} = -16.8$ v
2a	Calculate $\frac{(1 + \Delta r)}{(1 - \Delta r)}$	K_1	$\frac{1.07}{0.93} = 1.15$
2b	Calculate $\frac{(1 + \Delta e)}{(1 - \Delta e)}$	K_2	$\frac{1.05}{0.95} = 1.105$
2c	Calculate $\frac{I_1}{\beta_{min}}$	K_3	$\frac{17.5}{15.67} = 1.117$ ma
2d	Calculate $I_2 + I_0 + 2I_4$	K_4	$0.1 + 1.0 + 0.08 = 1.18$ ma
2e	Calculate $\frac{V_6 - V_9}{V_8 + V_9 - \overline{E_2}}$	K_5	$\frac{0.8 - 0.1}{0.1 + 0.1 + 15.2} = 0.0454$ volts
3	Calculate $\overline{R_4} \leq \frac{1}{K_3}\left[\frac{V_{10} - V_1}{K_1K_5} - K_1 (V_1 - \underline{E_2})\right]$		$\frac{1}{1.117}\left[\frac{2.2 - 0.35}{(1.15)(0.0454)} - 1.15 (0.35 + 16.8)\right] = 14.03$ K
4	Choose R_4	R_4	Let $R_4 = 13K \pm 7\%$; $\overline{R_4} = 13.91$ K; $\underline{R_4} = 12.09$ K
5	Calculate $\underline{R_3} \geq K_5 \overline{R_4}$		$(0.0454)(13.91K) = 0.632$ K
6	Choose R_3	R_3	Let $R_3 = 0.68$ K $\pm 7\%$; $\overline{R_3} = 0.7276$ K; $\underline{R_3} = 0.6324$ K
7	Check R_3 by calculating $\overline{R_3} \leq \frac{\underline{R_4}(V_{10} - V_1)}{V_1 - \underline{E_2} + K_3 \underline{R_4}}$		$\frac{(12.09 K)(2.2 - 0.35)}{0.35 + 16.8 + (1.117)(12.09)} = 0.730$ K; choice of R_3 satisfactory
8	Calculate $\frac{\overline{R_4}}{-V_5 - \overline{E_2} - I_5 \overline{R_4}}$	K_6	$\frac{13.91 K}{-0.5 + 15.2 - (0.14)(13.91)} = 1.091$ K/V

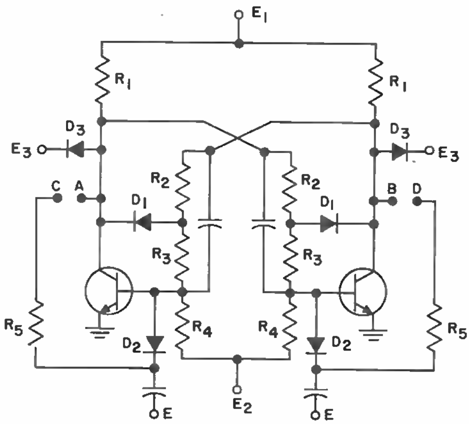
NON-SATURATING FLIP-FLOP DESIGN PROCEDURE (CONTINUED)

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
9	Calculate $\underline{R}_2 \geq \frac{K_6 (V_2 + V_5) - \underline{R}_3}{1 - K_6 I_4}$		$\frac{(1.091)(2.0 + 0.5)\,K - 0.632\,K}{1 - (1.091)(0.04)} = 2.19\,K$
10	Choose R_2 – *If there are difficulties at this point, assume a different E_2.*	R_2	Let $R_2 = 2.7\,K \pm 7\%$; $\overline{R}_2 = 2.889\,K$; $\underline{R}_2 = 2.511\,K$
11	Calculate $\frac{K_1^2 [V_3 - V_{12} + K_4 \underline{R}_2]}{V_4 - V_{11}}$	K_7	$\frac{(1.15)^2[9.0 - 0.3 + (1.18)(2.511)]}{13.0 - 2.8} = 1.51$
12	Calculate $\overline{E}_1 \leq \frac{K_7 V_4 - V_3}{K_7 - 1/K_2}$		$\frac{(1.51)(13.0) - 9.0}{1.51 - 1/1.105} = 17.63$
13	Choose E_1	E_1	Let $E_1 = 16$ volts $\pm 5\%$; $\overline{E}_1 = 16.8$ volts; $\underline{E}_1 = 15.2$ volts
14	Calculate $\overline{R}_1 \leq \frac{(\underline{E}_1 - V_3)\,\underline{R}_2}{V_3 - V_{12} + K_4 \underline{R}_2}$		$\frac{(15.2 - 9.0)(2.511)}{9.0 - 0.3 + (1.18)(2.511)} = 1.335\,K$
15	Calculate $\underline{R}_1 \geq \frac{(\overline{E}_1 - V_4)(\overline{R}_2)}{V_4 - V_{11}}$		$\frac{(16.8 - 13.0)(2.889)}{13.0 - 2.8} = 1.077\,K$
16	Choose R_1	R_1	Let $R_1 = 1.2\,K \pm 7\%$; $\overline{R}_1 = 1.284\,K$; $\underline{R}_1 = 1.116\,K$

(C) *Design Checks*

1	Check "off" stability. Reverse bias voltage is given by: $V_{EB} \leq \overline{E}_2 + \frac{\overline{R}_4}{\overline{R}_4 + \underline{R}_3 + \underline{R}_2}[V_2 - \overline{E}_2 + I_4 \underline{R}_2 + I_5 (\underline{R}_2 + \underline{R}_3)]$ Circuit stable if $V_{EB} \leq -V_5$	V_{EB}	$-15.2 + \frac{13.91}{17.05}[2 + 15.2 + (0.04)(2.511) + (0.14)(3.14)] = -0.7$ volts. The design value of V_5 was 0.5 volts. Therefore, the "off" condition is stable.

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
2	Check for non-saturation under the worst conditions. $V_{BE} \le \bar{E}_2 + \frac{\bar{R}_4 (V_{13} - \bar{E}_2)}{\bar{R}_4 + \underline{R}_3}$ Circuit non-saturated if $V_{BE} \le V_{14}$	V_{BE}	$-15.2 + \frac{13.91\ (0.9 + 15.2)}{14.54} = 0.19$ volts The design maximum of V_{14} was 0.2 volts.
3 3a	Check for stability. Calculate: $R_A = \bar{R}_1 + \bar{R}_2$	R_A	$1.284 + 2.889 = 4.173$ K
3b	$R_B = \bar{R}_1 + \bar{R}_2 + \bar{R}_3 + \underline{R}_4$	R_B	$1.284 + 2.889 + .728 + 12.09 = 16.99$ K
3c	$R_C = \bar{R}_3 + \underline{R}_4$	R_C	$.728 + 12.09 = 12.82$ K
3d	$E'_1 = \underline{E}_1 - K_4 \bar{R}_1$	E'_1	$15.2 - (1.18)(1.284) = 13.68$ volts
3e	$R_D = \underline{R}_1 + \bar{R}_2 + \bar{R}_3 + \bar{R}_4$	R_D	$1.116 + 2.889 + .728 + 13.91 = 18.643$ K
3f	$I_6 = \frac{R_D (\bar{E}_1 - V_2) - \underline{R}_1 [\bar{E}_1 - \underline{E}_2 - I_5 \bar{R}_4 - I_4 (\bar{R}_3 + \bar{R}_4)]}{\underline{R}_1 (R_D - \underline{R}_1)}$	I_6	$\frac{18.64\ (16.8 - 2) - 1.116\ [16.8 + 16.8 - (0.14)(13.91) - (.04)(.728 + 13.91)]}{1.116\ (18.64 - 1.116)} = 12.34$ ma
3g	$I_7 = \frac{R_B}{R_A R_C} (E'_1 - V_{10}) - \frac{1}{R_C} (E'_1 - \underline{E}_2)$	I_7	$\frac{16.99}{(4.173)(12.82)} (13.68 - 2.2) - \frac{(13.68 + 16.8)}{12.82} = 1.266$ ma
3h	$I_8 = \frac{I_1 + I_6 + I_7}{\beta_{min} + \underline{R}_4 / R_C}$	I_8	$\frac{0.2 + 12.34 + 1.266}{15.67 + 12.09/12.82} = 0.831$ ma
3i	$V'_{BE} = \underline{E}_2 + \frac{\underline{R}_4}{R_B} \left(1 + \frac{R_A}{R_C} \right) (E'_1 - \underline{E}_2) - \frac{\underline{R}_4}{R_C} (E'_1 - V_{10}) - I_8 \frac{\underline{R}_4}{R_B} \left(\frac{R_A \underline{R}_4}{R_C} - R_A - \bar{R}_3 \right)$	V'_{BE}	$-16.8 + \frac{12.09}{16.99} \left(1 + \frac{4.173}{12.818}\right) (13.683 + 16.8) - \frac{12.09}{12.818} (13.683 - 2.2) - 0.831 \frac{12.09}{16.99} \left(\frac{(4.173)(12.09)}{12.818} - 4.173 - 0.7276 \right) = .55V$ .55V is greater than $V_1 = .35V$, therefore the design is satisfactory.



[SYMBOLS DEFINED IN FIGURE 11.2 (A)]

CIRCUIT CONFIGURATIONS FOR NON-SATURATING FLIP-FLOP WITH CLAMPED OFF VOLTAGE

FIGURE 11.4

The non-saturating flip-flop design procedure just discussed has been extended to the circuit in Figure 11.4. This circuit is identical to that in Figure 11.2(A) except that a diode clamp (D_3E_3) determines the collector off voltage. A number of design solutions which have been calculated for a nominal 10 ma flip-flop and 5 volt logic level are shown in Figure 11.5. The standard conditions chosen are wide enough to include diode and transistor parameter variations from $-55°C$ to $75°C$ junction temperature. The solutions use only standard RTMA resistor values which are permitted to change up to ±10% during life.

$I_C(I_1)$ max ma.	I_{LOAD} Out (I_0) ma	Deviation from STD Conditions	$\Delta e = \pm 5\%$ $\Delta r = \pm 7\%$				$\Delta e = \pm 5\%$ $\Delta r = \pm 10\%$				$\Delta e = \pm 10\%$ $\Delta r = \pm 7\%$			
			R_1	R_2	R_3	R_4	R_1	R_2	R_3	R_4	R_1	R_2	R_3	R_4
10	1.0	–	2.7	2.4	.82	11	2.2	2.0	.68	9.1	2.4	2.2	.75	10
10	1.5	–	2.4	2.4	.82	11	2.2	2.2	.68	9.1	2.2	2.4	.75	10
15	1.0	–	1.8	1.5	.56	7.5	1.5	1.2	.47	6.2	1.8	1.5	.51	6.8
15	1.5	–	1.8	1.5	.56	7.5	1.5	1.3	.47	6.2	1.8	1.5	.51	6.8
10	1.25	$V_8 = .2v$ max	3.0	3.0	.91	13	2.2	2.0	.68	9.1	2.2	2.2	.75	10
10	1.25	$V_1 = .5v$ max	2.7	2.7	.91	12	2.4	2.7	.82	11	2.4	2.7	.82	11
10	1.25	$V_1 = .4v$ max	3.3	3.6	1.1	15	2.4	2.7	.91	12	2.7	3.0	1.0	13
10	1.25	$V_6 = .6v$ max	4.7	8.2	1.3	24	4.3	7.5	1.20	22	4.3	9.1	1.3	24

Standard Conditions: $E_1 = 18v$, $E_2 = -12v$, $E_3 = 6v$, $0.8v > V_{DIODE}$ (V_6, V_7) $> 0.2v$, $I_{DIODE\ LEAKAGE}$ ($I_4 < .04$ ma, $I_{CO} < .1$ ma, $2v > V_{CE\ ON}$ (V_2, V_8) $> 0v$, V_{BE} (V_1) $< .55v$, V_{EB} (V_5) $> .2v$, V_{BC} (V_9) $< .1v$, $I_{LOAD\ IN}$ (I_1) $= .2$ ma, $7.1v > V_{CE\ OFF}$ (V_3, V_4) $> 5.9v$, $h_{FE} = 18$ min. All resistor values in kilohms.

PRACTICAL CIRCUITS, BASED ON FLIP-FLOP CONFIGURATION IN FIGURE 11.4 (SYMBOLS DEFINED IN NON-SATURATING FLIP-FLOP DESIGN PROCEDURE)

FIGURE 11.5

The high on voltage ($V_{CE\ sat}$, V_2) when the transistor is conducting is primarily the result of the assumed forward voltage of the diode. It is seen that raising the minimum collector to emitter voltage (V_8) from 0 to 0.2 volts has a minor effect on the solutions. $V_8 = 0.1v$ gave identical solutions to $V_8 = 0.2v$.

The last solution in Figure 11.5 shows that a high conductance diode permits more efficient design.

The capacitors in the circuit are determined by the frequency response of the transistor or by the maximum trigger pulse repetition rate.

Type Number	Ambient Temperature Range in Degrees Centigrade Assuming Worst Case I_{CO} and h_{FE}	Potential Switching Speed	Type
2N43	—55 to 45	low	PNP
2N123	—55 to 60	med	PNP
2N396	—55 to 60	med	PNP
2N397	—55 to 60	high	PNP
2N404	—10 to 75	med	PNP
2N450	—55 to 60	med	PNP
2N524	25 to 55	low	PNP
2N525	—55 to 55	low	PNP
2N526	—55 to 55	low	PNP
2N527	—55 to 55	low	PNP
2N634	25 to 60	low	NPN
2N635	—55 to 60	med	NPN
2N636	—55 to 60	high	NPN
2N1289	—55 to 60	high	NPN

TRANSISTORS SUITABLE FOR FLIP-FLOP SOLUTIONS IN FIGURE 11.5
FIGURE 11.6

Figure 11.6 lists a number of military and industrial transistors which meet the conditions of the solution. In all cases the maximum ambient temperature is limited by I_{CO} while the minimum ambient temperature is limited by h_{FE}. No switching speeds are given because they depend on the trigger power available as well as on the inherent transistor speed.

TRIGGERING

Flip-flops are the basic building blocks for many computer and switching circuit applications. In all cases it is necessary to be able to trigger one side or the other into conduction. For counter applications, it is necessary to have pulses at a single input make the two sides of the flip-flop conduct alternately. Outputs from the flip-flop must have characteristics suitable for triggering other similar flip-flops. When the counting period is finished, it is generally necessary to reset the counter by a trigger pulse to one side of all flip-flops simultaneously. Shift registers, and ring counters have similar triggering requirements.

In applying a trigger to one side of a flip-flop, it is preferable to have the trigger turn a transistor off rather than on. The off transistor usually has a reverse-biased emitter junction. This bias potential must be overcome by the trigger before switching can start. Furthermore, some transistors have slow turn on characteristics resulting in a delay between the application of the trigger pulse and the actual switching. On the other hand, since no bias has to be overcome, there is less delay in turning off a transistor. As turn-off begins, the flip-flop itself turns the other side on.

A lower limit on trigger power requirements can be determined by calculating the base charge required to maintain the collector current in the on transistor. The trigger source must be capable of neutralizing this charge in order to turn off the transistor. It has been determined that the base charge for a non-saturated transistor is approximately $Q_B = 1.22\ I_C/2\pi f_\alpha$. The turn-off time constant is approximately $h_{FE}/2\pi f_\alpha$. This indicates that circuits utilizing high speed transistors at low collector currents will require the least trigger power. Consequently, it may be advantageous to use high speed transistors in slow circuitry if trigger power is critical. If the on transistor was in saturation, the trigger power must also include the stored charge. The stored charge is given by

$$Q_S = \frac{1}{2\pi}\left(\frac{1}{f_\alpha} + \frac{1}{f_{\alpha I}}\right)\left(\frac{1}{1 - \alpha_N \alpha_I}\right)\left(I_{B1} - \frac{I_C}{h_{FE}}\right)$$

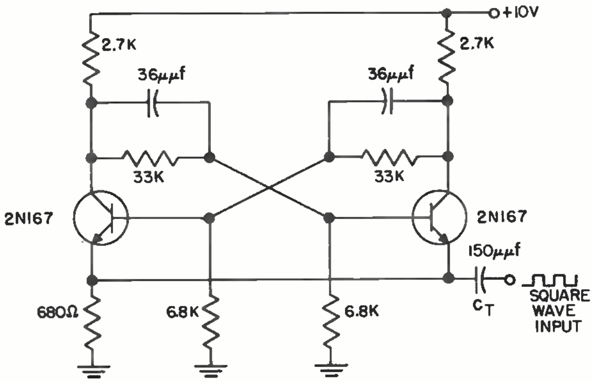
where the symbols are defined in the section on transient response time.

Generally, the trigger pulse is capacitively coupled. Small capacitors permit more frequent triggering but a lower limit of capacitance is imposed by base charge considerations. When a trigger voltage is applied, the resulting trigger current causes the charge on the capacitor to change. When the change is equal to the base charge just calculated, the transistor is turned off. If the trigger voltage or the capacitor are too small, the capacitor charge may be less than the base charge resulting in incomplete turn-off. In the limiting case $C = \frac{Q_B}{V_T}$. The speed with which the trigger turns off a transistor depends on the speed in which Q_B is delivered to the base. This is determined by the trigger source impedance and r'_b.

In designing counters, shift registers or ring counters, it is necessary to make alternate sides of a flip-flop conduct on alternate trigger pulses. There are so-called steering circuits which accomplish this. At low speeds, the trigger may be applied at the emitters as shown in Figure 11.7. It is important that the trigger pulse be shorter than the cross coupling time constant for reliable operation. The circuit features few parts and a low trigger voltage requirement. Its limitations lie in the high trigger current required.

At this point, the effect of trigger pulse repetition rate can be analyzed. In order that each trigger pulse produce reliable triggering, it must find the circuit in exactly the same state as the previous pulse found it. This means that all the capacitors in the circuit must stop charging before a trigger pulse is applied. If they do not, the result is equivalent to reducing the trigger pulse amplitude. The transistor being turned off presents a low impedance permitting the trigger capacitor to charge rapidly. The capacitor must then recover its initial charge through another impedance which is generally much higher. The recovery time constant can limit the maximum pulse rate.

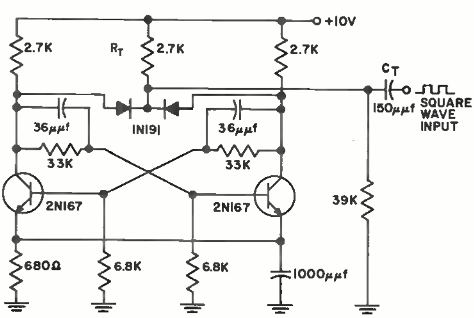
Steering circuits using diodes are shown in Figures 11.8 and 11.9. The collectors are triggered in 11.8 by applying a negative pulse. As a diode conducts during triggering, the trigger pulse is loaded by the collector load resistance. When triggering is accomplished, the capacitor recovers through the biasing resistor R_T. To minimize



EMITTER TRIGGERING
MAXIMUM TRIGGER RATE EXCEEDS 500 KCS WITH TRIGGER AMPLITUDE FROM 2V TO 12V

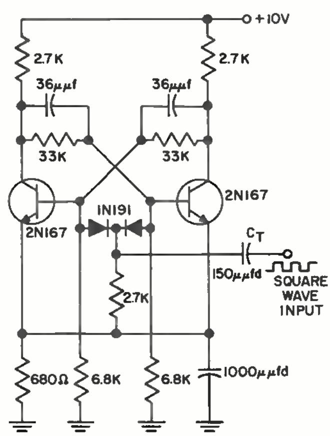
FIGURE 11.7

trigger loading, R_T should be large; to aid recovery, it should be small. To avoid the recovery problem mentioned above, R_T can be replaced by a diode as shown in 11.10. The diode's low forward impedance ensures fast recovery while its high back impedance avoids shunting the trigger pulse during the triggering period.



COLLECTOR TRIGGERING
MAXIMUM TRIGGER RATE EXCEEDS 1MC WITH TRIGGER AMPLITUDE FROM 4V TO 12V.

FIGURE 11.8

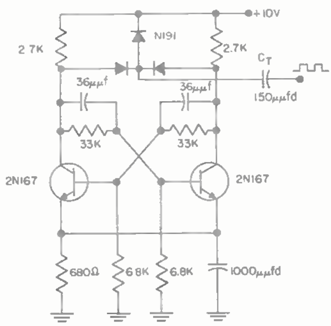


BASE TRIGGERING
MAXIMUM TRIGGER RATE EXCEEDS 1 MC WITH TRIGGER AMPLITUDE FROM 0.75 TO 13 VOLTS.

FIGURE 11.9

Collector triggering requires a relatively large amplitude low impedance pulse but has the advantage that the trigger pulse adds to the switching collector waveform to enhance the speed. Large variations in trigger pulse amplitude are also permitted.

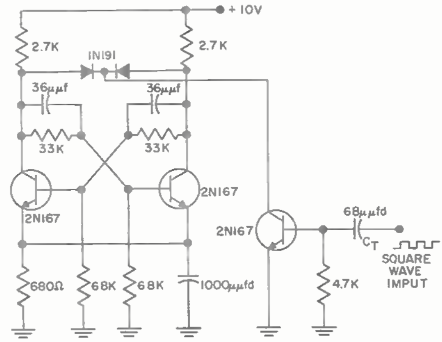
In designing a counter, it may be advantageous to design all stages identically the same to permit the economies of automatic assembly. Should it prove necessary to increase the speed of the early stages, this can be done by adding a trigger amplifier as shown in Figure 11.11 without any change to the basic stage.



COLLECTOR TRIGGERING

DIODE TO SUPPLY VOLTAGE REDUCES TRIGGER POWER AND EXTENDS MAXIMUM TRIGGER RATE

FIGURE 11.10



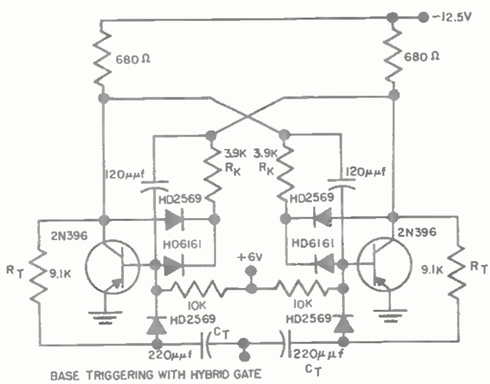
COLLECTOR TRIGGERING WITH TRIGGER AMPLIFIER

FOR 1MC TRIGGER RATE LESS THAN 1 VOLT TRIGGER AMPLITUDE REQUIRED.

FIGURE 11.11

Base triggering shown in Figure 11.9 produces steering in the same manner as collector triggering. The differences are quantitative with base triggering requiring less trigger energy but a more accurately controlled trigger amplitude. A diode can replace the bias resistor to shorten the recovery time.

Hybrid triggering illustrated in Figure 11.12 combines the sensitivity of base triggering and the trigger amplitude variation of collector triggering. In all the other steering circuits, the bias potential was fixed, in this one the bias potential varies in



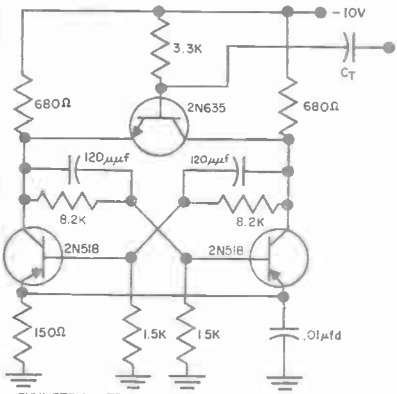
BASE TRIGGERING WITH HYBRID GATE

FIGURE 11.12

order to more effectively direct the trigger pulse. By returning the bias resistor to the collector, the bias voltage is V_{CB}. For the conducting transistor, V_{CB} is much less than for the off transistor, consequently, the trigger pulse is directed to the conducting transistor. This steering scheme is particularly attractive if V_{CB} for the conducting transistor is very small as it is in certain non-saturating circuits such as shown in Figure 10.11.

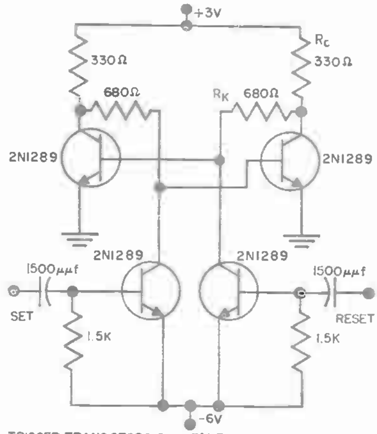
Care should be taken that the time constant C_TR_T does not limit the maximum counting rate. Generally R_T can be made approximately equal to R_K the cross-coupling resistor.

To design a shift register or a ring counter, it is only necessary to return R_T to the appropriate collector to achieve the desired switching pattern. The connections for the shift register are shown in Figure 11.3(A) and (B). A ring counter connection results from connecting the shift register output back to its input as shown in Figure 11.3(C).



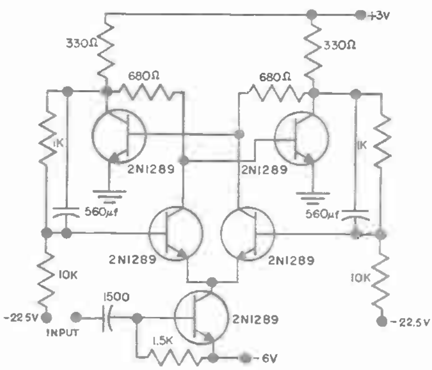
SYMMETRICAL TRANSISTOR TRIGGERS BOTH SIDES OF FLIP-FLOP SIMULTANEOUSLY.

FIGURE 11.13 (A)



TRIGGER TRANSISTORS SIMULTANEOUSLY SUPPLY CURRENT TO TURN OFF ONE SIDE OF FLIP-FLOP AND TO DEVELOP A VOLTAGE ACROSS THE COLLECTOR LOAD ON THE OTHER SIDE

FIGURE 11.13 (B)



CIRCUIT OF FIGURE 11.13(B) WITH TRIGGER STEERING ADDED FOR COUNTER APPLICATION

TRIGGER CIRCUITS

USING TRIGGER POWER TO INCREASE SWITCHING SPEED

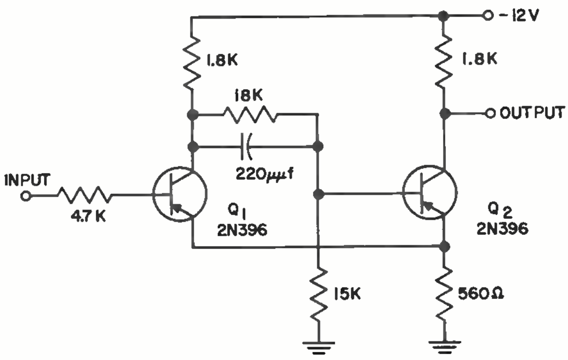
FIGURE 11.13 (C)

By using transistors as trigger amplifiers, some circuits superpose the trigger on the output of the flip-flop so that an output appears even if the flip-flop is still in the transient condition. Figure 11.13(A) shows a symmertical transistor used for steering. The transistor makes the trigger appear in opposite phase at the flip-flop collectors speeding up the transition. The circuit in Figure 11.13(B) can have R_C and R_K so chosen so that a trigger pulse will bring the collector of the transistor being turned on to ground even though the transistor may not have started conducting. The circuit in 11.13(B) may be converted to a steering circuit by the method shown in 11.13(C).

SPECIAL PURPOSE CIRCUITS

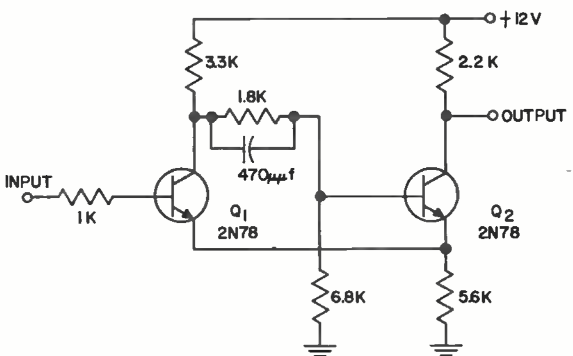
SCHMITT TRIGGER

A Schmitt trigger is a regenerative bistable circuit whose state depends on the amplitude of the input voltage. For this reason, it is useful for waveform restoration, signal level shifting, squaring sinusoidal or non-rectangular inputs, and for DC level detection. Practical circuits are shown in Figure 11.14.



FREQUENCY RANGE 0-500KC
OUTPUT AT COLLECTOR HAS 8V MINIMUM LEVEL CHANGE
Q1 ALWAYS CONDUCTS IF INPUT IS MORE NEGATIVE THAN -5V
Q2 ALWAYS CONDUCTS IF INPUT IS MORE POSITIVE THAN -2V
AMBIENT TEMPERATURE -55°C TO 71°C

(A)



FREQUENCY RANGE 0 TO 1 MC
OUTPUT AT COLLECTOR HAS 2V MINIMUM LEVEL CHANGE
Q1 ALWAYS CONDUCTS IF INPUT EXCEEDS 6.8V
Q2 ALWAYS CONDUCTS IF INPUT IS BELOW 5.2V
AMBIENT TEMPERATURE 0°C TO 71°C

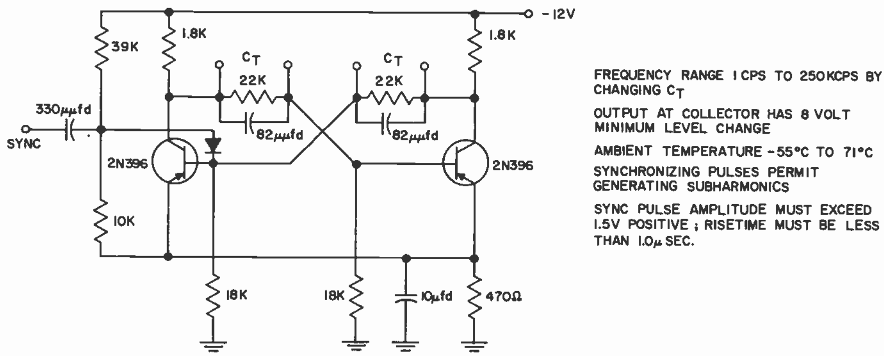
(B)

SCHMITT TRIGGERS
FIGURE 11.14

Circuit operation is readily described using Figure 11.14(B). Assuming Q1 is non-conducting, the base of Q2 is biased at approximately +6.8 volts by the voltage divider consisting of resistors 3.3K, 1.8K and 6.8K. The emitters of both transistors are then at 6.6 volts due to the forward bias voltage required by Q2. If the input voltage is less than 6.6 volts, Q1 is off as was assumed. As the input approaches 6.6 volts, a critical voltage is reached where Q1 begins to conduct and regeneratively turns off Q2. If the input voltage is now lowered below another critical value, Q2 will again conduct.

ASTABLE MULTIVIBRATOR

The term multivibrator refers to a two stage amplifier with positive feedback. Thus a flip-flop is a bistable multivibrator; a "one-shot" switching circuit is a monostable multivibrator and a free-running oscillator is an astable multivibrator. The astable multivibrator is used for generating square waves and timing frequencies and for frequency division. A practical circuit is shown in Figure 11.15. The circuit is symmetrical with the transistors DC biased so that both can conduct simultaneously. The cross-coupling capacitors prevent this, however, forcing the transistors to conduct alternately. The period is approximately $T = \frac{C_T + 100}{40}$ microseconds where C_T is measured in $\mu\mu$f. A synchronizing pulse may be used to lock the multivibrator to an external oscillator's frequency or subharmonic.



ASTABLE MULTIVIBRATOR
FIGURE 11.15

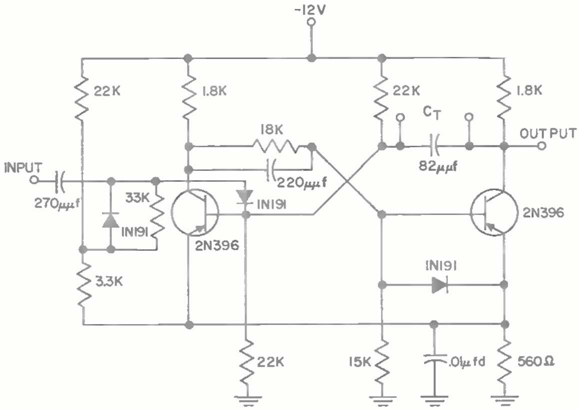
MONOSTABLE MULTIVIBRATOR

On being triggered a monostable multivibrator switches to its unstable state where it remains for a predetermined time before returning to its original stable state. This makes the monostable multivibrator useful in standardizing pulses of random widths or in generating time delayed pulses. The circuit is similar to that of a flip-flop except that one cross-coupling network permits AC coupling only. Therefore, the flip-flop can only remain in its unstable state until the circuit reactive components discharge. Two circuits are shown in Figure 11.16 to illustrate timing with a capacitor and with an inductor. The inductor gives much better pulse width stability at high temperatures.

INDICATOR LAMP DRIVER

The control panel of a computer frequently has indicator lamps to permit monitoring the computer's operation. The circuit in Figure 11.17 shows a bistable circuit which permits controlling the lamp by short trigger pulses.

A negative pulse at point A turns on the lamp, which remains on due to regenerative feedback in the circuit. A positive pulse at A will turn off the lamp. The use of complementary type transistors minimizes the standby power while the lamp is off.



(A)

OUTPUT AT COLLECTORS HAS 8 VOLT LEVEL CHANGE

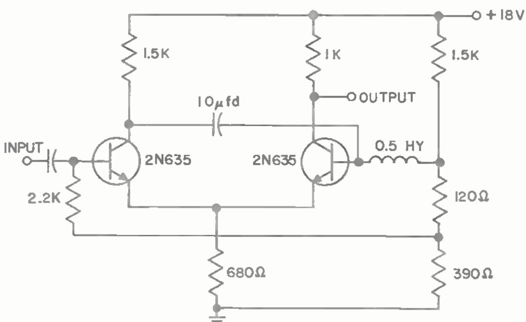
OUTPUT PULSE DURATION 2μSEC TO 1 SEC

MAXIMUM INPUT FREQUENCY 250KC

MAXIMUM REQUIRED INPUT PULSE IS 5 VOLTS

DUTY CYCLE EXCEEDS 60%

AMBIENT TEMPERATURE -55°C TO 71°C



(B)

OUTPUT AT COLLECTOR HAS 5 VOLT LEVEL CHANGE

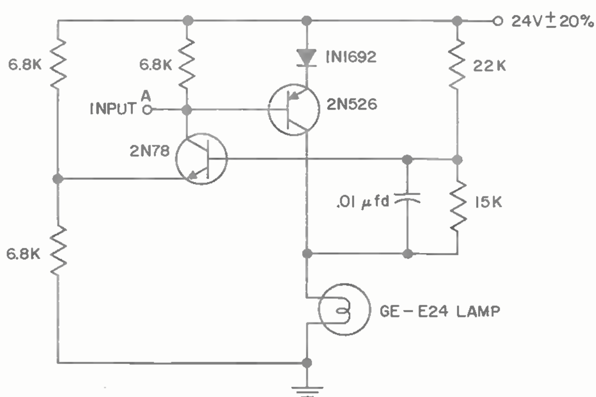
OUTPUT PULSE DURATION APPROX 600 MICROSECONDS

MAXIMUM INPUT PULSE REQUIRED 3 VOLTS

AMBIENT TEMPERATURE -55°C TO 71°C

MONOSTABLE MULTIVIBRATOR

FIGURE 11.16



TRIGGER PULSE REQUIREMENT 2 VOLTS MAXIMUM.
AMBIENT TEMPERATURE -55°C TO 71°C
RESISTOR TOLERANCE ± 10% AT END OF LIFE.

BISTABLE INDICATOR LAMP DRIVER

FIGURE 11.17

12. LOGIC

Large scale scientific computers, smaller machine control computers and electronic animals all have in common the facility to take action without any outside help when the situation warrants it. For example, the scientific computer recognizes when it has completed an addition, and tells itself to go on to the next part of the problem. A machine control computer recognizes when the process is finished and another part should be fed in. Electronic animals can be made to sense obstructions and change their course to avoid collisions. Mathematicians have determined that such logical operations can be described using the conjunctives AND, OR, AND NOT, OR NOT. Boolean algebra is the study of these conjunctives, the language of logic. A summary of the relations and operations of Boolean algebra follow the example of its use below.

Transistors can be used to accomplish logic operations. To illustrate this, an example from automobile operation will be used. Consider the interactions between the ignition switch, the operation of the motor and the oil pressure warning light. If the ignition is off, the motor and light will both be off. If the ignition is turned on, but the starter is not energized the warning lamp should light because the motor has not generated oil pressure. Once the motor is running, the ignition is on and the lamp should be off. These three combinations of ignition, motor and lamp conditions are the only possible combinations signifying proper operation. Note that the three items discussed have only two possible states each, they are on or off. This leads to the use of the binary arithmetic system, which has only two symbols corresponding to the two possible states. Binary numbers will be discussed later in the chapter.

	I	M	L	Result
1	0	0	0	✓
2	0	0	1	X
3	0	1	0	X
4	0	1	1	X
5	1	0	0	X
6	1	0	1	✓
7	1	1	0	✓
8	1	1	1	X

I = IGNITION
M = MOTOR
L = LAMP
R = RESULT
1 = ON
0 = OFF
✓ = ACCEPTABLE
X = UNACCEPTABLE
N = 3 = NO. OF VARIABLES
$2^N = 8$

Table of all possible combinations of ignition, motor and lamp conditions
FIGURE 12.1

To write the expressions necessary to derive a circuit, first assign letters to the variables, e.g., I for ignition, M for motor and L for lamp. Next assign the number one to the variable if it is on; assign zero if it is off. Now we can make a table of all possible combinations of the variables as shown in Figure 12.1. The table is formed by writing ones and zeros alternately down the first column, writing ones and zeros in series of two down the second; in fours down the third, etc. For each additional variable, double the number of ones or zeros written in each group. Only 2^N rows are written, where N is the number of variables, since the combinations will repeat if more rows are added. Indicate with a check mark in the result column if the combination represented in the row is acceptable. For example, combination 4 reads, the ignition is off and the motor is running and the warning light is on. This obviously is an unsatisfactory situation. Combination 7 reads, the ignition is on and the motor is running and the warning light is off. This obviously is the normal situation while driving. If we indicate that the variable is a one by its symbol and that it is a zero by the same symbol, with a bar over it and if we use the symbol plus (+) to mean "OR" and multiplication to mean "AND" we can write the Boolean equation $\overline{I}M\overline{L} + I\overline{M}L + IM\overline{L} = R$ where R means an acceptable result. The three terms on the left hand side are combinations 1, 6, and 7 of the table since these are the only ones to give a check mark in the result column. The plus signs indicate that any of the three combinations individually is acceptable. While there are many rules for simplifying such equations, they are beyond the scope of this book.

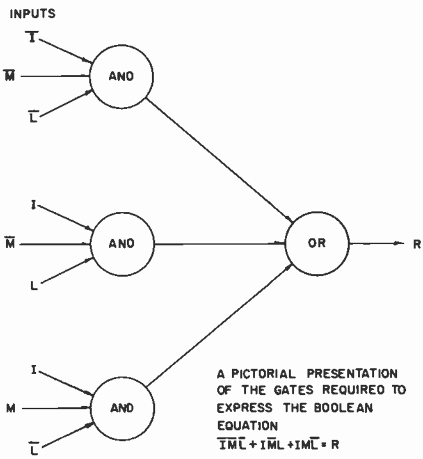


FIGURE 12.2

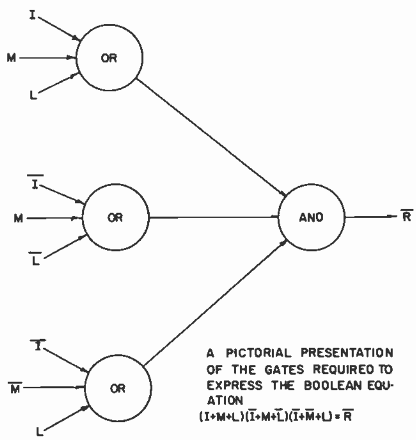


FIGURE 12.3

To express this equation in circuitry, two basic circuits are required. They are named gates because they control the signal passing through. An "AND" gate generates an output only if all the inputs representing the variables are simultaneously applied and an "OR" gate generates an output whenever it receives any input. Our equation translated into gates would be as shown in Figure 12.2. Only if all three inputs shown for an "AND" gate are simultaneously present will an output be generated. The output will pass through the "OR" gate to indicate a result. Note that any equation derived from the table can be written as a series of "AND" gates followed by one "OR" gate.

It is possible to rearrange the equation to give a series of "OR" gates followed by one "AND" gate. To achieve this, interchange all plus and multiplication signs, and remove bars where they exist and add them where there are none. This operation gives us,

$$(I + M + L)(\overline{I} + M + \overline{L})(\overline{I} + \overline{M} + L) = \overline{R}$$

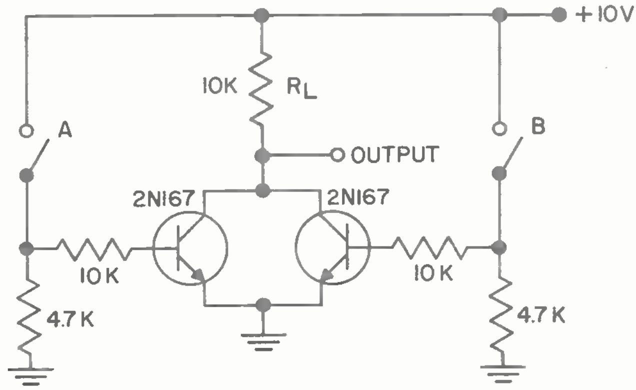
In ordinary language this means if any of the ignition or motor or lamp is on, and simultaneously either the ignition is off or the motor is on or the lamp is off, and simultaneously either the ignition is off or the motor is off or the lamp is on, then the result is unacceptable. Let us apply combination 4 to this equation to see if it is acceptable. The ignition is off therefore the second and third brackets are satisfied. The first bracket is not satisfied by the ignition because it requires that the ignition be on. However, the motor is on in combination 4, satisfying the conditions of the first bracket. Since the requirements of all brackets are met, an output results. Applying combination 7 to the equation we find that the third bracket cannot be satisfied since its conditions are the opposite of those in combination 7. Consequently, no output appears. Note that for this equation, an output indicates an unacceptable situation, rather than an acceptable one, as in the first equation. In gate form, this equation is shown in Figure 12.3.

Table 12.1 summarizes the definitions used with the Boolean equations above and indicates some of the rules which were used to convert the equation represented in Figure 12.2 to that of Figure 12.3. The more conventional symbols a, b, c are used in place of I, M, and L.

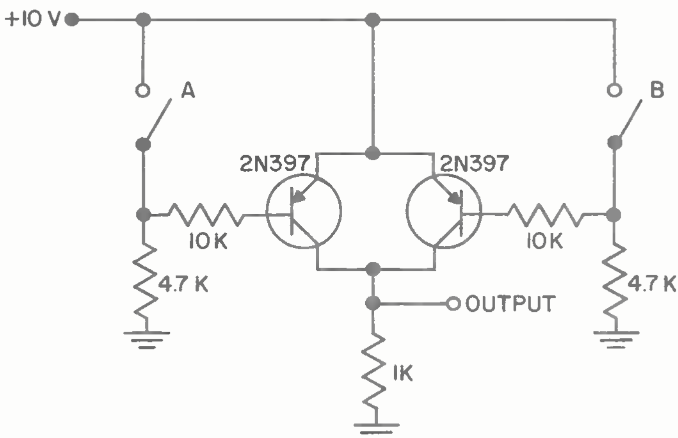
DEFINITIONS	
a, b, c, etc.	Symbols used in equations
ab or $a \cdot b$ or (a)(b)	Reads as "a and b"
$a + b$	Reads as "a or b"
$\bar{a}$	Reads as "not a"
1	Reads as "true" or "on"
0	Reads as "false" or "off"
LAWS	
Commutative Laws	Distributive Law
$a + b = b + a$	$a(b + c) = ab + ac$
$ab = ba$	Special Distributive Law
	$(a + b)(a + c) = a + bc$
Associative Laws	De Morgan's Theorem
$(a + b) + c = a + (b + c)$	$\overline{a + b} = (\bar{a}\bar{b})$ $\quad \overline{ab} = (\bar{a} + \bar{b})$
$(ab)c = a(bc)$	
RELATIONSHIPS	
$1 = \bar{0}$	$0 = \bar{1}$
$a + a = a$	$a \cdot a = a$
$a + 1 = 1$	$a \cdot 1 = a$
$a + \bar{a} = 1$	$a \cdot \bar{a} = 0$
$\bar{\bar{a}} = a$	$a + ab = a(1 + b) = a$

TABLE 12.1

Methods for using transistors in gate circuits are illustrated in Figure 12.4. The base of each transistor can be connected through a resistor either to ground or a positive voltage by operating a switch. In Figure 12.4(A) if both switches are open, both transistors will be non-conducting except for a small leakage current. If either switch A *or* switch B is closed, current will flow through R_L. If we define *closing* a switch as being synonymous with applying an input then we have an "OR" gate. When either switch is closed, the base of the transistor sees a positive voltage, therefore, in an "OR" gate the output should be a positive voltage also. In this circuit it is negative, or "NOT OR". The circuit is an "OR" gate with phase inversion. It has been named a "NOR" circuit. Note that if we define *opening* a switch as being synonymous with applying an input, then we have an "AND" circuit with phase inversion since both switch A *and* switch B must be open before the current through R_L ceases. We see that the same circuit can be an "AND" or an "OR" gate depending on the polarity of the input.



(A) GATE USING NPN TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT, THIS IS AN "OR" GATE
IF OPENING A SWITCH IS AN INPUT, THIS IS AN "AND" GATE
NOTE: PHASE INVERSION OF INPUT

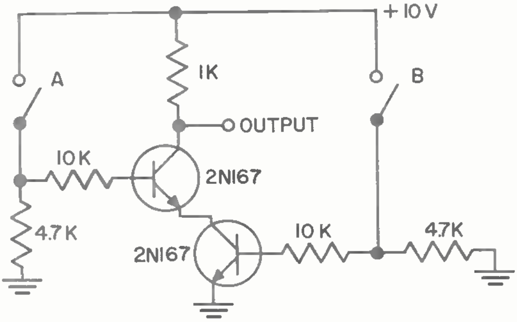


(B) GATE USING PNP TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT THIS IS AN "AND" GATE
IF OPENING A SWITCH IS AN INPUT THIS IS AN "OR" GATE
NOTE: PHASE INVERSION OF INPUT

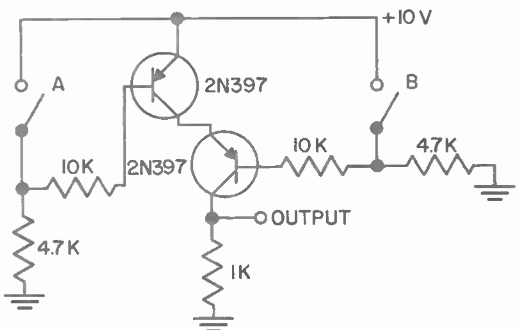
BASIC LOGIC CIRCUITS USING PARALLEL TRANSISTORS
FIGURE 12.4

The circuit in Figure 12.4(B) has identically the same input and output levels but uses PNP rather than NPN transistors. If we define closing a switch as being an input, we find that both switches must be closed before the current through R_L ceases. Therefore, the inputs which made the NPN circuit an "OR" gate make the PNP circuit an "AND" gate. Because of this, the phase inversion inherent in transistor gates does not complicate the overall circuitry excessively.

Figure 12.5(A) and (B) are very similar to Figure 12.4(A) and (B) except that the transistors are in series rather than in parallel. This change converts "OR" gates into "AND" gates and vice versa.



(A) GATE USING NPN TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT THIS IS AN "AND" GATE
IF OPENING A SWITCH IS AN INPUT THIS IS AN "OR" GATE
NOTE: PHASE INVERSION OF INPUT

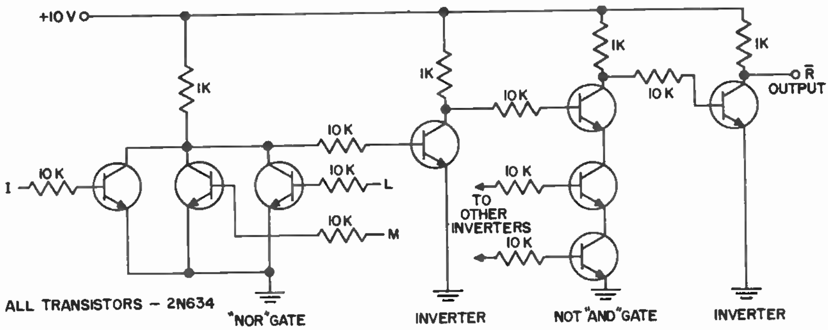


(B) GATE USING PNP TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT THIS IS AN "OR" GATE
IF OPENING A SWITCH IS AN INPUT THIS IS AN "AND" GATE
NOTE: PHASE INVERSION OF INPUT

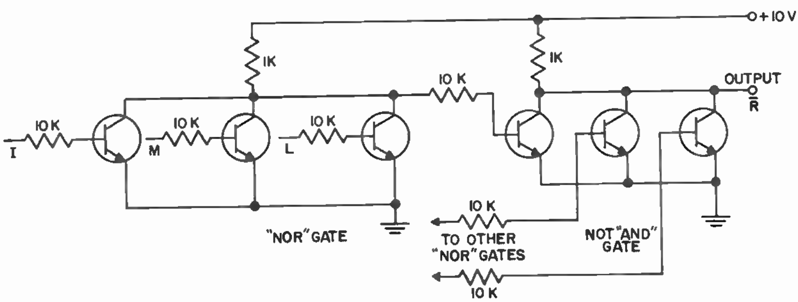
BASIC LOGIC CIRCUITS
USING SERIES TRANSISTORS
FIGURE 12.5

Looking at the logic of Figure 12.3, let us define an input as a positive voltage; a lack of an input as zero voltage. By using the circuit of Figure 12.4(A) with three transistors in parallel, we can perform the "OR" operation but we also get phase inversion. We can apply the output to an inverter stage which is connected to an "AND" gate of three series transistors of the configuration shown in Figure 12.5(A). An output inverter stage would also be required. This is shown in Figure 12.6(A).

By recognizing that the circuit in Figure 12.4(A) becomes an "AND" gate if the input signal is inverted, the inverters can be eliminated as shown in Figure 12.6(B).



(A) INVERTERS COMPENSATE FOR PHASE INVERSION OF GATES



(B) PHASE INVERSION UTILIZED TO ACHIEVE "AND" AND "OR" FUNCTIONS FROM THE SAME CIRCUIT.

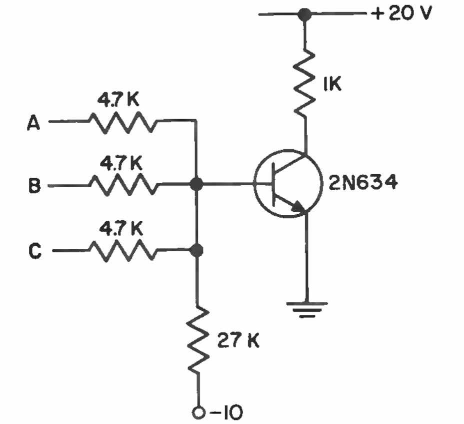
Circuits representing $(I + M + L)(\overline{I} + M + \overline{L})(\overline{I} + \overline{M} + L) = \overline{R}$

FIGURE 12.6

If the transistors are made by processes yielding low saturation voltages and high base resistance, the series base resistors may be eliminated. Without these resistors the logic would be called direct-coupled transistor logic DCTL. While DCTL offers extreme circuit simplicity, it places severe requirements on transistor parameters and does not offer the economy, speed or stability offered by other logical circuitry.

The base resistors of Figure 12.6 relax the saturation voltage and base input voltage requirements. Adding another resistor from each base to a negative bias potential would enhance temperature stability.

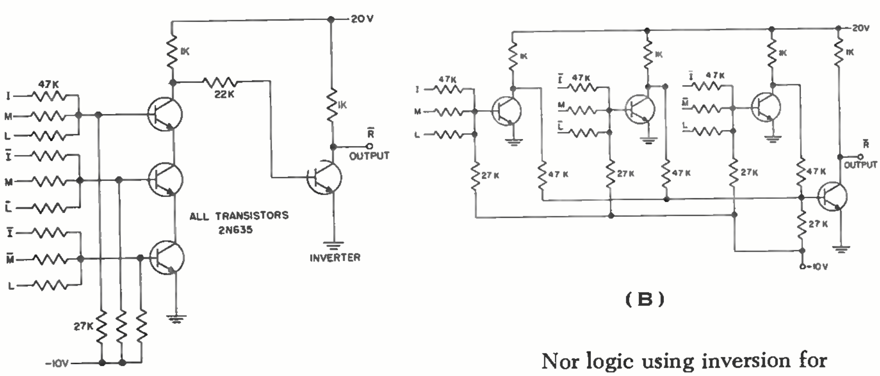
Note that the inputs include both "on" and "off" values of all variables e.g., both I and $\overline{I}$ appear. In order that the gates function properly, I and $\overline{I}$ cannot both be positive simultaneously but they must be identical and oppositely phased, i.e. when I is positive $\overline{I}$ must be zero and vice versa. This can be accomplished by using a phase inverter to generate $\overline{I}$ from I. Another approach, more commonly used, is to take I and $\overline{I}$ from opposite sides of a symmetrical flip-flop.



IF A OR B OR C IS RAISED FROM ZERO TO 12 VOLTS THE TRANSISTOR WILL CONDUCT.

BASIC NOR CIRCUIT
FIGURE 12.7

"NOR" logic is a natural extension of the use of resistors in the base circuit. In the circuit of Figure 12.7, if any of the inputs is made positive, sufficient base current results to cause the transistor to conduct heavily. The "OR" gating is performed by the resistors; the transistor amplifying and inverting the signal. The logic of Figure 12.3 can now be accomplished by combining the "NOR" circuit of Figure 12.7 with the "AND" circuit of Figure 12.5(A). The result is shown in Figure 12.7. In comparing the circuits in Figure 12.6(A) and 12.8, we see that the "NOR" circuit uses one-fourth as many transistors and one-half as many resistors as the brute force approach. In fact if we recall that the equation we are dealing with gives $\overline{R}$ rather than R, we see that we can get R by removing the output phase inverter and making use of the inherent inversion in the "NOR" circuit.



(A)

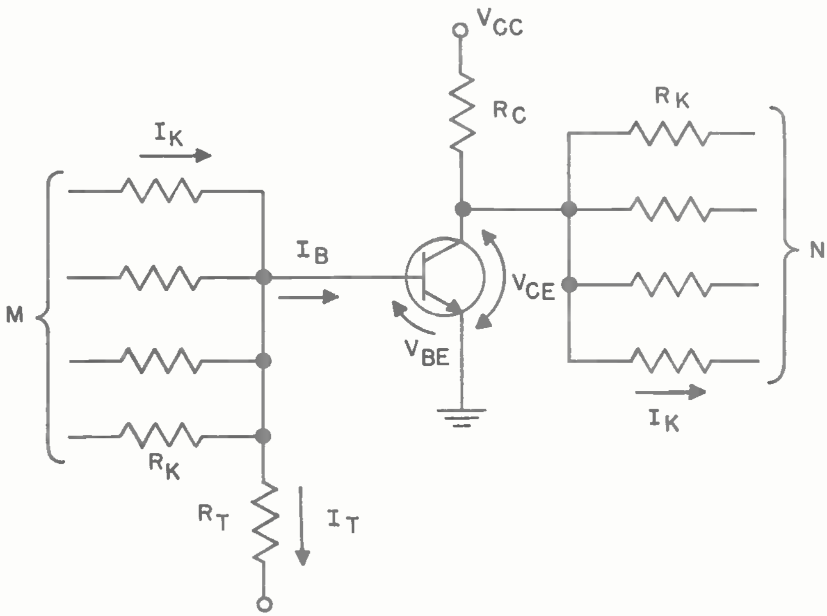
Nor logic using series transistors for "and" gate

(B)

Nor logic using inversion for "and" gate

FIGURE 12.8

Because of the fact that a generalized Boolean equation can be written as a series of "OR" gates followed by an "AND" gate as was shown, it follows that such equations can be written as a series of "NOR" gates followed by a "NOR" gate. The low cost of the resistors used to perform the logic and the few transistors required make "NOR" logic attractive.



DEFINITIONS

I_K = MINIMUM CURRENT THROUGH R_K FOR TURNING TRANSISTOR ON

I_B = MINIMUM BASE CURRENT FOR TURNING TRANSISTOR ON

I_T = BIAS CURRENT TO KEEP TRANSISTOR OFF AT HIGH TEMPERATURES

M = MAX. NUMBER OF INPUTS PERMITTED

N = MAX. NUMBER OF OUTPUTS PERMITTED

V_{BE} = MAX. BASE TO EMITTER VOLTAGE WHEN THE TRANSISTOR IS ON.

V_{CE} = MAX. COLLECTOR TO EMITTER VOLTAGE WHEN THE TRANSISTOR IS ON.

Circuit used for design of NOR circuitry

FIGURE 12.9

A detailed "NOR" building block is shown in Figure 12.9. The figure defines the basic quantities. The circuit can readily be designed with the aid of three basic equations. The first derives the current I_K under the worst loading conditions at the collector of a stage.

$$I_K = \frac{V_{CC} - V_{BE} - I_{COM}R_C}{R_K + NR_C} \quad \ldots\ldots\ \text{where } I_{COM} \qquad (12a)$$

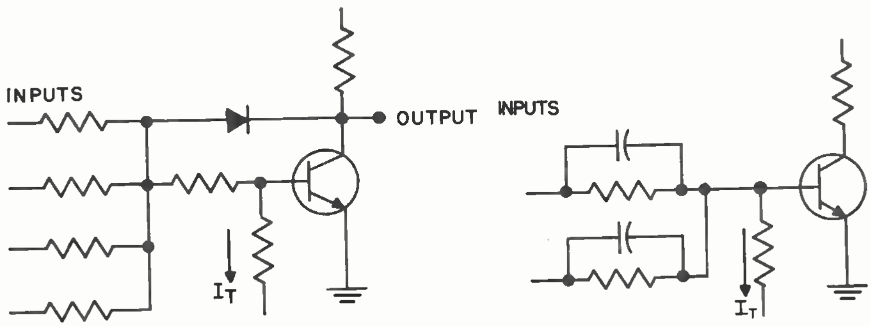
is the maximum I_{CO} that is expected at the maximum junction temperature. The second equation indicates the manner in which I_K is split up at the base of the transistor.

$$I_K = I_B + \frac{M\,(V_{CEM} - V_{CEN} + V_{BE} - V_{EB}) - (V_{BE} - V_{CEN})}{R_K} + I_{COM} \qquad (12b)$$

where V_{CEN} is the minimum expected saturation voltage, V_{CEM} is the maximum expected saturation voltage and V_{EB} is the reverse bias required to reduce the collector current to I_{CO}. V_{EB} is a negative voltage. The third equation ensures that V_{EB} will be reached to turn off the transistor.

$$I_{COM} + \frac{(V_{CEM} - V_{EB})M}{R_K} = I_T \qquad (12c)$$

Knowing I_T and choosing a convenient bias potential permits calculation of R_T. In using these equations, first select a transistor type. Assume the maximum possible supply voltage and collector current consistent with the rating of the transistor and the maximum anticipated ambient temperature. This will ensure optimization of N and M. From the transistor specifications, values of I_{COM}, V_{BE}, V_{CEN}, and I_B (min) can be calculated. I_B (min) is the minimum base current required to cause saturation. R_C is calculated from the assumed collector current. In equation (12a) solve for I_K using the desired value of N and an arbitrary value for R_K. Substitute the value for I_K in equation (12b) along with a chosen value for M and solve for I_B. While superficially I_B need only be large enough to bring the transistor into saturation, increasing I_B will improve the rise time.



CLAMPING DIODE REDUCES STORAGE TIME TO INCREASE SPEED

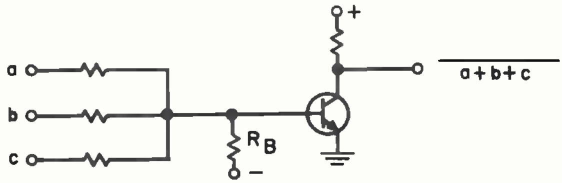
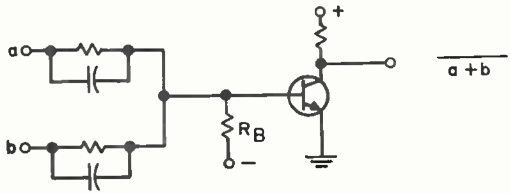
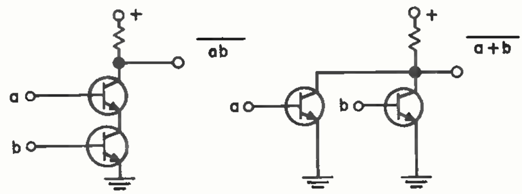
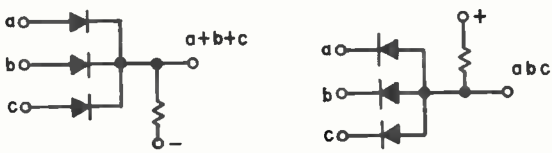
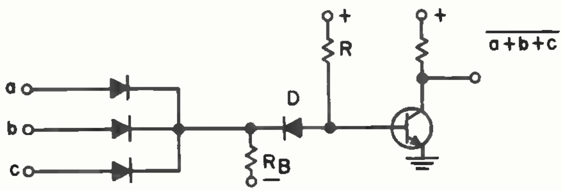
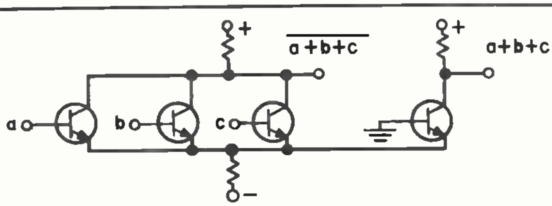
CAPACITORS REDUCE STORAGE TIME TO INCREASE SPEED

(A) (B)

FIGURE 12.10

Circuit speed can also be enhanced by using a diode as shown in Figure 12.10(A) to prevent severe saturation or by shunting R_K by a capacitor as in 12.10(B). The capacitors may cause malfunction unless the stored charge during saturation is carefully controlled; they also aggravate crosstalk between collectors. For this reason it is preferable to use higher frequency transistors without capacitors when additional speed is required.

Table 12.2 lists the characteristics of common logic systems employing transistors.

NAME	TYPICAL CIRCUIT (Positive signals are defined as 1)
RTL Resistor transistor logic (NOR)	
RCTL Resistor capacitor transistor logic	
DCTL Direct coupled transistor logic	
DL Diode logic	
LLL Low level logic	
CML Current mode logic	

COMMON LOGIC SYSTEMS

DESCRIPTION	FEATURES	SUITABLE TRANSISTORS	
		GERMANIUM	SILICON
Logic is performed by resistors. Any positive input produces an inverted output irrespective of the other inputs. Resistor R_B gives temperature stability. (See p. 131)	The circuit design is straightforward. All logical operations can be performed with only this circuit. Many transistors readily meet the steady state requirements.	2N43A* 2N78* 2N167* 2N169A 2N396* 2N525 2N526* 2N635 2N1057	2N335*
Same as RTL except that capacitors are used to enhance switching speed. The capacitors increase the base current for fast collector current turn on and minimize storage time by supplying a charge equal to the stored base charge.	Faster than RTL at the expense of additional components and stringent stored charge requirements.	No standard types are characterized specifically for this logic 2N404* 2N525 2N634 2N1115	
Logic is performed by transistors. V_{CE} and V_{BE}, measured with the transistor in saturation, define the two logic levels. V_{CE} must be much less than V_{BE} to ensure stability and circuit flexibility. (See p. 130)	Very low supply voltages may be used to achieve high power efficiency and miniaturization. Relatively fast switching speeds are practical.	4JD1A68 (PNP Alloy) Surface barrier types	
Logic is performed by diodes. The output is not inverted. Amplifiers are required to maintain the correct logic levels through several gates in series.	Several gates may be used between amplifiers. High speeds can be attained. Non - inversion simplifies circuit design problems. Relatively inexpensive components are used.	2N43A* 2N78* 2N123* 2N167* 2N396* 2N525 2N635	2N333* 2N337*
Logic is performed by diodes. The output is inverted. The diode D isolates the transistor from the gate permitting R to turn on the collector current. By proper choice of components only small voltage changes occur.	The number of inputs to the diode gate does not affect the transistor base current thus giving predictable performance. The small voltage excursions minimize the effects of stray capacitance and enhance switching speed.	2N123* 2N396* 2N525 2N526* 2N635 2N1115	2N335* 2N338*
Logic is performed by transistors which are biased from constant current sources to keep them far out of saturation. Both inverted and non-inverted outputs are available.	Very high switching speeds are possible because the transistors are operated at optimum operating conditions. Although the voltage excursion is small the circuitry is relatively unaffected by noise.	2N1289 Mesa Types	2N337* 2N338*

*Military types.

TABLE 12.2

BINARY ARITHMETIC

Because bistable circuits can be readily designed using a variety of components from switches to transistors, it is natural for counters to be designed to use binary numbers, i.e., numbers to the base, or radix, 2. In the conventional decimal system, a number written as 2904 is really a contraction for $2\times10^3+9\times10^2+0\times10^1+4\times1$. Each place refers to a different power of 10 in ascending order from the right. In the binary system, only two symbols are permitted, 0 and 1. All numbers are constructed on the basis of ascending powers of 2. For example, 11011 means $1\times2^4+1\times2^3+0\times2^2+1\times2^1+1\times1$. This is 27 in the decimal system.

This notation applies also to decimal fractions as well as integers. For example, the number 0.204 is a contraction of $2\times10^{-1}+0\times10^{-2}+4\times10^{-3}$. Similarly, the binary number 0.1011 is a contraction of $1\times2^{-1}+0\times2^{-2}+1\times2^{-3}+1\times2^{-4}$. Using this construction, a table of equivalent binary and decimal numbers can be obtained as shown below.

Binary	*Decimal*	*Binary*	*Decimal*
0	0	0.000	0.000
1	1	0.001	0.125
10	2	0.010	0.250
11	3	0.011	0.375
100	4	0.100	0.500
101	5	0.101	0.625
110	6	0.110	0.750
111	7	0.111	0.875

Arithmetic operations can best be described by comparative examples.

```
Addition                        | Subtraction
        42        101010        |        44        101100
       +18         10010        |       -18         10010
       ---        ------        |       ---         -----
        60        111100        |        26         11010
```

During addition, the digits in a column are added to the carry from the previous column. The result is expressed as a sum digit which is recorded and a carry digit which is applied to the next column. The term digit generally refers to the figures in a decimal number; the term bit (an abbreviation of binary digit) is used with binary numbers. If the digit being subtracted is the larger of the two in the column, the techniques used to handle this situation in decimal subtraction are also applicable in the binary system.

```
Multiplication                  | Division
    42             101010       |       1.35            1.0101
    21              10101       |    5 √6.7500    101 √110.11000
   ---         ----------       |      5              101
    42             101010       |      ----           -------
   84             101010        |      1 7              1 11
   ---           101010         |      1 5              1 01
   882           ----------     |      ----             -------
                 1101110010     |        25               1000
                                |        25                101
                                |                          ---
                                |                          110
```

Multiplying a binary number by two is equivalent to adding a zero to its right hand side, just as multiplying a decimal number by 10 adds a zero. This is equivalent to shifting the number one place to the left. In computers, this operation is done by a shift register. Division can be readily understood since it involves the operations of additions, subtraction and multiplication only.

Computers generally employ circuits called adders which can perform the operation of addition. Adders can also perform other arithmetic operations besides addition. For example, an adder can perform subtraction by the use of a number's complement. The complement is obtained numerically by interchanging all ones and zeros. In equipment the complement can be obtained by taking the output from the opposite side of flip-flops.

The manner in which subtraction with an adder is accomplished is given by the following example:

Problem:	Calculate 1101 − 1001
Complement of	1001 is 0110 (1111 − 1001 = 0110)
Add:	1101 + 0110 = 10011
Add 1	10011 + 1 = 10100
Omit left hand digit to obtain	1101 − 1001 = 100

Flip-flops can be connected in series so that the first flip-flop will alternate states with each input pulse, and successive flip-flops will alternate states at half the rate of the preceding flip-flop. In this way the flip-flops assume a unique configuration of states for a given number of input pulses. The flip-flops actually perform the function of binary counting. A practical circuit of a binary counter is shown in Figure 11.3(B) The count in a binary counter can be determined by noting whether each stage is in the 1 or 0 condition, and then assigning the appropriate power of 2 to the stage to reconstruct the number as in the examples above.

If it is required to count to a base other than 2, a binary counter can be modified to count to the new base.

The rules for accomplishing the modification will be illustrated for a counter to the base 10.

Rule	Example
1) Determine the number of binary stages (N) required to count to the desired new base (M)	M = 10 $2^3 < 10 < 2^4$ N = 4
2) Subtract M from 2^N	$2^4 - 10 = 6$
3) Write the remainder in binary form	6 = 110
4) When the count reaches 2^{N-1}, feed back a one to each stage of the counter having a one in the remainder shown in 3)	$2^{N-1} = 2^3 = 1000$ Feedback added gives 1 110

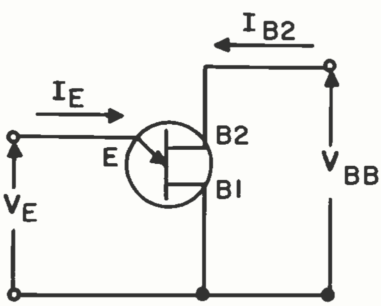
As additional pulses are added beyond the count 2^{N-1}, they will count through to M and then recycle to zero. This method is based on advancing the count at the point 2^{N-1} to the extent that the indicated count is 2^N when M input pulses are applied. The feedback is applied when the most significant place becomes a one but it is imperative that feedback be delayed until the counter settles down in order to avoid interference with the normal counter action.

13. UNIJUNCTION TRANSISTOR CIRCUITS

The unijunction transistor is a three-terminal semiconductor device which has electrical characteristics that are quite different from those of conventional two-junction transistors. Its most important feature is its highly stable negative resistance characteristic which permits its application in oscillator circuits, timing circuits and bistable circuits. Circuits such as sawtooth generators, pulse generators, delay circuits, multivibrators, one-shots, trigger circuits and pulse rate modulators can be greatly simplified by the use of the unijunction transistor.

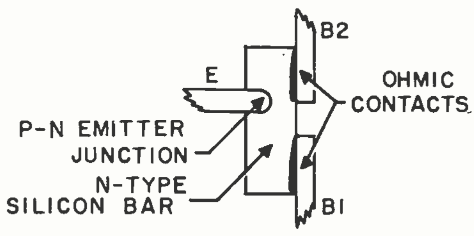
THEORY OF OPERATION

The construction of the unijunction transistor is shown in Figure 13.2. Two ohmic contacts, called base-one (B1) and base-two (B2) are made at opposite ends of a small bar of n-type silicon. A single rectifying contact, called the emitter (E), is made on the opposite side of the bar close to base-two. An interbase resistance, R_{BB}, of between 5K and 10K exists between base-one and base-two. In normal circuit operation, base-one is grounded and a positive bias voltage, V_{BB}, is applied at base-two. With no emitter current flowing, the silicon bar acts like a simple voltage divider (Figure 13.3) and a certain fraction, η of V_{BB} will appear at the emitter. If the emitter voltage, V_E, is less than $\eta\ V_{BB}$, the emitter will be reverse-biased and only a small emitter leakage current will flow. If V_E becomes greater than $\eta\ V_{BB}$, the emitter will be forward biased and emitter current will flow. This emitter current consists primarily of holes injected into the silicon bar. These holes move down the bar from the emitter to base-one and result in an equal increase in the number of electrons in the emitter to base-one region. The net result is a decrease in the resistance between emitter and base-one so that as the emitter current increases, the emitter voltage decreases and a negative resistance characteristic is obtained (Figure 13.5).



Symbol for unijunction transistor with indentification of principle voltages and currents

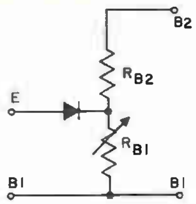
FIGURE 13.1



Construction of unijunction transistor—cross sectional view

FIGURE 13.2

The operation of the unijunction transistor may be best understood by the representative circuit of Figure 13.3. The diode represents the emitter diode, R_{B1} represents the resistance of the region in the silicon bar between the emitter and base-one and R_{B2} represents the resistance between the emitter and base-two. The resistance R_{B1} varies with the emitter current as indicated in Figure 13.4.

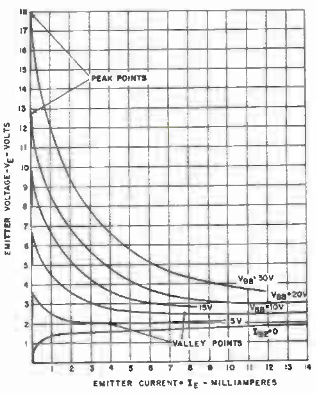


Unijunction transistor representative circuit
FIGURE 13.3

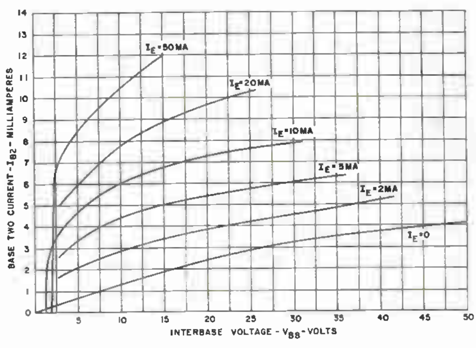
I_E (MA)	R_{B1} (OHMS)
0	4600
1	2000
2	900
5	240
10	150
20	90
50	40

Variation of R_{B1} with I_E in representative circuit (typical 2N492)
FIGURE 13.4

The large signal properties of the unijunction transistor are usually given in the form of characteristic curves. Figure 13.5 gives typical emitter characteristic curves as plots of emitter voltage vs. emitter current for fixed values of interbase voltage. Figure 13.6 gives typical interbase characteristic curves as plots of interbase voltage vs. base-two current for fixed values of emitter current. On each of the emitter characteristic curves there are two points of interest, the peak point and the valley point. On each of the emitter characteristic curves the region to the left of the peak point is called the cut-off region; here the emitter is reverse biased and only a small leakage current flows. The region between the peak point and the valley point is the negative resistance region. The region to the right of the valley point is the saturation region; here the dynamic resistance is positive and lies in the range of 5 to 20Ω.



Typical emitter characteristics (type 2N492)
FIGURE 13.5



Typical interbase characteristics (type 2N492)
FIGURE 13.6

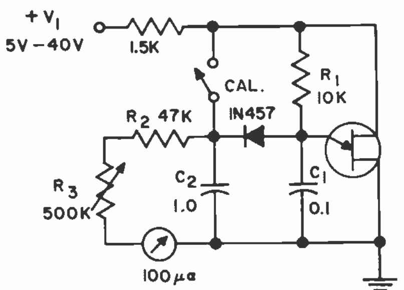
PARAMETERS—DEFINITION AND MEASUREMENT

1. R_{BB} – Interbase Resistance. The interbase resistance is the resistance measured between base-one and base-two with the emitter open circuited. It may be measured with any conventional ohmmeter or resistance bridge if the applied voltage is five volts or less. The interbase resistance increases with temperature at about 0.8%/°C. This temperature variation of R_{BB} may be utilized for either temperature compensation or in the design of temperature sensitive circuits.

2. η – Intrinsic Stand-off Ratio. This parameter is defined in terms of the peak point voltage, V_P, by means of the equation: $V_P = \eta V_{BB} + V_D$ . . . where V_D is about 0.70 volt at 25°C and decreases with temperature at about 3 millivolts/°C. It is

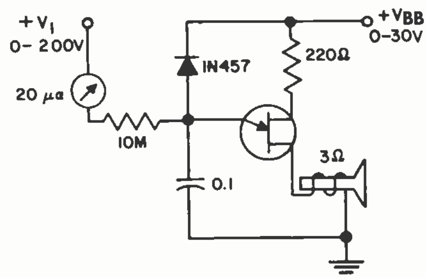
found that η is constant over wide ranges of temperature and interbase voltage. A circuit which may be used to measure η is shown in Figure 13.7. In this circuit R_1, C_1 and the unijunction transistor form a relàxation oscillator and the remainder of the circuit serves as a peak voltage detector with the diode automatically subtracting the voltage V_D. To use the circuit, the voltage V_1 is set to the value desired, the "cal." button is pushed and R_3 adjusted to make the meter read full scale. The "cal" button is then released and the value of η is read directly from the meter (1.0 full scale). If the voltage V_1 is changed, the meter must be recalibrated.

3. I_P – Peak Point Current. The peak point current corresponds to the emitter current at the peak point. It represents the minimum current which is required to fire the unijunction transistor or required for oscillation in the relaxation oscillator circuit. I_P is inversely proportional to the interbase voltage. I_P may be measured in the circuit of Figure 13.8. In this circuit, the voltage V_1 is increased until the unijunction transistor fires as evidenced by noise from the loudspeaker. V_1 is then reduced slowly until the unijunction ceases to fire and the current through the meter is read as I_P.



TEST CIRCUIT FOR INTRINSIC STANDOFF RATIO (η)

FIGURE 13.7



TEST CIRCUIT FOR PEAK POINT EMITTERS CURRENT (IP)

FIGURE 13.8

4. V_P – Peak Point Emitter Voltage. This voltage depends on the interbase voltage as indicated in (2). V_P decreases with increasing temperature because of the change in V_D and may be stabilized by a small resistor in series with base-two.

5. V_E (sat) – Emitter Saturation Voltage. This parameter indicates the forward drop of the unijunction transistor from emitter to base-one when it is conducting the maximum rated emitter current. It is measured at an emitter current of 50 ma and an interbase voltage of 10 volts.

6. I_{B2} (mod) – Interbase Modulated Current. This parameter indicates the effective current gain between emitter and base-two. It is measured as the base-two current under the same condition used to measure V_E (sat).

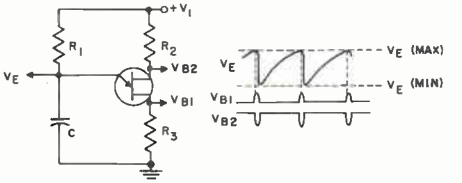
7. I_{EO} – Emitter Reverse Current. The emitter reverse current is measured with 60 volts between base-two and emitter with base-one open circuit. This current varies with temperature in the same way as the I_{CO} of a conventional transistor.

8. V_V – Valley Voltage. The valley voltage is the emitter voltage at the valley point. The valley voltage increases as the interbase voltage increases, it decreases with resistance in series with base-two and increases with resistance in series with base-one.

9. I_V – Valley Current. The valley current is the emitter current at the valley point. The valley current increases as the interbase voltage increases and decreases with resistance in series with base-one or base-two.

RELAXATION OSCILLATOR

The relaxation oscillator circuit shown in Figure 13.9 is a basic circuit for many applications. It is chiefly useful as a timing circuit, a pulse generator, a trigger circuit or a sawtooth wave generator.



BASIC RELAXATION OSCILLATOR WITH TYPICAL WAVEFORMS
FIGURE 13.9

Conditions for Oscillation.

$$\frac{V_1 - V_P}{R_1} > I_p, \quad \frac{V_1 - V_V}{R_1} < I_V$$

It is found that these conditions are very broad permitting a 1000 to 1 range of R_1 from about 2K to 2M. R_2 is used for temperature compensation, its value may be calculated from the equation:

$$R_2 \cong \frac{0.65\ R_{BB}}{\eta V_1} \text{ (units are ohms, volts)}$$

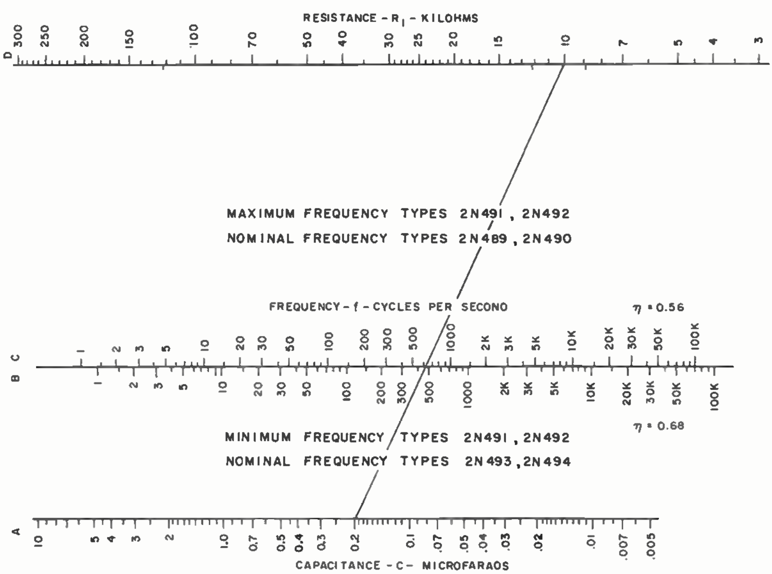
The maximum and minimum voltages of the emitter voltage waveform may be calculated from:

$$V_E\ (\text{max.}) = V_p = \eta V_{BB} + 0.7 \text{ volt}$$
$$V_E\ (\text{min.}) \cong 0.5\ V_E\ (\text{sat})$$

The frequency of oscillation is given by the equation:

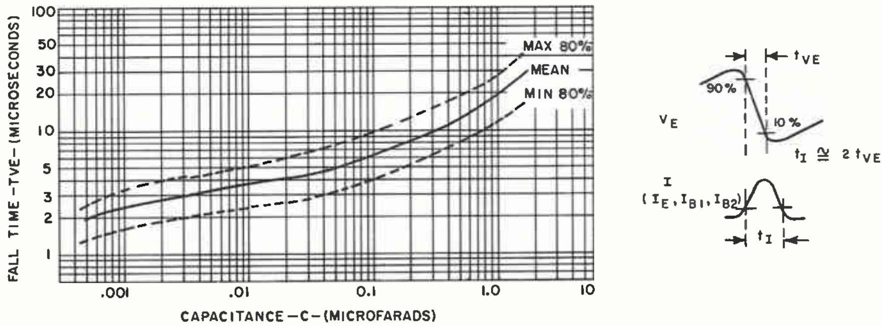
$$f \cong \frac{1}{R_1 C \ln\left(\frac{1}{1-\eta}\right)}$$

and may be obtained conveniently from the nomogram of Figure 13.10.



Nomogram for calculating frequency of relaxation oscillation
FIGURE 13.10

The emitter voltage recovery time, t_{VE}, is defined as the time between the 90% and 10% points on the emitter voltage waveform. The value of t_{VE} is determined primarily by the size of the capacitor C in Figure 13.9 and may be obtained from Figure 13.11.



Recovery time of unijunction transistor relaxation oscillator vs. capacity

FIGURE 13.11

The pulse amplitude at base-one or base-two may be determined from the equations:

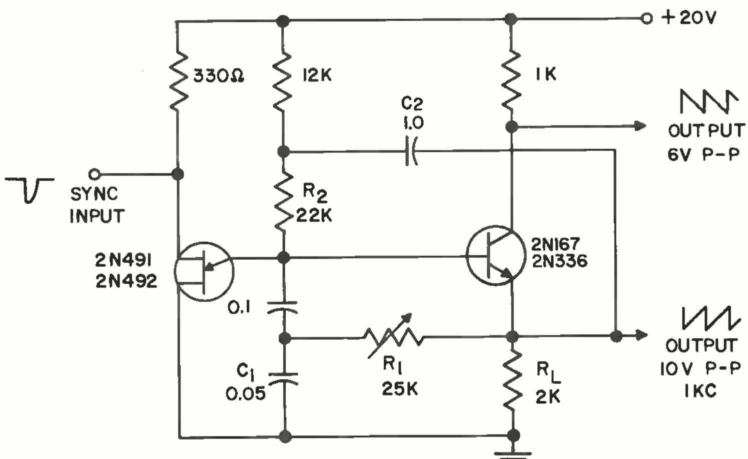
$$I_{E(peak)} \cong \frac{[V_p - 1/2\, V_E(sat)]\,C}{t_{VE}}$$

$$I_{B2(peak)} \cong \frac{I_{B2}\,(mod)}{7} \sqrt{I_{E(peak)}}$$

Units are ma, volts, mμf, μsec.

SAWTOOTH WAVE GENERATOR

The circuit of Figure 13.12 may be used as a linear sawtooth wave generator. The NPN transistor serves as an output buffer amplifier with the capacitor C_2 and resistor R_2 serving in a bootstrap circuit to improve the linearity of the sawtooth. R_1 and C_1 give integrator type feedback which compensates for the loading of the output stage. Optimum linearity is obtained by adjusting R_1. Linearity is 0.3% or more depending on h_{FE} of the NPN transistor.



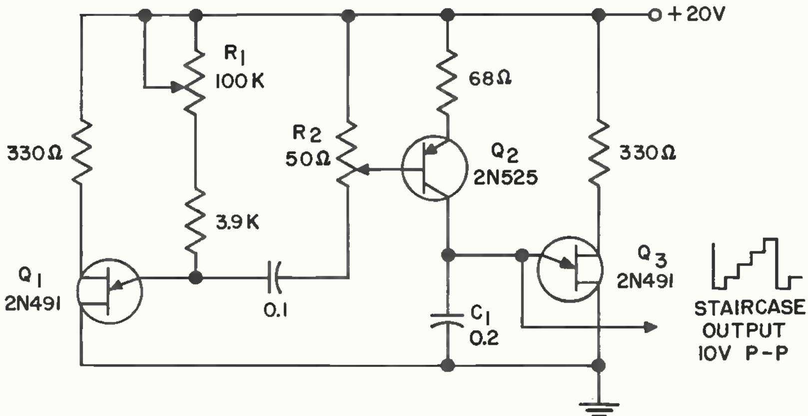
SAWTOOTH GENERATOR WITH HIGH LINEARITY

FIGURE 13.12

STAIRCASE WAVE GENERATOR

Figure 13.13 shows a simple staircase wave generator which has good stability and a wide operating range. The unijunction transistor Q_1 operates as a free running oscillator which generates negative pulses across R_2. These pulses produce current pulses from the collector of Q_2 which charge capacitor C_1 in steps. When the voltage across C_1 reaches the peak point voltage of Q_3 this transistor fires and discharges C_1.

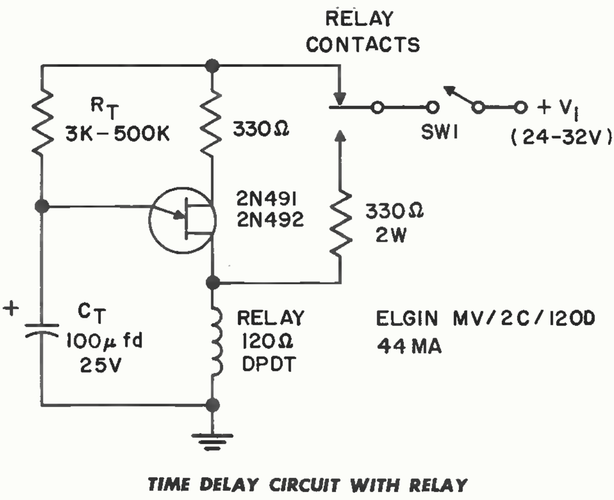
Resistor R_1 determines the frequency of the steps and resistor R_2 determines the number of steps per cycle. The circuit shown can be adjusted for a step frequency from 100 cps to 2 KC and the number of steps per cycle can be adjusted from one to several hundred. This circuit can also be adapted to a frequency divider by cascading stages similar to the stage formed by Q_2 and Q_3.



STAIRCASE WAVE GENERATOR
(FREQUENCY DIVIDER)
FIGURE 13.13

TIME DELAY RELAY

Figure 13.14 shows how the unijunction transistor can be used to obtain a precise delay in the operation of a relay. When the switch SW1 is closed, capacitor C_T is



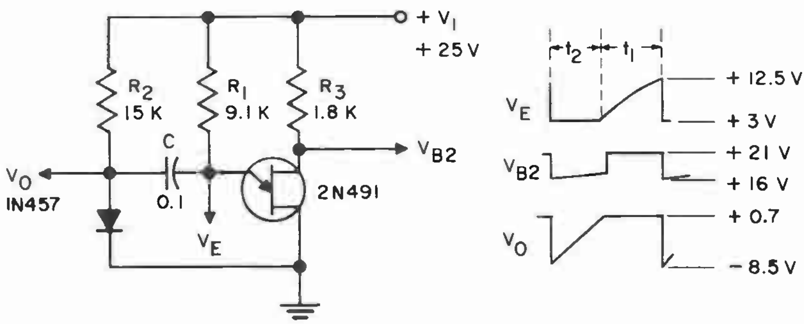
TIME DELAY CIRCUIT WITH RELAY
FIGURE 13.14

charged to the peak point voltage at which time the unijunction transistor fires and the capacitor discharges through the relay thus causing it to close. One set of relay contacts hold the relay closed and the second set of contacts can be used for control functions. To be used in this circuit, relays must have fast operating times, low coil resistance and low operating power.

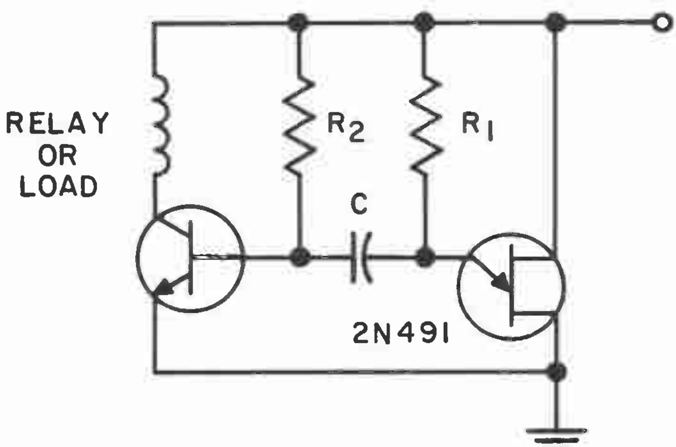
The time delay of this circuit is determined by R_T, about one second of delay is obtained for each 10K of resistance, R_T. The time delay is quite independent of temperature and supply voltage.

MULTIVIBRATOR

Figure 13.15 shows a unijunction transistor multivibrator circuit which has a frequency of about 1 Kc. The conditions for oscillation of this circuit are the same as for the relaxation oscillator. The length of time during which the unijunction transistor is off (no emitter current flowing) is determined primarily by R_1. The length of time during



UNIJUNCTION TRANSISTOR MULTIVIBRATOR WITH TYPICAL WAVE FORMS
FIGURE 13.15



Unijunction transistor multivibrator used to drive NPN transistor
FIGURE 13.16

which the unijunction transistor is on is determined primarily by R_2. The periods may be calculated from the equations:

$$t_1 = R_1C \ln\left[\frac{V_1 - V_E}{V_1 - V_p}\right]$$

$$t_2 = R_2C \ln\left[\frac{V_1 + V_p - V_E}{V_1 - V_p}\right]$$

Where V_E is measured at an emitter current of $I_E = \frac{V_1 (R_1 + R_2)}{R_1R_2}$ and may be obtained from the emitter characteristic curves.

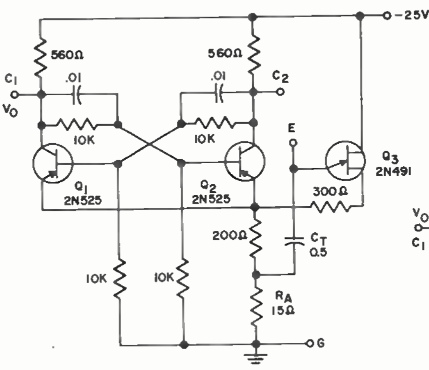
An NPN transistor may be direct coupled to the multivibrator circuit by replacing the diode as shown in Figure 13.16. This circuit has the advantage that the load does not have any effect on the timing of the circuit.

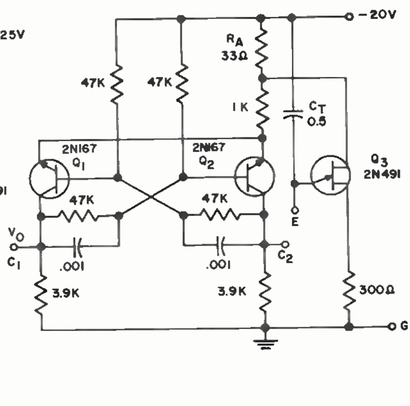
HYBRID TIMING CIRCUITS

The unijunction transistor can be used in conjunction with conventional PNP or NPN transistors to obtain versatile timing circuits such as symmetrical and unsymmetrical multivibrators, one-shot multivibrators, variable frequency oscillators and time delay circuits. The advantages of these circuits include: (1) The output at the collector of each transistor is very nearly an ideal rectangular waveform. (2) The circuits will tolerate large variations in h_{FE} or I_{CO} of the transistors as compared to conventional circuits. (3) The circuits are not prone to "lock-up" or non-oscillation. (4) The timing stability is excellent. (5) A single small timing capacitor C_T can be used, avoiding the use of electrolytic capacitors in many applications.

The hybrid timing circuits can use either germanium or silicon transistors as desired. The basic circuits for PNP or NPN transistors are shown in Figures 13.17 and 13.18. In both of these circuits, the junction transistors form a conventional flip-flop with the unijunction transistor serving the timing and triggering functions. Each time the unijunction transistor fires the discharge current from the capacitor C_T develops a pulse across R_A which triggers the flip-flop from one state to the other.

The basic circuits as shown in Figures 13.17 and 13.18 will operate at frequencies from about 1 cps to 500 cps and at temperatures above 75°C. Frequencies from 1 cycle per minute to 100 KC can be obtained by proper choice of C_T and R_A and suitable flip-flop design. The operating temperature range may be extended to 150°C by the use of silicon transistors.



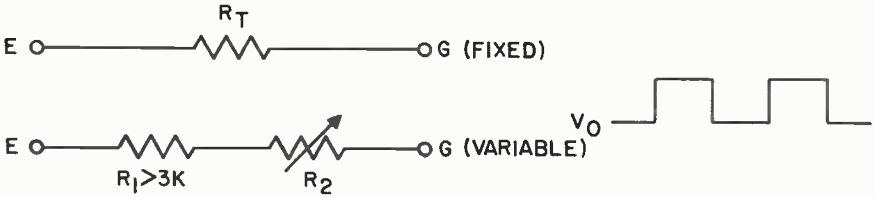


BASIC HYBRID TIMING CIRCUITS USING PNP AND NPN TRANSISTORS

FIGURE 13.17 FIGURE 13.18

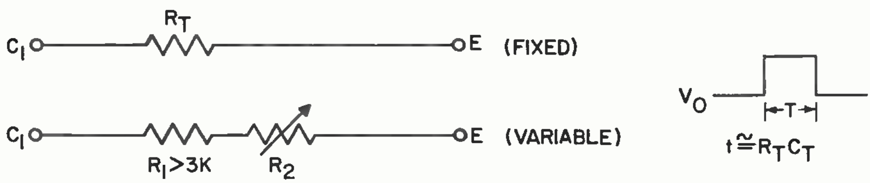
The basic hybrid timing circuits in Figures 13.17 and 13.18 can be adapted to perform desired functions by connecting resistors or potentiometers between the points in the circuit (C_1, C_2, E, G) as indicated below.

(A) Symmetrical Multivibrator — Square Wave Generator



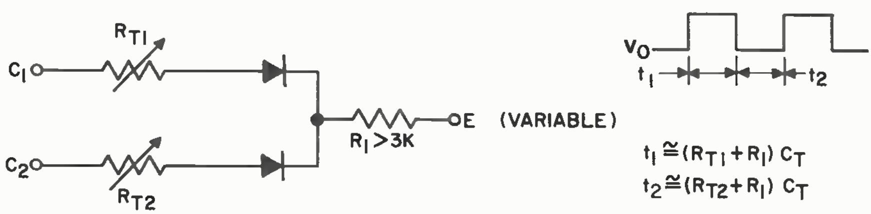
Connecting the resistor between points E and G in the basic circuits gives a square wave generator which has perfect symmetry. By the use of a 2 megohm potentiometer the frequency may be varied continuously from 1 cps to 500 cps. The frequency is $f = 1/2\, R_T C_T$.

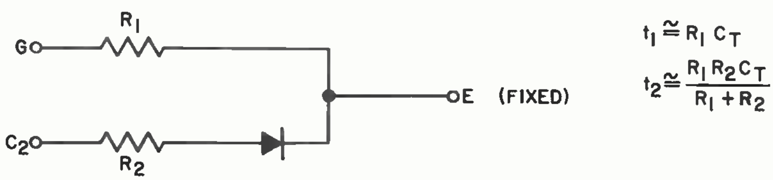
(B) One-Shot Multivibrator



The collector of Q_2 will be positive in the quiescent state. A positive pulse at the base of Q_2 in Figure 13.17 or a negative pulse at the base of Q_1 in Figure 13.18 will trigger the circuit. At the end of the timing interval, the unijunction transistor will fire and cause the circuit to revert to its quiescent state. This circuit has the advantage of a fast recovery time so it may be operated at a high duty ratio without any loss of accuracy.

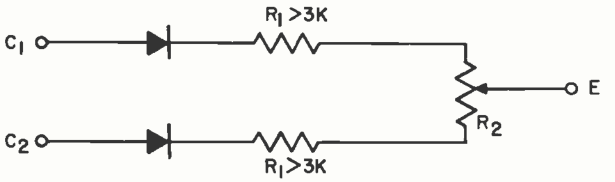
(C) Non-symmetrical Multivibrator





The timing capacitor C_T will be charged through the resistor R_{T1} or R_{T2} which is connected to the positive collector. The diodes will isolate the other resistor from the timing capacitor. The two parts of the period (t_1, t_2) can thus be set independently by R_{T1} and R_{T2} and may differ by as much as 1000 to 1.

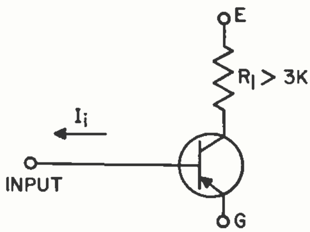
(D) Non-symmetrical Multivibrator — Constant Frequency



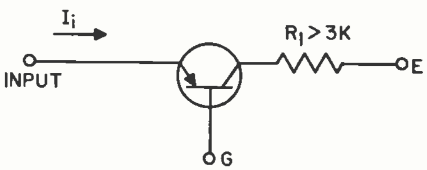
$$f = \frac{1}{(2R_1 + R_2)C_T}$$

This configuration gives a multivibrator which has a constant frequency but a variable duty cycle.

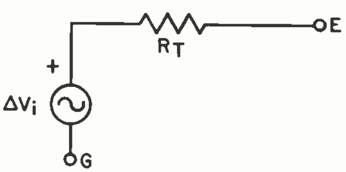
(E) Variable Frequency Oscillator



$$f = \frac{h_{FE} I_i}{2\pi V_{BB} C_T}$$



$$f = \frac{I_i}{2\pi V_{BB} C_T}$$



$$\Delta f \cong \frac{0.8\, \Delta V_i}{R_T C_T V_{BB}}$$

In the equations V_{BB} is the voltage between base-one and base-two of the unijunction transistor. These circuits give a variable frequency square wave output. For the first two circuits the frequency is proportional to the input current. The first circuit has a higher effective current gain than the second circuit, but the temperature stability is not as good. The third circuit is useful if only a small range of frequency variation is desired. The variation of frequency with input voltage is linear only for small changes in input voltage.

Further information on the characteristics and circuit applications of the unijunction transistor is given in application note ECG-380, "Notes on the Application of the Silicon Unijunction Transistor". Available on written request.

14. SILICON CONTROLLED RECTIFIER

The Silicon Controlled Rectifier (SCR) is a PNPN device structure which is the semiconductor equivalent of a gas thyratron. It is constructed by making both an alloyed PN junction and an ohmic contact to a diffused PNP silicon pellet as shown in Figure 14.1 along with the circuit diagram for an SCR.

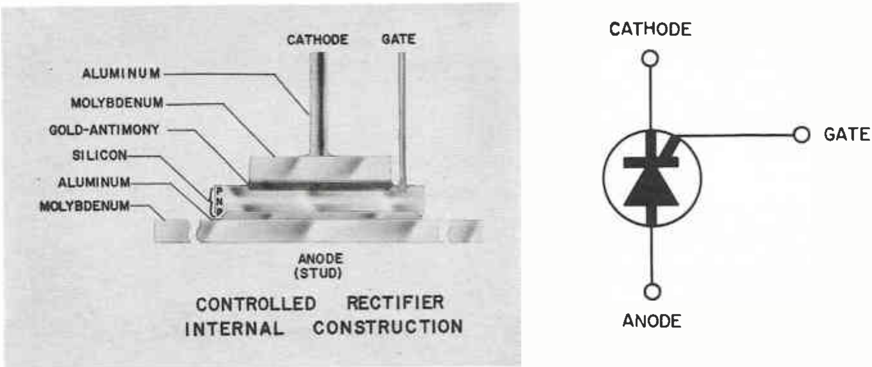


FIGURE 14.1

This basic structure is made in two general sizes having average current ratings of 16 and 50 amperes. SCR's are also classified within any basic size by the maximum voltage they can block.

The electrical characteristics of the SCR are shown by Figure 14.2.

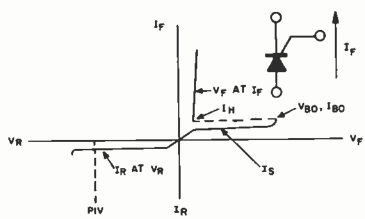


FIGURE 14.2

With reverse voltage impressed on the device (cathode positive), it will block the flow of current until the avalanche voltage is reached as in an ordinary rectifier. With positive voltage applied to the anode, the SCR also blocks the flow of current until the forward breakover voltage (V_{BO}) is reached. At this point the SCR goes into a high-conduction state and the voltage across the device drops to one or two volts. In the high conduction state, the current flow is limited only by the external circuit impedance and supply voltage. At anode to cathode voltages less than the breakover voltage, the SCR can be switched into the high conduction mode by a small pulse (typically 1.5 volts and 30 ma) applied from gate to cathode. This method of "turning-on" the SCR by means of the gate is used in the majority of applications since it permits the control of large amounts of power from low power signal sources. Once the SCR is in the high conduction state, it will continue conduction indefinitely after removal of the gate signal until the anode current is interrupted or diverted for about 20 microseconds after which the SCR will regain its forward blocking capabilities.

The gate pulse needed to turn-on an SCR varies with temperature and also from unit to unit so in order to achieve precise firing, it is desirable to use a short (10 μsec) gate pulse with an amplitude of about 6 volts and 300 ma. A simple and economical source of these pulses is the unijunction relaxation oscillator circuit shown in Figure 14.3.

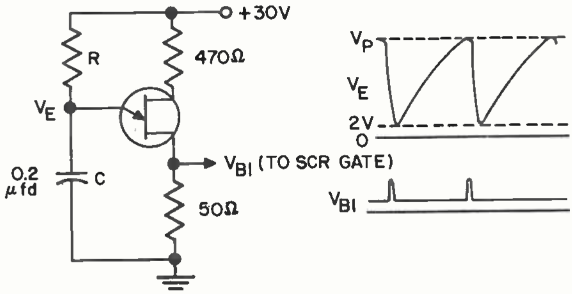


FIGURE 14.3

This circuit will produce pulses spaced roughly 0.2R μsec apart and is the basis for SCR firing circuits in DC to AC inverters or other equipment operating from DC supplies. A major advantage of the unijunction circuit is that the interval between pulses depends primarily on the values of R and C and is essentially invariant with changes in supply voltage or temperature.

When SCR's are used in a-c circuits, it is necessary that the firing pulses have a precisely determined relationship with the zero crossing of the supply voltage. This is achieved by the circuit of Figure 14.4.

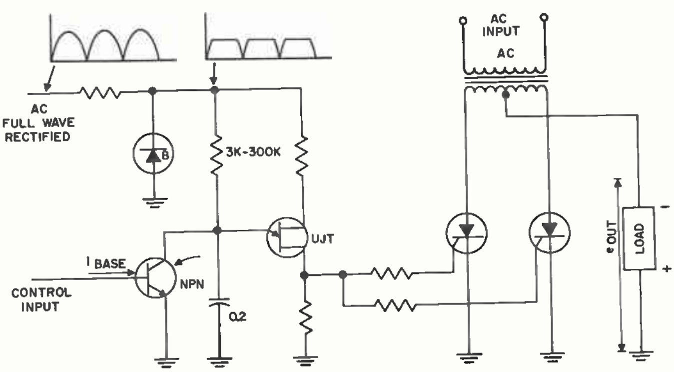
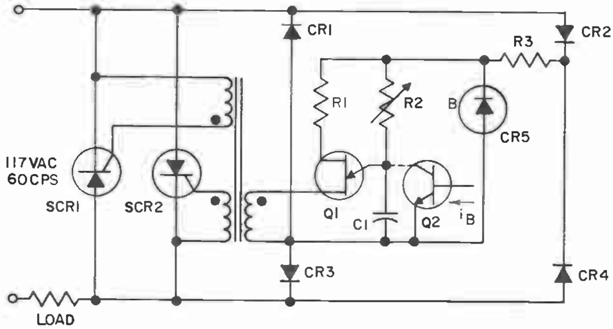


FIGURE 14.4

The UJT supply voltage is a full-wave rectified AC voltage that is clipped by the breakdown diode so that the maximum voltage is about 30 volts. The 0.2μfd capacitor begins charging at the start of the AC wave and will produce a pulse after a time interval depending on the value of the UJT emitter resistor. At the end of the half-cycle of a-c, the base-to-base voltage of the UJT drops to zero and the 0.2 μfd capacitor discharges to ground through the emitter. Therefore, the timing of the UJT pulses is always synchronized with the a-c supply voltage.

If a small current is injected into the base of the NPN transistor, a much larger current will flow from collector to emitter thus diverting some charging current from the 0.2 μfd capacitor. Reducing the charging current to the capacitor will delay the firing of the UJT and SCR and less average current will flow in the load. The power gain from the base of the NPN transistor to the output of the SCR is over 10 million so that this basic circuit can be adapted for high performance regulated power supplies, temperature controls and other similar applications.

Figure 14.5 is the circuit of a simple phase controlled AC switch suitable for controlling the intensity of incandescent lights.



R1 – 390Ω
R2 – 100,000Ω LINEAR POT.
R3 – 3300Ω, 5 WATT
C1 – 0.2 MFD
SCR1, SCR2 – C35B
CR1, CR2, CR3, CR4 – IN1695
CR5 – IN1527 ZENER DIODE, ONE WATT, 22VOLTS
Q1 – 2N489
T1 – MAGNETICS, INC, CORE, TYPE 50176-6H
3 WINDINGS, 125 TURNS EACH OF NO. 27 WIRE.

FIGURE 14.5

It uses a UJT as a source of pulses which are synchronized to the AC supply by the full-wave bridge composed of diodes CR-1 through CR-4. One SCR conducts during the positive half cycle of AC and the other conducts during the negative half cycle. By varying resistor R_2, the firing point can be varied from 0° to 180°. With type C-35B Controlled Rectifiers, this circuit can control up to 4.2 KW of power.

By using two SCR's and two conventional rectifiers in a full-wave bridge circuit, it is possible to obtain a continuously variable DC output.

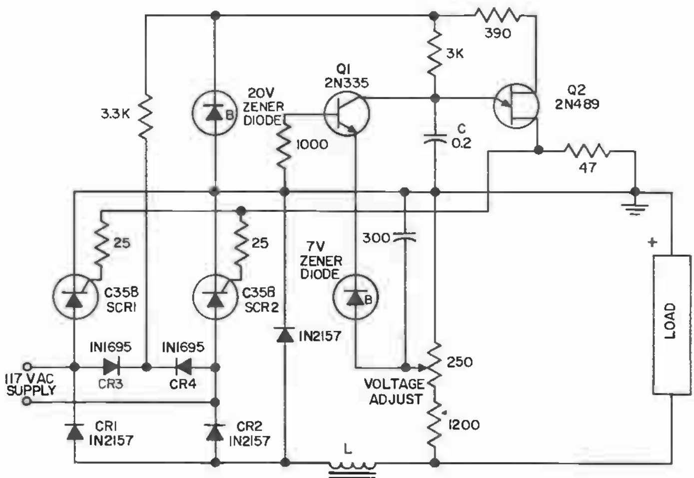


FIGURE 14.6

Figure 14.6 is the circuit of a regulated power supply that will maintain the output DC constant within ½ percent for wide variations of load or supply voltage. By making the feedback voltage to Q_1 proportional to current rather than voltage, a constant current supply will result. Figure 14.7 is the circuit of parallel type inverter suitable for converting DC to AC or else DC at a higher voltage level.

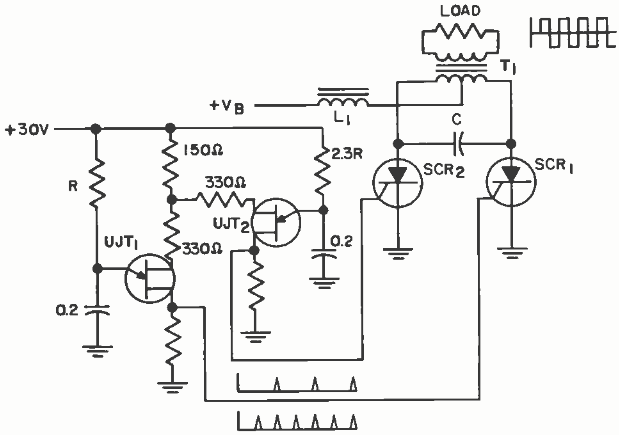


FIGURE 14.7

UJT_1 is the primary oscillator and UJT_2 is synchronized to UJT_1 through the common 150Ω resistor in their base two circuits so UJT_2 fires at exactly half the rate of UJT_1. Since UJT_1 produces the first pulse, SCR_1 will turn on first and SCR_2 will remain in a blocking condition. The current from the supply V_B will then flow through the right hand side of the transformer T1. The transformer action will produce a voltage of approximately $2V_B$ at the anode of SCR_2 and across the capacitor C. When the next trigger pulse is applied to the gate of SCR_2, it will turn on and the voltage at the anode of SCR_2 will fall to a value equal to the forward conducting drop. The voltage at the anode of SCR_1 will fall to approximately $-2V_B$ because of the action of the commutating capacitor C. The capacitor C will maintain a reverse bias across SCR_1 long enough for SCR_1 to recover to the blocking state. The next trigger pulse will occur at the gate of SCR_1 and cause the circuit to revert to the original state. In this manner, the current from the supply V_B will flow alternately through the two sides of the transformer primary and produce an AC voltage at the load.

The inductance L_1 serves as a ballast to prevent excessive current flow during switching. During the switching interval opposing currents can flow in both halves of the transformer primary to the commutating capacitor and to the anode of the SCR which has been turned on. If this current is not limited, the charging time for the commutating capacitor will be very short and the SCR which is to be turned off will not be reverse biased long enough for it to recover. Large values of L_1 on the other hand will prevent the supply from adjusting to rapid changes in the load. For example, if the load is suddenly decreased, a voltage will be generated across L_1 which will also appear at the anode of the SCR which is in the blocking condition. If this transient is greater than the breakover voltage, it will cause this SCR to turn on and the inverter will fail. This condition can be prevented by placing a rectifier in parallel with L_1.

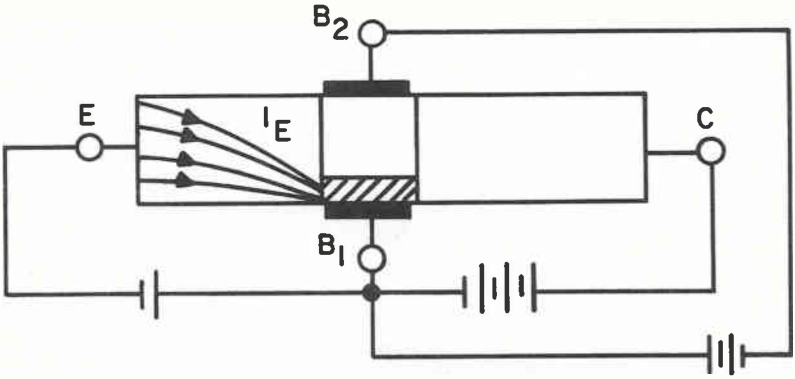
Additional information on Silicon Controlled Rectifiers and details on the design of inverters, motor drives, and other SCR circuits can be obtained by writing for ECG-371-1, "Notes on the Application of the Silicon Controlled Rectifier."

15. TETRODE TRANSISTORS

Transistor types 3N36 and 3N37 are grown germanium NPN tetrodes manufactured by the meltback process. The 3N36 is generally used between 30 MC and 90 MC while the 3N37 is used from 90 MC to 200 MC. Primarily intended for high frequency use as RF amplifiers, IF amplifiers, mixers and oscillators, these transistors are also excellent for wide band video amplifiers. The use of base-two for AGC control is also attractive in that very little detuning of the collector circuit results.

Formerly designated by the development number ZJ-22, these types are now in quantity production. The case dimensions of these transistors conform to the JEDEC TO-5 package. They are electrically isolated from the case, which may be grounded by the indexing tab, if required for shielding purposes. The design is suitable for automatic insertion into printed circuit boards.

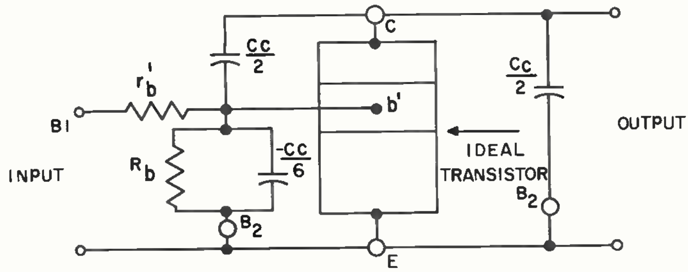
It has long been recognized that smaller bar size will improve high frequency transistor performance. In particular, small cross section base regions will reduce the base spreading resistance, r'_b, (or high frequency base resistance). High r'_b is the most degradating high frequency parameter and is almost always the performance-limiting factor. One approach to reducing r'_b is to use physically minute bars. While this solves the electrical problem and is technically possible, the cost of manufacture is high and mechanical reliability is low. To overcome these problems, G.E. uses a reasonable size bar and obtains the high frequency performance by electrical means. With the addition of a second base lead and the application of a suitable cross-base bias, an electric field is established which "compresses" the active base region and thereby brings about a significant reduction in the high frequency base resistance. See Figure 15.1.



Effect of base-two bias on current distribution
FIGURE 15.1

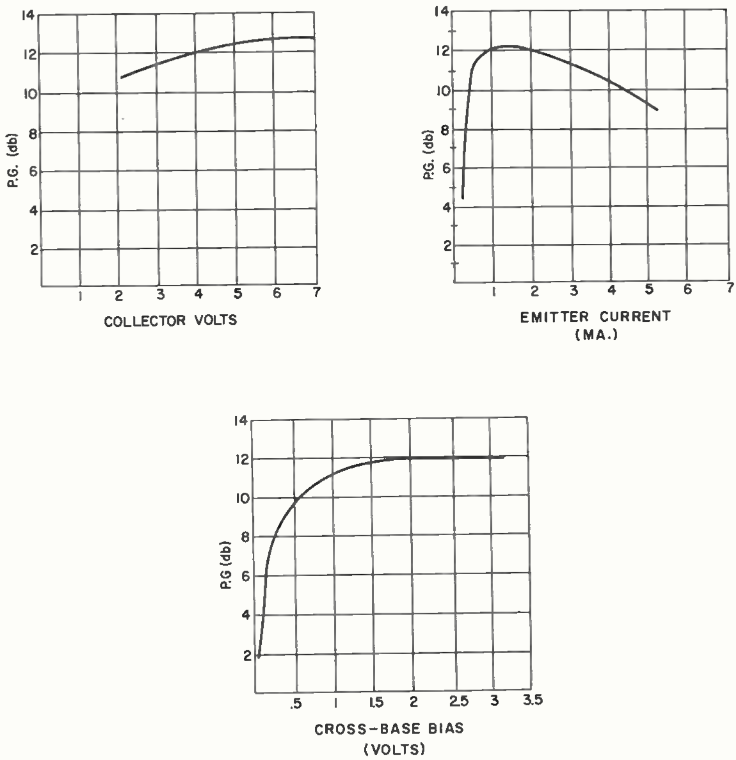
Improvements in base resistance of the order of 10 to 1 are achieved by the tetrode over the triode. Since the collector-base junction is normally biased in the inverse direction, the addition of base-two bias has relatively little effect on the collector junction. It merely increases the average bias by $V_{B_1B_2}/2$ which at any collector bias over a few volts has practically no effect.

Operation in the common emitter configuration is generally recommended for several reasons. Operation is more stable and is less likely to be regenerative. Power gain is higher except at the upper frequency limits. The effect of collector capacity on internal feedback is approximately halved when base-two is connected to a-c ground. See Figure 15.2 for a simplified equivalent circuit.



Approximate equivalent circuit of tetrode
FIGURE 15.2

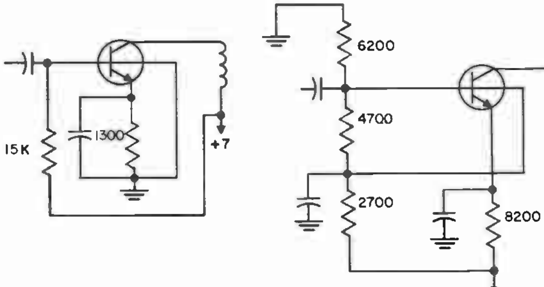
As can be seen, half the collector capacity is across the load and can be tuned out. Thus, it does not contribute to the internal feedback. Output impedance is increased by a factor of 2, with a corresponding improvement in high frequency available power gain. Figure 15.3 shows the typical power gain variations of a 3N36 at 60 MC with collector voltage, emitter current and base-two bias. Curves for the 3N37 at 150 MC have the same general shape.



Power gain variations with bias
FIGURE 15.3

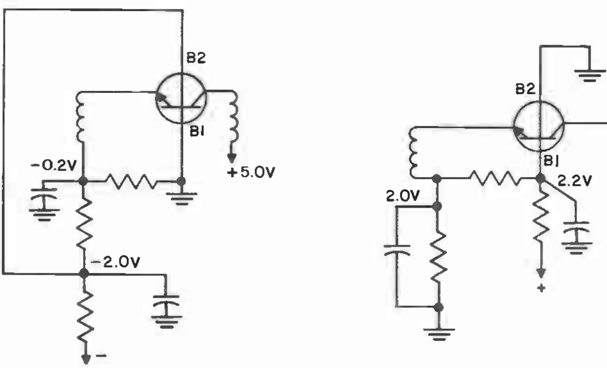
Typical d-c biasing methods are shown in Figures 15.4 and 15.5. Recommended conditions are:

> Collector to emitter voltage, $V_{CE} = 5$ volts; base-one to base-two voltage, $V_{B_1B_2} = 2$ volts; base-one to base-two current, $I_{B_1B_2} = .5$ ma; emitter current, $I_E = 1.5$ ma.



COMMON EMITTER

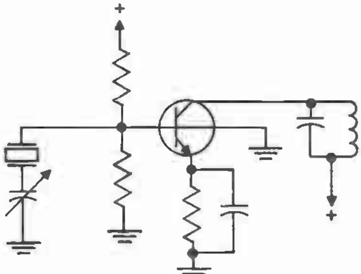
Typical biasing methods
FIGURE 15.4



COMMON BASE

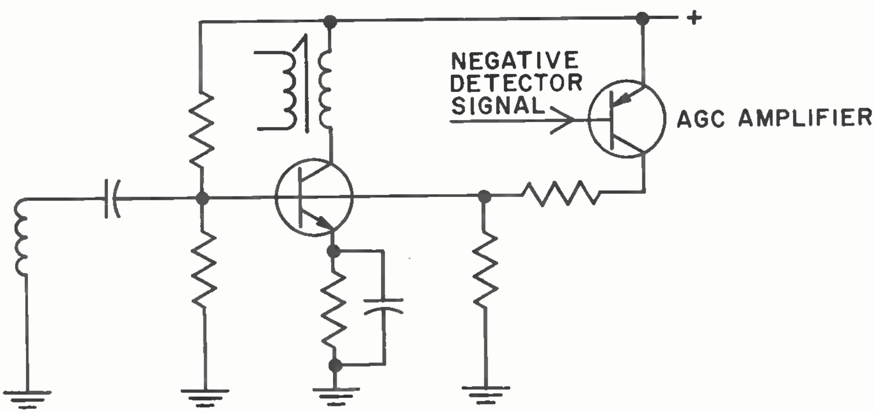
Typical biasing methods
FIGURE 15.5

Typical circuit configurations utilizing tetrode transistors are shown in Figures 15.6, 15.7, and 15.8.



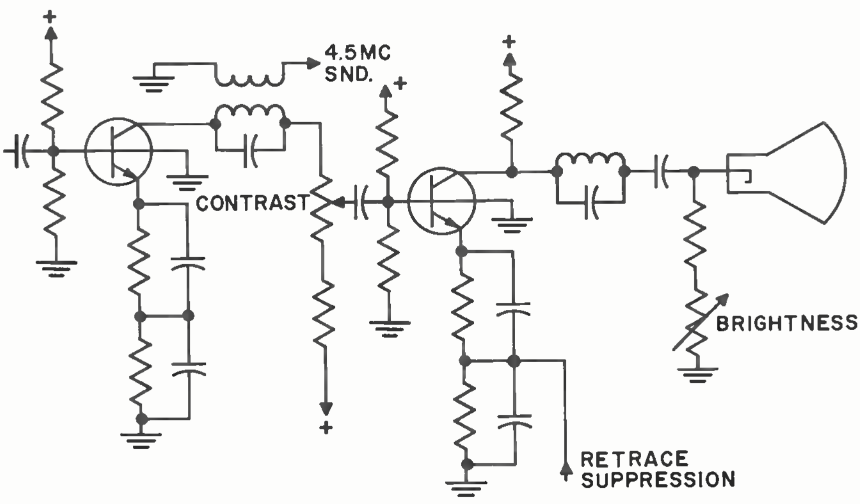
CRYSTAL CONTROLLED OSCILLATOR

FIGURE 15.6



BASE 2 AGC FOR RF AND IF AMPLIFIERS

FIGURE 15.7

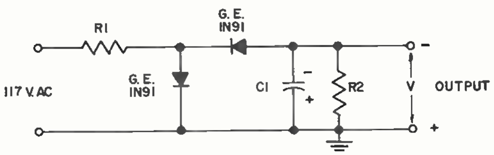


TV VIDEO AMPLIFIER (FOR HIGH Gm PICTURE TUBES)

FIGURE 15.8

16. POWER SUPPLIES

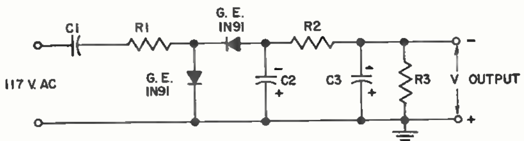
Both silicon and germanium cells can be used in the types of power supplies illustrated in Figures 16.1, 16.2, 16.3, and 16.4. All four of these power supplies are designed for low ripple output and high reliability at minimum expense. However, they are limited to Class A types of load in which the average load current does not vary with the amplitude of the impressed signal.



OUTPUT VOLTAGE V	OUTPUT CURRENT	RI	CI	R2*	APPROX. RIPPLE
12 VOLTS	1 MA.	43K, 1/2W	250 μf 15 VOLT ELECTROLYTIC	180K 1/2W	0.1%
12 VOLTS	2 MA.	22K, 1/2W	250 μf 15 VOLT ELECTROLYTIC	100K 1/2W	0.1%
25 VOLTS	2 MA.	18K, 1/2W	250 μf 30 VOLT ELECTROLYTIC	180K 1/2W	0.1%

*TO ADJUST VOLTAGE OUTPUT FOR OTHER OUTPUT CURRENTS, ADJUST R2.

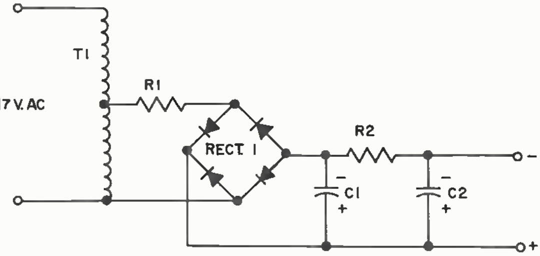
PRE-AMP POWER SUPPLY
FIGURE 16.1



OUTPUT VOLTAGE V	OUTPUT CURRENT	RI	R2	R3*	CI METALLIZED PAPER	C2	C3	APPROX. RIPPLE
12 VOLTS	100MA.	2Ω 1 WATT	100Ω 2W	2200Ω 1W	THREE 2-μf IN PARALLEL 200 V	250 μf 15 VOLT ELECTROLYTIC	250 μf 15 VOLT ELECTROLYTIC	0.5%
12 VOLTS	150MA	2Ω 1 WATT	100Ω 10 W	2200Ω 1W	FOUR 2-μf IN PARALLEL 200V	250μf 15 VOLT ELECTROLYTIC	250μf 15 VOLT ELECTROLYTIC	0.5%
25 VOLTS	50MA	2Ω 1 WATT	250Ω 2W	10,000Ω 1W	TWO 2-μf IN PARALLEL 200V	100μf 50 VOLT ELECTROLYTIC	250μf 30 VOLT ELECTROLYTIC	0.5%

GENERAL PURPOSE TRANSISTOR POWER SUPPLY
FIGURE 16.2

* TO ADJUST VOLTAGE OUTPUT FOR OTHER OUTPUT CURRENTS, ADJUST R3.



OUTPUT VOLTAGE V	OUTPUT CURRENT	R1	R2	C1	C2	RECT. 1	APPROX. RIPPLE
40 VOLTS	1 AMP.	3Ω 10 WATTS	20Ω 20 WATTS	300μf 150 VOLT ELECTROLYTIC	1000μf 50 VOLT ELECTROLYTIC	FOUR G.E. 1N537	1%

T1 - U.T.C. R-43 AUTOTRANSFORMER OR EQUAL
2:1 WINDING RATIO

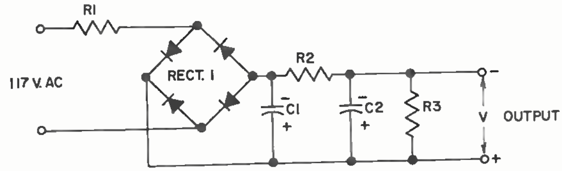
POWER SUPPLY FOR HIGH POWER CLASS A TRANSISTOR AMPLIFIERS
FIGURE 16.3

To prevent possible damage to the filter capacitors and rectifiers, it is essential that these power supplies always be operated with the rated load across the output terminals. Absence of this load will apply excessive voltage to the components. Class B loads require a stiffer voltage source than the resistance-capacity combinations of the illustrated power supplies can provide. For Class B and other loads that require good voltage regulation, it is recommended that the line voltage be reduced through transformers rather than series resistance or capacitance, and that chokes be substituted for the series resistance in the filter elements. Alternately, a regulated power supply such as shown in Figure 16.8 can be used.

This circuit uses a step-down transformer and full-wave rectifier as a source of unregulated DC. A power transistor acts as a series regulator and mercury batteries are used for the voltage reference. The battery drain is very small so battery life is essentially equal to the shelf life.

When a semiconductor rectifier feeds a capacity-input filter such as in Figures 16.1 through 16.4, it is necessary to limit the high charging current that flows into the input capacitor when the circuit is energized. Otherwise this surge of current may destroy the rectifier. Resistor R1 is used in Figures 16.1 through 16.4 to limit this charging current to safe values.

As shown, the four power supplies do not isolate the load circuit from the 117 volt AC line. In Figures 16.1 and 16.2, the load circuit may be grounded provided a polarized plug is used on the AC line cord to ensure that the grounded side of the AC line is always connected to the grounded side of the load. Figures 16.3 and 16.4 utilize what is called a single phase bridge rectifier circuit to achieve full wave rectification, and hence, lower ripple. Since ground cannot be carried through on a common line to the load in this type of circuit, it is necessary to insulate the load "ground" from accidental



OUTPUT VOLTAGE V	OUTPUT CURRENT	R1	R2	C1	C2	R3*	RECT 1	APPROX. RIPPLE
40 VOLTS	1 AMP	5Ω 20W	75Ω 100W	100µf 150 VOLTS ELECTROLYTIC	300µf 50 VOLTS ELECTROLYTIC	1000Ω 2 W	FOUR G.E. 1N538	1%

* TO ADJUST VOLTAGE OUTPUT FOR OTHER OUTPUT CURRENTS, ADJUST R3.

POWER SUPPLY FOR HIGH POWER CLASS A TRANSISTOR AMPLIFIER

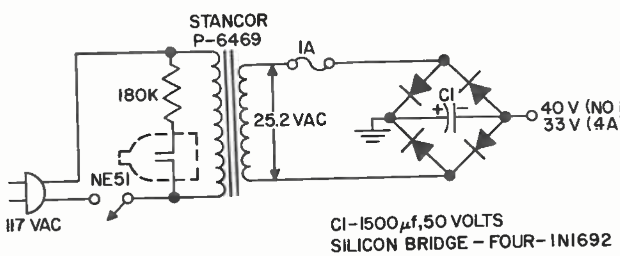
FIGURE 16.4

contact with true ground, or to insert an isolation transformer ahead of the power supply to isolate the two systems. Careful attention to these factors is of particular importance when supplying DC to high gain amplifiers to eliminate hum.

As illustrated, Figures 16.1 and 16.2 develop a negative output voltage with respect to ground as required when supplying P-N-P transistors with grounded emitters. To develop a positive voltage with respect to ground, it is only necessary to reverse the rectifiers and electrolytic capacitors in the circuit.

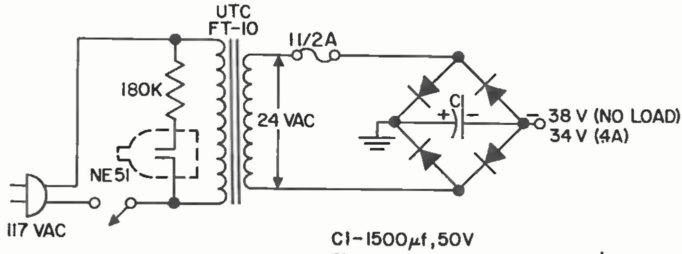
The power supply of Figure 16.3 uses an autotransformer to reduce the line voltage to one-half normal value before applying to the rectifiers. Provided the additional heat dissipation is not objectionable, Figure 16.4 provides a cheaper means of achieving the same objective by using resistor R2 to reduce the voltage to the desired value.

COMPLETE POWER SUPPLY CIRCUITS



POWER SUPPLY FOR SEVEN-WATT AMPLIFIER

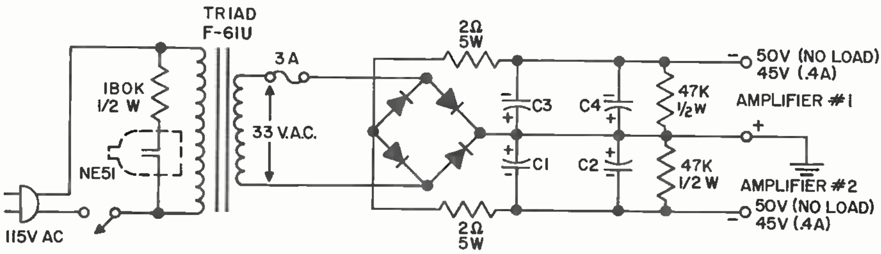
FIGURE 16.5



C1-1500μf,50V
SILICON BRIDGE-FOUR-1N537'S

POWER SUPPLY FOR DUAL SEVEN-WATT AMPLIFIERS

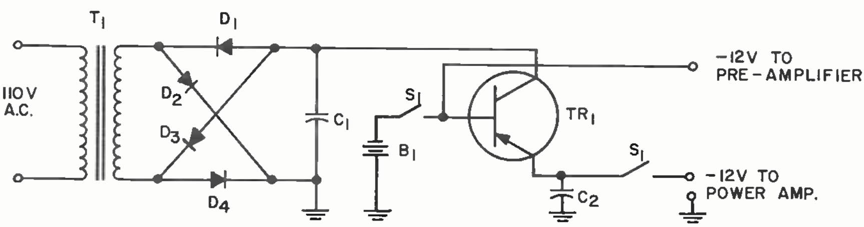
FIGURE 16.6



C1 – 1500 μf, 50 VOLTS
C2 – 1500 μf, 50 VOLTS
C3 – 1500 μf, 50 VOLTS
C4 – 1500 μf, 50 VOLTS
SILICON BRIDGE - FOUR - 1N1115

POWER SUPPLY FOR DUAL TEN-WATT AMPLIFIERS

FIGURE 16.7



TR_1 - POWER TRANSISTOR (MOUNT ON HEAT SINK) C.B.S. 2N256, 2N156 OR EQUIVALENT
S_1 - D.P.S.T.
T_1 - STANCOR P-6469 117VAC TO 25.2 OR EQUIVALENT
D_1, D_2, D_3, D_4 - GENERAL ELECTRIC 1N91 GERMANIUM RECTIFIERS
C_1, C_2 - 50μfd, 50 VOLT
B_1 - 3, 4 VOLT MERCURY CELLS IN SERIES, MALLORY TR-233R OR EQUIVALENT

AMPLIFIER REGULATED POWER SUPPLY

FIGURE 16.8

TRANSISTOR SPECIFICATIONS

HOW TO READ A SPECIFICATION SHEET

Semiconductors are available in a large variety of different types, each with its own unique characteristics. At the present time there are over 2200 different types of diodes and rectifiers and over 750 different types of transistors being manufactured.

The Characteristics of each of these devices are usually presented in specification sheets similar to the ones represented on page 161 and page 223 respectively. These specifications, particularly the transistor specification on the next page, contain many terms and ratings that are probably new to you, so we have selected several of the more important ones and explained what they mean.

NOTES ON TRANSISTOR SPECIFICATION SHEET

(1) The lead paragraph is a general description of the device and usually contains three specific pieces of information — The kind of transistor, in this case a silicon NPN triode, — A few major application areas, amplifier and switch, — General sales features, electrical stability and a standard size hermetically sealed package.

(2) The **Absolute Maximum Ratings** are those ratings which should not be exceeded under any circumstances. Exceeding them may cause device failure.

(3) The **Power Dissipation** of a transistor is limited by its junction temperature. Therefore, the higher the temperature of the air surrounding the transistor (ambient temperature), the less power the device can dissipate. A factor telling how much the transistor must be derated for each degree of increase in ambient temperature in degrees centigrade is usually given. Notice that this device can dissipate 125mw at 25°C. By applying the given derating factor of 1mw for each degree increase in ambient temperature, we find that the power dissipation has dropped to 0mw at 150°C, which is the maximum operating temperature of this device.

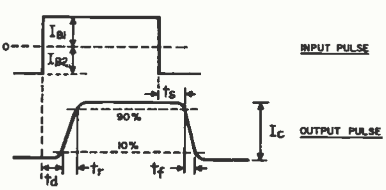
(4) All of the remaining ratings define what the device is capable of under specified test conditions. These characteristics are needed by the design engineer to design matching networks and to calculate exact circuit performance.

(5) **Current Transfer Ratio** is another name for beta. In this case we are talking about an a-c characteristic, so the symbol is h_{fe}. Many specification sheets also list the d-c beta using the symbol h_{FE}. Beta is partially dependent on frequency, so some specifications list beta for more than one frequency.

(6) The **Frequency Cutoff** f_{ab} of a transistor is defined as that frequency at which the grounded base current gain drops to .707 of the 1kc value. It gives a rough indication of the useful frequency range of the device.

(7) The **Collector Cutoff Current** is the leakage current from collector to base when no emitter current is being applied. This leakage current varies with temperature changes and must be taken into account whenever any semiconductor device is designed into equipment used over a wide range of ambient temperature.

(8) The **Switching Characteristics** given show how the device responds to an input pulse under the specified driving conditions. These response times are very dependent on the circuit used. The terms used are explained in the curves at right.



2N337, 2N338

Outline Drawing No. 4

① The General Electric Types 2N337 and 2N338 are high-frequency silicon NPN transistors intended for amplifier applications in the audio and radio frequency range and for high-speed switching circuits. They are grown junction devices with a diffused base and are manufactured in the Fixed-Bed Mounting design for extremely high mechanical reliability under severe conditions of shock, vibration, centrifugal force, and temperature. For electrical reliability and parameter stability, all transistors are subjected to a minimum 160 hour 200°C cycled aging operation included in the manufacturing process. These transistors are hermetically sealed in welded cases. The case dimensions and lead configuration conform to JEDEC standards and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

② ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CBO}	45	volts
Emitter to Base	V_{EBO}	1	volt
Current			
Collector	I_C	20	ma
③ **Power**			
Collector Dissipation*	P_C	125	mw
Temperature			
Storage	T_{STG}	−65 to 200	°C
Operating	T_A	−65 to 150	°C

④ ELECTRICAL CHARACTERISTICS: (25°C)
(Unless otherwise specified; $V_{CB} = 20v$; $I_E = -1$ ma; f = 1 kc)

		2N337			2N338			
Small-Signal Characteristics		Min.	Typ.	Max.	Min.	Typ.	Max.	
⑤ Current Transfer Ratio	h_{fe}	19	55		39	99		
Input Impedance	h_{ib}	30	47	80	30	47	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}		180	2000		200	2000	$\times 10^{-6}$
Output Admittance	h_{ob}		.1	1		.1	1	μmho
High-Frequency Characteristics								
⑥ Alpha Cutoff Frequency	f_{ab}	10	30		20	45		mc
Collector Capacitance (f = 1 mc)	C_{ob}		1.4	3		1.4	3	μμf
Common Emitter Current Gain (f = 2.5 mc)	h_{fe}	14	24		20	26		
D-C Characteristics								
Common Emitter Current Gain ($V_{CE} = 5v$; $I_C = 10$ ma)	h_{FE}	20	35	55	45	75	150	
Collector Breakdown Voltage ($I_{CBO} = 50$ μa; $I_E = 0$)	BV_{CBO}	45			45			volts
Emitter Breakdown Voltage ($I_{EBO} = -50$ μa; $I_C = 0$)	BV_{EBO}	1			1			volt
Collector Saturation Resistance ($I_B = 1$ ma; $I_C = 10$ ma)	R_{SC}		75	150				ohms
($I_B = .5$ ma; $I_C = 10$ ma)	R_{SC}					75	150	ohms
⑦ **Cutoff Characteristics**								
Collector Current ($V_{CB} = 20v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.002	1		.002	1	μa
Collector Current ($V_{CB} = 20v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			100			100	μa
⑧ **Switching Characteristics**								
Rise Time	t_r		.02			.06		μsecs
Storage Time	t_s		.02			.02		μsecs
Fall Time	t_f		.04			.14		μsecs

*Derate 1 mw/°C increase in ambient temperature over 25°C

EXPLANATION OF PARAMETER SYMBOLS

SMALL SIGNAL & HIGH FREQUENCY PARAMETERS (at specified bias)

Symbols	Abbreviated Definitions	
h_{ob}	Com. base — output admittance, input AC open-circuited	
h_{ib}	Com. base — input impedance, output AC short-circuited	
h_{rb}	Com. base — reverse voltage transfer ratio, input AC open-circuited	
h_{fb}	Com. base	forward current transfer ratio, output AC short-circuited
h_{fe}	Com. emitter	
h_{fc}	Com. collector	
h_{oe}, h_{ie}	Examples of other corresponding com. emitter symbols	
f_{ab}	Com. base	the frequency at which the magnitude of the small-signal short-circuit forward current transfer ratio is 0.707 of its low frequency value.
f_{ae}	Com. emitter	
f_{MAX}	Maximum frequency of oscillation	
C_{ob}	Collector to base	Capacitance measured across the output terminals with the input AC open-circuited
C_{oe}	Collector to emitter	
r'_b	Base spreading resistance	
G_e	Com. emitter Power Gain (use G_b for com. base)	
CG_e	Conversion gain	
NF	Noise Figure	

SWITCHING CHARACTERISTICS (at specified bias)

t_d	Ohmic delay time	These depend on both transistor and circuit parameters
t_r	Rise time	
t_s	Storage time	
t_f	Fall time	
V_{CE} (SAT.)	Saturation voltage at specified I_C and I_B. This is defined only with the collector saturation region.	
h_{FE}	Com. emitter — static value of short-circuit forward current transfer ratio, $h_{FE} = \frac{I_C}{I_B}$	
h_{FE} (INV)	Inverted h_{FE} (emitter and collector leads switched)	

UNIJUNCTION TRANSISTOR MEASUREMENTS

I_{B2} (MOD)	Modulated interbase current
I_P	Peak point emitter current
I_V	Valley current
R_{BBO}	Interbase resistance
V_{BB}	Interbase voltage
V_V	Valley voltage
η	Intrinsic stand-off ratio. Defined by $V_P = \eta V_{BB} + \frac{200}{T_J}$ (in ° Kelvin)

DC MEASUREMENTS

I_C, I_E, I_B	DC currents into collector, emitter, or base terminal
V_{CB}, V_{EB}	Voltage collector to base, or emitter to base
V_{CE}	Voltage collector to emitter
V_{BE}	Voltage base to emitter
BV_{CBO}	Breakdown voltage, collector to base junction reverse biased, emitter open-circuited (value of I_C should be specified)
V_{CEO}	Voltage collector to emitter, at zero base current, with the collector junction reverse biased. Specify I_C.
BV_{CEO}	Breakdown voltage, collector to emitter, with base open-circuited. This may be a function of both "m" (the charge carrier multiplication factor) and the h_{fb} of the transistor. Specify I_C.
V_{CER}	Similar to V_{CEO} except a resistor of value "R" between base and emitter.
V_{CES}	Similar to V_{CEO} but base shorted to emitter.
V_{PT}	Punch-through voltage, collector to base voltage at which the collector space charge layer has widened until it contacts the emitter junction. At voltages above punch-through, $V_{PT} = V_{CB} - V_{EB}$
V_{CCB} V_{CCE} V_{BBE}	Supply voltage collector to base Supply voltage collector to emitter Supply voltage base to emitter } NOTE — third subscript may be omitted if no confusion results.
I_{CO}, I_{CBO}	Collector current when collector junction is reverse biased and emitter is DC open-circuited.
I_{EO}, I_{EBO}	Emitter current when emitter junction is reverse biased and collector is DC open-circuited.
I_{CEO}	Collector current with collector junction reverse biased and base open-circuited.
I_{CES}	Collector current with collector junction reverse biased and base shorted to emitter.
I_{ECS}	Emitter current with emitter junction reverse biased and base shorted to collector.
R_{SC}	Collector saturation resistance

OTHER SYMBOLS USED

P_{CM}	Peak collector power dissipation for a specified time limit
P_{CAV}	Average maximum collector power dissipation
P_o	Power output
Z_i	Input impedance
Z_o	Output impedance
T_A	Operating Temperature
T_J	Junction Temperature
T_{STG}	Storage Temperature

NOTE: In devices with several electrodes of the same type, indicate electrode by number. Example: I_{B2}. In multiple unit devices, indicate device by number preceding electrode subscript. Example: I_{2C}. Where ambiguity might arise, separate complete electrode designations by hyphens or commas. Example: $V_{1C1-2C1}$ (Voltage between collector #1 of device #1 and collector #1 of device #2.)

NOTE: Reverse biased junction means biased for current flow in the high resistance direction.

GENERAL ELECTRIC TRANSISTOR SPECIFICATIONS

2N43

Outline Drawing No. 1

The General Electric Type 2N43 Germanium Alloy Junction Transistor Triode is a PNP unit particularly recommended for high gain, low power applications. A hermetic enclosure is provided by use of glass-to-metal seals and welded seams.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CB}	—45	volts
Collector to Emitter	V_{CE}	—30	volts
Emitter to Base	V_{EB}	—5	volts
Current			
Collector	I_C	—300	ma
Power			
Total Transistor Dissipation	P_M	240	mw
Temperature			
Storage	T_{STG}	—65 to 100	°C
Operating Junction	T_J	85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

		Min.	Design Center	Max.	
Small Signal Characteristics (V_{CB} or V_{CE} = —5 volts, I_E = 1 ma; f = 270 cps unless otherwise specified)					
Common base output admittance (input A-C open circuited)	h_{ob}	.1	.8	1.5	μmhos
Forward current transfer ratio (output A-C short circuited)	h_{fe}	30	42		
Common base input impedance (output A-C short circuited)	h_{ib}	25	29	35	ohms
Common base reverse voltage transfer ratio (input A-C open circuited)	h_{rb}	1	5	15	$\times 10^{-4}$
Common base output capacity (input A-C open circuited; f = 1 mc)	C_{ob}	20	40	60	μμf
Noise Figure (f = 1 Kc; BW = 1 cycle)	NF		6	20	db
Frequency cutoff (Common Base)	f_{ab}	.5	1.3	3.5	mc
D-C Characteristics					
Collector cutoff current (V_{CBO} = —45v)	I_{CO}		—8	—16	μamps
Emitter cutoff current (V_{EBO} = —5v)	I_{EO}		—4	—10	μamps
Collector Saturation Voltage (I_C = —20 ma; I_B = —1.3 ma)	$V_{CE}^{(SAT)}$	65	90	130	mv
Base input voltage, common emitter (V_{CE} = —1 volt; I_C = —20 ma)	V_{BE}	—180	—230	—280	mv
Common emitter static forward current transfer ratio (V_{CE} = —1 volt; I_C = —20 ma)	h_{FE}	34	53	65	
Common emitter static forward current transfer ratio (V_{CE} = —1 volt; I_C = —100 ma)	h_{FE}	30	48		
Collector to emitter voltage (10 K ohms resistor base to emitter; I_C = —0.6 ma)	V_{CER}	—30			volts
Punch-through voltage	V_{PT}	—30			volts
Thermal Characteristics					
Junction temperature rise/unit collector or emitter dissipation (in free air)				0.25	°C/mw
Junction temperature rise/unit collector or emitter dissipation (infinite heat sink)				0.11	°C/mw

2N43A

Outline Drawing No. 1

The 2N43A is identical to the 2N43 except that h_{fe} is guaranteed to be between 30 and 66. It is therefore electrically identical to the USAF 2N43A.

USAF 2N43A

Outline Drawing No. 1

Per MIL-T-19500/18

2N44

Outline Drawing No. 1

The General Electric Type 2N44 Germanium Alloy Junction Transistor Triode is a PNP unit particularly recommended for medium gain, low power applications. A hermetic enclosure is provided by use of glass-to-metal seals and welded seams.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CB}	−45	volts
Collector to Emitter	V_{CE}	−30	volts
Emitter to Base	V_{EB}	−5	volts
Current			
Collector	I_C	−300	ma
Power			
Total Transistor Dissipation	P_M	240	mw
Temperature			
Storage	T_{STG}	−65 to 100	°C
Operating Junction	T_J	85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

Small Signal Characteristics (V_{CB} or V_{CE} = −5 volts, I_E = 1 ma; f = 270 cps unless otherwise specified)		Min.	Design Center	Max.	
Common base output admittance (input A-C open circuited)	h_{ob}	.1	.9	1.5	μmhos
Forward current transfer ratio (output A-C short circuited)	h_{fe}		25		
Common base input impedance (output A-C short circuited)	h_{ib}	27	31	38	ohms
Common base reverse voltage transfer ratio (input A-C open circuited)	h_{rb}	1.0	4	13	$\times 10^{-4}$
Common base output capacity (input A-C open circuited; f = 1 mc)	C_{ob}	20	40	60	μμf
Noise Figure (f = 1 Kc; BW = 1 cycle)	NF		6	15	db
Frequency cutoff (Common Base)	f_{ab}	.5	1.0	3.0	mc
D-C Characteristics					
Collector cutoff current (V_{CBO} = −45v)	I_{CO}		−8	−16	μamps
Emitter cutoff current (V_{EBO} = −5v)	I_{EO}		−4	−10	μamps
Collector Saturation Voltage (I_C = −20 ma; I_B = −2 ma)	$V_{CE(SAT)}$	55	90	130	mv
Base input voltage, common emitter	V_{BE}	−200	−250	−300	mv
Common emitter static forward current transfer ratio (V_{CE} = −1 volt; I_C = −20 ma)	h_{FE}	18	31	43	
Common emitter static forward current transfer ratio (V_{CE} = −1 volt; I_C = −100 ma)	h_{FE}	13	25		
Collector to emitter voltage (10 K ohms resistor base to emitter; I_C = −0.6 ma)	V_{CER}	−30			volts
Punch-through voltage	V_{PT}	−30			volts
Thermal Characteristics					
Junction temperature rise/unit collector or emitter dissipation (in free air)				0.25	°C/mw
Junction temperature rise/unit collector or emitter dissipation (infinite heat sink)				0.11	°C/mw

USAF 2N44A

Per MIL-T-19500/6

Outline Drawing No. 1

2N78

Outline Drawing No. 3

The General Electric 2N78 is a rate grown NPN high frequency transistor intended for high gain RF and IF amplifier service and general purpose applications. The exclusive G-E rate-growing process used in the manufacture of the 2N78 enhances the stable and uniform characteristics required for military and industrial service. The 2N78's low collector cutoff current and controlled D-C Beta simplifies bias stabilization. In order to achieve the high degree of reliability necessary in industrial and military applications, the 2N78 is designed to pass 500G 1 millisecond drop shock, 10,000G centrifuge, 10G of vibration fatigue and 10G variable frequency vibration, as well as temperature cycling, moisture resistance, and operating and storage life tests as outlined in MIL-T-19500A.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Emitter (base open)	V_{CEO}	15	volts
Collector to Base (emitter open)	V_{CBO}	15	volts
Current			
Collector	I_C	20	ma
Emitter	I_E	−20	ma
Power			
Collector Dissipation*	P_C	65	mw
Temperature			
Storage	T_{STG}	85	°C

*Derate 1.1 mw/°C increase in ambient temperature.

ELECTRICAL CHARACTERISTICS: (25°C)

		Min.	Nom.	Max.	
Low Frequency Characteristics (Common Base)					
(V_{CB} = 5v; I_E = −1 ma; f = 270 cps) (See Note)					
Input Impedance (output short circuited)	h_{ib}	25	55	82	ohms
Voltage Feedback Ratio (input short circuited)	h_{rb}	.8	2	10	$\times 10^{-4}$
Current Amplification (output short circuited)	h_{fb}	.97	.983	.995	
Output Admittance (input open circuited)	h_{ob}	.1	.2	.7	µmhos
High Frequency Characteristics (Common Base)					
(V_{CB} = 5v; I_E = 1 ma)					
Alpha Cutoff Frequency	f_{ab}	5	9		mc
Output Capacity (f = 1 mc)	C_{ob}		3	6	µµf
Voltage Feedback Ratio (f = 1 mc)	h_{rb}			12	$\times 10^{-3}$
Noise Figure (V_{CB} = 1.5v; I_E = −0.5 ma; f = 1 kc)	NF		12		db
Power Gain in Typical IF Test Circuit (455 kc)	G_e	27			db
D-C Characteristics					
Collector Cutoff Current (V_{CB} = 15v)	I_{CO}		.7	3	µa
D-C Base Current Gain (I_B = 20µa; V_{CE} = 1v)	h_{FE}	45	70	135	

Typical Operation (Common Emitter) ($V_{CE} = 5v$; $I_E = 1$ ma)	IF Amp.	IF Amp.	RF Amp.	
Input Frequency	262	455	1600	kc
Input Impedance (resistive)	300	350	700	ohms
Output Impedance (resistive)	30	15	7	K ohms
Matched Power Gain	37	30	23	db

Note: The Low Frequency Characteristics are design limits within which 98% of production normally falls.

2N78

Outline Drawing No. 3

Also supplied as certified to meet MIL-T-19500/10

2N107

Outline Drawing No. 1

The General Electric type 2N107 is an alloy junction PNP transistor particularly suggested for students, experimenters, hobbyists, and hams. It is available only from franchised General Electric distributors. The 2N107 is hermetically sealed and will dissipate 50 milliwatts in 25°C free air.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector (referred to base)	V_{CB}	−12	volts
Current			
Collector	I_C	−10	ma
Emitter	I_E	10	ma
Temperature			
Junction	T_J	60	°C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

(Common Base, f = 270 cps $V_{CB} = -5v$, $I_E = 1$ ma)			
Collector Voltage	V_{CB}	−5.0	volts
Emitter Current	I_E	1.0	ma
Output Admittance (input open circuit)	h_{ob}	1.0	µmhos
Current Amplification (output short circuit)	h_{fb}	−.95	
Input Impedance (output short circuit)	h_{ib}	32	ohms
Voltage Feedback Ratio (input open circuit)	h_{rb}	3	$\times 10^{-4}$
Collector Cutoff Current	I_{CO}	10	µa
Output Capacitance	C_{ob}	40	µµf
Frequency Cutoff	f_{ab}	0.6	mc
Common Emitter ($V_{CE} = -5v$, $I_E = 1$ ma)			
Base Current Gain	h_{fe}	20	

2N123

Outline Drawing No. 7

The General Electric Type 2N123 is a PNP alloy junction high frequency switching transistor intended for military, industrial and data processing applications where high reliability at the maximum ratings is of prime importance.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Emitter (base open)	V_{CEO}	−15	volts
Collector to Base (emitter open)	V_{CBO}	−20	volts
Emitter to Base (collector open)	V_{EBO}	−10	volts
Current			
Collector	I_C	−125	ma
Peak Collector (10 μs max.)	I_{CM}	−500	ma
Emitter	I_E	125	ma
Power			
Peak Collector Dissipation (10 μs max.)*	P_{CM}	500	mw
Total Transistor Dissipation**	P_{AV}	150	mw
Temperature			
Storage	T_{STG}	−55 to 85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

		Min.	Typ.	Max.	
D-C Characteristics					
Common Emitter Current Gain (V_{CE} = −1v; I_C = −10 ma)	h_{FE}	30	65	150	
Saturation Voltage (I_B = −.5 ma; I_C = −10 ma)	$V_{CE(SAT)}$		−.15	−.2	volts
Cutoff Characteristics					
Collector Cutoff Current (V_{CB} = −20v)	I_{CO}		−2	−6	μa
Emitter Cutoff Current (V_{EB} = −10v)	I_{EO}		−2	−6	μa
Collector to Emitter Breakdown (I_C = −600 μa)	V_{CEO}	−15	−25		volts
Punch-through Voltage	V_{PT}	−20	−35		volts
High Frequency Characteristics (Common Base) (V_{CB} = −5v; I_E = 1 ma)					
Alpha Cutoff Frequency	f_{ab}	5	8		mc
Collector Capacity (f = 1 mc)	C_{ob}		15	20	μμf
Voltage Feedback Ratio (f = 1 mc)	h_{rb}		9		$\times 10^{-3}$
Base Spreading Resistance	r'_b		90	150	ohms
Low Frequency Characteristics (Common Base) (V_{CB} = −5v; I_E = 1 ma; f = 270 cps)					
Input Impedance	h_{ib}		28		ohms
Reverse Voltage Transfer Ratio	h_{rb}		8		$\times 10^{-4}$
Forward Current Transfer Ratio	h_{fb}		.987		
Output Admittance	h_{ob}		.6		μmho
Switching Characteristics (I_C = −10 ma; I_{B1} = I_{B2} = 1 ma)					
Delay Time	t_d		.18		μsec
Rise Time	t_r		.45		μsec
Storage Time	t_s		.90		μsec
Fall Time	t_f		.35		μsec

*Derate 8 mw/°C increase in ambient temperature.
**Derate 2.5 mw/°C increase in ambient temperature.

2N123A

Certified to meet MIL-T-19500/30

Outline Drawing No. 8

2N135, 2N136, 2N137

Outline Drawing No. 7

The General Electric types 2N135, 2N136 and 2N137 are PNP alloy junction germanium transistors intended for RF and IF service in broadcast receivers. Special control of manufacturing processes provides a narrow spread of characteristics, resulting in uniformly high power gain at radio frequencies. These types are obsolete and available for replacement only.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)		2N135	2N136	2N137	
Voltage					
Common Base (emitter open)	V_{CBO}	−20	−20	−10	volts
Common Emitter (R_{BE} = 100 ohms)	V_{CER}	−20	−20	−10	volts
Common Emitter (R_{BE} = 1 megohm)	V_{CER}	−12	−12	−6	volts

Current					
Collector	I_C	—50	—50	—50	ma
Emitter	I_E	50	50	50	ma
Power					
Collector Dissipation	P_{CM}	100	100	100	mw
Temperature					
Storage	T_{STG}	85	85	85	°C
ELECTRICAL CHARACTERISTICS: Design Center Values (Common Base, 25°C, V_{CB} = 5v, I_E = 1 ma)					
Voltage Feedback Ratio (input open circuit, f = 1 mc)	h_{rb}	7	7	7	$\times 10^{-3}$
Output Capacitance (f = 1 mc)	C_{ob}	12	12	12	$\mu\mu f$

2N167

Outline Drawing No. 3

The General Electric Type 2N167 is an NPN germanium high frequency, high speed switching transistor intended for industrial and military applications where reliability is of prime importance. In order to achieve the high degree of reliability necessary in industrial and military applications, the 2N167 is designed to pass 500G 1 millisecond drop shock, 10,000G centrifuge, 10G of vibration fatigue and 10G variable frequency vibration, as well as temperature cycling, moisture resistance, and operating and storage life tests as outlined in MIL-T-19500A.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CB}	30	volts
Collector to Emitter	V_{CE}	30	volts
Emitter to Base	V_{EB}	5	volts
Current			
Collector	I_C	75	ma
Emitter	I_E	—75	ma
Power			
Collector Dissipation (25°C)*	P_C	65	mw
Total Transistor Dissipation (25°C)**	P_M	75	mw
Temperature			
Storage	T_{STG}	85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

		Min.	Typ.	Max.	
D-C Characteristics					
Forward Current Transfer Ratio (I_C = 8 ma; V_{CE} = 1v)	h_{FE}	17	30	90	
Base Input Voltage (I_B = .47 ma; I_C = 8 ma)	V_{BE}	.3*	.41	.6***	volts
Collector to Emitter Voltage (Base Open; I_C = .3 ma)	V_{CE}	30			volts
Saturation Voltage (I_B = .8 ma; I_C = 8 ma)	$V_{CE(SAT)}$		.35		volts
Cutoff Characteristics					
Collector Current (I_E = 0; V_{CB} = 15v)	I_{CO}		.6	1.5	μa
Emitter Current (I_C = 0; V_{EB} = 5v)	I_{EO}		.35	5	μa
High Frequency Characteristics (Common Base) (V_{CB} = 5v; I_E = 1 ma)					
Alpha Cutoff Frequency	f_{ab}	5.0	9.0		mc
Collector Capacity (f = 1 mc)	C_{ob}		2.5	6	$\mu\mu f$
Voltage Feedback Ratio (f = 1 mc)	h_{rb}		7.3		$\times 10^{-3}$
Low Frequency Characteristics (Common Base) (V_{CB} = 5v; I_E = —1 ma; f = 270 cps)					
Forward Current Transfer Ratio	h_{fb}	.952	.985	.995*	
Output Admittance	h_{ob}	.1*	.2	.7*	μmhos
Input Impedance	h_{ib}	25*	55	82*	ohms
Reverse Voltage Transfer Ratio	h_{rb}		1.5		$\times 10^{-4}$
Switching Characteristics (I_C = 8 ma; I_{B1} = .8 ma; I_{B2} = .8 ma)					
Turn-on Time	t_o		.4		μsec
Storage Time	t_s		.7		μsec
Fall Time	t_f		.2		μsec

*Derate 1.1 mw/°C increase in ambient temperature.
**Derate 1.25 mw/°C increase in ambient temperature.
***These limits are design limits within which 98% of production normally fall.

USAF 2N167

Per MIL-T-19500/11

Outline Drawing No. 3

2N168A

Outline Drawing No. 3

The 2N168A is a rate-grown NPN germanium transistor intended for mixer/oscillator and IF amplifier applications in radio receivers. Special manufacturing techniques provide a low value and a narrow spread in collector capacity so that neutralization in many circuits is not required. The 2N168A has a frequency cutoff control to provide proper operation as an oscillator or autodyne mixer. For IF amplifier service the range in power gain in controlled to 3 db. This type is obsolete and is not recommended for new designs. For new designs we recommend type 2N1086.

CONVERTER TRANSISTOR SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Emitter (base open)	V_{CEO}	15	volts
Collector to Base (emitter open)	V_{CBO}	15	volts
Current			
Collector	I_C	—20	ma
Power			
Collector Dissipation at 25°C*	P_{CM}	65	mw
Temperature			
Operating and Storage	T_A, T_{STG}	—55 to 85	°C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

Converter Service			
Maximum Ratings			
Collector Suppiy Voltage	V_{CC}	12	volts
Design Center Characteristics			
Input Impedance (I_E = 1 ma; V_{CE} = 5v; f = 455 KC)	Z_i	400	ohms
Output Impedance (I_E = 1 ma; V_{CE} = 5v; f = 455 KC)	Z_o	12	K ohms
Voltage Feedback Ratio (I_E = 1 ma; V_{CB} = 5v; f = 1 mc)	h_{rb}	5	$\times 10^{-3}$
Collector to Base Capacitance (I_E = 1 ma; V_{CB} = 5v; f = 1 mc)	C_{ob}	2.4	μμf
Frequency Cutoff (I_E = 1 ma; V_{CB} = 5v)	f_{ab}	8	mc
Minimum Frequency Cutoff (I_E = 1 ma; V_{CB} = 5v)	f_{ab}	5	mc min
Base Current Gain (I_B = 20 μa; V_{CE} = 1v)	h_{FE}	40	
Minimum Base Current Gain	h_{FE}	23	
Maximum Base Current Gain	h_{FE}	135	
Conversion Gain	CG_e	25	db
IF Amplifier Performance			
Collector Supply Voltage	V_{CC}	5	volts
Collector Current	I_C	1	ma
Input Frequency	f	455	KC
Available Power Gain	G_e	39	db
Minimum Power Gain in typical IF circuit	G_e	28	db min
Power Gain Range of Variation in typical IF circuit	G_e	3	db
Cutoff Characteristics			
Collector Cutoff Current (V_{CB} = 5v)	I_{CO}	.5	μa
Collector Cutoff Current (V_{CB} = 15v)	I_{CO}	5	μa max

*Derate 1.1 mw/°C increase in ambient temperature over 25°C.

2N169

Outline Drawing No. 3

The General Electric Type 2N169 transistor is a rate-grown NPN germanium device, intended for use as an IF amplifier in broadcast radio receivers. The collector capacity is controlled to a uniformly low value so that neutralization in most circuits is not required. Power gain at 455KC in a typical receiver circuit is restricted to a 2.5db spread. The uniformity provided by the controls of collector capacity and power gain allows easy and economical incorporation of this type into receiver circuits. The 2N169 has special high beta characteristics required in the final stage of reflex IF circuits where large audio gain is desired.

IF TRANSISTOR SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Emitter (base open)	V_{CE}	15	volts
Collector to Base (emitter open)	V_{CB}	15	volts
Current			
Collector	I_C	−20	ma
Power			
Collector Dissipation at 25°C*	P_{CM}	65	mw
Temperature			
Operating and Storage	T_A, T_{STG}	−55 to 85	°C

ELECTRICAL CHARACTERISTICS:** (25°C)

IF Amplifier Service			
Maximum Ratings			
Collector Supply Voltage	V_{CC}	9	volts
Design Center Characteristics			
(I_E = 1 ma; V_{CE} = 5v; f = 455 KC except as noted)			
Input Impedance	Z_i	700	ohms
Output Impedance	Z_o	7	K ohms
Voltage Feedback Ratio (V_{CB} = 5v; f = 1 mc)	h_{rb}	10	$\times 10^{-8}$
Collector to Base Capacitance (V_{CB} = 5v; f = 1 mc)	C_{ob}	2.4	μμf
Frequency Cutoff (V_{CB} = 5v)	f_{ab}	8	mc
Base Current Gain (I_C = 1 ma; V_{CE} = 1v)	h_{FE}	72	
Minimum Base Current Gain	h_{FE}	34	
IF Amplifier Performance			
Collector Supply Voltage	V_{CC}	5	volts
Collector Current	I_C	2	ma
Input Frequency	f	455	KC
Minimum Power Gain in Typical IF Circuit	G_e	27	db
Power Gain Range of Variation in Typical IF Circuit	G_e	2.5	db
Cutoff Characteristics			
Collector Cutoff Current (V_{CB} = 5v)	I_{CO}	.5	μa
Collector Cutoff Current (V_{CB} = 15v)	I_{CO}	5	μa max

*Derate 1.1 mw/°C increase in ambient temperature.
**All values are typical unless indicated as a min. or max.

2N169A

Outline Drawing No. 3

The General Electric type 2N169A is a rate-grown NPN germanium transistor recommended for high gain RF and IF amplifier service and general purpose industrial applications where high beta, high voltage, low collector capacity and extremely low collector cutoff current are of prime importance.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CB}	25	volts
Collector to Emitter	V_{CE}	25	volts
Emitter to Base	V_{EB}	5	volts
Current			
Collector	I_C	−20	ma
Power			
Collector Dissipation*	P_C	65	mw
Temperature			
Storage	T_{STG}	−55 to 85	°C
Operating Junction	T_J	−55 to 85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

DC Characteristics		Min.	Design Center	Max.	
Collector to Emitter Breakdown Voltage (R_{BE} = 10 K; I_C = .3 ma)	BV_{CER}	25			
Punch-through Voltage	V_{PT}	25			
Forward Current Transfer Ratio (I_C = 1 ma; V_{CE} = 1v)	h_{FE}	34	72	200	
Base Input Voltage (I_C = 1 ma; V_{CE} = 1v)	V_{BE}	.1**	.14	.2**	
Saturation Voltage (I_B = .5; I_C = 5 ma)	$V_{CE(SAT)}$	.13**	.23	.4**	
Collector Current (I_E = 0; V_{CB} = 15v)	I_{CO}		.9	5	μa
Emitter Current (I_C = 0; V_{EB} = 5v)	I_{EO}		.9		μa
Low Frequency Characteristics (Common Emitter) (V_{CE} = 5v; I_E = 1 ma; f = 270 cps)					
Forward Current Transfer Ratio	h_{fe}		50		
Output Admittance	h_{ob}		.2		μmhos
Input Impedance	h_{ib}		55		ohms
Reverse Voltage Transfer Ratio	h_{rb}		2		$\times 10^{-4}$
High Frequency Characteristics (Common Emitter) (V_{CB} = 5v; I_E = 1 ma; f = 455 KC)					
Base Spreading Resistance	r'_b		250		ohms
Output Capacity	C_{ob}		2.4		μμf
Output Admittance	h_{oe}		140		μmhos
Input Impedance	h_{ie}		700		ohms
Reverse Voltage Transfer Ratio	h_{rb}		10		$\times 10^{-3}$
Noise Figure (B_W = 1 cycle) (f = 1 KC; V_{CB} = 1.5v; I_E = −0.5 ma) (Common Emitter)	NF		12		db
Power Gain (Typical IF Test Circuit)	G_e	27	28		db
Available Power Gain	G_e		39		db
Cutoff Frequency	f_{ab}		9		mc

*Derate 1.1 mw/°C increase in ambient temperature.
**These limits are design limits within which 98% of production normally falls.

2N170

Outline Drawing No. 3

The 2N170 is a rate grown NPN germanium transistor intended for use in high frequency circuits by amateurs, hobbyists, and experimenters. The 2N170 can be used in any of the many published circuits where a low voltage, high frequency transistor is necessary such as for regenerative receivers, high frequency oscillators, etc. If you desire to use the 2N170 NPN transistor in a circuit showing a PNP type transistor, it is only necessary to change the connections to the power supply.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Emitter	V_{CE}	6	volts
Current			
Collector	I_C	20	ma
Power			
Collector Dissipation*	P_{CM}	25	mw
Temperature			
Operating and Storage	T_A, T_{STG}	−55 to 85	°C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

High Frequency Characteristics			
(I_E = 1 ma; V_{CE} = 5v; f = 455 KC except as noted)			
Input Impedance (Common Emitter)	Z_i	800	ohms
Output Impedance (Common Emitter)	Z_o	15	K ohms
Collector to Base Capacitance (f = 1 mc)	C_{ob}	2.4	$\mu\mu$f
Frequency Cutoff (V_{CB} = 5v)	f_{ab}	4	mc
Power Gain (Common Emitter)	G_e	22	db
Low Frequency Characteristics			
(I_E = 1 ma; V_{CE} = 5v; f = 270 cps)			
Input Impedance	h_{ib}	55	ohms
Voltage Feedback Ratio	h_{rb}	4	$\times 10^{-4}$
Current Gain	h_{fb}	.95	
Output Admittance	h_{ob}	.5	$\times 10^{-6}$ μmhos
Common Emitter Base Current Gain	h_{fe}	20	
Cutoff Characteristics			
Collector Cutoff Current (V_{CB} = 5v)	Ico	5	μa max

*Derate 1 mw/°C increase in ambient temperature.

2N186A, 2N187A 2N188A

Outline Drawing No. 1

The 2N186A, 2N187A, and 2N188A are medium power PNP transistors intended for use as audio output amplifiers in radio receivers and quality sound systems. By unique process controls the current gain is maintained at an essentially constant value for collector currents from 1 ma to 200 ma. This linearity of current gain provides low distortion in both Class A and Class B circuits, and permits the use of any two transistors from a particular type without matching in Class B Circuits. These types may be substituted for Types 2N186, 2N187, 2N188 respectively.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base (emitter open)	V_{CBO}	−25	volts
Collector to Emitter (R_{EB} = 10K ohm)	V_{CER}	−25	volts
Emitter to Base (collector open)	V_{EBO}	−5	volts
Current			
Collector	I_C	−200	ma
Power			
Collector Dissipation*	P_{CM}	200	mw
Temperature			
Operating	T_A	−55 to 75	°C
Storage	T_{STG}	−55 to 85	°C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

Class B Audio Amplifier Operation		**2N186A**	**2N187A**	**2N188A**	
(Values for two transistors. Note that matching is not required to hold distortion to less than 5% for any two transistors from a type)					
Maximum Class B Ratings (Common Emitter)					
Collector Supply Voltage	V_{CC}	−12	−12	−12	volts
Power Output (Distortion less than 5%)	P_o	750	750	750	mw
Design Center Characteristics					
Input Impedance (large signal base to base) (ΔI_E = 100 ma)	h_{ie}	1200	2000	2600	ohms
Base Current Gain (V_{CE} = −1v; I_C = 100 ma)	h_{FE}	24	36	54	
Collector Capacity (V_{CB} = 5v; I_E = 1 ma; f = 1 mc)	C_{ob}	40	40	40	$\mu\mu$f
Frequency Cutoff (V_{CB} = −5v; I_E = 1 ma)	f_{ab}	.8	1.0	1.2	mc
Class B Circuit Performance (Common Emitter)					
Collector Voltage	V_{CC}	−12	−12	−12	volts
Minimum Power Gain at 100 mw power output	G_e	28	30	32	min db
Class A Audio Amplifier Operation (Common Emitter)					
(V_{CC} = 12v; I_E = 10 ma)					
Power Gain at 50 mw power output	G_e	30	32	34	db
Cutoff Characteristics					
Maximum Collector Cutoff Current (V_{CB} = −25v)	Ico	−16	−16	−16	max μa
Maximum Emitter Cutoff Current (V_{EB} = −5v)	I_{EO}	−10	−10	−10	max μa

*Derate 4 mw/°C increase in ambient temperature within range 25°C to 75°C.

2N189, 2N190, 2N191, 2N192

Outline Drawing No. 1

The 2N189, 2N190, 2N191, and 2N192 are alloy junction PNP transistors intended for driver service in transistorized audio amplifiers. By control of transistor characteristics during manufacture, a specific power gain is provided for each type. Special processing techniques and the use of hermetic seals provides stability of these characteristics throughout life.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Emitter (R_{EB} = 10K ohm)	V_{CER}	−25	volts
Current			
Collector	I_C	−50	ma
Power			
Collector Dissipation (25°C)*	P_{CM}	75	mw
Temperature			
Operating	T_A	−55 to 60	°C
Storage	T_{STG}	−55 to 85	°C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

Audio Driver Class A Operation (Values for one transistor driving a transformer coupled output stage)		2N189	2N190	2N191	2N192	
Maximum Class A Ratings (Common Emitter)						
Collector Supply Voltage	V_{CC}	−12	−12	−12	−12	volts
Design Center Characteristics						
Input Impedance base to emitter (I_E = 1 ma)	h_{ie}	1000	1400	1800	2200	ohms
Base Current Gain (V_{CE} = −5v; I_E = 1 ma)	h_{fe}	32	42	67	90	
Collector Capacity (V_{CB} = −5v; I_E = 1 ma)	C_{ob}	40	40	40	40	μμf
Frequency Cutoff (V_{CB} = −5v; I_E = 1 ma)	f_{ab}	.8	1.0	1.2	1.5	mc
Noise Figure (V_{CB} = −5v; I_E = 1 ma; f = 1 KC; BW = 1 cycle)	NF	15	15	15	15	db
Audio Circuit Performance (Common Emitter)						
Collector Supply Voltage	V_{CC}	−12	−12	−12	−12	volts
Emitter Current	I_E	1	1	1	1	ma
Minimum Power Gain at 1 mw power output	G_e	37	39	41	43	min db
Small Signal Characteristics (Common Base) (V_{CB} = −5v; I_E = 1 ma; f = 270 cps)						
Input Impedance	h_{ib}	29	29	29	29	ohms
Voltage Feedback Ratio	h_{rb}	4	4	4	4	$\times 10^{-4}$
Current Amplification	h_{fb}	−.96	−.973	−.98	−.987	
Output Admittance	h_{ob}	1.0	.8	.6	.5	μmhos
Cutoff Characteristics						
Maximum Collector Cutoff Current (V_{CB} = −25v)	I_{CO}	−16	−16	−16	−16	max μa

*Derate 2 mw/°C increase in ambient temperature within range 25°C to 60°C.

2N241, 2N241A

Outline Drawing No. 1

The 2N241 and 2N241A are medium power PNP transistors intended for use as audio output amplifiers in radio receivers and quality sound systems. By special process controls the current gain is maintained at an essentially constant value for collector currents from 1 ma to 200 ma. This linearity of current gain insures low distortion in both Class A and Class B circuits, and permits the use of any two transistors from a particular type without matching in Class B Circuits. The 2N241 is now obsolete and the 2N241A should be specified in new designs.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

		2N241	2N241A	
Voltage				
Collector to Base (emitter open)	V_{CBO}	−25	−25	volts
Collector to Emitter (R_{EB} = 10K ohm)	V_{CER}	−25	−25	volts
Emitter to Base (collector open)	V_{EBO}	− 5	− 5	volts
Current				
Collector	I_C	−200	−200	ma
Power				
Collector Dissipation	P_{CM}	100*	200**	mw
Temperature				
Operating	T_A	−55 to 60	−55 to 75	°C
Storage	T_{STG}	−55 to 85	−55 to 85	°C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

Class B Audio Amplifier Operation

(Values for two transistors. Note that matching is not required to hold distortion to less than 5% for any two transistors from a type)

Maximum Class B Ratings (Common Emitter)		2N241	2N241A	
Collector Supply Voltage	V_{CC}	−12	−12	volts
Power Output (Distortion less than 5%)	P_o	300	750	mw
Design Center Characteristics				
Input Impedance large signal base to base ($\Delta I_E = 100$ ma)	h_{ie}	4000	4000	ohms
Base Current Gain ($V_{CE} = -1$v; $I_C = -100$ ma)	h_{FE}	73	73	
Collector Capacity ($V_{CB} = -5$v; $I_E = 1$ ma; f = 1 mc)	C_{ob}	40	40	$\mu\mu$f
Frequency Cutoff ($V_{CE} = -5$v; $I_E = 1$ ma)	f_{ab}	1.3	1.3	mc
Class B Circuit Performance (Common Emitter)				
Collector Voltage	V_{CC}	−12	−12	volts
Minimum Power Gain at 100 mw power output	G_e	34	34	min db
Class A Audio Amplifier Operation (Common Emitter) ($V_{CC} = -12$v; $I_E = 10$ ma)				
Power Gain at 50 mw power output	G_e	35	35	db
Cutoff Characteristics				
Maximum Collector Cutoff Current ($V_{CB} = -25$v)	I_{CO}	−16	−16	max μa
Maximum Emitter Cutoff Current ($V_{EB} = -5$v)	I_{EO}	−10	−10	max μa

*Derate 3 mw/°C increase in ambient temperature within range 25°C to 60°C.
**Derate 4 mw/°C increase in ambient temperature within range 25°C to 75°C.

2N265

Outline Drawing No. 1

The 2N265 is an alloy junction PNP transistor intended for driver service in transistorized audio amplifiers. By control of transistor characteristics during manufacture, a specific power gain is provided· for each type. Special processing techniques and the use of hermetic seals provides stability of these characteristics throughout life.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Emitter (R_{EB} = 10K ohm)	V_{CER}	−25	volts
Current			
Collector	I_C	−50	ma
Power			
Collector Dissipation (25°C)*	P_{CM}	75	mw
Temperature			
Operating	T_A	−55 to 60	°C
Storage	T_{STG}	−55 to 85	°C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

Audio Driver Class A Operation

(Values for one transistor driving a transformer coupled output stage)

Maximum Class A Ratings (Common Emitter)			
Collector Supply Voltage	V_{CC}	−12	volts
Design Center Characteristics			
Input Impedance base to emitter ($I_E = 1$ ma)	h_{ie}	4000	ohms
Base Current Gain ($V_{CE} = -5$v; $I_E = 1$ ma)	h_{fe}	115	
Collector Capacity ($V_{CB} = -5$v; $I_E = 1$ ma)	C_{ob}	40	$\mu\mu$f
Frequency Cutoff ($V_{CB} = -5$v; $I_E = 1$ ma)	f_{ab}	1.5	mc
Noise Figure ($V_{CB} = -5$v; $I_E = 1$ ma; f = 1 KC; BW = 1 cycle)	NF	8	db
Audio Circuit Performance (Common Emitter)			
Collector Supply Voltage	V_{CC}	−12	volts
Emitter Current	I_E	1	ma
Minimum Power Gain at 1 mw power output	G_e	45	min db
Small Signal Characteristics (Common Base) ($V_{CB} = -5$v; $I_E = 1$ ma; f = 270 cps)			
Input Impedance	h_{ib}	29	ohms
Voltage Feedback Ratio	h_{rb}	4	$\times 10^{-4}$
Current Amplification	h_{fb}	−.991	
Output Admittance	h_{ob}	.5	μmhos
Cutoff Characteristics			
Maximum Collector Cutoff Current ($V_{CB} = -25$v)	I_{CO}	−16	max μa

*Derate 2 mw/°C increase in ambient temperature within range 25°C to 60°C.

2N292, 2N293

Outline Drawing No. 3

Types 2N292 and 2N293 are rate grown NPN germanium transistors intended for amplifier applications in radio receivers. Special manufacturing techniques provide a low value and a narrow spread in collector capacity so that neutralization in many circuits is not required. The type 2N293 is intended for receiver circuits where high gain is needed. In IF amplifier service the range in power gain is controlled to 2.5 db.

IF TRANSISTOR SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)		2N292	2N293	
Voltage				
Collector to Emitter (base open)	V_{CEO}	15	15	volts
Collector to Base (emitter open)	V_{CBO}	15	15	volts
Current				
Collector	I_C	20	20	ma
Power				
Collector Dissipation*	P_{CM}	65	65	mw
Temperature				
Operating and Storage	T_A, T_{STG}	—55 to 85	—55 to 85	°C
ELECTRICAL CHARACTERISTICS: (25°C)**				
IF Amplifier Service				
Maximum Ratings				
Collector Supply Voltage	V_{CC}	12	12	volts
Design Center Characteristics				
Input Impedance ($I_E = 1$ ma; $V_{CE} = 5$v; f = 455 KC)	Z_i	500	350	ohms
Output Impedance ($I_E = 1$ ma; $V_{CE} = 5$v; f = 455 KC)	Z_o	15	15	K ohms
Voltage Feedback Ratio ($I_E = 1$ ma; $V_{CB} = 5$v; f = 1 mc)	h_{rb}	10	5	$\times 10^{-3}$
Collector to Base Capacitance ($I_E = 1$ ma; $V_{CB} = 5$v; f = 1 mc)	C_{ob}	2.4	2.4	$\mu\mu$f
Frequency Cutoff ($I_E = 1$ ma; $V_{CB} = 5$v)	f_{ab}	5	8	mc
Base Current Gain ($I_B = 20\ \mu$a; $V_{CE} = 1$v)	h_{FE}	25	25	
Minimum Base Current Gain	h_{FE}	8	8	
Maximum Base Current Gain	h_{FE}	51	51	
IF Amplifier Performance				
Collector Supply Voltage	V_{CC}	5	5	volts
Collector Current	I_C	1	1	ma
Input Frequency	f	455	455	KC
Minimum Power Gain in Typical IF Test Circuit	G_e	25.5	28	db min
Power Gain Range of Variation in Typical IF Circuit		2.5	2.5	db
Cutoff Characteristics				
Collector Cutoff Current ($V_{CB} = 5$v)	I_{CO}	.5	.5	μa
Collector Cutoff Current ($V_{CB} = 15$v)	I_{CO}	5	5	μa max

*Derate 1.1 mw/°C increase in ambient temperature over 25°C.
**All values are typical unless indicated as a min. or max.

2N319, 2N320, 2N321

Outline Drawing No. 2

The 2N319, 2N320, and 2N321 are miniaturized versions of the 2N186A series of G-E transistors. Like the prototype versions, the 2N319, 2N320, and 2N321 are medium power PNP transistors intended for use as audio output amplifiers in radio receivers and quality sound systems. By unique process controls the current gain is maintained at an essentially constant value for collector currents from 1 ma to 200 ma. This linearity of current gain provides low distortion in both Class A and Class B circuits, and permits the use of any two transistors from a particular type without matching in Class B Circuits.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)			
Voltage			
Collector to Emitter	V_{CE}	—20	volts
Collector to Base	V_{CB}	—30	volts
Emitter to Base	V_{EB}	—3	volts
Current			
Collector	I_C	—200	ma

Power					
Collector Dissipation	P_{CM}			225	mw
Temperature					
Operating and Storage	T_A, T_{STG}			−65 to 85	°C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

D.C. Characteristics		2N319	2N320	2N321	
Base Current Gain (I_C = −20 ma; V_{CE} = −1v)	h_{FE}	34	50	80	
Base Current Gain (I_C = −100 ma; V_{CE} = −1v)	h_{FE}	31	45	70	
Collector to Emitter Voltage (R_{EB} = 10K; I_C = .6 ma)	V_{CER}	−20	−20	−20	volts
Collector Cutoff Current (V_{CB} −25v)	I_{CO}	−8	−8	−8	μa
Maximum Collector Cutoff Current (V_{CB} = −25v)	I_{CO}	−16	−16	−16	μa
Emitter Cutoff Current (V_{EB} = −3v)	I_{EO}	−2	−2	−2	μa
Small Signal Characteristics (Common Base) (V_{CB} = −5v; I_E = 1 ma; f = 270 cps)					
Frequency Cutoff	f_{ab}	2.0	2.5	3.1	mc
Collector Capacity (f = 1 mc)	C_{ob}	25	25	25	μμf
Noise Figure	NF	6	6	6	db
Input Impedance	h_{ib}	30	30	30	ohms
Thermal Characteristics					
Thermal Resistance					
Without Heat Sink (Junction to Air)		.27	.27	.27	°C/mw
With Clip On Heat Sink (Junction to Case)		.2	.2	.2	°C/mw
Performance Data (Common Emitter)					
Class A Power Gain (V_{CC} = −9v)	G_e	30	31	32	db
Power Output	P_o	50	50	50	mw
Class B Power Gain (V_{CC} = −9v)	G_e	27	29	31	db
Power Output	P_o	100	100	100	mw

2N322, 2N323, 2N324

Outline Drawing No. 2

The 2N322, 2N323, 2N324 are alloy junction PNP transistors intended for driver service in audio amplifiers. They are miniaturized versions of the 2N190 series of G.E. transistors. By control of transistor characteristics during manufacture, a specific power gain is provided for each type. Special processing techniques and the use of hermetic seals provides stability of these characteristics throughout life.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage					
Collector to Emitter	V_{CE}			−16	volts
Collector to Base	V_{CB}			−16	volts
Current					
Collector	I_C			−100	ma
Power					
Collector Dissipation	P_{CM}			140	mw
Temperature					
Operating	T_A			−65 to 60	°C
Storage	T_{STG}			−65 to 85	°C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

D.C. Characteristics		2N322	2N323	2N324	
Base Current Gain (I_C=−20 ma; V_{CE}=−1v)	h_{FE}	50	75	95	
Collector to Emitter Voltage (R_{EB} = 10K; I_C = −.6 ma)	V_{CER}	−16	−16	−16	volts
Collector Cutoff Current (V_{CB} = −16v)	I_{CO}	−10	−10	−10	μa
Max. Collector Cutoff Current (V_{CB} = −16v)	I_{CO}	−16	−16	−16	μa
Small Signal Characteristics					
Frequency Cutoff (V_{CB} = −5v; I_E = 1 ma)	f_{ab}	2.0	2.5	3.0	mc
Collector Capacity (V_{CB} = −5v; I_E = 1 ma)	C_{ob}	25	25	25	μμf
Noise Figure (V_{CB} = −5v; I_E = 1 ma)	NF	6	6	6	db
Input Impedance (V_{CE} = −5v; I_E = 1 ma)	h_{ie}	2200	2600	3300	ohms
Current Gain (V_{CE} = −5v; I_E = 1 ma)	h_{fe}	45	68	85	
Thermal Characteristics					
Thermal Resistance Junction to Air		.25	.25	.25	°C/mw
Performance Data Common Emitter					
Power Gain Driver (V_{CC} = 9v)	G_e	39	41	43	db
Power Output	P_o	1	1	1	mw

2N332

Outline Drawing No. 4

The General Electric Type 2N332 is a silicon NPN transistor intended for amplifier applications in the audio and radio frequency range and for general purpose switching circuits. They are grown junction devices with a diffused base and are manufactured in the Fixed-Bed Mounting design for extremely high mechanical reliability under severe conditions of shock, vibration, centrifugal force, and temperature. These transistors are hermetically sealed in welded cases. The case dimensions and lead configuration conform to JEDEC standards and are suitable for insertion in printed boards by automatic assembly equipment. All transistors are cycle-aged at a temperature of 200°C for a minimum of 160 hours to enhance their electrical stability.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base (Emitter Open)	V_{CBO}	45	volts
Emitter to Base (Collector Open)	V_{EBO}	1	volt
Current			
Collector	I_C	25	ma
Power			
Collector Dissipation (25°C)	P_C	150	mw
Collector Dissipation (100°C)	P_C	100	mw
Collector Dissipation (150°C)	P_C	50	mw
Temperature			
Storage	T_{STG}	—65 to 200	°C
Operating	T_A	—65 to 175	°C

ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified $V_{CB} = 5v$; $I_E = -1$ ma; f = 1 kc)

		Min.	Nom.	Max.	
Small Signal Characteristics					
Current Transfer Ratio	h_{fe}	9	15	22	
Input Impedance	h_{ib}	30	43	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}	.25	1.5	5.0	$\times 10^{-4}$
Output Admittance	h_{ob}	0.0	.25	1.2	μmhos
Power Gain ($V_{CE} = 20v$; $I_E = -2$ ma; f = 1 kc; $R_G = 1K$ ohms; $R_L = 20K$ ohms)	G_e		35		db
Noise Figure	NF		20		db
High Frequency Characteristics					
Frequency Cutoff ($V_{CB} = 5v$; $I_E = -1$ ma)	f_{ab}		10		mc
Collector to Base Capacity ($V_{CB} = 5v$; $I_E = -1$ ma; f = 1 mc)	C_{ob}		7		$\mu\mu$f
Power Gain (Common Emitter) ($V_{CB} = 20v$; $I_E = -2$ ma; f = 5 mc)	G_e		14		db
D-C Characteristics					
Common Emitter Current Gain ($V_{CE} = 5v$; $I_C = 1$ ma)	h_{FE}		14		
Collector Breakdown Voltage ($I_{CBO} = 50\ \mu a$; $I_E = 0$; $T_A = 25°C$)	BV_{CBO}	45			volts
Collector Cutoff Current ($V_{CB} = 30v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.002	2	μa
($V_{CB} = 5v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			50	μa
Collector Saturation Resistance ($I_B = 1$ ma; $I_C = 5$ ma)	R_{SC}		90	200	ohms
Switching Characteristics ($I_{B_1} = 0.5$ ma; $I_{B_2} = -0.5$ ma; $I_C = 5.0$ ma)					
Delay Time	t_d		.7		μsec
Rise Time	t_r		.65		μsec
Storage Time	t_s		.4		μsec
Fall Time	t_f		.13		μsec

2N333

Outline Drawing No. 4

The General Electric Type 2N333 is a silicon NPN transistor intended for amplifier applications in the audio and radio frequency range and for general purpose switching circuits. They are grown junction devices with a diffused base and are manufactured in the Fixed-Bed Mounting design for extremely high mechanical reliability under severe conditions of shock, vibration, centrifugal force, and temperature. These transistors are hermetically sealed in welded cases. The case dimensions and lead configuration conform to JEDEC standards and are suitable for insertion in printed boards by automatic assembly equipment. All transistors are cycle-aged at a temperature of 200°C for a minimum of 160 hours to enhance their electrical stability.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base (Emitter Open)	V_{CBO}	45	volts
Emitter to Base (Collector Open)	V_{EBO}	1	volt
Current			
Collector	I_C	25	ma
Power			
Collector Dissipation (25°C)	P_C	150	mw
Collector Dissipation (100°C)	P_C	100	mw
Collector Dissipation (150°C)	P_C	50	mw
Temperature			
Storage	T_{STG}	—65 to 200	°C
Operating	T_A	—65 to 175	°C

ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified $V_{CB} = 5v$; $I_E = -1$ ma; $f = 1$ kc)

		Min.	Nom.	Max.	
Small Signal Characteristics					
Current Transfer Ratio	h_{fe}	18	30	44	
Input Impedance	h_{ib}	30	43	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}	.25	2.0	10.0	$\times 10^{-4}$
Output Admittance	h_{ob}	0.0	.2	1.2	μmhos
Power Gain ($V_{CE} = 20v$; $I_E = -2$ ma; $f = 1$ kc; $R_G = 1K$ ohms; $R_L = 20K$ ohms)	G_e		39		db
Noise Figure	NF		15		db
High Frequency Characteristics					
Frequency Cutoff ($V_{CB} = 5v$; $I_E = -1$ ma)	f_{ab}		12		mc
Collector to Base Capacity ($V_{CB} = 5v$; $I_E = -1$ ma; $f = 1$ mc)	C_{ob}		7		μμf
Power Gain (Common Emitter) ($V_{CB} = 20v$; $I_E = -2$ ma; $f = 5$ mc)	G_e		14		db
D-C Characteristics					
Common Emitter Current Gain ($V_{CE} = 5v$; $I_C = 1$ ma)	h_{FE}		31		
Collector Breakdown Voltage ($I_{CBO} = 50$ μa; $I_E = 0$; $T_A = 25°C$)	BV_{CBO}	45			volts
Collector Cutoff Current ($V_{CB} = 30v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.002	2	μa
($V_{CB} = 5v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			50	μa
Collector Saturation Resistance ($I_B = 1$ ma; $I_C = 5$ ma)	R_{SC}		80	200	ohms
Switching Characteristics ($I_{B_1} = 0.5$ ma; $I_{B_2} = -0.5$ ma; $I_C = 5.0$ ma)					
Delay Time	t_d		.65		μsec
Rise Time	t_r		.55		μsec
Storage Time	t_s		.75		μsec
Fall Time	t_f		.14		μsec

2N334

Outline Drawing No. 4

The General Electric Type 2N334 is a silicon NPN transistor intended for amplifier applications in the audio and radio frequency range and for general purpose switching circuits. They are grown junction devices with a diffused base and are manufactured in the Fixed-Bed Mounting design for extremely high mechanical reliability under severe conditions of shock, vibration, centrifugal force, and temperature. These transistors are hermetically sealed in welded cases. The case dimensions and lead configuration conform to JEDEC standards and are suitable for insertion in printed boards by automatic assembly equipment. All transistors are cycle-aged at a temperature of 200°C for a minimum of 160 hours to enhance their electrical stability.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base (Emitter Open)	V_{CBO}	45	volts
Emitter to Base (Collector Open)	V_{EBO}	1	volt
Current			
Collector	I_C	25	ma
Power			
Collector Dissipation (25°C)	P_C	150	mw
Collector Dissipation (100°C)	P_C	100	mw
Collector Dissipation (150°C)	P_C	50	mw
Temperature			
Storage	T_{STG}	—65 to 200	°C
Operating	T_A	—65 to 175	°C

ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified $V_{CB} = 5v$; $I_E = -1$ ma; $f = 1$ kc)

Small Signal Characteristics		Min.	Nom.	Max.	
Current Transfer Ratio	h_{fe}	18	39	90	
Input Impedance	h_{ib}	30	43	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}	.5	2.5	10.0	$\times 10^{-4}$
Output Admittance	h_{ob}	0.0	.18	1.2	μmhos
Power Gain ($V_{CE} = 20v$; $I_E = -2$ ma; $f = 1$ kc; $R_G = 1K$ ohms; $R_L = 20K$ ohms)	G_e		40		db
Noise Figure	NF		15		db
High Frequency Characteristics					
Frequency Cutoff ($V_{CB} = 5v$; $I_E = -1$ ma)	f_{ab}	8.0	13		mc
Collector to Base Capacity ($V_{CB} = 5v$; $I_E = -1$ ma; $f = 1$ mc)	C_{ob}		7		$\mu\mu$f
Power Gain (Common Emitter) ($V_{CB} = 20v$; $I_E = -2$ ma; $f = 5$ mc)	G_e		13		db
D-C Characteristics					
Common Emitter Current Gain ($V_{CE} = 5v$; $I_C = 1$ ma)	h_{FE}		38		
Collector Breakdown Voltage ($I_{CBO} = 50\ \mu a$; $I_E = 0$; $T_A = 25°C$)	BV_{CBO}	45			volts
Collector Cutoff Current ($V_{CB} = 30v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.002	2	μa
($V_{CB} = 5v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			50	μa
Collector Saturation Resistance ($I_B = 1$ ma; $I_C = 5$ ma)	R_{SC}		75	200	ohms
Switching Characteristics ($I_{B_1} = 0.5$ ma; $I_{B_2} = -0.5$ ma; $I_C = 5.0$ ma)					
Delay Time	t_d		.65		μsec
Rise Time	t_r		.55		μsec
Storage Time	t_s		.80		μsec
Fall Time	t_f		.15		μsec

2N335

Outline Drawing No. 4

The General Electric Type 2N335 is a silicon NPN transistor intended for amplifier applications in the audio and radio frequency range and for general purpose switching circuits. They are grown junction devices with a diffused base and are manufactured in the Fixed-Bed Mounting design for extremely high mechanical reliability under severe conditions of shock, vibration, centrifugal force, and temperature. These transistors are hermetically sealed in welded cases. The case dimensions and lead configuration conform to JEDEC standards and are suitable for insertion in printed boards by automatic assembly equipment. All transistors are cycle-aged at a temperature of 200°C for a minimum of 160 hours to enhance their electrical stability.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base (Emitter Open)	V_{CBO}	45	volts
Emitter to Base (Collector Open)	V_{EBO}	1	volt
Current			
Collector	I_C	25	ma
Power			
Collector Dissipation (25°C)	P_C	150	mw
Collector Dissipation (100°C)	P_C	100	mw
Collector Dissipation (150°C)	P_C	50	mw
Temperature			
Storage	T_{STG}	−65 to 200	°C
Operating	T_A	−65 to 175	°C

ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified $V_{CB} = 5v$; $I_E = -1$ ma; $f = 1$ kc)

		Min.	Nom.	Max.	
Small Signal Characteristics					
Current Transfer Ratio	h_{fe}	37	60	90	
Input Impedance	h_{ib}	30	43	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}	.5	3.0	10.0	$\times 10^{-4}$
Output Admittance	h_{ob}	0.0	.15	1.2	μmhos
Power Gain ($V_{CE} = 20v$; $I_E = -2$ ma; $f = 1$ kc; $R_G = 1K$ ohms; $R_L = 20K$ ohms)	G_e		42		db
Noise Figure	NF		12		db
High Frequency Characteristics					
Frequency Cutoff ($V_{CB} = 5v$; $I_E = -1$ ma)	f_{ab}		14		mc
Collector to Base Capacity ($V_{CB} = 5v$; $I_E = -1$ ma; $f = 1$ mc)	C_{ob}		7		μμf
Power Gain (Common Emitter) ($V_{CB} = 20v$; $I_E = -2$ ma; $f = 5$ mc)	G_e		13		db
D-C Characteristics					
Common Emitter Current Gain ($V_{CE} = 5v$; $I_C = 1$ ma)	h_{FE}		56		
Collector Breakdown Voltage ($I_{CBO} = 50$ μa; $I_E = 0$; $T_A = 25°C$)	BV_{CBO}	45			volts
Collector Cutoff Current ($V_{CB} = 30v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.002	2	μa
($V_{CB} = 5v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			50	μa
Collector Saturation Resistance ($I_B = 1$ ma; $I_C = 5$ ma)	R_{SC}		70	200	ohms
Switching Characteristics ($I_{B_1} = 0.5$ ma; $I_{B_2} = -0.5$ ma; $I_C = 5.0$ ma)					
Delay Time	t_d		.6		μsec
Rise Time	t_r		.5		μsec
Storage Time	t_s		.9		μsec
Fall Time	t_f		.15		μsec

2N336

Outline Drawing No. 4

The General Electric Type 2N336 is a silicon NPN transistor intended for amplifier applications in the audio and radio frequency range and for general purpose switching circuits. They are grown junction devices with a diffused base and are manufactured in the Fixed-Bed Mounting design for extremely high mechanical reliability under severe conditions of shock, vibration, centrifugal force, and temperature. These transistors are hermetically sealed in welded cases. The case dimensions and lead configuration conform to JEDEC standards and are suitable for insertion in printed boards by automatic assembly equipment. All transistors are cycle-aged at a temperature of 200°C for a minimum of 160 hours to enhance their electrical stability.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base (Emitter Open)	V_{CBO}	45	volts
Emitter to Base (Collector Open)	V_{EBO}	1	volt
Current			
Collector	I_C	25	ma
Power			
Collector Dissipation (25°C)	P_C	150	mw
Collector Dissipation (100°C)	P_C	100	mw
Collector Dissipation (150°C)	P_C	50	mw
Temperature			
Storage	T_{STG}	—65 to 200	°C
Operating	T_A	—65 to 175	°C

ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified $V_{CB} = 5v$; $I_E = -1$ ma; f = 1 kc)

		Min.	Nom.	Max.	
Small Signal Characteristics					
Current Transfer Ratio	h_{fe}	76	120	333	
Input Impedance	h_{ib}	30	43	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}	.5	4.0	10.0	$\times 10^{-4}$
Output Admittance	h_{ob}	0.0	.13	1.2	μmhos
Power Gain ($V_{CE} = 20v$; $I_E = -2$ ma; f = 1 kc; $R_G = 1K$ ohms; $R_L = 20K$ ohms)	G_e		43		db
Noise Figure	NF		10		db
High Frequency Characteristics					
Frequency Cutoff ($V_{CB} = 5v$; $I_E = -1$ ma)	f_{ab}		15		mc
Collector to Base Capacity ($V_{CB} = 5v$; $I_E = -1$ ma; f = 1 mc)	C_{ob}		7		μμf
Power Gain (Common Emitter) ($V_{CB} = 20v$; $I_E = -2$ ma; f = 5 mc)	G_e		12		db
D-C Characteristics					
Common Emitter Current Gain ($V_{CE} = 5v$; $I_C = 1$ ma)	h_{FE}		100		
Collector Breakdown Voltage ($I_{CBO} = 50$ μa; $I_E = 0$; $T_A = 25°C$)	BV_{CBO}	45			volts
Collector Cutoff Current ($V_{CB} = 30v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.002	2	μa
($V_{CB} = 5v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			50	μa
Collector Saturation Resistance ($I_B = 1$ ma; $I_C = 5$ ma)	R_{SC}		70	200	ohms
Switching Characteristics ($I_{B_1} = 0.5$ ma; $I_{B_2} = -0.5$ ma; $I_C = 5.0$ ma)					
Delay Time	t_d		.5		μsec
Rise Time	t_r		.4		μsec
Storage Time	t_s		1.4		μsec
Fall Time	t_f		.2		μsec

2N337, 2N338

Outline Drawing No. 4

The General Electric Types 2N337 and 2N338 are high-frequency silicon NPN transistors intended for amplifier applications in the audio and radio frequency range and for high-speed switching circuits. They are grown junction devices with a diffused base and are manufactured in the Fixed-Bed Mounting design for extremely high mechanical reliability under severe conditions of shock, vibration, centrifugal force, and temperature. For electrical reliability and parameter stability, all transistors are subjected to a minimum 160 hour 200°C cycled aging operation included in the manufacturing process. These transistors are hermetically sealed in welded cases. The case dimensions and lead configuration conform to JEDEC standards and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CBO}	45	volts
Emitter to Base	V_{EBO}	1	volt
Current			
Collector	I_C	20	ma
Power			
Collector Dissipation*	P_C	125	mw
Temperature			
Storage	T_{STG}	−65 to 200	°C
Operating	T_A	−65 to 150	°C

ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified; $V_{CB} = 20v$; $I_E = -1$ ma; f = 1 kc)

		2N337			2N338			
Small-Signal Characteristics		Min.	Typ.	Max.	Min.	Typ.	Max.	
Current Transfer Ratio	h_{fe}	19	55		39	99		
Input Impedance	h_{ib}	30	47	80	30	47	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}		180	2000		200	2000	$\times 10^{-6}$
Output Admittance	h_{ob}		.1	1		.1	1	µmho
High-Frequency Characteristics								
Alpha Cutoff Frequency	f_{ab}	10	30		20	45		mc
Collector Capacitance (f = 1 mc)	C_{ob}		1.4	3		1.4	3	µµf
Common Emitter Current Gain (f = 2.5 mc)	h_{fe}	14	24		20	26		
D-C Characteristics								
Common Emitter Current Gain ($V_{CE} = 5v$; $I_C = 10$ ma)	h_{FE}	20	35	55	45	75	150	
Collector Breakdown Voltage ($I_{CBO} = 50$ µa; $I_E = 0$)	BV_{CBO}	45			45			volts
Emitter Breakdown Voltage ($I_{EBO} = -50$ µa; $I_C = 0$)	BV_{EBO}	1			1			volt
Collector Saturation Resistance ($I_B = 1$ ma; $I_C = 10$ ma)	R_{SC}		100	150				ohms
($I_B = .5$ ma; $I_C = 10$ ma)	R_{SC}					100	150	ohms
Cutoff Characteristics								
Collector Current ($V_{CB} = 20v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.002	1		.002	1	µa
Collector Current ($V_{CB} = 20v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			100			100	µa
Switching Characteristics								
Rise Time	t_r		.02			.06		µsecs
Storage Time	t_s		.02			.02		µsecs
Fall Time	t_f		.04			.14		µsecs

*Derate 1 mw/°C increase in ambient temperature over 25°C

2N394

Outline Drawing No. 2

The General Electric Type 2N394 is a germanium PNP alloy junction high frequency switching transistor intended for military, industrial and data processing applications where high reliability at the maximum ratings is of prime importance. As a special control in manufacture, all 2N394 transistors are subjected to a high pressure detergent test to enhance reliable hermetic seals and are also aged at a temperature of 100°C for 96 hours minimum.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CB}	−30	volts
Collector to Emitter	V_{CE}	−10	volts
Emitter to Base	V_{EB}	−20	volts
Current			
Collector	I_C	−200	ma
Power			
Dissipation	P_{AV}	150	mw
Temperature			
Storage	T_{STG}	−65 to 85	°C
Operating Junction	T_J	85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

D-C Characteristics		Min.	Typ.	Max.	
D-C Base Current Gain					
($V_{CE} = -1v$; $I_C = -10$ ma)	h_{FE}	20	70		
($V_{CE} = -1v$; $I_C = -100$ ma)	h_{FE}	10	40		
Saturation Voltage ($I_B = -1.0$ ma; $I_C = -10$ ma)	$V_{CE(SAT)}$		−.04	−.15	volts
Base Input Voltage ($I_B = -1.0$ ma; $I_C = -10$ ma)	V_{BE}		−.27	−.35	volts
Collector Breakdown Voltage ($I_C = -100\ \mu a$)	BV_{CBO}	−30			volts
Emitter Breakdown Voltage ($I_C = -100\ \mu a$)	BV_{EBO}	−20			volts
Collector to Emitter Breakdown Voltage ($R_{BE} = 10K$ ohms; $I_C = -600\ \mu a$)	BV_{CER}	−15	−26		volts
Cutoff Characteristics					
Collector Current ($I_E = 0$; $V_{CB} = -10v$)	I_{CO}		−2.5	−6	μa
Emitter Current ($I_C = 0$; $V_{EB} = -5$)	I_{EO}		−2.0	−6	μa
Punch-through Voltage	V_{PT}	−10	−25		volts
High Frequency Characteristics (Common Base)					
($V_{CB} = -5v$; $I_E = 1$ ma)					
Alpha-Cutoff Frequency	f_{ab}	4	9		mc
Collector Capacitance (f = 1 mc)	C_{ob}		12	20	μμf
Base Spreading Resistance	r'_b		150		ohms

Thermal Resistance

Derate 2.5 mw/°C for temperatures over 25°C

2N395

Outline Drawing No. 2

The General Electric type 2N395 is a PNP alloy junction high frequency switching transistor intended for military, industrial, and data processing applications where high reliability and extreme stability of characteristics are of prime importance.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Emitter	V_{CE}	−15	volts
Collector to Base	V_{CB}	−30	volts
Emitter to Base	V_{EB}	−20	volts
Current			
Collector	I_C	−200	ma
Power			
Dissipation	P_{AV}	200	mw
Peak Dissipation (50 μsec. max. 20% duty cycle)	P_M	500	mw
Temperature			
Storage	T_{STG}	−65 to 100	°C

ELECTRICAL CHARACTERISTICS: (25°C)

D-C Characteristics		Min.	Typ.	Max.	
D-C Base Current Gain					
($V_{CE} = -1v$; $I_C = -10$ ma)	h_{FE}	20		150	
($V_{CE} = -0.35v$; $I_C = -200$ ma)	h_{FE}	10			
Saturation Voltage ($I_B = -5$ ma; $I_C = -50$ ma)	$V_{CE(SAT)}$		−0.1	−0.2	volts

Cutoff Characteristics

	Symbol	Min.	Typ.	Max.	Units
Collector Cutoff Current ($V_{CB} = -15v$)	I_{CO}		−2.5	−6	µamps
Emitter Cutoff Current ($V_{EB} = -10v$)	I_{EO}		−2.0	−6	µamps
Punch-through Voltage	V_{PT}	−15	−30		volts

High Frequency Characteristics (Common base)
($V_{CB} = -5v$; $I_E = 1$ ma)

	Symbol	Min.	Typ.	Max.	Units
Alpha Cutoff Frequency	f_{ab}	3	4.5		mc
Collector Capacity (f = 1 mc)	C_{ob}		12	20	µµf
Voltage Feedback Ratio (f = 1 mc)	h_{rb}		9		$\times 10^{-3}$
Base Spreading Resistance	r'_b		130	200	ohms

Switching Characteristics
($I_C = -10$ ma; $I_{B1} = I_{B2} = 1.0$ ma)

	Symbol	Min.	Typ.	Max.	Units
Delay Time	t_d		.21		µsec
Rise Time	t_r		.55		µsec
Storage Time	t_s		.50		µsec
Fall Time	t_f		.40		µsec

Thermal Characteristics

Derate 3.33 mw/°C increase in ambient temperature over 25°C

2N396

Outline Drawing No. 2

The General Electric type 2N396 is a PNP alloy junction high frequency switching transistor intended for military, industrial, and data processing applications where high reliability and extreme stability of characteristics are of prime importance.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

	Symbol	Value	Units
Voltage			
Collector to Emitter	V_{CE}	−20	volts
Collector to Base	V_{CB}	−30	volts
Emitter to Base	V_{EB}	−20	volts
Current			
Collector	I_C	−200	ma
Power			
Dissipation	P_{AV}	200	mw
Peak Dissipation (50 µsec. max. 20% duty cycle)	P_M	500	mw
Temperature			
Storage	T_{STG}	−65 to 100	°C

ELECTRICAL CHARACTERISTICS: (25°C)

D-C Characteristics

	Symbol	Min.	Typ.	Max.	Units
D-C Base Current Gain ($V_{CE} = -1v$; $I_C = -10$ ma)	h_{FE}	30		150	
($V_{CE} = -0.35v$; $I_C = -200$ ma)	h_{FE}	15			
Saturation Voltage ($I_B = -3.3$ ma; $I_C = -50$ ma)	$V_{CE(SAT)}$		−0.08	−0.2	volts

Cutoff Characteristics

	Symbol	Min.	Typ.	Max.	Units
Collector Cutoff Current ($V_{CB} = -20v$)	I_{CO}		−2.5	−6	µamps
Emitter Cutoff Current ($V_{EB} = -10v$)	I_{EO}		−2.0	−6	µamps
Punch-through Voltage	V_{PT}	−20	−35		volts

High Freqency Characteristics (Common base)
($V_{CB} = -5v$; $I_E = 1$ ma)

	Symbol	Min.	Typ.	Max.	Units
Alpha Cutoff Frequency	f_{ab}	5	8		mc
Collector Capacity (f = 1 mc)	C_{ob}		12	20	µµf
Voltage Feedback Ratio (f = 1 mc)	h_{rb}		10		$\times 10^{-3}$
Base Spreading Resistance	r'_b		140	200	ohms

Switching Characteristics
($I_C = -10$ ma; $I_{B1} = I_{B2} = 1.0$ ma)

	Symbol	Min.	Typ.	Max.	Units
Delay Time	t_d		.19		µsec
Rise Time	t_r		.40		µsec
Storage Time	t_s		.60		µsec
Fall Time	t_f		.31		µsec

Thermal Characteristics

Derate 3.3 mw/°C increase in ambient temperature over 25°C

2N396A

Outline Drawing No. 2

Certified to meet MIL-T-19500/64

2N397

Outline Drawing No. 2

The General Electric type 2N397 is a PNP alloy junction high frequency switching transistor intended for military, industrial, and data processing applications where high reliability and extreme stability of characteristics are of prime importance.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Emitter	V_{CE}	−15	volts
Collector to Base	V_{CB}	−30	volts
Emitter to Base	V_{EB}	−20	volts
Current			
Collector	I_C	−200	ma
Power			
Dissipation	P_{AV}	200	mw
Peak Dissipation (50 μsec. max. 20% duty cycle)	P_M	500	mw
Temperature			
Storage	T_{STG}	−65 to 100	°C

ELECTRICAL CHARACTERISTICS: (25°C)

D-C Characteristics		Min.	Typ.	Max.	
D-C Base Current Gain					
(V_{CE} = −1v; I_C = −10 ma)	h_{FE}	40		150	
(V_{CE} = −0.35v; I_C = −200 ma)	h_{FE}	20			
Saturation Voltage (I_B = −2.5 ma; I_C = −50 ma)	$V_{CE(SAT)}$		−0.07	−0.2	volts
Cutoff Characteristics					
Collector Cutoff Current (V_{CB} = −15v)	I_{CO}		−2.5	−6	μamps
Emitter Cutoff Current (V_{EB} = −10v)	I_{EO}		−2.0	−6	μamps
Punch-through Voltage	V_{PT}	−15	−20		volts
High Freqency Characteristics (Common base) (V_{CB} = −5v; I_E = 1 ma)					
Alpha Cutoff Frequency	f_{ab}	10	12		mc
Collector Capacity (f = 1 mc)	C_{ob}		12	20	μμf
Voltage Feedback Ratio (f = 1 mc)	h_{rb}		11		$\times 10^{-3}$
Base Spreading Resistance	r'_b		160		ohms
Switching Characteristics (I_C = −10 ma; I_{B1} = I_{B2} = 1.0 ma)					
Delay Time	t_d		.17		μsec
Rise Time	t_r		.3		μsec
Storage Time	t_s		.7		μsec
Fall Time	t_f		.28		μsec

Thermal Characteristics

Derate 3.3 mw/°C increase in ambient temperature over 25°C

2N404

Outline Drawing No. 2

The General Electric Type 2N404 is a germanium PNP alloy junction high frequency switching transistor, intended for military, industrial and data processing applications where high reliability and extreme stability of characteristics are of prime importance.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Emitter	V_{CE}	−24	volts
Collector to Base	V_{CB}	−25	volts
Emitter to Base	V_{EB}	−12	volts
Current			
Collector	I_C	−100	ma
Power			
Dissipation	P_C	120	mw
Temperature			
Storage	T_{STG}	−65 to 85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

D-C Characteristics		Min.	Typ.	Max.	
Collector Breakdown Voltage ($I_C = -20\ \mu a$; $I_E = 0$)	V_{CBO}	−25	−45		volts
Emitter Breakdown Voltage ($I_E = -20\ \mu a$; $I_C = 0$)	V_{EBO}	−12	−40		volts
Saturation Voltage ($I_B = -.4$ ma; $I_C = -12$ ma)	$V_{CE(SAT)}$		−.1	−.15	volts
($I_B = -1$ ma; $I_C = -24$ ma)	$V_{CE(SAT)}$		−.14	−.20	volts
Base Input Voltage ($I_B = -.4$ ma; $I_C = -12$ ma)	V_{BE}		−.24	−.35	volts
($I_B = -1$ ma; $I_C = -24$ ma)	V_{BE}		−.32	−.40	volts
Cutoff Characteristics					
Collector Current ($V_{CB} = -12$ volts; $I_E = 0$)	I_{CBO}		−2	−5	μa
($V_{CB} = -12$ volts; $I_E = 0$; $T_A = 80°C$)	I_{CBO}			−90	μa
Emitter Current ($V_{EB} = -2.5$ volts; $I_C = 0$)	I_{EBO}		−1	−2.5	μa
Punch-through Voltage	V_{PT}	−24	−40		volts
High-Frequency Characteristics					
Alpha-Cutoff Frequency ($V_{CB} = -6$ volts; $I_E = 1$ ma)	f_{ab}	4	8		mc
Collector Capacitance ($V_{CB} = -6$ volts; $I_E = 1$ ma)	C_{ob}		12	20	μμf
Stored Base Charge ($I_B = 1$ ma; $I_C = -10$ ma)	Q_{sb}			1400	μμcoulombs
Thermal Characteristic ($T_J = T_A/P_C$)				.35	°C/mw

2N448

Outline Drawing No. 3

The General Electric Type 2N448 transistor is a rate-grown NPN germanium device intended for IF amplifier applications in radio receivers. Special manufacturing techniques provide a low value and a narrow spread in collector capacity so that neutralization in many circuits is not required. In IF amplifier service, the range in power gain is controlled to 2.5 db.

IF TRANSISTOR SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Emitter (base open)	V_{CE}	15	volts
Collector to Base (emitter open)	V_{CB}	15	volts
Current			
Collector	I_C	−20	ma
Power			
Collector Dissipation at 25°C*	P_C	65	mw
Temperature			
Operating and Storage	T_A, T_{STG}	−55 to 85	°C

ELECTRICAL CHARACTERISTICS:**

IF Amplifier Service			
Maximum Ratings			
Collector Supply Voltage	V_{CC}	12	volts
Design Center Characteristics			
Input Impedance ($I_E = 1$ ma; $V_{CE} = 5v$; $f = 455$ KC)	Z_i	500	ohms
Output Impedance ($I_E = 1$ ma; $V_{CE} = 5v$; $f = 455$ KC)	Z_o	15	K ohms
Voltage Feedback Ratio ($I_E = 1$ ma; $V_{CB} = 5v$; $f = 1$ mc)	h_{rb}	10	$\times 10^{-3}$
Collector to Base Capacitance ($I_E = 1$ ma; $V_{CB} = 5v$; $f = 1$ mc)	C_{ob}	2.4	μμf
Frequency Cutoff ($I_E = 1$ ma; $V_{CB} = 5v$)	f_{ab}	5	mc
Base Current Gain ($I_C = 1$ ma; $V_{CE} = 1v$)	h_{FE}	25	
Minimum Base Current Gain	h_{FE}	8	
Maximum Base Current Gain	h_{FE}	51	
IF Amplifier Performance			
Collector Supply Voltage	V_{CC}	5	volts
Collector Current	I_E	1	ma
Input Frequency	f	455	KC
Minimum Power Gain in Typical IF Test Circuit	G_e	23	db min
Power Gain Range of Variation in Typical IF Circuit	G_e	2.5	db
Cutoff Characteristics			
Collector Cutoff Current ($V_{CB} = 5v$)	I_{CO}	.5	μa
Collector Cutoff Current ($V_{CB} = 15v$)	I_{CO}	5	μa max

*Derate 1.1 mw/°C increase in ambient temperature over 25°C.
**All values are typical unless indicated as a min. or max.

2N449

Outline Drawing No. 3

The General Electric Type 2N449 transistor is a rate-grown NPN germanium device, intended for use as an IF amplifier in broadcast radio receivers. The collector capacity is controlled to a uniformly low value so that neutralization in most circuits is not required. Power gain at 455KC in a typical receiver circuit is restricted to a 2.5db spread. The uniformity provided by the controls of collector capacity and power gain allows easy and economical incorporation of this type into receiver circuits. Type 2N449 has special high beta characteristics required in the final stage of reflex IF circuits where large audio gain is desired.

IF TRANSISTOR SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Emitter (base open)	V_{CE}	15	volts
Collector to Base (emitter open)	V_{CB}	15	volts
Current			
Collector	I_C	−20	ma
Power			
Collector Dissipation at 25°C*	P_{CM}	65	mw
Temperature			
Operating and Storage	T_A, T_{STG}	−55 to 85	°C

ELECTRICAL CHARACTERISTICS:** (25°C)

IF Amplifier Service			
Maximum Ratings			
Collector Supply Voltage	V_{CC}	9	volts
Design Center Characteristics ($I_E = 1$ ma; $V_{CE} = 5$v; f = 455 KC except as noted)			
Input Impedance	Z_i	700	ohms
Output Impedance	Z_o	7	K ohms
Voltage Feedback Ratio ($V_{CB} = 5$v; f = 1 mc)	h_{rb}	10	$\times 10^{-3}$
Collector to Base Capacitance ($V_{CB} = 5$v; f = 1 mc)	C_{ob}	2.4	$\mu\mu$f
Frequency Cutoff ($V_{CB} = 5$v)	f_{ab}	8	mc
Base Current Gain ($I_C = 1$ ma; $V_{CE} = 1$v)	h_{FE}	72	
Minimum Base Current Gain	h_{FE}	34	
IF Amplifier Performance			
Collector Supply Voltage	V_{CC}	5	volts
Collector Current	I_C	2	ma
Input Frequency	f	455	KC
Minimum Power Gain in Typical IF Circuit	G_e	24.5	db
Power Gain Range of Variation in Typical IF Circuit	G_e	2.5	db
Cutoff Characteristics			
Collector Cutoff Current ($V_{CB} = 5$v)	I_{CO}	.5	μa
Collector Cutoff Current ($V_{CB} = 15$v)	I_{CO}	5	μa max

*Derate 1.1 mw/°C increase in ambient temperature.
**All values are typical unless indicated as a min. or max.

2N450

Outline Drawing No. 7

The General Electric Type 2N450 is a germanium PNP alloy junction high frequency switching transistor intended for military, industrial and data processing applications where high reliability at the maximum ratings is of prime importance. As a special control in manufacture, all 2N450 transistors are subjected to a high pressure detergent test to enhance reliable hermetic seals and are also aged at a temperature of 100°C for 96 hours minimum.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CB}	–20	volts
Collector to Emitter	V_{CE}	–12	volts
Emitter to Base	V_{EB}	–10	volts
Current			
Collector	I_C	–125	ma
Power			
Dissipation	P_{AV}	150	mw
Temperature			
Storage	T_{STG}	–65 to 85	°C
Operating Junction	T_J	85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

D-C Characteristics		Min.	Max.	
D-C Base Current Gain				
(V_{CE} = –1v; I_C = –10 ma)	h_{FE}	30		
(V_{CE} = –1v; I_C = –100 ma)	h_{FE}	15		
Saturation Voltage (I_B = –.5 ma; I_C = –10 ma)	$V_{CE(SAT)}$		–.2	volts
Base Input Voltage (I_B = –.5 ma; I_C = –10 ma)	$V_{BE(SAT)}$		–.35	volts
Collector Breakdown Voltage (I_C = –100 μa)	BV_{CBO}	–20		volts
Emitter Breakdown Voltage (I_C = –100 μa)	BV_{EBO}	–10		volts
Collector to Emitter Breakdown Voltage (R_{BE} = 10K ohms; I_C = –600 μa)	BV_{CER}	–12		volts
Cutoff Characteristics				
Collector Current (V_{CB} = –12v)	I_{CO}		–6	μa
Emitter Current (V_{EB} = –6v)	I_{EO}		–6	μa
Punch-through Voltage	V_{PT}	–12		volts
High Frequency Characteristics (Common Base)				
(V_{CB} = –5v; I_E = 1 ma)				
Alpha-Cutoff Frequency	f_{ab}	5		mc
Collector Capacitance (f = 1 mc)	C_{ob}		20	μμf
Base Spreading Resistance	r'_b		200	ohms

Thermal Resistance

Derate 2.5 mw/°C for temperatures over 25°C

2N489–2N494

Outline Drawing No. 5

The General Electric Silicon Unijunction Transistor is a hermetically sealed three terminal device having a stable "N" type negative resistance charactistic over a wide temperature range. A high peak current rating makes this device useful in medium power switching and oscillator applications, where it can serve the purpose of two conventional silicon transistors. These transistors are hermetically sealed in a welded case. The case dimensions and lead configuration are suitable for insertion in printed boards by automatic assembly equipment. The Silicon Unijunction Transistor consists of an "N" type silicon bar mounted between two ohmic base contacts with a "P" type emitter near base-two. The device operates by conductivity modulation of the silicon between the emitter and base-one when the emitter is forward biased. In the cutoff, or standby condition, the emitter and interbase power supplies establish potentials between the base contacts, and at the emitter, such that the emitter is back biased. If the emitter potential is increased sufficiently to overcome this bias, holes (minority carriers) are injected into the silicon bar. These holes are swept towards base-one by the internal field in the bar. The increased charge concentration, due to these holes, decreases the resistance and hence decreases the internal voltage drop from the emitter to base-one. The emitter current then increases regeneratively until it is limited by the emitter power supply. The effect of this conductivity modulation is also noticed as an effective modulation of the interbase current.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Emitter Reverse	$T_J = 150°C$	60	volts
Interbase	V_{BB}	See Fig. 1	
Current			
RMS Emitter		70	ma
Peak Emitter*	$T_J = 150°C$	2	amps
Power			
AV Dissipation		450	mw**
AV Dissipation — Stabilized***		600	mw**
Temperature			
Operating		−65 to 150	°C
Storage		−65 to 175	°C

*Capacitor discharge —10 μfd or less.
**Derate 2 mw/°C increase in ambient temperature.
***Total power dissipation must be limited by external circuit.

Types 2N489-2N494 are specified primarily in three ranges of stand-off and two ranges of interbase resistance. Each range of stand-off ratio has limits of ±10% from the center value and each range of interbase resistance has limits of ±20% from the center value.

2N489, 2N490

MAJOR ELECTRICAL CHARACTERISTICS:		2N489 Min.	2N489 Nom.	2N489 Max.	2N490 Min.	2N490 Nom.	2N490 Max.	
Interbase Resistance at 25°C Junction Temperature	R_{BB_O}	4.7	5.6	6.8	6.2	7.5	9.1	kilohms
Intrinsic Stand-off Ratio	η	.51	.56	.62	.51	.56	.62	
Modulated Interbase Current ($I_E = 50$ ma; $V_{BB} = 10$v; $T_A = 25°C$)	$I_{B_2(MOD)}$	6.8	12	22	6.8	12	22	ma
Emitter Reverse Current (B1 open circuit)								
($V_{B_2E} = 60$v; $T_J = 25°C$)	I_{EO}		.03	12		.03	12	μa
($V_{B_2E} = 60$v; $T_J = 150°C$)	I_{EO}		1.8	20		1.8	20	μa
MINOR ELECTRICAL CHARACTERISTICS: (Typical Values)								
Emitter Saturation Voltage ($I_E = 50$ ma; $V_{BB} = 10$v; $T_A = 25°C$)	$V_{E(SAT)}$	2.3	3.1	3.8	2.4	3.3	4.2	volts
Peak Point Emitter Current ($V_{BB} = 25$v; $T_A = 25°C$)	I_P		4	12		4	12	μa
Valley Voltage	V_V	1.1	1.9	3.4	1.0	1.9	3.5	volts
Valley Current	I_V	12	19	35	11	19	31	ma
Maximum Frequency of Oscillation ($I_{B_2} = 4.5$ ma; Relaxation Oscillator)	f_{MAX}		0.9				0.7	mc

2N491, 2N492

MAJOR ELECTRICAL CHARACTERISTICS:		2N491 Min.	2N491 Nom.	2N491 Max.	2N492 Min.	2N492 Nom.	2N492 Max.	
Interbase Resistance at 25°C Junction Temperature	R_{BB_O}	4.7	5.6	6.8	6.2	7.5	9.1	kilohms
Intrinsic Stand-off Ratio	η	.56	.62	.68	.56	.62	.68	
Modulated Interbase Current ($I_E = 50$ ma; $V_{BB} = 10$v; $T_A = 25°C$)	I_{B_2}(MOD)	6.8	12	22	6.8	12	22	ma
Emitter Reverse Current (B1 open circuit) ($V_{B_2E} = 60$v; $T_J = 25°C$)	I_{EO}		.03	12		.03	12	μa
($V_{B_2E} = 60$v; $T_J = 150°C$)	I_{EO}		1.8	20		1.8	20	μa
MINOR ELECTRICAL CHARACTERISTICS: (Typical Values)								
Emitter Saturation Voltage ($I_E = 50$ ma; $V_{BB} = 10$v; $T_A = 25°C$)	V_E(SAT)	2.5	3.4	4.3	2.7	3.6	4.5	volts
Peak Point Emitter Current ($V_{BB} = 25$v; $T_A = 25°C$)	I_P		4	12		4	12	μa
Valley Voltage	V_V	1.2	2.2	3.9	1.2	2.2	3.9	volts
Valley Current	I_V	13	20	37	12	20	38	ma
Maximum Frequency of Oscillation ($I_{B_2} = 4.5$ ma; Relaxation Oscillator)	f_{MAX}		0.8			0.7		mc

2N493, 2N494

MAJOR ELECTRICAL CHARACTERISTICS:		2N493 Min.	2N493 Nom.	2N493 Max.	2N494 Min.	2N494 Nom.	2N494 Max.	
Interbase Resistance at 25°C Junction Temperature	R_{BB_O}	4.7	5.6	6.8	6.2	7.5	9.1	kilohms
Intrinsic Stand-off Ratio	η	.62	.68	.75	.62	.68	.75	
Modulated Interbase Current ($I_E = 50$ ma; $V_{BB} = 10$v; $T_A = 25°C$)	I_{B_2}(MOD)	6.8	12	22	6.8	12	22	ma
Emitter Reverse Current (B1 open circuit) ($V_{B_2E} = 60$v; $T_J = 25°C$)	I_{EO}		.03	12		.03	12	μa
($V_{B_2E} = 60$v; $T_J = 150°C$)	I_{EO}		1.8	20		1.8	20	μa
MINOR ELECTRICAL CHARACTERISTICS: (Typical Values)								
Emitter Saturation Voltage ($I_E = 50$ ma; $V_{BB} = 10$v; $T_A = 25°C$)	V_E(SAT)	2.8	3.8	4.6	3.0	3.9	4.8	volts
Peak Point Emitter Current ($V_{BB} = 25$v; $T_A = 25°C$)	I_P		4	12		4	12	μa
Valley Voltage	V_V	1.4	2.5	4.4	1.4	2.5	4.3	volts
Valley Current	I_V	14	24	40	12	21	35	ma
Maximum Frequency of Oscillation ($I_{B_2} = 4.5$ ma; Relaxation Oscillator)	f_{MAX}		0.7			0.65		mc

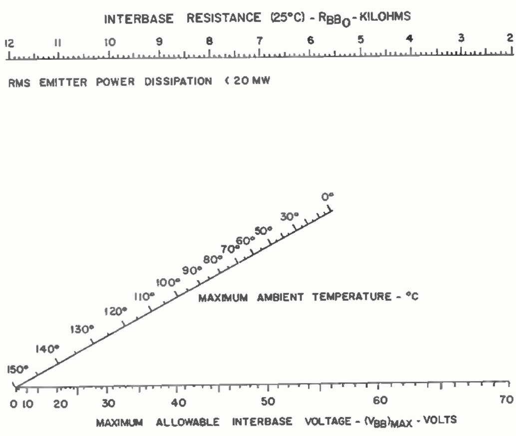


FIGURE 1

2N508

Outline Drawing No. 2

The 2N508 is an alloy junction PNP transistor intended for driver service in audio amplifiers. It is a miniaturized version of the 2N265 G.E. transistor. By control of transistor characteristics during manufacture, a specific power gain is provided for each type. Special processing techniques and the use of hermetic seals provides stability of these characteristics throughout life.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Emitter	V_{CE}	−16	volts
Collector to Base	V_{CB}	−16	volts
Current			
Collector	I_C	−100	ma
Power			
Collector Dissipation	P_{CM}	140	mw
Temperature			
Operating	T_A	−65 to 60	°C
Storage	T_{STG}	−65 to 85	°C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

D-C Characteristics			
Base Current Gain ($I_C = -20$ ma; $V_{CE} = -1$v)	h_{FE}	125	
Collector to Emitter Voltage ($R_{EB} = 10$K; $I_C = -.6$ ma)	V_{CER}	−16	volts
Collector Cutoff Current ($V_{CB} = -16$v)	I_{CO}	−10	μa
Maximum Collector Cutoff Current ($V_{CB} = -16$v)	I_{CO}	−16	μa
Small Signal Characteristics			
Frequency Cutoff ($V_{CB} = -5$v; $I_E = 1$ ma)	f_{ab}	3.5	mc
Collector Capacity ($V_{CB} = -5$v; $I_E = 1$ ma)	C_{ob}	24	μμf
Noise Figure ($V_{CB} = -5$v; $I_E = 1$ ma)	NF	6	db
Input Impedance ($V_{CE} = -5$v; $I_E = 1$ ma)	h_{ie}	3	K ohms
Current Gain ($V_{CE} = -5$v; $I_E = 1$ ma)	h_{fe}	112	
Thermal Characteristics			
Thermal Resistance Junction to Air		.25	°C/mw
Performance Data Common Emitter			
Power Gain Driver ($V_{CC} = -9$v)	G_e	45	db
Power Output	P_o	1	mw

2N524, 2N525

Outline Drawing No. 2

The General Electric types 2N524 and 2N525 are germanium PNP alloy junction transistors particularly recommended for low to medium power amplifier and switching application in the frequency range from audio to 100 KC. This series of transistors is intended for military, industrial and data processing applications where high reliability and extreme stability of characteristics are of prime importance. The 2N524 and 2N525 are equivalent to the 2N44 and 2N43 respectively and may be directly substituted in most applications.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CBO}	—45	volts
Collector to Emitter	V_{CER}	—30	volts
Emitter to Base	V_{EBO}	—15	volts
Current			
Collector	I_{CM}	—500	ma
Power			
Total Transistor Dissipation	P_{AV}	225	mw
Temperature			
Storage	T_{STG}	—65 to 100	°C
Operating	T_J	85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

Small Signal Characteristics

(Unless otherwise specified V_{CB} = —5v common base; I_E = 1 ma; f = 270 cps)

		2N524			2N525			
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Output Admittance (Input AC Open Circuited)	h_{ob}	.10	.65	1.3	.1	.6	1.2	μmhos
Input Impedance (Output AC Short Circuited)	h_{ib}	26	31	36	26	31	35	ohms
Reverse Voltage Transfer Ratio (Input AC Open Circuited)	h_{rb}	1	4.0	10	1	5.0	11	$\times 10^{-4}$
Forward Current Transfer Ratio (Common Emitter; Output AC Short Circuited)	h_{fe}	16	30	41	30	44	64	
Frequency Cutoff	f_{ab}	.8	2.0	5.0	1	2.5	5.5	mc
Output Capacity (f = 1 mc; Input AC open circuited)	C_{ob}	18	25	40	18	25	40	μμf
Noise Figure (f = 1 kc; BW = 1 cycle)	NF	1	6	15	1	6	15	db

D-C Characteristics

		2N524 Min.	2N524 Nom.	2N524 Max.	2N525 Min.	2N525 Nom.	2N525 Max.	
Forward Current Gain (Common Emitter, I_C/I_B) (V_{CE} = —1v; I_C = —20 ma)	h_{FE}	19	35	42	34	52	65	
(V_{CE} = —1v; I_C = —100 ma)	h_{FE}	13	31		30	45		
Collector Saturation Voltage (I_C = —20 ma;	$V_{CE(SAT)}$	45	70	110	50	75	110	mv
I_B as indicated)	@ I_B =	—2.0	—2.0	—2.0	—1.33	—1.33	—1.33	ma
Base Input Voltage, Common Emitter (V_{CE} = —1v; I_C = —20 ma)	V_{BE}	—.220	—.255	—.320	—.200	—.243	—.300	
Collector Cutoff Current (V_{CBO} = —30v)	I_{CO}		—5	—10		—5	—10	μa
Emitter Cutoff Current (V_{EBO} = —15v)	I_{EO}		—4	—10		—4	—10	μa
Collector to Emitter Voltage (R_{BE} = 10K ohms; I_C = —.6 ma)	V_{CER}	—30			—30			volts
Punch-through Voltage	V_{PT}	—30			—30			volts

Thermal Resistance (k)

Junction Temperature Rise/ Total Transistor Dissipation:

	2N524	2N525	
Free Air	.27	.27	°C/mw
Infinite Heat Sink	.11	.11	°C/mw
Clip-on Heat Sink in Free Air	.20	.20	°C/mw

2N526, 2N527

Outline Drawing No. 2

The General Electric types 2N526 and 2N527 are germanium PNP alloy junction transistors particularly recommended for low to medium power amplifier and switching application in the frequency range from audio to 100 KC. This series of transistors is intended for military, industrial and data processing applications where high reliability and extreme stability of characteristics are of prime importance.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CBO}	—45	volts
Collector to Emitter	V_{CER}	—30	volts
Emitter to Base	V_{EBO}	—15	volts
Current			
Collector	I_{CM}	—500	ma
Power			
Total Transistor Dissipation	P_{AV}	225	mw
Temperature			
Storage	T_{STG}	—65 to 100	°C
Operating	T_J	85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

Small Signal Characteristics

(Unless otherwise specified V_{CB} = —5V common base; I_E = 1 ma; f = 270 cps)

		2N526 Min.	2N526 Nom.	2N526 Max.	2N527 Min.	2N527 Nom.	2N527 Max.	
Output Admittance (Input AC Open Circuited)	h_{ob}	.1	.42	1.0	.1	.37	.9	µmhos
Input Impedance (Output AC Short Circuited)	h_{ib}	26	30	33	26	29	31	ohms
Reverse Voltage Transfer Ratio (Input AC Open Circuited)	h_{rb}	1	6.5	12	1	8.0	14	$\times 10^{-4}$
Forward Current Transfer Ratio (Common Emitter; Output AC Short Circuited)	h_{fe}	44	64	88	60	81	120	
Frequency Cutoff	f_{ab}	1.3	3.0	6.5	1.5	3.3	7	mc
Output Capacity (f = 1 mc; Input AC open circuited)	C_{ob}	18	25	40	18	25	40	µµf
Noise Figure (f = 1 kc; BW = 1 cycle)	NF	1	6	15	1	6	15	db

D-C Characteristics

		2N526 Min.	2N526 Nom.	2N526 Max.	2N527 Min.	2N527 Nom.	2N527 Max.	
Forward Current Gain (Common Emitter, I_C/I_B)								
(V_{CE} = —1v; I_C = —20 ma)	h_{FE}	53	73	90	72	91	121	
(V_{CE} = —1v; I_C = —100 ma)	h_{FE}	47	66		65	86		
Collector Saturation Voltage (I_C = —20 ma;	$V_{CE(SAT)}$	55	80	110	60	90	110	mv
I_B as indicated)	@ I_B =	—1.0	—1.0	—1.0	—.67	—.67	—.67	ma
Base Input Voltage, Common Emitter (V_{CE} = —1v; I_C = —20 ma)	V_{BE}	—.190	—.230	—.280	—.180	—.216	—.260	
Collector Cutoff Current (V_{CBO} = —30v)	I_{CO}		—5	—10		—5	—10	µa
Emitter Cutoff Current (V_{EBO} = —15v)	I_{EO}		—4	—10		—4	—10	µa
Collector to Emitter Voltage (R_{BE} = 10K ohms; I_C = —.6 ma)	V_{CER}	—30			—30			volts
Punch-through Voltage	V_{PT}	—30			—30			volts

Thermal Resistance (k)

	2N526	2N527	
Junction Temperature Rise/ Total Transistor Dissipation:			
Free Air	.27	.27	°C/mw
Infinite Heat Sink	.11	.11	°C/mw
Clip-on Heat Sink in Free Air	.20	.20	°C/mw

2N526

Outline Drawing No. 2

Also supplied as certified to meet MIL-T-19500/60

2N634

The General Electric type 2N634 is an NPN germanium alloy triode transistor designed for high speed switching applications.

Outline Drawing No. 2

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CB}	20	volts
Emitter to Base	V_{EB}	15	volts
Collector to Emitter	V_{CE}	20	volts
Current			
Collector	I_C	300	ma
Base	I_B	50	ma
Emitter	I_E	300	ma
Temperature			
Storage	T_{STG}	−65 to 85	°C
Operating Junction	T_A	85	°C
Power			
Dissipation	P_M	150	mw

ELECTRICAL CHARACTERISTICS: (25°C)

		Min.	Nom.	Max.	
Collector Voltage ($I_C = 15$ µamp; $I_E = 0$)	V_{CBO}	20			volts
Emitter Voltage ($I_E = 10$ µamp; $I_C = 0$)	V_{EBO}	15			volts
Collector to Emitter Voltage ($I_C = 600$ µamp; R = 10 K)	V_{CER}	20			volts
Collector Cutoff Current ($V_{CB} = 5$v; $I_E = 0$)	I_{CBO}			5	µamps
Punch Through Voltage	V_{PT}	20			volts
D-C Current Gain ($I_C = 200$ ma; $V_{CE} = 0.75$v)	h_{FE}	15			
Alpha Cutoff Frequency ($V_{CB} = 5$v; $I_E = -1$ ma)	f_{ab}	5	8		mc

Thermal Characteristic

Derate 2.5 mw/°C increase in ambient temperature over 25°C.

2N635

The General Electric type 2N635 is an NPN germanium alloy triode transistor designed for high speed switching applications.

Outline Drawing No. 2

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CB}	20	volts
Emitter to Base	V_{EB}	15	volts
Collector to Emitter	V_{CE}	20	volts
Current			
Collector	I_C	300	ma
Base	I_B	50	ma
Emitter	I_E	300	ma
Temperature			
Storage	T_{STG}	−65 to 85	°C
Operating Junction	T_A	85	°C
Power			
Dissipation	P_M	150	mw

ELECTRICAL CHARACTERISTICS: (25°C)

		Min.	Nom.	Max.	
Collector Voltage ($I_C = 15$ µamp; $I_E = 0$)	V_{CBO}	20			volts
Emitter Voltage ($I_E = 10$ µamp; $I_C = 0$)	V_{EBO}	15			volts
Collector to Emitter Voltage ($I_C = 600$ µamp; R = 10 K)	V_{CER}	20			volts
Collector Cutoff Current ($V_{CB} = 5$v; $I_E = 0$)	I_{CBO}			5	µamps
Punch Through Voltage	V_{PT}	20			volts
D-C Current Gain ($I_C = 200$ ma; $V_{CE} = 0.75$v)	h_{FE}	25			
Alpha Cutoff Frequency ($V_{CB} = 5$v; $I_E = -1$ ma)	f_{ab}	10	12		mc

Thermal Characteristic

Derate 2.5 mw/°C increase in ambient temperature over 25°C.

2N636

Outline Drawing No. 2

The General Electric type 2N636 is an NPN germanium alloy triode transistor designed for high speed switching applications.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CB}	20	volts
Emitter to Base	V_{EB}	15	volts
Collector to Emitter	V_{CE}	15	volts
Current			
Collector	I_C	300	ma
Base	I_B	50	ma
Emitter	I_E	300	ma
Temperature			
Storage	T_{STG}	−65 to 85	°C
Operating Junction	T_A	85	°C
Power			
Dissipation	P_M	150	mw

ELECTRICAL CHARACTERISTICS: (25°C)

		Min.	Nom.	Max.	
Collector Voltage ($I_C = 15$ μamp; $I_E = 0$)	V_{CBO}	20			volts
Emitter Voltage ($I_E = 10$ μamp; $I_C = 0$)	V_{EBO}	15			volts
Collector to Emitter Voltage ($I_C = 600$ μamp; R = 10 K)	V_{CER}	15			volts
Collector Cutoff Current ($V_{CB} = 5v$; $I_E = 0$)	I_{CBO}			5	μamps
Punch Through Voltage	V_{PT}	15			volts
D-C Current Gain ($I_C = 200$ ma; $V_{CE} = 0.75v$)	h_{FE}	35			
Alpha Cutoff Frequency ($V_{CB} = 5v$; $I_E = -1$ ma)	f_{ab}	15	17		mc

Thermal Characteristic

Derate 2.5 mw/°C increase in ambient temperature over 25°C.

2N1056

Outline Drawing No. 1

The General Electric Type 2N1056 is a germanium PNP alloy junction switching transistor, intended for military, industrial and data processing applications where high voltage, reliability and extreme stability of characteristics are of prime importance. Applications include neon indicator circuits, relay driver circuits and direct indicating counter circuits.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CB}	−70	volts
Collector to Emitter	V_{CE}	−50	volts
Emitter to Base	V_{EB}	−15	volts
Current			
Collector	I_C	−300	ma
Power			
RMS Total Transistor Dissipation	P_{AV}	240	mw
Temperature			
Storage	T_{STG}	−65 to 100	°C
Operating Junction	T_J	85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

D-C Characteristics		Min.	Design Center	Max.	
Collector to Emitter Voltage ($R_{BE} = 10$ K; $I_C = -600$ μamp)	V_{CER}	−50			volts
Punch Through Voltage ($V_{EBF} \leqq 1v$)	V_{PT}	−60			volts
Forward Current Transfer Ratio (low current) ($I_C = -20$ ma; $V_{CE} = -1v$)	h_{FE}	18	32	43	
Forward Current Transfer Ratio (high current) ($I_C = -100$ ma; $V_{CE} = -1v$)	h_{FE}	13	25		
Base Input Voltage (for low current condition) ($I_C = -20$ ma; $V_{CE} = -1v$)	V_{BE}		−240	−300	mv
Saturation Voltage (low level) ($I_B = -2.0$ ma; $I_C = -20$ ma)	$V_{CE(SAT)}$		−90	−130	mv

Cutoff Characteristics					
Collector Current ($I_E = 0$; $V_{CB} = -70$)	I_{CO}			−25	μamps
Emitter Current ($I_C = 0$; $V_{EB} = -15$)	I_{EO}			−16	μamps
Low Frequency Characteristics (Common Base or Common Emitter)					
($V_{CB} = -5v$; $I_E = 1$ ma; f = 1 KC)					
($V_{CE} = -5v$; $I_C = -1$ ma; f = 1 KC)					
Forward Current Transfer Ratio	h_{fe}		25		
Output Admittance	h_{ob}	0.1	0.9	1.5	μmho
Input Impedance	h_{ib}	27	31	38	ohms
Reverse Voltage Transfer Ratio	h_{rb}	1.0	4.0	13	$\times 10^{-4}$
Noise Figure (Bw = 100 cycles) (Common Emitter)	NF			20	db
High Frequency Characteristics (Common Base)					
($V_{CB} = -5v$; $I_E = 1$ ma; f = 1 mc)					
Output Capacity	C_{ob}	20	40	60	μμf
Cutoff Frequency	f_{ab}	0.5	1.0	3.0	mc
Thermal Characteristics					
Thermal Resistance from Junction to Mounting Base				.11	°C/mw
Free Air Thermal Resistance				.25	°C/mw

2N1057

Outline Drawing No. 1

The General Electric Type 2N1057 is a germanium PNP alloy junction switching transistor intended for low to medium power switching applications at low frequencies. A hermetic enclosure is provided by the use of glass-to-metal seals and welded seams.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CB}	−45	volts
Collector to Emitter	V_{CE}	−30	volts
Emitter to Base	V_{EB}	−5	volts
Current			
Collector	I_C	−300	ma
Power			
RMS Total Transistor Dissipation	P_{AV}	240	mw
Temperature			
Storage	T_{STG}	−65 to 100	°C
Operating Junction	T_J	85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

		Min.	Design Center	Max.	
D-C Characteristics					
Collector to Emitter Breakdown Voltage ($R_{BE} = 10$ K; $I_C = -600$ μamp)	BV_{CER}	−30			volts
Punch Through Voltage ($V_{EBF} \leq -1v$)	V_{PT}	−45			volts
Forward Current Transfer Ratio (low current) ($I_C = -20$ ma; $V_{CE} = -1v$)	h_{FE}	34	58	90	
Forward Current Transfer Ratio (high current) ($I_C = -100$ ma; $V_{CE} = -1v$)	h_{FE}	30	52		
Base Input Voltage (for low current condition) ($I_C = -20$ ma; $V_{CE} = -1v$)	V_{BE}		−230	−280	mv
Saturation Voltage (low level) ($I_B = -1.33$ ma; $I_C = -20$ ma)	$V_{CE(SAT)}$	−60	−80	−130	mv
Cutoff Characteristics					
Collector Current ($I_E = 0$; $V_{CB} = -45v$)	I_{CO}			−16	μamps
Emitter Current ($I_C = 0$; $V_{EB} = -5v$)	I_{EO}			−10	μamps
High Frequency Characteristics (Common Base)					
($V_{CB} = -5v$; $I_E = 1$ ma; f = 1 mc)					
Output Capacity	C_{ob}	20	40	60	μμf
Cutoff Frequency	f_{ab}	.5		3.0	mc
Thermal Characteristics					
Thermal Resistance from Junction to Mounting Base				.11	mw
Free Air Thermal Resistance				.25	°C mw

2N1086, 2N1086A, 2N1087

Outline Drawing No. 3

The General Electric Types 2N1086, 2N1086A, and 2N1087 are NPN rate grown germanium transistors intended for mixer/oscillator or autodyne converters in radio broadcast receivers. Special manufacturing techniques provide a low value and a narrow spread in collector capacity. Minimum conversion gain and narrow conversion gain spreads are guaranteed.

CONVERTER TRANSISTOR SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)		2N1086	2N1086A	2N1087	
Voltage					
Collector to Emitter (base open)	V_{CE}	9	9	9	volts
Collector to Base (emitter open)	V_{CB}	9	9	9	volts
Current					
Collector	I_C	—20	—20	—20	ma
Power					
Collector Dissipation at 25°C*	P_C	65	65	65	mw
Temperature					
Operating and Storage	T_S	—55 to 85	—55 to 85	—55 to 85	°C
ELECTRICAL CHARACTERISTICS:**					
Converter Service					
Maximum Ratings					
Collector Supply Voltage	V_{CC}	9	9	9	volts
Design Center Characteristics					
Input Impedance (I_E = 1 ma; V_{CE} = 5v; f = 455 KC)	Z_i	350	350	350	ohms
Output Impedance (I_E = 1 ma; V_{CE} = 5v; f = 455 KC)	Z_o	15	15	15	K ohms
Voltage Feedback Ratio (I_E = 1 ma; V_{CB} = 5v; f = 1 mc)	h_{rb}	5	5	5	$\times 10^{-3}$
Collector Capacitance (I_E = 1 ma; V_{CB} = 5v; f = 1 mc)	C_{ob}	2.4	2.4	2.4	μμf
Frequency Cutoff (I_E = 1 ma; V_{CB} = 5v)	f_{ab}	8	8	8	mc
Base Current Gain (I_C = 1 ma; V_{CE} = 1v)	h_{FE}	40	40	40	
Minimum Base Current Gain	h_{FE}	17	17	17	
Maximum Base Current Gain	h_{FE}	195	195	195	
Converter Performance					
Conversion Gain in Typical Converter Test Circuit	CG_e	24	24	26	db
Conversion Gain Range of Variation in Typical Converter Circuit		4	2	2	db
Cutoff Characteristics					
Collector Cutoff Current (V_{CB} = 5v)	I_{CO}	3	3	3	μa max.
Collector Cutoff Current (V_{CB} = 5v)	I_{CO}	.5	.5	.5	μa

*Derate 1.1 mw/°C increase in ambient temperature over 25°C.
**All values are typical unless indicated as a min. or max.

2N1097, 2N1098

Outline Drawing No. 2

The General Electric Types 2N1097 and 2N1098 are alloy junction PNP transistors intended for low power output and audio driver service in entertainment equipment. These types are similar to the General Electric Types 2N322 and 2N323 except for h_{FE} limits.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)			
Voltage			
Collector to Emitter	V_{CER}	—16	volts
Collector to Base	V_{CBO}	—16	volts

Current				
Collector	I_C		−100	ma
Temperature				
Storage	T_{STG}		−65 to 85	°C
Operating Junction	T_J		60	°C
Power				
Transistor Dissipation*	P_{AV}		140	mw

ELECTRICAL CHARACTERISTICS: (25°C)

D-C Characteristics		2N1097	2N1098	
Collector Current (V_{CB} = −16v)	I_{CBO}	−16	−16	μa max.
Forward Current Transfer Ratio (I_C = 20 ma; V_{CE} = 1v)	h_{FE}	34-90	25-90	
Low Frequency Characteristics (V_C = −5v; I_E = −1 ma; f = 1 KC)				
Output Capacity (Typical)	C_{ob}	25	25	μμf
Forward Current Transfer Ratio (Typical)	h_{fe}	55	45	

*Derate 4 mw/°C increase in ambient temperature over 25°C.

2N1115

Outline Drawing No. 7

The 2N1115 transistor is a germanium PNP switching type intended for highly reliable service in missile and other military equipment.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CBO}	−20	volts
Collector to Emitter	V_{CEO}	−15	volts
Emitter to Base	V_{EBO}	−10	volts
Current			
Collector	I_C	−125	ma
Emitter	I_E	−125	ma
Peak Collector*	I_C	−500	ma
Peak Base*	I_B	−500	ma
Temperature			
Storage	T_{STG}	−65 to 85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

DC Characteristics		Min.	Max.	
Base Input Voltage (for low current condition) (I_B = −0.25 ma; I_C = −10 ma)	V_{BE}		−0.4	volts
Base Input Voltage (for high current condition) (I_B = −1.7 ma; I_C = −60 ma)	V_{BE}		−0.5	volts
Saturation Voltage (low level) (I_B = −0.25 ma; I_C = −10 ma)	$V_{CE(SAT)}$		−0.15	volts
Saturation Voltage (high current) (I_B = −1.7 ma; I_C = −60 ma)	$V_{CE(SAT)}$		−0.35	volts
Cutoff Characteristics				
Emitter Current(V_{EB} = −10)	I_{EO}		−6	μa
Collector to Emitter Current (V_{CE} = −20; R_{BE} = 10K; V_B = 3)	I_{CEX}		−6	μa
High Frequency Characteristics (Common Base) (V_{CB} = −5v; I_E = 1 ma)				
Alpha Cutoff Frequency	f_{ab}	5.0		mcs
Collector Capacity (f = 1 ma)	C_{ob}		20	μμf
Switching Characteristics				
Storage Time	t_s		3.0	μsec

Thermal Characteristics

Derate 2.5 mw°/C for temperatures above 25°C

*Duration of intermittent current peaks is limited by the thermal transient response of the transistor.

2N1121

Outline Drawing No. 3

The General Electric Type 2N1121 transistor is a rate-grown NPN germanium device, intended for use as IF amplifiers in broadcast radio receivers. The collector capacity is controlled to a uniformly low value so that neutralization in most circuits is not required. Power gain at 455KC in a typical receiver circuit is restricted to a 2.5db spread. The uniformity provided by the controls of collector capacity and power gain allows easy and economical incorporation of this type into receiver circuits. Type 2N1121 has special high beta characteristics required in the final stage of reflex IF circuits where large audio gain is desired.

IF TRANSISTOR SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)			
Voltage			
Collector to Emitter (base open)	V_{CE}	15	volts
Collector to Base (emitter open)	V_{CB}	15	volts
Current			
Collector	I_C	—20	ma
Power			
Collector Dissipation at 25°C*	P_{CM}	65	mw
Temperature			
Operating and Storage	T_A, T_{STG}	—55 to 85	°C
ELECTRICAL CHARACTERISTICS: (25°C)**			
IF Amplifier Service			
Maximum Ratings			
Collector Supply Voltage	V_{CC}	9	volts
Design Center Characteristics			
($I_E = 1$ ma; $V_{CE} = 5$v; f = 455 KC except as noted)			
Input Impedance	Z_i	700	ohms
Output Impedance	Z_o	7	K ohms
Voltage Feedback Ratio (V_{CB} = 5v; f = 1 mc)	h_{rb}	10	$\times 10^{-8}$
Collector to Base Capacitance (V_{CB} = 5v; f = 1 mc)	C_{ob}	2.4	$\mu\mu$f
Frequency Cutoff (V_{CB} = 5v)	f_{ab}	8	mc
Base Current Gain (I_C = 1 ma; V_{CE} = 1v)	h_{FE}	72	
Minimum Base Current Gain	h_{FE}	34	
IF Amplifier Performance			
Collector Supply Voltage	V_{CC}	5	volts
Collector Current	I_C	2	ma
Input Frequency	f	455	KC
Minimum Power Gain in Typical IF Circuit	G_e	29.5	db
Power Gain Range of Variation in Typical IF Circuit	G_e	2.5	db
Cutoff Characteristics			
Collector Cutoff Current (V_{CB} = 5v)	I_{CO}	.5	μa
Collector Cutoff Current (V_{CB} = 15v)	I_{CO}	5	μa max

*Derate 1.1 mw/°C increase in ambient temperature.
**All values are typical unless indicated as a min. or max.

2N1144, 2N1145

Outline Drawing No. 1

The General Electric Types 2N1144 and 2N1145 are alloy junction PNP transistors intended for low power output and audio driver service in entertainment equipment. These types are similar to General Electric Types 2N1097 and 2N1098 except for package configuration.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)			
Voltage			
Collector to Emitter	V_{CER}	—16	volts
Collector to Base	V_{CBO}	—16	volts
Current			
Collector	I_{CM}	—100	ma
Temperature			
Storage	T_{STG}	—65 to 85	°C
Operating Junction	T_J	60	°C
Power			
Transistor Dissipation*	P_{AV}	140	mw

ELECTRICAL CHARACTERISTICS: (25°C)

D-C Characteristics		**2N1144**	**2N1145**	
Collector Current ($V_{CB} = -16v$)	I_{CBO}	−16	−16	μa max.
Forward Current Transfer Ratio ($I_C = 20$ ma; $V_{CE} = 1v$)	h_{FE}	34-90	25-90	
Low Frequency Characteristics ($V_C = -5v$; $I_E = 1$ ma; f = 1 KC)				
Output Capacity (Typical)	C_{ob}	40	40	μμf
Forward Current Transfer Ratio (Typical)	h_{fe}	55	42	

*Derate 4 mw/°C increase in ambient temperature over 25°C.

2N1198

Outline Drawing No. 3

The General Electric Type 2N1198 is an NPN germanium high frequency, high speed switching transistor intended for industrial and military applications where reliability is of prime importance. In order to achieve the high degree of reliability necessary in industrial and military applications, the 2N1198 is designed to pass 500G 1 millisecond drop shock, 10,000G centrifuge, 10G variable frequency vibration, as well as temperature cycling, moisture resistance and operating and storage life tests as outlined in MIL-T-19500A. The 2N1198 has the same low collector cutoff current and reliability as the 2N167 and is identical to the 2N167 on all parameters except voltage.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base	V_{CBO}	25	volts
Collector to Emitter	V_{CEO}	25	volts
Emitter to Base	V_{EB}	5	volts
Current			
Collector	I_C	75	ma
Emitter	I_E	−75	ma
Power			
Collector Dissipation (25°C)*	P_C	65	mw
Total Transistor Dissipation (25°C)**	P_M	75	mw
Temperature			
Storage	T_{STG}	85	°C

ELECTRICAL CHARACTERISTICS: (25°C)

D-C Characteristics		**Min.**	**Design Center**	**Max.**	
Collector to Emitter Breakdown Voltage (Base Open, $I_C = .3$ ma)	BV_{CEO}	25			volts
Forward Current Transfer Ratio ($I_C = 8$ ma; $V_{CE} = 1v$)	h_{FE}	17	30	90	
Base Input Voltage ($I_B = .47$ ma; $I_C = 8$ ma)	V_{BE}	.3***	.41	.6***	volts
Saturation Voltage ($I_B = .8$ ma; $I_C = 8$ ma)	$V_{CE(SAT)}$		.35		
Cutoff Characteristics					
Collector Current ($I_E = 0$; $V_{CB} = 15v$)	I_{CO}		.6	1.5	μa
Emitter Current ($I_C = 0$; $V_{EB} = 5v$)	I_{EO}		.35	5	μa
High Frequency Characteristics (Common Base) ($V_{CB} = 5v$; $I_E = 1$ ma)					
Alpha Cutoff Frequency	f_{ab}	5.0	9.0		mc
Collector Capacity (f = 1 mc)	C_{ob}		2.5	6	μμf
Voltage Feedback Ratio (f = 1 mc)	h_{rb}		7.3		$\times 10^{-3}$
Low Frequency Characteristics (Common Base) ($V_{CB} = 5v$; $I_E = 1$ ma; f = 270 cps)					
Forward Current Transfer Ratio	h_{fb}	.952	.985	.995	
Output Admittance	h_{ob}	.1***	.2	.7***	μmhos
Input Impedance	h_{ib}	25***		82***	ohms
Reverse Voltage Transfer Ratio	h_{rb}		1.5		$\times 10^{-4}$
Switching Characteristics ($I_C = 8$ ma; $I_{B1} = .8$ ma; $I_{B2} = .8$ ma)					
Turn-on Time	t_o		.4		μsec
Storage Time	t_s		.7		μsec
Fall Time	t_f		.2		μsec

*Derate 1.1 mw/°C increase in ambient temperature.
**Derate 1.25 mw/°C increase in ambient temperature.
***These limits are design limits within which 98% of production normally falls.

3N36

Outline Drawing No. 6

The General Electric Type 3N36 is a germanium meltback NPN transistor designed for high frequency use as an amplifier, oscillator or mixer. It is recommended for use in the frequency range from 30mc to 100mc. The 3N36 is excellent for wide band video amplifiers from low frequency to 10mc. All units are subjected to a rigorous mechanical drop test to control mechanical reliability. These transistors are hermetically sealed in welded cases. The case dimensions conform to the JEDEC TO-12 package and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base 1 or Base 2	V_{CB}	7	volts
Emitter to Base 1 or Base 2	V_{EB}	2	volts
Collector to Emitter	V_{CE}	6	volts
Current			
Collector	I_C	20	ma
Emitter	I_E	–20	ma
Base 2	I_{B_2}	2	ma
Power			
Total Transistor Dissipation	P_M	30	mw
Temperature			
Storage	T_{STG}	–65 to 85	°C
Operating Junction	T_J	85	°C

ELECTRICAL CHARACTERISTICS: (25°C)
(Unless otherwise specified $V_{CB_1} = +5v$; $I_E = -1.5$ ma; $V_{B_2B_1} = -2v$; f = 60 mc)

Small Signal High Frequency Parameters		Min.	Design Center	Max.	
Output Capacity	C_{ob}		2	3	μμf
Noise Figure (Common Base)	NF		11		db
Base Spreading Resistance	r'_b		50		ohms
Common Emitter "h" Parameters					
Input Impedance	h_{ie}		100 – j27		ohms
Reverse Voltage Transfer Ratio	h_{re}		.022 ∠ 47°		
Current Transfer Ratio	h_{fe}		2.2 ∠ –81°		
Output Admittance	h_{oe}		8 + j8.8		$\times 10^{-4}$ mhos
Common Base Cutoff Frequency	f_{ab}	50			mc
Common Emitter Power Gain	G_e	10	11.5		db
D-C Characteristics					
Voltage Collector to Emitter (R_{BE} = 10K; $V_{B_2E} = -2v$; I_C = 25 μamp)	V_{CER}	5			volts
Collector Cutoff Current ($V_{CB_1B_2}$ = 7v)	I_{CO}		3	10	μamps
Cross Base Resistance	$R_{B_1B_2}$	2.4	4	10	K ohms

Thermal Characteristic

Derate .5 mw/°C increase in ambient temperature over 25°C.

3N37

Outline Drawing No. 6

The General Electric Type 3N37 is a germanium meltback NPN transistor designed for high frequency use as an amplifier, oscillator or mixer. It is recommended for use in the frequency range of 100mc to 200mc. The 3N37 is excellent for wide band video amplifiers from low frequency to 10mc. All units are subjected to a rigorous mechanical drop test to control mechanical reliability. These transistors are hermetically sealed in welded cases. The case dimensions conform to the JEDEC TO-12 package and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage			
Collector to Base 1 or Base 2	V_{CB}	7	volts
Emitter to Base 1 or Base 2	V_{EB}	2	volts
Collector to Emitter	V_{CE}	6	volts
Current			
Collector	I_C	20	ma
Emitter	I_E	—20	ma
Base 2	I_{B_2}	2	ma
Power			
Total Transistor Dissipation	P_M	30	mw
Temperature			
Storage	T_{STG}	—65 to 85	°C
Operating Junction	T_J	85	°C

ELECTRICAL CHARACTERISTICS: (25°C)
(Unless otherwise specified $V_{CB_1} = +5v$; $I_E = -1.5$ ma; $V_{B_2B_1} = -2v$; f = 150 mc)

Small Signal High Frequency Parameters		Min.	Design Center	Max.	
Output Capacity	C_{ob}		1.5	3	μμf
Noise Figure (Common Base)	NF		11		db
Base Spreading Resistance	r'_b		50		ohms
Common Emitter "h" Parameters					
Input Impedance	h_{ie}		80 — j10		ohms
Reverse Voltage Transfer Ratio	h_{re}		.018 ∠ 84°		
Current Transfer Ratio	h_{fe}		1.1 ∠ —100°		
Output Admittance	h_{oe}		5.5 + j12.514		$\times 10^{-4}$ mhos
Common Base Cutoff Frequency	f_{ab}	90			mc
Common Emitter Power Gain	G_e	7	9		db
D-C Characteristics					
Voltage Collector to Emitter (R_{BE} = 10K; $V_{B_2E} = -2v$; $I_C = 25$ μamp)	V_{CER}	5			volts
Collector Cutoff Current ($V_{CB_1B_2} = 7v$)	I_{CO}		3	10	μamps
Cross Base Resistance	$R_{B_1B_2}$	2.5	4	10	K ohms

Thermal Characteristic

Derate .5mw/°C increase in ambient temperature over 25°C.

REGISTERED JEDEC TRANSISTOR TYPES — JUNE 1, 1959

For explanation of abbreviations, see page 218

					MAXIMUM RATINGS				ELECTRICAL PARAMETERS						
JEDEC No.	Type	Mfr.	Use	Dwg. No.	P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{ab} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE
2N22	Pt	WE	Sw		120	−100	−20	55	1.9α						
2N23	Pt	WE	Sw		80	−50	−40	55	1.9α						
2N24	Pt	WE	AF		120	−30	−25	50	2.2α						
2N25	Pt	WE	AF		200	−50	−30	60	2.5α						
2N26	Pt	WE	Sw		90	−30	−40	55							
2N27	NPN	WE	Obsolete	A	50	35*	100	85	100		1				
2N28	NPN	WE	AF	A	50	30*	100	85	100		.5				
2N29	NPN	WE	AF	A	50	35*	30	85	100		1		15	30	
2N30	Pt	GE	Obsolete		100	30	7	40	2.2α		2T	17T			Old G11
2N31	Pt	GE	Obsolete		100	30	7	40	2.2α		2T		150	25	Old G11A
2N32	Pt	RCA	Obsolete		50	−40	−8	40	2.2α		2.7	21T			
2N32A	Pt	RCA	Obsolete		50	−40	−8	40	2.2α		2.7	21T			
2N33	Pt	RCA	Obsolete		30	−8.5	−7	40							
2N34	PNP	RCA	Obsolete		50	−25	−8	50	40		.6	40T			2N190
2N34A	PNP	RCA	Obsolete		50	−25	−8	50	40		.6	40T			2N190
2N35	NPN	RCA	IF		50	25	8	50	40		.8	40T			2N169
2N36	PNP	CBS	AF	B	50	−20	−8	50	45T			40T			2N191
2N37	PNP	CBS	AF	B	50	−20	−8	50	30T			36T			2N190
2N38	PNP	CBS	AF	B	50	−20	−8	50	15T			32T			2N189
2N38A	PNP	CBS	AF	B	50	−20	−8	50	18T			34	−12	−3	2N189
2N41	PNP	RCA	AF	C	50	−25	−15	50	40T			40T	−10	−12	2N190
2N43	PNP	GE	AF	1	240	−30	−300	100	30	1	.5		−16	−45	2N43
2N44	PNP	GE	AF	1	240	−30	−300	100	25T	1	.5		−16	−45	2N44
2N45	PNP	GE	Obsolete		155	−25	−10	100	25T		.5	34	−16	−45	2N1056
2N46	PNP	RCA	AF	C	50	−25	−15	50	40T			4T	−10	−12	2N322
2N47	PNP	Phil	AF	D	50	−35*	−20	65	.975α				−5	−12	2N322 16V
2N48	PNP	Phil	AF	D	50	−35*	−20	65	.970α				−5	−12	2N321 16V
2N49	PNP	Phil	AF	D	50	−35*	−20	65	.975				−5	−12	2N322 16V
2N50	Pt	Cle	Sw		50	−15	−1	50	2α		3T				
2N51	Pt	Cle	Sw		100	−50	−8	50	2.2α				−350	−7	
2N52	Pt	Cle	RF		120	−50	−8	50							
2N54	PNP	W	AF		200	−45	−10	60	.95α			40T			2N1098 16V
2N55	PNP	W	AF		200	−45	−10	60	.92α			39T			2N1047 16V
2N56	PNP	W	AF		200	−45	−10	60	.90α			38T			2N322 16V
2N59	PNP	W	AF Out	C	180	−25*	−200	85	90T*	−100		35T	−15	−20	2N321
2N59A	PNP	W	AF Out	C	180	−40*	−200	85	90T*	−100		35T	−15	−20	2N321
2N59B	PNP	W	AF Out	C	180	−50*	−200	85	90T*	−100		35T	−15	−20	
2N59C	PNP	W	AF Out	C	180	−60*	−200	85	90T*	−100		35T	−15	−20	
2N60	PNP	W	AF Out	C	180	−25*	−200	85	65T*	−100		35T	−15	−20	2N321

JEDEC No.	Type	Mfr.	Use	Dwg. No.	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{ab} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE
2N60A	PNP	W	AF Out	C	180	−40*	−200	85	65T*	−100		35T	−15	−20	2N321
2N60B	PNP	W	AF Out	C	180	−50*	−200	85	65T*	−100		35T	−15	−20	
2N60C	PNP	W	AF Out	C	180	−60*	−200	85	65T*	100		35T	−15	−20	
2N61	PNP	W	AF Out	C	180	−25*	−200	85	45T*	100		35T	−15	−20	2N320
2N61A	PNP	W	AF Out	C	180	−40*	−200	85	45T*	100		35T	−15	−20	2N320
2N61B	PNP	W	AF Out	C	180	−50*	−200	85	45T*	100		35T	−15	−20	
2N61C	PNP	W	AF Out	C	180	−60*	−200	85	45T*	100		35T	−15	−20	
2N62	PNP	Phil	Obsolete	D	50	−35*	−20		.975αT						
2N63	PNP	Ray	AF	A	100	−22	−10	85	22T	1		39T	−6	−6	2N107
2N64	PNP	Ray	AF	A	100	−15	−10	85	45T	1		41T	−6	−6	2N322
2N65	PNP	Ray	AF	A	100	−12	−10	85	90T	1		92T	−6	−6	2N323
2N66	PNP	WE	Obsolete		1W	−40	.8A	80			.2		−300	−40	
2N67	PNP	Syl	Pwr	A	2W	−25*	−1.5A	70				23T			
2N71	PNP	W	Pwr		1W	−50	−250	60			.25	20			
2N72	Pt	RCA	Obsolete		50	−40	−20	55			2.5				
2N73	PNP	W	Sw		200	−50									2N1056
2N74	PNP	W	Sw		200	−50									2N1056
2N75	PNP	W	Sw		200	−20									2N1056
2N76	PNP	GE	Obsolete		50	−20*	−10	60	.90α		1.0	34	−10	−20	2N188
2N77	PNP	RCA	AF	C		−25*	−15	85	55		.70	44T	−10	−12	2N324
2N78	NPN	GE	RF/IF	3	65	15	20	85	45*	1	5	27	3	15	2N78
2N79	PNP	RCA	AF	C	35	−30	−50		46		.7	44			2N191
2N80	PNP	CBS	AF	B	50	−25	−8	100	80T				−30	−10	2N508
2N81	PNP	GE	Obsolete		50	−20	−15	100	20	1			−16	−30	Use 2N1098
2N82	PNP	CBS	AF		35 at 71° C	−20	−15	100	20	1			−16	−30	2N1098
2N94	NPN	Syl	RF	A	30	20	5	75	40T	.5	3T	25T	3	10	2N634
2N94A	NPN	Syl	RF	A	30	20	5	75	40T	.5	6T	25T	3	10	2N634
2N95	NPN	Syl	Pwr	A	2.5W	25*	1.5	70	40		.4T	23T			
2N96	PNP	RCA	Obsolete		50	−30	−20	55	35		.5				
2N97	NPN	GP	IF	A	50	30	10	75	.85α		.5	38T	10	4.5	2N169 15V
2N97A	NPN	GP	IF	A	50	40	10	85	.85α		.5	38T	5	30	2N169A 25V
2N98	NPN	GP	IF	A	50	40	10	75	.95α		.8	47T	10	4.5	2N169A 25V
2N98A	NPN	GP	IF	A	50	40	10	85	.96α		.8	47T	10	4.5	2N169A 25V
2N99	NPN	GP	IF	A	50	40	10	75	.95α		2.0	47T	10	4.5	2N169A 25V
2N100	NPN	GP	IF	A	25	25	5	50	.99α		2.5	53T	10	4.5	2N170 6V
2N101	PNP	Syl	Pwr	A	1W	−25*	−1.5	70				23T			
2N102	NPN	Syl	Pwr	A	1W	25*	1.5	70				23T			
2N103	NPN	GP	IF	A	50	35	10	75	.60α		.75T	33T	50	35	2N170 6V
2N104	PNP	RCA	AF	A	150	−30	−50	85	44		.7	33T	−10	−12	2N190
2N105	PNP	RCA	AF	C	35	−25	−15	85	55	.7	.75	42	−5	−12	2N191
2N106	PNP	Ray	AF	A	100	−6	−10	85	25		.8	28	−12	−6	2N1097
2N107	PNP	GE	AF	1	50	−6	−10	60	20		.6		−10	−12	2N107

					MAXIMUM RATINGS				ELECTRICAL PARAMETERS						
JEDEC No.	Type	Mfr.	Use	Dwg. No.	P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{ab} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE
2N108	PNP	CBS	AF Out	B	50	-20	-15								2N322
2N109	PNP	RCA	AF	A	150	-25	-70	85	75*			30T			2N320
2N110	Pt	WE	Sw	A	200	-50*	-50	85	32		1.5				
2N111	PNP	Ray	IF	A	150	-15	200	85	15		3T	33T	-5	-12	2N450
2N111A	PNP	Ray	IF	A	150	-15	-200	85	15		3T	33T	-5	-12	2N450
2N112	PNP	Ray	IF	A	150	-15	-200	85	15		5T	35T	-5	-12	2N450
2N112A	PNP	Ray	IF	A	150	-15	-200	85	15		5T	35T	-5	-12	2N450
2N113	PNP	Ray	RF	A	100	-6	-5	85	45T		10T	33T			2N450
2N114	PNP	Ray	RF Sw	A	100	-6	-5	85	65T		20T				2N450
2N115	PNP	Am	Pwr			-32	1.5A	90	45	.3A	.2T		.1 ma	-14	
2N117	NPN	TI	Si (=903)	A	150	30*	25	150	.90α	1	1		10	30	2N332
2N118	NPN	TI	Si (=904)	A	150	30*	25	150	.95α	1	2		10	30	2N333
2N119	NPN	TI	Si AF	A	150	30*	25	150	.974α	1	2		10	30	2N335
2N120	NPN	TI	Si AF	A	150	45*	25	175	.987α	1	7T		2	30	
2N123	PNP	GE	Sw	7	150	-15	-125	85	30*	-10	5		-6	-20	2N123
2N124	NPN	TI	Sw	A	50	10*	8	75	12*	5	3		2	5	2N293
2N125	NPN	TI	Sw	A	50	10*	8	75	24*	5	5		2	5	2N167
2N126	NPN	TI	Sw	A	50	10*	8	75	48*	5	5		2	5	2N167
2N127	NPN	TI	Sw	A	50	10*	8	75	100*	5	5		2	5	2N167
2N128	PNP	Phil	SB Osc	D	30	-4.5	-5	85	.95	.5	45 f_{max}		-3	-5	
2N129	PNP	Phil	SB RF	D	30	-4.5	-5	85	.92	.5	30 f_{max}		-3	-5	
2N130	PNP	Ray	AF	B	85	-22	-10	85	22T			39T			2N319
2N130A	PNP	Ray	AF	B	100	-40	-100	85	14	1	.7T	40T	-15	-20	2N319
2N131	PNP	Ray	AF	B	85	-15	-10	85	45T			41T			2N319
2N131A	PNP	Ray	AF	B	100	-30	-100	85	27	1	.8T	42T	-15	-20	2N319
2N132	PNP	Ray	AF	B	85	-12	-10	85	90T			42T			2N321
2N132A	PNP	Ray	AF	B	100	-20	-100	85	56	1	1T	44T	-15	-20	2N321
2N133	PNP	Ray	AF	B	85	-15	-10	85	25			36T	-12	-15	2N320
2N133A	PNP	Ray	AF	B	100	-20	-100	85	50T	1	.8T	38T	-15	-20	2N320
2N135	PNP	GE	RF/IF	7	100	-12	-50	85	20T		4.5T	29T			2N135
2N136	PNP	GE	RF/IF	7	100	-12	-50	85	40T		6.5T	31T			2N136
2N137	PNP	GE	RF/IF	7	100	-6	-50	85	60T		10T	33T			2N137
2N138	PNP	Ray	AF Out	B	50	-12	-20	50	140T			30T			2N508
2N138A	PNP	Ray	AF Out	B	150	-30	-100	85				29T			
2N138B	PNP	Ray	AF Out	B	100	-30	-100	85				29T			
2N139	PNP	RCA	IF	A	80	-16	-15	85	48	1	6.8	30	-6	-12	2N450
2N140	PNP	RCA	Osc	A	35	-16	-15	85	45	.4	7	27	-6	-12	2N450
2N141	PNP	Syl	Pwr		4W	-30	-.8A	65	.975αT	50	.4T	18T	-100	-20	
2N142	NPN	Syl	Pwr		4W	30	.8A	65	.975αT	-50	.4T	26T	-100	20	
2N143	PNP	Syl	Pwr		4W	-30	-.8A	65	.975αT	50	.4T	26T	-100	-20	
2N144	NPN	Syl	Pwr		4W	30	.8A	65	.975αT	50	.4T	26T	100	20	
2N145	NPN	TI	IF	A	65	20	5	75	30			30	3	9	2N293

JEDEC No.	Type	Mfr.	Use	Dwg. No.	MAXIMUM RATINGS Pc mw @ 25°C	BVCB BVCB*	Ic ma	TJ°C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fab mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE
2N146	NPN	TI	IF	A	65	20	5	75	33			33	3	9	
2N147	NPN	TI	IF	A	65	20	5	75	36			36	3	9	
2N148	NPN	TI	IF	A	65	16	5	75				32	3	12	2N169
2N148A	NPN	TI	IF	A	65	32	5	75				32	3	12	2N169
2N149	NPN	TI	IF	A	65	16	5	75				35	3	12	2N169
2N149A	NPN	TI	IF	A	65	32	5	75				35	3	12	2N169
2N150	NPN	TI	IF	A	65	16	5	75				38	3	12	2N169
2N150A	NPN	TI	IF	A	65	32	5	75				38	3	12	2N169
2N155	PNP	CBS	Pwr		8.5W	−30*	−3A	85			.15T	30	1 ma	−30	
2N156	PNP	CBS	Pwr		8.5W	−30*	−3A	85	24*	.5A	.15T	33	1 ma	−30	
2N157	PNP	CBS	Pwr		8.5W	−60*	−3A	85	20*	.5A	.1		1 ma	−60	
2N157A	PNP	CBS	Pwr		8.5W	−90*	−3A	85	20*	.5A	.1		1 ma	−90	
2N158	PNP	CBS	Pwr		8.5W	−60*	−3A	85	21*	.5A	.15T	37	1 ma	−60	
2N158A	PNP	CBS	Pwr		8.5W	−80*	−3A	85	21*	.5A	.15		1 ma	−80	
2N159	Pt	Sprague	Sw	A	80	−50	−10		26*	.5	2		5	40	
2N160	NPN	GP	Si IF	A	150	40*	25	150	.9α	−1	4T	34T	5	40	2N332
2N160A	NPN	GP	Si IF	A	150	40*	25	150	.9α	−1	4T	34T	5	40	2N332
2N161	NPN	GP	Si RF	A	150	40*	25	150	.95α	−1	5T	37T	5	40	2N333
2N161A	NPN	GP	Si RF	A	150	40*	25	150	.95α	−1	5T	37T	5	40	2N333
2N162	NPN	GP	Si RF	A	150	40*	25	150	.95α	−1	8	38T	5	40	2N335
2N162A	NPN	GP	Si RF	A	150	40*	25	150	.95α	−1	8	38T	5	40	2N335
2N163	NPN	GP	Si RF	A	150	40*	25	150	.975α	−1	6T	40T	5	40	2N335
2N163A	NPN	GP	Si RF	A	150	40*	25	150	.975α	−1	6T	40T	5	40	2N335
2N166	NPN	GE	Obsolete	C	25	6	20	50	32T	1	5T	24T	5	5	2N170
2N167	NPN	GE	Sw	3	65	30	75	85	17*	8	5		1.5	15	2N167
2N168	NPN	GE	IF	3	55	15	20	75	20T	1	6T	28	5	15	2N293
2N168A	NPN	GE	Obsolete	3	65	15	20	85	23*	1	5	28	5	15	2N1086
2N169	NPN	GE	IF	3	65	15	20	85	34*	1	8T	27	5	15	2N169
2N169A	NPN	GE	AF	3	65	15	20	85	34*	1	8T	27	5	15	2N169A
2N170	NPN	GE	IF	3	25	6	20	50	.95αT	1	4T	22T	5	5	2N170
2N172	NPN	TI	IF	A	65	16	5	75				22	3	9	2N293
2N173	PNP	Dlc	Pwr		40W	−60	−13A	95	85T*	1A	.6T	40T	−.5 ma	−40	
2N174	PNP	Dlc	Pwr		40W	−80	−13A	95	40T*	1A	.2T	39T	−10 ma	−60	
2N174A	PNP	Dlc	Pwr		85W	−80	−15A	95	40*	1.2A	.1		−8 ma	−80	
2N175	PNP	RCA	AF	A	20	−10	−2	85	65	.5	2	43T	−12	−25	
2N176	PNP	Motor	Pwr		3W	−12	−600	80				25T			
2N178	PNP	Motor	Pwr		3W	−12	−600	80				29T			
2N179	PNP	Motor	Pwr			−20	−60	88				32T			
2N180	PNP	CBS	AF Out	B	150	−30	−25	75	60T		.7	37T			2N188A
2N181	PNP	CBS	AF Out	B	250	−30	−38	75	60T		.7	34T			2N188A
2N182	NPN	CBS	Sw	B	100	25*	10	85	25T*		2.5		3T	10	2N634 or 2N167
2N183	NPN	CBS	Sw	B	100	25*	10	85	50T*		5		3T	10	2N634 or 2N167

JEDEC No.	Type	Mfr.	Use	Dwg. No.	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ°C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fab mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE
2N184	NPN	CBS	Sw	B	100	25*	10	85	100T*		10		3T	10	2N635 or 2N188A
2N185	PNP	TI	AF Out	A	150	−20	−150	75	35	−100		26	15	−20	2N188
2N186	PNP	GE	AF Out	1	100	−25	200	85	24T*	−100	.8T	28	−16	−25	Use 2N186A
2N186A	PNP	GE	AF Out	1	200	−25	200	85	24T*	−100	.8T	28	−16	−25	2N186A
2N187	PNP	GE	AF Out	1	100	−25	200	85	36T*	−100	1T	30	−16	−25	Use 2N187A
2N187A	PNP	GE	AF Out	1	200	−25	200	85	36T*	−100	1T	30	−16	−25	2N187A
2N188	PNP	GE	AF Out	1	100	−25	−200	85	54T*	100	1.2T	32	−16	−25	Use 2N188A
2N188A	PNP	GE	AF Out	1	200	−25	−200	85	54T*	100	1.2T	32	−16	−25	2N188A
2N189	PNP	GE	AF	1	75	−25	−50	85	24T*	1	.8T	37	−16	−25	2N189
2N190	PNP	GE	AF	1	75	−25	−50	85	36T*	1	1.0T	39	−16	−25	2N190
2N191	PNP	GE	AF	1	75	−25	−50	85	54T*	1	1.2T	41	−16	−25	2N191
2N192	PNP	GE	AF	1	75	−25	−50	85	75T*	1	1.5T	43	−16	−25	2N192
2N193	NPN	Syl	Osc	A	50	15		75	3.8	1	2		40	15	2N1086
2N194	NPN	Syl	Osc	A	50	15		75	4.8	1	2	15T	40	15	2N1086
2N194A	NPN	Syl	Osc	A	50	20	100	75	5	1	2	20	50	18	2N1087
2N206	PNP	RCA	AF	A	75	−30	−50	85	47T		.8				2N320
2N207	PNP	Phil	AF	D	50	−12	−20	65	35	1	2T		−15	−12	2N324
2N207A	PNP	Phil	AF	D	50	−12	−20	65	35	1	2T		−15	−12	2N324
2N207B	PNP	Phil	AF	D	50	−12	−20	65	35	1	2T		−15	−12	2N324
2N211	NPN	Syl	Osc	A	50	10	50	75	3.8	1	2		20	10	2N293
2N212	NPN	Syl	Osc	A	50	10	50	75	7	1	4	22T	20	10	2N293
2N213	NPN	Syl	AF	A	50	25	100	75	70	1		39	200	40	2N169A
2N213A	NPN	Syl	AF	A	150	25	100	85	100	1	10 Kc	38	50	20	None
2N214	NPN	Syl	AF Out	A	125	25	75	75	50	35	.6	26	200	40	None
2N215	PNP	RCA	AF	A	150	−30	−50	85	44		.7	33T	−10	−12	2N320
2N216	NPN	Syl	IF	A	50	15	50	75	3.5	1	2	26T	40	15	2N292
2N217	PNP	RCA	AF	A	150	−25	−70	85	75*			30T			2N321
2N218	PNP	RCA	IF	A	80	−16	−15	85	48	1	6.8	30	−6	−12	2N136
2N219	PNP	RCA	Osc	A	80	−16	−15	85	75	.4	10	32	−6	−12	2N137
2N220	PNP	RCA	AF	A	50	−10	−2	85	65		.8	43			2N323
2N223	PNP	Phil	AF	D	100	−18	−150	65	39	−2	.6T		−20	−9	2N323
2N224	PNP	Phil	AF Out	D	250	−25*	150	75	60*	−100	.5T		−25	−12	2N321
2N225	PNP	Phil	AF Out	D	250	−25*	150	75	60*	−100	.5T		−25	−12	2N321
2N226	PNP	Phil	AF Out	D	250	−30*	150	75	35*	−100	.4T		−25	−30	2N321
2N227	PNP	Phil	AF Out	D	250	−30*	150	75	35*	−100	.4T		−25	−30	2N321
2N228	NPN	Syl	AF Out	A	50	25	50	75	50	35	.6	23	200	40	2N169
2N229	NPN	Syl	AF	A	50	12	40	75	.9α	1	.55		200	5	2N169
2N230	PNP	Mall	Pwr		15W	−30	2A	85	60	.5A	12 Kc		−1.5 ma	−60	
2N231	PNP	Phil	SB RF	D	9	−4.5	−3	55	19	−.5	20 fos		−3	−5	
2N232	PNP	Phil	SB RF	D	9	−4.5	−3	55	9	−.5	30 fos		−6	−5	
2N233	NPN	Syl	IF	A	50	10	50	75	3.0	1			100	10	2N448
2N233A	NPN	Syl	IF	A	50	10	50	75	3.5	1			150	15	2N448

JEDEC No.	Type	Mfr.	Use	Dwg. No.	MAXIMUM RATINGS P_c mw @ 25°C	BV_{CE} BV_{CB}*	I_c ma	T_J°C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_c ma	MIN. f_{ab} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE
2N234	PNP	Bendix	Pwr		25W	−30	−3A	90			8 Kc	25	−1 ma T	−25	
2N234A	PNP	Bendix	Pwr		25W	−30	−3A	90			8 Kc	25	−1 ma T	−25	
2N235	PNP	Bendix	Pwr		25W	−40	−3A	90			7 Kc	30			
2N235A	PNP	Bendix	Pwr		25W	−40	−3A	90			7 Kc	30			
2N236	PNP	Bendix	Pwr		25W	−40	−3A	95			6 Kc	30	−1 ma	−25	
2N236A	PNP	Bendix	Pwr		25W	−40	−3A	95			6 Kc	30	−1 ma	−25	
2N237	PNP	Mar	AF	A	150	−45	−20	85	50		.5	42	−10	−22.5	2N192 25V
2N238	PNP	TI	AF	A	50	−20		75				37	−20	−20	2N191
2N240	PNP	Phil	SB Sw	D	10	−6	−15		16	−.5	30 $f_{\alpha b}$		−3	−5	
2N241	PNP	GE	AF Out	1	100	−25	200	85	73T*	100	1.3T	35T	−16	−25	2N241
2N241A	PNP	GE	AF Out	1	200	−25	200	85	73T*	100	1.3T	35T	−16	−25	2N241A
2N242	PNP	Syl	Pwr		20W	−45	−2A	85			5 Kc	30	−5 ma	−45	
2N243	NPN	TI	Si AF	A	750	60*	60	150	.9	−5		30	1	30	
2N244	NPN	TI	Si AF	A	750	60*	60	150	.961	−5		30	1	30	
2N247	PNP	RCA	Drift RF	A	80	−12	−10	85	60		30	37	−20	−12	
2N248	PNP	TI	RF	A	30	−25	−5	85	20T*	.5	50T		−10	−12	
2N249	PNP	TI	AF	C	350	−25	−200	85	30	−100			−25	−25	2N320
2N250	PNP	TI	Pwr		12W	−30	−2A	80	30*	−.5A			−1 ma	−30	
2N251	PNP	TI	Pwr		12W	−60	−2A	80	30*	−.5A		30	−2 ma	−60	
2N252	PNP	TI	IF	A	30	−16	−5	55				28	−10	−12	
2N253	NPN	TI	IF	A	65	12	5	75				32	3	9	2N293
2N254	NPN	TI	IF	A	65	20	5	75					3	9	2N293
2N255	PNP	CBS	Pwr		1.5W	−15*	−3	85			.2T	19			
2N256	PNP	CBS	Pwr		1.5W	−30*	−3	85			.2T	22			
2N257	PNP	Cle	Pwr		2W	−40*		85	55T	.5A	7 Kc	30	−2 ma	−40	
2N260	PNP	Cle	Si AF	B	200	−10*	−50	150	16T	1	1.8T	38T	.001T	−6	2N332
2N260A	PNP	Cle	Si AF	B	200	−30*	−50	150	16T	1	1.8T	38T	.001T	−6	2N332
2N261	PNP	Cle	Si AF	B	200	−75*	−50	150	10T	1	1.8T	36T	.001T	−6	2N332
2N262	PNP	Cle	Si AF	B	200	−10*	−50	150	20T	1	6T	40T	.001T	−6	2N333
2N262A	PNP	Cle	Si AF	B	200	−30*	−50	150	20T	1	6T	40T	.001T	−6	2N333
2N265	PNP	GE	AF	1	75	−25	−50	85	110T*	1	1.5T	45	−16	−25	2N265
2N267	PNP	RCA	Drift RF	A	80	−12	−10	85	60		30	37	−20	−12	
2N268	PNP	Cle	Pwr		2W	−80*		85			6 Kc	28	−2 ma	−80	
2N268A	PNP	Cle	Pwr		2W	−60		90	20*	2A			−2 ma	−80	
2N269	PNP	RCA	Sw	C	120	−24	−100	85	35		4		−5	−12	2N404
2N270	PNP	RCA	AF Out	A	150	−25	−75	85	70	150		35	−10	−25	2N321
2N271	PNP	Ray	RF	A	150	−10	−200	85	45T	1	10T	29T	−5	−12	
2N271A	PNP	Ray	IF	A	150	−10	−200	85	45T	1	10T	39T	−5	−12	
2N272	PNP	Ray	AF	A	150	−24	−100	85	60		1T	12T	−6T	−20	2N323
2N273	PNP	Ray	RF	A	150	−30	−100	85	10	50		29	−6T	−20	2N1098
2N274	PNP	RCA	Drift RF	D	80	−12	−10	85	60T	1	30T	45T	−20	−12	
2N277	PNP	Dlco	Pwr		55W	−40	12A	95	85T	1.2A	.5T	34T	−.5 ma T	−30	

JEDEC No.	Type	Mfr.	Use	Dwg. No.	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ°C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fab mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE
2N278	PNP	Dlco	Pwr		55W	−50	12A	95	85T	1.2A	.5T	34T	−.5 ma T	−20	
2N279	PNP	Am	AF	B	125	−20	−10	75	20	.5	.3T		−12	−4.5	2N319
2N280	PNP	Am	AF	B	125	−20	−10	75	30	3	.3T		−12	−4.5	2N320
2N281	PNP	Am	AF	B		−16	−50	75	45*	10	.35T		−15	−30	2N321
2N282	PNP	Am	AF	B	167	−16	−50	75	45*	10	.35T		−15	−30	2N321
2N283	PNP	Am	AF	B	125	−20	−10	75	30	.5	.5T		−6	−4.5	2N320
2N284	PNP	Am	Osc	A	125	−32	−125	75	45*	10	.35		−10	−10	2N1056
2N284A	PNP	Am	Osc	A	125	−60	−125	75	45*	10	.35		−10	−10	2N1056
2N285	PNP	Bendix	Pwr		25W	−40	3A	95			6 Kc	38	−1 ma	−25	
2N285A	PNP	Bendix	Pwr		25W	−40	3A	95			6 Kc	38	−1 ma	−25	
2N290	PNP	Dlco	Pwr		55W	−70	−12A	95	72T*	1.2A	.4T	37T	−1 ma T	−60	
2N291	PNP	TI	AF	A	180	−25	−200	85	30*	100		31	−25	−25	2N188A
2N292	NPN	GE	IF	3	65	15	−20	85	8	1	5T	25.5	5	15	2N292
2N293	NPN	GE	IF	3	65	15	−20	85	8	1	8T	28	5	15	2N293
2N297	PNP	Cle	Pwr		35W	−50	−5A	95	40*	.5	5 Kc		3 ma	−60	
2N297A	PNP	Cle	Pwr		35W	−50	−5A	95	40*	.5	5 Kc		3 ma	−60	
2N299	PNP	Phil	SB RF	E	20	−4.5	−5	85			90 fos	20	−3	−5	
2N300	PNP	Phil	SB RF	E	20	−4.5	−5	85	11	.5	85 fos		−3	−5	
2N301	PNP	RCA	Pwr		11W	−20	−1.5A	91	70T*	1A		33T	−3 ma	−30	
2N301A	PNP	RCA	Pwr		11W	−30	−1.5A	91	70T*	1A		33T	−3 ma	−30	
2N302	PNP	Ray	Obsolete	A	150	−10	−200	85	45T		7		−1T	−.12	2N186A
2N303	PNP	Ray	Obsolete	A	150	−10	−200	85	75T		14		−1T	−.12	2N186A
2N306	NPN	Syl	AF	A	50	15		75	25	1	.6	34	50	20	2N292
2N307	PNP	Syl	Pwr		10W	−35	−1A	75	20	200	3 Kc		15 ma	−35	
2N307A	PNP	Syl	Pwr		17W	−35	−2A	75	20	200	3.5 Kc	22	7 ma	−35	
2N308	PNP	TI	IF	A	30	−20	−5	55				39	−10	−9	
2N309	PNP	TI	IF	A	30	−20	−5	55				41	−10	−9	
2N310	PNP	TI	IF	A	30	−30	−5	55	28T			37T	−10	−9	
2N311	PNP	Motor	Sw	C	75	−15		85	25				−60	−15	2N123
2N312	NPN	Motor	Sw	C	75	15		85	25				60	15	2N167
2N313	NPN	GE	Obsolete		65	15	20	85	25		5	36 max			Use 2N292
2N314	NPN	GE	Obsolete		65	15	20	85	25		8	39 max			Use 2N293
2N315	PNP	GT	Sw	C	100	−15	−200	85	15	100	5T		−2	−5	2N396
2N316	PNP	GT	Sw	C	100	−10	−200	85	20	200	12T		−2	−5	2N397
2N317	PNP	GT	Sw	C	100	−6	−200	85	20	400	20T		−2	−5	
2N318	PNP	GT	Photo	A	50	−12	−20				.75T				
2N319	PNP	GE	AF	4	225	−20	−200	85	34T*	−20	2T		−16	−25	2N319
2N320	PNP	GE	AF	4	225	−20	−200	85	50T*	−20	2.5T		−16	−25	2N320
2N321	PNP	GE	AF	4	225	−20	−200	85	80T*	−20	3.0T		−16	−25	2N321
2N322	PNP	GE	AF	4	140	−16	−100	60	45T	−20	2T		−16	−16	2N322
2N323	PNP	GE	AF	4	140	−16	−100	60	68T	−20	2.5T		−16	−16	2N323

JEDEC No.	Type	Mfr.	Use	Dwg. No.	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{ab} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE
2N324	PNP	GE	AF	4	140	−16	−100	60	85T	−20	3.0T		−16	−16	2N324
2N325	PNP	Syl	Pwr		12W	−35	−2A	85	30*	−500	.15		−500	−30	
2N326	NPN	Syl	Pwr		7W	35	2A	85	30*	500	.15		500	30	
2N327	PNP	Ray	Si AF	C	335	−50*	−100	160	9	1	.3T	30	−.1	−30	
2N327A	PNP	Ray	Si AF	C	350	−50*	−100	160	9*	.1	.2T		−.1	−30	
2N328	PNP	Ray	Si AF	C	335	−35*	−100	160	18	1	.35T	32	−.1	−30	
2N328A	PNP	Ray	Si AF	C	350	−50*	−100	160	18*	1	.3T		−.1	−30	
2N329	PNP	Ray	Si AF	C	335	−30*	−100	160	36	1	.6T	34	−.1	−30	
2N329A	PNP	Ray	Si AF	C	350	−50*	−100	160	36*	1	.5T		−.1	−30	
2N330	PNP	Ray	Si AF	C	335	−45*	−50	160	9	1	.5	30	−.1	−30	
2N330A	PNP	Ray	Si AF	C	350	−50*	−100	160	25T	1	.5	34T	−.1	−30	
2N331	PNP	RCA	AF	C	200	−30*	−200	85	60	−50		44T	−16	−30	2N188A
2N332	NPN	TI-GE	Si AF	5	150	45*	25	200	9	1	10T	14T	2	30	2N332
2N333	NPN	TI-GE	Si AF	4	150	45*	25	200	18	1	12*	14T	2	30	2N333
2N334	NPN	TI-GE	Si AF	4	150	45*	25	200	18	1	8	13T	2	30	2N334
2N335	NPN	TI-GE	Si AF	4	150	45*	25	200	37	1	14*	13T	2	30	2N335
2N336	NPN	TI-GE	Si AF	4	150	45*	25	200	76	1	15*	12T	2	30	2N336
2N337	NPN	TI-GE	Si AF	4	125	45*	20	200	19	1	10		1	20	2N337
2N338	NPN	TI-GE	Si AF	4	125	45*	20	200	39	1	20		1	20	2N338
2N339	NPN	TI	Si AF	C	1W	55*	60	150	.9α	−5		30	1	30	
2N340	NPN	TI	Si AF	C	1W	85*	60	150	.9α	−5		30	1	30	
2N341	NPN	TI	Si AF	C	1W	125*	60	150	.9α	−5		30	1	30	
2N342	NPN	TI	Si AF	C	1W	60*	60	150	.9α	−5		30	1	30	
2N343	NPN	TI	Si AF	C	1W	60*	60	150	.966α	−5		30	1	30	
2N344	PNP	Phil	RF	D	40	−5	−5	85	11		30 f_{os}		−3	−5	
2N345	PNP	Phil	RF	D	40	−5	−5	85	25		30 f_{os}		−3	−5	
2N346	PNP	Phil	RF	D	40	−5	−5	85	10		60 f_{os}		−3	−5	
2N350	PNP	Motor	Pwr		10W	−40*	−3A	90	20*	−700	5 Kc	30	−3 ma	−30	
2N351	PNP	Motor	Pwr		10W	−40*	−3A	90	25*	−700	5 Kc	32	−3 ma	−30	
2N352	PNP	Phil	Pwr		25W	−40	−2A	100	30	−1A	10 Kc	30	−5 ma	−1 @ 85°C	
2N353	PNP	Phil	Pwr		30W	−40	−2A	100	40	−1A	7 Kc	30	−5 ma	−1 @ 85°C	
2N354	PNP	Phil	Si AF	D	150	−25*	−50	140	9	1	8 f_{os}		−.1	−10	
2N355	PNP	Phil	Si AF	D	150	−10*	−50	140	9	1	8 f_{os}		−.1	−10	
2N356	NPN	GT	Sw	C	120	18	100	85	20	100	3T		5	5	2N634
2N357	NPN	GT	Sw	C	120	15	100	85	20	200	6T		5	5	2N634
2N358	NPN	GT	Sw	C	120	12	100	85	20	300	9T		5	5	2N635
2N364	NPN	TI	AF	A	150	30*	50	85	9	−1	1		10	30	
2N365	NPN	TI	AF	A	150	30*	50	85	19	−1	1		10	30	
2N366	NPN	TI	AF	A	150	30*	50	85	49	−1	1		10	30	
2N367	PNP	TI	AF	A	100	−30*	−50	75	9	1	.3		−30	−30	2N189
2N368	PNP	TI	AF	A	150	−30*	−50	75	19	1	.4		−20	−30	2N189
2N369	PNP	TI	AF	A	150	−30*	−50	75	49	1	.5		−20	−30	2N190

JEDEC No.	Type	Mfr.	Use	Dwg. No.	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{ab} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE
2N370	PNP	RCA	Drift RF	A	80	−24*	−20	85	60T	1	30T	31M	−10	−12	
2N371	PNP	RCA	Drift RF	A	80	−24*	−20	85	.984T	1	30T	17.6M	−10	−12	
2N372	PNP	RCA	Drift RF	A	80	−24*	−20	85	60T	1	30T	12.5M	−10	−12	
2N373	PNP	RCA	Osc	A	80	−24*	−10	85	60T	1	30T	40T	−16	−12	
2N374	PNP	RCA	Drift Osc	A	80	−24*	−10	85	60T	1	30T	40T	−16	−12	
2N375	PNP	Motor	Pwr		45W	−60	−3A	95	35	1A	7 Kc		−3 ma	−60	
2N376	PNP	Motor	Pwr		10W	−40*	−3A	90	60T	1A	5 Kc	35T			
2N377	NPN	Syl	Sw	C	150	20	200	100	20*	200	5T		20	20	2N634
2N378	PNP	TS	Pwr		50W	−40	−5A	100	15*	2A	5 Kc		−500	−25	
2N379	PNP	TS	Pwr		50W	−80	−5A	100	20*	2A	5 Kc		−500	−25	
2N380	PNP	TS	Pwr		50W	−60	−5A	100	30*	2A	7 Kc		−500	−25	
2N381	PNP	TS	AF Out	C	200	−25	−200	85	50T	20	1.2T	31T	−10T	−25	2N320
2N382	PNP	TS	AF Out	C	200	−25	−200	85	75T	20	1.5T	33T	−10T	−25	2N321
2N383	PNP	TS	AF Out	C	200	−25	−200	85	100T	20	1.8T	35T	−10T	−25	2N321
2N384	PNP	RCA	Drift Osc	C	120	−30	−10	85	60T	1.5	100T	15	−16	−12	
2N385	NPN	Syl	Sw	C	150	25	200	100	30*	30	4		35	25	2N634
2N386	PNP	Phil	Pwr		12.5W	−60	−3A	100	20	−2.5A	7 Kc		−5 ma	−60	
2N387	PNP	Phil	Pwr		12.5W	−80	−3A	100	20	−2.5A	6 Kc		−5 ma	−80	
2N388	NPN	Syl	Sw		150	20	200	100	60*	30	8T		20	20	2N635
2N389	NPN	TI	Si Pwr		85W	60		200	12	1A			10 ma	60 @ 100°C	
2N392	PNP	Dlc	Pwr		70W	−60*	−5A	95	60	3A	6 Kc		−8 ma	−60	
2N393	PNP	Phil	Sw		50	−6	−50	85	20*	−50	40 fos		−5	−5	
2N394	PNP	GE	Sw	2	150	−10	−200	85	20*	−10	4		−6	−10	2N394
2N395	PNP	GE	Sw	2	200	−15	−200	100	20*	−10	3		−6	−15	2N395
2N396	PNP	GE	Sw	2	200	−20	−200	100	30*	−10	5		−6	−20	2N396
2N397	PNP	GE	Sw	2	200	−15	−200	100	40*	−10	10		−6	−15	2N397
2N398	PNP	RCA	Sw	C	50	−105	−110	85	20*	−5 ma			−14	−2.5	
2N399	PNP	Bendix	Pwr		25W	−40	−3A	90			8 Kc	33T	−1 ma	−25	
2N401	PNP	Bendix	Pwr		25W	−40	−3A	90			8 Kc	30T	−1 ma	−25	
2N402	PNP	W	AF	C	180	−20	−150	85	.96αT	1	.6T	37T	−15	−20	2N188A
2N403	PNP	W	AF	C	180	−20	−200	85	.97αT	1	.85T	32	−15	−20	2N187A
2N404	PNP	RCA-GE	Sw	2	120	−24	−100	85			4		−5	−12	2N404
2N405	PNP	RCA	AF	A	150	−18	−35	85	35T*	1	.65T	43T	−14	−12	2N188A
2N406	PNP	RCA	AF	C	150	−18	−35	85	35T*	1	.65T	43T	−14	−12	2N188A
2N407	PNP	RCA	AF	A	150	−18	−70	85	65T*	−50		33T	−14	−12	2N241A
2N408	PNP	RCA	AF	C	150	−18	−70	85	65T*	−50		33T	−14	−12	2N241A
2N409	PNP	RCA	IF	A	80	−13	−15	85	.98αT	1	6.7T	38T	−10	−13	2N450
2N410	PNP	RCA	IF	C	80	−13	−15	85	.98αT	1	6.7T	38T	−10	−13	2N450
2N411	PNP	RCA	Osc	A	80	−13	−15	85	75T	.6		32T	−10	−13	2N450
2N412	PNP	RCA	Osc	C	80	−13	−15	85	75T	.6		32T	−10	−13	2N450
2N413	PNP	Ray	RF	C	150	−18	−200	85	30T	1	2.5T	33T	−5	−12	2N450
2N413A	PNP	Ray	IF	C	150	−15	−200	85	30T	1	2.5T	33T	−5	−12	2N450

JEDEC No.	Type	Mfr.	Use	Dwg. No.	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ°C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fab mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE
2N414	PNP	Ray	RF	C	150	−15	−200	85	60T	1	7T	16T	−5	−12	2N450
2N414A	PNP	Ray	IF	C	150	−15	−200	85	60T	1	7T	35T	−5	−12	2N450
2N415	PNP	Ray	Osc	C	150	−10	−200	85	80T	1	10T	30T	−5	−12	2N450
2N415A	PNP	Ray	IF	C	150	−10	−200	85	80T	1	10T	39T	−5	−12	2N450
2N416	PNP	Ray	RF	C	150	−12	−200	85	80T	1	10T	20T	−5	−12	2N450
2N417	PNP	Ray	RF	C	150	−10	−200	85	140T	1	20T	27T	−5	−12	2N450
2N422	PNP	Ray	AF	C	150	−20	−100	85	50T	1	.8T	38T	−15	−20	2N320
2N425	PNP	Ray	Sw	C	150	−20	−400	85	20*	1	2.5		−25	−30	2N394
2N426	PNP	Ray	Sw	C	150	−18	−400	85	30*	1	3		−25	−30	2N395
2N427	PNP	Ray	Sw	C	150	−15	−400	85	40*	1	5		−25	−30	2N396
2N428	PNP	Ray	Sw	C	150	−12	−400	85	60*	1	10		−25	−30	2N397
2N438	NPN	CBS	Sw	C	100	25		85	20*	50	2.5		10	25	2N634
2N438A	NPN	CBS	Sw	C	150	25		85	20*	50	2.5		10	25	2N634
2N439	NPN	CBS	Sw	C	100	20		85	30	50	5		10	25	2N634
2N439A	NPN	CBS	Sw	C	150	20		85	30*	50	5		10	25	2N634
2N440	NPN	CBS	Sw	C	100	15		85	40*	50	10		10	25	2N635
2N440A	NPN	CBS	Sw	C	150	15		85	40*	50	10		10	25	2N635
2N444	NPN	GT	Sw	C	120	15		85	15T		.5T		2T	10	
2N445	NPN	GT	Sw	C	100	12		85	35T		2T		2T	10	
2N446	NPN	GT	Sw	C	100	10		85	60T		5T		2T	10	2N634
2N447	NPN	GT	Sw	C	100	6		85	125T		9T		2T	10	2N635
2N448	NPN	GE	IF	3	65	15	20	85	8*	1	5T	23	5	15	2N448
2N449	NPN	GE	IF	3	65	15	20	85	34*	1	8T	24.5	5	15	2N449
2N450	PNP	GE	Sw	8	150	−12	−125	85	30*	−10	5		−6	−12	2N450
2N456	PNP	TI	Pwr		50	−40	5A	95	130T*	1A			−2 ma	−40	
2N457	PNP	TI	Pwr		50	−60	5A	95	130T*	1A			−2 ma	−60	
2N458	PNP	TI	Pwr		50	−80	5A	95	130T*	1A			−2 ma	−80	
2N459	PNP	TS	Pwr		50	−60	5A	100	20*	2A	5 Kc		100 ma	−60	
2N460	PNP	TS	AF	C	200	−45*	−400	100	.94α	1	1.2T	34T	−15	−45	2N319
2N461	PNP	TS	AF	C	200	−45*	−400	100	.97α	1	1.2T	37T	−15	−45	2N320
2N462	PNP	Phil	Sw	F	150	−40*	−200	75	20*	−200	.5		−35	−35	
2N463	PNP	WE	Pwr		37.5W	−60	5A	100	20*	−2A	4 mc		−300	−40	
2N464	PNP	Ray	AF	C	150	−40	−100	85	14	1	.7T	40T	−15	−20	2N187A
2N465	PNP	Ray	AF	C	150	−30	−100	85	27	1	.8T	42T	−15	−20	2N320
2N466	PNP	Ray	AF	C	150	−20	−100	85	56	1	1T	44T	−15	−20	2N321
2N467	PNP	Ray	AF	C	150	−15	−100	85	112	1	1.2T	45T	−15	−20	2N508
2N469	PNP	GT	Photo	C	50			75	10	1	1T		−50	−6	
2N481	PNP	Ray	Osc	C	150	−12	−20	85	50T	1	3T		−10	−12	
2N482	PNP	Ray	IF	C	150	−12	−20	85	50T	1	3.5T		−10	−12	
2N483	PNP	Ray	IF	C	150	−12	−20	85	60T	1	5.5T		−10	−12	
2N484	PNP	Ray	IF	C	150	−12	−20	85	90T	1	10T		−10	−12	
2N485	PNP	Ray	IF	C	150	−12	−10	85	50T	1	7.5T		−10	−12	

JEDEC No.	Type	Mfr.	Use	Dwg. No.	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{ab} mc	MIN. G_e db	MAX. I_{CO} (µa)	@ V_{CB}	Closest GE
2N486	PNP	Ray	IF	C	150	−12	−10	85	100T	1	12T		−10	−12	
2N489		GE	Si Uni	5	SEE G-E TRANSISTOR SPECIFICATION SECTION										2N489
2N490		GE	Si Uni	5	SEE G-E TRANSISTOR SPECIFICATION SECTION										2N490
2N491		GE	Si Uni	5	SEE G-E TRANSISTOR SPECIFICATION SECTION										2N491
2N492		GE	Si Uni	5	SEE G-E TRANSISTOR SPECIFICATION SECTION										2N492
2N493		GE	Si Uni	5	SEE G-E TRANSISTOR SPECIFICATION SECTION										2N493
2N494		GE	Si Uni	5	SEE G-E TRANSISTOR SPECIFICATION SECTION										2N494
2N495	PNP	Phil	Si RF	C	150	−25	−50	140	9	1	8 f_{os}		−.1	−10	
2N496	PNP	Phil	Si Sw	C	150	−10	−50	140	9	1	8 f_{os}		−.1	−10	
2N497	NPN	TI	Si AF	C	900	60		200	12*	200			10	30	
2N498	NPN	TI	Si AF	C	900	100		200	12*	200			10	30	
2N502	PNP	Phil	MADT	C	25 @ 41°C	−20		85	9	2	200	8	−100	−20	
2N503	PNP	Phil	MADT	C	25 @ 41°C	−20	−50	85	9	2	100	11	−100	−20	
2N506	PNP	Syl	AF	A	50	−40*	−100	85	25	−10	.6		−15	−30	2N187A
2N507	NPN	Syl	AF	A	50	40	100	85	25	10	.6		15	30	
2N508	PNP	GE	AF Out	2	140	−16	−100	85	125T*	−20	3.5T		−16	−16	2N508
2N509	PNP	WE	RF	C	225	−30*	−40	100	.96α	10	750T		−5	−20	
2N515	NPN	Syl	IF	A	50	18	10	75	4	1	2	23	50	18	
2N516	NPN	Syl	IF	A	50	18	10	75	4	1	2	25	50	18	
2N517	NPN	Syl	IF	A	50	18	10	75	4	1	2	27	50	18	
2N519	PNP	GT	Sw	C	100	−15		85	15	1	.5		−2	−5	2N394
2N520	PNP	GT	Sw	C	100	−12		85	20	1	3		−2	−5	2N394
2N521	PNP	GT	Sw	C	100	−10		85	35	1	8		−2	−5	2N397
2N522	PNP	GT	Sw	C	100	−8		85	60	1	15		−2	−5	
2N523	PNP	GT	Sw	C	100	−6		85	80	1	21		−2	−5	
2N524	PNP	GE	AF	2	225	−30	−500	100	16	−1	.8		−10	−30	2N524
2N525	PNP	GE	AF	2	225	−30	−500	100	30	−1	1		−10	−30	2N525
2N526	PNP	GE	AF	2	225	−30	−500	100	44	−1	1.3		−10	−30	2N526
2N527	PNP	GE	AF	2	225	−30	−500	100	60	−1	1.5		−10	−30	2N527
2N529	PNP-NPN	GT	AF	C	100	15		85	15	1	2.5T		5	5	
2N530	PNP-NPN	GT	AF	C	100	15		85	20	1	3T		5	5	
2N531	PNP-NPN	GT	AF	C	100	15		85	25	1	3.5T		5	5	
2N532	PNP-NPN	GT	AF	C	100	15		85	30	1	4T		5	5	
2N533	PNP-NPN	GT	AF	C	100	15		85	35	1	4.5T		5	5	
2N534	PNP	Phil	AF	D	25 @ 50°C	−50	−25	65	35	−1			−15	−50	2N1057
2N535	PNP	Phil	AF	D	50	−20	−20	85	35	−1	2T		−10	−12	
2N535A	PNP	Phil	AF	D	50	−20	−20	85	35	−1	2T		−10	−12	

JEDEC No.	Type	Mfr.	Use	Dwg. No.	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ°C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fab mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE
2N535B	PNP	Phil	AF	D	50	−20	−20	85	35	−1	2T		−10	−12	
2N536	PNP	Phil	Sw	D	50	−20	−30	85	100*	−30	1		−10	−12	
2N538	PNP	M-H	Pwr		10W @ 70°C	−80*		95	40	2A	8 Kc T		−20 ma	−80	
2N538A	PNP	M-H	Pwr		10W @ 70°C	−80*		95	40	2A	8 Kc T		−20 ma	−80	
2N539	PNP	M-H	Pwr		10W @ 70°C	−80*		95	27	2A	7 Kc T		−20 ma	−80	
2N539A	PNP	M-H	Pwr		10W @ 70°C	−80		95	27	2A	7 Kc T		−20 ma	−80	
2N540	PNP	M-H	Pwr		10W @ 70°C	−80		95	18	2A	6 Kc T		−20	−80	
2N540A	PNP	M-H	Pwr		10W @ 70°C	−80		95	18	2A	6 Kc T		−20	−80	
2N544	PNP	RCA	RF	A	80	−24*	−10	85	60T	1	30T	30.4	−16	−12	
2N553	PNP	Del	Pwr		12W @ 71°C	−80*	−4A	95	40	−.5A	20 Kc		−2 ma	−60	
2N554	PNP	Motor	Pwr		10W @ 80°C	−40*	−3A	90	30T*	−.5A	8 Kc T	20	−50T	−2	
2N555	PNP	Motor	Pwr		10W @ 80°C	−30	−3A	90	20	−.5A	5 Kc	34T	−7 ma	−30	
2N556	NPN	Syl	Sw	C	100	25*	200	85	35*	1					
2N557	NPN	Syl	Sw	C	100	20*	200	85	20*	1					
2N558	NPN	Syl	Sw	C	100	15*	200	75	60*	1					
2N559	PNP	WE	Sw	C	150	−15	−50	100	25*	10			−50	−5 @ 65°C	
2N561	PNP	RCA	Pwr		50W	−50	−5A	100	65T	−1A	.5	24.6	−500	−30	
2N563	PNP	GT	AF	A	150	−25	−300	85	10*	1	.8T		−5	−10	2N44
2N564	PNP	GT	AF	C	120	−25	−300	85	10*	1	.8T		−5	−10	2N524
2N565	PNP	GT	AF	A	150	−25	−300	85	30*	1	1T		−5	−10	2N43
2N566	PNP	GT	AF	C	120	−25	−300	85	30*	1	1T		−5	−10	2N525
2N567	PNP	GT	AF	A	150	−25	−300	85	50*	1	1.5T		−5	−10	2N43
2N568	PNP	GT	AF	C	120	−25	−300	85	50*	1	1.5T		−5	−10	2N526
2N569	PNP	GT	AF	A	150	−20	−300	85	70*	1	2T		−5	−10	2N241A
2N570	PNP	GT	AF	C	120	−20	−300	85	70*	1	2T		−5	−10	2N527
2N571	PNP	GT	AF	A	150	−10	−300	85	100*	1	3T		−5	−10	
2N572	PNP	GT	AF	C	120	−10	−300	85	100*	1	3T		−5	−10	
2N574	PNP	M-H	Pwr		25W @ 75°C	−60*	−15A	95	10*	−10A	6 Kc T		−7 ma	−60	
2N574A	PNP	M-H	Pwr		25W @ 75°C	−80*	−15A	95	10*	−10A	6 Kc T		−20 ma	−80	
2N575	PNP	M-H	Pwr		25W @ 75°C	−60*	−15A	95	19*	−10A	5 Kc T		−7 ma	−60	
2N575A	PNP	M-H	Pwr		25W @ 75°C	−80*	−15A	95	19*	−10A	5 Kc T		−20 ma	−80	
2N576	NPN	Syl	Sw	C	200	20	400	100	80T*	30	5T		20	20	
2N576A	NPN	Syl	Sw	C	200	20	400	100	20*	400	5T		40	40	
2N577	PNP	MU	Photo	B	25	−25	−10	55			3 Kc				
2N578	PNP	RCA	Sw	C	120	−14	−400	85	10*	1	3		−5	−12	2N394
2N579	PNP	RCA	Sw	C	120	−14	−400	85	20*	1	5		−5	−12	2N396
2N580	PNP	RCA	Sw	C	120	−14	−400	85	30*	1	10		−5	−12	2N397
2N581	PNP	RCA	Sw	C	80	−15	−100	85	20*	−20	4		−6	−6	2N394
2N582	PNP	RCA	Sw	C	120	−14	−100	85	40*	−20	14		−5	−12	
2N583	PNP	RCA	Sw	C	150	−15	−200	85	20*	−20	4		−6	−6	2N394
2N584	PNP	RCA	Sw	C	120	−14	−100	85	40*	−20	14		−5	−12	
2N585	NPN	RCA	Sw	C	120	24	200	85	20*	20	3		8	12	2N634

JEDEC No.	Type	Mfr.	Use	Dwg. No.	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{ab} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE
2N586	PNP	RCA	Sw	A	250	−45*	−250	85	35T*	−250			−16	−45	
2N587	NPN	Syl	Sw	C	150	20	200		20*	200			50	40	
2N591	PNP	RCA	AF	C	50	−32	−20	100	70T	2	.7T	41T	−6.5	−10	2N324
2N592	PNP	GT	Sw	C	125	−20		85	20*	1	.4T		−5	−5	
2N593	PNP	GT	Sw	C	125	−30		85	30*	.5	.6T		−5	−5	
2N594	NPN	GT	Sw	C	100	20		85	20*	1	1.5		5	5	
2N595	NPN	GT	Sw	C	100	15		85	35*	1	3		5	5	
2N596	NPN	GT	Sw	C	100	10		85	50*	1	5		5	5	2N634
2N597	PNP	Phil	Sw	C	250	−40	−400	100	40*	−100	3		−25	−45	
2N598	PNP	Phil	Sw	C	250	−20	−400	100	50*	−100	5		−25	−30	
2N600	PNP	Phil	Sw	C	750	−20	−400	100	50*	−100	5		−25	−30	
2N602	PNP	GT	Drift Sw	C	120	−20		85	20*	.5			−8	−10	2N395
2N603	PNP	GT	Drift Sw	C	120	−20		85	30*	.5			−8	−10	2N396
2N604	PNP	GT	Drift Sw	C	120	−20		85	40*	.5			−8	−10	2N397
2N605	PNP	GT	Drift RF	C	120	−15		85	40T	−1		20	−10	−12	2N394
2N606	PNP	GT	Drift RF	C	120	−15		85	60T	−1		25	−10	−12	2N395
2N607	PNP	GT	Drift RF	C	120	−15		85	80T	−1		30	−10	−12	2N396
2N608	PNP	GT	Drift RF	C	120	−15		85	120T	−1		35	−10	−12	2N396
2N609	PNP	W	AF Out	C	180	−20	−200	85	90T*	100		30T	−25	−20	2N241A
2N610	PNP	W	AF Out	C	180	−20	−200	85	65T*	100		28T	−25	−20	2N188A
2N611	PNP	W	AF Out	C	180	−20	−200	85	45T*	100		26T	−25	−20	2N187A
2N612	PNP	W	AF	C	180	−20	−150	85	.96αT	1	.6T	37	−25	−20	2N189
2N613	PNP	W	AF Out	C	180	−20	−200	85	.97αT	1	.85T	32	−25	−20	2N190
2N614	PNP	W	IF	C	125	−15	−150	85	4.5T	.5	3T	26T	−6	−20	
2N615	PNP	W	IF	C	125	−15	−150	85	7.5T	.5	5T	34T	−6	−20	
2N616	PNP	W	IF	C	125	−12	−150	85	25T	.5	9T	20T	−6	−15	
2N617	PNP	W	Osc	C	125	−12	−150	85	15T	.5	7.5T	30T	6	−15	
2N618	PNP	Motor	Pwr		45W	−80*	−3A	90	60*	−1A	5 Kc		−3 ma	−60	
2N622	NPN	Ray	Si AF	C	400	50*	50	160	25T*	.5	.3	34T	.1	30	
2N624	PNP	Syl	RF	C	100	−20	−10	100	20	2	12.5	20T	−30	−30	
2N625	NPN	Syl	Sw	C	2.5W	30		100	30*	50			100	−40	
2N626	NPN	AR	Pwr		10W	30	3A	90	18,000	1A	7 Kc		2 ma	5	
2N631	PNP	Ray	AF Out	C	170	−20	−50	85	150T	10	1.2T	35T	−25	−20	2N508
2N632	PNP	Ray	AF Out	C	150	−24	−50	85	100T	10	1T	25T	−25	−20	2N324
2N633	PNP	Ray	AF Out	C	150	−30	−50	85	60T	10	.8T	25T	−25	−20	2N323
2N634	NPN	GE	Sw	2	150	20	300	85	15*	200	5		5	5	2N634
2N635	NPN	GE	Sw	2	150	20	300	85	25*	200	10		5	5	2N635
2N636	NPN	GE	Sw	2	150	20	300	85	35*	200	15		5	5	2N636
2N637	PNP	Bendix	Pwr		25W	−40	−5A	100	30*	−3A			1 ma	−25	
2N637A	PNP	Bendix	Pwr		25W	−70	−5A	100	30*	−3A			5 ma	−60	
2N637B	PNP	Bendix	Pwr		25W	−80	−5A	100	30*	−3A			5 ma	−60	
2N638	PNP	Bendix	Pwr		25W	−40	−5A	100	20*	−3A			1 ma	−25	

					MAXIMUM RATINGS				ELECTRICAL PARAMETERS						
JEDEC No.	Type	Mfr.	Use	Dwg. No.	Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ°C	MIN. hfe-hFE*	@ Ic ma	MIN. fab mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE
2N638A	PNP	Bendix	Pwr		25W	−70	−5A	100	20*	−3A			5 ma	−60	
2N638B	PNP	Bendix	Pwr		25W	−80	−5A	100	20*	−3A			5 ma	−60	
2N639	PNP	Bendix	Pwr		25W	−40	−5A	100	15*	−3A			1 ma	−25	
2N639A	PNP	Bendix	Pwr		25W	−70	−5A	100	15*	−3A			5 ma	−60	
2N639B	PNP	Bendix	Pwr		25W	−80	−5A	100	15*	−3A			5 ma	−60	
2N640	PNP	RCA	Drift RF	A	80	−34*	−10	85	.984αT	−1	42T	28T	−5	−12	
2N641	PNP	RCA	Drift IF	A	80	−34*	−10	85	.984αT	−1	42T	28T	−7	−12	
2N642	PNP	RCA	Drift Osc	A	80	−34*	−10	85	.984αT	−1	42T	28T	−7	−12	
2N643	PNP	RCA	Drift Sw	C	120	−29	−100	85	20*	−5	20		−10	−7	
2N644	PNP	RCA	Drift Sw	C	120	−29	−100	85	20*	−5	40		−10	−7	
2N645	PNP	RCA	Drift Sw	C	120	−29	−100	85	20*	−5	60		−10	−7	
2N647	NPN	RCA	AF	C	100	25	50	85	70T*	−50		54T	14	25	
2N649	NPN	RCA	AF	C	100	18	50	85	65T*	−50		54T	14	12	
2N656	NPN	TI	Si AF	C	40W	60		200	30	30			10	30	
2N657	NPN	TI	Si AF	C	4W	100		200	60	−30			10	30	
2N658	PNP	Ray	Sw	C	175	−16	−1A	85	25*	−1	2.5		−6	−12	2N394
2N659	PNP	Ray	Sw	C	175	−14	−1A	85	40*	−1	5.0		−25	−25	2N396
2N660	PNP	Ray	Sw	C	175	−11	−1A	85	60*	−1	10		−25	−25	2N397
2N661	PNP	Ray	Sw	C	175	−9	−1A	85	80*	−1	15		−25	−25	
2N662	PNP	Ray	Sw	C	175	−11	−1A	85	30*	−1	4		−25	−25	2N396
2N665	PNP	Dlc	Pwr		35W	−80*	5A (IE)	95	40*	−.5A	20 Kc		−2 ma	−30 @ 71°C	
2N679	NPN	Syl	Sw	C	150	20		85	20*	30	2		25	25	
2N1010	NPN	RCA	AF	C	20	10	2	85	35T	−.3	2T		10	10	
2N1017	PNP	Ray	Sw	C	150	−10	−400	85	70*	1	15		−25	−30	
2N1021	PNP	TI	Pwr		50W	−100	−[illegible]	95	70T*	−1A			−2 ma	−100	
2N1022	PNP	TI	Pwr		50W	−120	−5	95	70T*	−1A			−2 ma	−120	
2N1056	PNP	GE	Sw	1	240	−50	−300	100	18*	−20	.5		−25	−70	2N1056
2N1057	PNP	GE	Sw	1	240	−45	−300	100	34*	−20	.5		−16	−45	2N1057
2N1058	NPN	Syl	Osc	A	50	20	[illegible]	75	10	1	4	22.5	50	18	
2N1059	NPN	Syl	AF Out	A	180	15	100	75	50*	35	10 Kc	25	50	40	
2N1067	NPN	RCA	Si Pwr	C	5W	30	5A	175	15*	200	.75		500	60	
2N1068	NPN	RCA	Si Pwr	C	10W	30	1.5A	175	15*	750	.75		500	60	
2N1069	NPN	RCA	Si Pwr		50W	15	4A	175	10*	1.5A	.5		1 ma	60	
2N1070	NPN	RCA	Si Pwr		50W	45	4A	175	10*	1.5A	.5		1 ma	60	
2N1086	NPN	GE	Osc	3	65	9	20	85	17*	1	8T	24T	3	5	2N1086
2N1086A	NPN	GE	Osc	3	65	9	20	85	17*	1	8T	24T	3	5	2N1086A
2N1087	NPN	GE	Osc	3	65	9	20	85	17*	1	8T	26T	3	5	2N1087
2N1090	NPN	RCA	Sw	C	120	15	400	85	50*	20	5		8	12	2N634
2N1091	NPN	RCA	Sw	C	120	12	400	85	40*	20	10		8	12	2N635
2N1092	NPN	RCA	Si AF	C	2W	30	500	175	15*	200	.75		500	60	
2N1097	PNP	GE	AF Out	2	140	−16	−100	85	55T	1			−16	−16	2N1097
2N1098	PNP	GE	AF Out	2	140	−16	−100	85	45T	1			−16	−16	2N1098

JEDEC No.	Type	Mfr.	Use	Dwg. No.	MAXIMUM RATINGS: P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	ELECTRICAL PARAMETERS: MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{ab} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE
2N1101	NPN	Syl	AF Out	A	180	15	100	75	25*	35	10 Kc		50	20	
2N1102	NPN	Syl	AF Out	A	180	25	100	75	25*	35	10 Kc		50	40	
2N1121	NPN	GE	IF	3	65	15	20	85	34*	1	8 Kc		5	15	
2N1123	PNP	Phil	Sw	C	750	−40	−400	100	40*	−100	3		−25	−45	
2N1144	PNP	GE	AF Out	1	140	−16	−100	85	55T	1			−16	−16	2N1144
2N1145	PNP	GE	AF Out	1	140	−16	−100	85	45T	1			−16	−16	2N1145
2N1168	PNP	Dlc	Pwr		45W	−50*	5A (I_E)	95	110T	1A	10 Kc T	37T	−8 ma	−50	
2N1198	NPN	GE	Sw	3	65	25	75	85	17*	8	5		1.5	15	
3N21	Pt	Syl	Sw		100	−60		50	2.5						
3N22	NPN	WE	RF			15*		85	.92α		15		10	5	
3N23	NPN	GP	Obsolete			30	5				50	14	10	4.5	
3N23A	NPN	GP	Obsolete			30	5				35	12	10	4.5	
3N23B	NPN	GP	Obsolete			30	5				20	11	10	4.5	
3N23C	NPN	GP	Obsolete			30	5				10	9	10	4.5	
3N29	NPN	GE	Obsolete		50	6	20	85	100T		40T	10			
3N30	NPN	GE	Obsolete		50	6	20	85	100T		80T	10T			
3N31	NPN	GE	Obsolete		50	6	20	85	100T		80T	10T			
3N34	NPN	TI	Si RF		125	30	20	150	10	−.1	100T		.4	20	
3N35	NPN	TI	Si RF		125	30	20	150	10	−1.3	150T		.4	20	
3N36	NPN	GE	RF	6	30	6	20	85			50		10	7	3N36
3N37	NPN	GE	RF	6	30	6	20	85			90		10	7	3N37

T—Typical Values

ABBREVIATIONS

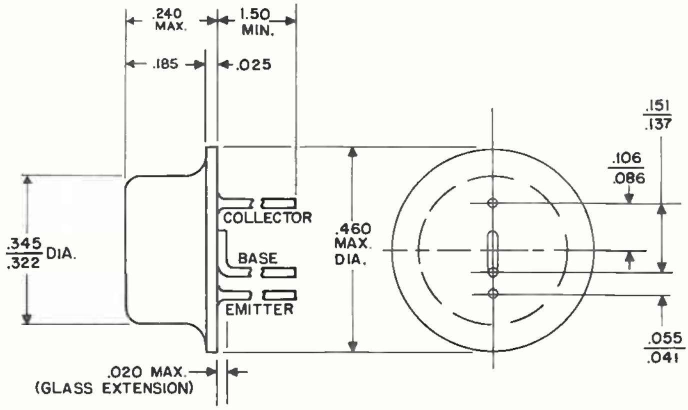
TYPES AND USES:

Si—Silicon High Temperature Transistors (all others germanium)
Pt—Point contact types
AF—Audio Frequency Amplifier and General Purpose
AF Out—High current AF Output
Pwr—Power output 1 watt or more
RF—Radio Frequency Amplifier
Osc—High gain High frequency RF oscillator
IF—Intermediate Frequency Amplifier
lo IF—Low IF (262 Kc) Amplifier
Sw—High current High frequency switch
AF Sw—Low frequency switch

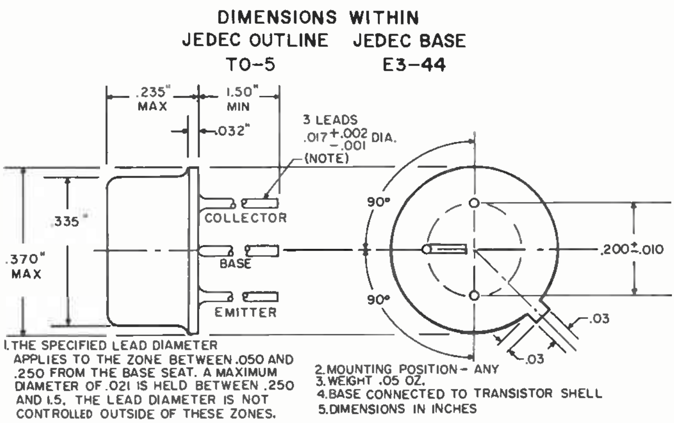
MANUFACTURERS:

Am—Amperex
AR—Advanced Research Associates, Inc.
Bendix—Bendix Aviation Corp.
CBS—CBS–Hytron.
Cle—Clevite Transistor Products.
Dlc—Delco Radio Div., General Motors Corp.
GE—General Electric Company.
GT—General Transistor Corporation.
GP—Germanium Products Corp.
Mall—P. R. Mallory and Company, Inc.
Mar—Marvelco, National Aircraft Corp.
M-H—Minneapolis-Honeywell Regulator Co.
Motor—Motorola, Inc.
Mu—Mullard Ltd.
Phil—Philco.
Ray—Raytheon Manufacturing Company.
RCA—RCA.
Sprague—Sprague Electronics Company.
Syl—Sylvania Electric Products Company.
TI—Texas Instruments, Inc.
TS—Tung-Sol.
W—Westinghouse Electric Corp.
WE—Western Electric Company.

OUTLINE DRAWINGS



1



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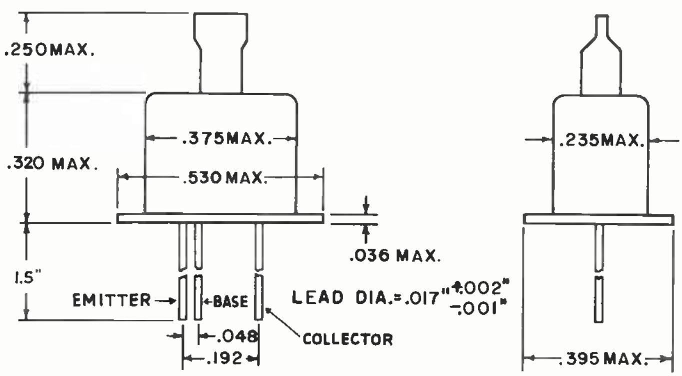


3

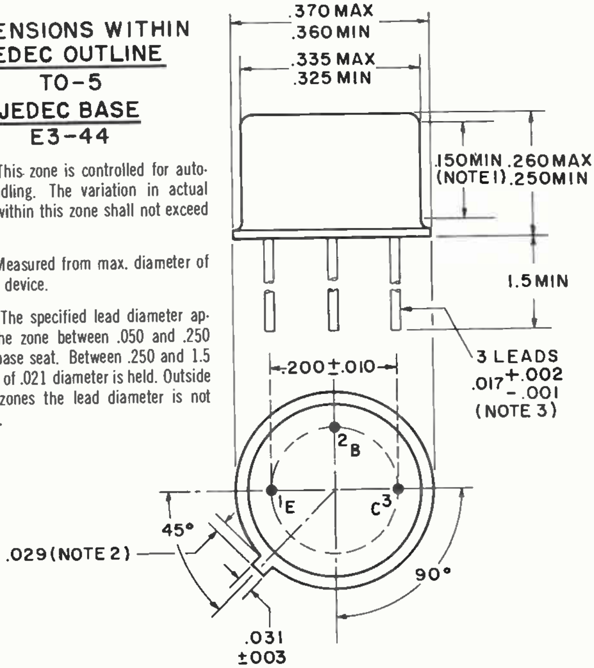
4

DIMENSIONS WITHIN JEDEC OUTLINE TO-5 JEDEC BASE E3-44

NOTE 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

NOTE 2: Measured from max. diameter of the actual device.

NOTE 3: The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and 1.5 maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled.



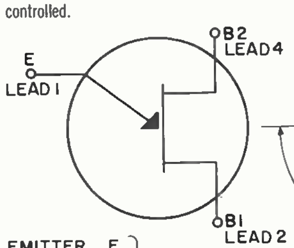
5

DIMENSIONS WITHIN JEDEC OUTLINE....TO-5 JEDEC BASE......E3-53

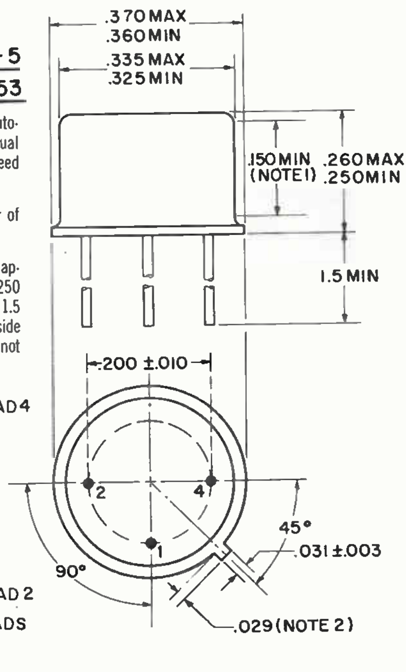
NOTE 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

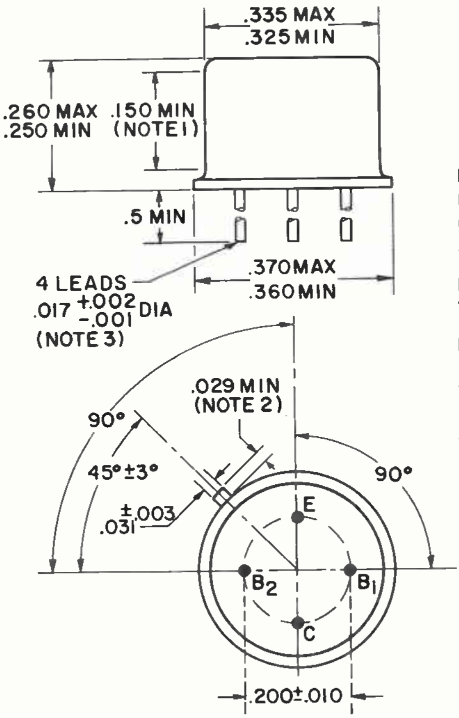
NOTE 2: Measured from max. diameter of the actual device.

NOTE 3: The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and 1.5 maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled.



EMITTER...E
BASE ONE..B1
BASE TWO..B2
} TINNED LEADS .017 +.002 -.001 (NOTE 3)





DIMENSIONS WITHIN JEDEC OUTLINE

TO-12

JEDEC BASE

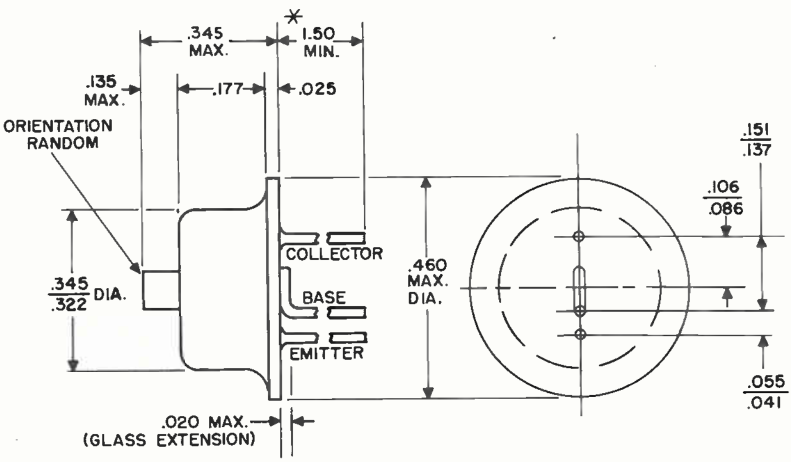
E4-54

NOTE 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

NOTE 2: Measured from max. diameter of the actual device.

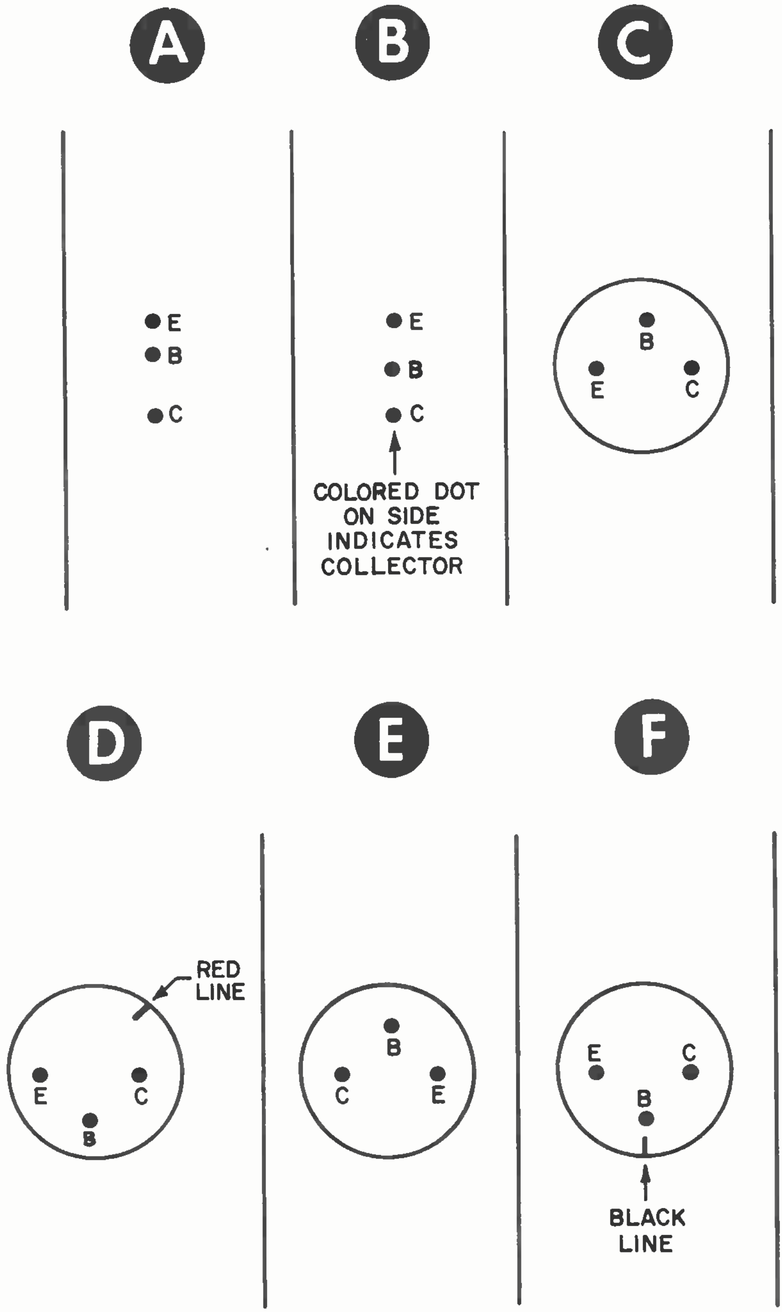
NOTE 3: The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and .5 maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled.

6



7

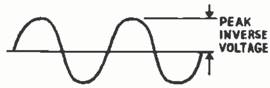
* CUT TO 0.200" FOR USE IN SOCKETS.
LEADS TINNED DIA. .018
MOUNTING POSITION – ANY
WEIGHT: .05 OZ.
BASE CONNECTED TO TRANSISTOR SHELL.
DIMENSIONS IN INCHES.


A
B
C
E
B
C
E
B
C
COLORED DOT
ON SIDE
INDICATES
COLLECTOR
B
E
C
D
E
F
RED
LINE
E
C
B
B
C
E
E
C
B
BLACK
LINE

18. RECTIFIER SPECIFICATIONS

NOTES ON RECTIFIER SPECIFICATION SHEET

The performance of a rectifier is judged primarily on four key measurements, or parameters. They are always given for specific ambient conditions, such as still air and 55°C, and are based on a 60 cycles per second (A-C) input with the rectifier feeding a resistive or inductive load (see Ⓐ below). A capacitive load will increase the Peak Inverse Voltage duty on the rectifier cell and will therefore necessitate a slightly lower set of ratings than shown here. These key parameters are:



60 CPS (CYCLES PER SECOND)
A-C INPUT

① **Maximum Peak Inverse Voltage** (usually referred to as PIV), the peak a-c voltage which the unit will withstand in the reverse direction; ② **Maximum Allowable D-C Output Current,** which varies with ambient temperature; ③ **Maximum Allowable One-cycle Surge Current,** representing the maximum instantaneous current which the rectifier can withstand, usually encountered when the equipment is turned on; ④ **Maximum Full-load Forward Voltage Drop,** measured with maximum d-c output flowing and maximum PIV applied. This is a measure of the rectifier's efficiency.

1N1692, 1N1693 1N1694, 1N1695

These alloy junction silicon rectifiers are designed for general purpose applications requiring maximum economy. These rectifiers are hermetically sealed and will perform reliably within the operating specifications.

RATINGS AND SPECIFICATIONS

Ⓐ ——— (60 CPS, Resistive or Inductive)

		1N1692	1N1693	1N1694	1N1695	
①	Max. Allowable Peak Inverse Voltage	100	200	300	400	volts
	Max. Allowable RMS Voltage	70	140	210	280	volts
	Max. Allowable Continuous Reverse DC Voltage	100	200	300	400	volts
②	Max. Allowable DC Output 100°C Ambient	250	250	250	250	ma
②	Max. Allowable DC Output 50°C Ambient	600	600	600	600	ma
③	Max. Allowable One Cycle Surge Current	20	20	20	20	amps
④	Max. Full Load Forward Voltage Drop (Full cycle average at 100°C)	.60	.60	.60	.60	volts
	Max. Leakage Current at Rated PIV (Full cycle average at 100°C)	0.5	0.5	0.5	0.5	ma
	Peak Recurrent Forward Current	2.0	2.0	2.0	2.0	amps
	Max. Operating Temperature	←	+ 115°C		→	

The other ratings or specifications are additional yardsticks of performance which are more or less critical depending on the operating conditions to be experienced. For instance, the 1N1692 Series for which specifications are shown, being silicon rectifiers, are able to show a higher range of *Ambient Operating Temperatures* with higher output than a germanium unit would, and are preferred on this basis for many applications. *Maximum Leakage Current* refers to the reverse current which will flow when voltage is applied, and here, too, can be a critical measure of performance for specific applications such as magnetic amplifiers.

Sometimes there is confusion as to whether a unit is a *Diode* or a *Rectifier*. Actually the word *Diode* means "two" and both rectifiers and diodes have two elements. However, rectifiers are capable of handling much larger currents than diodes. The term diode is used to describe units used in high frequency, low current, signal applications such as in high frequency circuits of television receivers.

CONDENSED RECTIFIER SPECIFICATIONS

RECTIFIER CELLS

JEDEC or G-E Type No.	PIV	Max. I_{DC} at T°C	Max. 1 Cycle (60 cps) Surge	Max. Oper. Temp. °C	Max. Storage Temp. °C
1N91	100	150ma at 55° amb.	25A	95°	105°
1N92	200	100ma at 55° amb.	25A	95°	105°
1N93	300	75ma at 55° amb.	25A	95°	105°
USN1N93	300	75ma at 55° amb.	25A	55°	85°
1N151	100	500ma at 55° amb.	25A	95°	105°
1N152	200	500ma at 55° amb.	25A	95°	105°
1N153	300	500ma at 55° amb.	25A	95°	105°
1N158	380	500ma at 55° amb.	25A	95°	105°
1N253	95	1000ma at 135° stud	4A	150°	150°
1N254	190	400ma at 135° stud	1.5A	150°	150°
1N255	380	400ma at 135° stud	1.5A	150°	150°
1N256	570	200ma at 135° stud	1.5A	150°	150°
1N315	100	100ma at 85° amb.	5A	85°	95°
USAF1N315	100	100ma at 85° amb.	5A	85°	100°
1N332	400	400ma at 150° stud	15A	170°	170°
1N333	400	200ma at 150° stud	10A	170°	170°
1N334	300	400ma at 150° stud	15A	170°	170°
1N335	300	200ma at 150° stud	10A	170°	170°
1N336	200	400ma at 150° stud	15A	170°	170°
1N337	200	200ma at 150° stud	10A	170°	170°
1N339	100	400ma at 150° stud	15A	170°	170°
1N340	100	200ma at 150° stud	10A	170°	170°
1N341	400	400ma at 150° stud	15A	170°	170°
1N342	400	200ma at 150° stud	10A	170°	170°
1N343	300	400ma at 150° stud	15A	170°	170°
1N344	300	200ma at 150° stud	10A	170°	170°
1N345	200	400ma at 150° stud	15A	170°	170°
1N346	200	200ma at 150° stud	10A	170°	170°
1N348	100	400ma at 150° stud	15A	170°	170°
1N349	100	200ma at 150° stud	10A	170°	170°
1N368	200	100ma at 85° amb.	10A	65°	85°

JEDEC or G-E Type No.	PIV	Max. I_{DC} at T°C	Max. 1 Cycle (60 cps) Surge	Max. Oper. Temp. °C	Max. Storage Temp. °C
1N606A	600	400ma at 100° amb.	10A	150°	175°
1N607	50	800ma at 135° stud	15A	150°	170°
1N607A	50	800ma at 135° stud	15A	150°	170°
1N608	100	800ma at 135° stud	15A	150°	170°
1N608A	100	800ma at 135° stud	15A	150°	170°
1N609	150	800ma at 135° stud	15A	150°	170°
1N609A	150	800ma at 135° stud	15A	150°	170°
1N610	200	800ma at 135° stud	15A	150°	170°
1N610A	200	800ma at 135° stud	15A	150°	170°
1N611	300	800ma at 135° stud	15A	150°	170°
1N611A	300	800ma at 135° stud	15A	150°	170°
1N612	400	800ma at 135° stud	15A	150°	170°
1N612A	400	800ma at 135° stud	15A	150°	170°
1N613	500	600ma at 135° stud	15A	150°	170°
1N613A	500	600ma at 135° stud	15A	150°	170°
1N614	600	600ma at 135° stud	15A	150°	170°
1N614A	600	600ma at 135° stud	15A	150°	170°
1N1095	500	425ma at 100° amb.	15A	150°	175°
1N1096	600	350ma at 100° amb.	15A	150°	175°
1N1100	100	500ma at 100° amb.	15A	165°	175°
1N1101	200	500ma at 100° amb.	15A	165°	175°
1N1102	300	500ma at 100° amb.	15A	165°	175°
1N1103	400	500ma at 100° amb.	15A	165°	175°
1N1115	100	1.5A at 85° stud	15A	170°	175°
1N1116	200	1.5A at 85° stud	15A	170°	175°
1N1117	300	1.5A at 85° stud	15A	170°	175°
1N1118	400	1.5A at 85° stud	15A	170°	175°
1N1119	500	1.5A at 85° stud	15A	170°	175°
1N1120	600	1.5A at 85° stud	15A	170°	175°
1N1487	100	250ma at 125° amb.	15A	140°	175°
1N1488	200	250ma at 125° amb.	15A	140°	175°
1N1489	300	250ma at 125° amb.	15A	140°	175°
1N1490	400	250ma at 125° amb.	15A	140°	175°

1N440	100	300ma at 100° amb.	15A	150°	175°
1N440B	100	500ma at 100° amb.	15A	165°	175°
1N441	200	300ma at 100° amb.	15A	150°	175°
1N441B	200	500ma at 100° amb.	15A	165°	175°
1N442	300	300ma at 100° amb.	15A	150°	175°
1N442B	300	500ma at 100° amb.	15A	165°	175°
1N443	400	300ma at 100° amb.	15A	150°	175°
1N443B	400	500ma at 100° amb.	15A	165°	175°
1N444	500	300ma at 100° amb.	15A	150°	175°
1N444B	500	425ma at 100° amb.	15A	150°	175°
1N445	600	300ma at 100° amb.	15A	150°	175°
1N445B	600	350ma at 100° amb.	15A	150°	175°
1N536	50	500ma at 100° amb.	15A	165°	175°
1N537	100	500ma at 100° amb.	15A	165°	175°
1N538	200	500ma at 100° amb.	15A	165°	175°
USAF1N538	200	500ma at 100° amb.	15A	150°	175°
1N539	300	500ma at 100° amb.	15A	165°	175°
1N540	400	500ma at 100° amb.	15A	165°	175°
USAF1N540	400	500ma at 100° amb.	15A	150°	175°
1N547	600	500ma at 100° amb.	15A	165°	175°
1N550	100	800ma at 135° stud	15A	150°	175°
1N551	200	800ma at 135° stud	15A	150°	175°
1N552	300	800ma at 135° stud	15A	150°	175°
1N553	400	800ma at 135° stud	15A	150°	175°
1N554	500	600ma at 135° stud	15A	150°	175°
1N555	600	600ma at 135° stud	15A	150°	175°
1N560	800	250ma at 100° amb.	15A	150°	175°
1N561	1000	250ma at 100° amb.	15A	150°	175°
1N562	800	400ma at 100° stud	15A	150°	175°
1N563	1000	400ma at 100° stud	15A	150°	175°
1N599	50	400ma at 100° amb.	10A	150°	175°
1N599A	50	400ma at 100° amb.	10A	150°	175°
1N600	100	400ma at 100° amb.	10A	150°	175°
1N600A	100	400ma at 100° amb.	10A	150°	175°
1N601	150	400ma at 100° amb.	10A	150°	175°
1N601A	150	400ma at 100° amb.	10A	150°	175°
1N602	200	400ma at 100° amb.	10A	150°	175°
1N602A	200	400ma at 100° amb.	10A	150°	175°
1N603	300	400ma at 100° amb.	10A	150°	175°
1N603A	300	400ma at 100° amb.	10A	150°	175°
1N604	400	400ma at 100° amb.	10A	150°	175°
1N604A	400	400ma at 100° amb.	10A	150°	175°
1N605	500	400ma at 100° amb.	10A	150°	175°
1N605A	500	400ma at 100° amb.	10A	150°	175°
1N606	600	400ma at 100° amb.	10A	150°	175°

1N1491	500	250ma at 110° amb.	15A	125°	175°
1N1492	600	250ma at 95° amb.	15A	120°	175°
1N1692	100	600ma at 100° amb.	20A	115°	125°
1N1693	200	600ma at 100° amb.	20A	115°	125°
1N1694	300	600ma at 100° amb.	20A	115°	125°
1N1695	400	600ma at 100° amb.	20A	115°	125°
1N2154	50	25A at 145° stud	300A	200°	200°
1N2155	100	25A at 145° stud	300A	200°	200°
1N2156	200	25A at 145° stud	300A	200°	200°
1N2157	300	25A at 145° stud	300A	200°	200°
1N2158	400	25A at 145° stud	300A	200°	200°
1N2159	500	25A at 145° stud	300A	200°	200°
1N2160	600	25A at 145° stud	300A	200°	200°
4JA60A*	100	84A at 120° stud	900A	200°	200°
4JA60B*	200	84A at 120° stud	900A	200°	200°
4JA60C*	300	84A at 120° stud	900A	200°	200°
4JA60D*	400	84A at 120° stud	900A	200°	200°
4JA60F*	50	84A at 120° stud	900A	200°	200°
4JA60G*	150	84A at 120° stud	900A	200°	200°
4JA60H*	250	84A at 120° stud	900A	200°	200°
4JA60J*	350	84A at 120° stud	900A	200°	200°
4JA62A*	100	40A at 120° stud	900A	150°	200°
4JA62B*	200	40A at 120° stud	900A	150°	200°
4JA62C*	300	40A at 120° stud	900A	150°	200°
4JA62D*	400	40A at 120° stud	900A	150°	200°
4JA62F*	50	40A at 120° stud	900A	150°	200°
4JA62G*	150	40A at 120° stud	900A	150°	200°
4JA62H*	250	40A at 120° stud	900A	150°	200°
4JA62J*	350	40A at 120° stud	900A	150°	200°

*Also available with reversed polarity.

RECTIFIER STACKS

G-E Type	PIV (up to)	Max. I_{DC} at T°C (up to)
4JA211	630 V	6 amps. at 55° amb.
4JA411	3360 V	18 amps. at 25° amb.
4JA3011	630 V	48 amps. at 55° amb.
4JA3511	1800 V	65 amps. at 55° amb.
4JA6011	840 V	573 amps. at 35° amb.
4JA6211	840 V	430 amps. at 35° amb.

19. NOTES ON CIRCUIT DIAGRAMS

TRANSFORMERS

The audio transformers used in these diagrams were wound on laminations of 1⅝" by 1⅜" and a ½" stack size, and having an electrical efficiency of about 80%. Smaller or less efficient transformers will degrade the electrical fidelity of the circuits.

OSCILLATOR COIL

Ed Stanwyck Coil Company #1265
Onondaga Electronic Laboratories #A-10047 or equivalent

VARIABLE CONDENSER

Radio Condenser Company Model 242
Onondaga Electronic Laboratories #A-10053 or equivalent

FERRITE ROD ANTENNA

Onondaga Electronic Laboratories #A-10067 or equivalent

If you are unable to obtain these components from either your local or a national electronic parts distributor, we suggest you contact:

Onondaga Electronic Laboratories
Box 8
Syracuse 11, N. Y.

20. READING LIST

The following list of semiconductor references gives texts of both elementary (E) and advanced (A) character. Obviously, the list is not inclusive, but it will guide the reader to other references.

Dewitt, D., Rossoff, A. L., *Transistor Electronics* (A), 1957, 381P (McGraw-Hill)

Garner, L., *Transistor Circuit Handbook* (E), 1956, 430P (Coyne)

Hunter, L. P., *Handbook of Semiconductor Electronics* (A), 1956, 633P (McGraw-Hill)

Hurley, R. B., *Junction Transistor Electronics* (A), 1958, 473P (Wiley)

Kiver, M. S., *Transistors in Radio and Television* (E), 1956, 302P (McGraw-Hill)

Lo, A. W., Endres, R. O., Zawels, J., Waldhauer, F. D., Cheng, C. C., *Transistor Electronics* (A), 1955, 521P (Prentice-Hall)

Shockley, W., *Electrons and Holes in Semiconductors* (A), 1950, 558P (Van Nostrand)

Shea, R. F., et al., *Principles of Transistor Circuits* (A), 1953, 535P (Wiley)

Shea, R. F., *Transistor Circuit Engineering* (A), 1957, 468P (Wiley)

Spenke, E., et al., *Electronic Semiconductors* (A), 1958, 379P (McGraw-Hill)

Turner, R. P., *Transistors — Theory and Practice* (E), 1954, 160P (Gernsback)

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