

electronics today

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Over
100
pages

**SOUND LEVEL
METER** – first ever
magazine project!
Build it in an
evening!



MPU Support –
the chips are down
Dolby C –
a new noise reduction system
IR Beam Alarm project

**FREE INSIDE
DIGITAL DESIGN
SUPPLEMENT**
all you ever wanted to know
and more...

NEWS...PROJECTS...MI

...AUDIO

When the LEDs are in place, carefully interwire them (on the top side of the PCB) to conform to the main circuit diagram and then make the 10 connections to IC2 (from the underside of the PCB) and the four connections to Q2-Q5 on the main PCB. At this point, wire the two toggle switches and the push-button switch into place, fit the transducer, connect the battery and give the unit a functional test. If the LEDs fail to illuminate correctly, re-check your interwiring.

When all is well, you can fit the two PCBs, etc. into a suitable case. Drill a circle of 37 holes in the top of the case, to coincide with the 37 LEDs and fit the push-button switch in the centre of the circle. The display board can be secured behind the case top by smearing drops of clear adhesive on the sides of the heads of a few of the LEDs and pushing them into the case holes. The project can be finished off by either marking the

roulette wheel artwork on top of the case by hand or by rubbing down a special ETIprint that we have prepared. Note that the numbers marked on the roulette scale do not, in fact, have to coincide with any particular LED numbers.

BUYLINES

Your local component shop should be able to provide you with all the components needed to build the ETI Roulette game. In case of difficulty Ambit International, who advertise with us, will supply the PB-2720 transducer.

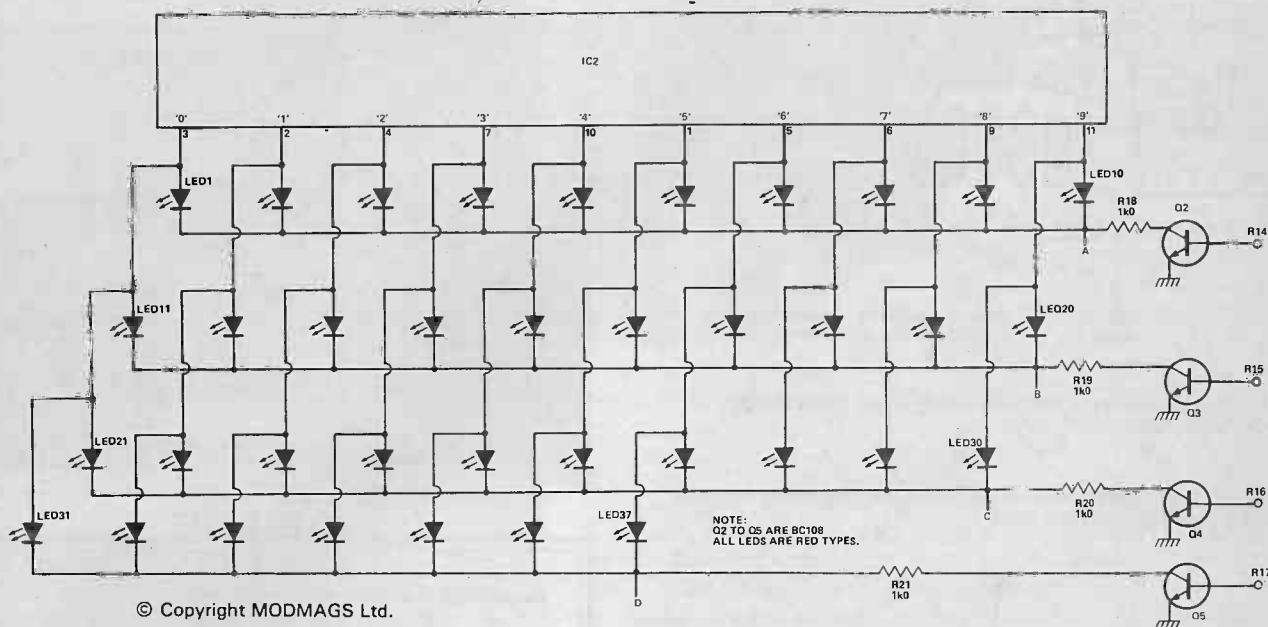


Fig. 2 LED display circuitry.

HOW IT WORKS

The circuit comprises a clock generator (IC1-Q1) and a multi-stage counter/decoder network (IC2-IC3-IC4) that drives a circle of up to 37 LEDs in the dot mode. The counter/decoder network is deceptively simple. CD4017 decade counter/decoders IC2 and IC3 are wired in series so that IC2 counts in units and IC3 counts in tens when the clock signal is fed to pin 14 of IC2. The '3' output of IC3 and the '6' or '7' output of IC2 are NANDed via IC4d and used to trigger monostable IC4b-IC4c, which generates a 16 μ s pulse and resets both counters to zero via IC4a each time that these two outputs go high simultaneously. The cascaded counters thus divide the clock signal by a fixed ratio of 36 or 37 (depending on the setting of SW1) and effectively produce 36 or 37 fully decoded outputs, which are used to sequentially turn on LEDs in the roulette ring or wheel.

The LED ring comprises three segments of 10 LEDs and one segment of seven LEDs. The anode drive to all LEDs is controlled by IC2 (the units counter), but the cathode paths of the LEDs are controlled by IC3 (the tens counter) via transistors Q2 to Q5. Thus, on the '15' count the '5' output of IC2 goes high and Q3 is driven on via the '1' output of IC3, so that only LED 15 illuminates. This multiplexing technique enables the 37 LEDs to be driven by fairly simple counter/decoder circuitry, which turns the LEDs on sequentially and produces an apparently-rotating ring of light.

The clock generator circuitry is delightfully cunning and is

designed around the VCO section of a 4046B phase-locked loop chip. The frequency of this oscillator is controlled by the value of C2, the resistance between pin 11 and ground and the voltage on pin 9. Slight bias is applied to the VCO by R7 to ensure that the VCO frequency falls to zero when the pin-9 voltage is reduced to zero. The output of the VCO is available at pins 3-4 and is fed directly to the input of IC2 and by R10 to the transducer (Tx), which produces a click sound each time a clock transition is generated.

The VCO circuit operates as follows. When PB1 is closed, pin 9 of IC1 is pulled high via D1-R4 (thus charging C1 to maximum voltage) and Q1 is turned on by DR-R5, thus connecting R8 between pin 11 of IC1 and ground. Under this condition the VCO operates at a few tens of kilohertz and causes the LED display to appear to spin at a rate of several hundred revs per second, so that the number of spins cannot be predicted by PB1.

When PB1 is released Q1 turns off, so that only R9 is connected between pin 11 and ground and C1 abruptly discharges to half-supply volts through D3-R2. Under this condition the wheel rotates at an initial visible rate of about two revs/sec. From this moment, C1 discharges exponentially through R3, so the pin-9 voltage and the wheel spin rate steadily decrease until, after about 15 s, the VCO stops generating and the wheel comes to rest. The operating sequence is then complete.

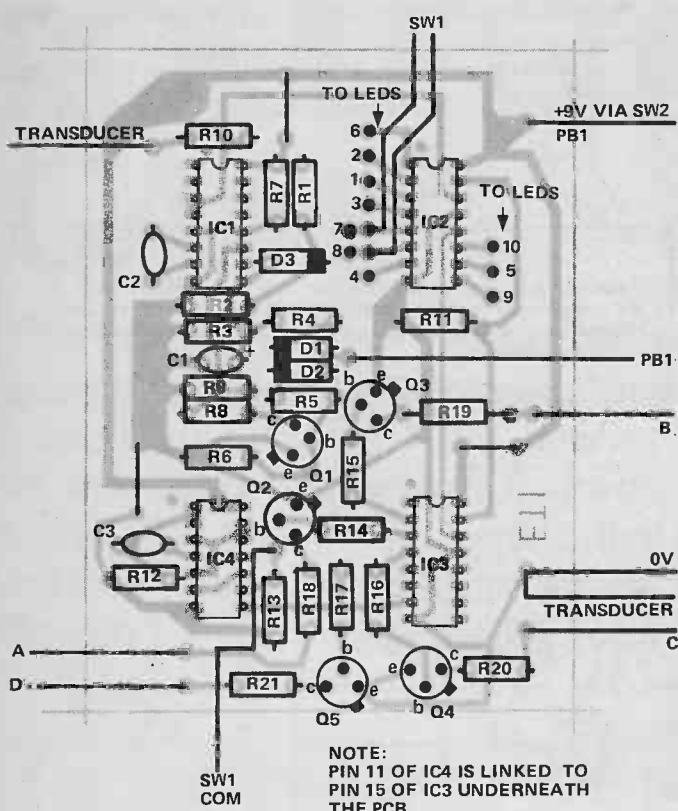


Fig. 3 Component overlay of the main circuit board. Don't forget the under-board link.

Inside the box (right). Construction of the front panel LED display is greatly simplified by our LED board (see Fig.4).

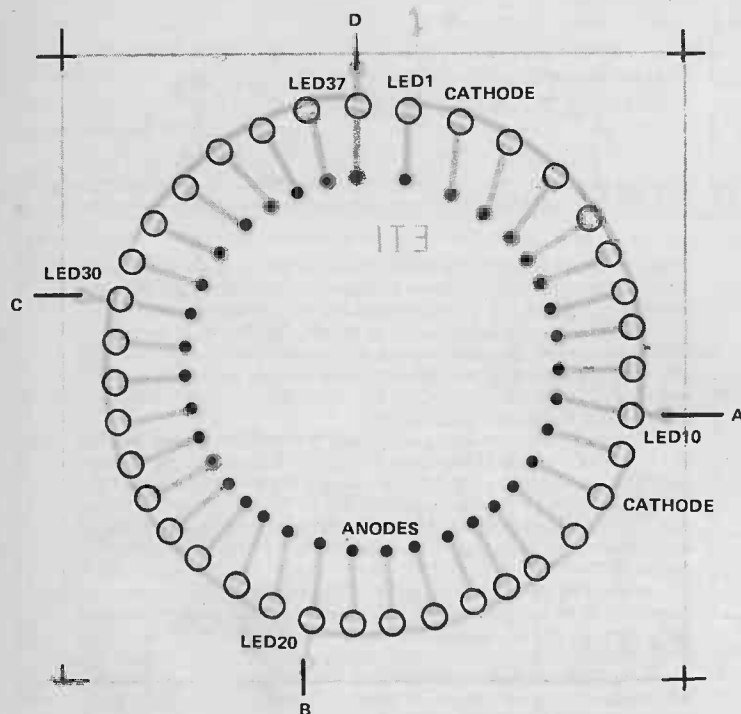
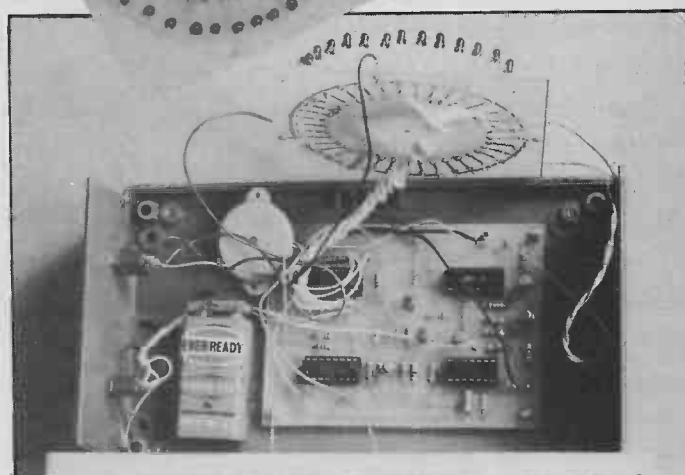
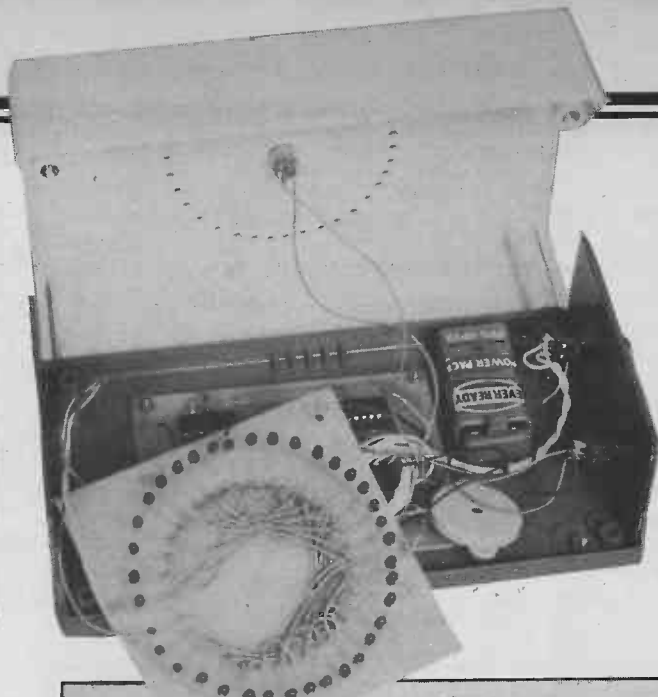


Fig. 4 Component overlay for the LED display.



PARTS LIST

Resistors all 1/4 W 5%

| | |
|-----------------|------|
| R1, 2 | 6k8 |
| R3, 9 | 1M0 |
| R4 | 470R |
| R5, 6 | 47k |
| R7 | 10M |
| R8 | 10k |
| R10 | 820R |
| R11 | 100k |
| R12 | 27k |
| R13 | 270k |
| R14, 15, 16, 17 | 12k |
| R18, 19, 20, 21 | 1k0 |

Capacitors

| | |
|----|-------------------|
| C1 | 10u 35 V tantalum |
| C2 | 10n polycarbonate |
| C3 | 1n0 polycarbonate |

Semiconductors

| | |
|----------------|-----------------------|
| IC1 | CD40468B |
| IC2, 3 | CD4017B |
| IC4 | CD4011B |
| Q1, 2, 3, 4, 5 | BC108 |
| D1, 2, 3 | 1N4148 |
| LED1-37 | 0.125" diameter (Red) |

Miscellaneous

| | |
|-----------------------|---|
| PB1 | momentary push button Vero case (order code 202-21031G) |
| SW1, 2 | SPDT miniature toggle |
| 1 off PP3 9 V battery | |
| Tx1 PB-2720 | |

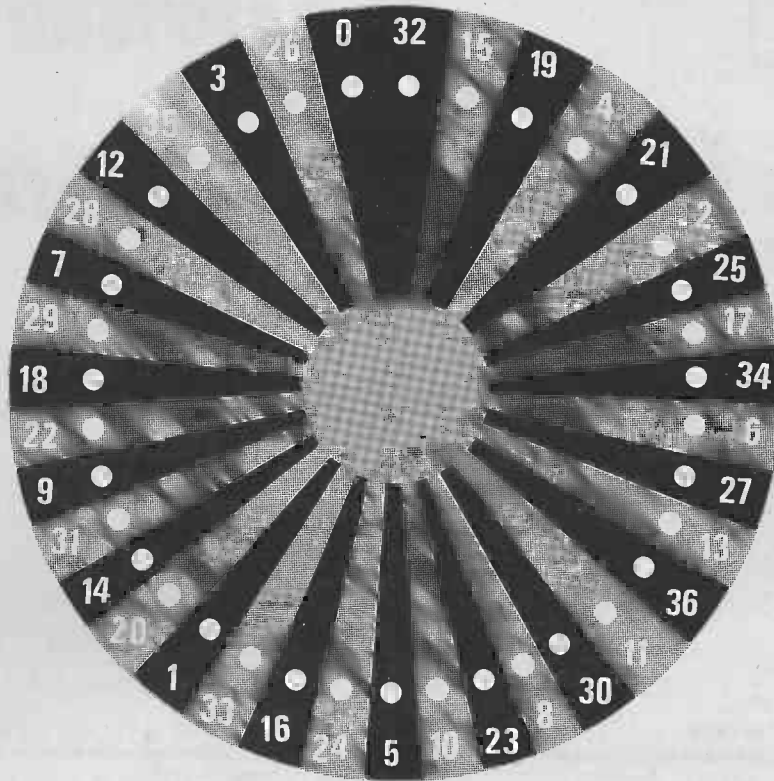


Fig. 5 Design for the 37 LED display.

| | | | | |
|---------------|-------|-----------|-----------|-----------|
| | | 0 | | |
| | | 1 | 2 | 3 |
| | | 4 | 5 | 6 |
| | | 7 | 8 | 9 |
| | | 10 | 11 | 12 |
| HIGH 19-36 | | 13 | 14 | 15 |
| | | 16 | 17 | 18 |
| | | 19 | 20 | 21 |
| | | 22 | 23 | 24 |
| | | 25 | 26 | 27 |
| | | 28 | 29 | 30 |
| | | 31 | 32 | 33 |
| | | 34 | 35 | 36 |
| 1-12 | 13-24 | 25-36 | 36-25 | 24-13 |
| | | COLM 1 | COLM 2 | COLM 3 |

BLACK

RED

EVEN

ODD

BETTING ODDS:

- 35:1 ANY SINGLE NUMBER
- 17:1 ANY TWO ADJACENT NUMBERS ON THE TABLE
- 11:1 ANY THREE HORIZONTALLY ADJACENT NUMBERS ON THE TABLE
- 8:1 ANY FOUR ADJACENT NUMBERS ON THE TABLE
- 5:1 ANY TWO ADJACENT HORIZONTAL ROWS ON THE TABLE
- 2:1 ANY OF THE SIX INDICATED BLOCKS OR COLUMNS OF 12 NUMBERS
- 1:1 HIGH, LOW, EVEN, ODD, BLACK OR RED

| | | |
|----|----|----|
| 4 | 5 | 6 |
| 7 | 8 | 9 |
| 10 | 11 | 12 |
| 13 | 14 | 15 |
| 16 | 17 | 18 |

- A. A BET ON A SPECIFIC NUMBER. (ODDS 35:1)
- B. A BET ON TWO ADJACENT TABLE NUMBERS (ODDS 17:1)
- C. A BET ON THREE HORIZONTALLY ADJACENT TABLE NUMBERS (ODDS 11:1)
- D. A BET ON FOUR ADJACENT TABLE NUMBERS (ODDS 8:1)
- E. A BET ON TWO ADJACENT ROWS OF TABLE NUMBERS (ODDS 5:1)

Fig. 6 Table layout and details of the betting odds.

Fig. 7 There's more than one way of placing a bet.

DOLBY C - REVOLUTION OR REHASH?

Ian Graham reports on the next generation of noise reduction systems from Dolby Laboratories — Dolby C.

If you're in the habit of reading the blurb on tape cassettes, then you're already familiar with the double D trademark of Dolby Laboratories. Perhaps you even have a posh tape deck with a Dolby selector switch. The system universally used in consumer hi-fi now is Dolby B, providing 10 dB of noise reduction above about 4 kHz. Tape noise has already been reduced a great deal — try listening to your favourite Osmonds tape with the Dolby system switched out. The noise tends to destroy the full esoteric impact of Little Jimmy's lethal lyrics. Come to think of it.

A, B, C,

Dolby C, as the new system is called, will provide 20 dB of noise reduction above about 1 kHz (Fig. 1). The obvious question is — is it just a stretched version of Dolby B? The operation of the two systems is certainly similar. Dolby C uses existing B-type chips. However, a stretched Dolby B giving 20 dB reduction was found to be impractical. The subjectively much cleaner high frequencies revealed a muddy mid-frequency band at higher listening levels. Hence, the new C-type design achieves its full 20 dB reduction above about 1 kHz. It reaches the maximum B-type reduction of 10 dB at only 300 Hz, offering (subjectively) uniform noise reduction across the whole audio band.

Design Points

If you already know how Dolby B works, then the new system holds few surprises for you. In principle, lower level high frequencies are selectively boosted just before the signal is recorded onto the tape. When the encoded tape is played back, the boosted frequencies are attenuated back to where they were originally, reducing the noise added by the recording process.

Signal processing is tackled in two stages in series, each supplying 10 dB of compression during recording and of expansion during playback (Fig. 2). The high level stage (Fig. 3) is sensitive to signals at about the same levels as are processed by a Dolby B network. The low level stage deals with signals in the previously unprocessed frequencies below the Dolby B region. Although the two stages are working together, at no time is a signal subjected to a full 20 dB compression or expansion with its accompanying undesirable side effects and inaccurate signal control.

Noise News

In addition, the C-type system incorporates a number of further innovations. Two are shown in Fig. 3. The anti-saturation and spectral skewing networks are frequency response modifications to reduce encode/decode errors, upper-middle and high frequency losses and intermodulation distortion. The end result is a new noise reduction system which is at least as free of side effects as the B-type system and just as practical in everyday use.

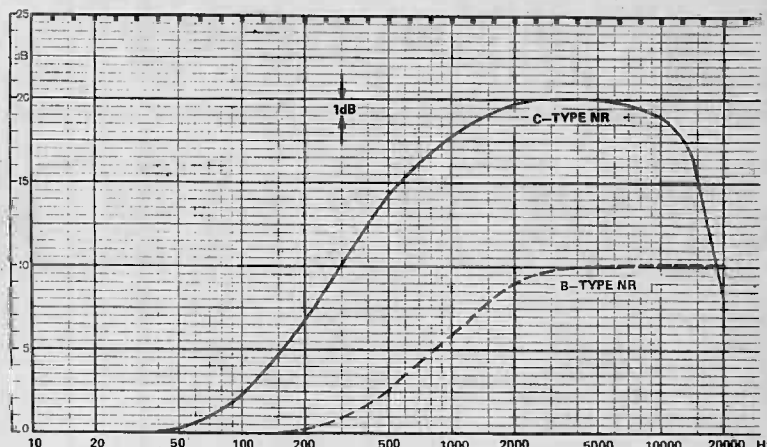
Compatibility

There's no point in producing a new noise reduction system if it is not compatible with existing tapes and hardware, so Dolby C has been designed with the universal use of Dolby B in mind. Recordings made using a C-type processor can be replayed on a B-type cassette machine with acceptable results and on machines without any noise reduction system. So, you don't have to rush out and buy a new tape deck tomorrow. Prototype C-type machines have already been on show across the Atlantic, so production models from all the major hi-fi manufacturers shouldn't be far behind. Because one half of the new system is essentially a B-type processor, tape decks can easily incorporate push-button selection of either B or C-type processing. Perhaps the first generation of cassette machines will feature this until Dolby C is as universal in use as its predecessor. Professional C-type encoders are being produced, so C-encoded cassettes will be available in the shops too. Dedicated Dolby C chips should be in production in about a year.

How Much?

Good question. Dolby C is about 2½ times as complex as existing B-type circuitry, so, in terms of component cost only, a C-type NR processor will be about 2½ times as expensive as existing units. In addition, Dolby C demands first class electrical and mechanical performance from the recorder incorporating it, including very low noise levels in the circuitry surrounding the processor. I guess you've heard the moral before — it pays to buy the best you can afford. The new system will be most useful for recording material of a wide dynamic range to be replayed at very loud listening levels.

Fig. 1 These curves show the maximum low level boost imparted by both C-type and B-type noise reduction in the absence of high frequency signals. Dolby C NR imparts more boost in recording and more cut in playback, thus providing more noise reduction. The effect also extends about two octaves lower with the C-type NR to maintain subjectively uniform noise levels across the spectrum. Processing at very low frequencies is not required with either system because low frequency noise is insignificant in properly engineered cassette recorders.



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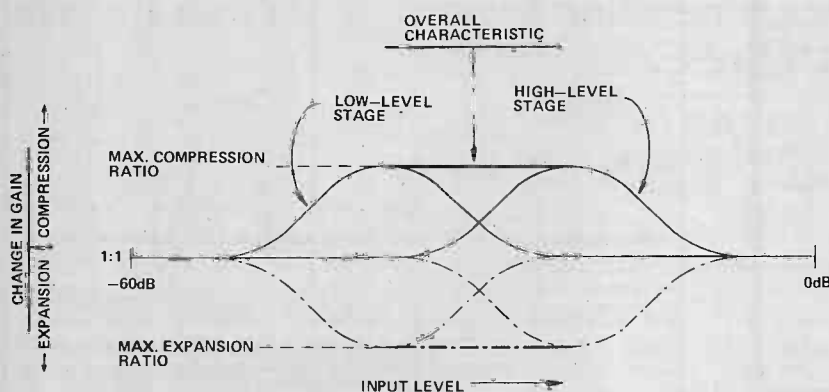
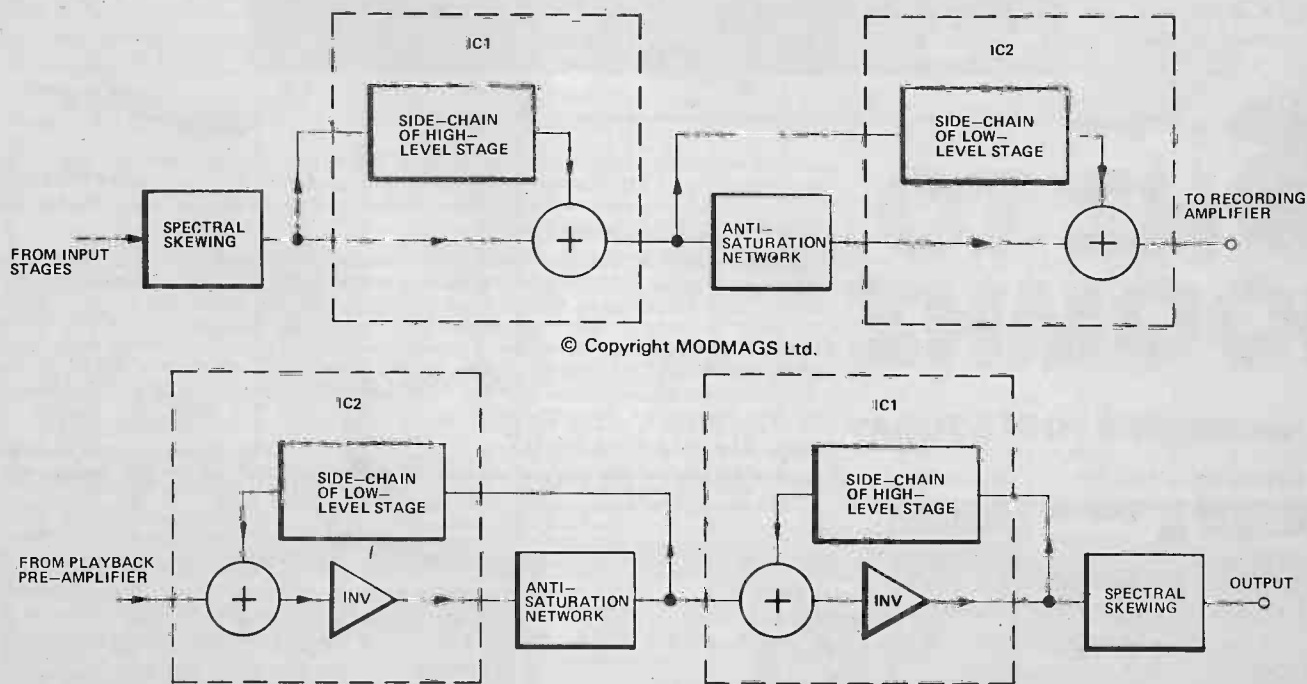


Fig. 2 The two-level, two-stage configuration. At no time is the signal subject to significantly more than the maximum compression or expansion effect of a single stage. Yet the effects of the two stages multiply (add in decibels) to achieve the full 20 dB of processing required for C-type noise reduction.

Revolution Or Rehash?

The truth probably lies somewhere between the two extremes. Dolby C represents the next stage in the evolution of noise reduction. It employs a new approach (dual level processing) to noise reduction yet it is fully compatible with existing tapes and hardware.

Fig. 3 Block diagram of the Dolby C noise reduction system showing the encoder (below) and decoder (bottom).



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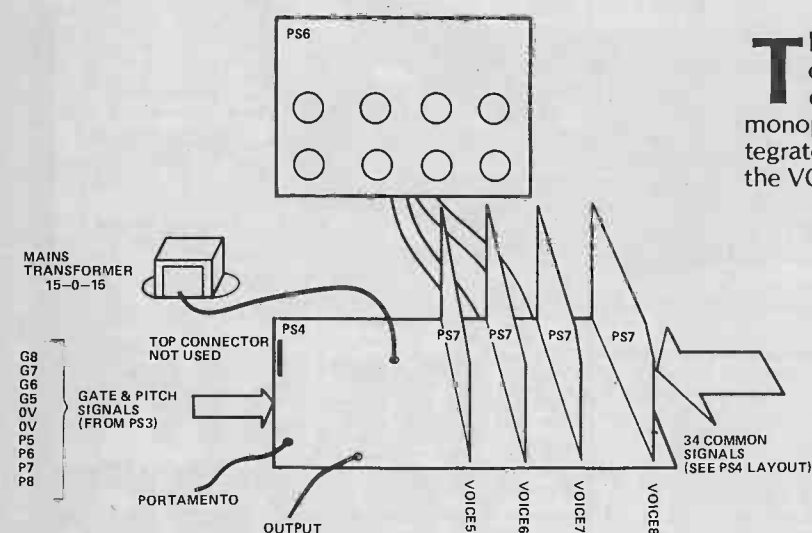
ETI

POLYSYNTH



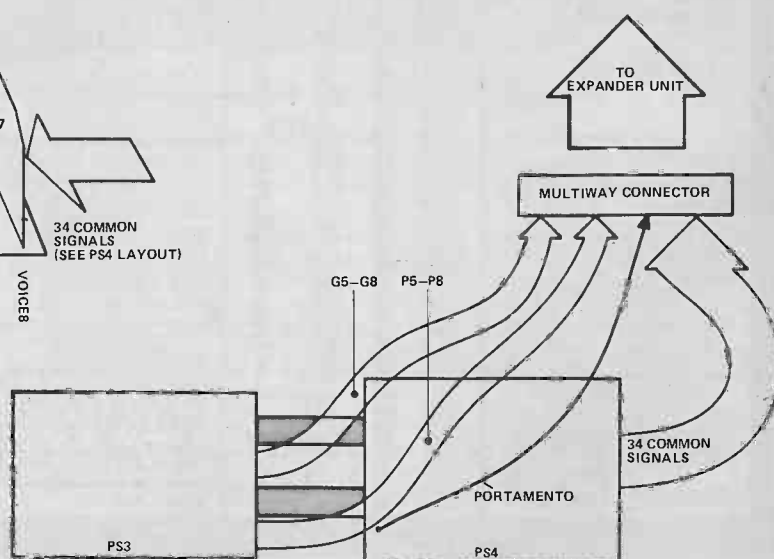
Part 3 of the Polysynth describes the voice boards and power supply, and shows how the four-voice expander unit may be built from the basic boards. Design and development by Tim Orr.

The Polysynth can generate up to four individual voices or eight voices when using the expander unit. Each voice contains the equivalent electronics of a medium-sized monophonic synthesiser. Dedicated music synthesiser integrated circuits have been used to enable voltage control of the VCO and ADSR units.



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Fig.1 (Above) Block diagram showing the boards and connections needed for the four-voice expander unit.



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Fig.2 (Right) The control signals for the expander are taken from the Polysynth via a multiway connector.

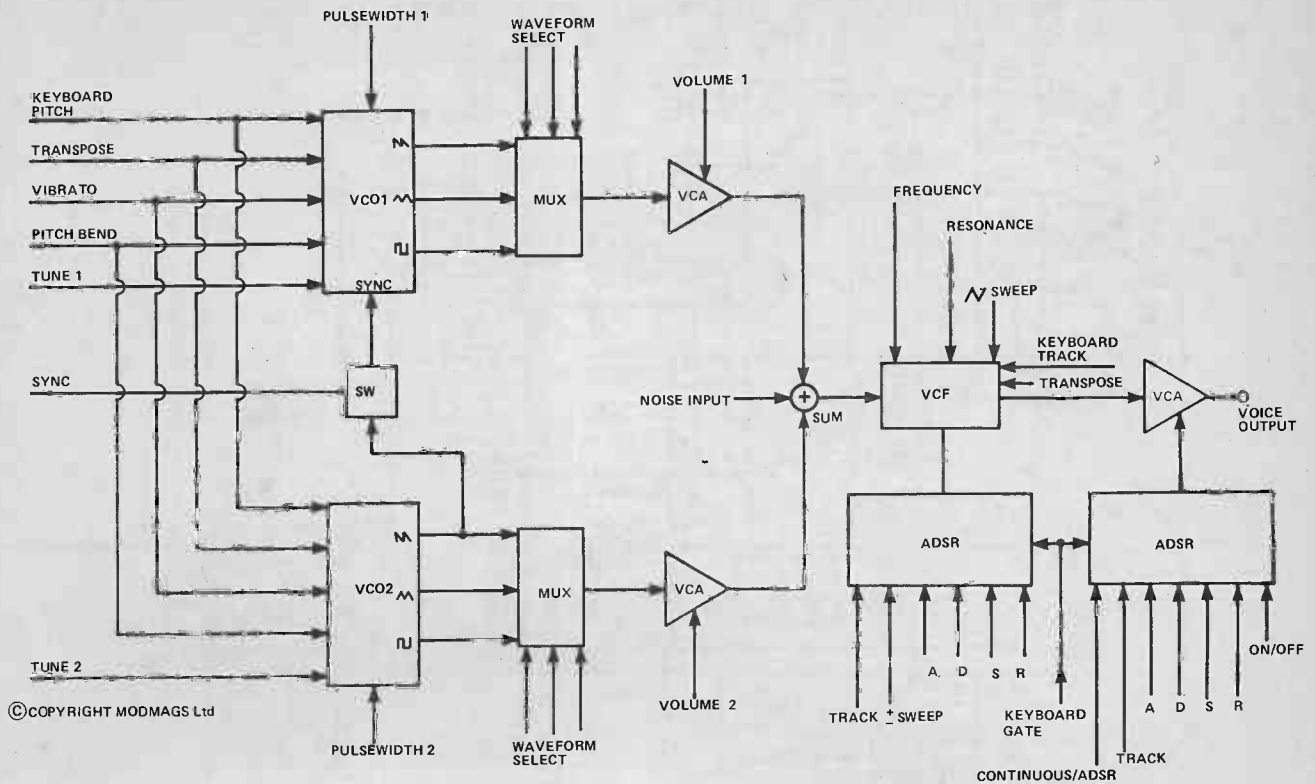


Fig.3 Block diagram of one voice of the Polysynth (PS7).

Expander Unit

In order to play eight voices, an expander unit is needed. (Fig. 1). It is self-powered and consists of a PS4 mother board, four PS7 voice boards, a PS6 panel board and a mains transformer. The tuning and alignment is exactly the same as for the first four voices. The expander unit is driven from a large multiway connector (Fig. 2). All 34 common signals plus the portamento are wired up on a one-to-one basis, that is vibrato to vibrato, transpose to transpose, etc. The independent pitch and gate signals are obtained separately from PS3 (don't forget to insert the extra sample and hold ICs on PS3). The output of the expander unit and the Polysynth have to be mixed externally.

BUYLINES

Powertran Electronics can supply a complete kit of parts for each option of the Transcendent Polysynth.

| | |
|-----------------------|------|
| 1 voice | £320 |
| 2 voices | £368 |
| 3 voices | £464 |
| 4 voice expansion kit | £295 |

All prices are exclusive of VAT. Powertran Electronics, Portway Industrial Estate, Andover, Hants SP10 3NM.

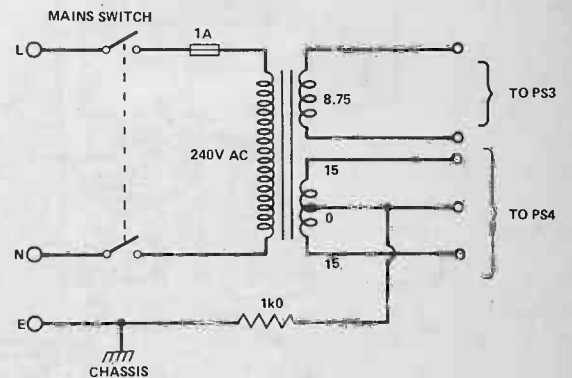
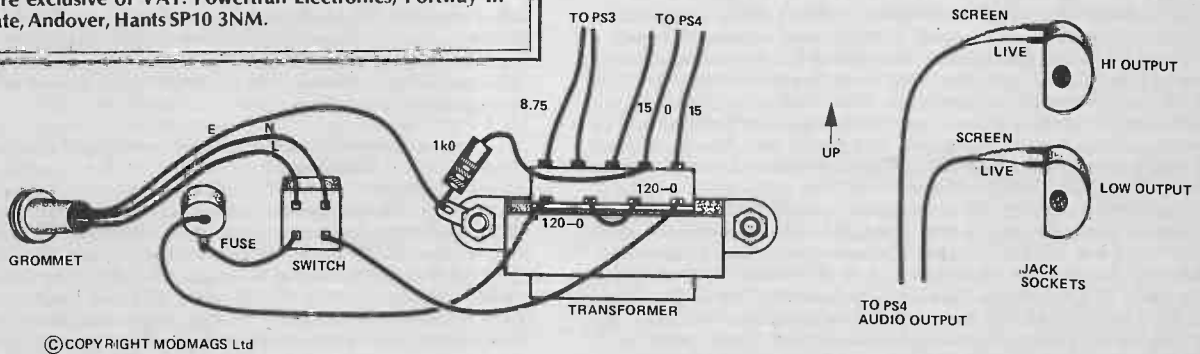


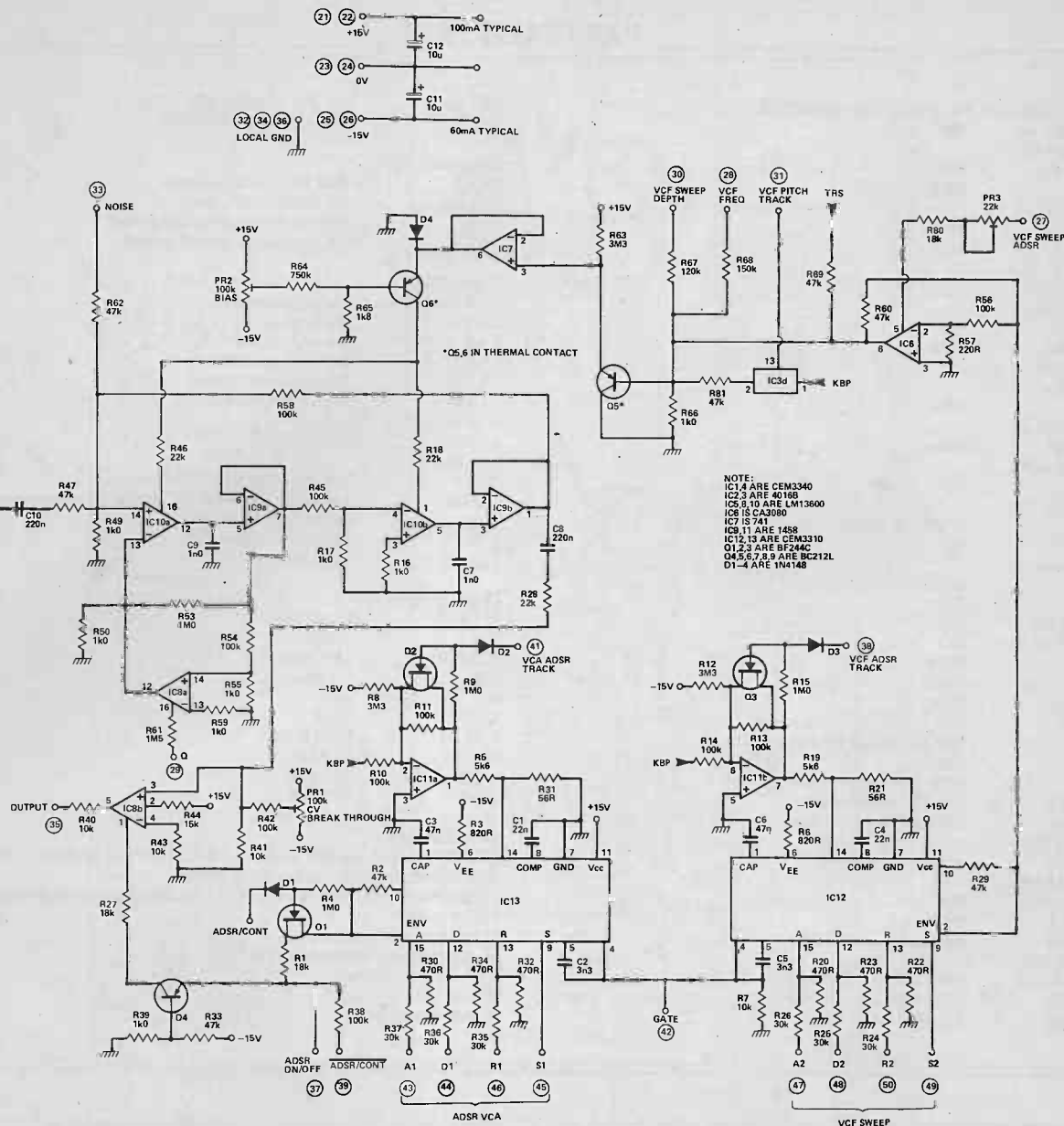
Fig.4 Circuit diagram of the power supply.

Fig.5 Wiring details for the components that mount on the back panel.





An analogue switch (IC2,3) is used to select the output waveforms from the VCOs. These signals are fed to IC5 which is used as a voltage-controlled amplifier. The VCO outputs are mixed together and fed into the VCF. This is known as a two-pole state variable lowpass filter with exponential frequency control and voltage-controlled resonance (Fig. 6). Two OTAs (IC10) are used as variable gain integrators. The gain is linearly proportional to the I_{ABC} current flowing into pins 1 and 16 of IC10. The filter cut-off frequency is linearly proportional to this gain. Therefore, a change in the I_{ABC} current will result in a similar change in the VCF frequency. Transistors Q5,6 convert the transpose, keyboard, frequency pot and sweep voltages into an I_{ABC} current (the



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Fig.6 Complete circuit diagram for one voice of the Polysynth (PS7). The ringed numbers refer to the edge connector sockets (see Fig.7).

collector current of Q6) which is exponentially proportional to the sum of these as seen at the base of Q5. IC8 (pins 12, 13, 14, 16) is used to voltage-control the Q factor of the filter. When the I_{ABC} current to this device (pin 16) is zero, the Q factor is determined by R50 and R53, resulting in a high Q response. IC8 provides a negative feedback route so that as its I_{ABC} current is increased, more negative feedback is applied. This damps the filter which lowers the Q factor.

It is possible to sweep the filter with an ADSR waveform via IC6. When the ADSR sweep pot (molex pin number 27) is at 0 V, PR3 is adjusted so that an ADSR waveform produces no movement at IC6, pin 6. When the ADSR sweep pot is then set to -15 V, IC6 is turned off and so an ADSR waveform will generate a positive change at pin 6 via resistor R60. When the ADSR pot is set to +15 V, IC6 is turned fully on and so the ADSR waveform generates a negative change at pin 6.

This circuit generates the characteristic synthesiser-swept filter sound.

There are two ADSR units, IC12, 13. These are Curtis CEM3310 devices. They have a 50,000:1 time-constant control range, with voltage control of all parameters and a true RC exponential envelope shape. Also, the voltage control of the time-constants is exponential. Every 18 mV increase at pins 15, 12 and 13 halves the A, D and R time-constants respectively. The time-constants of the ADSR units can also be transposed by injecting a voltage at pin 14. A +18 mV increase at this point will double the time-constants. All natural instruments have attack and decay times that are frequency-related. The top note on a piano dies away very quickly but the bottom note continues for a long time. It is possible to simulate this in the voice unit by injecting the keyboard pitch voltage into pin 14 of the CEM3310. This ADSR pitch tracking may be turned off by using FETs Q2 and Q3 to short out the keyboard pitch voltage.

IC12 is used to provide a sweep voltage for the VCF; IC13 generates the amplitude envelope for the output VCA (IC8 pins 1, 2, 3, 4, 5).

PARTS LIST : PS7

Resistors all 1/4 W 5% unless otherwise stated

| | |
|--|----------------------|
| R1,27,80 | 18k |
| R2,33,47,60,62,102 | 22k |
| R3,6 | 820R |
| R4,9,15,53,78,109 | 1M0 |
| R5,19 | 5k6 |
| R7,40,41,43,51,74,85,88,97,100,105,119 | 10k |
| R8,12,63 | 3M3 |
| R10,11,13,14,38,42,45,54,56,58 | 100k |
| R16,17,39,49,50,55,59 | 1k0 |
| R18,28,46,93,99 | 22k |
| R20,22,23,30,32,34 | 470R 2% metal oxide |
| R21,31 | 56R |
| R24,25,26,35,36,37 | 30k 2% metal oxide |
| R29 | 4k7 |
| R44,90,91 | 15k |
| R48,52,89,92 | 2k2 |
| R57 | 220R |
| R61,77,116 | 1M5 |
| R64 | 750k |
| R65 | 1k8 |
| R66 | 1k0 2% metal oxide |
| R67 | 120k |
| R68 | 150k 2% metal oxide |
| R69,81 | 47k 2% metal oxide |
| R70,108 | 332k 0.5% metal film |
| R71,82,101,115 | 470R |
| R72,73,94,95,96,98 | 68k |
| R75,114 | 10M |
| R76,112 | 100k 0.1% metal film |
| R79,84,104,110,111,118 | 1M0 2% metal oxide |
| R83,103 | 1k82 0.5% metal film |
| R86,106 | 22k 2% metal oxide |

| | |
|----------|----------------------|
| R87,107 | 5k6 2% metal oxide |
| R113,117 | 100k 0.1% metal film |

Potentiometers

| | |
|---------|-------------------------------|
| PR1,2 | 100k horizontal preset |
| PR3,5,6 | 22k horizontal preset |
| PR4,7 | 100k cermet horizontal preset |
| PR8,9 | 10k multiturn cermet preset |

Capacitors

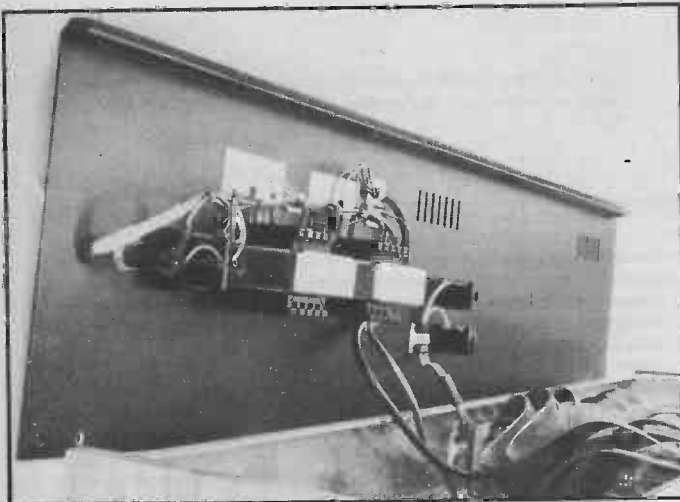
| | |
|--------------------------|--|
| C1,4 | 22n polycarbonate |
| C2,5 | 3n3 ceramic |
| C3,6 | 47n polycarbonate |
| C7,9 | 1n0 polycarbonate |
| C8,10 | 220n polycarbonate |
| C11,12 | 10u 16 V tantalum |
| C13,15,17,19,24,27,30,31 | 10n ceramic |
| C14,16,21,22,28,29 | 1u0 35 V tantalum |
| C18,26 | 1n0 polycarbonate (or Mullard ceramic multilayer for higher stability) |
| C20,25 | 100n polycarbonate |
| C23 | 220p ceramic |

Semiconductors

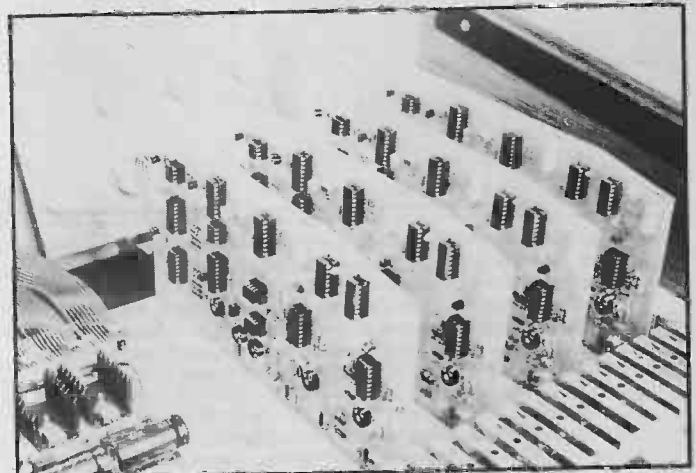
| | |
|--------------|---------|
| IC1,4 | CEM3340 |
| IC2,3 | 4016B |
| IC5,8,10 | LM13600 |
| IC6 | CA3080 |
| IC7 | 741 |
| IC9,11 | 1458 |
| IC12,13 | CEM3310 |
| Q1,2,3 | BF244C |
| Q4,5,6,7,8,9 | BC212L |
| D1-4 | 1N4148 |

Miscellaneous

PCB PS7, 4 off 8 pin DIL sockets, 2 off 14 pin DIL sockets, 7 off 16 pin DIL sockets, 5 off 10-way Molex sockets.
Transformer with 16-0-16 and 0-8.75 tapings (Powertran special)
Mains switch
Mains lead and grommet
20 mm fuse and fuseholder (1 A)
2 off 1/4" jack sockets
1k0 resistor
36 instrument knobs



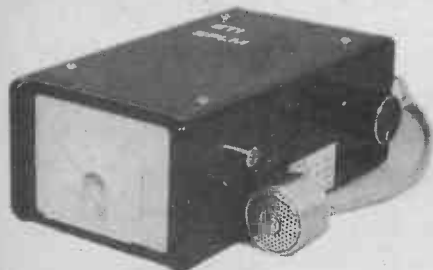
Above: prototype back panel. Production models may differ.
Right: the voice boards plug directly into the mother board.



Next month: We conclude the Polysynth project with full setting up and test details.



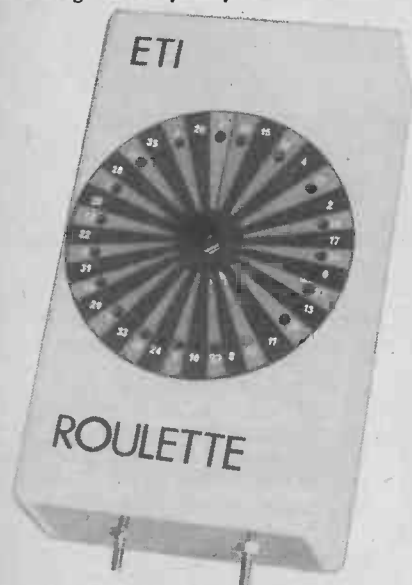
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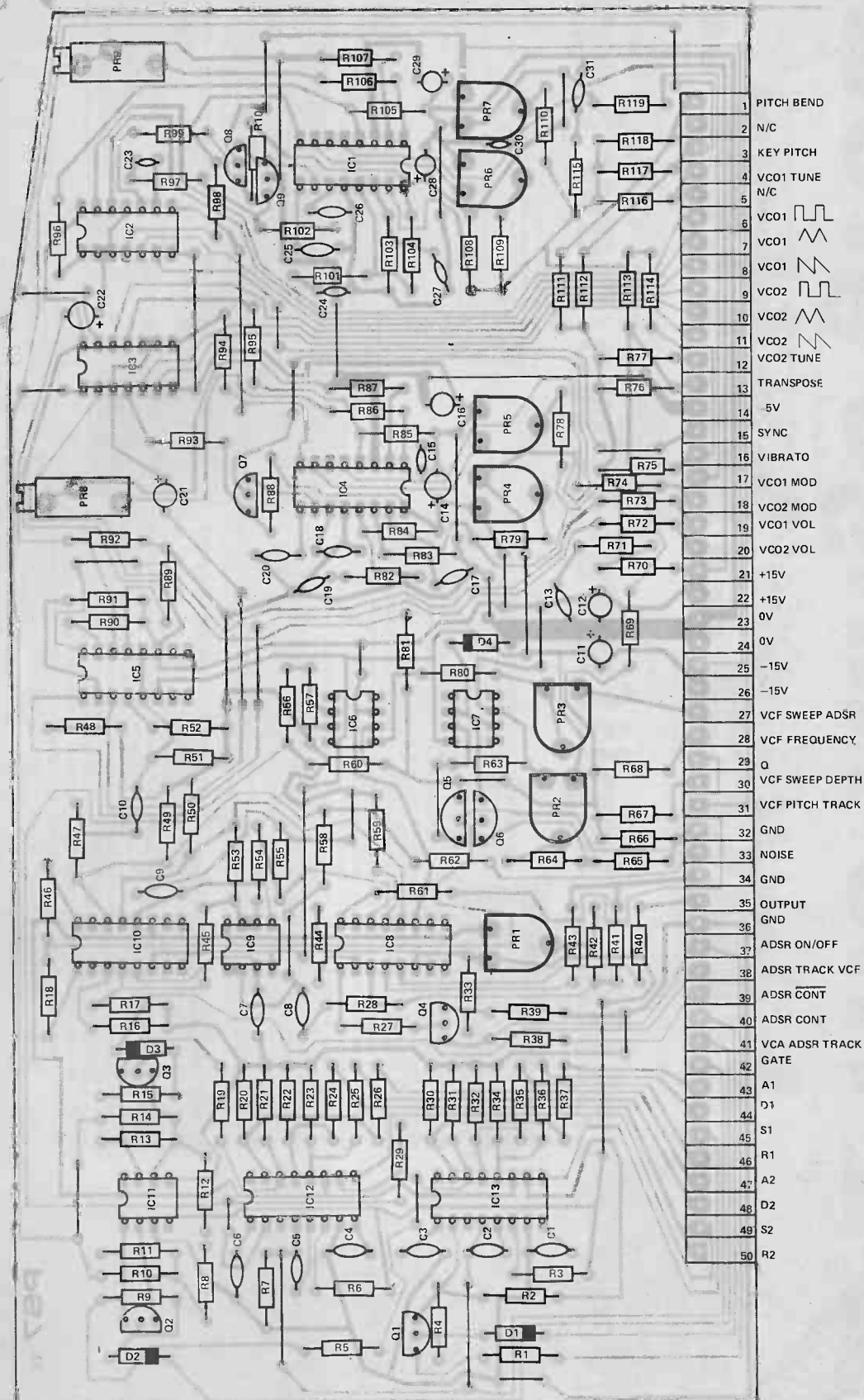


Fig.7 Component overlay for the PS7 voice board. Take care with the orientation of the ICs, especially IC1 and IC4. One corner of the board is cut off to avoid fouling the panel boards.

ETI

MICROBASICS



Henry Budgett warms his soldering iron in the glowing coals of the office fire, dabs a spot of flux here and there and sets about building Heathkit's H8 computer kit.

One of the best ways to get to grips with a microcomputer is to actually build one for yourself. Whilst the sheer complexity of this operation may seem to be beyond the average skills of an electronics enthusiast, the recent trends in personal computers has brought about a large number of micros that are available in kit form. Among the names that spring to mind are NASCOM, Acorn and Tangerine. One of the biggest electronic kit makers is Heathkit and, not surprisingly, they have a computer or two among their range. I have chosen to take their H8 computer as the basis of the next few parts of this series and I will actually build a complete system out of the various component parts that we have been discussing over the last few months.

System Choice

The selection of the H8 is based on two main points. It is supplied with the most incredibly detailed documentation, which is also available separately and it's about the only personal computer system I could find that could be broken down into the component parts of CPU, memory, I/O and control.

Certain parts of the system are supplied ready built regardless of whether you buy the kit or not. The CPU card and the 16K memory card are both built — for a good reason. The kit is by no means a simple one. It took me three very late evenings to build, but it is a tribute to the designers and the writers of the instruction books that it worked first time. Under normal circumstances I would have allowed a complete weekend for the construction of the main unit but editorial deadlines decided otherwise!

The basic kit consists of the box, the power supply, the

motherboard, the front panel controls and the ready-built CPU card. The manuals cover every possible aspect of the construction and possible fault-finding that you will be likely to need. The only possible quirk is that you will have to buy at least one memory card at the same time as you buy the kit or it simply won't work — frustrating for you, but ideal for me as I wanted a system made of separate parts.

In Bits

If you have been following the series from the very beginning you will know that we can break a computer down into a number of parts — the CPU, the memory and the I/O. Whilst this is fine from a general point of view, there are other vital parts that need to be taken into account.

The power supply is a vital component and, in the H8, is of a distributed load type. The mains is transformed down to $\pm 18\text{ V}$ and $+8\text{ V}$. These voltages are supplied through the bus to each card in the system. The card carries voltage regulators for each required power line and thus each card draws the power it needs in regulated form. Some other systems use a regulated power supply which provides a constant supply of exact voltages.

The advantages of the distributed load system are that the main driving line, in our case $+8\text{ V}$, will drop in voltage as the current drawn from it increases. This apparent failing is, in fact, an advantage, because the thermal output from the on-board regulator is directly proportional to the excess voltage across them, the lower the supply rail drops towards 5 V , the less heat is produced by each regulator. In fact the heat output will remain roughly constant regardless of the number of cards you have plugged in. ➔

Slot Machine

The H8 bus is a standard in its own right. It consists of 50 parallel connections between each of the cards that are plugged in, a maximum of eight slots are available. The first slot, the one nearest the front, is dedicated to the front panel control circuits and the last slot is dedicated to the expansion connector. The convention of the bus is such that the CPU is installed in slot two followed by the memory up to a maximum of 64K and then the I/O.

The signals carried by the bus are the address lines, the data lines and the necessary control signals as well as the power. We can break these down further. The 16 address lines are all inverted, that is they are normally at logic 1 and are set to logic 0 when active. The eight data bits follow the same convention, but they are capable of bi-directional operation, that is data can be sent and received and they can be isolated to allow processes like DMA (Direct Memory Access) to take place. The control bus consists of the signals and their functions given in Table 1.

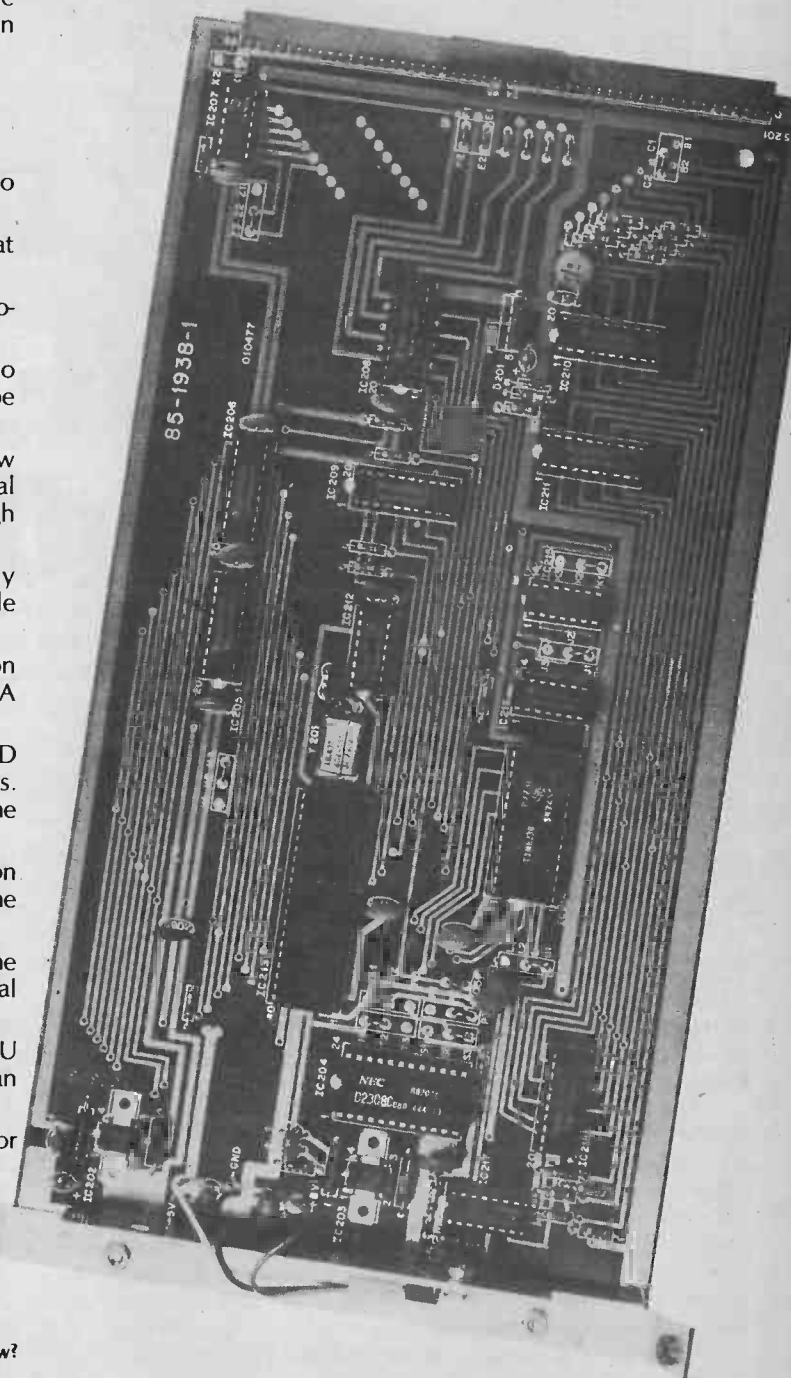
| Signal | Function |
|-------------------------------------|--|
| A_0-A_{15} | Tri-state address bus. Normally at logic 1, set to logic 0 when active. |
| D_0-D_7 | Tri-state bi-directional data bus. Normally at logic 1, set to logic 0 when active. |
| $\overline{O2}$ | CPU supplied clock signal derived from two-phase master clock. |
| HOLD | Input signal from bust that instructs the CPU to enter a hold state, this allows DMA type accesses to occur. |
| HLDA | The acknowledge signal from the CPU to show that it has entered the HOLD state. This signal occurs slightly before the bus assumes the high impedance state. |
| $\overline{INT}_1-\overline{INT}_7$ | The interrupt request lines. The CPU will only honour the interrupt if the interrupt enable register is set. |
| \overline{RESET} | Resets the CPU's program counter to location 0, resets the interrupt enable and HLDA register. Does not destroy register contents. |
| MEMR, IOR | Two control lines than enable READ operations on I/O and memory devices. Derived on the CPU card from DBIN and the appropriate status bit(s) of the CPU. |
| MEMW, IOW | Control lines that enable write operations on I/O and memory. Derived from WR and the appropriate status bit(s) of the CPU. |
| RDYIN | An asynchronous bus signal that causes the clock to produce a synchronous READY signal for the CPU. |
| M1 | CPU output to the bus that is set when the CPU is in the fetch cycle of the first byte of an instruction. Often used for synchronisation. |
| ROM | An input that allows the on-board monitor ROM to be turned off. |
| +8 V | Unregulated 10 A supply |
| +18 V | Unregulated 250 mA supply |
| -18 V | Unregulated 250 mA supply |

Table 1 What you get on the bus and what it does. Who needs 100 pins now?

Taking Control

Our basic system consists of a CPU installed on the bus, a power supply unit, an amount of memory and a simple I/O device. As discussed last month this may seem OK, but it requires the magic ingredient of a monitor program to actually do any thing useful.

The H8 uses a true front panel as its basic control device and this is almost unique in the micro world. The usual basic operations may all be performed from a keypad and the corresponding results observed on a set of LED displays. At this point you may be wondering why this is so wonderful. The truth of the matter is that it is really a micro using mini operating principles. Those of you who have had the great good fortune to use the PDP 8 series of computer, especially the PDP 8A, will be instantly at home. The CPU is a conventional 8080A running at 2 MHz, but the displays are in octal, not the usual Hex. To avoid



any confusion or misunderstanding I will give any relevant addresses in both Hex and octal.

Each of the keys on the keypad can perform a number of functions. Figure 1 gives their layout and corresponding function, but their main advantage is that they give direct access to the memory and register locations without having to go through a 'soft' routine as happens with a VDU. Critics of this kind of system probably have never seen a PDP 8 and thus can't appreciate the flexibility that it offers.

The monitor program is built into the CPU card and is aware that the keypad and the displays are the primary I/O device. If you are affluent enough there is a very intelligent VDU available, but more of that in a month or two.

Fig. 1 16 keys but not Hex! The H8 keypad gives both octal entry and monitor control. All registers, memory and I/O functions can be controlled from here.

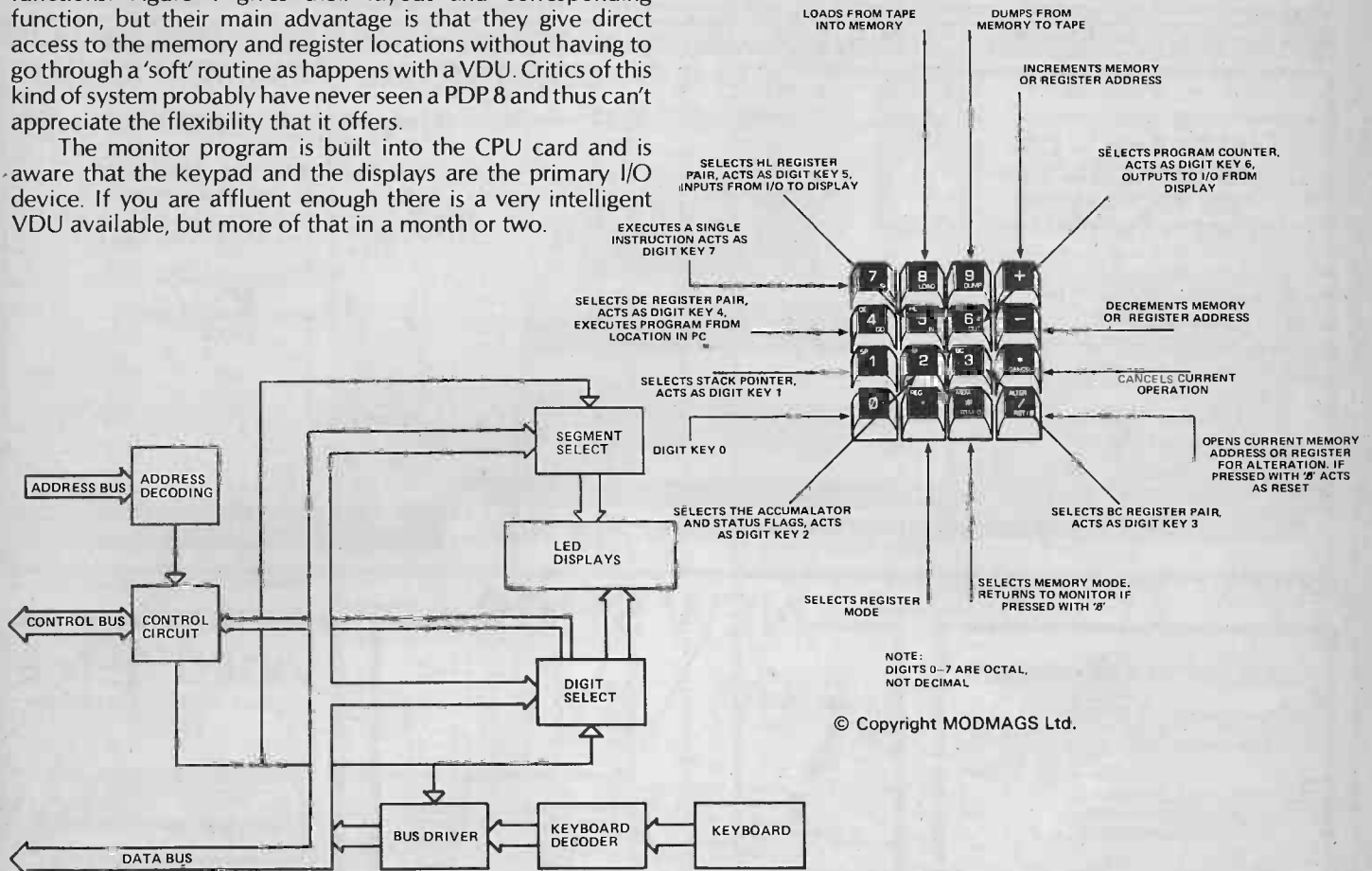


Fig. 2 Functional block diagram from the front panel. The keys are only connected to the displays through the monitor program. Any wrong keying is detected and an audio warning is given.

Mr. 10%

Because the monitor program has to continually scan the keyboard, some 10% of the CPU's time is taken up by this software. The addresses assigned to the keypad and the display are 360 (F0H7 and 361 (F1H) respectively. The displays require constant updating and the front panel circuitry (see Fig. 2 for a block diagram) issues an interrupt every 2 mS. This interrupt is decoded by the CPU and causes the data on the bus to be set into the I/O buffers and hence displayed on the LEDs. This write signal to the I/O device also causes the MON lamp on the front panel to be lit, indicating that the monitor program is running and hence servicing the front panel. Once the LEDs have been refreshed, the key pressed is locked into the data bus by a read operation.

Once the CPU has 'fired up' it generates an M1 pulse at the start of each machine cycle, as we discussed earlier in this series. This pulse is stretched and used to turn on the RUN lamp, indicating that the processor is 'up-and-running'. This lamp will go out if the processor is in a HOLD or WAIT cycle.

As an indication that a key has been pressed on the keypad, an audio tone is generated. The tone is normally short unless the monitor has accepted the keyed command when it is twice the usual length or when you have made an error when it is maintained for as long as you try to make the error.

Following On

Having introduced the complete system, next month's exposé will concentrate on the CPU card and how it communicates with the various components of the system through the bus.

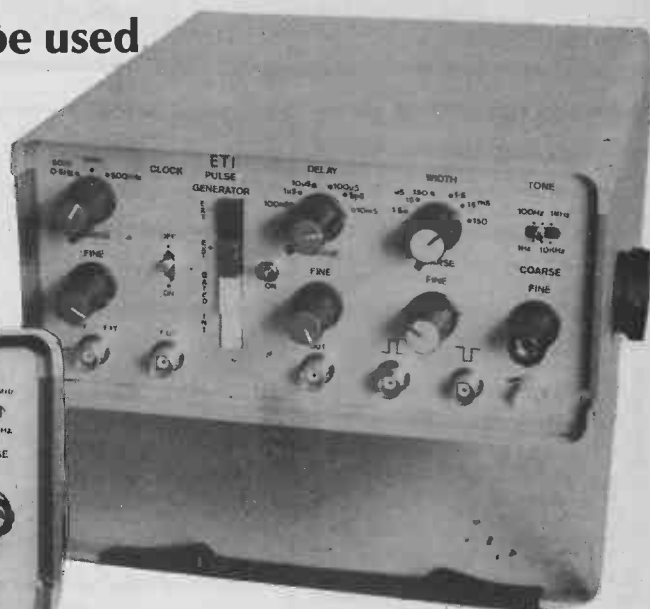
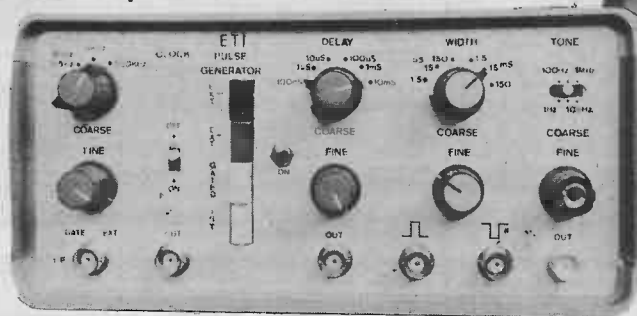
A few words of grateful thanks are due to Heathkit for the generous loan of the H8 and its associated parts. Those who are interested in constructing their own can buy the system manuals *before* you decide on buying the hardware. They cost £4 each and if you do buy the kit this will be deducted from the kit price.

The book that I mentioned, 'The use of microprocessors' by M Aumiaux, deals specifically with the 8080A and the 6800 and covers most of the groundwork needed by first-timers in the micro business. Published by John Wiley & Sons it will cost you £12 in hardback. For the seriously interested there can be no better source of information than Intel. After all, they do make the 8080A and they can be contacted at Dorcan House, Eldene Drive, Swindon, Wiltshire. They have a comprehensive range of both hardware and software manuals and these are well worth obtaining.

ETI

PULSE GENERATOR

A versatile piece of test gear that can be used as a single or dual pulse generator, a delayed-pulse generator, or a direct or delayed tone-burst generator. Design by Ray Marston. Project development by Steve Ramsahadeo.



Pulse generators have a variety of applications in the modern electronics workshop/laboratory. In its simplest form, a pulse generator can be used for testing the performance characteristics of a common-or-garden digital circuit or for testing the transient responses of AF or RF amplifiers. In a more advanced form, as a delayed-pulse/ tone-burst generator, the instrument can be used for simulating or implementing sophisticated systems such as ultrasonic movement detectors, range-finders, or RADAR systems.

The ETI pulse generator is the most versatile instrument that you could possibly wish for. It has two built-in pulse generators (a delay and a width generator), which can be effectively clocked in parallel or series. When parallel clocking is used, the unit simultaneously generates two independently controlled pulses from each clock pulse. When series clocking is used, the unit generates an output pulse that is delayed from the clock pulse by a period set by the delay generator. The pulse width and delay times are both fully variable over the range 100 nS to 150 mS.

The two pulse generators can be clocked from either internal or external signals. The internal clock generator spans the full range of 0.5 Hz to 500 kHz and can be used directly or can be gated by external signals. The clock signal is made available externally via an output socket.

The delay pulse of the unit is made externally available via a single output socket, while the main width pulse is available in direct and inverted form via a pair of sockets. The main pulse can also be used to trigger and gate an internally generated tone burst signal, which is available via another socket. The tone burst signal is fully synchronised to both the clock signal and the leading edge of the main pulse and is fully variable over the 1 Hz to 1 MHz range.

All outputs of the unit are buffered and short-circuit proof. The outputs are driven by TTL and are fixed-amplitude with typical rise and fall times of about 20 nS. The complete unit consumes a mean current of about 40 mA and can be powered from either a 6 V battery pack or from a mains-derived 5 V regulated supply.

Construction

First, wire up the PCB as shown on the overlay, noting the use of a large number of Veropins for making external connections. Take the usual precautions over the polarity of semiconductors and electrolytics. Note that two connecting links are used on the top of the PCB and that, on the underside of the board, insulated wire links are made from pin 1 of IC3 to pins 1-2 of IC5 and from pin 6 of IC3 to pins 9-10 of IC5.

When construction of the PCB is complete, fit it into a suitable case, make the interconnections to all switches/pots/ sockets, connect the circuit to a suitable power supply, and test/debug the circuit as follows.

Testing

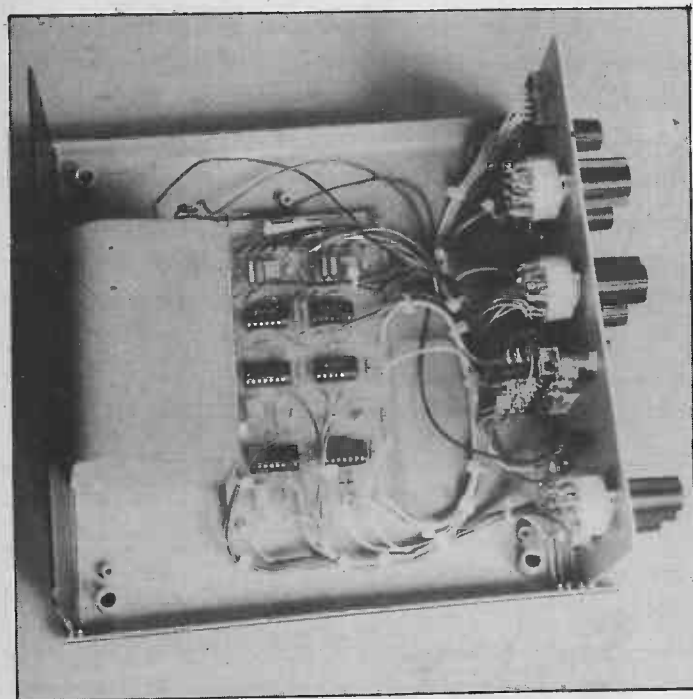
Turn SW2 to the INT CLK position, monitor SK2 on channel 1 of a two-channel 'scope and switch SW7 on. If the clock generator circuitry is operating correctly, a rectangular clock signal should be visible on the 'scope and should be variable over the 0.5 Hz to 500 kHz range using RV1 and SW1. If a clock signal is not visible, check through the SW2-IC6 and IC1 circuitry to find the error. If all is well, turn SW2 to the GATED CLK position and check that the generator can be gated on and off by SK1 signals. Finally, check that external clock signals (from SK1) are available at SK2 when SW2 is turned to the EXT CLK + or - positions.

Now, with SK2 still connected to channel 1 of the 'scope and with SW2 in the INT CLK position, monitor SK3 on channel 2 of the 'scope. With the 'scope synchronised to channel 1, check that a delay pulse is synchronously generated at SK3 and is fully variable by RV2 and SW3.

Next, monitor SK5 output on channel 2 of the 'scope, turn SW4 to the DELAY OFF position and check that a width pulse is synchronously generated at SK5 and is fully variable by RV3 and SW5. If all is well, turn SW4 to the DELAY ON position and check that the width pulse can be delayed relative to the clock using the RV2-SW3 delay controls. Check that an inverted version of the output pulse is available at SK6.

Finally, check that a tone burst pulse-controlled signal is available at SK4 and that the tone frequency is fully variable by the RV4-SW6 tone controls.

When making the above functional tests, note that the pulse period (or the sum of the pulse periods in the delay mode) must always be less than the period of the clock signal and that the period of the tone signal must be less than that of the width pulse.



Internal construction of the ETI Pulse Generator. We used a battery supply, but there is sufficient room in the case for a mains supply, if preferred.

PARTS LIST

Resistors all 1/4 W 5%

| | |
|-------------------|-----|
| R1 | 22k |
| R2 | 10M |
| R3 | 1k0 |
| R4 | 4k7 |
| R5, 7, 10, 11, 12 | 47R |
| R6, 8 | 1k5 |
| R9 | 10k |

Potentiometers

| | |
|--------|-----------------|
| RV1 | 22k logarithmic |
| RV2, 3 | 22k linear |
| RV4 | 2M2 logarithmic |

Capacitors

| | |
|----------------|-------------------------------|
| C1, 8, 14, 16 | 1u0 polycarbonate |
| C2, 6, 12, 17 | 10n polyester (C280) |
| C3, 18 | 47p ceramic |
| C4, 10 | 82p ceramic |
| C5, 11 | 1n0 polycarbonate |
| C7, 13, 19, 20 | 100n polyester (C280) |
| C9, 15 | 10u 16 V tantalum |
| C21 | 1000u 10 V axial electrolytic |

Semiconductors

| | |
|--------|---------|
| IC1, 4 | CD4046B |
| IC2, 3 | 74121 |
| IC5 | 7408 |
| IC6 | 7414 |
| Q1 | BC108 |
| D1, 2 | 1N4148 |

Miscellaneous

| | |
|--|--|
| SW1, 3, 5 | 1 pole rotary switch (Lorlin type) |
| SW2 | 2 pole changeover (4 off interlocking pushbutton type) |
| SW4 | SPDT miniature toggle |
| SW6 | 3 position slide switch |
| SW7 | SPDT slide switch |
| SK1, 2, 3, 4, 5, 6 | BNC 50R sockets |
| 7 off collet knobs | |
| Vero case (order as Hi Style 202-222231) | |

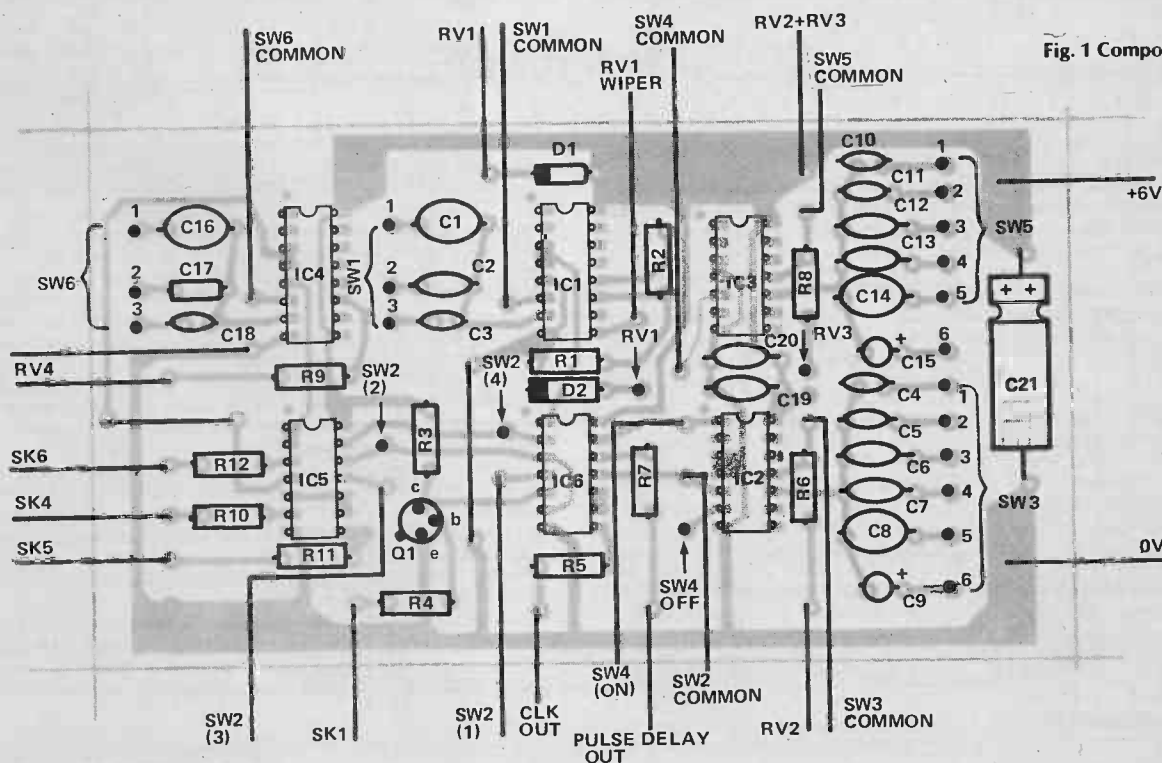


Fig. 1 Component overlay.

LINK UNDERSIDE OF PCB
PIN 6 OF IC3 TO PINS 9 AND 10 OF IC5
ALSO PIN 1 OF IC3 TO PINS 1 & 2 OF IC5

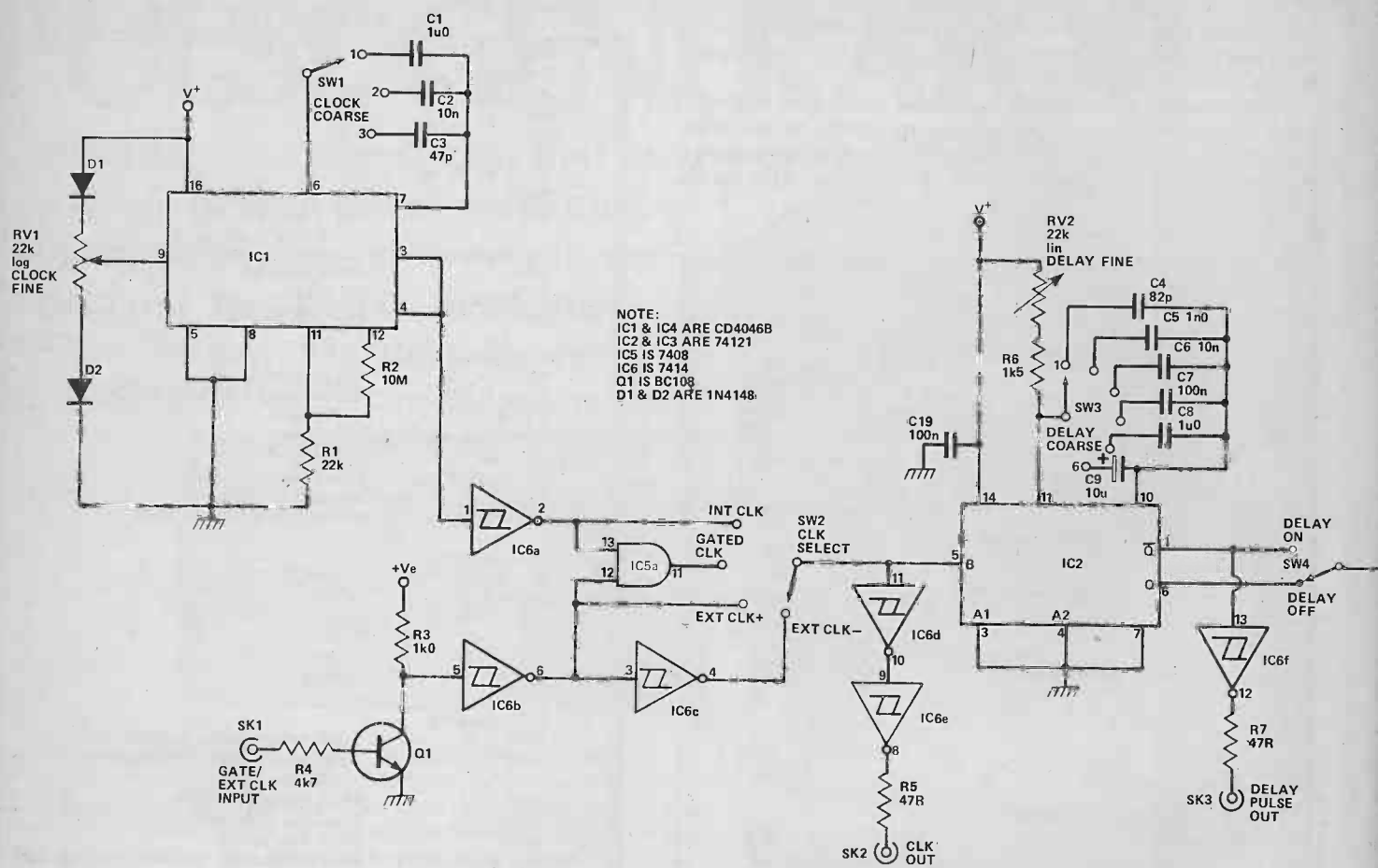
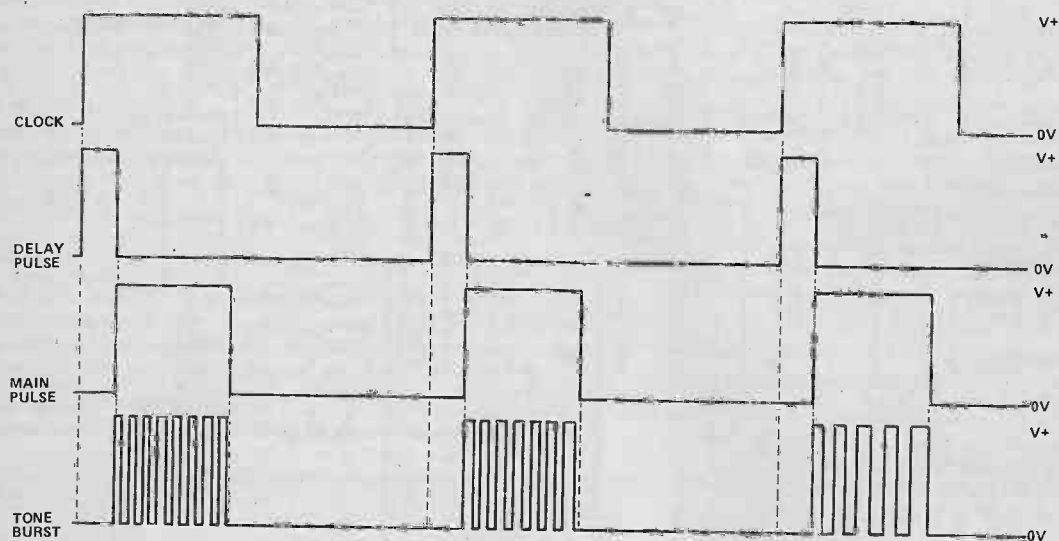


Fig. 2 Circuit diagram. Pulse delay, pulse width and clock generator ranges are shown below.

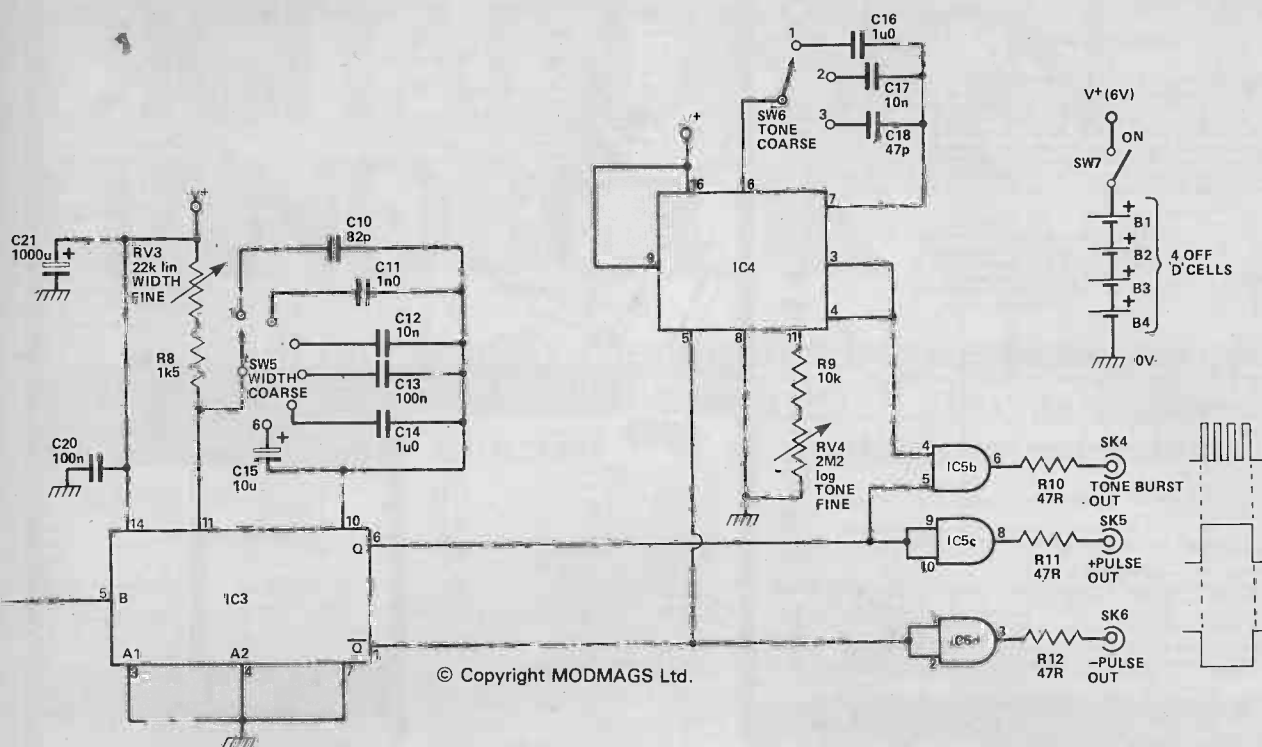
| PULSE-DELAY RANGES | |
|--------------------|--------------|
| 1 = | 100nS -1.5uS |
| 2 = | 1uS -15uS |
| 3 = | 10uS -150uS |
| 4 = | 100uS -1.5mS |
| 5 = | 1mS -15mS |
| 6 = | 10mS -150mS |



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Fig. 3 Pulse timing diagram.

PROJECT : Pulse Generator



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| PULSE-WIDTH RANGES | |
|--------------------|----------------|
| 1 | = 100ns -1.5uS |
| 2 | = 1uS -15uS |
| 3 | = 10uS -150uS |
| 4 | = 100uS -1.5mS |
| 5 | = 1mS -15mS |
| 6 | = 10mS -150mS |

| CLOCK-GEN RANGES | |
|------------------|---------------|
| 1 | = 0.5Hz-50Hz |
| 2 | = 50Hz-5kHz |
| 3 | = 5kHz-500kHz |

BUYLINES

All components used in the pulse generator are common types and should be available from the major mail order companies that advertise in this issue. The collet knobs can be obtained from Electrovalue.

HOW IT WORKS

The circuit comprises a clock generator (IC1), two pulse generators or monostables (IC2 and IC3), one gated tone generator (IC4) and a few gates and inverters. The most fundamental elements of the project are the two pulse generators, which are designed around 74121 TTL monostable ICs. In our particular application, these monos are triggered by the positive transition of a clock signal applied to pin 5 and then generate an output pulse with a duration determined by the R-C timing components connected to pins 10 and 11.

Note that these monostables generate a positive output pulse at pin 6 and an inverted or negative pulse at pin 1. Thus, if IC3 is triggered by pin 6 of IC2, both monos will effectively trigger at the same time (effective parallel clocking) and the IC3 pulse will not be delayed relative to the main clock signal. If IC3 is triggered by pin 1 of IC2, on the other hand, the IC3 pulse will be delayed relative to the main clock signal. In practice, both the delay and the main pulse widths are fully variable over the range 100 ns to 150 ms by independent controls.

The pulse generators can be clocked by an internal clock generator (IC1) or by external clock signals. The internal clock generator is designed around the VCO section of a 4046B phase-locked loop and can span the range 0.5 Hz to 500 kHz in three switch-selected overlapping bands. Each band spans a range of roughly 200:1 controlled by RV1. The output of this generator is buffered by IC6a (a TTL Schmitt inverter) and can be used to clock the pulse generators either directly or by AND gate IC5a. In the latter case, the gate signal must be gated on by an external signal applied to socket SK1.

External gate or clock signals can be applied to SK1. These signals

are amplified and inverted by Q1 and re-inverted and cleaned up by IC6b. The resulting signals can be used either to gate the internally-generated clock signals via IC5a or to directly clock the pulse generators via SW2. In the latter case, the pulses are generated in phase with the external clock signals when SW2 is in the EXT CLK + position, or in anti-phase in the EXT CLK - position. The final clock signals to IC2 are double-inverted by IC6d-IC6e and made externally available at SK2.

The pulse output of the IC2 delay circuit is buffered and made externally available at SK3 by IC6f. Simultaneously, the direct and inverted main-pulse outputs of IC3 are made available at sockets SK5 and SK6 respectively by buffer stages IC5c and IC5d. A tone burst signal is also available at SK4 and is generated as follows.

IC4 is a wide-range square-wave generator designed around the VCO section of a 4046B CMOS IC. This generator can span the range 1 Hz to 1 MHz in three switch-selected overlapping ranges, with each range spanning a 200:1 band controlled by RV4. The output of this oscillator is fed to one input of AND gate IC5b and the positive pulse output of IC3 is fed to the other input of the AND gate. IC4 is enabled only when pin 5 is pulled low. In our circuit, pin 5 is coupled directly to the inverted pulse output of IC3. Consequently, the IC4 signals are precisely synchronised to the pulse generator's clock signals and have a burst duration equal to the pulse width of IC3.

The complete pulse generator project consumes a mean current of about 40 mA and can be powered from a 6 V battery pack or from an external mains-derived 5 V regulated supply.

DIGITAL DESIGN HANDBOOK

The arrival of increasingly complex digital chips brings sophisticated designs within the scope of the hobbyist. It also makes the designer's job more difficult. Tim Orr lays down the ground rules for digital designers.

Digital electronics has become enormously sophisticated over the last decade. Just over 10 years ago I made a rhythm generator using discrete components, which occupied over one square foot of board. Within a few years digital ICs became available which reduced the size of the device by about a factor of 10. A few years later an LSI device became available that did it all in one chip. The same is true of a digital clock built in that same period. The device had a 100 kHz crystal oscillator, which was divided down by 100,000 to generate seconds, divided and decoded to display the seconds, and again for the minutes, hours and AM/PM. This used between 30 and 40 ICs and required considerable power. Now you can purchase a wide range of sophisticated clock and watch chips that can tell the time (even some that speak the time), handle several time zones, wake you up with a melody of your choice and can run for years on a single hearing aid battery, etc., etc.

This does not mean that digital design is now redundant. It just means that a lot of the hard work can now be done by VLSI chips, supported by a bit of conventional digital hardware. It also means that the problems you will be solving are considerably more complex than those of a decade ago. An important development is the introduction of the microprocessor. This device can be thought of as a programmable logic unit capable of simulating vast digital circuits, which can be relatively easily modified by altering the software, but which is only capable of medium to slow speed operation. If the digital circuit that you are designing is likely to contain about 40 ICs then perhaps a microprocessor design would be a better solution.

Basic Principles

One of the most common series of logic devices is the TTL series. These devices run on a standard +5 V power supply. They consume rather a lot of current and so a complementary range known as LSTTL has been produced (Low-power Schottky TTL). The LS range is generally slower than the TTL devices and now a new faster range called ALS (Advanced Low-power Schottky) is becoming available. There are other types of TTL including Schottky, High speed, Low power, etc, but these are generally only used in professional equipment.

The input to a TTL device is a single or multiple emitter. For the 7410, all the inputs must be high before the output will go low. The maximum current needed to pull an input low is 1.6 mA, but the high input current is 0.04 mA. If a TTL input is left open circuit, it will automatically float high, although for proper

operation all unused gates must be tied high and not allowed to float. The output of a TTL device is capable of sinking more current than sourcing it. For the 7410 it is a maximum of 16 mA (low) and 0.4 mA (high). This implies that the 7410 is capable of driving 10 input loads (fan-out of 10). The typical high output voltage is +3V5 and the low is +0V2.

When testing TTL it is important that 'sanitary' logic levels are observed. The signals should always be above +3 V and below +0V5. Signals between these may well produce unpredictable results. Short glitches can also generate problems. One source of glitches is a power supply with too high an impedance. As a TTL gate switches, it generates a short current surge on the supply rail which can produce large voltage spikes. This problem can be overcome by using thick ground and V_{cc} tracks and by regularly decoupling the power supply. Use a 10 to 100nF fast ceramic or 470nF tantalum capacitor for decoupling on every four or five packs.

CMOS

TTL can operate at frequencies as high as 50 MHz, but for higher frequencies ECL (Emitter Coupled Logic) devices should be used. These extend the range to as much as 1 GHz. For lower speed applications CMOS devices can be used. Maximum operating speeds of 5 MHz can be obtained. One tremendous advantage of using CMOS is that it consumes only micro-power. For example, the maximum quiescent current for the 4049 device is 20 μ A. Also, the output voltage swing goes within 10 mV of either supply rail (no load). The inputs are very high impedance, having typical input currents of a mere 10 pA. The output stages can usually deliver currents of 0.5 mA, giving CMOS an enormous fan-out capability, limited by speed rather than DC drive.

The B series of CMOS can run on supply rails between 3 and 18 V, making them ideal for battery operation where dropping supply voltage and low current outputs make TTL designs impossible. The CMOS transfer function shows a wide spread from device to device, which results in an indeterminate region of operation of about 60% of the supply voltage. As the input impedance is so high, the input terminals can often act as sample and hold devices. If you bias one to +3 V, say, and then let it float, it may well remain charged at this voltage. Unlike TTL, unused inputs can float anywhere. Some may well float into a region where both output FETs are partly on, thus presenting a load of a few kilohms across the supply rails, destroying the low power condition. Unused inputs should be tied

high or low, depending on the desired circuit operation. The CMOS range of devices is different in pinout and part number to TTL devices. However, there does exist a CMOS copy of TTL known as the 74CXX series. Decoupling should be used for CMOS designs, but it is less of a problem than for TTL.

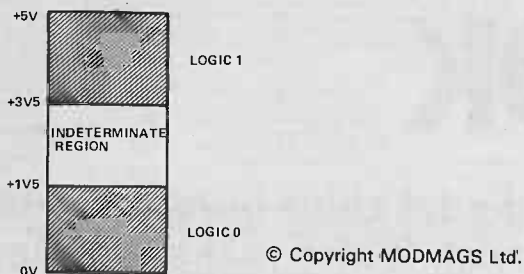


Fig.1 CMOS operation on a 5 V rail.

CMOS/TTL Interfacing

Interfacing to either TTL or CMOS can cause problems. To operate TTL a simple pull down transistor (Fig 2a) will suffice. When TTL is driving CMOS it is necessary to put the TTL output high, because the usual +3V5 high signal is just on the intermediate region of operation for the CMOS device (Fig. 2b). CMOS cannot pull down TTL. The typical 1.6 mA pull down is well beyond the output drive capabilities of most CMOS outputs (Fig 2c). The 4049 and the 4050 are buffer/converters, which can drive up to two TTL loads each. When powered from +5 V they can even accept CMOS levels up to +18 V (Fig. 2d). In doing so they are converting high level CMOS signals to low level TTL drives. Another CMOS converter is the 4041.

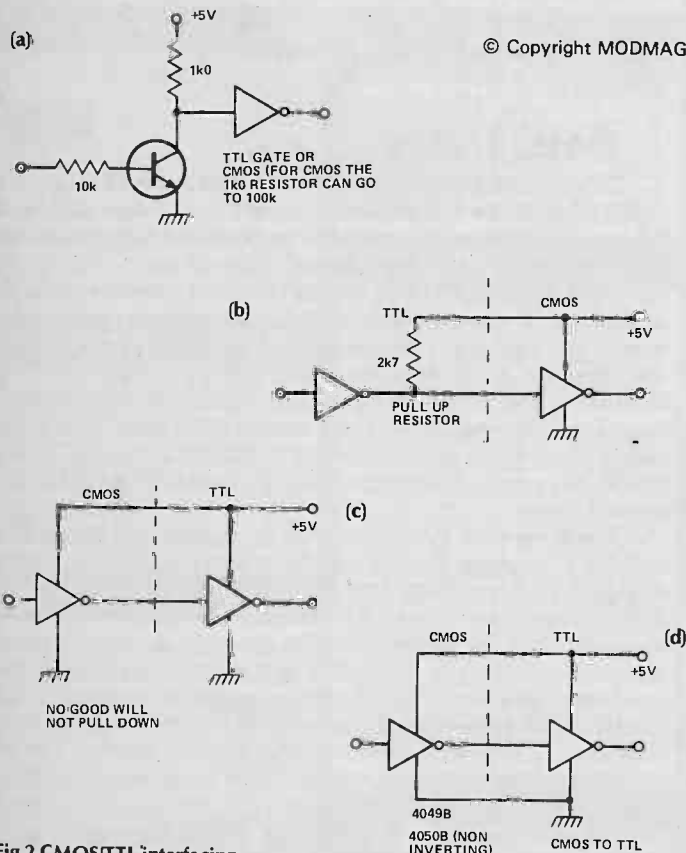


Fig.2 CMOS/TTL interfacing.

Logic Probes

If you don't have an oscilloscope then a simple logic probe can be a useful tool for debugging digital circuits. A simple probe is shown in Fig. 3a. If all six of the inverters are wired up, then the probe can diagnose the logic state of six signals simultaneously, making it very useful for examining data blocks. A logic 1 is represented by the LED being on. Probe B detects the presence of a clock signal. On the falling edge the monostable is fired and the LED turns on. Note that to drive LEDs directly from TTL a pull down circuit must be used. Probe C is for CMOS circuits. Note that the 3 mA drive from the 4050 is not sufficient to light the LED.

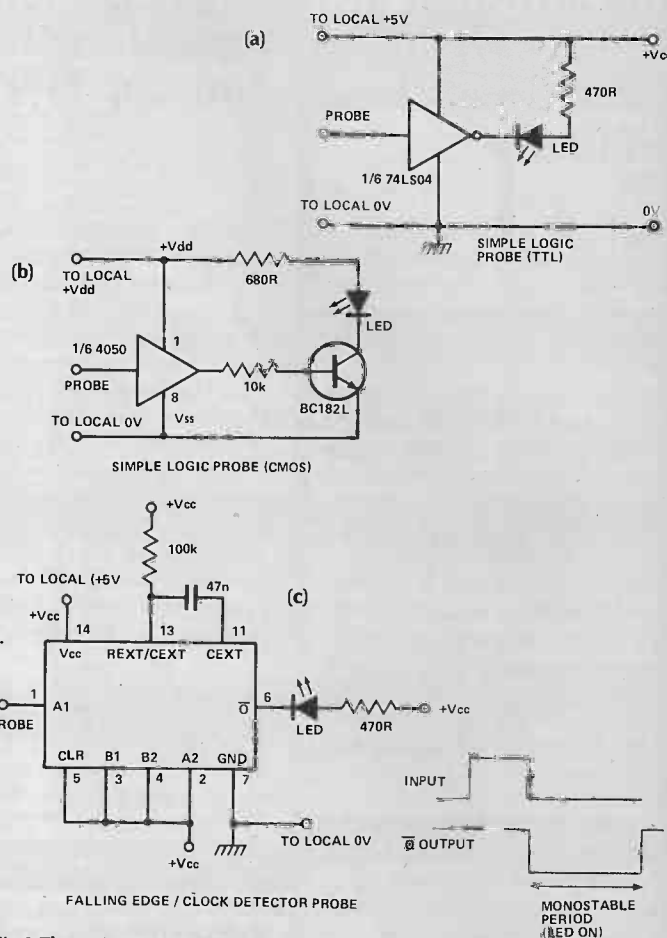


Fig.3 Three simple logic probes.

A set-reset flip-flop can be implemented using NAND or NOR gates. This device can be used to debounce switch actions or as a single bit memory. Note that positive-going pulses are needed for the NOR version and negative-going pulses for the NAND version.

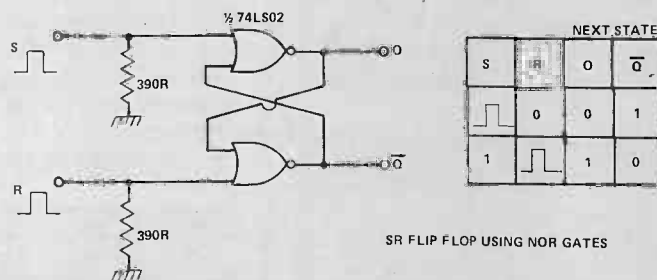


Fig.4a SR flip-flop using NOR gates.

DIGEST



We devoted a section of the Modmags stand to working projects like Space Invasion games and synthesisers.

Breadboard 80

Held as usual at the Royal Horticultural Society's New Hall, Breadboard once again proved to be a great success. By lunch-time on the opening day more people had arrived than on the whole of the first day last year. Our celebrity guest was Brian

Rix, star of the Whitehall farces, and of course, famous (or infamous) for dropping his trousers, which, we are grateful to say, he did not do at Breadboard 80! The attractions were numerous — suppliers of components, home and business computers, CB accessories, space invasion games, hi-fi and disco

equipment as well as all the leading electronics magazines to name but a few. The Modmags stand (that's us folks!) was the undisputed star attraction(?) mobbed by huge crowds. We presume this was because our staff were so helpful and pleasant but there is a sneaking suspicion that it might have had something to do with the two space invasion games we were displaying, offering free games to all, with the opportunity of winning your

own with the highest recorded score. Ah well... The show was certainly the electronics enthusiast's idea of paradise with every conceivable electronic noise pounding the ears and millions of devices to delight the eyes. If you weren't there this year to see it all, don't miss next year. Make a note in your new diary for November the 11th to 15th for Breadboard '81, it'll be better than ever, definitely not to be missed!



Some lucky visitors left the exhibition better off than when they arrived. Here, John Barnes collects his prize from Mike Humphrey of Vero Electronics.

Popular Electronics

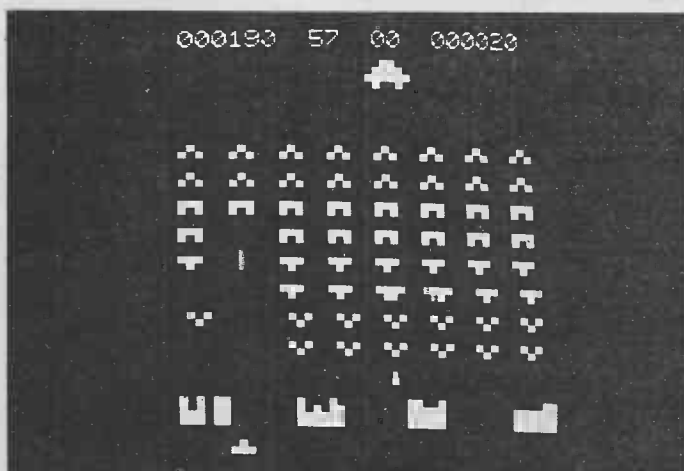
The latest offering from Bernard Babani (Publishing) is a collection of no less than 73 circuits in 149 pages, covering the broad topics of audio, radio, test gear, music and household projects. Each circuit in Popular Electronics Circuit Book 1 by R.A. Penfold is explained in detail. The circuit diagrams are clear and IC/transistor pinouts are given, so you don't have to wade through a data book before you start construction.

As the preface explains, the book is intended for readers with some experience of electronic construction and who can, therefore, work from a circuit diagram only. However, most of the designs are very simple and shouldn't pose any problems. Where necessary, setting up procedures are given.

Popular Electronic Circuits Book 1 by R.A. Penfold is £1.95 from most component dealers and mail order suppliers. If you can't get hold of a copy, write direct to Bernard Babani (Publishing) Ltd, The Grampians, Shepherds Bush Road, London W6 7NF enclosing the price of the book plus postage.

OOPS SW Converter

Please note that in the Spot Design for the Short Wave Converter (November 1980), it is the two 365pF tuning capacitors that should be ganged — the 50pF trimmer is separate.



Time Control

Smiths Industries Time Controls have recently launched a massive advertising campaign for their range of time switch products. This is the biggest advertising campaign ever undertaken by S.I. Time Controls. The theme of the campaign is 'make the most of your time' and is designed to illustrate the convenience and economy that can be provided by the use of time control devices, particularly in the home. As part of the advertising support, the London Underground will carry posters, these being ideally suited to explaining the advantages of the products to commuters who perhaps in their rush to get to work have left their immersion heaters/radiators/lights on all day by mistake. For further details on Smiths Time Controls contact: Smiths Industries Time Controls, Waterloo Road, Cricklewood, London NW2 7UR.

Aquiline Logic

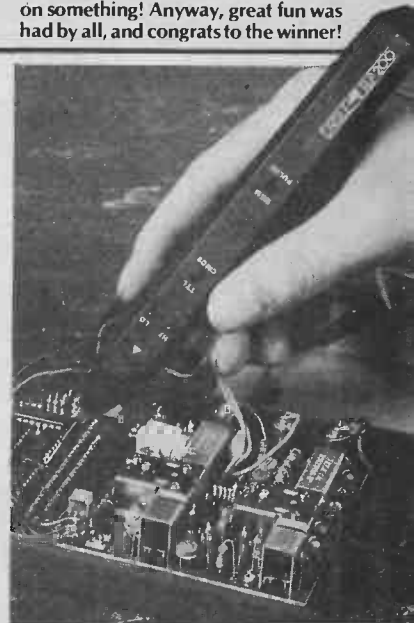
Two new logic probes from Eagle International join the digital test gear market. The ELP 150 and the ELP 200 can operate from a supply of 5-15 V, so the equipment under test can likely power the probes. The logic level is shown by a red LED (logic 1) or a green LED (logic 0).

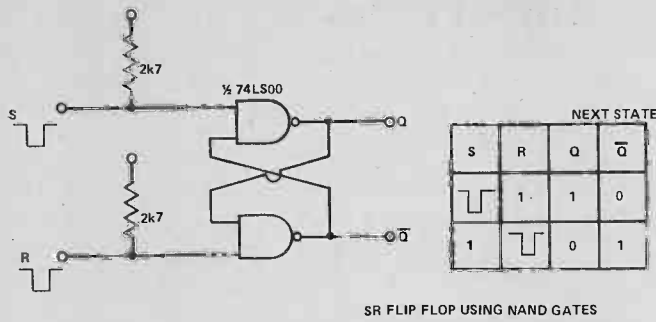
The more versatile ELP 200 also has a pulse stretcher to detect high speed switching (indicated by 1/3 S LED flashes) and a memory to detect infrequent signals without constant observation (shown by permanent LED illumination).

Both probes are TTL and CMOS compatible, have overload and reverse polarity protection and are covered by Eagle's two year guarantee. For further information on the ELP 150 and ELP 200, contact Eagle International, Precision Centre, Heather Park Drive, Wembley, Middlesex HA0 1SU.

Invasion!

On our stand at Breadboard this year we had two of our Space Invasion machines on show, supplying free games to all comers, with the added bonus of winning your own machine for the highest recorded score. Needless to say, the competition was very hot! The overall winner was Mr A Weircigroth of North London. The show proved how tough our machines are. They stood up well to five ten-hour days, and only once after a bashing did one of the machines suddenly decide to give an unlimited number of bases for a short time during one of the days. Ah well, Space Invasion is a very emotive sort of game, the losers have to take it out on something! Anyway, great fun was had by all, and congrats to the winner!





SR FLIP FLOP USING NAND GATES

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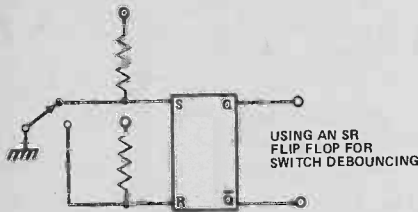
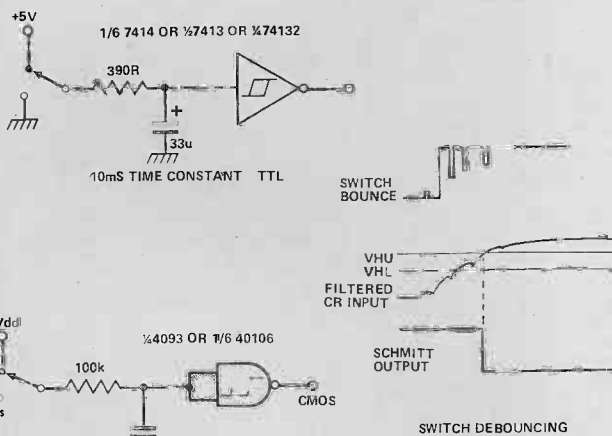


Fig.4b SR flip-flop using NAND gates.

Switch Debouncing

Contact bounce from a mechanical switch can cause problems in digital circuits. It can be seen as a multiple entry. By filtering the signal and then Schmitting it the bounce can be reduced to a single transition. Note that the TTL device needs a low value resistor to ensure that the logic low is reached.

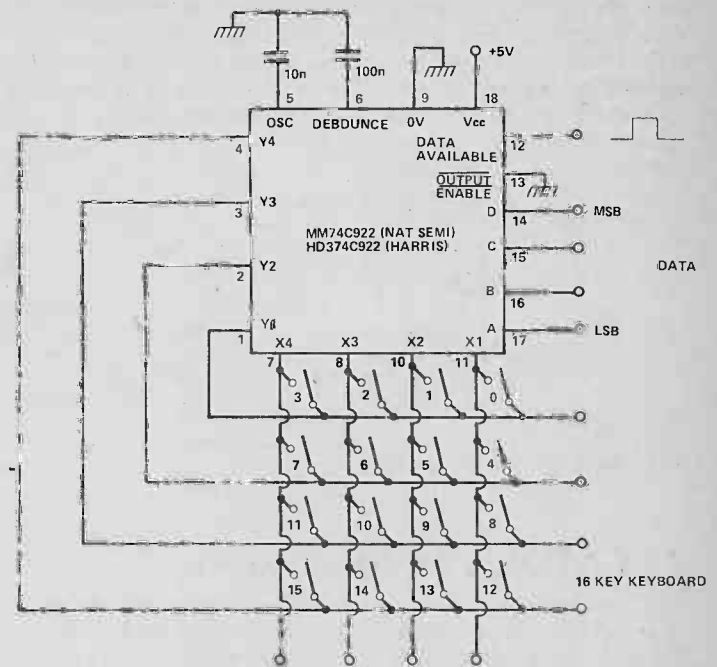


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Fig.5 Switch debouncing.

16 Key Encoder Chip

The 74C922 generates a four bit output code representing the last key pressed. The keyboard can be scanned by an external clock or by its own internal oscillator. All the switches are internally debounced by the IC. The output can drive low power TTL. The device can be used to encode a Hex keyboard or any other switch matrix. For 20 note operation the MM74C923 can be used.



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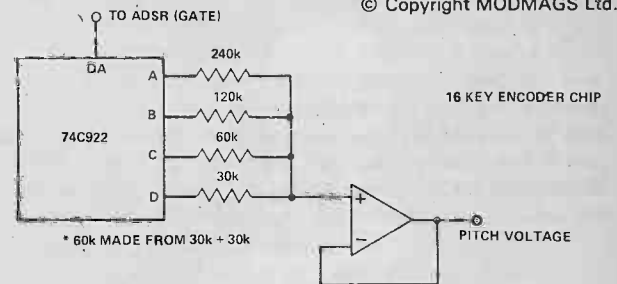


Fig.6 16 note keyboard for music synthesiser.

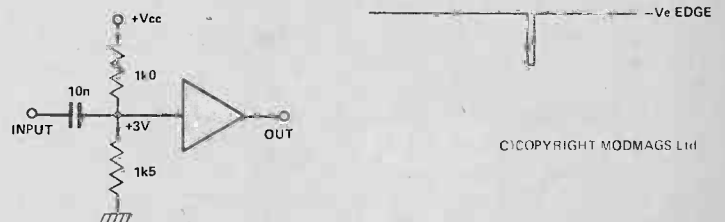
Edge Delay

This circuit is sometimes used to generate a short delay to help prevent a race condition between two signals. A Schmitt trigger gives sharp output waveform. If an ordinary gate is used then the output will have a slower falling edge.

Often a digital signal is very thin (50-100 nS), difficult to see on an oscilloscope and impossible on a logic probe. The monostable action of the pulse stretcher enables the pulse to become visible.



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Fig.7 TTL gates can be used to detect positive and negative edges by using simple CR input networks.

D-Type Flip-Flop

The 4013 is a CMOS dual type flip-flop. Data present at the D input is transferred to the Q output on the positive transition of the clock. The clock waveform should have a rise time of greater than 5 μ s. By programming the Set and Reset pins the outputs may be preset to any state. The device may be used as a single bit memory, or by connecting the D input to the Q output a divide by two counter may be built.

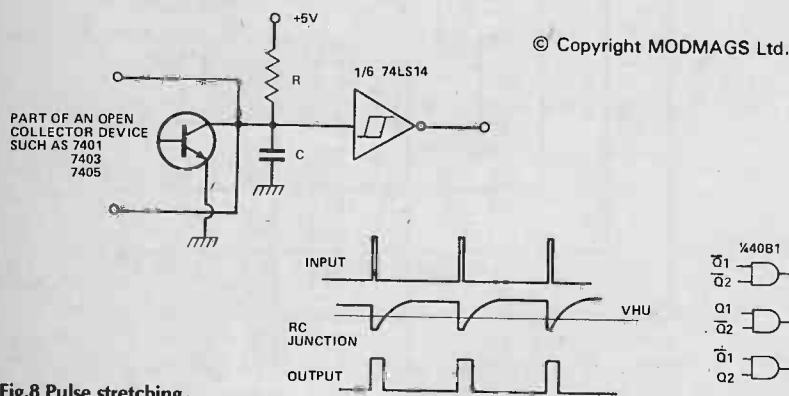


Fig.8 Pulse stretching.

The two halves of a 4013 are used as a two stage binary counter with complementary outputs. The four signals '0', '1', '2' and '3' are known as decoded outputs. These are obtained with two input AND gates. Let's see how decoded output '2' is obtained. Looking at the timing diagram, '2' occurs when Q2 is high and Q1 is low. We can, therefore, generate the waveform by ANDing together Q2 and the inverse of Q1, that is $\overline{Q1}$. The timing diagram is the most important tool for designing logic systems. Just by drawing out the timing that you need, it becomes very easy to both understand and implement the system. There is no need to even consider using Karnaugh maps or logic equations.

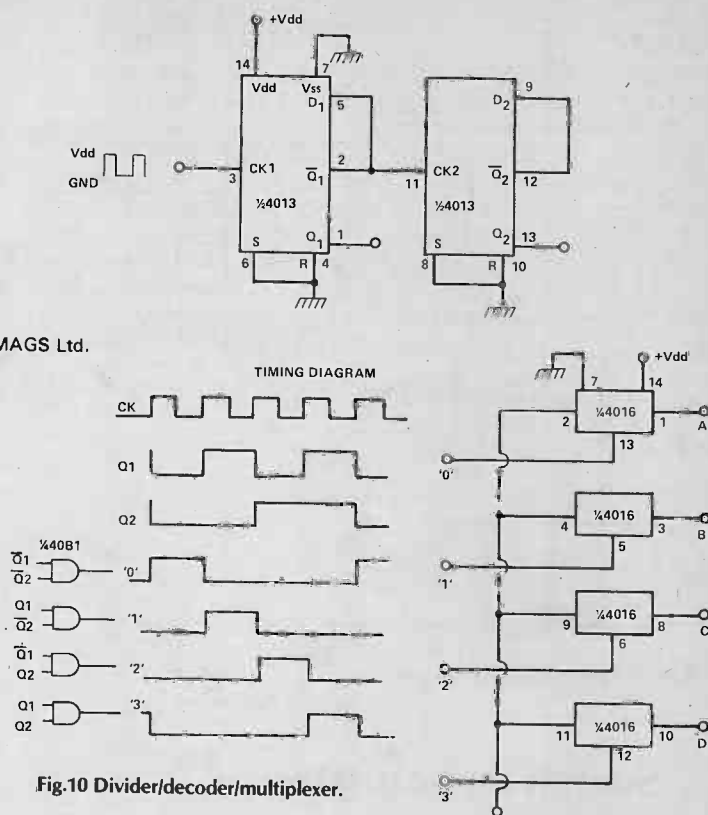


Fig.10 Divider/decoder/multiplexer.

Counting And Decoding

Another counter/decoder circuit is shown, but this time it uses TTL. The 74LS93 is a four stage binary counter. The four outputs are shown on the timing diagram and three decoded outputs '0', '1', and '11' are shown below them. To obtain these, all four outputs must be decoded. For example, to decode '11' we need to look at the timing diagram. Outputs A, B, D are high and C is low. Therefore, a four input AND gate must be driven with A, B, D and C. This could also be determined by studying the truth table. The decoded outputs will probably contain what are known as glitches. These are very thin (100 nS) pulses, which can cause problems in some designs. The outputs of the counter do not all change state at exactly the same time. The outputs further down are later in changing due to the time delays in the system. This counter is known as a ripple counter.

| CLK | D | R | S | Q | \overline{Q} |
|-----|---|---|---|---|----------------|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| X | X | 0 | 0 | Q | Q |
| X | X | 1 | 0 | 0 | 1 |
| X | X | 0 | 1 | 1 | 0 |
| X | X | 1 | 1 | 1 | 1 |

CMOS 4013 X = DON'T CARE STATE

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Fig.9 D-type flip-flop.

The last part of the circuit is the multiplexer. This is a digitally selected, analogue single pole four way switch, implemented with the 4016 analogue transmission gate. A logic 1 at the switch control pin turns the switch on, a logic 0 turns it off. Of course, there is a better way of implementing this design. The 4052 is a differential four channel MUX with its own decoding. Thus, the 4081 and the 4016 are replaced with a single 4052. Other multiplexers include the 4051 (eight way MUX) and the 4053 (triple two way MUX).

This device is a decade counter with 10 decoded outputs. A high on the reset line clears the counter back to zero. The decoded output is high, all the other outputs are low. The simple transistor circuit enables the counter to drive LEDs.

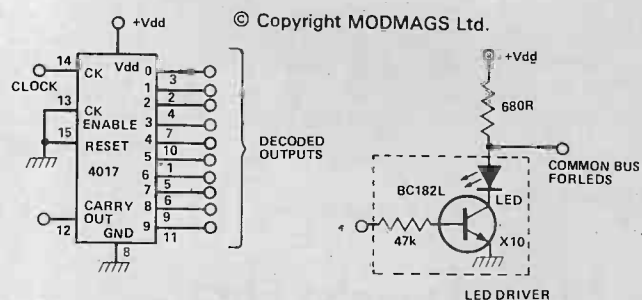


Fig.11 CMOS counter/decoder.

When the counter is clocked, the first stage changes state, which, after a short delay, sends a clock pulse to the second stage, which, after another short delay, sends a clock pulse to the next stage, etc. So, the information ripples down the counter causing a skew in the total output. If the output is then decoded,

TRUTH TABLE

| COUNT | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|-------|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| A | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| B | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| C | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

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| C | OSCILLATION FREQUENCY |
|-------|-----------------------|
| 0p | 50 MHz |
| 1000p | 2.2MHz |
| 10n | 250kHz |
| 100n | 25kHz |
| 1u | 2.5kHz |
| 10u | 250Hz |

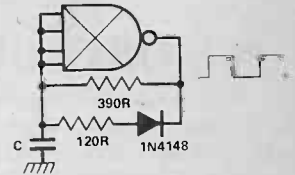
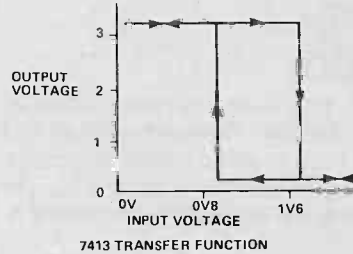
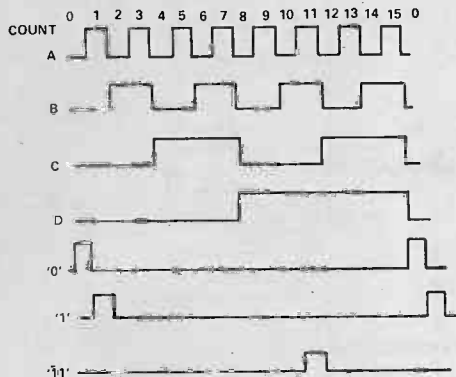
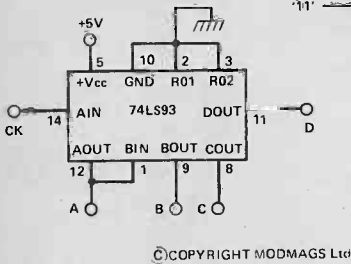


Fig.13b Modifying the feedback network to give a 1 to 1 output.



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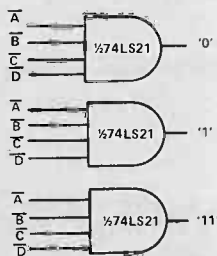
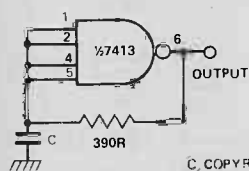


Fig.12 Counting and decoding.

it is possible to get a momentary illegal states caused by the time delays. These effects have been overcome in synchronous counters, which use synchronous clocking of all their storage elements. In these devices the skew time is very short.

Schmitt Trigger Oscillator

Using a simple RC timing circuit, a Schmitt trigger can be made to oscillate. The capacitor is exponentially charged and discharged between the hysteresis levels of the Schmitt trigger. If a TTL device is used, then the squarewave output will be asymmetric, mainly due to the relatively large input current of the TTL gate. A simple resistor/diode network will restore the symmetry. The resistor value must be kept low, otherwise the circuit will not be able to pull the input sufficiently low and will not then oscillate. Using a 7413 the maximum frequency obtainable was 50 MHz, which used the stray capacitance of the package as the timing capacitor, C. The same circuit will oscillate using CMOS Schmitts (4903 or 40106). The waveform will be inherently more symmetrical and, of course, the device has a very high input impedance. This will enable the use of timing resistors of up to 10 to 100 M.



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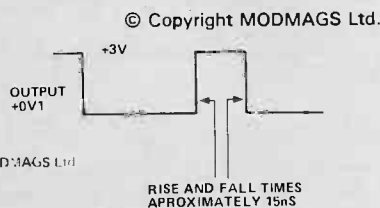


Fig.13a Schmitt trigger oscillator.

555 Oscillator

The 555 chip can be used as an oscillator in digital circuits. The bipolar version of the device can drive several TTL loads, but care should be taken with this device. During the output transition there is a large supply current surge (as much as 350 mA) which can cause problems, such as false triggering. However, if the CMOS is used the current surge is very much smaller and yet the device can still drive TTL loads.

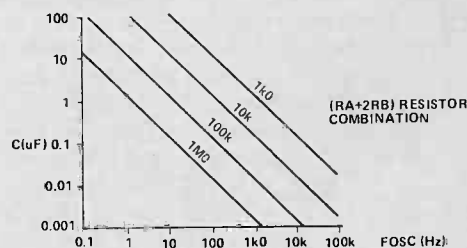
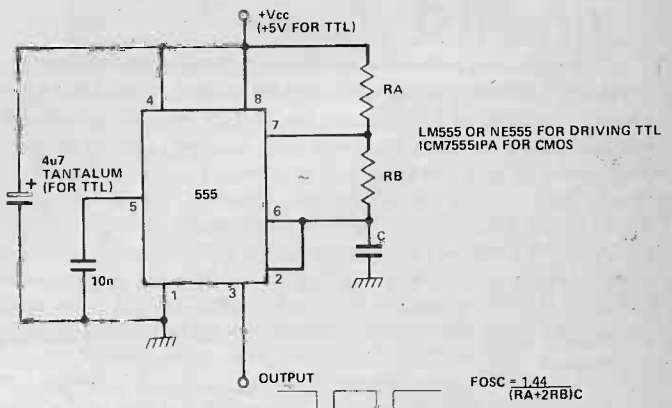


Fig.14 555 oscillator.

Ring Oscillator

By connecting an odd number of inverting gates in a loop, an oscillator is produced. The oscillation period is the sum of the delay times through all the gates. If outputs are taken from each gate in turn, then phased waveforms are available. ➔

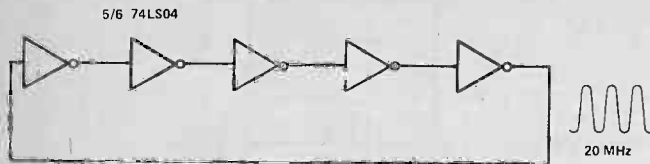


Fig.15 Ring oscillator.

CMOS Oscillator

This two gate oscillator Fig. 16 is a very common device in logic design. It uses simple AC positive feedback with an RC timing network. It defies all attempts to set up a precise formula defining its oscillation frequency. A close equation is $F_{osc} = \frac{1}{2\pi CR}$. It should be used where the oscillation frequency is unimportant.

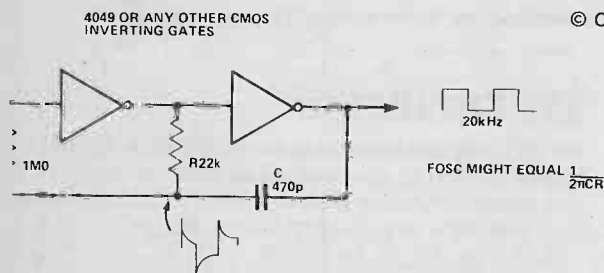


Fig.16 CMOS oscillator.

Crystal Oscillator

To obtain a stable and precise frequency reference, a crystal oscillator is usually used. The impedance of the crystal changes rapidly at its resonant frequency and so, by using it in the feedback loop of an amplifier, it is possible to stimulate oscillation at that frequency. The trimmer capacitor is used for fine tuning. Crystal oscillators are notorious for not oscillating. The classic CMOS oscillator always includes the resistor R (usually 22k). When I breadboarded it, there was no oscillation unless R was a short circuit! The circuit then oscillated with a wide range of standard TV and computer crystals, which included 1.8432, 4.0, 4.194304, and 5.125 MHz. One of life's little mysteries!

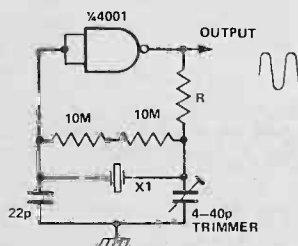


Fig.17 Crystal oscillator.

Bit Rate Generator

When computer terminals and data terminals 'talk' to each other, they do so at standard bit rates. The MC14411 is a bit rate generator IC that produces 14 standard bit rates. If your computer has a serial interface, then it is likely that it has a bit rate generator controlling the data rate.

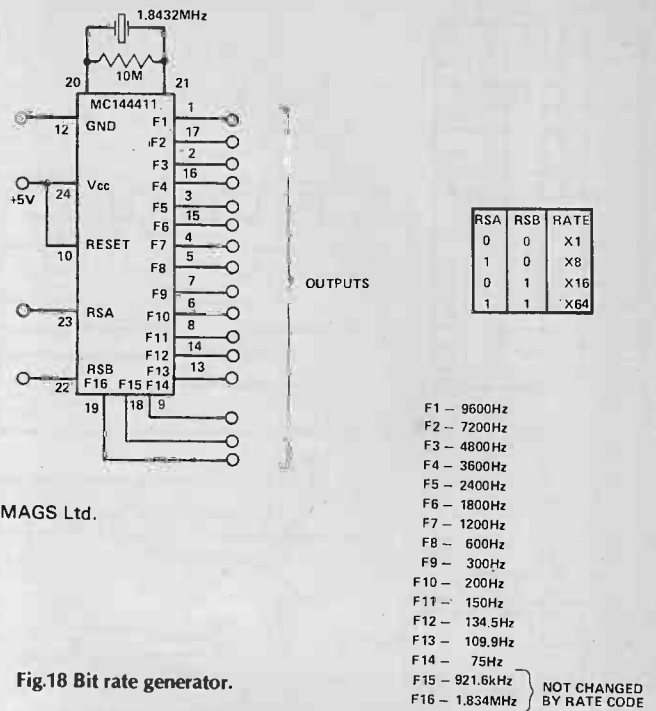


Fig.18 Bit rate generator.

Voltage Controlled Oscillator

A simple VCO can be constructed using a CMOS Schmitt trigger and a few other parts. The timing capacitor (C) is discharged by current from the current mirror Q1,2. A ramp waveform oscillating between the hysteresis levels of the Schmitt is produced. The oscillator generates a series of short positive-going pulses.

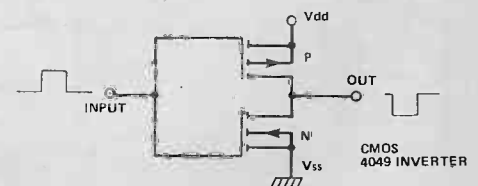
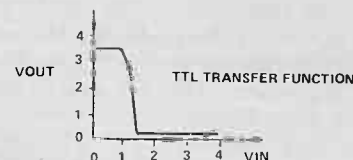
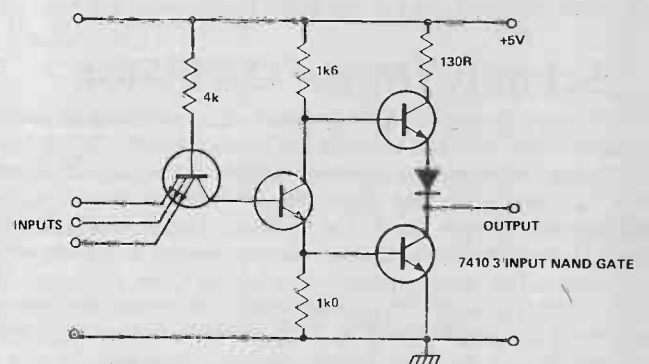
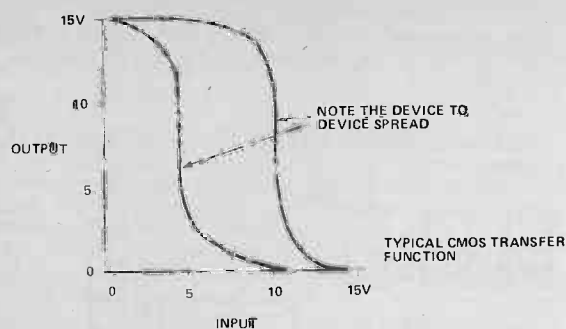


Fig.19a Going back to basic principles.



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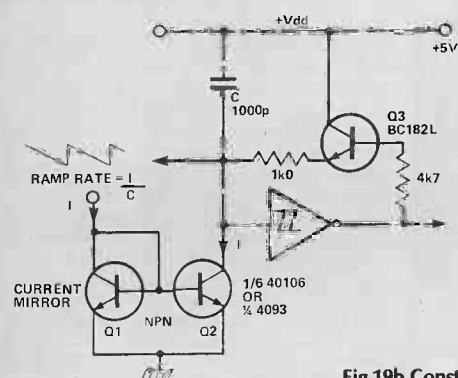


Fig.19b Constructing a VCO.

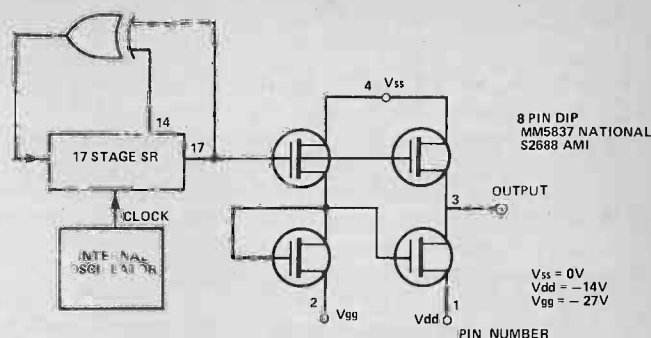


Fig.20b Using a special function chip.

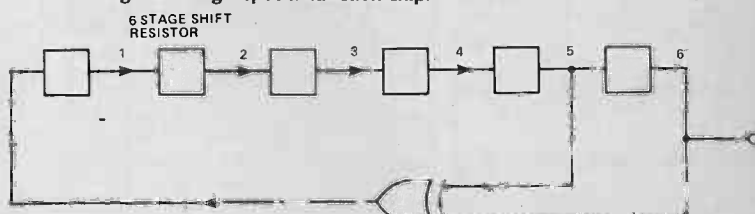


Fig.20c Pseudo-random noise generator

| SHIFT REGISTER LENGTH | SEQUENCE LENGTH | FEEDBACK POINTS |
|-----------------------|-----------------|-----------------|
| 2 | 3 | 1,2 |
| 3 | 7 | 2,3 |
| 4 | 15 | 3,4 |
| 5 | 31 | 3,5 |
| 6 | 63 | 5,6 |
| 7 | 127 | 6,7 |
| 9 | 512 | 5,9 |
| 10 | 1,023 | 7,10 |
| 15 | 32,767 | 14,15 |
| 17 | 131,071 | 14,17 |
| 18 | 262,143 | 11,18 |
| 31 | 2,147,483,647 | 28,31 |
| 33 | 8,589,934,591 | 20,33 |

Fig.20d Feedback points for various shift register lengths.

Pseudo-Random Generator

It is possible to generate noise digitally. A random binary sequence has most of the characteristics of a noise source. This random sequence may be produced by taking exclusive OR feedback from selected points in a shift register. The sequence that is produced does, in fact, regularly repeat itself, but the repetition rate is relatively slow. The longer the shift register length, the longer the repeat time. Also, by choosing the best feedback points, the sequence length will be maximally long. The chart shows the best feedback points for a selection of shift register lengths. Note that incredibly long sequences may be generated very easily.

A pseudo-random noise generator can be made from two CMOS chips. The output may be filtered to give any desired spectrum. There are also two noise generator chips available, the MM5837 and the S2688. The uses of pseudo-random generators include constant noise spectrums for audio testing, noise sources for music synthesisers and random number generators for premium bond pickers!

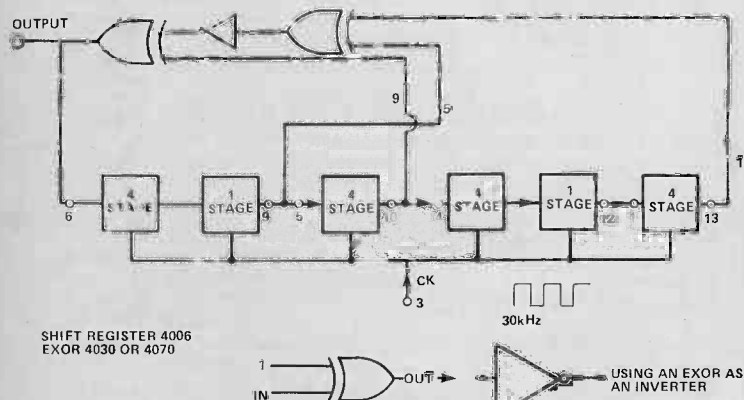


Fig.20a Pseudo-random noise generator using CMOS.

Memories

Memory circuits are becoming cheaper. Static RAMs (Random Access Memories) are the easiest memories to design into systems. Dynamic RAMs are, in fact, less expensive and more dense than static ones but they need extra support circuitry. The information they contain is very volatile and every piece of the memory must be refreshed every few milliseconds. A static RAM has no need to refresh its memory.

Memory is organised into 'handy' sizes. The 2101 has four data inputs and four outputs plus an eight bit address input. The 2102 has only one data input and one data output, but it has a 10 bit address input. The 2114 has four data terminals and a 10 bit address input. Note that the data terminals for the 2114 act as both inputs and outputs. The write cycle for the 2114 is as follows. Set up the memory address and take WE low. Set up the data and take CS low. The RAM has now been written into. Take CS and WE high. The RAM is now in its read mode (that is, it is outputting data) but it is disabled. To read data, set up the address, leave WE high and take CS low. The relevant data will appear at the data I/O pins. The 2114 is a convenient size for microprocessor memories. By using two of them, eight bit words can be stored. When the power is removed from a RAM all the information stored is lost. Some systems employ low power CMOS RAMs with a back-up battery. When the power is removed the battery keeps the RAMs powered up. CMOS RAMs are at present very much more expensive than the common 1K and 4K devices.

ROM (Read Only Memory) can be used to store data so that it is non-volatile. The data is preprogrammed into the

device and can only thereafter be read. It is not possible to subsequently write into a ROM. Many ROMs are externally programmable but by far the most popular is the EPROM (Erasable Programmable Read Only Memory). This device stores its information in small charge wells. It is electrically programmable and, if the contents should need to be altered, it is possible to erase the device by exposing it to hard ultraviolet radiation. It can then be reprogrammed. The 2716 is at present an industry standard, being 2K long and eight bits wide. Microprocessor software is often stored in 2716 arrays.

Fig.22 Digital to analogue converters: (a) eight bit CMOS DAC (b) DAC 0800 (c) eight bit companding DAC (d) ZN426 DAC (eight bit) (e) eight bit DAC + latch (Ferranti).

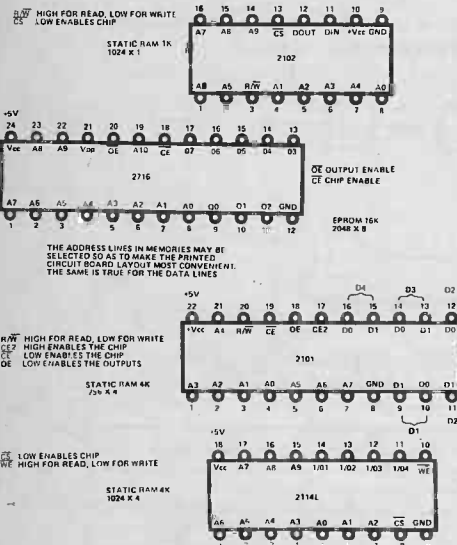
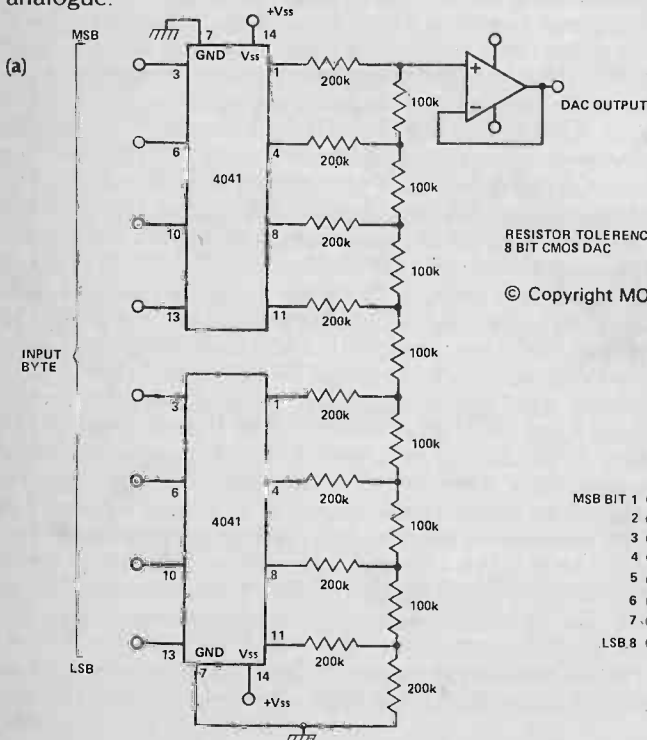


Fig.21 Typical memory configurations.

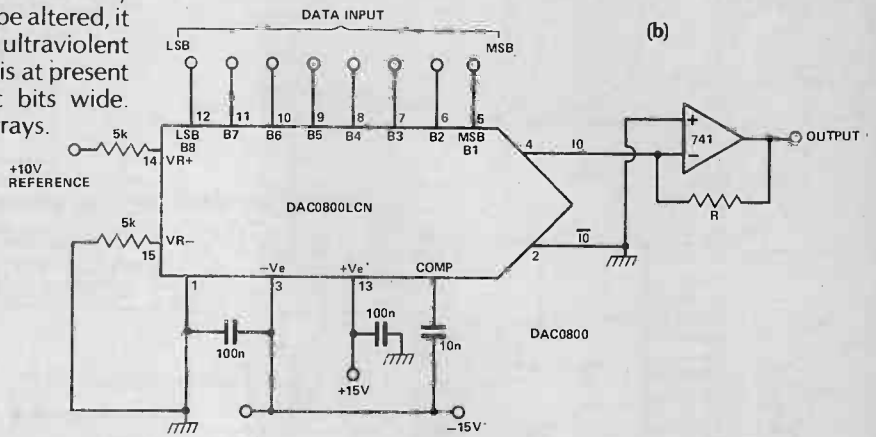
DACs

Once it is possible to interface analogue signals with digital hardware, a wide range of interesting products can be made. To input analogue information into a digital system an analogue-to-digital converter (ADC) is needed. A digital-to-analogue converter (DAC) is used to convert digital signals back into analogue.

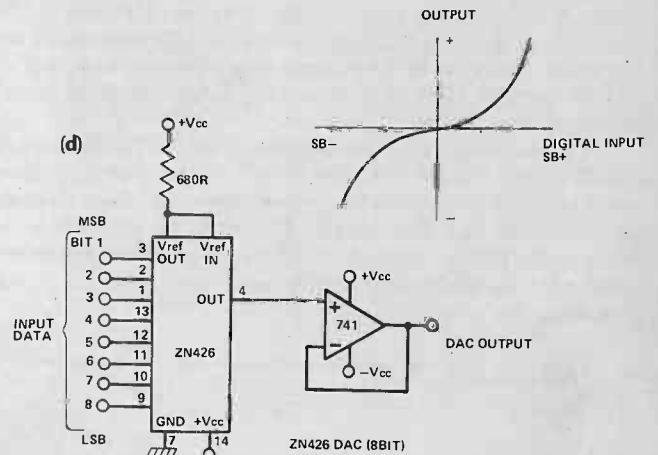
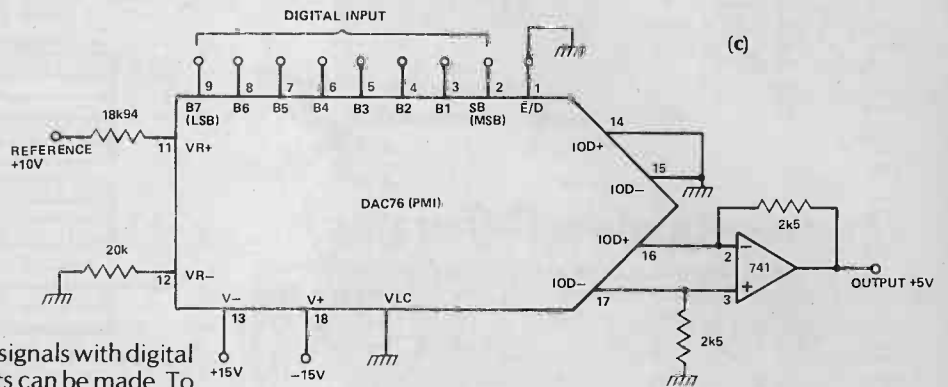


RESISTOR TOLERANCE 0.5%
8 BIT CMOS DAC

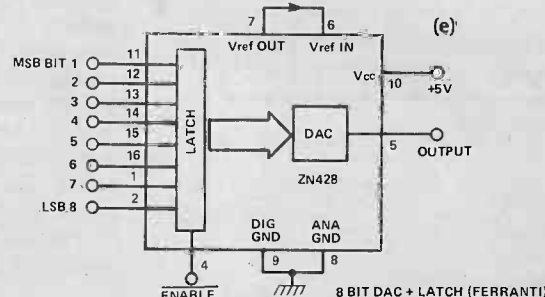
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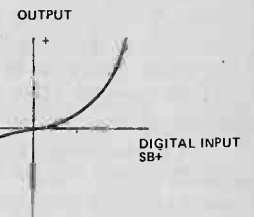
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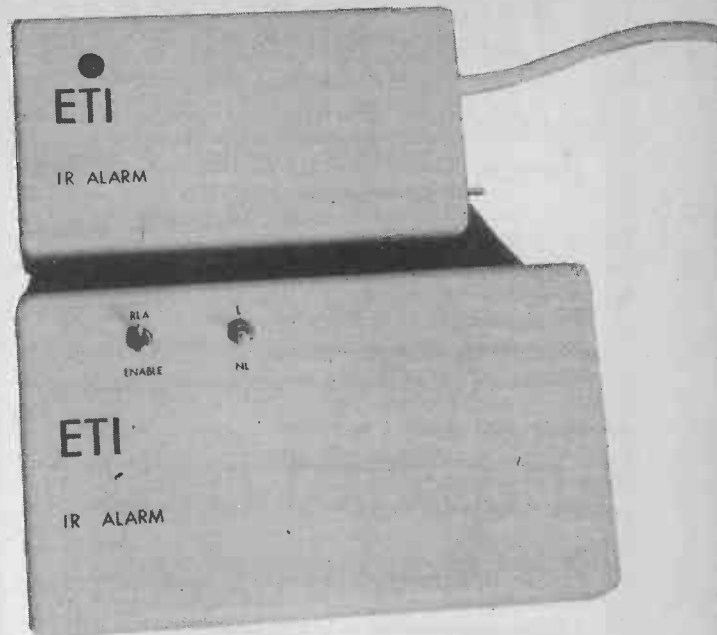
ZN426 DAC (8BIT)



8 BIT DAC + LATCH (FERRANTI)



INFRA~RED INTRUDER ALARM



This novel relay-output dual-beam infra-red alarm has an exceptionally high degree of false-triggering immunity and a useful range of about 10 metres. Design by Ray Marston. Project development by Steve Ramsahadeo.

This unusual infra-red beam alarm project has a maximum useful range of about 10 m and can form the basis of a first-class domestic or commercial security alarm system. The project comprises two units — an infra-red transmitter and an IR receiver with a relay output. Both of our prototype units are mains powered. The receiver unit contains facilities for operating the relay in either the latch or non-latch mode and for externally disabling the relay (for 20 S) via concealed 'by-pass' switches so that authorised persons can pass through the beams without activating the alarm.

The most unusual feature of our alarm system is the use of a dual-beam infra-red link. The two beams are spaced a few inches apart and both beams must be broken simultaneously to operate the alarm. Our system thus responds only to objects greater than the dual-beam size and cannot normally be false-triggered by moths or other insects passing through the beams or settling on the transmitter or receiver diodes.

IR-Beam Principles

Infra-red beam systems present a certain paradox in that the beam is not particularly directional (the transmitter and receiver do not need to be pointing directly at one another) yet the actual 'link' is highly directional and can be broken by a matchstick-sized obstruction placed anywhere along the link. To understand this paradox, try the following simple test.

Pick out a spot-sized object (a spot of paint or a screw head, etc). Now move around the room, noting that the object is visible from many different angles and that the visual communication beam is thus not particularly directional. Now, from any convenient viewing position, look at the object with one eye only and move a finger into the line of sight. The object is obscured — the visual link is thus highly directional. This is a good analogy of a conventional single-beam IR system, with the object acting as a single IR source and the eye as a single IR detector. This system is susceptible to false-triggering by moths or other small insects that stray into the beam or settle on the transmitter or receiver diodes.

Make Mine A Double

Now take the above visual test a bit further and pick out two spot-sized objects that are spaced roughly 7.5 cm apart and again check that they are visible from many different angles. Now look at the objects with *both* eyes and try to break the visual link by moving various items into the line of sight. You'll notice that the visual link can only be broken by a solid item with a width greater than the spacing of the two objects (7.5 cm), but that this item can break the link if placed anywhere along the line of sight.

This latter test is a good analogy of our dual-beam alarm system, with the two object spots acting as the two IR sources and the two eyes acting as the two IR detectors. Our system can only be activated by objects greater than a certain size and cannot normally be false-triggered by moths or other insects that stray into the beams or settle on the transmitter or receiver diodes. The beams are not unduly directional and do not require the use of lenses to complete the IR link, so installation is simply a matter of roughly pointing the transmitter and receiver towards each other.

Transmitter Construction

The transmitter construction should present few problems. We used two PCBs on our prototype, one for the mains power supply and the other for the actual transmitter circuit. Take the usual precautions over component polarity when assembling the boards and use sockets when mounting the two ICs.

When PCB construction is complete, make all necessary inter-connections, taking special care to ensure that the two infra-red LEDs and LED 1 are fitted with the correct polarity. Now switch on. If all is well, LED 1 will glimmer dimly, indicating correct transmitter action. If you have a 'scope you can check that the correct output waveform is generated across the two IR LEDs.

The completed unit can now be fitted in a suitable case, with the two IR LEDs pointing out from the box front. The IR

LED spacing determines the minimum object size that will be detected by the system; we used a spacing of about 4 cm on our prototype unit.

Receiver Construction

The receiver unit also uses two PCBs, one for the power supply and one large board for the preamp/main receiver. Some care is needed in the construction of the large board, due to the use of a compact layout and miniature components.

When construction of the boards is complete, fit them into a suitable case, together with T1, and make all necessary interconnections, taking special care to ensure that the two IRDs are connected with the correct polarity. The connections between the IRDs and the large PCB should be kept as short as possible to avoid unwanted pick-up. The IRDs should be mounted on the front of the cases, with the same spacing as used for the transmitter IR LEDs.

Setting Up

When construction is complete, set PR1 and PR2 to mid-value and enable the relay in the non-latching mode. Now space the Tx and Rx a metre or two apart, roughly facing one another, and turn the receiver on, but not the transmitter. The relay (RLA)

and LED 1 should turn on after a delay of about 20 S, indicating that no IR signal is being received.

Now turn on the transmitter and check that the relay and LED 1 turn off. Reduce the setting of delay control PR1 until relay 'chatter' starts to occur, accompanied by flashing of LED 1, and then turn PR1 back until the chatter/flashing ceases. This point marks the minimum delay setting that can be used with the system.

Now temporarily cover (with a finger) the face of one of the IRDs, reduce the setting of sensitivity control PR2 until RLA/LED 1 turn on and then turn PR2 back slightly past the point at which both components turn off. You should now find that RLA/LED 1 turn on only when both IR beams are broken simultaneously. The switch-on delay can at this stage be increased beyond the minimum established value if required.

Installation

Installation of the alarm system is simplicity itself. Merely space the Tx and Rx the required distance apart (up to several metres), point them roughly towards each other and then adjust sensitivity control PR2 until the required switching action is obtained. Hidden bypass switches (PB1 and PB2) can, if required, be placed on either side of the beam to allow authorised access.

BUYLINES

The infra red diodes and relay (RL6 12V) are available from Watford Electronics.

The PCB mounting transformer used in the transmitter can be obtained from Verospeed Electronics phone 10703-618525.

Vero cases have eyes! The two IR LEDs and IR detectors are mounted in the case ends.

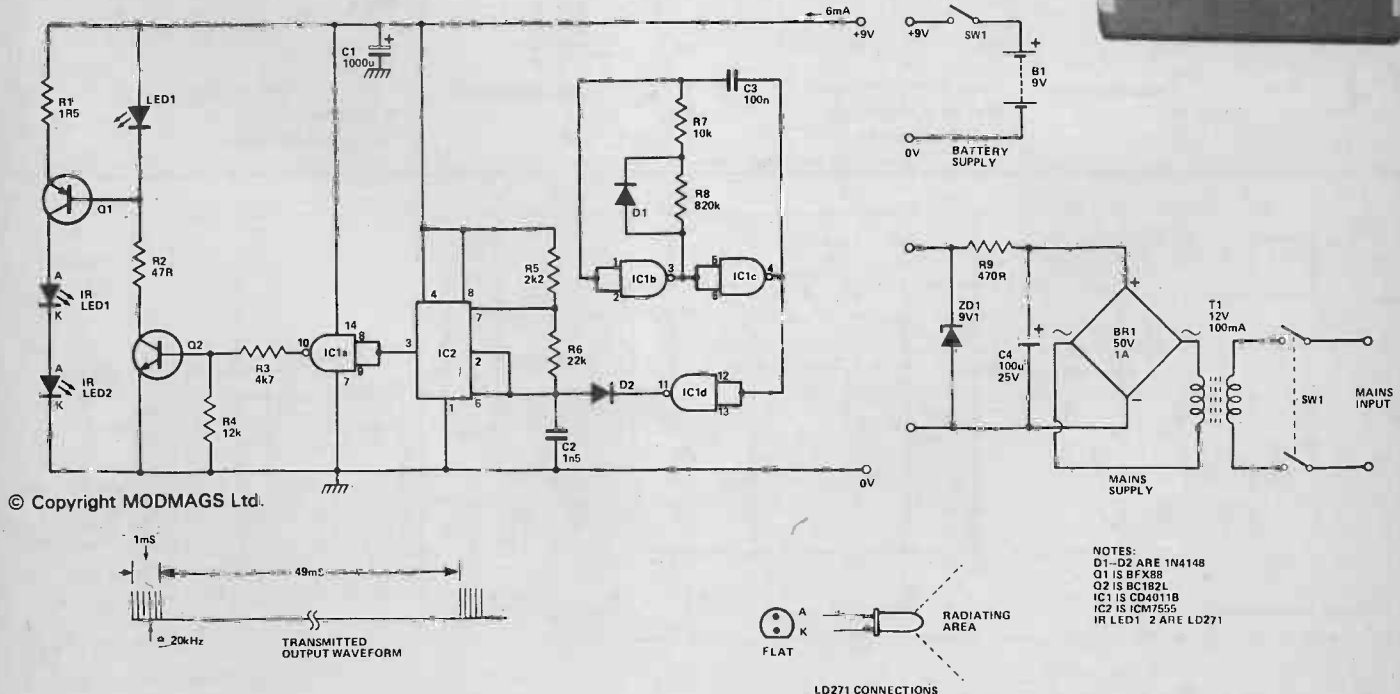
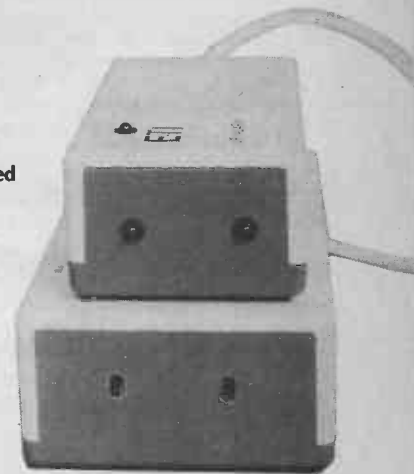


Fig.1 Circuit diagram of the transmitter and its own power supply.

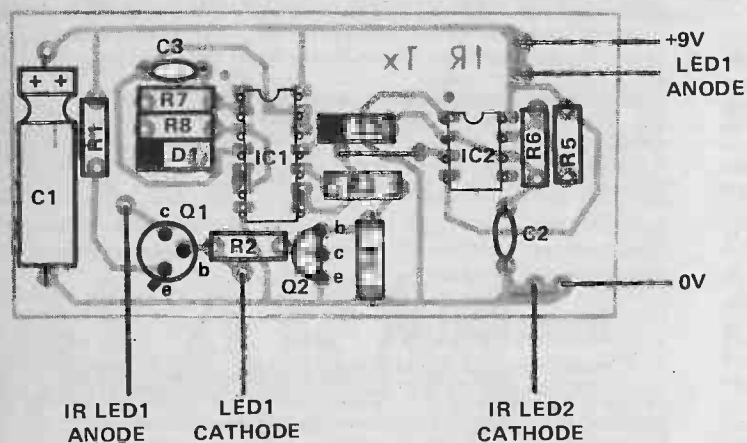


Fig.2 Transmitter component overlay.

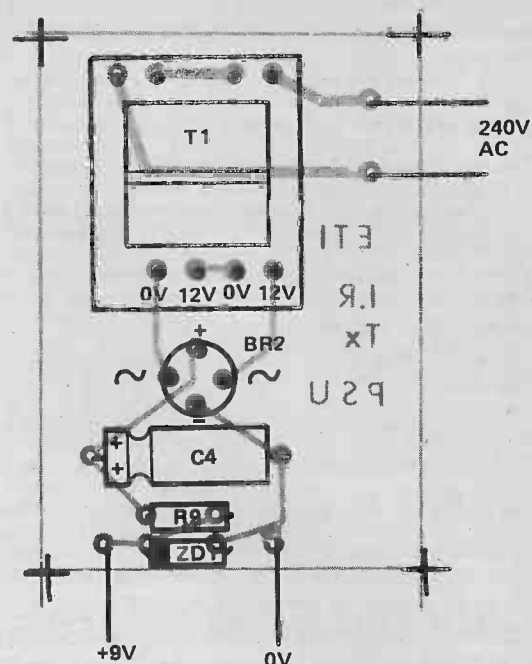


Fig.3 Transmitter power supply component overlay.

PARTS LIST

Resistors All 1/4

| | |
|----|------|
| W, | 5% |
| R1 | 1R5 |
| R2 | 47R |
| R3 | 4k7 |
| R4 | 12k |
| R5 | 2k2 |
| R6 | 22k |
| R7 | 10k |
| R8 | 820k |
| R9 | 470R |

Capacitors

| | |
|----|-------------------------|
| C1 | 1000u 16 V electrolytic |
| C2 | 1n5 polycarbonate |

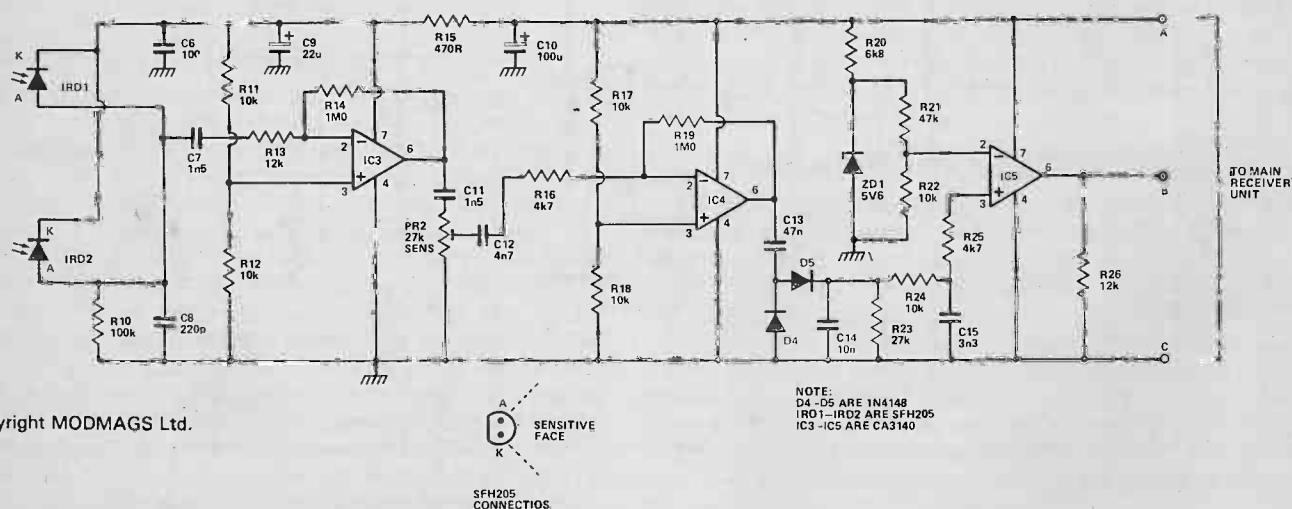
| | |
|----|------------------------|
| C3 | 100n polycarbonate |
| C4 | 100u 16 V electrolytic |

Semiconductors

| | |
|-------------|-----------|
| IC1 | CD4011B |
| IC2 | ICM7555 |
| Q1 | BFX88 |
| Q2 | BC182L |
| IR LED 1, 2 | LD271 |
| BR1 | 50 V, 1A |
| D1,2 | 1N4148 |
| ZD1 | 9V1 BZY88 |

Miscellaneous

| | |
|-----|-----------------------|
| T1 | 12 V 100 mA |
| SW1 | DPDT miniature toggle |



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Fig.4 Circuit diagram of the receiver preamp.

HOW IT WORKS

The IR transmitter beam signal comprises 1 mS bursts of 20 kHz pulses, repeated at 50 mS intervals. The transmitter generates peak IR diode currents of 600 mA but, because of the wide mark/space ratio (1:50) of the transmitter signal, the *mean* transmitter current is a mere 6 mA. This current can be provided by either a battery or a mains-derived supply. Both options are shown in the circuit diagram.

The basic transmitter signal is generated by IC1 and IC2. IC1b-IC1c are wired as a non-symmetrical astable multivibrator producing alternate periods of 1 mS and 49 mS. The output of this astable is buffered by IC1d and used to gate 20 kHz astable IC2 on and off via D2. The resulting waveform is used to gate 600 mA constant-current generator Q1-R1-LED 1 on and off via IC1a and Q2 and thus feed high energising currents to the two series-connected infra-red transmitter diodes. The high-current transmitter pulses are derived from storage capacitor C1.

The two infra-red detector diodes are connected in parallel and wired in series with R10, so that the detected IR signal is developed across R10. The signal is amplified by IC5. The output of IC4. These two amplifier stages have their responses centred on 20 kHz, with third order low-frequency roll-off provided via C7-11 and C12 and with similar high-frequency roll-off provided by C8 and the internal compensation capacitors of the two ICs.

The amplified output of IC4 is rectified and smoothed by voltage-doubler D4-D5 and associated C-R networks and fed to voltage-comparator IC3, fed to sensitivity control RV2 and then further amplified by IC5 (at point B) takes the form of a series of repetitive positive-going pulses when a strong IR beam signal is present, or of a logic 0 signal when the beam is broken. The B signal is passed to the main receiver unit.

To understand the operation of the main receiver unit, assume initially that the emitter of Q1 is shorted to ground. The output signal of the preamplifier circuit is fed to point B and rectified and smoothed by the D1-C1-R1 PR1 network and the resulting DC signal is inverted by

IC1a and fed to one input terminal of composite AND gate IC1b-IC1c. This signal takes the form of logic 0 if the IR beam is unbroken, or logic 1 if the beam is broken. The response time to a break can be varied via PR1.

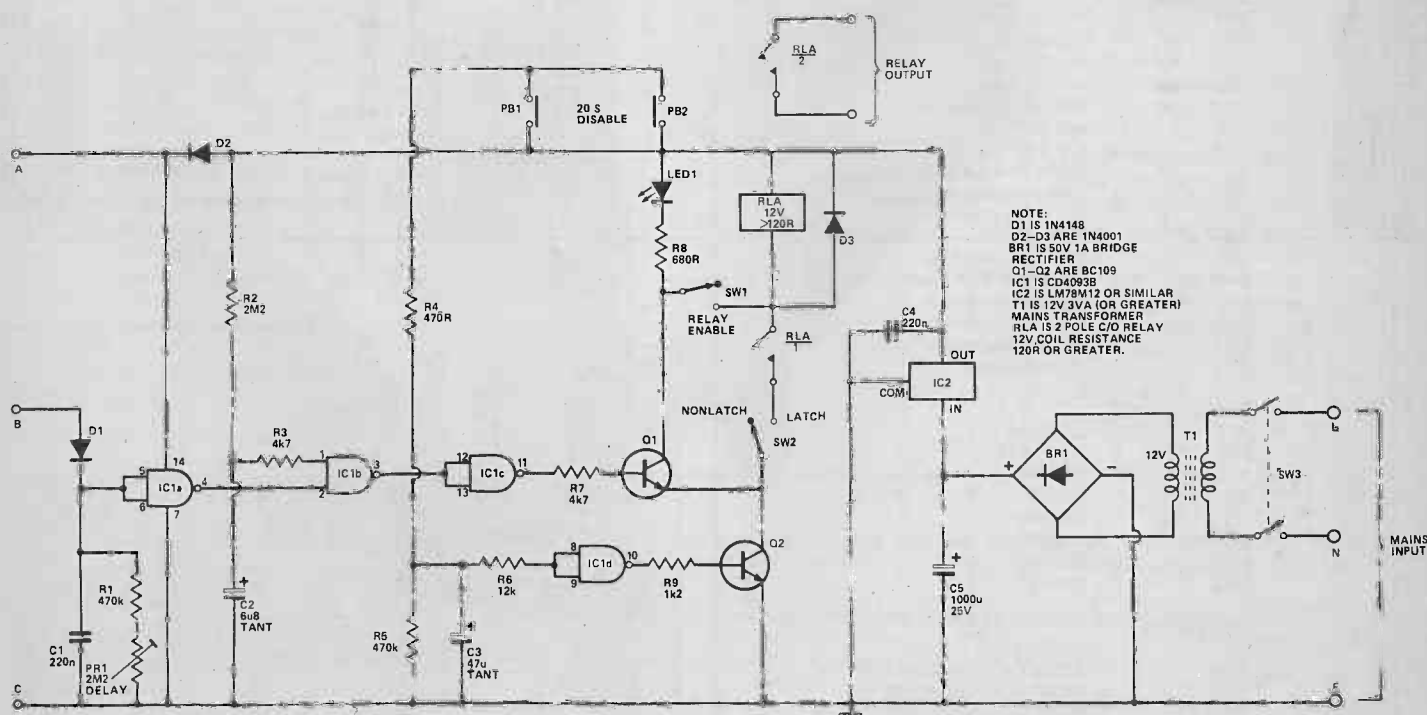
The second input to the composite IC1b-IC1c AND gate is derived from the positive supply line via the R2-C2-R3 switch-on delay network and is normally high (within a few seconds of supply switch-on). The output of the AND gate is fed to the base of relay driving Q1 via R7. SW1 can be used to connect (enable) or disconnect the relay from Q1 collector.

Thus, under normal circumstances, the presence of a beam signal results in the IC1a input to the AND gate being low, in which case the AND gate output is low and Q1 and RLA are off. When the IR beam is broken the IC1a input to the AND gate goes high, so the AND gate output goes high and drives Q1 and RLA and LED 1 on (assuming that SW1 is closed). An exception to this action occurs for a brief period following power switch-on of the receiver unit, when the relay-driving circuit is effectively disabled via the R2-C2-R3 delay network. Note that the relay can be operated in either the latching or the non-latching mode via SW2.

In the description above we've assumed that the emitter of Q1 is shorted directly to ground. In practice, however, the connection to ground is made via Q2 collector. Normally, the input to IC1d is low, so IC1d output is high and Q2 is driven to saturation via R9 and acts as an effective short circuit, so the above action is normally obtained. Q2 can, however, be cut off at any time, thereby disabling the relay circuit, by momentarily closing PB1 or PB2. This action causes C3 to charge rapidly via R4 and cut off the Q2 base drive via IC1d. The base drive is restored roughly 20 S after the release of PB1/PB2 as the C3 charge leaks away via R5. This 20 S disable facility allows an authorised person to pass through the IR beam without activating the alarm by first momentarily operating one of the PB1/PB2 buttons.

The complete IR receiver circuit is powered from the mains via the T1-BR1-C5 network and the IC2 12V regulator chip.

Fig.5 Circuit diagram of the receiver and power supply.



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Computer Pandas

Next time you put the wind up the local Bobbies — beware — the glassy-eyed passenger could be staring at Plessey's new Universal Mobile Communications Terminal (UMCT). It's a dashboard-mounted keyboard and VDU that allows transmission of digital data and computer information retrieval over speech band radio from all types of vehicles. Units are already in use in Canada and the US and are undergoing field trials in Sweden.

A UMCT operator can transmit data at 4800 bits per second, so that a

full screen of 315 characters can be transmitted in 0.6 s. 300 stations (vehicles) can, therefore, comfortably operate on one radio channel. The system features unique authorisation, automatic re-transmission, memory storage, graphic transmission and elaborate emergency facilities.

Information including road maps, car registration details, etc. can be accessed from a central data base in as little as 2 s. As the UMCT doesn't need any extra black boxes and is connected to the vehicle by only two leads (power and radio), it can be transferred from vehicle to vehicle in a matter of seconds. If necessary, it can even be plugged into the car cigarette lighter!



Cruising

EnviroSystems are now supplying what they claim to be the world's first 100% electronic cruise control system. Cruise controls aren't new, but existing units require adaptor kits for each make and model of car and fitting usually involves cutting into the vacuum line to the vacuum servo unit.

EnviroSystems' Cruise Sentry uses a small electric servo unit to accurately control the throttle (no cutting into the vacuum line) and picks up speed-related pulses from the coil. The unit is suitable for most

vehicles (4/6/8 cylinder, standard or electronic ignition), doesn't need fine tuning, is virtually maintenance free and can be fitted in about two hours.

Cruise Sentry can be set to keep your car at a constant speed, but it can be easily over-riden in one of three ways for safety. If you need to accelerate for any reason, Cruise Sentry will automatically resume the present speed. The preset speed value can be changed while driving without disengaging the system.

Cruise Sentry is available directly from EnviroSystems Ltd, Hampfell Road, Grange-over-Sands, Cumbria LA11 6BE. The recommended retail price is £78.50 + VAT.

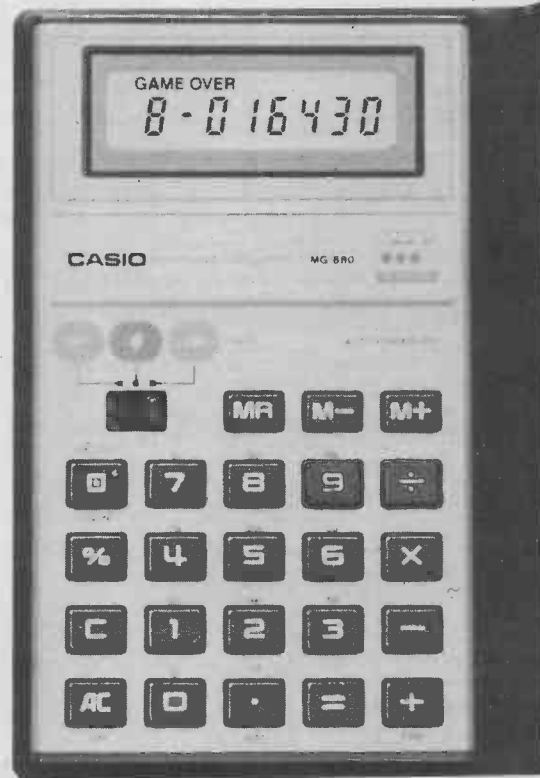
The Numbers Game

Casio calculators have done a lot of things in their time. Between showing the time, waking you up when it's time to go home and playing tunes, they've even been known to tot up a few digits quicker than you can pull out your slide rule. A slide rule is an antique calculating device (for those of you too young to remember). This Casio, the MG770, calculates (eight digits capacity with independent memory and perfect percent), plays a 30 s pre-programmed chunk of 'When the saints go marching in', plays any melody you care to hammer into it (in music mode

the keys sound 11 notes) and plays an electronic combat game.

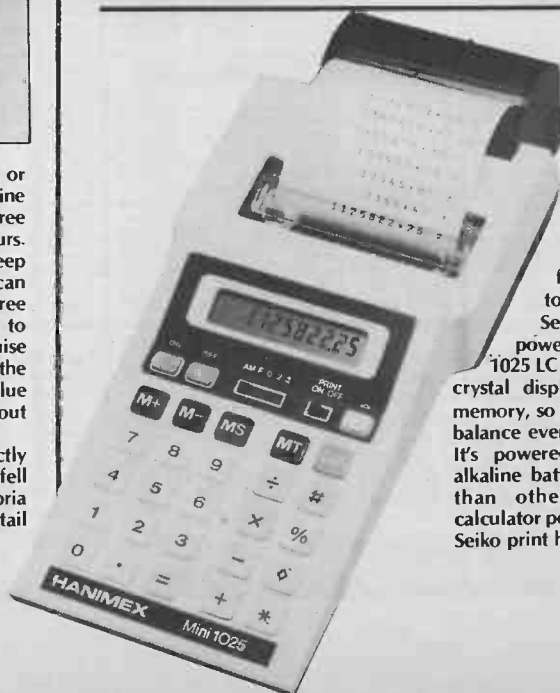
Throw the mode switch over to the game position and hit the game button. A series of random numbers move across the display. Use your aim button to match your defender with the intruder and daintily tread on the fire button to wreak murder and mayhem. The game gets faster until it's all a blur and it displays your score after every game.

The MG770 is credit-card size (85 x 54 mm), but if you prefer something a bit bigger, the MG880 has all the same features in a wallet-size case (114 x 68 mm). Both are supplied with a leatherette case. Prices? The MG770 should cross the counter for less than Casio's RRP of £14.95 and the MG880 for less than £12.95.

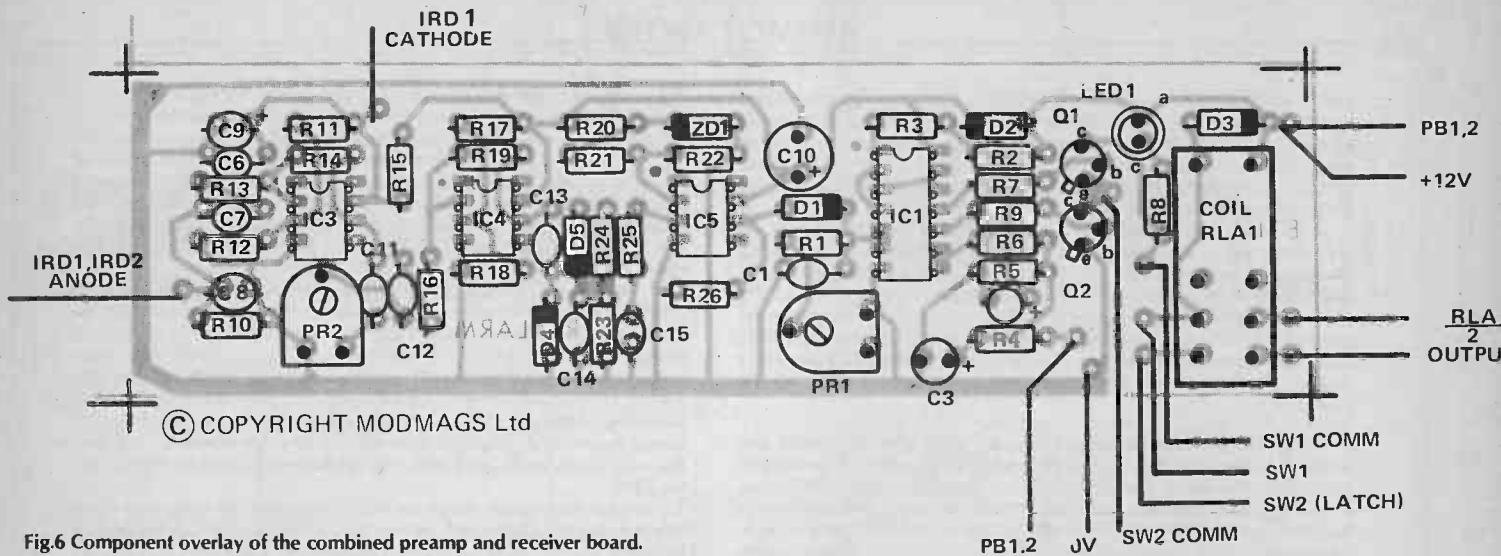


Mini Printout

The new Hanimex Mini 1025LC produces a printed record of your calculations faster than a large desktop machine, using a new Seiko high speed, low power drain print head. The 1025 LC feature a 10 digit liquid crystal display with a non-volatile memory, so it remembers your bank balance even when it's switched off. It's powered from four size AA alkaline batteries, which last longer than other print and display calculator power units because of the Seiko print head.



PROJECT : Infra Red Alarm



PARTS LIST

RECEIVER

Resistors all 1/4 W 5%

| | |
|--------------------|------|
| R1,5 | 470k |
| R3,7,16,25 | 4k7 |
| R4,15 | 470R |
| R6,13,26 | 12k |
| R8 | 680R |
| R9 | 1k2 |
| R10 | 100k |
| R11,12,17,18,22,24 | 10k |
| R14,19 | 1M0 |
| R20 | 6k8 |
| R21 | 47k |
| R23 | 27k |

Potentiometers

| | |
|-----|--------------------------|
| PR1 | 2M2 miniature horizontal |
| PR2 | 22k miniature horizontal |

Capacitors

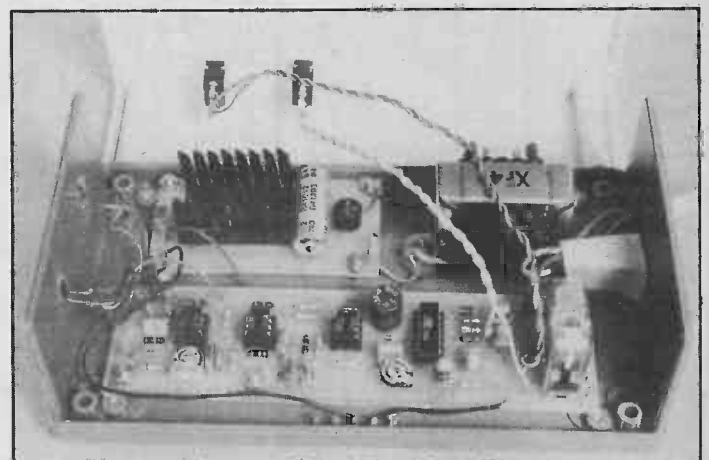
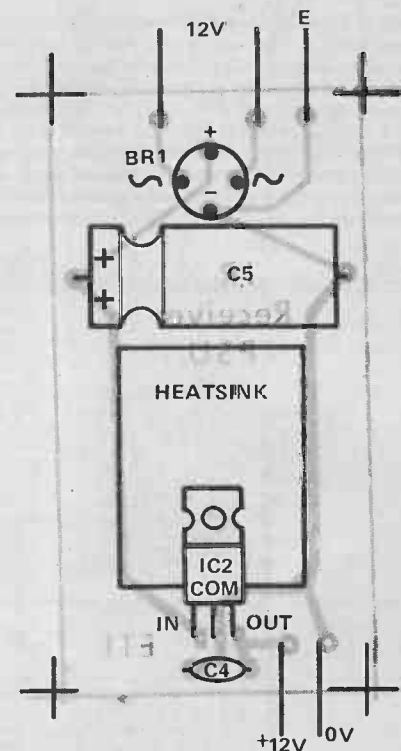
| | |
|-------|-------------------------|
| C1,4 | 220n polycarbonate |
| C2 | 6u8 25 V tantalum |
| C3 | 47u 16 V tantalum |
| C5 | 1000u 16 V electrolytic |
| C6 | 100n polycarbonate |
| C7,11 | 1n5 polycarbonate |
| C8 | 220p ceramic |
| C9 | 22u 25 V tantalum |
| C10 | 100u 16 V PCB type |
| C12 | 4n7 polycarbonate |
| C13 | 47n polycarbonate |
| C14 | 10n polycarbonate |
| C15 | 3n3 ceramic |

Semiconductors

| | |
|------------|-------------|
| IC1 | CD4093B |
| IC2 | 7812 + 12 V |
| IC3,4,5 | CA3140 |
| Q1,2 | BC109 |
| D1,2,3,4,5 | 1N4148 |
| D2,3 | 1N4001 |
| IRD1,2 | SFH205 |
| BR1 | 50 V 1A |

Miscellaneous

| | |
|---|---------------------------|
| T1 | 12 V 3 VA |
| RLA | 2 Pole C/O 12 V 120R Coil |
| SW1,2 | SPDT miniature toggle |
| SW3 | DPDT miniature toggle |
| Verocase (Transmitter) order code 202-21030k. | |
| Verocase (Receiver) order code 202-21031G. | |



ETI



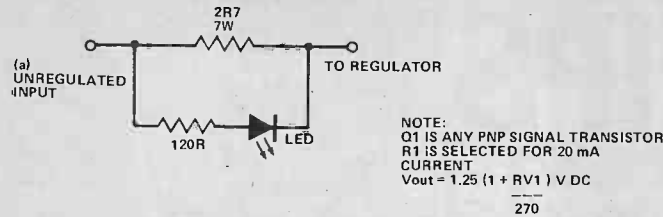
G. Durant, Selby

One of the inputs of IC1a is held high by a 3M9 resistor. If the touch plates are bridged, the input is pulled low by a 100k resistor. This triggers a latch formed by IC1a and b. The output of the latch is

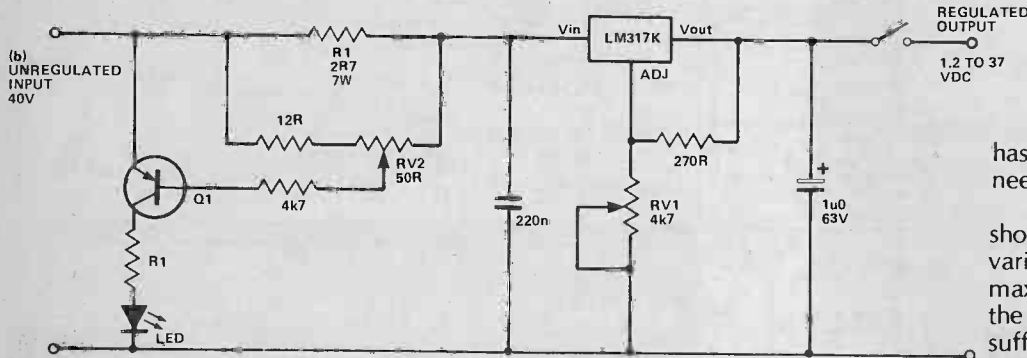
If another switch is activated, the first switch is reset and its output goes low again. At switch on, C1 sends a brief

The touch switch can be used on a radio for wave changing, or on a stereo amplifier as an input selector where noiseless switching can be achieved.

ETI is prepared to consider circuits or ideas submitted by readers for this page. All items used will be paid for. Drawings should be as clear as possible and the text should preferably be typed. Circuits must not be subject to copyright. Items for consideration should be sent to ETI TECH-TIPS, Electronics Today International, 145 Charing Cross Road, London WC2H 0EE.



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has been approached, eliminating the need for a meter.

In both circuits, component values shown are suitable for the LM317K variable voltage regulator which has a maximum current of 1.5 A. In circuit (a) the voltage drop across R1 will be sufficient to light the LED when 1.5 A is drawn. In circuit (b) the idea is developed to allow the current at which the LED is lit to be adjusted. Thus the calibration of RV2 enables the current flowing to be estimated with sufficient accuracy for most purposes.

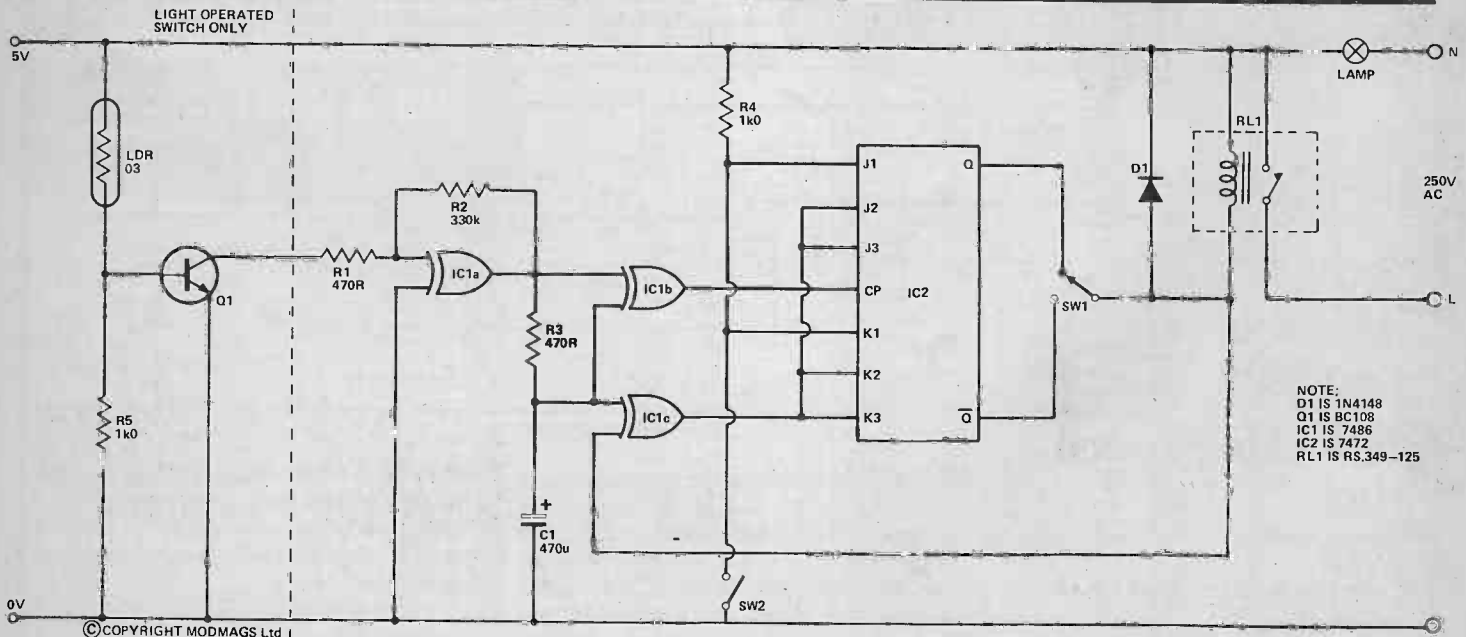
R1 will also provide some protection to the circuit in the event of a short circuit output.

Regulator Over-Current Indicator

H. Polecat, Colnbrook

Modern IC regulators are so accurate that calibrating the knob of the adjust potentiometer is all that is necessary to

ensure the correct output voltage. Many designs still include an expensive analogue meter, if only to indicate that the output voltage has not collapsed due to exceeding the current rating of the regulator. The circuits shown give two methods of using a LED to indicate that the current rating of the power supply



Automatic Porch Light

S. Grosvenor, Liskeard

We all know that automatic porch lights can be very useful, but they do have problems. For example, if they are left on all night they waste power or, if the light is switched off, the circuit cannot switch itself on the next day unless it is reset.

The circuit described below allows the light to be switched off at night and still work the next day. Although it was designed primarily for a porch light, it could be adapted for use on any automatic switching system that only has a permanent over-ride.

The input to R1 is cleaned up by IC1a acting as a Schmitt trigger. IC1b is a frequency doubler, producing a clock pulse for every change in input state. IC2 is a flip-flop with both outputs

connected to SW1. IC2 and SW1 work together, allowing one either to activate or de-activate relay RL1. IC1c works as a lock-out device, which stops the system getting out of phase, ie the light turning on at dawn and off at dusk. SW2 overrides the automatic circuit by locking the flip-flop in whichever state it is in at the time. A power failure could cause the system to get out of phase, but it will self-correct at the next clock pulse, or it can be corrected manually by throwing SW1.

SOUND PRESSURE LEVEL METER

Another first from ETI. An accurate and modestly priced sound-level meter with built-in calibrator.

An essential item for setting up true hi-fi systems, our meter has switch selection of either 'sound-level' or 'loudness' readouts.



Sound level meters have two obvious applications which are of interest to the electronics enthusiast or engineer. First, they can check absolute values of sound level or loudness to see if they conform to legal or medical requirements, e.g. to check that a neighbour is creating a legal nuisance with his home disco before prosecuting him, or checking that the loudness ('A' weighted sound level) of a working environment really is in excess of the 90 dB recommended maximum (or whatever) before calling in a factory inspector, etc.

The second major application is as an aid in setting up graphic equalisers in hi-fi systems, to ensure that the system produces equal sound levels at all frequencies at the designated mean listening point of the room, thereby fully integrating the room into the system.

Trouble is, commercial sound-level meters cost a small fortune, and home-built ones need to be calibrated against precisely known sound sources.

ETI to the rescue

The ETI sound-level meter has been designed to overcome cost and calibration problems. Our unit is designed around a special-purpose but modestly priced precision microphone insert. The complete meter covers 30-120 dB sound-level, has a built-in calibration facility that needs to be adjusted only once a year and has a typical accuracy better than 2 dB. The meter has a built-in 'A' weighting filter that can be switched in to give readings of loudness, or out to give readings of true sound level. The unit is powered from two 9 V batteries and consumes a total current of about 10 mA.

The instrument incorporates an eight-position switch-selected attenuator, calibrated from 40 dB to 110 dB in 10 dB steps. The actual sound-level readout is obtained on a linear moving coil meter with a logarithmically calibrated scale (in dB steps) to cover the range -10 dB to +10 dB. The microphone is simply placed at the desired monitor point and the switched attenuator is then adjusted to give a reading somewhere within the calibrated scale of the meter. The sound-level is then equal to the sum of the attenuator and scale readings, e.g. an attenuator reading of 70 dB and a scale reading of 4 dB corresponds to a sound level of 74 dB.

Construction

It should be noted that the instrument is designed to work ONLY with the microphone unit specified in Buylines. No other microphone type or make is suitable. Also note that all resistors used are 5% or better types.

Start the construction by assembling the microphone unit, taking care to wire R1 and Q1 directly to the microphone output terminals. Connect the completed unit to a suitable cable by passing the cable leads through one of the holes in the side of the microphone head and then epoxy the leads firmly to the inner side of the head. The electronics can then, if required, be encapsulated in wax or resin.

Next, take a standard 100uA moving coil meter and re-calibrate its scale with dB(log) divisions as shown. Then proceed with the construction of the main circuit board, as shown by the PCB overlay.

Fit the completed PCB into a suitable case and make the interconnections to the four switches and the meter, etc., taking special care to keep all leads as short as possible. On our prototype, we've used a 3-pin DIN socket to accept the microphone input, with R32 wired directly across its A and C terminals. Note that the connection between B and C2 must be as short as possible.

When construction is complete, temporarily short the 'a' and 'c' pins together on the PCB, switch the unit on and then trim PR1 to obtain FSD reading on the meter. Now switch off, remove the 'a' to 'c' short and wire pin 'a' to pin 'b'. Connect the microphone to the meter. The instrument is now ready for use.

Using The Unit

We've designed our unit to give maximum versatility and have, therefore, used a free-ranging (rather than built-in) microphone. This means that, when using the unit, you can either hold the microphone in one hand, or place it remote from the meter, or fix it to the meter body with a clip or sticky pad, etc.

If you want to use the instrument as a sound level meter (to indicate absolute sound pressure levels when setting up a hi-fi system, etc), set SW2 in the FLAT position. If you want to use the instrument as a loudness-level meter (to indicate 'nuisance' noise level, etc), set SW2 in the A Weighted position. Whichever way you use it, note that actual dB values are equal to the sum of the SW1 and meter readings.

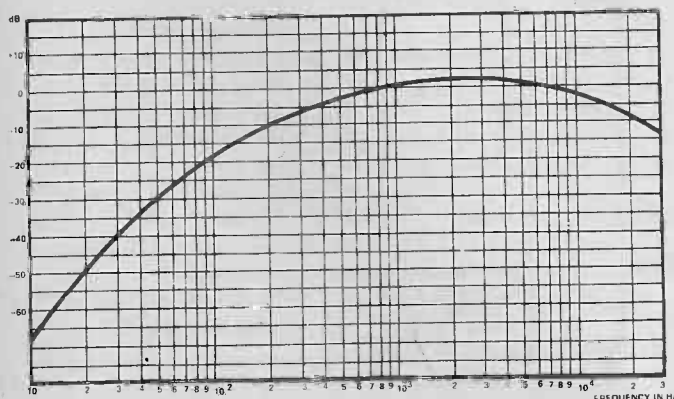
If your hi-fi system is fitted with a parametric equaliser, you can use the meter to aid the setting up of the system. First, place or fix (with a sticky pad, etc.) the microphone unit into the central listening point of the room. Now feed a 1 kHz signal into the system and adjust the sound level until a reading of 80 dB (or some other convenient reference level) is obtained on the meter when it is set in the 'FLAT' mode. Now sweep the input signal through the entire audio band (without changing the level of the input signal) and use the equaliser controls to maintain the meter readings as close as possible to 80 dB throughout the entire band. Do not be surprised if you find that your room exhibits acoustic peaks and troughs for up to 20 dB when the equaliser is switched out of circuit!

Sound Intensity And dBs

The human ear perceives sounds as a series of rapid variations of air pressure. The RATE of pressure variation is recognised as sound pitch, tone or frequency. The MAGNITUDE of pressure variation is recognised as sound level or intensity.

The human ear/brain combination has a poor ability to recognise absolute values of tone or frequency, but is very sensitive to changes in the logarithmic ratios of succeeding tones. Similarly, it has a poor ability to recognise absolute values of sound level or intensity, but is quite sensitive to changes in the logarithmic ratios of succeeding sound intensities. Some logarithmic ratios are usually expressed in terms of decibels (dB) it makes sense to express relative sound levels in terms of dB. Thus, if sound A is 'x' times more intense than sound B, we can express this fact by saying that sound A is so-many dB up on sound B.

Note from the above paragraph that, when quoting sound levels (or any other quantity) in terms of dB, it is necessary to state or know the quantity to which the dB value is referenced. In practice, absolute sound levels are now universally implicitly referenced to the so-called 'threshold of hearing', the minimum sound intensity or pressure that can be detected by a person with normal hearing. This '0 dB' reference level corresponds to a sound power level of 10^{-12} Wm^{-2} (10^{-10} uW/cm^2) or a sound pressure level of $0.0002 \text{ dynes cm}^{-2}$ ($0.00002 \text{ Newton/cm}^2$).



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Fig.1 The response of the A-weighted filter.

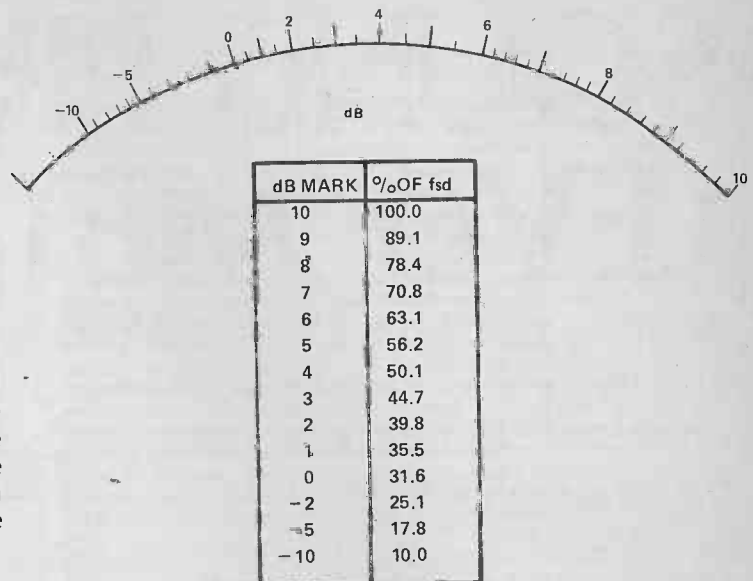


Fig.2 The meter scale (top) and a data table for hand-calibrating an existing linear meter scale.

Sound intensity is proportional to sound power (the analogue of electrical power) and proportional to the square of sound pressure (the analogue of electrical voltage). Thus, a sound level of 60 dB corresponds to a pressure increase of 1,000 or a power increase of 1,000,000 relative to the 0 dB values. Table 1 shows some examples of sound levels, with their pressures, relative energies and dB equivalents. Note that the human ear is able to accommodate the phenomenal max-to-min power ratio of 1,000,000,000,000:1, or a pressure ratio of 1,000,000:1.

Microphone Sensitivity

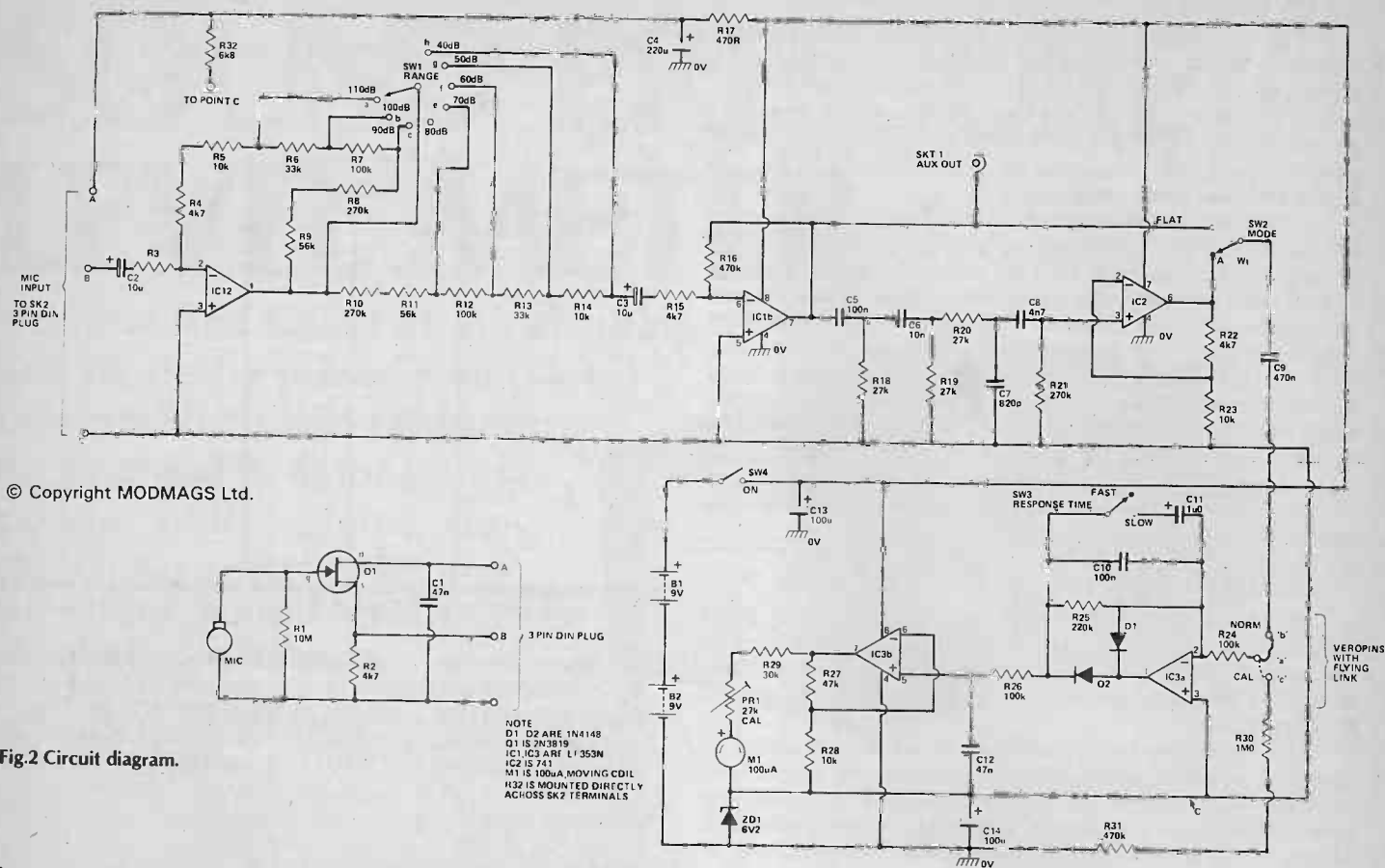
The electrical (voltage) output of most microphones is directly proportional to sound pressure. Thus, a 20 dB increase in the intensity of sound input will (ideally) result in a 20 dB increase in output voltage. Consequently, if the basic sensitivity of a microphone is precisely known, its output voltage can be directly related to the dB sound intensity scale.

Microphone sensitivity is almost invariably specified in terms of the output voltage obtained from a standard sound pressure level equivalent to conversational speech at 20 cm distance, this being equivalent to a pressure of one microbar (1 dyne cm^{-2}) or a sound intensity of 74 dB. The sensitivity may be quoted directly in terms of the output voltage obtained under this test condition or, rather confusingly, in terms of dB relative to 1 V (for example, and output of 1 mV may be expressed as -60 dB).

The microphone specified is designed for accurate sound measurement work and has a very tight sensitivity specification. Its nominal sensitivity is 1.41 mV (-57 dB), with a typical precision of 1 dB.

Loudness

Loudness is the subjective effect that a sound wave has on a listener and is dependent on both sound pressure and frequency, as demonstrated by the Robinson-Dadson equal-loudness curves. The ear has maximum sensitivity to frequencies around 3 kHz, its sensitivity falling off quite drastically at frequencies above 5 kHz or below 300 Hz. An analogue voltage-indicating meter can be made to exhibit a response approximating the loudness response of the human ear by feeding signals to the meter via an 'A' weighted filter with the response shown in Fig. 1. The ETI sound-level meter has a



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Fig.2 Circuit diagram.

built-in switch-selected 'A' weighting network, enabling the meter to give either sound intensity or loudness readings.

When a sound-level meter is used in the unweighted (flat) mode, it should be noted that the intensity and loudness readings coincide only at a test frequency of 1 kHz. On the loudness scale, a change of 10 dB corresponds to a doubling or halving of apparent sound level. The human ear can typically respond to a max-to-min loudness range of greater than 4000:1.

BUYLINES

Magenta Electronics Ltd have agreed to supply a full kit of parts including the M81 microphone case.
 Magenta Electronics Ltd.
 HC3, 98 Calais Rd
 Burton-on-Trent, Staffs
 DE13 0UL

| dB above threshold | Sound Intensity (Power) | | | Sound Pressure | | | LOUDNESS | | | |
|--------------------|-------------------------|------------|-----------------|-------------------|-----------------|-----------------|-------------------|----------------------|-----|----------------------|
| | Relative energy | $W m^{-2}$ | $\mu W cm^{-2}$ | Relative pressure | $dynes cm^{-2}$ | $Newton m^{-2}$ | Relative loudness | Loudness description | dB | typical examples |
| 120 | 10^{12} | 1 | 100 | 10^6 | 200 | 20.0 | 4096 | Deafening | 130 | Pain threshold |
| 100 | 10^{10} | 10^{-2} | 1 | 10^5 | 20.0 | 2.0 | 1024 | Very loud | 120 | Pneumatic drill |
| 80 | 10^8 | 10^{-4} | 10^{-2} | 10^4 | 2.0 | 0.2 | 256 | loud | 110 | Pop music group |
| 60 | 10^6 | 10^{-6} | 10^{-4} | 10^3 | 0.2 | 0.2 | 64 | Moderate | 100 | Underground train |
| 40 | 10^4 | 10^{-8} | 10^{-6} | 10^2 | 0.02 | 0.002 | 16 | faint | 90 | Factory, busy street |
| 20 | 10^2 | 10^{-10} | 10^{-8} | 10 | 0.002 | 0.0002 | 4 | Very faint | 80 | Noisy office |
| 0 | 1 | 10^{-12} | 10^{-10} | 1 | 0.0002 | 0.00002 | 1 | silent | 70 | Normal speech |
| | | | | | | | | | 60 | Large shop |
| | | | | | | | | | 50 | Quiet office |
| | | | | | | | | | 40 | Suburban home |
| | | | | | | | | | 30 | Public library |
| | | | | | | | | | 20 | Soft whisper |
| | | | | | | | | | 10 | Still country night |
| | | | | | | | | | 0 | Soundproof room |

Notes:

- For a sound to be perceptibly louder or softer, it must be changed by 3 dB.
- A noise twice as loud or half as loud is a change of 10 dB.
- Microphone sensitivity figures are normally quoted at a standard sound pressure of 1 microbar (1 dyne/cm²), which corresponds to a sound level of 74 dB or an air pressure variation of approximately 0.0001 atmospheres.

Table 1. Some examples of sound levels, with their pressures, relative energies and dB equivalents.

HOW IT WORKS

The microphone used in this project is a precision ceramic unit that is engineered to provide an output of 2.81 mV from a sound level input of 80 dB and 8.88 mV from 90 dB. The microphone has a high output impedance, so the Q1 JFET buffer is wired directly to the microphone output pins to provide a low impedance drive to the meter circuitry and avoid unwanted (hum) pick-up.

In essence, the unit acts as a multi-range AC voltmeter, with ranging provided by a switched-gain amplifier and with the meter scale marked in dB steps, with +10 dB corresponding to full scale and 0 dB corresponding to 31.6% of FSD: The basic meter has a full scale sensitivity (with the amplifier set to unity gain) of 888 mV and a sensitivity of 281 mV at the 0 dB mark.

Suppose, then, that the microphone is receiving a sound level of 80 dB, at which level it gives an output of 2.81 mV. The meter can be made to indicate this level at the 0 dB mark by switching the amplifier to give a gain of 40 dB, at which gain the range switch is marked as 80 dB, or at the 410 dB mark by giving a gain of 50 dB, at which gain the range switch is marked as 70 dB. The actual sound level is thus indicated by the sum of the range switch marking and the meter scale indication.

IC1a and IC1b are wired as the switched-gain amplifier, with overall

gain variable in eight 10 dB steps via SW1. Gain is 10 dB when SW1 is set to the 110 dB position and 80 dB when SW1 is set to the 40 dB position. The output of the amplifier is made externally available (for feeding into an audio amplifier, etc.) at SKT 1 and is also fed (either directly or via the IC2 filter network) to the input of the IC3 AC voltmeter circuit via SW2. The IC2 filter has an A weighted response, with unity gain at 1 kHz.

In the IC3 AC voltmeter circuit, IC3a is wired as a precision AC/DC converter, with smoothing or integration provided by C10 and C11. The output of the converter is fed to non-inverting DC amplifier IC3b, which drives the 100 uA moving-coil indicating meter via R29 and PR1. The meter circuit needs an input (from pin 7 of IC3b) of about 5 V for a FSD reading. The design of the complete AC voltmeter circuit is such that the meter gives a FSD reading from an AC input (to R24) of (ideally) 888 mV. In practice, our circuit is DC coupled throughout and we can drive the meter to full scale by feeding a DC current of $-3.95 \mu\text{A}$ into R24. This current can be obtained from the -6V2 rail via R30-R31 by shorting the 'a' and 'c' pins when initially calibrating the circuit.

The complete meter is powered from two 9 V batteries and typically consumes 10 mA. The common input or reference line (C) to the circuitry is derived from 6V2 zener ZD1.

PARTS LIST

Resistors 1/4 W 10%

| | |
|--------------|------|
| 1R1 | 10M |
| R2,3,4,14,22 | 4k7 |
| R5,14,23,28 | 10k |
| R6,13 | 33k |
| R7,12,24,26 | 100k |
| R8,10,21 | 270k |
| R9, 11 | 56k |
| R16,31 | 470k |
| R17 | 470R |
| R18,19,29 | 27k |
| R25 | 220k |
| R27 | 47k |
| R29 | 39k |
| R30 | 1M0 |
| R32 | 6k8 |

Potentiometers

| | |
|-----|--------------------------|
| PR1 | 22k miniature horizontal |
|-----|--------------------------|

Capacitors

| | |
|--------|------------------------------|
| C1 | 47n cermaic |
| C2,3 | 10u 35 V tantalum |
| C4 | 220u 25V electrolytic axial |
| C5,10 | 100n polycarbonate |
| C6 | 10n polycarbonate |
| C7 | 820p polystyrene |
| C8 | 4n7 polycarbonate |
| C9 | 470n polycarbonate |
| C11 | 1u0 16 V tantalum |
| C12 | 47n polycarbonate |
| C13,14 | 100u 25 V electrolytic axial |

Semiconductors

| | |
|-------|------------------|
| IC1,3 | LF353N |
| IC2 | 741 |
| Q1 | 2N3819 |
| D1,2 | 1N4148 |
| ZD1 | 6V2 BZY88 400 mW |

Miscellaneous

| | |
|----------------------|----------------------------|
| M1 | 100 uA moving coil meter |
| SW1 | 1 pole 8 way rotary switch |
| SW2 | SPDT miniature toggle |
| SW3,4 | SPST miniature toggle |
| SK1 | phono socket |
| SK2 | 3 pin din socket and plug |
| Case | BOC 709B (see bylines) |
| knot to suit | |
| 1 off PCB | |
| 1 off M81 microphone | |



Construction should not present any problems, if you use our PCB and the case specified.

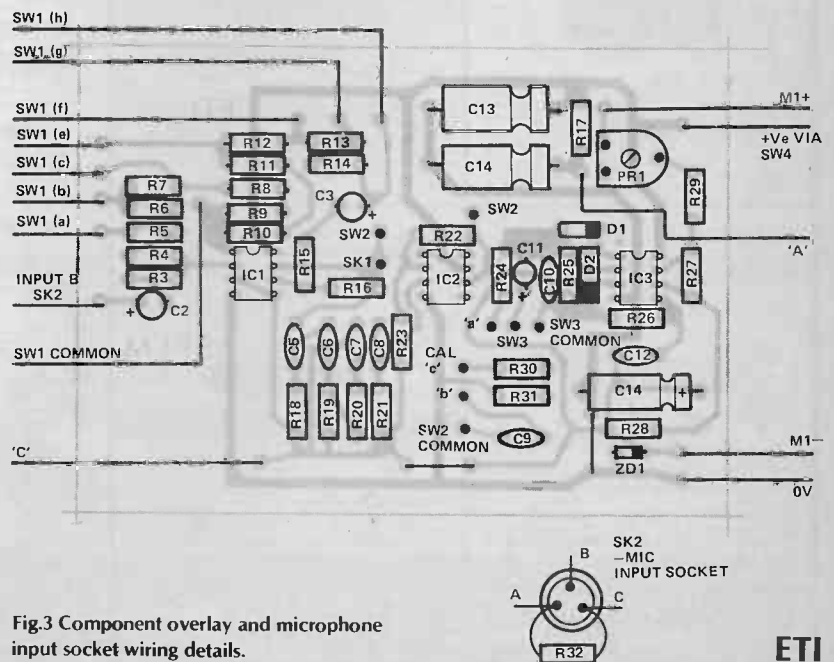
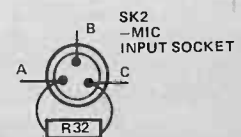


Fig.3 Component overlay and microphone input socket wiring details.



DESIGNER'S NOTEBOOK

Ray Marston looks at the LM3914 Dot/Bar Display Driver and shows a variety of ways of using the device.

The LM3914 is a dot/bar display driver, specifically designed to sense a DC input voltage and drive a line of 10 LEDs to give an analogue display of the magnitude of that voltage. It's an inexpensive and superior alternative to the conventional analogue-indicating moving-coil meter, does not suffer from 'sticking' problems, is unaffected by vibration, can be used in any attitude and has a very fast response.

The device has a built-in precision voltage reference, its output is internally current-limited and it can drive a variety of types of devices (LEDs, transistors, reed-relays, etc). LM3914s can readily be cascaded and their outputs used to drive a virtually unlimited number of LEDs or other devices. We've used the LM3914 in lots of projects in ETI and in Hobby Electronics in the past year or so. We were, in fact, the first UK magazine ever to use the device.

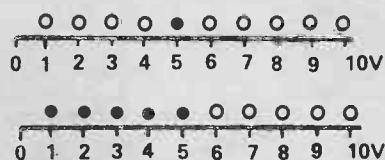


Fig. 1 Dot indication (top) and bar indication (above) of 5 V on a 10 V LED scale.

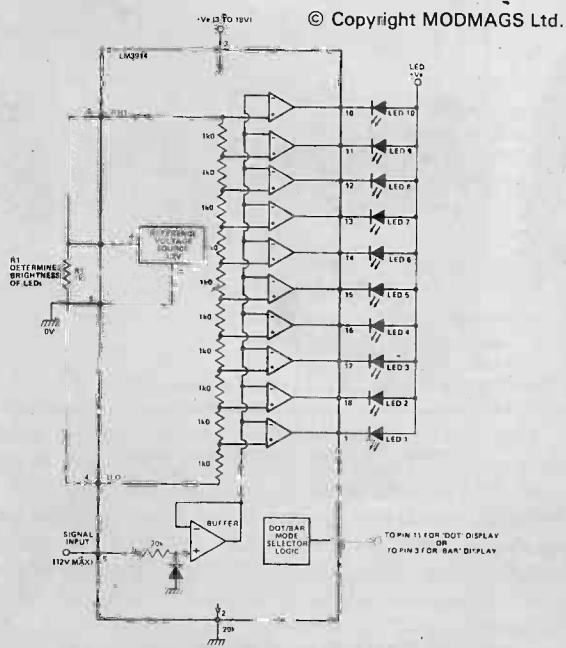


Fig. 2 Equivalent internal circuit of the LM3914 with connections for making a 0-1V2 dot or bar meter.

Basic Principles

Figure 2 shows the equivalent internal circuit of the LM3914, together with the connections for making it act as a 10-LED voltmeter with a full-scale sensitivity of 1V2. The IC contains 10 voltage comparators, each with its non-inverting terminal taken to a specific tap on a built-in precision multi-stage potential divider and with all inverting terminals wired in parallel and taken to input pin 5 via a unity-gain buffer amplifier. The output of each of the 10 voltage comparators is individually available at one of the output pins of the IC (pin 1 or pins 10 to 18) and is capable of sinking a current of up to 30 mA; the output currents are internally limited and can be preset by R1.

The IC also has a built-in 'floating' precision reference voltage source that provides a nominal 1V2 between pins 7 and 8. In Fig. 2 we've shown pins 7 and 8 externally connected to potential divider pins 6 and 4 respectively, so in this particular case 1V2 is developed across the 10-resistor divider network of the IC. The chip also contains an internal logic network that can be externally programmed to give either a dot or a bar display from the outputs of the 10 voltage comparators. In the dot mode, only one of the 10 outputs is enabled at any one time. In the bar mode, all outputs below and including the highest energised output are enabled at the same time.

Bar Sequence

Let's assume that the logic is set for bar mode operation. We've already set a reference of 1V2 across the internal 10-resistor divider, with the low (pin 4) end of the divider tied to ground (zero) volts. Thus, 0V12 is applied to the inverting or reference input of the lower comparator, 0V24 to the next, 0V36 to the next and so on. If a slowly rising voltage is now applied to input pin 5 of the IC, the following sequence of events takes place. When the input voltage is zero, the outputs of all 10 comparators are disabled and none of the LEDs is on. As the input voltage is slowly increased it eventually reaches and then exceeds the 0V12 reference value of the first comparator, which then turns on (its output conducts) and energises LED 1. As the input is increased it reaches 0V24 (the second comparator), which then also turns on and energises LED 2. At this stage LED 1 and LED 2 are on. As the input voltage is further increased, more comparators and LEDs are turned on, until eventually, when the input rises above, the last comparator and LED 10 turn on, at which point all 10 LEDs are illuminated.

A similar kind of action is obtained when the LM3914 logic is set for dot mode operation, except that only one LED turns on at any given time. At 0 V, none of the LEDs is on. At voltages above 1V2 (or whatever reference value is applied to the last comparator) only LED 10 is turned on.

Some Finer Points

Figure 2 shows R1 connected between pins 7 and 8. This resistor determines or 'programs' the ON currents of the LEDs. The resistor is actually connected across the output of the internal voltage source (1V2 nominal) and the ON current of each LED in fact approximates 10 times the output current of the voltage source.

The source can supply up to 3 mA, so the LEDs can be programmed to pass currents up to 30 mA. Thus, if a total resistance of 1k2 is placed across pins 7-8, the source will pass 1 mA and each LED will pass 10 mA in the ON mode. In Fig. 2, the total resistance across the source terminals is equal to the 1k2 of R1 shunted by the 10k of the IC's internal potential divider, so the reference actually passes about 1.1 mA and the LEDs conduct 11 mA. If R1 is removed from the circuit the LEDs still pass 1.2 mA due to the loading of the internal potential divider on pins 7 and 8.

Notice that the IC can pass total currents up to 300 mA when used in the bar mode with all 10 LEDs on. The IC has a maximum power rating of only 660 mW, so there is a danger of exceeding this rating when the IC is used in the bar mode.

General Supplies

The LM3914 IC can be powered from any DC supply of 3-25 V. The LEDs (or other external loads) can use the same supply or can be independently powered from supplies up to 25 V. The voltage across the internal potential divider can be up to 2 V below the main supply voltage, up to a maximum supply voltage of 25 V.

The IC's internal voltage reference produces a basic nominal output of 1V28 (limits are 1V2 to 1V32), but can be externally programmed to produce effective reference values up to 12 V. The input buffer of the IC has integral overload protection and can withstand inputs of up to ± 35 V without damage. The IC can be made to give a dot mode display by wiring pin 9 to pin 11, or a bar display by wiring pin 9 to positive supply pin 3.

Dot Mode Voltmeters

The basic Fig. 2 circuit can be converted into a practical 1V2 FSD meter by merely wiring a 10uF electrolytic capacitor directly between pins 2 and 3 of the IC, to suppress unwanted oscillations and ensure circuit stability. The range of the circuit can be changed in a variety of ways. The sensitivity can be increased, for example, by either interposing a DC amplifier between the input signal and pin 5 of the IC, or by reducing the reference voltage that is applied to pins 4 and 6. In this latter case the IC will operate quite well with a reference voltage down to a few hundred millivolts.

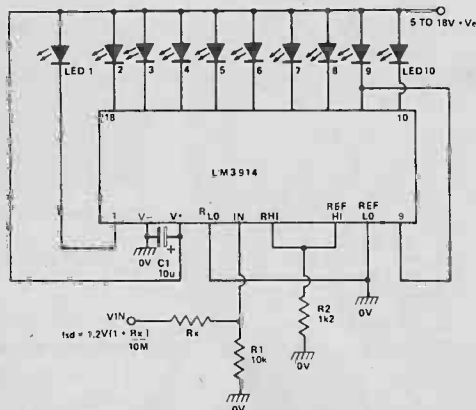


Fig. 3 1V2 to 1000 V FSD dot mode voltmeter.

The easiest and best way to reduce the sensitivity of the meter is to use the connections shown in Fig. 3. The basic circuit is that of a 1V2 meter, but the input signal is applied to the IC by a potential divider formed by Rx and R1. Thus, the circuit can be made to read 12 V full scale by giving Rx a value of 90k, so that Rx/R1 act as a 10:1 divider. The circuit can be used to read full scale voltages from 1V2 to about 1000 V.

An alternative connection is shown in Fig. 4. In this case the input voltage is applied directly to pin 5 of the IC, but the reference voltage on the internal divider is variable from 1V2 to 10 V by RV1. The internal reference develops 1V2 between pins 7 and 8, but this voltage is fully floating. By wiring RV1 between pin 8 and ground we can ensure that the output current of the reference flows to ground via RV1, thus providing a voltage that raises the pin 8 (and also pin 7) value considerably above 0 V. This increased voltage is applied to the top (pin 6) end of the internal potential divider, which has its low end (pin 4) grounded, and determines the full scale sensitivity of the circuit. This circuit has a useful voltage range of only 1V2 to 10V. The IC supply voltage must be greater than the required full scale voltage.

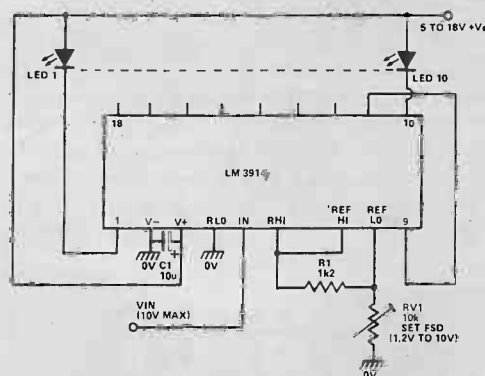


Fig. 4 An alternative 1V2 to 10 V FSD dot mode voltmeter.

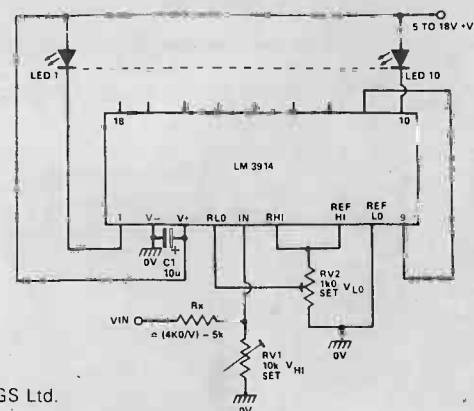


Fig. 5 An expanded scale (10-15 V, etc) dot mode voltmeter.

Figure 5 shows how the LM3914 can be used as an expanded-scale voltmeter that reads (say) 10 V at minimum scale but 15 V at full scale. Both the top and bottom ends of the internal potential divider (pin 6 and 4) of the IC are externally available, so the top and bottom limits of the scale can be individually set. In the diagram, the top of the divider is fed from the 1V2 reference, but the bottom is fed from the slider of RV2. The external input signal is fed to the IC via the Rx/RV1 potential divider. Thus, if 1V2 is set on pin 6 and 0V8 is set on pin 4 and the input divider has a ratio of 20:1, the circuit will read 24 V at full scale and 16 V at minimum scale.

Bar Mode Operation

The three basic voltmeter circuits (Figs. 3 to 5) can be used with the IC connected in either the dot or bar mode. When using the bar mode, however, remember that the power rating of the IC can easily be exceeded when all 10 LEDs are illuminated if excessive voltage is allowed to develop across the output terminals of the IC. LEDs normally drop about 2 V when they are conducting, so one way round this problem is to power the LEDs from their own low-voltage (3 to 5 V) supply (Fig. 6).

An alternative solution is to power the IC and the LEDs from the same supply but to wire a current-limiting resistor in series with each LED (Fig. 7), so that the output terminals of the IC saturate when the LEDs are on.

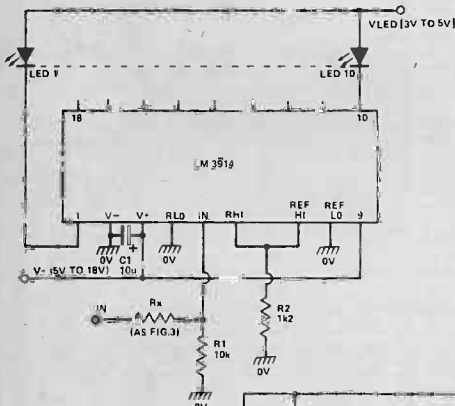


Fig. 6 Bar-display voltmeter with separate LED supply.

Fig. 7 Bar-display voltmeter with common LED supply.

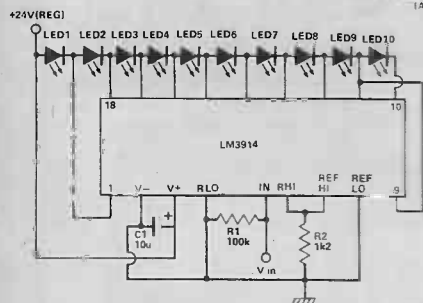


Fig. 8 Method of obtaining a bar display with dot mode operation, giving maximum energy conservation.

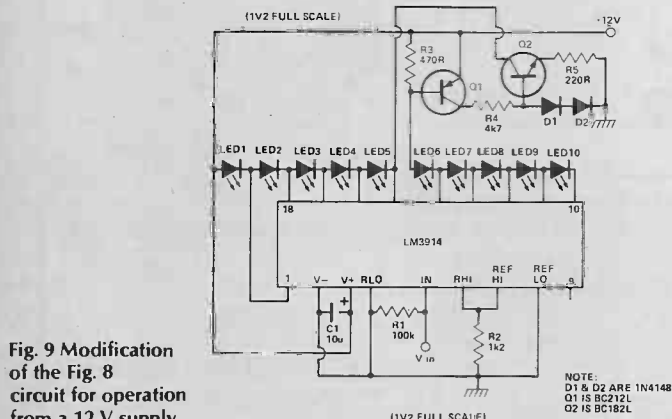


Fig. 9 Modification of the Fig. 8 circuit for operation from a 12 V supply.

Bars From Dot Mode

An alternative way of obtaining a bar display without excessive power dissipation is shown in Fig. 8. Here, the LEDs are all wired in series, but each one is connected to an individual output of the IC and the IC is operated in the dot mode. Thus, when (for example) LED 5 is driven on, it draws its current via LEDs 1 to 4, so all five LEDs are illuminated. In this case, however, the total LED current is equal to that of only a single LED, so power dissipation is quite low. The LED supply voltage in this circuit must be greater than the sum of the LED volt drops when all LEDs are on, so a regulated 24 V supply is required.

In Fig. 9 the LEDs are split into two chains. The transistors switch the lower chain on when the upper chain is active. This enables the circuit to be powered from a 12 V supply. The maximum total LED current is equal to twice the current of a single LED.

20-LED Voltmeters

Figure 10 shows how two LM3914s can be interconnected to make a 20-LED dot mode voltmeter. Here, the input terminals of the two ICs are wired in parallel, but IC1 is configured so that it reads 0-1V2 and IC2 is configured so that it reads 1V2 to 2V4. In the latter case, the low end of the IC2 internal potential divider is coupled to the 1V2 reference of IC1 and the top of the divider is taken to the top of the 1V2 reference of IC2, which is raised 1V2 above that of IC1.

The Fig. 10 circuit is wired for dot mode operation. In this case pin 9 of IC1 is wired to pin 1 of IC2 and pin 9 of IC2 is wired to pin 11 of IC2. Note that a 22k resistor is wired in parallel with LED 9 of IC1 in this mode.

Finally, Fig. 11 shows the connections for making a 20-LED bar mode voltmeter. The connections are similar to those of Fig. 10, except that pin 9 is taken to pin 3 on each IC and a 470R current limiting resistor is wired in series with each LED to reduce the power dissipations of the ICs.

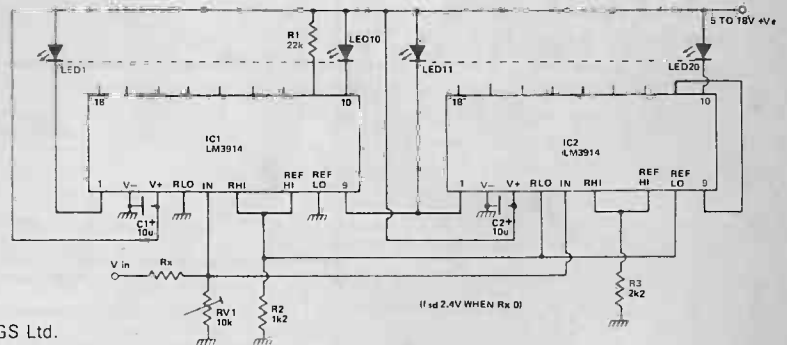


Fig. 10 Dot mode 20-LED voltmeter (FSD = 2V4 when Rx = 0).

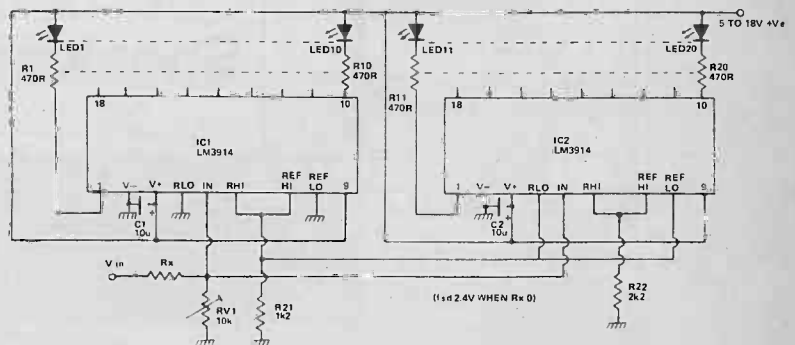


Fig. 11 Bar mode 20-LED voltmeter (FSD = 2V4 when Rx = 0).

ETI

MPU SUPPORT CHIPS

There's no shortage of technical tomes on microprocessors, but there is a distinct dirth of texts on chips that make the MPU do its stuff. Ian Sinclair comes to the rescue.

The first essential for a microprocessor is a clock pulse generator. A clock pulse is simply a rectangular pulse which repeats at a high frequency, usually 1 MHz or more. All microprocessors need clock pulses, because each operation within a microprocessor is triggered by a clock pulse, so no clock pulse — no action. Each little piece of a program will take a definite number of clock pulses to carry out.

How do we generate clock pulses? A few microprocessors, notably the much-loved INS8060 (SC/MP Mk. II) used in the Science of Cambridge Mk. 14 kit, can generate their own clock pulses. The INS8060 has two terminals which can be connected to external components as shown in Fig. 1. Either RC or crystal oscillator circuits can be used, providing the frequency is fairly high — the internal circuits simply won't oscillate if the time constants are too large. Keep to the values suggested by the manufacturer and you should have no problems.

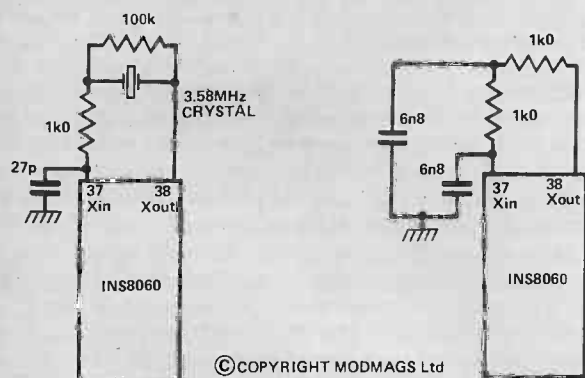


Fig. 1 Using a built-in oscillator — the INS8060 (SCMP II) can use its built-in oscillator along with a crystal or a simple R-C network.

Phase Relations

Most microprocessors, however, can't spare the extra pin for connections to a built-in oscillator and instead use only a single pin or a pair of pins for clock pulses. When a single pin input is used, the clock is a single phase clock (a straightforward oscillator). This can be obtained from a multivibrator or by squaring the output of a sinewave oscillator, but it's very important that the waveform should be steep-sided (Fig. 2). If you use a waveform which has long rise or fall times, so that its sides appear to slope when you view the waveform on the oscilloscope, then you'll have trouble when you try to use the microprocessor. The reason is that some gate circuits will oscillate if they are switched over too slowly and that can cause chaos. Don't be tempted to economise on circuits, therefore.

One particularly useful way of ensuring that all signals

entering the microprocessor have short rise and fall times is to use a type of TTL IC called a Schmitt trigger. Typical of these are the 74LS13 quad two input Schmitt NAND. Each of these chips has a Schmitt trigger built in, so the output will always be steep-sided even if the input is not. It's often easier to use a cheap 'n' simple oscillator and a Schmitt IC than to build an elaborate transistor oscillator.

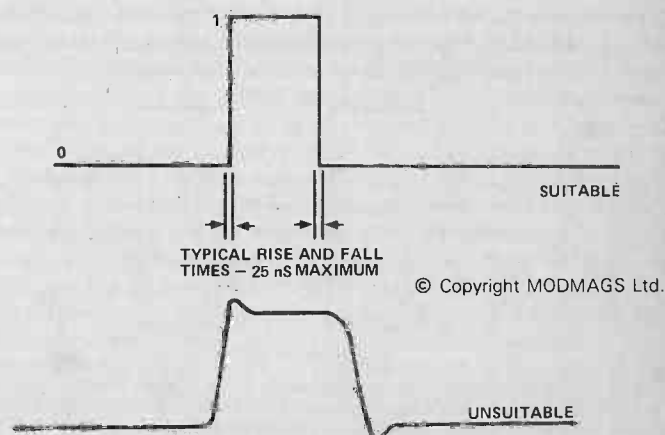


Fig. 2 Clock-pulse shapes. Most discrete-transistor oscillators and certainly all linear IC oscillators (such as 555) cannot generate sufficiently steep-sided clock pulses when driving a capacitive load. A TTL pulse generator is ideal, or a generator which is buffered by a Schmitt inverter, such as the 74LS14.

Refreshment Is Served

Several types of microprocessors, notably the 6800 and 6502, use two pins for the clock input. This is because the clock pulses have to be two-phase. One pin is being pulsed positive at a time when the other pin is at logic 0. Just to give one example, the 6800 carries out only internal actions on the second phase of its clock, so that during that phase all outputs are isolated. This means that you can run a low-cost memory system using dynamic RAM. Dynamic RAM needs refresh pulses and these can be delivered during the second phase of the clock pulse, when the memories are not connected to the microprocessor in any case.

Buffers

Buffers are the next group of ICs which have to be used in practically all microprocessor circuits. A buffer is basically an amplifier circuit with a three state output — explanation coming up. There are two reasons for using buffers. One is that microprocessor circuits use PMOS, NMOS or CMOS circuits,



ASTROLOGUE

Think of spaceflight and NASA springs to mind, but how much do you know about the European Space Agency? Ian Graham looks at ESA and reports on the latest news from Saturn PLUS lots of other space news items.

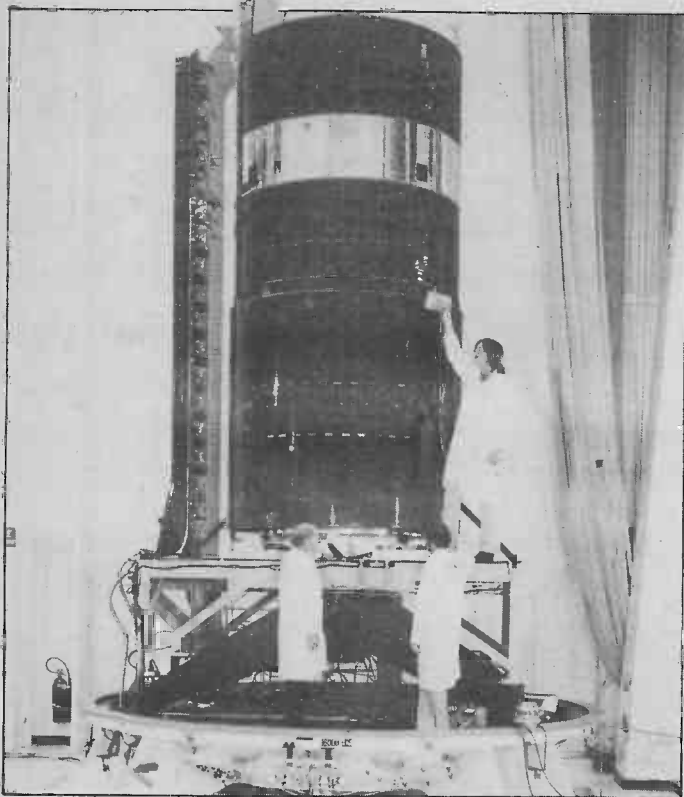
Austria, Canada and Norway also participate in some programmes. Representatives of the member states form the ESA Council, the agency's policy-making body.

COS And Effect

In August 1975 ESA launched COS B — a remotely controlled astronomical observatory, which in two years made the most sensitive survey of previously unexplained gamma radiation sources in the plane of the Milky Way. The GEOS programme was developed to study near-Earth space, the region where the Earth's magnetic field is active (the magnetosphere). GEOS-2, launched in April 1977, was not placed in the correct geostationary orbit because of a fault in the US Delta 2914 launcher. Instead, it was placed in a 12-hour eccentric orbit (38,000 km x 2,050 km), but even so, it played a valuable part in collecting data for the International Magnetosphere Study (IMS). In July 1978, only one month after GEOS-1's mission ended, GEOS-2 was successfully launched with an identical payload to continue the programme.

While we're constantly bombarded with film, photos, interviews and articles from or about NASA and its major space programmes, we hear very little about the space programmes which are on our doorstep and to which our taxes contribute. What do you know about ESA and its activities?

In May 1975 the European Space Agency succeeded two earlier organisations — the European Space Research Organisation (ESRO) and the European Launcher Development Organisation. ESA now has 11 member states — Belgium, Denmark, France, West Germany, Ireland, Italy, The Netherlands, Spain, Sweden, Switzerland and the UK.



The new SBS communications satellite was launched from Cape Canaveral on November 15. It is the first of three built by Hughes Aircraft for Satellite Business Systems, jointly owned by IBM, Comsat General and Aetna Life and Casualty to provide secure voice, video, data and facsimile service to American businessmen. At launch the satellite is nine feet high, but in orbit it extends to 22 feet to double the area of exposed solar cells.

The International Sun-Earth Explorer (ISEE) programme studied the solar wind and complemented the IMS project. In January 1978 the International Ultraviolet Explorer (IUE) was placed in geosynchronous orbit as part of a UV study involving NASA, the UK Science Research Council and ESA. UV spectra were obtained from the planets, interplanetary medium, stars, nebulae, supernovae remnants, galaxies and quasars. IUE is still active and is currently being used to study a supernova discovered in October by researchers at the University of Berne.

Spacelab

The agency's best known programme is probably that of the Ariane launch vehicle. I have already covered developments in the Ariane programme in recent Astrologues. Less well known, but equally interesting to the hardware freaks, is Spacelab — Europe's manned space laboratory. A team of three scientists, technicians or engineers will work in the lab for a week (a month in later missions). Spacelab will be launched and returned to Earth by the Space Shuttle. Unlike Skylab, Spacelab will be a re-usable vehicle. It is made from two components — a pressurised module and an instrument pallet. Between flights, the pallet can be replaced or removed completely to suit future mission applications.

Each Shuttle/Spacelab flight will be the responsibility of two ground control stations — the Kennedy Space Centre for the Shuttle and Spacelab Payload Integration and Co-ordination in Europe (SPICE) for the European experiments. SPICE lives in Porz-Wahn in West Germany. The first flight has been scheduled for 1983, but it is naturally dependent on the fortunes of the Shuttle programme. An engineering model of the vehicle has just been delivered to NASA.

In addition to its extensive scientific programme, ESA also maintains an active applications programme. Orbital Test Satellite (OTS) was launched in May 1978 to prove the performance of payload and spacecraft systems in the orbital environment. As OTS was an experimental satellite, built with the intention of development into future generations of experimental and communications satellites, it was built in modular form — service module plus payload module. OTS has performed so well that some equipment designs and concepts are being transferred directly to the European Communications Satellite (ECS). ESA also contributes to the World Weather Watch and the Global Atmospheric Research Programme with Meteosat, launched in November 1977.

Future Flights

ESA's plans extend well into the next decade. Spacelab and operational Ariane flights are still to come, of course. Exosat will investigate X-ray sources, possibly providing conclusive data on the existence of black holes. The Space Telescope, to be launched by the Shuttle in 1983, will be able to resolve objects in the sky 100 times fainter than is possible from the Earth's surface under our 'pea soup' atmosphere. It will also be able to make observations at ultraviolet wavelengths which just don't reach the Earth's surface.

The International Solar Polar Mission (in co-operation with NASA) will involve sending two spacecraft towards Jupiter in 1983 and use the Jovian gravitational field to divert the spacecraft out of the Earth's plane of orbit around the Sun into a solar polar orbit. The two craft will investigate space around the sun in the unexplored third dimension of the solar system. This will be ESA's first deep space mission.

In 1986 Halley's comet will once again visit our part of the universe. In March of that year an ESA satellite called Giotto is due to rendezvous with the comet. British Aerospace has just won the contract to produce the spacecraft, which will be based on the GEOS design, also built by a British Aerospace consortium. The payload will consist of about 50 kg of experiments to study the comet's nucleus and tail. Ariane is due to launch the satellite in July 1985.

I have barely scratched the surface of ESA's activities but I think you can see how wide-ranging and ambitious the projects are — atmospheric sounding rockets, manned orbital laboratories, launch rockets, communications, weather and scientific satellites, deep space vehicles and the Space Telescope.

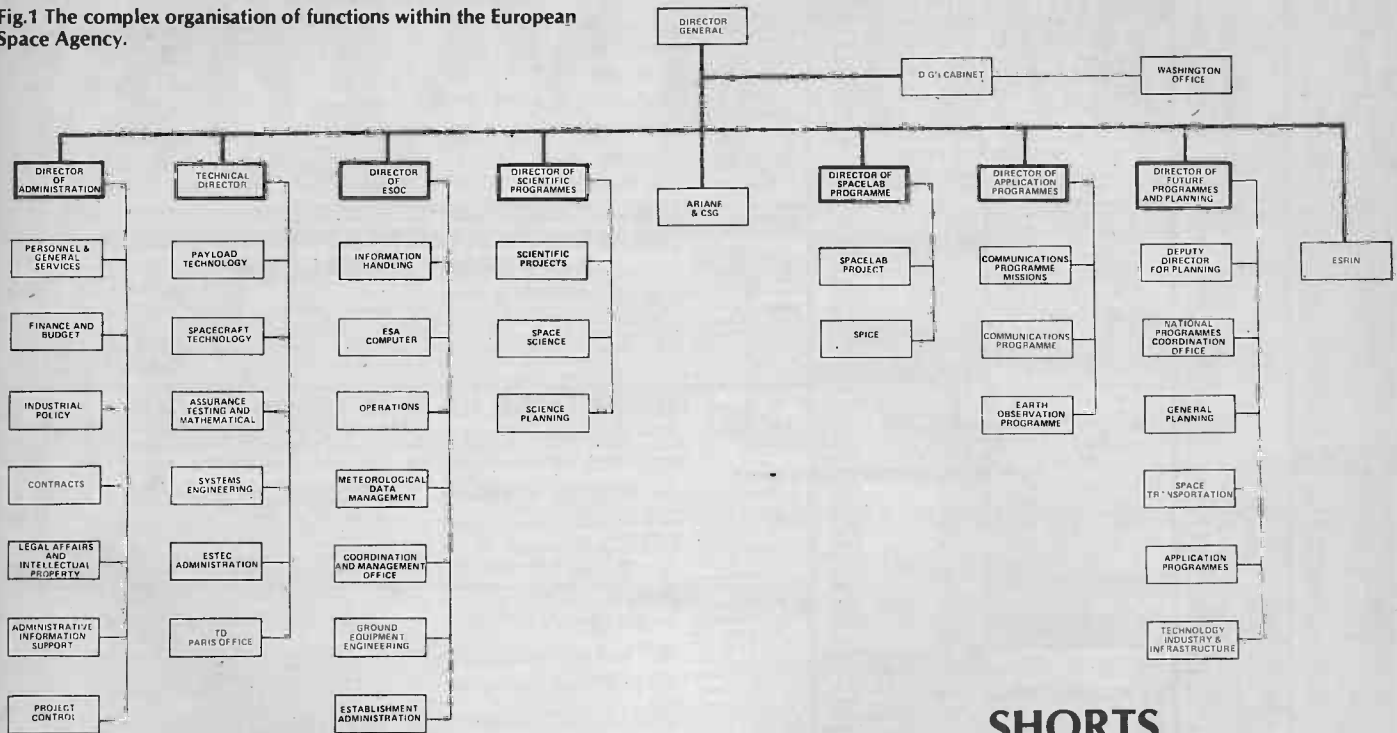
Ringling The Changes

I can't leave Astrologue this month without a mention of the information coming back from Voyager-1. The spacecraft made its closest approach to the planet on November 12th, passing within 125,000 km of the multi-coloured cloud tops. If I said that the scientists were *surprised* at the photographs

Nasa has adopted a modified Nikon F3 for use in the Space Shuttle. The model used will be fitted with motor-drive, 250-frame data magazine back, electronic flash unit and four modified Nikkor lenses — 35 mm, 55 mm, micro and 105 mm micro. Fifteen will be supplied to NASA. This isn't the first time that a Nikon has made it into orbit. It was also used during the Skylab and Apollo projects. Before the F3 became available, NASA used the F.



Fig.1 The complex organisation of functions within the European Space Agency.



SHORTS

The People's Revolutionary Republic of Guinea has joined the Intelsat group, bringing the total membership to 105 countries. Guinea has already announced plans to operate an Earth station with an Intelsat satellite over the Atlantic.

Also reported in Intellink, Intelsat's quarterly newsletter, are plans for the new generation of Intelsat satellites to be launched in 1986. Intelsat VI will achieve 2½ times the capacity of Intelsat V series by frequency re-use and SS-TDMA (Satellite-Switched, Time Division Multiple Access). It will also be compatible with ESA's Ariane 4 launcher and NASA's Space Shuttle. SS-TDMA allows signals to be switched from one satellite antenna beam to another to accommodate different types and densities of traffic. Intelsat VI is expected to have sufficient capacity for 30,000 telephone calls and two television channels.

Australia is to have its own communications satellite, able to broadcast TV and radio programmes direct to homesteads in isolated areas. The satellite, whose launch is expected by the end of 1984, and its Earth stations will be owned and managed by the Overseas Telecommunications Commission (OTC).

Paleomagnetic evidence suggests that the Earth's magnetic field has flipped over (north and south poles exchange places) every 50,000 to one million years. Magsat, a small satellite that burned up in the atmosphere in June 1980, collected data which showed that the strength of the Earth's magnetic field is declining. The last reversal was about 700,000 years ago. If the decline observed by Magsat (1% per decade) continues, the next reversal is due in 1200 years. The theorists are still arguing about the effects we can expect.

The Shuttle saga — NASA has attached the External Tank to its Solid Rocket Boosters for stress testing in preparation for the first flight in March. An engine cluster burn was shut down prematurely when overheating was observed. However, the fault was discovered to be in the exhaust nozzle, not in the engine itself. This slight set-back is not expected to delay the first flight.

coming back, it would be an understatement of astronomical proportions. Despite the Pioneer fly-by last year, no-one was prepared for Voyager's revelations. The apparently homogeneous broad rings are, in fact, composed of hundreds of separate rings. The Cassini division (previously thought to be a gap between A and B rings) has now been found to contain tiny particles ie it's a ring itself, but much less dense than the others.

The F ring, discovered by Pioneer 11, was thought to be a typical ring, albeit fainter and further out than the others. However, Voyager-1's photos show that the F ring is itself composed of three rings, which twine around one another like the threads of a rope. The ring as a whole also shows lumpiness at some points. Shadows also extend radially out into the rings at some points, so far inexplicably.

Mooning Around

Titan received special attention. As moons go, Titan is big — bigger than Mercury. Ground observations showed that it had an atmosphere of methane, but Voyager's ultraviolet spectrometer has detected a molecular nitrogen atmosphere. This raises the possibility of life on Titan, but it must be remembered that Titan is so far out from the Sun that its surface temperature is around -200° C, low enough to liquefy the atmosphere. Terrestrial organisms exposed to that sort of temperature tend to lie down, point their toes skyward and become ex-organisms.

Voyager has so far discovered three new moons around Saturn. Two straddle the outermost F ring and the third is the closest to Saturn yet discovered (800 km outside the A ring). Most of the moons are heavily cratered. Titan's surface is hidden under its atmosphere.

One moon, Janus, was discovered in 1966 and is listed in the text books as orbiting 159,000 km from Saturn and having a diameter of 350 km. Voyager has discovered that Janus is, in fact, two moons orbiting very close to one another.

The dynamicists have a great deal of head-scratching in store as Voyager-1's data is processed over the next few months. Voyager-2 will reach Saturn in August 1981 and will go on to encounter Uranus in 1986.

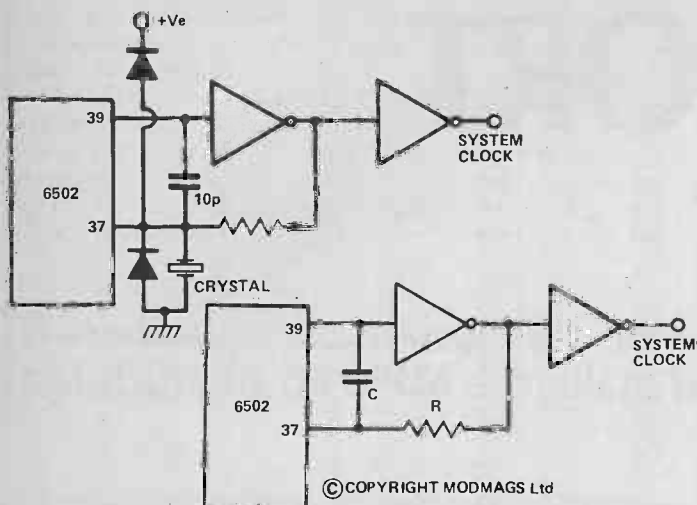


Fig. 3 The clock-pulse generator of the 6502. Either a crystal or R-C circuit can be used, but the external inverters are necessary, though they need not be Schmitt types.

which can't sink or source much current, usually a couple of milliamps at the most. A lot of the circuits which will be connected to the microprocessor will need quite a bit more current, so a buffer is needed — a current amplifier which can be comfortably driven by the microprocessor and which will sink or source enough current at its output to drive a lot more circuitry.

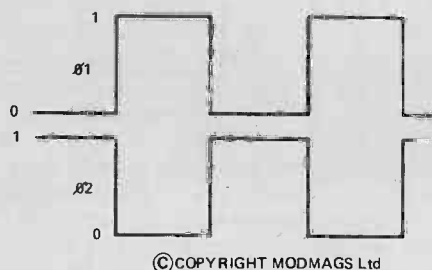


Fig. 4 Two-phase clocks. Where a two-phase clock is used, different actions are carried out in the two different phases. The sketch cannot show the correct scale; there is no overlap between the two positive phases.

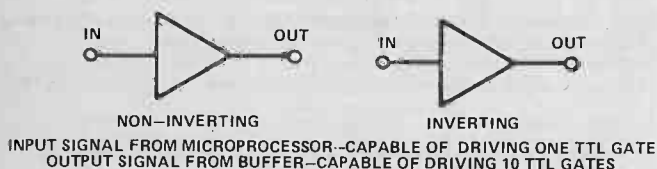


Fig. 5 Buffers, inverting and non-inverting. The MOS circuits of most microprocessors cannot provide enough current drive to activate more than one standard TTL gate and a buffer must be fitted between the MOS microprocessor and the TTL circuits if expansion is contemplated.

Buffers can also be used as switches. To take one example, the eight data lines of a microprocessor are used for feeding bits in and out. Since they can't do both at the same time, we need some method of switching so that input circuits are not connected at a time when the microprocessor is putting bits out on the data lines. This is another job for the buffer — in this case a three-state type of buffer.

The term three-state sometimes causes a bit of confusion. It means simply that the output of the buffer amplifier can be 0, 1 or isolated from all other circuits. In the type of output circuit shown in Fig. 7, for example, the output can be floated by connecting both the bases of the output pair to earth. This needs extra circuitry inside the IC and an extra 'state' pin on the package, but the advantages of having the floating state are enormous.

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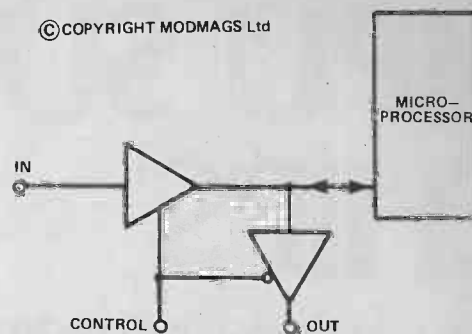


Fig. 6 Using three-state buffers. In this example, when the control signal is at logic 1, the input buffer is enabled and the output disabled. With the control signal at logic 0, the output buffer is enabled and the input disabled. The output of the disabled buffer acts like an open-circuit.

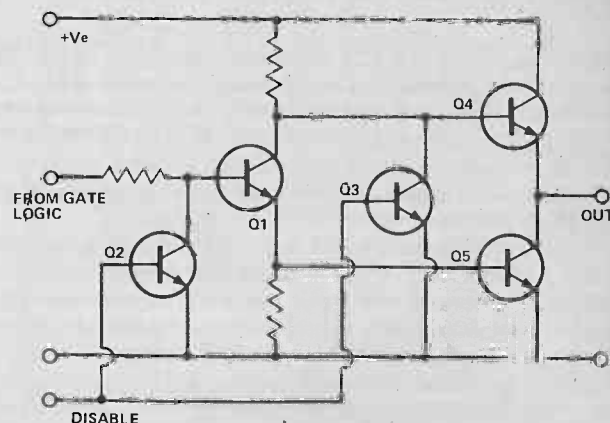


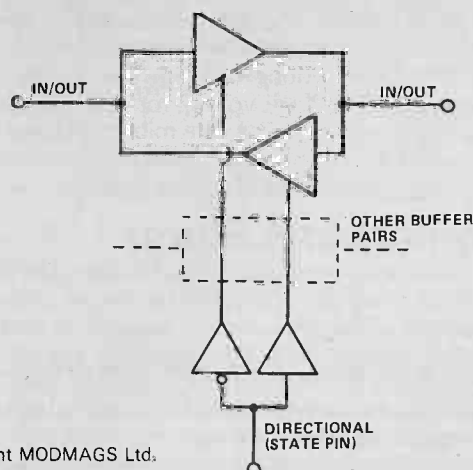
Fig. 7 A simplified form of three-state control. The normal gate output circuit consists of Q1, 4 and 5. When the disable pin is high, Q2 and Q3 conduct, shorting the bases of Q1 and Q4, so that both transistors are cut off. This isolates the output completely.

Buffers may be used unidirectionally or bidirectionally. A unidirectional buffer deals with the flow of signals in one direction only, perhaps from an input circuit to the data lines. Most of these are made in two versions, the difference being in the polarity of the three-state control pin. For example, one buffer may go open circuit at the output for a 1 at the three-state control pin and another type may go open circuit for a 0 at the control pin. When the buffer is being used unidirectionally, it's purely a matter of convenience which type is used. For example, if the buffer is used to connect input signals to the data lines and the microprocessor puts out a negative pulse at the time when it is ready to take in such information, then a buffer which is open circuit on a 1 signal and operates for a 0 signal at the state pin is ideal. If the other type of buffer is used, an inverter will need to be incorporated in the control line.

Much more common is bidirectional buffering, where a buffer amplifier is needed for both inputs and outputs. One single buffer can't do this, so a very common method is to use two lots. One lot is isolated by a 1 on its state pin, the other by a 0 on its state pin, so that the outputs of one set of buffers can be connected safely to the inputs of the other set as shown in Fig. 8 with the state pins connected together. In this way, the combined buffers conduct one way when the state pin is at 1 and the other way when the state pin is at 0.

Ah Yes, I Remember It Well

Most books on microprocessors assume that the readers know all about memory ICs. Assuming that you don't, point number one is that we make use of two types of memory systems, ROM and RAM. You can get bits out of ROM (Read



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Fig. 8 The bidirectional buffer. The buffer stages are connected input-to-output with the enable lines driven so that the two buffers of a pair cannot be enabled at the same time. This arrangement is sometimes described as a 'transceiver' — an example is the quad transceiver 74LS243. An octal buffer such as the 74LS241 can also be used in this way by connecting the enable inputs together.

Only Memory) but you can't, in normal operation, put any bits in. ROM is used for 'non-volatile memory', so that the data bits are still stored even when the whole system is switched off.

RAM (Random Access Memory) is misnamed, because practically all the memory ICs we use have random access, meaning that we can get at any one set of bits in the memory without having to sort through all the others.

There are several different types of technology which are used to make these memory chips, but the two important varieties are the two types of RAM (static and dynamic). Static RAMs are based on flip-flops (bipolar or MOS which will flip over one way or the other when set or reset by an input. Dynamic RAMs are based on storage of charge in capacitors and this charge is called 'refreshing'. A dynamic memory is refreshed by applying a refresh pulse to each memory cell which stores a 1.

Organisation

Apart from the question of whether to use static or dynamic RAM, the main factor we need to take into account when dealing with memory is the way in which the memory is

organised. Organisation in this sense means the way in which the memory cells are grouped. For example, one very popular way of organising memory is to have 1024 cells, each using a single common data input/output pin. This is classed as a 1K x 1 memory, the 1K (K in memory size means 2^{10} (1024), not 1000) referring to the total number of groups of memory cells and the 1 meaning the number of data lines. A memory like this would (normally) need ten address lines (because $1024 = 2^{10}$) so that 1024 different address numbers can be coded in binary on the lines.

A 512 x 4 memory, on the other hand, would have 512 groups of four cells each, with four data pins for input and output signals. With only 512 groups, only nine address lines are needed ($2^9 = 512$), but at each address number, four bits are being written or read. The total number of bits stored in such a memory is 2048 (512 x 4).

Chip-Ability

An essential feature of all memory types is a chip-enable pin. At one logic voltage on the chip-enable, the memory can be used for reading or writing in the usual way, but with the chip-enable shut off, the memory data pins go 'floating' as if a three-state buffer were in circuit. This saves using an additional buffer chip and enables us to use large numbers of memories connected together without any other form of buffering.

How, then, do we connect memory chips to the main microprocessor (or CPU) unit? There's no simple answer, because it depends on how the memory chips are organised. Take, for example, the use of 4K x 1 chips. Each chip will provide one bit of data, so that we need eight chips to give a complete byte of memory data, 4K in this example. The data connections are simple, each data line from the CPU goes to a different memory chip. The memory lines are equally easy. 4K is 2^{12} , so that twelve address lines of the microprocessor are connected to all twelve address pins on each memory unit (Fig. 9). This would be the normal layout for a medium sized system using the INS8060, for example, which has only twelve address lines; other microprocessors which use 16 address lines would have four address lines left spare. The lines which are left spare are, of course, the higher order address lines numbered A12 to A15 (they start at A0, so the twelfth line is A11), because the lower order ones are the first to be connected.

The shape of the circuit board would have to be rather

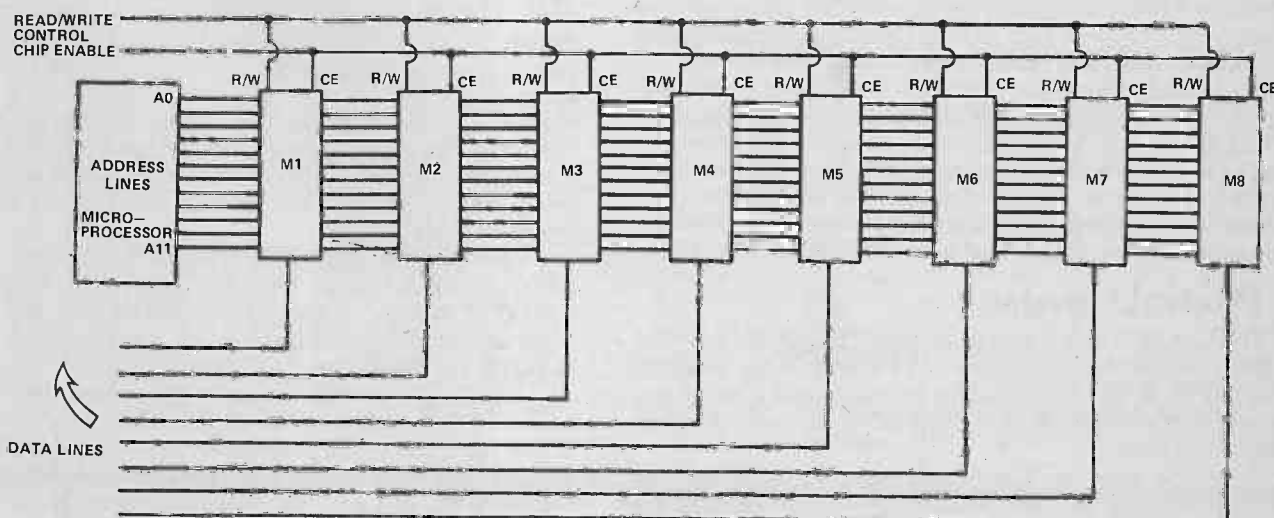


Fig. 9 Using single-bit memory chips. Eight chips are needed to form a memory bank and the read/write and chip-enable signals for each chip must be taken from the microprocessor — they will probably need to be buffered.

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different if we were using, say 2K x 4 memories. Each memory chip would have four data pins, so that a complete data byte would need only two chips, and with only 2K to address, only 11 address lines would be needed. On the other hand, had we used 1K x 8, a single memory chip would be connected to all eight data lines and 10 of the address lines.

That's simple enough, but suppose we wanted more memory than could be supplied by a single band of memory ICs? We might, for example, find that 2K of memory obtained from two of the 2K x 4 chips was insufficient and that we needed another 2K. How do we cope with the extra? The answer is that we use one lot (two of 2K x 4) for the first 2K of memory addresses and the other lot for the second 2K of memory — but how? When we have two identical lots of memory chips they will all use the same address lines and the same data lines. In our example using 2K x 4 chips, we want to use the first two chips for the first 2K of memory and the second two for the next 2K. Each chip, being a 2K chip has 11 address lines and four data lines, and all the address lines will be paralleled. In other words, the A0 pin of each chip is joined and connected to the A0 pin on the CPU, the A1 pins of the RAM are similarly connected to the A1 pin of the CPU and so on. The data pins 0 to 3 of chips 1 and 3 are connected to data pins D0 to D3 of the CPU and the data pins 0 to 3 of chips 2 and 4 are connected to data pins D4 to D7 of the CPU.

Bits Of Memory

If these were the only connections, we wouldn't have a workable system, because a given address, say 10010110110, would fetch data from (assuming that we're reading memory) both lots of chips and something would end up frying tonight. 'Address decoding' solves the problem. The simplest method is linear address decoding. The highest address for chips 1 and 2 is 1111111111. The next number above this is 100000000000. The lower address lines are now all at 0, so that both lots of memories 1 and 2 along with 3 and 4 are fetching from address 0.

This is where the chip-enable pin comes into the picture. Suppose line A11 is connected to the chip-enable pin of memory chips 1 and 2, and an inverter, whose output is connected to the chip-enable pins of memory chips 3 and 4.

Consider what happens if the chip-enable is active, allowing the chip to operate, when it is at zero. Addresses 0000 up to 07FF (that's all zeros up to all 1s) will be fetched from chips 1 and 2 only, because line A11 is low, activating the chip-enable of those two chips. Because of the inverter, the chip-enable of memory chips 3 and 4 is high, putting their data outputs into the floating state. The data bytes for the first 2K of addresses are, therefore, read from memory chips 1 and 2 only. When the address number reaches 100000000000 (0800 in hexadecimal), the A11 line goes to 1, so that the chip-enable pin of memory chips 1 and 2 goes high, putting the data outputs of those chips into the floating state. The inverter action ensures that the chip-enable pin of memory chips 3 and 4 will be low, so that the next 2K of address numbers are read from these chips only.

Partial Control

This system is only a partial solution, though, because the decoding does nothing about lines A12 to A15. As the program count proceeds, these lines will be activated and if nothing is attached to them, the memory chips will be controlled purely by the lower lines.

Since the upper four lines can have $2^4 = 16$ possible addresses on them for any given address on the lines which we're using, the sequence of use of memory can be repeated 16 times.

All this address decoding business, incidentally, applies

equally to ROM or RAM. The only extra complication which is present in RAM chips is the read/write pin which has to be taken to one logic voltage for writing data from the microprocessor to memory and to the other logic voltage for reading data from the memory to the microprocessor. The microprocessor CPU will control such pins directly from its read/write control pin, or pins, which will be indicated on the pinout diagram.

Any Port In A Storm

Most microprocessor systems need nothing like the 64K of memory which could be addressed by sixteen address lines. Even a computer with fairly extensive capabilities may use only 16K of RAM, though its ROM and other use of memory addresses can bring the total up to 32 K. All in all, then, there are several address lines floating about if we want to load data into the CPU directly or feed data out. An address-decoded or memory-mapped input/output system makes use of buffers and latches which are controlled by a signal gated out from the address lines.

For example, suppose the ROM and RAM that we use in a system take up a total of 8K. 8K of memory needs addresses up to 2^{13} , so that it uses 13 of the 16 memory lines and there are three left. Now three lines can be used in $2^3 = 8$ different sets of addresses, of which we have used one set in the 8K of memory addresses. That leaves seven sets of 8K (56K) of addresses which are spare if the top lines are fully decoded!

We can, for example, choose to use an address such as 36D6, which involves decoding all the address lines, or more simply, use any address which has line A13 high. Normally this would activate the memory, but we can easily arrange things so that when A13 is high, a gate circuit will disable all the memory chips, making use of the chip-enable inputs. That way, any memory address which has line A13 high can be used to activate a buffer and so connect the data lines to a connecting strip. The buffer would also be controlled by the read/write signals to ensure that signals were going in the right direction. A more common type of interface is an eight-bit latch, which holds data temporarily stored until either the CPU or any external circuits can deal with the bits.

Map Reading

Memory-mapping is a very common method of making use of the address lines to control inputs and outputs; porting is another. A port is usually a separate IC which is connected to the data lines and also to the control lines of the CPU, though most CPUs use some of the address lines. A typical port or PIO (Peripheral Input/Output) will have one or two sets of input or output pins — the usual eight connections to the data bus, and several (typically six) pins for control signals. It's a one-chip method of obtaining input or output at a time when the memory chips are not being used and because it's a single IC, manufacturers usually load on a lot of extra functions, such as being able to use some bits for inputs and others for outputs simultaneously.

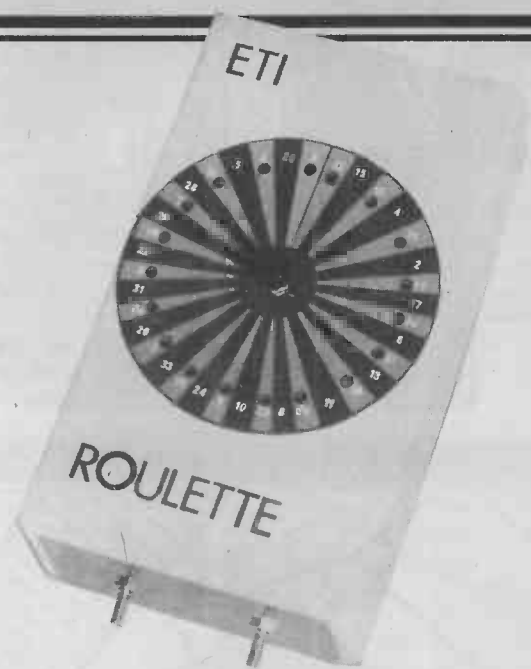
Port ICs are generally designed specifically for one particular CPU, though they are capable of a remarkable number of actions. No two are completely alike and there are always some restrictions on their use as compared to memory mapping. For this reason, memory mapping is used much more.

There's no end to the number of specialised chips which are produced for use with CPUs like the Z80. Even the humble SC/MP has a combined port/memory chip, the INS8154, which almost needs an instruction manual of its own. The units dealt with here are, however, the ones you're most likely to find in smaller systems and, more important, the chips you will use if you start designing your own microprocessor systems. Good Luck!

ETI

ROULETTE GAME

This home-casino project is battery powered and has switch-selection of biased (in favour of the house) or unbiased (no house) options. Naturally, the project includes a realistic sound-effects generator. Design by Ray Marston. Development by Steve Ramsahadeo.



This attractive little project can be guaranteed to provide hours of fun at home. It is an electronic version of the well known roulette game, with the 'wheel' replaced by a spinning circle of light on a ring of 37 LEDs and with the familiar wheel-clicking sounds simulated by an electronic generator.

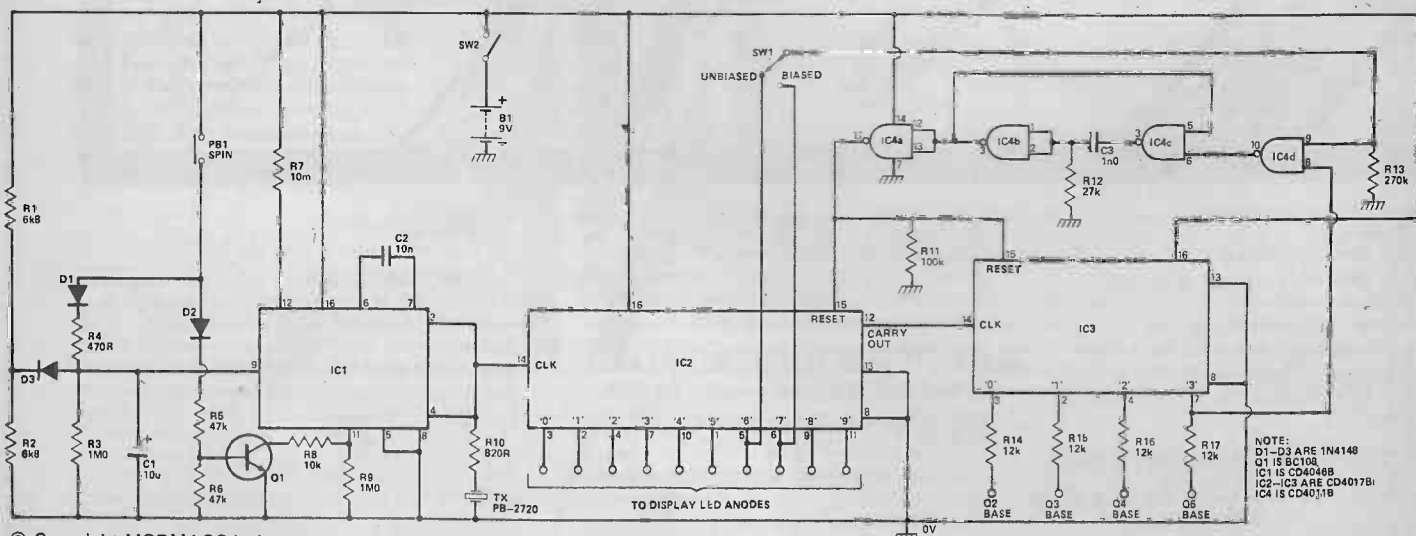
The basic concept of roulette is quite simple. On each spin, the wheel can randomly generate any one of 36 or 37 numbers (1-36 or 0-36). To start a game, each player forecasts (and bets money on) the number at which the wheel will stop by forecasting the number, or the colour of the number (red or black), or any of a variety of characteristics of that number. The wheel is then spun and eventually comes to rest against some randomly determined number, at which point the players with that number are declared winners and are each paid a sum determined by the rules of the game and the magnitudes of their initial bets.

A real-life wheel may generate either 36 or 37 numbers. On a 37-number wheel, the numbers run from 0 to 36, with 0 representing the house. The presence of the 0 biases the game in

favour of the house. On a 36-number wheel there is no zero; the numbers run from 1 to 36 and the game is said to be unbiased. The ETI roulette game has an option for 37 or 36 number operation via a selector switch. The wheel is 'spun' via a push-button switch and takes roughly 15 S to come to rest after each initial spin.

Construction

The ETI roulette game is built on two PCBs — one holding most of the electronic circuitry and the other holding the 37-LED display. Construction of the main board shouldn't present any problems. Construction of the display PCB, however, is rather fiddly, since it calls for a great deal of hard-wiring between the LEDs (using Veropins) and to the main PCB. When constructing this board, confirm the functioning and polarity of all LEDs before soldering them into position on the PCB. Note that all cathodes go to the outer segments of the PCB ring. All LEDs should be given equal heights (as long as possible).



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Fig. 1 Main circuit diagram. Biased and unbiased game options can be switch-selected.