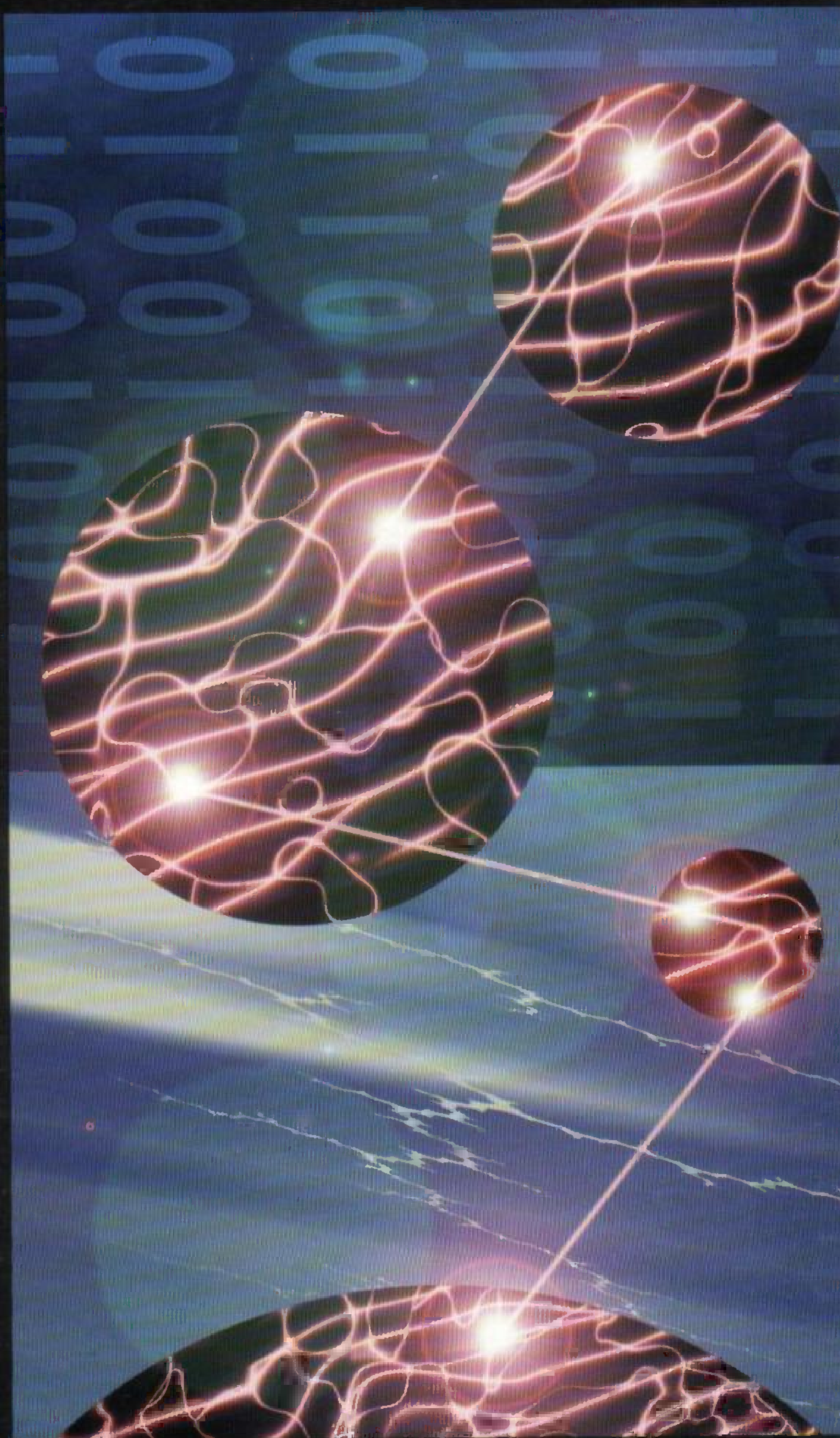
ETI ELECTRONICS TODAY INTERNATIONAL

DATA ON THE AIRWAVES

Digital Audio Broadcasting: The dial has come full circle



PC-CONTROLLED DOT MATRIX DISPLAY

4 lines x 24 characters pro-quality module and control board

IONISING RADIATION AND IONISATION CHAMBERS

History and an experimental Do-It-Yourself circuit

TRACKING FILTER GUITAR EFFECT

Phase locked loop controlled filter tracks changes in the guitar's pitch

PLUS

- MAGSTRIPE CARD READER
- DIY PC - FLASH BIOS UPGRADES
- PC-CONTROLLED SINE WAVE GENERATOR

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Electronics and Computing • Projects for the Future

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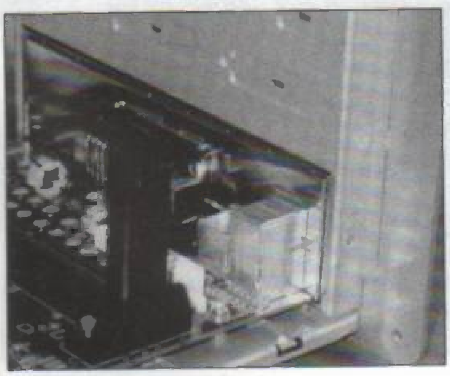
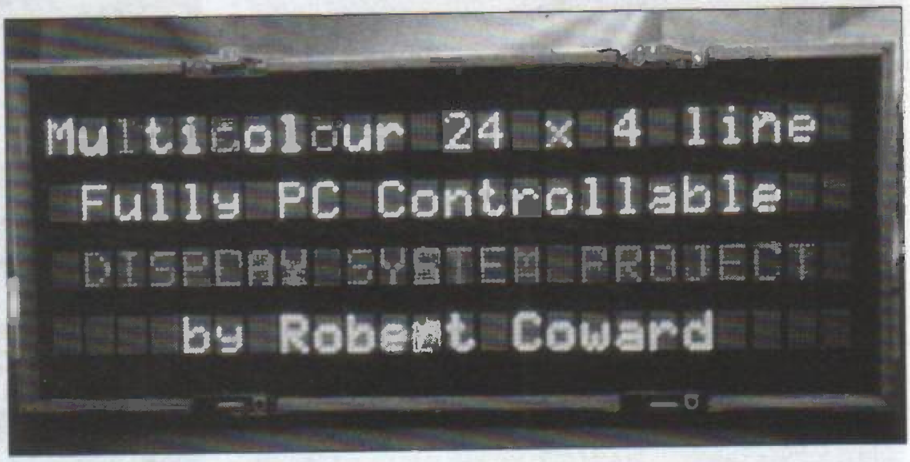




Regulars

ETI ELECTRONICS TODAY INTERNATIONAL News...

Basketball Board wins the development prize in 1998's YEDA

The winners of the 1998 Young Electronic Designer Awards received their presentations from His Royal Highness the Duke of York on 29th June at a celebration dinner in Manchester, attended by 200 guests.

The Awards, now in their 13th year, are intended to recognise (and encourage) young designers working with modern technology. Contestants must think through and design a solution to an everyday problem they have identified, and build a working prototype.

Prizewinning projects this year include a small, low-cost fridge alarm that warns if the door is left open, a black box flight recorded for model aircraft and an electronic location device that can be fitted to maritime lifejackets.

The winners are:

The Duke of York's Award for the most imaginative concept: Richard Paget of Bolton School: a model aircraft flight data recorder ("black box").

The Cable and Wireless Prize for the most commercially viable project:
Joint: Edith Butterfield of St. Margaret's Senior School, Midhurst: a fridge alarm; Andrew MacLachlan of King Edwards School, Birmingham: a portable basketball scoreboard.

The IEE Award for the best new entrant to YEDA:
Tom Maxwell-Wood, Zoe Spenser, Ashley Buck and Alex Dodkin of The Blue School, Wells, Somerset: A maritime rescue aid (location finder).

Senior category (18-25 years): First: Andrew MacLachlan, King Edwards School (see above). Second: Chris Tanner, Kingswood School, Bath: an intruder-activated light switching system. Third: Owen Dannatt, Bancroft's School, Woodford Green, Essex: a swimming pool timing clock. Highly commended: Anthony Dearden, St. Anselm's College, Birkenhead: a guitar learning aid. Leon Hughes, Brunel University: a vertigo surveillance system. Shaun O'Mahony, Leeds Grammar School: a robotic lighting effect device. Martin Peek, Brunel University: a pacer pro rally navigation aid.

Intermediate category (15-17 years): First: Richard Paget, Bolton School (see above). Second: Edith Butterfield, St. Margaret's Senior School (see above). Third: Tom Maxwell-Wood, Zoe Spenser, Ashley Buck and Alex Dodkin of The Blue School (see above). Highly Commended: Lars Blackmore, Sevenoaks School: an atheletes' track timer; Michael Leslie, Kingussie High School: a CD storage device; John Wyllie, David Kelnar, Ramsay Waller and Johathan Scott, Merchiston Castle School, Edinburgh: Hamlet, a computerised theatre lighting system.

Junior category (under 15 years): First: Martin Rosinski, Coates Endowed Middle School, Ponteland, Northumberland: a side wind warning device for lorries. Second: James Keigher and Richard Levien, Radley College, Oxfordshire: a karaoke machine. Highly commended: Welby McRoberts, Merchiston Castle School, Edinburgh: an electronic maze; Alastair Lynch, Merchiston Castle School, Edinburgh: a remote phone ringer; Valerie Diederichs and Lucy Palariet, Godolphin & Latymer School, London: a bus stop indicator.

For more information about YEDA's annual awards, contact The Yeda Trust, 60 Lower St., Pulborough, W. Sussex RH20 2BW. Tel 01798 874767 Fax 01798 873550 Email postmaster@yeda.compulink.co.uk

ETI News...

Hitachi H8.3644F low power microcontroller with onboard flash

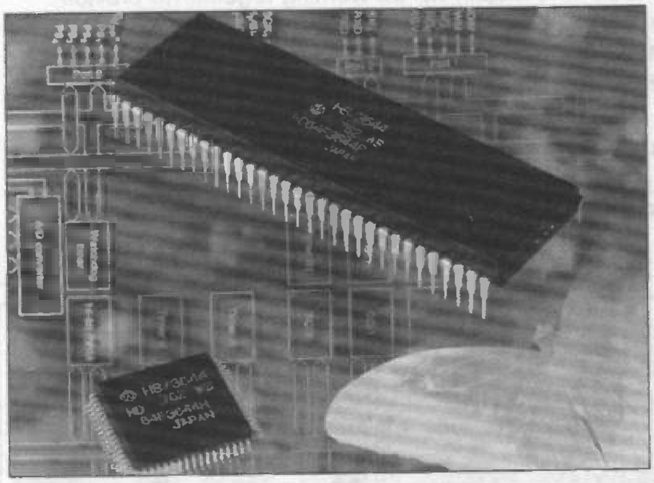
Hitachi's new H8/3644F is a new, low cost 8-bit microcontroller with an impressive speed/power ratio. At 10MHz the device can carry out a 16-bit add in 400ns, while consuming only 5mA. For the lowest power consumption, it can run at 32kHz, requiring only 10uA. At such low current consumption, a pair of AA cells should last almost for their shelf-life.

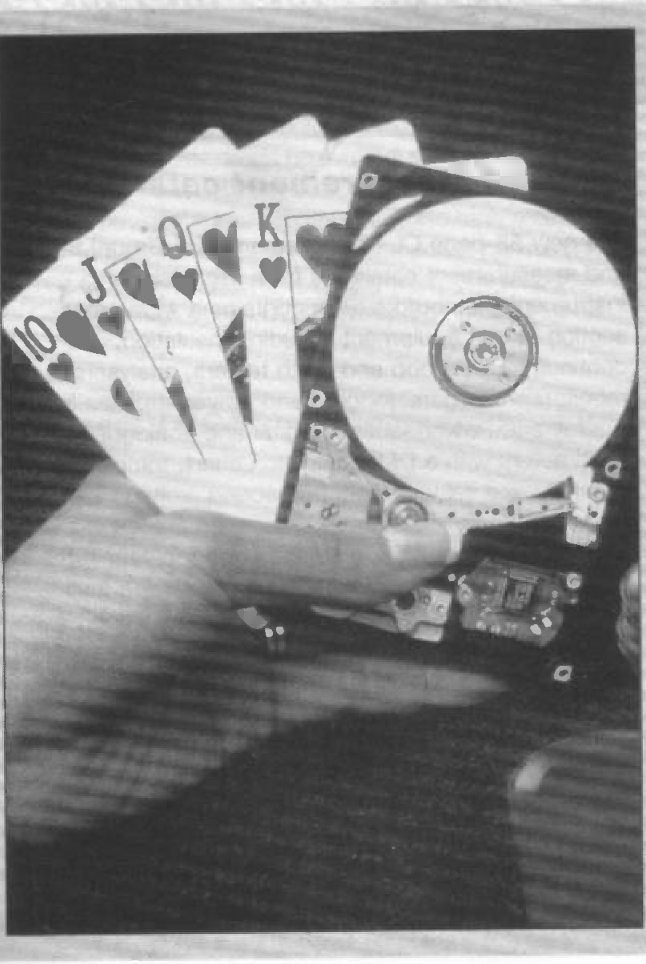
The H8/3644F contains 32k of on-board flash memory, permitting in-circuit programming. The chi also includes 1k of static ram, a 16-bit timer (with four input capture and two output compare registers), three 8-bit timers, a watchdog timer, an eight-channel 8-bit a to d converter, 53 I/O pins, a UART and a synchronous serial port.

To optimise the power versus speed equation, the processor can control its own clock speed using the programmable clock presecaler.

The EVB3644F evaluation kit includes an evaluation board with a socketed H8/3644F running at 10MHz, a flash programming board, and a Windows flash memory programming interface. Software tools include a GNU C compiler, flash programming software and HDI Windos source level debugger. The H8/3644F is available either in a 64 pin SDIP or a QFP package.

For more information contact Vince Pitt, Hitachi Europe Ltd., Whitebrook Park, Lower Cookham Rd., Maidenhead, Bertsk SL6 8YA. Tel 01628 585163 Fax 01628 585160.





Card-size hard drive set to increase the capacity of notebook computers

IBM has released the world's highest capacity hard disk for notebook computers. The 2.5-inch (12.5mm) Travelstar 6GT holds 6.4 gigabytes, which is around three times as much information as the average notebook hard drive currently contains.

The 6GT is the first notebook computer to come onto the market with IBM's Giant Magnetoresistive (GMR) head. The storage space of more than 4 billion bits per square inch outstrips the previous record (also held by IBM) by more than a billion bits per square inch. The GMR head is small enough to fit on the tip of a pencil and has achieved more than 11 billion bits per square inch in lab tests.

The technology allows a higher density of data to be stored on a smaller disk. Disks of this type can hold larger programs and graphics images and other data important to business users, web designers and other data-intensive applications.

The Travelstar 6GT, true to its name, has been ruggedised for everyday mobile use and also comes in a 5.4 gigabyte model.

Dell Computer Corporation as well as IBM itself are planning to use the drive in the Inspiron, Latitude and ThinkPad notebooks this year.

For more information about the Travelstar drives, contact 01795 568525 or IBM's mass storage website www.ibm.com/storage

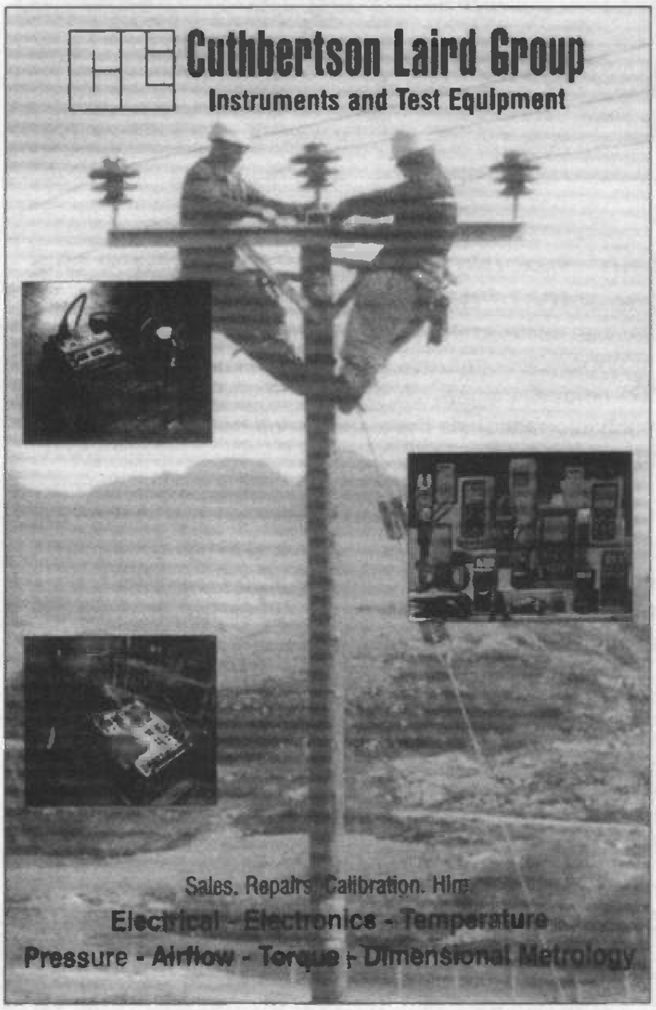
ETI ELECTRONICS TODAY INTERNATIONAL News...

Maplin joins the RSGB

Maplin Electronics has signed up as a member of the Radio Society of Great Britain. The RSGB and Maplin believe that membership will allow "closer links to be forged" between the popular component supplier and the UK representative of licensed Radio Amateurs. "The RSGB and Maplin will be working together to provide more information to customers about amateur radio and the equipment needed, with the aim of broadening the hobby," said an RSGB spokeswoman.

Customers at Maplin shops can pick up free, specially prepared RSGB information packs.

For more information and store locations, concact Maplin on 01702 554002.



European Space Talk Continues

The European Community and the European Space Agency (ESA) have approved a joint initiative to work together more closely to develop Europe's space programmes.

The resolution calls for the European Community and the Director General of ESA to involve each other more closely in defining action plans, particularly for satellite telecomms, Earth observation and navigation systems.

At a party in Brussels to celebrate to mark the 25th anniversary of the European Space Conference, UK Space Minister John Battle and Belgian Space Minister Yvan Ylieff announced the resolution.

Mr. Battle said: "I am delighted that the UK has played a key role in securing agreement to this resolution, which has the active support of all member states of both bodies." ESA's ruling Council is holding a two-day meeting in Brussels to coincide with the above celebration, during which it will also discuss ways of reducing the ESA's overhead costs.

MODMODMODMODMODMOD

In the 18-Channel Remote Control System (ETI Issue 9 1998) the 18-key encoder transmitter IC, IC1 BL9148, is also £8.00.

Test and Measurement catalogue

The new 56-page CL (Cuthbertson Laird Group) test and measurement catalogue from Professional Instrument Distributors (PID) contains a wide cross-section of test equipment including insulation, continuity, RCD, loop and earth testers, analysers, monitors, recorders, loggers and power supplies in the Energy and Power section, digital and analogue multimeters with a DMM selection chart, temperature, humidity and velocity, light and sound, voltage detection, tachometers and stoboscopes, gas detection and analysis, test leads and tool kits in the Safety and Environmental sections, cable and fault location, HV testers, test and oil test sets, signal sources, oscilloscopes and time and frequency meters among many others in the general electrical and electronic section.

The colour catalogue is available free from Quiswood Ltd., 01756 799737 or from PIC, 3 Brackenley Court, Embsay, North Yorks BD23 6PX.

OVERSEAS READERS

To call UK telephone numbers, replace the initial 0 with your local overseas access code plus the digits 44.

ETI News...

ELECTRONICS TODAY INTERNATIONAL

Three new USB microcontroller families from Cypress Semiconductor

Cypress Semiconductor has added three microchip families to its line of Universal Serial Bus (USB) microcontollers. The devices are designed for standalone USB hub applications, hubs integrated into keyboards and monitors, and individual peripherals such as modems.

The Cypress microcontroller line was developed specifically for USB applications, rather than using general-purpose architecture with functions not needed by the USB. The devices integrate various technologies, including SRAM, eprom and a high-performance RISC processor.

The CY7C66xxx family is designed for USB keyuboards with integrated hubs. Hubs increase the number of peripherals that can be attached to a PC by splitting one line into many. A USB keyboard/hub connects directly into one of the PC's USB ports, and then provides four other ports through which further peripherals can be connected. The CY7C66xxx devices can also offer up to 8KB or eprom and up to 39 general-purpose I/Os.

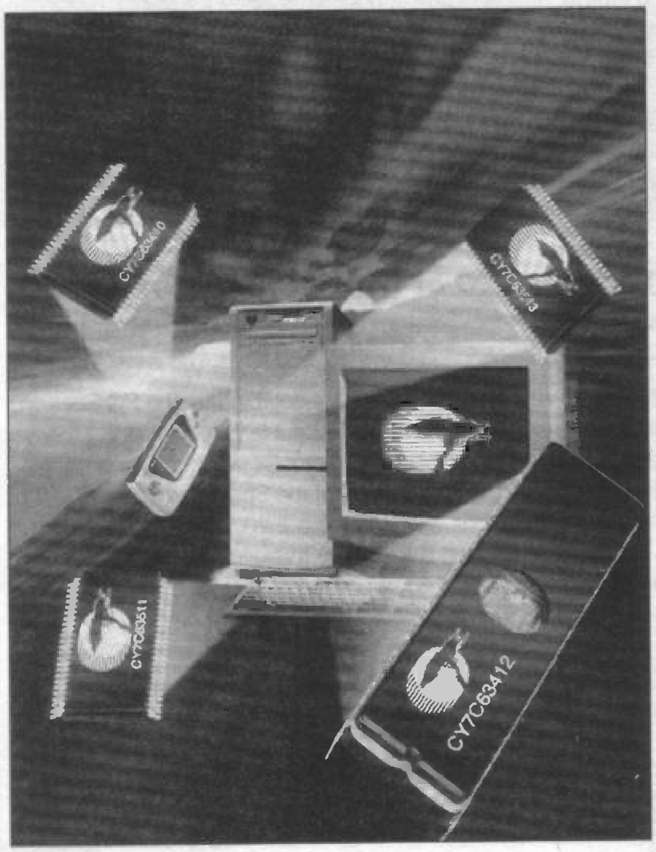
The CY7C65xxx family is designed for standalone hub applications, and hubs integrated into monitors. They provide 7- and 4-port hubs, an I2C interface for external communications, and up to 22 general-purpose I/Os.

The CY7C64xxx family addresses high-speed peripheral applications such as USB modems, providing up to 36 general purpose I/Os, I2C capability and up to 8KB of eprom.

The Cypress USB microcontrollers contain a built-in watchdog timer that needs no external timer circuitry. They offer internal clock doubling from a 6-MHz crystal to insure low electromagnetic interference. They also have a zero-power "instant on" capability to reduce power consumption by 70 percent while providing full asynchronous response.

Cypress's high-speed USB Developer's Kit costs £310 with debug, USB source code, reference designs and documentation.

For more information contact Paul Mayes, Cypress Semiconductor (UK) Ltd., Gate House, Fretherne Road, Welwyn Garden City, Herts AL8 6NS. Tel 01707 338888 Fax 01707 338811 Web www.cypress.com



Compact LCD panel meter from Vann Draper

Vann Draper Electronics' PM-128 3.5-digit LCD panel meter is a compact high performance module suitable for applications from prototyping to production runs. The circuit of the meter is based on a surface mount 7106 Ic using dual slope integration. The high contrast display includes annunciators for over range, decimal point (with selectable decimal point position) and polarity, with accuracy better than .05 percent with a reading rate up to x3 per second.

The meter measures 68 x 44mm with 13mm character height and includes a removable front panel bezel and full instructions.

For more information contact Vann Draper Electronics Tel 0116 2771400.

Year 2000 BIOS Fix

American Megatrends Inc. have developed a hardware card to ensure that the PC BIOS is not adversely affected by the potential Year 2000 change-of-date problem. The Year 2000 Enabler changes the system BIOS code so that the BIOS will read the time and date correctly. According to AMI, The Year 2000 BIOS Enabler card works on any major system BIOS. The card is designed to occupy a spare slot and integrate seamlessly into the boot-up sequence once installed.

AMI also warn that correcting the BIOS will not address any Y2000 problems relating to software, peripherals and other parts of the computer system, which must be addressed individually.

The one-off price for the card is £57.95, including the Y2000 test diskette

For further information in the UK phone 01293 882288 Fax 01293 886550. A catalogue is also available.

ETI Electronics Today International News...

Schools solar systems get lift-off

In a damp, cloudy British July this year, Energy minister John Battle activated the first of 100 solar panel systems due to be installed in UK schools and colleges. The photovoltaic cell systems are being installed under the Governments Foresight Scholar programme, designed to promote scientific and technical research and development. A further 16 schools have been cleared to fit solar systems.

The initial installation at the Cardinal Hinsley school in Willesden, West London, is a canopy of cells intended to provide enough energy to power a suite of computers in the school's science building. The package also includes a computer and information, giving access to the Internet and acting as the centre of a network. The schools taking part in the scheme will be demonstration sites for photovoltaic (PV) technology as well as teaching.

John Battle told the school: "The Government is considering how to meet 10 percent of electricity needs from renewable sources by 2010, which will be a four to five-fold increase on the current level. I have been impressed by the enthusiasm of the students I have seen here today for all aspects of sustainable energy, guided and supported by staff."

He added: "May the sun shine on all of you." - Just in time for the summer vacations.

Version 2.20 of Ivex WinBoard released with extras

The PC solution has released CAD package WinBoard 2.20, replacing V2.1. The new version, according to The PC Solution, includes many refinements and useful features, including the ability to launch the Specctra autorouter without having to leave WinBoard. A new version of the Specctra Interface automatically installs with WinBoard 2.20.

A second addition is the ability to launch Ivex View directly from WinBoard 2.20 and open Gerber files from inside WinBoard to view all selected objects before outputting.

A further useful addition is an electrical design rule check (EDRC) which allows the designer to check for violations of the net properties such as net isolation (spacing). The EDRC will check each net according to netlist stored values specific to that net, whereas typical mechanical design rule checking (MDRC) only checks global spacing violations.

EDRC properties are required for the proper operation of the circuit. MDRC properties are required for the manufacturing process. Different board makers apply different tolerances according to what they are capable of achieving, so that MDRC rules will change from manufacturer to manufacturer. The WinBoard PCB layout program already includes over 60 advanced MDRC checks to ensure the board has been laid out to foundry specifications.

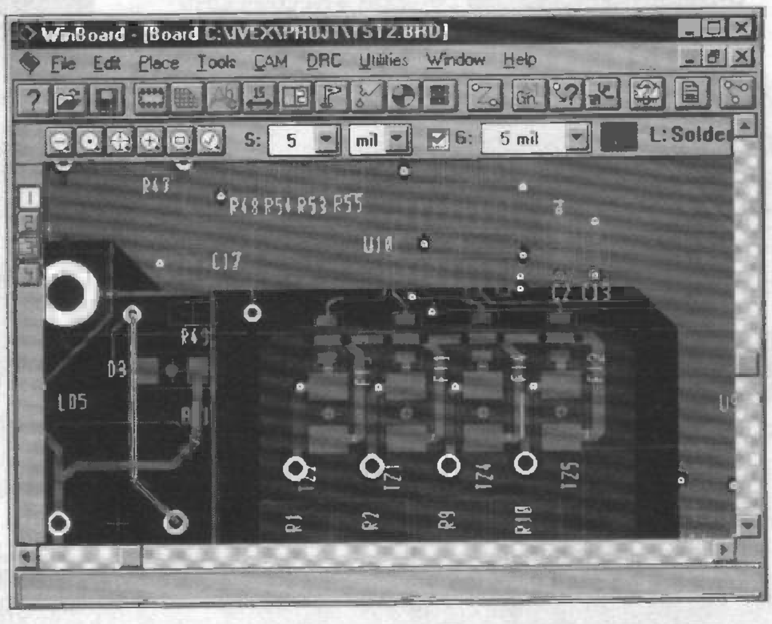
WinBoard's Real-Time DRC will now display the reason why an object cannot be placed in a location if a violation has occurred. Real-Time DRC can be run while routing the board, allowing designers to fix violations as they happen; alternatively Real-Time DCR can be turned off and the violation check carried out after layout.

Some of the further additions to WinBoard 2.20 include the ability of generate Drill symbols corresponding to drill holes on the board; re-number modules (Part Reference) on a board file; a Hotkey to go off-grid quickly when routing; a hotkey to reset the origin bookmark; the option to turn off auto-pan to prevent automatic scrolling; the ability to disable the netlist compile. The reference manual and users guide has been revised.

The unlimited pin capacity version of WinBoard is still only £395. Registered customers can purchase a new WinBoard version 2.20 for the update price of £35.

Free demo versions of Ivex WinDraft and WinBoard can be downloaded from The PC Solution Website at www.thepcsol.demon.co.uk. These demos are fully functional programs limited to an 100-pin capacity, and can be used as a viewer to view any size of design. Both programs run on Windows 95/98 and NT.

For more information contact The PC Solution, 2a High Road, Leyton, London E15 2BP. Tel 0181 926 1161 Fax 0818 926 1160. Email info@thepcsol.demon.co.uk.



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Gould OS 245A/250/255/300/3000/3351/4000	from £125
Hewlett Packard 180A/180C/181A/182C	from £200
Hewlett Packard 1740A, 1741A, 1744A, 100MHz dual ch	from £350
Hewlett Packard 54100D – 1GHz Digitizing	£2995
Hewlett Packard 54200A – 50MHz Digitizing	£650
Hewlett Packard 54201A – 300MHz Digitizing	£1500
Hitachi V650F – 60MHz Dual Channel	£350
Hitachi V152F/V302B/V302F/V353F/V550B/V650F	from £125
Intron 2020 – 20MHz Digital Storage (NEW)	£650
Iwatsu SS 5710/SS 5702 – 20MHz	from £125
Kikusui COS 6100 – 100MHz, 5 Channel, 12 Trace	£475
Kikusui 5100 – 100MHz – Dual Channel	£350
Meguro – MSO 1270A – 20MHz Digital Storage (NEW)	£850
Nicolet 310 – L.F. D.S.O. with twin Disc Drive	£550
Nicolet 3091 – L.F. D.S.O.	£900
Lecroy 9450A – 300MHz/400 Ms/s D.S.O. 2 ch	£2250
Philips PM 3211/PM 3212/PM 3214/PM 3217/PM 3234/PM 3240/PM 3243/PM 3244/PM 3261/ PM 3262/PM 3263/PM 3540	from £125
Philips PM 3295A – 400MHz Dual Channel	£1750
Philips PM 3335 – 50 MHz/20Ms/s D.S.O. 2 ch	£1500
Philips PM 3055 – 50 MHz DUAL Timebase	£450
Tektronix 434 – 25MHz – 2 Channel Analogue Storage	£250
Tektronix 454 – 150MHz – 2 Channel	£400
Tektronix 468 – 100MHz D.S.O.	£750
Tektronix 2213 – 60MHz Dual Channel	£425
Tektronix 2221 – 60MHz Digital Storage 2 Channel	£1500
Tektronix 2215 – 60MHz Dual trace	£450
Tektronix 2235 – 100MHz Dual trace	£800
Tektronix 2335 – Dual trace 100MHz (portable)	£750
Tektronix 2225 – 50MHz dual ch	£450
Tektronix 2440 – 300 MHz/500 Ms/s D.S.O. 2 Ch	£3750
Tektronix 455 – 50MHz Dual Channel	£350
Tektronix 464/466 – 100MHz An storage	from £350
Tektronix 465/465B – 100MHz dual ch	from £350
Tektronix 475/475A – 200MHz/250MHz Dual Channel	from £475
Tektronix 485 – 350MHz – 2 channel	£900
Tektronix 5403 – 60MHz – 2 or 4 Channel	from £250
Tektronix 7313, 7603, 7613, 7623, 7633, 100MHz 4 ch	from £300
Tektronix 7704 – 250MHz 4 ch	from £650
Tektronix 7904 – 500MHz	from £850
Trio CS-1022 – 20MHz – Dual Channel	£125

Other scopes available too

SPECIAL OFFER

HITACHI V212 – 20MHZ DUAL TRACE	£180
HITACHI V222 – 20 MHZ DUAL TRACE + ALTERNATE MAGNIFY	£200

SPECTRUM ANALYSERS

Advantest 4133B – 10KHz – 20GHz (60GHz with external mixers) + Ext. Keyboard	£7250
Advantest 4131B – 10KHz – 3.5GHz	£4950
Ando AC8211 – Spectrum Analyser 1.7GHz	£2950
Anritsu MS610B – 10KHz – 2GHz – (Mint)	£4750
Anritsu MS341A + MS3401B – (10Hz – 30MHz	£3995 + £4995
Anritsu MS62B – 10KHz – 1700MHz	£2500
Avcom PSA65 S – 1000MHz – portable	£1500
Hewlett Packard 3580A – 5Hz-50KHz	£995
Hewlett Packard 182T with 8559A (10MHz – 21GHz)	£3750
Hewlett Packard 35601A – Spectrum Analyser Interface	£1000
Hewlett Packard 3562A Dual Channel Dynamic Sig. Analyser	£7500
Hewlett Packard 3562A Dual Channel Dynamic Sig. Analyser	£7500
Hewlett Packard 853A + 8558B – 0.1 to 1500MHz	£3250
Hewlett Packard 182T + 8558B – 0.1 to 1500MHz	£2750
Hewlett Packard 8754A – Network Analyser 4-1300MHz	£2000
Hewlett Packard 8591A – 9KHz – 1.8GHz	£4995
Hewlett Packard 8594E – 9KHz – 2.9GHz	£7000
Hewlett Packard 3582A – 0.02Hz – 25.6KHz (dual ch.)	£2000
Hewlett Packard 3585A – 20Hz – 40MHz	£4995
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Marconi 2371 – 30KHz – 2000MHz	£1250
Meguro MSA 4901 – 1-300GHz (AS NEW)	£1500
Meguro MSA 4912 – 1-1GHz (AS NEW)	£1995
Polrad 641-1 – 10MHz – 18GHz	£1500
Rohde & Schwarz – SWOB 5 Polyskop 0.1 – 1300MHz	£1800
Takeda Riken 4132 – 1.0GHz Spectrum Analyser	£2500
Tektronix 7L18 with mainframe (1.5-60GHz with external mixers)	£2000
Tektronix 495P – 100Hz – 1.8GHz programmable	£4950

MISCELLANEOUS

Adret 740A – 100KHz – 1120MHz Synthesised Signal Generator	£800
ANRITSU ME 462B DF/3 Transmission Analyser	£3000
Danbridge JP30A – 30KV Insulation Tester	£1500
Anritsu MG642A Pulse Pattern Generator	£1500
Dranetz 626 – AC/DC – Multifunction Analyser	£850
EIP 331 – Frequency counter 18GHz	£700
EIP 545 – Frequency counter 18GHz	£1500
EIP 545A – Frequency counter 18GHz	£1600
EIP 575 – Frequency counter 18GHz	£1750
Farnell AP70-30 Power Supply (0-70v/30A) Auto Ranging	£750
Farnell TSV-70 MKII Power Supply (70V – 5A or 35V – 10A)	£250
Farnell DSG-1 Synthesised Signal Generator	£125
Farnell ESG-1000 Synthesised Signal Generator 1GHz (as new)	£1650
Flure 5100A – Calibrator	£2500
Guildline 9152 – T12 Battery Standard Cell	£550
Hewlett Packard 331A – Distortion Analyser	£300
Hewlett Packard 3336C – Synthesised Signal Generator (10Hz – 21MHz)	£1000
Hewlett Packard 3437A System voltmeter	£350
Hewlett Packard 3456A Digital voltmeter	£850
Hewlett Packard 3438A Digital multimeter	£200
Hewlett Packard 3488A – Switch/Control Unit	£650
Hewlett Packard 35600A Dual Ch. Dynamic Signal Analyser	£3750
Hewlett Packard 3711A/3712A/3791B/3793B Microwave Link Analyser	£2250
Hewlett Packard 3325A – 21MHz Synthesiser/Function Gen	£1500
Hewlett Packard 3488A – HP – 1B Switch control unit (various Plug-ins available)	£650
Hewlett Packard 3455A 6½ Digit M/Meter (Autocal)	£750
Hewlett Packard 3478A – Multimeter (5½ Digit) + HP – 1B	£550
Hewlett Packard 3586A – Selective Level Meter	£1000
Hewlett Packard 3776A – PCM Terminal Test Set	£1500
Hewlett Packard 3779A/3779C – Primary Mux Analyser	from £600
Hewlett Packard 3784A – Digital Transmission Analyser	£4995
Hewlett Packard 37900D – Signalling Test Set (No 7 and ISDN)	£6000
Hewlett Packard 4262A – Digital LCR Meter	£1350
Hewlett Packard 4275A – LCR Meter (Multi-Frequency)	£3950
Hewlett Packard 4338A – Millionmeter (As New)	£2000
Hewlett Packard 4342A 'Q' Meter	£995
Hewlett Packard 435A or B Power Meter (with 8481A/8484A)	from £750
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Hewlett Packard 4972A – Lan Protocol Analyser	£1750
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Hewlett Packard 6622A – Power Supply, Dual O/P	£1650
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Hewlett Packard 6652A – Power Supply (0 – 20V, 0 – 25A)	£1250
Hewlett Packard 6264B – Power Supply (0 – 20V, 0 – 25A)	£400
Hewlett Packard 7475A – 6 Pen Plotter	£250
Hewlett Packard 7550A – 8 Pen Plotter A3/A4	£450

HEWLETT PACKARD 6261B
Power Supply 20V-50A £450 ***Discount for Quantities***

Hewlett Packard 83555A – Millimeter – Wave source Module 33-50GHz	£4250
Hewlett Packard 8015A – 50MHz Pulse Generator	£750
Hewlett Packard 8405A – Vector Voltmeter	£350
Hewlett Packard 8165A – 50MHz Programmable Signal Source	£1650
Hewlett Packard 8350B – Sweep Oscillator Mainframe (various Plug-Ins available) extra	£2650
Hewlett Packard 8152A – Optical Average Power Meter	£1250
Hewlett Packard 8158B – Optical Attenuator (OPTS 002 + 011)	£1100
Hewlett Packard 8180A – Data Generator	£1500
Hewlett Packard 8182A – Data Analyser	£1500
Hewlett Packard 8350B – Sweep Oscillator Mainframe (vanous plug-in options available)	£2500
Hewlett Packard 83554A – Wave Source Module 26.5 to 40GHz	£3500
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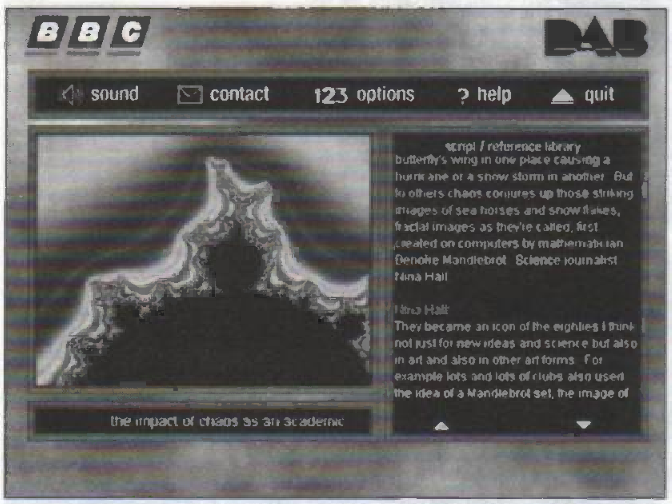
Data on the Airwaves

Digital Audio Broadcasting (DAB) radio is gathering in the wings, waiting to burst on the scene. Historically, it may be a step forward for radio broadcasting, especially for those with car radios, but data by radio has been developing for years to build up to this point.

Mike Bedford

The date - 12th December 1901. The place - Signal Hill, Newfoundland, Canada. History was about to be made. Present at this site overlooking the Atlantic Ocean was Gugielmo Marconi, and stretching out above him was 400 feet of wire held aloft by a massive kite. As the pre-arranged time approached, Marconi turned on his receiving equipment and listened intently. Then, through the noise of the static, the letter "S" in Morse Code could be heard - faint and distorted but quite clearly. That signal had originated over 2,000 miles away in Poldhu, Cornwall, Great Britain, and the world received the news in awe - this was the first time a wireless signal had been transmitted across the Atlantic.

The date - 27th September 1995. The place - the radio theatre, Broadcasting House, London, Great Britain. Another bit of radio history was about to be made. Present on this occasion was Liz Forgan, then Managing Director of Network Radio at the BBC. The event was the official launch of Digital Audio Broadcasting (DAB), making the UK - and Sweden, whose service was launched on the same day - the first countries in the world to have a digital radio service.



A multimedia DAB demonstration by the BBC. This is not to say that the BBC will be broadcasting pages like these - but it is technically possible with the right equipment to receive the data

If the second event was not quite so momentous as the first, it was still a milestone in the history of radio transmission, and the two events are more intimately connected than first impressions might suggest. The world's first radio transmissions used Morse Code, the world's first code for data transmission. With the launch of DAB, radio transmission comes full circle. Instead of the familiar analogue amplitude or frequency modulated carrier, DAB transmits data. Certainly, much of that data is used to reconstitute an audio signal in the receiver, but the basic material being transmitted is essentially the same as it was in Marconi's day: strings of data.

1998 was expected to be the year of DAB in the UK, and may be yet. Despite the launch in 1995, it will only be accessible to the majority of the UK in 1998. Without a doubt, DAB is going to be heavily hyped: the BBC have started advertising it on their TV channels.

So although this article has been prompted by the launch of DAB, it will cover the subject of data transmission by radio much more broadly. Although data radio should be seen as a progression, this is not a historical feature - virtually all the techniques described here are in use today.

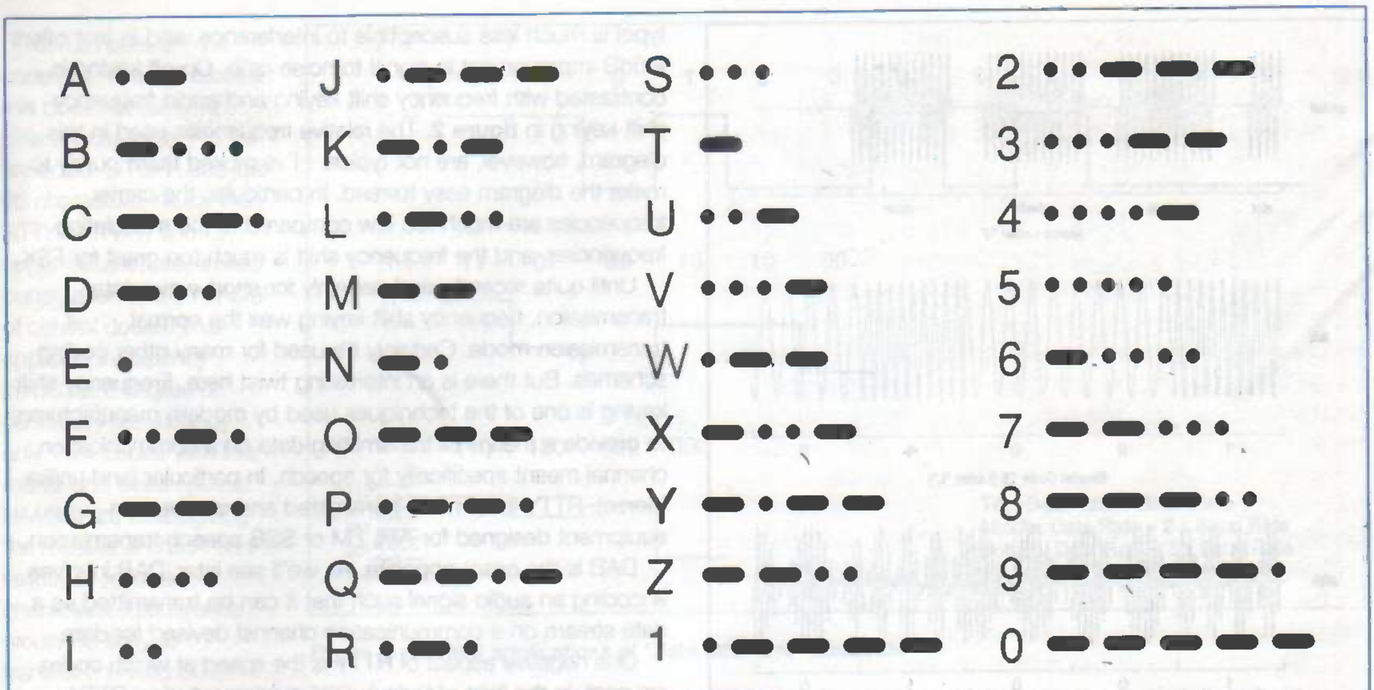


Figure 1: the Morse code alphabet, showing the relative symbol lengths

Morse Code

If you're not a radio amateur - and quite possibly if you are - Morse Code probably conjures up an archaic image of a Telegraph operator in a Wells Fargo office by a railroad in the Nevada desert late last century. And although the use of Morse Code seems to be in terminal decline, it hasn't yet been totally ousted. Furthermore, Morse Code can introduce a number of concepts which we shall build on as we look at more advanced methods of data transmission.

The one thing that everyone remembers about Morse Code is that it signals each letter as a combination of short and long signals, often called dots and dashes in recognition of the notation used to write the code down. Originally, Morse was used for transmitting signals by telegraph - that is, by wire - but in radio transmission, dots and dashes are signalled by the presence of a carrier (the "mark" state), and the gaps by the absence of a carrier (the "space" state). This most basic modulation method of data transmission is usually called on-off keying.

I have included **figure 1** because we can learn some interesting facts about it just by taking a look at the information presented. First of all, dots are a single time unit, and dashes are three time units. Dots and dashes within a letter are separated by a single time unit space, and letters are terminated by a three-unit space. Clearly different letters and figures are of different lengths. The letter E, at four units long (including the following three-unit space) is the shortest, and of the letters, J, Q and Y are the longest at 16 units. The Morse symbols were chosen very deliberately. You probably know that E is the most common letter in the English language, accounting for around 10 percent of all letters, but you may not have known that J is the least frequent at significantly less than 1 percent. Q and Y are not particularly common, either. This system of assigning short codes to common letters may mean that some rare letters have very long codes, but it is a good way of improving transmission efficiency. In fact, this is the technique used in Huffman encoding, one of the first methods devised for compressing ascii computer data. In Morse, taking into account the frequency of the various letters, the average length of Morse characters in plain English text is about 8 bits. This compares favourably with the length of ascii text, once start and stop bits have been added.

The Morse character set is much more limited than ascii (no lower case characters, no accented characters, limited punctuation and so on), but Morse was designed to be transmitted by hand and (normally) read aurally. Had it not been necessary to make the code user friendly and relatively insensitive to poor sending, it could have been made much more efficient: for instance, dashes need only have been twice as long as dots. Later on, we'll look at bandwidth considerations. For now, remember that Morse is about the most efficient in this respect. The catch is - as we'll see - that this is a direct consequence of it being just about the slowest form of communication imaginable.

And what of Morse today? Certainly it is still used by radio amateurs, and the proven ability to transmit and receive Morse is still an international requirement for obtaining an amateur radio licence for the short-wave bands. In professional communications, Morse is still used for ship-to-shore communication in some counties, although it was phased out in the UK at the beginning of this year.

The radio teleprinter

If we exclude Morse which - although it is occasionally transmitted and received by computer - was designed as a manual system, data transmission is, by and large, automated. Although some advanced methods today involve variable-length codes, traditionally, automation has required the use of fixed length symbols. Since Morse's variable length proved an advantage, going to a fixed length code must seem a retrograde step. However, considering that early automated data transmission was based on electro-mechanical equipment, it's clear that using variable-length symbols would have been almost impossibly complicated. This legacy remains with us: by far the most common coding system in today's computers, ascii, is a fixed length code.

But ascii wasn't the first such code. The first widely adopted code was Baudot, and the equipment used to generate and decode it was the teleprinter. This is like an electric typewriter that transmits codes for the characters typed on the keyboard

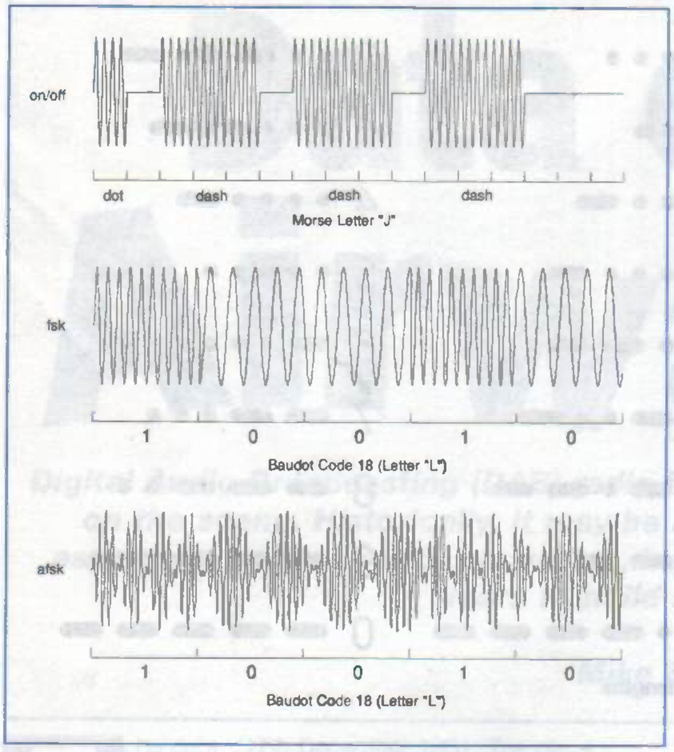


Figure 2: on-off keying (Morse) contrasted with frequency shift keying (Baudot) and audio frequency shift keying (Baudot). The frequencies are no typical, and have been chosen to stress the differences.

and prints out the characters corresponding to the codes received. The Baudot Code, otherwise known as the Murray Code, is a five bit code, so it is more efficient than Morse, even though it is fixed-length. Nevertheless, it still only copes with a limited character set containing upper case letters only. But if you've done the binary calculation, you've probably figured out that a five-bit code allows only 32 different characters, insuffcent even for 26 letters and 10 figures. This apparent anomaly is explained by the fact that two characters are assigned to each code - normally one letter and one figure or punctuation - and special "shift" codes are used to switch between letters and figures. Some codes are also assigned to control functions such as carriage return, line feed, and bell.

Much could be said for the use of teleprinters over land-lines, but our main interest here is radio teletype, also called RTTY.

Although Baudot Code could be transmitted, like Morse, by on-off keying, it is actually almost always transmitted by frequency shift keying. Here, the carrier is modulated (using AM, FM or SSB) with one audio tone to indicate mark - the binary ones in the code - and a different audio tone for space - the binary zeros. Strictly speaking, what I've just described is audio frequency shift keying, and is far more common than the alternative method of shifting the carrier frequency. In the case of SSB modulation, however, audio frequency shift keying produces what is essentially a frequency shifted carrier. Compared to on-off keying, frequency shift keying (of either type) is much less susceptible to interference, and in fact offers a 6dB improvement in signal to noise ratio. On-off keying is contrasted with frequency shift keying and audio frequency shift keying in **figure 2**. The relative frequencies used in this diagram, however, are not typical - I've picked them purely to make the diagram easy to read. In particular, the carrier frequencies are much too low compared to the modulating frequencies, and the frequency shift is much too great for FSK.

Until quite recently, and certainly for short-wave data transmission, frequency shift keying was the normal transmission mode. Certainly it's used for many other coding schemes. But there is an interesting twist here. Frequency shift keying is one of the techniques used by modem manufacturers to provide a means of transmitting data on a communication channel meant specifically for speech. In particular (and unlike Morse), RTTY is normally transmitted and received on equipment designed for AM, FM or SSB speech transmission.

DAB is the exact opposite. As we'll see later, DAB involves encoding an audio signal such that it can be transmitted as a data stream on a communication channel devised for data.

One negative aspect of RTTY is the speed at which codes are sent. In the light of today's 56K modems, typical RTTY speeds of 50, 75 or 110 baud - up to 1,000 times slower than state of the art telephone modems - seem positively pedestrian. This is partly a result of its electro-magnetic origins. However, it's also due to the difficulty of data transmission on short-wave. As we'll see shortly, this can be improved by modem data transmission modes, but short-wave data transmission will never be fast. And despite the fact that Baudot Code is well past its "best before" date, it's still in widespread use. If you tune around the short-wave bands, you are likely to come across far more commercial RTTY than Morse.

SITOR

Although it's much less of a problem in the VHF and UHF bands where much of our broadcasting, local mobile communications, and satellite communication takes place, data transmission on the short-wave bands is problematic. Some of the main difficulties are selective fading, electrical noise, and interference from other stations. If a burst of static coincides with the transmission of a character by RTTY, it will probably cause the received signal to be misinterpreted. In plain speech, an odd wrong letter can usually be corrected by looking at the context, although this may be more of a problem on a very poor link which results in a high error rate. However, when a "letters" or "figures" control code is corrupted, all the characters up to the next control code will be misinterpreted. When transmitting coded groups of letters - not uncommon - one wrong character can be disastrous: there's no possibility of spotting and correcting such an error manually.

The coding system called SITOR (Simplex Teleprinter Over Radio) commercially and AMTOR by radio amateurs takes a first step to addressing this drawback. There are two different SITOR modes; first, let's take a look at aspects of SITOR which apply to both modes.

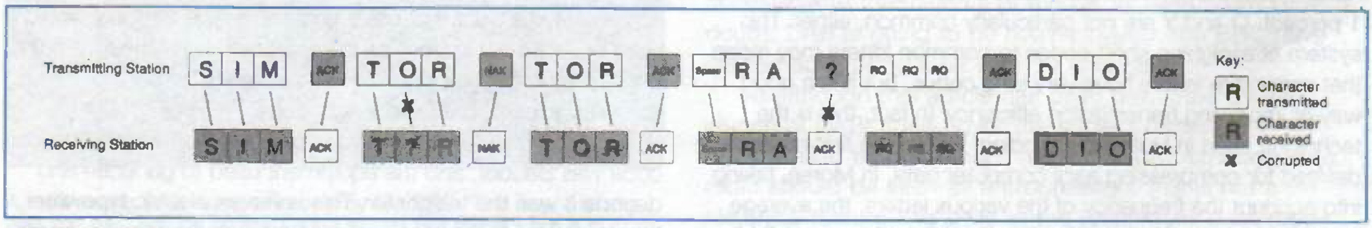


Figure 3: a diagram of a typical SITOR mode A transmission, showing the ACK and NAK codes used for error correcting

SITOR uses a 7-bit code but, unlike 7-bit ascii, this does not allow 128 different characters to be encoded. SITOR uses just 35 characters, much like RTTY with only figures, upper case letters, limited punctuation and a handful of control codes. This apparent inefficiency introduce a degree of necessary redundancy - only 7-bit codes with four marks and three spaces (4M/3S) are used, giving the receiver a check on the validity of received characters. Interference would be likely to transform a valid SITOR character into one which the receiver recognises as invalid. However, of far more use is a means of allowing an incorrect character to be corrected at the receiver. The two SITOR modes go about this in different ways.

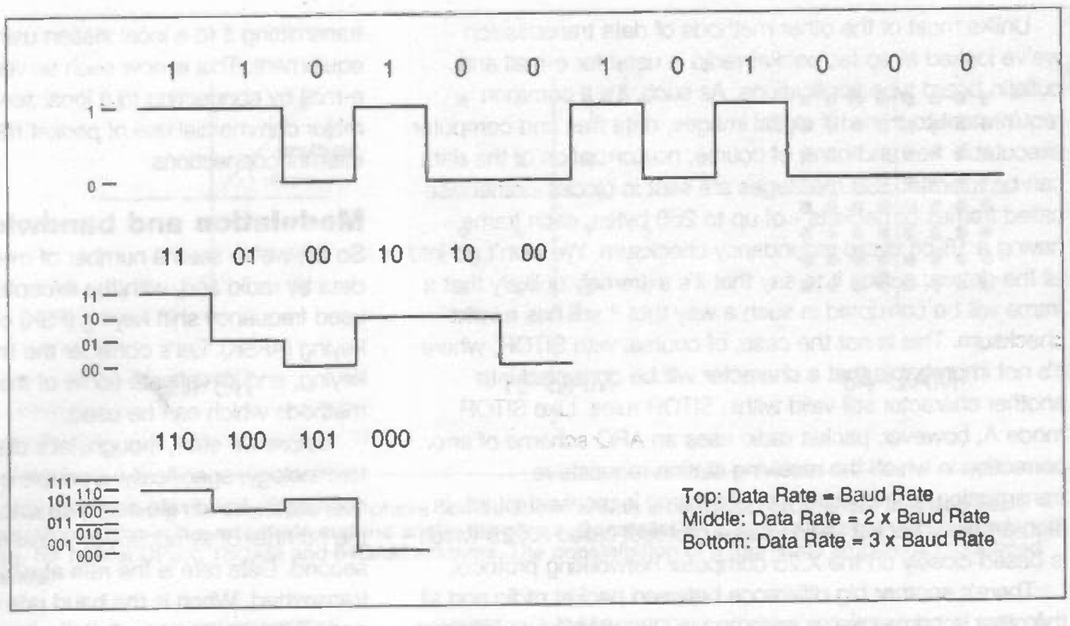


Figure 4: different applications of "data rate" and "baud rate"

Mode B is used for broadcasting, that is, multiple receiving stations which are not equipped to transmit back to the originating station. The error correcting scheme in mode B is primitive in the extreme - each character is transmitted twice. Bearing in mind that the commonly used speed is 100 baud, it's clear that the end result is slow. However, there is more to it. If both occurrences of a letter were to be transmitted one after the other, there's a good chance that a burst of static would wipe out, perhaps, three or four characters, taking out a repeated character along with the original. In SITOR mode B, however, the two data streams are separated by four characters. So, for example, a message starting "SITOR" would be transmitted as "2 1 2 1 2 1 2 1 S 1 I 1 T S O I R T...". (The characters shown as "2" and "1" are simply phasing signals which are used to synchronise transmitting and receiving stations at the start of a message.)

This method is generally known as a forward error correction scheme (FEC), but in mode A, an alternative method called automatic repeat request (ARQ) is used. An ARQ scheme is unusual as it can only work between a pair of stations both equipped for transmission and reception. In general terms, the originating station sends a block of characters and then switches back to receive and awaits a response from the receiving station. The receiving station responds with either an acknowledge code (ACK) or a negative acknowledge code (NAK) depending on whether the block consisted solely of valid characters or whether it contained a corrupted character. If the originating station receives an ACK code, it transmits the next block of characters. If a NAK code is received, the originating station re-transmits the corrupted block. In mode A, the blocks are three characters long and the criteria for deciding whether a character is valid is whether it corresponds to the 4M/3S pattern. The final bit of sophistication in mode A is that it allows for the ACK or NAK code to become corrupted. If an ACK or NAK code isn't received following the transmission of a block, the originating station sends a block consisting of special repeat characters (RQ) which requests the receiving station to re-send the ACK or NAK code. A typical SITOR mode A transmission is shown diagrammatically as **figure 3**.

As with RTTY, SITOR is sent by frequency shift keying at a low baud rate and its use is virtually restricted to the short-wave bands. Commercially, SITOR is about the most sophisticated data transmission scheme used on the short-wave bands, although radio amateurs use various other modes which aim to improve on speed and/or resilience to interference. For example, extensions to AMTOR have been introduced to facilitate the transmission of lower case characters, allowing short-wave AMTOR links to be used for packet radio as an alternative to a satellite link for inter-continental traffic. Generally, however, sophisticated techniques tend to be restricted to the higher frequency bands where propagation characteristics are more reliable.

You may recognise this demonstration screen from the BBC's 'Perfect Day' advertisement

Packet radio

With a more sophisticated error detection and correction scheme than the ones we've seen so far, higher speed data transmission can be achieved, even on the noisy short-wave bands. Packet radio is used on short-wave at 300 bits per second, but this is really a sensible limit. But when the more sophisticated protocol of packet radio is combined with the quieter conditions on the VHF and UHF bands where packet radio is mainly used, 9600 baud communication is quite feasible.

Unlike most of the other methods of data transmission we've looked at so far, packet radio is used for e-mail and bulletin board type applications. As such, it's a common requirement to transmit digital images, data files and computer executable files and here, of course, no corruption of the data can be tolerated. So messages are sent in blocks - otherwise called frames or packets - of up to 256 bytes, each frame having a 16-bit cyclic redundancy checksum. We won't go into all the details; suffice it to say that it's extremely unlikely that a frame will be corrupted in such a way that it still has a valid checksum. This is not the case, of course, with SITOR, where it's not improbable that a character will be corrupted into another character still valid within SITOR rules. Like SITOR mode A, however, packet radio uses an ARQ scheme of error correction in which the receiving station requests re-transmission, as necessary, until a frame is received intact. In fact, amateur packet radio uses a protocol called AX.25 which is based closely on the X.25 computer networking protocol.

There's another big difference between packet radio and all the other schemes we've seen so far. Like data on an Ethernet LAN, all packet radio frames include the addresses of the originating station and the destination. It's possible for multiple stations to share a single radio channel, greatly increasing the channel's capacity. If a station needs to transmit, it listens on the channel, only transmitting when it hears that it is clear. The first frame is then sent, after which the station listens for an acknowledgement. As soon as it's been confirmed that this first frame has arrived at its destination, the transmitting station prepares to send the next frame by waiting for the channel to become free once more. In the meantime, other stations will probably have sent frames. Clearly, therefore, frames which constitute a single message could well be separated by frames originating from and destined to other stations using the same channel. It's the job of the receiving station to reassemble a message from these isolated frames.

In the main, packet radio is used by the amateur radio community. Thousands of mailbox and repeater stations - mostly on the VHF and UHF bands - are scattered around the world. These act as a global network allowing, for example, someone to send a message to the other side of the world by transmitting it to a local station using low powered transmitting equipment. This is now seen as very similar to sending Internet e-mail by connecting to a local service provider. Indeed, a major commercial use of packet radio is to provide wireless Internet connections.

Modulation and bandwidth

So far, we've seen a number of mechanisms for transmitting data by radio and, with the exception of Morse Code, all have used frequency shift keying (FSK) or audio frequency shift keying (AFSK). Let's consider the limitations of frequency shift keying, and investigate some of the alternative modulation methods which can be used.

Before we start, though, let's clarify some of the terminology; specifically, a couple of terms which are frequently confused - baud rate and data rate. Baud rate is defined as the number of symbols - or signal transitions - transmitted per second. Data rate is the rate at which information is transmitted. When is the baud rate the same as the data rate and when do they differ?

A common method of encoding data is for two different signal states (which could be amplitude levels, frequencies, or phases) to represent binary zeros and ones. In this case, a symbol represents a single bit ; in other words, signal transitions can take place for every bit. In this case baud and data rate are same thing: a 1200bps data stream would be transmitted at 1200 baud. An alternative coding scheme involves assigning different signal states (once again, amplitude, frequency, phase, or a combination of these) to multiple bits. So for example, four signal states could represent the four combinations of two bits (00, 01, 10 and 11) or eight signal states could represent the eight combination of three bits (000, 001, 010, 011, 100, 101, 110, and 111). In this case, the data rate and the baud rate are clearly different. For example, with pairs of bits, a 1200 baud signal could carry data at 2400bps. These concepts are illustrated in **figure 4**.

Let's turn our attention to the bandwidth required to carry a signal at a given baud rate. For a given baud rate, the maximum signal frequency is half this figure in Hertz. So if

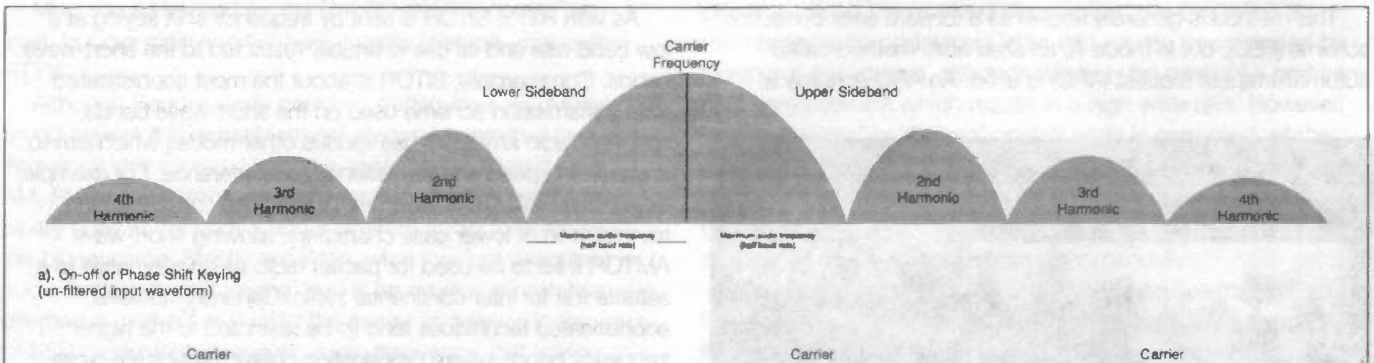


Figure 5: the relationship between fundamental frequency and harmonics in Phase Shift Keying, filtered Phase Shift Keying and filtered Frequency Shift Keying

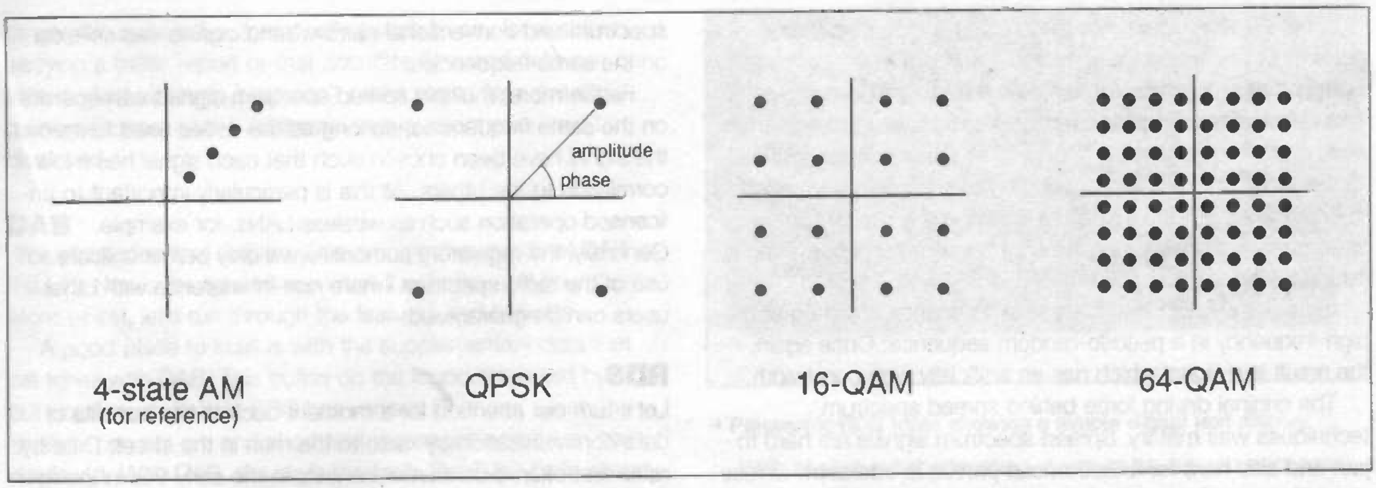


Figure 6: A common technique of summarising the amplitude and phase combinations is with a constellation diagram in which each combination is a vector, the length of which is the amplitude and the angle, the phase. Constellation diagrams using a vector with length = amplitude and angle = phase, for typical QPSK, 16QAM and 64QAM systems. The constellation of a four-state amplitude modulated signal is also shown for reference.

we're transmitting at baseband - that is, if we're transmitting down a length of wire and don't need to modulate the signal - this is the bandwidth of the signal. However, once we generate a modulated signal for transmission by radio, the bandwidth increases. What happens when a carrier is on-off keyed (or, for that matter, phase shift keyed)? If you're familiar with modulation methods, you'll know that the signal will spread on either side of the carrier, the width of these two "sidebands" being equal to the maximum frequency of the modulating signal. However, a square wave at a given frequency doesn't just contain that frequency; it is rich in harmonics, that is, it contains multiples of the fundamental frequency. So the modulated signal ends up with multiple lobes on either side of the carrier frequency corresponding to the second, third, fourth harmonics, and so on. In theory, the signal will be infinitely wide but in practice, the amount of power in the higher harmonics will be negligible, and beyond a certain point they can be ignored. With slow baud rates, this increasing bandwidth due to harmonics is often accepted since the signal will still be comparatively narrow. As the baud rate increases, however, the problem of harmonics has to be addressed. This is done by filtering the input waveform so that abrupt changes don't occur. This is an important technique in high baud rate modulation methods. Virtually all but the fundamental frequency is eliminated and the width of each sideband is the maximum modulating frequency. In other words, the complete signal has a bandwidth in Hertz which is equal to the baud rate. Parts **a and b of figure 5** contrast the spectra of on-off keying with an unfiltered and a filtered input waveform.

FSK can be thought of as two on/off keyed signals with slightly different frequencies, each of which has sidebands, the width of which are equal to the keying frequency. We'll assume that the input waveform has been suitably filtered as described above and so the resultant frequency spectrum is shown in **figure 5c**. Clearly, the bandwidth of an FSK signal is given by the following formula:

$$B = 2F + \Delta f$$

where F is the maximum keying frequency and Δf is the frequency shift, that is, the difference between the two frequencies. As the minimum allowable frequency shift is equal to the keying frequency, and the maximum signal frequency is half the baud rate, we can see that the minimum bandwidth of an FSK signal is one and a half times the baud rate. For example, a 1.8kHz channel permits a maximum baud rate of 1200 baud, and a 15kHz channel allows up to about 9600 baud.

For satellite communication in the microwave bands, where bandwidth is plentiful, high rates of data transmission are achieved using high bandwidth signals. In the lower frequency bands, however, bandwidth limits the baud rate and the technique of coding multiple bits into a single symbol is employed. Typically, phase, amplitude, or a combination is used. Common schemes are QPSK - Quadrature Phase Shift Keying, 16QAM, 64QAM, and even 256 QAM - 16, 64 and 256 Quadrature Amplitude Modulation in which 16, 64, or 256 combinations of phase and amplitude are used. A common technique of summarising the amplitude and phase combinations is with a constellation diagram in which each combination is a vector, the length of which is the amplitude and the angle, the phase. Constellation diagrams for typical QPSK, 16QAM and 64QAM systems are contrasted in **figure 6**. For reference, the constellation of a four-state amplitude modulated signal is also shown, although this is not a common technique. However, this technique of cramming more information into a given bandwidth by increasing the number of bits per symbol can't go on forever. In simple terms, this is because it becomes increasingly difficult to differentiate between ever smaller differences in phase and/or amplitude, especially in poor signal-to-noise ratio conditions. The information carrying capacity of any communication channel is given by the well-known equation:

$$bps = Blog^2(1+s/n)$$

where B is the bandwidth, and s/n is the signal to noise ratio. Telephone modems have already reached this limit, and 56k modems exceed it. This apparently impossible achievement is made possible by data compression. Data compression is, therefore, an increasingly important weapon in the data transmission arsenal.

Spread spectrum

Having spent some time looking at ways of cramming more information into a given bandwidth, let's now take a look at a technique which appears to do just the opposite - spread spectrum.

First of all, modulate a carrier with the data in one of the ways already described. Now, phase modulate the resulting signal at a much higher baud rate using a repeating pseudo-random binary sequence. The end result is a high bandwidth signal occupying much more space than the original signal. This is called the direct sequence method of spread spectrum, and must seem a strange approach to the unfamiliar. Why deliberately increase the bandwidth having gone to so much trouble to keep it down? Before justifying the use of spread spectrum, let's briefly describe another common approach, frequency hopping.

In frequency hopping, the carrier frequency is shifted at a high frequency in a pseudo-random sequence. Once again, the result is a signal which has an artificially high bandwidth.

The original driving force behind spread spectrum techniques was military. Spread spectrum signals are hard to jam and also hard for unauthorised parties to intercept. Unless a receiving station has the binary sequence used to spread the signal, the signal can't be recovered, and unless you have a high power, high bandwidth transmitter, the same binary sequence would be needed to jam a spread spectrum signal.

Today, however, there are many commercial applications of spread spectrum - wireless LANs, digital cellular networks, GPS for example. Spread spectrums are often described as "noise like" and this gives them some unique properties. Since spread spectrums have a high bandwidth, so long as the transmitter power remains the same, the signal has a much lower power density. In other words, there is a comparatively small amount of power on any one frequency. As a result, although a spread spectrum signal will contribute slightly to the background noise received by a narrow band receiver, this, like atmospheric noise, will rarely be disastrous. Interestingly, the converse also holds true - a spread spectrum receiver won't be unduly affected by a narrow band signal within its passband. What this means, of course, is that spread spectrum and conventional narrow band signals can co-exist on the same frequencies.

Furthermore, multiple spread spectrum signals can operate on the same frequencies, so long as the codes used to spread the signal have been chosen such that each signal has a low correlation to the others. All this is particularly important to unlicensed operation such as wireless LANs, for example. Generally, the regulatory authorities will only permit unlicensed use of the radio spectrum where non-interference with other users can be guaranteed.

RDS

Let's turn our attention for a moment back to the benefits of data communication by radio to the man in the street. Data by radio first offered consumer benefits in the early 90s in the form of Radio Data Service (RDS). RDS can be thought of as the radio equivalent of Teletext on TV. Both allow a small amount of data to be transmitted alongside a signal which is predominantly analogue. If your car radio is comparatively modern, then you probably use RDS, even though you might not be aware of its official name nor, for that matter how it works.

RDS involves the transmission of data at 1185.5bps by phase modulation of a 57kHz sub-carrier on the normal FM signal. This data includes a code which identifies the station, the type of program being transmitted (such as sport, news, classical music etc.), the time and date, and even information such as the title of a track, the phone number to call for additional information and so on.

What this means to the user - depending on the facilities the radio manufacturer has built in - is that the name of the station will be displayed on the radio, the radio will re-tune to another signal carrying the same station if you drive out of

A Grundig DAB screen display showing a map transmitted map range, the radio will automatically switch to any local station carrying a traffic report or that accurate time and date can be shown. And although it wouldn't make sense for a car radio, on home tuners all the additional textual information can be displayed.

DAB

We introduced this article by mentioning the launch of DAB in the UK. Now's the time to see what it will offer and how it works. First, let's run through the features and benefits.

A good place to start is with the supplementary data that will travel with DAB. This builds on the foundations laid by RDS but goes much further. RDS has various ID codes which the receiver can act on, and short text messages which can be displayed. With DAB, the sky's the limit. The BBC have already demonstrated multimedia content by DAB, and there is talk of distributing HTML pages, maps for navigation purposes and even still pictures by radio. Exactly what each broadcaster supplies remains to be seen, but the potential is there.

But this is icing on the cake. The BBC point out that despite all the talk of multimedia, DAB is not a rival to television, and that the primary focus is quality sound broadcasting. High quality sound is being promoted as one of the major benefit of DAB.

This improved quality takes two forms. First of all, unlike FM radio with its 15kHz maximum audio frequency, digital radio will offer what it calls CD quality, that is, audio up to 20kHz. Secondly, in common with all robust digital transmission schemes, the signal will be relatively immune to interference and fading caused by reflections off buildings. There is a limit to the immunity, but DAB will stand up for much longer than analogue radio.

The other main benefit of DAB is extended programme choice. The BBC, for example, are planning to supplement the existing national radio stations - all five of them - with BBC 5 Live Sports Plus, BBC World Service (currently only available on short wave) and BBC Parliament. What other services arrive will depend on the availability and take-up of DAB receivers, but there is also talk of BBC Now, BBC 5 Live News Plus, and BBC Music Plus. The commercial broadcasters have also been guaranteed frequency space, so we can expect to see more choice here too.

One benefit particularly important for car radios is that it will no longer be necessary to re-tune as you drive around the company. A single frequency will carry a given radio station wherever you might be.

How does DAB make all this possible? One of the main technical benefits of digitising an audio signal and transmitting it as binary samples is that it is far more bandwidth efficient. This is not always true - with uncompressed data, an audio signal sampled at an acceptable frequency and word length will need a much greater bandwidth than the original analogue signal. But the digital signal gains over the analogue because there is plenty of scope for data compression. Once the signal has been compressed, it needs much less bandwidth than an analogue signal and multiple radio stations can be time-division multiplexed into a single radio channel no wider than those currently used for FM broadcasting. As with digital TV, a number of these so-called multiplexes are being licensed, one for BBC national services, one for commercial national radio, four for BBC and commercial local radio, and one is still to be allocated. So the increased bandwidth efficiency is responsible both for the increased programme choice and the improved audio quality.

A Panasonic RDS tuner showing a simple digital text display

With analogue broadcasting, it would have been necessary to use yet more of the crowded bands in order to move to higher fidelity sound. With data compression, it's proved possible to increase the audio frequency response while reducing the bandwidth.

The small catch is that this has only been possible at the expense of a lossy compression scheme (that is, one that doesn't allow the exact binary values to be recovered) called MUSICAM. The aim of this form of compression is to discard information that the human ear won't notice is missing but, as always, there is debate among hifi purists as to whether the compression truly is transparent.

The other advantages of DAB - specifically its relative immunity to interference and fading and the fact that re-tuning is not necessary - all relate to the modulation method employed. Like digital TV, the modulation method is COFDM - Coded Orthoganal Frequency Division Multiplexing. Here, a large number of separate carriers are used, with the signal multiplexed between them in a pseudo-random sequence. The modulation scheme on each of these carriers will be any of the common ones such as 64-QAM. This has similarities to spread spectrum and some advantages, such as immunity to interference from conventional narrow band signals also apply. It also permits multiple transmitters to carry the same program on a single frequency without constructive and destructive interference causing problems as it would with an FM or AM signal. This means that it's no longer necessary to allocate a number of channels to a single radio station.

Hands on

As the year goes on, it's likely that we will be bombarded with advertisements tempting you to join the DAB revolution. Already a number of manufacturers have released products. Initially, the main offerings will be car radios. Later, home tuners, some of which will be able to take advantage of the multi-media content, will appear. These mass market products, but the most exciting DAB development for the more technically minded will be DAB expansion cards for the PC. And here, of course, multi-media will be the major selling point.

If you find the idea of data transmission by radio a fascinating one, you can do far more than play around with consumer products. Throughout the short-wave bands, hundreds of Morse, RTTY, SIMTOR, AMTOR, Packet and other types of data transmissions can be found, originating both from commercial radios and radio amateurs. To transmit data, you'll need an amateur radio licence, but to receive these transmissions, all you need is a communications receiver, an interface unit and a PC with the appropriate software. You'll find many suppliers of this type of equipment advertising in the amateur radio magazines.

Getting MORE out of PICs

Part 5

Robin Abbott

The second of two parts on using the I2C bus: the eeprom programmer.

Last month we looked at some routines to drive the I2C bus. This month we'll use the routines to make an 8-pin I2C bus eeprom programmer and reader. The project demonstrates the techniques which can be used to make a complete and flexible utility for working with these devices.

Microchip (and others) manufacture I2C eeproms in a range of sizes. In this article we shall construct a programmer for the 24LC65 (and compatible devices), which is an 8K x 8 memory suitable for data logging applications. For simple storage of configuration variables, smaller devices are probably more suitable, however all the devices are driven in similar fashion.

Driving the 24LC65

Figure 1 shows the pinout of the eeprom. The SCL and SDA pins are for the I2C bus, the address pins A0, A1, and A2 are connected to ground or Vdd. When the device is addressed these bits are used as part of the I2C address selector to choose the particular device. By using these pins it is possible to use up to eight devices on a single I2C bus, allowing up to 64K of eeprom to be addressed on a two-wire bus.

Thinking back to last month's article, the first byte transferred on the I2C bus is the control byte which selects the specific chip to be addressed. **Figure 2** shows the control byte for the 24LC65. Note that the bottom three bits of the address within the control byte for the 24LC65 are the address bits which match the pins on the device.

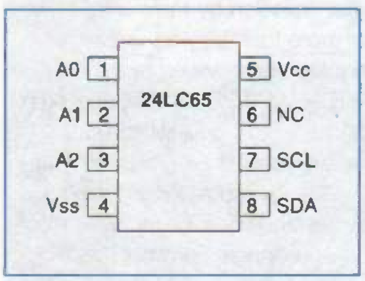


Figure 1: 24LC65 8K x 8 eeprom

The 24LC65 has a number of modes to access the memory array. We will not go into all these modes in this article, but will simply consider the Byte Write, Random Read, and Current Address (sequential) Read modes.

Byte write.

This mode allows a single byte of data to be written to any address in the memory. The control byte is written first with the R/W bit set to 0 to indicate a write, followed by the address which is transmitted as two byte transfers to the eeprom, the most significant byte of the address is written first, followed by the least significant byte. As in all other transfers the data is written Most Significant Bit first. The final byte written is the data byte. At the end of each of the four bytes written the 24LC65 generates an acknowledge bit. After all four bytes have been written the master device generates a stop state and the 24LC65 initiates an internal write cycle. The time taken to write the data is guaranteed not to exceed 5ms, so the master may either wait for this time to allow the data write to complete, or it may continuously poll the device sending control bytes until the 24LC65 acknowledges, which indicates the end of the write cycle. The Byte write cycle is shown in **figure 3**.

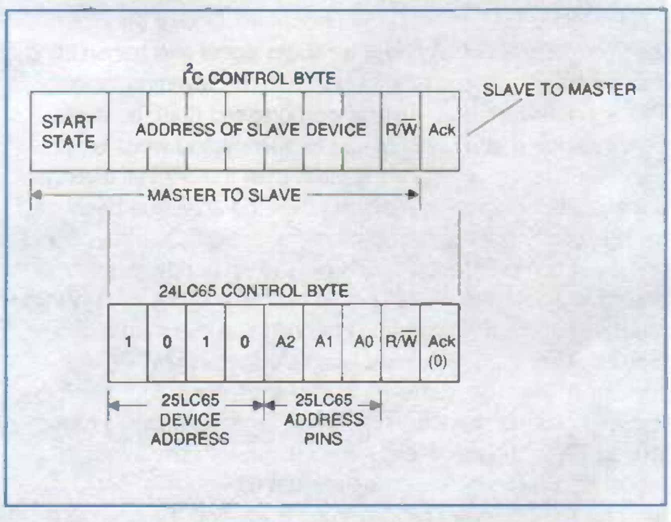


Figure 2: the control byte for the 24LC65

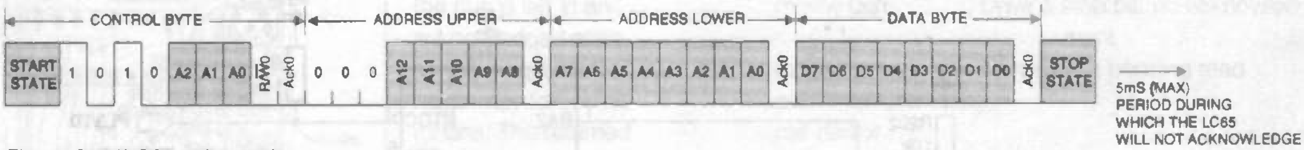


Figure 3: 24LC65 write cycle

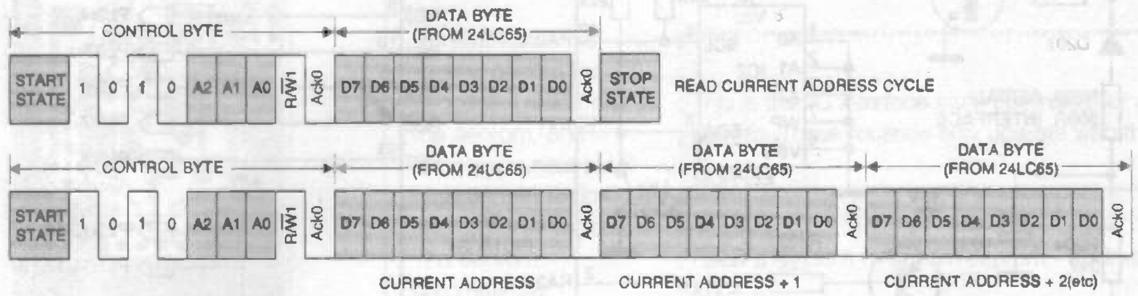


Figure 4: read current address cycle

Read current address - sequential reads.

To read a byte from the eeprom, the same control byte is used but with the R/W bit set to 1. Following the acknowledge bit from the 24LC65, the master sends an additional eight clocks to the 24LC65, and the 24LC65 then clocks out the requested byte. Following the last bit sent by the 24LC65, the master may either send an acknowledge bit, or will not acknowledge. If the master acknowledges, then the 24LC65 increments the current address, and the master may then send a further eight clocks to read the next byte, this allows the entire contents of the memory to be read rapidly. The read cycle is illustrated in **figure 4**.

Random read

A random read is performed by setting the current address as if a write cycle were to be undertaken. However following the lower byte of the address another start condition is generated by the master, this is followed by a control byte to read the current address, and then the contents of the supplied address may be read. **Figure 5** shows the random read cycle. Note that the random read cycle takes 5-byte transfers on the I2C bus, and using the routines shown last month this can be as much as 500us. Therefore, wherever possible the random read should only be used when absolutely necessary; otherwise, use sequential reads which take only one byte transfer per byte read.

Other modes.

The other write mode which is also very useful is the page write mode which allows up to 64 bytes to be written simultaneously, and so can increase write speed by up to 64 times. In similar fashion to the sequential read the master continues to send up to 64 data bytes before the stop state, and when the stop is received all 64 data bytes are written to the memory simultaneously. This mode is not shown further in this article as the code required to drive it would occupy too much space.

It is possible to program internal security bits to prevent further writes to the eeprom array.

The 24LC65 device has two eeprom areas internally, one has the capability for considerably more write operations than the other. This is known as the high endurance memory. There is also a mode available to re-map the high endurance memory internally.

Eeprom Programmer.

The eeprom programmer is based on the circuit shown in the first part of this series of articles. The circuit is shown again in **figure 6**, and the full construction details may be found in the first part. If you intend simply to make the programmer, PL3 can be omitted, and Veroboard-style construction may be used. Note that the circuit includes a space for the 24LC65 in IC2, the address bits in this circuit are all set to 0, and this socket is also pin compatible with other eeprom devices such as the 24LC16.

The programmer uses a simple serial protocol to communicate to the PC. This is illustrated in figure 7. There are four commands sent from the PC to the programmer. The first reads from a random address and leaves the programmer in a state to read the next byte sequentially; the second command reads the next byte sequentially; the third command writes a byte to a supplied address. Finally therefore is a simple command which forces the programmer to return a 'K' character, this confirms that the programmer is present.

PIC code

The code will use the serial routines from the first article, and the I2C routines from last month's article. As usual, the routines will be available on the net, or from the author. The serial and I2C routines should be combined and assembled successfully

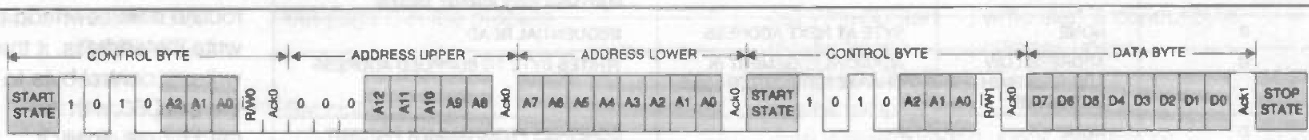


Figure 5: 24LC65 random read cycle

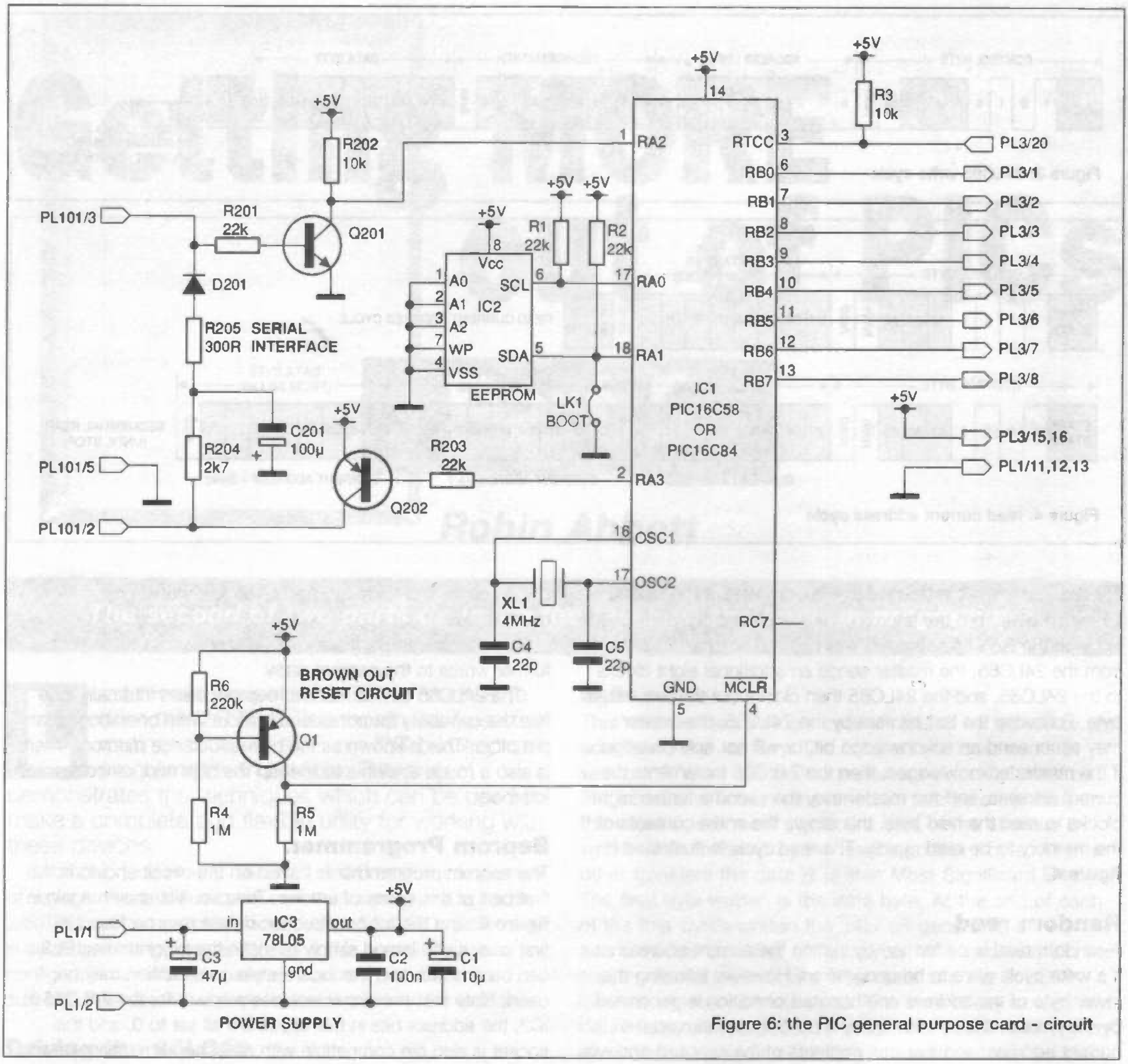


Figure 6: the PIC general purpose card - circuit

before adding any of this month's routines. This is straightforward: use the I2C routines from last month as a master, and change the serial initialisation routine from part 1 into a subroutine which should be called as part of the I2C initialisation. The start of the program should now look like **listing 1**. Also, add three new variables - AddrLo, AddrHi, and DataVal. These will hold information received on the serial port.

Now there are four routines which interface to the serial eeprom, shown in **listing 2**. Of these only three routines are called by applications. These routines call the function in last month's article which writes or reads a byte to the I2C bus. This function is called with two entry points - WriteIICStart and WriteIICNoStart. See last month's article for full details on this function. The four interface routines are described below:

eewrtadd. This routine writes the address part of a random read or write request. When called, the address is held in FSR. A start bit state is written to the bus, the control byte is written, and then the upper and lower address bytes, note that there is no stop state written after the control and address bytes to allow for the following read or write information.

eereadrand. This routine reads a single byte from a supplied address. The address is stored in memory with the lower byte of the address held first, the value in FSR points to the memory file where the address is held. The routine calls eewrtadd to write the address, it then writes a control byte to the 24LC65 with the read bit set, finally it reads the byte from the

COMMAND BYTE	PARAMETERS	RETURNS	NOTES
A	ADDRESS LOW ADDRESS HIGH	BYTE AT SUPPLIED ADDRESS	READS FROM ADDRESS SUPPLIED, ACKNOWLEDGES INTERNALLY TO ALLOW FURTHER SEQUENTIAL READS
B	NONE	BYTE AT NEXT ADDRESS	SEQUENTIAL READ
C	ADDRESS LOW ADDRESS HIGH DATA BYTE	ACKNOWLEDGEMENT (K CHARACTERS) AFTER 10mS	WRITES BYTE TO SUPPLIED ADDRESS
D	NONE	K	CONFIRMS PROGRAMMER PRESENT

Figure 7: the serial protocol used by the programmer

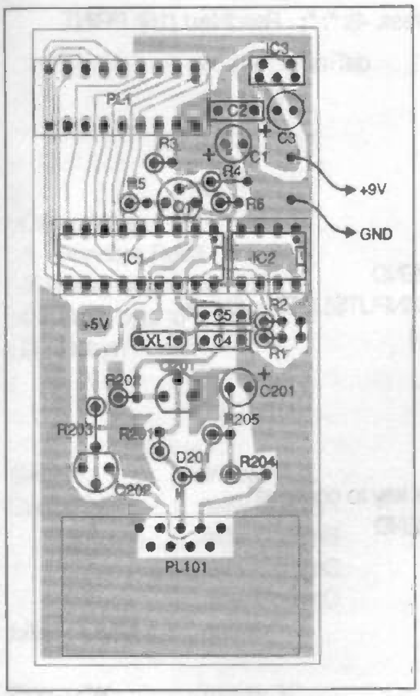


Figure 8: the component layout of the PIC card

eeprom. Note that the bus is left in an acknowledged state, so that sequential reads may follow this routine. The returned value is held in both temp4, and in the W register.

eereadnext. This routine performs a sequential read from the eeprom, and returns the next byte read in both temp4, and in the W register. The eeprom automatically increments the address, so this routine is useful for rapid repeated reads to the eeprom.

eewrite. This routine writes a byte to any address in eeprom. The address is stored in memory with the lower byte of the address held first, the value in FSR points to the memory file where the address is held. The routine calls eewrtadd to write the address. It then writes a control byte to the 24LC65 with the write bit set, and finally it writes the byte which is held in memory writeval to the eeprom. Note that there is no attempt to verify the acknowledge bit after the write, the calling routine should wait for 10ms (for safety), or may poll the acknowledge bit.

Finally, **listing 4** shows the main application loop which waits for incoming serial bytes, decodes them, and then runs the appropriate routine.

Listing 1: Eeprom Programmer code initialisation

```
;
; Start by org'ing code
;
     org 0              ; Restart vector
     goto start
;
; Interrupt service routine.
;
       org 4

;*****************************************************
;
; This is the start up code which sets up the device
;
;*****************************************************

start    ROMPAGE0       ; Set page 0 in the process
         RAMPAGE0
         movlw 0ffh
         movwf picio    ; Set clock bit high
         RAMPAGE1
         bcf picio,scl  ; Drive clock bit
         RAMPAGE0
         movlw 0ah      ; Drive a stop bit, no acknowledg
                          ment
         movwf temp3    ; Terminate a pending read
         call WriteIICNoStart
         call SerInit
```

Listing 2:Eeprom interface routines

```
;*****************************************************
;
; This is the IIC interface stuff, optimised for eeprom
; access. These routines only operate with the 24LC65
;
;*****************************************************
;

; Read a random byte from eeprom - address in FSR return in
temp4 & w

eereadrand call eewrtadd ; set write address
         movlw 4
         movwf temp3         ; read, ack & start bit
         movlw 0A1h          ; Address of 24LC65
         bsf picio,scl       ; drive clock high for start
         call WriteIICStart  ; Write, ack & start bit

; Read next byte from eeprom return in temp4 & w

eereadnext bsf STATUS,RP0    ; Read from data line
         bsf picio,sda       ; Data TRIS driver to read
         bcf STATUS,RP0
         movlw 0ch
         movwf temp3         ; Read, Ack, No start or stop
         call WriteIICNoStart ; read byte
retee    movfw temp4         ; Result in temp4
         return

; Write a byte to eeprom, address in FSR, byte in writeval

eewrite    call eewrtadd
         movlw 6
         movwf temp3              ; Acknowledge & stop bit
         movfw writeval
         goto WriteIICNoStart ; No start bit

; Write address part of read or write algorithm. This
; routine leaves the address written in temp (L) and temp1 (H)

eewrtadd   movfw 0
         movwf temp          ; save the lower address
         incf FSR            ; Now the upper byte
         movfw 0
         movwf temp1         ; Upper address in temp1
         call quikstop       ; Set bus to stop state
         movlw 4
         movwf temp3         ; ack & start bit
         movlw 0A0h          ; control byte
         call WriteIICStart  ; write start & control byte
         movfw temp1         ; address upper
         call WriteIICNoStart
         movfw temp
         goto WriteIICNoStart ; ack, no start bit
```

PC application program

To use the programmer from the PC we shall examine a very simple Qbasic program which allows the eeprom to be read or a file to be programmed to it. Qbasic is supplied as part of DOS.

Owing to lack of space for listings the program is minimal and can be much improved, it is presented here with just the essential features for reading and writing eeproms. **Listing 3** shows the Basic program, press key 1 to read the first 256 bytes of the eeprom, press 2 to read the next 256 bytes (sequentially), and press 3 to write a file. Note that the file is presented as a series of bytes in ascii decimal, one byte per line, the first byte is written to address 0, the second byte to address 1 etc. There is little commenting in the file, or within this article, the program is quite straightforward and Qbasic has comprehensive on-line help.

Listing 3 - BASIC programmer application

```
DECLARE SUB WriteFile ()
DECLARE FUNCTION NeatHex$ (xl, places!)
DECLARE SUB waitkey ()
DECLARE SUB Read256 ()
DECLARE SUB ReadFirst ()
DECLARE SUB ReadNext (Num!)
OPEN "COM1:19200,N,8,1,RS,DS,BIN" FOR RANDOM AS #1

DIM SHARED Address

WHILE 1
  CLS
  PRINT "EEPROM Programmer": PRINT
  PRINT "1-Read 1st 256 bytes of EEPROM"
  PRINT "2-Read sequentially - next 256 bytes of EEPROM"
  PRINT "3-Write file to EEPROM"

  a$ = "": WHILE a$ = "": a$ = INKEY$: WEND
  IF (a$ = "1") THEN ReadFirst
  IF (a$ = "2") THEN Read256
  IF (a$ = "3") THEN WriteFile
  IF (ASC(a$) = 27) THEN STOP
WEND

FUNCTION NeatHex$ (x, places)
  a$ = HEX$(x)
  WHILE LEN(a$) < places: a$ = "0" + a$: WEND
  PRINT a$; " ";
END FUNCTION

SUB Read256
  CLS
  FOR i = 1 TO 16
    PRINT (NeatHex$(Address, 4)); ": "; : ReadNext (16): PRINT
  NEXT
  waitkey
END SUB

SUB ReadFirst
  Address = 1
  PRINT #1, "A"; CHR$(0); CHR$(0);
  WHILE LOC(1) < 1: WEND
  CLS
  PRINT "0000 : "; NeatHex$(ASC(INPUT$(LOC(1), #1)), 2);
  ReadNext (15)
  PRINT
  FOR j = 1 TO 15
    PRINT NeatHex$(Address, 4); ": "; : ReadNext (16): PRINT
  NEXT
  waitkey
END SUB

SUB ReadNext (Num)
  FOR i = 1 TO Num
    PRINT #1, "B";
    WHILE LOC(1) < 1: WEND
    PRINT NeatHex$(ASC(INPUT$(LOC(1), #1)), 2);
    Address = Address + 1
  NEXT
END SUB

SUB waitkey
  PRINT : PRINT "Press a key to continue"
  WHILE INKEY$ = "": WEND
END SUB

SUB WriteFile
  Address = 0
  CLS
  PRINT "Enter filename >"; : INPUT f$
  OPEN f$ FOR INPUT AS #2
  DO WHILE NOT EOF(2)
    LINE INPUT #2, a$
    IF a$ <> "" THEN
      IF (ASC(a$) >= 48) AND (ASC(a$) <= 57) THEN
      x = VAL(a$)
      PRINT #1, "C"; CHR$(Address MOD 256); CHR$(INT(Address
/ 256)); CHR$(x);
      WHILE LOC(1) < 1: WEND
      IF INPUT$(LOC(1), #1) <> "K" THEN PRINT "Error on
Receive"
      PRINT "Programmed "; NeatHex$(x, 2); " to ";
NeatHex$(Address, 4)
      Address = Address + 1
     END IF
    END IF
  LOOP
  CLOSE #2
  waitkey
END SUB
```

Listing 4: Application main routine

```
Application call   Receive   ; Wait for a command

ExecCmd            movwf temp
                   movwf temp1
                   movlw LASTCOMM+1
                   subwf temp,w
                   skpnc
                   goto Application   ; Out of range - back to
main loop
                   movlw 'A'
                   subwf temp,f
                   btfsc temp,7
                   goto Application   ; Out of range - back to
main loop

                   movlw CommTab>>8 ; Find command routine
                   movwf PCLATH
                   movfw temp
```

```
        addlw CommTab
        call GetVal
        movwf PCL

;
; Commands
; A - Random Read
; B - Read Sequential
; C - Write byte to address
; D - Return K
;
        org 0x100

GetVal  movwf PCL
CommTab retlw CommA
        retlw CommB
        retlw CommC
        retlw CommD
LASTCOMM equ 'D'

CommOK  movlw 'K'
        call TxW
        return
;
; Do a random read
;
CommA   call Receive
        movwf AddrLo
        call Receive
        movwf AddrHI
        movlw AddrLo
        movwf FSR
        call eereadrand
        call TxW
        goto Application
;
; Do a sequential read
;
CommB   call eereadnext
        call TxW
        goto Application
;
; Write to eeprom
;
CommC   call Receive
        movwf AddrLo     ; Address
        call Receive
        movwf AddrHi     ; Address
        call Receive
        movwf DataVal    ; Data
        movwf writeval   ; Data to be written
        movlw AddrLo
        movwf FSR
        call eewrite
        DELAY .10000
        movlw 'K'
        call TxW
        goto Application
;
; Simply return a K character
;
CommD   call CommOK
        goto Application
```

PARTS LIST for the PIC General Purpose Card

Resistors

R1, R2	22k
R3	10k
R4, R5	1M
R6	220k
R201, R203	22k
R202,	10k
R204	2k7
R205	300R

Capacitors

C1	10u
C2	100n
C3	47u
C4, C5	22p
C201	100u

Semiconductors

IC1	PIC 16C58 or 16C84
IC2	eeprom
IC3	78L05
Q201	BC548
Q1, Q202	BC559
D201	1N4148

Others

XL1	4MHz
PL1	Veropins
PL101	9-pin PCB mounted D connector
PL3	16-pin dil socket

On using I2C eeproms

Note that the circuit application has a brown out reset circuit. This was originally inserted because the board was intended for use as the basis of the ETI PIC Basic series. In this application the eeprom is nearly always being read, and glitchey I/O lines during power down caused corruption of the eeprom. It is recommended that such a circuit should always be used.

Even with a brown-out circuit it is possible for corruption and failure to occur if the power supply disappears during a write operation. In important applications it is recommended that eeprom data should be protected with a checksum, or by writing data three times - a vote being taken to decide on the correct data.

There are a number of other eeprom devices with I2C interfaces which may be used, they are similar, and can be driven with little change to the application program.

Next Month

Next month we shall take a look at various techniques for mathematical operations and for handling data.

Obtaining code

At the end of this series a disk with all the examples shown in the series will be available, the programs may also be downloaded from the web: www.aaelectron.co.uk/eti/

I am happy to answer questions on the series by E mail. Write to me robin.abbott@dial.pipex.com.

DIY PCs

It is (theoretically) possible for a well planned computer upgrade to run smoothly - though it cannot be relied upon. One without all the facts can be a real nuisance.

Andrew Armstrong

In order to make an upgrade to your PC a practical proposition, you need to decide on the purpose of the upgrade, both for the immediate and the more distant future. For example: do you see the upgrade a means to get another year or two of use out of otherwise obsolete hardware? Or do you want to allow, as afar as it possible, for more upgrades in the future?

In the first case, it is only rational to spend very modest sums of money. If the performance you want can only be achieved with quite a bit of expense, and yet the computer is still in a "dead end" situation, where the next upgrade will mean throwing most of it away, then it might be better to spend more now in order to minimise the likely cost over a two-year period. Of course, this is easier said than done, because we are still only guessing what the standards might be in a couple of years time.

Two years ago, I would have expected that CD-RW (ReWriteable CD) would have been all but obsolete, with dvd (digital versatile disc, formerly known as digital video disc) taking over from CD technology. But reality has not kept pace with my preconceptions, and the use of CD-RW is still increasing. Problems over setting standards in dvd have been part of the reason. Users are realising that several competing variations on a standard can be bad news for the people who are trying to buy something to last. Write Once CD media can cost as little as £70.00 per hundred discs in some places at time of writing.

So, while it seems reasonable to fit a new CD-RW drive right now, if you can find a dvd drive which also reads the CD-RW format, that may be a viable choice. However, you may want to stick to a drive that can write to CD-RW media, as these can also be read by ordinary CD-ROM drives. In that way, it is possible to back up 650MB of files and use them on any other computer which runs a CD-ROM drive and the appropriate software to manipulate the files. This could be helpful for teleworkers who occasionally need to spend a day working in the office.

When dvd is more widely fitted to new machines, I suspect it will be the preferred format, but it is no use having your work on a dvd if the only readers available on site are for CD-ROM.

It is also possible to use CD-RW as a backup, using a utility which formats the disc to around 580MB and treats it as a high speed, high capacity floppy. This format cannot be read without the right utility, so it is mainly useful for keeping running backups.

You do keep offboard backups, don't you? It is vital to back up anything which you can't afford to lose before making any changes to a PC, particularly large changes like replacing the processor or the motherboard.

Socket 7 or Slot 1?

From one point of view, an upgrade to a slot 1 motherboard is not so much an upgrade as building a new computer. This is because most slot 1 motherboards are not the standard AT style, but the new standard ATX style. (Robert discussed this in part one of this series.) The main differences are the mounting, which is stronger, using screws instead of plastic clips, and the connectors from the power supply. The different connectors prevent the wrong supply voltage being fed to the motherboard.

For this reason, a new (and more expensive) case is needed, as well as the motherboard and processor. Oh yes, and the old memory may no longer be of any use, because many of the new boards use dimms (dual inline memory modules) instead of 72 pin simms. Some can support both, and some use simms only, but you may not find a motherboard which does this and also supports whatever other functions you need.

There are a few slot 1 motherboards available for the AT case, probably because of demand from upgraders, but bear several factors in mind if you consider this approach. First of all, the ATX power supply is specified to a high level of efficiency, and supplies the 3.3V needed by the Pentium II, while AT style boards must generate this voltage on board. The bus speeds available from this type of card are not the right specification to support the fastest Pentium II processors correctly, whereas some of the ATX motherboards will support the 100MHz bus speed.

It is also worth noticing that faster socket 7 processors are available, so that a socket 7 motherboard and, for example, a 266MHz processor from one of Intel's competitors might be better value than an AT style slot 1 motherboard.

The choice of a slot 1 motherboard can allow further upgrades in the future without the need to replace the motherboard. In particular, if you get a board with the BX chipset (I believe this is only available in the ATX style), which can run with a 100MHz bus speed, it should be able to support processors up to 400 or perhaps 450MHz when these become affordable. Quite likely the 450MHz processor will be perceived as "baby's first computer" in a couple of years.

In any case, you can still use the rest of the computer. If, for example, you upgraded the hard disc only last year, that is likely to be large enough for your purposes for some time to come. Equally, graphics and sound cards, CD-ROM and other drives can all work with the upgraded system.

A tale of several upgrades

A recent upgrade decision to purchase a new motherboard and case, and to use a 266MHz Pentium II, was based on the following reasoning:

The following upgrade would almost certainly have to be to a slot 1 motherboard, partly because Intel is likely to stop manufacturing socket 7 processors, and past experience has shown that much of the market will fall into line with Intel in the long run. There are also performance advantages to the socket 1 approach, two of which are related to the cache (see below). In addition, the socket 7 system is unlikely to jump to a much higher performance in the future than it has now. The processor speed may increase, but the motherboard will increasingly limit the overall performance.

The final straw came when I tried to do bandpass filtering on an image to remove a regular moire pattern without degrading the resolution unnecessarily. When it had reached 13 percent after 30 minutes it became clear that the machine could not do this task in a practical manner. My current motherboard could only support a processor up to 166MHz, and it was already running a 150MHz. A new motherboard was needed, so I chose an ATX socket 1 motherboard with 100MHz bus capability.

Photo 1 shows the motherboard resting on top of its packaging. The support bracket for the processor has been fitted, but no other assembly has been done. The support bracket is retained by four screws, which are supported by two small brackets beneath the board. I found, on this sample, that the locating pegs of one of the brackets would not fit into the holes in the pcb without the application of what I deemed excessive force, so I very carefully took a little of the plating from the inside of the holes, assiduously avoiding getting any filings on the pcb. Then it fitted. The alternative solution, of locating it and tightening the screws, pulled it off true rather than pulling the mountings into place, which was highly undesirable, so there was no reasonable alternative to using a file.

Fitting the cpu cooler is fiddly. The only way that worked was to slacken off the mounting screws as far as they would go, fit the locating pegs of the heatsink into the holes in the cpu module, and then tighten the retaining screws (visible either side of the fan in **photo 2**). In this picture the cpu cooler is shown fitted to the Pentium 2 processor.

The tower case was an advance over the previous one (purchased some years ago) in several ways. One advantage was that the motherboard mounting plate could be removed from the case completely. Another was that the metalwork had sprung contact fingers all around to keep interference inside the case. It has made radio reception in the vicinity of my computer much easier, so it does make a difference.

Photo 3 shows the motherboard mounted on the pullout panel, while **Photo 4** shows detail of the contact fingers connecting to the USB port, part of the general design for EMC. Most modern cases are likely to have this sort of design, but people upgrading older machines may wish to consider whether a new case may be justified for EMC reasons. Certainly, those interested in amateur radio may find it worthwhile.

The rest of the upgrade went easily, until the time came to make the network card work at the same time as the sound card. Windows 98, left to itself, puts both items on to IRQ5, according to the device manager. (To find the device manager, choose settings from the start menu, then click on control panel. When the control panel opens double click on System, and then click the device manager tab.)

The device manager assured me that one of the valid settings for the sound card was IRQ9, but it didn't work. At least the network card did work at that point. Eventually, documentation downloaded from the manufacturer's website told me that the card would not work on IRQ9, but would work on IRQ11, which it happily shares with another device. I had to set up the card manually and ignore Windows' dire warnings that it could not set up the card automatically to assure correct functioning.

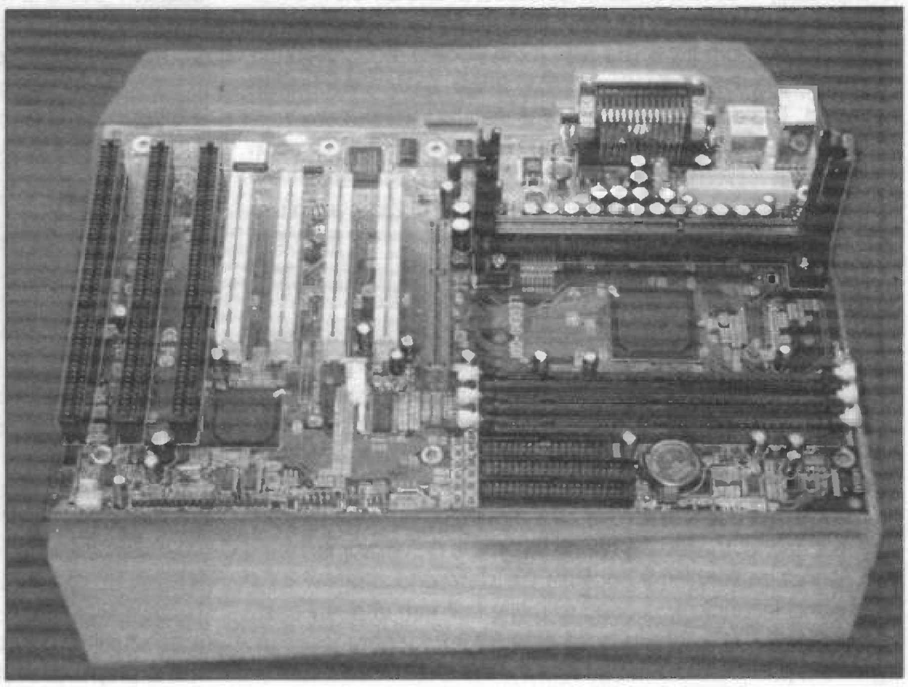
The upgraded machine is fast and works well. The use of an AGP graphics card has speeded up the display to some extent, and just as importantly freed a PCI expansion slot for future additions. All I need now is a T1 line to connect to the internet, a CD writer, and a fortune to pay for it.

While all this was in progress, I took a break to go to the Woburn Amateur Radio Rally. There I bought 64M of 10ns dimm for £45, cheaper than I have seen it elsewhere. I was told that memory prices are set to rise again. If this turns out to be true, then it might be a good idea not to wait too long before carrying out a planned memory upgrade.

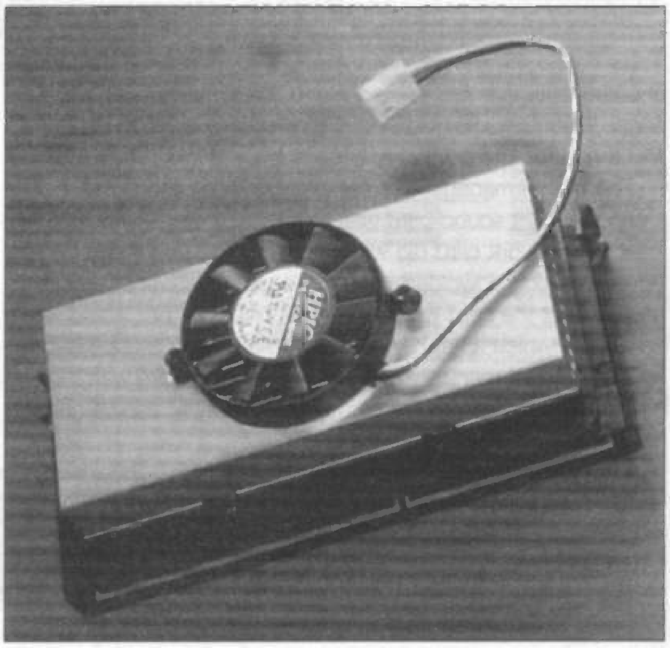
Another upgrade, carried out recently for a friend, was intended simply to be the addition of a larger hard disc and upgrade to Windows 98, but it turned into a nightmare.

Before I took the case apart, I had no doubts that the machine would be able to use the planned 4.3GB hard disc. It was already using a 1GB disc in LBA mode (necessary to address more than about 500MB directly). Early motherboards, unable to use LBA mode, would require a disc manager on the disc to permit it to be read. The motherboard would interface with the disc as if it was approximately 500MB, while the disc manager, loaded on the first part of the disc, would control access to the rest of the space.

Once that barrier is past, there is not another one between 1GB and well above 4.3GB.



The Slot 1 motherboard



The CPU cooler mouned on the Pentium II CPU module

However, the motherboard auto-recognised the disc as 82MB, and stubbornly prevented me from entering the parameters manually. I used another machine to search the internet for a bios upgrade, in the hope that would make it work, but to no avail. Close examination of the motherboard showed me why: the bios was not upgradeable by means of a flash memory writer. It was on UV erasable prom, and the chances of finding a more up to date eprom available looked slim. Perhaps the motherboard could not cope with an Ultra DMA drive. It should ignore the Ultra DMA capability and treat the drive as LBA, but it may have been too old for this capability to be present in the bios software. There was no straightforward way of telling in advance, and this can be one of the problems.

As an interim solution, we tried installing Windows 98 on the existing hard disc, in the hope of gaining an extra 200MB by use of FAT32. Unfortunately the motherboard would not permit Windows 98 to boot, except into safe mode.

Eventually we fitted a new motherboard, and a new processor, going from a 100MHz '586 made by Cyrix to a 200MHz '686 from IBM. The new motherboard recognised the disk, and runs the applications visibly faster, as we hoped and expected. The operating system was installed without any objections from the motherboard, and the owner has just sent me an email message saying that all his applications are reinstalled and running correctly. The data, of course, is on the old hard disc, now configured as a slave drive.

What is cache for?

Processor speeds increase year by year, but actual computer speeds do not increase pro-rata. The reason is, of course, that other parts of the machine do not speed up by the same proportion. The processor sits idle for part of the time, and its speed is not an advantage to the user.

One way to minimise the time when the processor is not doing anything useful is to use cache memory. A small and very fast cache, the level 1 cache, is on the processor itself. This cannot be very large because the semiconductor processing technology needed to make fast ram at a low cost and on a small chip area is quite different from that required to make fast processors. For this reason, the level 1 cache is supplemented by a much larger level 2 cache. This memory is separate from the main processor, and the faster it communicates with the processor, the faster the system as a whole can work. In socket 7 systems the level 2 cache is on the motherboard.

Disc information is also cached in main memory, which really represents a third level of cache. A disc cache keeps recently used hard disc data in the system memory, and when the processor requests data the cache manager provides it from this source if it is available. The hard disc, which is much slower than memory, is only accessed if the data is not in main memory.

When the processor needs information from main memory, it first checks to see if it is in level 1 or level 2 cache before waiting for data from main memory. Therefore sufficient cache memory is essential for good performance with faster processors.

Advantages of the Pentium II type of processor include the provision of Level 2 cache right next to the processor, (on the plug-in module) so that it can be operated faster than if it were separated by a length of track on a pcb.

There is another cache-related advantage: Socket 7 motherboards handle the memory caching, and in many cases the cache can only address up to 64MB of memory. (Cache actually consists of cache ram and tag ram, which stores the location of the data in the cache. Many socket 7 boards only have enough tag ram to store 64MB worth of addresses.) Adding memory above the 64MB limit can actually be slightly detrimental to some applications, because of the extra delay imposed by the lack of caching. However, later socket 7 boards are more likely to have enough tag ram to cache up to 0.5GB properly, and in any case the larger memory would prove an advantage when working on large files, for example when editing bitmap images of tens of megabytes using a photograph editing program.

The issue is a complex one, because applications are not necessarily addressed at the physical memory location at which they reside, but may be mapped over the 4GB of address space available. The physical memory is remapped transparently to the application, but this does make it very unclear whether a particular application will have its executable stored in a piece of physical memory which is cached or not.

What is clear is that increasing memory above 64MB on a socket 7 board is moving into the region of diminishing returns. With slot 1 (and Pentium pro) motherboards, the cache addressing is handled on the processor module, and this 64MB limitation does not apply.

Conclusion: If you expect to want to make use of over 64MB of memory in the next couple of years, an older socket 7 motherboard may not be ideal.

Bios upgrades

When the computer boots, the bios program starts. This has to do tasks like reading the hard disk, and must therefore be able to use the protocol required by modern hard discs. @B:Sometimes the bios may be unsuitable for the required function, or it may have a bug. In such cases, if the bios is on flash memory rather than on eprom, then it may be possible to upgrade it to a later version written for that specific make and model of motherboard.

However, if you upgrade to the wrong bios, your computer may not boot. This will mean that you cannot easily install the correct bios, and put you in a real corner!
Nevertheless, there are occasions when upgrading the bios is a sensible thing to do. For example, the current bios may not make proper provision to boot to a PnP (Plug and Play) operating system such as Windows 98, or may not be able to

recognise some modern hard discs correctly at all.
If you think that you do need to upgrade the bios, first try Wim's bios page http://www.ping.be/bios/ (linked from the ETI website) to help you to identify the motherboard, and to help you find a source of an upgraded bios if such exists.

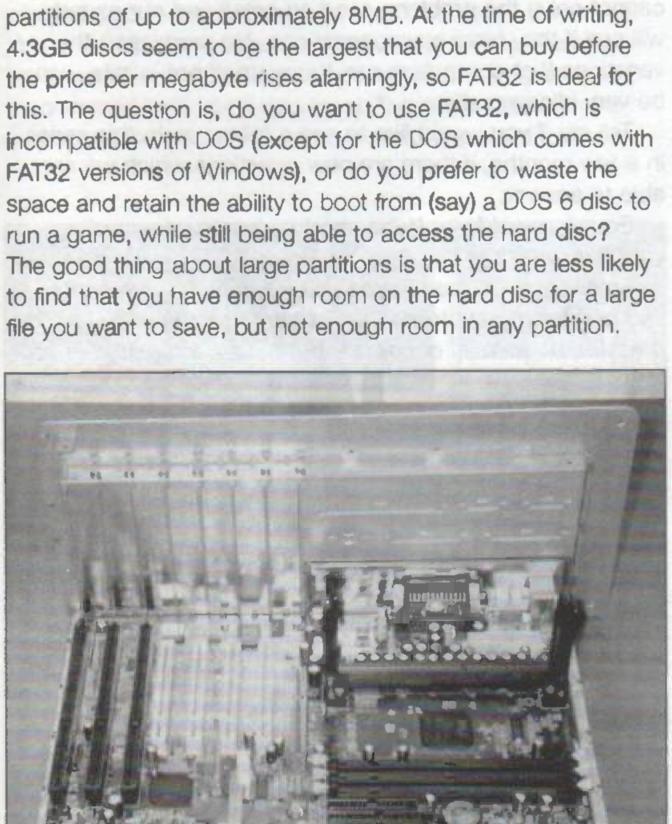
Before you actually upgrade the bios, go through the setup and write down the settings. When you have run the upgrade, you can restore any which may have changed. You may also need to auto recognise the hard discs again.

Tip: Using the AMI bios flasher, I have received the error message that the file I want to install does not exist. I have always run this program from a bootable floppy disc, with which I booted the machine to DOS mode. When I copied the data file to the hard disc, and pointed the flasher program to that, it worked correctly. This has happened twice, on the same type of motherboard, and may not affect your hardware. If you do see this error message you could try the same solution.

Partitioning revisited

How you partition your hard disc is partly a matter of personal taste, but there are constraints on the number of practical choices. If your operating system is Windows 95 upgrade version, then it will not support hard disc partitions above approximately 2.1GB. With partitions this size, you will have a cluster size of 32K, which means that a 1-byte file will still use up 32K of the disc. Temporary files, windows shortcuts and the like are all small files which exist in great profusion on the hard disc, and it is easy to end up with a nominal 1GB of data filling a 2.5GB drive.

FAT32 reduces the partition size to 4K, and can support partitions of up to approximately 8MB. At the time of writing, 4.3GB discs seem to be the largest that you can buy before the price per megabyte rises alarmingly, so FAT32 is ideal for this. The question is, do you want to use FAT32, which is incompatible with DOS (except for the DOS which comes with FAT32 versions of Windows), or do you prefer to waste the space and retain the ability to boot from (say) a DOS 6 disc to run a game, while still being able to access the hard disc? The good thing about large partitions is that you are less likely to find that you have enough room on the hard disc for a large file you want to save, but not enough room in any partition.



The motherboard mounted on the removable panel

Large graphics files can do this to you! A single partition on a large disc can be inefficient or impossible unless you use FAT32, in which case some compatibility with older DOS games is lost. One answer is to partition most of the disc as a single FAT32 partition, leaving a small partition to use with DOS games. The small partition will be FAT 16 anyway, because Windows will not use FAT32 for partitions so small that it is of no benefit.

If you choose one large partition for your hard disc, then a well designed directory structure can make it as easy to navigate as a setup with several partitions. Conversely, if you choose multiple partitions, it may be worth having a utility which can repartition discs without having to reformat and lose all the data. Partition Magic is one which I have used successfully in the past.

Copying your installation

If you are happy with the software installation you have at present, but are running out of hard disc space, then it will be easiest for you to simply copy the whole installation to a new hard disc of a larger size. Subsequently the old hard disc can be used to store large scans, sound files, or anything else which is not convenient to save on the boot drive.

There are utilities which allow you to do this, such as Partition Magic, and a related program which just copies a drive. However, if you only want a copy of the software and data, basically a booting duplicate of your boot drive on a larger hard disc, then the following procedure could be useful to you:

1) Install your new, blank hard drive as a slave. It is necessary to leave the boot drive, whose system you wish to transfer, installed as the master disc. In some cases it may be necessary to reset the configuration links to be "master disc with slave present" instead of "master disc - no slave". Most discs do not have such a setting, but if you have difficulty in making the computer recognise the hard disc, then it is worth searching for this link to see if (a) it exists and (b) therefore needs resetting correctly.
2) Format the new hard drive (using FDISK and FORMAT, for instance).
3) From a DOS window inside Windows 95, type the following command:

```
XCOPY C:\*.* D:\*.* /s/c/h/e/r/k
```

Notes: If you get a "switch not recognized" error, you have probably made a typing error. To find out what these switches do, type xcopy /? from a DOS window. The command above assumes that your new hard drive was assigned the letter D:\. Choose "yes" when asked to overwrite any files.
4) When copying is finished, turn off the computer, open it up, and reconfigure so that the new hard drive is the Primary Master drive.
5) Boot to the Win95 startup disk. Using FDISK (or other such utility), and set the Primary Partition on the new drive as Active.
6) Eject the Startup disk and reboot. If Windows95 does not boot from the hard drive, put the startup disk back in and boot to it. At the A: prompt, type:

```
SYS C:
```

This will recopy the system files to the new hard drive.
7) Reboot to the hard drive. It should boot to Windows95.

Windows 98 upgrade?

My own take on Windows is that there is more software for desktop computers to run under Windows than other operating systems, so most people need the most effective Windows setup possible. If you are running Windows 95, will Windows 98 be more useful to you?

There are several variants of Windows 95. You may or may not have support for FAT32, and for USB (the Universal Serial Bus, covered in ETI 1997 No. 7). If your copy of Windows 95 does not support FAT32, then your only route to FAT32 is to upgrade to Windows 98. There were never any upgrade versions of Windows 95 which supported FAT32 - the only copies which did were only sold with hardware. This would often mean a new computer, but a new hard disk and motherboard was normally assumed to qualify.

Some versions of Windows95 do support USB, but it is reported that Windows 98 supports it more effectively. After a long time during which USB peripherals were not available because they were not supported, they are now gradually becoming available. Digital loudspeakers are among the first, which could be good because sound cards have arguably wasted more time than any other add-on, owing to widespread compatibility problems.

If you do upgrade to Windows98, the quickest way to do it may be to run setup to install it over your present system. This can work well, but if you have run Windows 95 for a long time, perhaps since 1995, the registry is likely to contain a number of entries which are no longer valid, and there may be many files on the hard disc which are no longer needed. Unfortunately it is almost impossible to identify and remove these manually.

If you think this is the case, you might consider doing a clean install. To do this, you must first, clearly, back up anything on the hard disc that you want to keep. Then make sure that you have all your installation disks for the software applications that you will need to re-install, and also check that you haven't lost any of the CD-ROM security codes for software that came on CD-ROM. This is the point at which your filing system will be tested to its limits! Think carefully about whether this is a wise move or not.

Installation of a new system can reconfigure hardware settings which you were perfectly happy with. It is prudent to open control panel, system, and device manager, then note the IRQ and address settings of items which have a reputation for compatibility problems, such as sound or network cards (or, of course, anything which caused problems when you installed it). To see the settings, it may be necessary to check the manual configuration box under resources tab, when viewing the properties of the device.

Sometimes software is security protected by limiting the number of times it can be reinstalled. If this is the case, you should uninstall it back to the original installation discs first. (I would think twice about purchasing such software, as disk corruptions can happen repeatedly if you are unlucky, and you could lose your last possible installation.)

When you are sure you can re-install everything you need, the next step is to make a bootable floppy disc. To do this from Windows 95 you open control panel, then add/remove programs, and select the startup disc tab.

If you want to use any partition larger than 2.1GB, you will either need to be running a FAT32 version of Windows 95 already, or you will need to install Windows 98 over the current installation, make a Windows 98 startup disc, and then format the hard disc and reinstall to a clean partition.

When you reach this stage, re-boot the machine from the startup disc and check that you can access the cdrom drive. If you can, then it is safe to run fdisk to repartition the hard disc, or just run format if the partitioning suits your requirements. If you cannot, it may be necessary to copy the CD-ROM driver from your hard disk to replace the generic one loaded by Windows 98 (I have only seen this problem once, and it was for a very obscure type of CD-ROM drive).

Then run setup in the normal way, and after that reinstall your applications, and then the data.

If there are any hardware problems which you did not have previously, open the control panel, then double click on the system icon, and look at the device manager. Check that the obvious suspects, such as sound and network cards, are set to use the correct IRQ, addresses etc. and change them to the settings you wrote down earlier if there is any discrepancy. In some cases, even to see the settings requires you to check the manual configuration box under the resources tab. Don't forget to uncheck it if the automatic setup was satisfactory.

Everything should now be in proper working order.

We have tried to cover the subject of upgrades fully, but inevitably with new systems, questions will arise which none of us have seen before. If you run into a problem not mentioned in this series, and solve it we would appreciate an email telling us what you did. If, on the other hand, you cannot solve the problem, send an email and our experts will see if they have any suggestions. No promises - the variations that computers can throw up, if not infinite, can be very idiosyncratic.

Tell me if you would like to see a follow up to this series in a few months, if there are new questions which we are able to answer.

Equally, would you like a short series on constructing your own web site?

Email us at eti@aaelectron.co.uk with your comments and queries. It may take a little while to get back due to pressure of editorial deadlines, but we are interested in your views.

Note the contact fingers grounding the shield over the USB ports (lower right)

A PC-Controlled Sine Wave Generator

Mark Roberts

This audio project plugs into the PC printer port to provide an accurate audio generator.

The accompanying Softmark software generates the on-screen display and allows straightforward adjustment of the generator settings.

The project consists of a small number of parts (which helps to keep the cost down). The generator consists of one ic and a crystal oscillator. There is no need for an external power supply.

The project is designed first and foremost for modem and other telecommunications applications that need low-cost, accurate generation of precise test tones.

The circuit

The ML2037, IC2 [check this against his letters] uses direct digital synthesisers and has been designed to generate sine signals whose full scale amplitude can be set to 0.5 Vpp, 1.0 Vpp, 1.5 Vpp or 2.0 Vpp, and frequency from 2Hz to 64kHz. The sine wave output is derived from an external crystal. Frequency is programmed by a 16-bit data word. The relation between the output and the crystal is given by the following equation:

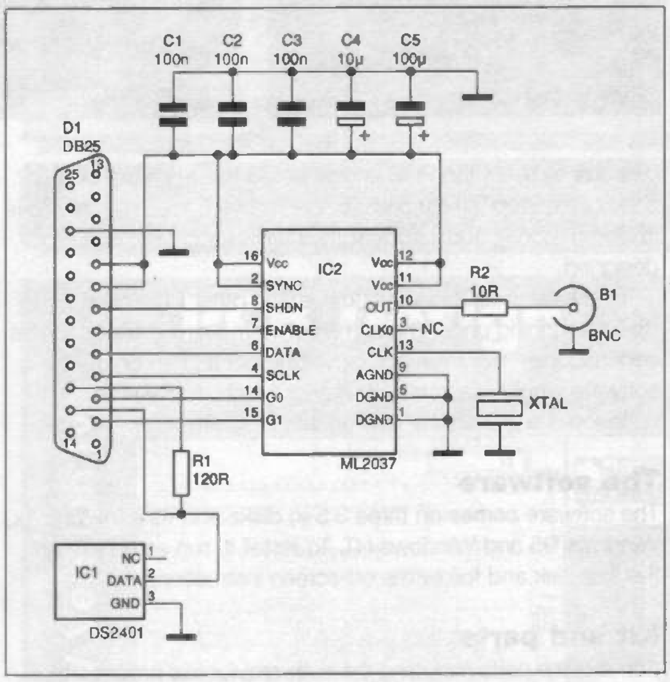


Figure 1: the circuit of the sinewave generator

fout = fxtal x DATA/2^23. The sinewave is available at pin 10 of IC2 (**figure 1**).

The sine wave Is available at IC2 pin 10 (**figure 1**).

Interfacing

The timing of serial data input SDATAIN, the serial clock (SCLK) and the enable Input -SENABLE is shown in **figure 2**.

The serial data word on SDATA is clocked into the 16-bit shift register on falling edges of SCLK. The LSB is shifted first. The data that has been shifted is loaded into the 16-bit data latch on the falling edge of SENABLE.

The device was tested to operate with a cable of about 1.5m in length.

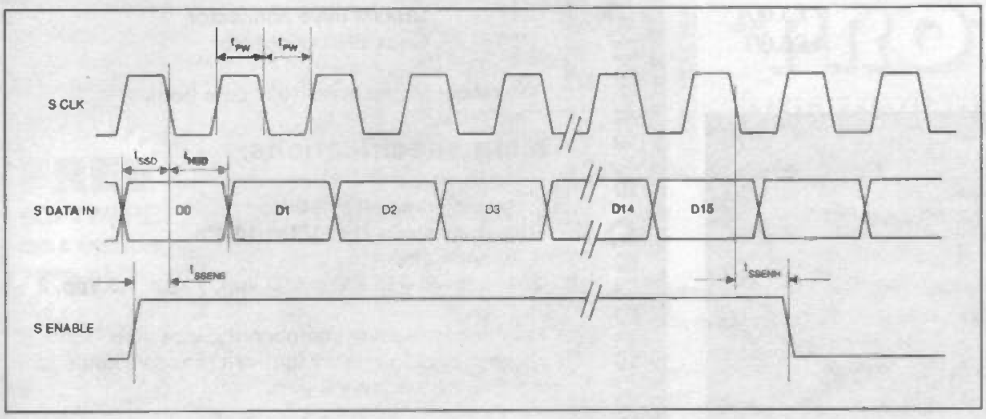
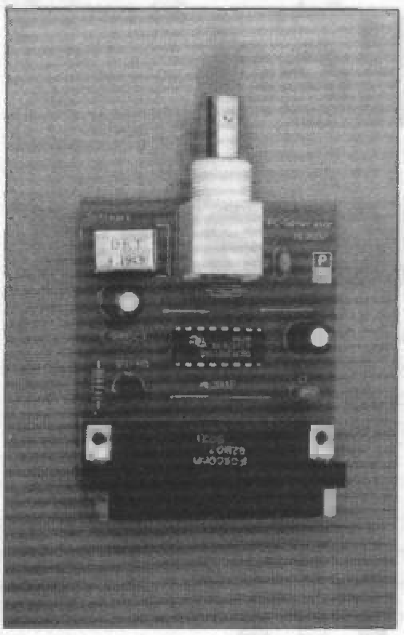
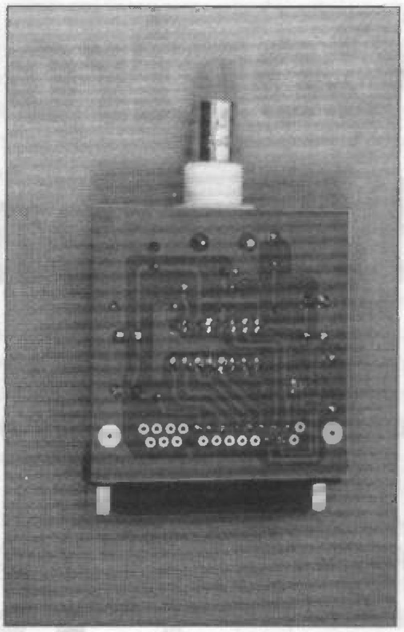


Figure 2: the timing of the serial clock, serial data input and the enable input

Construction

The Sine Wave Generator is built on a printed circuit board. The component layout is shown in **figure 3**. DS2401 is used as a





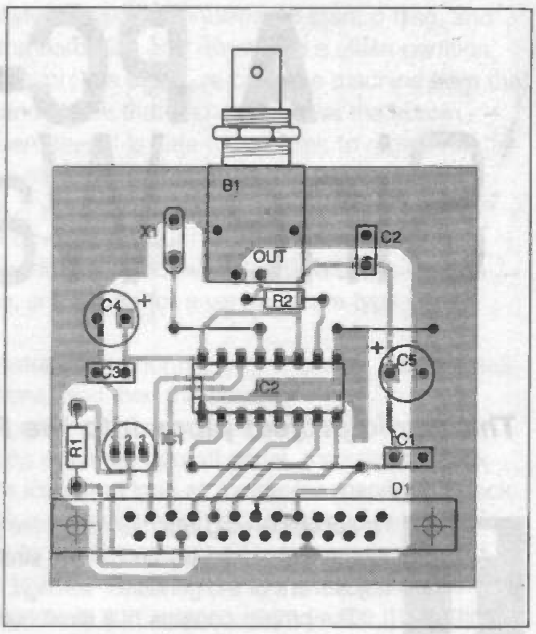


Figure 3: the component layout

detector to see if the PCB is connected to the printer port (in case of errors or discontinuities the software automatically runs in Demo mode), and also that the hardware project is built as designed.

One reason for this solution is that if other PC-based devices running under the same software were in use, such as oscilloscopes, power supplies, voltmeters and so on, the software would automatically detect which device was connected and start the appropriate program.

The software

The software comes on three 3.5-in disks and runs in Win3.1x, Windows 95 and Windows NT. To install it, run setup.exe on the first disk and follow the on-screen instructions.

Kit and parts

Some of the parts (including the software) for this project are specialised and only available from the author. Parts can be bought as a kit or separately. Prices are listed below. Local constructors who wish to enquire about other currencies should contact Softmark.

Software kit: three disks with the DS2401. (Software runs under Windows 3.1/Windows95/WindowsNT	£16.00
ML2037 (IC1)	£8.00
PCB	£4.00
4.194304 crystal	£2.00
BNC+DB25 connector	£3.00
Postage per order	*£3.00*
LPT2 card (option)	£6.00

Complete hardware and software: assembled £33 + £3 postage; unassembled £28 + £3 postage.

Cheques must be made out to Softmark and sent to:

Softmark, PO Box 1609, Hornsby NSW 2077, Australia
Tel/Fax (Australia) +61 2 9482 1565

PARTS LIST *for the Sinewave Generator*

Resistors

R1	120R
R2	10R if extra current protection is wanted; otherwise wire link or 0 ohms.

Capacitors

C1,C2,C3	100n ceramic
C4,C5	10u electro

Semiconductors

IC1	DS2401 DALLAS code-specific IC available from the author. The software will run only in demo mode with a different DS2401.
IC2	ML2037 (Microlinear)
Xtal	4.194304 crystal

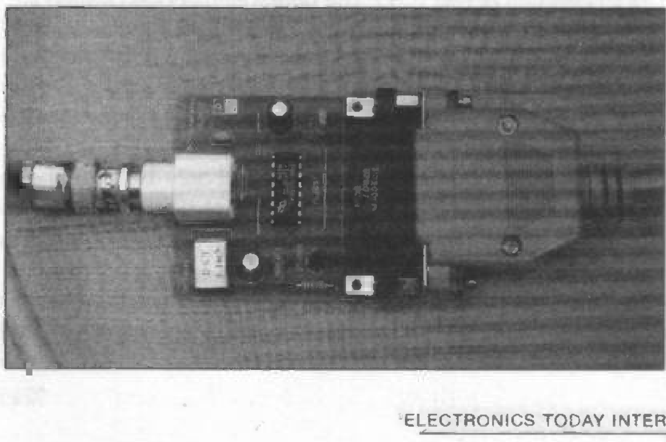
Miscellaneous

"D1"	DB23M male connector
"B1"	Coax BNC connector

Reference: MicroLinear 1997 data book

Main specifications:

Frequency range 0 to 64kHz
Frequency steps 2Hz, 10Hz, 100Hz
Waveform: sine
Output level: 0 to 2 Vpp (0.5 Vpp, 1 Vpp, 1.5 Vpp, 2 Vpp steps)
Spurious frequency components: less than -55dB
Three-channel memory that can preserve settings: voltage, frequency, PC port.



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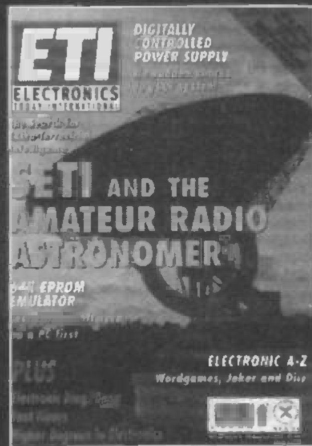

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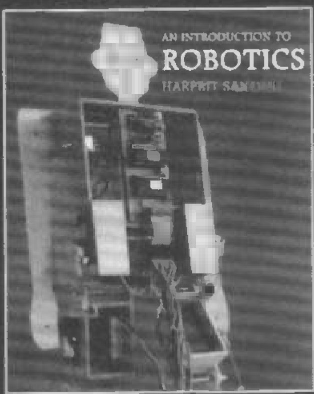

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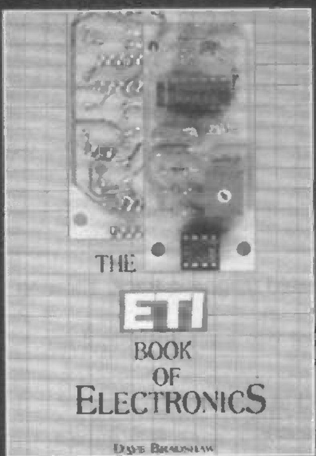

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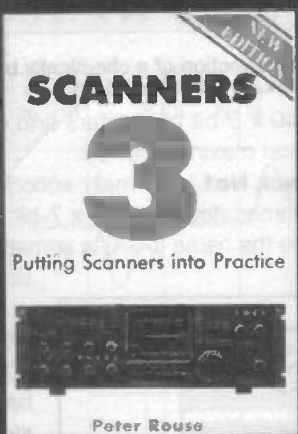

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A PC Magnetic Card Reader

Despite the proven advantages of smart cards, our wallets are quite likely to contain numerous magnetic cards well beyond the end of the century.

Patrick Gueulle

You can use a PC to look at what is encoded onto the mysterious dark stripes of, say, loyalty cards, or even credit cards.

Magnetic or "magstripe" cards are very standardised items, with only a few exceptions like some of the old fashioned phonecards (The Jerseycard or the now obsolete Mercurycard). **Figure 1** shows how the ISO 7810 and ISO 7811 standards precisely define the position and contents of three "tracks" on the magnetic stripe located 0.223 in from the upper edge of the plastic card.

This stripe is similar to an audio or video tape, half an inch wide, but is recorded in a completely different way.

A magnetic card only contains bits (ones and zeros) instead of analogue data. Numeric characters are encoded as groups of five bits (a nibble of data and a parity bit), but alphanumeric characters use an ascii-like seven bits code (six bits of data and a parity bit).

Track Nø2, the most widely used, is recorded at a "density" of 75 bits per inch (bpi), but because of the mandatory leading and trailing zeroes, its useful content is only 40 x 5-bit characters and not the easy-to-calculate physical maximum of 50.

Visual inspection of a chemically treated magnetic track, showing the "flux reversals" at 75 bpi

Track Nø1 is normally encoded at 210 bpi and accommodates up to 79 x 7-bit alphanumeric characters. I believe the name (IATA) is something to do with airline ticketing applications.

Track Nø3 is seldom used, despite its huge capacity of 107 numeric characters at 210 bpi (535 bits, more than can be stored in most low-end chip cards). Each bit is recorded by means of magnetic flux reversals, as shown in **figure 2**.

The tracks are evenly populated, like recording tape, with small, aligned magnetic domains whose polarity can be switched, during the recording process, from "north-south" to "south-north" and vice versa.

Adjacent N-S or S-N poles mutually neutralise themselves, but N-N or S-S combinations determine so-called "flux reversals", acting like very tiny permanent magnets.

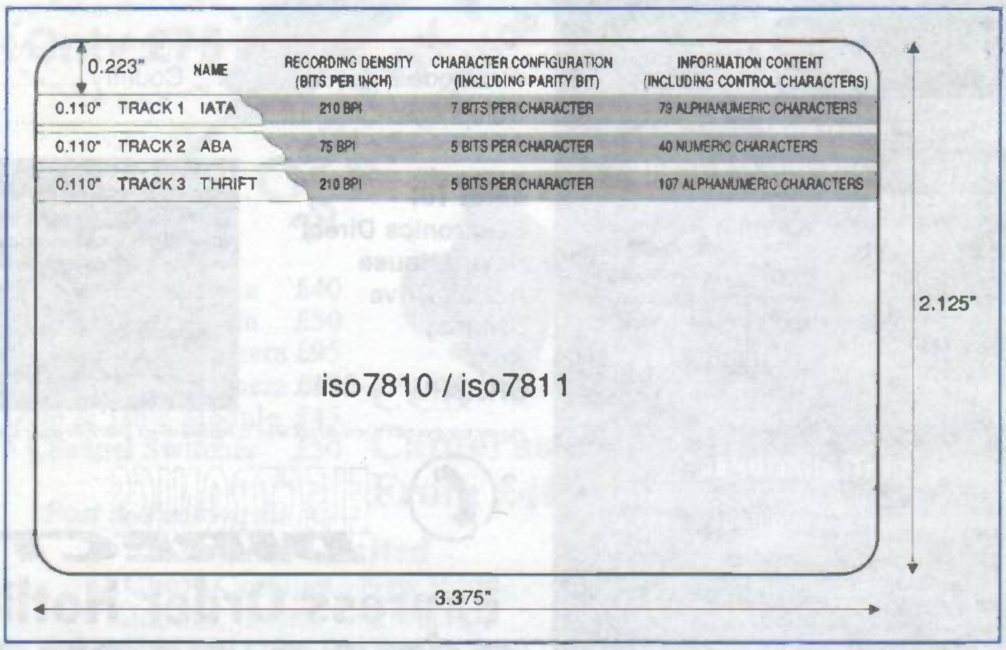


Figure 1: The three tracks of an ISO magnetic card

Purpose-made chemicals or films can be used for a visual inspection of the flux reversals (see photograph), but electromagnetic reading is by far the commonest way of reading magnetic cards.

As the stripe is swiped along a magnetic head, each flux reversal generates a slight voltage pulse of the corresponding polarity. Quite simple electronic circuits (amplifiers and flip-flops) can convert such pulses into clean logic levels (the "shaped signal").

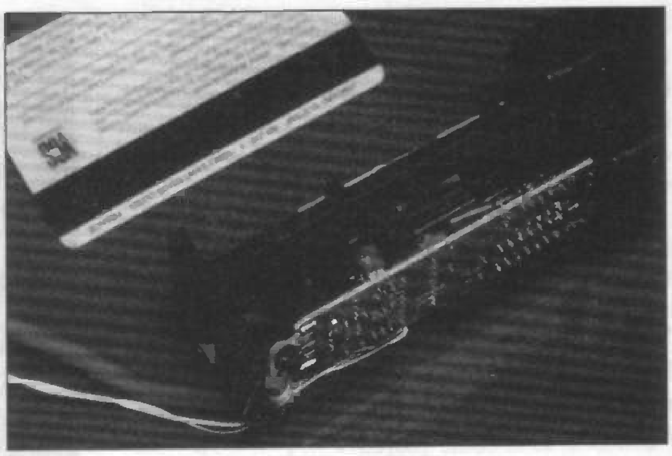
Extracting the data is a much more complex matter, since each and every bit is coded in the so-called "F/2F" format. **Figure 3** shows how a "zero" is coded as a single flux reversal, and a "one" as two consecutive flux reversals. This is a very robust encoding scheme, and allows the card sweeping speed to vary widely during the reading process.

Much more intricate circuits are required to decode the F/2F message into strings of ascii characters reliably. PC-compatible readers often make use of an embedded microcontroller and are interfaced through either a RS-232 port or a keyboard input.

Interfacing a TTL reader

TTL readers are much cheaper than RS-232 ones, and can be bought at around £10 (The BAR-31 model from Bull Electrical of Hove, Sussex is a perfect example). **Figure 4** describes the signals present on the /CLOCK and /DATA lines, a valid (but logically inverted) bit being available on the /DATA line at every trailing edge of the /CLOCK signal.

A third line (/CARD PRESENT) is usually driven low as long as a properly encoded card is being swept into the reader. The two remaining wires of most TTL readers are, obviously, the ground (GND) and the + 5 volts supply (Vcc). Interfacing such a reader to a PC is quite straightforward on the hardware side. **Figure 5** shows that the games port or joystick connector lends itself ideally to such an application, thanks to the + 5 volts and the four logic inputs available here.



The BAR-31 reader hardware

Please note, however, that the "/CARD PRESENT" line of the reader can remain unconnected (N.C.), because the software will easily derive the same information from the clock signal. Connecting a BAR-31 rader to the games port is just a matter of replacing its connector, or adapting a male DB-15 to an extension cord, since the original cable is rather short. The colours indicated for the wires are only valid for the BAR-31, and would probably be different on readers from another source. Make sure a wiring diagram is supplied, and check the wiring with that.

In any case, it is relatively easy to identify the five wires of virtually any TTL reader with just a multimeter and an oscilloscope. One will generally need to open the case to locate the ground and supply wires (connected to wide tracks on the internal PC board, and to one or more electrolytic capacitors).

With the reader being connected to a (possibly current-limited) 5-volt power supply, swiping a

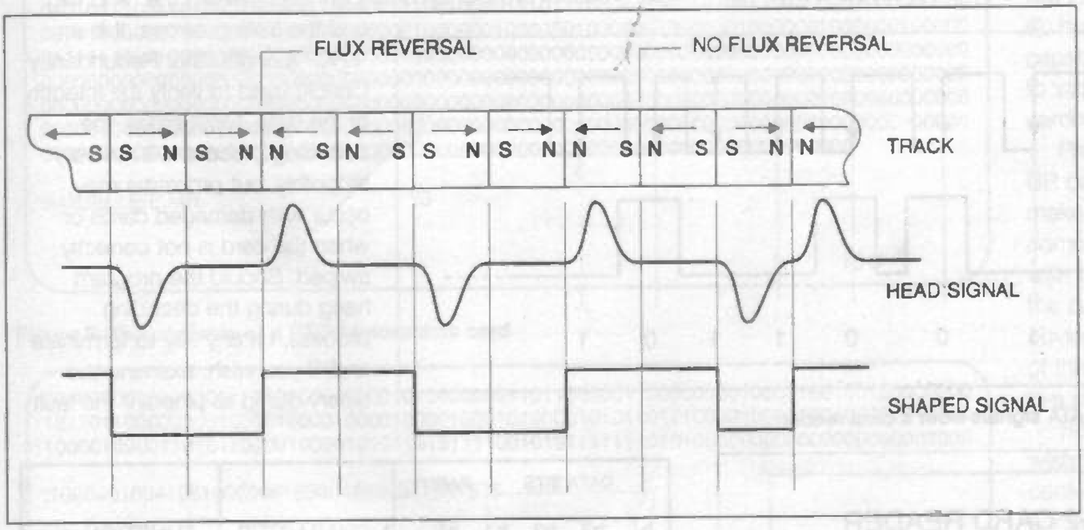


Figure 2: Reading a magnetic track

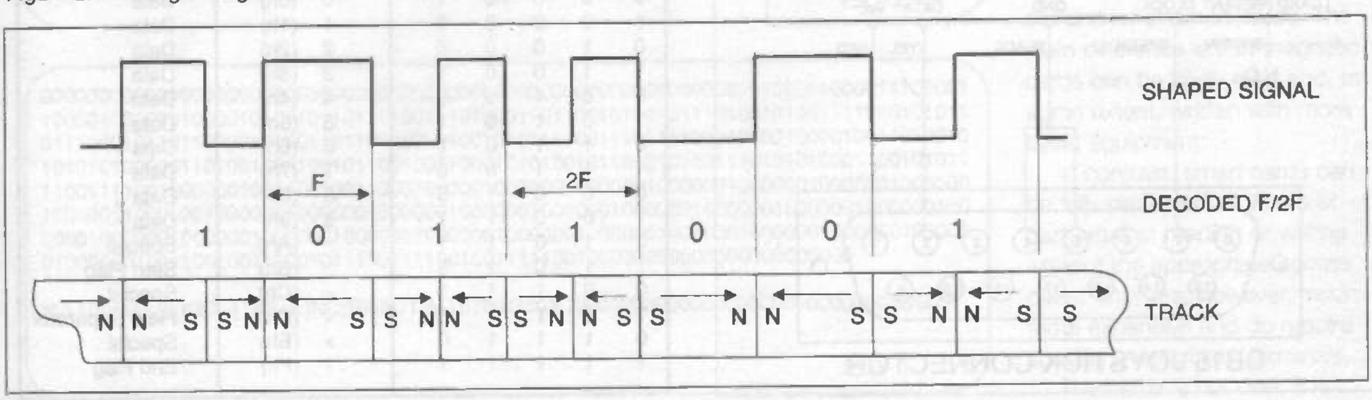


Figure 3: Decoding an F/2F signal

card through the slot should locate the /CARD PRESENT wire (a steady logic level), the /CLOCK signal (short regular pulses) and the /DATA output (an irregular rectangular signal). Some readers come with extra wires, either for signalling lamps or for a second or even a third track.

Most easily available readers only read track N°2, but we will soon discover that simple tricks can be tried for the reading of the other ones, especially track N°1.

An "American Magnetics" dual-track reader

The software

Because of the potentially unstable and often over-fast manual sweeping of the card, the decoding process is highly time-critical. On 386 computers running at 25 MHz or faster, the Turbo-Pascal program listed here will work fine, but only under MS-DOS (please completely exit Windows before running it).

MAG2.PAS should be compiled into an executable MAG2.EXE, then used in conjunction with the BAR-31 for the reading of track N°2. By the way, two other (and much longer) programs, MAG1.PAS and MAG3.PAS were developed for the reading of tracks N°1 and N°3 respectively, provided that the available reader does support them.

The BAR-31 can be temporarily modified for the track N°1 by inserting a small plastic ramp, exactly 3.3-mm thick, at the bottom of its slot. Reading track N°3 would actually involve cutting 3.3 mm off the card.

Once run, the program waits (forever) for a card being swept (in the direction of the arrow!), and may hang if the card is blank or defective. If this happens, please sweep a known-as-good card in order to terminate the execution.

Our real examples show that the software displays the contents of the track twice. First, as the raw binary data encoded on the card, including all leading and trailing zeroes (the reader hardware needs them for synchronisation purposes). Then, as the ascii string obtained when matching all significant groups of bits against the ANSI 5-bits code of **figure 6**, all leading and trailing zeroes being trimmed off. The first group of 5 bits after the leading zeroes should be 11010, the "start flag". Sixteen other combinations should be found later, the remaining 16 corresponding to parity errors, as the total number of bits in a character must always be odd.

Ten combinations are used to code the 0 to 9 figures, 3 are "specials", a "field separator" is available (10110), and an "end flag" (11111) marks the end of the data stream. However, a last group of five bits is usually added between the "end flag" and the trailing zeroes. It is an "LRC" (Longitudinal Redundancy Check) used to verify the integrity of the data. Most times, the decoding process will run very smoothly, but problems may occur with damaged cards or when the card is not correctly swiped. Should the program hang during the decoding process, hit any key to terminate and, if you wish, examine the binary dump to pinpoint the fault.

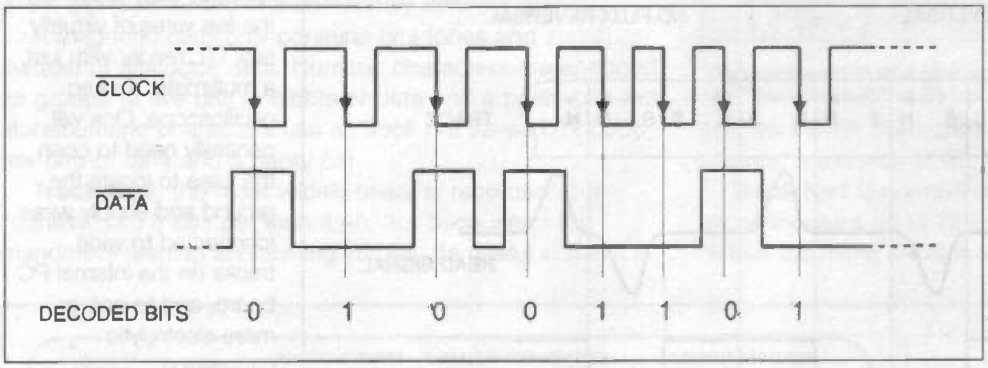


Figure 4: The /CLOCK and /DATA signals from a card reader

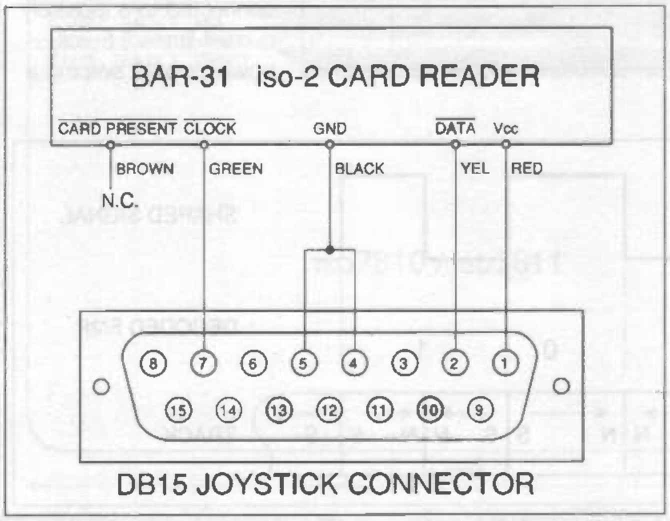


Figure 5: Interfacing a BAR-31 reader to the games port of the PC

DATA BITS				PARITY		
b1	b2	b3	b4	b5	CHARACTER	FUNCTION
0	0	0	0	1	0 (0h)	Data
1	0	0	0	0	1 (1h)	Data
0	1	0	0	0	2 (2h)	Data
1	1	0	0	1	3 (3h)	Data
0	0	1	0	0	4 (4h)	Data
1	0	1	0	1	5 (5h)	Data
0	1	1	0	1	6 (6h)	Data
1	1	1	0	0	7 (7h)	Data
0	0	0	1	0	8 (8h)	Data
1	0	0	1	1	9 (9h)	Data
0	1	0	1	1	: (Ah)	Special
1	1	0	1	0	; (Bh)	Start Flag
0	0	1	1	1	< (Ch)	Special
1	0	1	1	0	= (Dh)	Field Separator
0	1	1	1	0	> (Eh)	Special
1	1	1	1	1	? (Fh)	End Flag

Figure 6: The 5 bits numeric ANSI code

```
000000000001101001101110010010000001000010010000001000010000110000011010000010000
100001110010000101101100111011000001000010000100001000011100100001011011001110000
100001000010000100001000010000100001000011111111010000000000000000000000000000000

;6340040001600003069=0000030690000000000?;
```

iso-2

```
0000000000000000000000000000000000000000000000101000101101001100100001010100001
0000001000010101000010000001000000100100010101101000000100000010000001001100100
0001000110100100110010111010000100000010000001000000100000010011001000000010001 10
1001001100000010000001000000100000010000001000000100000010000001000000100111110 0
1010001000000000000000000000000000000000000000000000000000000000000000000000000
0000000000000000000000000000000000000000000000000000000000000000000000000000000
0000000000000000000000000000000000000000000000000000000000000000000000000000000
00000000000000000000000000000000000000000000000000000000000000000000000

%6340040001600003069=0000030690000000000?%
```

iso-1

Figure 7: The contents of a TESCO Clubcard

```
0000000000000110110000010000111001001001000011100010011111100000000000000000000000
0000000000000000000000000000000000000000000000000000000000000000000000000000000000
0000000000000000000000000000000000000000000000000000000000000000000000000000000000

;003417471
```

iso-2

```
00000000000000000000000000000000000000000000000101000111100111010111101001
0101011100110100011010101001011110010000111011100010110110100110000000100000010 0
0000100000010000001000000100000010000001000000100000010000001000000100000010000 0
0111111001100100000000000000000000000000000000000000000000000000000000000000000 00
0000000000000000000000000000000000000000000000000000000000000000000000000000000
0000000000000000000000000000000000000000000000000000000000000000000000000000000
0000000000000000000000000000000000000000000000000000000000000000000000000000000
00000000000000000000000000000000000000000000000000000000000000000000000

%GUELLE/P.MR                    ?3
```

iso-1

Figure 8: The contents of a P&O Motorpoints card

```
000000000000000011010100000000101000000011011000001100000000100001001001000000000
101101100000000100001000010000100001000101000010101101010000100001001000110100000
100001000011010110000100001010110101111001010111111101010000000000000000000000000

;1020=01004106100000815500460005115575?5
```

iso-2

```
0000000000000000000000000000000000000000000000000000101000110000111000 01
1000010000001000010101101101111001110100011011001011010111010010100111101010101 1
0111000101101100001010011011010001010010101110011101111000100001000010011010010
1010101000001101001001100101100100110001010100101101010100111010101000110010101 1
1100111100100000010011001001100010000001000000100000010000001000000100000010000 00
1000000100000010000001000000100000010000001000000100000010000001000000100000010 0
0000100000010000001000000100000010000001000000100000010000001000000100000010000 0
010000001001100100110001011100111100100111110010000000000000000000000000

%AA004MSBFKEYJ[T#R+E]NC(RI58DTR4T57B4G303C0000000000000000000000000003CG3?I
```

iso-1

Figure 9: The contents of a "Premier Points" card

Some practical examples

The tracks on a credit card roughly contain the same information as the ones "embossed" into the plastic (card number, cardholder's name, expiration date, and a few encrypted data). It can be used to make sure that both sets of data match, in other words that the card is "good", without erased or worn spots.

Loyalty cards of all kinds are much more interesting to explore, many different schemes being in use. Many of them are merely "ID" (identification) cards, all the value data being stored in the central computer of their issuer. The card is only used, at the point of sale level, to grant access to the data bank, either on-line or off-line.

A well-known example is the Tesco Clubcard, with exactly the same numbers being recorded on tracks 1 and 2, and embossed on the plastic card itself (**figure 7**). A similar principle applies to P&O Ferries MOTORPOINTS cards (**figure 8**), but the alphanumeric capabilities of track N°1 are used to store the name of the cardholder.

Premier Points ARGOS and BP cards, for instance, seem to make use of a much more complicated scheme, possibly with the points being stored on the card itself. The data are obviously encrypted, and a copy of them is likely to be kept safe in a central computer.

Here is a clue: should you wish to try to work out the contents of **figure 9**, this card actually carries 5 points. In fact, such a system is the direct competitor of smart cards. The main difference is that magnetic cards can be freely read and, to some extent, written with more basic equipment.

In contrast, smart cards can be fully protected, in whole or part, against reading or writing without the appropriate access code. They are, however, much more expensive and do require specific point of sale terminals.

The battle is not over, it is only just beginning!

Example: a Tesco Clubcard

Example: a P&O Motorpoints card

Example: a BP Premiercard

Software

A diskette containing the source and executable forms of all three programs can be ordered from the me. Just send a strong SAE and a blank formatted disk, along with a £5 banknote, to:

Patrick Gueulle
PO Box 279
76055 Le Havre Cedex
France

Of course, readers in France may send a cheque for 50 FRF.

Magnetic card reader: Turbo Pascal listing

```
program mag2;
uses crt;
var  t: array[1..240] of byte;
     e,i,j,k,v: byte;
procedure shape;
begin
clrscr;
sound(880);delay(500);nosound;
for k:=1 to 240 do
begin
t[k]:=t[k] and 16;
if t[k]=0 then t[k]:=1;
if t[k]=16 then t[k]:=0;
write(t[k]);
end;
writeln;writeln;
end;
  procedure read;
  begin
  for k:=1 to 240 do
  begin
  repeat
  e:=port[513];
  until e and 32 = 0;
  t[k]:=e;
repeat
until port[513] and 32 = 32;
end;
end;
   procedure decode;
   begin
   j:=0;
   repeat
   j:=j+1;
   until keypressed
or((t[j]=1)and(t[j+1]=1)and(t[j+2]=0)and(t[j+
3]=1)and(t[j+4]=0));
   repeat
v:=0;
for i:= 0 to 4 do
begin
v:= v*2;
v:= v + t[i+j];
end;
if v = 26 then write(';');
if v = 22 then write('=');
if v = 31 then write('?');
if v = 11 then write(':');
if v = 7  then write('<');
if v = 14 then write('>');
if v = 1  then write('0');
if v = 16 then write('1');
if v = 8  then write('2');
if v = 25 then write('3');
if v = 4  then write('4');
if v = 21 then write('5');
if v = 13 then write('6');
if v = 28 then write('7');
if v = 2  then write('8');
if v = 19 then write('9');
   j:=j+5;
   until keypressed or (j>235);
   end;
begin
clrscr;
writeln('PLEASE SWIPE THE CARD');
read;
shape;
decode;
writeln;writeln;
end.

(* Copyright (c) 1998 Patrick Gueulle *)
```

PARTS LIST

For the Magnetic Card Reader

Reader assembly
BAR-31 from Bull Electrical,
250 Portland Road, Hove, Sussex
BN3 5QT. Tel 01273 203500.

Connector
Male DB-25 with hood

Miscellaneous
5-conductor cable (optional), max 1 m

PC Controllable 4-Line Dot Matrix Display

Scroll multi coloured text through this large matrix display. The built in programmable controller can provide some spectacular effects.

Robert Coward

This project in three parts describes the building of a professional-quality 24-character by 4-line dot matrix LED display system. The display is fully PC controllable via an RS232 serial port. It is based on three QEDD9008 display modules. These were a surplus part, and they are available ready built from myself or from Greenweld Electronics (telephone 01703 236 363), part number X6877. See the end of this article. Together with the control board design described here, and suitable power supplies, they form a large display system costing a fraction of the price of an equivalent commercial unit.

The LED displays can show the full ascii character set in red, green and yellow, and are very bright at full contrast. The entire display can be dimmed almost to extinction under software control, allowing impressive fade effects. Other effects such as scrolls and wipes can be achieved using PC software commands. Two independent "flash clocks" allow individual words or letters to be flashed at different rates, adding to the visual impact of the display. The size of the characters means that the display should be readily visible up to 20 feet away, making it excellent for advertising and presentations.

This is a fairly large project, even though the display panel comes ready assembled. **As a mains project with some high wattage power supply capability, it can be hazardous if not treated carefully, and for this reason I do not recommend it for inexperienced designers.** Some of the components, such as the power supplies, are not strictly specified, so you will have to make some decisions in choosing these items, though some advice is given later in this article.

The first part of this project gives an overview of the system components, and detailed information on constructing the control board. The second part will cover choosing suitable power supplies, making cable assemblies, and assembling a working system. The final part will describe how to manufacture a suitable enclosure and assemble the system within it.

- **PC control interface**
- **Full ascii character set in red, green and yellow**
- **Dim, fade, scroll and wipe effects under software control**
- **Two independent "flash clocks" allow words or letters to be flashed at different rates**
- **Balanced red/green and yellow display intensity**

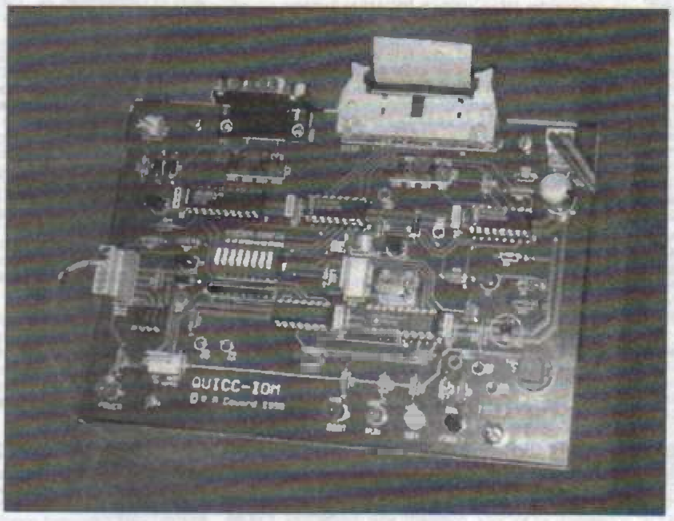


Figure 1: the circuit of the QUICC-10M controller board

Anatomy of the display panel

Each QEDD9008 display panel is a self-contained subsystem based on a HD64180 processor. It is designed to form a tile in a larger system (up to 15 panels, though this project - you may be relieved to hear - only uses three), and communicates to the outside world via a 26-way IDC connector, supporting an RS422 serial protocol at 12500 baud. On-board links select the tile number and other operating parameters, allowing up to three panels to be daisychained along one ribbon cable. All panels receive the same software commands, and work out what to display from their tile select links.

Four PCBs make up a working display panel; two identical display modules plug into the main processor board, and a mosfet transistor card plugs on the back. The latter provides drive to the seven rows for each colour, making a total of 14 transistors. Column drives are provided via a number of ULN2003 transistor arrays on the main board, which are fed from a giant shift register formed from 74HCT595 devices; the row drive data is also loaded into this shift register. The processor scans each row in turn, illuminating the appropriate column LEDs, and repeats this operation for the red and green colours. The entire scan cycle is repeated so that a red or green display is formed by scanning the appropriate colour twice, whereas yellow is achieved by alternating them; this way the yellow intensity is similar to the red and green intensity.

The LEDs are scanned at a rapid rate and at very high peak currents (circa 150mA); this runs them extremely efficiently, achieving high intensity for only 4mA approximate average current. The contrast is altered via pulse width modulation under processor

Figure 2: the QUICC-IDM component layout

control; this can be altered independently for red and green on a row by row basis, though the current firmware only allows the overall display contrast to be altered by software.

The processor subsystem consists of the HD64180 high integration CPU, 32K eprom and 16K ram, though unfortunately only half of the eprom is addressable in the existing design. Communication with the outside world is provided via a number of RS422 drivers and receivers; the panels can "talk back" to the PC if required, though the existing firmware only supports this in debug mode. There is also a special watchdog output, which is fed from a monostable on the transistor card; this is triggered by the row drive signals, so it only indicates a healthy status if all the row drivers are scanning correctly, and the display has power. It is designed to protect the system against a shorted row drive transistor or other fault which could result in excessive currents flowing (possibly damaging the display), by indicating the fault to a control circuit which would then shut the power down.

The watchdog signal is fed to the outside world via one of three link-selectable channels on the RS422 cable. This allows up to three panels to share the same cable. The processor reset is also controlled via an RS422 input from the ribbon cable, and this is used to put the system into a low power standby mode when not in use.

The display firmware accepts a simple set of software commands to display characters, set colour/flashing attributes and change the overall contrast. These are covered in detail in the documentation that comes with the PC driver software. Characters are sent as straight ascii codes, which closely match the PC character set for codes below 128. The full range of PC-compatible accented characters are also supported, along with special graphics and kanji characters which do not correspond to PC characters, but can still be displayed by sending the appropriate ascii codes. Attributes define the colour (red, green or yellow) and one of two flash modes for each character.

Two "flash clocks" are also fed to the display, and are continually scanned by the firmware. Any characters with one of the flash attributes set will be extinguished when the corresponding flash clock is in the "off" state. In this project, the flash clocks are driven in antiphase by default (though can be adjusted via special commands to the control board - see later), resulting in alternate flashing of characters with the corresponding attributes set.

Each display panel requires three power supply rails: 5V at approx. 300mA for the logic, 24V at approx. 20mA for the transistor drives and 8V at up to 5A for the LED drives. This latter supply is the most tricky to provide, as the current consumption can vary from almost nothing to approximately 15A for a three panel system, ruling out a supply with significant minimum load constraints. For safety, it also needs to be logic controlled, so that it can be shut down in the event of a fault. More details on choosing a suitable supply are given in the second part of this project.

Note that since the display panels are ready built, and the design belongs to the original manufacturer, a detailed description of the panel circuit and firmware is not included. Connection and configuration information is provided later in this article.

The PC Software

To drive the displays from a PC, you will require specialised software. For DOS-based systems, I have written QDSL (QEDD9008 Display Script Language), which allows you to quickly display messages and various special effects using a simple but flexible scripting language. The advantage of DOS software in this context is that you can get away with an extremely cheap and low power PC; a 286 system with only 640K base memory should be fine. Script files can be edited with an ordinary text editor, and are fairly intuitive once you have understood the basic concepts.

For a more user-friendly approach, you can used Windows-based WinDSL, written by a friend of mine, Huw Walters. This offers a full wysiwyg interface, and works like a proper word processor, even allowing you to paste in text from other Windows applications. While it does not yet offer the full feature set of QDSL, it is much more stylish and pleasant to use, and can output QDSL scripts, so you can still use a low performance DOS PC when actually running the system. You can, however, run the scripts directly from WinDSL if your PC is adequately powered.

Finally, there is IDMUTIL, a DOS-based utility program that allows you to fully test and configure the QUICC-IDM control board. More details on using this program are given later in this article. The latest releases of these programs can be downloaded from Huw Walters' web site, on http://www.realspace.demon.co.uk.

QUICC-IDM Control Board

The original display system was not specifically designed for PC control, though it runs at a baud rate very similar to what a PC can achieve (12500 baud as opposed to 12800 baud). It communicates via RS422 rather than RS232, and there are other signals that need to be managed, such as the flash clocks and display reset. For safety, the display power supply needs to be shut down in the event of a fault, so some form of protection circuit is necessary. Hence the extra control and interface circuitry that is needed.

Originally, I undertook the design of a simple control board, which was basically an RS232 to RS422 converter, with a monostable circuit to start the power supply and provide automatic power down facilities. This was called QUICC (QEDD9008 Universal Interface and Control Circuit), and a significant number have been sold to date via Greenweld, but stocks are now almost exhausted, and that design is being discontinued.

While the basic QUICC design was effective, it had some shortcomings, and was not particularly flexible or configurable for different operating environments. Therefore, I undertook the design of a more elegant and sophisticated board called QUICC-IDM (Intelligent Display Manager). This is based on a PIC16C84 (or PIC16F84) microcontroller, and provides significantly enhanced features, such as programmable timers, fault diagnosis, configurable flash clocks and software-controllable power-up and power-down. The PIC firmware contains a full software UART, allowing it to accept a number of PC commands, and provide

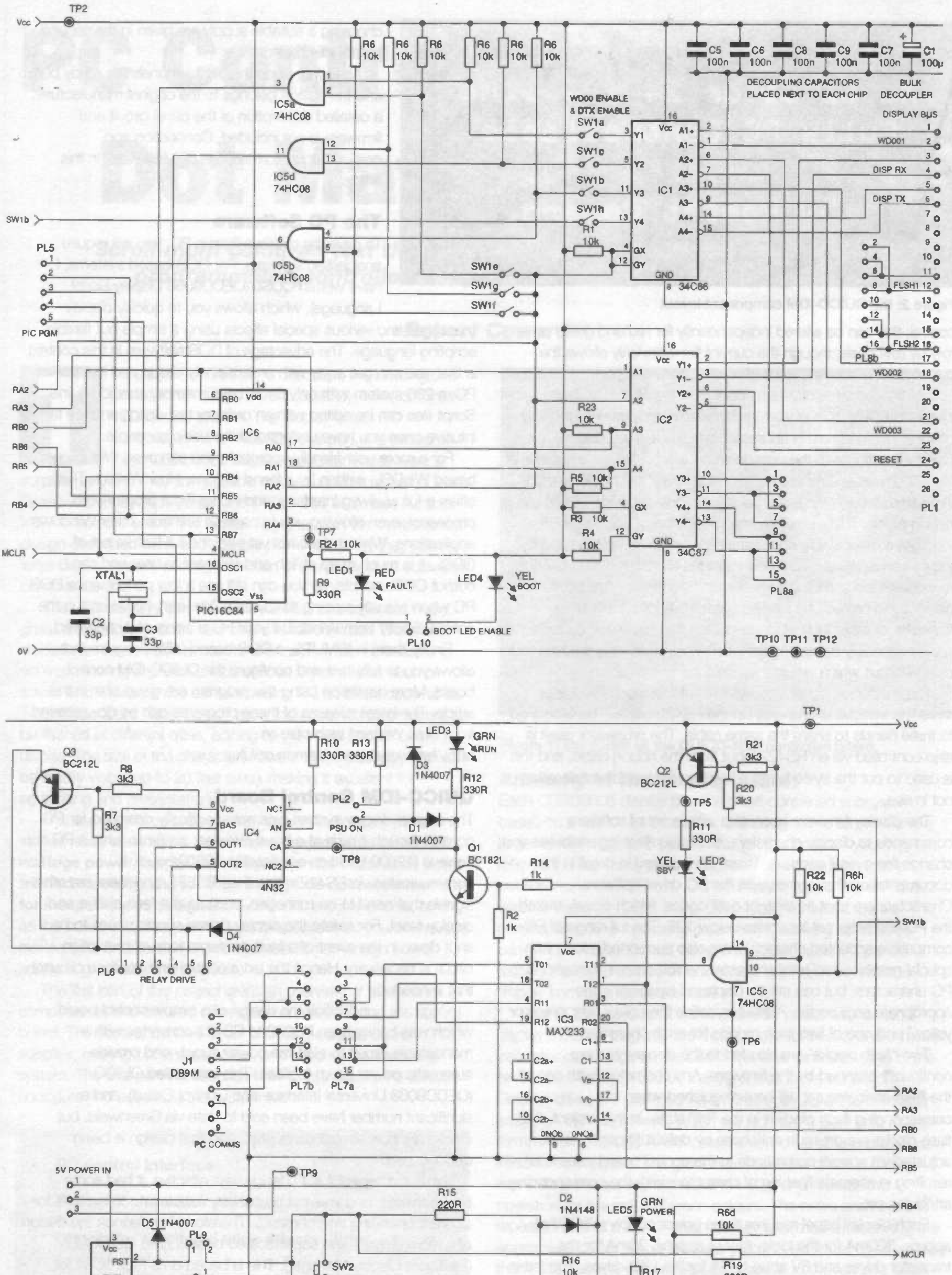


Figure 1: the circuit of the QUICC-10M controller board

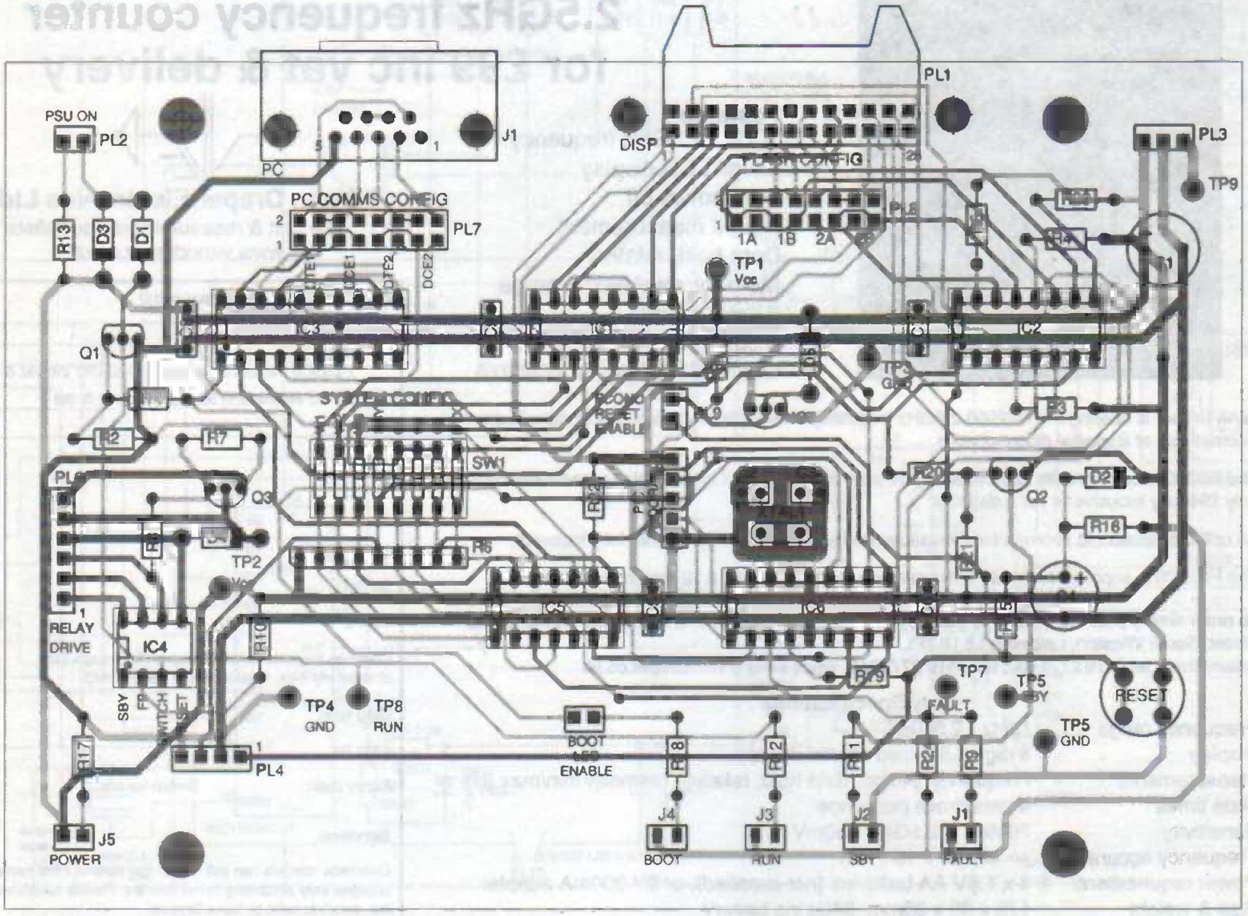


Figure 2: the QUICC-IDM component layout

information via response messages. The board also has an optional opto-isolated relay drive circuit to facilitate the logic control of the display power supply.

The rest of this month's article is given over to a description if this board, and full constructional details are provided. While PCB foil patterns are provided in this magazine, I recommend that you buy a ready-made board from Greenweld or myself, since this is a double-sided board. The ready-made board is a high quality, silk screened, double sided plated through hole board. (See the end of this article.)

The circuit

The full circuit diagram is given in **figure 1**, and a component layout diagram in **figure 2**.

The PC serial port is connected to 9-way male D-type CONN1, and the RS232 signals processed by IC3, a MAX233 dual transceiver. This has on-board charge pumps, so does not need external capacitors. The PL7 links allow the serial connector to be configured as DTE (requiring a reversed or "null modem" cable), or DCE (requiring a straight through cable). For DTE, pins 1, 2 and 3, 4 and 9, 10 and 11, 12 are shorted, and for DCE the shorting links are moved to the other four pairs of pins. The recommended setting is for DTE, as this is normally associated with a male connector. Note that you can of course plug gender reversers into the D type, but you cannot replace it with a female one (the pinout would not match). Apart from the RX and TX signals, DTR from the PC is used to drive the flash clocks to the panels, and DSR is used to indicate the display PSU status. Other handshake lines are unused, and RTS is connected to CTS to allow PC terminal programs to work.

Meanwhile, the display panel ribbon cable is connected to 26-way IDC plug PL1, and received RS422 signals are processed by IC1, a 34C86 CMOS quad line receiver. Note that this device has fail-safe inputs, and will read a logic high for disconnected or inactive inputs; the cheaper bipolar 3486 equivalent does not have this feature, and must not be used. Transmitted RS422 signals are processed by IC2, a 34C87 CMOS quad line driver. The cheaper 3487 bipolar part can be used instead, but at the expense of significantly higher power consumption.

Signals received by the display panels are RX data (PL1 pins 3 and 4), display reset (pins 23 and 24), and the two flash clocks (pins 11, 12 and 15, 16). The PL8 links are provided to allow you to preset the flash clock polarity (or selectively disable the flash clocks altogether), but since the PIC offers software configurability, they are generally left at their default settings (pins 1, 2 and 3, 4 shorted for flash 1, and pins 9, 10 and 11, 12 shorted for flash 2).

Signals transmitted by the display panels are TX data (PL1 pins 5 and 6), watchdog 1 (pins 1 and 2), watchdog 2 (pins 17 and 18) and watchdog 3 (pins 21 and 22). When you come to configure the display panels (described in part 2), you will find that each panel can output its watchdog signal on one of these three channels. The recommended setup is for the watchdog to correspond to the panel number, which makes fault diagnosis much easier.

At its simplest level, the board acts as an RS232 to RS422 converter, and transmitted data from the PC is fed directly from IC3 pin 3 to IC2 pin 1. Received data from the panels is fed from IC1 pin 13 (via switch SW1h) to IC3 pin 2, but this time via AND gate IC5a; this is necessary to allow the PIC comms to be gated in. Note that switch SW1h allows the received panel comms to be disabled for debugging or fault finding use (this was not present on early issues of the QUICC-IDM board).

PIC microcontroller

The heart of the system is the PIC microcontroller, IC6. This receives data from the PC via pin 6, and transmits it to the PC via pin 12, which feeds into the other input of IC5a. Thus the PIC receives all data transmitted from the PC (including that to the panels, which it ignores), and can transmit back to the PC, but only while the display panels are not transmitting. This is not a problem in practice, since the existing panel firmware does not transmit at all, except during debugging, and any new firmware would be designed to transmit only in response to a direct PC command. This is the way the PIC itself works, in that it only transmits a status message back to the PC in response to a valid PC command.

The PIC controls the display power supply via pin 2, feeding into common emitter stage Q1. This in turn provides a drive to the PSU logic control signal via PL2, suitable for the original 8V supplies that came with the display system, or any other PSU with an opto-isolated input control. Alternatively, you can use the opto-isolator drive circuit formed by IC4, either by connecting directly to the output pins via PL6, or using the output drive transistor Q3, also connected via PL6. Part 2 of this article contains more details on controlling PSUs via this circuit.

The PSU control signal also illuminates LED3, indicating that the system is running, and is fed to IC3 pin 1, which in turn generates the DSR signal to the PC. This allows the PC software to directly monitor the PSU status, to check that the system is running correctly, and flag an error if it shuts down unexpectedly. In this case, the PSU software would usually interrogate the PIC for further details regarding the fault.

The PIC also controls the reset to the display panels from pin 1, and this is fed to IC2 pin 7 which in turn generates the RS422 signal on pins 5 and 6. This signal is asserted low while the system is in standby mode, in order to blank the display panels cleanly (otherwise they would fade out while the PSU voltage decayed away), and minimise their power consumption from the logic supply (typically 25 percent saving compared to when the panels are running but blank). It therefore illuminates standby LED2, via common emitter driver stage Q2; the transistor is required to prevent the LED from pulling the PIC output voltage out of tolerance.

The PIC reads the DTR signal from the PC, via pin 11 (from pin 20 of IC3). This is normally toggled by the PC software when the system is running, to provide the flash clocks to the display, and to kick the PIC's internal standby timer to prevent it going into standby mode. The PIC generates the two flash clocks on pins 17 and 18, which are converted to RS422 by IC2. Normally, the PIC will simply set them to follow the PC DTR signal, so that they will run in antiphase, but internal dividers can be set up on software command, so that the clocks can run at entirely different rates, with varying mark-space ratio.

Switch SW1d feeds directly into pin 10 of the PIC, and is used to enable or disable standby mode. Because this is a common function, it is also brought out to the outside world via PL4 pins 3 and 4, so that an external switch can be connected. The PIC also directly drives LED4 (system booting) and LED1 (fault indication); resistor R24 converts the open collector to a logic level for monitoring via TP7. Note that link PL10 is provided so that LED4 can be disabled if, for example, it drains too much current for the in-circuit programming to work (see below).

Watchdog signals

In order to provide fault monitoring capability, the three display watchdogs are fed to the PIC pins 7, 8 and 9, via AND gates IC5a, IC5b and IC5d respectively (note that the watchdogs are shown out of order on the circuit diagram - this made the layout simpler). They also pass through switches SW1a to SW1c, allowing the watchdogs to be selectively disabled for fault finding. The other inputs to the AND gates are fed from config switches SW1e to SW1g, the other side of which are directly connected to the reset line from pin 1 of the PIC. This reset line also feeds into the enable signal on IC1, which will tri-state its outputs when it is asserted low. The net result is that the PIC monitors the display watchdogs when the panels are out of reset, but reads the config switches when they are in reset, effectively doubling the amount of I/O available. In practice, the PIC only reads the switches when it starts up, so needs to be reset or power cycled in order to pick up changed settings.

Note that an intrinsic feature of the fail-safe nature of the 34C86 part (IC1) is that watchdogs for disconnected or absent display panels will read "good", indicating a panel being present. This is a deliberate aspect of the design, so that less than three panels can be used with the board without having to manually disable the watchdog signals; forcing the user to disable the watchdogs for absent displays could be a hazard in the eventuality of more panels being added at a later date, as they may forget to re-enable them. The downside of this design is that certain panel faults, such as an absent 5V supply, will not be picked up, but these are not dangerous faults. Any single fault compromising the safety of the system, such as a shorted 8V supply or failed row drive transistor, will be detected. Since the PIC also uses the watchdogs to report the number of panels fitted to the PC, the PC software could check for a specific number of panels, and report an error if less were discovered (this would provide close to 100 percent fault coverage).

Clocks and reset

The PIC is driven by a 4MHz clock, derived from XTAL1. This may be a crystal or ceramic resonator; if using the former, then capacitors C2 and C3 are typically chosen to be 33pF. Alternatively, if using a resonator, they are typically 47pF. Note that you can use a three-terminal resonator, in which case the capacitors are not required.

Though the PIC has an internal power-on reset circuit, this is not adequate for slowly rising supply voltages, and provides no protection against brown-out conditions. Therefore, the board contains an external power-on reset circuit, consisting of C4, R16 and D2. A manual reset is available via button SW2, also brought to the outside world via PL4 pins 1 and 2. R15 protects the button from discharge currents from C4, while R19 protects the PIC MCLR input from noise spikes. D2 ensures the capacitor is discharged as the supply voltage falls.

An optional brown-out protection circuit can also be fitted (this was not present on early issues of the QUICC-IDM board), based around IC7, a DS1233-10 Econo-Reset device (this must be a DS1233 device, not a DS1233A or DS1233M device). This will put the system in reset whenever the supply voltage drops below 4.5V (other tolerances are available, but this 10 percent tolerance device is recommended because the PIC can work down to 4.0V). Link PL9 is present to allow the device to be disconnected when the in-circuit programming feature is used (see below), as the high voltages present on the PIC MCLR pin would otherwise damage it (D5 attempts to provide some protection if this is done inadvertently).

Miscellaneous

The board provides full in-circuit programming capability via PL5. More details on using this facility are given at the end of part 3 of this project, but it basically allows you to program the device insitu using any commercial or home-brew programmer that supports the modern serial programming protocol. When using the facility, 12.75V is applied via PL5 pin 4 to the PIC's MCLR pin, so link PL9 must be opened to protect IC7 and allow programming to take place. Programming clock and data signals are applied via PL5 pins 2 and 3, respectively. The ground connection should be made via PL5 pin 5, but you would not normally connect to the supply voltage on pin 1. Note that LED4 will illuminate during programming, acting as a handy programming indicator, but could present too much of a current drain for some programmers to work. In this case, it can be disabled via PL10.

The PIC firmware has three configurable timers stored in internal eeprom. These can be adjusted via software commands from the PC. The Standby timer determines how long the system waits before going into standby mode since the last toggle of DTR, or the.last "wake up" message sent from the PC. The two other timers are concerned with booting the system from standby mode:

When the system receives a "wake up" message from the PC (or the standby switch is open), the PIC attempts to perform a clean startup of the displays (to prevent their "sign on" message appearing). Firstly, it takes the displays out of reset, extinguishing LED2 (Standby) and illuminating LED4 (Boot). It then waits for the Boot timer interval, giving the PC software a chance to blank the display data, and switches on the PSU, illuminating LED3 (Run). It then waits for the PSU Override timer interval before extinguishing LED4 and beginning to monitor the display watchdogs. The PSU Override timer therefore gives the PSU time to reach full output, and defaults to 300ms; it may need to be lengthened for particularly slow PSUs. The Boot timer defaults to 400ms, but can be lengthened if required to prevent the PSU from being turned on too rapidly after previously being turned off (especially if the PSU is being switched at its mains input - some PSUs do not like short interruptions to their mains supply).

Construction

A PCB layout diagram is shown in **figure 2**. This is identical to the silk screen on ready made PCBs. The ready made board is a double sided plated through hole design, so if you are manufacturing your own non plated-through board, you must ensure that all through-board connections are made by soldering on both sides of the PCB. Via holes will have to be soldered via pins or small wire links, and some components, such as IC sockets, will have to be carefully chosen so that you can get access to solder the component side of the PCB.

Assuming you are using a ready made board, construction is very straightforward. The board has small pads, so you need a reasonably fine soldering iron and good soldering skills. You should also note that plated through boards are far more difficult to desolder than single sided ones, so correcting mistakes could be difficult and expensive, especially with multi-pin components such as ic sockets. I strongly recommend that you do not try to solder ics directly to the board, as replacement in the case of malfunction will then be impractical.

For this project, the board will be mounted in a case, with the LEDs and some switches brought out to a separate control panel via flying leads. Thus the five LED positions should be fitted with 2-way Molex headers, pin 1 to the anode connection on the left (the plastic polarisation tab toward the front of the board), so that the LEDs can be mounted remote from the board. It is also a good idea to use two 2-way Molex headers for PL4, rather than one 4-way one, so that the Standby and Reset switches can be individually plugged into the board. Note that the Standby switch is in parallel with SW1d (position 4 on the DIL switch), so this will have to be left open circuit for the external switch to work; alternatively, you could cut off pins 4 and 13 from the DIL switch package (and file them down to ensure they don't short to the board) before soldering it to the board. Note that the other DIL switch positions are not brought to the outside world, as they are for testing and debugging purposes only.

If you do not envisage changing the hardware flash clock configuration (it can be programmed in software via commands to the PIC, anyway), you can simply use four wire links for PL8, linking pins 1,2 and 3,4 and 9,10 and 11,12. Also, most programmers will have no trouble driving LED4, so PL10 can be replaced by a wire link if desired. And if you always want a fixed configuration for the PC comms, then PL7 can be replaced with wire links (see circuit description for configuration details).

If using a crystal for XTAL1, then the metal can should be anchored to the board by soldering it to one of the square pads on the topside of the board; this is best done before C2 and C3 are fitted. For crystals, C2 and C3 are typically 33pF, but check with your crystal manufacturer if in doubt. If using a 2-pin ceramic resonator, these capacitors are typically 47pF, though again this may depend on the specific device being used. For the most cost effective solution, use a 3-pin resonator, and dispense with C2 and C3 altogether. Note that the XTAL1 pads are deliberately very small, to prevent short circuits to the underside of the crystal body (however, it is still best to use an insulating washer if possible), so you should take extra care when soldering them.

If you never intend to use the in-circuit programming facility, then you can dispense with PL5 and replace PL9 with a wire link. D5 can also be omitted, and C4 reduced down to approximately 220nF, since it no longer has to provide power-on reset when PL9 is open. Alternatively, if full brown-out protection is not required, you can simply omit IC7, D5 and PL9.

The optional opto/relay drive circuit IC4, Q9, R7, R8 and D4 is highly dependent on the sort of power supply being used, and can be omitted altogether if one of the original 8V supplies (or another supply compatible with the drive from PL2) is being used. Part 2 of this project gives details on choosing a suitable PSU, so it is best to wait until the choice has been made before constructing this part of the circuit.

When mounting PL1, it should be secured to the board using M2.5 screws before soldering the pins, to prevent the solder joints being stressed. This also applies to CONN1, if it is not a snap-in design. For snap-in D types, solder the retaining lugs as well as the data pins to provide additional mechanical strength.

IC sockets are recommended for all devices, including the optoisolator IC4 (note that 6-pin optos should be fitted to the right hand side, with PCB pads 1 and 8 unconnected). Also, there are a number of test points provided, but you don't have to fit them all. To facilitate testing, fitting supply and ground points TP1-TP4 is recommended.

Note that IC7 must be a DS1233-10 (or at a pinch DS1233-5). The DS1233A and DS1233M devices cannot be used, as the former is for 3.3V systems, and the latter has a completely different pinout. As the device is physically small, the part number may be difficult to see, so check it very carefully before fitting it to the board.

In order to see what the board is doing, you really need to connect LEDs to the five Molex connectors along the front of the board (LED1 to LED5). To save time and effort, you might as well make up the LED assemblies that will go into the final system. These are basically 30cm lengths of lightweight twisted pair wires, with the LED soldered at one end (use insulating sleeving on the joints), and a 2-way Molex header on the other. Make sure that pin 1 of the connector goes to the LED anode.

For the proposed system, I recommend that you use high brightness water clear LEDs, as they look very smart through the clear freznel lenses that I also recommend. In order to identify which colour is which, you could make the anode wire match the LED colour (use grey or a different shade of green for the second green LED). The cathode wire can be another colour such as black. Once the assemblies are complete, plug them into the appropriate connectors, as follows:

LED5 (Power) - green
LED4 (Boot) - orange
LED3 (Run) - green
LED2 (Standby) - yellow
LED1 (Fault) - red

You will need to power the board in order to test it, so you should make up a twisted pair cable assembly to plug into PL3. In order to minimise voltage drops, you should use moderately thick wire, and terminate it in a 3 way Molex header, with +5V going to pin 1 and 0V to pin 2. Pin 3 is left unconnected. The cable assembly should be approximately 50cm long, and the wire colours should be red for 5V and black for 0V.

Assuming you have configured the board as DTE, you will need a serial cable in order to test the board with a PC. Such a cable can be bought commercially, as a 9 way female - 9 way female reversed or "null modem" cable. It may also be called an "AT data transfer cable", because it can be used to connect two PCs together. If you want to make up your own reversed cable, the following connections are required:

RX pin 2 - TX pin 3
TX pin 3 - RX pin 2
DTR pin 4 - DSR pin 6
GND pin 5 - GND pin 5
DSR pin 6 - DTR pin 4

If using the board as DCE, simply use a cable with the above pins wired one to one between the two connectors.

Testing the board

Once assembly is complete, it is a good idea to take time check carefully that all polarised components are the right way round, and that all solder joints are sound, with no bridges or splashes. It is also advisable to use a multimeter to check that the supply rails are not shorted. Finally, ensure that DIL switch position 4 (SBY) is open, and all others are closed.

Next, apply power to the board, preferably from a current limited supply set to no more than 100mA (unless you have used a bipolar device for IC2, where the limit should be more like 200mA). If the power consumption rises above approximately 60mA (150mA for bipolar IC2), then there is a fault, and you should turn off and re-check the board for assembly faults.

Assuming everything is OK, you can do some basic testing: LED5 (Power) should be lit, and when the reset button is pushed, LED2 (Standby) should light briefly, then go out and LED4 (Boot) should light. Shortly after this, LED3 (Run) should light, and shortly after that LED4 (Boot) should extinguish. LED3 (Run) should remain lit, and LED1 (Fault) should not light at all.

If you have observed this operation, then the PIC is basically functioning, though there could obviously be faults in the PC and display panel communications. To test the PC interface, you should connect the board to a COM port, and run the IDMUTIL program (use the /2 option to use COM2). The program should indicate the presence of the board, and display a block of information regarding the timer settings and switch configuration (you can use the /v option to obtain more detailed information). If the software fails to detect the board, then you should check the cable and connections, and failing this U3 and the PIC itself (U6).

The three configuration switches SW1e to SW1g (labelled C1 to C3) are only read by the PIC after reset or power-on, and with the current PIC firmware, control the following:

Switch C1 - Force QUICC compatibility mode (when open). The PIC will start the system whenever DTR is toggled by the PC, rather than when it receives a specific start-up command. This makes the board behave like the simple first generation QUICC board.

Switch C2 - Force "dumb" mode (when open). The PIC will no longer send any responses to the PC (so it will think the board is not present), but will still act on PC commands. If there is something wrong with this switch, or connection to the PIC, the board will not be detected by IDMUTIL.

Switch C3 - Write protect eeprom memory (when open). Any attempts to adjust the timers will fail, because the PIC will not update the stored settings in its non-volatile eeprom memory.

You can check the operation of these switches by changing them, and resetting the PIC afterwards. As long as switch C2 is closed, IDMUTIL will report whether any of the switches (including the Standby switch) are open. IDMUTIL can also be used to test LED1 (Fault) via the /t option, as long as you are using the latest firmware (1.06 and above).

Further testing of the board can be done once you have assembled a proper system, and this is covered in part 2 of this project next month.

Hardware

The Display Panels can be purchased from myself or Greenweld Electronics as surplus items, and currently cost £15 each inclusive. Some units suffered minor damage while being removed from the original system, so it is a good idea to request panels in good condition. I have also found manufacturing faults in a few of them, including unsoldered joints, an eprom leg bent under the device, and a reversed polarity reset capacitor that was causing the panel to shut down intermittently. It is a good idea to inspect each panel carefully for this type of fault before using it in this system.

The double-sided Controller PCB currently costs £40: the price includes the pre-programmed PIC (not copy protected), and a disk containing all the PC software, documentation, and the PIC hex files. The PIC source code is not included, though you can buy it directly from myself - please enquire. If you intend to make your own board, I can supply the PIC and software for £20. If you wish to obtain display panels and/or QUICC-IDM controller PCBs from myself, please write to: R. A. Coward, 22 Alexandra Park, Queen Alexandra Road, High Wycombe, Bucks HP11 2HJ or email enquiries to rcoward@dev.madge.com. Service by mail order only; please do not telephone or call. Please make cheques payable to R A. Coward and add £9 postage and packaging to any order that includes, or £5 if you are only buying boards and software. Display panels have not been inspected or tested. While I would attempt to ship the order as quickly as possible once payment has been received, please allow up to 28 days for delivery.

PARTS LIST for the Display Control Board

Resistors

R1,3-5,16,22-24	10k resistor 0.25W 5 percent
R9-13, 17-18	330R resistor 0.25W 0.25W 5 percent
R2, R14	1k resistor 0.25W 0.25 W 5 percent
R15, R19	220R resistor 0.25W 5 percent
R20-21	3k3 resistor 0.25W 5 percent
R6	10k 8-way 9-pin resistor network
R7-8	Application dependant (see text)

Semiconductors

IC1	34C86 quad RS422 line receiver (Farnell 406-843)
IC2	34C87 quad RS422 line driver (Farnell 406-430)
IC3	MAX233 dual RS232 transceiver (Farnell 407-215)
IC4	4N32 opto isolator (see text)
IC5	74HC08 quad 2 input AND gate
IC6	PIC16C84 PIC micro (pre-programmed)
IC7	DS1233-10 econo-reset 10 percent (Maplin LE15R)
Q1	BC182L NPN transistor
Q2, Q3	BC212L PNP transistor (see text for Q3)
D1,D3,D4,D5	1N4007 1A rectifier diode (see text for D4)
D2	1N4148 signal diode

External LEDs (water clear, high brightness):

LED1	Red 5mm LED (eg RS 260-9485)
LED2	Yellow 5mm LED (eg RS 260-9508)
LED4	Amber/Orange 5mm LED (eg RS 260-9514)
LED3, LED5	Green 5mm LED (eg RS247-1678)

Connectors

J1	9-way male right angled D type (Farnell 150-750)
PL1	26-way right angled IDC header (Farnell 249-245)
PL2, PL4a+b, PL9	2-way Molex header (PL4 in 2 parts) (Farnell 143-139)
LED1-LED5	2-way Molex header (see text) (Farnell 143-139)
PL3	3-way Molex header (Farnell 143-140)
PL5	5-way Molex header (Farnell 146-698)
PL6	6-way Molex header (Farnell 143-142)
PL7, PL8	Dual 8-way pin header (Farnell 672-063)
PL10	2-way pin header/wire link (see notes)

Capacitors

C1	100uF electrolytic capacitor 16V
C2, C3	33pF or 47pF ceramic capacitor (see text)
C4	2u2 tantalum capacitor 10V
C5 - C9	10-100nF polyester or ceramic capacitor

Miscellaneous

TP1-TP9	2144 or 2145 1mm dia. Veropin (see text)
PL7,PL8,PL9	Shorting links for headers
U3	20-way DIL socket
U6	18-way DIL socket
U1, U2	16-way DIL socket
U5	14-way DIL socket
PL1	M2.5 screws and nuts
XTAL1	4MHz crystal or resonator (see text)
SW1	8-way dil switch (Farnell 145-432)
SW2	click switch (Farnell 151-143)

Suppliers:

R. A. Coward, 22 Alexandra Park, Queen Alexandra Road, High Wycombe, Bucks HP11 2HJ. Email: rcoward@dev.madge.com.

Greenweld Electronic Components, 27E Park Road, Southampton, SO15 3UQ. Tel. 01703 236363 Fax 01703 236307.

Farnell Electronic Components: Canal Road, Leeds, LS12 2TU. Tel 0113 263 6311.

Electromail: PO Box 33, Corby, Northants NN17 9EL. Tel 01536 405555.

Tracking Filter Effects Unit

This unusual guitar effect reminiscent of a Theramin uses a phase locked loop and switched capacitor filter to track changes in the guitar's pitch.

Robert Penfold

I am always reluctant to claim that anything is new, particularly when dealing with guitar effects, but this tracking filter effect is certainly one that I have not encountered previously. Its primary effect is to filter the guitar so that it has a much more pure sound. It does not quite filter the signal to the point where a sinewave is obtained, but it comes quite close to achieving this! The purity of the sound, together with a slight tremolo effect as the filter initially locks onto each note from the guitar, gives a weird and wonderful effect. Although there is no slide from one note to the next, the sound is reminiscent of a Theramin, or a synthesiser set up to give that sort of effect. The unit has a second mode of operation which "notch" filtering. This results in the fundamental frequency disappearing as the filter locks onto each note from the guitar. To my ears at any rate, the "notch" effect is less musical than the lowpass type, but others might not agree.

Keeping track

Repetitive waveforms consist of a fundamental frequency plus harmonics (multiples) of that frequency. A sinewave is a tone where harmonics are totally absent, giving this type of waveform its characteristically pure sound. With all other repetitive waveforms at least one harmonic is present, and with many waveforms there are numerous strong harmonics. Harmonics tend to be strongest with waveforms that have fast leading and/or trailing edges, such as squarewaves and pulse types. In the world of analogue sound synthesis it is quite normal to use filtering to modify one waveform and produce another. For example, applying heavy lowpass filtering to a squarewave type can produce something approximating to a triangular signal.

This type of sound manipulation is easy with an analogue synthesiser because both the tone generators and the filters are voltage controlled. With some simple adjustments of the synthesiser's controls the filter will automatically track the tone generator. This ensures that the effect remains constant over a wide range of pitches. Matters are more difficult when this type of filtering is applied to a guitar, because there is no easy way of making the filter track changes in the guitar's pitch. Without accurate tracking neither the "notch" nor the lowpass filter effects are usable over a range of more than a few semitones. Although there is no way of producing a really simple tracking filter, a circuit of this type does not need to be particularly complex either. Tracking filters are actually quite common in test equipment and communications.

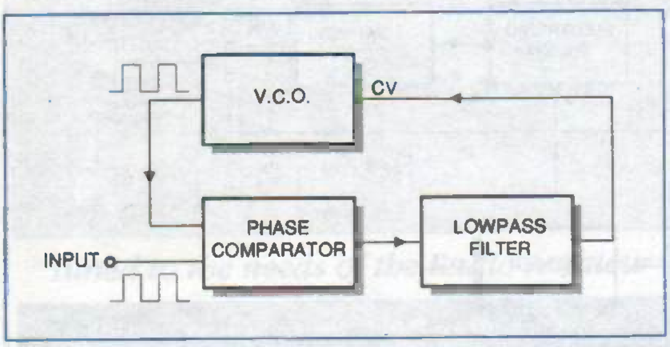


Figure 1: the simple arrangement used in a phase-locked loop

Phased locked loop

There are purely analogue approaches to the problem, but most circuits of this type are based on a phase-locked loop (PLL). A phase-locked loop uses the arrangement shown in the block diagram of **figure 1.** The basic action of the circuit is to maintain the output of the voltage-controlled oscillator (VCO) at the same frequency has the input signal, and also in phase with that signal. The output of the VCO and the input signal are applied to the inputs of a phase comparator. The output signal from the phase comparator consists of a pulse stream, and these pulses are smoothed by a lowpass filter to produce the control voltage for the VCO. If the VCO lags behind the input signal in phase of frequency, the output voltage from the lowpass filter goes much higher. Conversely, the output voltage

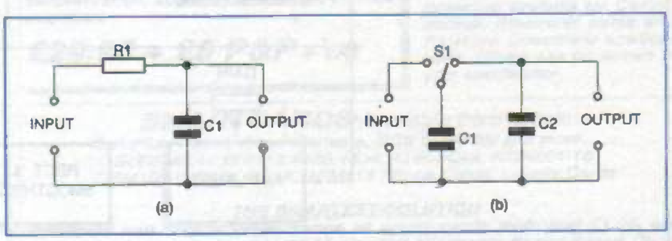


Figure 2: (a) conventional C-R low-pass filter and (b) the switched capacitor equivalent

from the lowpass filter goes much lower if the output from the VCO leads the input signal in terms of phase, or is at a higher frequency. This locks the phase and frequency of the VCO to the input signal by means of a conventional negative feedback action.

On the face of it, this is all very clever but does not help to produce a tracking filter. However, together with some additional circuitry a phase-locked loop can provide an extremely effective tracking filter. The other main ingredient is a switched capacitor filter. A conventional C-R lowpass filter uses the arrangement shown in **figure 2a**, and the switched capacitor equivalent of this is shown in **figure 2b**. In a practical switched capacitor filter the switch is an electronic type and a clock oscillator controls it. In the C-R version of the filter the resistor limits the rate at which current and flow into and out of the capacitor. If the input voltage changes slowly the signal across the capacitor is virtually the same as the input signal, but at higher frequencies the capacitor cannot charge and discharge fast enough to accurately track the input potential. The higher the input frequency, the lower the output amplitude will be for a given input level. The ultimate attenuation rate for a single stage filter is just six decibels per octave, which means that each doubling of the input frequency halves the circuit's gain.

The switched capacitor filter operates in a similar fashion. If the input voltage rises, C1 charges to this new potential when the switch is set to the left, and discharges into C2 when the switch is set to the opposite position. If the input potential falls, C1 charges from C2 when the switch is in the right hand position, and discharges into the input circuit when SW1 is set to the left. In the practical filter the value of C1 is made very much lower than that of C2, and it therefore takes several switch cycles for the output voltage to respond to changes in the input potential. Like the resistor in a C-R filter, the switch and the capacitor restrict the rate at which current can flow between the input and output of the filter. The crucial factor in this case is that the faster the switch is operated the higher the cut-off frequency of the filter. The ratio of the clock frequency to the cut-off remains constant over a wide frequency range. In practical switched capacitor filters the circuit values are normally arranged to give a ratio between the clock frequency and cut-off frequency that is either 50 to 1 or 100 to 1.

Getting it together

The block diagram of **figure 3** shows how a phase-locked loop and a switched capacitor filter are used to produce the tracking filter used in this effects unit. A phase-locked loop is very good at handling input signals that contain substantial amounts of noise. However, it is still necessary to produce a reasonably "clean" input signal if the circuit is to lock quickly and reliably onto the input signal. Guitars represent awkward signal sources for this type of thing due to the strong harmonic content of their output signals, and the changes that occur during the course of each note. Some signal conditioning is therefore required ahead of the phase-locked loop.

The first stage is simply a preamplifier with a preset gain control. This stage merely acts as a buffer when the unit is used with high-output pick-ups, but with low-output types it is used to boost the signal by a factor of about 10. The next stage provides further voltage gain, together with a substantial amount of lowpass filtering. Although only a single stage filter is used, the cut-off frequency is set quite low so that the harmonics on most input signals are severely attenuated. The signal is then applied to a trigger circuit that provides a (more or less) squarewave output signal.

Unaided, the phase-locked loop will provide a clock signal for the switched capacitor filter that is equal to the input frequency. In this case, we require a clock frequency that is one hundred times input frequency, and this is achieved by including two divide by 10 circuits between the output of the VCO and the input of the phase comparator. The phase-locked loop still operates in much the same way as normal, but it is the signal at the output of the divider chain that is kept in phase with the input signal. This provides the required clock signal from the output of the VCO, at one hundred times the input frequency. This is used as the clock signal for a four-stage switched capacitor filter that can operate in the lowpass and "notch" modes. A bandpass output is also available, but is not used in this case as it provides much the same effect as the one available at the lowpass output. The output signal from a switched capacitor filter is stepped type that is effectively modulated slightly by the clock signal. A lowpass filter at the output of the unit removes the stepping to produce a "clean" output signal.

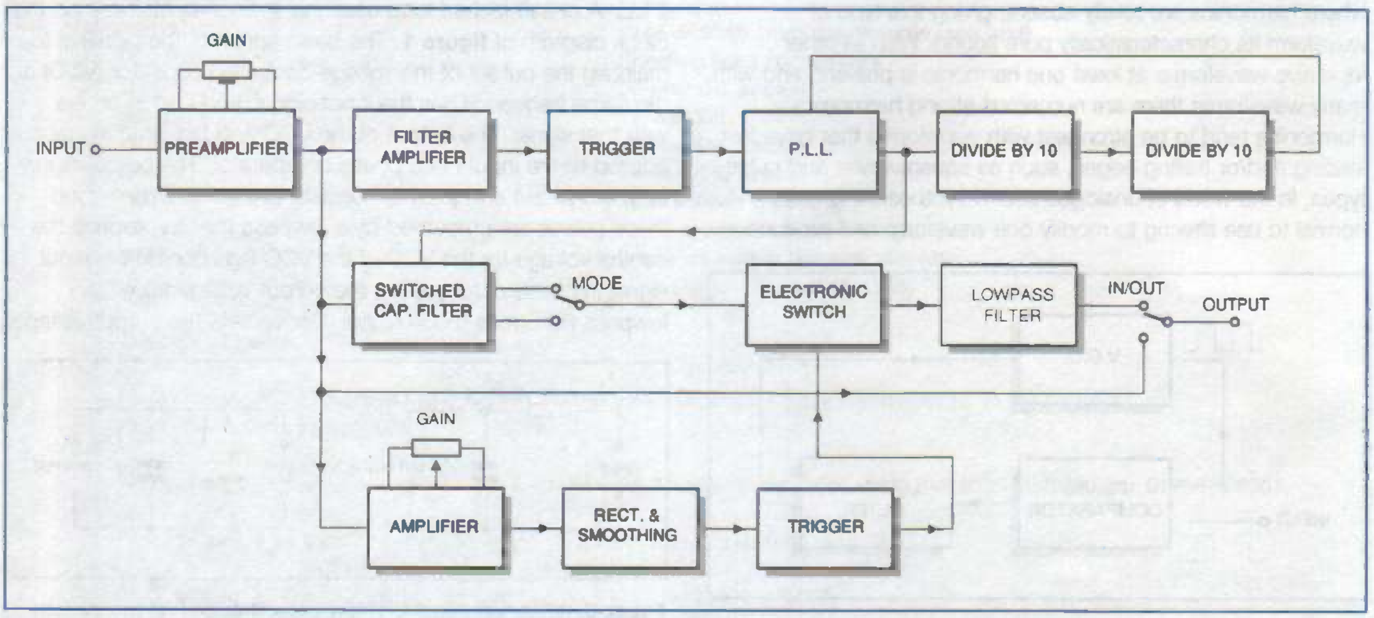


Figure 3: the block diagram for the Tracking Filter Effects Unit

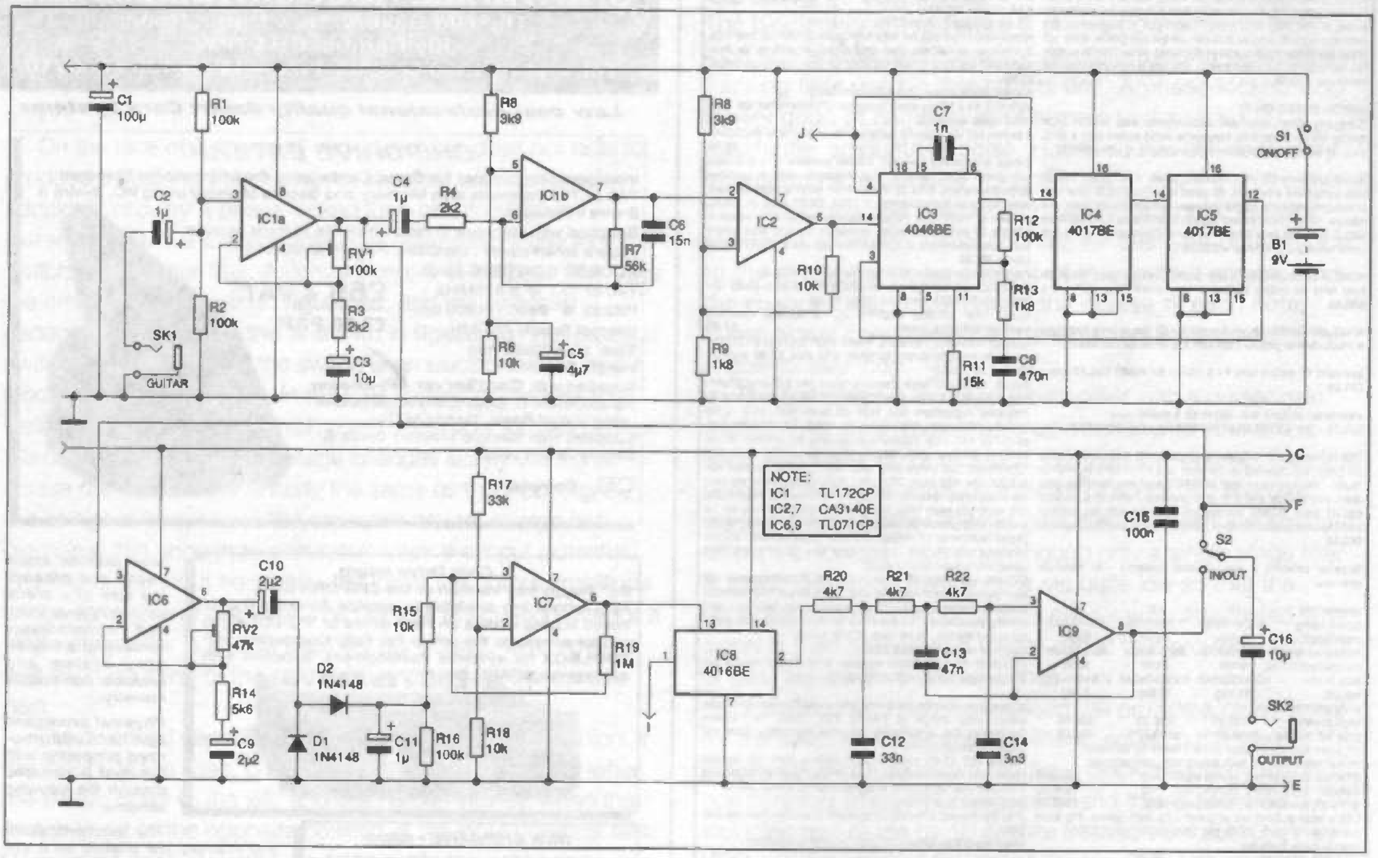


Figure 4: the circuit of the Tracking Filter Effects Unit

In practice there is a slight flaw with this arrangement in that it works very well when a reasonably strong input signal is present, but it gives unpredictable results when there is little or no input signal. What tends to happen is that the VCO drops to a low frequency as the input signal drops below a usable level, giving slight but noticeable audio tones and noises on the output. The easiest solution to this problem is to include a simple noise gate action in the circuit. An electronic switch is included between the output of the switched capacitor filter and the input of the lowpass filter. The control signal for the electronic switch is generated by first amplifying the input signal, and then rectifying and smoothing it to produce a DC output level that is roughly proportional to the strength of the input signal. This voltage is used to operate a simple trigger circuit. If the input level is high enough, the output voltage from the smoothing circuit will activate the trigger circuit, which will then turn on the electronic switch. When the input signal drops below a certain threshold level, there is an inadequate voltage to operate the trigger circuit, and the electronic switch is turned off.

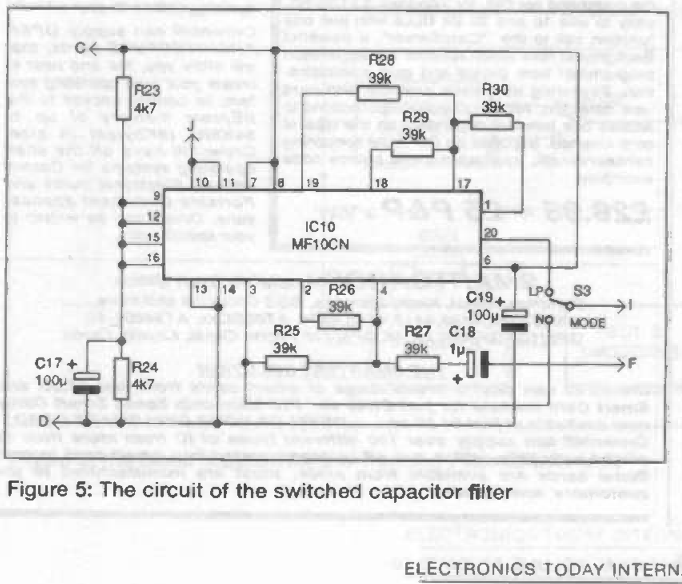


Figure 5: The circuit of the switched capacitor filter

This gives the required noise gate action, and the gain control in the amplifier stage enables a suitable threshold level to be set.

The circuit

The main circuit diagram for the tracking filter effects unit appears in **figure 4**, and the circuit for the switched capacitor filter is shown in **figure 5**. Starting with the main circuit, IC1a is used in the preamplifier stage and operates as a straightforward non-inverting mode amplifier. It provides an input impedance of about 50k, which is a good match for most guitar pickups. The voltage gain varies from the unity with RV1 at minimum resistance to about 46 times with this preset at maximum value. Output levels tend to vary substantially from one guitar to another, but the gain range available from RV1 should enable the unit to work well with any normal electric guitar. IC1b is used in the amplifier/filter stage, and it operates in the inverting mode. The lowpass filtering is obtained by including C6 in the negative feedback loop. At low audio frequencies, IC1b has closed loop voltage gain of about 25 times, but at high frequencies C6 produces increased feedback and reduces the gain of the circuit.

IC2 acts as a conventional inverting trigger circuit. R8 and R9 bias the non-inverting input to about one-third of the supply potential, which is lower than the (approximately) half supply output voltage from IC1b. Under standby conditions the output of IC2 therefore goes low, but on negative output half cycles from IC1b the input voltage goes below one-third of the supply voltage and the output triggers to the high state. Although the input signal to the trigger will normally be to some extent clipped, and will always be heavily filtered, it will almost certainly contain some irregularities. R10 is therefore used to provide a substantial amount of hysteresis in an attempt to further combat these irregularities.

The phase-locked loop is based on the CMOS 4046BE low-power phase-locked loop chip (IC3). The timing components for the VCO are resistor R11 and capacitor C7. The only other discrete components that are required are those in the single stage lowpass

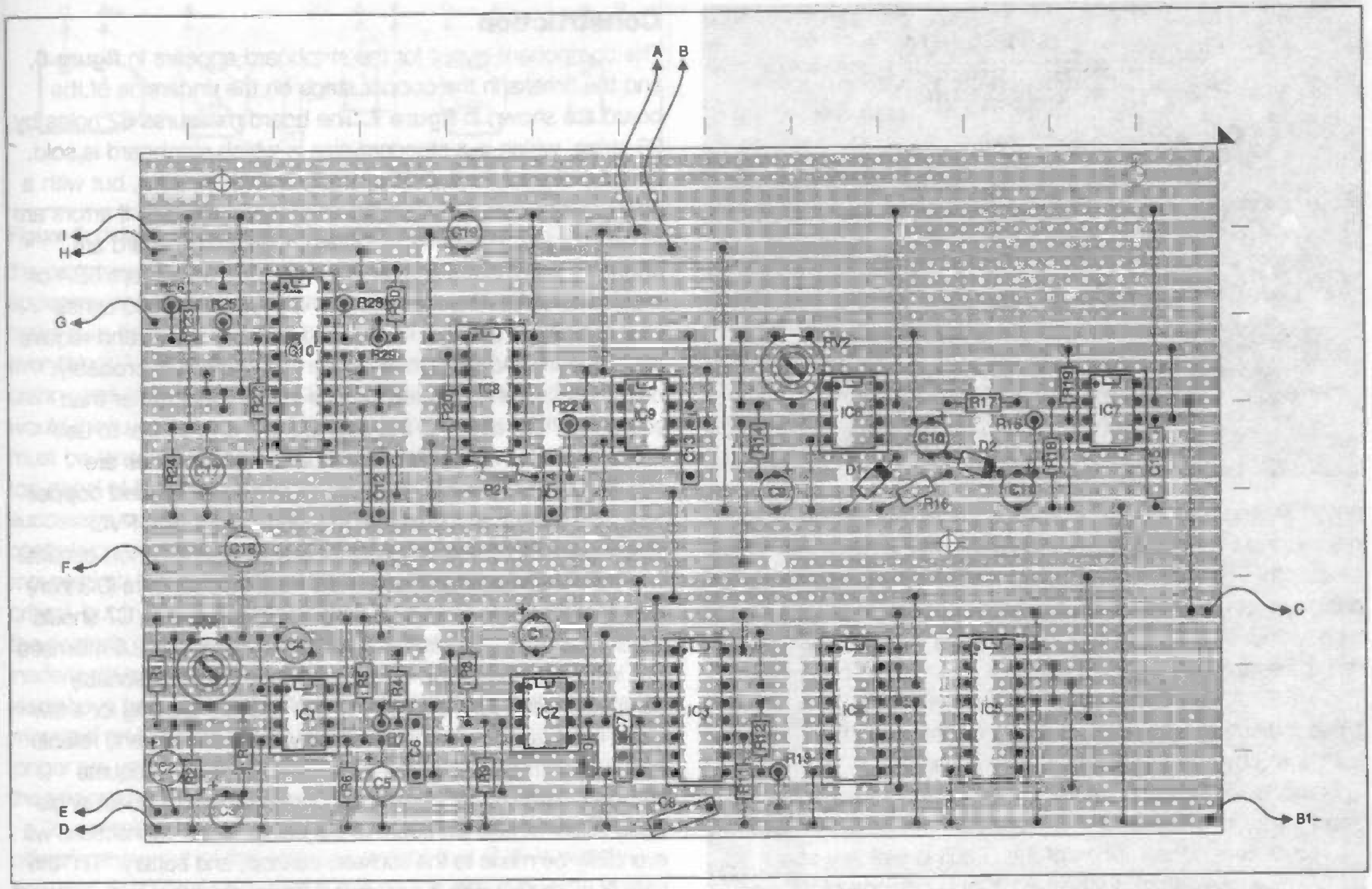


Figure 6: the component layout for the stripboard

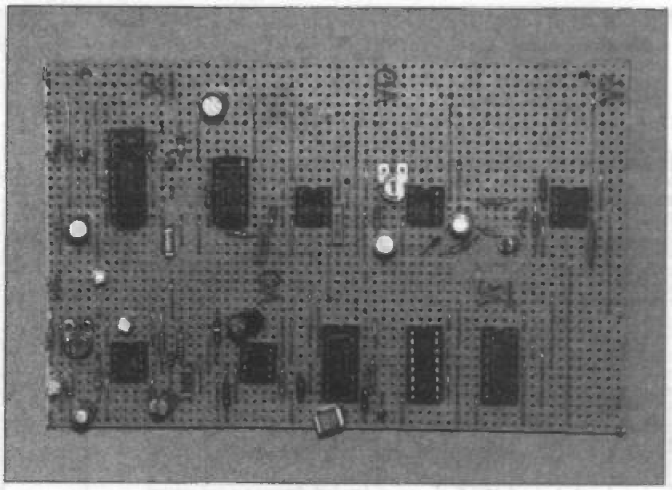
filter. These are R12 and C8, but there is an additional resistor in the filter (R13). This resistor serves no obvious purpose, and it would seem to do nothing more than increase the ripple level on the output of the filter. Without this resistor the phase-locked loop works well with a noise-free input signal, but in real-world applications the circuit does not lock reliably onto the input signal. Instead, it overshoots slightly one way then the other. The practical result in this application is a strong tremolo effect on the output signal. Including R13 in the circuit avoids this overshoot problem, and ensures that the circuit locks onto the input signal quite rapidly. A slight tremolo effect is generated at the beginning of each note, but this does not significantly detract from the effect, and if anything probably enhances it slightly.

The 4046BE phase-locked loop is rather unusual in that it has two phase comparators. The one that has its output at pin two provides normal operation with the VCO operating at its centre frequency with no input signal. In this case it is the other phase comparator that is utilised, and this has its output at pin 13. Under standby conditions this comparator allows the output frequency to drop to the point where the VCO cuts off. This second comparator has the advantage of enabling the phase-locked loop to operate over a much wider frequency range, which is important in an application of this type where the input frequency can vary over several octaves. IC4 and IC5 are CMOS 4017BE one of 10 decoders, but in this application they are both used as simple divide by 10 circuits. They are driven by the output of the VCO at pin four of IC 3, and the divided by 100 signal is fed to the phase comparator inputs at pin 3.

The amplifier at the input of the noise gate is based on IC6, which is a non-inverting mode circuit. Its voltage gain can be varied from unity with RV2 at minimum resistance to just under ten times with this control at maximum resistance. This enables the threshold level to be set high enough to remove the unwanted noises, but low enough to give a reasonable sustain characteristic to the output signal. Capacitor C9 couples the output of IC6 to a simple half wave rectifier and smoothing circuit based on D1 and D2. Due to the low source impedance the smoothing circuit has a very fast attacked time, and the gate therefore opens almost instantly when a new note is played. In order to produce a properly smoothed output signal the decay time must be much longer, but it is still kept reasonably short so that the gate responds quickly when the output from the guitar decays to a low level. IC7 is used in the trigger circuit, which is a conventional non-inverting type. The hysteresis provided by R19 helps to avoid instability when the output voltage from the smoothing circuit is close to the threshold level.

The electronic switch in the gate circuit is one of the four CMOS analogue switches in IC8. No connections are made to the other three switches. The output of IC8 is coupled to a third order lowpass filter that has IC9 as the buffer amplifier. With the clock circuit operating at 100 times the input frequency, the clock frequency will be at the upper end of the audio range when low notes are played on the guitar. The cut-off frequency of the lowpass filter therefore has to be set quite low so that audible breakthrough of the clock signal is avoided. The cut-off frequency of the filter is at approximately 2.5 kHz. It is important that the gate circuit does not introduce large switching glitches. It effectively forms a simple "hold" circuit in conjunction with the lowpass filter, and this helps to avoid "click" sounds as the gate switches on and off. SW2 enables all the filtering to be bypassed, and acts as the effect in/out control.

Turning now to the switched capacitor filter, this is based on the MF10CN dual switched capacitor filter chip (IC10). This has four filter stages used in two second order state-variable filters. The lowpass filtering is obtained by using the two filters in series, giving an attenuation rate of 24dB per octave. The



notch filtering is provided by the first state-variable filter, and the second filter is unused in this mode. Mode switch SW3 selects the required output signal. The MF10CN is primarily designed for use with dual (+/-) 5-volt supplies, but it can also work with a single supply rail if some of its inputs are biased to half the supply voltage. R23 and R24 provide this bias potential. The MF10CN can operate with the clock signal at 50 or 100 times the cut-off frequency, and in this case the 100 to 1 mode is selected by connecting pin 12 to the mid-supply bias circuit. This mode keeps the clock frequency as high as possible, which helps to avoid audible clock breakthrough at the output.

The current consumption of the circuit is typically about 15 to 17 milliamps. Although the MF10CN is designed for operation with a 10-volt supply, it actually operates quite well from a 9-volt battery. Due to the fairly high current consumption it is best to use a "high-power" PP3 size battery, or six AA cells in a holder. AA cells represent the cheaper means of powering the unit.

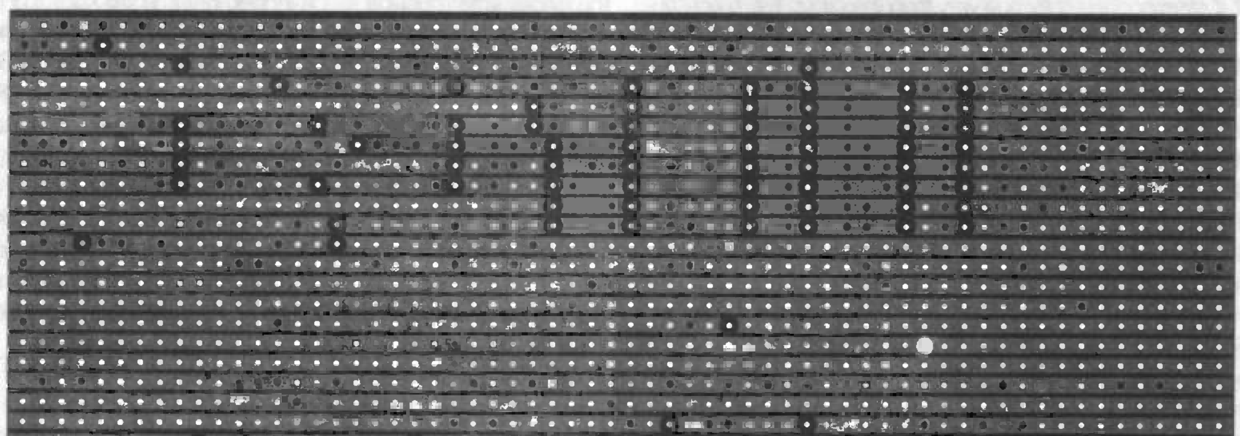
Construction

The component layout for the stripboard appears in **figure 6**, and the breaks in the copper strips on the underside of the board are shown in **figure 7**. The board measures 62 holes by 39 strips, which is a standard size in which stripboard is sold. Construction of the board is largely straightforward, but with a board of this size it is essential to proceed carefully if errors are to be avoided. The three mounting holes in the board are about 3.2 millimetres in diameter, and they will accept 6BA or metric M3 bolts. The MF10CN, CA3140E, and 4000 series CMOS devices are all vulnerable to static charges, and require the standard anti-static handling precautions. It is probably best to fit all the integrated circuits into holders rather than soldering them direct to the board, but it is essential to use holders for the MOS devices. A number of link-wires are required, and these are made from 24 swg enamelled copper wire. It is advisable to insulate the longer links with PVC sleeving so that there is no risk of any accidental short circuits.

Provided the polyester capacitors have 7.5 millimetre (0.3 inch) lead spacing they should fit into this layout quite easily. C7 should either be a Mylar capacitor or a polyester type having 2.5 millimetre (0.1 inch) lead spacing. In order to keep the layout reasonably compact it has been necessary to use vertical mounting for a few of the resistors. This method is somewhat less strong and reliable than horizontal mounting, but it should be perfectly adequate provided the component leads are cut very short. Connect single-sided solder pins to the board at the points where connections will eventually be made to the sockets, controls, and battery. "Tin" the tops of these pins with a generous amount of solder.

The circuit board is slightly too large to permit the unit to be built as a small foot-pedal unit, but it can be housed in a medium size aluminium box or an instrument case. I would not recommend using a plastic case for this type of project. A steel instrument case with an aluminium front panel is used to house

Figure 7: the underside view of the stripboard



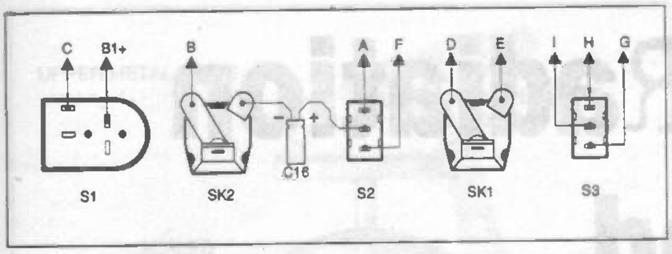


Figure 8: details of the hard wiring (use in conjunction with figure 6)

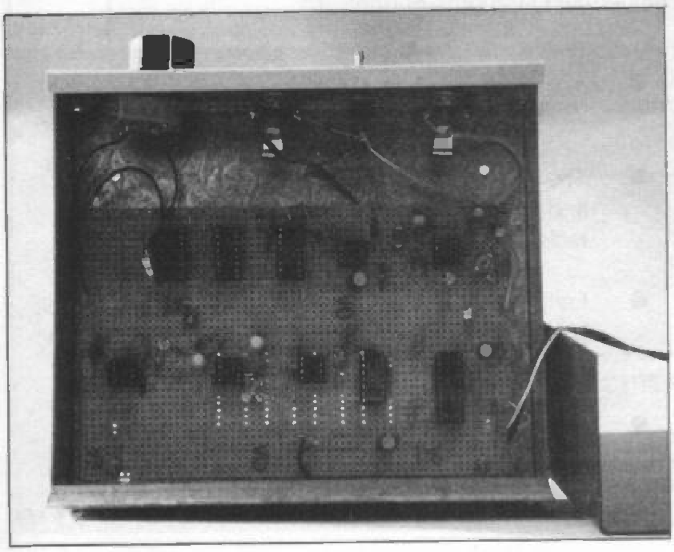
the prototype. This is tough, but also gives a very neat appearance. If the unit will be powered from an AA battery pack, make sure that you choose a case that can accommodate everything. A PP3 size battery will fit into practically any nook or cranny, but six AA cells in a holder require more space than you would think. If SW2 and (or) SW3 are to be foot operated, they must be reasonably tough pushbutton switches mounted on the top panel of the case. They can be either momentary action or successive operation switches, depending on the method of control you desire. The other controls and the sockets are mounted on the front panel of the case. The general layout is not critical, but try to have the sockets reasonably well spaced from the controls. Jack plugs are quite large, and it is and with inadequate spacing the controls might be difficult to use once leads have been connected to the sockets. The circuit board is mounted on the base panel, and spacers about 6 millimetres or longer are used on the mounting bolts to keep the connections on the underside of the board well clear of the metal case.

To complete the unit, add the hard wiring (**figure 8**). This offers nothing out of the ordinary, except that C16 is wired between SW2 and SK2, and is not on the circuit board. There should be no difficulty here provided the ends of its leadout wires are "tinned" with solder prior to wiring it into position. It is advisable to use a screened lead to connect SK1 to the circuit board. This should minimise any stray pickup of the clock signal at the input of the circuit.

Adjustment and use

The unit connects between the guitar and the guitar amplifier using standard screened jack leads. Start with RV1 and RV2 at roughly central settings. With SW2 set to the "Out" position, adjust RV1 for the highest resistance (most clockwise setting) that does not result in any clipping and noticeable distortion on the output signal. With low output guitars there will be a significant amount of voltage gain through the unit, and the volume control of the guitar amplifier will have to be backed-off accordingly. Next switch in the effect using SW2 (either mode will do). With RV2 set fully counter-clockwise there will probably be a lack of sustain from the guitar, and it might be difficult to get much output at all. Advancing RV2 in a clockwise direction should improve matters, but do not advance it so far that notes sustain beyond the point where the phase-locked loop locks reliably. If RV2 is given a suitable setting when playing a high note, good results should be obtained on all other notes.

Obviously the unit can only track one frequency at a time, which means that your playing has to be strictly one note at a time. The more "cleanly" you play the notes, the more quickly and reliably the unit will track from note to note. If there is a tendency for the filter to jump an octave high on some notes, increasing the value of C6 to about 33n should cure the problem. However, this will reduce the ability of the unit to sustain high notes (making it necessary to readjust RV2), so do not make C6 any higher in value than is really necessary.



PARTS LIST for the Tracking Filter Effect

Resistors

(All 0.25 W 5 percent carbon film)

R1,2,12,16	100k
R3,4	2k2
R5,6,10,15,18	10k
R7	56k
R8	3k9
R9,13	1k8
R11	15k
R14	5k6
R17	33k
R19	1M
R20,21,22	4k7
RV1	100k min hor preset
RV2	47k min hor preset

Capacitors

C1,17,19	100u 10V radial elect
C2,4,11,18	1u 50V radial elect
C3,16	10u 25V radial elect
C5	4u7 50V radial elect
C6	15n polyester
C7	1n Mylar
C8	470n polyester
C9, C10	2u2
C12	33n polyester
C13	47n polyester
C14	3n3 polyester
C15	100n ceramic

Semiconductors

IC1	TL072CP
IC2, IC7	CA3140E
IC3	4046BE
IC4, IC5	4017BE
IC6, IC9	TL071CP
IC8	4016BE
IC10	MF10CN
D1, D2	1N4148

Miscellaneous

SW1	Rotary on/off switch
SW2, SW3	SPDT (2 off - see text)
SK1, SK2	Standard jack socket (2 off)
B1	9 volt (PP3 or 6 x AA cells in holder)

Metal case about 180 x 150 x 50mm, 0.1 inch pitch stripboard 62 holes by 39 strips, 8-pin dil holder (5 off), 14-pin dil holder, 16-pin dil holder (3 off), 20-pin dil holder, battery connector, wire, solder, etc.

Ionising Radiation and Ionisation Chambers

Douglas Clarkson

While the techniques for measuring levels of ionising radiation have multiplied considerably, the core of accurate dosimetry remains with the various types of ionisation chamber.

Thus the series of National and International standards relating to dosimetry of ionising radiation specifically relate to the performance of ionisation chambers of standard design within known fields of ionising radiation.

It is easier to maintain the physical characteristics of an ionisation chamber than, for example, a solid state detector incorporating a semiconductor whose properties could change with exposure to radiation.

In the interaction of electromagnetic radiation with the human body, there are levels of photon energy that can induce ionisation in, for example, air and tissue, and photon energies which are not energetic enough to do so. Generally the threshold of photon energy for ionisation is around 5 to 25 eV (electron volts). The fact that ionising radiation can induce cellular damage and in particular can damage DNA that makes the accurate measurement of ionising radiation so important.

It is not widely appreciated that even though non-ionising radiation such as ultra violet does not actually induce ionisation, these photons still have enough energy to degrade DNA in living cells by the direct coupling of energy to the individual chemical bonds within strands of DNA. Fortunately, the effect normally only takes place in the very superficial layers of skin.

The early days

One of the most basic items of equipment used to monitor levels of ionising radiation was the gold leaf electroscope (**figure 1**). Initially a nylon rod would be charged up with a piece of fabric and the rod brought into contact with the upper plate of the unit. This would cause a charge of opposite polarity to be induced on the inner conductive plate, which was in turn connected to a suspended gold leaf whose two halves would move apart as a measure of the initial charge content of the device.

As ionising radiation entered the enclosure, charges would begin to neutralise the field inside the electroscope and the angular separation of the leaf would decrease with time. The activity of the source would be related to the rate at which the angle of separation of the two gold leaves decreased. The early quantitative measurements on radioactivity took place on equipment such as this. These devices were still in use at Glasgow University in undergraduate laboratories in the late 1960s.

The modern challenge

Using modest constructional care and operational amplifiers of high quality as regards leakage current, it is possible, in theory, to make an ionisation chamber to detect ionising radiation of the order of background levels. Some of the theory of ionisation chambers is helpful in order to appreciate the challenge of detection and the usefulness of such techniques in investigating the environment.

At its most basic, an ionisation chamber can be represented in **figure 2**. Where ionising radiation generates ion pairs in air, the established electric field will tend to sweep the charges onto the plates of the chamber. The generalised response of the chamber as a function of electric field strength is summarised in **figure 3**. On the first plateau at around a field strength of 100 V/cm almost all of the ion pairs being generated will be collected. At higher field strengths current

- The threshold of photon energy capable of inducing ionisation in, air and tissue, is around 5 to 25 eV
- The fact that ionising radiation can damage tissue and DNA makes accurate measurement of ionising radiation Important
- Early quantitative measurements on radioactivity took place using gold leaf electroscopes. These were still in use in undergraduate labs in the late 1960s
- High quality op-amps make it possibly, in theory, to detect naturally-occurring background levels of ionising radiation

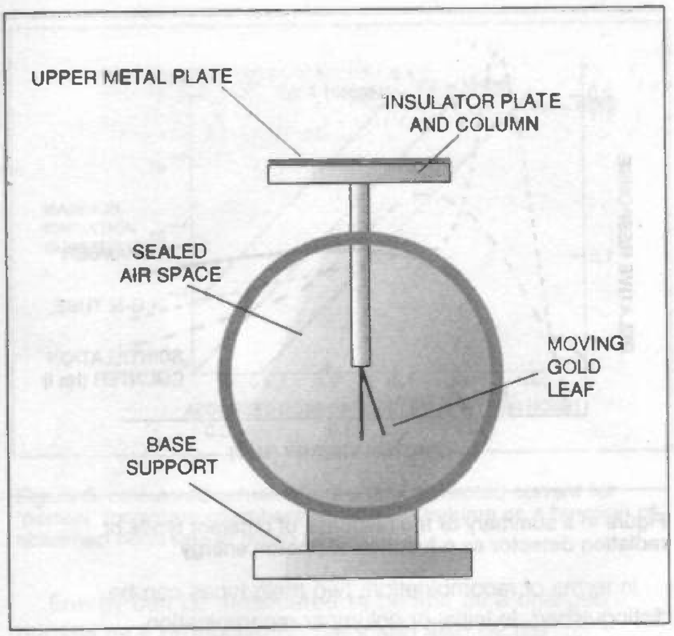


Figure 1: the basic structure of gold leaf electroscope

Multiplication takes place as electrons pick up sufficient energy to cause secondary ionisation of the gas. This is the mode of operation of the proportional counter. At even higher levels of field strength, however, avalanche breakdown takes place as utilised in the Geiger-Muller tube. With the chamber functioning as an ionisation chamber or as a proportional counter, the output signal of effectively collected charge is proportional to the incident level of ionisation activity. In the Geiger-Muller mode, however, the information has been degraded to that of counts and the relative contribution of each initiatory pulse of radiation is largely lost. **Figure 4** summarises the typical relative response of different types of radiation detection as a function of photon energy.

Detection modes

The basic options for measuring the output of an ionisation chamber are to integrate its charge or to produce a direct readout of radiation activity at any time. The specific circuits are shown in **figure 5a** (direct) and **figure 5b** (integration).

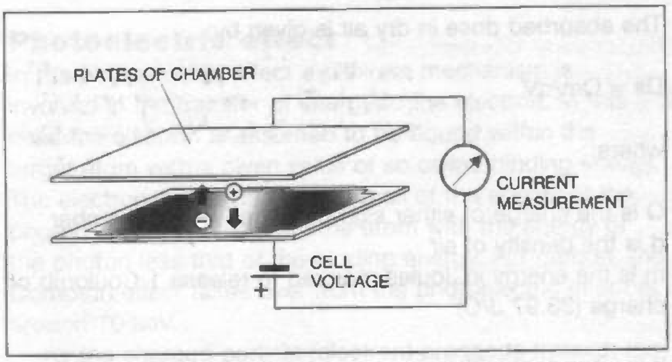


Figure 2: the basic design of ionisation chamber

Where, for example, the radiation output of an x-ray set is being determined, the integration mode will be selected since essentially the system will be integrating only for the time during which the x-ray set is activated.

One of the earliest measurements of levels of radiation was that of exposure, defined in units of Roentgen and equivalent to the amount of radiation that would produce 2.58 x 10^{-4} Coulombs of charge per kg of air under standard conditions. This is also equivalent to 1.61 x 10^{15} ion pairs per kg, equivalent to 0.00869 J/kg of air. The advantage of measuring exposure was the ability to measure the relative 'activity' of radiation through the mechanism of air ionisation.

The Radiation Absorbed Dose relates to the actual energy absorbed (in Joules) per kg by a specific medium. The unit of absorbed dose is that of the Gray. Working from the definition of the Roentgen, an exposure of 1 Roentgen in air will deposit 0.008690 J/kg, which is equivalent to an absorbed dose of 0.00869 Gy in air.

Dose equivalent

The dose equivalent in units of Sievert is given by :

dose equivalent = absorbed dose (Gy) x Q x N

where Q is the quality factor which reflects the ability of the particular type of radiation to initiate tissue damage. For the present N is assigned a value of 1 and reflects the possible effect of dose rate or system of fractionation of the radiation into smaller doses of radiation.

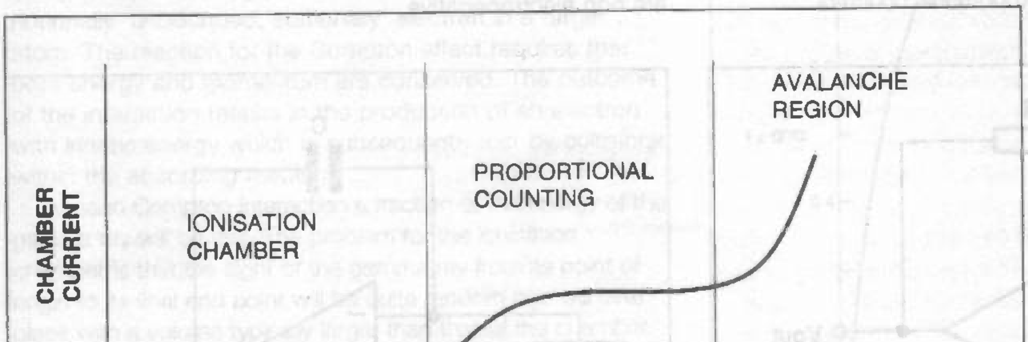


Figure 3: response of ionisation chamber as a function of established electric field. At increasing field value the chamber enters a region of proportional counting followed by an avalanche region as used in Geiger-Muller configuration

For x-rays, gamma rays and electrons the value of Q is unity and for alpha particles Q has a value of 20.

The key property of an ionisation chamber will be its current sensitivity. The detection of ionisation currents of the order of femto-amps (10^{-15}) associated with detection levels of the order of background levels is a severe limitation. When an ionisation chamber is used to measure the activity of an x-ray exposure, the peak current will be many thousand times that of background.

The absorbed dose in dry air is given by:

Da = Qm/dV

where:

Q is the charge of either sign produced in the chamber
d is the density of air
m is the energy in Joules required to release 1 Coulomb of charge (33.97 J/C)

It is important initially to determine the typical equivalent current produced in the chamber at a given rate of absorbed dose such as 1 micro Gray per hour for a range of sizes of ionisation chamber.

The ionisation current, I, is given by:

I = Da d V 0.000001/m 3600 A

where Da is the value of rate of absorbed dose in Micro Gray per hour.

Assuming a nominal value of density of 1.2 kg/m3, **figure 6** indicates the value of maximum current - assuming all released charge is in fact collected - for a range of values of absorbed dose rate and size of chamber. This approach provides a useful way of predicting the sensitivity of an ionisation chamber, although each chamber has to be individually calibrated against known input radiation field parameters.

With a lower limit of absorbed dose due to background radiation of 0.1 micro Gy per hour, it is only with relatively large chambers of capacity several litres and above that detection of background levels is possible using even ultra low bias current operational amplifiers.

Recombination Factors

Figure 7 indicates the typical variation of the ratio of collected current to produced current as a function of ionisation chamber potential. It is not possible, however, within the function of the ionisation chamber, to produce total collection by increasing the field strength, since with increased field strength free electrons acquire sufficient kinetic energy during their mean free path to ionise the next atom encountered - which is the effect exploited in proportional counters.

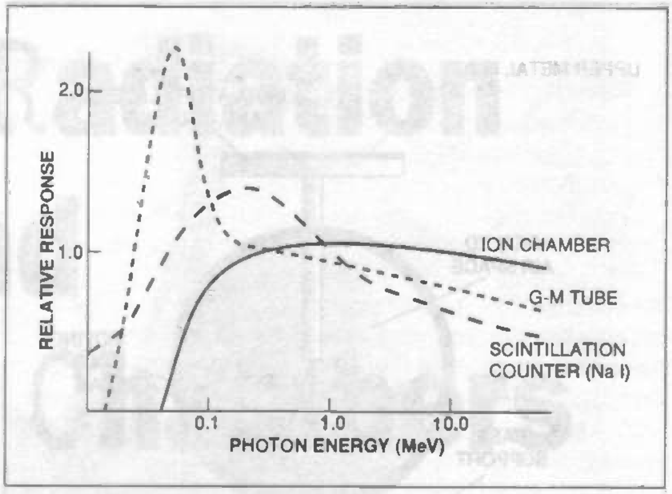


Figure 4: a summary of the response of different types of radiation detector as a function of photon energy

In terms of recombination, two main types can be distinguished. In initial or columnar recombination, ion/electron recombination can take place where recombination takes place in relation to a specific charged particle track. This effect is primarily taking place due to the initial proximity of the charged species. In what is known as general or volume recombination, the effect is one of interaction between the opposing charge species as they make their way to the respective electrodes. This form of recombination has a component of dose rate dependence, since the greater the number of charge species per unit volume the greater the chance of recombination taking place.

There is also an influence if the radiation is pulsed or continuous.

The mobility of electrons is typically 1000 cm/sec per V/cm and that of a negative/positive ion around 1 cm/sec per V/cm. If the electron can be prevented from forming negative ions by attracting a neutral gas molecule, then the electron can be swept out of the chamber rapidly - thus preventing recombination from taking place. Some degree of attaching of electrons to gas molecules will take place in air which contains the gases oxygen and water vapour which are described as electronegative. Improved performance can be achieved by using pure forms of nitrogen and carbon dioxide or argon and helium which are non electronegative.

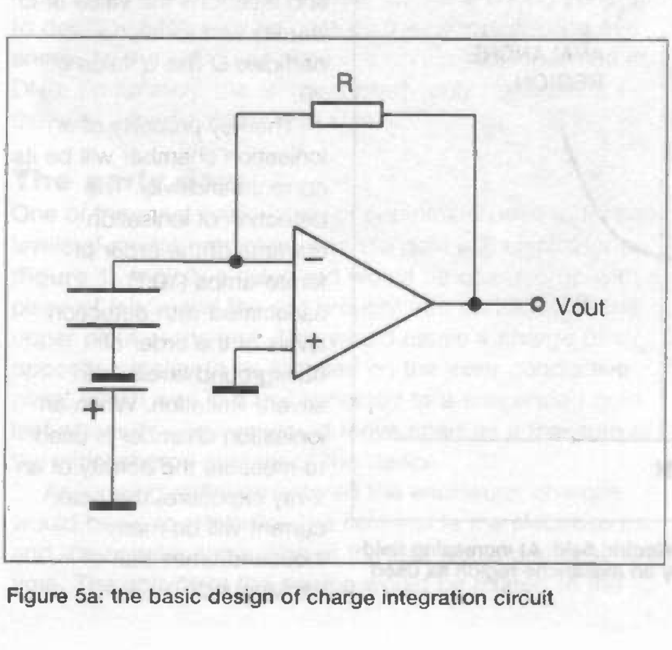


Figure 5a: the basic design of charge integration circuit

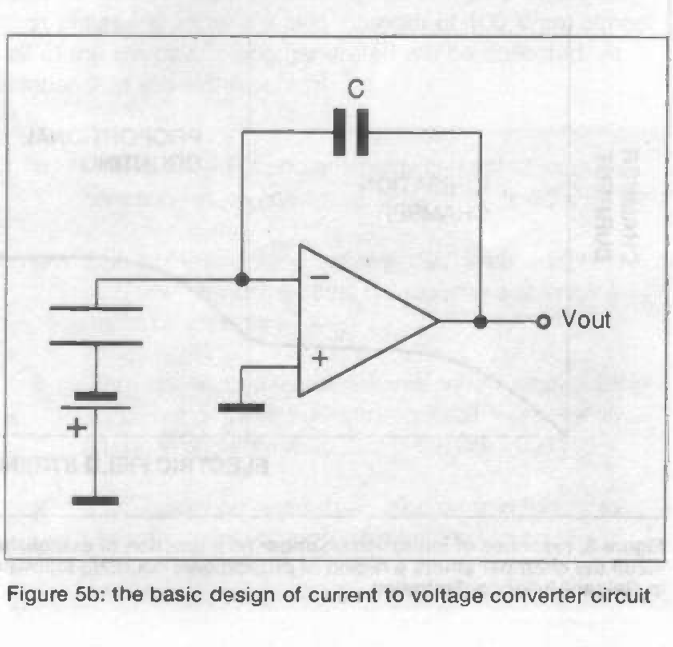


Figure 5b: the basic design of current to voltage converter circuit

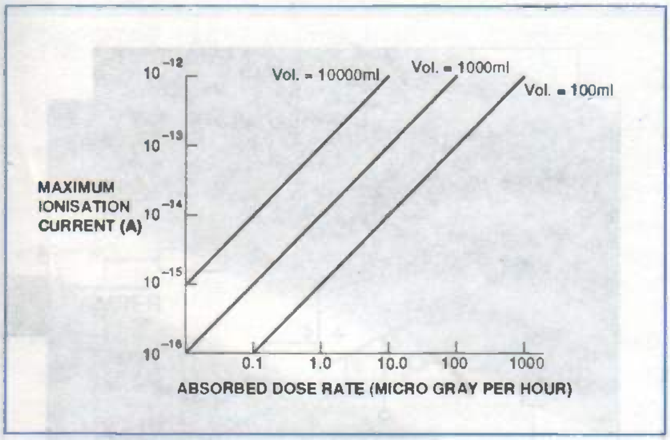


Figure 6: calculated values of maximum collected current for 'perfect' ionisation chambers of different volume as a function of absorbed dose rate in micro Gy per hour

Energy can be considered to be lost by a charged particle as it produces ion pairs and also by the mechanism of producing excitation of the energy levels of the atoms/ions. It is relevant, however, to refer to the mean energy typically in electron volts (eV) of a charged particle to produce an ion pair. This is given by the energy of the particle divided by the mean number of ion pairs produced.

In the example of helium, approximately 60 percent of initial particle energy is required to produce ionisation, 20 percent into excitation of electrons and 20 percent into heating the gas without further excitation or ionisation. In air a typical value or around 34 eV is used as a working value. For an electric field in excess of 50 V/cm, the collected charge will be approximately in excess of 70 percent.

Gamma Ray Interactions

The dose of background radiation which it is hoped to be detected by the ionisation chamber will originate from a range of sources. The main contribution will be that of gamma rays which lose their energy by the principal means of the Compton effect and the photoelectric effect. The Compton effect is essentially a 'billiard ball' interaction between the incoming photon of the gamma ray and a notionally 'unbounded, stationary' electron in a target atom. The reaction for the Compton effect requires that both energy and momentum are conserved. The outcome of the interaction results in the production of an electron with kinetic energy which is subsequently lost by collisions within the absorbing medium.

At each Compton interaction a fraction of the energy of the gamma ray will be lost. The problem for the ionisation chamber is that the flight of the gamma ray from its point of origin to its final end point will be quite random and will take place with a volume typically larger than that of the chamber.

The maximum energy which is transferred to the electron varies with incident energy and angle of scatter of the gamma ray. In general, Compton scattering can input large fraction of energy to the electron for large incident photon energies for a given scattering angle.

For a photon energy around 100 keV, however, values of energy transferred to electrons would be at most of the order of a few tens of keV. An electron receiving 10 keV would be able to produce a total of around 300 electron pairs if all the energy was translated into ion pair production.

Photoelectric effect

In the photoelectric effect a different mechanism is involved in the transfer of energy to the electron. In this case the electron is assumed to be bound within the target atom with a given value of so called binding energy. The electron proceeds to absorb all of the energy of the photon and is ejected from the atom with the energy of the photon less that of the binding energy. For carbon, the Compton effect takes over from the photoelectric effect at around 70 keV.

As the charged particle (electron) proceeds through the absorbing medium, the electron can interact with the target medium in a number of ways. In so called 'soft' collisions where the electron passes some distance from an atom, the coulomb field of the electron will tend to impart energy to the whole atom - resulting on occasions in the ejection of a valence electron.

About half of the energy of charged particles will be absorbed in this way. When the charged particle interacts with the atom directly, and approaches within an order of magnitude of the atomic diameter, a direct impact with an electron can take place - resulting in the emission of a delta ray.

On the track of a charged particle these can be seen as spurs on the main track of the particle. Although these collisions are much less frequent, a comparable amount of energy is dissipated in this way, since a large proportion of energy is lost in such a 'hard' collision. The resulting 'hole' in the electron structure of the atom will be filled by releasing of energy in the atom - resulting in the production of characteristic x-rays of the absorbing material.

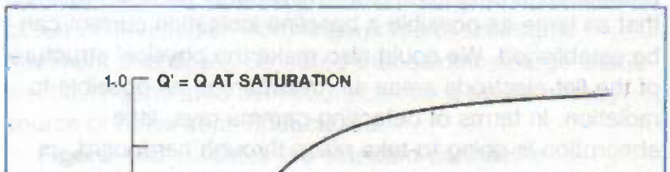


Figure 7: typical variation of the ratio of collected current to produced current as a function of ionisation chamber potential

Sources of natural radiation

The ionising component of cosmic radiation produces at sea level an average dose rate of 0.03 micro Sv per hour. This cosmic radiation originates within and outside our own galaxy and with a variable component of lower energy species from the sun. A value of around 0.05 micro-Gray per hour would be typical of the absorbed dose rate from this component. This component increases with altitude as the air gets thinner.

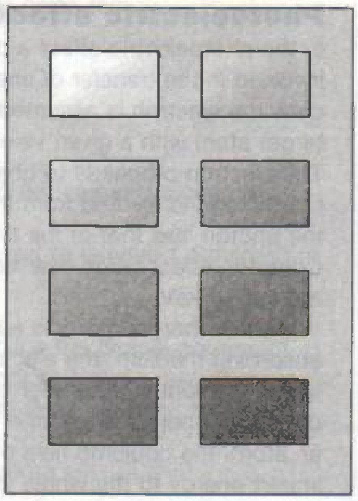


Figure 8: option of cut out windows on the surfaces of the ionisation chamber surfaces

Gamma background from the ground principally originates from potassium 40, uranium 238 and thorium series in ratio 35 percent, 25 percent and 40 percent respectively. There is generally slightly more activity at ground level than on the first floor of a house. Typical exterior absorbed dose rates will be around 0.05 micro-Gray per hour.

The total absorbed dose rate corresponding to background conditions will be around 0.1 micro-Gray per hour for 'average' conditions.

Constructing the chamber

At the heart of everything is the ionisation chamber. The temptation is to make its volume as large as possible so that as large as possible a baseline ionisation current can be established. We could also make the physical structure of the flat electrode areas as 'transparent' as possible to radiation. In terms of detecting gamma rays, little absorption is going to take place through cardboard, though beta rays may suffer some absorption. Alpha particles are going to be stopped by even short thicknesses of most materials. Also, if the electric field in the collecting cavity is too low, then the efficiency of collection of charge will be correspondingly low. A nominal one-centimetre gap with a voltage of around 100 V will give the electric field required of 100 V/cm to achieve reasonable charge collection efficiency. A 2-centimetre gap would give a reduced collection efficiency though there could be a gain in overall sensitivity.

One small unit was constructed from two sections of plastic used to locate an air extraction tube - providing an area 15 by 15 cms with an central aperture of diameter 10 cms. The total volume of the chamber is approximately 200 cm³. It is useful to walk round large Do-It-Yourself stores to see what novel use such mass produced items can be put to. This small chamber was tested with some low activity Cobalt 60 sources, but would generally be struggling to detect background rates of activty.

Fibreboard, available in art shops, is also a useful medium with which to work to make the larger parallel plate chambers. It is fairly light, being essentially foam-filled, though it has good rigidity and does not bend as readily as cardboard. It is available up to sizes 100 by 75 cm. Slots can be cut out of its area to improve the 'window' access to beta radiation though no more than about 50 percent of the available area should be cut away with a design as indicated in **figure 8**.

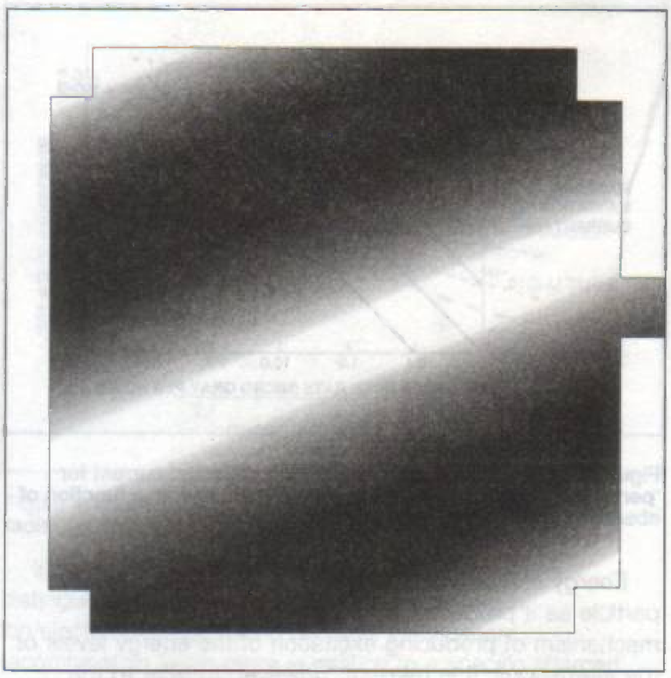


Figure 9: an area of foil should be cut away from areas where pillars are placed. Also a section should be available for securing with a crocodile clip

Aluminium foil is an excellent material to use for the electrode on each side of the ionisation chamber. The foil thickness available today, however, is astonishingly thin, which is a disadvantage for ensuring a crinkle free electrode surface and an advantage in providing low absorption to beta radiation. Glue such as PVA can be used to apply to the board surface to attach the foil - taking care that it is applied as evenly and thinly as possible. Readily available 'glue sticks' can also be used. Alternatively, the aluminium foil can wholly or in part be secured around its exterior by insulating tape. This allows the foil to be tensioned over the surface in which it is brought in contact.

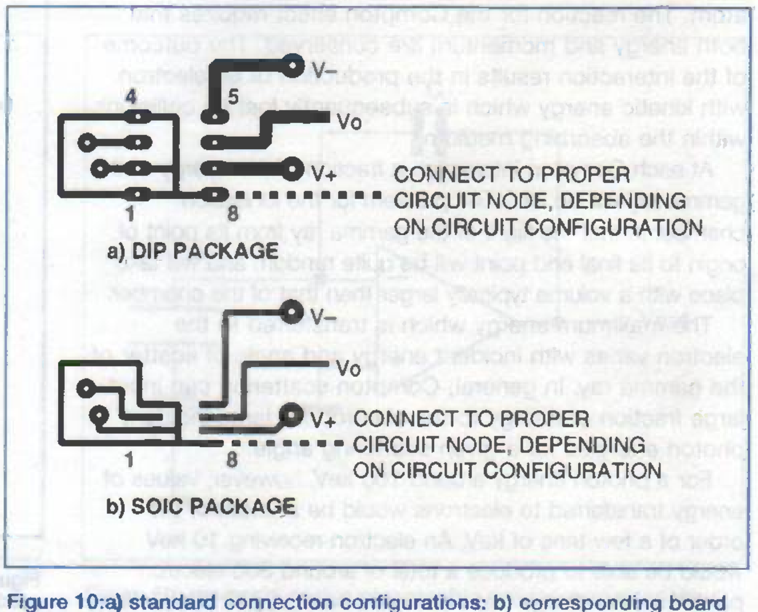


Figure 10:a) standard connection configurations: b) corresponding board layouts for input guard for OPA129

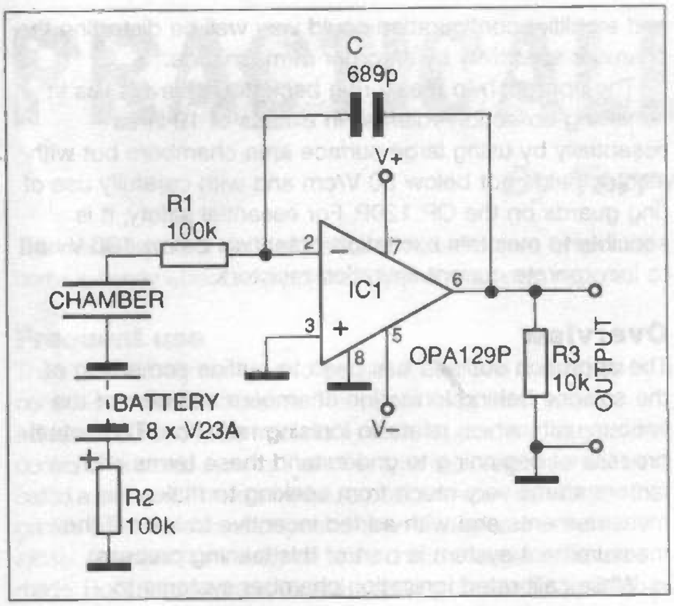


Figure 11 : circuit diagram of the ionisation chamber and associated electronics

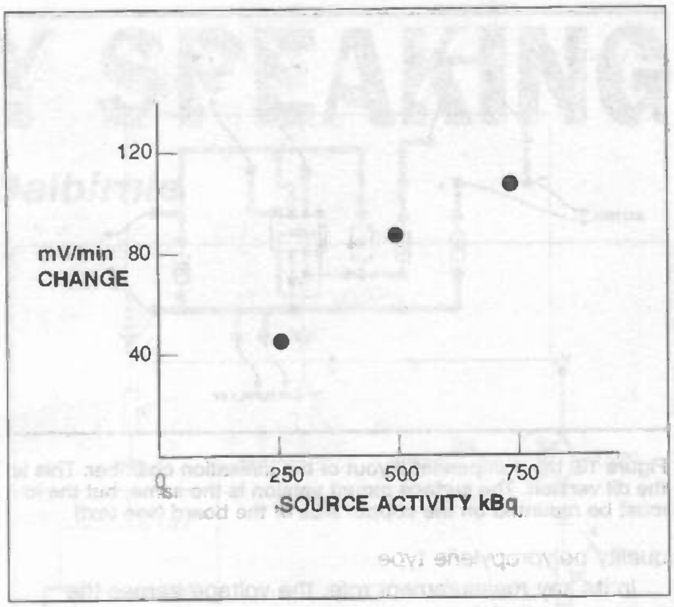


Figure 12: initial results with low activity Cobalt-60 sources for 250 ml capacity parallel plate chamber (open to air)

The foil should be cut away from the corners where separate pillars will be placed to keep the plates apart as shown in **figure 9**. Connection to the foil surface itself is readily undertaken using crocodile clips. The structure can also be made to stand vertically with suitable support on one side and with a single distance piece separating the two sections.

A key component of the design is to minimise the leakage current across the two sides of the chamber. Even if, say, a value of impedance of 10000 megohms is present across the gap of the chamber of 100 V, a current of 10 nA would flow - several orders or magnitude larger than activity levels it is required to measure. Thus the practical problems of minimising such leakage current are very real and at the heart of developing of a usable system.

For a small chamber, then support pillars of dry cork some 10 mm by 4 mm in cross section and 10 mm high are adequate. Small sections of polythene film can also be introduced at the opposite ends of the pillars. Some trial and error is required to stabilise the system and minimise the leakage currents.

The battery supply

It is simpler to use a battery supply which will provide around 100 V for the gap in the ionisation chamber. This involves using eight of the V23A 12 V batteries. This is the battery commonly used to power car alarm control devices. It is a relatively expensive exercise, however, to buy all eight batteries at once.

While small individual battery holders are available for this battery, there appears not to be a readily available unit that will hold eight such cells. The next best thing is to take a flat 4 x AA cell holder and carefully cut it in half at right angles as it were to each battery axis, separate the two halves by an additional 0.5 cm or thereabouts and glue the two sections to a section of stout card or plastic. When completed, this will provide a fairly compact power source for the field of the chamber. Ensure that there is sufficient tension in the springs of the battery holder to secure the batteries in place.

Take care not to touch the 100 V output lines of the battery at the same time - especially with wet hands!

The circuit

The DIFET technology introduced by Burr-Brown provides a range of relatively low cost operational amplifiers which have very low bias currents. The OPA129P, for example, which is available from RS/Electromail, has an input bias current between + 30 fA and - 30 fA. For a bias current as low as this value, the onus is on the circuit designer to avoid introducing spurious input current into the amplifier. Observe static precautions in handling the OPA12P.

In particular leakage currents can be increased on account of factors including leakage in test socket, unclean package, humidity or dew point condensation and circuit contamination from fingerprints or anti-static treatment chemicals. So called triboelectric charge (static electricity generated by friction) can be a troublesome source of noise from input cables.

Figure 10a indicates the standard connection configurations and **figure 10b** the corresponding board layouts for input guard.

The actual circuit diagram of the ionisation chamber is indicated in **figure 11**. Note that pin 8 should be connected to pin 1 and 4. As the operational amplifier functions, pin 2 is maintained very close to ground potential and in turn defines the potential of the chamber surface to which this is connected. The other side of the chamber is kept at a relative negative voltage, with the direction of the electric field pointing downwards - in the direction in which a positive charge would move. It is generally more practical to use the circuit as an integrator device than with a high value load resistance.

We have included a PCB layout adapted for a surface mount ic option as well as the dil configuration. Please note - if you use a surface mount chip, the chip is soldered to the copper side of the board, as given. You then have the option of mounting the other components on the non-copper side (as normal) or mounting them on the copper side and top-soldering. None of the remaining components need to be specifically orientated.

The values of R1 and R2 were 100 k ohms to prevent short circuit of the battery should the electrodes of the chamber touch each other. R3 is simply a load resistance of 10 kohms. C is nominally of value 680 pF. Use a high

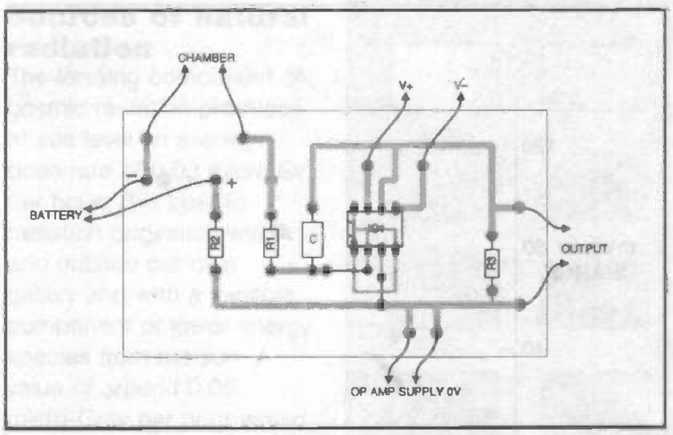


Figure 13: the component layout of the ionisation chamber. This is the dil version. The surface mount version is the same, but the ic must be mounted on the copper side of the board (see text)

quality polypropylene type.

In its key measurement role, the voltage across the capacitance is given by:

$$V = Q/C$$

where Q is the charge and C is the value of capacitance. Where this voltage is changing,

$$dV/dt = I/C$$

for C = 680 pF and I = 10-13 A the change in voltage is of the order of 10 mV per minute. This voltage can readily be measured by attaching a DVM across the output of the unit.

The challenge of measurement is to reduce leakage currents to a minimum so that real effects of ionisation can be detected. This can be offset by constructing a chamber large enough - in excess of say 10 litres capacity.

Initial measurements

Using a simple Veroboard assembly without guard rings on the amplifier chip as recommended, initial values of activity were noted with some low intensity Cobalt-60 sources - each of activity around 250 kBq (disintegrations per second). Initial results are indicated in **figure 12**.

With a 680 pF capacitance in place in integration mode, the calculated corresponding voltage change is approximate 0.3 mV/min at level of 1 micro Gy/hour. The actual level of 'background' drift measured is some 30 times this value and must be due to additional leakage factors in the notionally simple circuit implemented without guard rings on the OP 129P.

The calculated level of sensitivity of the detector of 1 mV/minute corresponds approximately to an activity of 3.3 micro Gy per hour. A single source placed over the chamber provides a change in rate of 40 mV/min corresponding to a calculated absorbed dose of 138.6 micro Gy per hour. The actual chamber geometry, however, and amplifier configuration could very well be distorting the chamber sensitivity by an order of magnitude.

The approach to measuring background levels lies in achieving collection volumes in excess of 10 litres - essentially by using large surface area chambers but with electric fields not below 50 V/cm and with carefully use of ring guards on the OP 129P. For essential safety, it is sensible to maintain excitation potentials below 100 V and to incorporate current limitation resistors.

Overview

The approach outlined has been to outline something of the science behind ionisation chambers and also of the various units which relate to ionising radiation. The actual process of beginning to understand these terms and factors stems very much from seeking to make measurements and with added incentive to learn if the measurement system is part of this leaning process.

While calibrated ionisation chamber systems to measure levels of ionising radiation with high certainty are of necessity of specialist design and expensive to manufacture, the fundamentals of these systems can be replicated with very basic components and the skill of a keen experimenter. It is also the case that a good deal of patience is required to develop an effective ionisation chamber - one of good sensitivity and low leakage current from non-radiation induced sources.

Also, the NRPB document (see references) is an extremely useful source of information about radioactivity from all manner of sources in the UK.

References

An introduction to radiological physics and radiation dosimetry, Frank Herbert Attix, Wiley-Interscience

An introduction to radiation protection, Alan Martin and Samual A. Harbison, second edition, Chapman and Hall, 1979.

Radiation Exposure of the UK population - 1993 Review National Radiological Protection Board. (current issues available from HMSO Bookshops)

PARTS LIST

All parts	
R1, R2	100
R3	10k
C1	689pF
Wire link	1k1
Wire link	1k2
IC1	OPA129P (RS/Electromail)
Battery	8 x V23A 12V batteries
V+,V-	PP3-type 9V

PRACTICALLY SPEAKING

By Terry Balbirnie

This month and next we shall look at some techniques which may come in handy when using potentiometers in your own designs.

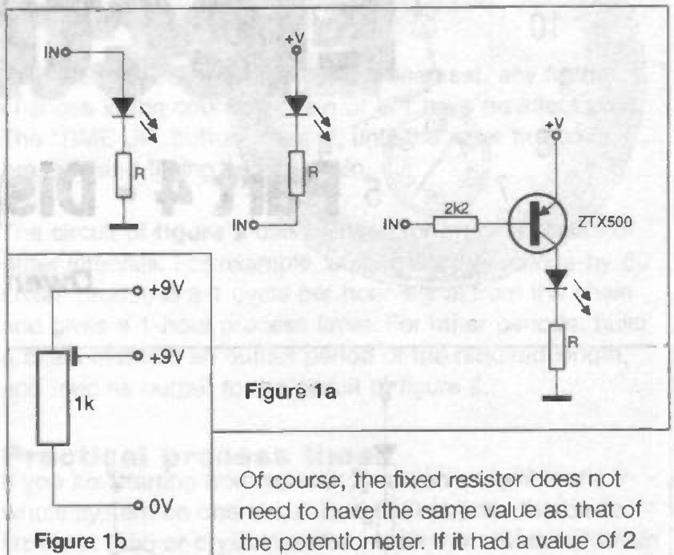


Figure 1a
Figure 1b

Frequent use

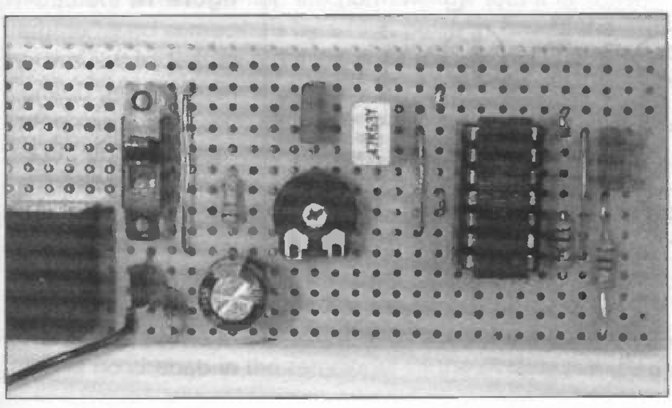
There are basically two types of potentiometer. One is operated by a control knob outside the case. This type is used when frequent adjustments need to be made to a circuit, for example, as a volume control on a stereo system. The other type is a preset (sometimes called a trimmer). This is a miniature potentiometer mounted on the printed circuit board and only used when setting-up the circuit initially. After that, it is usually left alone unless changes need to be made. Both horizontal and vertical-mounting presets are available in a range of values from about 100 ohms to over one megohm. The photograph shows a horizontal preset in a circuit.

Presets are useful in circuits to allow for component tolerances. For example, when making a design based on a 555 timer. Here, a capacitor charges through a known resistance. The voltage across the capacitor rises, and when it reaches a certain value, the circuit times out. However, the capacitor value is not usually known to an accuracy greater than 5 percent. This means that if you calculate the resistor value needed for a given period, it will probably not give the correct result. By including a preset, it may be trimmed at the end to provide the timing required. Normally you would make the calculation as for a fixed resistor, and then double it. You would now choose the nearest stock value. This will give the "correct" adjustment near the centre of the track.

Range narrowing

Look at the 1k potentiometer connected across the 9V supply. In **figure 1a**, the sliding contact is at the bottom of the track so the voltage appearing between the 0V line and the slider is 0V. When it is at the top, as in **figure 1b**, it is +9V. Smooth changes from 0 to +9V are therefore possible. However, there are times when the potentiometer only needs to adjust the voltage over part of the range. For example, you might require it to run from, say, 3V to 4V. This type of range-narrowing is easy to achieve using a fixed resistor or resistors connected in series with the potentiometer.

Look at the arrangement in **figure 2a**. Since the value of the fixed resistor, R1, is the same as that of the potentiometer, there will be +4.5V at the top end of it. The potentiometer will then allow adjustments between +4.5V and 9V. The fixed resistor could be placed instead as shown in **figure 2b**. Now the voltage at the bottom end of it is 4.5V so the potentiometer allows adjustments between 0 and 4.5V.



Of course, the fixed resistor does not need to have the same value as that of the potentiometer. If it had a value of 2 kilohms in **figure 2b**, the total resistance would be 3k and the voltage at the bottom end of R1 would be one third of 9V - that is, 3V. In this case the sliding contact will allow adjustment from 0 to 3V only.

Figure 3 shows a potentiometer with two fixed resistors, R1 and R2, - one above and one below it. Suppose these both have the same value as the potentiometer - 1k? There will be +3V at the top end of R2 and +6V at the bottom end of R1. The potentiometer will therefore allow an adjustment between 3V and 6V. Again, the choice of values of the fixed resistors can be used to tailor the range to suit the application.

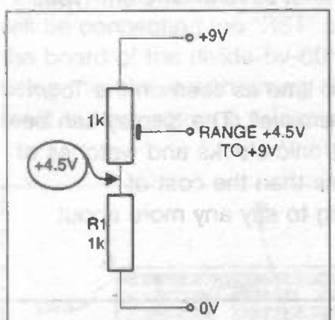


Figure 2a

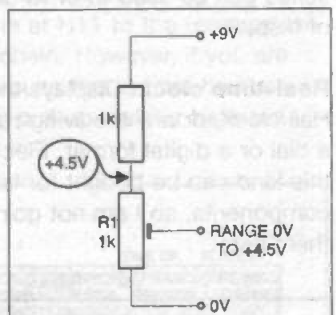


Figure 2b

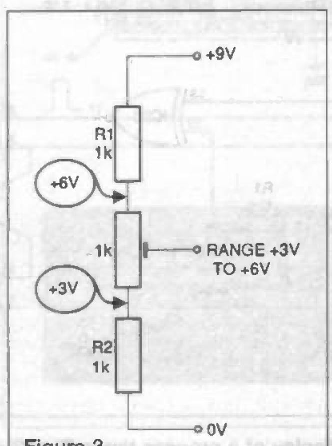
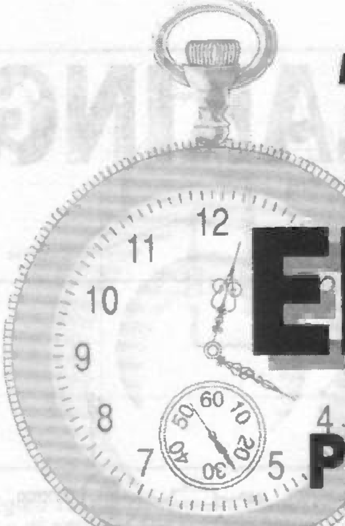


Figure 3

There is no point in allowing a potentiometer to cover a range much greater than required. In fact, this will make it difficult to adjust. This is because small movements of the sliding contact will cause large changes. Narrowing the range of adjustment makes it easier to get the setting right.

Next month, I will look at the result of a fixed resistor connected in parallel with a potentiometer.



Timing in Electronics

Part 4 - Displaying time

Owen Bishop

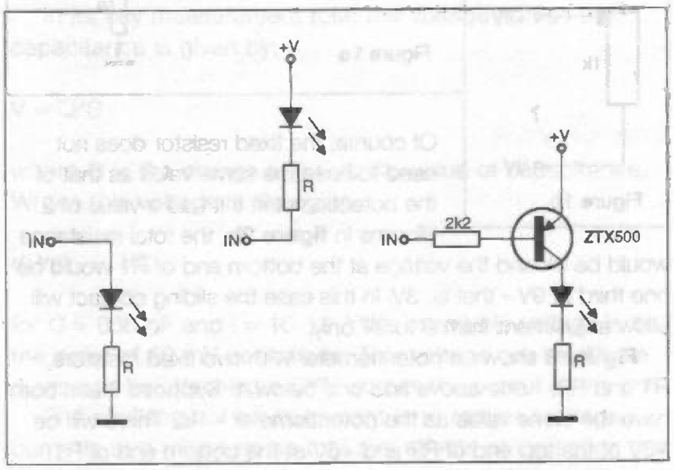


Figure 1: various ways of switching an LED from a timer output

The timing circuits described in the first three parts of this series can be used to drive one of several different types of display:

Real-time clock: Displays the time as seen on the Town Hall clock, or any the living-room wall. The display can be a dial or a digital format. Electronic clocks and watches of this kind can be bought for less than the cost of components, so I am not going to say any more about them here.

Elapsed time clock: Measure the interval between clock start and clock stop. These are available as analogue or digital stopwatches, but you can find novel applications for them that manufacturers have not thought of (yet). Triggering them electronically is part of the fun.

Process timers: Run for a pre-set period before indicating that time is up. Range from the hourglass used for timing sermons to the digital timers in microwave ovens which revert to real-time when the cooking is finished. There are always new applications for this kind of clock.

Process timers

I have described two ways of setting the period length. The simpler way is to use a monostable based on the 555 or similar ic and let it run for a single period. Monostables are suitable for relatively short periods of microseconds up to 5 or 10 minutes, but they are inaccurate for longer periods owing to the wide tolerances and poor stability of large-value capacitors. For longer periods, of minutes, hours, or days, use an astable, preferably one based on a crystal, and count its pulses.

For a visual display (I will look at audible and other indicators later in this series) LEDs have much in their favour. An LED can be ON while the timer is running and OFF at the end of the period, or vice versa. Or the timer can have one LED for each purpose.

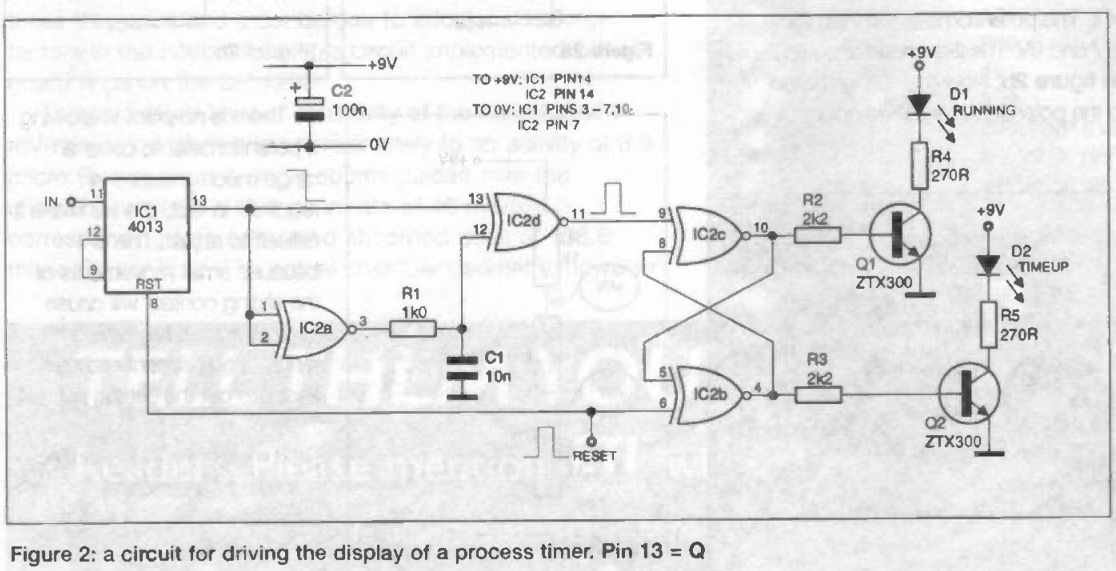
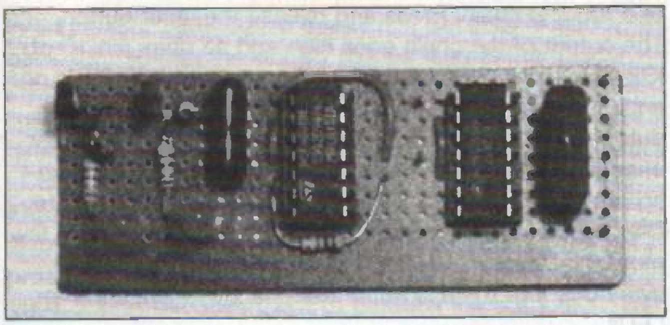
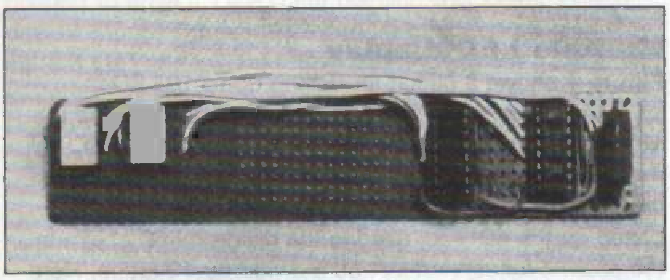


Figure 2: a circuit for driving the display of a process timer. Pin 13 = Q

If the circuit is based on a 555 or similar ic it has more than enough current output to drive an LED directly. In **figure 1a** the LED comes on when the output of the ic is high, that is, during the timed period. In **figure 1b** the LED comes on when the output is low, that is, when the ic is waiting to be triggered, and also after the period is ended.





Unfortunately we cannot connect both **figure 1a** and **figure 1b** to the same output, as this would put the LEDs in series. Current flows through both of them and they are both lit at the same time. In this case, or when the timer output does not have enough current to drive an LED directly (for example, the output comes from a logic gate), we use a transistor switch. The way to turn the LED on when output is high is shown in **figure 2**, with an npn transistor. For the reverse action with a pnp transistor, see **figure 1c**.

If the timing circuit is an astable followed by a counting chain, the approach is slightly different. Its output alternates between high and low. We need to reset the counter when we begin timing and arrange that an LED comes on and stays on at the end.

As an example, take **figure 2**, which is a 1-minute process timer. It is driven by a 1-Hz clock (the 555 astable or the crystal clock) followed by the 'divide by 60 chain'. The output terminal of the chain is connected to the IN terminal, pin 11 of IC1. The output of the chain runs at 1/60 Hz, so it changes state every 30s. The chain has a reset line, which is held low by a resistor but can be made high by pressing a button. The RESET input in figure 2 is connected to this line. IC1 is a D-type flip-flop with its inverter (Q-bar) output fed back to its data input. This makes the flip-flop act as a divide-by-2 counter. Its Q output changes state at 1/120 Hz. In other words, its output goes high when it is reset and stays high for 60s. This is the basis of the 1-minute timing period.

The LEDs are controlled by a set-reset flip-flop built from two cross-connected NOR gates (IC2b and IC2c). The inputs of this flip-flop are normally low and it is triggered to change state by a high pulse to one of the inputs. The sequence of timing is as follows:

1: Pressing the button resets both dividers in the chain, the flip-flop IC1, and also the set-reset flip-flop of IC2. This makes the chain output high. Also the output of gate IC2c goes high, turning on Q1 and lighting the 'RUNNING' LED, D1.

2: Counting proceeds. After 30s the output of the chain goes low, but IC1 is unaffected by a low-going edge so there is no change in the remainder of the circuit.

3: After a further 30 s the output of the chain goes high. This makes the output of IC1 go low, which triggers the pulse generator consisting two NOR gates, IC2a and IC2d (4001). This generator normally has a low output but now produces a short high pulse. This sets the set-reset flip-flop. The output of gate IC2c goes low and that of IC2b goes high. The 'RUNNING' LED goes off and the 'TIME UP' LED goes on.

4: Once the set-reset flip-flop has been set, any further changes in the counting chain or IC1 have no effect on it. The 'TIME UP' button stays lit, until the reset button is pressed and timing begins again.

The circuit of **figure 2** can be used for process timers of other intervals. For example, adding another 'divide-by-60 chain' produces a 1 cycle per hour signal from the chain and gives a 1-hour process timer. For other periods, build a chain that has an output period of the required length, and feed its output to the circuit of figure 2.

Practical process timer

If you are starting from scratch, you can assemble the whole system on one circuit board. First build the basic 1-Hz clock (555 or crystal version), then the 'divide by' chain or chains, as described in previous parts of this series. Add the circuit of figure 2, installing either one or both of the transistor switches and LEDs. The ZTX300 transistors are capable of switching up to 500 mA each so there is no need to limit yourself to LEDs. They can switch filament lamps, small DC motors, solenoids, or relays. Relays can be used for switching other devices. This circuit is the basis of a system for process and timing control. Use it in darkroom photography, model railways, home security systems, or many other applications.

Figure 3 shows the stripboard layout. This does not include a reset button because we are assuming that you will be connecting the 'RST' pin at H11 to the reset pin on the board of the divide-by-60 chain. However, if you are using this circuit with timing circuits that do not have a reset button, solder a 1-kilohm pull-up resistor between

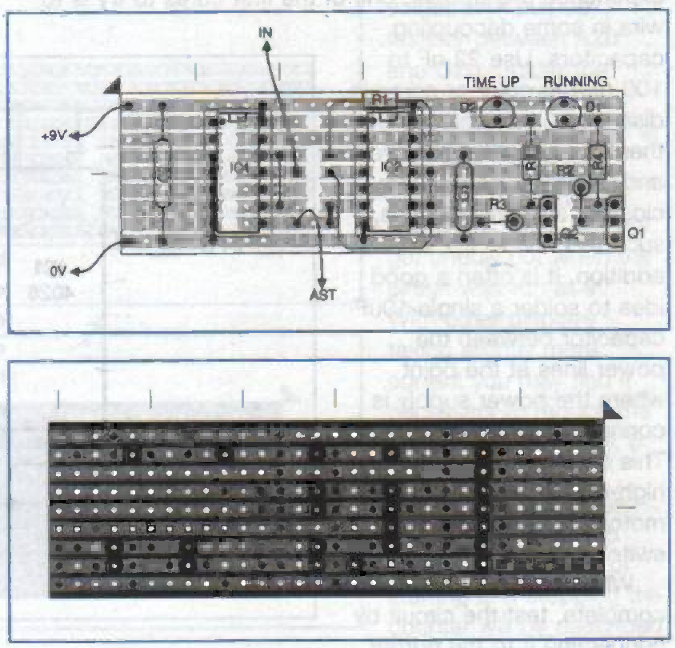


Figure 3: stripboard layout of the process timer of figure 2

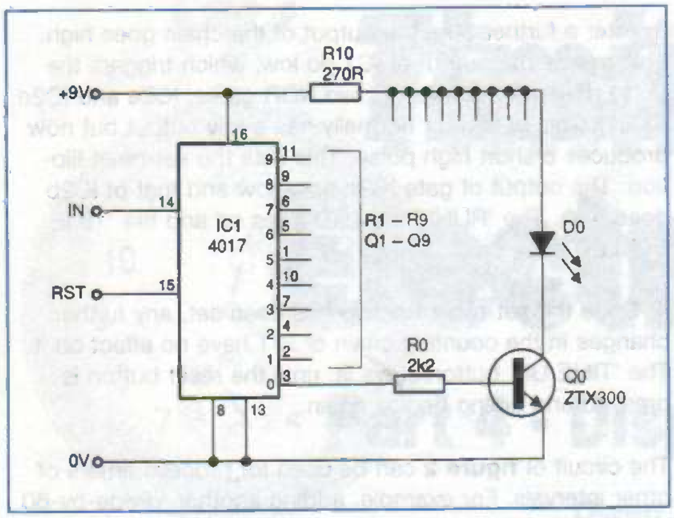


Figure 4: a process timer with up to 10 LEDs in its display. D1 - D9 are at top right.

A12 and H12. Solder the resetting push-button between the 'RST' pin at H11 and the 0 V line. The diagram shows two indicator LEDs. You may decide that you do not want both of these, in which case, omit it together with its transistor and two resistors.

When assembling this circuit you will notice that although the circuit diagram has many connections, there seem to be very few on the stripboard. This is because it uses the copper strips between and beneath the ics for making many of the connections. Check the stripboard layout diagrams carefully and cut the strips only where shown. Note that there are several places where solder bridges are used to join pins in adjacent strips. All of these are important.

C2 is the decoupling capacitor for the supply lines. Counters are particularly prone to operate incorrectly if spikes resulting from the sudden switching of currents as the ics and gates change state are present. When you have built up a system from several ics, you may find that although the parts of the system operate correctly separately, there is erratic behaviour when the whole system is joined. This depends a lot on how the various parts are laid out with respect to each other. If you experience this trouble, one of the first cures to try is to wire in some decoupling capacitors. Use 22 nF to 100 nF polyester or ceramic disc capacitors and solder them between the positive and 0V rails. Locate them close to sensitive devices, such as counter ics. In addition, it is often a good idea to solder a single 10uF capacitor between the power lines at the point where the power supply is connected to the board. This can be very helpful if high-current devices such as motors or relays are being switched.

When assembly is complete, test the circuit by connecting it to the output of a dividing chain. Press and release the reset button. The output of the chain goes high and so does pin 10 of IC2. Pin 4 of IC2 and pin 13 of IC1 are both low. D1 is on, and D2 is off. If you are using a divide-by-60 chain, its output goes low after 30 seconds, but there are no other changes. At 60 s the output of the chain goes high, and so does pin 13 of IC1. The flip-flop of IC2 changes state, D1 goes off and D2 comes on. Let the circuit run for a few more minutes; pin 13 of IC1 continues to change state every 60s, but there is no further change in IC2 and the LEDs.

Multiple LED display

Figure 4 shows a circuit for driving up to 10 LEDs, switching them on one at a time. The LEDs could be the 10 units of a bar-graph display or 10 separate LEDs mounted in a circle, so that a spot of light moves round the circle once for every 10 input counts. The circuit is based on the 4017 ic, used in the divide-by-60 chain. In the chain it functioned just as a divide-by-10 stage. Here we use the 10 individual outputs that are normally low but go high one at a time (from 0 to 9) each time the input rises from low to high.

This circuit has features of both a process timer and an elapsed time clock, much depending on how the display is set out. If, for example, we feed this circuit from a clock with a period of 1 minute, the count is incremented at the beginning of each minute. It takes 10 minutes for the display to go through its complete cycle. This gives a process timer for timing a sequence of processes each lasting a few minutes, the total not exceeding 10 minutes.

The LEDs are each driven by a transistor, only one of which is shown in figure 4. Use individual transistors or two arrays of transistors in a dil package such as the CA3082. As only one LED is on at a time, a single current-limiting resistor R10 can be used.

Elapsed time clocks

An elapsed time clock needs a numeric display, normally LED or LCD. The LED display uses the popular 7-segment devices, which come in a range of sizes and colours. LEDs are best in low light conditions and may be impossible to read in bright sunlight. LCD displays are more easily read

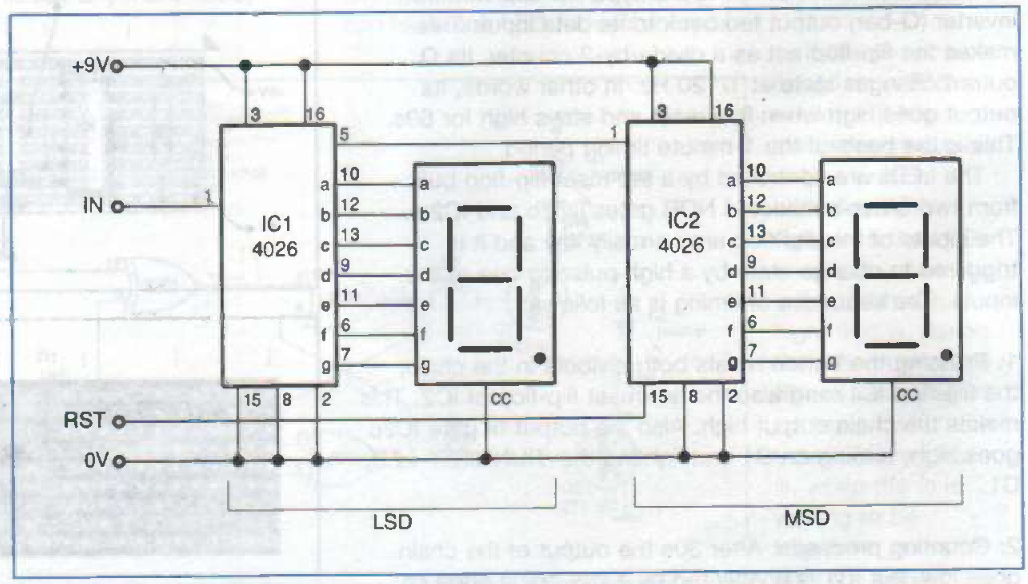


Figure 5: an elapsed-time timer with a two-digit display

in bright light. Although in theory it is possible to add a back-light so that the display can be read in the dark, in practice the designer is nearly always so mean with back-light wattage that the display is readable only with great difficulty. We will look at LED displays this month and leave LCDs until another part.

Figure 5 shows one of the simplest versions of an LED display. The 4026 is a decade counter/divider. Instead of producing the usual 4-bit decade outputs from 0000 to 1001, this ic decodes them to produce the outputs needed to drive a 7-segment display. This saves a great deal of wiring. The fact that the device can drive low-current LED and LCD displays directly, without transistor switches, means a big saving in additional components. However, this ic does not do some things, such as 'leading zero suppression'. Its counting sequence is displayed as 00, 01, 02, 03 etc, instead of 0, 1, 2, and 3. On the other hand, it puts 'tails' on the sixes and nines, which some decoder ics do not do.

Probably the most versatile and popular display driver is the 4511. This is a driver only, not a counter, so you need to feed it with the output from a regular decade counter ic. This needs four ics for a two-digit display like the one in figure 5. Features include display blanking (for leading zero suppression), lamp test (all LEDs come on), and latching, so that the display can be held for reading even though the output is changing. It needs a current-limiting resistor on all seven segments of the display. Although the 4511 has many useful features, we decided that the 4026 has all that is essential for a simply constructed elapsed-time clock.

Practical elapsed-time clock

If the circuit of figure 5 is fed with a 1-Hz signal from the astable or crystal clock, it counts from zero to 99 seconds before repeating. It can be reset to zero at any stage by pressing the reset button. If it is fed from the divide-by-60 chain, it counts minutes instead. It could also work in tens of minutes, hours or even longer periods.

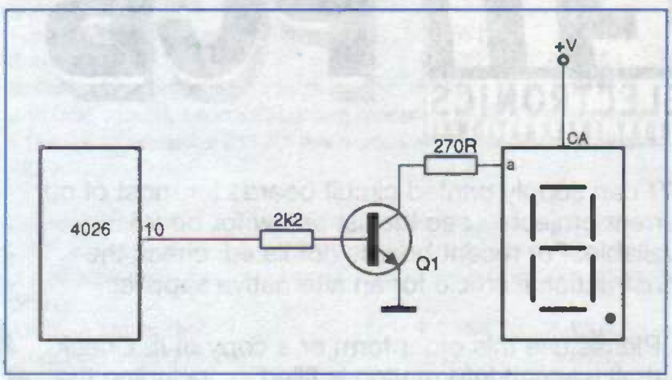


Figure 6: using a transistor to switch an LED segment

The 4026 ic produces outputs that are high when the LED segment is to be lit. We use a common-cathode display in which the cathodes of all the segments connect to a common line connected to the 0V rail. You may want to adapt the design for larger displays than our 7.5 mm low-current devices (there is room on the board). If so, you may need to use have each segment driven by a transistor. Then you should use a common anode display, and connect each segment as shown in **figure 6**.

The stripboard layout (**figure 7**) has room for up to three counters and displays, counting to 999. You need have only one or two of each, and make the board shorter. There are quite a lot of wired connections. Rather than make the drawing confusing by showing all the wires, we have marked their ends a to g to correspond with the segments. Note that the ic for the first digit, the *least significant digit* (LSD) is on the left of that for the second digit, the most significant digit (MSD), but the displays are the other way round. Get the connections the right length so that the assembly is tidy. Take care to make all connections correctly - if these are wrong it will soon show up as a set of strange symbols when counting begins. As before, a 100nF decoupling capacitor (C1) is advisable.

The circuit has a reset input intended for connecting to the reset pin of a counter chain. If you drive this circuit directly from a 1-Hz generator, which does not have a reset input, solder a 1k pull-up resistor between A20 and C20. Solder the resetting push-button between the 'RST' pin at C11 and the 0V line.

In the prototype we found that the ic did not get unduly hot when the circuit was run at 9V. With other displays taking slightly more current you may find it necessary to reduce the power supply to, say, 6 V.

Timing starts when the button is pressed and released. Ways of starting and stopping the counter will be described in the next part.

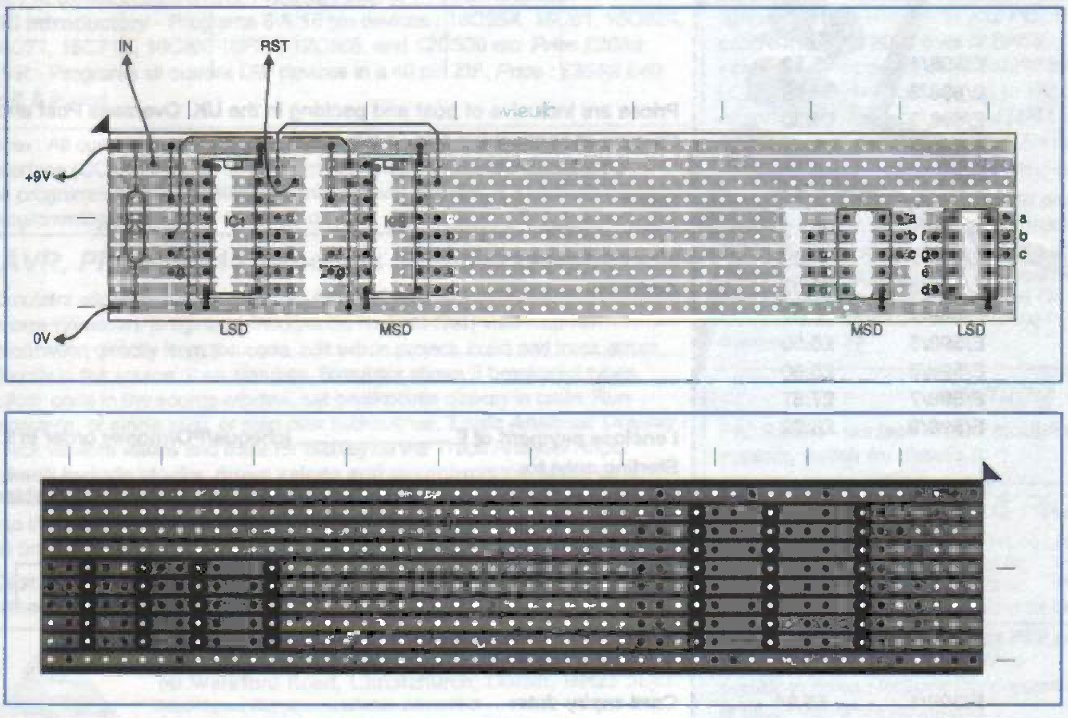


Figure 7: stripboard layout of the elapsed-time timer of figure 5

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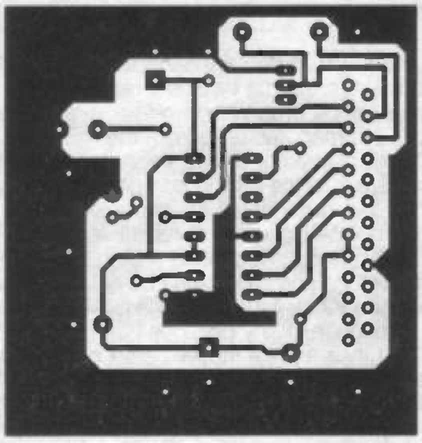

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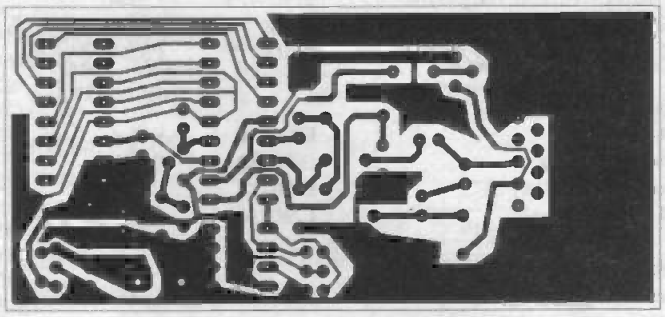

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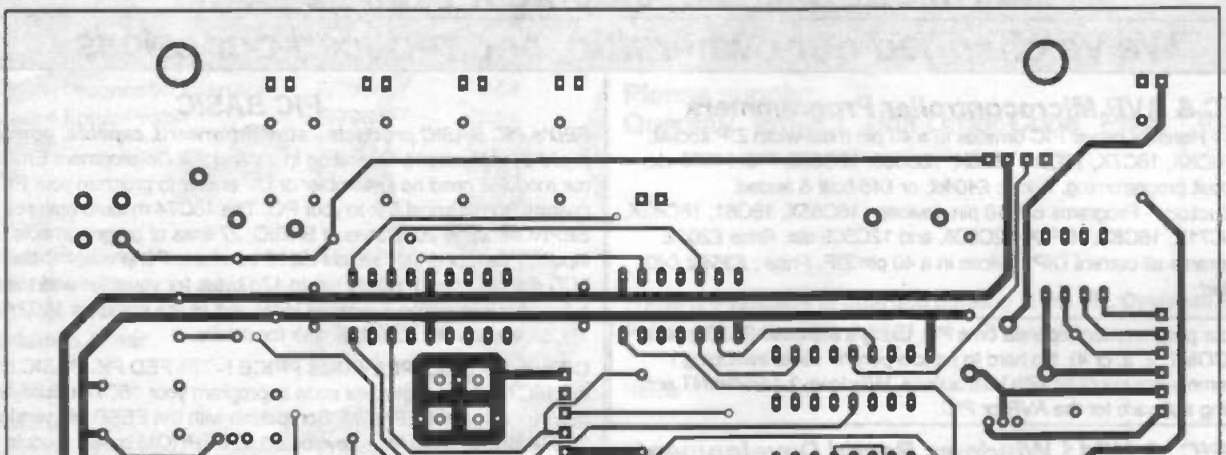

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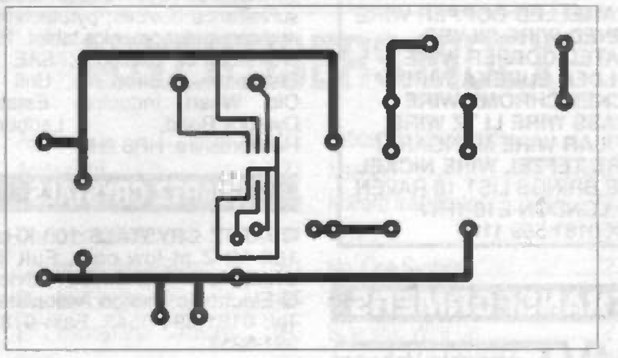

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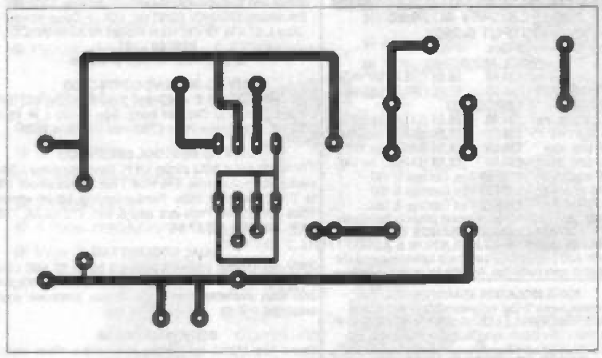

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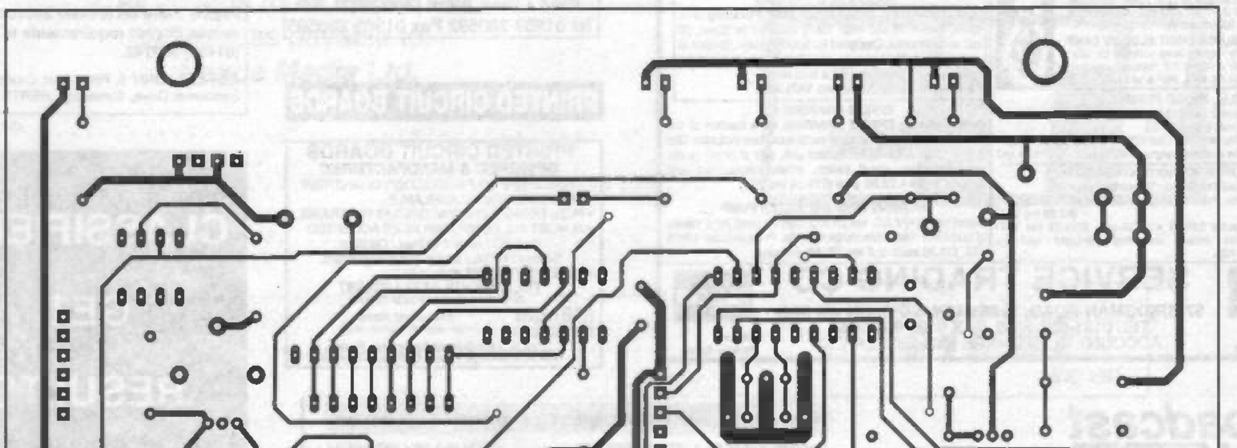

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Round the Corner

Lagging in Understanding

Politicians control the future, don't they? For better or worse, the decisions they make determine how we will live, and if we don't like it we have the occasional opportunity to select one pack of policies or another which may or may not be very different.

It is true as far as it goes, but engineers, scientists, and other technical folk are collectively responsible for providing the environment about which they legislate. These are the people who have more effect on our lives in the longer term. The general standard of living which we enjoy in the western world is the result of generations of technological development.

It is a sad fact that few if any of those who rule Britain have a scientific education, so they are often behind in understanding what is happening. Take the proposal made by the European Commission to tax data transfer on the Internet. A "bit tax" is probably unworkable. If it did work, it would simply hand more of the benefits of Internet trade over to other geographical regions. Since phone conversations are also digital, the tax would also presumably add to the cost of phone calls as well.

In France it is illegal for any civilian to use encryption, but it is not illegal in Britain. In the longer term, the need to use the available bandwidth efficiently, for economic and technical reasons, will probably render the question much less important. Shannon's law tells us that the most efficient use of bandwidth involves an even power density over a communications channel. Techniques that approach this will probably involve complicated coding which, while not encryption as such, will not be easy to demodulate without the specific decoding sequence.

The contortions used to get working pgp encryption software out of the USA is another amusing case of bureaucratic confusion. It was ruled illegal to export source code or compiled software, despite the fact that the mathematics of the encryption is known over a wide area of the world, but for some reason it was not illegal to carry out a book containing the code. This was scanned, optically character recognised, and put on a web server not in the USA.

Quite likely the issue of encryption will cease to be of great political interest, communications will normally be reliable and as secure as necessary, and some other item which the government of the day does not understand will be the new big concern.

Next Month

Volume 27 No 11 of *Electronics Today International* will be in your newsagents on 9th October 1998. Tony Howarth describes how to sail round the world on solar power ... just right for A British summer: Pei An's temperature and humidity logger operates from the Centronics port of a PC and stores data for future analysis, as well as displaying the measurements on LD readouts ... multiple circuits for Music Lovers, including that "Jimi Hendrix" sound ... those Versatile Diodes doing the unexpected ... and much more.

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