NEW: Chip Selekt programmable disco lights mating CMOS with TTL

Capacitance Meter
From varicaps to large electrolytics
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</tbody>
</table>

A new look for our cover this month which does not, however, mean a new look inside. We will continue to offer you in each issue a host of practical projects chosen from across the whole spectrum of electronics interspersed with articles of a less practical, but none the less interesting, nature in the field of electronics. Above all, we will continue to endeavour to keep up the high standards that readers of Elektor have come to expect.

Also new this month is the capacitance meter illustrated. This is the first in a range of test instruments which we will publish at (hopefully) regular intervals. All instruments in this range are designed to fit the same family of standard cases and, as our cover shows, they even look quite handsome!

We also start a new section this month: 'Chip Selekt'. This section will be published at irregular intervals, alternating with 'Applicator', and is intended to bring to your attention new or improved ICs which have recently been supplied to us by manufacturers or distributors.

A selection from next month's issue:
- real-time analyser
- UHF quartz modulator
- tape contents controller
- electronic labyrinth
- triac control board
- petrol saver
The DC working voltage of capacitors (other than electrolytic or tantalum types) is normally assumed to be at least 60 V. As a rule of thumb, a safe value is usually approximately twice the DC supply voltage.

Test voltages
DC test voltages shown are measured with a 20 kΩ/V instrument, unless otherwise specified.

U, not V
Normally, the international letter symbol "U" instead of the ambiguous "V" is used for voltage. "V" is reserved as an abbreviation for "volts."

For instance, U100 = 10 V, not V100 = 10 V.

Mains voltage
Mains (power line) voltages are generally published under 'Missing Links' as it is assumed that our readers know what voltage is standard in their part of the world.

Readers living in areas which use 60 Hz supplies should note that Elektor circuits designed for 50 Hz supplies will not normally be a problem, but in cases where the mains frequency is used for synchronization, some modification to the circuit may be required.

Technical services to readers
- EPS: Elektor printed-circuit board service
- Many Elektor articles include a layout for a printed-circuit board. Most, but not all, of these boards are available ready-etched and pre-drilled. The EPS in the current issue gives a list of available boards, front panels, and software cassettes.
- Technical queries Technical queries relating to articles published in Elektor may be submitted by telephone (Tel. 0227-53474) on Mondays between 13.30 and 16.15, or in writing. The telephone service does not operate during July/August. Letters should be addressed to Dept. TQ Please enclose a stamped self-addressed envelope or, if you live outside the United Kingdom, an International Reply Coupon.
- Missing Links Any important modifications to, additions to, or corrections in, Elektor circuits are generally published under 'Missing Links' at the earliest opportunity.
Did you notice?

Just inside the cover, things are not quite what they were. Up until now, we included three infocards in each issue; from now on there will be only one. The other two cards are replaced by a data card and a contents card. Why? Well...we think it makes a good mixture! Let's take a closer look at each.

The infocards have proved extremely popular — so much so, in fact, that readers are complaining: "some @$*#$* swiped my complete set! Can you supply me with new ones?". (To comply with this type of request, we are preparing a reprint of the first 100 cards.) However, the set is now fairly complete and so adding a further three cards each month would mean including less relevant data. Using only one card means that we can keep the set up-to-date, without it becoming a mine of useless information.

The data cards will give the most important specifications of semiconductors in short form. In effect, they complement the infocard series by listing devices that didn't meritan infocard of their own!

The contents cards are an answer to readers' prayers — as voiced again, recently, in our readership survey. Apparently, back copies over the last five years or more are used as a regular reference guide. Since we publish some two hundred projects each year, finding the one you want can be rather a problem. A card index can be great help — but what type of index is 'ideal'? If you're looking for a power amplifier, it would seem obvious to look under 'audio' cards for the last four or five years. However, if you want to look up 'that special gimmick they used in a symmetrical power supply, when was it...end of '83 or beginning of '84, I think', then it is much easier to use a chronological index that contains one card for each issue. Starting this month, you can collect both types of index. One side of the contents card gives last month's contents (with a picture of the cover, to jog your memory!); the other side contains one of the subject matter groups. In the course of one full year we will include them all (audio, measuring, et cetera) for the 1983 volume; meanwhile, 1984 will be listed on the reverse side month-by-month. In 1985, the 1984 contents will be grouped according to subject matter (giving a second 'audio' card and so on ...). The result will be a master index that becomes more and more valuable as years go by!

So, what else is new?

I hesitate to say...! Apparently, if we just change something, no one seems to mind; but if we mention it, even in passing, someone is sure to complain! A case in point: recently, I mentioned that we were attempting to strike a balance on the subject of microprocessors — based on the fact that the love-hate ratio amongst our readership appears to be 1:1. The gist of the message was: not too many pages on the subject, and a slant towards more 'universal' hardware that can also be used with commercial machines. Witness, say, the 64K dynamic RAM or the Universal Terminal. Believe it or not, several readers wrote to me, protesting against 'your plans to banish microprocessors from Elektor!' Hey, man, I never said that! Perish the thought! Our subject is 'up-to-date electronics', and microprocessors are very much a part of that scene. However, they are not the whole field, and we intend to keep them from dominating our pages. Just look at the last few issues, and you'll see what I mean: they are not banished, but we have found room for a few other projects — to put it mildly.

So: 'What else is new?' — look through this issue, and you may spot one or two new features... Next month? I'll leave you guessing!

Your editor.
future developments in ICs

Industrial developments are governed by economic feasibility on the one hand and physical possibilities on the other. This is no exception in the IC industry. As yet, there are no fundamental limits, as far as physics is concerned, to further reductions in the size of ICs. It follows that, for the time being at least, development in the field of ICs is governed totally by economic aspects.

Four cost factors play a role in determining the price of ICs: those of the crystal, development, testing, and packaging. At this time these four are about equal. There is, however, a tendency for development costs to take a larger share of the total, unless special attention is paid to this.

With no natural limits in sight (as yet), new methods to produce smaller structures are found continually. This is well illustrated by the development of substrates which can be processed, and the width of the tracks which can be realized on them. The diameter of substrates has grown in steps: it is already clear that processing of 6 in (15 cm) crystals is physically possible. The tracks industry can produce are getting narrower and narrower. In the early 1960s track-widths were of the order of 100 μm. Present-day techniques allow widths of 4...2 μm to be realized (figure 1).

The tendency towards larger substrates and narrower tracks means, of course, a sharp increase in the capital cost of manufacturing tools. The equipment required for the production of 20 000 chips per month cost between £3m and £4m in 1980; by 1990 those figures will have trebled. But by then, the chips will be larger and more complex and therefore worth more.

Complexity

The factor which has the greatest effect on costs is the component density: the number of components which can be housed on a single crystal. As the track-width is reduced by 10 per cent each year, the surface area of a transistor decreases by 20 per cent per year. Because the individual connections will occupy relatively more space, the average component density rises less rapidly than one would expect from these figures: about 15 per cent per year.

On the other hand it is possible to produce larger chips with a satisfactory turn-over.

Each year the producible chip area increases by about twenty per cent, which means that in principle the complexity of the designs can increase by 37 per cent. This possibility is fully utilized in certain sectors, such as memories. There is no reason why ever larger building elements should not be used in the construction of memories. In many other applications it is not so simple. With increasing complexity, a building element becomes more and more specific and it therefore becomes harder to find units in equipment which have enough applications in common to guarantee sufficiently large production runs (figure 2). It is for that reason that in practice the average complexity of newly introduced building elements increases by only twenty per cent per year (figure 3).
Cost reductions
The required area per transistor, including connections, is reduced by about 13 per cent per year. In spite of the higher capital costs mentioned earlier, the production costs per unit of area fall by about ten per cent per year. This is because larger substrates are being used. The combination of these two factors means that the cost of the transistor itself drops by around twenty per cent per year. The other cost factors should show a similar tendency.

What's being done
The problem is attacked in two ways: firstly, by increasing the productivity of designers and, secondly, by aiming at an increase in production per design. The latter means that more effort is required towards standardization and the use of universal components instead of specific ones.

Design productivity can be increased in various ways: in the first instance by the use of Computer Aided Design (CAD) in which the computer is used in practically all phases of the design process.

Planning
Furthermore, by changes in the design planning, in principle, the IC designer has a large degree of freedom in virtually every detail of the design. Making profitable use of this freedom takes time, however. Limiting the possibilities of the design increases efficiency, but will, of course, often mean that the design is realized at a higher abstract level. Freedom in the design can be further limited by planning a chip on the basis of a pattern of a large number of standard basic functions, where the designer can only determine which circuits are connected and how.

On the other hand, it is necessary that the productivity of the designer increases. Greater complexity renders the design more and more specific to certain applications. This results in a larger need for diversity: in other words, a growing number of more complex circuits will have to be designed.

Miscellaneous cost considerations
The increasing component density will also be a factor in the cost of testing a transistor. The complexity of ICs can become so great that it becomes extremely difficult to test individual transistors. The result may be an explosion in the cost of testing. This problem is tackled in several ways: by modifying test strategy, by making more allowance for testing during the design stages, and by introducing special test circuits onto the chips. The last two measures generally mean that test costs are exchanged for higher crystal costs. It is expected, however, that by adopting these measures the cost of testing will not rise, and may actually show a slight fall.

The price of packaging is virtually constant. As the contents of the chip become more complex, the number of pins will inevitably increase which means a rise in costs. Intrinsic material costs will, of course, rise as well. However, automation of the packaging processes in manufacture can compensate completely for these cost increases. All the same, the apportioned cost of the package in the price per transistor will decrease by about twenty per cent per year, because the number of transistors per package increases.

Summary
Undoubtedly there are many challenging tasks in store for the researchers. It would be regrettable, if only from the point of view of available resources, if national governments in Europe would engender local, subsidized IC industries which would all develop similar products. In this field also, European cooperation is of the utmost importance.

Extract from Philips press notice
Being able to see what a processor does as it runs a machine code program is a great aid in understanding the program, in fault finding, in testing, and in fact in everything a programmer does when developing some new software. The program given here makes it possible to do this automatically. At each step the contents of the CPU registers, the stack and its pointer are displayed for the corresponding instruction.

This program is aimed not only at users of the Junior Computer but also at the owners of any 6502-based system. It occupies about ¼ K of memory and uses two bytes in page zero. Very few changes are needed to adapt it to a system other than the Junior.

How is it used?

The program operates as a sort of 'step by step monitor.' This means in effect that any program the user wishes to analyse, or debug, is executed instruction by instruction with the contents of registers A, X, and Y, the status register flags (NV DIZC), and the stack pointer being displayed each time. It is notable from the list of flags (NV DIZC) that the 'break' flag is not included; the reason is that the '6502 TRACER' program accepts all instructions except those which are the result of, or which result in, an interrupt (BRK, IRQ and NMI).

As table 3 shows, it is much easier to analyse a program (the example here contains a lot of register and flag manipulations) with the aid of the information displayed by the tracer program in the three right hand columns. The first, at the extreme right, refers to the stack: SFF is the least significant byte of the pointer (the most significant byte is $01). Near the end of the listing there are a few addresses stacked during JSR or RTS instructions. The next column gives the logic levels of the status register flags NV DIZC. Finally, beside this the contents of the A, X, Y and processor registers are to be found. The step by step tracing of the program in these columns is followed in the first two columns by the disassembled listing of the addresses and instructions. The fact that all jumps and branches are included explains why the program returns from address $920D (DO/FA) to address $9209 but the Z flag remains low.

How does it work?

The length of this article does not give us the scope to provide a complete source listing of this tracer program, so we will have to be content with the hex dump shown in table 1. It is, however, quite important to have some pointers about how to use the software.

Before a run the start address of the program to be tested must be stored at addresses $800D and $800E which act as a pseudo program counter. The program under test may be in back-up memory but the tracer program must be in RAM; as shown here it starts at address $0508. Between addresses $0500 and $0523
several buffer bytes acting as a pseudo stack that starts at $0713 (we will return to this later) are initialized, the column headings are displayed and the IRQ vector is positioned (the IRQ routine begins at address $0526).

The tracing proper starts at $05A2, by displaying the program counter address, loading the op-code, filling the op-field with $06, and calculating the length of the instruction (the routine used begins at $06A9 and is quite similar to the LENACC routine in the Junior Computer). The op-field is a four-byte zone ($0619...$061C) where the analysis program places in turn each of the instructions of the program under test in order to execute them. As these instructions never contain more than three bytes they are always followed by at least one $00 and this function as a BRK.

Immediately after executing an instruction of the program under test, therefore, this BRK causes the IRQ routine at $0526 to be run.

The pseudo program counter ($00ED and $00EE) is incremented at $05DB. This incrementation depends on the format of the preceding instruction, with the number of bytes making up the instruction being stored in address $071E. Any jump instructions in the program must be filtered out to be dealt with separately and this begins at $05E6. From $050B onwards stacking of registers A, X and Y for the program under test starts. The op-field, located at $0619, contains the instruction to be analysed and because every instruction is always followed by at least one BRK it is also followed immediately by the IRQ routine. As could be expected, this begins by storing the conditions of the processor registers. Then it displays their contents and proceeds to the next instruction.

The special instructions for executing jump commands are located at $061D. The addresses for relative jumps are calculated at $0727 and $06A8. The addresses of the Junior Computer's PRBYT and PRCHA routines are contained in $06A1, $06A2, $06A6 and $06A7, so these must be changed if the program is to be used with a different 6502 system.

The commands for printing the headings of the columns are at $06CC to $0702. The format of each instruction that is to be run is determined by comparing it to the values contained in the look-up table located from $0703 to $0712. There are a number of buffers between $0713 and $0721 that are used by the tracer program to store the stack pointer, the contents of the top of the stack, the op-code under test, the number of bytes in the instruction, and so on...

These were the most important points about this program and the rest is easily deciphered with the aid of a disassembler.

### Table 2

<table>
<thead>
<tr>
<th>Address</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0100</td>
<td>200 23A</td>
</tr>
<tr>
<td>0101</td>
<td>123 456 789 09A BCD EFG</td>
</tr>
<tr>
<td>0102</td>
<td>0A9 0B0 0C0 0D0</td>
</tr>
</tbody>
</table>

### Table 3

<table>
<thead>
<tr>
<th>Address</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0200</td>
<td>27 02</td>
</tr>
<tr>
<td>0201</td>
<td>09 02</td>
</tr>
<tr>
<td>0202</td>
<td>1C 00 02</td>
</tr>
<tr>
<td>0203</td>
<td>6A 00 02</td>
</tr>
</tbody>
</table>

Table 2. These few instructions could be used to test the program of table 1. The results obtained should be the same as table 3.
A tachometer is probably the single most important 'meter' in a car’s dashboard (unless you’re in the habit of running out of fuel). It informs the driver how hard the engine is working and, when used correctly, it is an aid to economy, performance and engine longevity (to name but a few). These things are, of course, no less important to the driver of a diesel car than to his petrol-powered counterpart, but most electronic tachometers cannot be used with diesel engines. The reason for this is that they take their ‘timing’ from the ignition circuit, which diesel cars do not have. The engine speed of a diesel car can, however, be measured by 'picking the brains' of another part of the electrical system, namely the alternator.

The difficulty with fitting a tachometer to a diesel engined car has not escaped the car manufacturers' notice. Many diesel cars sold today have an extra (so-called 'W') connection available on the outside of the alternator, and the purpose of this is to enable the engine speed to be measured without unnecessary complication or cost. Petrol cars are, of course, not a problem as regards electronics. The supply is taken from the car battery via R1 and protection diode D1. The input resistance and input current (1.5 mA maximum) are defined by resistors R2 and R3. The pulse signal coming from the W connection is limited to 12 V by means of zener diode D2. Any high frequency noise that might be present is shorted to earth by C2. The signal is then fed to the inverting input of op-amp IC1 which operates as a schmitt trigger. The hysteresis of this schmitt trigger is about 6 V, and the signal at its output (pin 6) is a rectangular waveform with an amplitude of 6 Vpp and a frequency corresponding to that of the input signal. The signal oscillates about the 6 V line. Differentiating network C3/R8 converts the rectangular waveform into the 'peaked' signal shown at the junction of these two components. The positive peaks are limited to about 0.65 V by D3. The negative peaks, on the other hand, are used to trigger MMV IC2. The width of the output pulse from this 555 can be varied with P1 between 150 and 450 µs.

The output signal from IC2 is limited to 5.6 V by zener D4 and is then integrated by R11 and C6 before being fed to the moving coil meter M1. As a result of this integration, and also to a certain extent because of the inertia of the meter, M1 gives a stable read-out of the engine speed.
Construction and calibration

The printed circuit board layout for this circuit is shown in figure 2. The connection points from the circuit have purposely been made big so that the normal automotive type connectors and push-on clips can be used. No holes have been drilled in the board for the meter connections, but large copper areas have been left for this purpose. Holes can be drilled to suit the type of meter used, and the board can then be fixed directly to the rear of the moving coil meter. It goes without saying that the meter must be connected with the right polarity. The meter needs a suitable scale, of course; this could be made by using one of the dry transfer systems available.

There are three possible methods of calibrating the circuit (no, we don't mean do-it-yourself, get somebody else to do it, or don't do it at all). The handiest method is to use a hand-held tachometer, which can probably be borrowed from a garage (if you grease the right palms). If you also enlist the help of an assistant things will be considerably speeded up. Run the engine at about 2/3 of its maximum speed. Your helper measures the engine speed at the crankshaft with the borrowed tachometer and tells you what the reading is. You then adjust the Elektor tachometer to this value with P1.

The second method of calibration involves a bit of arithmetic but in this case no reference tachometer is needed. Knowing the rpm/mph ratios of the car in various gears enables you to calculate the engine speed corresponding to a certain road speed in a certain gear. Then find a straight level road and drive at a steady speed for which you have calculated the engine speed. Your (indispensable) helper now adjusts the tachometer to the appropriate reading. The disadvantage of this method is that you are using the car's speedometer as a reference so the reading is almost certainly going to be a few percent incorrect.

The third calibration method involves measuring the diameters of the pulleys on crankshaft and alternator carefully and thereby calculating the ratio of engine speed to alternator speed. An example of this is given in figure 3. From the technical
Figure 3. The ratio between the radii (radiuses?) of crankshaft and alternator pulleys can be used to determine the ratio of engine speed to alternator rotary speed.

Figure 4. The power/rpm and torque/rpm curves shown here tell a lot about the way an engine works. Studying them briefly can help a driver make the most intelligent use of a tachometer.

Table 1. Knowing the radii of the pulleys on the crankshaft (r1) and alternator (r2), the frequency of the signal given by the alternator at a certain engine speed (here 3000 rpm) can be calculated.

<table>
<thead>
<tr>
<th>Data:</th>
<th>r1 = 15 cm</th>
</tr>
</thead>
<tbody>
<tr>
<td>r2 = 12 cm</td>
<td>number of poles, p = 12</td>
</tr>
<tr>
<td>n = 3000 rpm</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Calculation:</th>
<th>f = \frac{r2 \cdot p \cdot n}{r1}</th>
</tr>
</thead>
<tbody>
<tr>
<td>f = \frac{12 \cdot 1 \cdot 3000}{15}</td>
<td></td>
</tr>
<tr>
<td>f = 375 Hz</td>
<td></td>
</tr>
</tbody>
</table>

The 'W' connection

Alternators that do not have a W connection as standard can often be modified using special adapter sets. (Bosch, for instance, market a kit, no. ET-1 127 011 062, for VW and Audi diesels.) The best thing to do is look at the make and type of alternator and then ask at the appropriate garage if an adapter kit exists. An adapter kit is not, however, strictly necessary. The rectifier in the alternator generally consists of a six-diode bridge as shown in figure lb. Points U, V and W are all located at the anode-cathode junction of two diodes. For our purposes there is no difference between the points and you can feed any one of them to the outside.

Using the tachometer

We are not, of course, going to tell you how you should drive, but nonetheless it may be no harm to see how a tachometer (any tachometer) can be put to its best use.

A lot of information about a car's engine can be gleaned by looking at graphs such as those shown in figure 4. These show the relationship between engine speed and both power and torque for a common diesel car, the Volkswagen Golf. The engine speed ranges from about 1000 to 5000 rpm. As one of the curves shows, the power rises almost linearly with (engine) speed up to about 4000 rpm. After this the power does not rise at the same rate so acceleration will be less. This is very important to know for overtaking, for example.

Torque is also dependent upon engine speed, but in this case maximum torque does not correspond to maximum engine speed. The engine is at its most efficient, and most economical, at maximum torque. This fact is used every day by people who wish to drive economically.

It is a common fallacy that only racing drivers need a tachometer. Certainly those for whom high speed driving is a profession do place a great importance on the information they get from the tachometer, but so can every driver on the road. Mechanical suffering is becoming more and more difficult to hear in today's well sound proofed cars, or at least that is the plea of the (obviously cloth-eared) driver who has his car ticking over at much too high a level and insists on thrashing it before it is fully warmed up. If you see him give him the message - don't put the pedal to the metal when the car is still cold. After all, can you work properly before you're well awake in the morning?
The essential ingredients for any self-respecting disco are well known, plenty of the right type of music, an abundance of coloured lights and gently top up the remaining space with people. Any hi-fi will provide the music but the light display is rather more specialized. There are of course many variations on the theme ranging from the mediocre to ‘way-out’ and invariably classified by price. The disco light display described in this article is a very advanced design with many desirable features but can still be built at a very reasonable cost.

programmable
disco light
display

Light displays are very popular for many applications other than discos. They are excellent in the home, for instance, as a means of providing ‘atmosphere’ at parties or social gatherings. They are also very useful for advertising purposes for the enterprising businessman. It cannot be denied that the more interesting a disco light display is, the more complex the electronics tends to be. This is mainly due to the fact that each light source, in most cases a mains powered lamp, must be controlled separately, resulting in a ‘channel’ usually consisting of some form of logic decoding, a mains interface, and a firing circuit. This channel must then be duplicated for however many lamps are involved. Regrettably, we have not been able to do away with this problem. Ironically however, it may be seen as an advantage simply because it allows for the easy expansion of the overall system – especially if the control electronics are designed with this in mind! It will become apparent that the circuit in this article can be as large as your imagination or your wallet allows!

A major disadvantage of the average disco light display is that the available light patterns are an integral part of the control circuit, possibly the contents of a memory IC, which must be purchased. This means that the pattern cannot be changed very easily, if at all. At this point we can start to sing the praises of the circuit here because this disco display is fully programmable. Furthermore, program changes can be made at any time by simply operating switches (no IC changes). The circuit also contains its own memory allowing up to 32 different programs to be stored. There are numerous other highly desirable features of the circuit that put this disco display on a totally different level from the average – including most commercial units. This list of do’s and don’ts explains all...

- Entirely user programmable at any time.
- Up to 30 channels can be accommodated.
- Program selection can be run fully automatically or manually.
- 8 switched program run times available.
- Internal memory divided into: 16 (2 ‘banks’ of 8) programs of 128 steps, or 32 (4 ‘banks’ of 8) programs of 64 steps.
- Overall size of memory optional.
- Battery back-up for memory.
- Programs, banks and current memory address indicated by LED displays.
- Opto isolation from mains.
- All lamps switched at zero-crossing point of mains to reduce interference.
- Personal choice of display configuration (a matrix configuration makes possible a display with 225 lamps!)

So much for what the circuit can do, now how about what it doesn’t do!
- It doesn’t cost an arm and a leg.
- It does not require any programming skill.
- It does not require a great deal of practical ability to build it.
- It doesn’t play the Hokey Pokey (although some may not consider this to be a major disadvantage) yet!

To sum up then, the circuit contains all of the desirable features (that we could think...
of at least) and yet it can be operated without 'computer' experience. The complete display can be as small or as large as desired; it may even be expanded at a later date.

Basic principles
Those readers who have already sneaked a quick look at figure 3 (this of course includes everybody) may be getting somewhat alarmed at what most articles would refer to as 'a slightly complex' circuit diagram. This impression is just a figment of the imagination as can be proved with the aid of the block diagram of figure 1.

Since it is the memory that holds all the information, this forms the heart of the circuit and all other 'blocks' either feed to or from it. The structure of the contents of the memory is illustrated in figure 2. It will be seen that it is divided into 'banks' (two or four depending on desired memory size) each of which in turn is divided into 8 programs. This simple method allows the total memory to be divided into reasonable program lengths and provides an excellent means of finding any given program quickly — especially if the program and bank counters are given 7-segment display read-outs! The address counter, as its name suggests, determines the address of that part of the program which is being displayed at any one time. Obviously the same can be said of the bank and program counters.

The block with the elegant title of 'mains sync' is a shade more subtle in both its activities and its purpose in life. Basically it provides a synchronization signal for the circuit at the frequency of the mains supply. Simple, you say — but wait. It also ensures that the clock signal is synchronized to the zero-crossing point of the mains frequency and, by doing so, it eliminates the need for all those zero-crossing detectors that usually accompany each lamp-switching triac in the mains interface of the display. The answer to the next question is that, since the clock is sync'd to the zero-crossing point of the mains, all data changes at the output of the memory will always occur at the same point. The lamps will therefore always switch on (or off) at the zero-crossing point!

One further point before we leave the block diagram. The printed-circuit board designs for the display drive circuits do not appear in this article but they should grace the next issue.

The circuit diagram
The mains zero-crossing point detector is formed by IC1 (gates N1...N3) in the circuit diagram of figure 3. The mains supply is present between the X and Z terminals and is applied to N1 via a variable frequency signal from N2. The inputs of N1 contain two diodes which chop the wave-form of the mains supply to provide a square wave with an amplitude that is equal to the supply voltage of IC1.

The output of N1 is differentiated by means of C1/R5 and C2/R6 and fed to the two inputs of N3. The resulting output of N3 is a pulse of about 200 µs at every zero-crossing point of the mains frequency. This pulse is then fed, via a driver transistor, T1, and an opto-coupler, IC2, to the clock input of FF1. This ensures complete isolation between the mains supply in the zero-crossing detector stage and the rest of the circuit.

Function table
S1: A - RUN MODE
B - PROGRAM & DATA switches
S2: STEP (Increment)
S3: BANK increment (+1)
S4: BANK automatic increment ON/OFF
S5: PROGRAM RUN TIMES in minutes
S6: MANUAL PROGRAM increment (+1)
S7: DATA WRITE
S8: WRITE PROTECT (key switch)
S9: Mains switch
S10: RESET switch
S11...S40: DATA switches
P1: RUN speed control

Figure 1. The block diagram of the programmable disco light display. Memory size can be chosen by the user.

Figure 2. This illustrates the manner in which the memory is structured to provide easy access to any program.
Figure 3. The circuit diagram shown here of the disco light display includes the full complement of four memory ICs. Initially only one need be used and the memory can be expanded at a later date with the addition of more.
display programmable disco light

The program counter can also be incremented by one step at a time by means of switch S6 which, incidentally, overrides the timer output. It should be realized that if S5 is switched to one of its off positions, any given program will run indefinitely until it is changed manually by S6.

The remaining half of IC8 (IC8b) forms the bank counter which, depending on the program size, continually counts up in either 2 or 4 steps. This counter can also be stepped manually by means of pushbutton S3. To obtain fully automatic operation, that is, a continuous cycle through all the programs in the memory, switch S4 can be closed and at the highest program count, the bank counter will be incremented by one. It will be seen that the counters for program and bank are interconnected via an OR gate, N8. This ensures that each time either the bank or program counters are updated the address counter is reset to zero; after all, it is only reasonable that a new program should begin at the beginning! For those who are wondering what that strange little thing perched on the line to S4 is, it is simply a redundant gate.

We now come to the memory itself, of which the full complement of four 2K-CMOS-RAMS are shown in the circuit diagram (IC10 ... IC13). In normal operation these are of course in the 'READ' mode and the contents of the address determined by the address, program, and bank counters, are used to switch on (or off as appropriate) the output to the display itself. Normally then, the R/W pins of each memory are held high by resistor R23. This line must therefore be taken low whenever a program is to be entered or modified and this is carried out by switch S7 via switch S8. Switch S8 is a safety 'lock-out' key switch which, although not absolutely necessary, is strongly recommended to prevent accidental damage to a program. How and when to use S7 will be covered a little later on.

The power supply for the memory ICs is taken from the 5 V line via diode D2. Should the 5 V supply fail (when the equipment is not in use for instance), the 4.5 V battery will preserve the contents of the memory via D3. At the same time, the absence of the 5 V supply will switch off transistor T2 and inhibit the memory outputs by causing the CE inputs of the memory ICs to go to logic 1 via resistor R24. In short, the memory will be inoperative (in the low power mode) but the contents of the memory will be preserved. The current consumption is so low in this condition that the battery will last quite literally for years but should still be changed every 12 months or so. A NiCd (three cells of 1.2 V) can also be used in which case resistor R18 (270 Ω) is required to provide a charging current. This resistor is not needed with a dry battery.

Each of the data lines of the memory ICs is led to the LED in an opto-coupler on the triac board via a driver, N15 ... N45, and an indicator LED. The indicator LED provides a direct read-out of the data at that particular address. This is of course essential during programming. The data lines are also fed to the programming switches S10 ... S40 via resistors. When S7 is pressed, and S8 is switched on, the data set by these switches is written in the memory at the address indicated.

One final detail before we leave the circuit diagram of figure 3. The D0 output of IC10, switch S10, and the associated LED via driver N15 all have a particular significance. It will be seen in 'programming' below that the length of a program (or sequence) can be a maximum of 128 or 64 steps. However, this may be more than required and therefore some means of programming the end of a sequence and returning to the beginning must be provided. This is where the data line D0 of IC10 comes in. In the normal course of programming D0 will be logic low until the end of a sequence when a 1 will be entered at this location (by S10). When the display is up and running, a 1 appearing at D0 will be synced with the address oscillator by FF2 and used to reset the address counter to zero via N8. The display sequence will then start from the beginning again. LED D8 serves to indicate this 'reset' pulse when it occurs.

The reset bit (D0 of IC10) is not synced with the zero-crossing-point pulses. However, as the reset only occurs at the end of a program, this will cause negligible inter-
The circuit diagram for the four LED displays, LD1...LD4, is shown in figure 4. The printed-circuit board layout for this circuit is shown in figure 6. The address reference A0...A10 refer to those at the right of the main circuit diagram of figure 3. An appropriate link must be made to set the program step-length at the input to the decoder for LD3. If the program step-length is 128 steps, transistor T1 switches on the decimal point of LD1 for address counts above 63.

Construction
If the printed-circuit boards illustrated in figures 5 and 6 are used, construction of the electronics section of the disco display should prove no problem. However, before assembly can begin, the final design format must be decided upon. This refers in particular to the LED read-out display board which, it will be noticed, can be divided into three separate sections. This has been done to allow the maximum flexibility of the design as it was considered that many readers may wish to build the display controller into an existing piece of equipment. The complete printed-circuit board as shown in figure 6 will match the suggested front panel design illustrated in figure 7.

After assembly has been completed, not forgetting the two links (64 or 128 step program length), the two boards should be interconnected. This can be carried out by short lengths of wire or, if preferred, ribbon cable can be used. All the address lines as marked on the two boards, with the exception of A6, must be connected. For a 64-step program this is taken to the point marked A6 on the board containing display LD3. If a 128-step program has been chosen, it must be connected to A6 on the board containing displays LD1 and LD2.

There are three + terminals and three - terminals on the display board. These are separately interconnected: one + and one - is connected to the + and 0 terminals respectively on the main board near C12. If the display board is separate, each + and - should be connected with the + and 0 on the main board. The common point for the anodes of the indicator LEDs should be taken to the + terminal near C12. The cathodes are connected to channel outputs 1...30. Another set of + and - terminals will be found on the main board: these are for the switches. The switch connections should preferably be commoned after the switches have been mounted on the front panel as this requires only two wires to be returned to the main board.

Normally, the channel indicator LEDs are connected in series with the LEDs in the opto-couplers on the triac board. To enable the circuit to be tested at this stage, some form of current limiting must therefore be included as a temporary measure. Two diodes type 1N4001 are therefore connected in series with the 5 V supply and the common anode connection of the indicator LEDs. The LEDs should have a forward voltage of about 1.6 V. If the indicator LEDs are dispensed with and only the opto-coupler LED is used, the display pattern is, of course, shown by the display itself: resistors R58...R87 should then be 330 Ω. It will be remembered that the supply for the mains zero-crossing point detector is derived from the triac control board: this

<table>
<thead>
<tr>
<th>Max. no. of channels</th>
<th>ICs required</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>7</td>
<td>10-1-15</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td>10-1-1-14-15-16</td>
</tr>
<tr>
<td></td>
<td>23</td>
<td>10-1-1-12-13-14-15-16-17</td>
</tr>
<tr>
<td></td>
<td>30</td>
<td>10-1-1-12-13-14-15-16-17-18</td>
</tr>
</tbody>
</table>
will be clarified in the next issue when the triac unit as a whole will be described. To enable the main board to be tested at this stage, the zero-crossing point detector can be supplied from the main board. DO NOT FORGET to remove these connections when the triac board is connected. The supply connections are: X to + and Y to 0 (near C12) and Z to one of the secondary a.c. terminals of the mains transformer (that is, one of the − terminals on the main board).
Programming
When the circuit is first switched on (prior to any programming), the memory ICs will contain garbage, but you knew that, of course! Display sequences will obviously depend on the contents of the memory and the chosen program format (64 or 128 steps). Further-

Parts list:

Resistors:
R1, R2, R8, R23 ... R25 = 47 k
R3, R13, R14 = 100 k
R4, R19 = 1 k
R5, R6 = 22 k
R7, R22 = 4 k
R9, R11, R17 = 470 k
R10, R12, R18 = 470 k
R15 = 150 k
R18 = see text
R20 = 56 k
R21 = 220 k
R26 ... R56 = 4 k
R57 = 330 k
R58 ... R97 = 160 k

Capacitors:
C1, C2 = 6 nF
C3, C7, C11 = 1 μ/10 V
C4, C5, C9, C10 = 100 n
C6, C8 = 1 n
C12 = 1000 μ/25 V
C13 = 10 μ/10 V

Semiconductors:
T1, T2 = BC 5478
D1 = red LED
D2, D3 = 1N4148
D4 ... D7 = 1N4001
D8 = LED
Optional: 30 LEDs for channel indication:
IC1, IC3, IC5 = 4053
IC2 = TIL 111
IC4 = 4075
IC6 = 4013
IC7, IC9 = 4040
IC8 = 4520
IC10 ... IC13 = 6116 or 5517
IC14 ... IC18 = ULN 2003
IC19 = 7805

Miscellaneous:
P1 = 1 M linear potentiometer
P2 = 1 M preset
S1 = single pole two-way toggle switch
S2, S3, S6, S7 = push-to-make switch
S4 = single pole toggle switch
S5 = 12 way wafer switch
S8 = single pole key-lock switch
S9 = double pole mains toggle switch
S10 ... S40 = single pole two-way toggle switch
Tr1 = mains transformer
4 V ... 12 V, 800 mA secondary
4.5 V battery
F1 = fuse 500 mA slow
Heatsink for IC19 (SK13, K105)
Printed-circuit board 84007-1

NOTE: remember that some components are not required and others in smaller numbers if all channels are not used.
more, a full memory will allow a total of 30 channels (lamps) and these can be arranged in any number of pleasing designs including a dot-matrix for alpha-numerics (that means letters and numbers, sir!).

Having decided upon the display format and the sort of programs that are to be used, the links at the A6 address line must be fitted as described under 'construction'.

Before starting the programming, it is advisable to commit the desired sequences or patterns to paper as even 64 steps can get decidedly confusing.

To adjust preset P2, set switch S5 in position ½ (minute) and adjust preset P2 so that the program display jumps on every 30 seconds.

Off we go then. Set switch S1 to position B (step mode), S4 to OFF, and S5 to off to prevent the program from jumping on during loading. Switch on the switch-key S8 and press S6 and S3 to get the right program and bank. The address display should read 00; if not, press S3 or S6 until the right program and bank are indicated on the display. The program data is set by switches S10 ... S40 (or whatever number you have decided upon). Any one of these switches set to 5 V denotes a logic high and causes the appropriate lamp to light. A switch set the other way gives a logic 0 and the corresponding lamp does not light. Are you still with us?

Set the program data and press switch S7. The data lines are now inputs and the memory ICs will be fed with a write pulse and accept the data set with the switches. When S7 is released, the data lines revert to being outputs and the set pattern will be indicated by the channel LEDs. Now press S2 once (to increment the address by one), set the data switches, and again press S7. If an error was made during the entering of...
the data, simply set the correct data and press S7 again. This works, however, only before S2 has been pressed. If S2 has been operated, press S6 until the same program is indicated on the display. Then go to the faulty address by means of S2, alter the data, press S7, and proceed to the next address by pressing S2.

As mentioned previously, data line D0 will remain logic low until the end of a pattern. On the address following the last line of the sequence, set S10 to 5 V (logic high); this can also be done on the last line of the sequence itself (together with the program data) if preferred. With some display patterns (especially running light patterns) it improves the display continuity, but it really is a matter of choice. Try some simple patterns to see the effect. And that's all there is to it apart from a few pointers.

At the end of the programming, do not forget to switch off the key-switch otherwise (in the case of disco's) you might find yourself arriving at a booking with this terrific new display you have been raving about only to find that you have a completely garbled memory. Not good for the old ego, chaps! Don't be too worried about making a false entry during programming as mistakes can be easily rectified. You do not have to reprogram the entire memory, just the line containing the error. Unless of course, you have a major disaster on your hands. In this case, turn the telly off and lock the door before starting!

It is possible to include delays and acceleration in your program by repeating the same data in several addresses. This makes a very effective display when properly done but it does require careful planning with due regard to program length (64 or 128 steps). Remember not to be caught out by the address counter read-out. This just indicates from 0 to 63. If a program length of 128 steps is opted for, the decimal point of LD1 signifies the 'upper' 64 step range.

Set S1 to position A when the program should run; adjust the run time with P1. It may happen that when the run time is increased (that is, smaller resistance of P1), the pattern on the display does not run smoothly (stutters) or even stops altogether. This is caused by the frequency of N4 being too high in relation to that of the zero-crossing pulses. Because the trigger levels of different makes of 4093 show wide variations, this erratic running may or may not occur. The adjustment range of P1 should be set by means of R8 and/or C3 so that stuttering or stopping of the pattern just does not occur.

A point worth noting! The disco display is completed, programmed, and ready to go to work... However, when it is switched on, nothing happens: no lights, no LEDs, just panic! Fear not, gentle DJ, all will be as it should be if you just press the program step switch, S6, and a program will start from the beginning.

To end, we are sure you don't need reminding that the mains supply is a little 'conspicuous' in this circuit. Please take care, as we have no desire to reduce our circulation by stopping yours!
The video combiner is a circuit which 'welds' the various components of a video signal, such as the synchronizing pulses, blanking signal, colour information, and so on, into a composite video signal. Although this is a fairly complex matter, a recently introduced integrated circuit, the TEA 1002, makes it possible to keep the combiner reasonably simple.

The TEA 1002 is a PAL colour encoder with video combining stages. It converts a number of appropriate input signals into a complete video signal, that is, one containing synchronizing pulses for the line and field scans, luminance and chrominance signals, blanking pulses, and a colour burst signal.

The required input signals are derived from the 'video sync box' described elsewhere in this issue. The printed-circuit boards for that box and the present circuit are of the same dimensions so that they can be built conveniently into one unit.

The TEA 1002

The 'innards' of the TEA 1002 are shown in schematic form in figure 1. The logic decoder generates colours according to the logic levels at pins 1...4 (see table 1). If only black and white signals are required, pins 2...4 are simply strapped together. In that case, neither the chrominance subcarrier oscillator (pins 13, 14) nor a signal at the CBF (colour burst flag) input (pin 15) is required.

The circuit diagram

The circuit may be divided into three parts (see figure 2): the PAL switch (FF1), the combiner proper (IC2), and a buffer stage (TI).

The PAL switch, flip-flop FF1, is controlled by the line synchronizing pulses at its clock input (pin 3). (See also 'video sync box' elsewhere in this issue.)

The TEA 1002 (IC2) contains a chrominance (chroma) and a luminance encoder. The luminance is dependent on the voltage level at pin 8, which is preset by Pi. If this voltage is greater than 4 volts, a 75 per cent colour signal (as defined by the EBU - European Broadcasting Union) is generated. When the voltage falls below 3 volts, the brightness is increased to 95 per cent, which, no doubt, will normally be preferred as it gives a clearer picture. It should be noted that the voltage at pin 9 should not rise above 5 volts to prevent saturation of the buffer, TI.

The TEA 1002 also contains a divider which produces a 3.54 MHz clock signal from the 8.86 MHz subcarrier oscillator. The clock (pin 17) may be used to synchronize other circuits. The oscillator can...
be pulled to its correct frequency by adjusting capacitor Cl for minimum interference (least ragged image fringe). Setting Cl to its mid-position will in practice normally be sufficient.

The output level of the buffer stage, emitter follower T1, is preset by means of P2. With values shown, the output impedance is around 75 ohms. The output level is normally adjusted to give 1 Vpp across 75 ohms, that is, 2 Vpp emf.

Construction and application

The printed-circuit board, shown in figure 3, has the same dimensions as that for the video sync box, so that the two boards can conveniently be built into one compact unit. The various terminals on the boards are located such that the length of the interconnecting wires is kept to a minimum. The circuits should, of course, be preset before making the interconnections.

The board has provision for an optional wire bridge. If this is used, the logic levels at pins 2...4 ('0') produce standard colours and the chrominance signal is at normal level. If the wire bridge is omitted, the colours are inverted (see table 1) and the chrominance signal is reduced by 6 dB.

Power supply requirements are 12 V at 100 mA maximum.

The combiner lends itself to a variety of applications. For example, when used with a personal computer with video interface which has colour information available (in the form of Red, Green, and Blue signals) it makes possible the production of a composite video signal.

In combination with the video sync box, the combiner can produce a colour bar which is suitable for use as a test signal, as a space marker for video recorders, or with local cable systems. For these uses, the R, G, and B pins on one printed-circuit board must be linked to the corresponding ones on the other board.

Finally, the combination may in appropriate cases form the link between electronic equipment and a colour TV.

Table 1. Correlation between logic levels at pins 1...4 and the colour produced.

<table>
<thead>
<tr>
<th>pin 2</th>
<th>pin 3</th>
<th>pin 4</th>
<th>pin 1</th>
<th>colour</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>black</td>
</tr>
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<td>1</td>
<td>red</td>
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<td>0</td>
<td>green</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>yellow</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
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</tr>
<tr>
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<td>1</td>
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</tr>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>black</td>
</tr>
</tbody>
</table>

1) red-blue
2) blue-green

Figure 2. From this circuit diagram it is evident that once all the complex functions are performed by the TEA 1002, the remainder of the design becomes relatively simple.

Figure 3. The printed-circuit board for the video combiner. Note the wire bridge described in the text near the centre of the board.
The testing of digital circuits can be quite a headache. Our old faithful, the multimeter, is quite useless because of the operating frequencies: the logic levels change so rapidly — thousands or millions of times per second — that even a digital multimeter is unable to cope. This problem can be solved in two ways: buy a higher quality test instrument or lower the operating frequency of the circuit under test. If you opt for the last, you will find our digitester just the thing!

**digitester with a difference**

universal test aid for digital circuits

Digital circuits normally operate at speeds which make it impossible for normal test instruments to be used for checking or fault finding. For instance, in an analogue multimeter, the inertia of the pointer prevents the reading of the level of a pulse train. The normal digitester does not help here either; it may well give an optical indication of the logic level at the pin of an IC, but only as regards a static or slowly changing situation. When rapid changes occur, the digitester is also quite useless. This is, however, not because of inadequacies in the instrument, but rather because of the slowness of our eyes. When an LED blinks at only 20 Hz, few of us see this as a series of light pulses: most will just see a continuous light.

It is by now evident that to test digital circuits or to be able to experiment with them it is necessary to slow down the speed of operation. The easiest way to do this is to disable the internal clock of the circuit and replace it by an external one operating at a much lower frequency. In some cases, it is even better to work with just one pulse at a time, instead of with a pulse train.

Apart from single pulses, there is, of course, a need for low-frequency pulse trains. The generator required for this is formed by NAND Schmitt trigger N9, resistor R13, and capacitor C1. With values shown, the frequency is around 50 Hz. A second pulse-train oscillator, formed by N10, R14, and C2, operates at the much lower frequency of 2 Hz, which is optically indicated by LED D5.

So much for the description of the required generators. But what if you want to apply a single pulse followed by a pulse train to a circuit? It would not do to have to change from one output to another. No, for this purpose we have added an electronic switching circuit consisting of S3, NOR gates N5...N7, NAND Schmitt Triggers N8, N11, and NAND gates N12/N13 and N16/N17. The output, pin 8 of N17, depending on the setting of S3, is either the Q2, the 2 Hz, or the 50 Hz signal. The logic output level is optically indicated by LED D6:

- If D6 lights continuously and independent of the setting of S2, the output is a 50 Hz pulse train;
- If it blinks rhythmically, the output is a 2 Hz pulse train;
- If it lights depending upon the setting of S2, the output is the logic level of Q2.

All outputs are buffered, which enables up to 30 TTL circuits to be connected to them. Finally, the function of switch S4. When this switch is open, the output of N17 is open, that is, it contains the signal selected by S3. If S4 is closed, however, the output of N17 is logic low and the signal selected by S3 is therefore not available at pin 8.
Construction

As you have seen from the circuit diagram, the digitester needs a supply of 5 V. This is best obtained by means of a 5 V voltage regulator: a 500 mA type will do nicely. The supply voltage to each of the ICs should be individually decoupled by a 100 nF capacitor.

The power supply is best built into a case together with the digitester so that you have an independent, self-contained test instrument for digital circuits.

If you want to use the digitester with CMOS circuits, it will be necessary to adapt the (TTL) outputs to the CMOS logic under test. This is relatively simple and is described in some detail in the article 'mating logic families' elsewhere in this issue.
Almost every new car manufactured in the world today is fitted with reversing lights. Great idea! Not only do they help you see where you are reversing in the dark, but they also make your intentions clear to anybody behind the car. In some Asian countries it is even a legal obligation for every car to have an externally audible reversing indicator. The one problem with these ideas is that the car driver does not directly benefit from them.

reversing buzzer

It is an undeniable fact of human nature that we often forget or neglect the care and caution instilled into us while learning a new skill. Nowhere is this more obvious than in driving a car. We frequently tend to do what is convenient rather than what is correct. Just one small, but common, 'fault' is starting the car in gear with the clutch depressed. Then you only have to release the clutch and away you go . . . But in which direction? It can prove very 'surprising', to say the least, when you expect to move smoothly forwards but instead find the driver of the 'slightly shortened' car behind you tapping on your window to express his opinion of your character in a somewhat heated manner.

The circuit

The circuit here also gets excited when you start the car in reverse gear but all it does is buzz at you in displeasure. When the ignition is switched on the car battery voltage is applied to the circuit and the oscillator around N2 starts. This provides one of the inputs to N3. If the car is in reverse gear, this last line must have +12 V when the reversing lights are lit. This provides an externally audible reversing indicator. The one problem with these ideas is that the car driver does not directly benefit from them.

reversing buzzer

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The circuit

The circuit here also gets excited when you start the car in reverse gear but all it does is buzz at you in displeasure. When the ignition is switched on the car battery voltage is applied to the circuit and the oscillator around N2 starts. This provides one of the inputs to N3. If the car is in reverse gear, the second input of N3 is taken high via R7, and this causes the buzzer to sound.

Simultaneously, pin 12 of the CD 4060 is taken high and this chip is reset. This IC is a 14-stage binary counter and oscillator, the frequency of which is set by external components (C2, R3 and R4). After a certain time (about six seconds), the Q13 output (pin 3) of IC1 goes high and stops oscillator N2 by taking its input (pin 5) low via N1. This, of course, stops the buzzer and ensures that it does not sound every time the car is put into reverse gear, which would be very annoying.

An alternative to using the buzzer is the small circuit shown in figure 2, consisting of a loudspeaker driven by a darlington pair. Transistors T1 and T2 may also be replaced by a single-package darlington such as a BC516.
How accurate is your watch?
(January 1984, page 1-22)
The photo transistor at the input of the block diagram (figure 1) is designated T1: this should be T2. In the circuit diagram (figure 2) C16 is stated to be 1000 V/25 µ; this should, of course, be 1000 µ/25 V.

VDU card
(September 1983, page 9-38)
The top left-hand of page 9-45 should read: for correct operation with the VDU card, so:
- pin 18 of IC4 should be joined to pin 20;
- the following connections should be made: M-J, G-I, F'-G', J'-L'; G'-N', O-M.
The following pages contain the mirror images of the track layout of the printed circuit boards (excluding double-plated ones as these are very tricky to make at home) relating to projects featured in this issue to enable you to etch your own boards.

- To do this, you require: an aerosol of 'ISOdraft' transparentizer (available from your local drawing office suppliers; distributors for the UK: Cannon & Wrin), an ultraviolet lamp, etching sodium, ferric chloride, positive photo-sensitive board material (which can be either bought or home made by applying a film of photo-copying lacquer to normal board material).
- Wet the photo-sensitive (track) side of the board thoroughly with the transparent spray.

- Lay the layout cut from the relevant page of this magazine with its printed side onto the wet board. Remove any air bubbles by carefully 'ironing' the cut-out with some tissue paper.
- The whole can now be exposed to ultra-violet light. Use a glass plate for holding the layout in place only for long exposure times, as normally the spray ensures that the paper sticks to the board. Bear in mind that normal plate glass (but not crystal glass or perspex) absorbs some of the ultra-violet light so that the exposure time has to be increased slightly.
- The exposure time is dependent upon the ultra-violet lamp used, the distance of the lamp from the board, and the photo-sensitive board. If you use a 300 watt UV lamp at a distance of about 40 cm from the board and a sheet of perspex, an exposure time of 4...8 minutes should normally be sufficient.
- After exposure, remove the layout sheet (which can be used again), and rinse the board thoroughly under running water.
- After the photo-sensitive film has been developed in sodium lye (about 9 grammes of etching sodium to one litre of water), the board can be etched in ferric chloride (500 grammes of FeCl₃ to one litre of water). Then rinse the board (and your hands!) thoroughly under running water.
- Remove the photo-sensitive film from the copper tracks with wire wool and drill the holes.
The problems of address decoding in a microprocessor system are generally summarised in the question 'where, when and how is the memory accessed?'. Our first article on address decoding did not answer the 'when' part of this question. For this reason we decided a second article was needed to deal with the timing of operations and signals. We also decided to have a look at an example of modifying an existing decoding system.

memory timing

A logic combination of most significant address lines can be used to provide an enable signal that is only active for certain configurations of the lines used. As we have already seen in our first article, this signal is applied to one or a number of memory ICs accessed by the least significant address lines, which, in fact, control the chip's internal address decoder. Data is transferred via the data bus. No matter how high the clock frequency of the processor, the address and data signals do not appear either instantaneously or simultaneously. On the one hand there is always what is known as a set-up time for the signals and on the other hand even the clock signal itself takes a finite time to appear. This is an added complication, but fortunately the difficulties are somewhat reduced by the presence of control signals supplied by the processor. These signals are used to synchronize the address decoding and read or write operations.

Timing of Z80 and 6502 signals
As the timing diagram of figure 1 shows, the MREQ, RD and WR signals of the Z80 do not appear at the beginning of read or write operations. When the MREQ and RD signals are not 'low' during a read operation (left half of the timing diagram), the address signals A0...A15 cannot be considered stable. The same applies to a write cycle when MREQ is not active. The upshot of this is that the MREQ signal and address decoding signal must always be combined before being applied to a memory IC. As the right half of figure 1 shows, the WR signal is followed after a significant delay by MREQ and the beginning of the phase to establish the data signals. These latter can only be considered stable after WR appears. It should be noted that the WR line becomes inactive again half a clock cycle before the address and data words change (T3 of the write cycle). The WR signal could also be used as to change the memory from read to write mode and vice versa (R/W).

The timing diagram for Z80 signals corresponding to an input/output instruction is shown in figure 2. Note in passing the presence of a spontaneous wait cycle generated by the processor itself to allow the generally slow input/output circuits to produce a WAIT signal if necessary. Here again, the address and data signals can only be considered stable after the appearance of control signals.

In the 6502 timing diagram shown in figure 3 the essential enable signal is 82. As soon as this signal is 'high' the address signals, and, immediately after them, the data signals, can be considered stable. The same is true of the signal to change between read and write modes (R/W). As this processor has no specific I/O instructions, it also lacks any particular control signals for this type of circuit. A RAM-R/W signal is often found on 6502 systems, and this is obtained by combining the 82 and R/W signals. This can then be applied as and when desired to memory ICs to change between reading and writing. For EPROM chips the 82 is combined with the address decoding signal (this is shown as gates N41 and N44 on the interface card of the Junior Computer). For inputs/outputs, various combinations of 82, R/W and the address decoding signal are possible. The R/W signal (and possibly 82) could also be used for switching the bi-directional data buffers (the READ and WRITE mode-switching signals on the Junior Computer interface card are obtained from, among others, the R/W signal). We must stress the importance here, for the designer, of carefully noting the timing of the control signals which must be catered for by the logic for decoding and enabling memory ICs.

Modifying an existing decoding system
After so much theory we will now deal with a practical example of using an existing system: the interface card of the Junior Computer, in fact. The aim of the modification is to reduce the importance of the doubly addressed zone between F800 and F9FF (or 1800...19FF in the DOS ver-
The existing circuit allows small modification to address decoding. A zone to be made smaller has only a fairly 'coarse' on the JC interface card considered stable. The 6522 VIA (IC1 on the interface card) occupies addresses F800 ... F9FF (1800 ... 19FF), but this is a bit wasteful as 16 addresses are sufficient to address all the registers of this IC. The K6 signal is active between F800 and F9FF (1800 ... 1BFF). Address line A9 permits the zone of F800 ... F9FF occupied by the VIA to be distinguished from the FA00 ... FBFF (1A00 ... 1BFF) area occupied by the 6532 on the main board. It would be nice to 'regain' the unused addresses for a new input/output circuit, as long as there are not too many modifications required. Looking at the 'circuit' of figure 4, we recognize it as a section of the circuit for the interface card containing the VIA, gate N35 and PROM IC17. Signal K6 applied to the CS2 input is active between F800 and F9FF (1800 ... 1BFF), while the CS1 input receives a signal called VIA (active at logic 'high') obtained from K6 and address line AB9, between F800 and F9FF; this same signal is applied to the PROM and thus enables the buffers in read or write mode while the address signals are present on the bus. Every little detail must be taken into account! The same components are seen in figure 5, along with a new 6520 PIA and a slight modification to the address decoding. The VIA signal is unchanged; it is still applied to the CS1 input of the 6522 and to the PROM (if this signal were modified then so also would the enable signal for the bi-directional buffers be changed). The CS2 signal for the 6522 is now supplied by AB8, and this means that the VIA no longer occupies addresses F800 ... F9FF (1800 ... 1BFF). Line AB8 is also connected to the CS0 input of the 6520 PIA for which our VIA signal (still obtained from K6 and AB9) provides the CS1 signal (active logic high, just like CS0). The third enable input of the 6520, CS2, is activated by the AB9 signal, so that the PIA is addressed between F900 and F9FF. This IC can be put anywhere as long as it is after the bi-directional data buffers (IC11 and IC12 of the interface board). Table 1 shows a summary of the operation of the new configuration in the form of a truth table. Instead of mounting the new PIA on the bus, it could also be soldered directly on top of the 6522 on the interface board. This operation, relatively perilous in itself, has the advantage that is makes things much simpler. The lines common to both ICs are DB0 ... DB7 (pins 33 ... 26), RES (pin 34), φ2 (ENABLE; pin 25), +5 V (pin 20), earth (pin 1), R/W (pin 22 of the 6522 - pin 21 of the 6520), RA3 (AB8; pin 38 of the 6522 - pin 36 of the 6520), R1 (A1; pin 37 of the 6522 - pin 35 of the 6520) and IRG (pin 21 of the 6522 - pins 37 and 38 of the 6520). The connection between K6 and pin 23 of the 6522 (CS2) must be broken; this pin is then connected to AB8. Pin 23 of the 6520 (CS2) must be connected to AB9, pin 24 (CS1) to the VIA line (pin 24 of the 6522), and pin 22 (CS0) to AB8 (pin 23 of the 6522).
Finally, we must give some indication about how to access the registers of the 6520 PIA.

The addressing is as follows:
- SF900: PAD or PADD (data or direction register A)
- SF901: CRA (command register port A)
- SF902: PBD or PBDD (data or direction register B)
- SF903: CRB (command register port B)

When the CRA bit is high, the register addressed at SF900 is PAD, the data register. If this bit is low, the register addressed is PADD, the data direction register. The same applies for CRB, with PBD and PBDD.

In spite of this somewhat peculiar addressing method, the operation of the 6520 ports is the same as those of the 6522 except for some details (essential for some applications) which will not go into here. Complete information on the 6522 is, in any case, contained in the Elektor book about this IC.
Connecting digital ICs within the same logic family will rarely cause any problems, as long as such things as fan-out and parasitic line and input capacitance are taken into account. It is quite a different matter, however, to try to use the different logic families, TTL (standard, LS and ALS) and CMOS, together. There is a great temptation to do just this as the possibilities for combinations becomes even greater with logic families continually being expanded. The new family of high speed CMOS (HCMOS) recently released onto the market prompts even more questions about the compatibility of its two variations with existing logic circuits. Maybe a lot of problems will be solved if we simply answer the question 'How digital is digital?'.

The popularity of digital electronics is very easy to understand. What could be simpler than a system in which there are only two values, '1' or '0'? Certainly this makes design and fault finding much simpler, but there are also some other considerations. As long as the elements of a design are kept 'in the family', with only TTL or only CMOS, for example, the manufacturers have already sorted out the problem of matching different gates. The logic levels are well defined and the input and output currents are virtually the same. Combining different logic families, however, is a completely different kettle of fish. Then our old friend Murphy appears with a vengeance and seems to have taken a personal dislike to your design, whatever it is. With a bit of determination, however, even Murphy can be defeated (temporarily at least).

How the families compare

There are, of course, some advantages to having different logic families. It becomes easier, for instance, to combine speed

<table>
<thead>
<tr>
<th>series</th>
<th>TTL</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>7400</td>
<td>74LS</td>
</tr>
<tr>
<td>supply voltage</td>
<td>5 V</td>
<td>5 V</td>
</tr>
<tr>
<td>dissipation per gate</td>
<td>10 mW</td>
<td>2 mW</td>
</tr>
<tr>
<td>gain delay time</td>
<td>10 ns</td>
<td>10 ns</td>
</tr>
</tbody>
</table>

Table 1.

Possibilities for combination

First we will see which families are matched purely on the basis of input and output levels. Most notable is the fact that interconnecting elements within the TTL group causes no problems. In one case the noise margin is even improved; this happens if LS or ALS is used in place of standard TTL.

Connecting TTL to HCTMOS is no problem either as this version of high speed CMOS is TTL compatible. Furthermore the user does not even need to know he is working with CMOS because its gates appear to be extra-efficient LS/TTL devices. The supply voltage tolerance with HCTMOS is larger than with TTL (10% instead of 5%), which simply means that the
Table 2.

<table>
<thead>
<tr>
<th>VCC</th>
<th>TTL</th>
<th>LSTTL</th>
<th>ALSTTL</th>
<th>CMOS</th>
<th>HCTMOS</th>
<th>HCMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>5 V ± 5%</td>
<td>5 V ± 5%</td>
<td>5 V ± 5%</td>
<td>3 V</td>
<td>18 V</td>
<td>5 V ± 10%</td>
</tr>
<tr>
<td><strong>UIH</strong> - logic 1 input level (min.)</td>
<td>2.0 V</td>
<td>2.0 V</td>
<td>2.0 V</td>
<td>3.5 V</td>
<td>2.0 V</td>
<td>3.15 V</td>
</tr>
<tr>
<td><strong>UIL</strong> - logic 0 input level (max.)</td>
<td>0.8 V</td>
<td>0.8 V</td>
<td>0.8 V</td>
<td>1.5 V</td>
<td>0.8 V</td>
<td>1.1 V</td>
</tr>
<tr>
<td><strong>UOH</strong> - logic 1 output level (min.)</td>
<td>0.5 V</td>
<td>0.5 V</td>
<td>0.4 V</td>
<td>0.4 V</td>
<td>0.4 V</td>
<td>0.4 V</td>
</tr>
<tr>
<td><strong>UOI</strong> - logic 0 output level (max.)</td>
<td>1.6 mA</td>
<td>0.36 mA</td>
<td>-0.2 mA</td>
<td>0.005 μA</td>
<td>-1.6 mA</td>
<td>-0.36 mA</td>
</tr>
<tr>
<td><strong>IL</strong> - input sink current (max.)</td>
<td>40 μA</td>
<td>20 μA</td>
<td>20 μA</td>
<td>0.005 μA</td>
<td>40 μA</td>
<td>20 μA</td>
</tr>
<tr>
<td><strong>IH</strong> - output source current (max.)</td>
<td>16 mA</td>
<td>8 mA</td>
<td>4 mA</td>
<td>0.4 mA</td>
<td>4 mA</td>
<td>4 mA</td>
</tr>
<tr>
<td><strong>OL</strong> - input sink current (min.)</td>
<td>-400 μA</td>
<td>-400 μA</td>
<td>-400 μA</td>
<td>-0.4 mA</td>
<td>-4 mA</td>
<td>-4 mA</td>
</tr>
<tr>
<td><strong>OH</strong> - output source current (min.)</td>
<td>-400 μA</td>
<td>-400 μA</td>
<td>-400 μA</td>
<td>-0.4 mA</td>
<td>-4 mA</td>
<td>-4 mA</td>
</tr>
</tbody>
</table>

TTL supply can be used for HCTMOS but the reverse is not necessarily true. It is not quite so easy to connect TTL to CMOS. The UOH in TTL is lower than the UH in CMOS with a supply of 5 V. This means that a logic 1 at a TTL output will not be interpreted as 'high' by a CMOS input. The same applies if we want to use HCMOS and TTL with a supply of 5 V. In this case UH (for HCMOS) is a minimum of 3.15 V, which is much too high for TTL. All is not lost, however, as the supply voltage for HCMOS can be anywhere between 2 and 6 V. If the HCMOS section of a circuit is operating on a supply of 3 V then UH is 2.1 V (70% of 3 V). Now TTL can provide a logic 1, with a margin of 0.3 V. One situation that can arise here, however, is that the TTL output level can be higher than the HCMOS supply voltage. In this case the current flowing through the 150 Ω input resistor and the input protection diode is limited by the resistor and by the collector resistance in the output circuit of the TTL gate. As long as the input current does not exceed 20 mA nothing untoward should happen. What logic 0 means in this case is three things: UIL is a maximum of 0.6 V (20% of 3 V), while the UOL for TTL is 0.5 V which leaves a margin of 0.1 V. Fortunately it is not such a problem to drive TTL from CMOS or HCMOS, as long as the supply is 5 V. The input levels for TTL do not have to be very precise; UIL is relatively high and UIH fairly low. The CMOS output voltages are therefore quite suitable for the TTL inputs, but care must be taken to ensure that the CMOS can handle the relatively high TTL input current. This applies particularly to driving standard TTL from ordinary CMOS, we will deal with this further under 'fan-out'. If the CMOS is operating at a higher supply level then obviously a level adapter circuit is needed at the connection to TTL or HCTMOS.

**Fan out**

As regards input current a distinction must be made between TTL and CMOS. The input of a TTL gate consists of a (multi-emitter) transistor whose base is connected to VCC via a resistor, as shown in figure 3. Consequently a floating input is always seen as a logic 1. The output is logic 0 if the input is earthed, then a current, the sink current, flows from the input. The sink current is 1.6 mA in standard TTL, 0.4 mA for LSTTL and 0.2 mA with ALSTTL. These values are also stated in table 2. The output of the driving gate must be able to handle this current. This, of course, presents no problems for TTL as the outputs are designed with this in mind, but CMOS is a different matter. Within the CMOS family the outputs are not expected to deliver large currents. The only current that will flow is the charging current for the input capacitance (and otherwise only the input leakage current) which has a value of a few nA. As a general rule the fan out, even between different families, can be calculated by dividing the maximum output current by the required input current. These currents are defined for both logic levels (see table 2 again). Because of the set-up of the
TTL input circuit IIH is considerably greater than IIL. As a consequence of this lack of symmetry the fan out at both logic levels must be calculated and the smaller value taken as the limit. Using the data in table 2, the fan out for various different combinations is easily found. A separate table (table 3) has been drawn up to show a summary of the results. This fan out is only shown for the combinations whose logic levels adapt directly to each other, as indicated by table 4.

Because of its large sink current, TTL can be heavily driven. The fan out, for driving normal TTL, is, as a rule, low. Not even CMOS can handle the sink current of 1.6 mA. As a result of this it is not possible to connect CMOS directly to TTL, even though their voltage levels are similar. There are, however, some CMOS ICs available with buffered outputs that can sink a current of 1.6 mA. Otherwise the CMOS outputs could also be connected in parallel until the IIL required is reached. The data sheets from the relevant manufacturer should be studied for more details about this.

There are less problems with driving LSTTL and ALSTTL because of their smaller sink current. CMOS can also drive LSTTL and ALSTTL directly.

The input requirements of all the MOS families are so modest that the fan out is theoretically very high (several thousand). In practice this is limited by the input capacitance and the load capacitance. If the maximum frequency stated by the manufacturer is to be attained (generally given by $C_L = 10$, $15$, $50$, or $100$ pF), then the fan out is defined by dividing $C_L$ by the input capacitance. As a general rule $10$ pF per input can be taken as the norm. Remember, of course, that the input capacitance is very dependent on the technology used; CMOS ICs manufactured by metal gate techniques have a larger input capacitance than those made using silicon gate technology. Also, a length of ribbon cable or a track on a printed cir-

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**Figure 4. Different adapter circuits.**

4a: from TTL (5 V) to CMOS (5 V).
4b: from CMOS (at, for example, 18 V) to TTL (5 V).
4c: from TTL (5 V) to CMOS (at 15 V, for example).
4d: two discrete versions of 4c.
Adapter circuits

In order to connect TTL (standard, LS and ALS) to 5 V supplied CMOS and HCMOS, the TTL must be able to provide the logic 1 level needed by the CMOS (at least 3.5 V). This is simply done using a pull up resistor, as figure 4 shows. A small value results in a high speed as parasitic capacitances are then charged more quickly. The minimum resistance possible is decided by the maximum load for the output. In theory the number of inputs driven by this output must also be taken into account, but if they are MOS inputs, which have negligible input current, that can simply be ignored. The minimum value of the pull up resistor is defined by:

$$R_{\text{min}} = \frac{V_{CC} - \text{UOH}}{|I_{OL}| + \Sigma I_{IN}}$$

The second term in the denominator, the sum of the input currents, can be neglected if we are talking about MOS inputs.

There is also a maximum permissible value for the pull up resistor. Because of leakage currents at the output (I, for example, several open collector outputs are connected together) and the input, there is a voltage drop across the pull up resistor at logic 1. As the output voltage may never be less than UIH, the maximum value of the pull up resistor is defined by:

$$R_{\text{max}} = \frac{V_{CC} - \text{UOH}}{|I_{OH}| + \Sigma I_{IN}}$$

Here again the second term of the denominator can be ignored for MOS inputs.

What all this means, in effect, is that the pull up resistor must have a value of 1...10 kΩ. Generally these formulae can be applied to the pull up resistors of open collector outputs whether they drive CMOS or HCMOS or not.

The situation is quite different if one logic device operates at a different supply level, which also means different logic levels. A single 4008, 4010, 4049 or 4050 buffer can be used as a high-low adapter, for example from 18 V CMOS to 5 V TTL. Each package contains six buffers, and in the case of the 4008 and 4049 they are also inverters. These buffers, which can be connected to 1 TTL inputs or 2 LSTTL inputs, can also be used, for example, to drive standard TTL from CMOS.

And so to the last combination possibility, from 5 V TTL to CMOS working at a higher level, or HCMOS at 8 V. This is also fairly straightforward if we are working with open collector outputs. In some cases the output transistor’s UCE is higher than VCC. Examples of this are the 7406 and 7407 with 30 V open collector outputs and the 7410 and 7417 with 15 V open collector outputs. The value of the pull up resistor must be carefully chosen so that the sink current does not become too large.

The fan out of the 74XX buffers listed above is three times the standard fan out, so the pull up resistor is unlikely to be too small. The disadvantage of this is that unnecessarily small pull up resistors can only a much larger current for a negligible increase in speed. A discrete buffer stage could, of course, be built using a transistor and two resistors to drive CMOS from TTL. This effectively creates an open collector output. Two possibilities for this are shown in figure 4d, the first having the advantage of a faster switching time.

Finally

It is not a good idea to leave unused TTL inputs floating, even though they normally act as if they were logic 1. If, for example, a certain LSTTL IC with a floating input is used, then the HCTMOS equivalent will cut off at logic 1. Generally these formulae can be applied to the pull up resistors of open collector outputs whether they drive CMOS or HCMOS or not. The situation is quite different if one logic device operates at a different supply level, which also means different logic levels. A single 4008, 4010, 4049 or 4050 buffer can be used as a high-low adapter, for example from 18 V CMOS to 5 V TTL. Each package contains six buffers, and in the case of the 4008 and 4049 they are also inverters. These buffers, which can be connected to 1 TTL inputs or 2 LSTTL inputs, can also be used, for example, to drive standard TTL from CMOS.

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The fan out of the 74XX buffers listed above is three times the standard fan out, so the pull up resistor is unlikely to be too small. The disadvantage of this is that unnecessarily small pull up resistors can only a much larger current for a negligible increase in speed. A discrete buffer stage could, of course, be built using a transistor and two resistors to drive CMOS from TTL. This effectively creates an open collector output. Two possibilities for this are shown in figure 4d, the first having the advantage of a faster switching time.

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The two printed-circuit boards are housed on this (aluminium) mounting tray. After they have been interconnected, the metering board is connected to the front panel. The resulting entity can then conveniently be slid into the grooves provided in the case.

'Special bulk purchase: 250 assorted capacitors for only £4.99!' A typical advert from an electronics mail order firm offering 'surplus stock'. A tempting offer for the electronics hobbyist. But will you ever be able to find out exactly what you have bought? Are all those values within their stated tolerance? Our new capacitance meter will be able to put your mind at rest.

'Capacitors are used mainly as blocking, smoothing, or decoupling elements, and also as frequency determining components in HF and AF engineering. If capacitors are to be used in filters, they should be as close as possible to the calculated value. That normally means the use of high stability capacitors, but the precise value can of course, be determined by some sort of measuring instrument, and this is where our capacitance meter comes in! It will enable you to make use of the 'only £4.99' offer and determine the exact value of the capacitors, easily and conveniently. The capacitance meter will, of course, also be to tell you whether a suspect capacitor needs replacing or not.

The meter is a precision instrument with a 3½-digit liquid crystal display which enables the measurement of capacitances from 0.1 pF to 20 mF in six ranges.

In the early days of electronics, the values of capacitors and inductors were determined by impedance measurement in bridge circuits. Such measuring bridges contained, apart from an oscillator, power supply, and sensitive meter amplifier, also very precise and therefore very expensive reference capacitors or inductors. Furthermore, operating these bridges correctly was not a simple matter. None the less, there can be no doubt about the superiority of them. For instance, they make possible the quick determination of factors other than the value, such as the Q factor and inherent losses, which are equally important for the calculation of the impedance of a circuit. However, these factors are not normally of great importance to us.

Capacitive meters usually require the unknown capacitor, Cx, to be inserted into an oscillator circuit. The frequency of the resulting signal is measured with a frequency counter or a voltmeter (after conversion to a proportional voltage). An appropriately calibrated scale on these instruments makes it possible to read off the value of the capacitor directly (see, for instance, Elektor, December 1981: ‘capacitance meter module’ page 12-18).

A different method of measurement is illustrated in figure 1. The point of this method is that the unknown capacitance, Cx, after differentiation of the input signal (by Cx/Rs), is determined by a voltage measurement. By making the value of Rs much smaller than the impedance Xc,
the value of \( C_X \) can be calculated from

\[
C_X = \frac{U_1}{2\pi f_0 R_s U}
\]

in which \( \pi, f_0, R_s, \) and \( U \) are known constants, so that only the value of the measured voltage, \( U_1 \), needs to be inserted.

You don't, of course, want to be bothered with pen, paper, and pocket calculator every time you measure a capacitor, but want to read off its value directly. The diagram of figure 1 is therefore extended into that of figure 2.

The triangular output of the generator is passed to \( C_X \) which has been connected in a differentiating circuit. The output of this circuit is a square wave of which the amplitude is proportional to the value of \( C_X \) (like \( U_1 \) in figure 1). The square wave is rectified in a phase-selective synchronous rectifier: the level of the resulting voltage is measured by a digital voltmeter.

The phase-selective rectifier operates as follows. The square-wave output of the differentiator is applied to electronic switch ES5 in phase with the rectangular output of the generator, and to electronic switch ES6 in antiphase with the rectangular output of the generator. The switches are synchronized with the triangular waveform and only pass the positive portions of the square waves. The two resulting square waves are added to provide a d.c. voltage. The relationship between the waveforms is illustrated in figure 3. The 'rooftops' on the rectangular waves are caused by the leakage current through \( C_X \). This current, which is caused by the triangular output of the generator, does not affect the measurement. Firstly, it largely disappears in the build-up of the average level (figure 3B), and, secondly, it is not accepted by the phase-selective rectifier because it is 90° out of phase with the triangular current. In an ideal circuit, the triangular signal superimposed onto the d.c. voltage (figure 3C) does not rise at all.

The circuit diagram

The waveform generator is built up from two opamps: a Schmitt trigger (IC1) and an integrator (IC2). When the output of the integrator reaches the upper trigger level of the Schmitt trigger, the input to the integrator is inverted. The output level of IC2 then decays until the lower trigger level of the Schmitt trigger is reached. In this way, IC1 produces a rectangular signal and IC2 a triangular one.

The output voltage of IC2 is the test signal for \( C_X \) and is connected to the inverting input of the differentiator IC3. The output of the differentiator is therefore a rectangular voltage, the level of which is proportional to the value of \( C_X \).

The phase-selective rectifier consists of electronic switches ES5 and ES6 which obtain their signals direct from IC3 and inverted from IC4. The control signal for the switches is taken from IC1 and fed direct to ES5 and inverted (by ES4) to ES6. The output signals of ES5 and ES6 are added and taken to the digital voltmeter via R20 (see figure 5).

The low-pass filter formed by P1, R6, and C2 derives a small triangular signal from the square-wave output of IC1, which is applied to the input of IC3 via C3. As the test signal is in antiphase with this voltage, the unavoidable parasitic capacitance at the test terminals is simply 'spirited away'. In practice this means: adjust P1 with open test terminals so that the DVM reads '0'. If the wrong measuring range has been selected, IC5 switches on electronic switch ES7 at a certain input level. When that happens, a large d.c. voltage is applied to the capacitive meter...
the DVM via R21 and the meter shows an overflow.

When the value of $C_X$ is too high for the selected measuring range, IC3 no longer functions as differentiator but rather as comparator for the triangular signal at its input. The result is that a rectangular signal appears at the output of IC3 which is 90° out of phase with respect to the signal which would have appeared under correct conditions. The rectifier will then not have an output, and the DVM reads '0'.

Some points about the measuring ranges and the test signals. Switch S1 is the range selector. For capacitors between 0 and 2 µF, the amplitude of the triangular signal is about 1.8 Vpp at a frequency of around 1000 Hz. Switches ES1 and ES2 are then closed. This enables the measurement of all non-electrolytic capacitors in three ranges: the test conditions conform to the manufacturers' specifications. Three ranges are also available for the measurement of electrolytic capacitors. These measurements are carried out at lower frequency and voltage ($f = 100$ Hz, and $U_1 = 18$ mVpp) and are also in accordance with manufacturers' conditions of test. In the 'f' range, the frequency is reduced to 10 Hz (ES3 closed), because the current at 100 Hz would be about 72 mA which is too much for the opamp. The consequence of this is that the accuracy in this range is only 10 ... 15 per cent. Fortunately, this is not so bad, because the exact value of electrolytics in this range is normally not very important. If it is required to measure an electrolytic capacitor in range 'c', switch S2 raises the test signal by about 1 V to ensure that the test voltage in this range is always positive. In the other ranges, the very small negative voltage of about 9 mVpp causes no harm.

The circuit of figure 5 is basically that of the 'LCD panel meter' featured in the October 1981 issue of Elektor. However, in the present circuit the decimal point is switched by S1b and associated diode matrix. Moreover, the selected range is indicated by LEDs D3 ... D7.

Construction

First of all, mount (but do not solder) all resistors up to and including R11 and all capacitors up to and including C9 onto the metering board shown in figure 6. It's best to use soldering pins for this to simplify the soldering after calibration. Next, fit all components except R1 and R7 to the display board shown in figure 7. The display and LEDs must be located on the track side: solder the LEDs so that they are well separated from the display. For
The mechanical construction is best carried out with an eye on the sketch in figure 8. We have used a Vero case into which the aluminium mounting tray can simply be inserted after the calibration. Both printed-circuit boards are mounted onto this tray: the display board at the front and the meter board at the rear. This method also ensures the screening of these circuits from one another.

Terminals with identical markings on the two boards should be interconnected with short lengths of wire, but keep terminals '1', 'CDp', and 'Z' on the display board free. The terminals for connecting Cx should be connected to the meter board by twin screened cable. The screen should be soldered ONLY to the common earth terminal (1) near the Cx pins.

Finally, the time has come to connect S2 to the meter board and the earth terminals on the front panel and mounting tray to earth. Then mount the mains transformer, mains on/off switch, and the fuse carrier and fuse in the case. Keep the transformer as far away as possible from the meter board. After sticking the transfer onto the front panel, this and the mounting tray may be inserted into the grooves provided on the case.

Applications

The capacitance meter can also be used as interface for a digital voltmeter: the display board is then, of course, not required. Resistor R20 should be 100 kΩ instead of 1 MΩ and a multi-turn preset of 1 MΩ should be connected between terminals HI and LO. The wiper of this preset becomes the output of the interface. The new preset will be used instead of P1 (on the display board) for calibrating the circuit. There is only one (minor) snag: the decimal point is not in the right position! So, remember this!

It is also possible to use the capacitance meter for the measurement of varicaps, but it will then have to be provided with a variable voltage source. A design for
Figure 6. Component layout and track side of the printed-circuit board for the metering unit. The range selector is soldered onto this board to reduce parasitic capacitances.

Parts list — metering board

Resistors:
- R1 = 5.6 kΩ
- R2 = 47 kΩ
- R3 = 4 MΩ
- R4, R19 = 1 kΩ
- R5 = 3.9 kΩ
- R6, R22, R23 = 100 kΩ
- R7 = 10 MΩ
- R8 = 8.2 kΩ
- R9 = 3 MΩ, 1%
- R10 = 33 kΩ, 1%
- R11, R13, R14 = 330 kΩ, 1%
- R12 = 3.3 kΩ, 1%
- R15, R16, R21 = 10 kΩ
- R17, R18, R24, R25 = 10 kΩ, 1%
- R20 = 1 MΩ
- R26 = 100 nΩ
- P1 = 1 MΩ preset
- P2 = 5 kΩ multi-turn preset
- P3 = 25 kΩ preset

Capacitors:
- C1 = 100 μF/4 V
- C2 = 22 nF
- C3 = 47 nF
- C4, C5 = 1 μF
- C6 = 220 nF
- C7 = 1 pF
- C8 = 150 pF
- C9, C10 = 15 nF
- C11, C12 = 150 nF
- C13, C14 = 1 μF/18 V
- C15 = 220 μF/40 V
- C16 = 330 nF
- C17 = 100 nF
- Capacitor 10 nF ± 1%
  (for calibration)

Semiconductors:
- D1 ... D10 = 1N4148
- D11 ... D14 = 1N4001
- IC1 = CA3130E
- IC2 ... IC5 = LF356N
- IC6, IC7 = 4066
- IC8 = 7815
- IC9 = 741

Miscellaneous:
- S1 = printed-circuit switch, 2 pole, 6 way
- S2 = SPST switch
- S3 = DPST mains switch
- T2 = mains transformer, 18 V/150 mA secondary
- F1 = 100 mA slow blow mini fuse with carrier
- Case, Vero 20221035F
- Printed-circuit board 84012-1

Important!

Before connecting any capacitor, more especially electrolytics, to the Cx terminals, make sure that it is completely discharged by connecting a resistor in parallel with it! Do not use test leads on the lowest range ('a')!

This is shown in Figure 9. The indicated capacitance is proportional to the applied voltage which makes it possible to determine the diode characteristic. Care should be taken not to apply a voltage below 2 V, otherwise the diode may conduct. Because of the metering a.c., the measurement may show an error of a few per cent. Since pin 6 of IC3 is connected to the pole of S1a, it would, of course, be possible to run a wire from there to a 'varicap' terminal on the front panel.
Summarizing . . .

. . . some of the outstanding points of the capacitance meter:
- All capacitances are measured at the correct frequency.
- Leakage currents have negligible influence on the measurement results.
- The effect of wiring capacitances has been reduced to such an extent that capacitance values smaller than 1 pF may be measured.
- After the capacitor under test has been connected, the display indication will appear in less than one second: this remains true for values up to 1000 µF!


Figure 8. Test circuit for the determination of the characteristic of varicap diodes.
Two of our recent projects, the VDU card and the Basicode-2 interface, can both be used individually with the Junior Computer. However, there are bound to be some JC users who are interested in using these two ‘extra’s’ together. The program given here was designed to do just this and thus provide the best of both worlds. Two versions of the software have been developed, for the extended Junior and for the DOS Junior.

The description of Basicode-2 and the adaption to use Basicode-2 with the Junior Computer in particular have already been dealt with in Elektor no. 102, October 1983. All details of the hardware and software needed are given there so we will not go into that again here. The only change needed to use Basicode-2 with the Junior Computer and VDU card is to modify the standard subroutines. Two tables of these subroutines are given in this article: one for the extended Junior with VDU card and the other for DOS Junior with VDU card.

A few changes
Some modifications or additions to the ‘old’ subroutines are needed. Subroutine 110 is changed. We have written a small machine-code program to speed up the positioning of the cursor (to HO, VE). Whenever a jump to line 20 is made in a Basicode-2 program (as always happens), then a piece of machine-code is first written into RAM. If the program then comes to subroutine 110 at any stage this machine-code program is called and the cursor is brought very quickly to the position defined by HO and VE. Subroutine 120, requesting the position of the cursor on the screen, is possible with this combination even though it did not work with the Junior/Elekterminal combination.

The only routine that is still unworkable is subroutine 200. The Junior simply cannot determine if a key is pressed at a particular moment. A GOSUB 200 in a program must therefore be changed. Actually there are two routines that do not work, the second being subroutine 260. However, the beep that should be generated by a GOSUB 250 can hardly be considered essential for the correct operation of a program.

One further important note. If the Basicode-2 translation program is used with the DOS Junior, great care should be exercised when using the DISK!! ... command. If, for instance, a BASIC program is loaded from the floppy with the command DISK! "..." and this program is then to be saved on tape in Basicode-2 format, the ’save’ may not work because DISK!! ... ” causes page zero to be ‘swapped’. The result of this is that the pointers needed in the Basicode-2 translation program are not longer correct. There is a very simple solution for this. After removing anything from (or storing anything on) the floppy disk the number 1 is typed and a (CARRIAGE) RETURN given. A dummy line has then been included and the pointers are again correct. Everything will work correctly provided there is nothing on line 1, otherwise a different (blank) line number must be used.

Table 1. These are standard subroutines for the extended Junior with the VDU card.

Table 2. This is a list of the subroutines to use for the DOS Junior with the VDU card.
Elektor staff are a versatile lot! The present design came into being because one of our designers is a fervent spelaeologist, more popularly known as a caver. Regularly he risks life and limb in all sorts of dark caves, only to emerge hours later into daylight, covered in mud, sweating, and dead-tired, but happy and content. A good, reliable light source is, of course, indispensable for those treks in the dark. Many of the caver's lamp units in use today are powered by rechargeable (lead-acid or NiCd) batteries. Such batteries are inexpensive over their life — provided they are used often and regularly — and provide a near-constant output voltage. Dry batteries are relatively inexpensive to buy, offer small volume and low weight, and can easily be carried as spares. The last three points are, of course, of inestimable value during caving and in many other applications! Unfortunately, dry batteries have a serious drawback: their output voltage falls linearly with time, so that at the beginning of their life the lamp burns brightly, while long before they are exhausted, the lamp begins to resemble a glowworm! Not only is this highly undesirable from a safety point of view, but it also makes for low efficiency. Our versatile designer decided, therefore, to design a voltage source for battery-operated lamps which offers a substantially constant output at high efficiency.

**constant voltage source...**

The design is basically a dc/ac converter based on a cleverly thought-out circuit which keeps the power supplied to the lamp, and therefore the light intensity, virtually constant over the normal life of the battery. The circuit itself has very low power consumption so that the efficiency of the whole is high.

**The principle**

To control power at high efficiency, it is best to make use of pulse-width control. As the power supplied to the lamp must remain constant, the control should work so that the pulse width increases as the battery voltage decreases. To be sure, it is quite simple to design a pulse-width control whereby the pulse width is inversely proportional to the supply voltage. That is, however, not the solution to the requirement, because the power to the lamp is given by \( P = \frac{U_b^2}{R} \), where \( U_b \) is the battery voltage and \( R \) is the resistance of the lamp. What is required is compensation of \( U_b^2 \), and this is achieved by using two pulse-width controls, operating at different frequencies, but with identical duty factors (see figure 1). One reference voltage determines the pulse-width setting of both controls (the pulse width remains inversely proportional to the battery voltage). The outputs of the controls are multiplied in an AND gate, resulting in a signal of which the pulse width is inversely proportional to \( U_b^2 \).!

**The circuit**

The constant voltage source is based on one IC — a quad comparator type LM 339 — and a couple of transistors (see figure 1). Simplified block schematic to show the ingenuity of the voltage source: two pulse-width controls together with a multiplier ensure that the power fed to the lamp is kept constant.

---

**constant voltage source...**

...for battery operated lamps
Figure 2. The circuit diagram: a voltage quad comparator with open-collector outputs and three discrete transistors are the active components on which the voltage source is based.

One stage of the LM 339, A2, in conjunction with transistor T1, forms a voltage reference source for pulse-width controls A1 and A3. The voltage source is formed by diode D1 to which the output of T1 is applied via R3. The reference voltage is set by P1. For a supply voltage, \( U_b \), of 10 volts, the reference voltage, \( U_r \), can be preset between 1.0 and 3.0 V by P1.

The two pulse-width controls (PWC) operate at frequencies of about 1.2 kHz and 3.6 kHz respectively. The frequency separation is necessary to prevent (visible) interference between their output signals. The outputs of A1 and A3 are fed to the non-inverting input of A4 via R10 and R16. Opamp A4 is connected as an AND gate so that its output is only '1' if both A1 and A3 have a '1' at their output.

The circuit terminates in an economical output amplifier based on transistors T2 and T3. Power transistor T3 is a type BD 437 which has a low collector/emitter saturation voltage.

With values shown in figure 2, the constant-voltage source is suitable for lamps of 3.5...6.3 V consuming not more than 1 A. A graph of the efficiency, \( n \), of various...
Some arithmetic

In the following,

\( U_b = \) battery voltage

\( U_e = \) effective value of pulse voltage

\( D = \) duty factor of BOTH pulse-width controls

\( P = \) power supplied to lamp

\( R = \) resistance of lamp

The duty factor, \( D \), is inversely proportional to \( U_b \).

Each PWC delivers a (pulse) voltage of which

\[ U_e = U_b \cdot D \]

Multiplier \( A_4 \), an AND gate which only recognizes logic levels, multiplies pulse-widths but NOT voltages; its output is, therefore

\[ U = U_b \cdot D / D = U_b \cdot D \]

The power supplied to the lamp is therefore

\[ P = U_b \cdot D^2 / R \]

As both \( U_b \) and \( D \) are expressed as second-order quantities which are inversely proportional, and \( R \) is constant, it is evident that \( P \) is independent of \( U_b \).

Lamps versus \( U_b \) is given in figure 3. The circuit is suitable for use with input voltages, \( U_b \), of 3.5...15 V. The average current consumed is about 15 mA.

Calibration

Calibrating the voltage source is fairly simple. Connect a suitable lamp to the lamp terminals and a variable, stabilized power supply to the battery terminals. Set the output of the power supply to the nominal voltage of the lamp used.

Connect an oscilloscope to pin 2 of ICI and adjust PI until A1 just commences to oscillate.

If no instruments other than a multimeter are available, the voltage source may be calibrated as follows. Connect a suitable lamp to the lamp terminals, and the multimeter (resistance range) between pin 6 of ICI and the junction of PI-RI. Adjust PI for minimum resistance. Remove the multimeter and connect a suitable battery to the battery terminals. Adjust PI for good brightness of the lamp.
TELEPHONE BELL IC TYPE
MC 34012
(Motorola Limited)

The MC 34012 is intended primarily as replacement for the usual telephone bell and is therefore of particular interest to Elektor readers who want a second telephone bell. The MC 34012 presents a load to the telephone line which is smaller than that of a "real" second telephone bell.

The input of the chip is connected to the usual input wires to the telephone bell, and its output to a piezo-electric buzzer (e.g. a Toko type). As soon as the ringing signal (intermittent a.c.) on the line exceeds 35 V, the IC is turned on and the buzzer emits a pleasant tone. Note that the IC needs no power supply as the necessary energy is drawn from the ringing signal! The quiescent current is therefore zero.

DIGITAL CLINICAL THERMOMETER IC TYPE
ZN 412
(Ferranti Electronics Limited)

The recently announced ZN 412 contains all the necessary linear and digital functions to enable a clinical thermometer to be constructed with a minimum of external components. The multiplexed data outputs of the chip are capable of directly driving a 3-digit seven-segment LED display. These outputs are controlled by an integral A/D processor which converts the output of an external probe into a digital number. A temperature range of 35.0...47.6°C can be displayed with an accuracy of 0.1°C and a response time of 8 seconds. The ZN 412 includes a self testing facility, battery status indication, reset, and display hold. Supply requirements are 4.5 V at 14 mA.

Shown at the far right is a prototype of a digital clinical thermometer based on the ZN 412.

PRECISION CENTIGRADE TEMPERATURE SENSORS
SERIES LM 35
(National Semiconductor Corporation)

The series LM 35 temperature sensors are precision ICs which have two important advantages over the usual sensors in that they already calibrated and start at 0°C. Their output voltage is directly proportional to the temperature measured in degrees centigrade (10 mV/°C). The usual sensor must invariably be calibrated to obtain the required voltage/temperature slope and starts at 0 K (−273°C).

The low output impedance of the LM 35 series (0.1 ohm for a 2 mA load), linear output, and precise, inherent calibration make interfacing these sensors to read-out or control circuits very easy. Power supply may be single or symmetrical: the operating voltage may lie between 4 and 30 volts. Accuracy is typically 0.5°C. Owing to the low current consumption of 80 μA, the internal heat dissipation amounts typically to only 0.05°C in still air.
COMPLEX SOUND GENERATOR ICS TYPES
SN 76488 & SN 76495
(Texas Instruments Inc.)

These circuits are updated versions of the SN 76477, which was featured in our March 1981 issue. The SN 76488 is a simplified version in a 16-pin housing, while the SN 76495 retains a 28-pin package. The main advantage of the present circuits over the SN 76477 is the on-chip audio amplifier which can deliver up to 125 mW into an 8-ohm load. Unlike the SN 76477, both circuits are compatible with computer systems. Unlike their predecessor, however, they operate from a 7.5...10 V supply. An on-chip regulator provides a stabilized 5 V supply for driving external circuits, or for use as high logic level.

Shown at the left is a typical demonstration circuit of the SN 76495.

POWER SWITCHING REGULATOR IC TYPE L296
(SGS-ATES)

The L296 is a high-power monolithic switching regulator (the first in the world according to the makers) which can supply a current of 4 A at voltages of 5.1...40 V. As the IC is capable of operating at switching frequencies of up to 200 kHz, external components such as inductors and capacitors can be kept small and therefore relatively inexpensive. Features include soft start (which slows down the rise time of the output voltage when the power is switched on), programmable current limiting (with the load current sensing resistor on the chip), reset output (intended primarily for microprocessors), and thermal shutdown at junction temperatures above 150°C.

MAINS-CARRIER TRANSCEIVER IC TYPE LM 1893
(National Semiconductor Corporation)

As the name implies, mains-carrier transceivers use the mains supply lines to transfer information between remote locations. The LM 1893 bipolar chip performs as a mains interface for bi-directional (semi-duplex) communication of serial bit streams of virtually any coding. During transmission, a sinusoidal carrier is FSK modulated and superimposed on the mains voltage via an on-chip driver stage. During reception, a PLL type demodulator extracts the information from the mains. Some of the features of the LM 1893 are: transmission rate of up to 4800 baud, choice of carrier frequency between 50 and 300 kHz, TTL and CMOS compatible logic levels, and regulated voltage to power logic.
The syncbox is a circuit for use with a video-audio modulator (VAM) or a video combiner. It provides all kinds of signals that are needed to build up a complete video signal. A syncbox can be used, for example, to fill up the space between two recordings on a video tape. The 'noise' that would then normally appear can thus be replaced by a black image or a colour bar.

**Video Syncbox**

This syncbox is an independent video signal source using an oscillator signal of 125 kHz to produce a number of basic signals that can be used for all kinds of video equipment and circuits. An external crystal-controlled signal can be used to clock the circuit if very high stability is demanded. Using the signals from the syncbox a black image (for video recorders) or even good quality colour bar can be produced.

**The Circuit**

In the circuit diagram shown in figure 1 all signals are formed from the output signals of the 4040 (IC1). This IC, together with gates N4, N8 and N9, function as a 'divide by 2496' circuit. A simple clock oscillator (N2, N3) supplying a frequency of 125 kHz, feeds the input of the divider. Using this signal the divider provides a raster frequency of 50.08 Hz. The raster frequency is normally 50 Hz, but because we want a non-interlaced image (that does not shake) we have chosen a raster time that is 32 μs shorter than normal. The number of lines per raster is then 312 instead of the normal 312½. Without a lot of extra electronics interlacing is not possible with this circuit. The line frequency is the normal value of 15625 Hz, and this is necessary as the PAL delay line in colour television sets is tuned exactly to this value of 64 μs. Longer or shorter line times give rise to colour faults on the screen as colours run into each other. The line frequency (horizontal synchronization, HS) is derived by adding the oscillator signal from N2/N3 and outputs Q0, Q1 and Q2 of IC1. Because of the fairly symmetrical block of the 125 kHz clock a synchronization pulse of about 1 μs results.
4 µs width appears at the output of N7. The raster synchronization pulse is derived directly from the line synchronization signal by inverting the latter during the raster synchronization time. The advantage of this is that the line synchronization signal remains safe during the raster synchronization. The electronics in the TV set automatically ensures that the inverted line synchronization is recognized as the raster synchronization.

Switching between line and raster synchronization is handled by FF1 which is clocked at the line frequency from output Q2 of IC1. The positive edge of this clock signal occurs in the middle of the line time so the raster synchronization, which lasts for eight line times, always starts and ends with a half line. The outputs of FF1 are connected to N10 and N11, which in turn feed N12, thus combining the line and raster synchronization.

Note that the raster synchronization signal eventually has the same polarity as the HS signal (as a quick glance at the timing diagram of figure 2a will confirm). The HS signal is also fed to the outside world, where it is used in colour video systems to control the PAL switch. The CS signal (Composite Synchronization) is not suitable for this because it contains an extra positive and negative edge during the raster synchronization (see figure 2a). One of these two edges will trigger the PAL flip-flop (in the VAM or video combiner) one extra time which is enough to confuse the receiver and activate the colour killer. The problem is avoided by using the HS signal.

The carrier for the colour information must be regularly synchronized in order to keep the colours reproducible. This happens directly after the line synchronization by means of a burst signal (consisting of a number of periods of colour carrier with a fixed phase). The BE (Burst Enable) signal (or BE) is used to activate this burst. This signal is generated with the aid of two monostable multivibrators formed from FF3 and FF4. The inverted trailing edge of the HS signal triggers FF3, and the output of this flip-flop gives a pulse of 1.6 µs (set with P2). The same trailing edge of HS triggers FF4 and this in turn gives a BE pulse of 2.25 µs (set with P3). This is shown by the small timing chart in figure 2b. Small deviations from these times are rarely a difficulty as neither a shorter delay between synchronization and burst nor a longer burst pulse are likely to cause any problems.

A blanking signal is not absolutely necessary but it is often handy. In our circuit this signal is produced by FF2, which, again, operates as an MMV. The pulse width is set to about 12 µs with R2 and C2. During the raster synchronization the pulse widths of FF2, FF3 and FF4 are defined by FF1 as this then disables the set inputs of the three flip-flops. A false burst pulse is then given by the BE output, but this causes no adverse effects as it appears in the middle of the line time. Simultaneously the signal at the set input of FF2 causes a raster blanking signal CBLK (composite blank) to be generated.

Construction

The printed circuit board layout for this circuit is shown in figure 3, and if this is used construction should give absolutely no problems. We do, however, recommend that sockets be used for the ICs.
Figure 3. The printed circuit and component layouts for the circuit are shown here.

Figure 4. This is how the video syncbox is connected to the VAM and video combiner respectively.

The supply for the circuit can be between 5 and 12 V, and current consumption is only a few milliamps. To use this circuit with the video combiner elsewhere in this issue we suggest that that article be read before building the syncbox. An oscilloscope is needed for adjusting the three presets. Failing this they will simply have to be set up 'by eye'.

Use

The syncbox is only useful when combined with some other suitable circuit. It could, for example, provide the control signal for a simple pattern generator, or it could be used with the video/audio modulator (VAM) from Elektor, February 1983, or the video combiner in this issue.

Outputs, CBLK and CS of the video syncbox must be connected to the BE, BL and SYNC inputs of the VAM. Links V-W and X-Y on the VAM board must be removed. If the VAM is only used in combination with the video syncbox, IC4 and IC5 of the VAM may be removed.

A blank image (for example to fill up a video tape) can be obtained by connecting the BL input (or the R G B inputs) to ground. For a colour bar there are three extra connections between syncbox and VAM needed. Points R, G and B of the syncbox must be connected to the R, G and B inputs of the VAM. The three inputs per colour of the VAM can be connected together. The resulting colour bar has the following colours in this sequence (from left to right), blue-red-magenta-green-cyan-yellow. White and black do not appear on the screen. Different colour combinations and patterns can be made by using different outputs of the 4040. If the syncbox and video combiner are used together the 'common' points on both boards must be linked. In this case points R, G and B need only be connected if a colour bar is required with this combination.
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