usually loaded with forty discrete operations and these are called up by the input logic variation, but in type (c) the number of operations carried out by the device is controlled only by the binary number range the device will accept. In many cases as many as nine inputs or program lines are available, thus giving 2^9 variations, ie. 511 different lines. Since we originally stated that the channelling was at 10kHz intervals this gives a tuning range of 5.11MHz.

The simple operation of a synthesiser PLL circuit is shown in **Fig. 2.** When the reference frequency f_r and the VCO frequency f_o are applied to the phase detector, the phase difference is measured in the phase detector and converted into a DC output which is applied to the VCO via the low pass filter. Since the comparison is made every cycle there will be harmonics and noise at the output P, hence the need for the low pass filter. The integrated DC voltage applied to the VCO causes a frequency change to occur, the VCO output being returned to the phase detector. The closed loop will continue to operate until there is no phase difference between the voltage generated in the VCO and that of the reference. The VCO is then locked on to the reference frequency and the VCO output (f_o) is in phase lock with the reference.

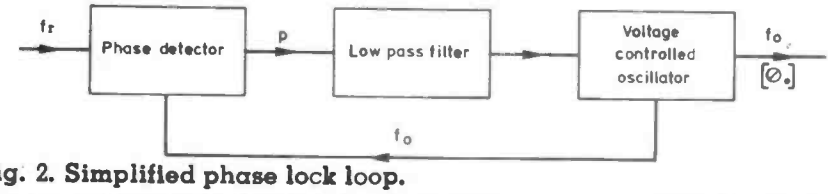

Fig. 2. Simplified phase lock loop.

To apply this technique in real terms some additional sophistication is required. Since variable frequency dividers used in these circuits have a fairly low frequency maximum count limit and we require a 10kHz channel spacing we have to accept that we are referring to a 10kHz reference and that our VCO frequency of approximately 17MHz has to be divided by some 1700. To overcome this problem the VCO frequency is mixed with an offset oscillator, to give a lower variable frequency which does not require such a high division ratio. **Figure 3** indicates a fully operational arrangement.

In order to achieve a range covering 29+MHz it is necessary to alter VCO to give 29.5-11.695MHz as the operating range.

In the example quoted the channel switch on channel 1 gives an output code of 136, so our new frequency on 29MHz at the lowest end of the range should be controlled by a 136 programmed input to the PLL to be used. By substituting a 17.245 crystal for the 14.910 crystal in the original circuit our transmit frequency should now be between 29.300 and 29.700. However, due to FCC regulations, the original FCC frequency allocation to CB had certain discrete gaps at 50kHz intervals. The channel switches were designed to skip these numbers in their output; so a typical output sequence from the switch used in our example would be 136, 137, 138, 140, 141, 142, 143, 145, 146, 147, 148, 150 and so on up to channel 20, where normal sequential counting took over up to channel 22. Channel 23 required a count of 165, whereas channel 22 was 162. The sequence at this point was channels 22 — 24 — 23 — 26; then normal counting up to level 44 or in our instance 180.

By interrupting the program lines from the switch and feeding them via a suitably programmed EPROM the necessary corrections can be made to the coding, so that the switch reading 1-40 gives a progressive binary input to the PLL, enabling a true 10kHz channel sequence.

In some instances the VCO coil may not tune to the new frequencies. This can be changed fairly easily either by reducing the length of the coil or by reducing the coil padding capacitor.

Where it is necessary to replace the synthesiser due to it being a dedicated device, the simplest method is to introduce a composite board containing the EPROM and the alternative synthesiser. A suitable board is shown in **Fig. 4** together with the circuit and layout in **Figs. 5 & 6.** As the circuit indicates the program lines are fed to the EPROM and the modified program is then fed to the synthesiser. The details of operation and installation will be dealt with later in the article.

PCB drawings Figs. 4, 6 and 9 will appear in a future issue.
Unfortunately there were mistakes in the original artwork — Ed.

Another technique was often used to cut the number of crystals. By taking the 10.240MHz signal and dividing it by two, a 5.12MHz signal was derived. This frequency was multiplied by three to give 15.36MHz which was then mixed with the VCO. This was then submitted to the divide-by-N module, giv-

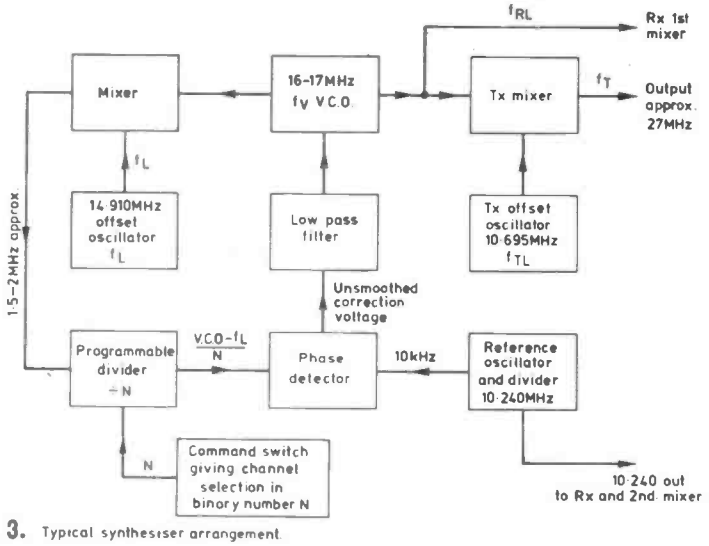

Fig. 3. Typical synthesiser arrangement.