information in that particular location is available to the data bus, in just the same way as the diode matrix.

The next stage is to be able to write to the RAM. To do this we need to bring the keyboard onto the data bus. An ASCII keyboard has seven data outputs, and supplies a code to these outputs dependent on which letter is selected. The keyboard also supplies a short pulse called 'strobe', every time we press a key. This strobe pulse could be 'active high' or 'active low'. Most keyboards provide both. Our circuit requires active low, often called $\overline{ST}$. When this signal occurs the outputs of IC1, (74LS244) which are normally floating, assume the same state as the inputs and thus feed the keyboard output to the data bus. The strobe pulse also passes to the RAM where pin 10 of our memory chips (2114) are driven low. This puts them into a 'write mode' so the keyboard data is stored.

The next problem is to control where the keyboard data is stored. By inserting IC4 in the address lines to the RAM we can switch the address lines in the write mode. IC4 (74LS157) is a 4-bit data selector and functions just like a 4-pole double-throw switch, in that when pin 1 is driven low the RAM address lines are fed from the QA, QB, QC, QD outputs of our counter chip IC5.

IC5 is a counter which counts up to 16 and then resets. By using the strobe pulse to advance it, its count will increase by one every time we press a key, ensuring that the selected letter is stored in the next location in memory. When IC5 has been clocked to location 16 it will automatically reset to character location 1.

The next stage is to display a 'cursor' so that we can see the next location to be typed into on the screen. To do this we compare the 'read' and 'write' addresses in the 4-bit magnitude comparator IC6 (74LS85). When the two addresses are the same ie. the character generator is scanning the location which we will next type into, then the output of the comparator, pin 6, goes high. This high state is connected to pin 8 of our RAM which is the chip enable pin (active low), so when our two addresses are the same the RAM is disabled, causing the data bus to be pulled high by the 10k pull-up resistors. This ensures the data bus assumes a high state in the absence of RAM data.

If the diode programme module is operating erratically then the addition of these pull-up resistors to the diode module may be the answer. It depends upon the diodes used.

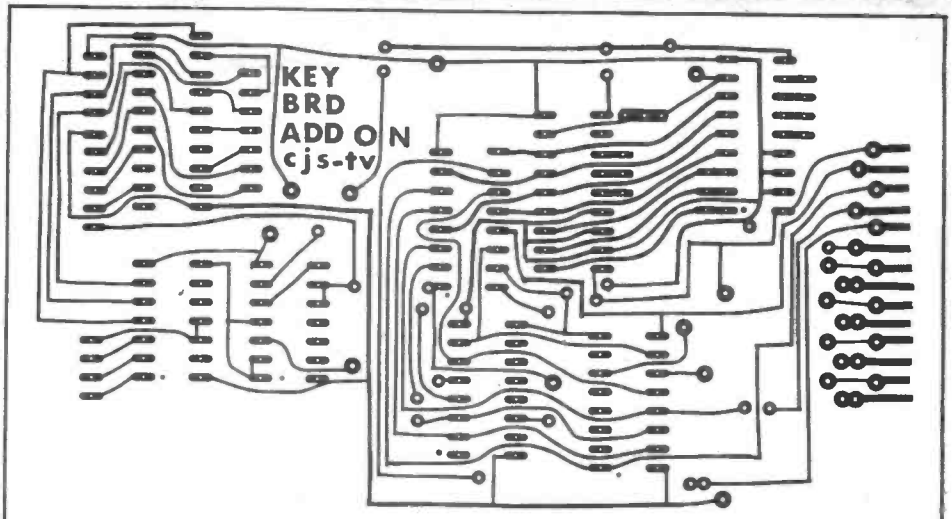

Fig. 2. Wiring side of double sided PCB

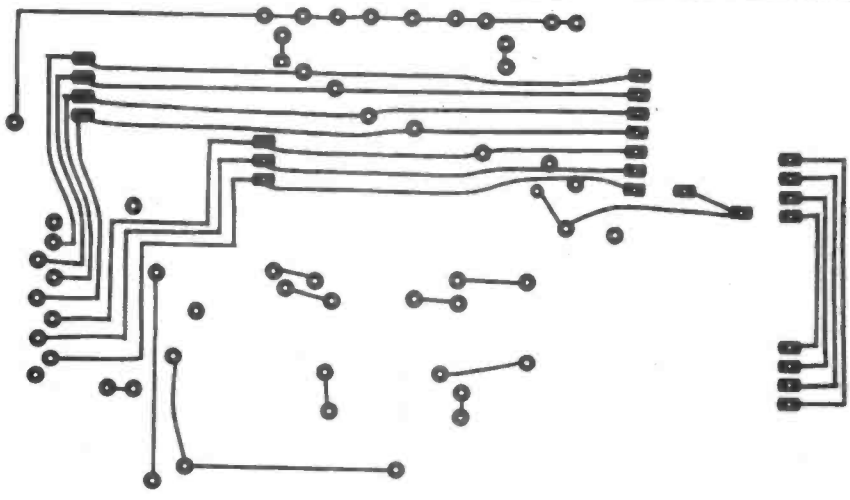

Fig. 3. Component side of double sided PCB

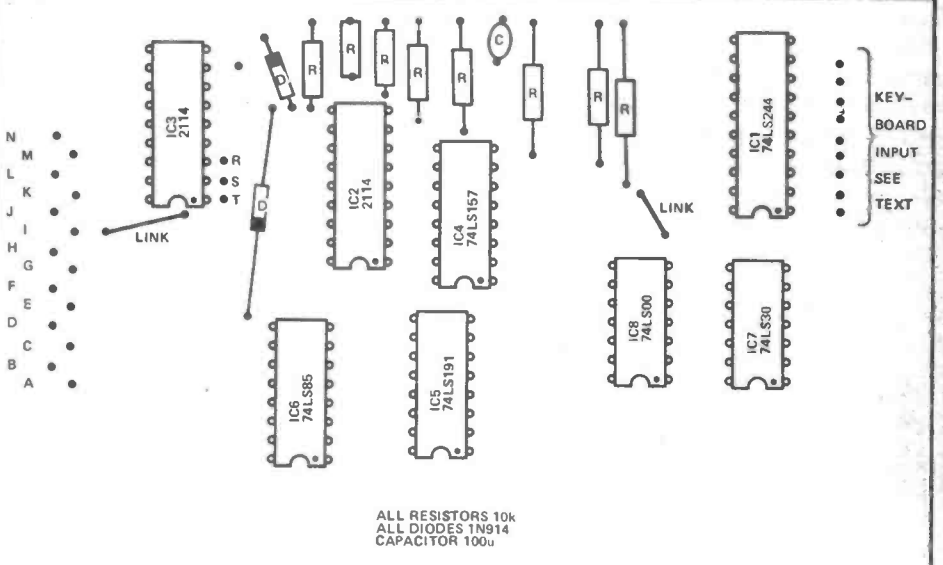

Fig. 4. Component layout