An Auto-Powered Semi 'break-in' Keyer

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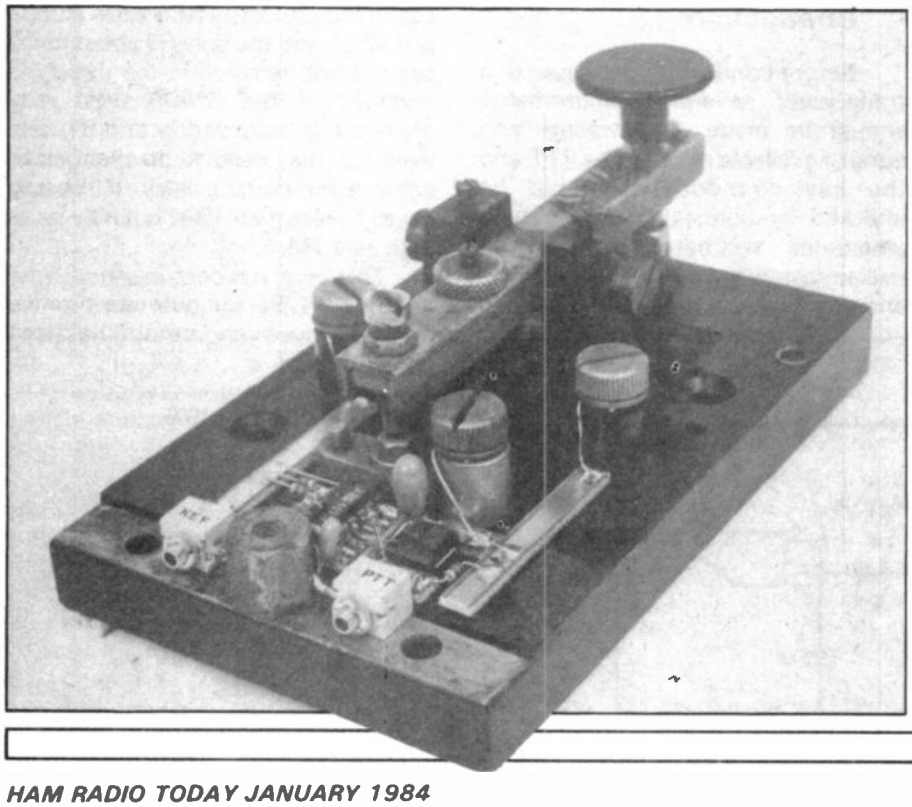
With the recent growth in the use of CW at VHF and UHF there is a need for a simple circuit which can provide 'break-in' facilities for VHF/UHF transceivers which do not have it.

Most modern HF transceivers are equipped with semi break-in keying as standard — most VHF transceivers are not.

In a transceiver equipped with break-in keying the receiver is active whenever the key is not closed — the operator can thus listen for responses in the short intervals between dots and dashes. The design of receivers capable of working in this way is very demanding since they must respond to weak signals within milliseconds of the transmitter ceasing to generate very high powers at the same frequency — this places great constraints on the strong-signal performance and the operation of the agc. With semi break-in keying the receiver switches off when the key closes and remains off until the key has been open for a predetermined period — normally of the order of a few hundred milliseconds — the demands on receiver design are correspondingly less stringent. The operator can still monitor while transmitting but must make an infinitesimal pause to do so. Transceivers fitted with semi break-in keying normally use the VOX (voice-operated transmit/receive) circuitry to perform the function.

The present design does not use VOX circuitry but instead uses a CMOS logic arrangement driving a VMOS output transistor to switch the PTT (push to talk) line of the transceiver. The use of MOS allows the keyer to run from the small current which may be taken from the PTT and key lines without keying and the circuit needs no other power supply. This is particularly convenient during contests since keyer batteries are notorious for failing when no replacements are available.



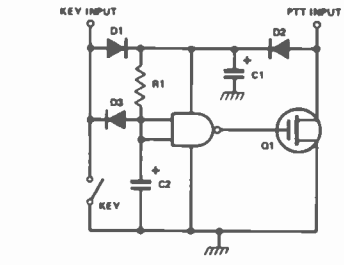


Fig. 1 Simple keyer circuit

The Circuit

A circuit which will perform the function is shown in **Fig 1.** It consists of a single schmitt input CMOS gate and an N-Channel VMOS transistor. There are also three diodes, two capacitors and a resistor (which may be variable).

Its operation is simple — when first powered the capacitor C1 is charged via D1 and/or D2 (whichever is at a higher potential) and then this capacitor powers the CMOS circuit, which draws well under 1 microamp of current from its supply. When the key is open C2 is charged, the input to the gate is at logic 1 and hence its output and the gate of Q1 are low so that Q1 is turned off.

When the key is closed C2 at once discharges through D3 and the output of the gate rises, turning on Q1, which grounds the PTT line, switching the transceiver to 'TRANSMIT'. Being a VMOS device Q1 draws no gate