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PERSONAL COMPUTER WORLD

UK 50p
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Vol. 1, No. 11
March 1979

Europe's first magazine for personal computers for home and business use

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Editorial and Advertising Office:

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A Zgorelec

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Cover: The SYM 1. Photographed by: Yoshi Imamura

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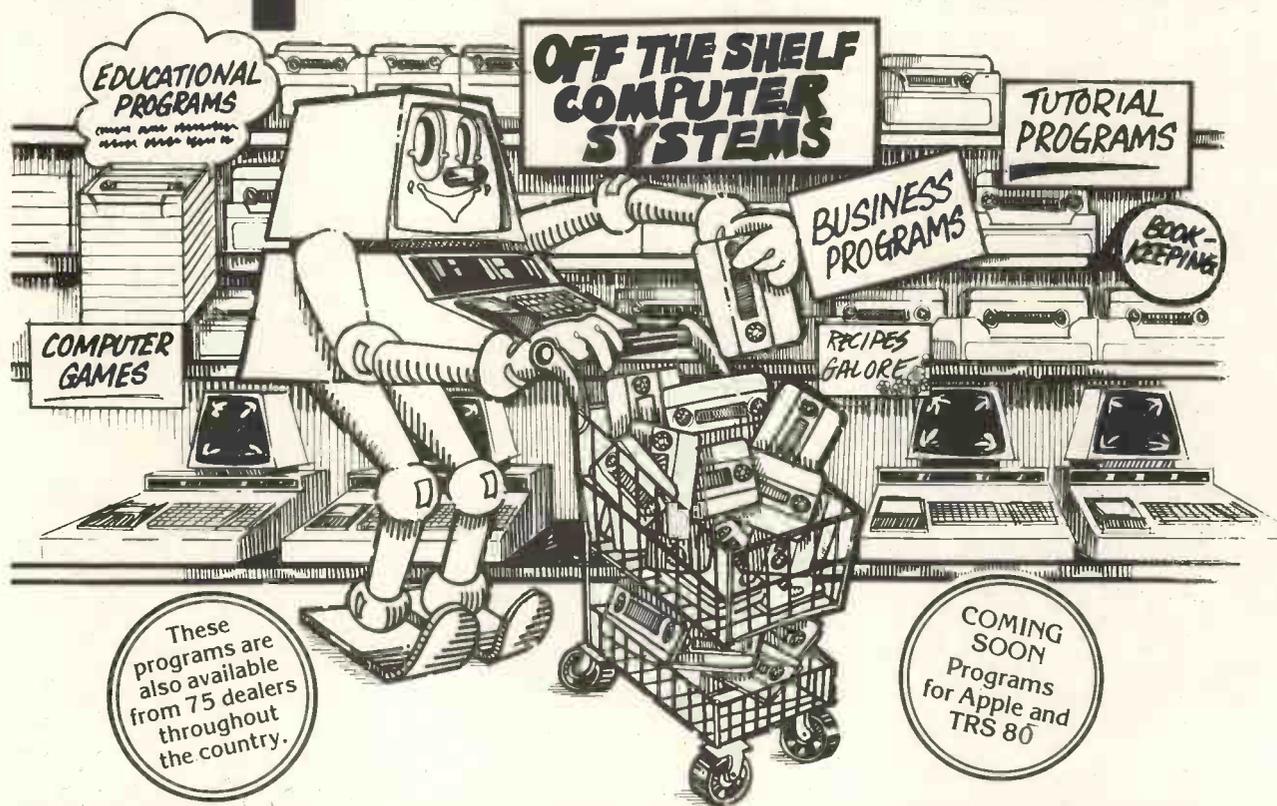
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Editorial

Readers' Letters

When the post comes in, the publisher makes a bee line for the subscriptions and advertising, and I make a bee line for readers' letters and articles. Reading your letters is one of the high points of my day. When it comes to selecting which letters to print, I am faced by what I call a renescent cliché — an embarrassment of riches. I don't like mutilating letters, though I do edit a few slightly. I cannot put in as many as I would like. So, this issue, we've put in a lot more letters; and we will do the same thing very occasionally.

I get the occasional letter saying that I allow readers too much of a say in what goes into PCW, instead of giving a lead. Of course, everyone should be subjected to this "lead" except the writers of these letters! I may say here that I am more than happy to "follow" readers' suggestions if they improve the magazine: we're changing to a serif typeface, after appeals from readers, and we've added the month and year to each page.

I haven't taken up residence on Mount Olympus, and I don't pretend to be knowledgeable about all aspects of computing — so I say to PCW readers — keep "leading". I'll follow if it's for the good of PCW — that's where I exercise my judgement.

John Miller Kirkpatrick

John was literally the first author to write for us. He had the first article in our first issue. I did not meet him often, and didn't know him very well, so I thought it fit that others who knew him better should write about him first after he died. But I do know this: he was humorous, bright, and a good man.

Written for the Nascom

Among the programs written to run on the Nascom-1 and available now are:

ICL Dataskil Letter Editor

This software provides a comprehensive set of data operations. Text can be input, displayed, edited, stored on tape, retrieved and further amended. Control functions include cursor, character, word, line, scrolling, tabbing, tape store and retrieve, text printing. All in less than 2K byte plus workspace for up to almost two full screens. Price on 2 x 2708 EPROM £70 plus VAT.

TINY BASIC

A 2K BASIC Interpreter in 2x2708 EPROM. Normal commands: 1-32767 MSL/single array/arithmetic constant/ <>≠≠≠ /strings valid in PRINT/supplied with user manual/additional three level keyboard control/compatible with NASBUG and B.Bug Price £25 Plus VAT.

An extended version of the above is our SUPER TINY BASIC which has all the TINY BASIC functions plus full editing features and additional operator command. Price in 3x2708 EPROM £35 plus VAT.

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An editor/assembler which runs under NASBUG and provides the powerful advantages of writing programs in Z80 assembly language instead of directly in machine code. Uses less than 3K bytes of memory and is supplied on cassette priced £30 plus VAT.



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Publisher's Letter

Dear Reader,

Elsewhere you will see PCW announcements which mean that we are now becoming very active in the publishing, seminar and exhibition field. We expect 1979 to be a great year. Exhibitors at our last Show say that people are still talking about it. This year's Show will be even better — we would not be PCW if we didn't have aces up our sleeve!

Watch this space.

MEMORIAL FUND

John Miller Kirkpatrick was one of the originators of personal computing. He was a bright and good man. He died young, leaving a wife and family.

Personal Computer World appeals to readers to contribute to a fund being set up to help his wife and family.

Let us show that we care.

Please send donations to:

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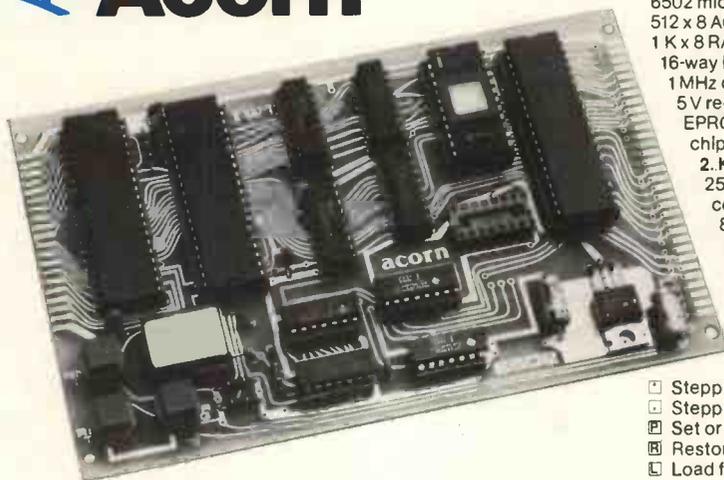
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Computer Trader

Introducing Acorn



A professional MPU card

Designed as a general purpose industrial controller based on the 6502 MPU, this card is complemented by a matching Eurocard hex keyboard and CUTS standard cassette interface, to create the new...

Acorn Microcomputer



This compact stand-alone micro-computer is based on standard Eurocard modules, and employs the highly popular 6502 MPU (as used in APPLE, PET, KIM, etc). Throughout, the design philosophy has been to provide full expandability, versatility and economy. Take a look at the full specification, and see how Acorn meets your requirements

Acorn technical specification

The Acorn consists of two single Eurocards:

- 1. MPU card**
6502 microprocessor
512 x 8 ACORN monitor
1 K x 8 RAM
16-way I/O with 128 bytes of RAM
1 MHz crystal
5 V regulator, sockets for 2 K EPROM and second RAM I/O chip.

- 2. Keyboard card**
25 click-keys (16 hex, 9 control)
8 digit, 7 segment display
CUTS standard crystal controlled tape interface circuitry

Keyboard Instructions:

- M Memory Inspect/Change (remembers last address used)
- ☐ Stepping up through memory
- ☐ Stepping down through memory
- ☐ Set or clear break point
- ☐ Restore from break
- ☐ Load from tape
- ☐ Store on tape
- ☐ Go (recalls last address used)
- ☐ Reset

Compact, easy to use Acorn Monitor includes the following features:

- System program
- Set of sub-routines for use in programming
- Powerful de-bugging facility displays all internal registers
- Tape load and store routines

Acorn - with real expandability!

The standard Acorn is fully expandable to 65 K of memory, and the Acorn bus is available on the 64-way edge-connector. Whether you're a beginner in the field, an ambitious home computer buff, a development engineer, a teacher or a businessman, the Acorn and its family of modules will provide a practical solution in virtually every situation.

Future expansion for Acorn includes the following software and hardware.

Software
Basic interpreter, assembler, dis-assembler, editor, TTY and disk operating system.

Hardware
Memory-mapped VDU system (with upper and lower case ascii graphics and hardware scroll) floppy disk controller for 5 1/4 in and 7 in disks, a memory card with 8 K bytes of static RAM (2716) and 4 K bytes of EPROM (2114), a PROM programmer (for all types of PROM usable on ACORN a full ascii keyboard, a backboard for the ACORN bus, and a Eurocard racking system.

Acorn Operating Manual

With Acorn, you'll receive an operating manual that covers computing in full, from first principles of binary arithmetic, to efficient hex programming with the 6502 instruction set. The manual also includes a listing of the monitor programs and the instruction set, and other useful tabulations; plus a selection of 12 interesting and educative program samples.

Acorn, as a kit or fully assembled, the choice is yours with this coupon!

With such flexibility at such a price, the ACORN package is one you'll want to make the most of, soon. Whether you're a hobbyist, computer technician, R&D engineer or a computer user, Acorn provides you with a highly cost-effective basis for a computer or an industrial development system.

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Letters

PCW *THE PUZZLE DAZZLE* set by reader David Broughton (*Letters*, Vol. 1, No. 7) brought us an immense number of PUZZLE UNDAZZLES. PCW Consultant Neil Harrison has been looking at them and is writing up the result. PCW.

3D Noughts and Crosses

May I compliment the author of the 3-D Noughts and Crosses program published in the December '78 edition — it certainly plays a good game. However, there is a small oversight in the setting of the N0 and N1 value arrays which causes the program not to stop its competitor's rows of 3 under certain circumstances. Other than playing to win itself, the next most important move is to stop the opponent winning with his move; thus, an X must be played where the opponent already has 3 on the row.

With the value of 15 for N0 (3 + 1) it is possible for the computer to ignore this move in favour of a square scoring 8 (N0 (2 + 1)) on two different lines. So N0 (3 + 1) should be increased to, say, 30 and N1 (3 + 1) to any value higher than 30 to ensure that the program will take every opportunity of completing its own winning line.

J. M. Collier, M.Sc., M: B.P.I.C.S., *Basic Computing*, Oakville, Oakworth Road, Keighley, West Yorkshire.

PCW Readers — in a few issues' time — another 3-D Noughts and Crosses program will be featured. PCW.

Pythagorean Triplets

Following the publication of my article, "Three Novelty Programs for a Pocket Calculator", I have received an interesting range of correspondence from readers of PCW. Most of these letters provided proofs that they are infinitely many integer solutions of $x^2 + y^2 = z^2$, by giving a formula for generating an infinite subset of solutions.

My special thanks to those who provided me with the formula given by Oliver Dixon, "Brains v Brawn", PCW December '78, from whom I borrow the term, "Pythagorean Triplets".

It seems that the problem is only part of the enormous problem of finding integral solutions of $x^n + y^n = z^n$.

My article was intended to be entirely non-controversial, but in defence of my statement that calculators are not computers (see P. R. Rowley, Letters December '78) I would just like to add that with cheaper "programmables" no peripherals can be attached, there is no mass storage, and the possibility of manipulating one program by means of another, as with assemblers etc. is prohibited by the storage arrangements; but clearly, the matter is debatable.

Derek J. Chown,
49 Wickham Road, Brockley, London SE4 1LT

6502 Users Club Working Party

We are in the process of forming a National Association for all those working with the 6502 microprocessor (KIM-1, SYM-1, AIM-65, SUPERBOARD II, PET, APPLE II, etc).

We see the objectives of the Association as providing a medium for the sharing of information which will benefit both the new user, and people with more experience in this field.

If you are interested, please contact:

Walter R. Wallenborn, Secretary,
6502 Users Club Working Party
21 Argyll Avenue, Luton, Beds. LU3 1EG
Telephone: (0582 26967) evening.

Privacy — The Prerogative of the Free

In the correspondence in your October and December issues both Dr. Michael Hendry and A. J. Borer miss the point about the confidentiality of the medical record on the microcomputer.

The patient record wherever it is generated can be recorded on floppy discs which can be carried in the doctor's briefcase and not left unprotected in a vast data bank in charge of non-medical personnel. This is a very significant achievement because in the distant past all patients records were kept by the doctor himself and were not available to an outsider without his consent. The era of mass medicine for a larger population has necessitated General Practice and hospital records we all know today which is often too freely available for all and sundry to read.

By using floppy discs when part of the data is required for a second opinion or for statistical returns it can be either printed

out by the computer or transferred on a distributed system to where it is required but *ONLY* with the consent of the doctor.

By recording on a personal computer with a floppy disc unit the technology is enabling the doctor to return to the craft of yesterday with the opportunities of tomorrow.

H. C. Price, Consultant Physician,
Western Hospital,
Seagrave Road,
London SW6 1RZ

Astronomical request

Firstly, I must thank you for your superb magazine and also for the Show which I found highly entertaining. Keep up the good work!

As soon as funds permit I hope to buy a home computer — possibly a PET or TRS-80 and since I'm interested in Astronomy I would welcome any details of relevant software. Reciprocally, I am willing to have a go myself — time permitting of course.

Here's an idea which it might be possible to implement for micro enthusiasts. We have gift, book and record tokens so why not "Software Tokens" for any program material on cassette. New software shops take note!

A s.a.e. for reply would be appreciated with enquiries about astronomical programs.

M. W. Datko,
18 Roman Road,
Luton LU4 9DN, Beds.

Future Shock

After reading 'On The Line' by David Hebditch I am tempted to write to you. I am glad you have now got an article on the social effects of the personal computer and micro's as a whole. This, I'm sure, is going to be the stumbling block in advance. At the moment there is a frightening phrase 'Where there is a micro, there are redundancies'. I think that more discussion should be held on this line, as it is the unions who are going to slow down the advance to a computer society (with good reason at the moment, fear of unemployment and such). Is it possible for education at an early age to help 'line children up' with what will inevitably happen sooner or later (rather sooner)? i.e. would education in leisure activities and such like help ease the problem (if that is the right word) of unemployment.

Maybe Mr. Charles Sweeten could comment on the education aspect of this letter and perhaps a sociologist on other aspects.

Thank you and I hope you can reply or publish this as I feel that it is a problem that ought to be faced now and not when it arises, if it hasn't already.

Paul Williams,
Undergraduate of Mechanical Engineering at
Birmingham University,
37 Torridon Croft,
Moseley,
Birmingham B13 8RG

Another letter from Elisabeth (PCW, Vol 1, No. 9)

In reply to your asking me why the solution that I proposed for clearing the memories of an 8080 computer was not correct.

Since I sent my suggestion to you, I have been informed that although switching the computer off does clear the stores, when it is switched on again, the stores do not become zeroed but take up random states.

I think I may have been misled to some extent by hand held calculators which can be cleared completely by the use of the on/off switch.

Elisabeth Else,
33 Albany Gardens,
Hampton Lane,
Sofihull,
W. Midlands, B91 2PT

PCW After a savage battle with the Publisher, the Editor prised £2 off him and sent it to Ms. Else. PCW.

Ideas

I suspect that there are readers of PCW who often undertake original research relevant to computers and their potential applications, yet who are unable to pursue such research full time as they might wish. This is unfortunate, as one of the benefits of studying at a University (for example) is the ease with which

one's ideas may be discussed with other like-minded people. Such discussion may well improve the quality of an original concept.

It occurs to me that PCW could be a good alternative to a University for the less fortunate students amongst us, by providing a forum for subscribers to contribute articles of an original nature. Of course, such a forum will only work if people can be encouraged to send in their ideas. To this end, it should be emphasised that concepts need not be "complete" to justify publication. In fact, it may well be desirable to ask for contributions concerning ideas which have not been shown to work or are even impractical. Any original study should be welcomed.

Well, those are my ideas, for what they are worth. I hope that you find them interesting.

R. D. Prosser,
8 Sketchley Road, Burbage, Nr. Hinckley,
Leicestershire LE10 2DZ
PCW Readers, how about it? PCW

A seven minute, twenty second, tea break

I read with interest Mr. L. R. Carter's letter in your January issue, about his transcription of an algorithm for evaluating a square root from computer to TI 57 calculator.

Like Mr. Carter, I am interested in the 'programmability' of calculators, and I ran the program on a Commodore PR100. The execution of the program took 13 hours, 5 minutes and 57 seconds!

However, if one combines the principle of the algorithm with the Newton-Raphson formula for finding roots of equations it is possible to write a program for the PR100 which will evaluate the square root of a number to the accuracy of the calculator, and in a very short time compared with using the summation sequence.

For the given number, 99999, the square root takes only 7 minutes 20 seconds — just enough time for a tea break!

I. W. Morrison,
54 The Fairways,
Leamington Spa, Warwickshire CV32 6PS

The NASCOM — Paging it

Nascom users may like to know about the following problem that occurs if they extend their system with additional memory and try to run programs across the page 0 — page 1 boundary.

The Execute command in NASBUG or B-BUG sets the stack pointer at 1000 hex, and although the first instruction of a program may set the stack pointer to a more convenient location, a program residing across the 1000 H boundary will be corrupted by the Execute command pushing the AF and HL registers onto the stack. The solution is to modify the 'reflective' locations 0C3D and 0C3E to the desired new stack address before using the execute command. The locations are reset to 00 and 10 when the system RESET or 'RST 0' are used.

Another useful tip is that the KDEL routine in NASBUG or B-BUG may be called by the single byte CALL 'RST 56'. If the accumulator is first set to zero the delay will be a maximum of approximately 7½ millisecs, and shorter delays can be made by using smaller values i.e. 80 would give 3¾ millisecs.

A Happy New Year to you and congratulations on what is undoubtedly the best computing magazine in the country.

M. B. Scutt, (Director C. C. SOFT)
83 Longfield Street,
London, S.W.18

CRUCial Defence of the TI TMS 9900

I feel I must reply to the statement made by Mr. Aylward in his letter of the Europa buss in the December '78 edition.

In this he states that the 9900 CRU facility is 'just a complicated and difficult to use method of achieving I/O'.

If I may be permitted to explain the facilities offered by the 9900 CRU, perhaps I can dispel this view.

The 9900 CRU is a simple alternative to memory mapped I/O for medium speed applications (i.e. approx. 1 MHz max). It consists of three lines CRU CLK, CRU IN and CRU OUT. These are used in conjunction with the address buss (A3 through A14). Output ports are provided by addressable latches, the SN74LS259 is an example; the CRU information is available as a serial bit stream from the CRU OUT pin. At the same time the CRU address is output on the address buss. This output information is clocked into the latch at CRU CLK time. The address is then changed and the next bit of information transferred. MEMEN is high during CRU operations.

Input information is sampled from the CRU IN line during CRU input cycles. The appropriate address being supplied by

address bits A3 through A14 again. Input interfacing can be done using 8 to 1 multiplexers such as the SN74LS251. CRU CLK is not present during CRU input cycles.

Only address bits A3 through A14 are used for CRU addressing, the address is developed in two ways.

Single Bit CRU Operations

The address is derived by using a base register (WR 12) and adding a signed displacement to it. The contents of bit 15 of the base register are ignored, as bit 15 of an address is the byte indicator. Bits 0, 1 and 2 are also set to zero as the total number of CRU ports is 4096 which only require 12 address bits.

Multiple Bit CRU Operations

The base register is again used, but this time it is incremented for each bit to be transferred, i.e. if base address is zero and we transfer eight bits the final address output will be 0007.

The 9900 supports three single bit CRU instructions; these are:—

SBO Set bit to one; **SBZ** Set bit to zero; **TB** Test bit. and two multiple bit instructions, these can transfer from one to sixteen bits.

LDCR Load communications register; **STCR** Store communications register.

Summing up therefore:

The CRU provides:— 1) Up to 4096 individually addressable input and output ports. 2) The ability to set, reset or test any bit in the CRU I/O field. 3) Multiple transfers of up to 16 bits with one instruction. 4) No bi-directional data buss buffering required. The data buss is not used. 5) Any port can be used as a uart controlled by software. 6) No memory space used up by mapping, all available for program memory.

Reference: TMS 9900 Microprocessor Data Manual; Texas Instruments Limited — Application Report B199; TMS 9900 System Development Manual.

J. R. Gould,
18 Lombard Street, Lidlington, Bedford MK43 0RP

Librarian's Layout

We are now taking the magazine in our library and think it will be very useful.

May I, however, make a small suggestion on layout?

Can you please add the issue date to your running headline?

This is common practice and very useful to all and sundry.

Nan Irvine, Librarian,
London College of Furniture, 41-71 Commercial Road,
London E1 1LA

PCW We've taken up your suggestion. Another reader phoned in with the same advice. PCW.

Praise Indeed

I have been an avid reader of your magazine since issue one and would like to congratulate you upon the quality of your production.

The open format allowing coverage of highly technical items through to non-technical and interest items, software and hardware, is ideal. However, I would like to say that a few more regular items on designing and building homebrew systems, and improvements (treated in a general manner so that they can be applied to as wide a range of micro's as possible) would be welcome.

I believe that many of your readers will be in possession of a home-brew or kit system rather than a commercial micro, if only because of the price. My own start is an MK 14 kit, not particularly impressive I grant you, but it is shortly to be transferred to a new pcb which will allow for full decoding, a VDU, full keyboard and tape in/out plus some extra memory. I started this way as I felt it to be more of a challenge to develop gradually a fully fledged micro from the SC/MP 2 with all its limitations (and some advantages).

This does however pose a major software problem. I am quite capable of writing in assembler for the SC/MP; however, to write say a game program for the Star Trek game without knowing how the game works is, at the best, difficult. Software houses tend to supply PET or CUTS standard BASIC tapes, and since a suitable BASIC interpreter has not yet been produced for the SC/MP (and probably could not be in less than about 16K) these are of no value. Why therefore do they not supply BASIC programs in listing form, as these could then easily be interpreted? Or if they do, then why not advertise the fact.

Still, enough of my complaining, at least your excellent magazine gives some useable software details so perhaps somebody else may sit up and take notice.

Peter Blair, B.A. (Open University) Garthend, 3 Annas Garth Close,
Harmby, Nr. Leyburn, Nth. Yorks. DL8 5PJ

The Agony and the Extra IC

With reference to Mr. McIvor's letter in your November '78 issue. I would like to draw your attention to National Semiconductor's application note AN-176 (contained in MOS/LSI Data Book 1977). This covers interfacing SC/MP with (MM5670 thru MM5674) Calculator Chips, which may save a few of your readers with only one Sinclair Programmable an agonising choice.

R. W. Toogood,

4 St. James Avenue East, Stanford-le-Hope, Essex.

PCW We resisted the temptation for the obvious pun on the writer's name. PCW.

Improved Agility

With reference to the article 'An Agile Algorithm' in last November's issue of 'PCW' Mr. Ferguson's program requires about 10ⁿ iterations to produce an n - digit square root - a slightly more sophisticated program will produce an n - digit root in about 10n iterations, which is a vast improvement if any sort of accuracy is required.

This improvement is achieved through a judicious shifting of the decimal place; an indication of the effect this has is given by the following:

Mr. Ferguson's program requires only 2 iterations to show that $2 < \sqrt{7}$ but requires 200 iterations to show $200 < \sqrt{70,000}$ despite the fact that the latter is immediately obvious from the former.

The full method will, I hope, be made clear by the following worked example and explanatory notes.

Example: Calculate $\sqrt{17460}$

Counter C	Effective Iterations I	Subtrahend 5=I+C	Partial Square P	Remainder R=P-S	Partial Answer A	
1	.0	1	1	0	1	
3	0	3	0	-	-	←S>P
3	20	21	74	53	11	
3	20	23	53	30	12	
5	20	25	30	5	13	
7	20	27	5	-	-	←S>P
1	260	261	560	299	131	
3	260	263	299	36	132	
5	260	265	36	-	-	←S>P
1	2640	2641	3600	959	132.1	
3	2640	2643	959	-	-	←S>P
etc.						

So result to 4 sig. figs. is $\sqrt{17460} = 132.1$

Notes:

1) Initially C = 1, I = 0, A = 0. The square is split into pairs of digits (with the decimal point between two pairs) and P is set equal to the most significant pair.

2) S = I + C is calculated and compared with P.

If $P \geq S$, R = P - S is calculated and A is incremented by one.

Then C is incremented by two, P is set equal to R and the process is iterated (from (2))

If $P < S$ then C is reset to one, I is set equal to $10^{*(S-1)}$ and A is multiplied by ten. P is multiplied by one hundred and has the next pair of digits from the square added to it. The process is again iterated (from (2)).

3) The iteration is halted when A has sufficient significant digits.

I apologize for the length of this explanation (the method is actually easier than it looks) but this is a fast and important algorithm. I hope that my calculation of the square root of a five digit number in eleven steps will encourage people to implement this method on their own machines.

Stephen Marsh,

Merton College, Oxford OX1 4JD

Reader's advice

Reading your magazine, I find it both useful and informative but would like to make one suggestion which I feel is a fair one: when publishing listings of programs and subroutines, would it be possible to include details of the compilers, interpreters, or assemblers which they were written to run with. (I feel that this is most applicable in the case of assembly code listings where such information would save a lot of cross-referencing with processor instruction set summaries to deduce which processor they are written for.)

G. Sweeper,

Programmer, COMPUTER & DESIGN SERVICES LTD.,

19b Moor Road, Broadstone, Dorset.

PCW Contributors, please note. PCW

The Z8000 Zooms In

My recent remarks (Letters, Vol. 1, No. 9) drawing attention to the need for *block move* facilities on computers have been

emphasised by the Zilog Z8000 MPU.

Details have just been received showing that over a third of the possible instruction types relate to various kinds of block operations. Single instructions perform operations that require whole routines on other designs.

Blocks may, in many cases, be up to 8 megabytes in length and processed word by word and/or byte by byte. Moves may increment or decrement so avoiding memory loss when blocks overlap.

The many facilities provided will make such operations as string handling, compiling, program loading, file updates etc., very easy to program.

In brief outline, the facilities offered are as follows:-

- a) Moves of any size block of the 16 registers to or from memory so simplifying interrupts and sub routine operations.
- b) Comparison of a block of memory with a register value for example to find a label or to sort at high speed.
- c) Comparing two blocks of memory word by word or byte by byte.
- d) The basic move of a memory block to a new address.
- e) Indexing one memory block with another.
- f) As in e) but testing the result.
- g) Moving a block of memory to output.
- h) Loading a block of memory from input.

All in all many practical programming needs will be greatly simplified by this wide-ranging approach.

R. G. Silson,

Near Station, Tring, Herts. HP23 5QX

Three dimensional satisfaction

I read and studied, with great satisfaction, Bill Davy's article on '3-D Noughts and Crosses' (Vol. 1, No. 8). I am presently learning BASIC without any tuition and purely out of interest, using a desk-top computer at work. Three months ago I knew nothing about computing, but I seem to be picking it up quite easily so far.

This is mainly due to the chance of following and understanding other people's programs, which your magazine gives me ample opportunity to do. Having grasped how the 3-D program works, and having run it on the 'desk-top', I've come up with this observation: Using the weightings given in table 2 it's far too easy to beat the computer. I've amended the H column to read V=0,3,15,26 and it makes the game a satisfying struggle. Having only run it twice so far, when it won each time, I'm not even certain whether it's possible to beat it; though obviously it can be held to a draw.

As this program works so well with the revised weightings, I cannot imagine that a better algorithm exists. Is this logic sound?

David Smith,

252 Cavendish Street, Ipswich IP3 8BQ

Software Shuffle

Concerning the shuffling of cards: the algorithms given by Mr. Lounds (Letters, September '78) does not make all permutations of the cards equally likely. His algorithm can proceed by any of 52^{52} equally likely ways, but the number of distinct permutations, disregarding suits is $\frac{52!}{(4!)^{13}}$

divide 52^{52} exactly, it follows that some permutations must be generated more often than others. A correct algorithm can be obtained as follows (not tested as I do not have a BASIC interpreter!):

```

100 FOR A = 52 TO Z STEP -1
110 LET R = INT(RND(1)*A + 1)
120 LET V = P(A)
130 LET P(A) = P(R)
140 LET P(R) = V
150 NEXT A
    
```

These lines unchanged

This material can proceed in 52! different ways. In practice I imagine that the difference between the two methods would be extremely small, unless the size of the pack were reduced or the program used very many times.

A. R. Aylward,

54 Trumpington Street, Cambridge.



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Tid Bits

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Integrated Computer Systems Publishing Company is organising a whole series of educational courses. One such course is on Microprocessor Education; Amsterdam, March 6-9; Stockholm, March 13-16; London, April 24-27; Copenhagen, May 15-18. For full details of all courses, including fees and team/group discount write or phone Computer Marketing, 15 Bevis Marks, London EC3A 7LH. Telephone 01-283 3974. Phone numbers for Belgium: (02) 762 60 00 (Brussels); France: (01) 749 40 37 (Rueil-Malmaison); West Germany: (089) 19 80 66 (Munich); Sweden: (046) 30 70 70 (Lund.)

INTEL MDS USERS GROUP

An Intel Microprocessor development system users group has now been formed in the U.K.

The group is entirely independent from Intel and has been formed solely for the benefit of Intel MDS System users.

Membership of the group is free and loosely restricted to those organisations or individuals who either own, hire, use or intend to use either Intel MDS Series I configurations or Intel MDS Series II configurations.

No Intel MDS users group has existed until now although Intel reports that it is going to improve its system of distributing new product information to its MDS system users.

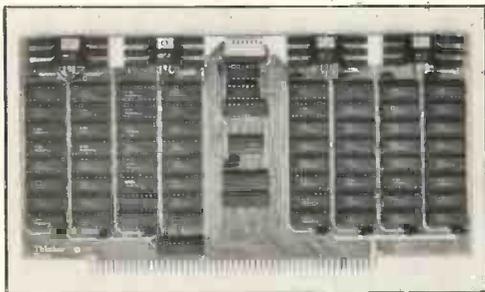
The users group will attempt to keep users up to date with new Intel products and will provide a platform for users software and hardware products.

Currently the users group has clarified for the benefit of new Series II users that Intel has not released in its Series II documentation any detailed software information relating to direct read/write operations to their floppy disc sub-system.

Intel is at present treating this as an oversight and assures Series II users that their configuration is similar to the Series I configuration in this respect and that Series II users wishing to read/write directly to their floppy disc sub-system should purchase the Series I MDS D.O.S. manual.

The users group is keen to expand its membership and any organisation or individual wishing to join the users group should write to: **Intel MDS Users Group, 29 Chaucer Road, Bedford.**

The **SuperRam™ 32K** static RAM board is a recent addition to the line of S-100 memories designed by George Morrow. It uses the National 5257 or the TI equivalent 4044 Kx1 NMOS memory chips and can be run at 2 MHz for standard 8080 systems or 4 MHz for Z-80 systems. A phantom option has been provided for CPUs using this line. All control signals, addresses and data lines are fully buffered. Each 16K block is independently addressable and write protected. This board contains only seven support ICs and the typical power consumption is 2.6 amps.



Superam™ 32K Static RAM Board

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Further information: **Hilda Sendyk, (415) 524-2101, 1202 10th Street, Berkeley, CA 94710, USA.**

COMPUTER ART EXHIBITION

A computer art exhibition held last November at the offices of **Zeus-Hermes**, the real-time and communications software specialist. Zeus-Hermes sponsored three prizes for the best pieces of work on show that evening, provided that the piece was directly related to computing, either by content or by how it was produced.

Both these categories drew a good selection of interesting and accomplished works of art. The competition was judged by Alan Cane, Sue Ritchie, a designer who works for Zeus-Hermes, and Mick Punter, Zeus-Hermes Managing Director. The winner was Chris Emmet with "Serpent's Egg" a vivid impression illustrating the passing of the year. It was produced by a Stromberg-Carlson microfilm plotter and then screen-printed for the colours. Runner-up was Colin Jones with a montage of computer "output", and the other prize winner was Dr D Vince with "Seahorse" (SHRINK). This was produced with a plotter and a program called PICASO. SHRINK is the routine which produced the remarkable effect of the Seahorse, the outline of which is reproduced smaller and smaller until arriving at a central point.

Further information:

Mick Punter, Zeus-Hermes, Tel: 01-323 0637



Picture shows Sue Ritchie — Director of SoftPlum — a design house subsidiary of Zeus Hermes and Mick Punter — Managing Director of Zeus Hermes — studying exhibits.

Hard Disk Fact

IMSAI MANUFACTURING CORPORATION has introduced the HD-10 Hard Disk Systems, featuring the CDC Hawk Model 9427H hard disk. HD-10 provides 10 megabytes of formatted on-line storage per unit.

The 9427H is a "high-performance, random access storage device which uses a single fixed disk for 5 megabytes of storage". An industry standard 5440-type removable disk cartridge provides an additional 5 megabytes of storage. This removable media capability allows for file back-up and unlimited off-line storage. Average random access time is under 35 milliseconds, faster than floppy disks.

HD-10 is compatible with all IMSAI 8080/85-based micro-computers. The system employs a single S-100 bus I/O board to interface with up to two external disk controllers. Each controller supports up to four hard disks. Therefore, any IMSAI system may be expanded to 80 megabytes of hard disk storage with only one I/O card.

Included with the HD-10 system is the new IMDOS II operating system. Any applications written under IMDOS will run under IMDOS II with little or no modification. Simply assign the hard disk as the logical device used by the application. All of IMSAI's utilities and languages will also run. IMDOS II is compatible with other versions of IMDOS and CP/M® Version 1.33.

Contact: **Imsai Mfg. Corp., 14860 Wicks Blvd., San Leandro, CA 94577, USA. Phone: (415) 483-2093**

CROMEMCO COBOL

The Cromemco Z2-D and System 3 with 48k Byte memory now have COBOL, implemented to ANSI 1974 standard with all level one features and the most useful features of level 2. Price £85.

Contact:

John Lamb, Marketing Director, Comart Ltd., P.O. Box 2, St. Neots, Huntingdon, Cambs PE19 4NY

Another Newbear Fact

A 63 key ASCII standard keyboard capable of producing all upper and lower case alphanumeric symbols and control functions. The keyboard requires only the addition of a 5 volt power supply.

A simple optional switch allows the selection of upper case only or upper and lower case and a red LED is provided as standard to indicate when the keyboard is in upper case mode. The keyboard is fully debounced.

All inputs and outputs are TTL compatible and follow normal 7400 series loading and level requirements. Positive logic is used, the eighth bit is an optional parity bit, and parallel output is standard. Serial output can be provided by the addition of a serial clock.

The complete kit is £56 (Unencoded keyboard £27.50), details are available from Newbear.

Details:

John Day, Newbear Computing Store, 7 Bone Lane, Newbury, Berks RG14 5SH. Telephone: Newbury (0635) 49223



Newbear's ASCII Keyboard

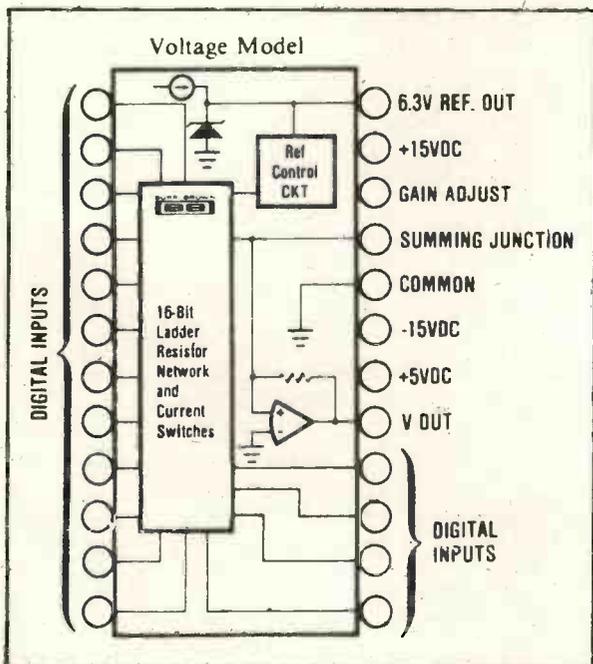
Low Cost 16 bit D/A Converter from Burr-Brown

Burr-Brown have announced a "revolutionary" digital-to-analogue converter which provides good performance and high reliability at "the lowest cost ever for a product of this type."

The DAC 71 is available for three types of digital input at TTL levels (complementary offset binary, complementary straight binary and complementary binary-coded decimal), and there are versions with either current or voltage output (six models in all). All are housed in 24-pin DIP compatible ceramic packages and are intended for use over the industrial temperature range from 0 to 70°C.

Significant figures from the specification of the DAC 71 include a maximum linearity error of $\pm 0.003\%$, and a maximum total error over the operating temperature range (including gain, offset and linearity) of $\pm 0.083\%$ of full-scale reading. Output is 0 to 10V, $\pm 10V$, 0 to $-2mA$ or $\pm 1mA$, depending on the model.

Cost is £31.20 (100-off DAC 71 current output). For use in such equipment as function generators, test equipment, calibration standards, machine tool controllers, graphic composition machines and anywhere else where a very high resolution D to A converter is required.



More information:
Roger Isaacson, Burr-Brown International Ltd., 17 Exchange Road, Watford, Herts WD1 7EB. Telephone: (0923) 33837

TRS-80 Software

Lifeboat Associates, offers "the first professional disk-based language and utility package for the Radio Shack TRS-80 computer". Written by Microsoft, creators of Level II BASIC, it runs on a TRS-80 system with 32K RAM, one or more drives and TRSDOS. The software is supplied on diskette and consists of:

- FORTRAN — a true relocatable machine code compiler for ANSI FORTRAN X3.9 (except COMPLEX variables);
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- LINKING LOADER — to link-edit and load FORTRAN and assembler modules for execution; and,
- DISK TEXT EDITOR — to create and modify FORTRAN and assembler programs as disk files; also can be used as a general purpose text editor for correspondence and other documents.

Available at the discount price of \$325 per computer system plus \$2 shipping (\$5 foreign) from: Lifeboat Associates, 164 West 83rd Street, New York, New York 10024. Telephone: (212) 580 0082. (Dealer inquiries invited).

The Microcomputer Investors Association is U.S. based, at 2415 Ansdel Court, Reston, Virginia 22091. Its members participate actively in contributing to its journal, *The Micro Computer Investor*. The January '79 issue has eighteen articles and 214 pages. The emphasis is on utilising micros to make and/or manage investments. Articles deal with subjects as Elements of Estate Planning, Data Smoothing, and Investment Opportunities in the Microcomputer Industry. Those interested in membership should send a self-addressed envelope with sufficient funds for postage to J. Williams at the above address.

TEXAS INSTRUMENTS TI 58 Navigation package

Navigatronic is a package for the TI 58 programmable calculator. Features: up to 480 program steps, a marine navigation solid-state program library, and a 12-24 volt dc adaptor/charger. Also supplied is a 220V ac adaptor for shore use. A comprehensive library of 30 programs is available at the touch of a key: coastal navigation programs, celestial navigation programs and sailing and tactical programs. An additional diagnostic program is used to verify the proper operation of the TI 58 and the library/calculator interface.



TI 58



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Other systems available include the
C3 OEM with 32K RAM, 512K of disk storage and
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HORIZON



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PROFESSIONAL HARDWARE

Use of the North Star Horizon for a short period will enable you to appreciate the professionalism in the product. There's a solid well-built chassis, a good power supply, a quiet fan and an attractive wooden case. There's a Z80A processor running at 4MHz with the 250ns static RAM boards.

There are dual integral Shugart minifloppy drives (capacity of about 360 KB on line, with an option for a further two drives), enabling easy and quick handling and copying of programs and data files.

And of course, there's the 12 slot S-100 bus which enables you to plug in many types of peripheral boards, including a hardware floating point board for increased "number crunching" performance.

PROFESSIONAL SOFTWARE

North Star Computers built their professional reputation around their powerful, but simple, Disc Operating System and Disc Extended BASIC Interpreter.

The latter contains, in addition to the usual BASIC commands, random and sequential access disc files, strings, string operators, multiple dimensioned arrays, formatted output, machine language CALL, memory EXAMine and FILL, line editor, program chaining and more.

The CP/M operating system is also available as an option and provides access to a Macro Assembler, C BASIC Compiler and FORTRAN-80 and COBOL-80 Compilers. A standard UCSD PASCAL has now been implemented.

TYPICAL APPLICATIONS SOFTWARE

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The Major LSI chips

The microprocessor employed in the system is the 6502, operating at a clock frequency of 1 MHz. This is the microprocessor of KIM and Pet fame, and as such has an increasing amount of software available.

There are two 6522 versatile interface adaptors (VIA) in the system, which are powerful chips containing two 8-bit bi-directional ports, two interval timers, a serial-to parallel/parallel-to-serial shift register, and input data latches on the peripheral ports. Several of the peripheral I/O lines can be controlled by the timers, allowing the generation of programmable frequencies, external pulse counting and timing of real time events. There is an extra socket on the board allowing a third 6522 chip to be added.

One 6532 RAM, I/O, timer chip is fitted on the board. This chip has similar capabilities to the 6522 but includes 128 bytes of RAM. A further refinement of this chip is a programmable edge detect interrupt circuit. The board does not have sockets for additional 6532 chips.

Memory in the SYM-1

On-board ROM consists of a 4K x 8-bit chip containing the SUPER-MON monitor which will be discussed later. There are sockets for a further three ROM chips, which Synertek project will be used to hold an 8K Basic interpreter and an editor assembler. Thus expansion of the system to include a high level language is very simple.

The RAM provided consists of the 128 bytes present in the 6532 chip and a further 1K in the form of two 2114 (1024 x 4-bit) RAM chips. Sockets are provided to allow expansion of the on-board RAM to 4K.

Input/Output

General I/O lines are present on the 6522 and 6532 chips. Four of these lines have a single stage transistor buffer with "circuit positions" provided for the user to add resistors, capacitors and diodes in various positions to configure inverting, non-inverting stages, input resistive or capacitive coupling, etc. This is a very useful feature for interfacing peripheral devices and is just one of the many well-thought-out features provided on the SYM-1 board.

A TTY interface is present on the board and full instructions for its use are given in the reference manual. The use of a TTY requires a -9v to -15v line to be added, and adjustment of a resistor within the interface allows different current loops to be used. The resistor installed is 300 ohms, and with a -10 volt supply this gives a 20mA current loop.



An RS232 interface permits the use of a VDU with the system and the addition of a TV/KBD interface module allows the use of a domestic TV. Again, full instructions for attaching a VDU to the system are given.

The cassette interface allows the storage of programs and data in two formats. The first is Kim compatible at 135 baud, the second is a high speed 2400 baud version. In both cases the cassette records are given an identifier tag and the software included in the ROM facilitates searching for a particular program.

The cassette system is quite reliable in operation. However, some users have reported difficulty in selecting a suitable recorder for the system. So it would seem better to borrow and try out different makes of recorders before buying one for the SYM-1.

One recorder I have found particularly suited to audio cassette data storage is the Decca Legato. This recorder proved adequate for use with the SYM-1, but is apparently out of production. Perhaps users of the SYM-1 could write to PCW giving details of recorders they have found suitable.

It is often the cassettes themselves that cause problems, both in tape quality but also in the quality of the spool mechanisms. Smaller cassette lengths are advisable. (PCW Readers, send in your recommendations, stating also the system you are using. PCW). I have found Memorex MRX2 oxide tapes often adequate, as was the case with the SYM-1.

Record/Replay Levels

The setting up of correct record and replay levels is simplified in the SYM-1 by the generation of "sync" tapes. These tapes are played back to

the computer and the tone and volume controls of the tape recorder are adjusted until an "S" on the hex display disappears. Very clear instructions are given for attaching and adjusting a tape recorder.

An unusual addition to the interfaces is one provided for the generation of alphanumeric and graphics on an oscilloscope. The circuit is ingenious in theory and relies upon the generation of a sawtooth waveform on the scope, which may be "switched off" or blanked under program control. Thus a dot or line may be generated at any position on the scope screen. The sawtooth waveform is "switched off" by grounding the output of the interface thereby causing a fast return of the scope beam from its present position, to the zero volts level. (See Fig. 2).

In practice, I found that this method rarely produced clear characters (the program for generating characters is provided with the system) and three different oscilloscopes were tried without much success.

The problem is that this method relies on a fast return to zero volts of the sawtooth waveform effectively blanking the beam, and on the scopes I tried, this did not prove adequate.

Another annoying feature of this method is that when characters are generated they are effectively "underlined" on the scope by the beam at its zero volt level. Often the beam spends more time "switched off" at zero volts than it does generating the characters, and so a very bright line is generated at zero volts.

However, for all that, this output is very well worth persevering with and hints are given in the reference manual for its adjustment. For potential users with their own scopes, the superior quality of most scope graphics cannot be overstressed. The

particular advantages are the speed and resolution at which graphics can be displayed. The approach I adopt, is to employ two D/A converters for X and Y outputs; Z-mod blanking is provided by a third line and gives a true blanked beam. The SYM-1 could be adapted for such a display technique by using its I/O lines, and two R2-R networks can provide a cheap alternative to the D/As.

written programs may incorporate them.

One section in the reference manual is devoted to advanced monitor and programming techniques. A fully annotated listing of the monitor program is also provided. All the normal monitor functions are present with some extra features. These commands are outlined in Table 1.

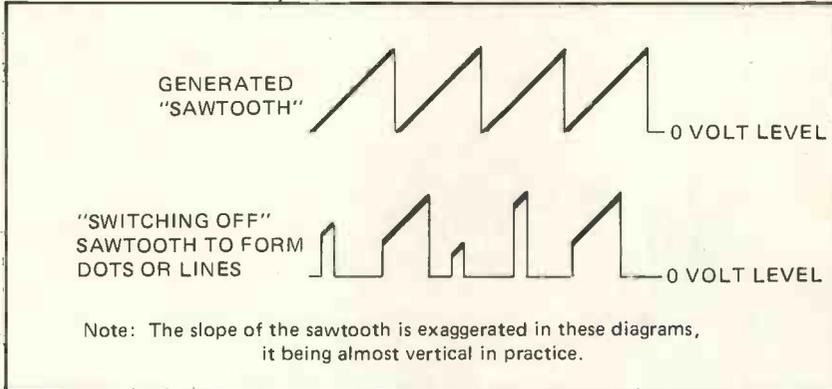


Figure 2

It was noted earlier that four I/O lines are buffered and one of these could be used to generate the Z-mod blanking signal. In fact the on-board scope interface could be greatly improved by using one of these buffered lines to blank the scope beam more effectively.

All I/O in the SYM-1 is memory mapped, and the reference manual gives detailed information on memory address allocation in the form of diagrams and text. The I/O lines are brought to various edge connectors on the board. (See Fig. 1). An expansion port containing the address and data lines is brought to an edge connector, full details being given on how to expand the memory and I/O facilities using this connector.

The Keyboard and Monitor

The keyboard supplied is a twenty-eight double function keypad, the layout of which is shown in figure 3.

The keypad is touch sensitive with audible response (an on-board speaker) on all keys except debug on/off. The review computer's speaker was damaged in transit — a good argument against packing manuals along with a computer. The omission of an audible response on the debug on/off key is, I feel, a mistake; you tend to press this key harder to ensure the correct function is selected, perhaps reducing the life span of the key.

The SUPERMON monitor is one of the most versatile I have come across in systems of the SYM-1 type. After all, it does occupy 4K! The whole of the monitor is well organised, and the addresses and descriptions of the subroutines it contains are fully documented, so that user

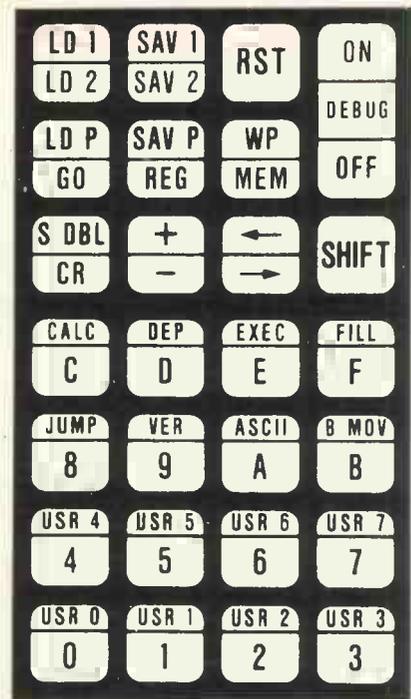


Figure 3

The provision of user keys is an instance of good keyboard monitor interaction. These keys, when pressed, generate a hash code which is not recognised by the monitor, so causing it to go to a vector contained in ROM. This normally points to a return to subroutine sequence, but may be modified to point to a program in RAM which checks for a particular hash code and then performs a user written routine. The use of these keys allow the already comprehensive monitor to be greatly extended.

The debug key when "on" causes the computer to single step through a routine on a go command. This may be modified to perform an automatic trace. Here the program performs an instruction, pauses, displays

the contents of the program counter and accumulator and then performs the next instruction. This trace routine may be further modified to perform a user written trace routine which may display any data required on each program step. A listing is supplied for a program which implements a trace routine that displays the next instruction op-code to be performed.

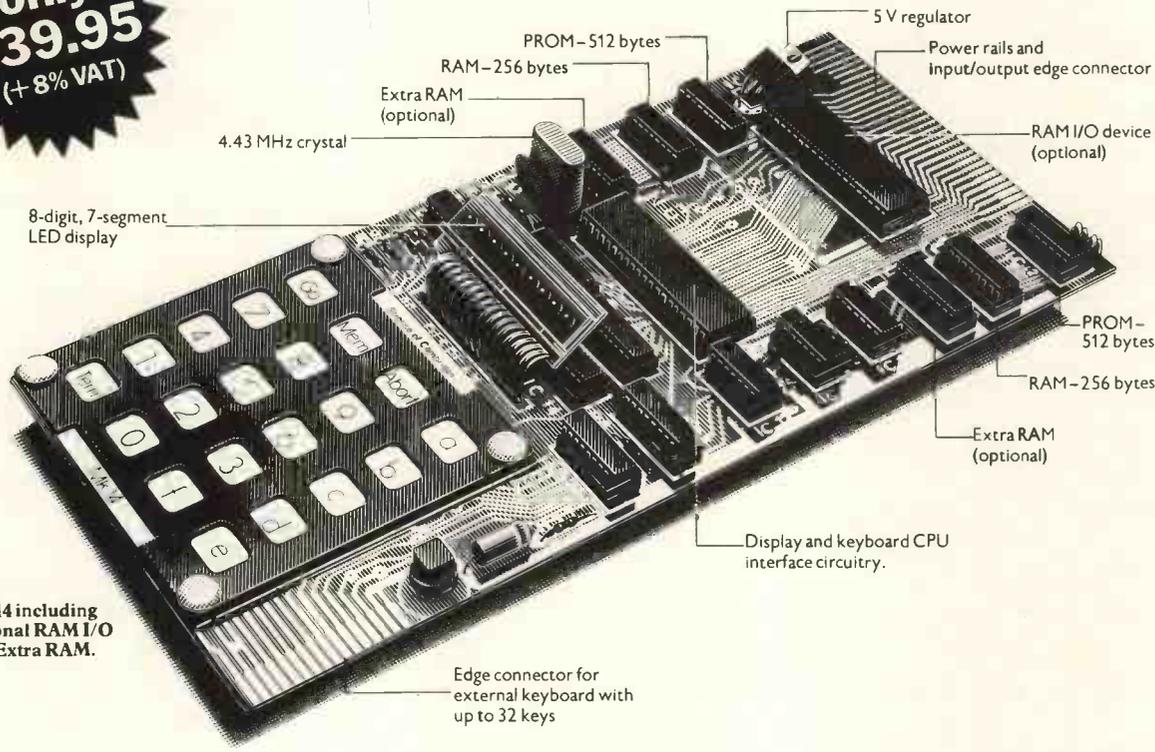
In this review I have only been able to convey a fraction of this computer's capabilities. Apart from a few minor problems, I was most impressed by its performance and versatility. The whole computer is well thought out, and the manuals are very good. Many thanks to Newbear for their loan of the SYM-1 for a generous length of time.

KEY	FUNCTION
MEM	Memory Examine/Modify
REG	Register Examine/Modify
GO	Resume execution at address contained in program counter
VER	Display 8 bytes of data with their checksum
DEP	Deposit to memory at address given
CALC	Calculate displacements 2's complements etc.
BMOV	Block move of data from one area to another
JUMP (n)	Loads PC with address specified in jump table at point n. (n has the range 0 - 7)
SDBC	Store double byte
FILL	Fill defined block of memory with defined byte
WP	Write protect user RAM
LD1	Load KIM format record from cassette
LD2	Load high speed record from cassette
LDP	Load paper tape record
SAVP	Save paper tape record
SAV1	Save KIM format cassette record
SAV2	Save high speed format cassette record
EXEC	Adjust input vectors to receive input from RAM
CR	Carriage return (command string terminator)
+	Advance 8 bytes
-	Retreat 8 bytes — also parameter delimiter
→	Advance 1 byte or register
←	Retreat 1 byte or register
USR0-7	User keys (see text)
SHIFT	Select upper case function
RST	System reset
DEBUG ON	Turn hardware debug function on
DEBUG OFF	Turn hardware debug function off
ASCII	Next two keystrokes (hex) will be combined to form 1 ASCII character.

Table 1

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TEACH-IN

Two's Complement

(with apologies to Strich & Sinden)

Bob Gidden

The Problem

A problem arises in Machine Language Programming with the handling of

Negative numbers merely correspond to ordinary numbers *measured in the opposite direction* to the positive variety. (Fig. 2).

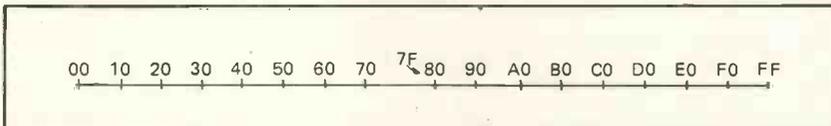


Figure 1. Ordinary 0 to 255 Representation (in Hex).

negative numbers. All is well provided we stick to the use of positive numbers in the range of 0 to +255 (for an 8-bit machine) (Fig. 1).

For example (using Hexadecimal notation):

Hex	Binary
48	: 0100 1000
-16	: 0001 0110
=32	: 0011 0010

[Hex uses 16 digits, so that there have to be new symbols for 10 (= A), 11 (= B), 12 (= C), 13 (= D), 14 (= E) 15 (= F). So, for instance, 18 is written F3 in Hex].

But what happens if we subtract a larger number from a smaller?

Decimal	Binary
16	: 0001 0110
-48	: 0100 1000
=	1100 1110

this, provided we don't ask awkward questions about where the 'borrow' for the left-most bit subtraction came from! Now this answer in Hex is CE, a number *higher* than either of the starting numbers: how can we explain this? Is it just an error?

One way of looking at the idea of negative numbers is with a graph.

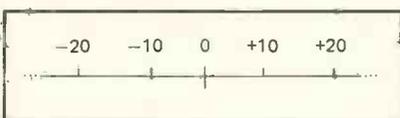


Figure 2. Positive and Negative Direction

Another way of looking at a negative number is to think of "-20" as "0 minus 20". If we translate these Hex numbers to binary, this becomes:

bit no	: 7654 3210
0	: 0000 0000
-20	: 0010 0000
=	1110 0000
=	EO (Hex)

Working from right to left as usual, bits 0 to 4 are obvious. Bit 5, when subtracting 1 from 0, needs a

On the most practical level, this bit of chicanery is justified only if it makes the arithmetic work! The result, translated to Hex, is E0 and corresponds to a count of 20 *down* from the FF end of the scale (or rather from Hex 100). This means that to the *left* of 00 in Fig. 1, we can *imagine* a scale continuing, not with -1 down to -10, -20 etc., but with FF down to F0, E0 etc. This is shown in Fig. 3. The top line of figures is the actual Hex version of the stored binary, and the lower line is the *interpretation* of these as negative numbers to the left of 00.

Since we still have only 256 different numbers in an 8-bit word, this notation limits us to -128 to +127 (decimal). If the left most bit (bit 7) is a 1 (actually the number is stored as 80 to FF) then we must *regard* the number as negative *if* we are working in 2's complement form.

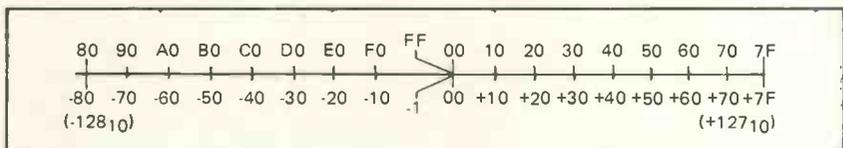


Figure 3.

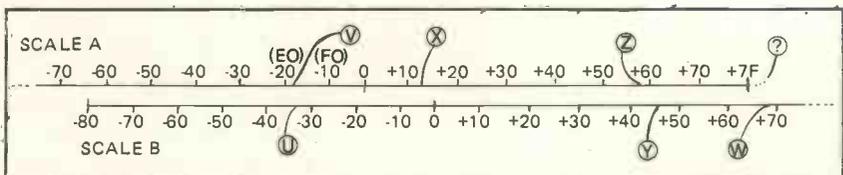


Figure 4. Addition and Subtraction

'borrow' from the bit 6 column, so as to subtract 1 from 10. The answer is 1, but we now have to repay the borrow to the bit 6 column. Immediately the same problem arises: continuing further left-ward, we obtain a string of 1's. In the bit 7 column, we borrow from the *non-existent* bit 8 column to obtain the final one! This is usually noted in the same way as a carry in addition.

Using Two's Complement Numbers

(i) *Addition* (see Fig. 4)

Suppose we wish to add 48H to 16H? Start from the 00 on scale A (the upper one), move 16 to the right (point X) and position the zero of Scale B there. Then use Scale B to measure a further 48 to the right (point Y) and read off the answer on Scale A: 5E (point Z)! (Any who

notice a resemblance to a previous generation of computers, made of funny white plastic strips, immediately date themselves in the prehistoric era!)

In binary, we get:

```

16   :   0001 0110
+48  :   0100 1000
-----
=    0101 1110, which is 5E.
    
```

So far, so good, but we picked the easy one first! What about 16 + 6C? After a lot of carry 1's, we get:

```

16   :   0001 0110
+6C  :   0110 1101
-----
=    1000 0011, which is 83,
    
```

which looks quite reasonable until we remember that if bit 7 = 1, we regard the number as **NEGATIVE!** In other words, a carry into bit 7 must be regarded as an **OVERFLOW** as the biggest one-byte number in 2's Complement Arithmetic is 7F. (This can be seen on Figure 4 as: point X + point W gives an answer at point ?, off the end of the scale). Of course if we were using several bytes to hold the number so as to get a bigger possible range, then we could reset bit 7 to 0 (i.e. 83 becomes 03), and carry a 1 into the next byte to the left.

(ii) *Subtraction*

The problem 16 - 35 can also be visualized with our scales. Position Scale B Zero against the first number (16 on Scale A) as before. Now this time we move backwards 35 to point U; and read off the answer on Scale A at point V as -1F.

Trying this in binary:

```

16   :   0001 0110
-35  :   0011 0101
-----
=    1110 0001, which is E1.
      Oh dear!
    
```

All is not lost however, if we remember that since bit 7 = 1, the answer can be thought of as a negative 2's Complement number:

```

0   :   0 000 0000
-E1 :   1 110 0001
-----
=    1 001 1111
or   - 001 1111, that is -1F
    
```

So we subtract in binary and if the answer is negative, the correct absolute value (i.e. number without sign) is the 2's Complement. Actually on the machine, there is an operation to do this for us painlessly, called **NEGate** usually.

If we subtract a large positive number from a small negative number, we can run into overflow problems again by going off the end of the scale left-wards past 80. This can be dealt with in a similar fashion to that for addition.

For the 6800

In the case of the 6800 system, the current state of affairs is kept track of by the Condition Code Register. The N bit indicates if the number can be regarded as negative or not (bit 7 = 1 or 0) and the BMI and BPL branches can be used to act accordingly. The V bit shows if an overflow has occurred (either in addition or subtraction) into bit 7, thus corrupting the sign. The branches BVS and BVC sense this. The C bit is set if a carry or borrow (as appropriate) had to be made out of "bit 8", and BCS or BCC may be used in this case. Combinations of the Sense bits may readily be acted upon by the other Conditional Branch Instructions, thus enabling one to perform any arithmetic operation without worrying too much about what is going on at the binary level.

If you wish to try out what is happening, I have described a program for the 6800 which does simple one-byte arithmetic and then prints out the CCR contents followed by tests of whether a branch would have occurred in the case of each conditional branch. By trying such a program for yourself, it is possible to gain more familiarity with these ideas.

6800 Conditional Branches

I must make clear straight away that I am no expert on this subject, but possibly this helps me to pinpoint possible areas of confusion! I have not seen a simple explanation of Conditional Branches, and the brief section in a Motorola 6800-manual merely left me more confused. Is FF greater than 10 or not? Apparently sometimes it is, but not at other times - it depends on whether you regard FF as -1 or as +255!

Well, that 1/4-inch square piece of Silicon inside the black plastic obviously understands it, so my approach in all such cases is to try it and see. Purely exploratory software does not have the potential for producing blue smoke (with a dull-red glow somewhere underneath?) that similarly novice-built hardware does!

The program attached is intended to make the machine teach me how it decides whether to branch or not. Even the most halting programmer can cope with BEQ (and therefore BNE too) - it either is equal, or not! But what is the difference between a carry, an overflow, and a half-carry(!)? Merely load the program and ask it! Enter a two-character Hex number, then a symbol to say whether you want addition or some other operation, and then a second Hex number. These are converted to Binary and the answer is also printed in both Hex and Binary. The con-

tents of the Condition Code Register (CCR) and the results of the branching tests (Y if it would branch with each code in turn, N if not) are then given.

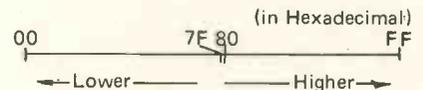
The program is located in the 2000 block, but may readily be shifted elsewhere; the addresses that need changing are 'flagged' with a % symbol after the mnemonic code.

The Bits

The I bit to indicate an Interrupt is not concerned with conditional branches, and the half-carry bit, H, is not directly testable by a program, being mainly used by the 'Decimal Adjust' instruction, DAA. The Zero bit, Z, should be straightforward, using the BEQ or BNE instructions. That leaves us with the N, C, and V bits.

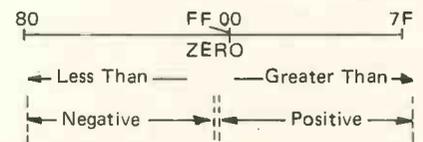
To interpret these you have to decide whether to regard FF as -1 or not. If so, you are working in what is called "2's Complement Notation", which I attempted to explain earlier.

For now, let us regard the numbers as being set out on a scale, like a ruler:



and we may use BHI or BLS to distinguish between numbers at different places on the scale, or in the same place.

Now imagine that we saw the ruler in half between the 7F and 80 marks and swap the pieces over (keeping the figures the same way round so that you can read them!), and stick the two ends touching (the ones labelled FF and 00):



Thus we see that FF is 1 to the left of ZERO, i.e. it is -1! If we use this way of handling both positive and negative numbers, we can of course only use numbers between -128 and +127, instead of the full 255 for all-positive numbers. The consequences of this have been described. The BGT, BGE, BLE and BLT codes apply most usefully in this case. Thus if 10 is compared with FF, then 10 does turn out to be "greater"!

CMP may be treated as a SUB, and BIT may be treated as an AND, except in these two cases, the original number in the Accumulator is left intact after the operation, so that further use may be made of it.

Listing Overpage

Branch Tester

BRANCH TESTER VER 2

* ALTER ADDRESSES MARKED % IF YOU RELOCATE

```

2000          ORG $2000
2000 CE 20C5  START  LDX #MSG1          %   TITLE
2003 BD B07E  JSR PDATA1
2006 0E          CLI
2007 8D 59     LOOP  BSR CRLF          New line
2009 8D 4B     BSR OUTS          & space
200B BD B055  JSR EYTE          Get first number,
200E B7 A020  STAA NO1          & store
2011 8D 43     BSR OUTS
2013 8D 53     BSR BINOUT        O/P as Binary.
2015 8D 4B     BSR CRLF
2017 BD B1AC  JSR INCH          Get Op-code
201A 36          PSHA          & save it.
201B BD B055  JSR BYTE          Get No 2
201E B7 A021  STAA NO2
2021 8D 33     BSR OUTS
2023 8D 43     BSR BINOUT
2025 CE 2106  LDX #MSG2          %   'HINZVC' etc.
2028 BD B07E  JSR PDATA1
202B 33          PULB
202C B6 A020  LDAA NO1          Recover Op-code to B-reg.
202F 8D 66     BSR QADD          Recover first No.
2031 36          PSHA          Go check & execute.
2032 07          TPA          Save Ans dont alter CCR
2033 B7 A023  STAA CCRST        Get CCR & store
2036 32          PULA
2037 B7 A022  STAA ANS          Recover Answer.
203A CE A022  LDX #ANS          Point to it
203D BD B0CA  JSR OUT2HS        & output
2040 B6 A022  LDAA ANS          also in Bin.
2043 8D 23     BSR BINOUT
2045 8D 0D     BSR OUT2S
2047 F6 A023  LDAB CCRST        Get CCR back.
204A 58          ASLB
204B 58          ASLB
204C 86 06     LDAA #6          Only 6 bits in CCR
204E 8D 1B     BSR BINOUT+3
2050 8D 29     BSR BRANCH
2052 20 B3     BRA LOOP          Check on branching
                                     Go back for another sum.
    
```

* SUBROUTINES USED BY PROGRAM

```

2054 8D 00     OUT2S  BSR OUTS          O/P two spaces
2056 B7 A024  OUTS   STAA TEMPA        Save A-reg
2059 86 20     LDAA #20          & O/P a space
205B BD B1D1  JSR OUTCH
205E B6 A024  LDAA TEMPA
2061 39          RTS
    
```

```

2062 CE 213F  CRLF  LDX #MSG3          %   CR & LF: new line
2065 7E B07E  JMP PDATA1          (RTS at end of that)
    
```

* OUTPUT CONTENTS OF A-REG AS BINARY STRING

```

2068 16          BINOUT TAB          PUT No in B-reg
2069 86 08     LDAA #8          8 bits to be O/P
206B 36          BIN1  PSHA          Save bit count
206C 4F          CLR A
206D 58          ASLB
206E 24 01     BCC BIN2          Shift bit into Carry
2070 4C          INCA          is it 0 or 1?
2071 8B 30     BIN2  ADDA #30        Add ASCII offset
2073 BD B1D1  JSR OUTCH          Get bit count back
2076 32          PULA
2077 4A          DECA
2078 25 F1     BNE BTN1          Done 8 bits yet?
207A 39          RTS
    
```

* TESTS STORED CCR WITH ALL BRANCH INSTRUCTIONS

```

207B 05 22     BRANCH LDAB #22        First Cond Bra Code
207D F7 20B6  STEP  STAB CODE          %   Sorry! Self-modifying!!
2080 8D D2     BSR OUT2S
2082 B6 A023  LDAA CCRST
2085 06          TAP
2086 20 04     CODE  BRA YES          Sets up CCReg.
2088 86 4E     LDAA #'N          (Replace BRA w. BHI, etc)
208A 20 02     BRA OUT          If didnt, load N
208C 86 59     YES   LDAA #'Y          If did, load Y
208E BD B1D1  OUT   JSR OUTCH
2091 5C          INCB
2092 C1 30     YES   CMPB #30        Step to next BRA type
2094 25 E7     BNE STEP          Done yet?
2096 39          RTS          If not, go round
    
```

* EXECUTE CORRECT OPERATION

```

2097 C1 2B     QADD  CMPB #'+'        Query ADD? (+)
2099 26 04     BNE SUB          if not, jump
209B BB A021  AD7A NO2          Else add
209E 39          RTS          & return
209F C1 2D     SUB   CMPB #'-'        Similarly the others;
20A1 26 04     BNE AND          (- SUBtract)
20A3 B0 A021  SUBA NO2
20A6 39          RTS          (& AND)
20A7 C1 26     AND   CMPB #'&
20A9 26 04     BNE OR          (. OR)
20AB B4 A021  ANDA NO2
20AE 39          RTS
20AF C1 2E     OR    CMPB #'.'
20B1 26 04     BNE EXOR
20B3 BA A021  ORAA NO2
20B6 39          RTS          (E Exclusive OR)
20B7 C1 45     EXOR  CMPB #'E
20B9 26 04     BNE ERROR
20BB BB A021  EXORA NO2
20BE 39          RTS
20BF 8D A1     ERROR BSR CRLF        Request unreckognized:
20C1 31          INS          restore stack
20C2 31          INS          & restart.
20C3 7E 2007  JMP LOOP          %
    
```

* TITLE & MESSAGES

```

20C6 0D          MMSG1 FCB 13,10,0,0,0
20CB 20          FCC / BRANCH TESTER /
20DD 2B          FCC /+ ADD - SUB & AND . OR E EXCL OR/
2105 04          FCB 4
2106 20          MMSG2 FCC / HINZVC HI LS CC CS NE EQ /
2121 56          FCC /VC VS PL MI GE LT GT LE/
2138 0D          FCB 13,10,0,0,0,3D,4
213F 0D          MMSG3 FCB 13,10,0,0,0,4
                                     END
    
```

Some Examples of the output of the Program:

```

J 2000
BRANCH TESTER + ADD - SUB & AND . OR E EXCL OR
16 00010110
+C 01101100 HINZVC HI LS CC CS NE EQ VC VS PL MI GE LT GT LE
=82 10000010 101010 Y N Y N Y N N Y N Y N Y N Y N

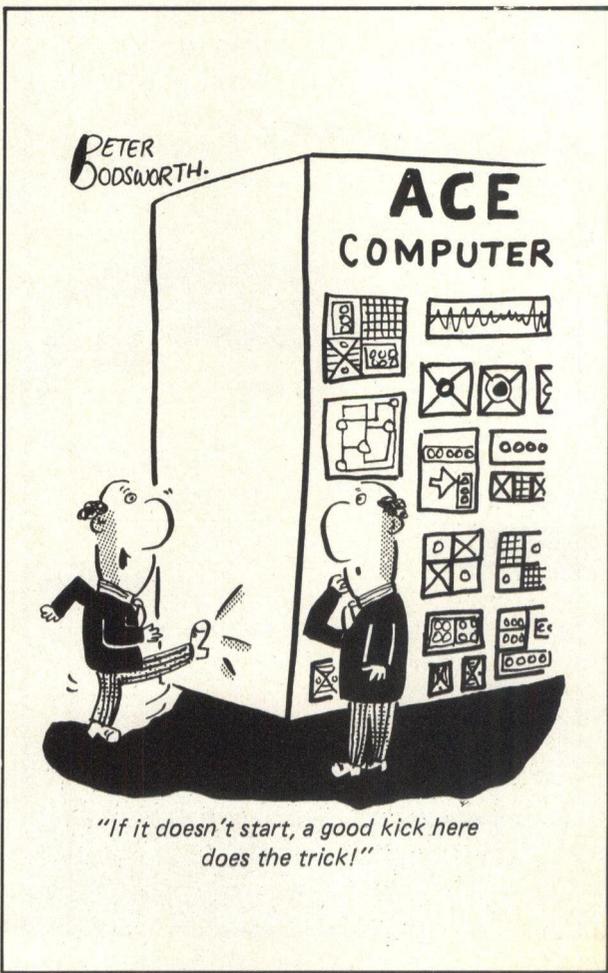
4E 01001110
-CC 11001100 HINZVC HI LS CC CS NE EQ VC VS PL MI GE LT GT LE
=82 10000010 001011 N Y N Y Y N N Y N Y N Y N Y N

A5 10100101
.A 010101010 HINZVC HI LS CC CS NE EQ VC VS PL MI GE LT GT LE
=FF 11111111 001000 Y N Y N Y N Y N N Y N Y N Y N Y

5A 01010101
&A5 10100101 HINZVC HI LS CC CS NE EQ VC VS PL MI GE LT GT LE
=00 00000000 000100 N Y Y N N Y Y N Y N Y N N Y N

7C 01111100
EAM 10100100 HINZVC HI LS CC CS NE EQ VC VS PL MI GE LT GT LE
=D8 11010100 001000 Y N Y N Y N Y N N Y N Y N Y N Y

09 00001001
+09 00001001 HINZVC HI LS CC CS NE EQ VC VS PL MI GE LT GT LE
=12 00010010 100000 Y N Y N Y N Y N Y N Y N Y N Y N
    
```



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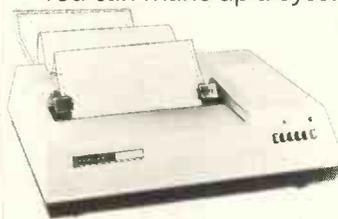
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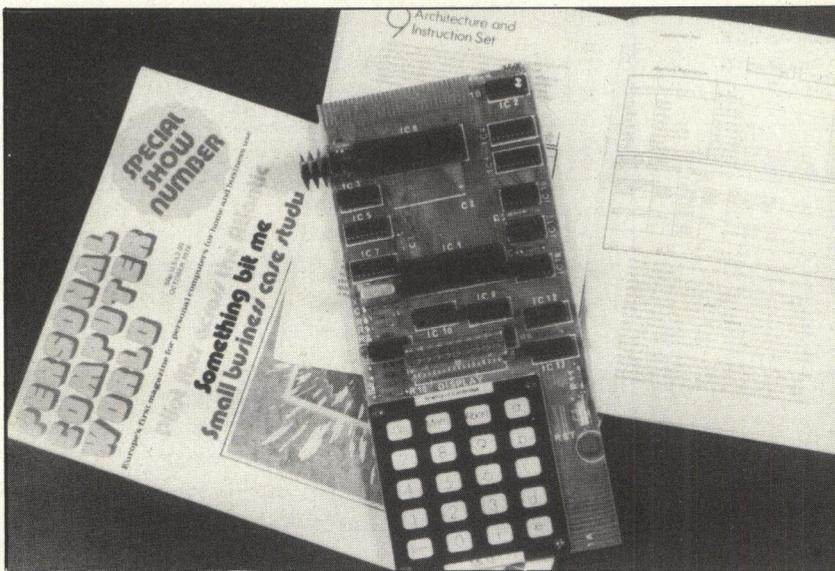
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USING THE MK 14

Clifford Clark



The MK 14 in an appropriate resting place.

The Science of Cambridge MK 14 Microcomputer is an economic and versatile unit which gives "hands on" experience to a wide range of professionals and hobbyists. Its two main weaknesses, the keyboard and the instruction manual, have been highlighted in various technical reviews.

The first weakness, the keyboard, is more or less acknowledged by the manufacturers in as much as they provide an edge connector on the printed circuit board for an external keyboard. Most constructors will have either modified an existing calculator keyboard or made up an assembly with push-button switches.

The second short-coming is of the instruction manual, which jumps from simple memory switching instructions to sample programs laid out in assembler format. There are statements about out-putting to the display with no instructions on how to do it. This presents no problems to those experienced in the 'software' of data processing and are familiar with the jargon and style of layout.

The object of this article and any which, space permitting, may follow, is to help the beginner in his experiments with the MK 14.

The memory map in Figure 1 is for the basic kit. Each block can be viewed as a large page or section of memory with the starting and end address of each shown. Most of the memory is permanently occupied with fixed instructions or data. This is essential for the 'house-keeping' of the system and display. When the computer is first switched on and only the six dashes are visible the 'monitor' program is running to be able to display the dashes. Press the 'GO' button twice and 'Error' is shown. This sensing and action and the other features of control require memory storage space. The accessible part of the memory is the main concern of the user. By writing an appropriate series of instructions (program) the computer is at your service, within its limitations. To start the way into the fascinating realm of computer control it is appropriate to start with display control experiments.

Display Control Program No. 1

This simple program demonstrates the "software" control of the eight, seven segment light emitting diodes (LED's). These diodes form the visual display output of the basic Science of Cambridge MK 14 Microcomputer. From the memory map (Fig. 1) note that the first eight address locations in the display sectors are the outputs to the eight LED's. In other words, the eight LED's are addresses in the memory each having eight connections (seven segments plus decimal point) which are switched on or off depending upon the setting of the bits of the 'byte' addressed to the locations. The relationship between the bit settings and the LED segments are illustrated in Fig. 2.

On running this program all eight sections of the diode assembly will be showing. Stop the program by the 'RESET' button. Address the memory to location "OF1A" and alter the "FF" contents to other settings, as shown in Fig. 2, to become familiar with the bit settings and their effect on the display. So far only one LED unit has been addressed or operated.

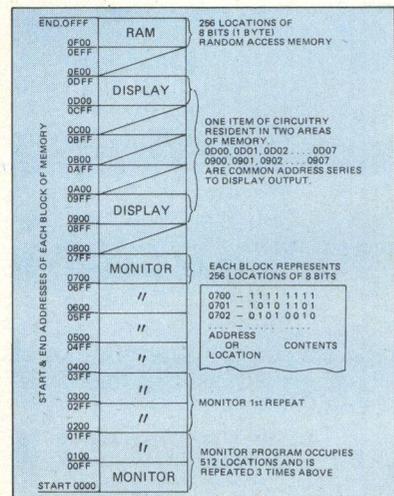


Figure 1. Mark 14 Memory Map Basic Kit

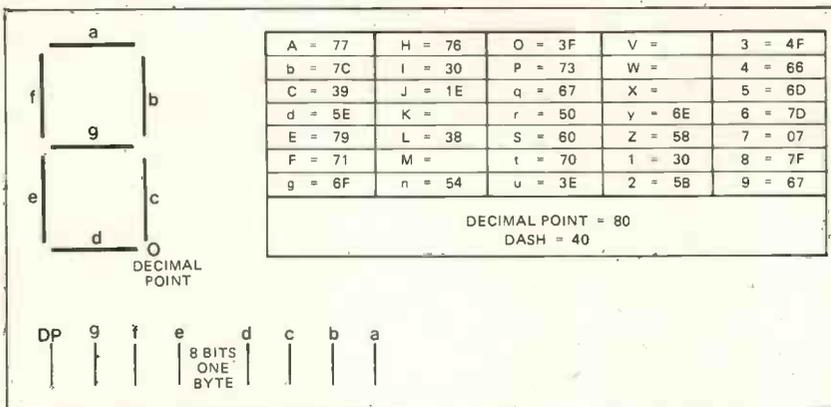


Figure 2.

Now alter the display address "ODO0" to "ODO1", "ODO2", "ODO3" ... and so on up to "ODO7" and notice that the lowest address is on the right and "ODO7" the first operable LED on the left. This addressing arrangement must be borne in mind when sequentially addressing with output text because this is naturally read from left to right.

Having so far controlled the LED's separately, the next step is to output to all eight in the one program. At any instant in time only one specific action is taking place within the computer, so the program is written to cycle through the various switching steps rapidly. Thus the action appears to be frozen and steady. This program cycling action is referred to as the "refreshing" technique as applied to a visual display!

Display Control Program No. 2

This second program to demonstrate the display output uses the auto-indexing feature of the memory address instructions and also uses a counting procedure to check that each LED is addressed before the program repeats or "refreshes".

Program De-bugging Hints

When writing programs of any length it is rarely that they run correctly on the first loading into memory. One has then to go through the various steps of the program to find where the error or errors are located. In computer jargon this procedure is called *debugging*.

It is sometimes possible to get clues as to which section of the program to look into by the output results on first trying to run a newly written program.

At this experimental stage it is useful to *deliberately* introduce errors into Display Control Program No. 2 and to note the effects and thus gain experience in logical debugging.

In this program, address location "OF25" and insert data "C9" (an error in code for auto-indexing). On running the program no incremental

addressing will take place, all the segment signals will be to the one address. Note the difference in illuminating intensity between the various segments, this indicates over-writing of the program instructions into the one location.

Re-insert the correct data at "OF25" and now assume an incorrect

count set up at location "OF20". Insert data "07" in place of "08" and run the program. Note that one of the LED units is *not* being illuminated. This indicates that the program is looping back *too soon* and therefore missing the final display address.

These two examples demonstrate the importance of having an overall view of both the "hardware" (electronic circuitry especially the memory map) and the "software" (the program instructions and what they are supposed to be doing) arrangements to be able to save time in program debugging.

PCW We advise readers who are interested in obtaining MK 14s to first write and obtain a firm undertaking on a delivery date for this outstandingly good value-for-money kit. Readers should also understand that the MK 14 is an introductory kit, most useful for hobbyists and engineers. When in doubt, join the Amateur Computer Club! PCW

DISPLAY CONTROL PROGRAM #1.		
MEM.ADD.	CONTENTS.	ACTION & RESULTS
OF12	02	CLEAR CARRY LINK FLAG.
OF13	C4	LOAD DATA "0D"
OF14	0D	INTO ACCUMULATOR.
OF15	35	TRANSFER "0D" TO POINTER REGISTER #1 HI BYTE.
OF16	C4	LOAD DATA "00"
OF17	00	INTO ACCUMULATOR.
OF18	31	TRANSFER "00" TO POINTER REGISTER #1 LO BYTE.
OF19	C4	LOAD "FF" INTO
OF1A	FF	ACCUMULATOR(AC).
OF1B	C9	STORE "FF" FROM AC INTO ADDRESS
OF1C	00	CONTAINED IN POINTER REGISTER #1.
OF1D	90	JUMP BACK TO START OF PROGRAM AT OF12
OF1E	F4	AND REPEAT UNTIL STOPPED BY "RESET".

DISPLAY CONTROL PROGRAM #2.		
MEM.ADD.	CONTENTS.	ACTION & RESULTS.
OF12	02	CLEAR CARRY LINK FLAG
OF13	C4	OF13 - OF18 STORES DISPLAY STARTING
OF14	09	ADDRESS "0900" INTO POINTER
OF15	35	REGISTER #1.
OF16	C4	
OF17	00	
OF18	31	
OF19	C4	OF19 - OF1E STORES TEXT STARTING
OF1A	0F	ADDRESS "0F60" INTO POINTER
OF1B	36	REGISTER #2.
OF1C	C4	
OF1D	60	
OF1E	32	
OF1F	C4	LOAD COUNT
OF20	08	#8 INTO AC.
OF21	C8	STORE #8 AT
OF22	1E	ADDRESS "0F40".
OF23	C6	LOAD CONTENTS OF POINTER REGISTER #2 INTO AC
OF24	01	AND ADD ONE TO POINTER #2 CONTENTS.
OF25	CD	LOAD CONTENTS OF AC INTO ADDRESS GIVEN BY
OF26	01	POINTER REGISTER #1 AND ADD ONE TO POINTER #1
OF27	B8	DECREMENT NUMBER STORED AT "0F40". RESULT
OF28	B8	INTO AC AND ALSO BACK INTO LOCATION "0F40".
OF29	98	IF AC=0 JUMP TO START
OF2A	E8	OF PROGRAM(OF12).
OF2B	90	JUMP TO "OF22". (COUNTDOWN NOT FINISHED SO
OF2C	F6	REPEAT UNTIL ALL EIGHT LED'S ADDRESSED).
OF40	'XX	LOCATION USED FOR STORING COUNT"#".
OF60	6E	Y
OF61	50	R
OF62	70	T
OF63	40	-
OF64	5E	D
OF65	5C	O
OF66	5C	O
OF67	6F	G

TURNING THE TABLES

L. R. Carter

An application for a programmable calculator that keeps the kids out of your hair and off your machine can't be bad. The application described below tests the user *randomly* on his knowledge of any given times table. If the answer is correct the test continues; if the answer is wrong the calculator gets angry and flashes the correct answer at you.

(Technical note: Some calculators are not angry flashers, there are calculators who more politely point out an error by displaying the letter E. The coding below is for a TI 57, a well known flasher - I think it runs in the family).

The program flow chart is shown in figure 1. Before running the prog-

ram a number less than one is entered into store 0 to be used as the initial seed for the random number routine. The value of the 'times table' to be practised is entered into store 2. Starting the run causes the calculator to go to the subroutine and generate an integer random number between 1 and 12, revise the seed in store 0 and to store the random number in store 1. The correct answer is then calculated and stored in 7. The random number is now displayed for practise.

When the supposed answer is entered it is compared to the correct answer in store 7. If the answers correspond the program loops to generate another number between 1 and 12 and the practise continues. If the supplied answer is wrong the correct answer is displayed, then an error condition is deliberately induced to start the flashing.

The error condition is cancelled by using the CLR key and the practise continued by keying RUN. Changing the multiplier in store 2 allows the practise to continue on another table.

The key entry sequence for the program follows.

The keying sequence.

(; is simply used as a separator, to save space).

```
LBL 1; SBR 2; RCL 1; x; RCL 2; =; STO 7;
RCL 1; R/S; x=t; GTO 1; RCL 7; GTO 6;
RST; LBL 2; π; +; RCL 0; =; γx; 8; -;
INT; =; STO 0; x; 12; +; =; INT; STO 1;
INV SBR
```

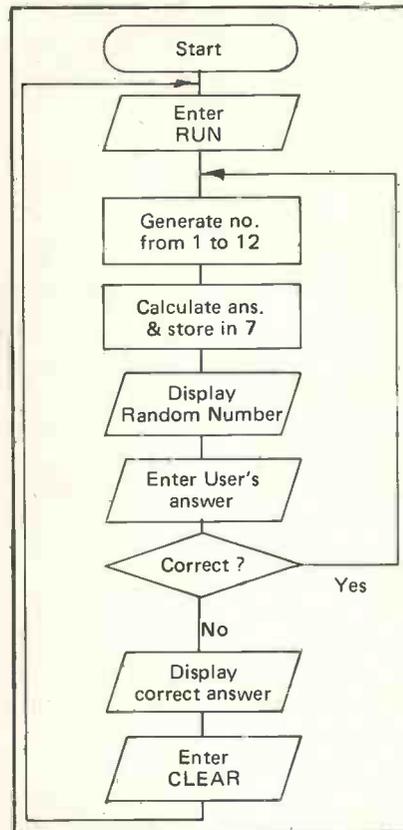


Figure 1. Times Table flow chart



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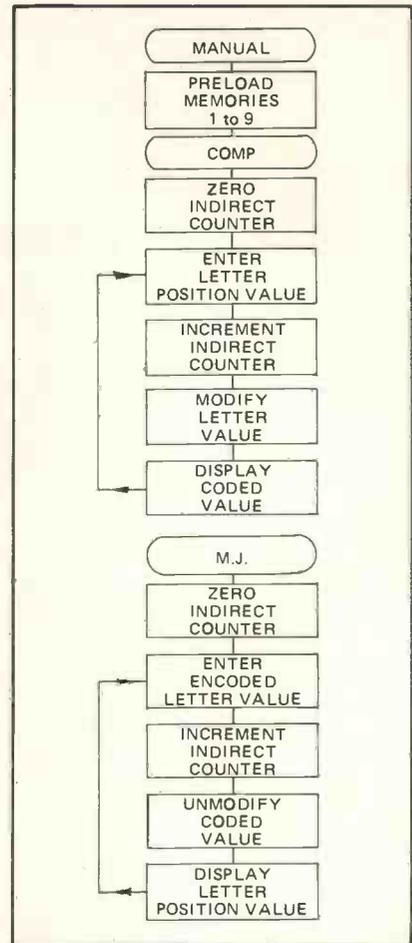
Decode

Manual Jump puts the user in this mode.
 Enter the received encoded values at ENT 0
 ANS 0 is the alphabetical position of the decoded letter ie 1=A, 2=B etc.

Program

```

I=K0:
ST#0; ENT0:
I=I+K1:
O=O+IM:
ANS0: GOTO#C:
MJ
I=K0:
ST#1: ENT0:
I=I+K1:
O=O+IM:
ANS0:GOTO#1:
    
```



Encode - decode flowchart

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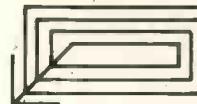
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UNRAVELLING

The PET IEEE-488 Bus

Dr. C. Preece

University of Durham, Department of Engineering Science



The Commodore PET 2001 computer is provided with a bus connector for peripheral equipment. The bus is designed to conform to the IEEE-488 standard digital interface for programmable instrumentation (1). What Commodore have done is to implement a sub-set of the possible IEEE-488 facilities which are directly programmable from BASIC. Nevertheless comparatively sophisticated interfaces can be designed to operate with the commands available. A brief and somewhat incomplete description of the IEEE-48 bus is given in the PET User's Handbook (2). In particular the information on what signals are actually produced by the PET when each BASIC instruction is executed is at best vague, and in some cases misleading. The purpose of this article is to present this information in a usable form.

The Bus Groups

The parallel lines of the IEEE-488 bus can be divided into three groups. The first group of eight lines form the data bus. An eight bit word is placed on the data bus by connecting the individual lines to earth (true) or disconnecting them, when they float to 5 volts (false). The second group of five lines form the management bus. Only two of the five lines are fully implemented on the PET. These lines define the type of information sent. The first line, ATN (attention), is true when an interface control word is being transmitted on the data bus, and is false when a data word is transmitted. The second line, EOI (end or identify), is normally false, but is set to true when the last data word of a message is being transmitted. It can therefore be used as an end-of-message indicator. The third group of three lines forms the transfer bus. Signals on this bus control the handshake sequence between devices on the IEEE-488 bus. The handshake sequence ensures successful word transmission.

Word Transmission

Each eight bit word, whether it be an interface command word or a data word, is transmitted along the IEEE-488 bus by the same handshake sequence. This means that the sending device waits for acknowledgement from the receiving device at each stage of the transmission process. If there are more than two devices connected to the bus the handshake sequence ensures that all devices have sent their acknowledgement signals before the next stage of the transmission process proceeds.

The three lines of the transfer bus control all stages of transmission. A typical timing sequence for the transmission of one word is shown in Figure 1. The lines are normally held false (5 volts), but any device can set a line to true by applying an earth to it. Only when all devices have removed their earths does a line revert to the false state.

Transmission commences when all devices set NRFD to false which means that they are all ready for data. (Point A, Fig. 1). The transmitting device, designated the talker, places the data on the eight lines of the data bus, (Point B), and then sets DAV true (Point C). Each listening device holds the NDAC line true until it has read the data word. Only when all devices have removed their true (earth) signals from this line will NDAC go false. (Point D). Once NDAC goes false the talker sets DAV false (Point E) and removes the data

from the data bus. The listening devices, once DAV goes false, set NDAC to true again for the next cycle of transmission, and when they are ready to receive the next data word they set NRFD to false (Point F).

Each peripheral device connected to the IEEE-488 bus must have an interface which is capable of providing this sequence of handshake signals for transmission to be accomplished successfully.

Interface Control Words

Before communication can be established with a peripheral device, that device must be 'opened'. The OPEN command in BASIC assigns a logical device address (i.e. the number used in the BASIC PRINT statement) to the physical device address. The physical device address is a number which is transmitted along the IEEE-488 bus by the interface control word.

As each appropriate BASIC command is executed, interface control words and data words are transmitted by the PET to the bus. The sequence and format of these words is determined by the type of OPEN command used. There are three variants of this command and the resulting transmission formats are illustrated by examples in tables I, II and III.

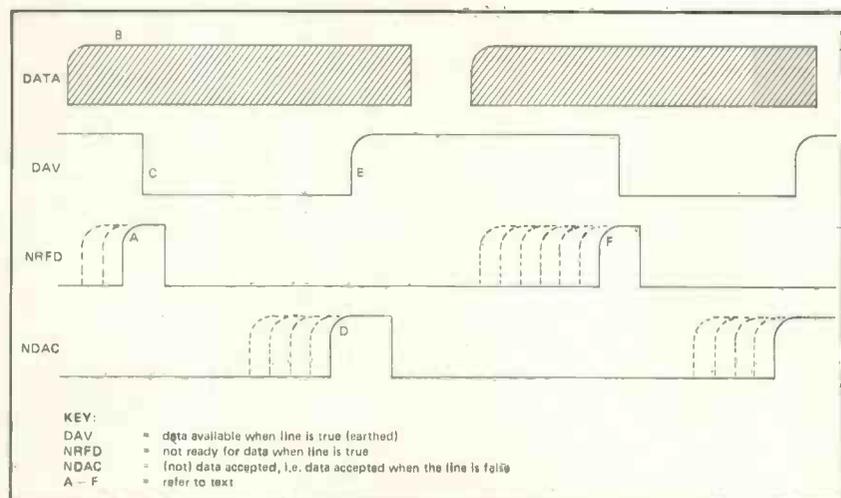


Figure 1. Transfer bus-handshake sequence waveforms

BASIC	ATN	EOI	DATA WORD		CHARACTER	NOTES		
			octal	binary				
OPEN4,6						nothing transmitted		
PRINT #4,"ABC"	1	0	46	00100110	(LAG)	listen address group (device no. 6) } ascii characters		
	0	0	101	01000001	A			
	0	0	102	01000010	B			
	0	0	103	01000011	C			
	0	0	15	00001101	cr			
	0	1	12	00001010	If			
	1	0	77	00111111	(UNL)		unlisten	
INPUT #4,A\$	1	0	106	01000110	(TAG)	talk address group *** input accepted here ***		
	1	0	137	01011111	(UNT)		untalk	
GET #4,A\$	1	0	106	01000110	(TAG)	talk address group *** input accepted here ***		
	1	0	137	01011111	(UNT)		untalk	
CMD4	1	0	46	00100110	(LAG)	listen address group		
	0	0	15	00001101	cr			
	0	0	12	00001010	If			
	0	0	15	00001101	cr			
	0	0	12	00001010	If			
	0	0	122	01010010	R			
	0	0	105	01000101	E			
	0	0	101	01000001	A			
	0	0	104	01000100	D			
	0	0	131	01011001	Y			
	0	0	56	00101110	.			
	0	0	15	00001101	cr			
	LIST	0	0	12	00001010		If	} program text listed here
		0	0	15	00001101		cr	
0		0	12	00001010	If			
CLOSE4	0	0	15	00001101	cr	} program text listed here		
	0	0	12	00001010	If			
	0	0	122	01010010	R			
	0	0	105	01000101	E			
	0	0	101	01000001	A			
	0	0	104	01000100	D			
	0	0	131	01011001	Y			
	0	0	56	00101110	.			
	0	0	15	00001101	cr			
	CLOSE4							nothing transmitted

Table I Output to IEEE-488 bus opened by Physical Device Address only.

The CLOSE command disassociates the logical address from the device address and allows re-assignment of both. It should be noted that only in table III does the OPEN command itself actually transmit interface control words and data words to the bus. In the other cases it merely sets the PET software so that the other commands such as PRINT are transmitted in the correct format.

For the purposes of the examples in the tables, the following assumptions are made.

Logical Device Address	=	4
Physical Device Address	=	6
Secondary Device Address	=	3
Filename	=	F1

It can be seen from the tables, that the data words are transmitted between interface control words. The interface words contain the device numbers and the secondary addresses. They have formats which are specified in the IEEE-488 Standard (1), and these are given in table IV in the forms that apply to the PET. The SCG (secondary command group) words are further modified when used by the CLOSE command or when a file name has been specified.

If a secondary address is used then the SCG format for the CLOSE statement is	
1110SSSS	(see table II)
If a file name is specified then the SCG format for the OPEN command is	
1111SSSS	(see table III)

Whenever data is transmitted to the bus the EOI line is set to true during the transmission of the last data word. This can be seen in the examples of the PRINT statement and also in the transmission of the file name in table III.

The variations in the formats enable the interface designer to distinguish between the different stages of transmission and to construct the interface circuit to respond accordingly.

When the CMD instruction is used, all list output is directed to the specified logical address. Subsequent use of the LIST command will not produce any further interface command words, nor will it actuate EOI. Only when the logical device is closed, or when the CLR command is used will a line feed character be sent together with a true EOI to signify the end of message.

Interfacing to the bus

If the PET IEEE-488 bus is to be used with only one peripheral connected to it, say a printer, then the printer interface can be designed to ignore all the interface control words, and simply accept the data words. This is achieved by the interface only

BASIC	ATN	EOI	DATA WORD		CHARACTER	NOTES		
			octal	binary				
OPEN4,6,3						nothing transmitted		
PRINT #4,"ABC"	1	0	46	00100110	(LAG)	listen address group (device no. 6) } ascii characters		
	1	0	143	01100011	(SCG)		secondary command group (sec. addr. 3)	
	0	0	101	01000001	A			
	0	0	102	01000010	B			
	0	0	103	01000011	C			
	0	0	15	00001101	cr			
	0	1	12	00001010	If			
INPUT #4,A\$	1	0	106	01000110	(TAG)	talk address group secondary command group *** input accepted here ***		
	1	0	143	01100011	(SCG)			
GET #4,A\$	1	0	106	01000110	(TAG)	talk address group secondary command group *** input accepted here ***		
	1	0	143	01100011	(SCG)			
CMD4	1	0	46	00100110	(LAG)	listen address group secondary command group		
	1	0	143	01100011	(SCG)			
	0	0	15	00001101	cr			
	0	0	12	00001010	If			
	0	0	15	00001101	cr			
	0	0	12	00001010	If			
	0	0	122	01010010	R			
	0	0	105	01000101	E			
	0	0	101	01000001	A			
	0	0	104	01000100	D			
	0	0	131	01011001	Y			
	0	0	56	00101110	.			
	0	0	15	00001101	cr			
	LIST	0	0	12	00001010		If	} program listed here
0		0	15	00001101	cr			
0		0	12	00001010	If			
CLOSE4	0	0	15	00001101	cr	} program listed here		
	0	0	12	00001010	If			
	0	0	122	01010010	R			
	0	0	105	01000101	E			
	0	0	101	01000001	A			
	0	0	104	01000100	D			
	0	0	131	01011001	Y			
	0	0	56	00101110	.			
	0	0	15	00001101	cr			
	CLOSE4	1	0	46	00100110		(LAG)	listen address group secondary command group with bit 8 set.
		1	0	343	11100011		(SCG)	

Table II Output to IEEE-488 bus opened by Physical Device Address and Secondary Address.

accepting input when the ATN line is false. However if other devices are to be connected in parallel then the circuitry of each interface must decode the interface control words and detect the appropriate address before becoming active. For most purposes unique device addresses would seem to be an adequate means of identification, and if this is the case the commands of table I would apply. However, if something like a disc controller is to be attached, then the commands in table III, which specify a filename may need to be used.

Interfacing with other computers is most easily done by implementing the handshake sequence in software on the second machine. A general purpose parallel I/O port such as a peripheral interface adaptor (PIA) will suffice. It was via such an interface that the information in this article was discovered.

References

1. IEEE Standard Digital Interface for Programmable Instrumentation. IEEE Std. 488-1975-ANSI MC 1.1-1975. pub. IEEE Inc. New York.
2. Commodore PET computer Users Handbook. Commodore Systems Div. Euston Road, London.

BASIC	ATN	EOI	DATA WORD		CHARACTER	NOTES
			octal	binary		
OPEN4,6,3,"F1"	1	0	46	00100110	(LAG)	listen address group (device no. 6) sec. command gp. with bits 8 & 5 set (sec. addr. 3)
	T	0	363	11110011	(SCG)	
	0	0	106	01000110	F	} filename in ascii characters
	0	1	61	00110001	T	
	1	0	77	00111111	(UNL)	unlisten
PRINT #4,"ABC"						as table II
INPUT #4,A\$						as table II
GET #4,A\$						as table II
CMD4						as table II
LIST						as table II
CLOSE4						as table II

Table III Output to IEEE-488 bus opened by Physical Device Address, Secondary Address and Filename.

Binary word format	IEEE mnemonic	IEEE description
0100AAAA	(TAG)	talk address group
0010AAAA	(LAG)	listen address group
01011111	(UNT)	untalk
00111111	(UNL)	unlisten
0110SSSS	(SCG)	secondary command group
Key:	AAAA =	binary physical device address in range 4 - 15
	SSSS =	binary secondary address in range 0 - 15

Table IV Format of Interface Control Words applicable to the PET

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Graham Trott

The Motorola 6809 16-bit MPU

At their MICROFORUM at the IEE, Savoy Place in June 1978, Motorola gave details of, among other items, the forthcoming MC6809. At about the same time, technical information was also made available from which I have gleaned the following about this new addition to the M6800 family.

The 6809 is (or will be) an 8-bit microprocessor as far as the outside world is concerned. Internally, however, most of its operations concern manipulation of 16-bit data, and a high proportion of its instructions generate a double-byte opcode, so it appears to sit on the fence, midway between the 8 and 16-bit arguments. Motorola argue that since the 6809 is aimed at applications involving editors, word processors, assemblers and HLL (High Level Language) compilers, much of its data will come eight bits at a time, so the advantages of a full 16-bit machine in superior computational speed will be offset by the penalty of inefficient memory usage.

Preserving Compatibility

As have Intel with their 8086, Motorola have tried to preserve as much compatibility as possible with their previous products, while attempting to cram as much as they can into the new baby. The result is a machine with hardware characteristics practically identical to those of the MC6802 (any difference being additions that may be ignored rather than changes that may not), but, owing to the considerable improvements, with only partial software compatibility. The assembler mnemonics of the 6800 are all there, with a few exceptions that can be implemented by other means, but not all of the machine codes are the same; and some of those that are, operate differently.

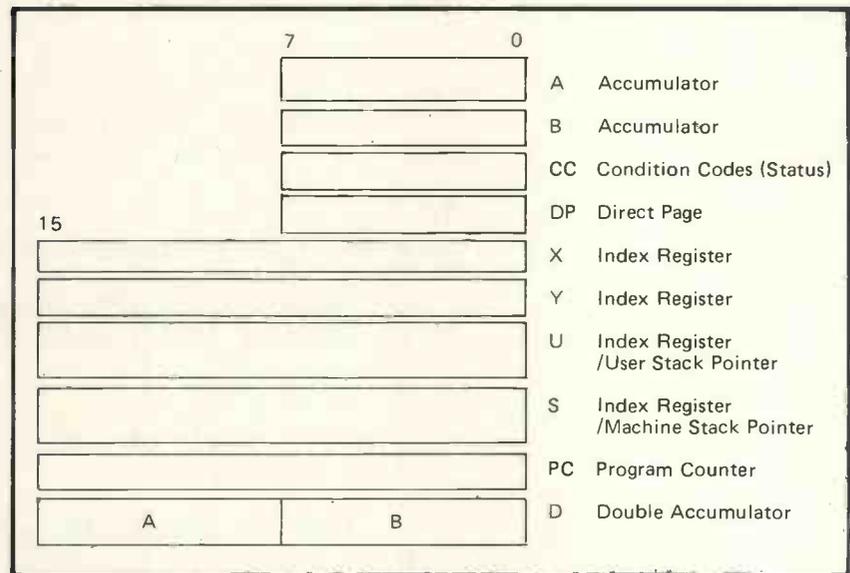
The reason for these differences lies primarily in the addition of two extra 16-bit registers, together with a host of new software features to use both them and the old ones. As well as the 6800 Index Register and Stack Pointer are the Y and U pointer registers, and there are instructions that concatenate the A and B accumulators to form a D (Double) accumulator. A glance at the programming model will help to explain:—

Programmer's Lib

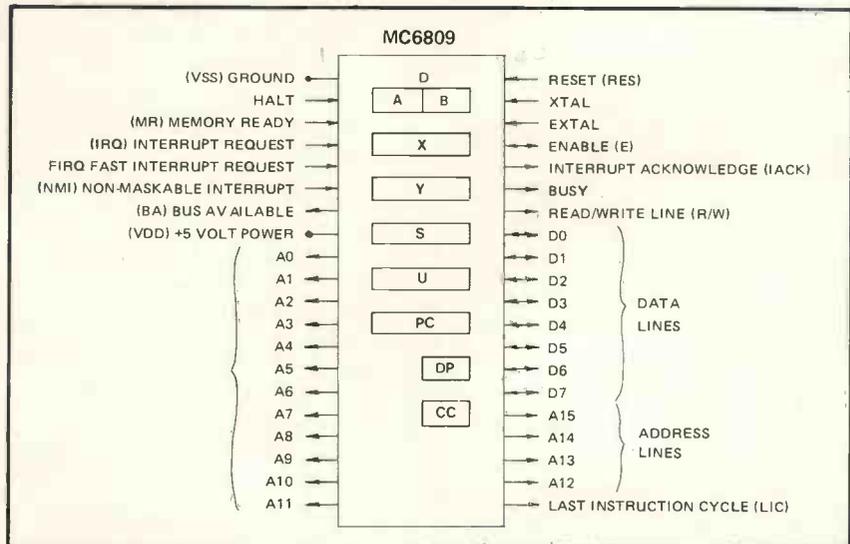
The main difference between the 6800/6802 and the 6809 in programming terms lies in the use of the 16-bit pointer registers X, Y, U and S. The 6800 allows indexed operations using X or stack pushes and pulls using S, whereas the 6809 allows the programmer virtually complete freedom in the use of the pointer registers. They may all be used as index registers or as stack pointers at any time, although only U and S have explicit push and pull mnemonics relating to them. In the indexed addressing mode, there are a total of 16 different ways of using the pointer registers, for EACH register and for ANY instruction where indexed addressing is appropriate. Indirect addressing, via the pointer registers, is also possible, signified in the examples below by square brackets. This means that the pointer register doesn't actually contain the address at which to load or store or whatever, but instead points to a location in memory containing that address (just sit and think about it for a while).

The following examples show some of the possible instructions that might result from the use of Indexed

ressing mode, there are a total of 16 different ways of using the pointer registers, for EACH register and for ANY instruction where indexed addressing is appropriate. Indirect addressing, via the pointer registers, is also possible, signified in the examples below by square brackets. This means that the pointer register doesn't actually contain the address at which to load or store or whatever, but instead points to a location in memory containing that address (just sit and think about it for a while).



MC6809 Programming Model



The MPU.

addressing. The total number of different indexed instructions is well over a thousand, so this is just a sample:—

LDA O,X	Load Accumulator A from address pointed to by X. (2 bytes)
STB [B,X]	Store Accumulator B indirectly via X. (2 bytes)
CMPA ,Y+	Compare A with the byte pointed to by Y, then increment Y. (2 bytes)
ADDD ,Y++	Add to D the two bytes pointed to by Y, then increment Y twice. (2 bytes)
LEAY [,S++]	Pull two bytes from the S stack. Use these bytes as a pointer to the data to load into Y. (2 bytes)
ROL ,—X	Decrement X then rotate left through carry the byte pointed to by X. (2 bytes)
STY ,—U	Decrement U twice and store Y at the address U then points to (equivalent to PSHU Y, indicating that any of the pointer registers may be used as stack pointers. (2 bytes)
LDD [,—Y]	Decrement Y twice, then load D indirectly via the result. (2 bytes)
LEAX N,X	Add N to X, where N is signed and may be 5, 8 or 16 bits. The source and destination may each be any one of the pointer registers. This demonstrates the power of the LEA (Load Effective Address) instruction. (2, 3 or 4 bytes)
ADCA [N, Y]	Add to Accumulator A with carry indirectly via Y+N. N may be up to 16 bits as before. (2, 3 or 4 bytes)
CMPD A,U	Compare D with the data pointed to by the sum of U and Accumulator A. (2 bytes)

There are five more types of indexed addressing similar to the last, using A, B or D as an offset (three of them indirect).

Are you still there?

Anybody still with me will realise that indexed addressing, as exemplified above, makes the 6809 enormously powerful in its ability to access memory and to modify register contents, but hold on—I haven't finished yet! If there is one feature of the 6809 that makes it stand out from other 8-bit machines (and many 16-bit ones), it is its ability to run position-independent code.

Consider the position of a writer of a ROM-based HLL interpreter or compiler; how can he decide where it should be located in the memory maps of 1001 different systems? In the case of the 6809, the answer is "Who cares?", since programs can easily be written that will run any-

where. To do this are needed two things; firstly, relative control transfers (branches, to 6800 users) of up to 16 bits (signed) and secondly, program counter relative access to data tables within the program. To enable the former a complete set of 16-bit Branch instructions are provided in addition to the 8-bit ones, and the latter is achieved by extending relative addressing to memory access instructions. A typical instruction might be:—

```
LEAX DATA,PCR
```

This means "Load X with the address given by that of DATA relative to the current position of the Program Counter". In practice, the assembler would translate the offset into a number N, and the instruction would assemble as though it had been written:—

```
LEAX N,PC
```

meaning "Add N to PC and load X with the result". N may be 8 or 16 bits (signed), resulting in a 3 or 4 byte instruction respectively. An indirect mode is also available (Relative Indirect).

There is plenty more I could write about the new features of the 6809, but let's leave it at that for now. What most people will be interested in is how it compares with other

microprocessors. Comparisons are difficult to make since so much depends on the programming examples used, but Motorola state that using benchmark programs proposed by their rivals (a neat touch), the 6809 performs at better than twice the speed of the Z-80 or the 6800 (with the same memory access time) and uses 50% fewer instructions occupying 30% (Z-80) to 50% (6800) less bytes.

All this would be good news if the 6809 were actually available now, but the \$64,000 question is "When can I get hold of one?" Present indications are that samples should be forthcoming in the first quarter of 1979, so you'll have to bite your nails 'till then. From what I have heard, there is a lot of activity in the production of software for the new machine — I gather that FORTRAN, COBOL, BASIC and PASCAL compilers may well all be available in ROM at about the same time as the device itself, so it certainly seems that someone is taking the 6809 seriously.

To conclude, the 6809 represents another leap forward in 8-bit processing and should bring the power of a small minicomputer to even the most cost-conscious amateur, as well as ensuring effective and efficient software generation by major users.

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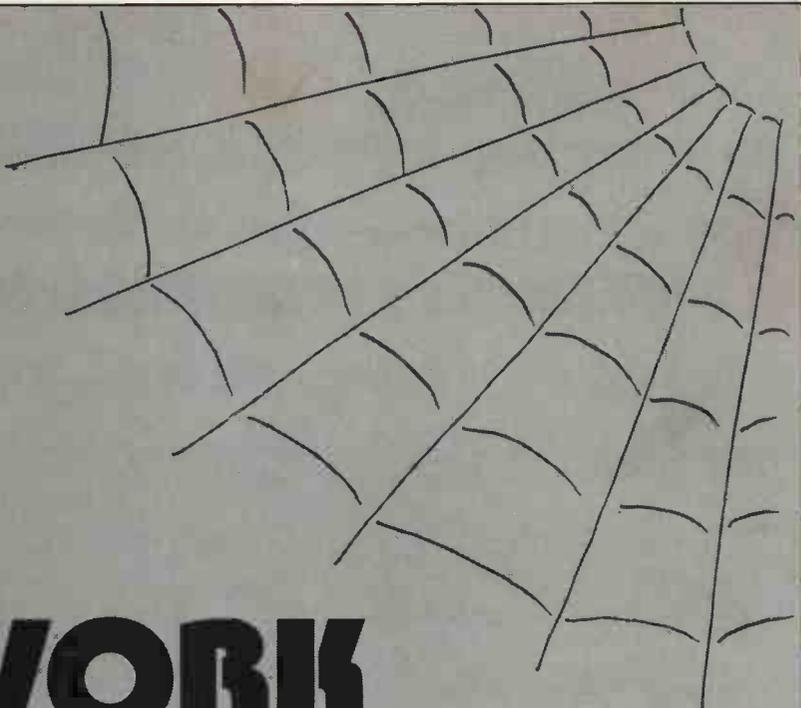
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NETWORK

L. K. Darnton

Microprocessors are now entering our personal lives from many directions. They probably constitute the greatest single technological development since invention of the internal combustion engine and will catalyse an even greater restructuring of human social interaction, for better or for worse.

Of the rapidly increasing number of microcomputer users, a large percentage regard themselves as non-professional and relatively inexperienced in the field of computing generally. However, professionalism is not defined by the associations with which one is affiliated, but rather by a set of ethical and behavioural codes according to which one carries out work activities.

From this viewpoint, many microcomputer enthusiasts are potentially highly professional in attitude and practical application of their skills, however limited.

The foundation of a national association for the education of computer science fundamentals to 'amateur enthusiasts' and for the creation of standards in microcomputer hardware, software and data processing procedures could (i) expedite the abolition of "mystery" which has over the years become synonymous

with "computers" and (ii) tap a vast reserve of dormant knowledge and enthusiastic creative experimentation, thereby enabling each member to contribute towards the development of a national public computer communications network on the same scale as our present voice grade telephone networks.

Pooling resources

Systems such as Viewdata, Ceefax, Oracle, etc., indicate the possibility of a multi-national domestic computing network. Microprocessor manufacturers currently offer a wide range of cheap, powerful computing resources to amateur, domestic, small business and process control users. Compared with our experience with large mainframes, microsystems are very primitive. But progress is accelerating in developing large, cheap semiconductor memories enabling low power and very high speeds, higher quality acoustic couplers, portable modems and a spectrum of plug-in accessories including graphics packages and voice recognition/simulation modules. Urgent attention to software is required, for this is where micros so obviously lag behind their ancestral mainframes.

When the present labyrinth of micro sales promotions has been

thoroughly debugged, some true industry standard may emerge, giving birth to the standard elements for the design of a fully integrated national, continental or even global artificial intelligence network.

Design of industry standards requires the specification of certain parameters, determined by the requirements of potential systems users. 'Presently, few people have any idea of where micros are taking us; there are few, if any, useful guidelines and it seems we have a product which needs a purpose. This is not quite so; the limits of human creativity are defined largely by a set of fixed ideas about what is and is not possible. A brief glimpse through science-fiction of the fifties and space exploration of the seventies will bear out my point. What we actually have in microprocessors is a product of today's technology awaiting tomorrow's conceptual reorientation. As the global use of microcomputers is as inevitable as the pre-requisite conceptual reorientation, what better time than now to throw out some new ideas and banish a number of obsolete systems we continue to use through shortsightedness about present conditions and future requirements?

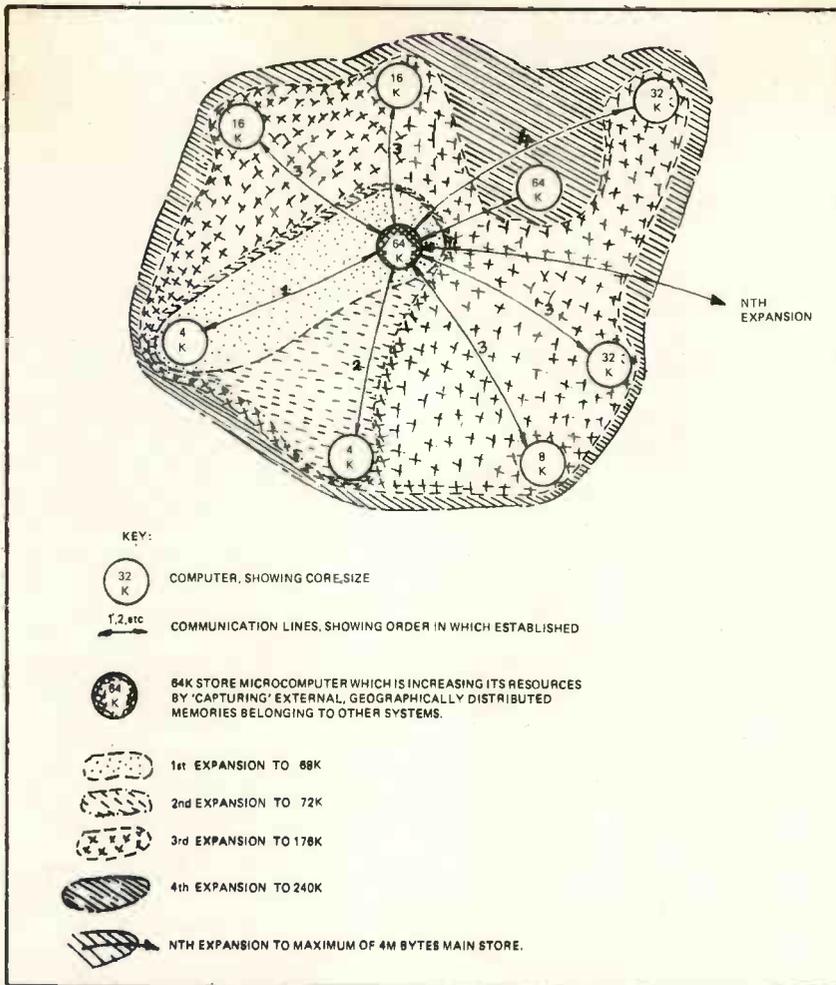


Fig. 1. Geographically Distributed Machine of Variable Size:

BASIC CONCEPTS

My original concept of a multinational computer network involved the interconnection of several computer installations in such a way that two or more computers geographically distributed could operate as a single geographically distributed machine. (See Fig. 1).

I took the viewpoint that a microcomputer is a machine whose component circuit boards are spatially distributed throughout a volume of space measuring some units of cubic feet. I then shifted my viewpoint and realized that given the ideal communications medium, the circuit boards could be located several miles apart. The now geographically distributed components would still constitute a single microcomputer. Returning to our living room micro, the addition and removal of memory boards and other accessories effectively constitutes a machine of variable size, assuming all modules to be plug compatible.

In fact, any computer is actually a machine of variable size, in that at different moments in time, different amounts of memory are being utilized according to resource requirements. The unused memory and peripherals are lying dormant and currently invisible to the system. Prog-

rams will run O.K. until system resources are exceeded and then it would be useful to be able to hook in additional resources automatically. The greatest problem lies in needing additional resources for a short period of time, too infrequently to warrant the purchase of expensive hardware and/or software.

My proposed network would enable a micro user to hook up with other machines down the line in such a way that he addresses those machines as if they were simply subsystems of his own system. From the viewpoint of a user looking into the network, it would appear as a single machine of variable size, whose resources would lie somewhere between that of his personal computer and the total network resources, depending upon his requirements and network conditions at any point in time.

This appearance of total control over vast computing resources would apply equally to large mainframe installations and domestic computer systems because the definitive boundaries between systems would no longer be geographical but conceptual and functional.

My original concept included a description of a parallel network of system controllers whose function would be to monitor user-network conditions, implement security

measures and ensure that no disruptions occur at any point in the network. Such system controllers, being supervisory and administrative in function, would remain completely transparent to all users and is too complex a subject to enter into here. For this article I will take the viewpoint that we are situated in a living room, using our minimum-configuration microcomputer and having purchased the additional hardware we need to hook into an already existing network. Later, I will expand on some ideas about practical experimentation which ought to be possible using today's primitive telephone network. This could be a starting point for 'amateurs' to initiate some solid research and thereby contribute towards a realistic network design. It could be through such research that we may pinpoint future potential and requirements leading to the evolution of standards and the guidance of manufacturers towards production of items we need in quantity.

Practical advantages of a distributed centralization network

A network is a system of communication lines linking two or more computers, each of which remains a separate, independent entity. The computers may communicate, but they effectively remain limited according to the resources available at the individual installations; and incompatibility between machines handicaps free interaction. Centralized systems involve a number of terminals, remote job entry stations, etc., connected to a central computer installation. Centralization may in many cases improve efficiency and reduce operating costs but there are important trade-offs such as:— if the central computer goes 'down' all dependent terminals become inoperable; although security procedures are implemented, certain conditions may give rise to loss and/or corruption of users' data/programs which may be difficult or impossible to recover; communication is often slow, especially when the system is heavily used and can entail costly overheads.

When a system is about to go down, there is normally sufficient time to dump current users' programs on to backing storage such as magnetic disc for later recovery. Higher speed communications lines could enable the copying of vital data/programs by other network computers which, in a Distributed Centralization network, could reconfigure themselves so as to duplicate the original machine and thus continue processing without loss of time or information. The use of low power devices would enable micros to be permanently hardwired into the network and maintained in

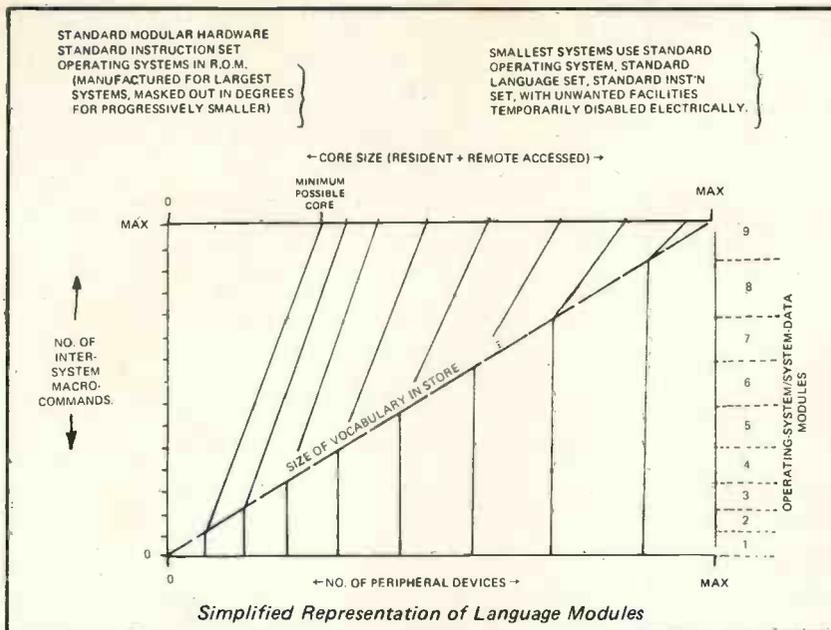


Fig. 2. Universal Computing Language:

'standby' mode, powered by D.C. line voltage, at no additional cost to the user. Thus the total amount of computer resources lying idle for 8 - 16 hours per day while their owners are asleep or at work could be used by other systems when required.

Thus, any user who wishes to burn the midnight oil would have at his disposal a computing machine of vast potential. I have considered the problems of debiting and crediting accounts of users who utilise and donate resources from/to the network; again, this alone is a vast area which need not come under discussion here.

A modular architecture upon which all computers and network elements would be built, would ensure 'super-mass production' of basic hardware units, reducing prices to a level enabling most people to purchase a minimum system, but gain access to vast resources. One critic told me that manufacturers would reject my ideas because a point would be reached at market saturation when sales would fall; I doubt this very much because the passage of time would be accompanied by changes in system requirements and a modular system architecture would enable modifications to be implemented rapidly and fairly cheaply.

Hardware and Software requirements
Complete standardization, compatibility and portability of both hardware and software would have to be implemented throughout the network. Anyone involved in networking will understand the difficulties inherent in getting two incompatible machines to 'talk' with each other.

Assembly languages are the nearest most of us will ever get to true machine language. They are machine dependent; thus an assembly lan-

guage program written for one machine will usually not run on a different family of machine.

Even with high level languages we encounter difficulties. Some compilers recognise only a subset of a particular high level language. Different computers sometimes use different character codes, so high level source programs may require modification before they can be transported between machines. Object programs generated by a high level compiler are not always portable because of the several ways different machines store data. A great deal of research and development is going on in the field of language translators, cross compilers, etc., but this is slow and very expensive. Basically we are trying to apply a costly corrective technology to an obsolete system.

Although high level languages are relatively portable, they are very much application oriented, which is why we have so many such languages. What is badly needed is a 'universal computer language'.

The universal computing language would be vast by any standards. It would constitute a 'super set' containing all sets of all language modules required by all types of computer and application. Impractical by today's standards, but future production of cheap ROM's may enable the mass production of standard universal compilers. Language structure would be a hierarchy, with 'super-macro commands' at the top through to machine language instructions at the bottom. An 'unmasking' procedure would 'enable' the use of whichever language modules are able to run on a particular machine. (See Fig. 2).

All circuit boards would contain a tiny ROM holding details about the board's components and function. (See 'ROM-Z' in Fig. 3). A 'system

interrogator' module would, on power up, scan all the circuit identity ROM's and file a report to the system supervisor, which would then initiate the unmasking procedure to enable use of language modules; the supervisor would ensure that all irrelevant modules remain masked. When two or more machines interconnect to operate as a single geographically distributed machine, further language modules would be temporarily unmasked. The more machines connect together, correspondingly higher levels of macro-commands become unmasked. (See Fig. 2). A new addition to system software is the concept of 'system data' and the related term 'macro-data'. In human terms, the word 'television' is a macro-data word. To a TV engineer, that one word is sufficient to gain access to his total knowledge about TV sets. It is in effect a file-name. Macro-data vocabulary could be mass produced in ROM form and unmasked according to system configuration, synchronised with unmasking of the compiler.

Communications would be via 'wide-band differential gates' instead of the obsolete modem. The gate would be imposed between CPU and all other sub-systems. (See Figs. 3/4). To a micro not using the network, the gate would be transparent. It would have an address which would be regarded as the base address of the installation's address range. To the CPU, its own gate would be address zero. (See Fig. 4). All memory locations would be relative to this address. To other network users, the gate would have a network address and to access locations in memory, they would first transmit the network address to their own gates, which would route instructions down the line to the required user instead of to their own memory. In this way a 16 bit address could gain access directly to 4 Mbytes of remote memory without any special programming techniques required. The gate, being an intelligent device, would take care of all memory allocation.

Data, address and control signals would be integrated into a composite signal somewhat akin to a TV transmission. Analogue signals and the transmission of macro data, macro commands comprising entire program modules symbolised by a short string of characters, would speed up communications dramatically.

When a micro is running a program which exhausts its own address space, the gate transmits a 'resource request' code down the line. Any machine in the network which has the required resources lying idle, automatically transmits a 'resource available' code to the requesting machine. On receipt of this reply, the first machine transmits a series of

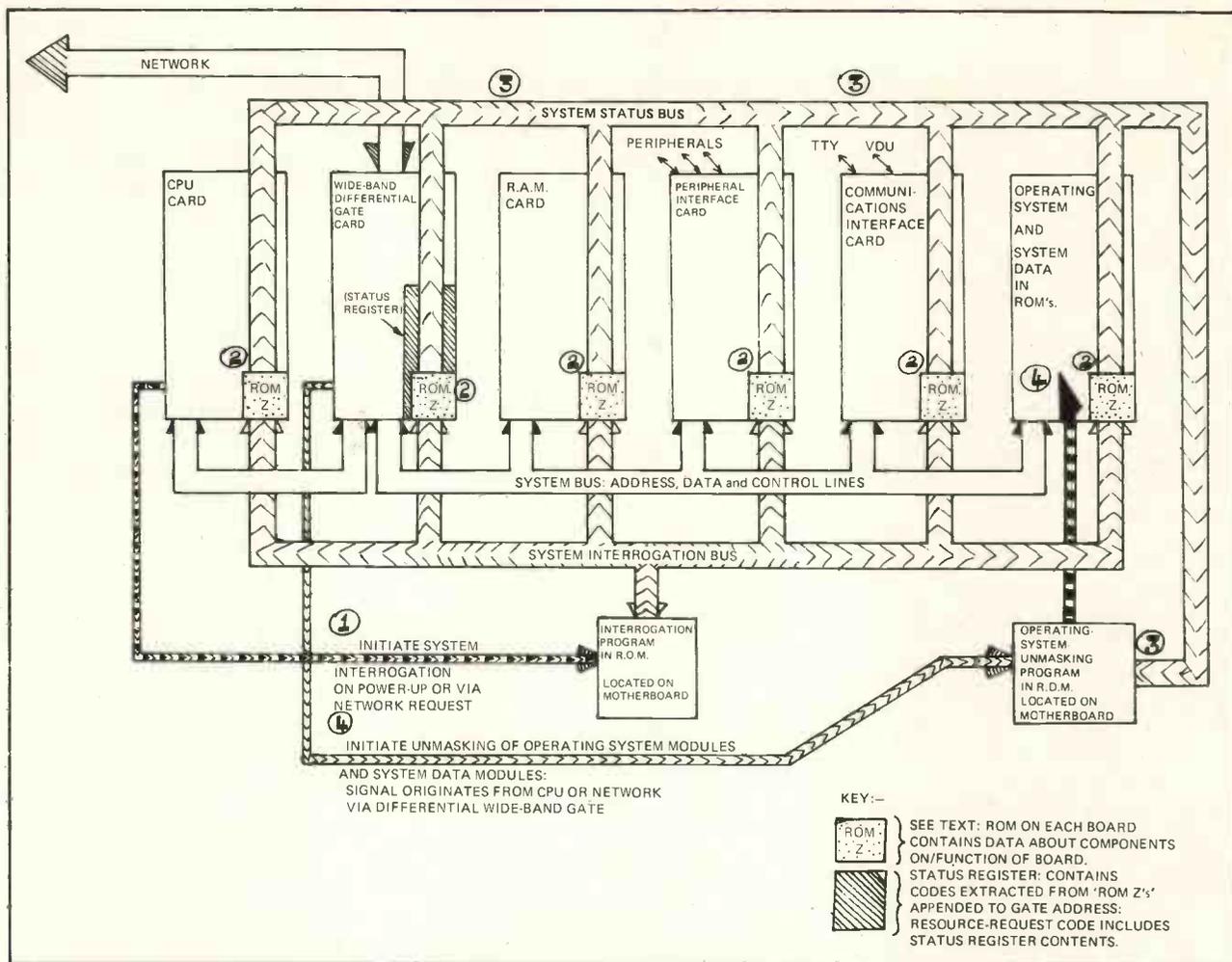


Fig. 3. System Architecture for Minimum-Configuration Microcomputer:— 1 Thru 4 Illustrates Procedure for Unmasking Operating System Modules.

'inter system macro commands' which causes control to pass from the CPU to the gate. From that moment on, the requesting computer can address the remote memory space as if it were its own. When the additional resource is no longer required, the 'process terminated' codes cause the 'captured' gate to 'return the borrowed memory to its owner'.

The gate is somewhat analogous to a multiplexer with chip select functions provided via the network.

If a CPU is currently using its own resources, it disconnects or disables the network 'chip select' control functions, thereby ensuring integrity of its own processing.

Analogue communications occupy the upper sideband of the composite signal, the lower sideband being used for overall network control functions. Thus, a transmission would include, on the lower sideband, a 'line busy' code which would prevent all users below a certain priority from even entering the line. In this way, net-

work users could guarantee the security of their data and programs.

Experimental Communications

Such a network as outlined above does not yet exist. It may not be representative of the type of system we will see in the future. However, it is possible and future systems will be very different from today's. Our present primitive public network could be used, with permission if necessary from relevant authorities, to investigate the possibilities of geographically remote memory access. Given a couple of identical computers and two identical telephone lines I would not hesitate to commence my own experiments. The resultant system would most likely be somewhat clumsy compared with the ideal system I have outlined.

The hardware required at each end would consist of a microcomputer, acoustic coupler or modem, a gate based upon, but more primitive than my suggestion and some very ingenious software. The latter two items would be the key to an effective system. The system buses would require slight modifications, (best carried out using bus extender cards rather than gambling away your electronic pet) in order that the communications gate can be inserted be-

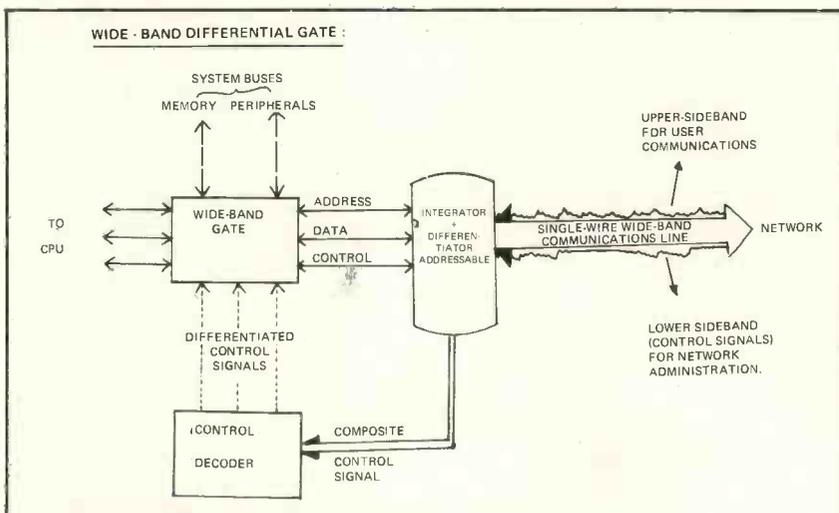


Fig. 4.(a) Simplified Block Diagram (Above)

tween either your CPU or memory and the rest of the system.

As the required communications lines do not exist, other than within large mainframe installations, you will require a friend who will synchronize his watch with yours and a clean line (line noise can play havoc with acoustic couplers). I visualise early experiments to be fairly simple; storing data in your friend's remote memory; your friend accessing the

data; compare data to ensure (a) it has been transmitted and received and (b) it has not been corrupted. That can be tried both ways. The next stage would be the transmission of programs. Check that the programs transmitted and received are identical. Next, transmit a program and initiate the remote computer to (a) process data against the program and (b) let you know when it has finished and (c) transmit back to you the results

of its processing the same data against the same program on your own machine. Full documentation should be kept of all plans, procedures undertaken and results.

Failures are as valuable as successes as long as they are all well documented. The one type of failure to guard against is the building of hardware which just is not compatible electrically with your system. There are programmers who are not electronic engineers and vice-versa. By communicating ideas via a central point from which information could be disseminated to relevant parties, co-operative research and creative experiments with each person contributing from his own field of special experience or aptitude, could in the long run produce some solutions to very real computing problems.

I would personally welcome any feedback from readers, in the form of ideas, opinions or criticisms; whether they relate directly to computing or to more distant areas such as sociology, industry, politics, economics, etc.

These latter areas are as important to us as the hardware itself, for microcomputers will affect the lives of us all and, TV games included, we are engaging in an activity which is rapidly reshaping the environment of ourselves and our descendants.

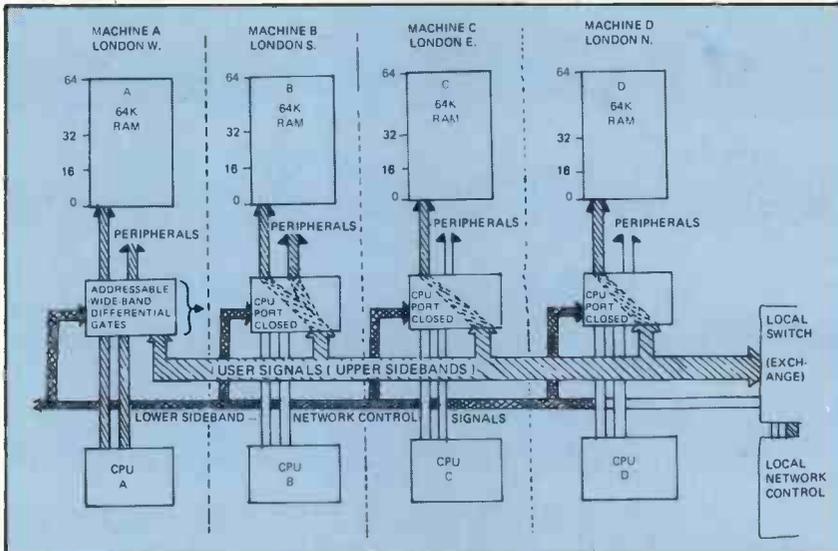


Fig. 4.(b) Machine A (64K) has expanded itself to 256K by 'Capturing' 3 other 64K machines; it has addressed their gates & obtained permission to use their resources; use is also being made of machine B's peripherals.

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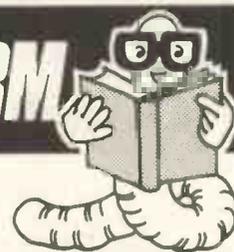
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Homebrew TMS9900 - based computer

Caspar Bowden

Introduction

There is a great difference between writing assembly language programs for large computers and for microcomputers, because of the limited capabilities of MPUs. Low-level programming can be fascinating and challenging, but on micros it is frequently tedious.

The TMS9900 is an exception; this 16-bit MPU has an instruction set equal to those of many minicomputers and an architecture superior to most. This article discusses some of the hardware and software necessary to implement a 9900 based system, which can be used as an assembly language trainer, and also as a general purpose computer system.

9900 Architecture (Ref. 1)

The 9900 can address a 64K byte memory space which is physically organised in 16-bit words. Instructions are always on even byte boundaries, and memory locations are represented as even byte addresses. 32K words are addressed by the 15-line address bus and the 16th bit is used

internally to select the odd or even byte.

Instead of one or two accumulators inside the CPU, the 9900 uses main memory locations in blocks of 16 as general CPU registers, R0 - R15, any of which may be used in instructions. These register blocks are called workspaces and the current workspace is defined by an internal register, the workspace pointer (WP), which holds the memory address of R0. There are two other CPU registers, the Program Counter (PC) and Status Register (ST), which are found in all micros.

The 9900 does not use a stack for linking subroutines or interrupt service routines. Instead a "context switch" occurs. The transfer vector for the switch, which consists of the entry address and workspace pointer of the subroutine, is obtained from a specified address. The current WP, PC and ST are stored in R13, R14 and R15 of the new workspace and then control is passed to the subroutine. A return to the main program is accomplished in a single instruction by restoring the original CPU register con-

tents. Providing each subroutine has a new workspace, linkage is preserved.

There are 16 "prioritised" interrupts, 16 extended operation instructions (XOPs - calls to frequently used subroutines) and a general subroutine call instruction, which cause context switches. The processor expects to find the transfer vector for XOPs and interrupts in locations 0000 - 007E (space for 32 vectors). Before an interrupt or XOP is used, the transfer vector must be installed in the correct location.

I/O in the 9900 is performed over two serial lines, CRUIN and CRUOUT (CRU stands for Communications-Register Unit). From 1 to 16 bits may be transferred by a single instruction and 4096 I/O bits can be uniquely addressed. The 12 bit address of each I/O bit appears on the address bus as it is transferred and in output operations the CRUCLK line is pulsed for each bit. Parallel I/O is possible using the SN74LS251 and SN74LS259 components and the circuits in fig. 1.

System Hardware

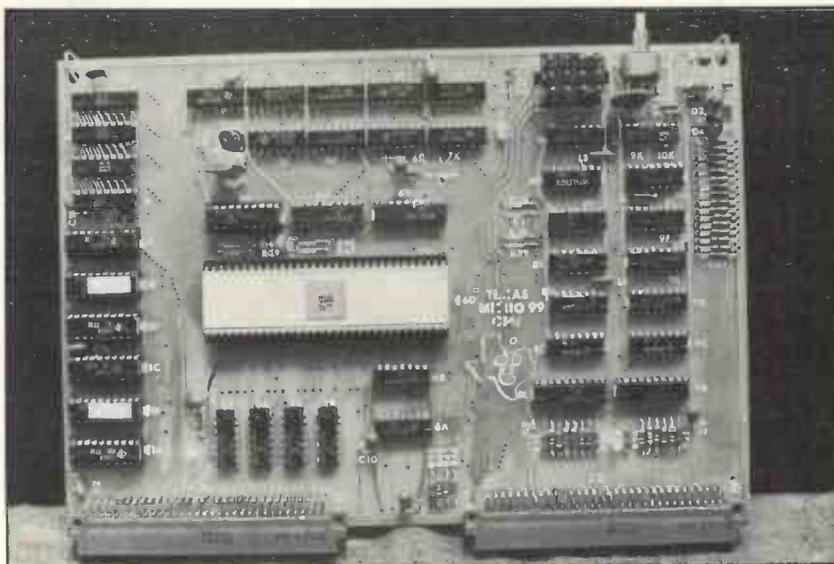
The basis for this system is the Texas Instruments Micro 99-16 CPU Board (Photo 1) which supports the following features on one double Eurocard:

1. TMS9900 MPU
2. 3MHz clock driver
3. 16 prioritised interrupts
4. 16 bits parallel I/O
5. Separate, buffered buses
6. RS-232/20 mA serial terminal interface
7. 168 words user RAM (00B0 - 01FE)
8. TIBUG system monitor and a simple, interactive assembler in PROM.

The prototype system incorporates the additional hardware below:

1. 4K words user RAM (static)
2. 2K words user EPROM (2708)
3. Software driven EPROM programmer
4. CUTS cassette storage interface
5. Vero KM4 Case/Frame
6. Four voltage regulated power supply.

The power supply must provide these regulated voltages (*minimum* current rating in brackets); +5V(4A),



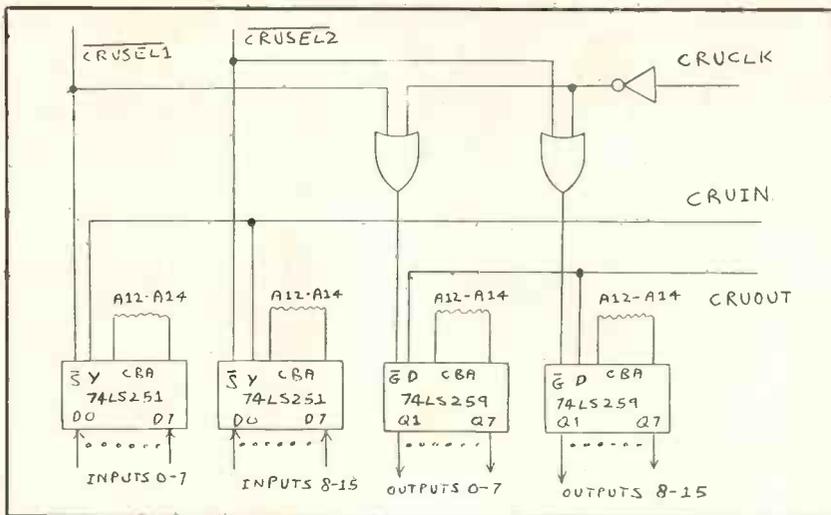


Fig. 1

+12V(1.5A), -12V(0.5A), -5V (0.1A). A suitable unit may be obtained from ref. 2. An additional regulator is required to provide the -5V.

The cassette interface is simple and inexpensive and is obtained from Electronic Systems (they advertise in BYTE). The TTL serial interface makes this unit ideal for use with the 99-16 (see later discussion of TIBUG I/O arrangements).

The EPROM programmer (fig. 2) is based on a design by Steve Ciarcia in March '78 BYTE (see article for details). The programming software is discussed in the original article but some special considerations apply to the 9900.

- 1) The programming software must be written in assembly language, not BASIC.
- 2) The data to be programmed is obtained from a 1024 word block of RAM. The left and right bytes of a word are put in separate 2708 EPROMS.
- 3) To generate the EPROM address (between 0 and 1023) of a data byte, shift the RAM address right one position (to convert a byte address to a word address). Output the 10 least significant bits to the CRU. The block of data must begin on a 1K word boundary.
- 4) The proposed I/O port assignments are:
 Data Byte CRU bits 0 - 7
 R12 base address = 0060
 Data Address CRU bits 0 - 9
 Program Enable CRU bit 14
 Program Pulse CRU bit 15
 R 12 base address = 0080

Circuit Board Assembly

The 4K RAM card (fig. 3), 2K EPROM card (fig. 4) and EPROM programmer should be constructed on prototyping boards using the logic diagrams, as described below. The IC layout and edge connector wiring is not critical and is not specified. Three decoding circuits are required to drive the MSEL, DSEL and CRUSEL inputs to the cards (see figs. 5 and 6). There is space for these circuits on the EPROM programmer card. The suggested memory map is given in fig. 7. The 9900 memory cycle with no wait states requires a memory access time less than 510 ns.

When delays caused by buffers and decoding logic are considered this is comparable with the access time of the 2708 EPROM (450 ns). Therefore one wait state may be required, depending on the particular system. Wait state logic is included in fig. 4, but when testing the EPROM card leave the READY and WAIT lines unconnected and see if the card works reliably. If not, the wait state may be required.

There are two types of prototyping board used in this project:

- 1) The EPROM Programmer is assembled on a Vero DIP double Euro-

card which use two piece indirect 64/96 connectors (ref. 3). There are 64 pins per connector and two connectors per board. Connections between ICs are made by point to point links using insulated hookup wire on the component side of the board. The stripped ends of the wire protrude through the underside of the board and are soldered to copper pads.

2) The 4K RAM card and 2K EPROM card are assembled on Vero International size boards which use direct connectors (ref. 4). The connector has two rows of 42 pins. Connections between ICs are made using the Verowire system. Two or more IC pins are linked together with insulated wire from a continuous reel, on the underside of the board, using a wiring pen. The wire is attached to the pins first by wrapping, then by soldering to a copper pad. This melts the wire insulation giving a reliable joint.

Hints for Construction

- 1) Draw the IC layout on the plan provided with the board.
- 2) Make upside-down pin diagrams of the ICs; most of the wiring is done with the board upside down.
- 3) Use sockets for all ICs.
- 4) Make power connections to the ICs with thick wire, since the wiring pen wire is very thin.
- 5) Solder the wrapped pins a row at a time, not one by one; it's faster and solder bridges are immediately obvious.

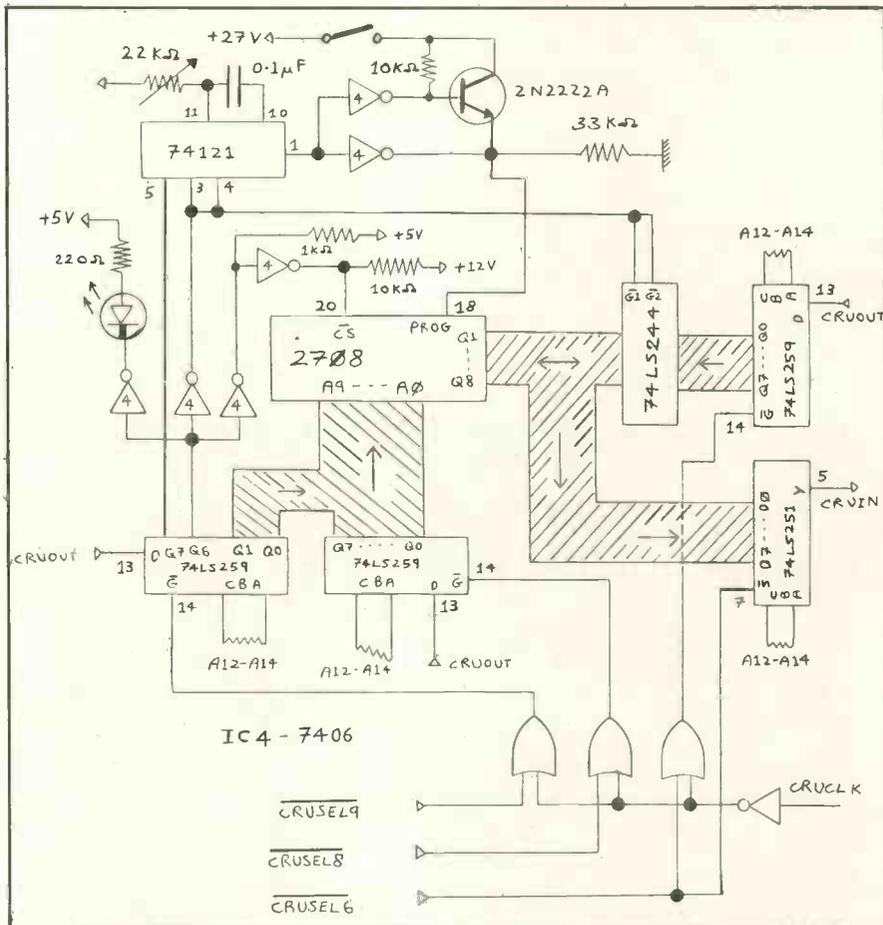


Fig. 2

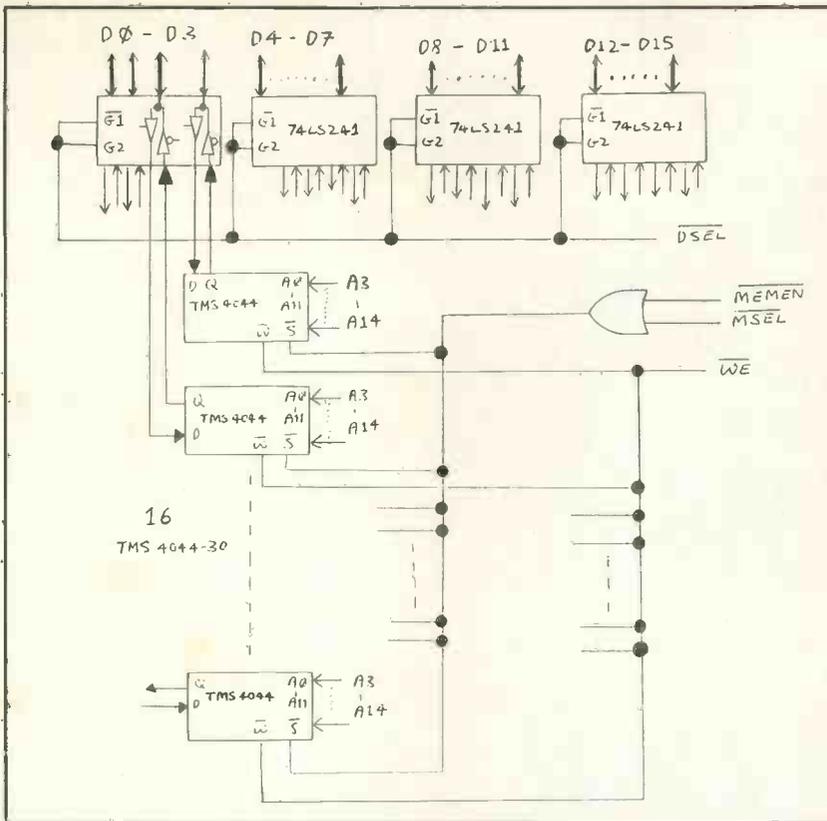


Fig. 3

- 6) A short circuit across the power lines must be avoided at all costs. Check this every few joints. Imagine trying to find a short on a board with several hundred joints!
- 7) Practice a few joints on some old strip-board before starting for real.

The Case

The KM4 case (Photo 2 and ref. 5) will accept double and single size Eurocards as well as International cards (with a slight modification). The connector sockets for the circuit boards are screwed to parallel rails in the rear of the case and links between connector pins are made using ribbon cable (Photo 3). Sleeving insulates the soldered joints. This method is slow but flexible, and it is easy to correct mistakes. Each card requires a different subset of the 99-16 bus and only the essential signals are wired to each connector.

The back panel of the case can be removed, giving easy access to the rear, where there is ample space to mount a power supply. The position of the cards in the racks is not important and can be configured to suit the user's requirements. In the author's system all front panel controls are contained in a single module (Photo 4). The controls are:

- 1) DPDT keyswitch which isolates the power transformer from the mains.
- 2) Latching push-switch which operates a cooling fan.
- 3) Large filament lamp power indicator.
- 4) Display bezel containing two LED power indicators and ten user-defined status LEDs connected to CRU output bits 6-15.

A lower panel contains two, 25-way "D-type" connector sockets, one for a teletype and the other for a parallel keyboard.

99-16 Firmware

The line-by-line assembler (ref. 6) allows programs to be written using instruction mnemonics instead of machine code. Each instruction is translated into machine code and loaded into RAM, as it is typed in; hence there are no assembler directives and absolute addresses must be used instead of labels. The TIBUG monitor (ref. 7) provides commands for debugging and executing the programs written with the assembler.

A competent programmer could use the existing firmware as the basis of a much more extensive operating system, incorporating a full two pass assembler, by making patches to his own software, stored in 2708 EPROM. However a special technique is needed to make a patch in PROM-resident programs.

Modifying TIBUG

The commands that TIBUG recognizes are given in table 1. Each command is handled by a separate routine in the TIBUG program. A routine called MONTP (ref. 8) reads

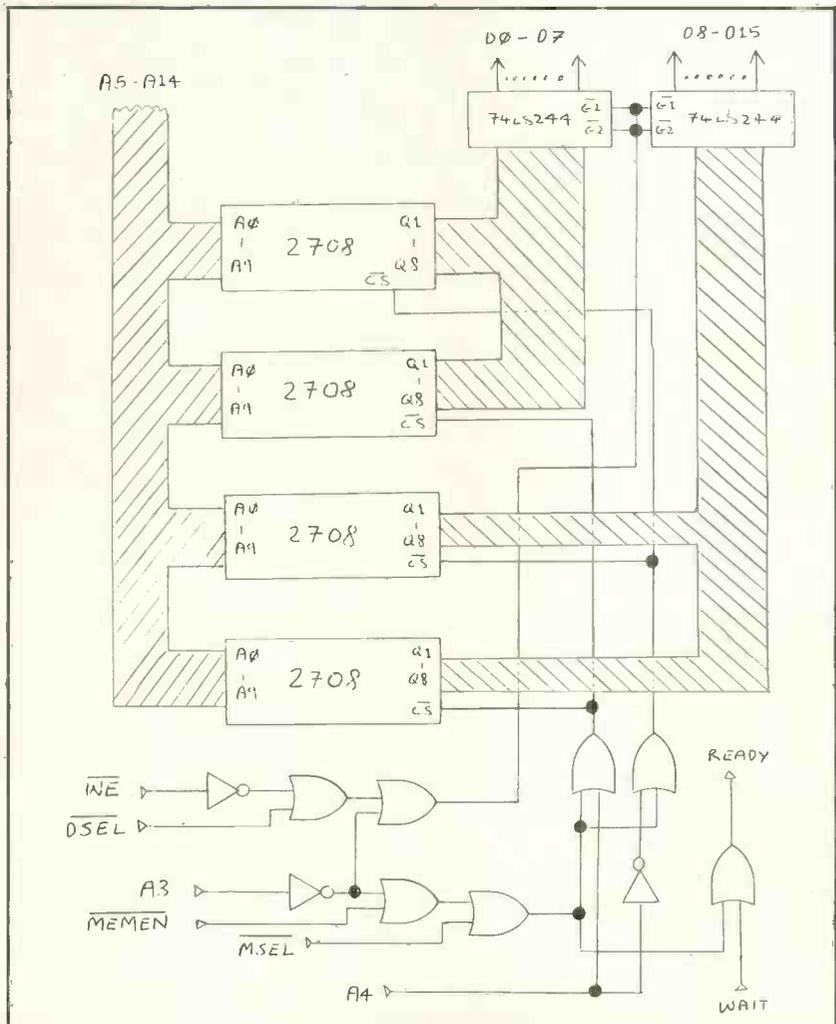
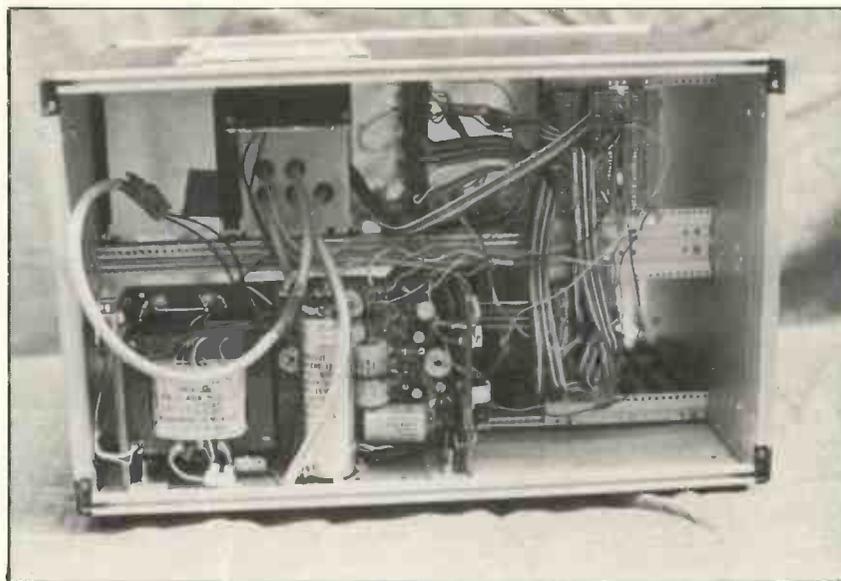


Fig. 4



the command letter from the terminal and branches to the appropriate routine using an address from a table. The table contains the command letter followed by the entry address of the command routine. Unfortunately these routines terminate in a return to the start of MONTTP, not a return to an arbitrary link address (as in a true subroutine). Hence these routines cannot be used directly by other programs. However many of the facilities of TIBUG will still be required in the user's new operating system. Therefore the TIBUG command routines will have to be reproduced in the new operating system, with minor changes to allow linkage to the main program. This copying procedure wastes space in the EPROM and is error prone.

Fortunately there is a way of using the command routines in the existing TIBUG PROM. The entry address of MONTTP is $F896_{16}$ (symbolic name MONTOP) and each command routine terminates with a B @MONTOP instruction (see ref. 9).

After executing this instruction the processor puts out $F896_{16}$ on the address bus, in order to fetch the instruction at that location (in the

TIBUG PROM). A network of logic gates and inverters detects when $F896_{16}$ appears on the address bus and the signal generated is used to disable temporarily the output from the TIBUG PROM (fig. 8).

TIBUG Commands			
B	Execute under breakpoint		
C	CRU inspect/change		
D	Dump memory to cassette/paper tape		
E	Execute		
F	Find word/byte in memory		
H	Hex arithmetic		
L	Load memory from cassette/paper tape		
M	Memory inspect/change		
R	Inspect/change user registers	WP,PC,ST	
S	Execute in step mode		
W	Inspect/change current Workspace		
.	Decimal to hex conversion		
>	Hex to decimal conversion		

TABLE 1

Instead data from a row of DIP switches is enabled on to the data bus through tri-state buffers (which are otherwise in their Hi-Z state). This "data" is of course the machine code for a branch instruction. The branch will be to the user's own command scanner routine which replaces MONTTP. The new routine has access to all the facilities of TIBUG, but new commands are readily incorporated, merely by extending the table of command routine branch addresses.

The 99-16 CPU Board communicates with the user through a serial I/O port which is connected to a teletype. Characters are written and read one at a time, and the parallel-serial conversion is done by software. The TIBUG subroutines which read and write a character are called from the main program using XOP instructions. The XOP transfer vectors for these routines are loaded into RAM by MONTTP at power-up and at the end of every TIBUG command. The new

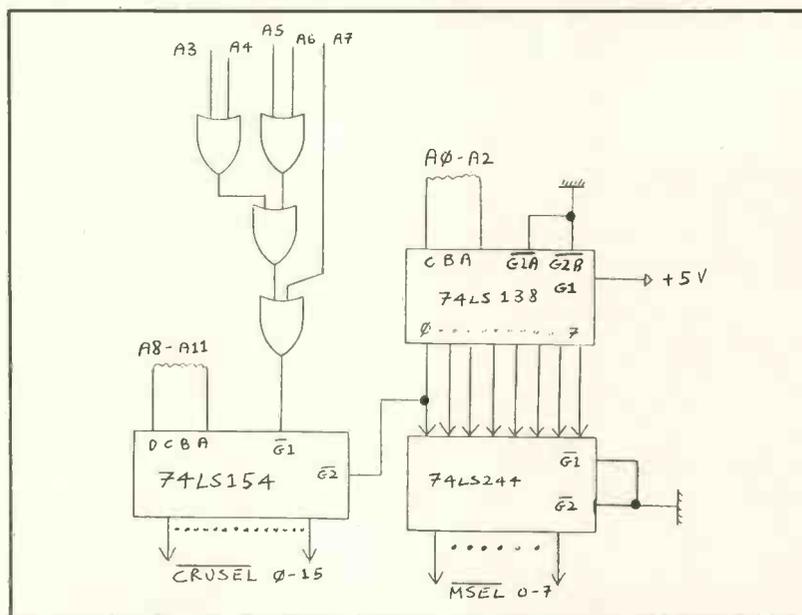


Fig. 5

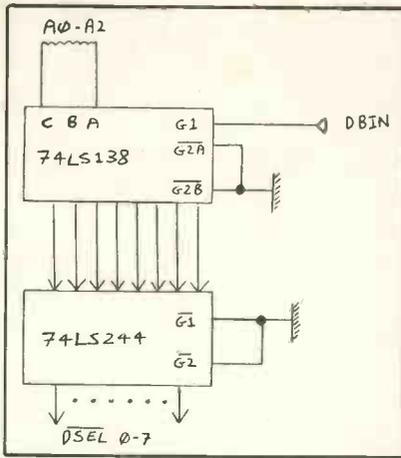


Fig. 6

command scanner routine can change the XOP transfer vectors to point to user-defined I/O subroutines, which can support a VDU, parallel input keyboard, cassette interface or any peripheral the user wishes.

To implement this scheme, some changes must be made to the CPU Board. Before making any alteration, obtain a copy of ref. 10 from TI Bedford, and study the logic diagrams associated with the chip selects of the TIBUG PROMs, and the data bus buffers.

The active-low signal $\overline{ROMEN2}$ is decoded from the address bus by logic on the CPU Board. It indicates when memory between $F800_{16}$ and $FBFE_{16}$ (the first half of the TIBUG program) is being addressed. This signal is attached to the chip selects of two of the four SN74S472 TIBUG PROMs. $\overline{ROMEN2}$ and $A6-A13$ (from the address bus) are further decoded by the logic in fig. 8 to indicate when either of the words $F896_{16}$ or $F898_{16}$ are being addressed. A symbolic branch is a two-word instruction and when the processor reads the opcode for the branch (0460_{16}) at location $F896_{16}$, it will then read the next location ($F898_{16}$), which contains the branch address. 32 switches are needed to set up the two-word instruction.

When $F896_{16}$ or $F898_{16}$ is decoded, $\overline{ROMEN2}$ is forced high (disabling the TIBUG PROM), the CPU Board bidirectional bus buffers are forced to input mode, and data from the correct set of 16 DIP switches are put on the data bus. For this to happen the signals D (which controls the bus buffers) and $\overline{ROMEN2}$, must be taken off the CPU Board, put through OR gates, and then returned to the CPU Board. The printed circuit track must be broken between the two points of connection.

Signals taken off the board are given the suffix "IN" and those returned, the suffix "OUT" (because they are going IN and OUT of the OR gates). The suggested points of connection are:

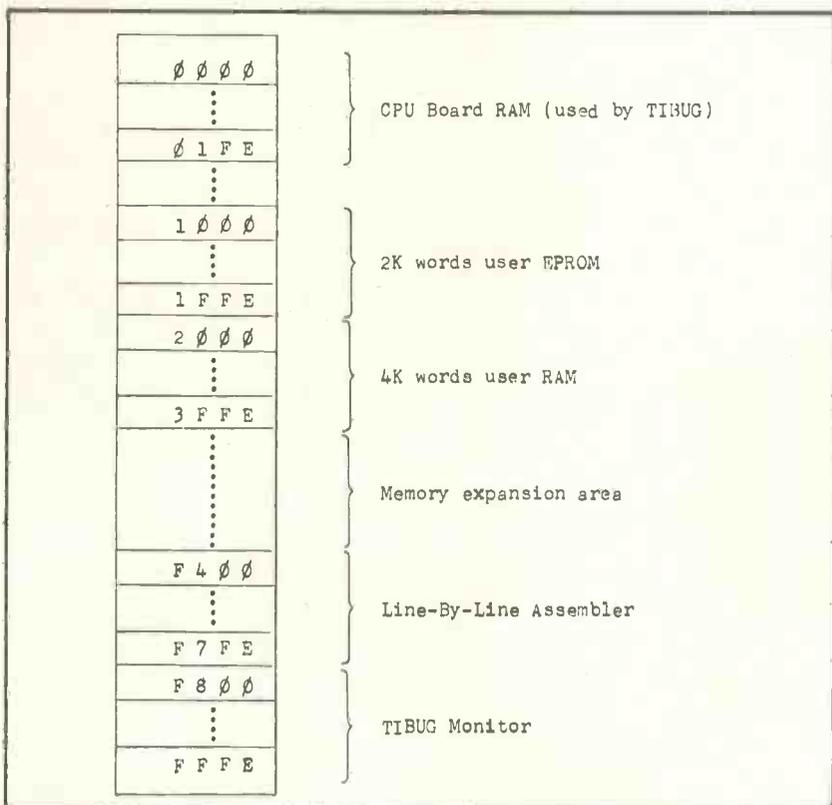
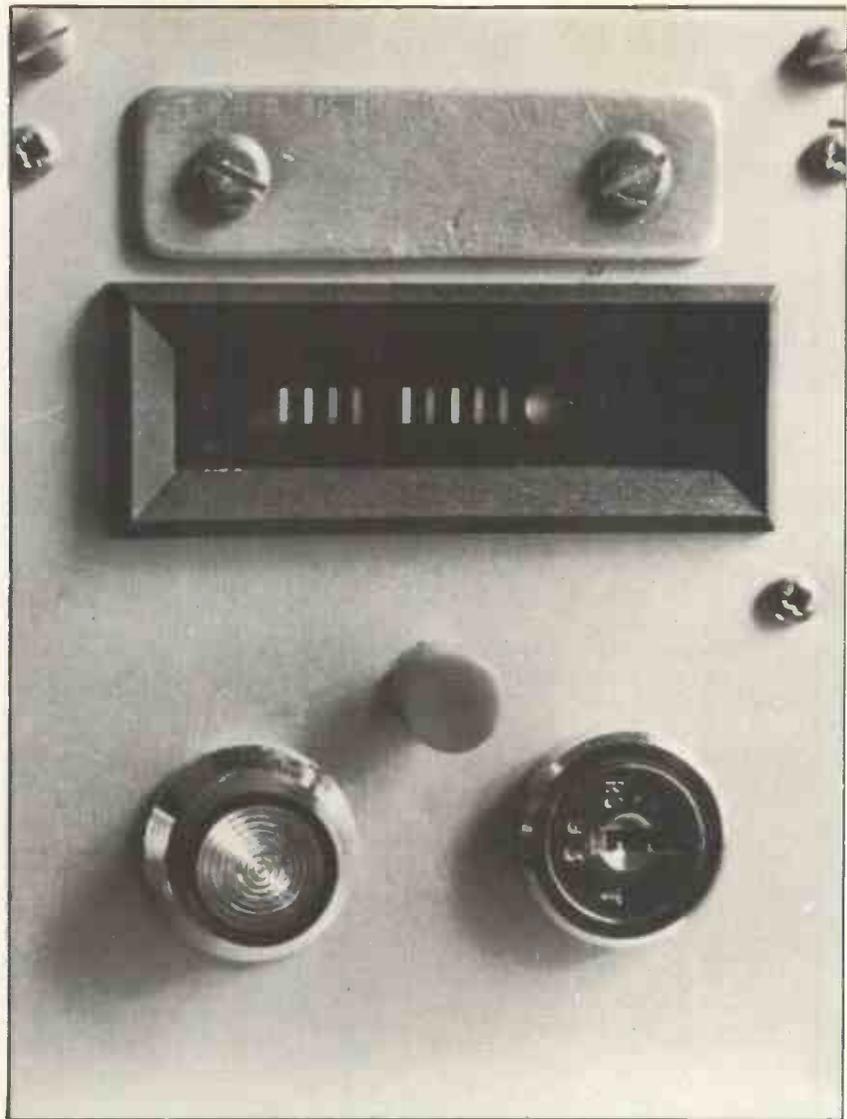


Fig. 7

DIN to pin 4, IC 6A
 DOUT to pin 1, IC 2A

Sever the track between these two points.

For ROMEN2 there are two convenient plated through holes between pin 15 of IC 1C and pin 8 of IC 2L, which can be used for connections. The hole nearest to IC 2L is ROMEN2IN (ref. 10). Again sever the track between the two holes. The four signals may be taken off the CPU Board through uncommitted pins on the edge connector.

Conclusion

Because of the flexible design of the system, the expanding software support for the 9900 can be fully exploited. Memory expansion is provided for by the buffered buses, and in the card select decoding circuits (figs. 5 and 6). BASIC, FORTRAN and PASCAL language translators already exist for the 9900. The 99-16 is a good introduction to the 9900, and can be developed into a powerful computer.

References

- 1) TMS9900 Microprocessor Data Manual
- 2) Lambda Electronics, Abbey Barn Road, High Wycombe, Bucks. Part No.: LOT-W-5152-A
- 3) DIP double Eurocard, Order Code: 10-3183G; 64/96 connector plug, Order Code: 17-2876D; 64/96 connector socket, Order Code: 17-2874C.
- 4) International card, Order Code: 06-1631F; 84-way direct connector, Order Code: 14-0584F.
- 5) Vero Electronics Packaging Catalogue.
- 6) Micro 99-ASM, Line-By-Line Assembler Manual.
- 7) TIBUG User's Instruction Manual.
- 8) TIBUG Monitor Source Listing.
- 9) 9900 Assembly Language Programmers Guide.
- 10) Micro 99-16 CPU Board Hardware Manual.
- 11) 9900 System Development Manual.

Ref. 11 is particularly recommended as a source of useful circuits and application notes.

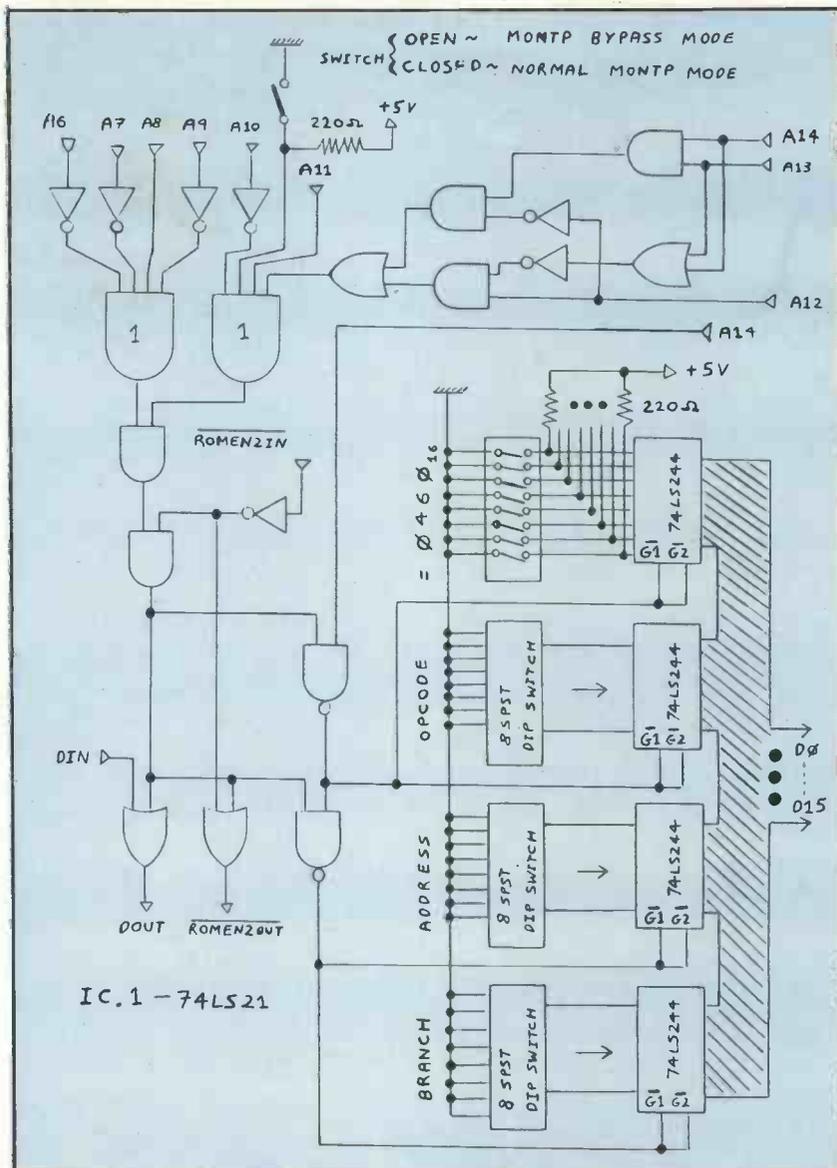


Fig. 8

Acknowledgements

The author wishes to thank Texas Instruments and Vero Electronics, particularly David Bonham and B. E. Gay of those companies, who to-

gether donated the components for this project. Special thanks are owed to Frank Elliott for his sound advice and determined efforts to procure components.

PHREAKSTEIN



“They think he’s related to Einstein!”

PCW OPEN PAGE



THE AMATEUR VIEW

Mike Lord

NEWS FROM THE CLUBS

The North London Hobby Computer Club has now grown to the point where specialised sub-groups are forming within it, dedicated to a particular type of processor or activity. At the time of writing, four such groups have been established, and readers may obtain further information from:

Jim Edgar on 01-349 1170 (evenings) for Business Users
 Ted Gregory on 01-607 2700 x 221 for NASCOM
 M. O'Reilly on 01-607 2789 x 2100 for PET
 S. Emmett on 01-607 2789 x 2447 for Homebrew

Southampton Amateur Computer Club is inviting Kerr Borland, of NASCOM fame, to speak on microcomputing on Friday 2nd March, and they will be showing the film 'Now The Chips Are Down', from the BBC Horizon program, on Friday 9th March. Both meetings are at the University of Southampton and start at 7.30 p.m. For further details contact Paul G Dorey 'Casilla', 757 Portswood Road, Swaythling, Southampton SO2 3SU.

The Lincoln Computer Club — chairman Mike Alexander of 5 Brattleby Crescent, Lincoln LN2 2EB — has now established itself successfully. One of their members has a TRS 80 which he regularly brings to club meetings. Another has a 77-68 system, while other members have various systems under construction.

Following the announcement in the August issue of PCW, the Cheltenham Group has got off to a good start, and is holding regular meetings at the North Glos College of Technology. Mike Pullin is the driving force behind this group, and he may be reached at 45 Merestones Drive, The Park, Cheltenham or telephone (0242) 25617.

Finally, Mr. Alder invites anyone interested in forming a local group in the Edmonton/Enfield/Southgate area to ring him on 01-805 2989.

THE EXETER AND DISTRICT AMATEUR COMPUTER CLUB

We received a letter and a notice of dates and meetings. Unfortunately the letter was not sent in time for the dates to be relevant. We urge all groups to send us information by the first week of the month for inclusion in the following month's issue of PCW.

We did get an interesting bit of information, though! The Exeter Club's membership is increasing rapidly and even now about fifty people turn up to meetings from as far away as Taunton and Plymouth.

Details from the Secretary: Doug Bates, 2 Station Road, Pinhoe, Exeter (Tel: 69844); or The Chairman, David Carne, 44 George Street, Exmouth (Tel: 74479).

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Gwent Amateur Computer Club

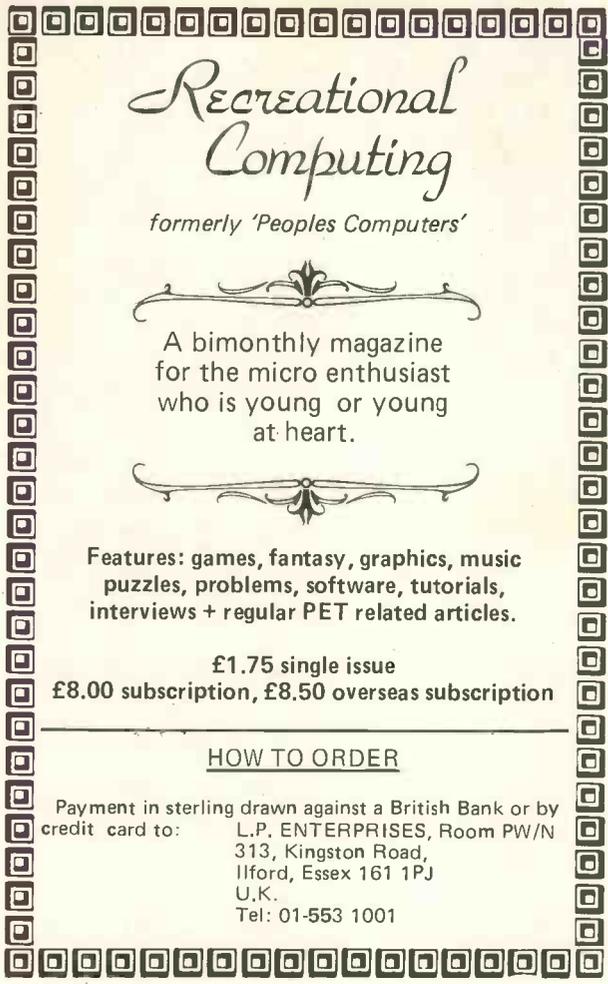
A computer club has been formed in Gwent by a group of enthusiasts with an interest in amateur computing. Its meetings, held on alternate Wednesday evenings, are very informal and anyone with an interest in the construction or programming of their own computer is welcome to come along. For further details ring:

Alan Beale on Newport 50207
 or Pete Hesketh on Shirenewton 596

TELETYPE KSR33, Serial Interface RS232, sprocket feed, good condition, (working to NASCOM 1), with manuals and circuit £175. From: D. Johnson, Tel: (evenings only) Ipswich (0473) 79023. Modified NASCOM operating system also available with full teletype compatibility.

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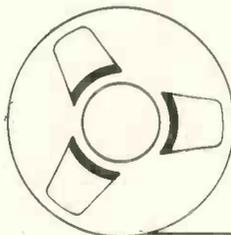
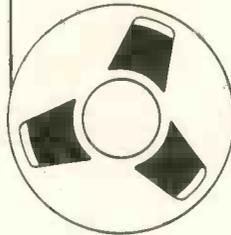
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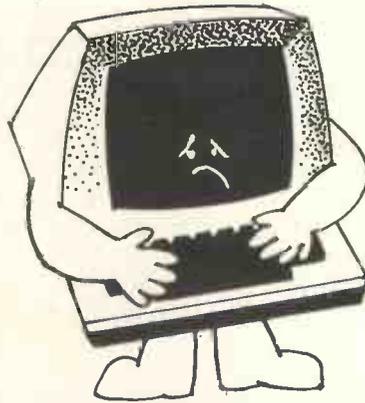
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Personal Experience

PROGRAMMING FOR PLEASURE

David McBreen



"I've indigestion to the core!"

I am already a dedicated reader of PCW and I suspect that you are too. In that case we probably share a common goal, namely to acquire our very own micro and truly enter the 'PCW' rather than just sitting on the side-lines. Having entered the promised land I imagine that you will soon tire of playing the standard games and running the same old puzzle demonstrator programs. You will want to control your computer in your own personal fashion and make it perform tasks relevant to your particular sphere of interest. To do this you will have to enter the perhaps unfamiliar world of programming, a world potentially full of excitement and satisfaction. I have been a programmer now for about twelve years (though my job titles have not always described me as such) and would like to recall for you some of the highlights of my work in this period.

Plugboards and Data Indigestion

I arrived on the Data Processing scene just in time to work with unit record machines that were controlled by plug-boards through which one directed the function of the machine. This could not be called programming in the modern sense since one 'coded' with pieces of wire with a plug on each end, but the effect was essentially the same. One could cause data input and output, move data, total it, reproduce it and use logic tests. In fact the 'collator' was a very clever example of these machines, and contained devices called selectors which would give you an output signal only when two chosen input signals were present — rather like some of today's logic gates, I think, though the term was not known commonly then. Just as now, bad programming and logic errors could lead to disastrous consequences — the machines would sometimes grind to a halt literally screaming about a huge crunched up mass of data cards somewhere inside them.

Card punch

My next step was to master the humble card punch, also vaguely programmable via a pre-punched card wound around a controlling drum. This gave (and still gives) the ability

to reproduce certain data, skip to the beginning of defined fields, automatically set upper-case or numeric shift and quite impressively define some fields as purely numeric and ask the punch to provide enough leading zeroes to fill the field while you only key in the significant digits. Many modern programmers of today's big CPUs would benefit a lot from a simple course in 'programming' this basic device.

At this stage real computers came on the scene and I worked for some time with the IBM 1401. This was a super machine on which to learn the real art of computer programming since one could always tell exactly what the machine was doing. The only thing in it was your program and there was no operating system (or supervisor or monitor) to get between you and the hardware. It had some very simple operation codes such as 1 for read a card, 2 for print a line, 4 for punch a card; all of which could be added to produce multiple effects (6 for punch a card and print a line) and thereby save you one valuable storage location. This meanness with storage certainly occupied our minds then, since my installation had the largest 1401 available with a "massive" 16K char-

acters of memory. Compare that with some of today's figures!

Pioneer programmers

There was always then a wonderful feeling of competitiveness and thirst for knowledge among operators and programmers. You always wanted to know something that your colleagues didn't (though of course you would be pleased to teach them) or else be able to do something in less storage than they could. I still remember winning a competition where the object was to develop a single card containing a small program that could be placed anywhere in a normal object program deck; and, as the program was being loaded into the machine, this card would cause a line of X's prefixed and suffixed with a letter O to be printed, without prejudice or ill effect to the user's program. This was done so that the operator could verify that all print positions were working satisfactorily at the beginning of a run.

Another little gimmick we learnt was based on the variable length data fields that the instructions would process. There were no built-in fields like 'words' and no lengths defined in the instructions. It was the user's responsibility to define the senior position of each field with what was known as a word-mark. Because of this we could enter into our 16K machine a single multiply instruction and give it two operands each of approximately 8K digits. Once started, this instruction took about 5 minutes to execute and could only be stopped prematurely by turning off the machine power supply!

International Business Machines — the Big Boys

The 1401 was eventually turned out to grass in favour of the IBM

(International Business Machines) 360 and programming life started to change radically at that time. Luckily for me, my employer carried on programming with Basic Assembler Language so I got to know the new hardware and its instruction set pretty well. It offered wonderful new instructions like Edit and Mark, Translate, Translate and Test (all of which I mastered) and Branch on Index High or Branch on Index Low or Equal (which I never really got to grips with). I did quite a lot of work on programs to process paper tape — which is always a rather doubtful data medium because of its fragility and easy mis-use.

Here the Translate and Translate and Test instructions were invaluable, the first to alter any incoming data code to that required by the machine and the second to scan incoming data streams for field and record delimiters.

A little later I had to write some supporting software for an unofficial paper tape reader to be used on IBM machines and this was one of my most interesting projects. The problem with the device was that once data transfer from it was initiated it could not be stopped until all the data had been read. This forced me to use a very special technique whereby I had two large input buffers and a long string of read CCW's (Channel Command Words to read X bytes of data) that addressed each buffer alternately. Using a feature known as PCI (Program Controlled Interrupt) I asked the hardware to give me a nudge each time it filled up one buffer and was about to switch to the other. I then had to process the filled buffer and get the data out of the way before getting the next nudge from the hardware. In the design of this program I actually made the only practical use in my life of calculus to help me allocate buffer-size and the number of CCW's to process the maximum amount of data for a given program size.

Binary Delights

This program also introduced one of the delights of machine level coding, namely the use of an instruction in an unusual fashion. For hardware reasons the input data arrived with each byte of data separated from its neighbour by an unused filler byte. The fillers had to be removed and I could have achieved this by a little MOVE loop but once again my trusty friend the TRANSLATE instruction came to my aid. Normally, one translates a data field according to a fixed translate table but a friend showed me a trick with which one could translate a table according to

the data. This meant that if I set up a table with values 01030507 etc., moved it to my output area and then translated this table with my data, the output area then contained bytes 01, 03, 05, 07 etc., of the incoming data. Quite a neat little trick, don't you think.

One can also use the TRANSLATE (again!) for the purpose of cycling a one-byte field through a range of values such as you do for the head number on a disk when writing your own disk processing programs. The byte is given the initial value 00 and the table set up as 01020300 for example. Successive translations will give you in turn the values 01, 02, 03, 00 etc., and so on in a very neat fashion.

Never mind what's inside — it works

While I went on enjoying myself with the Assembler language, most sensible Data Processing centres turned to the use of high-level languages (Cobol, RPG, Fortran, PL1) for their ordinary production programming. New programmers were trained only in the particular language used by their installation and never really understood the hardware or what went on inside the machine when they coded MOVE A TO B. They also used debugging techniques specialised for their particular programming language and so were (and are) virtually machine independent.

Now, I don't decry the use of high-level languages having had some experience of COBOL, FORTRAN and BASIC. Indeed for carrying out some kinds of work they are ideal and any programmer however keen on machine code would be misguided to turn his back on them totally. It is still quite a nice feeling to code a COBOL program and put it in for a completely successful first test, a rare event with BAL. One accepts that the generated code, because of being generalised, occupies a lot more storage (really a lot) and executes a lot more slowly; but then, machines are much bigger and much faster so we are no worse off. In fact the ease of programming and the higher in-built standard of program readability gives big advantages to programming management. The sad result is that programmers in general do not need the same level of skill as the old 1401 boys and do not get to know their computers so well. The competitive spirit is not there nor the excitement and so the job loses its appeal and its professional standing.

Job Mobility

In order to avoid this rut, I in common with many others in the business have changed jobs a few times. One change brought me out of the IBM world and gave me the chal-

enge of new hardware; namely, the XDS Sigma range. I soon got to grips with the new buzzword vocabulary but took a long time to absorb the different format for writing Assembler instructions. Old habits die hard and my first listings were for a long time littered with syntax errors. However it was very interesting to work on a word-based machine, and I really appreciated two things it offered. First was the removal of the need to provide base registers for addressing storage, and second was my first experience of indirect addressing. These were two big bonuses unfortunately offset by one big problem. All byte (or character) oriented instructions had to specify a byte displacement within the word addressed. If you forgot to specify one, the assembler conveniently (?) assumed a byte displacement of zero and gave no error signal. Only at testing time was a lot of head-scratching necessary to work out what had happened.

Old waters

Sadly, most of the above events are quite old water under the bridge and my current job requirements call for little actual programming, so I am spending my leisure hours trying to rekindle the old flame and get back some of the excitement. I had a little 'play' with programmable calculators. The limit on program size and the restricted instruction set make them exhilarating for a little while but the lack of any real addressable memory or proper input/output facilities soon become over-powering.

Then, all of a sudden, I took notice of the little whisper that grew to a murmur and I think will soon grow to a shout, *Micro Processors*. I am quickly devouring all possible literature on the subject and reading comparative reviews just as I did when entering the Hi Fi scene. The micros seem to offer again all the old charm of my earlier days in computing. There is the wonderful mixture of the real world of Data Processing with all that computers can do for man, and the joy of being able to afford a true computer of one's own. There is also a fast growing band of micro-enthusiasts who want to get together and share knowledge and experience. Marvellous, just what programming is all about and what will once again help it to flourish into a true art.

So let me end by encouraging you to follow my example. First, by whatever means (well, almost) get hold of your own micro processor and then join in the fraternity of enthusiasts so that you can experience some of the pleasures that I have had (and hope to go on having). Let us give a new meaning to MPU: *Micro Programmers Unite!*

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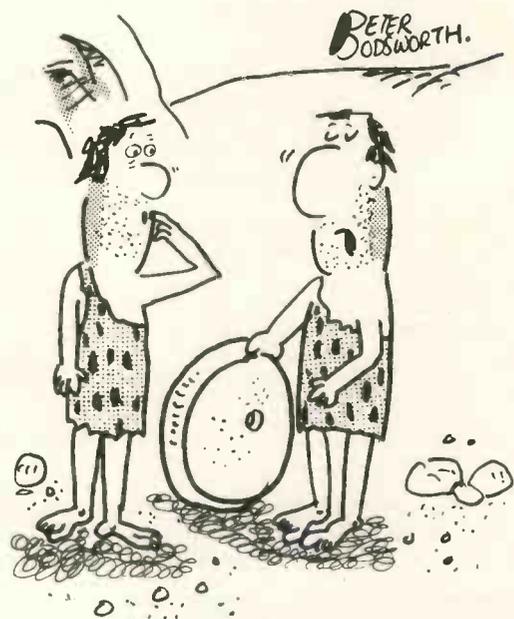
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ON THE LINE

David Hebditch

3. DOWN TO BASICS: LINE SIGNALLING

In the first two articles of this series, we looked at the longer-term future of linking personal computers in the home and office to telecommunication facilities.

This month we shall be getting down to the basics of linking your own personal computer to a telephone line. But, first of all, why should you want to do this? Well, by providing access to the telephone network you could link your microcomputer to someone else's (perhaps for program-swapping or game-playing). It would also enable someone with a display or printer terminal to dial up and use your system. Such an arrangement would make it possible for two or more friends (and they would have to be friends!) to share a computer for a fairly small additional cost, or to pool available funds to obtain a more sophisticated system. By sharing a system its utilization could be much increased (so long as you can agree on who is going to use it and when).

What will you need? A simple schematic is shown in Figure 1.

This arrangement is by no means the only way of doing it, but I believe that it is the cheapest and simplest and the one which can be most easily implemented at home. We shall work our way from right to left in the schematic and describe the requirements at each level in the system.

Telephone lines are designed to carry an electrical analogy of the sound waves made by the human voice. The microphone in the handset is used to create this signal and it is converted back to sound waves by

the speaker in the handset at the receiving end. The signal produced is infinitely variable within certain ranges of amplitude and frequency imposed by filters within the telephone system.

These constraints are important

because they limit the speed at which we can transmit data. Figure 2 shows how the standard network bandwidth of about 3000Hz is a compromise set to cover the different spectra of frequencies covered by the voice and the ear.

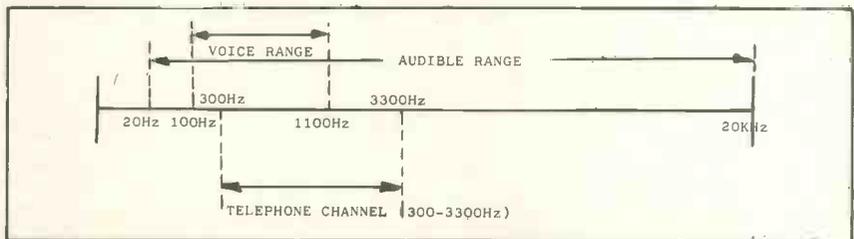
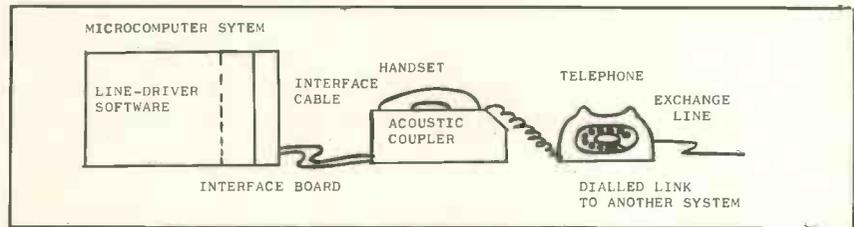


Figure 2. The Standard Bandwidth of the Telephone Network

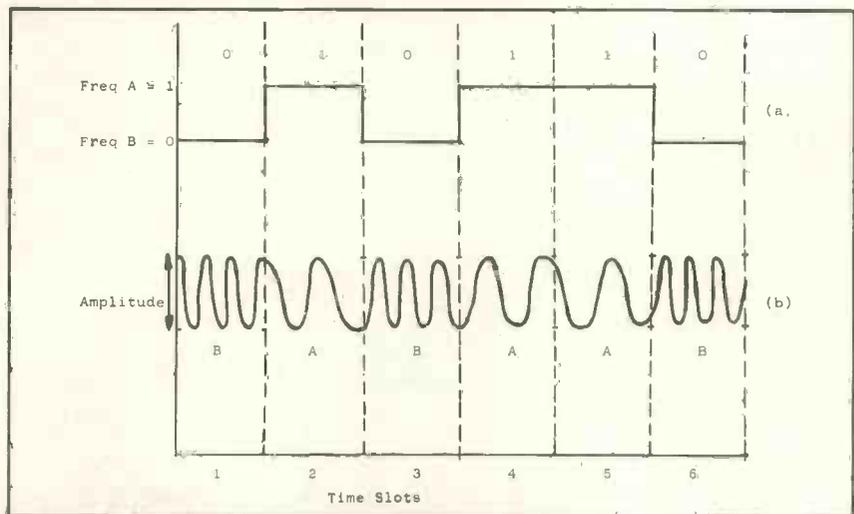


Figure 3. Frequency Modulation to represent Data Bits

Channel 1	0 - bits	1180 Hz
	1 - bits	980 Hz
Channel 2	0 - bits	1850 Hz
	1 - bits	1650 Hz

Figure 4. The frequencies used for FSK signalling

Clearly, the analogue signalling employed on the telephone network is completely different from the direct current (DC) methods employed in computer systems. In the latter case DC voltage levels are used to represent 'one' bits or 'zero' bits. To send these down a telephone line we need to convert them to a suitable analogue form.

There are many techniques for doing this, but the one likely to be of greatest interest to us is known as *frequency modulation* or *frequency shift keying* (FSK). This is based upon the idea of using different signalling tones to represent our zero and one bits. Figure 3 (a) shows a train of bits modulated in this fashion and Figure 3 (b) the same thing in another form.

Obviously, the frequency used must be in the 3KHz range of the telephone system and by international convention:

980 Hz represents 1 bits and 1180 Hz represents 0 bits.

The 980Hz signal is called the *carrier* and when transmitting represents a series of 1-bits. The signal is increased to 1180 Hz each time it is necessary to send a 0-bit.

At the speeds we shall be operating, the bandwidth is adequate for us to have two transmission channels; one for sending and one for receiving. When this can be done simultaneously, we describe the circuit as *full duplex* (FDX). The four frequencies employed are shown in Figure 4.

Now we know *what* we are going to send on the telephone to represent our data bits, how do we get them on there (and off again)? To achieve this we employ a modulator/demodulator, which is fortunately contracted to *modem*.

A modulator takes the DC bit-sig-

nals and converts them to the frequencies shown in Figure 4. A demodulator samples an incoming AC signal and converts back to DC. Unless we only want to transmit in one direction (which is unlikely) then that is all we need. But usually a complete modem is required at each end (one is no good to us at all). This is illustrated in Figure 5.

A modem at rest is set to transmit on Channel 1 and receive on Channel 2. If both did this we would not, of course, get to send anything. So the *called modem* (the one you dial to) must be able to switch to receive on Channel 1 and transmit on Channel 2.

Next month we shall describe the timing and synchronism problems. For further reading in the meantime try the Post Office Handbook of Data Transmission (NCC Publication, at least £8.50).

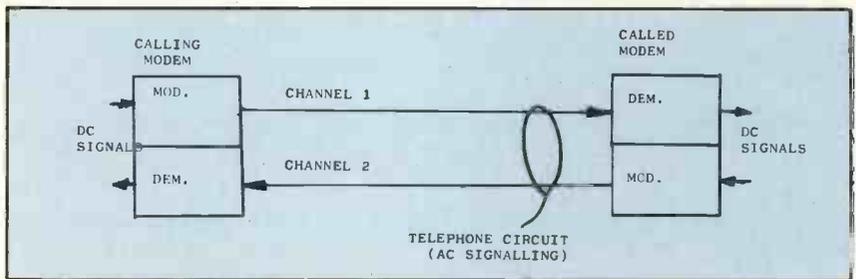
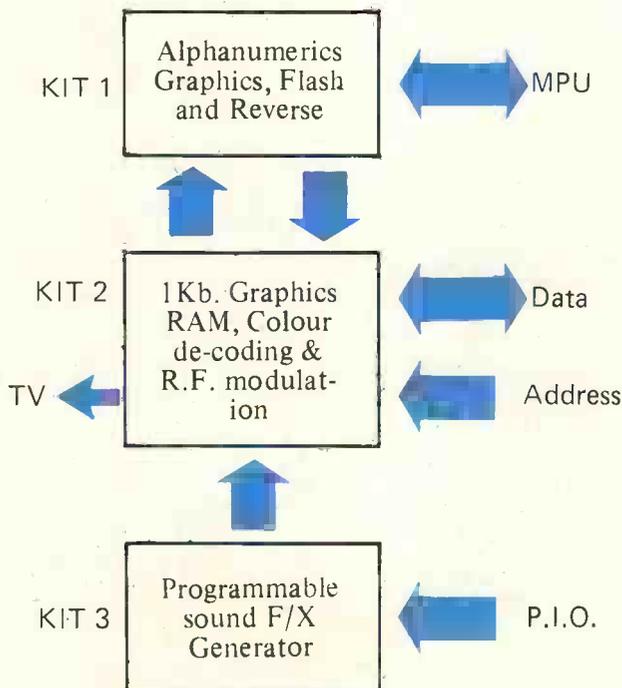


Figure 5. Digital/Analogue conversion using modems



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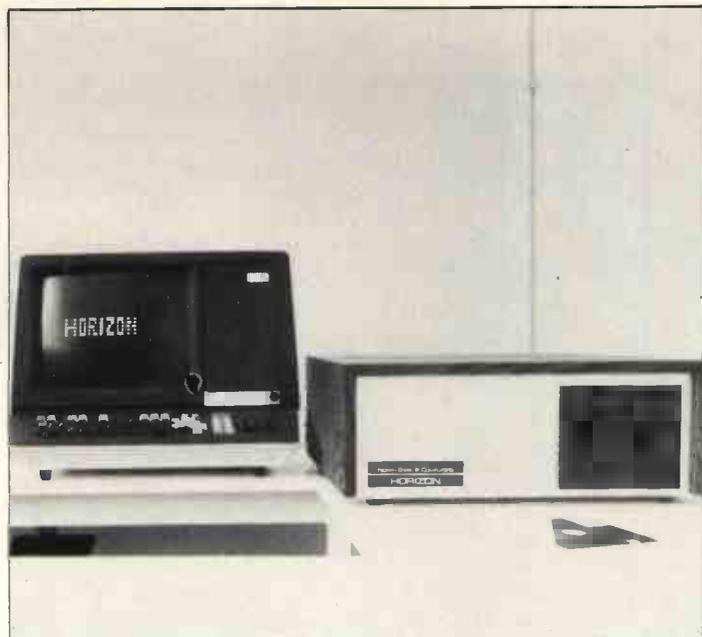
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BUSINESS COMPUTING

Part 2 (Conclusion)

Rodnay Zaks

The Mailing List

The mailing list is often neglected in a business system. This is because most business systems provide a *complete record* of sales (the sales list). In such a sales record, the name of the customer, as well as all information relevant to the transaction, has been entered. At first sight, it might therefore look as if the system has all the information available that it needs in order to list customers for a promotional action. Technically this is correct. However, in practice, *such a sales list is not usable as a mailing list for immediate use.*

For *short mailings*, the sales list can indeed be processed by a specialised program which will generate the names and addresses and print them. For *long lists* (such as several thousand names) direct processing of the sales list is completely impractical. First, it would be slow, as the information in the sales list is block structured and only a few entries must be retrieved from every block. Second, the information in the sales list will normally be bulky, so that relatively few names will reside on a single physical medium such as a diskette. Processing the sales list will therefore require significant time and frequent manual changing of diskettes. In short, it is generally unacceptable.

For efficient mail list management, it is also imperative that the user codes every transaction at the time it is performed. For example, the user might code the type of business, or the type of individual involved in the transaction. He might code the nature of the items purchased or the range of the sale. In this way, a compact code can be used which can be utilised as a *selection criterion* within the list. An efficient mailing list is created by processing the *customer's*

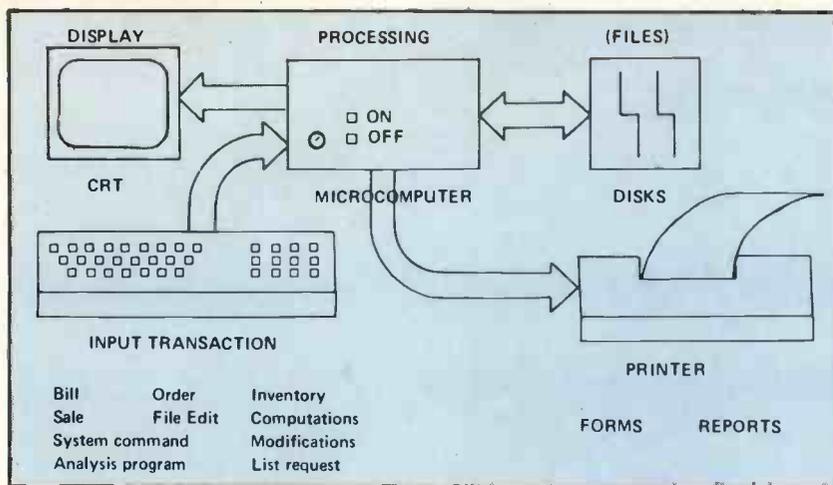
list or else the *sales list* periodically. It must be kept sorted, either alphabetically, or by zip code or by a special user code. In this way, whenever a new name is entered into the list, possible duplication can be checked immediately and efficiently. Even so, a typical mailing list, reduced to the name, address, and code, will contain a large number of characters for each entry. Let us look at it: it will contain the first name, middle initial, name, title, company name, division or mail stop, street or PO Box, city, state, zip. In addition it will contain a 5 to 20 digit code for efficient retrieval of names. Result: perhaps 100 characters per entry. Let us assume that 80 characters are sufficient for our purposes. A typical block on a diskette contains 256 characters. In our example such a block would contain only 3 names. A typical diskette will provide about 1200 such blocks, and will therefore store about 3600 names.

This is not sufficient for most mailing lists. An efficient mailing list program should be capable of handling anywhere from 1,000 to 10,000 or 50,000 names. Clearly, such a system would be very cumbersome to use, as diskettes would have to be changed manually frequently until the complete list is processed. This may not be acceptable.

As a result of this constraint, microcomputers, restricted by their limited amount of disk memory, impose the necessity of a *specialty structured* mailing list file. An *index block* is created, which contains only a few bytes per entry. It contains the customer name or code, and a customer pointer, usually a number. In this way it can be restricted to 20 to 30 characters maximum. A complete diskette will be typically allocated to this mailing list index. Whenever a

selection is to be performed, only the *index block* diskette needs to be mounted initially. As an example, the mailing list selection is for all companies in the distribution field, which have ordered more than £100 worth of parts in the last three months. The selection program will derive all its information from the *index file* and will *generate a list* of customer numbers meeting the specified criteria. This list can then be used by a simple mailing list *printing program* which will print the addresses from the customers or sales file, as selected by the list of customer numbers. Whenever the selection has been performed, the program will start generating messages such as "please load diskette number 2-5". This diskette contains the first block of entries that this mailing list processor wants to print. A number of diskettes will still have to be successively mounted on the system, if the mailing list is long, in view of the limitations inherent to each diskette. However, the complete selection, which can be a lengthy process, has been performed efficiently in a very short amount of time using only the index block diskette. A good system will write on a diskette the names it will print and will signal the user on the CRT display that it wishes to have another specific diskette mounted next. The user will have the time to mount the next diskette while the system is busy printing labels. By the time the printer, which is a slow device, has finished printing the last name of the previous diskette, the next one will already have been mounted. The system will perform at the maximum mechanical speed it is capable of.

The drawback of having to feed successive diskettes to a system can be eliminated by purchasing much



The Elements of a Business System

larger hard disks or dual drive dual density diskette drives. New low cost fixed head disks are beginning to become available.

Existing Software Facilities

Most microcomputer systems available today offer the hardware capabilities required to perform all of the operations that have been described at sufficient speed, provided no complex arithmetic is required. Unfortunately, *no complete business programs have yet been developed, which completely automate all the tasks required.* It can be seen easily from the above description that the task of the file management system and of the various processing programs is complex. Such programs have been created only for the larger computers.

The cost of developing such programs is much larger than the cost of developing the actual hardware on which it resides. For this reason, manufacturers are usually not anxious to develop such expensive programs when they are in the business of selling hardware. Consulting firms and software houses have traditionally had a good business selling specialised programs or packages to business users. However, because software cannot be efficiently protected against duplication, it is difficult to sell software programs at a profit for low cost hardware.

Most microcomputer systems available today will offer a few business programs. Typically they will offer a general purpose file system, which allows the user to create and manipulate files symbolically. *This is totally insufficient.* Specialised processing programs must exist, which allow the business user to gather data automatically, conveniently, to update it, and to have the computer perform automatically the necessary updates in other files. Most programs available solve only one of the problems. Usually, there is an accounts receivable program, and a *separate* accounts payable, and a *separate* inventory program, and so on. These

separate "packages" are useful to maintain independent files. Provided that the number of transactions is high for any one of these files, they provide a valuable service. However, they do only part of the job. The business user is still required to update manually all of the files that might be involved in a single transaction.

Using Microcomputers for Business Applications

Now that the limitations have been pointed out, *is this a reason not to consider a microcomputer system in a business application?* No.

The facilities that have been described are the ideal facilities for a business automation system. However, even solutions far from this ideal will provide benefits far in excess of the cost of the system. A useful system can be purchased for as little as 5 to 10,000 pounds. Such a system with minimal software packages will permit the automation of the inventory, the accounts payable, the accounts receivable, and often other functions such as mailing lists, back orders, payroll or tax computations. Such benefits by themselves usually far outweigh the initial cost of the system. For this reason microcomputer systems are a very valuable tool for limited business automation. However it should be kept in mind that an invisible price will be paid. If extensive files are created, or if specific programs are written, the so-called "software investment" will become dominant. After a period of time, the investment in structuring these files or developing new programs will become more significant than the initial purchase price of the system. After a few years, limitations will be felt and there will be a desire to move to a larger, more complete system. Naturally there is a possibility that the manufacturer of the original system will have expanded its resources. Typically this is unlikely in the long run. In view of the constantly decreasing price of hardware, it is likely

that, within a few years, the hardware itself will be obsolete, and that the manufacturer will be marketing a new system, which will not be completely compatible with the first one. The business user will then have to move to the new system and reformat his files and redevelop new programs.

However, it is the author's feeling that even if the first system is essentially abandoned after a few years, it will provide an extremely valuable transition into the true computerised business management world. It is correct that the initial hardware investment will have been lost after a few years, and that a substantial software investment might also be lost. However, this will have been translated in a structuring of business procedures, computerised operation, the training of personnel, and an awareness by management of the additional capabilities which will be needed in future systems. Such a system will provide immediate initial benefits that will typically far outweigh its cost, and it will provide substantial educational benefits to its purchaser. After using such a system for one or two years, the intelligent purchaser who understands the nature of his needs, will be in a position to thoroughly understand the ideal system for his business needs. At this point, his second choice is likely to be an optimal one.

The comparison is analogous to the recommendation that a new driver should first drive a low cost car before purchasing the car of his dreams. The first machine which may be inadequate, but provides educational value by expanding the skills of its user.

Custom Business Programs

Once the specific needs of a business have been identified, it becomes possible to evaluate whether a specific microcomputer system will meet its needs. If it does not, additional software programs or packages should be obtained. The essential question at this point is: *is it worth writing a program or contracting outside to add specific programs required by the business?* The usual answer is: *no.* Clearly, if the programming capabilities are available in house, or if the educational value of programming is significant to you, then it might be worth writing your own programs. The important point is that most business users simply *thoroughly underestimate the amount of effort needed* for a usable correct, and documented business program. It is indeed possible to develop quickly in a high level language such as BASIC a program which will appear to meet the main needs. However, unless such a program is well developed, well documented, well adapted



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PCW Book Review



Michael James

AN INTRODUCTION TO PERSONAL AND BUSINESS COMPUTING

Rodnay Zaks
(SYBEX, 5½ x 8½, £4.95)

This is the best introduction to personal and business computing I have found so far. It opens with a fanciful picture of life in the future, with microprocessors carrying out just about everything you can think of. How long we will have to wait for it all to come about is not easy to say, but that it will, is close to certain. Chapter 2 moves on to using a system of the present, with VDU's, keyboards, etc. The illustrations are nice but they seem to disappear as we move into the book, being replaced by photographs of real systems and the usual factual diagrams. Chapters 3 and 4 form an introduction to the hardware. Both are well written and my only misgivings are whether they are necessary in such detail for someone just interested in the computing side of personal computing — even the power supply is mentioned. The ideal *introduction* should tell you what things do, how *you* can make them do it, and then, only after all of this has been mastered and someone has bought a micro-system, should the question how does *it* do it be answered.

Chapter 5 is the first on programming and talks very generally about the activity. After Chapter 5, the title of Chapter 6 is something of a shock. "BASIC" yes — but "BASIC AND APL"! The idea of discussing APL in an introduction unnerved me slightly, but the small taste that Rodnay Zaks has managed to give in three pages was very interesting. I'm still not convinced about APL being an alternative to BASIC as a beginners language but I'm still open to argument.

Chapter 7 is about business computing and is full of advice and common (?) sense. It draws the beginner's attention to the possibilities and the problems — mainly in the software.

The next three chapters are about selecting a business system and gives information on peripherals and complete systems. My only wish is that the information on each of the systems was longer.

Chapter 11, on the economics of a business system, is a little worrying and serves to make one think about whether a computer system is worth while. Both it and Chapter 12 on how to fail with a business system are too short.

The remainder of the book gives ways of obtaining further help — more useful in the States than this country at the moment — and a collection of useful appendices.

This is not the best imaginable introduction to personal computing but it is the best I have found to date. Every reader should get something from this book.

M.J.

MICROPROCESSORS — FROM CHIPS TO SYSTEMS

Rodnay Zaks, 1977, 416 pp.
(SYBEX, 5½ x 8½, £7.95)

This book is for people interested in the engineering aspects of microprocessors. The preface claims that "No preliminary knowledge of computers is required to read this book," and as far as I can determine this is as true as it can be in a book of 416 pages. The treatment is logical, methodical and yet easy to read. However, this is not a book to read if you only want to know about microprocessors in personal computer systems as it deals in too much detail with the actual functioning of the basic chips.

Chapter 1 deals with the usual introductory topics, but very well. There are some interesting notes on the history of microprocessors and Silicon Valley. Chapters 2 and 3 deal with the internal operation of a microprocessor and the various system components, e.g. RAM, ROM, PIO, etc. A comparative evaluation of microprocessors is presented in Chapter 4 and makes very

interesting reading even if you are not involved in selecting microprocessors — if you are, then it's *essential* reading! Chapter 5 describes how all the chips discussed in previous chapters are brought together to make a system.

After building a system it would be logical to do something with it. This is where quite a lot of microprocessor books are a "let-down", but Rodnay Zaks has included, in Chapter 6, an excellent collection of applications. He first classifies the uses of micros — and some readers will be surprised to find "computer systems" as a separate item. Then we have a front panel controller, a papertape reader/punch controller, etc., described in moderate detail, and four case studies: an urban traffic controller, a spark timing system, a microwave oven controller and a copier controller. All are worth reading.

Chapter 8 deals with programming — in one chapter! (I did say that this was a book for engineers.) However the treatment is surprisingly good for so few pages. Finally, the last two chapters deal with development systems and the future of microprocessors and round the book off nicely.

This is a book that I can recommend without reservation to the *right* people. It joins my list of best books.

M.J.

MICROPROCESSOR LEXICON — ACRONYMS AND DEFINITIONS

The Staff of SYBEX, 1978, 110 pp.
(SYBEX, 4¼ x 5½)

A handy little pocket book of acronyms, definitions, microprocessor code numbers, S100 bus definition RS232C pin definition, IEEE488 bus definition, microcomputer manufacturers, microprocessor manufacturers and a few other things. The main part of the book consists of definitions and acronyms. It is well done and easy to use. I have found no major omissions.

I found the listing of microprocessors and support chips by number fascinating — but I'm not sure how useful it will be in the future.

It would be nice to have an ASCII code table and a few of the other pieces of information that a working programmer finds useful. However if you are having jargon trouble and can't wait until PCW's BUZZWORDS reaches Z then buy this book.

M.J.

BASIC For Beginners:

Brian Kavanagh (Holmes McDougal, £2.95)

Every schoolchild knows the difference between books, which are read for pleasure, and text-books, which are not. That is, they're not read in the conventional manner; starting at one end and proceeding, in an orderly manner, to the other. Text-books are used without reading most of what the author has written. You simply do the questions Teacher set you and that's it, most of the time.

BASIC for Beginners is unashamedly a text-book, aimed at the unfortunate 15/16 year old. The author, in common with most writing in this field, alternately assumes too much and too little previous knowledge on the part of the reader, which, at times makes him both patronising and baffling. However, since few will read his efforts, that doesn't really matter — does it?

On the whole, though, it's an instructive book. The large number of example programs are taken from actual hard copy, giving it a realistic feel; and are an added bonus if your pupils don't have access to a real computer. Arithmetic is kept very simple throughout, the emphasis being on programming techniques and methods. These are covered comprehensively, from LET statements through to relatively complex matrix operations. You ought to be able to write fairly useful programs by the end of it.

Certainly a book worth having around the classroom, but not intended for personal use.

David Bannister



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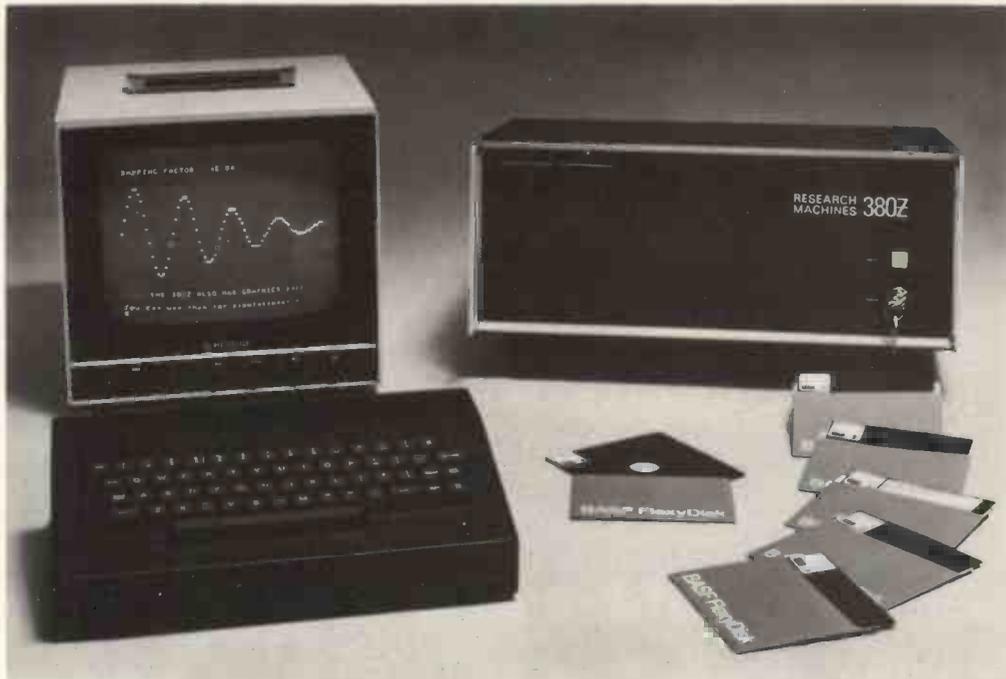
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Versions of BASIC are available with the 380Z which automatically provide controlled cassette data files, allow programs to be loaded from paper tape, mark sense card readers or from a mainframe. A disk BASIC is also available with serial and random access to disk files. Most BASICs are available in erasable ROM which will allow for periodic updating.

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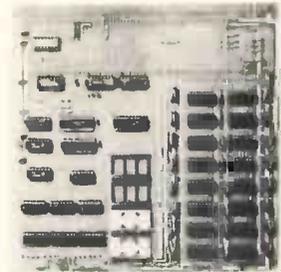
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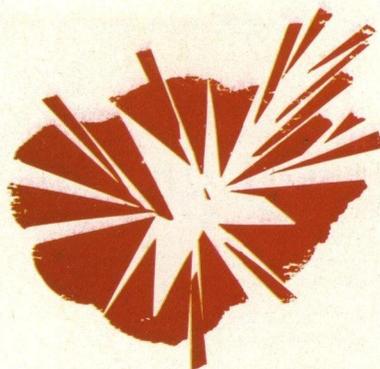
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MINEFIELD



Scott Bell and Simon Dowson

The Game

Like many computer games, 'Minefield' is played upon a board or grid. The object of the game is to cross the minefield from square 0,0 to square 9,9 without stepping on a mine. The mines themselves are invisible to the player and the only clue as to their whereabouts is given just before each move, when you are informed of how many mines there are immediately around you.

To make the game a little more difficult there are a number of rocks scattered randomly about the minefield. Unlike the mines, these rocks can be seen and the player is not permitted to enter these squares and must move around them in order to continue.

Should you take more than 20 moves whilst crossing the minefield you will be told that the batteries in your mine detector have become exhausted and that all subsequent moves must be made blindly, i.e. no

more warnings of the mines around you will be given.

When you reach square 9,9 or have been blown up, you can if you wish, see a printout of the board showing your route and the positions of the mines. Your path through the minefield is marked so that if you get into difficulties you can backtrack into some safe squares, but be warned, your number of goes is totalling up all of the time. If you have stepped on a mine, your last position will be marked with a 'B'.

If you decide to play another game, a new minefield is produced with the mines and rocks in different positions.

Getting Down to Basics

The program takes up between 5-6 kilobytes of memory when the array and all variables have been set up. By removing the instructions and leaving the bare minimum, the program can be made to run in 2-3 kilobytes.

Only one array, A(11,11), is used and this stores the board information. The array is dimensioned larger than the minefield to allow for attempted moves off the board. The positions of the rocks and the mines are entirely random except that squares (0,0) and (9,9) are always kept clear.

To make the game easier or more difficult, the number of rocks or mines may be altered by changing the FOR — NEXT loops associated with that particular routine.

The program should run on most machines which support BASIC with a few minor changes. For the CBM 'PET 2001', the randomize statement should be omitted, 'RND' changed to 'RND(1)' and 'LEFT(A&,1)' changed to 'LEFT&(A&,1)' etc.

Care should be taken to ensure correct punctuation in the routine that prints out the board. Other than that the program is fairly straightforward

```

10 PRINT
20 PRINT "MINEFIELD"
30 PRINT "-----"
40 PRINT "YOU ARE IN SQUARE (0,0)."
50 PRINT "YOUR OBJECTIVE IS TO CROSS THE MINEFIELD AND"
60 PRINT "REACH SQUARE (9,9) IN ONE PIECE!!!!"
70 PRINT "A NUMBER OF MINES HAVE BEEN PLANTED, BUT"
80 PRINT "YOU WILL NOT BE ABLE TO SEE THEM"
90 PRINT "ALSO THERE ARE A FEW ROCKS SCATTERED ABOUT"
100 PRINT "THESE SQUARES ARE OFF LIMITS"
110 PRINT "BEFORE EACH MOVE A WARNING WILL BE GIVEN"
120 PRINT "OF THE NUMBER OF MINES IMMEDIATELY AROUND YOU."
130 PRINT "BUT YOU WILL NOT BE GIVEN THE POSITIONS."
140 PRINT "IF YOU EXCEED 20 MOVES THEN YOU WILL NO"
150 PRINT "LONGER BE GIVEN THE WARNING"
160 PRINT "YOU MAY MOVE IN ANY DIRECTION EXCEPT"
170 PRINT "DIAGONALLY."
180 PRINT "COMMANDS ARE 'UP', 'DOWN', 'LEFT' OR 'RIGHT'"
190 PRINT "PRINT 'GOOD LUCK' . . . ."
200 RANDOMIZE
210 DIM A(11,11)
220 MAT A=ZER:Z=0
230 CLEAR
240 REM**SET UP ROCKS**
250 FOR I=1 TO 10
260 K=INT(9*RND+1):J=INT(9*RND+1)
270 IF A(K,J)=6 THEN GOTO 260
280 IF A(1,1)=6 THEN A(1,1)=0:GOTO 260
290 IF A(10,10)=6 THEN A(10,10)=0:GOTO 260
300 A(K,J)=6:NEXT I
310 REM**SET UP MINES**
320 G=0:N=0
330 FOR I=1 TO 15
340 K=INT(9*RND+1):J=INT(9*RND+1)
350 IF A(K,J)=1 THEN GOTO 340
360 IF A(1,1)=1 THEN A(1,1)=0:GOTO 340
370 IF A(10,10)=1 THEN A(10,10)=0:GOTO 340
380 IF A(K,J)=6 THEN GOTO 340
390 A(K,J)=1:NEXT I:J=1:A(K,J)=2:A(10,10)=5
400 REM**START OF GAME**
410 GOTO 670
420 PRINT "MOVE NO. 'G+1: INPUT' . . . WHICH DIRECTION";A$:T=0
430 IF LEFT(A$,1)="U" THEN J=J+1:T=3:GOTO 480
440 IF LEFT(A$,1)="D" THEN J=J-1:T=4:GOTO 480
450 IF LEFT(A$,1)="L" THEN K=K-1:T=5:GOTO 500
460 IF LEFT(A$,1)="R" THEN K=K+1:T=6:GOTO 500
470 PRINT "COMMANDS ARE UP, DOWN, LEFT OR RIGHT." GOTO 420
480 IF J<1 THEN J=1:GOTO 570
490 IF J>10 THEN J=10:GOTO 570
500 IF K<1 THEN K=1:GOTO 570
510 IF K>10 THEN K=10:GOTO 570
520 IF A(K,J)=6 AND T=3 THEN J=J-1:GOTO 590
530 IF A(K,J)=6 AND T=4 THEN J=J+1:GOTO 590
540 IF A(K,J)=6 AND T=5 THEN K=K-1:GOTO 590
550 IF A(K,J)=6 AND T=6 THEN K=K+1:GOTO 590
560 G=G+1:GOTO 600
570 PRINT "STAY ON THE MINEFIELD, COWARD!!!"
580 GOTO 420
590 PRINT "YOU CAN'T MOVE INTO A SQUARE WHERE THERE ARE ROCKS." GOTO 420
600 IF T=3 THEN A(K,J-1)=4
610 IF T=4 THEN A(K,J+1)=4
620 IF T=5 THEN A(K-1,J)=4
630 IF T=6 THEN A(K+1,J)=4
640 IF K=10 AND J=10 THEN 1000
650 IF A(K,J)=1 THEN A(K,J)=7:PRINT "BOOM!!!! YOU'RE DEAD" G0
660 A(K,J)=2
670 REM**DETECTS IF ANY MINES AROUND YOU**
680 V=0
690 FOR A=K-1 TO K+1
700 FOR B=J-1 TO J+1
710 IF A(A,B)=1 THEN V=V+1
720 NEXT B
730 NEXT A
740 REM**PRINT BOARD**
750 FOR A=10 TO 1 STEP -1
760 PRINT "-----"
770 PRINT A-1
780 FOR B=1 TO 10
790 PRINT " "
800 IF A(B,A)=0 THEN AS=" "
810 IF A(B,A)=1 THEN AS="M"
820 IF A(B,A)=1 AND Z=1 THEN AS="M"
830 IF A(B,A)=4 THEN AS="*"
840 IF A(B,A)=7 THEN AS="B":N=1
850 IF A(B,A)=2 THEN AS="V"
860 IF A(B,A)=5 THEN AS="H"
870 IF A(B,A)=6 THEN AS="R"
880 PRINT AS:NEXT B:PRINT " " :NEXT A
890 PRINT " 0 1 2 3 4 5 6 7 8 9 "
900 PRINT " 0 1 2 3 4 5 6 7 8 9 "
910 IF A(K,J)=5 THEN GOTO 1030
920 IF G<20 THEN GOTO 970
930 PRINT "THE BATTERIES IN YOUR MINE-DETECTOR"
940 PRINT "ARE EXHAUSTED"
950 PRINT "YOU WILL HAVE TO NAVIGATE BLINDLY"
960 PRINT "FROM NOW ON HA HA HA"
970 IF N=1 THEN GOTO 1060
980 IF G<20 THEN PRINT "THERE ARE 'V' MINE(S) AROUND YOU."
990 GOTO 420
1000 PRINT "WELL DONE. . . . WOULD YOU LIKE TO SEE"
1010 INPUT "YOUR ROUTE AND WHERE THE MINES WERE";A$
1020 IF LEFT(A$,1)="V" THEN Z=1:GOTO 740
1030 PRINT "IT TOOK YOU 'G' MOVES AS WELL."
1040 INPUT "ANOTHER GAME?";B$
1050 IF LEFT(B$,1)="Y" THEN GOTO 210
1060 PRINT "O.K. THEN. . . GOOD-BYE":GOTO 1100
1070 PRINT "HARD LINES, WOULD YOU LIKE TO SEE":GOTO 1010
1080 PRINT "THE LETTER 'B' IS WHERE YOU STOOD"
1090 PRINT "ON A MINE." GOTO 1030
1100 END

```

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The kit is complete, all that is required is a power supply a domestic T.V. and a domestic cassette recorder.

POWER SUPPLIES

There are two power supplies available, a 3 amp supply which will power the basic kit and some expansion and an 8 amp supply with toroidal transformer which will power a very large system. Both supplies can be mounted in the vero frame.

- 3 amp P.S.U. kit..... **£26.46**
- 8 amp P.S.U. kit..... **£64.80**

EXPANSION

Nascom I is expanded by connection to a buffer board which creates a 77 way bus structure "NASBUS" into which expansion boards plug directly. The bus structure is carried along a motherboard which allows future boards to be added and to keep your computer neat the Nascom I, power supply, buffer board, mother board and expansion boards can all be mounted in a vero frame.

- Buffer Board..... **£35.10**
- Mother board..... **£10.26**
- Mini Motherboard..... **£3.13**
- Vero frame..... **£31.86**

NASBUS

The 77 way Nasbus has the following advantages:—

1. Uses standard Veroboard as a motherboard and Standard 0.1 single sided edge connectors for expansion cards. These components are readily and cheaply available.
2. The bus structure leaves 8 spare data lines and 4 spare address lines for future use of 16 bit processors.
3. The power lines are regulated, on board regulators are therefore not needed which obviates the necessity for fan assisted cooling.

All prices include VAT and Carriage.

4. All cards use lower power, low noise shottky buffering which means the bus is quiet and does not need sophistications like active termination or interleaved ground planes.
5. Expansion boards are standard 8" x 8" vero DIP boards which are economic and give a good useable area.

MEMORY

The memory expansion board can carry 16 dynamic RAM chips, these can be either 4K bit or 16K bit chips and the board is offered with 8, 16 or 32K bytes of RAM. The 16K board can be expanded to 32K by plugging in 8 more 4116 chips.

The memory expansion board also has room for 4 2708 UVEPROMS each of 1K bytes and a lot of pre-programmed systems software is available to fit these sockets.

- 8K RAM board kit..... **£91.80**
- 16K RAM board kit..... **£151.20**
- 32K RAM board kit..... **£216.00**
- Set 8 x 4116..... **£75.60**
- Additional 2708..... **11.34**

INPUT/OUTPUT

For people wanting to use more peripherals than the standard kit allows for, Nascom are producing an I/O board which can carry a counter timer chip and a number of PIO's and UARTS. This will be available in March.

- I/O board..... **£37.80**
- CTC..... **£8.64**
- UART..... **£5.94**
- PIO..... **£8.64**

BASIC

To allow high level language programming Nascom have produced a 2K Tiny basic and a 3K Super Tiny Basic in 2 or 3 2708 EPROMS respectively. Also available is an 8K Microsoft precision floating point basic in 8 2708's which will be available in April on a single 64K bit ROM to fit the EPROM board.

- Tiny Basic..... **£27.00**
- Super Tiny Basic..... **£37.80**
- 8K Basic (8 x 2708)..... **£108.00**
- 8K Basic (ROM)..... **£43.20**

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Graphics board..... **£102.60**

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Nasbug T4..... **£27.00**

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- Zeap (tape)..... **£32.40**
- Zeap (Eprom)..... **£48.60**
- Letter Editor..... **£75.60**

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In the near future a mini-floppy disk system will be available with either single or double drive. These will probably offer in excess of 1/2 a megabyte and 1 megabyte respectively at prices that will allow even the hobbyist to have a large data base. To take full advantage of the business and scientific uses opened up by disks Nascom intend to release several high level languages. Looking further forwards Nascom is a developing product, and the fact that many thousands are now in use will ensure that the latest in computer technology will be available at a competitive price.

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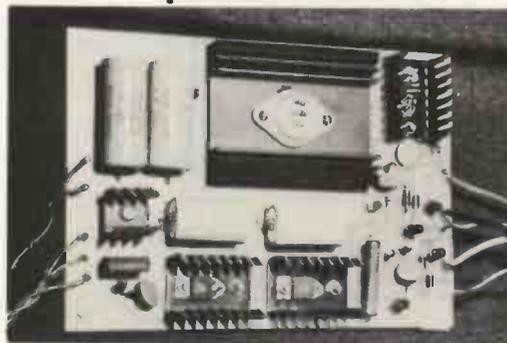
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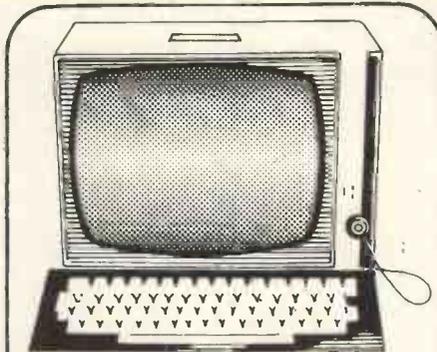


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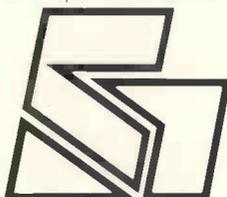
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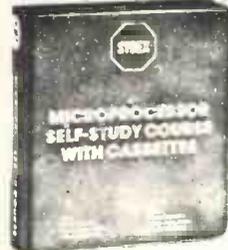
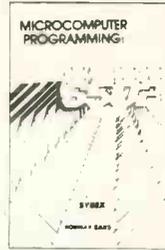
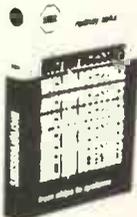
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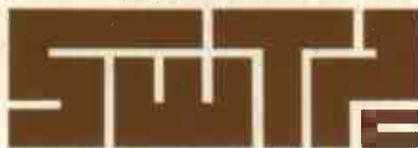
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