

## POWER PACKED - by POWERTRAN

Powertran's black boxes are packed with punch. Not only are they superb kits to buy and build they really do the job! Imaginative and ingenious design goes hand in hand with top quality materials and outstanding performance capability. With their smart black styling the kits harmonise visually as well as musically.
You can build each unit independently for its set task and then gradually increase your array until you have a complete bank of formidable controllable power.


Complete Kit $-\mathbf{£ 4 9 . 9 0}+$ VAT

MPA 200 - is a low price. high power 100W amplifier its smart styling. professional appearance and pertormance. make $t$ one of our most popular designs Adaptable inputs mixer accepts a variety of sources yet straightforward constructoon makes it ideal for the first-time builder


Complete Kit $-\mathbf{£ 1 7 5 . 0 0}+$ VAT


Complete Kit - £64.90 + VAT

Chromatheque 5000 - a 5 -charinel lighting system powerful enough for professional discos yet controllable for home effects Sound to light. strobe to music level, random or sequential effects - each channel can handle up to 500 W yet minimal wiring is needed with our unique single board design

ETI Vocoder - 14 channels, each with independent level control, for maximum versatility and imtelligibility. two input amplifiers - speech, external - each with level and tone control The vocuder is a powerful yet flexible machine that is interesting to build and, thanks to our easy to follow construction manual, is within the capability of most enthusiasts

## STOP PRESS: NEW FROM POWERTRAN DESTINY Modular Mixer AS BEING FEATURED

IN THIS MAGAZINE!


This versatile modular mixer, featured as a constructional article in this magazine can be built up to a maximum of 24 inputs, 4 outputs and an auxiliary channel. Each input channel has Mic and Line inputs, variable gain, bass and treble controls and a parametric middle frequency equalizer. There are send and return jacks, auxiliary, pan and fader controls and output group switching. The output channels have PPM displays and record and studio outputs. The auxiliary channel also has a PPM display and there is a headphone monitor jack and a built-in talk-back microphone. The mixer modules plug into base units each of which takes up to 6 channels. To eliminate hum, the power supply is in a separate cabinet.

|  | Kit Prices: |  |  |
| :--- | :--- | :--- | :--- |
| Input channel | $\mathbf{£ 1 9 . 9 0}$ | Base unit and wooden front | $\mathbf{£ 2 7 . 5 0}$ |
| Output channel | $\mathbf{£ 1 8 . 5 0}$ | Pair of mahogany end cheeks | $\mathbf{£ 1 2 . 5 0}$ |
| Auxiliary channel | $\mathbf{£ 2 2 . 5 0}$ | Power Supply and cabinet | $\mathbf{£ 1 9 . 5 0}$ |
| Blank Panel | $\mathbf{£ 3 . 0 0}$ | All prices are VAT exclusive |  |

## Quite simply the best way to make music



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## PRACTICAL <br> ELECTRONICS

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## COMPUTER CORNER

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## Unicase

Over the years ILP has been aware of the need for a complete packaging system for it's products, it has now developed a unique system which meets all the requirements for ease of assembly, adaptability, ruggedness, modern styling and above all price.
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Our power slaves, which have numerous uses i.e instrument, discotheque, sound reinforcement, feature in addition to the hi fi series, front panel input jack, level control, and a carrying handle. Providing the smallest, lowest cost, slave on the market in this format.


in

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| HIFI Separates |  |  |  |  | $\begin{aligned} & \text { Price inc. } \\ & \text { VAT } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| UC1 | Preamo |  |  |  | £29.95 |
| LP1X | $30+30 W / 4-8 \Omega$ | Bipolar | Stereo | $\mathrm{H}_{1} \mathrm{~F}_{1}$ | $£ 54.95$ |
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| UP7X | 120W/4-8 | MOS | Mano | HiF | £84.95 |
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| US2X | $120 \mathrm{~W} / 4 \Omega$ | Bipolar | Power | Slave | ¢79.95 |
| US3X | $60 \mathrm{~W} / 4-8 \mathrm{~S}$ | MOS | Power | Stave | ¢69.96 |
| US4X | $120 \mathrm{~W} / 4-8 \Omega$ | MOS | Power | Slave | $£ 89.95$ |

Piease note $x$ in part mumber denotes mains voltage. Please insert $O$ in place of $X$ for 110 V . ' ' in place of $X$ for 220 V (Europe), and ' 2 ' in place of $X$ for 240 V (U.K.) Alt units except UCI incorporate our own toroidal transformers.

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THINK OF THE POSSIBUITIES The KIT THINK OF THE POSSIBILITIES. The KIT includes all PCBs and components for one transmitter and two receivers, plus a drilled Order Xki12
der as Xkil2.

## ELECTRONIC LOCK KIT XK101

This KIT contains a purpose designed lock IC io-way keyboard, PCB and all components to construct a Digital Lock, requiring a 4 -key sequence to open and providing over 5000 different combinations. The open sequence may be easily changed by means of a preswired plug. Size: $7 \times 6 \times 3 \mathrm{cms}$. Supply: 5V to 15 V dc. at 40 uA . Ouput: 750 mA max. Hundreds of uses for doors and garages, car antitheft device, electronic equipment, etc. Will drive most relays direct. Full instructions supplied

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sequence, speed of sequence
and frequency of direction and frequency of direction
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The kit comprises a mains powered receiver, a lour button transmitter. complete with ore drilled box, requiring o 9 V battery and one
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and off at preset times over a 7 day cycle egg. 10 control your central FEATUR

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Day of week, am/pm and output status indicators. 4 zero voltage switched mains outputs. Battery backup saves stor Display blanking during po
18 programme time sets 18 programme time sets
Powerful "Everyday" function enabling output to switch every day but use only one time set. Useful "sleep function-hurns on output tor one hour immediately or after a specified time interval. 20 function keypad for programme entry
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(Kit includes all components, PCB, assembly
and programming instructions). ORDER AS CT5000

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latched, momentary or "break beam" receiver. Operates from 6.13 d d
MK 18 HIGH POWER
MK 18 HIGH POWER IA TRANSMITTER
Similar to MKS
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Opto-isolated with zero voltage switching, No
MK 15 DUAL LATCHED SOLD STATE RELAY
MK 15 DUAL LATCHED SOLID STATE RELAY
Comprises $2 \times$ solid state relays and latch for
66.20

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Switches any appliance up to 1 kW
on and off at present times once per CT 1000 K Basic Kit
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- 5 push button
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- 6 watt output - Ready etched
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aligned push button tuning unit
£12.95
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Suitable stainless steel fully retractable aerial (locking) and
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 To boost your car radio or radiocassette to $15 W$ r.m.s. per channel. £9.95 + £1.50 p\&

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Ideal for Church
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ACCESSORIES: Suitable mains power supply kit with
transformer: $£ 8.00$ plus $£ 2.00$ p\&p.
Suitable LS coupling electrolytic: $£ 1.00$ olus $\mathbf{2 5 0}$ p\&p.


SPECIFICATIONS
Max. output power (RMS): 125W.
Operating voltage (DC): 50-80 max
Loads: 4-16 ohms.
Frequency response measured @ 100 watts: $25 \mathrm{~Hz}-20 \mathrm{KHz}$. Sensitivity for 100 watts $400 \mathrm{mV} @ 47 \mathrm{~K}$.
Typical T.H.D. @ 50 watts, 4 ohms: $0.1 \%$
Dimenstons: $205 \times 90$ and $190 \times 36 \mathrm{~mm}$.

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- Positive $\&$ negative voltage with an FSD of - Positive \& negative voltage with an
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With this fully buitr and calibrated module a wide range of accurate equipment such as multimeters. details are supplied for extending the voltage range, measuring current, resistance and temperature Fully guaranteed, the unit has been supplied to electricity buthorities. Government departments, atc.

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leatuch mow mode offers all the possible reatures likely to be required when building an 2 magnetic switches or in conjunction with several ultrasonic alarm modules or infrared units, a reaily effective system can be constructed at a fraction of the cost of comparable ready-made units. Supplied with a fully explanatory Data Sheet that makes installation straight forward. the module is fully rested and guar anteed.

- available in kit form $£ 16.95$ plus VAT
-Stabilised output voltage
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Produces a loud and penetrating sliding tone opera ing from 9.15V. Capable of driving 2 off 8 ohm speakers to SPL of 110 db at 2 M Contains an inhibit facility for use with shoo lifting toops or other break to activate circuits.

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# Alexandra Pavilion London November 18-211982 The biggest and best event ever to be staged for the electronic hobbies enthusiast! 

Walk into a whole world of electronic equipment - Everything from resistors, IC's to home computers, transmitting and receiving units, citizens band radio and peripheral equipment, video games, musical instruments, radio control models. . . In fact whatever your particular electronic hobby you'll find this show will be the most interesting and informative wav to discover all the latest developments in your particular field.
Other attractions will include radio and TV transmission, electric vehicles, radio controlled models, and demonstrations by local and national organisations.
This is the age of the train - British Rail are offering a cheap rate rail fare from all major
stations in the country direct to Alexandra Palace - a bus will be waiting on your arrival to take you to the show. Iicket price also includes admission to the exhibition - so let the train take the strain to the Electronic Hobbies Fair.
Ticket prices at the door are $\boldsymbol{\Sigma 2}$ for adults, $\mathcal{E 1}$ for chlidren but party rates are available for 20 people or more. To find out more, contact the Exhibition Manager, Electronic Hobbies Fair, IPC Exhibitions, Surrey House, 1 Throwley Way, Sutton, Surrey SM1 400. Tel: 01-643 8040.

Electronic Hobbies Fair is sponsored by Practical Electronics, Everday Electronics and Practical Wireless and is organised by IPC Exhibitions Lta.

OPENING TIMES Thursday 18 Nov. - 10.00-18.00 Friday 19 Nov. $-10.00-18.00$ Saturday 20 Nov. - 10.00-18.00 Sunday 21 Nov.-10.00-17.00
E.H.F. JUST one last reminder re. Electronic Hobbies Fair (November 18th to 21 st Alexandra Pavilion), this will be the best event ever for the hobbyist in this country. Just about all the top names in the retail supply business will be theresome are arranging special offers for the Fair, our own 50p off coupon is on the opposite page. In addition to the trade stands there will be a number of special attractions; like the Luxor satellite TV receiver mentioned last month; a display of electric vehicles built by members of the Battery Vehiole Society (more about them later); a demonstration of holography by Holographic Developments (you will be able to purchase some examples); some working radio controlled models; an exhibit by the Royal Signals and an amateur radio talk-in station operating on the 2 m band, channel S 22 ( 145.55 MHz ).

You will be able to try out computers have a go at the latest video games and much, much more. There will be stands representing clubs and organisations-like the RSGB-and plenty to buy.

On the PE stand Editorial staff will be waiting to meet you and discuss the
various projects on display. Among other things we will be showing Micrograsp, Microsynth, Microcontroller our Semi-Professional Mixing Desk, Ultimum and one or two future projects. The other sponsoring magazines PW and EE will have similar stands and the following IPC magazines will also have a presence at the Fair; Practical $\mathrm{Hi}-\mathrm{Fi}$, Television, Wireless World, Practical Computing, Your Computer, and CB World.

## ACCESS

Access to the show is easy-there's plenty of car parking and a park-andride bus. The Victoria and Piccadilly lines provide fast access to and from the West End and British Rail main line stations-King's Cross, St. Pancras, Euston and Victoria. Finsbury Park and Wood Green underground stations are linked to Alexandra Pavilion by the London Transport W3 bus service which runs every 7 to 10 minutes on all the Fair days. Also Alexandra Palace British Rail station will be linked to the show by a free bus shuttle service; this station is close to Wood Green underground station and is on the $B R$ main and suburban lines from King's Cross and Moorgate.

Special fares are available from all
major British Rail stations direct to Alexandra Palace station and ticket price will include admission to the show-over 300 stations in the U.K. can provide access to Alexandra Palace with only one change of train. Through tickets to BR Alexandra Palace are available at underground ticket offices.

## B.V.S.

Finally, a word about the Battery Vehicle Society. The B.V.S. was foundied in 1973 to promote battery alectric vehicles in all their forms and to provide a forum for everyone interested in this form of transport. The Society publishes a monthly magazine, Battery Vehicle Review, containing articles on the history, development and use of battery vehicles.

Following the 1979 Lucas 'How far can you get" competition for design and construction of lightweight electric vehicles, the B.V.S. competition sectimon has monthly runs where the creations of members challenge each other to make the best of 56 lbs of lead/acid battery. Some of these vehicles will form the special B.V.S. display at Electronic Hobbies Fair-see you there.


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[^1]
## Back Numbers

Copies of most of our recent issues are available from: Post Sales Department (Practical Electronics), IPC Magazines Ltd., Lavington House, 25 Lavington Street, London SE 1 OPF, at $£ 1$ each including Inland/Overseas p\&p. Please state month and year of issue required.

## Binders

Binders for PE are available from the same address as back numbers at $£ 4.60$ each
to UK or overseas addresses, including postage and packing, and VAT where appropriate. Orders should state the year and volume required.

## Subscriptions

Copies of PE are available by post, inland or overseas, for $£ 13.00$ per 12 issues, from: Practical Electronics, Subscription Department, Oakfield House, Perrymount Road, Hayward Heath, West Sussex RH 16 3DH. Cheques and postal orders should be made payable to IPC Magazines Limited.

Items mentioned are available through normal retail outlets unless otherwise specified. Prices correct at time of going to press.

## Now is the Winter for Public Debate'

Both the IBA and the BBC are concerned about the affects unregulated cable TV could have on the standard of British Broadcasting. The Independent Broadcasting Authority has called for a winter of public debate on the expansion of cable and satellite broadcasting. After its first Autumn meeting the IBA made the following statement.
-The Independent Broadcasting Authority recognises the Government's commitment to the establishment of a national information grid through the expansion of broadcasting in the United Kingdom; and it is eager to use its many years of experience to contribute to the opportunities presented by this expansion of communications in the 80s while maintaining the high standards of British broadcasting. The unique quality of output which has earned a world-wide reputation for British programme-makers must not be eroded.
'The proposals of the Hunt Committee will be crucial to the expansion of broadcasting. Mistakes made now would take years to correct. It is for this reason that the Authority calls for a winter of public debate before the final decisions are taken. The Authority has no wish to delay the changes which clearly are on the way-on the contrary, the Authority believes that the creation of Channel Four was far too long delayed-but it believes that it is crucial to lay down the best possible framework for new developments and to ensure that meeting the challenge of wider choice need
not mean lower standards."
Meanwhile the BBC in its evidence to the Hunt Committee said that unregulated cable TV would be "socially divisive, sacrifice hard won programme standards and coarsen popular taste". It also warns that it might lead to the disappearance of big sporting events such as the FA Cup Final and the Olympic Games from BBC and ITV screens because the BBC says cable operators concentrating their resources on 'blockbuster' attractions might well be in a position to outbid the BBC and ITV in the areas of sport and entertainment, thus posing the public service broadcasters with a cruel dilemma. "They must either commit a disproportionate amount of their resources to matching the bids of the cable operators-thus impoverishing other areas of programming-or see the majority deprived of such star attractions in favour of a paying minority". The BBC also pointed out that perhaps no more than $50 \%$ of British viewers will have access to the proposed cable systems and that individuals will have no power to affect the issue because access will be determined by economic or geographical status.

## POWER MODULE

The C15 mono power booster amplifier from ILP is designed to increase the output of any in-car entertainment system to a nominal 15 W r.m.s. The amplifier is encapsulated into an integral heatsink making it a very compact, robust unit.


The system features automatic supply switch-on which is activated when the radio or cassette is turned on. It also has a selectable input level facility so it can be driven from either the low signal levels of a pre-amp or straight from the existing units speaker leads. If stereo operation is required then two units can be used.

Priced at $£ 9: 14$ inclusive of VAT and $p \& p$ the C15 is available from ILP Electronics Ltd., Graham Bell House, Roper Close, Canterbury, CT2 7EP (0227 54778).

## AVO2000

A new British design concept in handheld digital multimeters-for a wide range of electrical maintenance, field servicing and vehicle testing applications-has been launched by THORN EMI Instruments Limited.

With the AVO 2000 Series the company has concentrated on providing a design offering a host of 'ease-of-use' features.

Initially, the AVO 2000 Series comprises three instruments for specific applications: the AVO Digiminor 2000; the AVOmeter 2001 and the AVO Vehicle Test 2002.

Each is housed in a tough ABS case and fitted with non-slip safety pads, the important new features of all three instruments include: Direct entry prods-giving true one-hand operation; A $3 \frac{1}{2}$ digit l.c.d. readout at the
base of the housing: Positive action slide switching with dustproof, positive range selection; Improved safety, with fully shrouded plugs for the lead set; and a three-position stand-the instrument can be used in the hand, on a bench or while hung from a hook.

Ideally suited to maintenance applications, the Digiminor 2000 incorporates a special buzzer socket for sim-

ple continuity testing without reference to the display.

The AVOmeter 2001 is designed primarily for field servicing applications. Featuring more comprehensive ranges than the Digiminor 2000, it ensures correct mode and range selection by the inclusion of an audible alarm which signals any discrepancy. Both the unit and mode of measurement are displayed on the l.c.d.

The AVO Vehicle Test 2002 is unique: it is the first digital multimeter of its kind designed specifically to simplify the testing of electrical circuits of any road vehicle from a small saloon car to HGV.

The AVO Digiminor 2000 is priced at $\mathbf{£ 6 9 . 4 0}$, the 2001 at $£ 85.40$ and the 2002 at $£ 97 \cdot 00$. Each multimeter is supplied with the appropriate lead sets, battery and operating instructions.

Thorn EMI Instruments Ltd., Archcliffe Road, Dover, Kent 10304 202620).

## CAPACITANCE METER

The Metertech model MT301 is a low cost hand held digital capacitance meter which is battery operated with a $3 \frac{1}{2}$ digit liquid crystal display capable of measuring

capacitance values from 0.1 pF to $2000 \mu \mathrm{~F}$ over 8 push button ranges.

The unit is priced at $£ 69$ and is available from Centemp Instrument Co., 62 Curtis Road, Hounslow, Middlesex (01-894 2723).

## ENERGY SAVER

The Velleman Heating Controller is designed to control the temperature inside offices, factories, houses etc., enabling central heating systems to work more economically.

It provides a 4 program daily cycle controlling the temperature at any given period. The programs are totally independent and therefore it is possible to select day and night temperatures separately.

The display functions as a clock as weil as a thermometer with the device replacing conventional mechanical thermostats without additional wiring. The unit can be manually over-ridden at any time without disturbing any of the preselected programs.

The system is available in kit form ( $£ 75.00$ ex VAT) and also as a built and tested unit.

Velleman (UK) Limited, P.O. Box 30, St. Leonards on Sea, East Sussex, TN37 7NL. (0424 753246).


## CHIP LEG HAND TOOL

A simple hand tool that restores splayedout legs on integrated circuits to the correct spacings has just been introduced by Aries Electronics. Called the DIP-R-SIZER, the new tool can handle integrated circuits with either 0.300 in or 0.600 in leg spacing.

When manufactured, the legs on integrated circuits are often outside the tolerances specified for centre spacings. The nominal 0.300 in and 0.600 in centres have a maximum tolerance of +0.020 in , In practice a considerable proportion of integrated circuits leave the factory with spacings up to 0.095 in above the nominal centre spacing. Particularly with high pin-count devices, attempts to insert out-of-tolerance legs into integrated circuit sockets or printed circuit boards often results in damage to the legs, the contacts in the socket or the holes in the printed circuit board,

The tool which has a pair of jaws hinged at one end is held open with a spring at the other. An anvil between the jaws is contoured to the correct angle and spacing for the integrated circuit legs. One side of the anvil takes $0 \cdot 300$ in centre devices while the other takes the 0.600 in size. To rectify splayed legs, the device is placed on the appropriate side of the anvil and the jaws squeezed lightly together. This presses the legs against the anvil, and brings them automatically into tolerance. While inten-

ded primarily for correcting leg spacings as received from the manufacturer, the tool can also be used to rectify legs put out of tolerance through mishandling. However, it cannot restore damaged devices where the legs have been displaced longitudinallythat is where the pitch between individual pins have been disturbed.

The tool which is priced at $£ 10.50$ including VAT and p\&p. is available from Aries Electronics (Europe) Ltd., Metrostore House, Eastways, Witham, Essex CM8 3YQ. (0376519318).

## SUPERSWITCH HOME COMMAND GENTRE

1 ite Superswitch Command Centre has been developed for the remote control of lamps and electrical appliances.

The unit which transmits high frequency coded signals along existing mains wiring is capable of controiling up to 16 appliances either manually or automatically. The centre can be pre-programmed up to 7 days in advance with a maximum of 24 programs.

The coded signals are received by modules which plug into the 13A socket outlets. Appliance modules operate electrical loads up to 13A whereas. lamp modules can control Tungsten lighting loads up to 400 W .

Other features of the unit include the manual dimming and brightening of lamps, battery back-up and the ability to turn on all lamps simultaneously. The Command Centre is priced at $£ 73.70$ with the appliance and lamp modules priced at $£ 24.00$ each.

Another Superswitch system which uses mains wiring is the Plug-In Intercom. This FM unit can plug into any 13A socket anywhere on a ring main, and send messages
using the mains wiring.
Up to 5 units can be used in conjunction with each other or a private conversation can be carried out between two units without the others on the system being able to hear. The intercom is priced at $£ 37.45$ per unit.

Superswitch, 7 Station Trading Estate, Blackwater, Camberley, Surrey.


## CHESS SENSOR

The CG1 Sensor Computer chess game from Systema has 8 levels and is priced under E3O. The unit measures only $175 \times 120 \times 47 \mathrm{~mm}$ and can be either battery powered for up to 50 hours from a standard PP3 or mains operated.

## Sensalite

An automatic light switch called Sensalite enables a room light to be automatically switched on when someone enters a room where lights are needed and then automatically switches the lights off when the room is vacated.

The unit operates by looking for movement and then at the prevailing lighting condition.


The unit has a built-in sensory board which is operated by pressing down on the piece you are moving, a light shows your 'from' position and pressing down the piece on your 'to' position. The computer then records your move and indicates its reply.
Other features include changeable levels during play, side changes during play, enpassant captures, castling and pawn promotion.
Systema (UK) Limited, 25 King's Road, Reading, Berkshire.


When the unit detects movement it checks the natural light level and, if required, switches on the light. The level at which the lights are energised can be set by the user.

Sensalite, a 100 mm cube which is linked into the existing lights has provision for an additional burglar alarm module.

The unit is priced at 585 including VAT. Leading Edge Technologies Ltd., 1-4 Kings Parade, Croydon, Surrey (01-6860255).

A new 16K RAM pack for the ZX81 which overcomes the "wobble" or disconnection problems associated with many add-on units is also available with a keyboard sounder as an optional extra. The sounder enables a faster entry of programs from the keyboard by giving an audible feedback when a key is pressed.

The RAM pack is priced at $£ 19.95$ and with a keyboard sounder is priced at $£ 24.95$.

Ground Control, Alfreda Ave, Hullbridge, Essex, (0702 2303 24).

## POINTS <br> ARISING . . .

COMBO AMPLIFIER (Sept. '82)
The following winding details should accompany L1 in Fig. 2.8: Three layers of ten turns each ( 30 turns total) should be wound using 18 s.w.g. enamelled copper wire. Resistor R13 should be 15 k . The drain and source annotations of TR8 and TR9 in Fig 2.1 should each be transposed.

## Anunldinunl...

Please check dates before setting out, as we cannot guarantee the accuracy of the information presented below. Note: some exhibitions may be trade only. If you are organising any electrical/electronics, radio or scientific event, big or small, we shall be glad to include it here. Address details to Mike Abbott.

Comper Nov. 16-19. Olympia. Z 1
Electronic Hobbies Fair Nov. 18-21. Alexandra Pavilion, London. Z1
INTRON Nov. 23-25. RDS Dublin, Ireland. V
BEX Bristol Nov. 24-25. Holiday Inn. K
Northern Computer Fair Nov. 25-27. Belle View, Manchester. Z1
Christmas Holography (+items for sale) Dec. 2-Mar. (1983) Light
Fantastic Gallery, London. A8
ElectroNORTH Dec. 7-9. Harrogate Supercenter. Q
IT82 (Information Technology Year Conf.) Dec. 8-9. Barbican. 0
Continuous exhibitions at the National Microprocessor \& Electronics Cntr. (nr. tower of London). Ll
Peripherals Feb 2-4 1983. Cunard Int. Hotel, Hammersmith, London. Z1
BEX Bournemouth Feb. 9-10 1983. The Pavilion. K
Microsystems Feb. 23-25 1983. West Cntr. Hotel, Fulham, London. Z 1
CAD North Mar. 1-3 1983. Belle Vue Ex. Cntr., Manchester. ZI
Mailing Efficiency Mar. 1-3 1983. Bloomsbury Cntr. Hotel, London. Z Local Networks Mar. 8-10 1983. Royal Lancaster Hotel, London. O

Laboratory Edinburgh Mar. 16-17 1983. Assembly Rooms, George St. E
Brighton Electronics March 1983. T
BEX Leeds Mar. 16-17 1983. Dragonara Hotel. K
INSPEX Mar. 21-25 1983. National Exhibition Cntr. Birmingham International. Z 1
Sensors \& Systems Mar. 22-24 1983. The Forum, Wythenshawe. T Compec Wales Mar. 22-24 1983. Cardiff University. Z1
ETM (Electronic Test/Measurement) Mar. 22-24 1983. The Forum, Wythenshawe, Manchester. T
Laboratory Manchester Mar. 23-24 1983. New Century Hall, Corporation St. E
American Holography Mar.-June inc. Light Fantastic Gallery, Covent Garden, London. A8
All Electronics Show April 19-21 1983. Barbican Cntr. London. E
Fibre Optics April 19-21 1983. Porter Tun Rooms, The Brewery (!),
Chiswell St., London EC1. E
International Materials Handling April 19-26 1983. Earls Court. I
International Packaging Exhibition April 25-29 1983. NEC B/ham. I

A8 Holographic Exhibitions $\mathbb{C} 01-8366423$
E Evan Steadman $\int 079922612$
K Douglas Temple Studios $\int 020220533$
L1 World Trade Cntr., Europe Ho., London E1
O Online 『 0927428211
Q Exhibitions For Industry $\int 088334371$
T Trident $\int 08224671$
Z BETA Exhibitions 601-4056233
Z1 IPC Exhibitions \& 01-6438040


## The Jupiter Ace uses FORTH

The Jupiter Ace personal computer runs in FORTH, an easily understood language, typically four times as compact and ten times as fast as BASIC. Before the Ace all personal computers used BASIC and FORTH was only available to a privileged few. The Jupiter Ace also features a full-size moving-key keyboard, high-resolution graphics, sound, floating point arithmetic, a fast and reliable cassette interface and 3 K of RAM.

## Available soon

## Plug-on parallel printer interface.

For around $£ 20.00$ this will connect your Jupiter Ace to anything from high-speed dot matrix to letter-quality daisy wheel printers.
Plug-on 16K Memory Expansion
For around $£ 30.00$ you will increase the memory of your Jupiter Ace to 19 K giving you instant access to enormous amounts of information.

## Software

A catalogue will be sent with every machines, and includes, initially, programs for education and entertainment.

## All inclusive <br> price

For £89.95 you receive

The manual is a complete introduction to the world of personal computing and a course in FORTH programming on the Ace.
Even if you are a complete
newcomer to computers, the
manual will guide you step by step
from first principles to confident
programming
The price includes postage packing
and V.A.T.
The Jupiter Ace is backed by a full 12 month warranty.

The Jupiter Ace is available only by mail order Please allow up to 28 days for delivery
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## Technical information <br> Hardware <br> Z80A running at $3.25 \mathrm{MHz}^{2}$ <br> $8 K$ bytes ROM

3K bytes RAM
Kayboard 40 Moving-key keyboard with auto repeat on every key and Caps Lock.
Screen Memory mapped 32 column $\times 24$ line flicker-free display with upper and lower case ascii character set.
Graphics Chunky graphics ( $64 \times 46$ pixels) may be plotted. unplotted or over-plotted (XOR operation). Also, the entire character set (128 characters and their video inverses) may be redefined allowing intricate shapes to be drawn with a resolution equivalent to $256 \times 192$ pixels. Sound Internal loudspeaker may be programmed to operate over the entire audio spectrum
Cassette Programs and data in the compact dictionary format may be saved, verified, loaded and merged. 8locks of memory can be saved. veriked, loaded and relocated. All tape files are named. Running at 150 C. 1 por rais and ful 780 Expansion Port Contains D.C. and control signals. May be used to connect extra memory and other peripherals. IN and OUT words allow port-based peripherais to be addressed.
Data Siructures Integer, Floating point and String data may be held as constants, variables of arrays with multiple dimensions and mixed data types. There ape no restrictions on names.
Control Structures IF-ELSE-THEN. DO-LOOP DO-+LOOP, BEGIN-WHILE-REPEAT. BEGIN-UNTIL, all may be mixed and nested to any depth.
The Jupter Ace closely follows the FORTH 79 standard with extensions for floating point, sound and cassette. It has a unique and remarkable editor that allows you to list and alter words that have been previousty compiled into the dictionary. This avoids the need to store screens of source. allowing the dictionary itself to be saved on cassette. Comprehensive erfor checking removes the worry of accidentally crashing vour programs.


## Designed by

 Jupiter CantabComputer Designers Steven Vickers and Richard Altwasser played a major role in creating the ZX Spectrum and then formed Jupiter Cantab to develop advanced ideas in personat computing. The Ace is the result, another all-British computer to lead
the world. all-British computer to lead
the world.


## HOW IT WORKS

The main i.c. being used is the 5024 top-octavegenerator, (also coded S50240 by Tandy). From a single frequency input of 2.0024 MHz it will produce thirteen semitones, equally tuned. This frequency is generated by the ast the multivibrator IC1a and $b$, adjustment being made by VR1. If the input frequency is halved, the 13 outputs will also halved, sounding an octave lower. Consequently IC2 (part of a 4013), is connected as a $\div 2$ divider which fds 1.0012 MHz into another 5024 to give another lower octave of notes. The 4013 is a dual D type flip-flop, and contains two identical circuits. If the data pin is connected to the $\overline{\mathrm{Q}} \mathrm{pin}$, and the set and reset pins are connected to earth it will divide the incoming frequency by two. See Fig. 2 for details. Thus half of the 4013 was still unused, and this can be utilised to divide the output of the multivibrator prior to entry into IC2b and IC3, giving the unit an octave-down shift. Originally IC1a and b fed IC2b and IC3 direct, but it was found during development that switching in the octave shift caused a slight shift in frequency, affecting the tuning, so IC1d was included to act as a buffer, and this cured the problem.

The outputs from the top-octave-generators are connected to the appropriate keys, (see Fig. 3) and selected by either of the stylii, with S2 selecting whether one or both of IC5 and 6 are connected to each stylus. R2 and R3 are included to make sure that the inputs of IC5 and 6 are grounded when not in use. These i.c.s further divide the frequencies to bring them into the required audio octave range. Four outputs of each can be selected by the switch bank S3-S6, being square waves from IC5 and triangular waves from IC6, the change in waveform shape being accomplished by the resistors R8-R15, and capacitors C2-C5.

If pin 12 of IC6 is taken as an example, a square wave comes out, but R8 controls the charging rate of C2, giving a slope to the leading edge of the square wave; and R12 controls the discharge rate, giving a slope to the trailing edge resulting in an approximate triangular waveform. None of these values are critical and constructors should experiment to find the most satisfactory result. Different values will affect the waveform shape and the amplitude (loudness) of each voice.

## TWIN PROBE STYLUS ORGAN




Fig. 4. PSU circuit diagram

-

## -

Fig. 6. PSU component layout (right)


The outputs can be switched in via S3-S6 and the result goes via the potential divider VR2 acting as a volume control to the audio amp. IC7, an LM380 2 watt i.c. If high frequency oscillation occurs, a Zobel network consisting of a 2.7 ohm resistor and a $1 \mu$ polyester capacitor in series from pin 8 to earth can be inserted, but this was not found to be necessary in the prototypes. However, space is made for these two components on the p.c.b.

The inctusion of a mains power supply may seem strange
to readers, but there are several reasons for it. IC3 and 4 require 11-16 volts, so the convenient PP range of batteries couldn't be used, and with the volume control turned up, the battery drain would be quite high. Also a mains powered regulated supply ensures a reliable voltage source, preventing frequency stability problems. Readers can, of course, omit the power supply and replace it with batteries, and it is for this reason that the power supply p.c.b. is separate.


Fig. 7. Stylochord p.c.b. (actual size)


Fig. 8. Stylochord component layout

## COMPONENTS

| Resistors |  |
| :--- | :--- |
| $R 1$ | 2 k 2 |
| $R 2, R 3$ | $100 \mathrm{k}(2$ off) |
| $R 4, R 7$ | $330 \mathrm{k}(2$ off $)$ |
| $R 5$ | 270 k |
| $R 6$ | 220 k |
| $R 8$ | 3 k 9 |
| $R 9$ | 4 k 7 |
| R10 | 6 k 8 |
| R11 | 8 k 2 |
| R12,13,15 | $68 \mathrm{k}(3$ off) |
| R14 | 47 k |
| R18 | $680 \Omega$ |
| $R 16$ | 10 k |
| R17 | 2.7 Ohm (see text) |
|  |  |
| Capacitors |  |
| C1 | 47 p ceramic |
| C2-C6 | 100 n polyester $(5$ off) |
| C7 | $220 \mu$ elect. |
| C8 | 100 n poly (see text) |
| C9 | $330 \mu$ elect 16 V |
| C10 | $1000 \mu$ elect. 25 V |
| C11 | 220 n polyester |
| C12 | $10 \mu$ elect. 16 V |


\section*{Potentiometers <br> | VR1 | 10 kmin horiz |
| :--- | :--- |
| VR2 | 5 klog | <br> Integrated Circuits <br> | IC1 | 4011 |
| :--- | :--- |
| IC2 | 4013 |
| IC3,4 | 5024 (S50240 Tandy) (2 off) |
| IC5,6 | 4024 (2 off) |
| IC7 | LM380 |
| IC8 | 7812 |}

## Miscellaneous

8 Ohm loudspeaker
0-12, 0-12V transformer (RS 196-303 for example)
Bridge rectifier (e.g. RS 262-141)
2 probes
6 off 2 pole latching push-button switches \SUE series $\left.\begin{array}{ll}8 \text { way bracket, } 15 \mathrm{~mm} \text { spacing } \\ 6 \text { knots ' } A \text { ' } 4 \text { red, } 2 \text { black) }\end{array}\right\}$ (AMBIT)
L.e.d. + Holder

Vero case (Order Code 75-1715G)
D.p.d.t. toggle switch

Knob
20 mm fuseholder and 500 mA fuse
P.c.b.s

Ribbon cable
Veropins, grommet, nuts and bolts etc.


Fig. 9. Keyboard printed circuit

## CONSTRUCTION

Readers are advised to use p.c.b.s, designs for which are given in Figs. 6 and 7, as this makes construction easier. There are quite a lot of interconnections to be made, and the prototype used ribbon cable, so that each wire is individually colour-coded and therefore easily traceable. Assemble the components, making sure that the i.c.s, diode, capacitors, and voltage regulator etc. are the correct way round. It is recommended that single-sided Veropins be used as solder terminals for all the wires.

The main p.c.b. and the power-supply p.c.b. are bolted to the base panel of the case, and the plastic housing is drilled to accept the cable retention grommet, fuseholder, speaker holes, switches, l.e.d., pot and probe sockets, see drilling details in Fig. 10.

The aluminium panel for the keyboard is cut and the keyboard mounted behind this with small spacers, nuts and bolts. The smaller aluminium panel is drilled to accept the switch bank. These switch modules are much cheaper than miniatures toggle switches, and the finished result looks extremely professional. Slot them into the 8 -way bracket (positions 2 and 7 are left blank), bend the small tabs over to retain them, and then mount the unit behind the panel.

Make all wire interconnections (except those connecting the power supply to the main p.c.b.), taking care, as there are a number of them. See Fig. 11. Shielded audio lead was used where necessary, to avoid hum pick-up, and the case of the pot was earthed. When a final check has been made, turn on the mains and check that 12 V is delivered by the regulator, and if so, turn off, connect up the two p.c.b.s



Fig. 10(a). Base plate drilling details

Fig. 10(b). Switch fascia drilling details


Fig. 10(c). Keyboard bezel details

and turn on once more. Adjust the preset VR1 to tune the whole instrument up or down as necessary, and if all is well, bolt the unit together. You are now ready to start playing. If the probe switch is closed you cannot use both probes as you will try to put two different frequencies into ICs 5 and 6. A nasty sound will result!

## CONCLUSION

The author has a prejudice against the vibrato effect, and so did not include one, but readers who are adventurous enough will find scope for development in this instrument, such as adding a phaser or a delay unit. However, the unit as described should give many hours of enjoyment, with various combinations of voices and stylii being possible. For greater variety, switches S3-S6 can be separated ' $a$ ' and ' $b$ ' to give e.g. $16^{\prime}$ square with $2^{\prime}$ triangular ... a pig-andwhistle effect!

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Robotic experience is becoming as essential a subject as computing. MICROGRASP provides the lowest cost means of acquiring that experience but despite its ultra low price the robot has considerable versatility. There are 5 axes each using a servo motor and there is feedback from each of the arm movements. Control is by any computer with an expansion bus - the ZX81 being particularly suitable. Servoing is achieved with hardware on the interface board to keep programming simple and the robot is operated under BASIC commands with no computer-specific software required. The interface board is memory mapped using only 64 bytes at any of 1024 switch selectable locations.
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HEBOT II is a turtle-type robot which takes programming out of the two dimensional world of the VDU into the real three dimensional world. Given a DC supply of 9-15V it can perform a bewildering number of moves under computer control - forwards, backwards, left and right - with each wheel independently controlled. It has blinking eyes, bleeps with a choice of two tones and has a solenoid operated pen to chart its progress. Touch sensors coupled to its shell return data, about its environment, to the computer for it to caiculate evasive or expioratory I/O port or alternatively with the universal interface board io the expansion bus of a Z 881 or other computer.
Hebot II kit
Universal computer interface board
23 way edge connector
Z×81 peripheral/RAM Pack splitter board


GENESIS P102 PROCESSOR BOX, HAND HELD CONTROLLER AND CORTEX COMPUTER

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READY BUILT $£ 395.00$ (Electronics Today International December issue on CORTEX)

## POWFPTRAN

 cybernetics

MICROGRASP, INTERFACE BOARD AND ZX81

## ‘HIGH-TECH’ FROM HANTS . . .



GENESIS S101 AND GENESIS P101 WITH PROCESSOR BOXES AND HAND-HELD CONTROLLERS

With prices starting below $£ 1,000$ the Genesis range of general purpose robots provide a first rate introduction to robotics for both education and industry. Each has a self-contained hydraulic power source, which enables loads of several pounds to be smoothly handled. The system operates from a single phase 240 or 120 V AC supply or a 12 V DC supply. The machine can be supplied with up to 6 axes each of which is fully independent but capable of simultaneous operation. Position control is achieved by means of a closed-loop feedback system based around a dedicated microprocessor. Movement sequences can be entered, stored and replayed by use of a hand held controller, alternatively the systems can also be interfaced to an external computer via a standard RS 232C link.

Example prices and specifications

[^2]MICROGRASP was designed to be priced at under £200 inclusive of power supply, computer interface board and even VAT! However, despite that restriction, it has some very powerful features. Driven by a simple computer, the ZX81 being eminently suitable, Micrograsp has an articulated arm jointed at shoulder, elbow and wrist positions. The entire arm rotates about the base and there is a motordriven gripper. Each of the arm movements is servo controlled i.e. there are position sensors feeding back information to the interface board, where it is compared with the programmed-in intended position, and automatically taking corrective action. This servo action is independent of the computer, greatly simplifying the software to drive the robot and all programming is carried out with a small number of Basic commands.

## MECHANICAL OPERATION

For each of the five axes there is a motor with integral gearbox. For the wrist and gripper motors small in-line gearboxes are used. The other axes use more powerful gearboxes in heavy duty zinc alloy castings. The shoulder and elbow joints are driven directly from the motors gearboxes with both motors mounted on the lower arm (Fig. 1). On the upper arm and the shoulder support bracket are steel bushes clamping the gearbox shaft so that when the motors are driven there is relative movement between the lower arm and the upper arm and the support bracket.

Also on the lower arm are the position sensing potentiometers. On the bushes of these are plastic bushes on which the arm rotates. The shaft of each potentiometer is held in the steel bush fitted to the upper arm or support bracket.

For rotating the arm (axis $O$ ) it is not possible to have the gear box shaft, the potentiometer and the shoulder support bracket all in line so the power is taken from the gearbox (Fig. 2) by a pair of spur gears which being of $2: 1$ ratio result in a doubling of torque. For this axis the gearbox shaft is taken out from the motor side of the gearbox.

For raising and lowering the wrist (axis 3) the gearbox shaft rotates a bar to which the potentiometer shaft and gripper mounting plate are fitted (Fig. 3). Through this bar the drive shaft for the gripper lead screw passes. When the

The Genesis range of robots published in these pages last winter have most effectively filled their role of providing a low cost introduction to robotics. Although their price is well within the budgets of further education establishments, industrial production and research and development departments; state run schools and home constructors have found it more of a struggle to raise the funds. In order to provide them with hands-on-experience of robotics we have created the ultra low cost Micrograsp.

At the same time further development of the Genesis P101 has resulted in P102, a higher performance version.



Fig. 2 Linkage between motor, spur gears, shoulder support bracket and potentiometer for axis $\mathbf{0}$ movement


Fig. 3 Linkage between motor, gripper mounting bar and potentiometer for axis 3 movement
always be required for the arm to be motionless and a considerable torque would also have to be provided by the gearboxes causing an undue strain upon them.

## CIRCUIT OPERATION

The interface board is designed to operate as a memory mapped peripheral of the controlling computer which generates the positional and manipulative commands whilst servoing is taken care of by linear circuitry on the interface board greatly simplifying the work of the computer and avoiding the requirement for extensive software specific to each type of machine. Some computers have I/O ports by which data could be sent to the robot, however the commonest and cheapest computer on the market, the ZX81 does not have this facility. It does however have an expansion bus giving access to all the address, data and control lines. Virtually all other micro computers also have this facility making practical a universal interface. The signals required are the address bus, data bus, WRite and $\overline{M e m}$ REQuest. The connector format choice could have been arbitrary but in view of the particular cost effective suitability of the ZX81 the layout of that machine was selected and by using two back-to-back 23 way double sided connectors, a very neat connection with no wires can be made.

For any other computer a 23 way connector would be wired to one of the type recommended by that computers


Fig. 4 Operating mechanism for the gripper
manufacturer. Using back-to-back connectors does however prevent the use of the 16K RAM pack limiting program length to about $30-60$ lines. This restriction is avoided by use of the three way adaptor p.c.b. (Fig. 5) whereby the RAM pack lies neatly on top of the computer.

By setting the ten bank DIL switch (Fig. 6) any one of 1024 blocks of 64 bytes of the memory area can be selected. Actually only six bytes are required but to narrow down the memory area used would call for extra circuitry and with memory costs per byte of around 0.15 p or less such extra complexity is pointless. IC2 is a ten bit comparator. The ten most significant address lines are compared with the +5 V or OV levels set up by the switch and when there is a match, i.e. when the computer selects an address within the 64 byte block, pin 13 goes high. The three least significant address lines are connected to IC3, a three into eight decoder, to select which axis is to be given a fresh command.


Fig. 5 Printed circuit of three way adaptor
The output of the decoder is enabled only when WR and MREO are low and IC2 pin 13 is high i.e. when the computer is addressing the chosen axis as if it were a memory location into which data is to be written. For example if the top of the address space is to be used all the switches would be set to be open therefore addresses 65472-65535 are allocated to the robot. To move the rotation axis (servo circuit A) to the centre position the command would be POKE 65472, 128. 128 being the centre of the range of positions defined as 0


Fig. 6 Circuit of computer interface

## COMPONENTS

## INTERFACE BOARD

## Resistors

| R1, R2, R15A-D, R16A-D, ) | 4 k 7 (12 off) |
| :---: | :---: |
| R31,R33 | 4k7(12 of) |
| R3-10 | 4k7 SIL network |
| R11 | 82R |
| R12 | 68R |
| 13A-D, R18A-D, R19A-D, | 1 k (18 off) |
| R21A-D, R27, R30 J | 1 k (18 off) |
| R14A-D | $3 \mathrm{k9}$ (4 off) |
| R17A-D | 470R (4 off) |
| R20A-D, R22A-D, R25, R28, | 100 |
| R32, R34 |  |
| R23A-D, R24A-D, R35, R36 | 3R3 (10 off) |
| R26, R29 | 10k (2 off) |

## Potentiometers

VR1A-D, VR2A-D
$22 k$ preset ( 8 off)

## Capacitors

C1, 2
C3. 4
C5A-D
C6A D $\quad 100 \mu / 10 \mathrm{~V}$ vertical electrolytic (4 off)
C7A-D 100p ceramic (4 off)
C8A-D $\quad 47 \mu / 10 \mathrm{~V}$ vertical electrolytic (4 off)
C9A-D 47n polyester (4 off)
C10A-D, C11A-D.
C1 2 A-D, C13A-D,
C1 $16-19$
C14, C15 $\quad 47 \mu / 6 \vee 3$ tantalum (2 off)
Integrated Circuits

| IC1 | 7805 |
| :--- | :--- |
| IC2 | DM8130 |
| IC3 | 74 LS 138 |
| IC4 | 74 LS04 |
| IC5A-D | 74 LS373 (4 off) |
| IC6A-D | DAC0808 (4 off) |
| IC7A-D | $1458(4$ off $)$ |
| IC8A-D, IC10 | LM2877 (5 off) |
| IC9 | $74 L S 123$ |



## Miscellaneous

Printed circuit board
Si-S10-SPST 10 bank DIL switch
TV5 heatsink
8 pin i.c. socket (4 off)
.14 pin i.c. socket
16 pin i.c. socket ( 6 off)
20 pin i.c. socket (4 off)
24 pin i.c. socket

## ROBOT

## Capacitors

C101, C102, C105A-D.) C106A-D,C107,C108

47n ceramic ( 12 off)
C103, C104 $4700 \mu / 16 \mathrm{~V}$ horizontal electrolytic (2 off)

## Diodes

REC1 6A rectifier block

## Transformer

T1 $0-120 \mathrm{~V}, 0-120 \mathrm{~V}$ primary $6-0-6 \mathrm{~V}$ at 4A secondary

## Potentiometers

VR101A-D 1k linear

## Miscellaneous

Motors, mechanical parts, fixings etc.
A kit of parts is available from-
Powertran Cybernetics,
Portway Industrial Estate,
Andover,
Hants, SP10 3NN £ 125-Robot plus 15\% VAT
£48-50-Interface plus 15\% VAT.
to 255 . Because of the redundancy in address selection 65480, 65488, 65496, 65504, 65512, 65520 and 65528 would be equally effective addresses.

The decoder enables IC4 which is an eight bit wide data latch which holds the data indefinitely after the writing-in process is completed. The data is converted into a d.c. level in the range $O V$ to 1 V by IC6 which is a digital-to-analog converter and IC7 a converts the current output of the DAC into a voltage, the feedback resistor R 18 giving it a gain of 1 volt/ma. 1C7a is also used to add in an offset voltage to balance out the residual voltage from VR101 when the axis is at its zero code position i.e. lowest or furthest left position. The position of the axis is sensed by VR101 to which is applied about 2 V derived from the 5 V rail via R11, R12. 1 V corresponds to the position in the centre of the travel of that axis. VR2 is used in setting the range of movement and IC7b is a unity gain buffer enabling the low ( 1 k ) input impedance of the power amplifier stage to be driven without loading VR101 significantly.

IC8 performs two functions simultaneously. It compares the measured position of the axis with the programmed-in desired position and serves as a bridge output power amplifier to drive the motor either backwards or forwards with a voltage dependent on how far away from the desired position the axis has reached. To see how the circuit operates,
first we consider the half with pins $7,8,10$. The desired position voltage (DPV) is applied to pin 8, feedback via R22 makes pin 7 a virtual earth point elevated above ground by the voltage on pin 8 . The measured position voltage (MPV) forces a current into this point via R21 resulting a voltage at pin 10 which is R22(DPV-MPV)/R21 i.e. pin 10 will go positive when MPV is less than DPV.

The other half of the i.c. behaves similarly except that pin 2 will go negative when MPV is less than DPV. As the circuit is symmetrical the voltage applied to the motor is therefore twice R22(DPV-MPV)/R21. The components selected resulting in a servo action which is close to critically damped.

R23 + C10 and R24 + C11 are the Zobel networks used almost universally to stop power amplifiers becoming power oscillators in the MHz region.

Capacitors C12, C13 are for local decoupling to also assist in ensuring stability and C105, C106 are suppression capacitors fitted as close as possible to the motor. Without these the interference from the motor brushes is sufficient to make the computer abort its program. Only four of the five axes are servo controlled as the gripper needs only to be either holding or releasing.

The gripper is activated by a motor turning a lead screw which then pulls together the jaws. To hold an object IC9a is triggered in a manner similar to the enabling of the data
latches. This monostable then provides a signal for about 2 seconds, as determined by R25, C14, which causes IC 10 to apply a voltage to the motor to pull in the jaws. When an object is seized the motor will stall but the amplifier is fully protected and as the stall period is less than 2 seconds no overheating occurs. On triggering IC9b the motor is driven the opposite way until it stalls at the jaws fully open position. Gripper operating commands could be POKE 65477,0 to hold and POKE 65478,0 to release, though this data as indicated by 0 is quite irrelevant and anything between 0 and 255 could be written. If the address allocated to axis 0 (servo circuit $A$ ) is $A$ then axis 1 is $A+1$, axis 2 is $A+2$, axis 3 is $A+3$, hold is $A+5$ and release is $A+6$.

The rotation shoulder and elbow motors take up to about 1 A each and the other two motors up to about 0.5A each. The reference voltage for the DAC and the position sensing potentiometers comes from IC1 which provides excellent stability. The amplifiers requirements however are noncritical and an unstabilised supply is entirely adequate. The circuit shown (Fig. 7) provides $\pm$ approximately 9 V . The supply is sited in the robot base where, as well as providing useful ballast at the rear of the base the mains connections are fully enclosed. The interface board is therefore free of mains and is safely operated whilst unenclosed and closely connected to the computer.
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# Ulimum Compluter <br> Interface Pour 2 

THE ULTIMUM is a motherboard organised universal interface system, the bus of which is broad based enough to allow it to interface with almost any microcomputer. It can also evolve to become a computer in its own right.

## THE 16/64K RAM CARD

The first card available for the ULTIMUM is a dynamic RAM card. It may be configured as a 16 or 64 Kbyte card dependent on the RAM i.c.s used.

Fig. 2.1 shows the circuit diagram. This is a rather unconventional design as it has to cater for both Z80 and 68/65xx busses which have very different timing requirements.

The dynamic RAMs have to be refreshed to preserve their contents, and this is done when the microprocessor is not reading or writing to the memory. This kind of refresh is called transparent as it does not affect the processor.

65/68 series microprocessors never address memory when their clock output is low (the Q1 cycle) so this time slot is used for refresh. The Z80 on the other hand, provides a refresh timing signal to indicate that the memory is not being accessed. The $Z 80$ also provides other refresh signals but these are not used in this design.

The refresh involves sequencing through a series of consecutive addresses on the RAM address lines. IC13 has a built in counter which is incremented on each memory refresh cycle.

Because dynamic RAMs are in 16 pin packages, there are not enough lines to fully address them. Consequently some of the pins have to have addresses multiplexed into them. IC13 will do this for 16 K memories, but additional circuitry is needed for the 64 K RAMs and this is provided by IC16 and IC17.

ULTIMUM is the missing link between your computer
and the outside world! Just take a look at the interface
board line-up

## WEO1 RAM

A $16 / 64 \mathrm{~K}$ Byte dynanic RAM card (detailed in this article).

## WEO2 BRR

A ROM/Battery back-up RAM card for use with $2516 / 2716 / 2732$ EPROMS and 6116 static memory chips. There are two sockets available for 6116 RAMS with battery back-up allowing up to 4 K per card of RAM to be stored permanently when the system is switched off.

## WEO3 PRG

An EPROM programmer designed for use in conjunction with the EPROM card above. This has hardware timers and EEPROM facilities.

## WEO4 FDC

This is perhaps the most complex of the daughter cards. It is a very comprehensive floppy disc contro!ler for up to 5 disc drives per card. It has its own processor which performs all the standard disc read/write routines and communicates to the ultimum bus via a pia chip. This makes software patching for different computers possible. The card includes an operating system ROM programmed for each host computer.

## WEO5 PRT

A part card with RS232c, parallel and Centronics interfaces, and a real time clock.

## WEO6 ADC

An analogue card with 12 -bit precision $A>D$ and $D>A$ capability. A fast conversion 8-bit $A>D$ is also included.

## WE07SBD

A sound board using a brand new chip to give up to nine oscillators with programmable frequency, waveform, ADSR envelope shaping and band filtering.

## WEO8SPK

A phoneme speech sard which is software programmable from RAM or ROM.

## WEO9 RES

A terminal card which provides 80 column video output and a keyboard interface to allow for connection of up to eight keyboards. It has optional character sets including teletext and block graphics

## WE10 CPU

A second processor card based on the very powerful 6809 c.p.u. This card can share the other system cards with the host computer and can be used to control the terminal card for multitasking operations.

## WE11 PRO

The system breadboarding card-an invaluable card for anybody wishing to experiment with their own daughter cards.

## WE12 EMU

This card has facilities to emulate up to 4 K of ROM. RAM is memory mapped into host computer, then software switched into emulation.


Fig. 2.1. Circuit diagram of the 16/64K Dynamic RAM board


Fig. 2.2. Component layout of the RAM board

IC12 is used to provide the multiplex timing. The rest of the circuitry is decoding and buffering to allow paging and connection to the mother board.

## ASSEMBLY

The component layout is shown in Fig. 2.2. As with the ULTIMUM, start with the sockets, then the capacitors and resistors and finally insert the i.c.s. taking special care with the static-sensitive memories.

## THE LINKS

There are several links to be set up. To make life a little easier, many are initially configured for 64 K RAMs, as most people will opt for this capacity.

Link 2 is set to the Rfsh position for 280 based systems and Q2 for 65/68xx computers.
To give the user a wide range of decoding options there are several links used for setting up the address space. The function of these links is given in Table 2.1. The paging facility can be used to allow the 64 K RAM to be mapped in pages of 16 K , and 4 K blocks for the 16 K . Many other configurations are possible. The paging may be omitted if not required.

If you are using 16 K memories, link sets 1 and 3 require cutting and switching over. Cutting the set-up tracks is best done with a sharp blade. Applying a hot soldering iron will then remove the tracks between the cuts.


ULTIMUM is a motherboard configured universal interface system designed to work with most microcomputers

## COMPONENTS <br> 16K/64K DYNAMIC RAM CARD

## Resistors

R1, R2
$5 \mathrm{k} 1 \frac{1}{4} \mathrm{~W} 5 \%$ (2 off)
Capacitors
C1, C2
C3, C4
C5-C20
$100 \mu / 6 \mathrm{~V} 3 \operatorname{tant}$. (2 off)

Integrated Circuits
IC1-IC8 IC9
IC10, IC11
IC12
IC13
IC14
C16, IC19
IC15, IC17
IC18

10 p disc ceramic (2 off)
100 n disc ceramic (16 off)

4816/4864* (8 off)
74LS373
74 LS 138 (2 off)
74LS123
MC3242
74LS148
74 LSO 0 (2 off)
74LS32 (2 off) 74LSO4

## Miscellaneous

14 pin di.l. socket ( 5 off)
16 .. .. .. (12 off)
20 .. ..
28 ,"
Printed circuit board WE01
PL1 $2 \times 32$ 'A $+C^{\prime}$ DIN Euro Plug (right-angled pins)

## Option*

4
a) For 16 K RAM IC1- $8=4816$ ( $16384 \times 1$ bit i.c.)
b) For 64 K RAM IC1-8 $=4164 / 4864(65536 \times 2 \text { bit i.c.) })^{8}$

TABLE 2.1. Links for the RAM board. Some links are in sets

## Link set 1 ( 7 links near IC 13)

These links set for 64 K RAM. Cut and change over for 16 K option. Their function is to set up IC13 address multiplexer for 64 K or 16 K operation.

## Link set 2 (one link)

Set to RFSH position for Z80 systems, to Q2 position for $68 / 65 \times \times$ systems.
This all-important link tells the refresh circuitry when it may perform the refresh. It also gives the timing for read and write.

Link set 3 (2 links near IC 14)
These links set for 64 K RAM. "Cut and change over for 16 K operation.
These links determine whether the RAM is to be decoded in 8 K or 16 K blocks.

Link set 4 (4 links near IC 11 )
These links set for permanent (not pqged) memory mapping. Cut one or more links and connect to Q0, Q1, Q2 or Q3 to allow AS lines (from 8255 port on mother board) to map in/out memory.

Link set 5 (four double links near IC15)
These are the main decoding links. Y $\emptyset$ to Y 7 of IC 10 allow you to map the RAM in blocks of 16 K (in the case of 64 K RAM) to any 16 K boundary. If 16 K RAM is fitted and link set 6 set up (see below), the memory may be mapped to any 8 K boundary, in 2 blocks of 8 K each.

## Link set 6 (three links near IC 1 0)

These are set up for 64 K RAM. Cut and link the other way for 16K RAMs.
These links set the decoder up to decode in 8 K or 16 K blocks. If left in their default position, these only $\mathrm{Y} \emptyset, \mathrm{Y} 1, \mathrm{Y} 2, \mathrm{Y} 3$ are available from IC10. Linked the other way, all outputs are enabled each representing an 8 K boundary.

## ROM AND BATTERY BACK-UP RAM CARD

This card provides five sockets each of which may be configured to accept a 4 K EPROM, a 2 K EPROM or a $2 \mathrm{~K} \times 8$ RAM. Two of the sockets have back-up power from a rechargeable battery, giving up to 4 K of non-volatile RAM. All the necessary address decoding and selection is provided on the card.

## OPERATION

This is a nice simple card. IC6 provides address decoding to 4 K boundaries which is sufficient for 2732 EPROMS. The provision of the inverter on the A11 line and ICs 8 and 9 allows decoding to 2 K boundaries for $2716 / 2516$ PROMS and 6116 RAMs. Fig. 2.4 shows the link layout for setting up the addressing. The As lines allow for the overlaying in sophisticated systems of up to three 4 K slots per Battery RAM/ROM card, accessible under software control by writing the appropriate data to the Motherboard 8255 AO acts as an enable. A1 as a disable. Care should be taken not to enable more than one chip into the same part of memory space at a time.

Sockets 4 and 5 are provided with the option of a battery back-up power supply of 3 V . This is sufficient for low power 6116 RAMs to hold information for about a year-even if the card is unplugged. The power for normal-mode use and for the battery trickle charge is derived from the twelve volt rail by a Zener shunt regulator (R1 D2). Switching between
main and back-up power is effected by diodes D3 and D1. The transistor circuitry on the CS lines ensures that they stay up with the back-up power line when the main power disappears, keeping the RAMs deselected and thus in low power mode. Links 6 and 7 provide for not using the battery backup if this option is not required. Links 1 to 5 configure respectively sockets 1 to 5 for 2732s, 2716/2516s or 6116 s . Fig. 2.4 shows the required layout of these links. Finally IC10 tells the motherboard when the data bus buffers must be activated.

## CONSTRUCTION AND TESTING

Construction is straightforward. Links should be inserted and soldered in place first, discrete components next, and then the integrated circuits. The battery should be fitted last.

Testing the card requires an operational Motherboard and host computer. To test for EPROM you will require (a) an EPROM with known contents, and (b) a program to read it. If you have access to a PROM programmer and an eraser then life is made easy for you; simply copy your operating system or language system ROM into a spare EPROM drop this into the socket to be tested and write a little program to check the copy against the original. Mere mortals will have to make do with viewing their language ROMs first few bytes using operating system facilities, noting them down on a scrap of paper, moving the ROM in question to the socket under test and viewing them again in their new position in


Fig. 2.3. Circuit diagram of ROM/Battery Back-up RAM board

| LK9 | LK 11 |
| :---: | :---: |
| BASE $+800 \mathrm{HEXO} \mathrm{O}-\mathrm{O}$ | O F000 |
| BASE O-O-O1 | - E000 |
| LK8 | O 0000 |
| $1 C_{5}(0-0$ | O C 000 |
| $10^{0-0}$ | - 8000 |
| $1 c^{(0-0}$ | O A000 |
| $1 C^{10-0}$ | O 9000 |
| 103 O-0 | O8000 |
| IC 3 lo-0 | 07000 |
| 102 O-0 | O 6000 |
| 162 100 | O 5000 |
| 10-0 | - 4000 |
| cl | - 3000 |
| LK 10 | O 2000 |
| Asn 0-0-0 | - 1000 |
| As n + 7 O-0-0 | 100000 |
| As $n+140-0-01$ | BASE <br> ADDRESS |
|  | IN HEX |

Fig. 2.4a. Addressing links on the Battery Back-up board. Link one of the pad pairs for each i.c. in L8 to the appropriate one in L11 to set the 4 K base address. If the i.c. is only $\mathbf{2 K}$, link the other pair to either of the $L 9$ triplets to set the 2 K boundary. Otherwise, link the two pad pairs together (unless you want to be clever and bring in an As line with L10! N is the number of the Euroconnector into which the card is plugged. The relationship between the As line numbers and the 8255 port bits was shown last month on the Motherboard circuit diagram)

| LKG | LK7 |
| :---: | :---: |
| 164 | $1 C 5$ |
| 0 | 0 |
| 0 | 10 |
| BACKUP NORMAL | BACKUP |
| NORMAL |  |

E6991
Fig. 2.4b. Power links

LK 1, 2, 3, 4, 5 .
0

| 611600 |
| ---: |
| 2732 |
| 2516 |
| 2516 |

E6997

Fig. 2.4c. Configuration links


Fig. 2.5. Battery back-up board component layout
memory. If your system is such that you cannot move a ROM without losing your operating system then you have real problems!

Testing RAM is more simple; all that is required is to write
a known pattern into a location (e.g. all zeroes or all ones), read it back to check it, and go on to the next one. Keep a count of the errors; it should be zero over several cycles through the RAM

## COMPONENTS . . .

## BATTERY BACK-UP BOARD

## Resistors

| R1 | 47 IW |
| :--- | :--- |
| R2 | $2 \mathrm{k} \frac{1}{2} \mathrm{~W}$ |
| R3, R4 | $330(2$ off $)$ |
| R5-R8 | $1 \mathrm{k}(4$ off $)$ |
|  |  |
| All resistors |  |

## Capacitors

C1-C11
C12
100n disc. cer. (11 off)
$47 \mu / 6 \mathrm{~V} 3$ tant.
C13 $100 \mu / 6 \mathrm{~V} 3$ tant.
C14, C15 330p polystyrene (2 off)

## Semiconductors

| TR1,TR2 | BC109 (2 off) |
| :--- | :--- |
| D1, D3 | 1N914 (2 off) |
| D2 | $5 V 6 / 1$ W'3 Zener |

## Integrated Circuits

| IC1/IC5 | EPROM/RAM see text (5 off) |
| :--- | :--- |
| IC6 | 74 LS 154 |
| IC7 | 74 LS04 |
| IC8. IC9 | 74 LS 32 (2 off) |
| IC10 | 74 LS30 |

## Miscellaneous

14 pin low profile d.i.l. socket (4 off)
24 pin low profile di.i. socket ( 6 off)
P.c.b. mounting battery 3V6
P.c.b. WEO2 BRR
$2 \times 32$ A + C DIN Euro-Angle plug

## Constructors Note

All kits for the Ultimun system are to be available from Watford Electronics (See advertisers' Index). Send SAE for price list of boards now available.


## Genesis

Overwhelmed by the profusion of electronics in daily life all the way from children's toys to giant computers, we tend to forget that in the beginning all we had was wireless telegraphy as distinct from telegraphy by wire. The 'wireless' in its then embryonic state had only one application where it could obviously score and that was in maritime communication where, quite clearly, it was impractical to link ships at sea by wires. Up to the advent of what we now call radio communications a ship's position could be reported only when visually sited and identified by a watcher on shore. Similarly, ships at sea could only communicate when in visual or hailing range of each other.

When Marconi formed the Wireless Telegraph and Signal Company Ltd on 20th July 1897 it was the maritime world which quickly saw new possibilities. The Italian navy was first off the mark in adopting the Marconi system but within months Lloyds of London, the great shipping insurance syndicate, also became interested. The impetus thus originated with both naval and mercantile shipping interests becoming enthusiastic supporters of a remarkable invention which was to blossom years later into the huge and exciting industry which we now call electronics.

Marine radio and electronics nowadays doesn't get much of a press. We take it for granted as 'old hat'-a remote and hazy background to more exciting and immediate developments such as the laser or optical fibres or the popular crazes for personal computers and video.

Although in the background, marine electronics remains big business and highly competitive. I was reminded of this as further details of maritime operations in the Falklands conflict came to light. A total of 51 warships and 52 merchant ships were employed together with 171 aircraft of the

Fleet Air Arm. Eighteen thousand sailors and marines were at sea and at any one time during the operation the supply 'pipeline' of 8,000 miles length was carrying half a million tons of fuel and stores to sustain the armada

One may imagine the organisation required and the level of efficiency of communications necessary to ensure smoothness, particularly as the sharp end was in perpetual flux of battle. And, as this was in every sense a war (albeit undeclared by either side as is today's custom) there would have been the additional complications of encryption to preserve secrecy and periods of radio silence to conceal ship movements

The whole electromagnetic spectrum from VLF (for submerged submarines) to microwave (satellite communication to the operations centre near London) was employed. VHF and UHF to aircraft and between ships at short range. The bulk of naval ship-to-ship traffic, however, was on HF through the Marconi Integrated Communications System Mk 3 (ICS3), standard in the Royal Navy and adopted by other NATO and non-NATO navies. ICS3 is flexible both in frequency and power management and enables cornmanders to access the transmitter, receiver and antenna systems best suited to his comnunications requirement at any time with a number of different users working into the system simultaneously on different frequencies using voice, telegraphy or data

ICS3 is also adaptable to new technology. It already has frequency agility from extensive use of hroad-band techniques and auto-tuning enabling rapid change of frequency. Although unlikely to have been used in the South Atlantic it is also adaptable to frequency hopping.

In the merchant navy, too, we have come a long way from early spark transmission Minimum radio requirements for vessels over 1,600 grt were established at the 1974 Safety of Life at Sea Convention (SOI_AS 74). They include main and reserve MF telegraphy transmirters and receivers, automatic keyers radiotelephone transmitter and receiver on the distress frequency with auto-alarm, VHF radiotelephone and portable lifeboat transceiver.

Most large vessels have far more than the minimum equipment with additional high-powered HF transmitter and telex and facsimile facilities. radio direction finders, and other radio navigation equipment which may include Loran C, Decca Navigator, Omega la world-wide VLF positioning system), and Satellite Navigation. If we include raciar loften a dual installation) and echo sounders. the total electronic package can approach £ 100,000.

Although world shipbuilding, including the UK, is in recession, ships are being built and the race is on to supply equipment. Marconi International Marine, who supply radio and electronic sea-going officers if required as well as hardware, have recently won orders for complete installations in ten new buildings under construction in India, Japan and Korea. Apart from proven quality
of equipment, Marconi export successes in merchant shipping are due to the worldwide servicing network with a Marconi presence in every major port.

The slack caused by decline in the number of ships at sea has been taken up by large installations on oil rigs which, in addition to SOLAS requirements, have continuous need for commercial transmission and extra housekeeping requirements such as UHFNHF radio paging and aero-nautical beacons for helicopter guidance.

## Balance

Overseas sales of marine electronics equipment is just one area of industry that contributed. to a record $£ 6$ billion surplus on current account balance of payments last year and helped repay $£ 1.6$ billion on foreign currency borrowing. Compare this performance with the rising total of virtually bankrupt countries unable to service interest charges let alone repay capital borrowed.

## Surprise

There were plenty of raised eyebrows when Racal announced entry into the PayTV business. This was a company which had always shunned the entertainment sector of electronics. When Racal acquired Decca they couldn't get rid of Decca's domestic TV interests fast enough, eventually selling it off to a Far Eastern entrepreneur. Had Sir Ernest Harrison gone off his rocker doing a U-turn? Closer examination showed that he hadn't lost his touch or his sense of direction.

In fact Racal stays in the capital goods sector of the industry as an extension of traditional communications business and expect to generate billions of pounds in the next decade in cable and subscription TV. To get in on the act Racal has teamed itself on a 50/50 basis with Oak Industries of San Diego, California, who are already established with not only the technology but also operating experience with five Oak-owned STV systems and 610,000 paying subscribers. Old-timers in the industry will remember Oak switches which were the first products.

Oak moved into Pay-TV in 1977 and is now in all modes, cable, STV and direct broadcast by satellite (DBS). All use encryption technology to ensure that programmes can be received only by subscribers who have appropriate decoding apparatus. Racal have great experience in signal encryption and will no doubt contribute to the technology in the years ahead.

Immediately, however, Oak need to expand into international markets and the new joint company, Racal-Oak Communications Ltd, although based in the UK will cover the whole of Europe. The two equal partners are clearly delighted with their marriage which was blessed at the inauguration ceremony by none other than Mr Kenneth Baker, Minister for Information Technology, who hinted ever so slightly that he, himself, might have been the marriage broker following a meeting with Oak's chairman last June.


APPEARING hot on the heels of the Intel 8080A in 1974, the 8 bit NMOS Motorola 6800 soon established a significant following of designers who liked it for its single 5 volt supply operation and its elegant instruction set which had been modelled after the PDP1 1 minicomputer. By the end of the decade Motorola was building on its success and introducing several new devices, all described as "6800 family members" and all bearing a close resemblance to their parent. The 6802 was one of these, and was intended to directly replace the 6800 in new applications where its on-chip clock and RAM array would make it easier to use than the basic 6800 which was itself becoming obsolete.

The powerful 6801 is intended as a 6800 system-on-a-chip, with RAM, ROM, Clock, Multiplier, Serial and Parallel I/O all available in a single package. The 6803 is a ROM-less version of the 6801 but the 6805 goes the other way with a "sawn-off" version of the 6800 architecture for smaller single chip applications and low cost. The shortened registers and reduced memory addressing range of the 6805 allow it to fit into a 28 pin package complete with ROM R.AM and parallel I/O. A CMOS version, the MC 146805 and an EPROM version, the 68705, are also available. Perhaps the thing to note about the 6801 and the 6805 is that they share, to a large extent, the instruction set and features of their ancestor

Also in the 6800 family is the 6809 which represents an attempt to capture a slice of the data processing market for the Motorola family which until the 6809, could not compete well in this field with the 8080A or more particularly with the Z80. The 6809 is a very nice chip with most of the problems of the 6800 put right and with lots of new features and facilities, but unfortunately for Motorola, it turned up too late, when most of the data processing sockets had already been gobbled up by the 6502 made by MOS Technology. The 6502 is to the 6800 what the $Z 80$ is to the 8080A, a successful attempt by outsiders to improve on the basic chip and to steal a march on the originators.

The 6800 and 6802 , then, can be considered to be at the centre of a large and expanding family of devices which have a big following, and a large part of this success must be attributed to the original designers of the 6800 who came up with a simple but capable architecture and an elegant instruction set. The popularity of these devices should ensure their availability for many years to come.

## REGISTERS

With so much going for it, you may be wondering why the 6800 lost out to the 8080 and its "messy" instruction set in many applications. Although there are many secondary reasons, the primary reason must surely be the 6800's lack of CPU registers. In some respects the 6800 register set is good. There are two general purpose accumulators, compared with the one on the 8080A, and there is a 16 bit index register where the 8080 has none, but that is as far as it goes. Where the 8080A has six general purpose 8 bit registers the 6800 has none, with the result that temporary data storage and counters usually have to reside in main memory. To be sure, the use of main memory for this purpose is well supported with extra instructions to allow register like operations to be performed there, and it could be argued that access is made available to a virtually unlimited register set by this method, but the net result is a reduction in flexibility and in speed of access to the temporary data and the counters.

Even more of a problem, according to some, is the provision of only one index register, since most programs need two. Although
the 8080 has no true index registers, it is quite possible to use the DE and HL pairs as pseudo index registers at the cost of a few extra instructions. Achieving the same result with the 6800 would be a more difficult and time consuming job.

As can be seen from the file sheet, the 6800 and the 6802 share the same register set, which has two 8 bit registers ACCA and ACCB, and three special purpose 16 bit registers IX (Index register) SP (Stack Pointer) and PC (Program Counter). In addition there are 5 single bit flags which are for some operations grouped together as the 8 bit CCR (Condition Code Register).

The two accumulators are identical and are used as the focus of many of the instructions, particularly those which use the ALU (Arithmetic and Logic Unit). The accumulators may be added or compared with one another and either can be used to hold the result of arithmetic, logic, data test, and data handling instructions.

The Index Register is intended for use as a memory pointer and is used to implement register indirect addressing of data tables which are created in RAM by the programmer. Since only the Index Register is available as an indirect address pointer, this addressing mode is actually termed Indexed Addressing. The Index Register pointer can be moved through the full address range of 64 K bytes by increment and decrement instructions, but the real advantage of this 6800 feature lies in the ability to add an offset value which is specifed in the instruction. In effect, the Index Register may be used to hold the base address of a table with access to individual table entries being gained by specifying a $0-255$ offset value to be added to the Index Register value. The contents of the Index Register itself are not modified when this addressing mode is invoked. For example, the two byte instruction: ADDA OOH,X adds the content of the memory location pointed to by the Index Register to the accumulator, while: ADDA $08 \mathrm{H}, \mathrm{X}$ adds the content of the memory location pointed to by the Index Register value plus 8 , to the accumulator, leaving the Index Register itself unmodified. It is this offset capability which makes Indexed addressing so efficient; the 8080A programmer would have to use extra register arithmetic instructions to achieve the same result and would end up with a modified pointer value into the bargain.

The Stack Pointer register in the 6800 and 6802 works in exactly the same manner as the 8080A version, and is used to control access to a Last-fn-First-Out (LIFO) stack in RAM memory. In comparison with the 8080A however, the 6800 stack instructions are more limited, the 6800 is restricted to pushing or pulling a single byte from one of the two accumulators. The stack concept is also important for automatically storing subroutine return addresses and processor status following an interrupt, and the 6800 comes out well here since on interrupt it saves all the CPU registers on the stack automatically whereas the 8080A saves only the Program Counter, leaving the programmer to save the rest using PUSH instructions.

The Program Counter holds no surprises and is virtually identical to the 8080A in terms of its addressing range and its operation.

The 6800 and 6802 flags are somewhat different to those of the 8080A. There is no Parity flag, and this is sometimes a drawback, but there are two extras, namely Overflow, which is set if arithmetic overflow occurs as the result of an ALU operation, and Interrupt, which indicates whether interrupts have been enabled or disabled.

## INSTRUCTIONS

The 6800/6802 instruction set is regular and elegant, and this makes these processors easy to program and ideal for use in tutorial systems.

## 6800/6802 REFERENCE FILE SHEET

GENERAL
Although appearing shortly ofter the 8080A the 6800 never-really caught on quite as well. Ihis is mainly dua to the more powerful architecture of the former but it is apity because the 6800 has a more elegant instruction set and hardware which makesita good device for beginner-s and a better device than the 80804 when it is: ․onble of doing the job. The 6802 is a simple upgrade of the 6800 uthich has an an-chip dock generator and 128 bytes of RAM. The 6802 is recommended for all new devigns.

REGISTERS The 6800/6802 have two 8bit genaral purpoase dota registers (ACCA\&ACC B) and three specialised 16 bit memory pointers.

|  | ACCUM A | 8 | ACCA ACCB |
| :---: | :---: | :---: | :---: |
|  | ACCUM B | 8 |  |
| INDEX REG |  | 16 | /X |
| STACK POINTER |  | 16 | Sp |
| PROGRAM CNTR. |  | 16 | PC |

FLAGS:-

| D9 | $\infty$ | $\begin{gathered} \text { DJ } \\ \text { AUX } \\ \text { CARRY } \end{gathered}$ | INT ${ }^{\text {D4 }}$ | S/GN | ZERO | $\begin{aligned} & \text { Ol } \\ & \text { OVER } \\ & \text { Fow } \end{aligned}$ | CARRY |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

BASIC TWO CHIP 6800 CPU CCT

## INSTRUCTION SET AND SOFTWARE

The 6800 and 6802 share a common instruction set which has been modelled ofterthe PDPII minicompurter as far as possible. The instruction set is more elegont and less messy tham the competing 80804/80854 but is hindered by a scorcity of CPUregisters which is overcome to some extent by the "Direct"oddressing mode which allows fast access to page zero $(256$ Bytes) of memory. Reset coruses branch to address which must bestored in addresslocations FFFE E-FFFF. One, two and three byre instructions are used and "Orect, Extended, immediate, Ralative, Indexed and /mplied "addressing modes are available. Chips are wall supported in software including Tiny Basic.


BASIC SINGLE CHIP 6802 EQUIVALENT



| (1) (Bif N) Test Sign bit of most significant (MS) byie of resuit $=1$ ) <br> (2) (Bit $V$ ) Test. 2's complement overfiow from subtraction of ms bytes? <br> (3) (BitN) Test Result less than zero? (Bit 15-1) |  |  |
| :---: | :---: | :---: |
|  |  |  |
|  |  |  |



## 6800-6802 INSTRUCTION SET

There are 72 basic instructions in the set, but the availability of more than one addressing mode for many of them results in a total set of 197 different instructions. Instructions may be one, two or three bytes in length, where the first (or only) byte contains sufficient information to identify the instruction and its addressing mode, and the other byte or bytes contain ancilliary information such as a memory address. Instructions are provided for binary and BCD 8 bit arithmetic, logic operations, shifts and rotates, data load, data store, conditional or unconditional branch, and interrupt and stack manipulation.

Two instructions of particular note are SWI and WAI. SWI stands for SoftWare Interrupt and is rather similar in operation to the 8080A Restart (RST) instruction with the exceptions that there is only one (as opposed to 8 RSTs) and SWI causes all registers to be stacked, not just the PC. The SWI vector is also in high memory (FFFAH and FFFBH) as opposed to low memory for the 8080A RSTs. WAI stands for Wait for Interrupt, and has no direct equivalent in the 8080A. It causes all CPU registers to be stacked and the processor to be halted while awaiting an interrupt. This provides a fast interrupt response but also nullifies some of the advantages to be had from asynchronous interrupts. A comprehensive set of addressing modes are available as follows:- Direct; in which a single byte page zero address is specified as part of the instruction; Extended; in which a two byte address is specified (like 8080A Direct!), Immediate; in which the instruction contains the data to be used, not an address reference, Inherent; (the same as 8080A Implied), Relative; which allows branching forwards or backwards in memory relative to the program counter value, and Indexed which uses the Index Register and an offset supplied by the instruction as already described. Both the Relative and the Indexed mode have no direct equivalent in the 8080A instruction set. The Relative addressing range is from -125 to +129 locations relative to the first byte of the two byte relative branch instruction, this mode reduces the size and the execution time of a program.

## SOFTWARE

Like the 8080A family, the 6800 family has extensive software support because of its popularity and its long existence. It does, however, lack a universally accepted disc operating system such as the 8080A's CP/M. Perhaps the best known 6800 software is the Motorola MIKBUG monitor which was supplied with their evaluation board, the MEK68D2, but there are also a number of other software tools including Editors, Assemblers, Compilers (notably for FORTRAN) and Interpreters, including a TINY BASIC.

## INTERFACING

The 6800/6802 have no need of the IO/M line of the 8080A family since there is no separate I/O address space. Also, instead of the separate $\overline{R D}$ and $\overline{W R}$ lines of that family the 6800/6802 have a single RD $\overline{W R}$ line and a separate VMA (Valid Memory Access) line. By use of appropriate gating it is possible to convert the 6800 scheme to the 8080A version and vice-versa, and this is important if you ever wish to use peripheral chips such as UARTS from a different family to that of the processor itself.

The 6800 requires an external two phase clock generator, and two approaches to this are possible. The first approach to appear was a rather unconventional hybrid device, the MC6871, which included not only the clock generator electronics but also an appropriate crystal inside the package. Later on, the more conventional MC6875 appeared in a 16 pin DIL. This device provides some extra facilities but needs an external crystal.

The 6802 does not need an external clock generator, only a crystai, and has the added bonus of a 128 byte RAM array on the chip. The first 32 bytes of this array may be retained in a low power standby mode by using the additional supply pin, VCC Standby. These differences mean that the 6802 is not completely pin compatible with the 6800. The DBE (Data Bus Enable) and TSC (Three State Control) pins of the 6800 are not available on the 6802 , and neither are the $\emptyset 1$ and $\emptyset 2$ clock inputs for obvious reasons. Since the $\emptyset 2$ clock signal is used for systems control, an equivalent output is provided on the 6802 by E (Enable). Two other new 6802 pins (in addition to the crystal pins) are MR (Memory Ready) which when driven low causes the memory cycle to be extended to allow interface to slow memory or peripherals, and RE (RAM Enable) which is used to select the internal RAM array when required.

The interrupt schemes used by the 6800 and 6802 are identical and fairly simple. One advantage of the 6800/6802 over the 8080A is that the former have a Non-Maskable Interrupt (NMI) in addition to the standard maskable input available on all three. The NMI can never be disabled and is therefore useful in some systems to warn of power failure or other not-to-be-ignored happenings. Intel at first said that there was no need for an NMI, and then introduced one on their 8085A!

On the occurrence of an NMI, the processor stores the CPU registers on the stack and then loads the PC with the address stored in memory locations FFFCH and FFFDH. The maskable IRQ interrupt has the same general effect except that the vector is fetched from FFF8H and FFF9H. Note that only a single vector is normally available for each source and without an external interrupt controller chip, multiple interrupt sources have to be polled by software. The 8080A is difficult to compare directly, since it always needs at least some external gating to accept vectors, but thanks to the single byte RST instructions it is a comparatively simple matter to build a scheme to cater for up to 8 separate sources without polling. The 8085A has additional direct interrupt lines of course.

## PERIPHERALCHIPS

The 6800 series is blessed with an extensive family of peripheral devices capable of performing most of the commonly required functions and some of the rather more exotic ones.

Apart from the clock generators mentioned earlier, perhaps the most often specified peripheral device is the Peripheral Interface Adaptor or PIA for short. This function is performed by the 6821 device which has two 8 bit parallel ports useful for communicating with the full range of possible input and output devices such as switches, lamps, and line printers.

Communication with the CPU takes place over the bidirectional CPU data bus using standard 6800 or 6802 control signals, and two interrupt outputs (one for each port) are available for connection to an interrupt controller chip like the 6828 or to be WireOR'ed to the IRQ input of the processor. Each of the four possible sources of interrupt can be separately enabled or disabled by the processor if required. After the 6821 in popularity comes the 6850 Asynchronous Communications Interface Adaptor (ACIA) which most (Non-Motorola!) people call a UART. The 6850 is a simpler device than the Intel 8251 USART because while the 8251 provides asynchronous or synchronous serial communication, the 6850 is asynchronous only, with an additional part, the 6852, available if a synchronous link is required.

Other devices available include the 6840 triple 16 bit timer, the 6844 Direct Memory Access (DMA) controller, and the 6860 Modem. The 6802 also has its own special "Combo" peripheral device, the 6846 , which provides 2 K bytes of ROM, 10 parallel I/O lines and a timer. Since this device uses masked ROM it is not usually suitable for home projects.

## APPLICATIONS

As with the 8080A/8085 there would appear to be little point in using the 6800 in new applications now that the 6802 is available at a reasonable price. An added incentive to use the 6802 is the fact that CMOS versions are available from other manufacturers making it possible to build a low power consumption system when necessary for battery powered applications.

Both processors are ideal for learning about both the hardware and software aspects of microprocessors and the 6800 is widely used in tutorial systems for this reason. Neither chip can be recommended for data processing applications, however; if this is your requirement and you like the style of the 6800, then choose the 6502 or better still the 6809 .

The 6800 and 6802 come into their own as controllers for small systems and are mostly used for this purpose. Their simple lowcost hardware approach and their elegant easy to use instruction set suit them ideally for jobs such as appliance control, vending machines, car computers, and PROM programmers. In the author's opinion, if a 6802 is powerful enough to perform a particular control task then it is probably wise to choose it in preference to the 8085A because the resulting system will probably be simpler, cheaper, and easier to program. All in all the 6800 or the 6802 are not a bad choice for the hobbyist because it will later be easy to move on to more powerful chips like the 6502 or the 6809.


# SEMI-PROFESSIONAL MIXING DESK Part Three <br> THE p.c.b. design for the power supply unit is shown in 

Fig. 1 with the component layout shown in Fig. 2. Before the components are soldered, the ' $L$ ' shaped heatsink should first be fitted to the p.c.b.

All the components should then be soldered into position with mica washers being used on the two i.c.s. Carefully check the orientation of the semiconductors and the electrolytic capacitors.

The case components should be mounted as shown in Fig. 3 and all the mains wiring covered with rubber sleeving. The two output rails should be tested before the power supply is connected to the mixing desk.

## PA MIXING—LIVE CONCERTS

Mixing the sound for a live music show differs considerably from mixing in a recording studio. Firstly everyone plays at the same time which means that there are many more mixer channels to be balanced and equalised etc. Secondly the high sound level on stage makes it difficult for the players to hear each other with any degree of sound balance. Fig. 4 shows how all the instrument amplifiers, drums and singers are set-up and fed to the mixer which is normally positioned in the audience where the sound engineer can hear clearly the sound of the PA system. It also shows how a separate sound system is provided for the players on stage, so that they can all hear what each person is playing. This other mix is derived from an auxiliary mixer output which is independent from the main stereo PA mix.


Fig. 3. Wiring diagram for the p.s.u.

The mixer also adds effects to the overall sound, such as reverb and echo, using the other auxiliary outputs as well as taping the stereo mix for the inevitable post-mortem of the concert. Live sound mixing is certainly more liable to problems than studio recording, the most common one being feedback or howl-round between the microphones and the on-stage monitoring systems which are placed close to the players. Highly directional microphones are favoured for this reason. Also, because there is never any second chance with live sound it is essential to set up the system and balance the sound before the audience arrives, so that everything is ready when the players walk on to give their performance.

## USING THE MIXING CONSOLE

The mixing desk is a modular system built up from sets of 6 input channel modules, individual output channels and the Auxiliary PFL/Headphone output channel. Its main applications lie in the small four-track recording studio where cassette systems are now available for around $£ 600$, and live music mixing with PA systems. However, it is flexible enough to be considered for almost any sound mixing requirement. A simplified description follows to illustrate how the mixer is used in the multitrack studio for recording and mixing down as well as in the live concert situation.


Fig. 4. Live concert mixing


Fig. 1. P.c.b. design for the p.s.u.

[EP982
Fig. 2. Component layout


Fig. 5. Recording rhythm tracks

BOUNCING DOWN 3 TRACKS ONTO I


Fig. 6. Bouncing down 3 tracks onto 1

## THE MULTITRACK STUDIO

## Recording

The first stage of most music recording involves laying down on tape the basic rhythm structure. This usually means drums and bass guitar, along with a rough 'guide' track of vocals to help the rhythm players through the song's arrangement. Fig. 5 shows 4 microphones set up around the drum kit, the bass guitar and the vocal microphone which have all been connected to the mixer input channels. Listening on headphones the recording engineer uses the Pre Fade Listen (PFL) function to examine the sound coming in on


Fig. 7. Mixing down
each mixer channel, to check that all is well and to add equalisation to any sounds that need it. The drum microphones are all routed to one mixer output and recorded onto one tape track, while the bass and vocals are separately recorded on two other tracks. During this process the players listen to each other using headphones, driven from one of the auxiliary outputs of the mixer which allows them a balanced mix of what is being recorded onto tape. Next comes the addition of the other instrument sounds like guitars, keyboards and vocals, but because of the limited number of tracks available on tape a process known as 'bouncing-down' is used to conserve tape track space. Fig. 6 shows how the mixer may be used to mix three tracks together onto the one remaining track, which then makes room for three new tracks. In this way the recording is built up layer by layer until all the necessary ingredients of the sound are on tape and ready for the final 'mix-down'.

## Mixing Down

In this final stage of the recording process the four tracks of sound are reduced to a two-channel stereo format which necessitates the use of a second tape recorder. Fig. 7 shows how the mixer is used to transfer the sound across from one recorder to the other, and in doing so it allows a number of useful enhancements to be made for the final result. Firstly there is the question of attaining the right balance between the four tracks and the positioning of each track within the stereo sound image. This is known as panning. Final alterations are also made to the equalisation of each track to highlight the overall tone quality, and there is a further opportunity to add special effects such as reverberation, echo, chorus and phasing etc. The auxiliary mixer outputs are used to send any mixture of the sounds to these effects, whose outputs are then brought back on the remaining mixer input channels. Finally the end result is reached with a stereo tape that may be played on any domestic sound system. Improvements in technique come with practice, and care is taken to ensure that maximum level goes onto tape wherever possible.


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# SEMICONDUCTOR UPDATE R.W.Coles 

FEATURING<br>MC1468705G2 D60T OP-22

## ONE CHIP WONDER

I have always considered one chip microprocessors (that is to say those devices that cram CPU, RAM, ROM and I/O onto a single silicon chip), to be ideal for hobby projects. I say this because these devices are relatively simple to program and understand, and because they do not require any of the complex interconnections which would be necessary to support a multi-chip system based on, say, a Z80. All the budding designer has to worry about is interfacing to the outside world and program design, what could be easier?

Unfortunately there are some snags: The first one-chippers, such as the Intel 8048 , had masked ROM which meant you had to buy them by the truck-load. These were soon followed by EPROM versions, such as the 8748 , which improved things a lot, but even with these you still had to have a suitable PROM programmer. They also had the limitation of being made in NMOS only, so small battery powered systems were out because of the current drain. There has in fact always been at least one good excuse for not using them in the latest pet project!
Well the excuses have now run out, and as far as I can see there is absolutely no valid reason for not planning to build that pseudo-random, microprocessor controlled lawn sprinkler you have always promised yourself, thanks entirely to Motorola and their brand new MC1468705G2. (By the way, if you find that long part number offputting, look at it this way: The MC14 bit just means its Motorola and CMOS, the 7 means that it has EPROM rather than masked ROM, and the G2 means that it is better than a G1(?) Take that lot away and you're left with a Motorola 6805, which my "Boys Wonder Book of Micros" tells me is just a sawn-off 6800 with added RAM, ROM and $1 / O$ ).

The MC1468705G2 has 2106 bytes of U.V. erasable EPROM, 112 bytes of RAM, 4 eight bit $1 / O$ ports and a timer, all squeezed inside a 40 pin d.i.p. Enough to implement a pretty nifty sprinkler system! Even better, the chip has a 128 byte chunk of masked ROM pre-programmed with an EPROM programming algorithm so you don't even have to buy one of those. This means that you can make up a simple circuit board with a socket for the MC1468705G2 and a few external components which, given appropriate input data and a -13 volt programming supply, will act as your very own EPROM programmer.

Best of all though, the new chip is made in low power CMOS and has two additional instructions which also help to reduce supply current. The operating power consumption is typically 10 milliwatts, but execute a

WAIT instruction and this drops to 4 milliwatts even though data is retained and the clock and timer continues to run. Execute a STOP instruction and everything does just that, causing the power consumption to plummet to just 10 microwatts without destroying memory or register data. After issuing a STOP you can get the whole thing running again by generating an external interrupt or using the RESET input.

Anyone who knows the 6800 will get on fine with the MC1468705G2, although there are some differences. The new device only has a 13 bit address width to cover RAM, ROM and I/O, but this is more than enough for the on-chip resources and even allows for the addition of external EPROM if ports can be sacrificed as busses.

## WHOPPER

In these days of glamorous microprocessors and ever more complex integrated circuits, it is easy to forget the humble transistors and diodes which were of course the start of it all. But these simple components are still essential at the "business-end" of most systems, and the development of newer and better devices continues despite the fact that the lions share of research funding has been diverted towards producing the ultimate microprocessor or memory chip.

The designers at Westinghouse have certainly not neglected semiconductor development it seems, because their latest device, the D60T, has pushed the frontiers of power transistor technology further out than ever before by providing the capability to switch 40 amps and 650 volts at 20 kHz ! There is nothing simple about the D60T either. Its semi-conductor chip is nearly 1 inch in diameter for example, bigger by far than most microprocessor chips, and the manufacture involves a triple diffusion process. Even the package is bigger and better, because that massive chip is mounted in a hex-nut housing which measures over 1.5 inches across the points and stands nearly 2 inches above the heat sink surface. (Yes, you definitely need a heat sink if you want to get anywhere near the D60T's maximum 885W dissipation at 25 degrees C!)

But mere physical details do not do justice to the mighty D60T, and the real story can only be revealed by examining the electrical specs. Would you believe a maximum collector current of 100 amps? or a maximum base current of 20 amps? Well then, how about a sustained collector-toemitter voltage ( $\mathrm{V}_{\mathrm{CEO}}$ ) of 800 volts, or even 1200 volts if you reverse bias the base? Yes folks, the D60T can do all this and more!

Probably the most important feature of the D60T though, is not all those noughts after the amps and volts numbers, but the speed at which it operates. Switching at 20 kHz may not sound fast to all you logic fans who are used to Shottky TTL switching in a nanosecond or two, but at 40 amps and 600 volts its very fast

There are two problems with D60T, and the first is what on earth can you use it for. The manufacturers intend people to use it in place of Thyristors for motor speed controllers hooked up to 30 horsepower induction motors, but maybe you could use it in a 25 kilowatt class $D$ disco amplifier, or to control your arc welder or .. or .. or something.

The second problem is that a single D60T could set you back around $£ 50$. Makes microprocessors look like childs play, doesn't it!

## TIDDLER

Well if microprocessors make your head spin and the hairy-chested D60T makes you worry about your electricity bill, why not try an OP-22 from Precision Monolithics Inc?

PMI are famous, as their name suggests, for high grade analogue integrated circuits and especially op-amps. Their usual ploy is to take a standard design and to produce from it a higher performance version which they can sell to those who need that little bit extra and are prepared to pay a bit more for it. The OP-22 has been introduced as a high specification version of micropower op-amps like the National LM4250, with which it is pin compatible.

Micropower" generally means supply currents of a few tens of micro-amps for battery supply applications, and the new PMI device brings precision operation to these areas for the first time. The supply current of the OP-22 can be set externally with a single resistor anywhere between 1 and 400 microamps, but as you may expect, bandwidth is also affected, so to get 10 kHz you would need at least 300 microamps and even PMI cannot overcome that constraint
Where PMI can deliver the goods however, is in the areas of open loop gain, input offset voltage, and common-mode rejection. The OP-22 has a gain of more than a million, a guaranteed offset voltage of 300 microvolts or less, and it can realise a common-mode rejection ratio of over 100 dB for voltages to within 1.5 volts of the supply rails. Supplies of from 3 to 30 volts, single or split, can be used, and the OP-22 is available in either an 8 pin minid.i.p. or a TO99 metal can.


THIS month we describe in detail how to use the DISBUG monitor facilities. The instruction set for the 6800 is listed in full in Micro-file and there is a description given here of the full range of addressing modes. A step-by-step example of how to enter and run a program on the Microcontroller is included. Finally, the circuit and operation of the power supply module is described.

## DISBUG MONITOR FACILITIES

The DISBUG monitor provides the user with facilities to allow the entry of programs into the user RAM area, the examination and change of memory locations (including PIA registers), the debugging of prototype routines, and the control of execution of developed programs. The user communicates with DISBUG via the keyboard, and the monitor uses the display to respond with prompts and information.

The Microcontroller contains 1024 bytes of read/write memory (addresses 0000 to 03FF inclusive). Some of this memory is required to allow DISBUG to operate, but the remainder ( 0000 to 03AO) is available for user applications. Fig. 2.1 shows the allocation of address space in the RAM area.

The DISBUG monitor facilities are grouped into editor modes (memory, register, preset and breakpoint) and command functions (go, proceed and restart). Each mode or function is invoked separately, and they are each described in detail below.

## DISBUG DISPLAYS

The displays output by DISBUG follow a standard format. The normal prompt used when DISBUG is awaiting a command from the keyboard is ". . . dIS . . .". When an editor key (MEMORY, REGISTER, PRESET or BREAKPOINT) is pressed, the display will change to the form "p-aaaa-dd". The " $p$ " field will contain a prompt character to remind the user what input is expected next (e.g. "A" for address), the "aaaa" field will hold the address value, and the " $d$ " field will hold the data value. Initially the second and third fields will often be empty. e.g. when the preset editor is invoked, the

# MICRD CONTROLIER MICHAEL TOOLEY в.я. DAVID WHITFIELD m.a.m.sc. PART TMVO 

display will show "L--", indicating that the lower address value is expected. The data field will sometimes be used to display advisory information, rather than a strict data value. Such information (e.g. the breakpoint number) will not use standard numeric representation, to avoid confusion.

The numbers which are mentioned in the descriptions which follow, and those which appear in the DISBUG displays, are all in hexadecimal notation. All addresses must comprise of four hex digits (e.g. 008F), and all data values must comprise of two hex digits (e.g. 07); leading zeroes must be used where necessary to fill the fields to the appropriate lengths.

## THE MEMORY EDITOR

The contents of any memory location may be examined and (optionally) changed using the memory editor. The memory editor is also used for entering programs into the user RAM area ( 0000 to 03A0). Remembering that the 6800 treats PIA registers as memory locations, the memory editor may even be used directly to control the operation of the Microcontroller's PIAs; modifications to the programming of the keyboard and display PIAs, however, may interfere with the normal operation of DISBUG. Writing new values to


Fig. 2.1. Microcontroller RAM address allocations

EPROM addresses and unused addresses in the address map will have no effect, but beware of address images.

The memory editor may be invoked whenever the ". . . dIS . . ." prompt is displayed by pressing the MEMORY key. The display will then change to " $\mathrm{A}--$ ", indicating that the memory editor is expecting the address of the memory location to be examined to be input. The numeric keys 0 to $F$ are then used to specify the appropriate 4-digit address. After the fourth digit has been struck, the prompt character will change from " $A$ " to " $d$ ", and the current contents of the specified location will be displayed in the data field of the display. The " $d$ " prompt indicates that, if the user wishes to change the contents of this location, a new 2 -digit value may now be input. When the first digit of the new value is entered, the data field will be cleared, and the new digit displayed, e.g. the display might show "d-01Fb-7". No change is necessary, however, and by default the contents of the location will remain as currently displayed.

After any new value, if any, has been entered, the location may be closed with the ENTER key. This will cause the "A- - " prompt to re-appear, ready to examine another location. If the NEXT key is used in place of the ENTER key, the next sequential location will automatically be opened and displayed. The PRIOR key will cause the previous location to be opened and displayed.

The CANCEL key may be used at any time to abandon an uncompleted memory change and return to the ". . . dIS . . ." prompt. To exit from the memory editor when the "A--" prompt appears, either the ENTER or CANCEL keys may be used.
To gain familiarity with the operation of the memory editor, readers are encouraged to step through the DISBUG EPROM (addresses F800 to FFFF), safe in the knowledge that the contents of these locations are permanently programmed.

## THE REGISTER EDITOR

After a breakpoint has been encountered in a program under development, the contents of the CPU registers may be examined/changed using the register editor. The REGISTER key may be pressed to invoke the register editor whenever the ". . . dIS . . ." prompt is displayed. The register values with which the program will 'proceed' may then be examined, and optionally changed. Users should note that changing the address held in the program counter will affect the address from which the program will proceed.

The display of register contents used by DISBUG is cyclic in nature, and shows only one 8 -bit (2 hex digit) value at a time. The sequence is as follows:


The initial display will show the current contents of the A register. Typically the display would be "d- rA -32 ", indicating that the current contents of register $A$ is 32 , and that this may be changed by entering a new 2 -digit data
value (hence the " $d$ " prompt character). The ENTER key will cause the currently displayed value to be saved and the register editor to be exited. The NEXT key will cause the current value to be saved, and the contents of the next register ( $B$ in this case) to be displayed. The PRIOR key will cause the displayed value to be saved and the contents of the previous register (the condition code register in this case) to be displayed. The previous value of any register will remain unchanged if no new value has been specified.

The CANCEL key may be used at any time to exit from the register editor, and this will abandon any change which has not yet been completed.

## THE BREAKPOINT EDITOR

Temporary halts or breakpoints are often useful as an aid to debugging a program. They allow the programmer to split programs into convenient blocks so that each block may be tested separately. In practice, breakpoints are implemented by using the monitor program to replace instruction codes at the specified point(s) with software interrupt codes (3F's on the 6800). The replaced instruction codes, and their addresses, are remembered by the monitor so that the breakpoints may be removed when required. The software interrupt allows the contents of the CPU registers to be examined at the breakpoint because these are pushed onto the stack; users should remember to allow 7 bytes of stack to be used by the breakpoint editor.

Breakpoints are set and reset by pressing the BREAKPOINT key to enter the breakpoint editor. This may be done whenever the ". . . dIS . . ." prompt is displayed. DISBUG allows the user to insert up to four breakpoints in a program; these breakpoints are numbered from 0 to 3 , and are identified in the displays as b0 to b3, respectively. It is important to note that, for 2-byte and 3-byte instructions, the breakpoint must be set at the FIRST byte of the instruction, i.e. at the op code byte.

When the breakpoint editor is entered it displays the address at which the first breakpoint (bO) has been set. A typical display of "A-01E5-bO" would indicate that breakpoint 0 has been set at address 01E5. If no breakpoint has been set, the address shown will be FFFF; this address is within the DISBUG EPROM, and is therefore not a possible breakpoint address. The address of the breakpoint may be changed by entering a new 4-digit address (hence the A prompt character), followed by ENTER, NEXT or PRIOR. These keys will respectively: change the current breakpoint address to any new value specified and then exit from the breakpoint editor; change the current breakpoint address to any new value specified and then display the next breakpoint; or change the breakpoint address to any new value specified and then display the previous breakpoint. A breakpoint is reset by specifying an address of 'FFFF'. No change to a breakpoint is required, however, and unless a new 4-digit address is specified, the breakpoint address remains unchanged. The CANCEL key may be used at any time to exit from the breakpoint editor; any uncompleted breakpoint change will be abandoned.


The display of breakpoints is cyclic, i.e. the next breakpoint from 3 (the last one) is breakpoint 0 , and the prior breakpoint from 0 (the first one) is breakpoint 3 .

## THE PRESET EDITOR

Areas of read/write memory may be preset to the userdefined values using the preset editor. This is particularly useful for initialising RAM to known values, e.g. all zeroes, filled with NOP instruction codes ( $01^{\prime} \mathrm{s}$ ), etc.

The area of memory to be preset is specified by entering the lower and upper addresses for the block. If the two addresses are equal, only the specified address will be preset with the data value; in effect the same as using the memory editor, but much slower. If the lower address is specified as greater than the upper address, all memory locations except those between the two limits, but including the limits, will be preset. This will also have the effect of causing DISBUG to crash if the memory over-written includes the DISBUG RAM!

The preset editor may be entered whenever the normal DISBUG prompt is displayed. Pressing the PRESET key will cause the display to change from ". . . dIS . . ." to "L- - ". This indicates that the lower (start) address of the block of memory to be over-written should be entered. After the appropriate four digits have been entered, the ENTER key should be pressed to record the address. The display will then change to " $U_{--}$". indicating that the upper (end) memory address should be entered. After the appropriate four digits have been entered, the ENTER key should again be used to record this address. DISBUG will then output $\varepsilon$ display of "d--" to indicate that the data value to be written to memory should be entered. When the appropriate two digits have been entered, the ENTER key should be pressed. This will cause the data value to be recorded, and the block of memory identified to be over-written with the specified data value. Over-writing DISBUG EPROM addresses and "unused" addresses in the address map will have no effect. After the preset operation has been completed, DISBUG will return to its usual ". . . dIS . . ." prompt.

A preset operation may be abandoned at any stage by using the CANCEL key; no change to any address specified occurs until the ENTER following the data value is pressed.

## THE GO FUNCTION

A user program is started using the GO function key. After GO has been pressed, DISBUG will prompt for the program start address by displaying "A- - ". The user should then enter the 4-digit address from which execution of the program should commence. After entering the four address digits, the program may be started by pressing the ENTER key. Alternatively, using the CANCEL key will abandon the start request.

When DISBUG starts a program the 6800's registers are set up to the following initial values:-

$$
\begin{aligned}
r A & =00 \\
r B & =00 \\
\text { In } & =0000 \\
S P & =03 A O \text { (Start of the user stack) } \\
P C & =\text { The requested start address } \\
C C r & =00 \text { (Interrupts enabled and all status bits clear) }
\end{aligned}
$$

Before the user program is actually started, DISBUG inserts any breakpoints which may have been set. A breakpoint which has been set at the program start address will be ignored, but it will be remembered for a future occasion le.g. for starting at a different address or proceeding from a breakpoint). DISBUG then starts the program from the address now held in the PC, with all of its other registers in the states specified above.

## THE PROCEED FUNCTION

The proceed function allows the user to continue with the execution of a program after a breakpoint has been encountered. Alternatively, proceed can be used to start a program from a defined point, but with the CPU registers in userdefined states. This is achieved by first using the register editor to set up the required register values, with the start address in PC, and then using proceed to start the program. The proceed function may be called whenever the ". . . dIS . . ." prompt is displayed.

After the PROCEED key has been pressed, DISBUG will respond by producing a display of the form " E -aaaa- $\mathrm{Pr}^{\prime}$ ". The " $E$ " prompt indicates that the next input expected is the ENTER key. The "aaaa" value will show the address from which the program will resume execution. The "Pr" reminds the user that a proceed has been requested. Pressing the ENTER key will cause the program to proceed (after a brief delay). The display will go blank unless the user program writes to the display PIA. The CANCEL key in place of ENTER will abandon the proceed request and return to the ". . . dIS . . ." prompt.

If the user has changed any register contents since the last breakpoint, the program will resume with these new values; any change to the program counter will change the address from which execution restarts. Before DISBUG passes control back to the user program, any breakpoints which have been set (with the exception of any set at the restart address) will be re-installed

When an executing program encounters a breakpoint (or other software interrupt instruction), it will cause control to return to DISBUG. The monitor will then remove all of the breakpoints which have been set, and replace the original op codes. Any SWI instructions inserted directly will remain. DISBUG will then output a display of the form "E-aaaa-Br". where "aaaa" specifies the address of the breakpoint, and "E" indicates that the ENTER key will cause the "...dIS ..." prompt to re-appear. The address of the breakpoint (or other SWI) encountered may always be reinspected by examining the PC contents with the register editor. A command key may be used in place of ENTER to enter an editor or function directly instead of via the prompt.

## THE RESTART FUNCTION

The restart function is provided to allow the user to reinitialise the DISBUG monitor program. A restart will have the same effect as entering the monitor from switch-on, but without the need to interrupt the mains supply. The RAM area used by DISBUG (03A1 to 03FF) is reset to its start-up values, and the display and keyboard PIAs are correctly configured; the user RAM area is totally unaffected. Restarts are thus a convenient way of ensuring that user programs have not corrupted the DISBUG RAM or PIAs.

A restart may be requested whenever the normal ". . . dIS ..." prompt is displayed. Pressing the RESTART key will result in the display of the restart prompt, "rEStArt". The restart may then be activated by pressing the ENTER key, or abandoned by pressing CANCEL. ENTER causes the welcome message "dIS r1.0" to be displayed for approximately 2 seconds, followed by the normal DISBUG prompt of ". . . diS....".

## THE 6800 INSTRUCTION SET

The 6800 instruction set contains 197 different instructions which fall into four major categories:
(a) accumulator and memory
(b) index register and stack
(c) jump and branch
(d) condition code register

The full instruction set is shown in Micro-file. This table also summarises the op codes, number of bytes, number of machine cycles required for execution, and the effect of the instruction on the registers and memory. Each instruction is also represented by a mnemonic code (e.g. CLR for clear), which is of no significance to the 6800, but which provides a useful standard notation for writing programs.

In many cases, more than one instruction op code is associated with each mnemonic (e.g. LDA A can have op codes of $86,96, A 6$ or B6). The actual op code selected will depend on the addressing mode required; in the case of LDA A the modes available are immediate, direct, indexed and extended, respectively. When an assembler is used to translate from mnemonic codes to hex op codes, and there is a choice of addressing modes, some means must be provided to indicate the mode required. This is usually specific to the assembler being used, but for example $\#$ is often used to indicate the immediate mode. In manual translation, the programmer selects the appropriate op code from the table, but such a notation is still useful when writing the program in mnemonics.

The following sections describe the features of the six addressing modes which are available. When translating from mnemonic codes to op codes, the programmer should select the most appropriate mode, bearing in mind the length and flexibility of the resulting instruction. No attempt is made to provide a full description of the operation of each instruction; users are referred to a 6800 programming manual for further details. It should be remembered that the 6800 treats the peripheral registers in the PIAs as memory locations and the same instructions are used for manipulating their contents, e.g. B7 1802 writes the contents of register A to the A control register in the display PIA.

## INHERENT ADDRESSING MODE

Some instructions do not require additional address information for them to be completely meaningful since the required data is already present in the microprocessor's own internal registers. The following are examples of the inherent addressing mode:

CLRA sets register $A$ to zero (i.e. it clears the register).
PSHA pushes data onto the stack. The contents of register $A$ is stored on the stack at the address specified by the stack pointer and the stack pointer is then decremented by one.
INX increments the index register by one.
SEI sets the interrupt mask in the condition code register. The processor is then inhibited from servicing an interrupt emanating from a peripheral device, and will continue to ignore interrupts and execute the program instructions until interrupts are re-enabled by means of a clear interrupt mask instruction (CLI).

NOP
causes the program counter to be incremented without affecting any of the other registers. It is useful during program development as a "stand-in" for some other instruction that is to be determined during debug, and also for equalising execution time through alternate paths in a control program.

## IMMEDIATE ADDRESSING MODE

In this addressing mode the operand immediately follows the op code, and may consist of one or two bytes. Two byte operands are only used for instructions relating to the index
register and stack pointer (CPX, LDX, LDS). In all other cases a single byte follows the op code. Examples of immediate addressing are:

LDA AFF this instruction loads register A with the value FF (the instruction would be coded as 86 FF).
LDX 0300 this instruction loads the index register with the value 0300 (the instruction would be coded as CE 0300 ).

## DIRECT ADDRESSING MODE

Using this mode of addressing the operand of the two-byte instruction is stored in a memory location with an address which has a most significant byte equal to 00, and the least significant byte equal to the second byte of the instruction. With direct addressing, the valid memory address range is 0000 to OOFF, and consequently only a restricted range of memory is accessible. This addressing range falls within the user RAM area of the Microcontroller.

Examples of the use of direct addressing are:
LDA A 43 this instruction loads the contents of location 0043 into register A (the instruction op code would be 9643 ).
CMP B BC this instruction compares the contents of register $B$ with the contents of memory location $O O B C$, and sets the condition code register bits as appropriate (the instruction op code would be 91 BC ).

## EXTENDED ADDRESSING MODE

In this mode the memory address of the operand is specified by the second and third bytes of the instruction. The most significant byte of the memory address is specified by the second byte of the instruction, and the least significant byte of the memory address is specified by the third byte. Instructions using the extended addressing mode are able to access the full 64 K bytes of the 6800 's address range, i.e. 0000 to FFFF. Examples of instructions using the extended addressing mode are:

LDA B OOBC this instruction loads register $B$ with the contents of memory location OOBC (the instruction op code would be F6 00 BC ). Note that this instruction would use only 2 bytes if it used direct addressing, but is a valid instruction, nevertheless.
INC 03B7 this instruction increments by one the contents of memory location 03B7 (the instruction op code be 7 C 03 B 7 ).
LDX 01A5 this instruction loads the most significant byte of the index register with the contents of location 01A5, and the least significant byte with the contents of location 01A6 (the instruction op code would be FE 01 A5). Note that the index register, like the stack pointer, is a 16-bit register and requires 2 bytes of memory to specify its contents.

## RELATIVE ADDRESSING MODE

The relative addressing mode in the 6800 is used solely for branch instructions. These instructions allow the normal sequence of "one instruction following another" to be
changed, and enable the implementation of decision making in programs. The instructions used for branching are twobyte instructions. The first byte contains the opcode which specifies the branch condition (e.g. BCS is used to branch if the carry bit is set), and the second byte contains the offset.
The offset is a 2's complement 8 -bit number which is used to specify where the program will branch to if the branch condition is satisfied; in the example the branch will only occur if the carry bit is set when the instruction is encountered. The range of destination addresses is restricted to -7 D to +81 relative to the branch instruction (hence the name). This range results from the fact that, when the branch instruction is executed, the program counter will be pointing to the next instruction, which will be two bytes on from the branch code. If $A$ is the address of the branch instruction in memory, then the destination address, D, will be in the range:

$$
[(A+2)+7 F] \geqslant D \geqslant[(A+2)-80 \mid
$$

Two examples are given in Fig. 2.2 which illustrate how to calculate the two hex-digit offset value, J, which must be coded as the second byte of the branch instruction. With practice the values may rapidly be worked out by mental arithmetic!

## INDEXED ADDRESSING MODE

Indexed addressing involves 2-byte instructions, and makes use of the contents of the 16 -bit index register, in addition to op code, to specify the address of the source/destination of the instruction operand.

The address is calculated by taking the contents of the in-


Fig. 2.2. Calculation of branch offset values
dex register and adding the offset value contained in the second byte of the instruction. For example, if the current contents of the index register are 0300, an instruction of STA A $27, X$ (coded as A7 27) would result in the contents of register $A$ being stored in memory location 0327. The offset in the second byte of the instruction may take any value in the range 00 to FF , and is assumed to be positive. The index register is unaffected by indexed instructions; thus STA A 27,X followed by STA B $28, X$ would result in registers $A$ and $B$ being stored in locations 0327 and 0328, respectively.

Special instructions are provided for loading, manipulating and storing the contents of the index register, as used by the indexed addressing modes of instructions. Typical instructions relating to the index register are LDX, INX, DEX, and STX. The use of indexed addressing is particularly useful for manipulating tables, and for jumping to addresses picked up from tables/memory locations (JMP nn, $X$ and JSR nn, X); this is a technique much used internally by DISBUG.

## THE STACK

The 6800 uses part of its read/write memory to implement a stack. This stack is used for:
(a) storing subroutine return addresses
(b) temporary program data storage
(c) storage of CPU status (register contents) while responding to interrupts.
The stack works on a last-in first-out (LIFO) principle and a stack pointer ( 16 bits) is provided in the CPU to indicate the address of the next free stack location. When data (e.g. a return address) is "pushed" onto the stack, the stack pointer is decremented by the number of bytes pushed (e.g. two for a return address). When data is "pulled" from the stack, the stack pointer is correspondingly incremented.

The stack pointer must be initialised (via the LDS instruction) to the start (top) of the stack area. The amount of RAM allocated for stack operations must allow two bytes for each nested subroutine call, and seven bytes for each category of concurrent interrupt (NMI, IRQ, SWI). Additional allowance must be made if the stack is to be used for temporary variable storage (via PSHA and PSHB). Every stack push must have a corresponding stack pull if the stack is not to extend indefinitely! Once initialised, maintenance of the stack pointer is performed automatically by the CPU.

## GETTING STARTED

A practical demonstration of programming the Microcontroller concludes the second part of this series. The program which is presented is used as a means of demonstrating the operation of DISBUG. However, it is not expected that readers will fully understand the detailed operation of the program since it uses a number of subroutines which are contained within DISBUG itself. In the next issue further examples of programs will be presented to illustrate how control programs may be constructed. Once the user has become familiar with the way in which programs are entered and controlled, it is but a short step to write a PIA control program. The sample program is:-

| Address | Instruction Mnemonic |  |  |  | Op Code |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0000 | LDA | A | \# | 15 | 86 | 15 |  |
| 0002 | JSR |  |  | F9BD | BD | F9 | $B D$ |
| 0005 | CLR |  |  | 03FA | 7F | 03 | FA |
| 0008 | LDX |  | \# | 03FB | CE | 03 | FB |
| 000B | LDA | A |  | O3E3 | B6 | 03 | E3 |
| O00E | JSR |  |  | F8F7 | BD | F8 | F7 |
| 0011 | LDA | A |  | 03E2 | B6 | 03 | E2 |
| 0014 | JSR |  |  | F8F7 | BD | F8 | F7 |
| 0017 | JSR |  |  | F814 | BD | F8 | 14 |
| 001A | BRA |  |  | E4 | 20 | E4 |  |

When the Microcontroller is switched on, DISBUG outputs a display of "dIS r1.0" for approximately 2 seconds. After this time, the display changes to the normal prompt of ". . . dIS . . ." to indicate that DISBUG is awaiting a user command from the keyboard. The memory editor is used to enter programs into the user RAM area of memory. The sequence of keystrokes required to enter the demonstration program is as follows:


## EG985

The program is now stored in RAM. To demonstrate the use of the breakpoint editor, a breakpoint will now be placed at the end of the loop at location 001A. This is done as follows:

KEYSTROKE(S)
DISPLAY
...dis...
BREAKPOINT
A-FFfF-bo

A- $00-60$

A-001A-b0
ENTER ...dIS

## E6982

The program is now run from the start address (0000) as follows:


E9983
The display will now go blank, flash briefly, and then return with a display of "E-001A-bP" to indicate that it has found the breakpoint at location 001A. Pressing the ENTER key will cause ". . . dIS . . ." to reappear. The PROCEED key is then struck to request that the program continue from the breakpoint:

$$
\begin{gathered}
\ldots . . d I S \ldots \\
E-001 A-P r
\end{gathered}
$$

## EG986

The program will then restart from location 601 A . The display will go blank for a short period, and then a four-digit running seconds count will appear in the centre of the display. The program, which uses the 1 second reat time clock interrupt, must be stopped by interrupting the power.

P.s.u. board


## POWER SUPPLY

The power supply provides the following outputs which are required for the Microcontroller:
(a) +12 V high current supply (unregulated) for the four output interface buffers. Unloaded output is approximately 17 V .
(b) +5 V regulated supply for the CPU, RAM, ROM system clock, and control logic
(c) +40 V supply for the gas discharge display
(d) 4.6 V a.c. for the display filament.

In addition to the above supply rails, logic control signals are provided for detecting the presence of low-voltage or mains failure conditions.

The mains transformer has two series-connected 110 V primary windings and two separate secondary windings. One of these provides 12 V at approximately 2 A for the bridge rectifier arrangement formed by D4, D5, D6 and D7. The other secondary winding provides approximately 17 V at 0.5 A and is not used in the basic Microcontroller system. It may, however, be used in conjunction with ancillary equipment or for system expansion.

The complete circuit diagram of the Microcontroller power supply is shown in Fig. 2.3. The unregulated d.c. output from the bridge rectifier is developed across reservoir capacitor, C1, and additional high frequency decoupling is provided by C18. The regulator operates on the switched mode principle with series-pass transistor, TR2. IC1a is connected as an oscillator which produces a square wave output at approximately 33 kHz . The output of this oscillator is inverted by means of the comparator formed by IC1b. Overcurrent protection is provided by means of TR1 which effec-
tively turns off the comparator stage. The output current is sampled by means of the voltage drop developed across R9 and trip operates at a load current of approximately 1.5 A .

The voltage reference for the supply regulator is provided by D8 and associated components. Potentiometer, R2, provides accurate adjustment of the reference voltage to 5 V . The reference voltage is compared with the output voltage of the supply using the comparator arrangement formed by IC2. Feedback components, C6 and R16, improve the stability of this stage.

Failure of the supply mains is detected by a further comparator arrangement formed by IC1a. Low voltage detection is similarly provided by IC1d. Both the mains failure and lowvoltage control signals are used in the Microcontroller RAM control logic.

A simple inverter arrangement is used to provide the +40 V rail. TR5 and TR6 are connected as an astable oscillator which operates at 12 kHz and is gated by means of TR7. The secondary of the inverter transformer feeds the bridge rectifier, D12, D13, D14 and D15. Positive feedback to the bases of TR5 and TR6 is by means of two further secondary windings and these are also used to provide the 4.6 V a.c. filament supply. The display is enabled by a logic 'high' which turns TR4 and TR7 'on'. Note that R22 acts as a pull-up which ensures that the inverter supply operates when the power supply is disconnected from the Microcontroller.

NEXT MONTH: Programming the PIA's, writing control programs, controlling peripheral hardware and sample applications.

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Now, the British Library is publishing a series of newsletters, called PIN Bulletins, which deal with interesting and important patents in popular and topical subject areas. These bulletins can be a very valuable short cut. Bulletin No. 2, for instance, discusses the patents on the Sinclair flat screen television research. Bulletin No. 3 looks at the patent coverage on Prestel-Viewdata, the war-time Enigma coding machines and satellite data communications. You can get copies of the PIN Bulletins free, from any of the libraries in the Patents Information Network. In practice this means any large library which keeps copies of published patents.

## THE CRANFIELD PATENT

There's an interesting story behind British Patent 1394 291. It was applied for in February 1972, by the Cranfield Institute of Technology, with Jack Dinsdale named as inventor. Dinsdale is a lecturer at Cranfield and hi-fi enthusiast, who had invented a clever bearing for a gramophone turntable. The patented bearing is like a fairly loose fitting piston and cylinder arrangement, but with helical grooves cut in the mating cylin-
drical surfaces. The bearing is filled with oil and when the central piston part (which carries the gramophone turntable) is rotated, the helical grooves create a hydrodynamic thrust which pumps the oil downwards. So the rotating parts float on oil. If the spindle is turned in the opposite direction the oil is pumped upwards and the bearing locks like a brake.

The patent application was accepted and published by the British Patent Office in May 1975 and in December that year Cranfield sold the patent rights to Plessey, then the parent company of hi-fi manufacturer Garrard. The sale price was said to be $£ 5,000$. At that time hi-fi sales were still reasonably strong and Garrard was a major name in British hi-fi. Garrard planned to incorporate the Cranfield bearings in a new, top range turntable. But hi-fi sales slumped and so did Garrard's fortunes. No turntable with the Cranfield bearing ever appeared. But even after Plessey shed loss-making Garrard, the Ilford company kept on paying the annual renewal fees necessary to keep the Cranfield patent in force. This has prevented other manufacturers from using the idea.

The Rock turntable made by Elite Townshend of Walton-on-Thames incorporates other Cranfield technology, such as artificial granite material for damping and a viscous fluid damped pickup arm. But Cranfield could not license Elite Townshend to use the patented bearing and had to design another, which relies on a cup of PTFE. It's unclear why Plessey kept the patent in force, because after the Garrard experience Plessey showed no further interest in hi-fi. Perhaps the patent was automatically renewed because no one thought to decide otherwise.

In April, 1982, however, Plessey sold the patent rights back to Garrard, for a nominal £ 1 . So it is now up to Garrard to keep the patent in force and this will entail paying over $£ 100$ a year in renewal fees. After being sold off by Plessey, Garrard was bought by the Brazilian company Gradiente Electronica, but the future of Garrard is again in doubt. The company pulled out of the 1982 Harrogate International Festival of Sound and Video at the last minute, leaving the official exhibition catalogue with a glossy advert for Garrard on the front page, but no Garrard products on display. The next renewal fee for the Cranfield patent falls due for payment on February 2nd, 1983. Although there is a period of grace available for late payment it's likely that several hi-fi manufacturers will be checking with the Patent Office in February to establish
whether or not Garrard is still keeping the Cranfield patent alive.

## LOUDSPEAKERS

The Hohyu Rubber Company Ltd of Osaka, Japan has filed a British patent application for a new type of loudspeaker diaphragm. (2 087 688). Although patents for new speakers and new diaphragm materials, all supposedly offering perfect sound reproduction, are two a penny, this Japanese proposal is worth noting because of its radical thinking. This is probably due to the fact that the applicants are primarily involved in rubber technology, rather than loudspeaker design.

Traditionally a loudspeaker diaphragm is built as light and rigid as possible, so that it moves as a piston without isolated vibrations which cause cone breakup. The Japanese here suggest that this approach should be abandoned. Instead the diaphragm should be made of cured rubber with a very low rigidity so that it can vibrate freely, and not as a piston. The inventors liken their new cured rubber diaphragm to "artificial vocal cords".

Various rubber materials are listed, all highly flexible and formed by moulding and heat-curing under pressure. According to the patent the conventional diaphragms were stripped out of a three-way hi-fi speaker system and replaced by samples of the new floppy rubber units. Signals were then fed in from a hi-fi system (Sansui amplifier, Denon turntable and Shure V-15 type III cartridge) while a panel of "four trained listeners" made notes. Whereas the original system sounded only "ordinary" the system modified according to the invention sounded consistently "excellent".

European Patent Application 0054945 from the Nissan Motor Company offers a high level of sound in a motor car from a small loudspeaker drive unit. Most in-car systems, especially budget units factoryfitted prior to sale, rely on small loudspeaker drive units mounted in the door panels. These easily overload when the system is played loud, for instance on a motorway. They are also prone to irritating cavity resonances at specific frequencies in the high bass range. Nissan suggests the answer is to join the resonance problem rather than fight it. Instead of using a conventional loudspeaker, with drive coil and diaphragm, the Nissan unit has a driver which is coupled directly to a panel of the vehicle. So the vehicle panel acts as a diaphragm. Obviously the system is usable only at fairly low frequencies.

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[^3]
## UNIVERSAL PROBE

THIS unit consists of a square wave generator with a 27 kilohm output resistance. The frequency of oscillation is about 1 kHz .
Tracing is done through an operational amplifier with a gain of about 2.2. Further gain is oblained by use of TR2 which drives an earphone. This should be mounted on the circuit board, inside the unit, to avoid too many umbilical cords. The sound tube on the earphone should be removed. If low level signals, with a d.c. component, are to be traced, C4 and S3 provide decoupling of the input probe. This may load some high impedance circuits but is not likely to prevent testing for most applications.

S4 allows the unit to be switched from an analogue function to a digital function. It should be noted that for most digital uses, S3 should remain open.

The input voltage is fed to the inverting input of the 741 , so that the output is normally high. As the input voltage of the amplifier rises, so the output voltage falls; as decided by the amplifier gain R11/R8. The high to low transition of the gates in IC3, was found to be approx. 3.6 V ; but if this varies, R11 can be set accordingly. When the output of the 741 falls below 3.6 V the flip flop of IC3 changes state, and a logical high is indicated. Variations exist at the construction stage-precise voltage level change may be obtained by using a Schmitt device in place of IC3. The input voltage that causes a logical ' 1 ' to be indicated can be altered by changing R11. If R11 is reduced, the gain of the amplifier is reduced, and so the input voltage level which is necessary to cause a low to high change will rise. The object of the universal instrument is to use a voltage level suited to both TTL and CMOS.

As mentioned previously in the article, the Universal Probe may be used for other-more diverse applications. When S2 is open, the output lead, through R3 and R4, is at a logical ' 1 ' and so if used in conjunction with the input probe (Set to 'Logic' mode), continuity tests on high resistance circuits can be made; e.g. the instrument indicates logical ' 1 ' if the circuit is continuous.


If the output lead were connected to one side of a good capacitor and the input probe to the other side, the logical ' 1 ' indicator may flash momentarily but logical ' 0 ' should prevail. If now the 'Push to Send' button is pressed, an alternating current will pass through the capacitor and the logic l.e.d.s will indicate pulses. This test could be done with the unit set to 'Trace' and an audible indication of capacitor operation will follow. The square wave contains some high frequency harmonics so most capacitors can be tested in this way. High value electrolytic capacitors may take some time to charge through R3 and R4 before a logical ' 0 ' is shown. This fact could be used to estimate the value of an electrolytic capacitor. The
unit should be calibrated with certain known values. Charging time to 1.5 V can be counted since it will take 10 s of seconds and differences will be noticed between capacitors of different sizes.

Semiconductor components may also be tested using the logical high at the output lead, and the input probe. Diodes will conduct and show a logical ' 1 ' when the output lead is connected to the anode and input probe to the cathode. Where reverse connection is made a logical ' 0 ' will result. Transistors may be tested in a similar way-testing base-emitter, base-collector junctions.
J. L. Gordon,

St. Helens,
Merseyside.

THE circuit shown is a Disco Lights Sequencer with four channels rated at whatever wattage the user chooses. The unit, as well as having the standard " 1 bulb on, 3 bulbs off' operating mode has, in addition, two other operating modes, which makes it considerably more versatile and yet cheaper than the expensive units that are bought commercially.

The two new modes are:
(a) An invert mode where instead of " 1 on, 3 off" there is the converse mode of " 3 bulbs on, 1 bulb off" which gives a higher ambient light level.
(b) A pulse/chain mode which gives a pronounced effect of the bulbs being pulsed rather than the usual ef fect of switching instantaneously from one bulb to the next and results in a very convincing stroboscopic effect being obtained. This strobe effect is greatly enhanced if different coloured bulbs are used and an exciting strobe lighting display occurs when fast, lively disco music is being played.
From the technical viewpoint the circuit features some distinct advantages over some commercial units. It has zero voltage switching so essential if r.f.i. is to be avoided and has the unique feature of powering the bulbs on both the positive and negative swings of the mains supply which means that the bulbs have full power and give full illumination in contrast with many commercial units that supply only half-wave to the bulbs. In addition,

## DISCO LIGHTS SEQUENCER


there is the all important safety aspect, because many commercial units require their circuitry to be live and so are inherently dangerous; however, the design given here has its circuitry tied to the neutral rail
and so the circuitry is harmless if accidentally touched.
P. McChesney,

Wirral,
Merseyside.


SONY TC377 open reel stereo recorder, mixing, s.o.s. echo f 120 . Swap UK 101 plus/or expansion, printer etc. Mr. M. A. Saunders, 7 Drumcliff Road, Thurnby Lodge, Leicester LE 5 2LH
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WANTED. Charger and instruction manual for Tandy TRS 80 Printer cassette interface. Mr. K. Wenman. 2 Hythe Road, Sittingbourne, Kent
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# Sinclair ZX Spectr 

## 16Kor 48K RAM... full-size movingkey keyboard... colour and sound.... high-resolution graphics...

 From only £125!First, there was the world-beating Sinclair ZX80. The first personal computer for under $£ 100$.

Then, the ZX81. With up to 16K RAM available, and the ZX Printer. Giving more power and more flexibility. Together, they've sold over 500,000 so far, to make Sinclair wortd leaders in personal computing. And the $\mathrm{ZX81}$ remains the ideal low-cost introduction to computing.

Now there's the ZX Spectrum! With up to 48 K of RAM. A full-size moving-key keyboard. Vivid colour and sound. High resolution graphics. And a low price that's unrivalled.

## Professional powerpersonal computer price!

The ZX Spectrum incorporates all the proven features of the ZX 81 . But its new 16K BASIC ROM dramatically increases your computing power.

You have access to a range of 8 colours for foreground, background and border, together with a sound generator and high-resolution graphics.

You have the facility to support separate data files.

You have a choice of storage capacities (governed by the amount of RAM). 16 K of RAM (which you can uprate later to 48 K of RAM) or a massive 48 K of RAM.

Yet the price of the Spectrum 16K is an amazing $£ 125$ ! Even the popular 48 K version costs only $£ 175$ !

You may decide to begin with the 16 K version. If so, you can still return it later for an upgrade. The cost? Around $£ 60$.

## Ready to use today, easy to expand tomorrow

Your ZX Spectrum comes with a mains adaptor and all the necessary leads to connect to most cassette recorders and TVs (colour or black and white).

Employing Sinclair BASIC (now used in over 500,000 computers worldwide) the ZX Spectrum comes complete with two manuals which together represent a detailed course in BASIC programming. Whether you're a beginner or a competent programmer, you'll find them both of immense help. Depending on your computer experience, you'll quickly be moving into the colourful world of ZX Spectrum professional-level computing.

There's no need to stop there. The ZX Printer-available now - is fully compatible with the ZX Spectrum. And later this year there will be Microdrives for massive amounts of extra on-line storage, plus an RS232 / network interface board.


## Key features of the Sinclair ZX Spectrum

- Full colour-8 colours each for foreground, background and border, plus flashing and brightness-intensity control.
- Sound-BEEP command with variable pitch and duration.
- Massive RAM-16K or 48K.
- Full-size moving-key keyboard- all keys at normal typewriter pitch, with repeat facility on each key.
- High-resolution-256 dots horizontally $\times 192$ vertically, each individually addressable for true highresolution graphics.
- ASCll character set - with upper- and lower-case characters.
- Teletext-compatible-user software can generate 40 characters per line or other settings.
- High speed LOAD \& SAVE-16K in 100 seconds via cassette, with VERIFY \& MERGE for programs and separate data files.
- Sinclair 16K extended BASICincorporating unique 'one-touch' keyword entry, syntax check, and report codes.



## The ZX Printeravailable now

Designed exclusively for use with the Sinclair ZX range of computers, the printer offers ZX Spectrum owners the full ASCII character set-including lower-case characters and high-resolution graphics.

A special feature is COPY which prints out exactly what is on the whole TV screen without the need for further instructions. Printing speed is 50 characters per second, with 32 characters per line and 9 lines per vertical inch.

The ZX Printer connects to the rear of your ZX Spectrum. A roll of paper ( 65 ft long and 4in wide) is supplied, along with full instructions. Further supplies of paper are available in packs of five rolls.


## The ZX Microdrivecoming soon

The new Microdrives, designed especially for the ZX Spectrum, are set to change the face of personal computing.

Each Microdrive is capable of holding up to 100 K bytes using a single interchangeable microfloppy.

The transfer rate is 16 K bytes per second, with average access time of 3.5 seconds. And you'll be able to connect up to 8ZX Microdrives to your ZX Spectrum.

All the BASIC commands required for the Microdrives are included on the Spectrum.

A remarkable breakthrough at a remarkable price. The Microdrives are available later this year, for around $£ 50$.


## RS232/network interface board

This interface, available later this year, will enable you to connect your ZX Spectrum to a whole host of printers, terminals and other computers.

The potential is enormous. And the astonishingly low price of only $£ 20$ is possible only because the operating systems are already designed into the ROM.

## ZX Spectrum

## Available only by mail order and only from



Sinclair Research Ltd,
Stanhope Road, Camberley.
Surrey, GU15 3PS
Tel: Camberley (0276) 685311

## How to order your ZX Spectrum

BY PHONE-Access, Barclaycard or Trustcard holders can call 01-200 0200 for personal attention 24 hours a day, every day. BY FREEPOST-use the no-stamp needed coupon below. You can pay by cheque, postal order, Access,

Barclaycard or Trustcard. EITHER WAY-please allow up to 28 days for delivery. And there's a 14-day money-back option, of course. We want you to be satisfied beyond doubt - and we have no doubt that you will be.

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|  | $3 \times 015$ <br> 30016 | $22 \cdot 22$ $25 \cdot 25$ | - 181 | -0/95167 | 110 2650 mm | 7x014 | $10+18$ $22+22$ | ( $\begin{aligned} & 83 \\ & 682\end{aligned}$ |  |
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|  | 3*028 | 110 | 072 |  | 6\% | $7 \times 017$ | $30+30$ | 5.00 |  |
|  | 3x029 | 220 | 036 |  |  | 7x018 | $35+35$ | 4.28 |  |
|  | 34030 | 240 | 033 |  |  | 7x026 | 40+60 | ${ }^{3} 15$ |  |
| $\begin{gathered} 120 \mathrm{VA} \\ 90 \times 1 \mathrm{mmm} \\ \times 2 \mathrm{~mm} \\ \text { Regulation } \\ 11 \% \end{gathered}$ | $4 \times 10$ | 5.6 | 1000 |  |  | $7_{8003}$ | 50+50 | 3.00 |  |
|  | 48014 | 9*9 | 666 |  |  | $7 \times 028$ | 110 | 272 |  |
|  | $4 \times 012$ | 12-12 | ${ }^{5} 00$ |  |  | $7 \times 029$ | 220 | 1 36 |  |
|  | $4 \times 013$ | 15+15 | 400 3 3 3 | $\underline{6.90}$ |  | $7 \times 030$ | 240 | + 25 |  |
|  | ${ }_{4}{ }_{4 \times 014}$ | $18+18$ $22+22$ | 272 | -.9106167 | 500 VA | $8 \times 016$ | $25+25$ | 1000 |  |
| $160 \mathrm{VA}$ $\begin{gathered} 10 \times 1 \mathrm{~kg} \mathrm{~m} \\ \hline \end{gathered}$ <br> Regulation | 4x016 | $25 \cdot 25$ | 240 | -vatcios | $140 \times 60 \mathrm{~mm}$ | $8 \times 017$ | 30.30 | 833 |  |
|  | $4 \times 097$ | $30+30$ | 200 | Toratay | ${ }^{4} \mathrm{~kg}$ | $8 \times 018$ | 35.35 | 714 | 13.53 |
|  | $4 \times 188$ $4 \times 028$ | $\stackrel{35}{1035}$ | 1717 |  | Reguialion | 88026 | 40+40 $45 \cdot 45$ | 6.25 5.55 | - bite |
|  | 4×029 | 220 | 054 |  |  | ${ }_{8 \times 033}$ | 50 050 | 5.00 | -vat |
|  | 4×030 | 240 | 050 |  |  | $8 \times 042$ | $55+55$ | 154 | 'OTALETE 76 |
|  | $5 \times 011$ | 9.9 | ${ }^{9} 89$ |  |  | $8 \times 028$ $8 \times 029$ | 110 220 | 4.4 2.27 2 |  |
|  | $5 \times 012$ | $12 \cdot 12$ | 666 |  |  | ${ }_{8 \times 0}^{80}$ | 240 | 208 |  |
|  | ${ }_{5 \times 013}$ | ${ }_{15}+15$ | 533 |  |  |  |  |  |  |
|  | 5x014 $5 \times 015$ | $18 \cdot 18$ $22 \cdot 22$ | 444 <br> 363 | 27.91 | ${ }_{140 \times 75 \mathrm{mma}}^{625}$ | $\left\lvert\, \begin{aligned} & 9 \times 017 \\ & 9 \times 018\end{aligned}\right.$ | $30+30$ $35+35$ | 1041 882 |  |
|  | 5x016 | $25 \cdot 25$ | 320 | -0,08167 | 10. kg | ${ }^{9 \times 026}$ | 40+40 | 181 | .13 |
|  | $5 \times 017$ | $30+30$ | 256 | - wat 11.4 | Aegularion | $9 \times 025$ | 45*45 | 634 | - pingase |
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