Low-price robots from POWERTRAN

- hydraulically powered
- microprocessor controlled

The UK-designed and manufactured range of Genesis general purpose robots provides a first-rate introduction to robotics for both education and industry. With prices from as low as £425, even the home enthusiast can aspire to his or her own robot.

Each robot in the Genesis range has a self-contained hydraulic power source operated from single phase 240 or 120v AC or from a 12v DC supply. Up to six independent axes are capable of simultaneous operation and all except the grip axis have sensing devices fitted to provide positional control by a closed loop system based on a dedicated microprocessor. Movement sequences can be programmed by means of a hand-held controller or the systems can be interfaced with an external computer via a standard RS232C link.

The top-of-the-range P102 has dual speed control, enhanced memory and double-acting cylinders for increased torque on the wrist and arm joints. There is position interrogation via the RS232C interface, increasing the versatility of computer control and inputs are provided for machine tool interfacing.

All Genesis robots are available either ready-built or in kit form. The latter provides not only extra economy but also valuable additional training as an assembly project.

HEBOT II
Turtle-type robot

For under £100, Hebot II takes programming off the VDU and into the real world. Each wheel is independently controlled by a computer, enabling the robot to perform an almost infinite number of moves. It has blinking eyes, a two-tone bleep and a solenoid-operated peristaltic arm movements. Touch sensors coupled to its shell return data about its environment to the computer enabling evasive or exploratory action to be calculated.

The robot connects directly to an I/O port or, via the interface board, to the expansion bus of a ZX81 or other microcomputer.

HEBOT II
Weight 1.91kg
complete kit with assembly instructions £85
Interface board kit £10

MICROGRASP

A real, programmable robot for under £200! Micrograsp has an articulated arm jointed at shoulder, elbow and wrist positions. The entire arm rotates about its base and there is a motor-driven gripper. All five axes are motor-driven and four of these are servo controlled giving positive positioning. The robot can be controlled by any microcomputer with an expansion bus – the Sinclair ZX81 being particularly suitable.

MICROGRASP
Weight 8.7kg, max. lifting capacity 10kg
Robot kit with power supply £145.00
Universal computer interface board kit £48.50
23 way edge connector £2.50
AX81 peripheral/RAM pack £48.50
Splitter board £3.00

GENESIS S101
Weight 29kg, max lifting capacity 1.5kg
4-axis model (kit form) £425
5-axis complete system (kit form) £737

GENESIS P101
Weight 34kg, max lifting capacity 2kg
6-axis model (kit form) £675
6-axis complete system (kit form) £945

GENESIS P102
Weight 36kg, max lifting capacity 2.8kg
6-axis system (kit form) £1175.00
Powertran Cortex microcomputer self-assembly kit £295.00

POWERTRAN cybernetics ltd.
PORTWAY INDUSTRIAL ESTATE, ANDOVER, HANTS SP10 3PE. TEL (0264) 64455

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SPECTRUM AUTOSAVE by R. A. Penfold
Automatic cassette control unit for the Spectrum

ANTI THEFT ALARM by M. Tooley BA and D. Whitfield MA MSc CEng MIEE
Audio and visual protection unit for property or goods

COMPUTER TERMINAL Part 2 by Ray Stuart
Construction and use

EXPANDING THE VIC 20 Part Five by Sam Withey
Two stepper motor drivers

GENERAL FEATURES

SEMICONDUCTOR CIRCUITS by Tom Gaskell BA(Hons)
Tachometers (LM 2917N–8 and LM 2917N)

VERNEN TRENT AT LARGE

MONITORS FOR HOME COMPUTERS by M. Tooley BA and D. Whitfield MA MSc CEng MIEE
A review of two commercial monitors

INMOS by Tom Ivall
The UK semiconductor company in detail

INTRODUCTION TO DIGITAL ELECTRONICS by M. Tooley BA and D. Whitfield MA MSc CEng MIEE
Part 6 of our electronics course

MICRO-BUS
A monthly focus on micro's for the home constructor

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INDUSTRY NOTEBOOK by Nexus
News and views on the electronics industry

SPECIAL OFFER-CASSETTES

READOUT

SPACEWATCH by Frank W. Hyde
The European Space Station Project

SPECIAL SUPPLEMENT

MICRO-FILE by R. W. Coles
Filesheet 14 8073
between pages 34 and 35

OUR APRIL ISSUE WILL BE ON SALE FRIDAY, MARCH 2nd, 1984
(for details of contents see page 14/6 of Micro-file)
**COMPUTER CORNER**

- SEIKOSHA GP100A - Unihammer Printer, normal & double width characters, dot resolution graphics 10" Tractor feed, parallel interface standard. **£185**
- SEIKOSHA GP 250X Printer **£199**
- EPSON FX80 PRINTER 160 CPS, 11x9 matrix, proportional spacing, superscript, subscript, dot addressable, italic & Emu cour-acters. Up to 256 user definable characters. Down loading of graphics & fonts. 2X, 3X, 6X drive, high speed printing. 4 user defined margin positions. Tractor and Friction feed. 10" maximum width, bi-directional, logic seeking. Centronics Interface standard. **£345**
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- EPSON RX 80 FT PRINTER **£259**
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- Connecting lead for KAGA monitors **£215**
- ZENITH 12" Hi-RES, Green Monitor 40/80 K. **£140**
- MICROVITEC 14" colour monitor. RGB input lead. **£205**
- MICROVITEC 1451 Hi-res 14" Monitor incl. Lead. **£70**
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The power amp kit is a module for high power applications - disco units, hi-fi amplifiers, public address systems and even high power domestic systems. The unit is protected against short circuiting of the load and is safe to use in normal household conditions. A large safety margin exists by use of generous rated components, resulting in a high powered rugged unit. The P.E. FM/AM back printed kit with transformer: (10.50 plus £2.00 p&p. £17.50 + £1.75 p&p.

This audio cassette recorder offers full UHF coverage with pre-selected tuning controls. It can also be used in conjunction with your video recorder. Dimensions: 10½" x 7½" x 2½".
BRITAIN'S FUTURE

Does Britain have an independent future in high technology? Has £50m of public money assured the UK of its own chip maker? Will the Transputer put the UK ahead of the world in electronics?

There are no single word answers to these questions but the answers could be vital to the future UK economy. Just recently the name of Inmos has been hitting the headlines again for a number of reasons not the least being their incorporation, names like Philips, SGS, Fujitsu and Western Electric have also been reported. Inmos was the subject of much press comment back in '79 and '80 when the 'new' Government hesitated about providing its second £25m.

In the October 1980 issue of PE Nexus wrote the following words "As I write there is still no decision on Inmos an ominous sign reflecting lack of enthusiasm for, if not imminent abandonment of, Government (i.e. taxpayers) support." Within a week or two of that being written the Government (i.e. taxpayers) did cough up and Inmos was away, albeit after losing a valuable six months waiting for a decision. Over the last three years Inmos has quietly built a reputation in the industry for technical excellence and has proved its ability to process high volume chips at Newport; surely it would be madness to let it slip into foreign ownership now.

Sir Clive Sinclair recently predicted that a "wall of secrecy" will soon be built around high tech. research and he went on to add "Either we get ourselves back into the hardware business or we're out of the game."

Sir Clive suggested that hardware and software would be so closely related that to ensure our ability to stay in the field, and not be reliant on foreign manufacturers, we must develop both. He stressed the "very serious implications" if Inmos was allowed to be bought by a non-UK company.

With this background PE has commissioned Tom Ivall to look at Inmos and its first five years. The article does not provide straightforward answers to the above questions but it gives clear indications of where the UK chip maker is now, how it got there and where it might go in the near future.

TRANSPUTER

The future of Inmos is closely tied up with the Transputer so in order to round off the scene we also commissioned Ray Coles (who writes Micro-File) to take an in depth look at this exciting device. The Transputer article will be published next month in place of Micro-File.

These two articles should interest anyone involved in electronics at any level, because of the implications outlined above, make sure you read them.

Incidentally Sir Clive is not slow in developing new products—see News and Market Place for details of his new computer.
SINCLAIR'S QUANTUM LEAP

You are probably going to see the computer shown here a great deal over the next few years. It's Sinclair's new QL (Quantum Leap, would you believe) the name is perhaps OTT but then so is the computer. Based on the Motorola 68 008 32 bit chip the QL has 128K of usable RAM (up to 32K can be required from a screen bit map) extendable up to 640K, and 32K of ROM extendable up to 64K containing a new "Sinclair Super BASIC" and Sinclair QDOS operating system.

The unit has a full size "proper" keyboard, two 100K microdrives built-in and sockets for microdrive extension (up to six extra drives), local area network, RGB monitor port, u.h.f. tv port, two standard RS-232-C sockets, two joysticks sockets, ROM cartridges slot and expansion slot for extra memory or peripherals.

Planned enhancements under development are: PASCAL compiler, 68000 assembler, terminal emulator, 0:5mb memory expansion, A to D converter, Winchester interface, modem, parallel printer interface and IEEE-488 interface.

Super BASIC is said to be a radical enhancement of Spectrum BASIC, and QDOS is a new Sinclair development which allows single-user multiple tasking, time sliced priority job scheduler, display handling for multiple screen windows and device-independent I/O.

The QL comes complete with an extensive manual in an A4 ring binder, a 1.8A power supply, a suite of four software programs on microdrive cartridges and four blank cartridges. The software supplied has been developed by Psion and is claimed to "completely out perform existing software for micro's" it comprises QL Abacus for spreadsheet analysis, Archive or database management, Easel for graphics and Quill for word processing. All are said to be immediately usable and very advanced, so much so that it is claimed "you probably won't refer to the manual!"

All this is provided for £399 including VAT; by mail order only at present. Other things that may be of interest are: The 68008 runs at 7.5MHz and a second processor (Intel 8049) controls keyboard, sound. RS-232-C receive and real time clock functions.

FOOD FOR THOUGHT

It is unlikely that Ocean Software have bitten off more than they can chew with 'Mr Wimpey', a new game for the 48K Spectrum, indeed it looks like a recipe for success.

The game involves a culinary concoction of ingredients pinching nasties who constantly hamper the player's attempts to assemble hamburgers. The program also incorporates the company logo and jingle.

Even if this first UK company commissioned program does not go down well the business principle behind it certainly will. In the USA company sponsored games are already big business, the advantages are obvious if the games climb high in the popularity charts. This will certainly be the first of many such attempts by companies to cash in on the infinite commercial possibilities within the home computer market. Interesting variations spring to mind, who knows what AndrEx could come up with.

'Mr Wimpey' is written in 100% machine code and has hi-res graphics and sound. It can be snapped up from leading stores for around £5:90 and will shortly be available for the Commodore 64K.

MULTI-FUNCTION KEYBOARD

The Concept keyboard is a new approach to educational computing, allowing easier pupil-computer integration.

The Concept keyboard takes interchangeable A4-size overlays which define the number, shape, size, colour, position and legend of the keys. Each program can use a separate overlay, with keys appropriate to the application. The ability to respond directly to programmed questions, via keys labelled 'Yes', 'No', 'True', 'False' for example, greatly improves pupils' interaction with the computer.

The keys can be made large enough to allow operation by visually or physically handicapped pupils.

The flat pressure-sensitive keyboard also gives great flexibility in designing teaching programs. A program to teach shopping skills, for example, could use a model trolley and an overlay showing the floor-plan of a supermarket with the various aisles and counters.

The Concept keyboard can be used with any microcomputer. It is of value in any educational application and special education where the normal QWERTY keyboard presents operating difficulties.

The keyboard has an 8x16 matrix of touch-sensitive areas, each producing a unique 7-bit ASCII code which the programmer defines as required. A bleeder with on/off control, and two additional user-dedicated touch pads, are also provided.

The price of the Concept keyboard (£91.00 ex VAT) includes full documentation and, for educational applications, a connecting lead for the majority of micros and a set of demonstration software.

Star Microterminals Limited, 22 Hyde Street, Winchester, Hampshire, SO23 7DR. (0962) 51422.
PICO-POWER

Probably the smallest power supply of its type available is the Picopac range from Rastra Electronics; these 1W mains packages would certainly fit into the proverbial matchbox.

The supplies feature small physical size (43.2 x 25.4 x 21.5mm) coupled with high reliability. Modules are available with inputs at 115/220V a.c. 50/60/400Hz and with single or dual outputs. Single outputs range from 5V to 24V d.c. the dual output type being +15V d.c. Since the units feature series regulation, the residual ripple is well under 1mV.

Despite the tiny size of these units the manufacturers claim an impressive 2kV a.c. isolation for 1 minute between primary and secondary. The Picopac is encapsulated and is intended for p.c.b. mounting. Prices however are not quite so small at £26 for the single and £42 for the dual output version, exc VAT. Details from Rastra Electronics Ltd, 275-281 King Street, Hammersmith, London W6 9NF (01-748 3143/2960).

Silicon News Corner

Zilog (Exxon) introduces 12MHz version of entire 28 micro family. Zilog (UK) Ltd., Zilog House, Moorbridge Rd., Maidenhead, Berks SL6 8PL.

OMRON Flat mini-sized relay uses "see-saw" system which is free from contact bounce and highly shock resistant. IMO Precision Controls. 1000 North Circular Rd., Staples Corner, London NW2.

Ti IMS1400M high performance 16K static RAM. 70ns CE access, 165mW standby power (660mW active). Single supply (5V). I/O is TTL compatible. Inmos, Whitefriars, Lewins Meads, Bristol BS1 2NP.

CTS101AGB is a high performance, general purpose op. amp. High gain, s/c protected, excellent temp. stability and simplified compensation. CTS0002GB buffer amp., high speed, high impedance follower. CTS0081B hybrid, high voltage, high current driver, DTL/TTL to 3A (pulsed) drive.

Inmos IMS2600 high performance 64K x 1 dynamic RAM. 100ns access, 22mW standby power (303W active). Single supply (5V) with on-chip refresh. I/O is TTL compatible. Bit & nibble mode capability.

Got any bright ideas? Unemployed? Live in London? The GLC are spending £40 million on a scheme to make University and Polytechnic equipment and know-how available to the public. Ideas can be brought to the prototype stage using the scheme which already has a list of new ideas including medical systems and a robot arm. It is hoped that jobs may ultimately be created to fill up some of the 33 million square feet of idle factory space in the capital.

Sixty of the world's top CMOS experts agree that Ultra Large Scale Integration will, within five years, allow chips with one billion transistors on them, to go into production. How this will be achieved is shrouded in some mystery, but Alan Aitken, of Mitel, has stated that ULSI is already possible, the only thing holding up production he said is the investment required to adapt existing equipment.

Briefly...

An electronic potato has been developed by the Scottish Institute of Agricultural Engineering in an attempt to reduce damage during mechanical processing.

The potato—a direct descendant of a similarly pseudo raspberry from the same stable uses an Entran accelerometer to gather information about the forces acting upon it during its automated journey. A v.h.f. transmitter sends out data from the foam potato to remote recording equipment.

It is hoped that the present day loss of over 10 per cent of the nation's maincrop will be reduced using data gleaned from this unlikely 'spudnik'.

Countdown...

Please check dates before setting out, as we cannot guarantee the accuracy of the information presented below. Note: some exhibitions may be trade only. If you are organising any electrical/electronics, radio or scientific event, big or small, we shall be glad to include it here. Address details to Mike Abbott.

Barclays Techmart Feb. 21-25. NEC, B/ham. J4

Eletrex Feb. 27-March 2. NEC, B/ham. L3

Hybrid Microtech Feb. 28. Cunard Int. Hotel, London. R2

Scotest March 6-8. Anderson Exhibition Cntr., Glasgow. T


Home Appliances International March 12-15. NEC, B/ham. M


Electro-Ops/Laser Int. March 20-22. Metropole, Brighton. T1

Information Technology (Conf. & Ex.) March 20-22. London. T

Scottish Computer Show March '84. Holiday Inn, Glasgow. T1


Micro City May 15-17. Exhibition Complex, Bristol. F3

Scotest June 5-7. Royal Highland Exhibition Halls, Inglisiston, Edinburgh. OS


Building & Home Improvement Sept. 25-30. Earls Court, London. M

D4 Network £0 280 815226

E Evan Steadman £0 799 26699

F3 Tomorrow's World £0 272 292156

J4 NEC £0 211 780 4141

L3 Electrex £0 483 22888

M Montbuild £0 4186 1951

O5 Institute of Electronics £0 706 43661

R1 Battery Vehicle Association. £ Brian Hampton, 0908 316991

R2 £0 89056 32746

T Trident £0 822 4671

T1 Cahners £0 483 38085

Z1 IPC £0 643 8040

Practical Electronics March 1984
THE popular Sinclair ZX Spectrum computer has a quite fast and efficient cassette interface, but it can be a little awkward to use. One reason for this is that problems can arise if the “Ear” and “Mic” sockets of the computer are both connected to their respective sockets on the cassette recorder, and for satisfactory results it is usually necessary to only connect the lead that is actually being used. Another problem is the lack of any automatic control of the cassette motor when loading and saving. This is not really too important when loading since the computer will continue to search until the program is found, giving the user unlimited time to load the cassette into the recorder and run it through to the beginning of the appropriate program. On the other hand, when saving a program it is very much easier if the cassette and recorder can be set up ready to record, and the computer will then automatically start the recorder, record the program, and switch the recorder off again.

SIMPLE AUTO SWITCH

The problem of having to unplug one lead and plug in the other, every time a change is made from loading to saving (or vice versa), is easily overcome by using a switch to disconnect whichever of the leads is not required. A simple way of providing an auto-save facility would be to have a switch which would activate the cassette motor when an output from the “Mic” socket of the recorder was detected. There would obviously be some slight delay between the start of an output from the computer and the recorder beginning to record properly, but the Spectrum precedes all data with a tone leader (to operate the auto recording level of the recorder), and in practice this system gives no loss of data.

This auto-save unit uses what is basically the system outlined above, as can be seen from the block diagram of the unit which is shown in Fig. 1.

A two pole switch is used to connect either the “Mic” lead or the “Ear” lead, depending on the mode of operation selected. A set of relay contacts control the cassette motor via the “Rem” (remote) socket of the recorder, and a third pole on the save/load switch is used to place a short circuit on the “Rem” output when the unit is in the “load” mode and the auto switching is inoperative. This also enables the recorder to be used in the fast forward and rewind modes without having to unplug the remote lead.

Although it might, on the face of it, appear that using a simple amplifier, rectifier, smoothing circuit, and relay driver would give satisfactory results and activate the relay in the presence of an output signal, in practice things are slightly less straightforward. The problem stems from the fact that signals other than the “save” signal are fed to the “Mic” socket. These come from the computer’s sound generator, and apart from the signal produced by BEEP commands there is also the signal generated each time a key is operated.

The problem is largely overcome by using a phase locked loop tone decoder to drive the relay. This does not respond to the short bursts of keyboard tone even if a number of them follow in rapid succession. It will respond to any signals within its narrow lock range that are caused by BEEP.
instructions, but this can be overcome by avoiding this small range of frequencies, and in practice the tape recorder would normally be switched off anyway when a program is running. It would therefore be irrelevant even if a spurious operation of the unit did occur.

It can be very helpful to monitor the output of the recorder when loading programs as it is then immediately obvious if a program is being fed into the computer but is failing to load, or if some other loading problem occurs. A loudspeaker is therefore used to monitor the signal being fed into the computer.

**THE CIRCUIT**

It will be apparent from the circuit diagram of Fig. 2 that the unit uses few components and has a very simple circuit.

IC1 is an NE567 PLL tone decoder, and as this requires an input signal of only about 20 millivolts r.m.s. no pre-amplification is required. However, as there is normally a very low input impedance at the microphone input of a cassette recorder, R1 is added in series with the output to the recorder to prevent loading from reducing the signal to an inadequate level. Of course, losses through R1 substantially reduce the signal level reaching the “Mic” input of the recorder, but in practice the signal level still seems to be far higher than the minimum acceptable level.

The timing components for the oscillator in the PLL are VR1, R2 and C2. The Spectrum has a nominal tone leader frequency of 800 hertz, and VR1 is adjusted for an 800 hertz centre frequency.

A switching action is used to determine whether or not the oscillator has locked on to the same frequency as that of the incoming signal. Basically, all that happens is the oscillator operates an electronic switch and the input signal is fed through this switch. If the two signals are at the same frequency the switch cuts off negative half cycles but allows positive ones to pass. This rectified signal is smoothed and used to drive an internal npn switching transistor. C4 is the smoothing capacitor and the collector of the switching transistor connects to pin 8 of the NE567. C3 is the capacitor in the lowpass filter of the PLL, incidentally.

If the input signal and the oscillator are at different frequencies the two signals will have a constantly changing phase relationship so that the electronic switch passes a mixture of positive and negative signals. This gives zero average voltage across C4 and the output transistor is not switched on.

The output transistor is activated continuously when the 800 hertz tone leader is present, but when data is being saved the output tone is modulated and the output transistor is pulsed on intermittently. The output of IC1 is therefore used to drive a smoothing circuit which has a fast attack and a long decay of about 4 seconds, and this drives discrete switching transistor TR1 which in turn drives the relay. This system prevents the relay from cutting out while a program is being saved and gives good reliability. A relay is better than some form of electronic switching in this application since the relay contacts are totally isolated from the rest of the circuit. With some tape recorders neither side of the REM socket is at earth potential. Also, using a relay there is no significant voltage drop through the switch.

LS1 is the loudspeaker which monitors the signal entering the computer during load operations. This is actually a ceramic resonator rather than a normal loudspeaker, and although it only provides limited volume, it is adequate in this respect. In fact, higher volume would be unnecessary although it only provides limited volume, it is adequate in this respect. In fact, higher volume would be unnecessary and undesirable in this application.

S1 is the switch which connects the “Ear” or “Mic” lead, as appropriate, and places a short circuit across the “Rem” socket when the unit is set in the “load” mode. Power for the circuit is obtained from the 0V, 5V and 9V rails of the Spectrum edge connector.

**COMPONENTS ...**

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<th>Resistors</th>
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<tr>
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<td>R3</td>
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<td>R4</td>
<td>10k</td>
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<tr>
<td>All resistors</td>
<td>1W 5% carbon film</td>
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<table>
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<tr>
<td>C1</td>
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<tr>
<td>C2</td>
<td>100n polyester</td>
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<tr>
<td>C3</td>
<td>330n polyester</td>
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<tr>
<td>C4</td>
<td>1µF 63V radial electrolytic</td>
</tr>
<tr>
<td>C5</td>
<td>22n ceramic plate</td>
</tr>
<tr>
<td>C6</td>
<td>100µF 10V radial electrolytic</td>
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<td>TR1</td>
<td>BC179</td>
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<tr>
<td>IC1</td>
<td>NE567</td>
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<table>
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<th>Miscellaneous</th>
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<tbody>
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<td>4 way 3 pole rotary (with end stop)</td>
</tr>
<tr>
<td>LS1</td>
<td>PBN2720 ceramic resonator</td>
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<tr>
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<td>3.5mm jack sockets (4 off)</td>
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<tr>
<td>R7</td>
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**Fig. 2. Circuit diagram of the Auto-Save**
decoupling capacitor C5 should be fitted close to IC1 or instability is almost certain to occur. S1 is a 4 way 3 pole rotary type having an adjustable end-stop which is set for 2 way operation.

Provided the specified relay is used it can be mounted on the printed circuit board, but if an alternative is used it will be necessary to modify the p.c.b. or mount the relay off-board. Any relay having at least one set of make contacts (or a set of changeover contacts), a coil resistance of about 300 ohms or more, and capable of operating from a 9 volt supply can be used in the unit.

The plain side of ceramic resonator LS1 is glued to the inside of the case at any convenient place using a good quality general purpose adhesive. This component does not have any tags or ready-connected leads, and soldered connections are made direct to the inner disc and outer ring. The connection to the inner disc should be completed fairly rapidly, to avoid damaging the component due to overheating.

As mentioned earlier, the “Rem” socket of the recorder may have neither terminal at earth potential, and if a metal case is used SK5 should be an insulated socket, or it should be insulated from the case. Alternatively, a plastic case could be used, but a wire to connect the earth tags of the other four sockets would then be needed.

The connection to the Spectrum edge connector is made via a 3 way cable, and an exit hole is drilled for this in one side of the case. The edge connector is a 2 x 28 way type, and should preferably be a type having the Spectrum polarising “key”. Refer to page 160 of the Spectrum manual for connection details of the edge connector.

VR1 must be given the correct setting before the finished unit will function properly, and a suitable setting is found by empirical means.

CONSTRUCTION

The printed circuit board design is shown in Fig. 3, with the component layout and wiring diagram shown in Fig. 4. If a different form of construction is used, note that supply connection details of the edge connector. As mentioned earlier, the “Rem” socket of the recorder may have neither terminal at earth potential, and if a metal case is used SK5 should be an insulated socket, or it should be insulated from the case. Alternatively, a plastic case could be used, but a wire to connect the earth tags of the other four sockets would then be needed.

Fig. 3. P.c.b. design

Fig. 4. Component layout and wiring diagram

The printed circuit board design is shown in Fig. 3, with the component layout and wiring diagram shown in Fig. 4. If a different form of construction is used, note that supply connection details of the edge connector.

WANTED manual for Tektronix scope type 546B. Will buy or borrow to copy, willing to pay. T. Measor, 5 Midlothian Road, Harlepool, Cleveland TS25 3RH.

WANTED Smart 2-updated Nov. 1980—assembly instructions, especially page 7—system layout—one sheet copy only. Classens Guido, Overenslaan 51-2610 Wilryk, Belgium. Tel: (03) 828 2314.

VOCODER, best of ETIs—Elektors, sensible offers, or exchange for colour computer plus accessories (value £200). J. Logsdon, Top Flat, 13 Holdway, Flat 20, Studland Close, Millbrook, Southampton.

OLIVETTI PR 1350 DOT Matrix printer with reference and service manuals. £130 o.n.o. Mr. A. L. G. Senior, 22 Robinia Walk, Whitchurch, Midlothian EH27 8BJ.

PET 2001 8K RAM (expandable) with integral monitor and cassette deck £200 o.n.o. Tel: Lytham (0253) 737397. D. R. Worley, 14 Mythop Ave., Lytham, Lancs.


TELEQUIPMENT D61a dual trace oscilloscope with X10 probe and manual wanted. E. M. Jackson, Coombe Farm, Gidleigh, Chagford, Newton Abbot, Devon TQ13 8HP.

BREAKING UK101 Cegmon Word Processor new basics 1, 3 & 4 assembler editor chips available. Tel: (0642) 484122. D. Doyle, 21 Skelton Drive, Marske-by-the-Sea, Redcar, Cleveland TS11 THN.

VALVES wanted, must be new and boxed. Also valve sockets and plugs, transformers, capacitors, tuners, amplifiers. N. Covington, 25 Ride Road, Letchworth, Herts SG6 1PT. Tel: (04626) 79681.

MENTA, Z80 Microcomputer for control applications, including manual £75, five interface modules designed for Menta, s.a.e. Mr. D. H. Slater, rear of 25 New Market Street, Colne, Lancs BB8 9BJ.

Bazaar

PET 2001 8K RAM (expandable) with integral monitor and cassette deck £200 o.n.o. Tel: Lytham (0253) 737397. D. R. Worley, 14 Mythop Ave., Lytham, Lancs.


OLIVETTI PR 1350 DOT Matrix printer with reference and service manuals. £130 o.n.o. Mr. A. L. G. Senior, 22 Robinia Walk, Whitchurch, Midlothian EH27 8BJ.

PET 2001 8K RAM (expandable) with integral monitor and cassette deck £200 o.n.o. Tel: Lytham (0253) 737397. D. R. Worley, 14 Mythop Ave., Lytham, Lancs.

One World

We learn something new every day. For example the greatest civil engineer of his time, Isambard Kingdom Brunel, was not as British as I had believed, his father having been French and the young Brunel educated in Paris. I learnt this from an IBM advertisement designed to convince us all that this huge multinational corporation, though not British in parentage, is at least as British as Brunel ever was because it practises its skills in Britain just as Brunel did in his time.

So what? The electrical and electronic sciences have always been international in character and, in fact, origin. Our own fundamental units of measurement, the Volt, Amp and Ohm are derived from the names of early Italian, French and German pioneers, the Farad from an Englishman.

The developments that led to radio are attributed to Maxwell, Hertz, Popoff and Marconi, respectively British, German, Russian and Italian. In television the inventor of the first camera tube, the iconoscope, was Zworykin who emigrated to the United States after the Russian revolution. Zworykin was building on earlier work such as the discovery of cathode rays by Crookes (British) and the invention of the cathode ray oscilloscope by Braun (German).

The scientific community has always believed in open publication of findings for the benefit of all. Not so the business community who guard their secrets, prudently patenting their products before disclosure.

But while protecting their products individually the electronics industry has always been a big sharer of ideas and even designs through cross licensing both within and across national boundaries whenever it is to mutual advantage. This sharing has accelerated in the age of solid state when it soon became apparent that second sourcing was not giving a product away to a competitor but greatly expanding a market. Joint ventures are also common, a recent example being CMOS gate arrays designed in Britain by Smiths Industries' subsidiary Micro Circuit Engineering to be processed by ITT in establishments in the United States and Belgium.

One American company, Advanced Micro Devices, is trying to go beyond cross-licensing into co-operative R & D. AMD's president, Jerry Sanders, is clearly worried over his own company's 100 million dollar spend on R & D in a single year. He recently stated that he and other like-minded semiconductor manufacturers together with equipment manufacturers were contemplating joint formation of R & D organisations and then sharing the research results.

This idea has its parallel in government-sponsored schemes for advancing technology. Whether a private enterprise R & D co-operative would be more effective or even workable is an open question. The most likely cash benefit is in the potential for reducing duplication in R & D activities among participating companies. On the other hand it can be argued that the intense competition in private enterprise to introduce exciting new products is the prime mover of technological advance.

The proof is clearly visible in a comparison of the competitive system of the West with the non-competitive Soviet Union. There is no reason to suppose Russian engineers to be dimmer or less numerous than those in the West and yet they continue to lag behind in almost every field with the possible exceptions of space exploration and armaments.

Let's get back to IBM and Brunel! I may be wrong but I have it as a dim memory that the founder of IBM was himself British, or of British parentage. But who cares in any serious way? My colour TV bears the label of a famous British company whose parent organisation is in the Netherlands where it was most probably designed. The receiver was assembled in Singapore from components manufactured in several other countries.

IBM's long awaited personal computer will proudly bear the IBM label. But its 'works', the circuit boards made by a British company unheard of by those not in the trade. I refer to AB Electronics whose shares gained over £1 on announcement of the IBM contract which, through IBM Greenock, will serve the computer markets in Europe, the Middle East and Africa. Electronics is truly international, one world, and I'm glad it's so. But I suspect that all of us still enjoy a patriotic glow on achievements by and in our own country.

Piracy

Joint ventures, cross-licensing and other mutually advantageous deals have proved their worth over many years through legal or even gentlemen's agreements arranged in a civilised way. In October 1983 I drew attention to look-alike personal computers flooding the market from the Far East and, in particular, the possibility of pirated software becoming an even greater menace.

My fears seem to have been fully justified with software houses claiming collective losses of tens of millions of pounds. Pirating goes right across the board from schoolboy amateurs to skilled computer crooks who can make a good living by selling pirated programs of the more expensive business types at about one tenth of the list price. Protective devices have so far proved ineffective and the copyright laws, as far as the UK is concerned, are anachronistic and artistic content. New legislation is contemplated.

Lady Harrison

One of the least publicised activities of the Racal Group is services for oil exploration. These were inherited through Decca's earlier involvement in navigation and precise positioning systems and, since the acquisition of Decca by Racal, have been greatly expanded through the formation of Racal Energy Resources Ltd.

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Needless to say the ship is stuffed full of electronics and her complement of 34 crew and scientists are all accommodated in single-berth air-conditioned cabins.

Cablesat

Whatever the merits of privatisation (the controversy is still very much alive) the mere prospect continues to galvanise British Telecom. On March 1st BT starts rousing, via Intelsat V, entertainment TV programmes to local cable networks.

The programmes come from United Cable Programmes, a consortium of British companies. They will be transmitted to London Telecom's London Earth Station at North Woolwich and then on to the other to Penmarche on the coast of France. One American company, Advanced Micro Devices, is trying to go beyond cross-licensing into co-operative R & D. AMD's president, Jerry Sanders, is clearly worried over his own company's 100 million dollar spend on R & D in a single year. He recently stated that he and other like-minded semiconductor manufacturers together with equipment manufacturers were contemplating joint formation of R & D organisations and then sharing the research results.

This idea has its parallel in government-sponsored schemes for advancing technology. Whether a private enterprise R & D co-operative would be more effective or even workable is an open question. The most likely cash benefit is in the potential for reducing duplication in R & D activities among participating companies. On the other hand it can be argued that the intense competition in private enterprise to introduce exciting new products is the prime mover of technological advance.

The proof is clearly visible in a comparison of the competitive system of the West with the non-competitive Soviet Union. There is no reason to suppose Russian engineers to be dimmer or less numerous than those in the West and yet they continue to lag behind in almost every field with the possible exceptions of space exploration and armaments.

Let's get back to IBM and Brunel! I may be wrong but I have it as a dim memory that the founder of IBM was himself British, or of British parentage. But who cares in any serious way? My colour TV bears the label of a famous British company whose parent organisation is in the Netherlands where it was most probably designed. The receiver was assembled in Singapore from components manufactured in several other countries.

IBM's long awaited personal computer will proudly bear the IBM label. But its 'works', the circuit boards made by a British company unheard of by those not in the trade. I refer to AB Electronics whose shares gained over £1 on announcement of the IBM contract which, through IBM Greenock, will serve the computer markets in Europe, the Middle East and Africa. Electronics is truly international, one world, and I'm glad it's so. But I suspect that all of us still enjoy a patriotic glow on achievements by and in our own country.

Piracy

Joint ventures, cross-licensing and other mutually advantageous deals have proved their worth over many years through legal or even gentlemen's agreements arranged in a civilised way. In October 1983 I drew attention to look-alike personal computers flooding the market from the Far East and, in particular, the possibility of pirated software becoming an even greater menace.

My fears seem to have been fully justified with software houses claiming collective losses of tens of millions of pounds. Pirating goes right across the board from schoolboy amateurs to skilled computer crooks who can make a good living by selling pirated programs of the more expensive business types at about one tenth of the list price. Protective devices have so far proved ineffective and the copyright laws, as far as the UK is concerned, are anachronistic and artistic content. New legislation is contemplated.

Lady Harrison

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TACHOMETERS (LM 2917N–8 AND LM 2917N)

**Methods of Operation**

The input to the i.c. is a differential amplifier with hysteresis. (Hysteresis is the effect whereby the input passes through a threshold voltage in the positive direction before the output will turn off. It helps to prevent spurious oscillations at the exact point of changeover.) In the '8' device, the input is protected to ±28V, since the input must swing about 0V, inferring an a.c. coupled input in most cases. Since it is possible to bias both inputs to the 14 pin i.c., this has no such protection, hence the earlier warning. Because of the very high gain of the input amplifier, and the absence of any negative feedback, the output is a square wave, the frequency of which is identical to the input signal.

The square wave signal causes the 'charge pump' circuit to charge, or discharge (as appropriate) the timing capacitor \( C_T \) between two internal voltage references which are half the Zener supply voltage apart. As a result, the average of the current pulses pumping into

<table>
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<th>Notes</th>
<th>Min.</th>
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<td>Op-amp i/p voltage</td>
<td>(Also, collector voltage)</td>
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<tr>
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<tr>
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<td>(Variation in correct o/p voltage, with respect to 5kHz voltage)</td>
<td>±0.3</td>
<td>±1.0</td>
<td>%</td>
<td></td>
</tr>
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</table>

*0–28V for the LM 2917N*

\( C_T \) is given by:

average current = \( V_x \times f_1 \times C_T \)

where \( V_x \) = Zener voltage and \( f_1 \) = input frequency.

The output of the charge pump 'mirrors' an exactly equivalent current into the integration network \( C_1 \) and \( R_1 \). The resistor acts as a load for the current mirror, and the capacitor smooths the pulsed waveform to provide a d.c. voltage at pin 3 (for LM 2917N–8) given by:

\[
V_3 = V_x \times f_1 \times C_T \times R_1
\]

In practice, due to i.c. tolerances, the d.c. voltage can vary from 0.9 to 1.1 times this value. This 'gain constant' error varies from one i.c. to the next, but stays constant within each i.c.

**PRACTICAL CONSIDERATIONS**

The larger the value of \( C_T \), the less ripple will be produced, but the slower the circuit will be to respond to changes in frequency. The values of \( C_T \) and \( R_1 \) will also affect response speed; \( C_T \) should be kept larger than 100p to avoid voltage errors. The value of ripple on the output is given by:

\[
\text{ripple voltage p/p} = \frac{V_x \times C_T}{2 \times C_T} \times \left( 1 - \frac{V_x \times f_1 \times C_T}{I_0} \right)
\]

\( I_0 \) is the available output current from pin 2 or pin 3. This can vary from 140–240mA; typically it is 180mA. Finally, the maximum input frequency for the system is:

\[
f_{\text{max}} = \frac{I_0}{V_x \times C_T}
\]

**BASIC CIRCUITS**

The most effective way to illustrate the use
Fig. 2. Block diagram of LM 2917-8

of the output op-amp and transistor is to consider two typical examples of basic circuits. Fig. 4 shows a simple tachometer, with the transistor connected as an emitter follower. The connection to pin 7 therefore provides a voltage at pin 3 which exceeds the voltage at pin 7 and the threshold at which the output op-amp acting as a comparator. When the output op-amp turns off, the output transistor turns on, causing D2 to light up and TR1 to turn on, effectively connecting R14 in parallel with C6, which results in the voltage across C6 starts to rise again when this happens, which in turn causes the output op-amp to turn on. The connection from the resistor chain R2, R3, and R4 to pin 7 of IC1 provides extra hysteresis in the system, ensuring that the system does not oscillate at high frequencies around the turn on/turn off point of the output op-amp. There will, of course, be the low frequency oscillation as described above, the frequency of which will be determined by the rate at which IC1 pin 3 can charge up C6, which is determined by the input frequency.

The circuit will have no effect until a certain frequency is exceeded, at which point D2 will start to flash on and off slowly. If the input frequency increases, the i.e.d. will flash at a faster and faster rate, until it remains illuminated continuously. The threshold frequency at which the i.e.d. first lights up can be determined from the equations given by:

\[
\text{Switch} = \frac{1}{2 \times R_i \times C_t}
\]

**APPLICATION**

Fig. 5 shows the circuit diagram of a more sophisticated 'speed switch', with Fig. 7 showing the Veroboard layout required for this. R2, R3, and R4 set the threshold at which the output amplifier switches. When this happens, the

**AUDIBLE WARNING**

IC2 is a 555 timer i.e. connected as an audio frequency oscillator. TR2 and TR3 turn on whenever IC2 is illuminated, providing an audible warning. The transducer used for this can be a piezo-sounder, in which case no series resistor is likely to be needed, or a loudspeaker, in which case the impedance of the loudspeaker, in series with dropper resistors, should ideally be approximately 70 ohms or more. The series dropper resistors shown asterisked in Fig. 6 should total 1W for low impedance loudspeakers. Use a pair of 0.5W 150 ohm resistors in parallel for a 4 to 16 ohm loudspeaker.

**Fig. 6 (Below). Circuit diagram of overspeed alarm or 'speed switch'**
D1 protects against incorrect connection to the supply, and, together with decoupling capacitors C1 and C2, provides a measure of isolation if used in "noisy" automotive electrical systems. The circuit can be used to monitor car or motorbike engine revs if the input conditioning circuit shown in Fig. 6 is used. This circuit provides decoupling, filtering, and attenuation of the contact breaker voltage spikes, and is suitable for both positive and negative earth systems. Don't forget to include a fuse in the positive supply feed to the circuit, though, for safety (or negative supply for positive earth vehicles). If the LM 2917N is being used, a Zener diode should be fitted between pin 1 and OV (with its anode connected to OV) to protect against reverse voltages. The value is not critical, but 12V should be adequate in most cases (other changes to the circuit of Fig. 6 are also necessary, of course).

SOME ADVICE

Although this circuit works well, it would not be advisable to rely on it for keeping to speed limits, since it monitors engine revs, not road speed!

The LM 2917N-8, and LM 2917N, are useful devices for many frequency-to-voltage conversion applications. They can be used from Cricklewood Electronics Ltd., 40 Cricklewood Broadway, London NW2 3ET.

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It was Thursday—"Press day"—when my morose friend and I called on STN. In one room a trio of ladies were busy unpacking and sorting the returned C60 cassettes carrying the previous week's issue (five mailbags of them in all). In another room a team of editors were scanning the local newspapers, supplied free by the publishers, for the 'hard news' side of the tape. Contrary to what you might expect, there is no bias in selection towards only pleasant or neutral news. "The blind dislike the idea of being protected from unpleasant things," said Lesley. "They want to hear about both the good and the bad so that they can discuss current events with their sighted friends. Anything goes, from muggings to garden fetes." The second side of the tape accommodates the 'magazine' section. In this the blind themselves have a large slice of the action. They provide articles, seek out interviews with local officials and prominent personalities. There are items about holidays and leisure pursuits. One blind man has even contributed an account of his experiences as a mountaineer!

"You're out of date, dad. Your mind is pre-microchip"

In the control room I spoke with Doug Cook, formerly an engineer with the Post Office. He was in the process of making the master tape of the magazine section. "With our duplicating machines," he said, "we can edit them so that halfway through there's a break for music which gives our 'readers', as we call the listeners, a chance to put the kettle on." By now all was ready for recording the news. The team consisted of one presenter and four readers, all of whom identified themselves by name. Their professionalism was remarkable, though, says Lesley: "We don't really need professionals—just people with enthusiasm and clarity."

The clock stood at 8.30 p.m. All the tapes were completed and checked. A standard procedure, by the way, is to include a reminder to turn off the recorder and to turn over the reversible label on the postal pouch for return of the tape to STN headquarters. And in case you're wondering how blind persons differentiate between the two sides of the tape, there's a tactile strip on the face of the cassette.

The rest was sheer humungous. First, the registration of each pouch before it went into the mailbag. Then a trip to the back door of the main Post Office. The mailings—handled free of charge in both directions—would be dealt with overnight and the majority of tapes would reach their destinations by first post.
In this month's issue we begin a new series which provides some practical examples of digital techniques. These projects, which have been carefully selected to complement the series entitled 'Introduction to Digital Electronics', also make excellent constructional projects in their own right, finding numerous applications in the home, school and workplace. Each project uses low-cost, readily available components and single-sided p.c.b.s are used throughout.

We start this month, with a simple Anti-Theft Alarm which is designed to provide an audible and visual warning that property or goods are being tampered with. This project illustrates the use of some of the basic logic gates, demonstrates techniques for driving I.e.d.s, and shows how simple square wave oscillators can be constructed using Schmitt logic gates. A separate power supply module is also described. This module provides a regulated 5V supply of up to 500mA and is suitable for use with both the Anti-Theft Alarm and any of the subsequent projects.

CIRCUIT DESCRIPTION

The complete circuit of the Anti-Theft Alarm is shown in Fig. 1. The alarm is provided with four input loops which link points A, B, C, and D respectively to the common 0V rail. Whenever one, or more, of the loops is broken the respective pull-up resistor, R1 to R4, will generate a logic 1 input at IC1 which is arranged to form a four-input OR gate. The normal state of the output of IC1c, when all of the loops are closed, will be a logic 0. If, however, any of the loops is broken, the output from IC1c will become logic 1.

In order to provide a visual indication of which one of the loops is broken, IC4 is arranged as an I.e.d. driver, inverting the logical input to IC1 so that the respective I.e.d. becomes illuminated whenever an output goes low. A fifth I.e.d. is included merely to indicate that the supply is connected and that the alarm is active.

IC2a uses a Schmitt inverter to form a simple oscillator which produces a square wave output at approximately 3kHz. A similar stage, IC2f, operates at the much lower frequency of 3Hz. An inverting buffer follows each oscillator and then both square wave signals are applied to a two-input AND gate, IC3d. The resulting output from IC3d consists of 200ms bursts of 3kHz signal which is then fed to a further two-input AND gate, IC3a.

The gated square wave signal from IC3d only appears at the output of IC3a when a logic 1 appears at the output of IC1c (i.e. when any one, or more, of the loops is broken). In order to provide an audible output at ample volume, a VMOS f.e.t., TR1, follows IC3a. This device has a near infinite input impedance and is capable of driving the low impedance load presented by the loudspeaker. A series resistor, R13, is included in order to both reduce the volume of the output signal and reduce the peak drain current flowing in TR1 to an acceptable value.

The circuit diagram of the Power Supply Module is shown in Fig. 2. This uses a conventional i.c. regulator and an I.e.d. is incorporated in order to provide a visual indication of the d.c. output. Little further comment is necessary other than that the nominal 6V a.c. input is derived from a fully encapsulated mains transformer of similar type to that used with the Logic Tutor.

CONSTRUCTION

The Anti-Theft Alarm is built on a single sided p.c.b. measuring approximately 140x90mm, the copper foil layout of which is shown in Fig. 3. The corresponding component layout on the top surface of the p.c.b. is given in Fig. 4. Interconnections from the p.c.b. to the four input loops, I.e.d. indicators, loudspeaker and power supply are all made via 0-1" matrix p.c.b. connectors, the wiring for which is shown in Fig. 5.

Components should be assembled on the p.c.b. in the following sequence: d.i.l. sockets, p.c.b. connectors, resistors, capacitors, f.e.t. Once assembly has been completed the underside of the p.c.b. should be carefully
checked for solder splashes, bridges between adjacent tracks, and dry joints. Finally, the i.c.s may be inserted in their respective holders, taking care to ensure the correct orientation of each device. Constructional details of the enclosure and off-board wiring have not been given since this will undoubtedly be a matter of preference for the individual constructor.

The p.c.b. layout for the Power Supply Module and corresponding component layout are shown in Figs. 6 and 7. Assembly is very straightforward; however, care should be taken to ensure that the bridge rectifier is correctly orientated. The i.c. regulator should not require a heatsink for this project; however, if one is available rated at around 17.5°C/W, it may be fitted to meet the supply current demands of more ambitious projects. Once complete, and before the a.c. input is applied, the Power Supply Module should be carefully checked for soldering faults. The mains transformer is rated at 6V 3VA and should be housed in a fully insulated plastic encapsulation integral with the mains lead and plug.

TESTING

Testing the Anti-Theft Alarm is simply a matter of checking that the 5V supply is present and, if this is the case, D5 should be illuminated. Each of the input loops should then be open-circuited in turn. The alarm should be activated whenever any one of the loops is broken and the corresponding I.E.D., D1 to D4, should become illuminated. The input loops will normally consist of lengths of stranded insulated wire running through the goods to be protected.
They may also consist of thin strips of foil fastened to windows and glass doors by means of a suitable adhesive. Indiscriminate breaking of the glass will cause the foil strip to break and the alarm to be set off.

**MODIFICATIONS**

The sound level of the output may be adjusted by varying R13 which should be reduced in value if more output is required or increased in value if less output is required. If R13 is reduced to less than 5-6 ohms a small heatsink will be required for TR1.

The frequency (pitch) of the audible warning signal may be changed by altering the value of C2. A larger value (say 470nF) will decrease the frequency, whilst a smaller value (say 100nF) will increase the frequency. If it is necessary to alter the rate at which the audible output is pulsed on and
off. C1 may be similarly varied. Appropriate values lie in the range 100µF to 680µF.

To drive several loudspeakers, the circuit around R12, TR1, and R13 should be duplicated. Each loudspeaker then has its own driver circuit. The signal input for all of the driver circuits is derived from pin 3 of IC3a. The loudspeakers should be placed at various strategic points. These may, for example, include passageways, doorways, counter and checkout areas.

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IN THIS, the concluding part, details of the p.c.b. assembly and case construction are given. The project is a remote VDU/Keyboard terminal capable of RS232 serial communication with any home computer with an RS232 port.

P.C.B. ASSEMBLY
The p.c.b. foil pattern and component layout are shown in Figs. 2.1 and 2.2.

The components should be installed on the p.c.b. in the following order:

a) Links, terminal pins and regulator leads.
b) I.c. sockets.
c) Capacitors and resistors.
d) Modulator, buzzer and crystals.
e) Connectors.

It is strongly recommended that i.c. sockets are used, as it is difficult to change faulty or incorrectly installed devices if they are soldered to the p.c.b. Before proceeding any further it is wise to check for incorrect component locations and solder bridges. These are most likely to be found in the RAM area of the p.c.b.

CASE
There is a wide range of commercially available cases that the reader may choose from to house the system. However, the author found none suitable for his requirements and so constructed the case shown in the photographs. The side plates are made of solid mahogany, with the chassis, back and cover plates made from aluminium sheet, spray painted. The wooden side plates are cut to size and the support battens screwed to them as shown in Fig. 2.3, and the aluminium panels cut and drilled to the dimensions shown in that Fig. The back panel carries the UHF and monitor output sockets, mains input socket, the full/half duplex switch, the 25-way D-series connector for the RS232 link, and is also used as a heat sink by the three voltage regulators which should be fitted using insulating mica washers. The back plate is connected to the chassis by a length of 13mm aluminium angle as shown. Two identical covers should be constructed, one of these being cut to accept the chosen keyboard. All the aluminium panels should be rubbed down with wire wool before being sprayed. The keyboard is then secured to its cover, the various components fitted to the back plate which can be bolted to the chassis. The p.c.b., mounted on insulating spacers, and the transformer are then fitted to the chassis. The various parts should next be wired together as shown in Fig. 2.4. Finally, No. 5 x ½ inch countersunk screws are used to mount the aluminium panels to the side plate battens, with the exception of the top cover plate which should be fitted after the Computer Terminal has been tested.

TESTING
Before inserting any i.c.s the power supplies should be checked to establish that the correct voltages are being produced. Check that the correct voltages are present on the various i.c. power pins. If all is well the unit should be switched off and the i.c.s inserted, taking care to insert IC12 and IC15 the correct way round. The normal precautions should be employed when handling the i.c.s, especially the RAMs. The full/half duplex switch should be set to the half duplex position, the monitor or television connected and switched on.

The terminal can now be switched on. If a television is being used, it should be tuned to channel 36 (that used by video recorders). The screen will be filled with random characters. It may be necessary to adjust VR1 and VR2 for best results. The reader will notice a flashing cursor somewhere on the screen: characters entered on the keyboard will be displayed at the cursor position. The cursor itself may be moved around the screen, or the screen cleared by entering the ASCII control characters listed in Part 1.
### COMPONENTS

#### Resistors
- R1-9, R11, R17: 10k (11 off)
- R10: 10M
- R12: 100R
- R13: 2k
- R14, R18: 1k (2 off)
- R15: 4k7
- R16: 82R (3/4W)

All resistors 1W 5% unless otherwise stated.

#### Potentiometers
- VR1: 470R
- VR2: 100R

#### Capacitors
- C1: 100p
- C2: 22μ/10V
- C3,4: 2200μ/25V (2 off)
- C5-30: 100n (26 off)

#### Semiconductors
- IC1-7: 2102 (7 off)
- IC8: 74LS374
- IC9: SFF98364
- IC10: 2716 EPROM
- IC11: 6402 or AY-5-1013 (see text)
- IC12: 2716 EPROM
- IC13: 74LS163
- IC14: 74121
- IC15: 74LS165
- IC16: COM8126
- IC17: 74LS08
- IC18: 74LS00
- IC19: 74LS08
- IC20: 74LS132
- IC21: 1486
- IC22: 1489
- IC23: 7805
- IC24: 7812
- IC25: 7912
- TR1,2: BC109, BC547 etc (2 off)
- D1-4: 1N4001 (4 off)

#### Miscellaneous
- VR1: 1MHz crystal
- VR2: 5.0688MHz crystal
- UHF-modulator: Aspic 1233 (8MHz)
- S1-4: 4-way p.c.b.
- S5-10: 6-way p.c.b.
- S11: S.p.d.t.
- SK1: 25-way D-Series
- SK2,3: BNC Chassis Mounting
- SK4: IEC Mains Connector
- SK5: 5-way p.c.b. Connector
- SK6: 3-way p.c.b. Connector
- SK7: 8-way p.c.b. Connector
- Buzzer: Verospeed 41-22515K
- T1: 12-0-12 25VA transformer
- Keyboard
- Case (see text)
- Double Eurocard single-sided p.c.b.
- I.c. sockets

#### Constructors' Note

A Hex dump of the EPROM contents is available from P.E. (Poole office); please send 230 x 150mm SAE. Pre-programmed EPROMs and COM8126s are available from: "Peripheral Projects," 25 Braycourt Avenue, Walton-on-Thames, Surrey KT12 2AZ. Printed circuit boards, if not found available from P.E.'s usual suppliers (see advertisers), will in any case be available from this supplier.
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Fig. 2.1 (facing page). P.c.b. layout of the Computer Terminal (actual size)

Fig. 2.2 (above). Component layout
Fig. 2.3. Constructional details of the d.i.y. option case
The BEL function can be checked by pushing the CTL and G keys together, whereupon a buzzing sound should be heard. Note that the UART latches its receiver outputs to the last character detected. As the buzzer’s monostable is edge triggered it will only respond to the first CTL/G when several are sent consecutively. Normally CTL/G would be followed by a different character.

Switch to full duplex, the screen will remain unchanged, but characters entered on the keyboard will not appear on the screen. Connect the terminal to the host system via an RS232 cable. The host system’s output should now be displayed on the screen. Similarly the host system should respond to characters entered on the keyboard.

ADDITIONAL FEATURES

As previously described, the control EPROM is programmed so that four of its outputs respond to the ASCII control characters as shown below:

- **03** — CTL/G (BEL) — p.c.b. pin A
- **04** — CTL/Q (DC1) — p.c.b. pin B
- **05** — CTL/R (DC2) — p.c.b. pin C
- **06** — CTL/S (DC3) — p.c.b. pin D

A p.c.b. plug is provided so that these signals may be used to drive additional circuitry.

The circuit in Fig. 2.5 shows how normal or reversed video could be selected using the ASCII control characters DC2 and DC3. Gates 1A and 1B form a bistable flip-flop, set by DC2 and reset by DC3. The flip-flop’s output is exclusive ORed with the normal video signal to produce normal or reversed video which is fed to the transistor mixer TR1. Issuing a DC2 character will cause all following characters to be reversed until a DC3 character is issued to revert back to normal video. The reader can therefore select various parts of the screen to display reversed video at will. If this circuit is used link “L” must be removed from the p.c.b.

A similar circuit (see Fig. 2.6) could be used to control a relay which could drive, for example, a cassette recorder’s motor. DC3 would turn it on and DC2 turn it off. These two examples serve to indicate the types of additional facilities that may be included in the system and is by no means an exhaustive list.
INTERFACING WITH THE BBC COMPUTER

As stated at the beginning of this article, the Computer Terminal can be used as a second terminal for a BBC computer. The following notes describe how this can be achieved. With this terminal, or “glass teletype”, connected to the BBC’s RS423 socket, the command *FX2,1 allows the BBC computer to get characters from the “glass teletype”, whilst *FX3,7 allows data to be sent from the BBC computer to the “glass teletype”. Note that in this mode the BBC computer’s keyboard and screen are disabled. The BBC computer’s baud rate is set to the same value as that of the PE terminal (say 2400 Baud) by using the commands *FX7,5 and *FX8,5 for receive and transmit rates respectively. Reference should be made to the BBC computer’s “user guide” for further information on the use of the RS423 port.

CONCLUSION

Although reference has been made to the BBC computer, it is by no means the only system to which the terminal may be interfaced. The Computer Terminal can be used with any system fitted with a RS232 or RS423 interface. Examples of such systems are: Microprocessor development systems, Modems, EPROM programmers, Printers, as a terminal for a such systems are: Microprocessor development systems, Modems, EPROM programmers, Printers, as a terminal for a--

Readout...

Gas Saver

Sir—The boiler referred to in this article is obsolete, production finishing in 1970; although later series continued the basic design through to 1980.

The heating interests of Ideal-Standard Ltd. were incorporated into the Stelrad Group Ltd. in 1976 and it is with Stelrad that I am employed as Senior Controls Engineer within Group R&D department. In this capacity I must point out the problems associated with “add-on” modifications to approved gas appliances.

Interference with the working parts (in particular the electrical controls) of an approved gas boiler could invalidate the approval and warranty/service agreements as well as infringing the Gas Safety Regulations and, more to the point, could seriously impair the safe working of the appliance.

Any modification must give due regard as to the consequences—in particular taking full responsibility for the modifications carried out.

Obviously appreciable running cost savings can be made and manufacturers are currently investigating many possibilities for future incorporation into manufactured appliances.

The article also seems to suggest that only electronics can give the savings indicated. However, with the inclusion of a clamp-on cylinder thermostat and some simple wiring modifications the indicated savings could be achieved for less initial outlay, without invalidating the above comments.

It would appear that there is little appreciation for heating, as the article seems to concentrate on controlled hot water and controlled boiler temperature rather than total comfort and cost effectiveness. As regards to controlling the gas valves via triacs and the associated gates and comparators, this is at present not accepted by the Industry for primary output because of its possible failure mode resulting in an unsafe condition, among other factors. It is true though that the article does suggest the thermostats provided with the boiler should be connected in series with the “Gas Saver” but this is not shown on the diagram and is not highlighted sufficiently within the article.

As you state in the article “… Safety is all important in any equipment … using gas and electricity simultaneously, particularly, when running continuously without supervision.” Hence we would suggest this should be left to experts as a little knowledge can be, so often, dangerous.

The subject is too large to handle in a few lines but it is hoped that the foregoing will be seen as constructive and helpful as we all endeavour to further the interest of electronics to the benefit of the Industry and our customers.

M. J. Blissett,
Senior Controls Engineer,
Stelrad Group Ltd.

We have received a couple of similar letters, and it seems I must first plead guilty to perpetuating the misconception that the copper tube in the typical boiler thermostat conducts heat directly. In fact, it contains a fluid which expands when heated, and the capillary action is used to operate electrical contacts via a “bellows” mechanism. Although not as rapid as electronics, the action is not as slow as the article suggested.

To respond to the particular points raised by Mr. Blissett: First, I believe most consumers cannot afford to replace their C.H. system (or any other appliance) each time it is declared obsolete. Gas Saver was intended to allow the older, or cheaper, system to become more economical, given its inherent limitations.

An older system will not be covered by a manufacturer’s warranty, but of course, Mr. Blissett is right to point out that a consumer should not carry out d.i.y. modifications that will invalidate a service agreement, and is indeed personally responsible for any such alterations. Beyond this, it is difficult to see how Gas Saver could impair reliability when connected, as suggested, in series with the existing thermostat. However, if I did not “highlight” this precaution sufficiently in the article, let me stress it now. A number of hobbyists experiment with electronics C.H. control, and look upon published material as further input, which is why I emphasised safety in general.

We accept the fact that “mechanical” equivalents to circuits published in Practical Electronics often do exist; as in “timers” for example. The clamp-on cylinder thermostat will not be as cheap if a professional is called in to install it—which I presume is advocated. The electronics enthusiast will argue that his approach paves the way to more flexible programming, making it possible to consider a timer that not only turns the C.H. system on and off, but which permits a programme of differing temperatures etc.

Failure modes should obviously be taken into account, and the article did underline this, hopefully to benefit also the hobbyist with his own ideas. But whether or not magazines should publish projects with which someone could have an accident, is a broader issue. I am sure the d.i.y. brand of hobbyist generally knows his own limitations and has the sense to avoid activities about which he has doubts.

M.A.
It would appear that about the only thing the various single-chip microprocessor families have in common is that they are all different! This month we are going to take a look at the gospel according to National Semiconductor as expounded by their 8070 family, and as usual there are a few surprises in the approach they have taken.

At first sight National appear to have been an also-ran in the great microprocessor race, because although they have produced a number of original chip designs, they have never become a serious challenge to the Intel-Motorola-Zilog "Big three", and have probably made more money from second-sourcing Intel designs such as the 4040, 8080, and 8048 than they have from the chips from their own stable. Whether this somewhat mediocre performance is a reflection on the quality of their designs or whether it is due to shortcomings in their marketing policy I cannot say, but it will be interesting to see how their latest offering, the very powerful 16 bit NS16032 fares in the coming months.

The first National microprocessor to achieve popular prominence was the 8 bit SC/MP, which pioneers in the microprocessor hobby field may remember as one of the first devices to become available in hobby kit form. I certainly remember reviewing for P.E. one of the first evaluation kits in the country, and I remember being impressed by its "generous" provision of 512 bytes of ROM based monitor software and its 256 byte RAM area for user programs. All of that squeezed onto just one single Eurocard! Of course, that was in the antediluvian days of 1976 or 1977 and things have changed a lot since then. The PMOS SC/MP caught on quite well, especially in Europe, and was soon followed by a 5 volt NMOS version, the SC/MP 8060, but in the end its limited processor performance and restrictive 12 bit direct addressing range caused it to lose ground to the competing Intel and Motorola processors.

National did not abandon the basic architecture of the 8060 however, and in 1980 they introduced the 8070 family which features extended performance and the capability to use an on-chip ROM and RAM array, a logical move since the original 8060 had proved most successful in the low cost controller applications most suited to single chip processors.

One of the most successful features of the 8060 family was its suitability for use in multi-processor systems thanks to an extensive set of control inputs and outputs, and it was decided to retain this feature on the 8070. A decision was also made to have separate non-multiplexed data and address busses, using 24 pins in all, and this, combined with the extensive control facilities, left only five pins available for I/O use.

This lack of the usual complement of parallel I/O ports puts the 8070 family on the fringes of the single chip processor scene, and makes the use of external I/O chips a necessity in most applications, but despite this apparent disadvantage there are certainly plenty of jobs in which the particular characteristics of the 8070 family make it the most suitable choice.

There are currently three devices in the family, the 8070 itself which has 64 bytes of on-chip RAM but no ROM, the 8072 which has 2 5K bytes of masked ROM for high volume applications, and the 8073 which is an 8072 with the ROM preprogrammed with a monitor and a Tiny BASIC interpreter, in the style of the Zilog Z8671 discussed last month. All three chips have the same basic internal architecture, instruction set, and pin connections, and all feature an 8 bit data bus, a 16 bit address bus and a 16 x 16 bit hardware multiplier/divider.

The 8070 and 8073 are both usable for hobby applications, but there seems to be little to recommend the multichip 8070 solution over competitive devices unless a potential user suffers from 8060 nostalgia! Since there is no EPROM version I have chosen to feature the 8073 which is one of the two devices available which feature on-chip BASIC (the other being the Z8671).

Even when programming in BASIC, it is desirable to know something about the internal architecture of the chip itself, and so these details, common to the whole family are given as usual. Details of the BASIC interpreter which is of course specific to the 8073, are given in the Software section.

As you may have expected, the launch of the on-chip BASIC 8073 caused quite a surge of interest and more requests for data sheets than had ever been received for any previous National product. This must have generated mixed feelings at National, because data mailings are expensive and they must have realised that most recipients were either just plain curious, or were serious potential customers who would ultimately buy only one or two devices, since a device programmed in BASIC is not a cost effective solution for high volume applications.

Still, their loss is our gain, since a single-chip processor programmable in BASIC is an excellent choice for many one-off hobby applications!

**REGISTERS**

The original 8060 register set is carried through into the 8070 family with little change, although some names have been changed to reflect improvements in register usage and flexibility. The new family uses a single 8 bit accumulator register which acts as the implied source or destination for many instructions in typical first generation style, but this has been extended by means of an additional 8 bit register called the Extension register (E) which can be used either by itself as a temporary data store, or together with the accumulator to form the 16 bit EA accumulator for 16 bit operations.

There are five 16 bit registers, two of which are the Program Counter (PC) and the Stack Pointer which are quite conventional. There are two pointer registers (P2 and P3), which would be called index registers in most other processors, and finally something a little different, the Temporary (T) register which is needed for the 16 bit multiplier or divider in multiplication or division operations, and can also be used as a general purpose 16 bit data store.

The only other user accessible register is the Status register (S), and this contains the eight flag bits as shown on the file sheet. Five of the flag bits are used for the two input lines, SA and SB, and the three output lines F1, F2 and F3, which are the closest the 8070 family comes to having any parallel I/O capability on-chip.

The only other flags available are the conventional Carry (CY), Overflow (OU), and Interrupt Enabled (IE), which means that there are no zero, sign, or auxiliary carry flags. No doubt the zero and sign functions can be simulated easily enough, but the lack of an auxiliary carry flag has the potentially serious implication that no direct BCD arithmetic is possible. Fortunately however, there is no requirement for BCD arithmetic when using the 8073's Tiny BASIC, and so there is no need to worry too much about this feature unless the use of an 8070 is being considered.

Apart from the above mentioned flag limitations, the 8070 family has quite a useful complement of registers.

**INSTRUCTION SET**

Although the 8070 family instruction set has obvious links with the earlier SC/MP 8060 set, there are some deletions and several useful additions.
**GENERAL**

The 8073 is a member of the National Semiconductor range of 8-bit NMOS processors which has been developed from the earlier SC/MP 8060 family. The 8073 has the outstanding feature of an on-chip Tiny BASIC interpreter stored in 2.5k bytes of ROM and is designed for low cost controller applications which do not require the high speed of machine code. Unlike most other single chip microprocessors the 8073 has very few on-chip I/O lines, but it does have extensive control features to allow multiprocessing.

**REGISTERS & MEMORY**

The 8073 has a useful set of dedicated registers including 3.16 bit memory pointers (SP, P2, P3), there is a 2.5k ROM array and 64 bytes of RAM on-chip.

**INSTRUCTION SET AND SOFTWARE**

The machine code instruction set of the 8073 is identical to that of the other chips in the family and contains some very useful features such as signed 16 bit multiply and divide instructions. The Tiny BASIC is based on National's earlier NIBL interpreter, offers 16 bit integer arithmetic, a useful set of control orientated BASIC statements and functions, and allows the use of embedded machine code routines if required.

**PERFORMANCE DATA 8073**

- **MEMORY ADDRESS RANGE**: 64k8
- **I/O ADDRESS RANGE**: Memory mapped
- **CLOCK FREQUENCY**: 4MHz
- **POWER SUPPLIES**: 5V
- **INTERRUPTS**: INTA, INTB
- **BENCHMARKS**: 8073
  - ADD REGISTER TO ACCUM: 4.15s
  - OR ACCUM TO PORT: 7.3s
  - MOVE FROM MEMORY TO MEMORY: 14.6s
  - *DIRECT (8BIT)* MODE

**OTHER FAMILY MEMBERS**

- **8060 (SC/MP)**: This device was the predecessor of the 8040 family but had limited addressing and no on-chip memory.
- **8070**: Basic family member with 64 bytes of RAM but no ROM.
- **8072**: Like 8073 with 2.5k of on-chip ROM but without Tiny BASIC. For mass production applications.

**SUPPORT CHIPS**

Unlike the 8748, 68701 and Z8 the 8073 does not have much on-chip parallel I/O capability but can interface to the 8080 peripheral chip family externally. Although there are 64 bytes of RAM on-chip, the 8073 needs at least 256 bytes of external RAM.

**MANUFACTURERS**

- **ORIGINATOR**: NATIONAL SEMICONDUCTOR
- **2ND SOURCE**: AMD

**REFERENCE FILE SHEET**

PE Micro-file March 1984
### INSTRUCTION SET SUMMARY

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<th>SECOND OPERAND</th>
<th>OPERATION PERFORMED</th>
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<td></td>
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</tr>
<tr>
<td>P3</td>
<td>EA</td>
<td>(P3) → (EA)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>EA</td>
<td>(T) → (EA)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EA</td>
<td>T</td>
<td>(EA) → (T)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>E</td>
<td>(A) → (addr)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EA</td>
<td>(AE)</td>
<td>(addr + 1, addr)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADD</td>
<td>ADD</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>E</td>
<td>(A) → (A) + (E)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EA</td>
<td>(EA)</td>
<td>(EA) → (EA) + (addr + 1, addr)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SUBTRACT</td>
<td>SUB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>E</td>
<td>(A) → (A) + (E)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EA</td>
<td>(EA)</td>
<td>(EA) → (EA) + (addr + 1, addr)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MULTIPLY</td>
<td>MPY</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EA</td>
<td>T</td>
<td>(EA) → (EA) * (T)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DIVIDE</td>
<td>DIV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>E</td>
<td>(A) → (A) / (E)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S</td>
<td>(S)</td>
<td>(S) → (S) / (E)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OR</td>
<td>OR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>E</td>
<td>(A) → (A) + (E)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S</td>
<td>(S)</td>
<td>(S) → (S) + (E)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EXCLUSIVE-OR</td>
<td>XOR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>E</td>
<td>(A) → (A) + (E)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### INSTRUCTIONS

- **EXCHANGE REGISTERS**: XCH
  - EA → (EA)
  - SP → (SP)
  - P2 → (P2)
  - P3 → (P3)

- **SHIFT RIGHT**: SR
  - A → (A) → (A - 1)
  - 1 → 0 → A

- **SHIFT RIGHT WITH LINK**: SRL
  - EA → (EA - 1)
  - 1 → 0 → EA

- **ROTATE RIGHT**: RR
  - A → (A - 1)
  - 1 → 0 → A

- **ROTATE RIGHT WITH LINK**: RRL
  - A → (A - 1)
  - 1 → 0 → EA

- **SHIFT LEFT**: SL
  - A → (A + 1) → (A)
  - 0 → 0 → A

- **SEARCH AND SKIP IF CHARACTER MATCHED**: SSM
  - EA → (EA - 1) → (EA - 1)
  - 14 → 0 → EA

- **BRANCH IF NOT DIGIT**: BND
  - (A) → ASCII (PC) → addr
  - If not digit 0 or 1 bit is 0

- **PUSH**: PUSH
  - (SP) → (SP - 1, SP)
  - (E)

- **PUSH AND LOAD IMMEDIATE**: PLI
  - (SP) → (SP - 1, SP)
  - (E)

- **BRANCH UNCONDITIONAL**: BRA
  - (PC) → (PC) + 000

- **BRANCH POSITIVE**: BP
  - (A) → 0 → (PC) → (PC) + 000

- **BRANCH ZERO**: BZ
  - (A) → 0 → (PC) → (PC) + 000

- **BRANCH NOT ZERO**: BNZ
  - (A) → 0 → (PC) → (PC) + 000

- **JUMP UNCONDITIONAL**: JMP
  - (PC) → (PC) → byte 2

- **JUMP TO SUBROUTINE**: JSR
  - (SP) → (SP) → byte 2

- **CALL**: CALL
  - (SP) → (SP) → byte 2

- **RETURN**: RET
  - (PC) → (PC) → byte 2

- **LOAD PC**: LD
  - EA → (PC) → (PC) → (EA)

- **EXCHANGE PC**: XCH
  - EA → (PC)

- **INCREMENT AND LOAD**: ILO
  - A → (A + 1) → (addr)

- **DECREMENT AND LOAD**: DLO
  - A → (A - 1) → (addr)

- **NO OPERATION**: NOP
  - (PC) → (PC) → 000
This feature makes possible the creation of stand-alone, BASIC programmed control systems, which need not use a terminal (for example a central heating controller). Programs can be developed using RAM and a terminal, then blown into EPROM for continued automatic use.

In program development (or RAM) mode, the user is required to initialise the system by entering two commands as follows:—

NEW (ADDRESS)
NEW Carryage Return.

These commands establish the start and end addresses for the new program which can then be entered, with line numbers, in the normal way.

In addition to NEW, the RUN, CONT (Continue), and LIST commands are available.

A useful range of BASIC statements is catered for, as follows:

REM anything: Remark (no operation).
CLEAR: Initializes all variables to 0, disables interrupts, and resets all stack (GOSUB FOR NEXT DO UNTIL).
(LET) var = expr: Assigns expression value to variable.
(LET) STAT = expr: Sets the STATUS word equal to the least significant byte of ‘expr’. When the STATUS word is used to enable interrupts at the hardware level, interrupt processing will be deferred for one statement.
(LET) & factor = expr: Sets the memory location pointed to by ‘factor’ equal to the least significant byte of ‘expr’. (LET) $ factor = “string”: Assigns a string in RAM starting at the address ‘factor’. Strings are terminated by a carriage return.
(LET) $ factor = $ factor: Memory to memory assignment (copy).
PRINT expr: Prints the value of ‘expr’.
PRINT “string”': Prints the string.
PRINT $ factor: Prints the string starting at the memory address ‘factor’.
IF expr (THEN) statements: Remainder of the program line is executed if ‘expr’ is true (non-zero).
FOR var = expr TO exp (STEP expr): For loop initiation. Loops may be nested to four levels.
NEXT var: For loop termination.
DO: DO loop initiation. DO loops may be nested to eight levels.
UNTIL expr: DO loop termination.
GO TO expr: Transfer control to statement number ‘expr’.
GO SUB expr: Call subroutine at statement number ‘expr’. Subroutines may be nested to eight levels.
RETURN: Return from subroutine.
INPUT var: Read value from console into variable.
INPUT $ factor: Read string from console into memory beginning at address ‘factor’.
LINK expr: Links an assembly language subroutine which begins at address ‘expr’. A “RET” instruction in this routine will cause continuation of the NSC Tiny BASIC program.
hyprogram
\(3) expr: Interrupt processing definition. When interrupt number 1 or 2 occurs, NSC Tiny BASIC will execute a GOSUB beginning at line number ‘expr’. If ‘expr’ is zero, the corresponding interrupt is disabled at the software level.
DELAY expr: Delay for ‘expr’ time units (nominally milliseconds). DELAY O gives the maximum delay of 1040 milliseconds.
STOP: Terminate program execution. A message is printed and the Microinterpreter returns to COMMAND mode.

Note the useful machine code LINK statement, ON 1 or 2 interrupt handler, and the DELAY capability, each of which make the 8073 BASIC ideal for control applications.

All arithmetic is performed in 16 bit signed integer format (–32768 to +32767) and the following operators and functions are provided.

Arithmetic operators: addition, subtraction, multiplication, division

Relational operators: less than, greater than, equal to, not equal to, less than or equal to, greater than or equal to

Logical operators: logical AND, logical OR, logical NOT
FUNCTION SUMMARY

@ factor: The memory/peripheral address for memory-I/O read/write operations.
STAT: STATUS register.
TOP: Top-Of-Program address (first available memory address after end-of-program byte).
INC(x), DEC(x): Increment or Decrement a memory location (non-interruptable for multiprocessing).
MOD(x,y): Modulus function (remainder of x/y).
RND(x,y): Random number generator (in interval x,y).

When used as interrupts (IE = 1) INTA has higher priority than INTB, and the IE bit has to be zero. The programmer is responsible for storing appropriate BRANCH or JUMP instructions in locations 0004H and 0007H, so that interrupt to access routines stored anywhere in memory can be achieved. (In the case of the 8073, this is handled automatically by the Tiny BASIC interpreter of course.)

Applications

The 8070 family provides a useful compromise between the 8048/28 style “everything-on-board” single-chip processors and the 8800/8808 style multi-chip solutions. It is probably not as good as the 880701 which can also provide this compromise, but it is, after a good deal less expensive!

I personally would not use the basic no-ROM 8070, because it has few advantages over other multi-chip processors like the 8802, but the 8073 with its on-chip BASIC interpreter is an excellent choice for hobby projects and can be recommended to everyone who wants to get into system design with the minimum financial outlay and risk. The design of a homebrew 8073 development system is quite straightforward, but for those who want to get started quickly there are a number of 8073 single board systems now available, such as the one designed by Essex University.
No. 2
LOGIC DESIGN CARD

Our second logic card covers logic sources, TTL supplies, supply distribution and a typical p.s.u. design for TTL.

MICROSTEPPEPER

"Freeze frame" your micro, instruction by instruction, to see what's going on during educational and debugging exercises.

TRANSPUTER

Inmos claim the Transputer array processor will set new standards in ease of programming, provide maximum performance to the user, exploit future developments in VLSI within a compatible family and be able to form fifth generation systems with large numbers of concurrent computing elements. Next month we take a close look at the device.

PRACTICAL ELECTRONICS

APRIL ISSUE ON SALE FRIDAY, MARCH 2, 1984
EUROPEAN SPACE AGENCY PROJECT

It is proposed that the ESA should submit designs for a space station for a joint enterprise with the United States. It is expected that it will require funding of some ten million pounds. ESA would retain the option of going it alone if the United States decided not to participate. It is, however, apparent that the radical re-designing necessary for use with a single shot launcher suggests that it is better to spend the money on launching by shuttle and concentrate on space stations. The experience with Ariane may also have influenced the decision. Greater attention is now being paid to finance when dealing with these very large projects. Of course, it is also true that new techniques are more reliable and that the hardware can be built to a high standard. The source of money has realised that risks are reduced by the methods in use, it must also be remembered that failures are less likely now so that insurance rates have fallen. It is true that some of the large organisations do this, but what of the smaller commercial concerns whose work is essential in the new world to come? It is essential in the long run that cooperation is the operative word. And by cooperation that it means all the nations of the world would participate.

COLUMBUS PROGRAMME

The study carried out by Germany and Italy was called Columbus. This was undertaken as a special study and centres on a pressurised module, capable of being docked with a station, for long duration missions. Thus it could be used by the USA to build space stations. The module could contain a docking facility, complete with pressurised docking-berthing port, and one experimental airlock. This module would be compatible with the Shuttle space orbiter's payload bay, since it will be of the standard size. A service module using a portion of the Columbus module could be developed as a support/link vehicle to the space station. It would be equipped with a Solar array that could provide power when going to and from the station. There would be a small manoeuvring system. Crew transfer would be by a manned space vehicle.

Unmanned platforms would be derived from Eureka or the German SPAS to operate from the station as free-flying carriers of scientific experiments. It is evident that commercially viable processes may be achieved effectively, as the shuttle has proved, it is already attracting finance. This is clear with the fall in insurance rates and movement to get places in the launch queue. It would be wise, for the sake of the vital experiments that science needs to continuously carry out, that the two sides get together. One way of doing itself a commercial service would be for commerce to finance science in a more extensive manner. It is true that some of the large organisations do this, but what of the smaller commercial concerns whose work is essential in the new world to come? It is essential in the long run that cooperation is the operative word. And by cooperation that it means all the nations of the world would participate.

FUEL CELLS

In the Orbiter Columbia, each fuel cell has been tested to a peak power of 16kW. Hitherto this has been at the lower level of 14/15kW, the reason for this being that the power was much more in demand for the 34 workdays of the mission of Columbia 9. The fuel cell power and water generation system contained one-third more than previously allotted. There are three stacks of 32 cells each in the vehicle. Earlier units flew with two stacks of 32 cells each. Each cell contains hydrogen and oxygen electrodes and an electrolyte of potassium hydroxide and water. The fuel cell normally will supply 2-12kW. At 2kW per cell, each stack can supply 32-5V and 61.5A of direct current. At 12kW it can supply 27-5V at a current of 43.6A. Water is recovered from the system which is used for drinking and cooling. The designers, United Technologies Power Systems, could be used in a system can be developed to supply a 24kW output and a 5,000 hour operating lifetime.

HEARING AND SPACE

Spacehab has proved an old theory of hearing originally proposed in 1914. This was related to the semi-circular canals of the inner ear. It was found that if air at different temperatures was blown into the ear, then the sensation of turning was induced, even if the person was not moving. It was believed that the cause was the different density of the air and the fluid in the semi-circular canal. Spacehab has now confirmed this theory. The investigators used the eye movements of the astronauts to assess the temperatures. Another test, which was designed to determine the adaptation of the body to weightlessness, caused movement sickness for specialist crew member Byron K. Lichtenberg, requiring the termination of a life-sciences experiment. A further test designed by an English psychologist, and mentioned in a recent Spacewatch, was designed for estimating different densities of pairs of balls which were visually of the same size.

A partially completed experiment was undertaken with Owen Garriott and Byron Lichtenberg; it was completed by Owen Garriott only because it caused Lichtenberg pain. The object was to discover the effect of weightlessness on reflexes and posture. The method was to drag the astronaut towards the floor while holding the knees to his chest during his descent. In order to minimise motion sickness the crew slowed all their movements during the mission. It is believed by Garriott that the movement of the head plays an important part in solving the problem. It certainly seems that some re-thinking needs to be done on these matters. Another experiment consisted of observing a field of dots which is rotating, followed by 35mm photographs of eye movements of the reaction of the subjects. This could not be completed owing to the failure of the photoflash. There will be a report published later and this will appear in a future issue of Spacewatch.

VENUS OBSERVED

There have been some reports of the Russian Space Explorer which are quite informative in that they confirm the finding of earlier space and ground-based instruments. The information is interesting for the planet has been the subject of two probes, Venera 15 and 16, which have been orbiting Venus since October. They have radar for investigating in close-up mode. It is claimed that resolution of one to two kilometres has been achieved. It needs a resolution of as good as at least one kilometre to assess the mountain elevations. If the resolution on these vehicles is one kilometre then we will have to wait for the publication of the results. The USA will not be ready to map at this level before 1988 or thereabouts. There are some pictures of the Soviet work around Venus. These are clear and show the general terrain, both craters and elevated land. There are large craters and considerable signs of volcanic activity. Near the pole it was noticeable that there is a large volcanic dome rising from an undulating terrain. One picture shows distinct lava flows, another shows a crater some 32 x 43 miles in size. Such pictures are only available after penetration of the cloud cover. The Soviet orbiters are able to overcome this.
EXPANDING THE

STEPPER MOTOR
CONTROL...

FOR AROUND £29

THIS month, we first catch up on the input and output routines held over from Part 4, and then go on to look at two stepper motor control boards ideal for the robotics experimenter.

Fig. 5.1. OUTPUT ROUTINE for displaying the state of ports in Binary

The following programs are not the most sophisticated, but it is hoped that they will help realise the potential of this series of interfaces.

05 PRINT"Shift/C1rHome":REM Clear screen
10 POKE 37138,255:REM Set DDR to required state
15 PRINT"DDR SETTING"
18 PRINT PEEK(37138):REM Display DDR setting
19 PRINT:PRINT:REM Spaces
20 PRINT"SET I/O REGISTER"
30 INPUT X:REM To put a decimal value in I/O Register
35 IF X<0 OR X>255 GOTO 20:REM Must be 0 to 255 inclusive
40 POKE 37136,X:REM Enter value
45 PRINT"I/O REGISTER"
50 PRINT PEEK(37136):REM Display it:PRINT:PRINT
55 PRINT PEEK(37136):REM Display it:PRINT:PRINT
60 PRINT"STATE OF PORTS"
70 PRINT"P7 P6 P5 P4 P3 P2 P1 P0"
80 GOSUB 100:REM Go to Decimal to Binary conversion
85 GOTO 20:REM To reset I/O Registers
90 GOTO 20:REM To reset I/O Registers
95 GOTO 20:REM To reset I/O Registers
100 PO=X-INT(X/2)*2:REM Decimal to Binary conversion
105 X=INT(X/2)
110 P1=X-INT(X/2)*2
115 X=INT(X/2)
120 P2=X-INT(X/2)*2
125 X=INT(X/2)
130 P3=X-INT(X/2)*2
135 X=INT(X/2)
140 P4=X-INT(X/2)*2
145 X=INT(X/2)
150 P5=X-INT(X/2)*2
155 X=INT(X/2)
160 P6=X-INT(X/2)*2
165 X=INT(X/2)
170 P7=X-INT(X/2)*2
175 X=INT(X/2)
200 PRINT P7;P6 ;P5 ;P4 ;P3 ;P2;13 I ;PO
205 PRINT:PRINT
210 RETURN:Return to line 80 in program

The conversion program is an integer arithmetic process and should therefore be possible on even the simplest machines. The principle is to divide the decimal figure by 2 and place the remainder in the least significant bit.

e.g. 255 Decimal becomes 11111111 Binary

<table>
<thead>
<tr>
<th>P7</th>
<th>P6</th>
<th>P5</th>
<th>P4</th>
<th>P3</th>
<th>P2</th>
<th>P1</th>
<th>P0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Similarly, 131 Decimal becomes 10000011

<table>
<thead>
<tr>
<th>P7</th>
<th>P6</th>
<th>P5</th>
<th>P4</th>
<th>P3</th>
<th>P2</th>
<th>P1</th>
<th>P0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
Fig. 5.2. This program makes further use of changing outputs during the running of a program.

```plaintext
05 PRINT "Shift/ClrHome":REM Clear screen
10 POKE 37138,255:REM Set DDR to required state
15 PRINT "DDR SETTING"
20 PRINT SET I/O REGISTER"
30 INPUT X:REM To put a decimal value in I/O Register
35 IF X<0 OR X>255 GOTO 20:REM (0 to 255)
40 POKE 37136,X:REM Enter decimal value
42 PRINT:PRINT
45 PRINT "INITIAL STATE OF PORT"
50 Z=X:REM Put value of X into Z
55 GOSUB 200:REM To dec/bin conversion routine
60 PRINT "CHANGE OUTPUT?"
65 INPUT Y:REM Enter decimal value
70 IF Y <0 OR Y>255 GOTO 60
72 Z=Y:REM Put value of Y into Z
75 GOSUB 200
80 INPUT "YES OR NO";AS:REM Examine output
82 IF AS="YES" GOTO 90:REM pattern before accepting
85 IF AS="NO" GOTO 60
90 POKE 37136,Y:REM Satisfactory, so enter
95 PRINT:PRINT:PRINT:PRINT
100 PRINT "I/O REGISTER"
105 PRINT PEEK(37136):REM Display it:PRINT:PRINT
110 PRINT "STATE OF PORTS"
120 PRINT "P7 P6 P5 P4 P3 P2 P1 P0"
130 GOSUB 200:REM To dec/bin conversion routine
140 GOTO 60:REM To reset I/O Registers
200 PO=Z-INT(Z/2)*2:REM Decimal to Binary conversion
205 Z=INT(Z/2)
210 P1=Z-INT(Z/2)*2
215 Z=INT(Z/2)
220 P2=Z-INT(Z/2)*2
225 Z=INT(Z/2)
230 P3=Z-INT(Z/2)*2
235 Z=INT(Z/2)
240 P4=Z-INT(Z/2)*2
245 Z=INT(Z/2)
250 P5=Z-INT(Z/2)*2
255 Z=INT(Z/2)
260 P6=Z-INT(Z/2)*2
265 Z=INT(Z/2)
270 P7=Z-INT(Z/2)*2
275 Z=INT(Z/2)
200 PRINT P7;P6;P5;P4;P3;P2;P1;PO:REM Display ports
205 PRINT:PRINT
210 RETURN:REM Return to line 140 in program
```

Fig. 5.3. INPUT ROUTINE for changing the DDR register and displaying the state of ports in Binary

```plaintext
05 PRINT "Shift/Clr Home":REM Clear screen
10 POKE 37138,255:REM Set DDR to required state
15 PRINT "DDR SETTING"
20 PRINT SET I/O REGISTER"
30 INPUT X:REM To put a decimal value in I/O Register
35 IF X<0 OR X>255 GOTO 20:REM (0 to 255)
40 POKE 37136,X:REM Enter decimal value
42 PRINT:PRINT
45 PRINT "INITIAL DDR SETTING"
50 GOSUB 200:REM To dec/bin conversion routine
55 PRINT "CHANGE DDR SETTING?"
60 INPUT "Y OR N";AS:REM Examine output
62 IF AS="YES" GOTO 300:REM To bin/dec conversion routine
65 IF AS="NO" GOTO 100:REM Carry on
100 PRINT "STATE OF DDR"
105 PRINT PEEK(37136):REM Display it:PRINT:PRINT
110 PRINT "KEY THIS IN":PRINT:PRINT
115 INPUT Y
120 PRINT "STATE OF PORTS"
125 PRINT "P7 P6 P5 P4 P3 P2 P1 P0"
130 Z=Y:REM Put value of Y into Z
135 GOSUB 200:REM To dec/bin conversion routine
140 GOTO 100:REM To reset display of I/O Registers
200 PO=Z-INT(Z/2)*2:REM Decimal to Binary conversion
205 Z=INT(Z/2)
210 P1=Z-INT(Z/2)*2
215 Z=INT(Z/2)
220 P2=Z-INT(Z/2)*2
225 Z=INT(Z/2)
230 P3=Z-INT(Z/2)*2
235 Z=INT(Z/2)
240 P4=Z-INT(Z/2)*2
245 Z=INT(Z/2)
250 P5=Z-INT(Z/2)*2
255 Z=INT(Z/2)
260 P6=Z-INT(Z/2)*2
265 Z=INT(Z/2)
270 P7=Z-INT(Z/2)*2
275 Z=INT(Z/2)
200 PRINT P7;P6;P5;P4;P3;P2;P1;PO:REM Display ports
205 PRINT:PRINT
210 RETURN:REM Return to line 140 in program
300 INPUT "ENTER BIT PATTERN ":BS:REM Binary to Decimal converter
310 IF LEN(BS) <> 8 THEN PRINT "8 BITS PLEASE"
315 GOTO 300:REM Do again if wrong
320 M=0:N=0
330 FOR P=8 TO 1 STEP -1:N=N +1
340 M=M+VAL(MIDS(BS,N,1))*2^(P-1)
350 NEXT P
360 PRINT BS="=";M
365 PRINT "KEY THIS IN"
370 INPUT M:POKE 37138,M
380 PRINT "STATE OF DDR"
390 Z=M:GOTO 45:REM Return to program
```

STEPPER MOTOR INTERFACES

The next stage in this series concerns interfacing the computer with stepper motors, and their application in practical experiments. Two stepper motor controllers are described, with designs for two p.c.b.s which will each accommodate four controllers. This enables experimentation with XY movement involving two axes, or simple robotics having four axes, as opposed to the usual five or six axes normally found on commercial controllers, but of course, at a fraction of the cost of the latter.

The SDB520 I.C. is chosen for its versatility and power handling capabilities, whilst the SAA1027, though more limited in its application, has been a popular device in schools and colleges for several years.

The prime consideration in interfacing is always the safety of the host computer. The SDB520 and SAA1027, because of their different inherent characteristics, are treated differently where the method of electrical isolation from the computer is concerned. This is explained within the text covering the individual devices.

Stepper motors are available, suitable for such a wide variety of applications that it is impossible to report on them to any great extent in the space available here. A useful
source of very cheap, yet top quality low and medium power motors is ex-equipment. This source often provides much of the hardwear required for constructing a functional machine. A visit to an Amateur Radio rally is well worth the entrance fee, as many of the advertisers in Practical Electronics and Practical Wireless attend with such bargain packages. More important, in general, these people are not just salesmen, but practical constructors who have tried the equipment out for themselves, and are free with advice on wiring and serviceability. Some general comments are therefore included which are applicable to the article.

Some programming hints are included, suggesting methods of "stepping" the motors clockwise, counter-clockwise, and for angular movement where more than one motor is being operated.

Those who have constructed the l.e.d.s and switches board can use it for development of their programs as with any other output program.

THE SDB520 DRIVER BOARD

The first p.c.b. described uses the versatile SDB520 Stepper Motor Driver i.c., which can be used with 3-phase or 4-phase motors. In addition to this, the chip enables the use of either type of motor in single, dual, or single/dual phase excitation.

In order to accommodate all these functions, connections from pins 3, 4 and 5 have been left open. In all modes, pins 7 and 10 are connected via a 2k2 resistor to the +5V d.c. supply, whilst pins 3, 4 and 5 are either individually coupled with these, or taken to ground. Provision has also been made to mount capacitors between motor coils 1 and 2, 2 and 3, 1 and 3 for 3-phase motors and 1 and 2 and 4 for 4-phase motors.

Opto isolated output from the computer is provided, a feature that the author normally recommends. However, in the case of the SDB520, it is well protected internally against short circuit, making opto isolation at low motor voltages and current, less necessary. It is provided for the less experienced constructor, and those who may have larger motors available.

The SDB520 uses the +5V d.c. supply from the computer, provision for external supply being made for use with computers other than the Vic 20. The outputs from the driver turn on their associated transistors sequentially, allowing current to flow through the relevant motor coil. The transistors used on the board are BFY51, 2N3053 or similar 0.7W NPN transistors that can handle up to 1A of current.

<table>
<thead>
<tr>
<th>RESISTORS</th>
<th>VALUE</th>
<th>PARTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1,2,6,7,11,12,17,18</td>
<td>2k2 (8 off)</td>
<td>1N4001 (14 off)</td>
</tr>
<tr>
<td>R3,4,5,8,9,10,13–16, 19–22</td>
<td>100 (14 off)</td>
<td>2N3053 or similar (14 off)</td>
</tr>
<tr>
<td>R23</td>
<td>See note</td>
<td></td>
</tr>
</tbody>
</table>

**Capacitors**

- C1,6,11,15: 2μF (4 off)
- C2,7,12,16: 10μF (4 off)
- C3,4,5,8,9,10,13,14,17,18: 1μF poly (10 off)

**Transistors & Diodes**

- D1–14: 1N4001 (14 off)
- TR1–14: 2N3053 or similar (14 off)

**Integrated Circuits**

- IC1–4: SDB520 (4 off)
Should there be a need for greater current handling, 2N3055 transistors can be mounted externally on heatsinks. Motor voltages are typically 12 to 24V d.c. and might require a small value 50W wirewound resistor at the common positive motor supply to correct L/R ratio. This information should be available with the motor.

The p.c.b. is single-sided fibre-glass, approximately 165 x 148mm, and requires short links on the upper surface. As mentioned earlier, in order to increase the versatility of the board, connections have to be made between pins 3, 4 and 5 and ground, or commoned with pins 7 and 10. A solder blob is all that is required, and this can be carried out neatly by using a single strand from multi-strand cable to bridge the gap and allowing solder to flow over it from side to side.

Pulses are supplied to two inputs, CD Counter clockwise, at pin 1 and CU Clockwise, at pin 2. A change from Low to High and back to Low will trigger the chip. The inputs are designed with high noise margin, and comprise a Schmitt trigger circuit.

OC at pin 3 selects 3 phase, Low, or 4 phase, High, operation. EA and EB on pins 4 and 5, comprise the mode switching terminal.

```
<table>
<thead>
<tr>
<th>EB</th>
<th>EA</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>0</td>
<td>Line drive facility</td>
</tr>
<tr>
<td>01</td>
<td>0</td>
<td>Single phase excitation</td>
</tr>
<tr>
<td>01</td>
<td>1</td>
<td>Dual phase excitation</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>Single/dual phase excitation</td>
</tr>
</tbody>
</table>
```

Mo at pin 6, provides a sequence monitor, low, when counter content is 000. OFF 01.3 on pin 7 and OFF 02.4 on pin 10 provide excitation OFF or line drive input terminal, when terminals become Low without relation of sequence content, when output terminals are = 0. At pin 8 is the OV supply terminal. Vcc2 at pin 9, the output driver power supply. Output driver terminals are at pin 11, 4, pin 12, 2, pin 13, 3, and pin 14, 1. A clamping diode is inserted in the output. R at pin 15 is the Reset input terminal, tied to Vcc via a 2k2 resistor. Vcc1 at pin 16 is the power supply for the logic circuit.

### USE OF OPTO ISOLATORS

Those who have followed this series will note that the I.e.d.s in the opto isolators are turned on by making the cathode low relative to the power supply. This means, without the inclusion of inverters, that the logic is incorrect for an output on the Vic 20. For the purists this is overcome by complementing the binary pattern required at the output port and placing this value in the I/O Register.

```
| Output required | 10101010  |
| Complement      | 01010101  |
| Total           | 11111111  |
```

The easiest way, of course, is to treat the outputs required as inputs.

### SDB520 DRIVER EXCITATION SEQUENCE

#### 3-Phase motor excitation

<table>
<thead>
<tr>
<th>Single phase</th>
<th>Dual phase</th>
<th>Single/dual phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1 Q2 Q3 Q4 CCW</td>
<td>Q1 Q2 Q3 Q4 CCW</td>
<td>Q1 Q2 Q3 Q4 CCW</td>
</tr>
<tr>
<td>0 1 0 0 0</td>
<td>0 1 1 0 0</td>
<td>0 1 0 0 0</td>
</tr>
<tr>
<td>1 0 1 0 0</td>
<td>1 0 1 1 0</td>
<td>1 1 1 0 0</td>
</tr>
<tr>
<td>2 0 0 1 0</td>
<td>2 0 0 1 1</td>
<td>2 0 1 0 0</td>
</tr>
</tbody>
</table>

#### 4-Phase motor excitation

<table>
<thead>
<tr>
<th>Single phase</th>
<th>Dual phase</th>
<th>Single/dual phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1 Q2 Q3 Q4 CCW</td>
<td>Q1 Q2 Q3 Q4 CCW</td>
<td>Q1 Q2 Q3 Q4 CCW</td>
</tr>
<tr>
<td>0 1 0 0 0</td>
<td>0 1 1 0 0</td>
<td>0 1 0 0 0</td>
</tr>
<tr>
<td>1 0 1 0 0</td>
<td>1 0 1 1 0</td>
<td>1 1 1 0 0</td>
</tr>
<tr>
<td>2 0 0 1 0</td>
<td>2 0 0 1 1</td>
<td>2 0 1 0 0</td>
</tr>
<tr>
<td>3 0 0 0 1</td>
<td>3 0 0 0 1</td>
<td>3 0 1 1 0</td>
</tr>
</tbody>
</table>

Sequences and stages 0 and 1 at other stages of sequence.

Pads are provided on the p.c.b. should it be wished to monitor the outputs whilst developing programs and setting up motors.

The monitor is active low, therefore when it becomes active at the beginning of each sequence, the cathode of the I.e.d is pulled down relative to the 5Vd.c. supply and comes on.

### THE SAA1027 DRIVER BOARD

The SAA1027 is intended for pulse to step control of four-phase two stator motors. It is capable of driving a motor winding load of 350mA per phase and is encased in a 16 pin dual in line plastic package.

Pulses are supplied to a single input, whilst the direction of rotation is controlled by a voltage level applied to a gate input. A further input sets the four output stages. Supply voltages can be between 9.5 and 18Vd.c., but a single 12Vd.c. power supply is normally used to operate the driver.
Fig. 5.4(a). Circuit diagram of SDB520 driver (3-coil motor type) annotated as in the p.c.b. layout shown below (channels A and B).

Fig. 5.5. P.c.b. layout of stepper motor control board 1. SDB520 type (actual size). This is a versatile board, designed to accommodate various component configurations. For example, the ILQ74s (IC5 & IC6) optoisolators are optional.
Fig. 5.4(b). Circuit diagram of SDB520 driver (4-coil motor type) annotated as in the p.c.b. layout shown below (channels C and D)

Fig. 5.6. Stepper motor control board 1 component layout, shown with channels A & B dedicated to the 3-coil configuration, and channels C & D dedicated to the 4-coil configuration. Asterisks draw attention to the link areas that allow reconfiguration. The I.e.d.s allow optional data signal monitoring.
i.c. and the motor. The output drivers (pins 6, 8, 9, 11) are open collector. The breakdown voltage is 18Vdc and this must not be exceeded.

**Pin connections**
(1) no connection  
(2) Set input S  
(3) Direction input (CW/CCW) R  
(4) Bias resistor B (positive supply)  
(5) Ground (negative supply)  
(6) Q1 (output)  
(7) no connection  
(8) Q2 (output)  
(9) Q3 (output)  
(10) no connection  
(11) Q4 (output)  
(12) Ground (negative supply)  
(13) VD (positive supply)  
(14) VP (positive supply)  
(15) Trigger input T  
(16) no connection

**INPUTS**
The three inputs are controlled by applying high or low voltage levels to the terminals. The high level voltage can be between 7.5 and 18Vdc (12Vdc typical) and is normally equal to, but not greater than, the voltage on pin 14. Input current is high, typically 1µA. The low level voltage can be between 0 and 4.5Vdc maximum. Low level current is typically ~30µA per input.

**TRIGGER INPUT**
The voltage on T, pin 15 is normally high when not being pulsed and is held at Vs via a 4k7 resistor. A change from high to low and back to high will trigger the i.c. The motor is connected to the output stages on the positive edge, low to high of the pulse.

**SET INPUT**
Pin 2, S is tied to Vs, enabling all outputs.

**DIRECTION INPUT**
Applying a high level to pin 3 causes the motor to be stepped CCW, whilst a low level to pin 3 causes the motor to step CW. The input is tied high via 4k7 resistor for maximum noise immunity.

**BIAS RESISTOR**
RB can be calculated, first from supply voltage and motor coil resistance to arrive at IQ. Then, by reference to graph, 1B and VS permits calculation of RB. When motors with current of 350mA (max) per winding are used, the bias current to pin 4 should be 80mA (max).
A typical surplus/ex-equipment stepper motor

Bias current and output current relationship of SAA1027 output stage

Fig. 5.10. Component layout of stepper motor control 2
Likewise, when the output current is 50mA, bias current should be 20mA. A linear graph plotted between these values is shown on page 43.

The R/C network at pin 14 stretches the pulse from trigger input, pin 15, to a length detectable by the trigger stage.

OUTPUTS
The switching sequence of the four phases is controlled by the logic part of the circuit and the four output stages, Q1 at pin 6, Q2 at pin 8, Q3 at pin 9 and Q4 at pin 11 are protected against transient spikes by integrated diodes.

OPTO ISOLATION
It is usual to use TTL Buffers between the computer and the SAA1027, but due to the danger of the maximum 18Vd.c. being exceeded, and added susceptibility of the i.c. to overheating and breakdown, it was decided to use opto isolation.

The collector of the transistor in the opto isolator is held high at logic “1” via the 270k resistor connecting it to the power supply. When a logic “0” at the output port sinks the i.e.d. and turns it “on”, the transistor is turned on also, causing the collector to go low. When the output changes back to logic “0” the i.e.d. turns off. The transistor also turns off, bringing the collector once again to high, causing excitation and creating a pulse.

Should overheating be experienced, clip-on d.i.i. heatsinks are available from most advertisers.

This board is much smaller than the SDB520 board because the driver is complete in itself and requires no external components beyond the capacitor and resistors mentioned. It is made on a 120mm square of single sided fibreglass p.c.b. Short links are required on the component side to connect the ground rails. Provision is made for an external 5Vd.c. power supply if used on a computer other than the Vic 20.

STEPPER MOTORS
A summary of various descriptions of a stepper motor would be “a direct digital motion control device that converts electrical pulses into discrete mechanical rotational movements. It possesses the ability to rotate in either direction, as well as start and stop at various mechanical, rotational positions. Its shaft moves in precise angular increments for each input excitation or step. The stepper motor allows control of position, velocity, distance and direction”.

STEPPING
Due to the nature of its construction, unlike a normal running motor, a stepper motor moves through a precisely defined arc of a complete revolution for each pulse and is held in that position until the next pulse, which moves the rotor through the same angle of rotation. Small motors usually come in 3 or 4 phase types and the number of steps to a complete revolution varies greatly, typically from 4 to 90, or angular movements varying from 90 degrees to 4 degrees.

SEQUENCE
Each phase is excited sequentially, the rotor moving in precise steps, in the same direction, for each excitation. Reversing the stepping sequence of the phases reverses the direction of movement of the rotor by the same precise angle. These processes are controlled by the internal logic of the stepper motor driver i.c.

ACCURACY
Unlike a normal motor, which keeps running after removal of power until stopped by friction, the stepper motor stops at a predictable position. Any errors of angular position are restricted to each single movement and are non-accumulative. An error of 1 degree in each and every step, no matter how many steps are performed, will be an error of just 1 degree at the end of a cycle. Accuracy varies from 0-01 degree for small steps to 5 degrees for large steps. Obviously, for precise positioning, the greater the number of steps the greater the accuracy.

In dual-excitation mode, two coils are excited simultaneously. This stops the motor in a position half-way between normal stopping positions, but because of increased holding torque gives consistent accuracy.

HOLDING TORQUE
At standstill, the torque required to deflect the motor a full step is called the Holding Torque. This is normally higher than the running torque and acts as a strong brake in holding the load. The higher the holding torque the more accurate the position of the rotor. Most stepper motors will operate at much lower voltages than that recommended by the manufacturer, but with decreased holding torque and therefore decreased accuracy. A similar situation can arise with increased step frequency due to the fact that the rise time of the coil limits the percentage of power actually delivered to the motor. The result can be incorrect starting or lack of steps. This effect is sometimes compensated for by increasing the supply voltage and including a series resistor to correct the L/R ratio of the circuit as depicted in the SDB520 4-phase schematic.

Next Month: Applications and control of stepper motor boards. Also, DAC and ADC boards.
Step-by-step fully illustrated assembly and fitting instructions are included together with circuit descriptions. Highest quality components are used throughout.

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- Contact breaker triggered - includes bounce suppression circuit.

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- Contactless adaptors included for majority of 4 & 6 cylinder vehicles
- Easy to assemble, easy to fit

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- Gives highest possible spark energy
- Clip-to-coil or remote mounting
- Rugged die-cast case
- Contactless adaptors included for majority of 4 & 6 cylinder vehicles

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- a.c. I 3mA, 10mA, 30mA, 100mA, 1A, 10A
- d.c. I 50µA, 100µA, 300µA, 1mA, 10mA, 30mA, 100mA, 1A, 10A
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- a.c. V 100mV, 1V, 3V, 10V, 30V, 100V, 300V, 1000V
- a.c. I 3mA, 10mA, 30mA, 100mA, 1A, 10A
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This month we complete our brief look at monitors for home computers by reviewing two current models. The two units tested are representative of the most popular types of monitor for home computing: a high resolution monochrome monitor, and a medium resolution RGB monitor. The monitors have been reviewed primarily from a user's viewpoint, and the usual technical tests have been largely replaced by an extended practical evaluation with a BBC Micro.

**NOVEX MONOCHROME MONITOR**

**First Impressions** The Novex 12/800 is a transistorised custom-designed monochrome monitor from Taiwan. It comes well packed, and is supplied complete with a manual and a phono-to-phono lead. The manual, although rather quaintly worded in places, is well illustrated and provides all of the necessary information.

The unit has a 12-inch green (P31) phosphor display tube, and is attractively packaged in a two-tone beige and brown steel case measuring approximately 30x29x30cm. The colour scheme and styling are pleasing to the eye, and are a good match for Apple or BBC computers. The tube has a moulded surround which includes an illuminated mains switch and a door concealing a number of controls. The monitor weighs approximately 8kg, and is mounted on rubber feet. The video connectors, mains lead and two slide switches are located on the rear panel.

**Front Panel** The screen surround includes the illuminated mains switch, and a button to release the door concealing the preset adjustments and controls. The two screwdriver preset adjustments are for picture height and width. These are factory adjusted for optimum setting, and should therefore need little or no attention. The remaining controls are intended for user adjustment and allow setting of brightness, contrast, horizontal hold, and vertical hold. All of the presets and controls are clearly labelled.

The four controls all have a useful range of adjustment. Correct setting of the two hold controls is well described in the manual. The adjustment of contrast and brightness is not quite so well covered in the manual. The best way to perform the adjustment was easily found to be as follows. Both controls should be turned fully clockwise for the brightest possible picture; the raster should then be clearly visible. Next the brightness is reduced until the raster just disappears. Finally the contrast should be adjusted to produce an acceptable picture; the actual setting here is a matter of personal preference. Once set, little adjustment to any of the controls is necessary, and then usually only to take account of different ambient lighting conditions.

**Rear Panel** The mains power lead enters through a securing grommet on the monitor's rear panel. The length of this lead is a rather miserly 1.5 metres (in common, it must be said, with much other equipment); no plug is provided. Also on the rear panel are two miniature slide switches and two phono sockets, all clearly labelled. The reviewers' first reaction to the use of phono sockets was to look around for a spare pair of BNC sockets to fit in their place, but this again is a matter of personal preference.

The video input signal is connected to one of the phono sockets, and the second socket is internally connected to the input socket. This provides a video output signal which is useful for loop-through connection to more than one monitor. In order to be able to obtain the maximum video bandwidth, the video signal should be terminated (by 75 ohms) at the last monitor in the chain. A switch is provided to allow the signal to be left unterminated (high impedance for an intermediate unit), or terminated in 75 ohms (for the last or only monitor). In practice, the two phono sockets are interchangeable, and are labelled merely for convenience.

The second slide switch on the rear panel is labelled 'GRAPHICS' and 'DATA'. This allows the monitor's performance to be separately optimised for high resolution graphics and 80-column text.

**Inside The Case** On the rear of the case is a removable panel bearing warnings of electrical shock risk, and advising of no user serviceable components. The internal construction is based on a large single-sided p.c.b. which is securely mounted on the base plate. This contains the majority of the components, and is screen printed for ease of component identification. Mounted on the base of the tube is a much smaller p.c.b. which carries the video amplifier. This is a common practice to minimise stray capacitance, and hence allow the the maximum video bandwidth to be retained.

The internal construction is very compact, and represents a utilitarian appearance in interesting contrast to the external styling. The unit is clearly a custom designed monitor, rather than a modified television chassis. The power supply incorporates a mains transformer chassis. The power supply incorporates a mains transformer, and has no provision for operation from an external 12 volt d.c. supply.

Looking inside the case from the rear, there are three...
preset controls mounted on the edge of the main circuit board. These turn out to be (left to right): picture height, focus and black level adjustments. These are factory presets which are not intended for user adjustment.

**Picture Quality** In order to evaluate the picture quality, the monitor was connected to the video output of a BBC Micro. Tests were conducted using 20, 40 and 80-column text, and resolution coloured graphics displays. The video signal was terminated by 75 ohms.

After using a black and white television, the first thing that strikes the user is the clarity of the display. The difference between the display on a monochrome television, and the display on the monitor, has to be seen to be believed. In fact, going back to the television display after a number of hours of use with the monitor can cause acute frustration. The temptation is to keep trying to adjust the television tuning to regain the 'lost' definition; a substantially fruitless exercise. It is on 80-column displays, however, that the difference is most apparent. The test is easily readable on the monitor, whereas on a television display, prolonged viewing is tiring.

The other factor which is quite noticeable is that the green phosphor has a significantly longer persistence than the white phosphor. This is quite typical of the P31 phosphor. When displayed in a white background, and probably contributes to the strain-free display which can be obtained on 80-column displays. This is quite typical of the P31 phosphor, and probably contributes to the strain-free display which can be obtained on 80-column displays. It is on 80-column displays, however, that the difference is most apparent. The test is easily readable on the monitor, whereas on a television display, prolonged viewing is tiring.

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In 80-column mode the use of the 'graphics/data' switch eventually becomes clear. When switching from 'graphics' to 'data', very close observation of the screen shows that the leading edges of all characters become very slightly emphasised. This does not have any noticeable effect except on a very narrow vertical line (e.g. the centre upright of 'V'), which then becomes more clearly visible. Such lines represent very high video frequencies, and often result in a slightly fainter display, although remaining quite visible. The 'data' position appears to compensate for this effect by altering the time constant of the video amplifier to induce slight ringing. The end result is to allow the display of 80-column text to be outstandingly clear, but without compromising very high resolution graphics displays.

The overall display shows good linearity in both horizontal and vertical directions. There is no evidence of power supply problems with the display brightness, and the unit runs cool even after many hours of use. The picture focus is generally excellent, with only slight defocusing evident in the top right corner of the display. This would normally go unnoticed in everyday use. The display resolution is quoted at 1000 lines in the screen centre, and 800 lines in the corner. This is more than adequate for 80-column text, and in practice individual pixels can be distinguished (the BBC Micro uses 640 pixels per line in 80-column text mode).

The BBC Micro produces displays in up to eight colours, although black is not really a colour as such. When displayed on the Novex monitor, these colours appear as shades of green, but they are still distinguishable by virtue of their different brightness levels. In order of decreasing brightness, the colours appear as:

- **WHITE** (Brightest)
- **YELLOW**
- **CYAN**
- **GREEN**
- **MAGENTA**
- **RED**
- **BLUE**
- **BLACK** (Darkest)

As delivered, the review unit was unable to display blue at all, and had some difficulty with red. However, after adjustment of the black level internal preset (not a user adjustment), all of the colours were visible and distinguishable.

**VERDICT** The overall impression after prolonged use (including preparing this review!) is excellent. The monitor is neat, compact, pleasant to use and fuss-free. It is ideal for word processing and any high resolution applications, and would make a very welcome addition to any home computer system.

**CABEL RGB MONITOR**

**First Impressions** The Cabel 370A is an RGB colour monitor which is supplied complete with a BBC Micro compatible RGB video lead. The unit as delivered has its colour settings optimised for the BBC Micro, and is extremely well packed in a double box. A single A4 instruction sheet is supplied which gives basic operating information, but this appears to have been rather hastily prepared, and contains a number of typographical errors. Hopefully this is an interim measure, pending production of a more substantial manual.

The monitor has a 14-inch Mullard colour tube with a dot pitch of 0.65mm, and is packaged in a strong moulded case with an integral combined carrying handle and ventilation slot. The colour scheme is beige (case body) and black (front panel). It must be said, however, that the overall styling is spoilt by poor design of the front panel. This is a great shame because the effect could have been so much better with only a little more effort and attention to matters of styling and ergonomics. As it is the two front panel controls (round knobs) are too close together, and in sharp contrast to the square mains switch. The mains indicator is a small (round) I.E.D. in the middle of a large blanking plug filling the hole occupied on previous models by the video connector. This said, we should remember that the prime function of the unit is to produce colour displays.

The overall dimensions of the monitor are probably the smallest possible for a unit using a 14-inch tube, and are approximately 39 x 36 x 41 cm. The case itself tapers from front to back, and also inclines the screen usefully backwards to assist viewing. The height of the screen above the bench would allow it to stand behind many micros, in the (unlikely) event that sufficient bench space is available. The best alternative viewing position involves placing the monitor beside the computer. The unit weighs approximately 13 kg, and is mounted on four rubber feet. All controls are on the front panel, and all leads connect at the rear.

**Front Panel** The front panel contains the mains switch and power indicator. The indicator provides a useful indication of whether the automatic power supply shut-down

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circuitry has operated. Two controls allow adjustment of brightness and 'interlacing'. The latter control seems wrongly labelled (and spelt!), and behaves as a contrast control; it certainly has no effect on picture scan interlacing. Both controls work well and have a useful range of adjustment.

Rear Panel The mains power lead enters the unit through a grommet on the rear panel. This lead is approximately 2 metres long (still a little on the short side, but a useful length), and has a fitted 13A plug. The video input is via a 6-pin DIN socket, wired to be compatible with the BBC Micro. The RGB input is terminated in 75 ohms, and automatically switches to accept inputs with positive or negative sync. The rear of the case contains ventilation slots, which are numerous enough to provide a good flow of air, yet narrow enough to prevent the intrusion of foreign objects.

In the second case at the rear of the case is a cable which warns of electrical shock hazard if the cover is removed, and indicates that there are no user serviceable parts inside. Access is provided to ten preset adjustments through small holes in the base and rear of the case, obviating the need to remove the cover. The adjustments provided are for: red/green/blue input sensitivity, horizontal/vertical shift, field sync/linearity/amplitude, line width and linearity, and focus. The unit is provided fully aligned, and no adjustments were found to be necessary to the review sample.

The case itself is of substantial construction, and is removed by unscrewing the four feet. The internal construction of the monitor is extremely impressive, and is based around a standard Mullard colour monitor chassis, to which the case is attached. The chassis is built around the cradle which supports the colour tube. The tube itself is a standard television style 90-degree tube. The main circuit board is mounted in the base of the cradle, and is neatly laid out for automatic component insertion. The three (red, green, blue) video amplifiers, and the focus control, are mounted on a smaller second board mounted in the base of the cradle, and is neatly laid out for automatic component insertion. The three (red, green, blue) video amplifiers, and the focus control, are mounted on a smaller second board mounted on the tube base. Signal connections between the sub-assemblies are by means of multi-way cables/connectors. All in all, a very well constructed unit incorporating the very latest technology.

Picture Quality The picture quality of the Cabel monitor was evaluated by driving it from the RGB output of a BBC Micro. The tests involved 20,40 and 80-column text, and high resolution colour graphics.

When set against a standard, well-adjusted domestic colour television, the picture quality from the monitor can only be described as excellent. The difference has to be seen to be believed. The saturated, stable colours which are obtained are a delight to observe, and it is possible (using only the front panel controls) to obtain a colour display to suit all tastes. The usual problem is that no two people can ever agree on the subjectively 'correct' settings for any colour display; the reviewers certainly disagreed! The important point, however, is that the range of adjustment available on the monitor is more than enough to cater for all tastes. Whatever your preference, the final picture quality is excellent.

When used for text displays, the CE370A produces perfectly acceptable and stable displays for 20 and 40-column text. However, the 10MHz bandwidth causes a few problems with 80-column text. The actual horizontal resolution quoted for the display is 430 pixels per line, and the BBC Micro uses 640 pixels per line for 80-column text. The resulting text is still quite readable, but not pleasantly so for prolonged periods. A viewing distance of approximately 12 metres (eye-to-screen) was found to be the optimum for 80-column text. If contemplating frequent and prolonged use with 80-column text, the higher resolution CAT370 (22MHz, 0.65mm dot pitch, 430 pixel) or HR370 (22MHz, 0.3mm dot pitch, 640 pixel) models should be considered as possible alternatives.

The ideal, and the recommended, position for the monitor is behind the computer console. This has the advantage of increasing the separation between the eye of the user and the screen. The bottom of the screen is then 9cm above the bench level, and this means that it is not obscured by most micros. The screen size should be considered when deciding where to position any monitor; a large screen too close can be as bad as a small screen too far away. Both situations can lead to fatigue with prolonged use. In use the monitor normally runs warm, but the ventilation is quite adequate, and no hot spots are evident.

VERDICT The overall impression gained from prolonged use (including preparing last month's article) is of a unit which offers good performance for price. The styling is a matter of personal taste, but the colour quality of the display is unreservedly excellent. It would be unreasonable to expect too much from a medium resolution RGB monitor when it comes to displaying 80-column text. The performance achieved is as good as could be expected, and in general it is necessary to spend around twice as much to obtain a monitor to match (say) the Novex in this respect.

FINAL THOUGHTS

The selection of a monitor for your particular application, and to suit your budget, will always be a matter of personal choice. The two units reviewed are both worthy of serious consideration. The reviews also indicate some points which might be considered when making a selection. Wherever possible, try and see your final choice of monitor in action before you take delivery; both review samples arrived damaged after carriage by road and rail, despite having been very well packed. Prices for monitors appear to have substantially stabilised, so there is unlikely to be any significant price reductions in the near future.

The Novex 12/800 is priced at £75.62 excluding VAT and p&p and is available from Display Distribution Limited, 35 Grosvenor Road, Twickenham, Middlesex (01-891 1923).

The Cabel 370A is priced as £199.50 excluding VAT and p&p and is available from Cabel Electronics, 19 High Street, Tewkesbury, Glos. (0684 298840).
Soon after Britain's state-owned microelectronics company passed its fifth anniversary it sent out advance information on its latest development, a single-chip microcomputer called a Transputer. The fact that the device did not at that moment exist as a real component illustrates both the confidence of Inmos and the commercial conditions in which the company has to operate.

With fierce competition from the mighty American and Japanese semiconductor industries and prices of integrated circuits falling all the time, the only way to survive commercially is to keep on developing new products that will leapfrog their rivals in facilities, performance or price. In such conditions you have to announce and describe your latest development well ahead of its actual existence as a component on the market.

The idea, of course, is to stake a claim as soon as possible with the potential customers—the electronic equipment manufacturers—who are always waiting to pounce on devices using the latest and most advantageous technology to give their own products a competitive edge. To make such claims ahead of actuality you have to be very confident.

**Genesis**

So what has Inmos actually achieved in its first five years in this dangerously competitive world? Inmos International PLC, as it is now known, was founded in August 1978 specifically to develop, manufacture and sell very large scale integrated circuits (VLSI) as standard devices in volume production. This means ICs with 100,000 or more transistors on a single chip.

The Labour government of that time had become convinced that the UK should have a stake in this high-technology business. Apart from the international trading advantages of being in such a field of manufacture, they felt it would create more jobs and would also help the UK electronics industry to be less dependent on imported devices, or the products of foreign-owned companies, and therefore less vulnerable to technical/commercial decisions made in other parts of the world.

As British private capital had not produced any such VLSI company it was decided to invest £50M of public money in the venture, £25M immediately (1978) and a further £25M at a later date. This was arranged through the National Enterprise Board (NEB), a state run agency already existing to launch or support industrial companies felt to be important to the economy.

The NEB is now part of the British Technology Group. Recently it has been given the new role of assisting technology transfer and will be divesting itself of its holdings in the share capital of various companies.

It so happened that the government's aim had coincided with the ambitions of two very able technologists, who were then looking for an opportunity to exploit their ideas of producing large information processing systems on small silicon chips. Iann Barron, an English systems research specialist, then aged 42, had formed the first UK minicomputer company, Computer Technology Ltd, in 1965 and later had been a consultant in computers and information technology. The second party was Dr Richard Petritz, an American physicist, then 55, who had directed Texas Instruments' semiconductor research for ten years from 1958 and later had formed a company in Dallas for launching new electronics firms—one of which was Mostek.

Legend has it that these two discussed and formulated their common aims at Chicago Airport after a technical conference in 1977. Iann Barron was already aware of UK government intentions through his consulting work for the Department of Industry (now DTI), and it was only a matter of months before an agreement was signed to set up the new British VLSI company with these two individuals as founders.

A third founder was another American physicist, Dr Paul Schroeder, then 38, who had worked for Bell Telephone Laboratories on memory design and in 1967 had become director of memory design engineering at Mostek. (Dr Schroeder, an expert on MOS dynamic memory devices, resigned from Inmos in 1982.)
The essence of the setting-up agreement was that Inmos would be a subsidiary of the NEB. In return for the £50M of public funds, the NEB was to hold 72½ per cent of the equity in the company. A further 15 per cent of the shareholding was to be divided among the three founders and the remaining 12½ per cent between key employees of the company. Richard Petritz was appointed managing director.

The overall plan was to start by developing, manufacturing and selling random access memories (RAMs) because there was already a large and growing market for these devices. This activity would provide a manufacturing and commercial base from which other VLSI devices would be launched. Process technology and initial manufacturing would be based in the USA because that country had a large pool of people already skilled in VLSI technology. Then, after the products had been launched there, they would be transferred to the UK for volume production. Memories would be marketed and sold from the USA because North America provided a very big demand for these products.

THE EARLY YEARS

Less than a year after the founding of Inmos, and before the NEB had produced the second £25M of the investment capital, the 1979 General Election brought in a Conservative government—a government opposed to the principle of state-owned industries, committed to keeping down public expenditure and unwilling to use public funds to support loss-making owned industries, committed to keeping down public expenditure and unwilling to use public funds to support loss-making owned industries. The affairs of Inmos then moved into the political arena.

The new government hesitated for about a year and clearly would have liked the second £25M to be found from private sources of capital. There was disension within the Department of Industry and lengthy deliberations on where the UK factory was to be sited. But Sir Keith Joseph, the then industry minister, was in favour of the original method of funding and in the end the remaining £25M of public money was provided, by a new NEB, in August 1980.

Meanwhile the Inmos plans for an American plant had gone ahead on schedule. Colorado Springs had been chosen as a good area for potential employees and by September 1979 the company had started building a plant there. By March 1980 an experimental establishment at Harrison Park had developed an NMOS process for making RAMs with 2–3μm active area widths in the silicon. And by May 1980 the first samples of 16K static RAMs made by this process were available. The Colorado Springs plant started operations in March 1981 and by December of that year had produced the first samples of dynamic RAMS.

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The abbreviation MOS stands for the three kinds of material, metal—oxide—semiconductor, used to construct the integrated field-effect transistors in these devices. The N in NMOS indicates that the conducting channel of these integrated f.e.t.s is silicon containing impurity atoms giving it a greater density of conduction electrons, making them the majority carriers, than of mobile holes—in other words the silicon is an n-type semiconductor. In the RAMs referred to the f.e.t. structures within the silicon are 2–3μm wide.

Static RAMs are constructed on the principle of using an integrated flip-flop or bistable circuit to store each binary digit, 1 or 0. They are faster than dynamic RAMs but dissipate power continuously to hold the information, have a lower packing density and are usually more expensive.

Dynamic RAMs are constructed on the principle of using a MOS capacitor, in conjunction with a MOS field-effect transistor, to store each 1 or 0 binary digit as an electric charge. Consequently, to hold information the charge in the capacitor has to be constantly maintained, or 'refreshed', by other circuitry. Dynamic RAMs use power only when reading and writing is taking place and their standby power dissipation is very low.

UK FACTORY SITE

Back in the UK the government eventually decided that the factory for volume production should be built in South Wales, and in January 1981 the construction of a plant of spectacularly advanced architectural design was initiated at Cardiff Road, Duffryn, Newport, Gwent. This was conveniently just a few miles over the Severn Bridge from the Inmos administration and R&D centre in Bristol, at Whitefriars, Lewins Mead. The Newport factory started operations in June 1982 and by November of that year was producing in volume the first 16K static RAMs, initially manufactured at Colorado Springs. And in February 1983 the Newport factory started volume production of the dynamic RAMs.

Altogether these three Inmos establishments now employ an average of 1350 people. There are 750 at Inmos Corporation, Colorado Springs; 500 at Inmos Limited, Newport; and 100 at Bristol. The R&D people at Bristol work on microcomputers and computer aided design, while those at Colorado Springs are concerned with memory products and process technology.

INMOS TODAY

What, then, is the position of Inmos now, in terms of its products, markets, technical developments, commercial viability and plans for the future?
First, the products. At the time of writing the i.c.s in production and on the market are all semiconductor memories. Categorized purely in terms of storage capacity and/or chip organization there are seven basic products, but these have variants with different specifications, packaging etc. that make a total of 32 type numbers.

The range of 16K static RAMs contains the 16K x 1 type IMS1400 in versions with access times down to 35ns; the 4K x 4 type IMS1420; and the slightly different 4K x 4 IMS1421, both in versions with access times down to 45ns.

All these are available in plastic or ceramic d.i.p. or in chip carrier packaging. In addition there are military specification versions, the IMS1400M and 1420M, both available in d.i.p. or chip carrier form. Inmos claim that the 16K IMS1400 and 1420 are "the fastest static RAMs available for use in military and computer applications."

The company also make a range of 64K dynamic RAMs. The 64K x 1 type IMS2600 comes in versions with access times down to 100ns and is available in either d.i.p. or chip carrier packaging. IMS2620 has a 16K x 4 organization and is also in versions with access times down to 100ns, while the IMS2630 is an 8K x 8 memory in versions with access times down to 120ns—these two devices both being packaged in d.i.p. form. Recently Inmos and the Intel Corporation have agreed a common specification for future dynamic RAMs made by a new high speed CMOS process, so that users will have two sources of functionally identical products.

Finally, to complete the seven basic products, the latest to be marketed is a 64K electrically erasable programmable read-only memory (EEPROM) in a d.i.p. package, the IMS3430. Made by a process called Nitrox which produces memory cells of very small area, this device has an 8K x 8 organization and requires only a single 5V supply. The whole ROM can be programmed in 1-3s.

In the dynamic RAMs, two particular features contributing to good performance and convenience in use are what are called the 'nibble' mode of operation and the 'CAS before RAS' method of refresh assistance. The term 'nibble' means simply half a byte (a metaphor built on a pun!), or four bits. It describes a facility in the 64K dynamic RAM which allows four data bits to be read or written sequentially for a single address access. It is a design response to the electronic industry's demand for faster and faster memory operation and is provided by other manufacturers under the name 'serial access'. In the IMS2600, for instance, the nibble mode allows serial access to two, three or four bits at a bit rate of 25MHz.

All dynamic RAMs need refresh assistance, but the techniques used by some manufacturers have the effect of restricting memory expansion and increasing the standby power dissipation. The Inmos method of refresh assistance avoids these problems. To determine whether a normal access or a refresh cycle should be performed the chip samples the high/low state of the column address strobe (CAS) as the row address strobe (RAS) falls to the low state. If CAS is low as RAS goes low, the memory ignores any address inputs and substitutes the contents of an on-chip 8-bit counter to determine the row to be refreshed.

MANUFACTURING PROCESSES

All these memory devices are manufactured by advanced VLSI processes, in which Inmos invested very heavily in order to remain competitive. This technology has three main characteristics. First, the etching of the different layers of material on a chip is done by the plasma, or dry, method, to achieve greater dimensional stability than is possible by the use of acids.

Secondly, ion implantation is used to give a more controllable depth of impurity atoms in the crystal lattice below the semiconductor surface than is possible with the conventional diffusion method. Depth of penetration is controlled by the energy imparted by acceleration to the ions bombarding the silicon surface. Thirdly, the Inmos process technology uses wafer stepping photolithography, in which the circuit patterns are projected onto the semiconductor wafer one chip at a time. This gives better line definition and alignment accuracy, and hence higher yields, than when a pattern is projected onto the whole wafer in one operation.

Another technique which improves the yield of memory chips is to introduce redundancy, in the form of spare rows and columns of cells in the memory matrix. At the wafer testing stage any failed cells are identified and this information is programmed into the chips in such a way that when these cells are addressed the device brings in the spare good cells to replace them.

MARKETS

The principal markets of Inmos memories are in the USA and these take over 70% of the company's output. The remainder are distributed throughout the rest of the world. Inmos claims to have secured "a major share" of the world market for 16K fast static RAMs, which are going mainly to the USA, Europe and Japan. In general the firm's memory products are used in main-frame and mini computers, peripheral buffers, radar systems, aircraft flight computers, video displays and telecommunications digital switching equipment.
RECENT TECHNICAL DEVELOPMENTS

In the past few years technical developments from Inmos have included the OCCAM programming language for single and multiple microcomputer applications and a set of computer based aids for designing VLSI devices. In semiconductor products probably the most advanced development is the Transputer (see January issue editorial, p.13). This name, derived from 'transistor' and 'computer', actually refers to a family of products. The first of these, due on the market soon as the IMS T424, is a 32-bit microcomputer on a single chip capable of handling 10 million instructions per second. An article by Ray Coles will explain the device in more detail next month.

The most significant thing about this device is that, as well as being suitable for conventional applications, it is designed to allow operation in arrays of similar microcomputers all working in co-ordination with each other—"concurrent processing" as Inmos calls it. For this purpose the single VLSI chip includes circuits allowing it to communicate with other such microcomputers—four 15Mbyte/s two-way serial data links. This principle of array processing is very much aimed at the future "fifth generation" computer systems, which will probably work at about a thousand times the performance level of present computers to provide intelligent interaction between people and machines. The CMOS silicon chip of the IMS T424 contains 250,000 active devices, includes 4Kbyte of RAM and is packaged in an 84-contact ceramic chip carrier.

HOW THE MONEY WAS USED

From the beginning the Inmos management realized that the original funding of £50M would not be enough to sustain the corporate plan aimed at profitability. In the intervening years the effects of inflation and the falling value of the pound sterling relative to the US dollar have made the deficiency even worse. A market and technical assessment by independent consultants—"concurrent processing" as Inmos calls it. For this purpose the single VLSI chip includes circuits allowing it to communicate with other such microcomputers—four 15Mbyte/s two-way serial data links. This principle of array processing is very much aimed at the future "fifth generation" computer systems, which will probably work at about a thousand times the performance level of present computers to provide intelligent interaction between people and machines. The CMOS silicon chip of the IMS T424 contains 250,000 active devices, includes 4Kbyte of RAM and is packaged in an 84-contact ceramic chip carrier.

Total funding to about £100M to date.

How has all this money been used? The ultimate purpose of the investment, of course, is to create a profitable company financing itself out of its own trading activity. The NEB, having performed its function of launching the enterprise, would then be able to sell off its shareholding in a going concern to good advantage, at the least recovering the investment of public money and at the best obtaining some return for it.

The 1982 annual report is the latest account showing how far Inmos has progressed along this road. First of all, its use of the capital investment. The company now has tangible fixed assets of £44.1M, in the form of various buildings and their equipment. This sum is made up of £20.2M in freehold land and buildings, £168,000 in short-leasehold land and buildings and £23.7M in plant and equipment. There are also current assets, in the form of stocks, cash and debts, and after the current liabilities have been deducted this leaves the company with total assets of £47.2M.

Now to the current trading position. In 1982 sales of MOS memory products amounted to £13.7M. This was a very big increase from the corresponding 1981 sales figure of £2.1M. However, the operating costs relating to these 1982 sales—manufacturing, engineering, product support, distribution and administration—totalled £22.3M, resulting in an operating loss of £8.6M. Apart from this, starting up the Newport factory cost £3.6M, the continuing research and development work required £4.5M, the interest charges on loans were £1.2M, while losses on the dollar-pound exchange rate came to £2.3M.

Altogether the profit and loss account for 1982 showed a loss of £20.3M. Losses brought forward from previous years amounted to £21.6M, so the accumulated loss carried forward from 1982 was £42M.

PROFIT IN 84?

Obviously Inmos still has a long way to go. In the 1982 report the directors said that they expected the 1983 results to show "a move towards profitability", while the chairman, Malcolm Wilcox, said that if all went well "the scene will be set for a move into profit in 1984." The 1983 annual report, soon to be published, will show to what extent these optimistic comments are justified. They seem to suggest that by the end of 1983 Inmos would at least have broken even on its monthly revenues. At the turn of the year company officials were saying no more, but seemed to be quietly confident that the 1983 results would show a more than doubled turnover.

"What does the future hold for Inmos? To begin with, a company spokesman told PE that there is "no immediate danger of going bust." The firm now has enough money to keep going. But it still has to keep up with the relentless march of technical innovation to remain among the leaders in the field of manufacture, and also has to contend with equally relentless commercial competition in world markets. This means, for example, that "significant sums" will be needed to build new wafer processing facilities.

For such future investment Inmos is now looking towards private sources of finance, and the 1982 annual report stated that "discussions in this regard are now on course." One result could be that other companies or financial institutions will be buying significant minority shareholdings in the firm.

If this does indeed happen and the process continues, with the NEB gradually divesting itself of its majority shareholding as intended, Inmos will eventually end up as a public company with share prices quoted on the Stock Exchange. This transformation, from ownership by the state to a variegated ownership by pension funds, insurance companies, institutions, trade unions and even private individuals, is a process that could well be starting some time this year.
So far in the series we have only dealt with logic gates having two inputs. The time has now come to extend our knowledge to include gates having three, or more, inputs. The two-input gates which we have previously considered are: AND, OR, NAND and NOR. We shall now consider their three-input counterparts.

A three-input logic gate has inputs which we shall, for convenience, label A, B and C. Again there is no particular significance in the choice of letters other than that they are simply the first three letters of the alphabet. To be consistent with the two-input gates previously considered, we shall again refer to the outputs as X. The Boolean expression for each of the three-input gates will, of course, involve the three variables A, B and C. Taking the three-input AND gate first, we find that its output is \( A \text{ AND } B \text{ AND } C \). Putting this in correct Boolean form gives:

\[
X = A \cdot B \cdot C
\]

In terms of the logical state of the inputs, the output \( X \) will be a 1 whenever \( A, B \) and \( C \) are all 1. Any other combination of inputs (e.g. \( A = 0, B = 0, C = 1 \)) will produce a 0 output. Since we are dealing with a three-input gate, there are \( 2^3 = 8 \) possible combinations of the logical input states. The truth table will, therefore, consist of eight lines covering the input states arranged in four columns, three for the inputs and one for the output, as shown in Table 6.1.

The output of a three-input OR gate is \( A \text{ OR } B \text{ OR } C \). In correct Boolean form this is:

\[
X = A + B + C
\]

This is an important result which we shall be returning to in Part Seven when we introduce De Morgan's Theorem.

The truth table for a three-input OR gate is shown in Table 6.2. As in the case of their counterparts, three-input inverting gates, NAND and NOR, produce the complement of their respective AND and OR counterparts. The output of a three-input NAND is NOT (A AND B AND C), or:

\[
X = \overline{A \cdot B \cdot C}
\]

The truth table for a three-input NAND gate as that used for the three-input AND except that the output column will contain 1's in each line except for that which corresponds to the input state: \( A = 0, B = 0, C = 0 \). This, incidentally, yields the important result that the output of a three-input OR gate is the logical opposite (complement) of the output of a gate for which the Boolean expression is \((\overline{A}) \text{ AND } (\overline{B}) \text{ AND } (\overline{C})\). Thus we conclude that:

\[
A + B + C = \overline{A \cdot B \cdot C}
\]

This is an important result which we shall be returning to in Part Seven when we introduce De Morgan's Theorem.

The truth tables for the three-input NAND and NOR gates are respectively shown in Tables 6.3 and 6.4. Unfortunately, these two are easily confused and the recommended method for distinguishing between them is to FIRST consider the output of the corresponding non-inverting gate (i.e. AND or OR) and simply complement its output state (i.e. whenever a 1 appears in the output column change it for 0, and vice-versa).
FOUR (AND MORE!) INPUT GATES

Having dealt with three-input gates it is worth considering what happens when we are presented with gates with four, and more, inputs. The procedure for deriving the Boolean expressions and truth tables naturally follows that adopted for the three-input gates. The Boolean expression for a gate with n different inputs will have \(2^n\) lines. The truth table will have n columns for the inputs and just one column for the output. Hence the Boolean expression for the output of a four-input gate \((n = 4)\) will involve four variables \((A, B, C\) and \(D)\) and its truth table will have \(2^4\) (= 16) lines.

The Boolean expressions of the outputs of four-input gates are shown below. The symbols for these Gates are, together with those for their three-input counterparts, shown in Fig. 6.1.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A 0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>B 0 0 1 0</td>
<td></td>
</tr>
<tr>
<td>C 0 1 0 0</td>
<td></td>
</tr>
<tr>
<td>D 0 1 1 0</td>
<td></td>
</tr>
<tr>
<td>E 1 0 0 0</td>
<td></td>
</tr>
<tr>
<td>F 1 1 0 0</td>
<td></td>
</tr>
<tr>
<td>G 1 1 1 0</td>
<td></td>
</tr>
</tbody>
</table>

**Table 6.4. Truth table for a three-input NOR gate**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A 0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>B 0 0 1 0</td>
<td></td>
</tr>
<tr>
<td>C 0 1 0 0</td>
<td></td>
</tr>
<tr>
<td>D 0 1 1 0</td>
<td></td>
</tr>
<tr>
<td>E 1 0 0 0</td>
<td></td>
</tr>
<tr>
<td>F 1 1 0 0</td>
<td></td>
</tr>
<tr>
<td>G 1 1 1 0</td>
<td></td>
</tr>
</tbody>
</table>

**Table 6.5. Truth table for the direct inputs of a J-K bistable**

<table>
<thead>
<tr>
<th>J K</th>
<th>Q</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>0</td>
<td>NO CHANGE</td>
</tr>
<tr>
<td>0 1</td>
<td>1</td>
<td>OUTPUT PRECleared</td>
</tr>
<tr>
<td>1 0</td>
<td>0</td>
<td>OUTPUT PRESet</td>
</tr>
<tr>
<td>1 1</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

**Table 6.6. Truth table for the clocked inputs of a J-K bistable**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>A 0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>B 0 0 1 0</td>
<td></td>
</tr>
<tr>
<td>C 0 1 0 0</td>
<td></td>
</tr>
<tr>
<td>D 0 1 1 0</td>
<td></td>
</tr>
<tr>
<td>E 1 0 0 0</td>
<td></td>
</tr>
<tr>
<td>F 1 1 0 0</td>
<td></td>
</tr>
<tr>
<td>G 1 1 1 0</td>
<td></td>
</tr>
</tbody>
</table>

**Fig. 6.1. Symbols used for three- and four-input logic gates. Note: BS symbols follow the style of Fig. 6.2.**

**Fig. 6.2. Symbol for a J-K bistable**


J-K BISTABLES

Unlike the two types of bistable which we have met previously in Part Five, the J-K bistable provides direct as well as clocked inputs. The direct inputs, usually labelled ‘preset’ and ‘preclear’, are normally used to initialise the state of the bistable before data is clocked into it by means of the J and K inputs. There is, incidentally, no particular significance in the letters J and K other than that they are consecutive letters in the alphabet and are unlikely to be confused with other letters used thus far to identify inputs and outputs.

The symbol for a J-K bistable is shown in Fig. 6.2. Note that there are five inputs: preset and preclear (the two direct inputs), J and K (the two clocked inputs), clock, and two outputs: Q and \(\overline{Q}\). As with the previous forms of bistable, the two outputs are complementary (i.e. when \(Q = 1\), \(\overline{Q} = 0\), and vice versa). It should also be noted that, in the case of practical J-K bistables like the 7473 that we shall be considering separately the four possible conditions which can arise for both the direct and clocked inputs, referring initially to Table 6.5:

1. If both preset and preclear inputs are taken to logic 0 an indeterminate state exists and the outputs, Q and \(\overline{Q}\), may no longer be complementary. This condition must be avoided.

2. If the preset input is taken to logic 1 and the preclear input is taken to logic 0, the state of the Q output immediately becomes logic 0 whilst the Q output becomes logic 1; i.e. the bistable is precleared.

3. If the preset input is taken to logic 0 and the preclear input is taken to logic 1, the Q output immediately becomes logic 1 whilst the Q output immediately becomes logic 0; i.e. the bistable is preset.

4. If both preset and preclear inputs are taken to logic 1 the bistable is ready for clocked operation and the following rules are obeyed (as in Table 6.6):
(a) If both J and K inputs are taken to logic 0 the Q and Q̅ outputs do not change state on a falling clock transition. Thus Q_{n+1} is the same as Q_n and Q̅_{n+1} is the same as Q̅_n.

(b) If the J input is at logic 0 and the K input is at logic 1 the Q output stays, or becomes, 1 when the next falling clock transition occurs. The Q output takes the opposite logical state.

(c) If the J input is at logic 1 and the K input is at logic 0, the Q output stays, or becomes, 1 when the next falling clock transition occurs. The Q̅ output takes the opposite logical state.

(d) If both the J and K inputs are taken to logic 1 the Q and Q̅ outputs change state when the next falling clock transition occurs. Thus Q_{n+1} is the same as Q_n and conversely Q̅_{n+1} is the same as Q̅_n.

In case (a) the bistable ignores the clock transition whilst in cases (b) and (c) the complementary states of the J and K inputs are effectively passed, on the falling clock edge, to the Q and Q̅ outputs respectively. In case (d) the bistable is configured for operation as a binary divider. If this still appears to be a little difficult to understand the following practical investigation should help to make things clear!

THE 7473 J–K BISTABLE

The 7473 contains two independent J–K bistables, as shown in Fig. 6.3. The 74107 is electrically identical to the 7473 but has more conventional supply connections (TTL devices usually have pins 14 and 7 as the +5V and OV connections respectively). The two internal bistable stages are themselves identical and each has the usual J, K and clock inputs. A preset input is, however, not provided and only a preclear input is available for the direct control of the bistable. The preclear is, incidentally, an 'active low' input as mentioned previously. To all intents and purposes, the bistable operates as if the missing preset input were internally connected to logic 1. Thus, for normal clocked operation, it is only necessary to connect the preclear input to logic 1. In actual fact the preclear input 'floats' to logic 1 if left unconnected. However, since leaving inputs unconnected is not generally considered good practice, it is recommended that a physical link to logic 1 be made external to the i.c. There can then be absolutely no doubt about the logical condition present on the preclear input! It should also be noted that the state of the J and K inputs should not be changed once only during each clock cycle. Ideally this change should be made immediately after the clock transition. Any subsequent changes in the logical state of the J and K inputs can cause invalid states within the bistable.

Insert the 7473 into the dual-in-line socket marked 'A' on the Logic Tutor. The chip should be orientated so that the clock becomes 0 when the data is transferred from the master to the slave. The final Q output of the complete arrangement is thus logic 1. The operation of the preclear input is similar. In this case, however, the resulting final Q output is a 0. When both preset and preclear are taken to logic 1 an attempt is made to set and reset both bistables at the same time. It is thus impossible to predict what will happen and the final output is indeterminate. When both preset and preclear are taken to logic 1 the two OR gates are ready to pass data from the three-input AND gates to the set and reset inputs of the master bistable. Note that the final Q and Q̅ outputs are fed back to the three-input AND gates and thus they must generate complementary logic states by virtue of the opposite state of the Q and Q̅ outputs. The master is thus set or reset depending upon the state of the J and K inputs whenever the clock is at logic 1. When the clock changes to logic 0, data is transferred from the master to the slave by means of the two-input AND gates.

**MASTER-SLAVE BISTABLES**

At this point readers may be wondering what the internal logic of a J–K bistable looks like. It is, in fact, an elegant and ingenious arrangement known as a 'master-slave'. Both the master and the slave are simply conventional R–S bistables, the trick comes in the arrangement of the logic gates which interconnect them.

The basic arrangement of a J–K master-slave bistable is shown in Fig. 6.4. Let us assume that, initially, J, K and clock are all at logic 0. If preset is taken to logic 1 whilst preclear remains at logic 0 then the master bistable is set and its Q output becomes logic 1. Since the clock is at logic 0, the inverted clock will be a 1. This, together with the Q output from the master bistable, is fed to a two-input AND gate which generates a logic 1 to set the slave bistable. The final Q output of the complete arrangement is thus logic 1. The operation of the preclear input is similar. In this case, however, the resulting final Q output is a 0. When both preset and preclear are taken to logic 1 an attempt is made to set and reset both bistables at the same time. It is thus impossible to predict what will happen and the final output is indeterminate. When both preset and preclear are taken to logic 1 the two OR gates are ready to pass data from the three-input AND gates to the set and reset inputs of the master bistable. Note that the final Q and Q̅ outputs are fed back to the three-input AND gates and thus they must generate complementary logic states by virtue of the opposite state of the Q and Q̅ outputs. The master is thus set or reset depending upon the state of the J and K inputs whenever the clock is at logic 1. When the clock changes to logic 0, data is transferred from the master to the slave by means of the two-input AND gates.
in practice J-K bistables may also be of the edge-triggered variety. Unlike the master-slave type, where data is fed into the bistable during the logic 1 part of the clock cycle and appears at the output when the clock goes to logic 0, the edge-triggered bistable transfers data from input to output on the same edge of the clock cycle. This is achieved by means of an internal pulse narrowing circuit which converts the clock to a narrow 'spike' shorter in duration than the delay which occurs in the bistable changing its state. The truth table is, however, identical for both types.

CLOCKS AND OSCILLATORS

Clocks are vital to the correct timing of operations in digital logic circuits. The basic requirement of a clock is that it provides a repetitive pulse waveform of accurate period. The most basic form of clock is merely a TTL compatible oscillator which produces a square wave output of 5V pk-pk at a known frequency. More complex clocks, such as those which are used for 'real time' applications, may be required to operate with a frequency stability and accuracy of better than ten parts per million. Oscillators may also be required for purposes other than purely timing. These applications include the testing of logic systems, the generation of alarm and warning signals, and the transmission of data in serial form. Before examining the subject in greater detail it is worth defining some of the relevant terms in popular use.

FREQUENCY: The frequency of an oscillator is the number of cycles of its output which occur in a second. An oscillator which, for example, generates 50 pulses per second has a frequency of 50Hz. Similarly, an oscillator which provides an output of 1kHz is producing 1000 pulses per second.

PERIOD: The period of an oscillator is the time for one complete cycle of its output. Naturally, the higher the frequency the smaller the period will be. In the previous examples the periods are 1/50 second (or 20ms) and 1/1000 second (or 1ms), respectively. The period of a waveform (in seconds) is thus simply the reciprocal of its frequency (in Hz).

MARK TO SPACE RATIO: The mark to space ratio of a pulse waveform is the ratio of 'on' (logic 1) to 'off' (logic 0) time. For a perfect square wave the 'on' and 'off' times will be the same, hence it is said to exhibit a 1:1 mark to space ratio.

DUTY CYCLE: The duty cycle of a pulse waveform is the ratio of the 'on' to ('on plus 'off') times, normally expressed as a percentage. A perfect square wave would thus exhibit a 50% duty cycle.

OSCILLATOR USING SCHMITT INVERTERS

A very simple TTL oscillator configured around two gates of a hex inverter is shown in Fig. 6.5. This arrangement uses a 7414 device rather than the more familiar pin-compatible 7404. The 7414 is much to be preferred for this particular application by virtue of its internal Schmitt action which offers an amount of hysteresis in the voltage levels for the logic 0 and 1 thresholds. The 7404 will not operate reliably in this circuit.

The first of the two gates has two external components: a resistor which provides positive feedback from the output to the input, and a timing capacitor connected from the input to 0V. The second gate merely acts as an inverting buffer to provide a measure of isolation of the first gate from the load connected to the output.

In order to explain the operation of the oscillator we must consider what happens when power is first applied to the circuit (A in the waveform diagram of Fig. 6.7). Furthermore, we shall only be concerned with the first of the two logic gates since the second stage merely acts as an inverter and takes no part in the oscillatory action. The capacitor C will be initially uncharged and thus the voltage across it will be zero. The input to the first logic gate will then be logic 0 whilst its output will be logic 1.

Table 6.7. Values of C and corresponding output frequency for the circuit in Fig. 6.5

<table>
<thead>
<tr>
<th>C</th>
<th>f out</th>
</tr>
</thead>
<tbody>
<tr>
<td>470μ</td>
<td>1.5Hz</td>
</tr>
<tr>
<td>67μ</td>
<td>15Hz</td>
</tr>
<tr>
<td>45μ</td>
<td>150Hz</td>
</tr>
<tr>
<td>470n</td>
<td>15kHz</td>
</tr>
<tr>
<td>67n</td>
<td>15kHz</td>
</tr>
<tr>
<td>47n</td>
<td>15kHz</td>
</tr>
<tr>
<td>470p</td>
<td>1.3MHz</td>
</tr>
<tr>
<td>47p</td>
<td>8MHz</td>
</tr>
</tbody>
</table>
the oscillator to be exceptionally stable in output frequency and, where precise timing is important, accurately maintained at a particular frequency. Furthermore, in many applications the clock is required to operate at a high frequency, often in excess of 1 or 2MHz. In such applications a quartz crystal may be employed to act as the frequency determining element, as shown in Fig. 6.8. This circuit is somewhat similar to that shown previously with the addition of a crystal and extra capacitor. The circuit can be considered as a free-running oscillator, like those previously described, which is locked to the crystal frequency. The value of C1 in particular has to be chosen so that the stage will operate, or near, the desired output frequency with the crystal disconnected. Values for C1 of 47pF and 220pF are appropriate to the frequency ranges 8 to 15MHz and 2 to 8MHz respectively. A clock frequency of greater than 2MHz may appear to be somewhat high at first sight. It is, however, a relatively simple matter to divide the oscillator output frequency by a fixed amount (e.g. 10, 100, 16, 64 etc.) as we shall see in Part Seven.

Even when the circuit is correctly operating in the crystal locked condition there may still be a very slight error between the actual frequency produced and that desired (or that marked on the crystal). In such a case a small amount of capacitance may be connected in parallel with the crystal to trim the frequency precisely. This capacitance should not normally exceed a value of 68pF. A practical solution would be to connect a 50pF trimmer directly across the crystal terminals and adjusting this component using a digital frequency meter connected to the clock output.

CRISTAL OSCILLATORS
Many applications for clocks require

VARIABLE FREQUENCY OSCILLATORS
Occasionally one requires a variable frequency oscillator capable of adjustment over a wide range. Whilst such a signal can, of course, be readily derived from a conventional laboratory signal generator, there is a very simple and effective circuit arrangement based on the 74S124 which provides this function using only two external components.

The circuit of a variable frequency clock using a 74S124 is shown in Fig. 6.9. This produces a reasonable 50% duty cycle square wave output and is capable of reliable operation extending from below 1Hz to beyond 20MHz. The frequency is continuously variable by means of the control potentiometer, which provides an adjustment range of approximately 4:1. Typical values of capacitator together with maximum and minimum operating frequencies are shown in Table 6.9.

TWO-PHASE CLOCKS
In microprocessor systems, and sophisticated logic systems generally, there is often a need for a clock which produces complementary outputs. Such a clock is known as a two-phase (or bi-phase) clock, the typical output waveform of which is shown in Fig. 6.10. Fortunately, complementary outputs are easy to obtain from a bistable
element and thus a two-phase clock may simply consist of an oscillator followed by a bistable. There is, however, one minor complication: the bistable effectively operates as a binary divider and hence the oscillator must be set to operate at twice the desired clock frequency.

**TWO-PHASE CLOCK USING THE 7414 AND 7473**

A two-phase clock which illustrates some of the principles discussed earlier, is shown in Fig. 6.11. Here the oscillator uses a 7414 hex Schmitt inverter which produces an output at about 2Hz with a mark:space ratio of approximately 3:1. The oscillator output is fed to the clock input of a 7473 J–K bistable. The timing diagram for the circuit is shown in Fig. 6.12. It should be noted that the output frequency is a symmetrical square wave having a frequency which is exactly half that of the oscillator. This arrangement can be tested by inserting 7414 and 7473 devices in sockets A and B respectively of the Logic Tutor and then making the following connections:

- **Output** to 7414 (A1)
- **Output** to 7473 (pin 14)
- **Pin 14 to Logic 1**
- **Pin 13 to Logic 1**
- **Pin 12 to Logic 1**
- **Pin 11 to Logic 1**
- **Pin 10 to Logic 1**
- **Pin 9 to Logic 1**
- **Pin 8 to Logic 1**
- **Pin 7 to Logic 1**
- **Pin 6 to Logic 1**
- **Pin 5 to Logic 1**
- **Pin 4 to Logic 1**
- **Pin 3 to Logic 1**
- **Pin 2 to Logic 1**
- **Pin 1 to Logic 1**

The state of D1, D2 and D3 are used to indicate the oscillator, clock, and clock outputs respectively. D1 should be seen to flash at approximately 2Hz whilst D2 and D3 flash at exactly half this rate and will always have opposite states. The speed of operation may be varied by making suitable changes to the value of R. The value of C should, however, not be changed since 1kΩ is optimum for this circuit. Increasing the value much above 1kΩ will render the circuit inoperative (the logic 0 input state is no longer properly maintained) whilst reducing it much below 1kΩ means that an impractically large value of capacitor has to be used in order to obtain a particular clock rate. Values of C, together with approximate output frequencies produced, with R = 1kΩ are shown in Table 6.9.

**MONOSTABLES**

The R–S, D, and J–K bistables which we have met so far all possess two stable states. Once put in one or other of the states they will remain in that state until something happens to produce a change of state. There are, however, a number of applications in which a momentary pulse of fixed duration is required. A device which fulfills this function has only one stable state and is known as a monostable.

The action of a monostable is quite simple: its output is initially logic 0 until a level change or edge arrives at its trigger input. This level change can be from 0 to 1 (positive edge trigger) or 1 to 0 (negative edge trigger). Immediately the trigger is received, the output of the monostable changes state to logic 1. Then, after a time interval determined by external components, the output reverts to logic 0. The monostable then awaits the arrival of the next trigger.

Monostables are available in a variety of forms and, whereas it is possible to make a simple form of monostable from individual logic gates, the use of a purpose designed integrated circuit monostable is much to be preferred. To understand the basic principles of monostable pulse generators we will, however, first consider some simple yet effective monostables which employ familiar logic gates.

**SIMPLE MONOSTABLES USING INVERTERS**

The simplest method of generating a monostable pulse involves the use of an inverting gate together with an external capacitance–resistance (C–R) network. The arrangement of Fig. 6.13 shows how a negative output pulse (1 \(\rightarrow\) 0 \(\rightarrow\) 1) can be generated by a positive edge trigger. If we need to
produce a positive output pulse (0 → 1) then we only need to add a second inverting stage, as shown in Fig. 6.14. In order to explain how the circuit operates we need to consider what happens when the trigger arrives. Initially, capacitor C is uncharged since the voltage level at the input is zero before the trigger pulse arrives. When the trigger does arrive, the input voltage rapidly rises from OV to approximately 5V. This is conveyed, via the capacitor, to the input of the inverting gate. The inverter recognises a logic 1 input whenever the voltage at its input exceeds approximately 1.5V thus its output changes state, from 1 to 0 when the input voltage passes through 1.5V. The capacitor then charges through the resistor, R, and the voltage at the input of the gate then falls exponentially back towards OV. When the input voltage falls below approximately 1.5V, the gate recognises a logic 0 input and its output state reverts to logic 1. Waveforms for this circuit arrangement are shown in Fig. 6.15. The time taken for the capacitor to charge depends upon the time constant of the circuit (C x R). Thus the duration of the monostable output pulse can be varied simply by changing the values present.

The positive edge triggered monostable follows the arrangement shown in Fig. 6.14 and is constructed using the following links on the Logic Tutor:

A1 to S1 via 100µF capacitor (+ve to S1)
A1 to 0V via 470Ω resistor
A2 to A3
A4 to D1 (D1 indicates the output)
A7 to 0V (0V)
A16 to +5V (positive supply)

The 7404 should be inserted into socket A, taking care to orientate the package so that pin 1 aligns with A1. In the absence of any input from S1, D1 should remain extinguished. Immediately S1 is depressed, however, a positive edge is generated and D1 should flash momentarily (i.e. approx. 0.2 second) and then become extinguished again. If S1 is pressed and held down, only one flash will be generated. If S1 is pressed and then released repeatedly D1 will flash once for each positive edge generated.

The negative edge triggered monostable follows the arrangement shown in Fig. 6.16 and uses the following links on the Logic Tutor:

A1 to S1 via 100µF capacitor (−ve to S1)
A1 to 0V via 1kΩ resistor
A1 to +5V via 1kΩ resistor
A2 to D1 (D1 indicates the output)
A7 to 0V (0V)
A16 to +5V (positive supply)

The 7404 should again be inserted into socket A. In the absence of any input from S1, D1 should again remain extinguished. When S1 is depressed nothing should happen and D1 should remain extinguished since the circuit is designed to ignore a positive edge transition. Releasing S1, which produces a negative edge, should cause D1 to flash momentarily and then become extinguished again. If S1 is pressed and released repeatedly D1 should flash once for each negative edge generated.

NEXT MONTH: We continue by looking at the 74121 monostable, pulse stretching techniques, a variable width pulse generator, De Morgan’s Theorem, Karnaugh Maps and an intruder alarm for our electronic shop.
COPYING M/C

Sir—when copying machine code tapes for the UK101 to make back-up copies or for a high speed cassette interface, there can be problems due to some programs overwriting e.g. page zero memory. Also in order to exit machine code games etc. it is very often necessary to press reset, and this may foul up the program making it pointless to attempt to save it.

A way round this problem is to use the NMI (non-maskable interrupt). By connecting a push-to-make switch from ground to either pin 6 of the 6502 or pin 2 of J1 you can jump to any memory location via the NMI vector at HEX 0130. With Cegmon the ideal place to jump to is FEOC, the machine code monitor warm start. To do this enter the monitor by reset M and enter 0130 4C,OC,FE (0130 JMP FEOC).

Before the program can be SAVED you need to know the start, end and entry points (RAM addresses) of the code. To make it easy to find the end address it is advisable to fill all RAM with the same number so that when loading the program it will only overwrite the RAM it occupies. For example the original BASIC 4 chip will, when cold-starting, fill all user RAM with HEX 24, and by finding the last "24" overwritten you can find the end address of the code to be saved.

The start and entry (or "Go") addresses can usually be found by watching the screen when loading. When loading with Cegmon the start address appears first, followed by Hex pairs of digits and then the "Go" address. It is possible that the first address may be that of a checksum or other loader so this method may not work in every case. A better way is to use Exmon but you may need a relocated version that doesn’t clash with the program for memory space.

To summarise, cold start (if RAM test doesn’t fill RAM) then fill all RAM with a FOR-NEXT loop e.g. FOR J = 768 TO 16348: POKE J,36 : NEXT), then enter the machine code monitor and enter 0130 4C,OC,FE. Now LOAD the program to be SAVED and note down the start address and entry address when they appear on the screen—but you’ll have to be ready as they will disappear almost immediately. The program or game will start but press the NMI switch and the computer will jump to the monitor warm start. Cegmon’s tabulate command will assist in finding the last RAM location before all the “24s”—you can now tell the end address. Finally SAVE by typing S,START,END ENTRY e.g. S 0240,OFFF 0800.

Here are some useful routines:

To jump out of BASIC and load M.C.: POKE 251,1 : 80OE F988 or POKE 251,1 : CALL —1655

To jump out of M.C. and run BASIC: JSR £A477

If saving non-continuous blocks of RAM then the "Go" address is £FA2E e.g. S 0235,02FF FA2E then S 1C00,1CFF then the “Go” address is £FA2E e.g. S 0240,OFFF 0800.

To summarise, cold start (if RAM test doesn’t fill RAM) then fill all RAM with the same number so that when loading the program it will only overwrite the RAM it occupies. For example the original BASIC 4 chip will, when cold-starting, fill all user RAM with HEX 24, and by finding the last "24" overwritten you can find the end address of the code to be saved.

Dave Henniker, Edinburgh.

UK101 REM REMOVER

Sir—I have a UK101 with 48K of RAM and the original monitor.

The following program may be of interest to your readers. It is a "REM remover" for UK101. As the program is fairly long (303 bytes) it is shown as a memory dump. The program occupies locations 1E80 to 1FAF. Memory will need restricting if the program is to be resident while BASIC programs are running.

To use the program, have the code resident and load a BASIC program with lots of REMs. It is worthwhile doing a ?REM(1) at this point. Press reset, M, 1E80 and G. The program returns to BASIC when it has finished. All REMs should have been removed. Do a ?REM(1) to see how much space has been recovered.

S. Jaworski, Walsall.

1E80 A9 01 85 38 09 03 85 31
1E88 A9 00 85 38 A0 00 EA B1
1E90 30 D0 2E C8 B1 30 D0 29
1E98 A5 38 F0 22 A9 00 A8 91
1EA6 38 C8 91 36 38 A5 30 E5
1EAE 36 85 36 A3 31 E5 37 85
1EB6 37 38 A5 7B E5 36 85 7B
1EB8 A5 7C E5 37 85 7C 4C 74
1EC6 A2 A0 00 EA B1 30 85 32
1EC8 C8 B1 30 85 33 A0 04 EA
1ED6 B1 30 C9 8E D0 1B A5 38
1ED8 D0 A5 8C A5 30 85 36 A5 31
1EE8 85 37 A9 B1 85 38 A5 32
1EEA 85 30 A5 33 85 31 4C 8C
1EF6 1E A5 38 D0 2D A9 05 EA
1EFA B1 30 F0 EA C9 8E F0 04
1F00 C4 4C F8 1E 1E 98 1B 65 30
1F08 85 36 A9 00 65 31 85 37
1F16 A9 00 88 91 30 A8 A5 36
1F1B 91 30 C8 A5 37 91 30 4C
1F20 E2 1E 38 A5 30 E5 36 85
1F28 2C A5 31 E5 37 85 2D 38
1F30 A5 7B E5 2C 85 7B A5 7C
1F38 E5 2D 85 7C A5 36 85 2E
1F40 A5 37 85 2F A5 30 85 34
1F48 A5 31 85 35 A0 00 EA 38
1F50 B1 30 85 32 E5 2C 91 30
1F58 C8 B1 30 85 33 E5 2D 91
1F66 30 88 A5 33 F0 0B A5 32
1F68 85 30 A5 33 85 31 4C 4C
1F70 1F A5 32 D0 F1 A9 00 91
1F76 30 C8 91 30 88 A8 00 EA
1F80 B1 34 91 36 E6 36 4E 34
1F88 A5 34 D0 02 E6 35 A5 36
1F90 D0 02 E6 37 A5 37 C5 7C
1F98 D0 E6 A5 36 C5 7B D0 EB
1FA6 A5 2E 85 30 A5 2F 85 31
1FA9 A9 00 85 38 4C 8C 1E

HELP!

Sir—I would very much like to hear from any reader who might be in a position to supply me with either a R.O.M., tape or just a listing of the full advertised plug routines for the Computer User Aids UK101 High Resolution Board.

Harry Odes, London.
ZX81 SCREEN SAVE

Sir—This should interest owners of the ZX81 (16K), and provide a means whereby the contents of the screen can be recorded on tape and then retrieved at a later date.

The program puts the contents of the display file into a numeric string, which is recorded on tape following the command Save. After a Load instruction this same string is loaded into memory and on the command GOTO 50 the string is POKED into the new display file. There is just one important proviso: Do not use the instruction Run, as its use will wipe out the string and cause the program to crash. Lines 18, 40, 42, 52, 54, 56, 76 and 78 check for just such a crash and advise the user should it happen.

The Screen Save program is meant to run with any other user program (space permitting) and has been specially condensed into less than 100 lines such that it can be sandwiched into existing programs. To illustrate the point, Screen Save (lines 16–80) has been written in conjunction with “Cheese Nibbler” (lines 95–130).

To perform the programs/program run “Cheese Nibbler” at 100. When an interesting pattern presents itself, press any key which will cause the display to be memorised in a “II” string. At this stage the program and the display can be taped with “SAVE Screen Save”. At a later date the tape can be loaded back with “LOAD Screen Save”. The original display is available on the command “GOTO 50” or the “Cheese Nibbler” program is entered on the instruction “RUN 100”. The illegal command “RUN” or “RUN 50” will cause a crash into the user advice in line 78.

Incidentally I do not claim any originality for “Cheese Nibbler”; it is straight out of the ZX81 BASIC programming book chapter 18.

J. Vella, Carlisle.

Temperature Sense

Sir—As a regular reader of PE, I was interested in the article Gas Saver in the December issue. The point of my letter concerns additional experiments (using diode sensors on a solid fuel system), and these included monitoring the hot water tank temperature to obtain a differential control of the system in a similar manner to the author’s; and there may obtain a differential control of the system in a way to illustrate the original calibration could accommodate it. There may appear to entail any circuit changes, and the original calibration could accommodate it.

Due to the exchange losses in the boiler the temperature in the return pipe will initially be lower than the outflow pipe, but will increase as less heat is absorbed in the heat exchanger, and it is possible to obtain a correlation between the pipes’ differential and tank temperature. The reason for my suggestion is two-fold—it removes the possible requirement of any structural work for the feed wire and access to the tank, and therefore reduces the feed wire to a foot or two. The length of this lead caused me problems, not structural as I only had a free lead, but I found that due to the length of the lead my central heating was being operated by my son’s CB, even after I used screened lead and attempted several filtering methods. This suggestion is offered to anyone suffering from a similar problem, as it would not appear to entail any circuit changes, and the original calibration could accommodate it.

N. L. Smith, Stoke-on-Trent.

Chip Query

Sir—In your current issue is a letter by E. J. Hatch about the series “Introduction to Digital Electronics”. I endorse what he says but I would like to query your reply, giving a list of necessary i.c.’s; the last of these is given as 745124, which doesn’t exist.

Could you please tell me what was intended? Also do we need more than one of any of these i.c.’s?

J. A. J. Jarvis, Chester.

We are sorry but an error did in fact creep into our reply. The 745124 should have been a 74S124 which is available from Waford Electronics. Only one of each of the i.c.s is necessary.

J. A. J. Jarvis, Chester.

42 POKE 16507, E
44 PRINT AT 21, 0, “DISPLAY SAVED IN MEMORY ”
46 SLOW
48 GOTO 180
50 FAST
52 LET C=PEEK 16507
54 LET E=PEEK 16405
56 IF E>C+1 OR E<C-1 THEN GOTO 76
58 LET D=PEEK 16396+256*PEEK 16397
60 LET V=PEEK 16400+256*PEEK 16401
62 LET Q=0
64 FOR P=D TO (V-I)
66 LET A (P)=PEEK P
68 NEXT P
70 SLOW
72 GOTO 140
74 SLOW
76 SLOW
78 PRINT “YOU HAVE WIPED OUT THE DATA RELOAD TAPE AND GOTO 50” MAIN PROG AT 100
80 STOP
85 REM “CHEESE NIBBLER”
100 PLOT INT (RND*64), INT (RND*44)
110 UNPLOT INT (RND*64), INT (RND*44)
120 IF CODE INKEY$=0 THEN GOTO 100
130 GOTO 20
140 STOP
NOTE: Bold characters represent inverse video
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Our book “Best of E&M Projects Vol. 1” brings together 21 fascinating and novel projects from E&M’s first year. Projects include Harmony Generator, Guitar Tuner, Hexa-
DIGITAL LOGIC

Digital logic is based on the idea of only two (binary) states. These two states are known variously as true &
false, on & off, logic 1 & logic 0, or more frequently just 1 & 0. A digital signal is
always in one of these two states (or moving between them). Digital logic
gates allow these signals to be manipulated. Suitable combinations of
digital signals and logic gates allow circuits to be built to perform a wide range of
useful functions.

LOGIC SYMBOLS

Digital circuit diagrams use standard symbols to represent logic gates. The
most frequently used symbols are from the BS or the MIL series. The common
symbols from these two series are shown below.

PIN NUMBERING

TTL i.c.s are usually in dual-in-line (d.i.l.) packages. These have oblong
plastic or ceramic bodies which protect the silicon chip. Parallel rows of pins
0.1" apart protrude from the two long sides of the i.c., with a total of usually
14, 16 or 24 pins. The pins are numbered anti-clockwise from 1 when look-

GATE FUNCTIONS

A two-input gate can have 16 possible
functions. Not all of these are actually available as logic gates. The table
below identifies the possible inputs, with their corresponding outputs, for all
16 functions.

<table>
<thead>
<tr>
<th>LOGICAL FUNCTION</th>
<th>INPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOGIC C</td>
<td>0</td>
</tr>
<tr>
<td>A &amp; B</td>
<td>0</td>
</tr>
<tr>
<td>NAND</td>
<td>0</td>
</tr>
<tr>
<td>A</td>
<td>0</td>
</tr>
<tr>
<td>A &amp; B</td>
<td>0</td>
</tr>
<tr>
<td>A &amp; B</td>
<td>1</td>
</tr>
<tr>
<td>A &amp; B</td>
<td>1</td>
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<tr>
<td>A &amp; B</td>
<td>0</td>
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<td>A &amp; B</td>
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<td>1</td>
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<tr>
<td>A &amp; B</td>
<td>0</td>
</tr>
<tr>
<td>A &amp; B</td>
<td>1</td>
</tr>
</tbody>
</table>

7400 TTL FAMILY

Logic families are collections of logic
gates based on the same basic gate, and
they greatly simplify the construction of
logic circuits. Gates from a family all use
a common power supply, and they may
be connected together using a simple set of rules, safe in the knowledge that
they are all compatible. The most common
family is the 7400 series of TTL
gates. Within this family there are a
number of sub-families, and the num-
bering of TTL i.c.s is according to the
following general rules.

SN74LS86N

<table>
<thead>
<tr>
<th>SN</th>
<th>Indicates 7400 series TTL</th>
</tr>
</thead>
<tbody>
<tr>
<td>74</td>
<td></td>
</tr>
</tbody>
</table>

makers prefix (may be
any letters)

LS Indicate which TTL sub-
family:

null = standard
H = high speed
L = low power

86 Indicates gate function
e.g. 00 = quad 2/p NAND

<table>
<thead>
<tr>
<th>N</th>
<th>Manufacturer's package code</th>
</tr>
</thead>
<tbody>
<tr>
<td>74</td>
<td></td>
</tr>
</tbody>
</table>

Typically, TTL i.c.s are referred to in cir-
cuits without any reference to the
manufacturer's prefix or suffix, e.g. the
device above would be described as
74LS86.

LOGIC LEVELS

The voltage levels used to represent
logic 0 and logic 1 are defined for TTL
signals as below. Voltages between
these levels are not permitted TTL
levels.

Gate outputs: Logic 0 0V to +0.8V
Logic 1 Above +2.4V
Gate inputs: Logic 0 0V to +0.8V
Logic 1 Above +2.0V

An unloaded standard TTL gate has output levels of around +0.2V for logic
0 and +3-5V for logic 1. These levels
tend to move up and down, respectively,
as more gates are connected to the out-
put.

BOOLEAN SYMBOLS

Boolean Algebra is a shorthand way
of representing the behaviour of gates.
It uses true and false to represent logic
1 and logic 0. For inputs of A and B, and
an output of X, the Boolean shorthand
for the common gates is as follows.

| Buffer | X = A |
| Inverter | X = X |
| AND | X = A . B |
| OR | X = A + B |
| NAND | X = A . B |
| NOR | X = A + B |
| Exclusive-OR | X = A @ B |

USEFUL IDENTITIES

The following are useful Boolean
identities which allow simplification
of logic circuits, or the use of a smaller
number of different gates, to perform
the same function.

A + 0 = A
A + 1 = A
A + A = A
A + A = A
A = A

When looking at inverting gates, each
logical inversion introduces an over-rule
on the signal (to represent the inver-
sion). Over-rules of identical length can-
cel out in pairs, as indicated in the last
identity.
7400 Quad 2-input NAND
7401 Quad 2-input NAND oc
7402 Quad 2-input NOR
7403 Quad 2-input NAND oc
7404 Hex inverter
7405 Hex inverter oc
7406 Hex inverter 30V o/p
7407 Hex buffer 30V o/p
7408 Quad 2-input AND
7409 Quad 2-input AND oc
7410 Triple 3-input NAND
7411 Triple 3-input AND
7412 Triple 3-input NAND oc
7413 Dual 4-input NAND Schmitt
7414 Hex inverter Schmitt
7415 Triple 3-input AND oc LS
7416 Hex inverter 15V o/p
7417 Hex buffer 15V o/p
7420 Dual 4-input NAND
7421 Dual 4-input AND
7422 Dual 4-input NAND oc
7423 Dual 4-input NOR expand
7424 Dual 4-input NOR strobe
7425 Dual 2-input NAND high volts