Low-price robots from POWERTRAN

- hydraulically powered
- microprocessor controlled

The UK-designed and manufactured range of Genesis general purpose robots provides a first-rate introduction to robotics for both education and industry. With prices from as low as £470, even the home enthusiast can aspire to his or her own robot.

Each robot in the Genesis range has a self-contained hydraulic power source operated from single phase 240 or 120v AC or from a 12v DC supply. Up to six independent axes are capable of simultaneous operation and all except the grip axis have sensing devices fitted to provide positional control by a closed loop system based on a dedicated microprocessor. Movement sequences can be programmed by means of a hand-held controller or the systems can be interfaced with an external computer via a standard RS232C link.

The top-of-the-range P102 has dual speed control, enhanced memory and double acting cylinders for increased torque on the wrist and arm joints. There is position interrogation via the RS232C interface, increasing the versatility of computer control and inputs are provided for machine tool interfacing.

All Genesis robots are available either ready-built or in kit form. The latter provides not only extra economy but also valuable additional training as an assembly project.

Hebot II
Turtle-type robot

For a little over £100, Herbot II takes programming off the VDU and into the real world. Each wheel is independently controlled by a computer, enabling the robot to perform an almost infinite number of moves. It has blinking eyes, a two-tone bleep and a solenoid-operated pen to chart its moves. Touch sensors, coupled to its shell return data about its environment to the computer enabling evasive or exploratory action to be calculated.

The robot connects directly to an I/O port or, via the interface board, to the expansion bus of a ZX81 or other microcomputer.

Micrograsp

A real, programmable robot for a little over £200! Micrograsp has an articulated arm joined at shoulder, elbow and wrist positions. The entire arm rotates about its base and there is a motor driven gripper. All five axes are motor driven and four of these are servo controlled giving positive positioning. The robot can be controlled by any microcomputer with an expansion bus - the Sinclair ZX81 being particularly suitable.

Universal computer interface board kit £54.00
23 way edge connector £3.00
AX81 peripheral/RAM pack splitter board £3.50

Micrograsp Weight 8.7kg, max. lifting capacity 1.6kg
Robot kit with power supply £160.00

Genesis S101

Weight 29kg, max. lifting capacity 1.5kg
4-axis model (kit form) £470
5-axis model (kit form) £525
5-axis complete system (kit form) £817

Genesis P101

Weight 34kg, max. lifting capacity 1.8kg
6-axis model (kit form) £750
6-axis complete system (kit form) £1165

Genesis P102

Weight 36kg, max. lifting capacity 2.0kg
6-axis system (kit form) £1350
Powertran Cortex microcomputer self-assembly kit £295.00

All prices are exclusive of VAT and apply to the U.K. only. A low 21 days for delivery. Overseas Customers - please contact your export department for the name and address of your local dealer.
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OUR MAY ISSUE WILL BE ON SALE FRIDAY, APRIL 6th, 1984
(for details of contents see page 61)
**PRINCIPAL ELECTRONICS STEREO CASSETTE RECORDER KIT**

**COMPLETE WITH CASE**

**ONLY £34.50 plus £2.75 p&p.**

- **NOISE REDUCTION SYSTEM.**
- **AUTO SURROUND.**
- **TAPE COUNTER.**
- **SWITCHABLE E.G., INDEPENDENT LEVEL CONTROLS.**
- **TWIN V.U. METER.**
- **REMOTE & FLUTTER 0.1%.**
- **RECORD/PLAYBACK I.C. WITH ELECTRONIC SWITCHING.**
- **FULLY VARIABLE RECORDING BIAS FOR ACCURATE MATCHING OF ALL TYPES.**

**Kit includes:**
- Tascam transport mechanism, ready punched and tucked.
- Printed circuit board and all electronic parts. (i.e., semiconductors, resistors, capacitors, hardware, top cover, printed scale and mains transformer.

You must only include order and p&p in the telephone or mail order.

**STEREO TUNER KIT**

**SPECIAL OFFER!**

**£19.95**

This easy to build 3 band stereo AM/FM tuner kit is designed in conjunction with P. E. Ludy **(81)**, for ease of construction and alignment it incorporates three Mullard mod and an I.C. IF System. Front scale size 10½"x4½" approx. Complete with diagram and instructions.

**125W HIGH POWER AMP MODULES**

The power amp kit is a module for high power applications - disc units, guitar amplifier, mobile address systems and high power domestic systems. The unit is protected against short circuiting of the loading and is safe in an open circuit condition. A large safety margin exists by use of generously rated components, a highly powered r.m.s. unit. The PC board is back printed, etched and ready to drill for ease of construction and the aluminium chassis is preformed and ready to use. Supplied with all parts, circuit diagrams and instructions.


**HI-SPEAKER BARGAINS**

**AUDAX 8" SPEAKER**

**£5.95 plus £2.25 p&p.**

High quality 40 watts RMS.

**AUDAX 4" FERRRO-FLUX HI-FI TWEETER**

**£4.95 plus £2.45 p&p.**

5kHz-22kHz. Imp: 8 ohms. 60-70W max. p.s.m. 0.5% distortion.

**GOODMAN SPEAKERS**

8 ohm. Rs 12 ohm. Suitable for input up to 40W. £3.95 plus £1.05 p&p.

**MONO MIXER AMP**

**£45.00 plus £2.85 p&p.**

**£40 watt, 6 channel.**

40 watts: 20kHz sensitivity for 100W, 0.001% distortion. 40kHz. Stereo pairs £70. £79.50 p&p. £15. £15.50 p&p.

**MONO MIXER PREAMP**

**£10.50 plus £1.15 p&p.**

Complete with case.

**CALLERS!**

April 1984
HOME LIGHTING KITS
These kits contain all necessary components and instructions & are supplied complete with UK wiring. These kits are popular for customers who prefer to fit their own lighting. 
TDR300 Remote Control £14.95
MK5 Transmitter for all MK1000 Series kits £4.50
Screwdriver £1.50
TDR300K 200mA DC Relay £7.75
TDR300T 50mA DC Relay £7.75
TDR500K Remote Control £6.50
TDR500T Remote Control £6.50
LDR300 Rotary Control £3.50

MINI KITS
MK1 ELECTRONIC THERMOSTAT
Uses MK1001 to control temperature (9°C-29°C) and provides a steady 200mA for a full scale reading automatic on/off limit.

MICROPROCESSOR CONTROLLED MULTI-PURPOSE TIMER
Now you can turn your household electronic devices either permanently ON or OFF with just one programmable timer! Each timer is provided with 10 different time settings. A seven day cycle, e.g. to control other equipment in your system. 

PACK 1 £59.00
PACK 2 £118.00

PACK 3 £177.00

PACK 4 £236.00

PACK 5 £295.00

PACK 6 £354.00

PACK 7 £413.00

PACK 8 £472.00

PACK 9 £531.00

PACK 10 £590.00

DVM/ULTRA SENSITIVE THERMOMETER KIT
This new design is based on the CE 7726 A, a low powered version of the CE 7726 child and a 7 independent digital display. This kit will form the basis of a digital multimeter (only a few additional resistors and switches are required). The kit includes the display unit, all electronic components, a 9V battery, and full instructions for an ideal project for beginners. 

DVM ULTRA SENSITIVE THERMOMETER KIT £11.50

HOME CONTROL CENTRE
For opening and closing motorised garage doors plus switching garage and drive lights on and off up to a range of 400 ft. Numerous other applications like controlling lights and TV's etc. in the home. 

HOME CONTROL CENTRE £105.00

INFRA RED GARAGE DOOR CONTROLLER KIT
For opening and closing motorised garage doors plus switching garage and drive lights on and off up to a range of 400 ft. Numerous other applications like controlling lights and TV's etc. in the home. 

INFRA RED GARAGE DOOR CONTROLLER KIT £105.00

DVF113 MH RADIO KIT
Based on the 2N1505, kitchi an 825, 725, 150mA, 2 channel and crystal & circuit and a full range of electronic components. Requires a 5 to 15V four digit code easily changed.

DVF113 MH RADIO KIT £55.00

COMPLETE PACKS
PACK 1 £59.00
PACK 2 £118.00
PACK 3 £177.00
PACK 4 £236.00
PACK 5 £295.00
PACK 6 £354.00
PACK 7 £413.00
PACK 8 £472.00
PACK 9 £531.00
PACK 10 £590.00

MICROPROCESSOR CONTROLLED MULTI-PURPOSE TIMER
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PACK 6 £354.00
PACK 7 £413.00
PACK 8 £472.00
PACK 9 £531.00
PACK 10 £590.00

FREE YELLOW CATALOGUE
It's packed with ideas for all your stock range all at competitive prices.

Copyright Practical Electronics April 1984
Train for success in Electronics Engineering, T.V. Servicing, Electrical Engineering—or running your own business!

ICS have helped thousands of ambitious people to move up into higher paid, more secure jobs in the fields of electronics, T.V., electrical engineering—now it can be your turn. Whether you are a newcomer to the field or already working in these industries, ICS can provide you with the specialised training so essential to success.

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The expert and personal guidance by fully qualified tutors, backed by the long ICS record of success, is the key to our outstanding performance in the technical field. You study at the time and pace that suits you best and in your own home.

You study the subjects you enjoy, receive a formal Diploma, and you’re ready for that better job, better pay.

**FREE CAREER BOOKLET**

**TRAIN FOR SUCCESS IN ELECTRONICS, T.V. SERVICING, ELECTRICAL ENGINEERING—OR RUNNING YOUR OWN BUSINESS!**

**ELECTRONICS ENGINEERING**

A Diploma Course, recognised by the Institute of Engineers & Technicians as meeting all academic standards for application as an Associate.

**T.V. & AUDIO SERVICING**

A Diploma Course, training you in all aspects of installing, maintaining and repairing T.V. and Audio equipment.

**RUNNING YOUR OWN BUSINESS**

If running your own electronics, T.V. servicing or electrical business appeals, then this Diploma Course trains you in the vital business knowledge and techniques you’ll need.

**ELECTRICAL ENGINEERING**

A further Diploma Course recognised by the Institute of Engineers & Technicians, also covering business aspects of electrical contracting.

**THE 1984 GREENWELL CATALOGUE NOW AVAILABLE**

It’s Bigger, Brighter, Better, more components than ever before. With every copy there’s discount vouchers, Bargain List, Wholesale Discount List, Bulk Buyers List, Order Form and Reply Paid Envelope. All for just £1.00! (Order now for early delivery)

**STABILIZED PSU PANEL**

A199 A versatile stabilized power supply with both voltage (±20V) and current (20mA-2A) fully variable. Many uses inc. bench PSU, Ni-cad charger, den purifiers testing Panel ready built and tested and calibrated. £7.75. Suitable transformer and pots. £6.99. Full data supplied.

**PUSH BUTTON BANKS**

W476 An assortment of latching and independent switches on banks from 2 to 7 way, DPDO to 6PCO. A total of at least 40 switches for £2.95; 100: £5.50; 250: £14.95; 1000: £45.00.

**SEAT BELT ALARM**

Originally for sale at £29.95, these well made units 70 x 50 x 25mm provide both audible and visual alarms. Uses 2 9V cells. £25.00. £2272 transducer, etc. Available ready built, with circuit and instructions for just £2.95. Also available as a kit, PCB and all components, box, wire etc. together with instructions. Only £3.95.

**LOGIC POWER SUPPLY**

This hefty built mains adapter supplies 4.5V @ 150mA DC, so can easily be modified to a stabilized 5V supply. Built in continuous plug for standard mains supply. Only £1.95; 10 £16; 25 £32; 100 £110.

**1N5401 3A 50V RECTS**

Bulk purchase enables us to offer these at special prices. 25: £1.00; 50: £1.45; 250: £12; 1000: £43; 5000: £200.

**5mm RED LED SCOOP!!**

Full spec brand new devices at a low, low price! 25: £1.95; 100: £25; 250: £50; 1000: £200.

**2N3055 SCOOP!!**

Made by Texas – full spec devices 60p each; 10 for £4; 100 for £34; 250 for £75; 1000 for £225.

**VEROBLOC £1 OFF!!**

Our biggest selling board on offer at a special price of £4.10.

**FABRIC CHLORIDE**

New supplies just arrived — 250mg bags of granules, easily dissolved in 500ml of water only £1.15; 10 for £9.95; 25 for £16; 100 for £60. Also abrasive polishing block 95p.

**TELESCOPIC AERIALS**

As used in Sinclair microvision, 9 section 110cm long. Only 95p.

**TTL PANELS**

Panels with assorted TTL ICs, LS types. Big variety. 20 chips £1.00; 100 chips £4.00; 1000 chips £30.00.

**RIBBON CABLE**

Special purchase of multicoupled 14 way ribbon cable — 40p/metre. 50m £18.00; 100m £32.00; 250m £65.00.

**NICAD CHARGERS**

Versatile unit for charging AA, C, D and PP3 batteries. Charger/test switch, LED indicator, switch selectable from the 5 charging points. Mains powered. 210 x 100 x 55mm £7.95. Model A124. Unit plugs directly into 13A socket, and will charge up to 4 AA cells at a time. £13.50; 1000 £39.50.

**Ni-CAD BATTERIES**

Aa size 99p each; C size 199p; D size 299p; PP3 size 399p.

**PRECISION PCB DRILL**

Small size, 35mm dia x 15mm long. 12V operation. Supplied with collet + 1mm bit 6000rpm. Only £7.50.

**1000 COMPONENTS $1!!!**

Amazing variety of passive components — carbon, film, oxide, wirewound resistors from 1W to 1/2W, ceramic, polystyrene, polyester and electrolytic capacitors in an extremely wide range of types and values. £100mm, £200mm, £300mm, £600mm. Suitable for all types of work. Order now!£17.95.

**CLOCK CASES**

A wide variety of shapes, sizes and styles. From oval £1.25 to square £5.00. Supplied complete with movement and glass. £10.00; 100 £90.00.

**OUR LARGE RETAIL SHOP STOCKS A WIDE RANGE OF COMPONENTS AND IS OPEN 9.30-5.30 MON-SAT.**

**GREENWELL**

443c MILLBROOK RD, SOUTHAMPTON SO1 0HX

ALL PRICES INCLUDE VAT; JUST ADD 60p P&P

EX-STOCK

Practical Electronics April 1984
MINIATURE TOOLS FOR HOBBYISTS

**FLEXDRIVER**
A flexible shaft screwdriver for those difficult jobs. Overall length 6 Inch.
Order No: FS-2 Cross point no. 1. £1.75 each.

**GRIP-DRIVER**
Ratchet long screwdriver with spring loaded grip on end to hold screw in position while reaching into difficult places. Order No: FS-1 Flat blade 4mm SI-2 Cross point no. 2. £9.50 each.

**MINIATURE BEND NOSE PLIERS**
With side cutter and serrated jaws - insulated handles Snip length Order No: Y042 ALL AT £1.25 each.

**VALUE PACKS**

<table>
<thead>
<tr>
<th>No.</th>
<th>Qty</th>
<th>Description</th>
<th>Price</th>
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<tbody>
<tr>
<td>VP1</td>
<td>300</td>
<td>Assorted Resistors Mixed Types</td>
<td>£0.01</td>
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<tr>
<td>VP2</td>
<td>200</td>
<td>Carbon Resistors 10k ohm. mixed forms</td>
<td>£0.02</td>
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<tr>
<td>VP3</td>
<td>300</td>
<td>1 Watt Resistors 250-500 ohm-Mixed</td>
<td>£0.01</td>
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<tr>
<td>VP4</td>
<td>500</td>
<td>1 Watt Resistors 100 ohm-Mixed</td>
<td>£0.005</td>
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<tr>
<td>VP8</td>
<td>100</td>
<td>Mixed Capacitors</td>
<td>£0.005</td>
</tr>
<tr>
<td>VP20</td>
<td>50</td>
<td>Ceramic Disc 5pf - 1000pf Mixed</td>
<td>£0.02</td>
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<tr>
<td>VP21</td>
<td>100</td>
<td>Ceramic Disc 470pf - 1uf</td>
<td>£0.12</td>
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<tr>
<td>VP22</td>
<td>100</td>
<td>Electrolytics</td>
<td>£0.05</td>
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<tr>
<td>VP23</td>
<td>50</td>
<td>Large Assorted Resistors Mixed Types</td>
<td>£0.025</td>
</tr>
<tr>
<td>VP24</td>
<td>50</td>
<td>Large Assorted Capacitors Mixed Types</td>
<td>£0.025</td>
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**MINIATURE END NIPPERS**
Insulated handles 5 Inch length. Order No: Y043 £0.75 each.

**MINIATURE FM TRANSMITTER**
A flexible shaft screwdriver for those difficult jobs. Overall length 6 Inch.
Order No: FS-2 Cross point no. 1. £1.75 each.

**MINIATURE TOOLS FOR HOBBYISTS**

**SILICON BRIDGE RECTIFIERS**

<table>
<thead>
<tr>
<th>Description</th>
<th>Price</th>
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<tr>
<td>Comprising 4 x 1.5 amp miniature rectifiers mounted on PCB</td>
<td>£0.70</td>
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<tr>
<td>VRM = 150vuts</td>
<td>£1.05</td>
</tr>
<tr>
<td>Size: 1 inch square</td>
<td>£1.50</td>
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**MINIATURE FM TRANSMITTER**
Free: 35-45 MHz Range 1 mile Size: 45 x 25 x 30mm fitted for Battery. 10 pence each.

**MULTITESTERS**

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<th>Description</th>
<th>Price</th>
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<tbody>
<tr>
<td>Input: 240V AC 50Hz. Output: 0-200V AC &amp; DC, 0-20mA AC &amp; DC</td>
<td>£1.75</td>
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<tr>
<td>Dimensions: 180 x 120 x 40mm. Includes 20 pence leads and batteries.</td>
<td>£5.50</td>
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**SIREN ALARM MODULE**

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<th>Description</th>
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<tr>
<td>Siren 20mm Add 9v battery to 4 or 8 ohms</td>
<td>£1.00</td>
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<tr>
<td>Power consumption 50mA.</td>
<td>£3.85</td>
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**SIREN ALARM MODULE**

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<tr>
<th>Description</th>
<th>Price</th>
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<tr>
<td>American Police type siren available from any 12 volt supply into 4 or 8 ohms.</td>
<td>£3.85</td>
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**TRANSISTOR CLEANER**

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<th>Description</th>
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<tr>
<td>All Transistors, A mixed Bag NPN-PNP Silicon &amp; Gemini. Mainly fished out to Son Price. 100 each includes Instructions for Making Simple Transistor Tester.</td>
<td>£1.00</td>
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**TECASBOTY**
The Electronic Components and Semi-conductor Bargain of the Year! This collection of Components & Semiconductors for the hobbyist is probably the most value-packed selection ever offered. It consists of Resistors, carbon and wirewound of various values. Capacitors, both fixed and variable, and some including, electrolytics, Potentiometers - single, dual, slider and preset. Switches, fuses, Heatsinks, Wire, PWB Board, Plugs, Connectors etc., PLUS a selection of Semiconductors for everyday use in popular hobby Projects. These include: SCR's, Diodes, Rectifiers, Triacs & Bridges as well as a first class mix of Transistors and I.C.'s. In all, we estimate the value of this in current Retail catalogue is 50% So, help yourself to a great surprise and order a BOX TODAY for just £6.50 ONLY at BI-PAK. Remembere to have your Barclaycard or Access Card - cash availability Service - NOW. Order No. V906.

**USE YOUR BARCLAYCARD OR ACCESS CARD**

<table>
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<tr>
<th>Description</th>
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**TRIACS**

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<th>Description</th>
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<tr>
<td>4 AMP - 400V - T0222 - TAG16G</td>
<td>£1.00</td>
</tr>
<tr>
<td>1000pF</td>
<td>£1.00</td>
</tr>
<tr>
<td>1000pF</td>
<td>£1.00</td>
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<tr>
<td>40p</td>
<td>£1.75</td>
</tr>
<tr>
<td>28 AMP DC</td>
<td>£5.00</td>
</tr>
<tr>
<td>28 AMP 400V - T0222 - TAG425</td>
<td>£5.00</td>
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**VOLTAGE REGULATORS T0220**

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<th>Description</th>
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<tr>
<td>Push + Negative</td>
<td>£5.00</td>
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<tr>
<td>7805</td>
<td>£5.00</td>
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<td>7805</td>
<td>£5.00</td>
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<tr>
<td>7812</td>
<td>£5.00</td>
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<tr>
<td>7812</td>
<td>£5.00</td>
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**We hold vast stocks in stock for fast immediate delivery, all items in our Catalogue are available ex stock.**

**To receive your NEW 1984 BI-PAK Catalogue, send 75p PLUS 25p p&p to: BI-PAK BARGAINS.**
SPECIAL FEATURES:
AIDS TO BETTER GARDENING—
Hand Cultivators, Chemical
Weed Killers and sprayers.

EXTRA, EXTRA, Home Plus colour magazine,
is also carried in these three issues. Feature Articles
include Raising the Readies, Gadgets for the home
and winter ravages repaired.
Heathkit - IT'S A PLEASURE TO BUILD

Bring the enjoyment back into your hobby with a kit from Heathkit. The beautifully illustrated documentation and step-by-step instructions make building a Heathkit a relaxing, absorbing pleasure! Choose from their huge range of fascinating kits and self-instruction electronics and computing courses. The Heathkit range includes the ultimate in amateur radio kits, computerised weather stations, a highly sophisticated robot, a 16-bit computer kit and a range of home (or classroom) learning courses. These state-of-the-art courses have easy-to-understand texts and illustrations, divided into sections so that you can progress at your own pace, whilst the hands-on experiments ensure long-term retention of the material covered.

You'll find Heathkits available for Amateur Radio Gear • Car Test Equipment • Kits For The Home • Self-Instruction Courses • Computer Kits • Test Instrument Kits • Kits For Weather Measurements.

All the most popular kits and educational products are fully detailed in the 1984 Maplin catalogue (see outside back cover of this magazine for details) or for the full list of Heathkit products send 50p for the Heathkit International Catalogue complete with a UK price list of all items.

All Heathkit products available in the UK from:

Maplin Electronic Supplies Ltd.
P.O. Box 3, Rayleigh, Essex, SS6 8LR.
Tel: (0702) 552911.
(For shop addresses see back cover.)
SECURITY

A COMPLETE INTRUDER ALARM

ALARM CONTROL UNIT

CA 1250

Price £15.95 + V.A.T.

This is the heart of any alarm system. The CA 1250 offers every possible feature that is likely to be required when constructing a system whether it is a highly sophisticated installation or simply connecting a single magnetic switch on the front door. It is an expert in 250m dual beams of 2040 one adjustable range up to 25m. Provides two loud speakers - Off, Test and Operate.

SIREN & POWER SUPPLY MODULE

PS 1000

only £10.50 + V.A.T.

Price £18.95 + V.A.T.

Horn speaker MS 588

Price £7.99

A horn speaker provides extremely high sound pressure levels (100dB) in a compact enclosure. It is designed for indoor use and is powered by the power supply unit. It is operated from a 15 amp power supply and is suitable for use in public address systems.

ultrasonic module

IR 1470

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Teaching you in a step-by-step method the MPF1 PLUS helps the user fully understand the Software and Hardware of a microprocessor easily and conveniently – as opposed to micro-computers that aim to teach high-level languages instead of microprocessor systems fundamentals.

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Prior to this advertisement, all quoted regular prices have been charged during the last six months at the Tandy Store. Times may vary at different stores and price changes may occur. Prices subject to availability.
ELECTRONICS has really emerged from recession with a predicted growth for 1984 in every area of the market. Much can be blamed on the microprocessor which has made possible the integration of computers in automation, manufacture and communications. Fastest growth predicted, not surprisingly, is for memories, but the microprocessor is dragging along all the associated areas like p.s.u.s, lithium batteries, connectors, switches, displays—i.e., for hand held computers and c.r.t.s for v.d.u.s—and of course the passives, capacitors and resistors.

SMD
The humble resistor is about to lead (no pun intended) the march into SMDs (surface mounted devices) with a market which is expected to grow from $90m in 1983 to $140m in '84. The introduction of SMDs has already started in a big way, with the Japanese (who else?) setting the pace. The technology is concerned with cost saving by doing away with costly p.c.b. holes, the space they take and the simplification achieved when mounting on both sides of the p.c.b. or with multilayer boards. Fast, automatic "onsertation" (as opposed to insertion) and additional savings on connectors and mechanical hardware, as a result of smaller boards, also provide significant cost reductions. We will be publishing a feature on SMDs in the near future.

Of course a whole new area of industry has now come of age, again with thanks to the m.p.u. CAD/CAM or computer aided design and manufacture has taken off with a predicted growth for '84 of 30-40 per cent. CAE (computer aided engineering) has also taken on a significant role and it is predicted that this area will stay on 80 per cent growth rate for the next few years. Clearly the potential is vast.

HOBBY
What does all this mean to the hobbyist? It is obvious that components with leads will be around for a long time yet: although it is possible to hand mount SMD's, so even with them we will be able to continue our hobby.

Of course the microprocessor has had a significant impact on what the hobbyist can build and indeed on what he wants to build. Would we have needed a Logic Analyser or the Microstepper (see page 18) a few years ago? How many people would have wanted an EPROM Duplicator or a Computer Terminal in the 70's?

It is obvious that each time industry steps forward the benefits are quickly felt in the hobby area, usually long before they become obvious to the general consumer. We can however see one disadvantage in this fast growth—component shortages and the resulting price increases.

Three years ago I wrote the following:

"Unfortunately the present buying spree by industry is creating component supply problems and once again we suspect the hobbyist is beginning to suffer. Delivery dates are lengthening and sometimes being broken by manufacturers, so have some sympathy with your component retailer if he is out of stock and says it could be a month or two before a certain device is again available—very often he can only pass on information from the manufacturer and that information has sometimes proved to be unreliable."

We anticipate that this situation may return towards the end of '84 so it may not be a bad time to stock up with a few components!
DRAGON MEMORY UP 32K

Following in the steps of the Dragon 32 home computer is their latest model, the Dragon 64K which utilises the 6809E microprocessor. Compared to the 8055 and 6502 processors used by many of Dragon's competitors, the 6809 contains several 16-bit registers to allow for flexible address mode capabilities, making high level language implementation more practical. BASIC, PASCAL and COBOL can all be used in conjunction with the Dragon 64.

The new model was launched late last year along with their disk based OS-9 operating system designed specifically for the Dragon 64, which will give the user a wide range of possible business applications.

The OS-9 system is seen by Dragon Data as the user's passport to professional software, which will include packages for stock control, invoicing, accounting, payroll and even spreadsheet analysis.

The Dragon 32 has proved to be a successful machine and has placed Dragon Data high in the home computer market.

The introduction of the powerful Dragon 64, the OS-9 operating system and the recent introduction of their disk drives gives them the means to enter other markets, where they are confident and expect to achieve equal success.

The Dragon 64 offers three different operating modes. The '32' mode allows the user to operate the machine as a Dragon 32. The '48K Mode' gives 48K RAM and 16K Basic Interpreter and the '64K Mode' enables full use of the 64K RAM.

It is important to note that all the features on the Dragon 64 are in addition to, and not at the expense of, those offered on the Dragon 32. The high resolution display of 256 x 192 pixels is retained and all the currently available software for the 32, both in plug-in cartridge and cassette form, is compatible with the 64.

In addition the recently launched Dragon Disk Drives will run on both the 32 and 64. The Dragon 64 costs £225 and will be available through the usual Dragon dealerships, including both Boots and Dixons.

Match That

An ultra-miniature 50 volt microswitch with actuator arm has been announced by Semiconductor Supplies International. This 300mA single pole changeover switch weighs 0.3 grams. Dimensions are height (inclusive of pins and with lever compressed) 10mm, width 8mm, thickness 3mm. The actuating lever of this switch is shaped for cam follower applications as well as for ordinary compression applications.

Uses include the tamper proofing or safety switching of small equipment including security equipment such as sensors or for switching models etc. Price per pack of 10 is £4.00 inc p & p. Semiconductor Supplies, Sutton, Surrey SM1 4RS (01-643 1126).

DE-SOLDERER

A new electric desoldering iron from OK Industries combines the virtues of a handheld, manual unit with the performance of an industrial desolder station. The lightweight SA-6 features 'one-hand' desoldering and eliminates the need for two tools, combining heat and suction in one.

The vacuum chamber is easily removed for cleaning, and replacement tips are available with 1.5mm and 1.77mm hole diameters. 115 or 230V a.c. 50/60Hz versions are offered; the 230V type costs £18 all inc.

OK Industries UK Ltd, Dutton Lane, Eastleigh, Hants SO5 4AA (0703 619841).

OXYGEN IONS

A £1.2m ion blasting machine, to be built at the Atomic Energy Authority's Harwell research laboratories, could give Britain a world lead in an area of advanced chip production.

To be completed by next year, the machine will be capable of creating a circuit beneath the surface of a slice of silicon.

What happens is this: The silicon is bombarded with high energy oxygen ions at a minimum of $10^{17}$ ions/sq. cm. Because of their high energy, these ions rip through the surface of the silicon and come to rest at about one micron deep, where they form a subsurface layer of silicon dioxide. The technique is currently known as ion implantation, and is used to introduce dopants, such as boron and arsenic. But with ten times the ion current, Harwell's machine will be able to create a "buried dielectric" because the absorbed oxygen ions form an insulating layer which can be patterned so as to create circuit elements. It is necessary to maintain the silicon at a temperature of 500 deg. C in order to create a self-healing effect where the ions tear through the silicon's surface.

Mechamorphosis

A simple yet innovative joystick has been developed by E.E.C. Ltd. It is designed for use with the ZX Spectrum and is purely a mechanical device.

The joystick clips onto the machine and directly depresses the relevant keys without obstructing any other command keys, neither will it interfere with any of the Spectrum peripherals. This UK patented invention was launched late last year and is already being exported to many European countries. Although High Street availability is planned by the company the device is only presently available on a mail order basis.

Perhaps the most appealing feature of this unit is its price, £9.95 plus 55p p&p. Details from, E.E.C. Ltd, 1 Whitehouse Close, Chalfont St Peter, Bucks SL9 0DA (0753 985401).
Briefly...

Whilst the Home Office's position is that the protection afforded UK laboratory animals represents a satisfactory balance between the need to experiment on living creatures and public revulsion at their suffering, it does point out that the 1876 Cruelty to Animals Act is to be reviewed when Parliamentary time permits.

Meanwhile, the rodents and monkeys behind bars may diminish in numbers thanks to computer models of their body chemistry. Computers that can simulate the cardiovascular and respiratory systems, and graphically illustrate changes therein, will increasingly be substituted as research aids.

Available from Verospeed, is a unique non-volatile RAM that can retain its data for ten years without a power supply.

Manufactured by Mostek, the MK48Z02 incorporates 16K (2K x 8 bits) of static RAM and two moulded-in lithium batteries, all in a standard 24-pin d.i.l. package. The device operates from 5V at 385mW (10mW standby), and at a speed of 250ns.

Sir Keith Joseph's proposed changes in the school curriculum should improve skills in school-leavers, better fitting them for immediate employment. Surprisingly, for Sir Keith has many critics, there was general agreement from all sectors of education that this was a good thing. The young are increasingly being substituted as research aids.

POLYtechnic places in science, mathematics, and engineering and technology.

catalogues as 96364E (E for plastic) for some time to come, as far as the maker is concerned it is now known as the EF9364, with suffix P for plastic and C for ceramic. The device is available from Technomatic Ltd., and Watford Electronics.

Silicon News Corner

Burr-Brown MPY100 is a low cost, precision multiplier/divider. Four quadrant multiplication, square root, r.m.s. to d.c., linearisation and algebraic computation often without need of amps or potentiometers.

JFET op amp, called OPA 100, has initial bias current of 0.5pA @ room temp., and only 35pA at 125°C!

Burr-Brown, Cassiobury House, Station Rd., Watford WD1 1EA.

National Semiconductor New series of 16 large 0-43 in. 7-seg. d.l.d. display. Red, yellow and green are 5082-760, 5082-7660 & 5082-7670 respectively.

National Semiconductor, 301 Harpur Centre, Horncastle, Lincs.

TRW LSI Launches 3 member family of economical Flash ADCs. TDC 1029 offers 6-bit at 100 MSPS at bandwidth of 50MHz. Places video speed A/D within reach of more applications.

MCP Electronics, 38 Rosemont Rd., Alperton, Wembley, Middlesex HA0 4PE.

Plessey New range of CCDs. MS 1002-1/3 is 850 bit register. MS 1003-1/3 is 910 bit register. Both have video bandwidth above 5MHz and clock frequency of 13 MHz.

High speed ECL 10-bit synchronous up/down counter is SP9215. Clock to 50MHz.

Information: Charles Baker Lyons, 30 Farrington St., London EC4A 4EA.

IR Two new ranges to power MOSFETs (HEXFETs). Range 1: 30 parts in TO 39 package in N & P channel, eight different voltages. Range 2: Extension to d.i.l. MOSFETs. 4-pin device is "stackable" to make arrays of N or P channel switches. Rated 200V.

International Rectifier, Hurst Green, Oxsted, Surrey RH8 9BB.

TI First two in series of CMOS 8-bit, single-chip microcomputers add to TMS 7000 family. NMOS capability with CMOS power advantage. TMS 7000C and TMS 707C.

Texas Instruments, Manton Lane, Bedford MK41 7PA.

POINTS ARISING...

COMPUTER TERMINAL
February '84

The CRT controller chip SFF96364 (manufactured by Thomson CSF) will continue its existence under a new part number, and although it may be seen in its present incarnation it is now known as the EF9364, with suffix P for plastic and C for ceramic. The device is available from Technomatic Ltd., and Watford Electronics.

CLOCK TIMER
February '84

The value of C2 should be 15nF not 150nF.

Countdown...

Please check dates before setting out, as we cannot guarantee the accuracy of the information presented below. Note: some exhibitions may be reviewed when Parliamentary time permits.
The Microstepper described here is a "clip-on" device which allows you to follow the operation of a microprocessor system. Unlike other electronic systems, the operation of a microprocessor system cannot be seen with standard test equipment such as the C.R.O. and multimeter etc. The address bus and data bus lines transfer large amounts of data at high speed—typically 24 bits of data one million times per second.

To understand or debug such a system, a detailed analysis is required of all this, slowed down to "human" speed, and presented on some form of visual display.

The professional answer is to use a logic analyser. This is a very versatile instrument, which can store, and then display, a sequence of binary states of bus and control lines in any logic system. Logic analysers are expensive, and considerable expertise is required in setting up the instrument, and interpreting results.

The Microstepper device is dedicated to microprocessor systems. In use, it is attached to the system under test, and puts it into "single step" mode. In this mode, each individual step of a program can be followed. Data can be "seen" going to or from memory, I/O ports etc.

Quite apart from the obvious hardware and software debugging uses, a fascinating method of self teaching is provided. To see a program executed by the hardware before your eyes is the surest way to understand both hardware and software.

**OPERATION**

There are only three controls:

S1 — A push button labelled "GO" which, when pressed, runs the system to the next step.

S2 — A three position switch, labelled "RUN", "STEP", and "BREAK". These functions are explained later.

S3 — 10 and S11—18 — a total of 16 "in-line" switches, for setting up a binary address "break point".

Data display is by six 7-segment I.e.d.s, four for the address bus, and two for the data bus. Connections to the Microstepper are shown for a Z80, but the device is adaptable to other microprocessors. A 40 pin test clip is used to attach the Microstepper to the microprocessor chip in the system under test. In the illustrations, this is shown wired directly to the circuit board.

If, however, operation with more than one type of microprocessor is envisaged, the Microstepper connections to the 40 pin test clip should be made via a 30 pin plug/socket on the Microstepper board. Each different type of microprocessor can then have a separate test connector, wired appropriately for that chip.

Power supply may be taken from the system under test, or from an external supply, the choice being made by S19. Power supply requirements are 5V at 600 mA.

To use the device, attach the test clip to the microprocessor, before applying power. Switch S2 to "STEP". Apply power, and press "GO" to reset the Microstepper. Reset the system being tested.

**SINGLE STEP MODE**

The first address (0000 Hex in the case of the Z80) will appear on the address display, and the contents of that memory address will appear on the data display, both in hexadecimal form.

Step through the program by pressing "GO". Each time "GO" is pressed, the next "read" or "write" operation will be displayed. Compare the observed results with the program at each step. Any software bugs will be evident because the system does exactly what the program tells it to do, which may not be what the programmer intended! Hardware faults are evident when the program is correct, but the system responds incorrectly—perhaps with unexpected address or data displays. Frequent causes of this type of fault are bus lines open circuit, earthed, or interconnected, producing strange symptoms.

This is the printed circuit version of Microstepper. Sheer speed in a computer creates the illusion of intelligence, but the illusion can be removed to allow measurements and readings to be taken step by step.
Fig. 1. Full circuit diagram of the Microstepper. As an educational aid, or diagnostic tool, Microstepper can "action replay" your computer in slow motion.
An example will show how to deal with this type of fault. Suppose part of a program reads:

<table>
<thead>
<tr>
<th>Address</th>
<th>Code</th>
<th>Mnemonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>0010</td>
<td>3E</td>
<td>LD. A 34</td>
</tr>
<tr>
<td>0012</td>
<td>32</td>
<td>LD. (3012). A</td>
</tr>
</tbody>
</table>

In a good system, stepping through from address 0010 should show on the displays—

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0010</td>
<td>3E</td>
<td>Opcode fetch</td>
</tr>
<tr>
<td>0011</td>
<td>34</td>
<td>Second byte</td>
</tr>
<tr>
<td>0012</td>
<td>32</td>
<td>Opcode fetch</td>
</tr>
<tr>
<td>0013</td>
<td>12</td>
<td>Low byte of address</td>
</tr>
<tr>
<td>0010</td>
<td>3E</td>
<td>High byte of address</td>
</tr>
<tr>
<td>3E12</td>
<td>34</td>
<td>Write from Accumulator to memory location 3E12 (?)</td>
</tr>
</tbody>
</table>

Note that we see not only code held in ROM, but also data being written to RAM. Now, suppose a faulty system gives these displays—

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0010</td>
<td>3E</td>
<td>Opcode fetch</td>
</tr>
<tr>
<td>0011</td>
<td>34</td>
<td>Second byte</td>
</tr>
<tr>
<td>0012</td>
<td>32</td>
<td>Opcode fetch</td>
</tr>
<tr>
<td>0013</td>
<td>12</td>
<td>Low byte of address</td>
</tr>
<tr>
<td>0014</td>
<td>10</td>
<td>High byte of address</td>
</tr>
<tr>
<td>1012</td>
<td>34</td>
<td>Write from Accumulator to memory location 1012</td>
</tr>
</tbody>
</table>

The last step shows the processor attempting to write data into a strange address—3E12 Hex. This is because, in the previous step, the high byte of the address was read from RCM location 0010 instead of 0014. If we reset the system, and go to the 5th. step, where things appeared to go awry, a simple voltage check on bit 3 of the address bus shows zero volts (logic 0) instead of logic 1, possibly caused by an earth.

That caused binary address 0000 0000 0001 0100 to become 0000 0000 0001 0000 = 0010 Hex

This example illustrates another point, which is, hold the process at any point, and you can check for correct logic levels, under static conditions, with a simple multimeter.

---

Fig. 2. Printed circuit board layout of the Microstepper. This is the "copper-side" view at full size.
BREAK POINT OPERATION
Pressing "GO" to get to a particular part of a program can be tedious. Imagine going round a counting loop 10,000 times! To go to a particular address quickly, set S2 to "BREAK", and set up the desired address as a binary pattern on S3–18. Reset the processor, and press "GO". The system will run normally until the required address is reached, when the Microstepper holds the processor, displaying address and data as before. Now switch to "STEP", and step through the program from there. Alternatively, set S3–18 to a new address, press "GO", and the program will run up to the new address.

RUN MODE
With S2 in the "RUN" position, press "GO", and normal program execution will result.

DYNAMIC RAM
Note that where any dynamic RAM in the system is refreshed by the microprocessor, as in the Z80, refresh will not take place whilst the processor is halted by the Microstepper. In this case, ROM and program operation can still be observed, using "break" operation to skip over all data storage operations up to an area of interest in the program.

CIRCUIT DESCRIPTION
Consider first S2 at "STEP". Pressing "GO" takes IC14 pins 1, 2 low, making IC14 pin 3 high. IC13 is an edge triggered data bistable, so it is "set" by the rising voltage on IC13 pin 3. The resulting "high" on IC13 pin 5 is connected to the microprocessor "WAIT" line, so the processor is free to run normally. After reset of the processor, the first address (0000 Hex in the case of the Z80) appears on bits 0 to 15 of the address bus, and the processor signals a READ operation, by pulling RD low. IC14 pin 11 goes high, IC14 pin 5 is high due to S2, so IC14 pin 6 is low, and IC14 pin 8 goes high to set IC13b. IC13b pin 5, now low, resets IC13a, and pulls the WAIT line low, stopping the processor.

In this state, the 16 bits of the address bus are buffered by IC1, IC2, to drive the comparators IC9, IC10, IC11, IC12, and decoders IC5, IC6, IC7, IC8. Each decoder takes one 4-bit "nibble" to produce a hexadecimal readout on the 7-segment displays X3 to X6.

Meanwhile, the memory in the system under test responds by placing data on the data bus, which is decoded by IC3, IC4, and displayed on X1 and X2.

This condition holds until the "GO" button is pressed, taking IC14 pins 1, 2 low, IC14 pin 3 high, thus setting IC13b. IC13b pin 5, now high, removes the reset from IC13a, and places a "high" on the WAIT line. The processor now runs to

Fig. 3. P.c.b. layout of "component-side" (actual size)
COMPONENTS...

Resistors
- R1, 2, 19: 10k (3 off)
- R3–10, R11–18: 8 x 10k s.i.l. (2 off)

Capacitors
- C1: 4μF tant.
- C2, C3: 220n poly (2 off)

Integrated Circuits
- IC1, IC2: 74LS244 (2 off)
- IC3–8: 9368PC (6 off)
- IC9–12: 74LS85 (4 off)
- IC13: 74LS74
- IC14: 74LS132

Displays
- X1–6: DL704 comm. cath. (6 off)

Diodes
- D1: OA202

Switches
- S1: Keyboard push-button (p.c.b. mounting)
- S2: 2P3V/ slide switch (only one pole used)
- S3–10, S11–18: 8-way d.i.l. switch (2 off)
- S19: 1P2W toggle switch

I.c. sockets
- 20-pin: 2 off
- 16-pin: 10 off
- 14-pin: 2 off

Miscellaneous
- Printed circuit board
- 40-pin test clip (RS 424 153)
- Ribbon cable for above
- Supply leads (for power supply)
- Eyelets, or pins for "through board" connections
- Solder pins for wire terminations

Constructor's Note
If the test clip can only be found in the RS Components catalogue, it may interest non-trade readers to know that components can be obtained from RS indirectly, via Ace Mailtronix, 3a Commercial St., Batley, West Yorkshire.

Fig. 4. Component layout of the Microstepper
**RH Software**

RH Electronics has a whole series of excellent software for the BBC Microcomputer Model B. For games, business and education, they will be highly valued by any BBC Micro owner.

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Guide the snake around its electric cage devouring as much food as you can. Avoid touching the electrified walls, swallowing unsavoury food or causing the snake to eat its own tail.

**FOR THE BBC MICROCOMPUTER**

**The DAC PACK (Digital to Analogue Converter)** will give your computer, for the first time, the capability to communicate with the outside world in its own language. The DAC PACK features a 2.5 V internal reference voltage for rock steady output and a step resolution of 1024 levels. It has 16 bit input and output, 8 bit input port and a separate 8 bit output port. It is housed in a neat thermo-plastic case the INTERBEEB and therefore requires no further installation. The DAC PACK connects to the DCP bus and therefore requires that either the INTERSPEC or INTERBEEB be present. As with all other DCP products, the DAC PACK comes complete with a comprehensive manual and costs £19.95 + postage & packing.

**The AD PACK (Analogue to Digital Convertor)** is easy to use and understand and consists of a fast A to D convertor with an internal precision voltage reference source for accurate conversions. The input voltage swing is 0 to 2.5 V with a tolerance allowable of ±5%, therefore giving a 10 bit input resolution. The AD PACK is connected using the DCP bus and will therefore require either the INTERSPEC or INTERBEEB to be connected to the host computer. The AD PACK comes with a manual which includes examples of operation and costs £19.95 + postage & packing.

**The S-PACK**

The Speech Pack is a completely self-contained add-on speech synthesiser for the ZX81 or Spectrum Computers which may be used in addition to a ZX RAM PACK, DCP PACK and/or ZX printer. The S-PACK is supplied complete with Word Pack ROM 1 which contains all the letters of the alphabet, numbers 0 to over a million and some other general words which can all be 'spoken' under computer control. Up to three more Word Pack ROM's can be fitted to expand the vocabulary, details of which are available on request. The 2 versions of the speech pack for the ZX81 and Spectrum operate in similar manners but are NOT interchangeable, therefore the type of host computer should be specified when ordering. The S-PACK comes complete with an operating manual and is available for £9.95 plus postage & packing.

**3 in 1 (A)** £7.50

This set of three games for the younger enthusiast includes: Task Force — a strategic battle of sea and air; Demolish — blow your way to freedom avoiding radioactive fall-out and falling masonry as you go; Cosmos — where you have to defend the earth from an invading battle fleet.

**Ed-master** £12.95

This program uses the quiz format, combining the element of fun with educational teaching. 160 questions may be programmed by the teacher divided into eight subject areas of 20 questions each. Questions and answers can be changed as often as you wish. The computer will tell the teacher whether or not, but cheating is prevented as pupils cannot access the program to find out the correct answers. The scores of up to 40 pupils are stored in the quiz memory and easily recalled for comparison.

**Snaill Trail** £4.95

Help the snail escape from the maze he's fallen into before he starves to death. There are two skill levels to this cassette.

**Database** £12.95

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**AT LAST!! A worthwhile peripheral**

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**INTERBEEB**

The self-powered INTERBEEB is a nugget new peripheral, housed in a neat thermo-plastic case the INTERBEEB contains the following hardware to allow your computer to control the outside world... and get an answer without having to re-invent the wheel.

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2) 4 high current relay outputs 3) an 8 bit input port and a separate 8 bit output port.
4) switch inputs.
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The unit comes complete with all the necessary cables, a mains power unit and a manual giving examples for beginners, all for £9.95 + postage and packing.

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The INTERSPEC gives users of Sinclair computers the same facilities for control and interrogation of the outside world as the INTERBEEB and with the advantage of the DCP bus connector, which presents all the necessary bus connection allows communication with other units in the DCP range.

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the next RD or WR signal, when the next program step appears on the displays.

"Break point" operation is selected by S2 on "BK". Now, a "low" can only appear on IC14 pin 6 to set IC13a and stop the processor if IC14 pin 5 and IC14 pin 4 are both high. This will happen only if the processor is performing a read or write operation, and the address bus bit pattern matches that on S3–18. When this happens, comparators IC12, IC11, IC10, IC9, will all give "=-" outputs, producing a "high" on IC15 pin 6, giving the required "high" on IC14 pin 5.

If "RUN" is selected by S2, IC14 pin 5 is held low, so, after pressing "GO" IC13a cannot be set, IC13b cannot be reset, and WAIT is held high. S19 selects 5V supply from either the system 5V rail, labelled "Sys. 5V." on the diagram, or from an external, separate supply, labelled "Ext. 5V."

CONSTRUCTION

All i.c.s and displays are in sockets on my prototype (see photograph) mounted on matrix board, and connected by the "Vero" or "Roadrunner" pen wiring system. The technique is based on a "wiring pen", carrying a spool of fine, polyurethane insulated wire, which emerges from the tip. Using the pen, wire is connected from pin to pin of i.c. sockets, along "wiring combs" which hold the wires neatly. Subsequently, connections are soldered, using a very hot (800°F) soldering iron which melts the insulation and solders the joint at the same time. A very neat, high density circuit board results, but the wiring must be systematic.

It was decided to present a p.c.b. layout for this article, which, although is less compact than that which can be achieved using the prototype approach, does allow an easier and neater approach for the less experienced. The p.c.b. and its component layout is shown in Figs. 2–4.

A MONOSTABLE may be used as a versatile frequency divider, as in the circuit shown in Fig. 1.

Here the monostable is triggered by the positive edge of a signal applied to the B input. The R/C timing components are chosen so that the monostable will time-out in the centre of the positive half of the number of cycles that it is being divided by. So that in a divide by three situation, such as this the output will time-out in the centre of the positive half of the third cycle of the input (Fig. 2). This provides enough leeway to allow for timing drift whilst maintaining an adequate duty cycle for jitter-free operation.

This circuit will divide an incoming waveform by any integer up to a practical maximum of eight. The waveforms shown illustrate the circuit in operation for a divide by three.

P. Thompson, Glasgow.

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Articles submitted for publication should conform to the usual practices of this journal, e.g. with regard to abbreviations and circuit symbols. Diagrams should be on separate sheets, not in the text.
THE TRANSPUTER
A COMPONENT FOR THE FIFTH GENERATION

R.W. COLES

O VER the last ten years or so we have witnessed an exponential rise in the performance of microprocessor chips. Four bit processors rapidly gave way to eight bits, then sixteen, and now manufacturers are jostling for position in the race to introduce thirty-two bit devices which promise to bestow the power of a mini-computer to the most humble office and domestic applications well before the end of the decade, the new Sinclair Quantum Leap (QL) being a fine example both in name and computing capability. Clock speeds have increased from a few hundred kHz to several MHz, and already 25 MHz has been promised for advanced versions of devices now in production. To make all this possible, semiconductor manufacturers have been shrinking the geometries of the individual active components on the chip so that line widths of only one micron (10^-6 metres) will soon be routine, and up to one million components will be possible on each chip.

An uninformed statistician could no doubt analyse these trends and draw elegant graphs which would probably predict that by the year 2000 the average home computer would have a 512 bit word size, a clock speed of 1 GHz, and would contain a CPU chip with one thousand million active components using line widths of one hundredth of a micron. A similar exercise carried out at the zenith of railway development would probably have predicted that by now, every house would be on a branch line carrying Mach 2 locomotives. A prediction which, fortunately, has not been fulfilled due both to a strictly limited need for such travel facilities, and to the development of other more convenient forms of travel which have, to some extent, made railway travel obsolete.

Similar limitations apply to microprocessor development. There is no real need for word sizes much beyond 32 bits, and computing capability. Clock speeds have increased from a few hundred kHz to several MHz, and already 25 MHz has been promised for advanced versions of devices now in production. To make all this possible, semiconductor manufacturers have been shrinking the geometries of the individual active components on the chip so that line widths of only one micron (10^-6 metres) will soon be routine, and up to one million components will be possible on each chip.

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Similar limitations apply to microprocessor development. There is no real need for word sizes much beyond 32 bits, and although we may get as far as 64 bits for some specialised applications, we will soon see this particular growth curve flatten out. As to shrinking chip component geometries, unfortunately this fundamental route to growth will soon be up against limits set by the physics of semiconductor materials and the resolution available, even theoretically, from the lithographic process used in chip manufacture. Clock speeds too, are unlikely to go much above 100 MHz.

One of the few remaining routes to growth will involve the eventual production of larger chips, using the so-called wafer-scale integration technique, but this process is more likely to be used for building complete systems which include lots of memory and I/O, than it is for the creation of bigger and better microprocessor devices. So, are we about to witness the end of the microprocessor revolution? Not if Inmos have their way!

The real root of the problem is that nearly all current computers and microprocessors use the same conceptual approach to data processing, an approach which relies on a single, central, processor, which can run only one program at a time. This concept is so fundamental to our thinking that in the constant deluge of microprocessor enhancements and developments, we hardly even notice that all the “new” devices are based on exactly the same basic principles; principles which were in fact laid down as the bed-rock of digital data processing way back in the nineteen forties. This so-called Von Neumann approach to computer architecture has served us well, but the limits to growth we have already examined will ensure that it will eventually have to be replaced by something radically different, and one of the first attempts to formulate a new approach has come from the British based semiconductor manufacturer, Inmos.

INMOS

Inmos, you may recall, was set up by a group of expatriate British chip designers based in the USA with the help of massive financial backing from the good old British taxpayer. For once, our money was not used to subsidise or prop up ailing industries within the UK, but was instead bet fairly and squarely on the roulette wheel of international semiconductor development, an enterprise renowned for its high stakes, high risks, and high pay-offs for the winners.

Inmos was not set up to be a half hearted “me-too” semiconductor house to second-source other manufacturers’ successful products. From the outset it was planned and organised to become just one thing: a market leader. To begin with, Inmos concentrated on the memory market, introducing a string of innovative devices which quickly established its reputation as a supplier of the fastest memories available. Its first products, the 1400 series of 16K static RAM chips, were designed in the USA and launched on a receptive world in 1981. Since then, Inmos has built a new manufacturing facility in South Wales and has introduced a family of high speed 64K dynamic RAMs which will assure them a secure place among the memory leaders.

While building up its capabilities in the specialist memory area though, Inmos has not forgotten other aspects of system design, and has been very busy at its second design centre in Bristol working on the development of a show-stopping new microprocessor concept, which, if it succeeds, will change the
whole face of digital data processing as we know it today.

Inmos itself does not use the word "microprocessor" very often when describing its new processor. Instead, the new term "Transputer" (which is a contraction of Trans(istor) and (com)puter) has been coined to underline the expectation that its new devices will become universal components, used together in large quantities just as transistors are today.

**TRANSPUTER**

The first Transputer product, the T424, is a 32 bit microcomputer with all the resources normally required by a computer system, including processor, memory and communications, all available on a single chip of silicon containing 250,000 separate active devices. The first T424 devices are not planned for release until late 1984, but in view of the radical design and programming concepts involved, Inmos have wisely decided to "launch" the Transputer concept early so that potential users can become familiar with its capabilities. No doubt the need to raise further funding to complete development also figured in the decision!

The basic architecture of the T424 is shown in Fig. 1, and at first sight there is nothing particularly remarkable about it, except perhaps the ambitious scale of the device with a 32 bit processor, memory, and I/O all on one chip. The most important features of the Transputer though, are not to be found in its sheer size (or lack of it), but are more intimately related to its communications links and its simple, even primitive, instruction set.

The Transputer is not designed, as most other processors are, to be the Prima Donna of a microcomputer system, sitting in the centre of a large supporting cast of memory and peripheral devices. Instead, it is at its best when used as part of a team of other Transputers, all tightly coupled and working closely together to increase processing power and system throughput.

Despite this unusual propensity for team-work, a Transputer can be used alone like a conventional processor if required, and many of the initial applications for this device will probably use it alone or in small numbers, if for no other reason than that it will initially be quite expensive. Later, as prices fall and as other processors run out of steam in the continuing race for higher performance, the building-block capabilities of the Transputer will enable powerful data processing systems to be built up on a single circuit board containing tens, or even hundreds, of separate T424 chips, all working in concert. Furthermore, when the wafer-scale integration technique mentioned earlier becomes a practical reality, large arrays of Transputers can be interconnected directly on a single wafer of silicon to create, for example, a processing engine for the supercomputers of the so-called fifth generation.

As can be seen in Fig. 1, the T424 is unusual in having six separate interface channels on the chip. The memory interface is a 32 bit, multiplexed address/data channel with a 25Mbytes per second bandwidth, able to access up to four gigabytes of external static or dynamic memory at very high speed. The 32 bit address range includes the 4Kbytes of 50ns static RAM, and the Transputer is used as a jelly-bean component in an array, this may be all the memory required to hold both instructions and data. Even in array applications however, there will probably need to be at least one Transputer with access to a large conventional memory array holding the main operating program and the data base.

The peripheral interface is unusual in that it is separated from, and can act concurrently with, the memory interface to access standard peripheral devices such as I/O processors and controllers at high speed, while normal external memory operations take place at the same time. At 4Mbytes per second, the bi-directional peripheral interface is no slouch, and can even be used to perform block memory transfers (from ROM for example) if required.

Finally, and most importantly, there are four bi-directional serial communications channels which can also operate concurrently with each other and with the memory or peripheral interfaces. A collection of four serial interfaces would be of benefit to any microprocessor of course, but the serial channels on the T424 are not intended for traditional and mundane tasks such as driving printers or Modems. These serial interfaces are provided purely as inter-Transputer communication links, and with four available, a two dimensional array of Transputers can easily be constructed with tight coupling to neighbours in the up, down, left and right directions. Each inter-Transputer link can transfer data at 1.5Mbytes per second in both directions simultaneously, using a byte organised message format which can transmit data blocks of any length for memory to memory or CPU to CPU communications. The use of a serial protocol and separate links for each channel has obvious advantages over the shared parallel bus approach used by other inter-processor communications schemes, simplifying board layout and increasing the overall communications data rate by facilitating the simultaneous operation of multiple links in each system.

The on-chip memory array uses the much vaunted high-speed static memory technology already in use in other Inmos products to achieve an impressive 50ns cycle time with separate access ports for the CPU, the peripheral interface, and all four of the serial channels.

The CPU itself is a very fast 32 bit parallel processor which can execute most of its instructions in just 50ns. The CPU utilises the "Reduced Instruction Set Computer" or RISC approach, having only 70 instructions in all, and keeping data access operations separate from logical or arithmetic operations. This approach avoids the usual requirement to cater for multiple combination of data types and addressing modes which often cause the total instruction sets of more conventional microprocessors to mushroom to many thousands of variations. Despite the simplicity of the RISC approach however, Inmos
CONCURRENCY
As we saw earlier, current computer architectures are based on the historical premise that the processor is more expensive than the memory which serves it, and this has resulted in the “Von Neumann bottleneck” which puts constant emphasis on improvements to the central processing “engine” for the achievement of increased performance. With the coming of VLSI (Very Large Scale Integration) this economic perspective no longer holds true, and perhaps even more significant, the performance which can be squeezed from a single processor is fast approaching a physical limit. It is therefore time for the “railway-engine” approach of the all-powerful Von Neumann architecture to give way to the “private-car” approach of multiple, concurrent processing activity. This approach is at the very heart of the Transputer concept.

Unfortunately, the tangled infrastructure of today’s data processing methodology, including all the high level languages such as BASIC and PASCAL, caters only for the Von Neumann approach to computer design, making the re-education burden now shouldered by Inmos all the more daunting. Realising the problems they would face in overcoming the inertia inherent in such an ingrained methodology, Inmos wisely recognised that simply presenting the world with a revolutionary piece of new hardware would not be enough to effect any change. To back up their Transputer they needed to introduce a new software approach to handle concurrency, and to satisfy this need they have developed a brand new computer language called Occam after the fourteenth century philosopher who first formalised the concept known as “Occam’s razor” which in a nutshell states: keep it simple!

Occam and the Transputer operate hand-in-glove to implement what is known as the “process model” of computing as illustrated in Fig. 2. A process is an independent sequential computation, complete with its own program and data, which can communicate with other processes executing at the same time. Communication between processes is by message passing using explicitly defined channels which may either be implemented using physical links (such as an inter-Transputer serial channel) or by using software organised channels using memory buffers as the link. Communication between processes is synchronised so that a message can only be sent over a channel when both the sender and receiver are ready, and as a consequence, the process which first becomes ready must wait for the second process before the link is completed.

The Transputer directly implements the Occam model of a process to the extent that internally it can behave like any Occam process which is within its capability. In particular, a Transputer can implement internal concurrency by timesharing processes using the instruction set facilities provided directly for that purpose, and can implement external concurrency by using its inter-Transputer links for message exchange with processes running on other devices. As a result, the same Occam program may be executed either by a single Transputer, or by a whole network, with consequent gains in performance.

OCCAM
The Occam language is a high level language when judged against conventional criteria, but it is also the lowest level at which a Transputer will be programmed. The instruction set of the processor is not pure Occam however, and represents a somewhat more primitive level of operation which is optimised for direct compilation from Occam itself. Direct use of the Transputer instruction set is not supported, and no assembler will be available, because compiled Occam will be at least as efficient as a hand coded alternative.

Occam may have been developed specifically for the Transputer, but it is not limited to use on that processor and software development tools are already available to facilitate its use on a number of other systems including the Apple II, the Sirius, and the IBM PC. Although practical working Occam software can therefore be developed for other processors, the full potential of the language will not be realised until the Transputer itself is in widespread use.

Even the Transputer, though, is not limited to the use of Occam alone, since its instruction set has also been optimised for efficient compilation from other high level languages such as PASCAL, ADA, and even BASIC. As a result, the Transputer programmer may use Occam alone to take advantage of its efficient handling of concurrency, or may simply use it as a harness to link software modules written in other high level languages which may be better suited to certain types of data processing task.

CPU ARCHITECTURE
The Transputer CPU architecture (Fig. 3) over turns many of the old established concepts of “desirability” which have been preached in the PE Microfile series and elsewhere. An array of general purpose registers is nowhere to be seen, there is no stack.
in the conventional sense, and the long sought after concept of virtual memory addressing is ignored. The reason for this upturned apple-cart, however, is not hard to find.

Take a look at any conventional 16 or 32 bit microprocessor and you can see the lengths to which chip designers have had to go to squeeze the ultimate in performance from their Prima-

Donna processor. Every conceivable useful concept and add-on hardware extra has been included to overcome the restrictions which result directly from the Von Neumann bottleneck. As a result, data manuals are getting thicker, and learning a new processor has become a time-consuming business for both the hardware designer and the programmer.

A Transputer system, on the other hand, is not constrained by the single CPU bottleneck, and as a result “Occam’s razor” can be applied to the processor architecture to keep everything as simple as possible. Unlike other microprocessors the Transputer does not have a large register file, instead, it has a minimum set of functionally dedicated registers and an evaluation stack. This approach simplifies compiler design since all of the operands are in a uniformly addressed data space. It also minimises the context switching time required for interrupts by eliminating the need to save lots of registers on a stack. This in turn reduces the time overheads involved when executing concurrent processes and improves the real-time response of the system.

A sequential process is executed using just six registers, each one word long, or 32 bits for the T424. This register arrangement is also shown in Fig. 3, and is the ultimate in simplicity.

The instruction pointer defines the next instruction to be executed, and is therefore what we generally call a program counter, the operand register is used in the formation of instruction operands, and the workspace pointer defines an area of RAM memory where local variables are held. Programmers never have to refer to these registers directly since their function is implicit in any instruction which uses them, as is the function of the remaining three registers together forming the evaluation stack.

The evaluation stack operates in a similar way to the stack used in the famous Hewlett Packard range of scientific calculators, and anyone who has learned to use one of those would never swap it for the messy algebraic notation used by most of the competition. Expressions are evaluated on the three entry stack, and instructions refer to the stack implicitly. When an Add instruction is executed for example, the top two values in the stack are added and their sum is placed on the top of the stack. The use of an evaluation stack removes the need for

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instructions to continually respecify their operand locations.

Also implemented in the CPU logic is a hardware scheduler which enables any number of concurrent processes to be executed together and to share the processor time in a controlled way. Two process status levels are supported, normal and priority, with the priority classification reserved for processes which would normally be performed using interrupt routines.

If a normal process is being executed and a message arrives from a priority process (over an inter-Transputer link for example), the processor saves the context of the current process in the RAM workspace area and begins to execute the priority process within 2 microseconds. Normal processes will only be resumed when all priority processes are unable to proceed or have been completed. Special instructions are provided to support the concept of concurrent processing on the Transputer.

INSTRUCTION SET

Like the architecture of the Transputer CPU, the instruction set is simple and straightforward, with all instructions being only one byte long. One consequence of this simple approach is the incredible speed of processing which the Transputer can attain, up to 10 Million Instructions Per Second (10 MIPS) when running from internal memory. The very best conventional microprocessors, such as the Motorola 68000, can manage only about 1 MIPS.

Each one byte instruction is divided into two four bit fields:

<table>
<thead>
<tr>
<th>I Byte</th>
<th>Function</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 6 5 4 3 2 1 0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The four most significant bits are a function code, and the four least significant bits are a data or address offset value. There are two basic types of instructions as follows:

One Address Instructions:

These instructions, of which there are thirteen, represent the most common operations performed by a program such as loading or storing one of a small number of variables, or loading a constant. With only four bits available for variable addressing there is clearly no way to access the 4Gbyte memory space directly. To overcome this limitation, the four bits are used as an offset, relative to the 32 bit workspace pointer or to a previously computed 32 bit pointer in the operand register. The basic single address instruction format therefore provides for immediate access to 16 locations in the workspace area and another 16 locations which may be located anywhere in memory. This is considered sufficient for over 80% of memory access operations. When larger offsets are required, the rather unusual approach of using a sequence of instructions to extend the offset by four bits for each instruction can be employed. In effect, memory addresses are frequency encoded which is more efficient overall than the use of a fixed, full width address for every access, even for locations in close proximity.

Zero Address Instructions:

All the remaining instructions use the evaluation stack as the implicit source for operands, and this type can be subdivided into the following classes:—Arithmetic, Logical, Conditional, Data Structure and Process.

The arithmetic operations include multiplication and division, and support multilength and floating point arithmetic with overflow monitoring. The basic division operation, for example, is division of a signed 32 bit number, giving a signed 32 bit result and remainder.

The data structure operations provide the means to access byte and word data structures which may include multidimensional arrays, and enable data structure access to be independent of word length.

The process instructions support the Occam model of processes. They include instructions analogous to the input, output, block move and procedure call instructions of other microprocessors, with the difference that the Transputer instructions are designed to support a well-defined model of concurrency in which all process communication is synchronised.

As mentioned earlier, it is not proposed that Transputer programmers will have access to the basic instruction set, but it is listed here for completeness in Fig. 4. Of more relevance to programmers is the Occam syntax, which is listed in Fig. 5. It is easy to see why the basic machine code instruction set can be ignored in favour of Occam by looking at the “Program Size” column which shows that most Occam statements compile into very short machine code instruction sequences, often of only 1 or 2 bytes.

TRANSPUTER SYSTEMS

So far we have looked exclusively at the 32 bit T424 Transputer which will be the first device to become available in late 1984. A great advantage of the Transputer concept, though, is the fact that many other compatible configurations are...
possible without the need to change the Occam syntax.

Also planned is a 16 bit version, the T222, which will have an identical instruction set and will operate at the same speed as the T424 within the restrictions of its shorter word length. Also planned are specialised Transputer devices such as the G213 graphics processor, and the M212 disc processor which will both be based on the 16 bit architecture of the T222.

The package style chosen for all Transputer products is the ceramic Leadless Chip Carrier (LCC) which is also being used for advanced conventional microprocessors such as the Intel 80286. The T424 will use an 84 connection LCC roughly one inch square (Page 26), while the T222 will use a 68 connection package. All Transputers will be fabricated using a CMOS process and will run from a 5MHz system clock. The T424 will operate from a 5 volt supply and will dissipate only 900mW.

A basic single Transputer system can be assembled with relatively few components as shown in Fig. 6. This simple system is comparable to any other high performance single CPU disc based microcomputer and demonstrates how conventional a Transputer system can be. The two arrangements shown in outline form in Fig. 7 provide a glimpse of the more exotic system architectures which are more likely to justify the use of the Transputer in large numbers. With networks like these available, the age of the truly intelligent supercomputer cannot be far away!

---

**35 LED TACHO**

This circuit uses the MM5451N shift register and I.C.D. driver to provide a bargraph display of engine revs.

The circuit operates as follows: When the output of IC1d is high, pulses are received from the points via IC1a & b which operate as a Schmitt trigger, and are used to clock the shift register—the data input is held high. When the output of IC1d is low the data input is low and IC1e & f provide clock pulses to fill the shift register with zeros—the shift register will not accept any more data after it is full until the data input goes high again. Thus, a number of I.E.D.s are switched on corresponding to the number of ignition pulses received. The display updates every 0.3 seconds.

The IC1a & b clock should be set to 3.33Hz for a four cylinder engine (5Hz for a six- and 6.67Hz for an eight-cylinder engine). This gives a maximum reading of 7000 r.p.m. The value of capacitor C2 may need to be decreased.

C4, 5 and 6 are decoupling capacitors and should be connected as close to the i.c.s as possible. C7 decouples the brightness input which is set to maximum. IC4 provides a stable 5V supply and requires a heatsink.

The MM5450N could be used instead—this only has 34 outputs and a 'data enable' input on pin 23 which should be tied to 0V.

This circuit is suitable for negative earth vehicles.

I. Benton, Bardney, Lincoln.
HAVE never, as a journalist, been much of a scoop-artist. Let others, if they must, spend fruitless nights on the steps of No. 10 in the vain hope that, as the result of a dubious tip-off, they'll nab the PM coming home stoned from a summit meeting. Let others seek to build up evidence that Dean Martin is secretly addicted to lemonade and that Robert Mitchum really lives. Personally I've always taken the authenticated news as it comes.

Yet this philosophy, Kismet being what it is, does not prevent one stumbling across the occasional exclusive. Such a thing happened to me last week when taking a milk and taken the authenticated news as it comes. Mitchum really lives. Personally I've always secretly addicted to lemonade and that Robert

seek to build up evidence that Dean Martin is tip-off,

the vain hope that, as the result of a dubious

I

classics. The fact that it was eventually super-

functions, from the liquidisation of solids to

without memory—were planning to mark the 100th

of senior engineers—long in both tooth and

August 1982 when an article appeared in a

honey in one of the better class bars with

flapped untiringly for the best part of an hour

reduced in my mind to the status of bungling

here nor there. The seed of multi-function

a forest in a matter of minutes—is neither

keys to playing simulated versions of the light

revolution in the electronics industry in a flip-

But Gummidge and Goldblatter—whose

Talking of cooking, 'Manservant' includes,

perhaps the most exciting feature is a

but not only to our very own Prestel, but also to

sophisticated data processing unit and inputs

Not so fast, the one obstacle to its universal

from the lapels of sloppy diners. A shoe-

and trouser pressing—a full

bachelor

and fixed abode. MAC: What you leave at

News readers on diets. Addressability: The

shortly be using to pay our life, house and car

polishing unit is an optional extra.

A shoe polishing unit is an optional extra

"Perhaps the most exciting feature is a

stunningly-designed personal helicopter. It

consists of an ultra-lightweight yoke assembly

which, when clipped to the shoulders, enables

the user to cruise comfortably at an altitude

of 50ft at a speed of about five miles an

hour—ideal for getting from shop to shop when
doing your Christmas shopping in Ox-

ford Street. Power is supplied by one of 'Man-

servant's' vast range of modules. Controls, set

in a chest-mounted panel, are no more com-

plicated than those of a basic gas cooker.

Talking of cooking, 'Manservant' includes,

as well as a super high-speed microwave oven,
a subsidiary unit, tentatively named 'Maid-

servant', which will peel potatoes, slice meat,

shred cabbage, skin onions, dice carrots and

turn out an acceptable strawberry mouse.

It can even handle the washing-up and serve

coffee and bran.

'Manservant', let it be made clear, is no ill-

chosen name. For the lonely and helpless

bachelor it will handle—including ironing

and trouser pressing—a full 14lb load of

washing and, if needs be, remove soup stains

from the lapels of sloppy diners. A shoe-

polishing unit is optional extra.

These are but a few of the blessings—there

are many more too numerous to be mentioned

here—which in the near future will enrich

the lives and increase the leisure of those of us

fortunate enough to have been born in the

electronic age. The fact that the complete

'Manservant' unit packs compactly into a

carrying case the size of a piano accordion is

a consideration not to be sneezed (or should it

be squeezed) at.

'manservant', if and when available in the

UK, would rank in price with a seven-

bedroom, two-bathroom, double-garage,
centrally-heated family house standing in six

acres in the stockbroker belt of South-East

England. Maybe some enterprising building

society will come up with a 'Manservant'

mortgage scheme.

In the meantime, the US consortium can-

not afford to be complacent. A state research

establishment, sited in the bowels of a defunct

volcano on the shores of the Black Sea, is

already working on a Soviet version called 'Dogsbodya'.

The race, then, will be to the swiftest.

You may recall that I recently drew atten-

tion to the plight of the middle-aged engineer

who couldn't come to terms with modern

technology. In particular he was bugged by

the new gobbledygook which is so cruelly dis-

figuring the noble English tongue.

Since then I've been reflecting upon his

distress and I've come to the conclusion that I've got a touch of the same trouble. Every day some fresh distortion is thrust upon us. Indeed, I have the feeling that somewhere in

the electronics industry there is a little clique

whose only contribution to progress is to

think up grotesque words and phrases for

foisting upon those who once took a pride in

speaking English as she ought to be spoken.

My view was not changed when there

plopped through my letter-box the other
day—along with some bumph about double-

glazing and a red notice from the Gas

Board—a newly-published glossary of terms

used in Satellite and cable TV.

The document was a revelation. And to

show the extent to which the mists of mutual

understanding have been dispelled, let me

give you some examples of my former inter-

pretations of well-known expressions which

are now being bandied about—with entirely

new meanings—by those in the SCT know.

Tiers: Lacrymical scissions which exude

from the eyes when watching a sick-making

wedding or convenient demise on Coronation

Street. Another form of this condition is
called the Russell Harty syndrome. Premium

Channels: The electronic means we shall

shortly be using to pay our life, house and car

insurance contributions. Narrowcastsers:

News readers on diets. Addressability: The

possibility of communication with anybody

with a fixed abode. MAC: What you leave at

home—because Michael Fish seems such a

reliable lad—and subsequently need.

Scrambling: Something that pilots used to

do during World War II and what housewives

have been doing with eggs ever since the hen

was invented.

(It is the April issue! Ed.)
KMT
The unique new modular enclosure.
Suitable for alarm systems, counters, interfaces amplifiers, model control units and many other projects.

Easy to assemble - just 10 screws.
Easy on the pocket - house your projects economically and professionally.

For full size eurocards (100 x 160mm) mounted horizontally in the 35TE front panel kit.
Half size eurocards (90 x 90mm) mounted vertically included as part of all front panel kits (except 35TE), with connector included.

Hi-Style Desk Top Case
Designed to house keyboards and displays on top of the 11mm silver anodised aluminium panel. The light brown case is manufactured from high impact polystyrene and has a textured finish.

- Casing - High impact textured ABS
- Colour-Brown

This box is moulded in two sections and has a textured finish. The bottom compartment accepts a PP3 or nickel cadmium stack 25 x 45mm. A circuit board 56 x 105mm may be mounted on three pillars in the base, location being provided by a 3mm spigot. The top moulding will accept a circuit board 71 x 107mm.

- Material-Textured ABS
- Colour-Dark brown attached

Hands Held Box
Plastic Boxes
Type A
Plastic boxes consisting of a top and bottom moulding with front and rear aluminium panels, positively retained in the two halves.

- Top and bottom moulding-High ABS
- Colour-Light grey top: dark grey base
- Front and rear panels-Satin anodised aluminium 1.6mm thick.

Type B
Constructed of high impact polystyrene, these handsome two-toned grey boxes are suitable for wall mounting and free standing instruments.

- Material-High impact polystyrene
- Colour-Top light grey: base dark grey
- Panels-Satin anodised aluminium

Send £5 for a copy of the catalogue with details of the full range available.

ULTRA VIOLET BLACK LIGHT FLUORESCENT TUBES
20 watt £4.75 25 watt £5.25 (5% inc. VAT)
30 watt £8.95 45 watt £10.95 (5% inc. VAT)
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200 watt £95.00 500 watt £200.00 (5% inc. VAT)
300 watt £250.00 1000 watt £625.00 (5% inc. VAT)
400 watt £625.00

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230V A.C. 240VA 90W 120VA 150VA 220VA 300VA 440VA 660VA 1000VA 1500VA
115VA 220VA 380VA 550VA 820VA 1230VA 2000VA 3000VA 4500VA 6000VA

EPROM ERASURE KIT
17.8 watt 2537 Angst Tube. Ballast unit.
Price £13.00 inc VAT & P&P
Includes test leads.

FROM STOCK AT PRICES THAT COMPETE!

AC GEARED MOTORS
DC GEARED MOTORS
MICROSWITCHES
RELS
REED SWITCHES
SOLENOIDS A.C. or D.C.
PROGRAMME TIMERS
MOTORS

Phone in your enquiries
Stockists for Frenchman paint and Waxoyl products. Good normally dispatched within 7 days.
UK101

Sir—This program will display an enlarged character set on the UK101 in which the full ASCII upper case character set may be displayed. The program will ask you to input your message. This is stored in N$ and may contain any upper case ASCII character. To start a new line use CONTRL N. The space bar inserts a space between characters. The display is 9 character wide by 5 high on a 32 line screen. For a 16 line screen the variable TX should be 54272. The character definitions are stored in AS(J).

P. N. Martin,
Weymouth.

170 REM**** READ IN THE CHARACTER DEFINITIONS
180 READ AS:IF AS<"0" THEN NC=NC+1:GOTO180
190 RESTORE:DIM AS(NC-1)
200 FOR 1=0 TO NC-I:READ AS(1):NEXT
210 READ AS:J=0
220 READ CH(J):IF CH(J) THEN J=.1 + I :GOT0220
230 T0=53261:TX=55296:REM**** START AND FINISH OF DISPLAY 32 LINES
240 A=ASC("A"):Z=ASC("Z")
250 ZE=ASC("0"):NI=ASC("9")
260 PRINTCHR$(26);:REM" CLEAR SRCREEN CEGMON
270 INPUT "Message"; INS
280 PRINT CHR$(26);:TI=T0:TL=T0
290 FOR T=1 TO 6:PRINT::NEXT
300 FOR I=1 TO LEN(INS):REM ** EXTRACT THE CHARACTER TO BE DISPLAYED
310 CH=ASC(MIDS(INS,I))
320 IF CH=Z THEN360 REM IF NOT SPACE THEN SKIP
330 FOR T=1 TO 6:PRINT:NEXT
340 T1=T+384:IF T1>TX THEN TI=TX
350 D1=T-T1:GOTO480
360 CHS=ASC(CH-32):REM EXTRACT THE RELEVANT DEFINITION STRING
370 FOR J=2 TOLEN(CHS)
380 C=161

390 C0=ASC(MIDS(CHS,J))
400 IF C0=A AND C0<Z THEN430
410 J=J-1:IF J<LEN(CHS)THEN390
420 GOTO470
430 Y=INT((C0-A)/5)
440 X=C0-A-5Y;
450 POKE TL+X+Y,64,C
460 NEXT J
470 TL=TL+ASC(CHS)-ZE+1
480 NEXT I

500 REM**** DEFINITIONS OF CHARACTERS, ARRANGED IN ASCENDING ASCII

510 REM* VALUE, STARTING WITH ASCII SPACE
520 DATA 40A
530 DATA 1AFKU
540 DATA 3AC
550 DATA 45A6B5C6DFGHI5K6L5M6NPQRS5U6V5W6X
560 DATA 4DCBAFK3KL2NS4X
570 DATA 41D1H4I5L4M1N2O3P4Q5R6S7T8U9V
580 DATA 43X6SR2ML2G3F1AB2C
590 DATA 4CH5IU4VW
600 DATA 41D1H4I5L4M1N2O3P4Q5R6S7T8U9V
610 DATA 42D1F3G4H2I5J6K7L8M9N0P1Q2R3S4T5U6V7W
620 DATA 4ABCD4I1H2L3M4N5O6P7Q8R9S0T1U2V3W4X
630 DATA 41D1H4I5L4M1N2O3P4Q5R6S7T8U9V
640 DATA 41D1H4I5L4M1N2O3P4Q5R6S7T8U9V
650 DATA 41D1H4I5L4M1N2O3P4Q5R6S7T8U9V

Practical Electronics  April 1984
Let there be light!
And let it remain whilst we are grappling with our seat belts.

This circuit, for a car interior light delay switch, is designed for permanent addition to the car wiring system without having to break any wires in the existing harness. Other features include low quiescent current consumption—less than 100µA, solid state switching, and an abort facility if the door is reopened during the timing cycle.

The circuit is designed around the popular CMOS 555 timer package. Although the bipolar device may be used as a direct substitute, the quiescent current consumption will rise to about 4 mA. The device is suitable only for NEGATIVE ground vehicles with a +12 volt battery supply and with ground line door switches.

The design is economical in that costly electromechanical devices such as relays are eliminated through the use of semiconductor switching. Samples of the design have been fitted to British and foreign cars, and they have shown total reliability over a period of six months.

Typical cost of the components involved is about £3, exclusive of the printed circuit board or Veroboard, and the wiring connectors.

CIRCUIT DESCRIPTION

The CMOS 555 is wired as a monostable or "one-shot". The length of the on period is determined by R4 and C3. Capacitor C3 should be a low-leakage tantalum capacitor to ensure good timing consistency. The timing period is determined by the following formula:

\[ T = \frac{1.1 \times R \times C}{R_{\text{mohms}} \times C_{\text{µF}}} \]

In the circuit illustrated:

\[ T = 1.1 \times 1 \times 10 \text{ seconds} = 11 \text{ seconds} \]

Desired variations in the timing cycle may be made using the formula above, bearing in mind the limited availability of high value low leakage tantalum capacitors at the specified voltage. Also, the value of R4 should preferably lie between 3k3 and 10M.

Diode D1 is a polarity protection diode in the positive supply line. Resistor R1 and capacitor C1 provide smoothing and filtering of the supply line.

OPERATION

Whilst the car door is shut, S1 is open and the circuit is in its quiescent state. If the door is opened, S1 closes and the interior light comes on, but the circuit remains inactive since pin 4 (Reset) is momentarily held low through D2 to ground, disabling the timer. When the door is closed S1 opens, pin 4 goes high via the pull-up resistor R5—there are now two diode drops to ground, D2 and transistor TR3. At the same time a positive pulse appears by way of R8 at the base of TR1. This pulse is blocked by D2 which is forward biased so pin 4 is not affected. Transistor TR1 is a switch and also an inverter so the pulse which now appears at the collector of TR1 is negative going. This negative pulse is a.c. coupled by C2 to pin 2 (Trigger) of the 555, and initiates the timing cycle. Pin 2 is returned to rail voltage by the resistor R3. Resistor R2 supplies the collector of TR1. Any further pulses arriving at pin 2 are ignored during the timing cycle unless the cycle is aborted and reset.

As soon as the timing cycle begins, the output from pin 3 goes high, turning the solid state switch, transistors TR2 and TR3 fully on and shunting the switch S1 so that the interior light remains on for the duration of the timing cycle.

Transistors TR2 and TR3 are a made up complementary Darlington pair in order to reduce the total Vbe to one diode drop, that is, to about 0.7 volt. An n.p.n. Darlington, which is available as an on-chip device would have added offset voltages of about 1-4 volts causing a decrease in lamp brightness. If this is tolerable then an n.p.n. device such as the ZTX 600 may be used. R7 and TR2 and TR3 are omitted and the ZTX 600 is used in place of TR2, R7 being replaced with a wire link.

---

Fig. 1. Full circuit diagram
Transistors TR2 and TR3 are silicon devices, so the base of TR3 would provide an adequate collector current for TR2. However, for peace of mind R7 is included to ensure that TR2 operates correctly.

When the delay period is over, pin 3 goes low, snapping off TR2 and TR3 extinguishing the interior light. If the door is opened during the delay period, a negative pulse arising from the closure of S1 passes through the diode D2 to the reset pin 4 of the 555 pulling it below its operational voltage and aborting the timing cycle. Thus every time the door is opened and closed a complete delay cycle occurs regardless of the state of the circuit.

CONSTRUCTION

A printed circuit layout is shown in Fig. 2, and a component overlay is shown in Fig. 3. Alternatively the circuit may be built on a small piece of stripboard. If the bipolar 555 is to be used then a 10n capacitor (C4) should be connected from pin 5 to ground. It is omitted if the CMOS 555 is used.

All the resistors are soldered in place first, followed by diodes and capacitors—observe polarity! The use of a socket is recommended for the integrated circuit. Finally, solder the three connecting wires in place.

Insert the 555 correctly in its socket. Although CMOS devices can be damaged by static discharge, they are usually robust enough to withstand normal handling. However, the device should be removed if any soldering "afterwork" is to be done. Also the i.c should neither be inserted nor removed from its socket whilst the circuit is connected to a power supply.

The circuit may now be added to the car wiring system. Scotchlok connectors are useful at this stage (available from motoring accessory dealers), or spade connectors can be used. It is a good idea to disconnect the car battery whilst wiring up. It is also worthwhile to add an in-line fuse in series with the positive line—the lowest value fuse available will do. Reconnect the battery and operate the car doors to check for correct action.

Two, possibly three 6 watt lamps may be operated with this circuit. If it is required to operate more lamps then a "beefier" transistor must be used in place of TR3, possibly with a heatsink. A BD14O or a PNP 3055 may be used, mounted on a small piece of aluminium, away from the circuit board. The circuit board itself may be mounted in a small box, or bolted to the car metalwork with spacers or brackets, or merely wrapped in stout plastic and wedged in the wiring loom.
THERE are many instances in electronic circuitry where analogue voltages must be compared with each other. The conventional way to implement this is to use a comparator with a differential input stage. If one of the two inputs is higher in voltage than the other, the output is at a 'high' level, and if the reverse is true, then the output becomes a 'low' level.

In many cases, however, a simple comparison of two voltages is insufficient. We may wish to know if a voltage lies within a certain range, and if not, whether it is above the top limit of that range, or below the bottom limit. The range of voltage in question is known as a 'window', and if not, whether it is above the top voltage limit or below the bottom limit. Either comparator turns on, the input signal is deemed to be outside the window. The complementary output of comparator A is that derived by an inverter, is that the output is turned Off.

OPERATING MODES

There are actually two window inputs to the comparators, one defining the centre of the window, and the other defining the width of the window. The voltage $V_c$ at pin 9 is added to the voltage $V_e$ at pin 8 and fed to comparator B, but is subtracted from $V_e$ before being fed to comparator A; the difference between the voltages fed to the comparators is therefore the full window width. This allows the i.c. to be used in two different modes, as shown in Figs. 3 & 4. The limits mode shown in Fig. 3 is the simpler of the two. The comparator is therefore the full window width. This allows the i.c. to be used in two different modes, as shown in Figs. 3 & 4. The limits mode shown in Fig. 3 is the simpler of the two. Here, the resistive divider $R_1$, $R_2$, and $R_3$ sets the upper and lower window limits at pins 6 and 7. Although $R_4$ and $R_5$ are shown setting a half window width voltage at pin 9, this would only rarely be used in the limits mode, and would normally be set near to 0 volts. Hence, the voltage at pin 8 is directly compared with the voltage at pins 6 and 7. The results of this comparison are presented at pins 2, 3, 13 and 14, as shown.

In the window mode of Fig. 4 we provide the limit conditions in a rather different way. The voltage at pin 8 set by $R_1$ and $R_2$, defines the centre of the voltage window, and the voltage at pin 9, set by $R_3$ and $R_4$, defines the half window width. This mode is especially useful when the window remains constant in width, but needs to be 'tuned' in its position, i.e. its centre voltage. Pins 6 and 7 are commoned and fed with the input signal. Because this input signal is now being fed into the op-
positive comparator inputs to those used in Fig. 3, the output polarities at pin 2 and pin 14 are reversed; pin 2 is now the 'above' output, and pin 14 is the 'below' output.

**Voltage Reference**

Although resistive dividers between the supply rails can be used to set the various limit or window voltages, this is not usually a very accurate arrangement due to the possibility of supply voltage variations, noise, etc. The TCA 965 has an internal reference voltage generator to help overcome these problems. Fig. 2 shows the arrangement of this generator. A 3 volt reference voltage is amplified by a non-inverting amplifier. R1 and R2 set the gain at x2, so the voltage \( V_{\text{stab}} \) at pin 10 is nominally 6 volts. This voltage can be changed, however, by connecting external resistors between pin 5 and 0 volts, or between pin 5 and pin 10. To stabilise the output voltage, a 10µF electrolytic capacitor must be provided between pin 10 and 0 volts, as close to the i.c. as possible. Up to 10mA is available from this \( V_{\text{stab}} \) output.

**Applications**

Because of its very flexible internal configuration, this i.c. lends itself well to a whole myriad of applications. It can be run from supplies as low as 4.75 volts, enabling its use within 5 volt logic systems, yet can also handle supplies of up to 27 volts. The main outputs (pins 2, 3, 13 and 14) can each sink up to 50mA current from a load, enabling the direct driving of relays, lamps, l.e.d.s, etc. Be cautious, however, with the input voltage range which the i.c. will work normally with; on pins 6, 7 and 8, this is defined as 1.5V to the positive supply less 1 volt. The upper limit should present no problems, but the 1.5 volt lower one might limit its usefulness in some situations.

The TCA 965 will be an obvious choice in many system control applications. The window can be configured as a 'dead space' between a control turning on and turning off again, and as such the i.c. is ideal for use with temperature control systems, providing a flexible and easily defined hysteresis. The other main area of use is within measurement systems, setting limits of acceptance on incoming d.c. values. For example, coupled to a simple analogue measurement system it could
PLANT WATERING METER

To illustrate the basic principles of use of the i.c., Fig. 5 shows a simple plant watering meter, loosely based on the front end of the moisture meter described in Semiconductor Circuits last September. IC2a forms a square wave oscillator with a frequency of approximately 2.8kHz. This is a.c. coupled via C2 to the plant pot with water. As soon as the soil became wet enough, the pump would turn off again.

Fig. 6 shows the Veroboard layout for this circuit. The probes can be made from stiff copper wire glued inside old ball-point pen cases. The components specified have been deliberately chosen to be very small devices, so can be used in plastic cases. The components specified have been deliberately chosen to be very small devices, since the aim was to get the size down as far as possible, so ¼ watt resistors, or ½ watt, should be used throughout to be consistent with this. In use, adjust VR1 to give the correct reading for your preferred moisture level, or change R10, R11, and R13 to give an even greater range of possible settings. IC2 is a dual op-amp of the 741 type, so almost any similar device would suffice. Finally, note that diode D1 protects against reverse connection if a battery is being used to supply the current; be extremely careful if a mains-derived supply is to be used, since the proximity of water or moisture could be very dangerous indeed.

Although this applications circuit, it does demonstrate the great versatility of the TCA 965, which should find considerable use in the field of analogue control and measurement.

The TCA 965 is available from Electrovalue Ltd, 28 St Jude's Road, Englefield Green, Egham, Surrey.

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BLOCK CAPITALS PLEASE

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This circuit allows four momentary action switches to be used as a push button bank, whereby the last button operated is latched electronically, and if another button is operated, its output supersedes. This of course may be achieved mechanically as indeed it is; however, mechanical switch banks do not guard against more than one switch being operated at the same time. This may prove disastrous in say motor control systems, as if Forward and Reverse were operated simultaneously something would have to give. This circuit is automatically reset if more than one button is operated at the same time. The circuit was originally designed for a logic controlled reel to reel tape deck for the function keyboard, so that say 'play' and 'rewind' pressed at the same time would not result in ten yards of tape on the floor and a pair of smoking motors inside the deck.

The switches are debounced using S-R latches formed around IC1, 2 and 3. The outputs which are normally high go to a falling edge detector formed around a Schmitt trigger in IC4. The outputs of these are commoned via diodes so as to give a short pulse every time a switch is operated. This strobes the latches.

The outputs of the debouncing latches which are normally low, go to IC5, the heart of the circuit. IC5, a 4514, latches the binary input when strobed, and converts it into a one of sixteen output. As the inputs are connected each to a binary input pin, if one switch is pressed, the appropriate '1', '2', '4' or '8' output latches high. If, however, more than one switch is pressed simultaneously, a binary input other than 1, 2, 4 or 8 is set up at the input, so another output pin goes high. An optional 'reset' output may be built by commoning all the unused outputs via diodes. Also, an optional 'reset' switch may be added as shown by making it form a non single bit number to appear at the input.

Many variations of this circuit may be designed, including the use of more than one 4514 to give more switch capability. It may also be useful to note that if IC5 is substituted for a 4515, the outputs will all be inverted, as this i.c. uses negative output logic.

G. Durant,
Selby,
N. Yorks.
SEVERAL popular games rely on the toss of a coin to introduce an element of chance when a simple decision is to be made. Furthermore, the teaching of statistics also invariably involves some reference to the probability of obtaining a 'head' or 'tail' when tossing a coin. Students are usually asked to investigate this by repeatedly throwing a coin and noting the outcome on each occasion. The results of a large number of observations are then collated and the probability of a 'head' or 'tail' is verified as being 0.5, or 1:2. Such an outcome is, of course, independent of a previous result, i.e. if tossing a coin five times produces a 'head' on each occasion, there is still an even chance of producing a 'head' on the sixth throw. Since the outcome of tossing a conventional coin is quite predictable, the teacher of statistics may require a teaching aid in which there are similarly only two outcomes (we will dismiss the possibility that the coin might land on its edge) but in which the odds can be loaded in favour of one or other of the states.

This month's Digital Project, therefore, is a device which finds applications in both the classroom and home. The Heads and Tails Generator produces an output consisting of a letter 'h' or 't' displayed on a seven segment I.e.d. indicator. A coin toss is initiated from a momentary push-button; as soon as the button is depressed, the display is blanked but returns a few seconds later to display the outcome. The odds may be weighted in favour of either a 'head' or 'tail', or may be set precisely to an even chance.

CIRCUIT DESCRIPTION

The complete circuit of the Heads and Tails Generator is shown in Fig. 1. IC1a acts as a clock oscillator which produces a square wave of near 50% duty cycle. This stage is followed by an inverting buffer, IC1b, and a further inverter, IC1c. Complementary outputs are derived from these latter two stages and fed to D-type bistables, C2a and IC2b. The clock inputs to the bistables are commoned and fed from the de-bounced switch arrangement formed by IC1d and associated components. This circuit produces a logic 1 on the clock line whenever the switch is depressed. The outputs of the bistable stages, IC2a and IC2b, are fed to the two-input NAND gates, IC3b and IC3a, respectively. These are used to gate the outputs of the bistables to the display such that the outputs of IC3a and IC3b will only go low when their common input is taken high. Readers should note that it is only necessary to make changes to the state of two of the display segments on the transition from 'h' to 't', and vice versa. The remaining unaffected segments are simply wired permanently 'on'. It is, however, necessary to ensure that the whole display is blanked during the period in which a conventional coin is in the air. This is achieved by means of the monostable, IC4, and series pass transistor TR1. This latter device interrupts the positive supply to the common anodes of the display during the monostable timing period.

CONSTRUCTION

The Heads and Tails Generator is built on a single sided p.c.b. measuring approximately 120x70mm, the copper foil layout of which is shown in Fig. 2. The corresponding component layout on the top surface of the p.c.b. is shown in Fig. 3. Interconnection from the p.c.b. to the 5Vd.c. supply is made via a 0.1" matrix p.c.b. connector, the wiring scheme for which is also shown in Fig. 1.

Components should be assembled on the p.c.b. in the following sequence: d.i.l. sockets, p.c.b. connector, links, resistors, capacitors, switch, transistor, and I.e.d display. Once assembly is complete, the underside of the p.c.b. should be carefully checked for solder splashes, bridges between adjacent tracks, and dry joints. Finally, the i.c.s may be inserted in their respective holders, taking care to ensure the correct orientation of each device. Constructional details of the enclosure have not been given since this will undoubtedly be a matter of preference for the individual constructor. A small ABS case will normally be found to be quite adequate in this respect. Constructional details of a suitable
Fig. 1. Circuit diagram of the Heads and Tails Generator

Fig. 2. P.c.b. design

Fig. 3. Component layout
COMPONENTS ...

Resistors
R1  1k
R2  470
R3  4k7
R4  100
R5  10k
R6-R10 270 (5 off)
R11-R13 1k (3 off)
All resistors are 0.25W 5% carbon

Capacitors
C1  22µ 25V tantalum
C2  10µ 16V p.c. electrolytic
C3  220µ 16V p.c. electrolytic
C4-C7 47n ceramic (4 off)
C8  100µ 16V p.c. electrolytic

Semiconductors
TR1  BC548
IC1  7414
IC2  7474
IC3  7400
IC4  74121
X1  Seven segment common anode l.e.d. indicator

Miscellaneous
p.c.b.
Push-to-make p.c.b. mounting switch
14-pin d.i.l. sockets (4 off)
3-way 0.1” p.c.b. plug and socket

power supply module were given in the January issue of PE; alternatively, for portable applications, power may be derived from three fresh 1.5V dry cells connected in series. These should be connected to the Heads and Tails Generator via a suitable miniature toggle or slide switch.

CHANGING THE ODDS
The probability of obtaining a ‘head’ or ‘tail’ depends primarily upon the mark to space ratio of the square wave produced by the clock oscillator. The odds can thus easily be changed by means of appropriate modifications to the clock oscillator. With the values of R1 and R2 as specified, the mark to space ratio is very nearly 50%. If, however, R1 is made variable, the mark to space ratio can be varied and the odds changed in favour of either ‘heads’ or ‘tails’, as desired. The appropriate circuit modification is depicted in Fig. 4.

If, alternatively, a precise evens chance is required, it is only necessary to ensure that the clock waveform is a perfectly symmetrical square wave. This can be accomplished by inserting an extra J-K bistable stage between IC1a and IC1b, as shown in Fig. 5. The bistable produces a symmetrical square wave output regardless of the mark to space ratio of its clock input. It should be noted that, since the output of the bistable is at half the frequency of its clock input, it is necessary to alter the value of C1 if the clock frequency is to remain approximately the same.

Copies of British Patents can be obtained from: The Patent Office, Sales, St. Mary Cray, Orpington, Kent (£1.75); and copies of Foreign Patents can be obtained from The Science Reference Library, 25 Southampton Buildings, London, WC2A 1AJ. (Prices on application.)

HI-FI VIDEO SYSTEMS
This year both the VHS and Beta home video manufacturers will be launching hi-fi sound systems. In a conventional helical scan domestic video recorder, the luminance and chrominance vision signals are recorded by rotating video heads and the sound is recorded by a stationary head. Because tape speed is low (one inch per second or less) the sound quality is poor, especially in stereo where the already narrow track must be split into two. In June 1982 Sony announced an alternative approach; using the video heads to record stereo sound as f.m. buried in the video waveform.

The Sony Beta Hi-Fi system has been on sale in NTSC countries, Japan and the USA, since last summer. But Sony has been cagey over exactly how the system works. This is because the Beta Hi-Fi system to be launched in Europe, for PAL and SECAM, will not be the same as Beta Hi-Fi in the USA and Japan. In fact Beta Hi-Fi in Europe will be almost exactly the same as the VHS Hi-Fi system. Two extra heads on the rotating drum lay down the f.m. sound carriers a fraction of a second in advance of the video heads. The f.m. sound carrier is of relatively low frequency, consequently it records deep into the magnetic coating of the tape.

The video signal is on a higher frequency f.m. carrier which wipes out and replaces the top layer of the sound carrier. The result is a layered recording, video on top and audio below. The technique is called depth multiplex recording.
Recent British patent application 2113894 from Sony explains how the two head Beta Hi-Fi system works and gives a clue to the problems which Sony has found insuperable for Europe.

Fig. 1 shows the schematic circuit. Left channel audio enters at 11, and right channel audio at 12. The right channel frequency modulates a carrier of frequency F1 (1.325MHz) at 16, and simultaneously modulates a second carrier at frequency F2 (1.475MHz) at 17. The right hand channel modulates carrier F3 (1.625MHz) at 18 and carrier F4 (1.775MHz) at 19. One left channel signal (LF1) and one right channel signal (RF3) are combined at 31, mixed with the luminance (LM) and chrominance (C) video signals at 33 and sent to helical scan recording head 46. The other left signal LF2, and the other right signal, RF4, are combined at 32, mixed with chrominance and luminance at 34 and sent to recording head 47. The frequency spectrum is shown in Fig. 2.

Fig. 3 shows the signals sent to video head 46, and Fig. 4 shows the signals sent to video head 47. So the helical tracks across the tape alternately have the spectrum of Fig. 3, then the spectrum of Fig. 4, then the spectrum of Fig. 3 again, and so on. As a result, adjacent tracks do not use the same frequencies. This reduces the problem of crosstalk between the sound carriers of adjacent tracks. Video crosstalk is handled in the usual way, by making two video heads with gaps of different azimuth and altering the video signal phase so that unwanted signals are ignored. The level of the carriers is automatically adjusted before recording, to compensate for the non-linear characteristic of magnetic tape at high frequencies.

The system works, for NTSC recorders in Japan and the USA, because NTSC video needs less bandwidth than European video. So there is room in the spectrum for the four carriers used. But in Europe there is not enough room in the spectrum. Hence the adoption by both Beta and VHS of systems which rely on extra heads and depth multiplex recording. But why is Sony filing patents in Europe for a system which won't be used in Europe? Probably because when the patents were filed here (December 1982) the company still hoped to make the NTSC system work for PAL and SECAM.

Incidentally, anyone checking application 2113894 in a library, should also look at the patent on the shelf next to it. Number 2113893 was filed by JVC and describes the technology used to reduce the size of the head drum in a portable video recorder and camera combined 'camcorder' while still retaining compatibility with machines of standard drum size. In fact this patent reveals the startling news that JVC is working on a VHS camcorder with video drum half the normal size. JVC's prototype camcorder, VHS Video Movie, sneak-previewed at the Berlin Radio Show, uses a head drum two thirds normal size. So a camcorder with half size drum and commensurately smaller mechanics, could be even smaller than VHS Video Movie.
EXPANDING THE
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ADC/DAC BOARD...

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LAST month we looked at a stepper motor controller. This month we examine the applications and control techniques of stepper motors, and include suitable software. This is followed by a new interface for VIC 20 which allows DAC and ADC.

Apart from robotic applications, where all four motors could be used to control separate functions, yet be used simultaneously, the most likely use will be for control of linear movement or plotting on an X-Y axis.

A single motor has many useful applications including control of length and depth as well as rack and pinion linear positioning. Two motors enable X-Y plotting as well as applications such as for azimuth and elevation control.

Simple BASIC programming is best carried out by the use of subroutines. To start with, a simple forward and reverse step for each motor, with timing accessible from the keyboard. Next a subroutine to be able to step one pair of motors (two if required) diagonally either on a horizontal or a vertical plane. To give three dimensional movement, such as to move from a corner of a cube towards the centre, three motors need to be stepped simultaneously. These three motors would normally work in association with each other, in pairs, or on their own. Then there is the fourth motor, which might work simultaneously with, yet independent of, the others. The four motors can be controlled independently in 8 subroutines and X-Y movement of two motors in another four. This is sufficient to get moving.

First we'll try a short program to make one motor step CCW, then CW.

SDB 520 CONTROLLER
Let P0 control Motor 1 CCW and P1 control it CW. P2 and P3 would control Motor 2 similarly. Finally P4 and P5 to Motor 3 and P6 and P7 to Motor 4.

SAA 1027 CONTROLLER
Let P0 pulse Motor 1 and P1 logic "0" step it CCW, P1 logic "1" to step it CW. Because of the opto-isolator, the logic for direction is the reverse of that expected, as stated in the manufacturer's specifications. The change of logic does not affect the pulse. Pair off P2/P3 to Motor 2, etc.

Write subroutines for stepping CCW and CW.

SDB 520
200 POKE 37136,1:REM Set I/O for pulse to ICI pin 1 (CCW)
201 POKE 37136,0:REM Negative going pulse
202 FOR I=1 TO 200:NEXT:RETURN:REM Set speed
300 POKE 37136,2:REM Set I/O for pulse to ICI pin 2 (CW)
301 POKE 37136,0:REM Negative going pulse
302 FOR I=1 TO 200:NEXT:RETURN

SAA 1027
200 POKE 37136,1:REM Set I/O for pulse to IC1 pin 15 (Pulse)
201 POKE 37136,0:REM Step CCW (See note on reversed logic)
202 FOR I=1 TO 200:NEXT:RETURN
300 POKE 37136,3:REM Set I/O for pulse to IC1 pins 15 and 3
301 POKE 37136,0:REM Step CW
302 FOR I=1 TO 200:NEXT:RETURN

EITHER CONTROLLER
10 POKE 37138,255:REM Set DDR for all ports as outputs
20 GOSUB200:GOSUB200:GOSUB200:GOSUB200:REM Step CCW 4 steps
25 FOR I=1 TO 800:NEXT:REM Delay before changing direction
30 GOSUB300:GOSUB300:GOSUB300:GOSUB300:REM Step CW 4 steps
35 FOR I=1 TO 800:NEXT
40 GOTO20:REM Loop until stopped from keyboard

Having already written subroutines for stepping Motor 1 CCW and CW, we now do the same for Motor 2.
SDB 520
400 POKE 37136,4:REM Set I/O for pulse to IC2 pin 1 (CCW)
401 POKE 37136,0:REM Negative going pulse
402 FOR I=1 TO 200:NEXT:RETURN:REM Set speed
500 POKE 37136,8:REM Set I/O for pulse to IC2 pin 2 (CW)
501 POKE 37136,0:REM Negative going pulse
502 FOR I=1 TO 200:NEXT:RETURN

SAA 1027
400 POKE 37136,4:REM Set I/O for pulse to IC2 pin 15 (Pulse)
401 POKE 37136,0:REM Step CCW (See note on reversed logic)
402 FOR I=1 TO 200:NEXT:RETURN
500 POKE 37136,12:REM Set I/O for pulse to IC2 pins 15 and 3
501 POKE 37136,0:REM Step CW
502 FOR I=1 TO 200:NEXT:RETURN

The next stage is to program motors 1 and 2 to provide an X–Y plot movement.

SDB 520
600 POKE 37136,5:REM Motors 1 & 2 CCW Binary
00000101
601 POKE 37136,0
602 FOR I=1 TO 200:NEXT:RETURN
605 POKE 37136,10:REM Motors 1 & 2 CW Binary
00001010
606 POKE 37136,3
607 FOR I=1 TO 200:NEXT:RETURN
610 POKE 37136,9:REM M1 CCW M2 CW Binary
00000101
611 POKE 37136,0
612 FOR I=1 TO 200:NEXT:RETURN
615 POKE 37136,6:REM M1 CW M2 CCW Binary
00000110
616 POKE 37136,0
617 FOR I=1 TO 200:NEXT:RETURN

SAA 1027
600 POKE 37136,5:REM Motors 1 & 2 CCW Binary
00000101
601 POKE 37136,0
602 FOR I=1 TO 200:NEXT:RETURN
605 POKE 37136,15:REM Motors 1 & 2 CW Binary
00001111
606 POKE 37136,3
607 FOR I=1 TO 200:NEXT:RETURN
610 POKE 37136,13:REM M1 CCW M2 CW Binary
00000111
611 POKE 37136,0
612 FOR I=1 TO 200:NEXT:RETURN
615 POKE 37136,7:REM M1 CW M2 CCW Binary
00000111
616 POKE 37136,0
617 FOR I=1 TO 200:NEXT:RETURN

We'll try some X–Y movements. Motor 1 moves plotter vertically. Motor 2 moves plotter horizontally.

EITHER CONTROLLER
10 POKE 37138,255:REM Set DDR for output at all ports
20 GOSUB300:GOSUB300:GOSUB300:GOSUB300:GOSUB300 Start
30 GOSUB500:GOSUB500:GOSUB500:GOSUB500
40 GOSUB610:GOSUB610:GOSUB610:GOSUB610
50 GOSUB600:GOSUB600:GOSUB600:GOSUB600
60 GOSUB615:GOSUB615:GOSUB615:GOSUB615
70 GOSUB605:GOSUB605:GOSUB605:GOSUB605
80 END

For users of 80 based computers the method of programming is similar to that for the l.e.d.s simulator. Stepping movement values are the same as for those used with the VIC 20, but are placed in the A register in Hex form. In summary, these are as follows:

SDB 520
Motor 1 CCW 01H CW 02H
Motor 2 CCW 04H CW 08H
Motors 1 & 2 CCW 05H CW 0AH
Motor 1 CCW Motor 2 CW 09H
Motor 1 CW Motor 2 CCW 07H

SAA 1027
Motor 1 CCW 01H CW 03H
Motor 2 CCW 04H CW 0CH
Motors 1 & 2 CCW 05H CW 0FH
Motor 1 CCW Motor 2 CW 0DH
Motor 1 CW Motor 2 CCW 07H

Again, the delay is put at the beginning of the program to enable an easy introduction of stepping sequences and is placed at 1000H to allow relocation. No system monitor routines are included, so the program should work on any 280 computer without further modification.

An X–Y program similar to that for the VIC 20 could take a similar form.

```
1000 0010
1000 0640 0020 DELAY
1002 08 0030 DELY1
1003 AF 0040
1004 F5 0050 DELY2
1005 F1 0060
1006 F5 0070
1007 F1 0080
1008 3D 0090
1009 20F9 0100
100B 00 0110
100C 10F4 0120
100E C9 0130
100F 00 0140
1010 3E01 0150 M1CCW
1012 D304 0160 OUT (EO4),A;Output through PIO
1014 3E00 0170 LD A,EO1;Motor 1 CCW
1016 D304 0180 OUT (EO4),A;pulse shape
1018 C9 0190 LD A,EO2;Motor 1 CW
1019 00 0200 RET
101A 3E02 0210 M1CW
101C D304 0220 OUT (EO4),A
101E 3E00 0230 LD A,EO3
1020 D304 0240 OUT (EO4),A
1022 C9 0250 LD A,EO4;Motor 2 CCW
1023 00 0260 RET
1024 3E04 0270 M2CCW
1026 D304 0280 OUT (EO4),A;Output through PIO
1028 3E00 0290 LD A,EO5;Clear A to complete
102A D304 0300 OUT (EO4),A;pulse shape
102C C9 0310 LD A,EO6;Motor 2 CW
102D 00 0320 RET
102E 3E08 0330 M2CW
1030 D304 0340 OUT (EO4),A
1032 3E00 0350 LD A,EO8
1034 D304 0360 OUT (EO4),A
1036 C9 0370 LD A,EO9
1037 00 0380 RET
```
ADC/DAC CONVERTERS

In any electronic system, two basic kinds of signals are generated or measured. These are analogue or digital signals. Analogue signals exist as a continuous range of values, whereas digital signals are only apparent when a predetermined threshold level is reached. Typical examples of analogue signals are the varying speed of a motor, the varying intensity of a light source and the changing temperature of an oven. Each of these, being an analogue variable, are able to assume an infinite number of intermediate values between zero and maximum. On the other hand, a binary signal is a digital signal, which assumes one of two states. Either ‘on’, logic 1, or ‘off’, logic 0.

In this part of the series we explain briefly the principles of digital to analogue conversion (DAC) and analogue to digital conversion (ADC) and describe the construction of a low priced board which performs both functions, whilst using the minimum of components. The heart of the system is the Ferranti ZN425E 8 bit D-to-A/A-to-D Converter i.c.

In DAC and ADC applications, two important factors arise, resolution and speed, and these generally relate to the cost of the system. Converters are normally designed as 4 bit, with 16 stages of resolution; 8 bit, with 256 stages of resolution and 16 bit, with 65536 stages of resolution. With 16 bit systems, problems regarding stability are encountered, which leads to complexity of circuit design and a corresponding increase in cost. There are many low priced separate 8 bit DACs and ADCs on the market, including some in the Ferranti range. However, the ZN425E is an easy i.e. to use. It makes an ideal compromise with regard to resolution and though a little slow for some practical purposes, serves to illustrate the functions of D/A and A/D conversion with little outlay.
THE ZN425E 8 BIT D TO A/A TO D CONVERTER

The ZN425E is an 8-bit dual mode analogue/digital, digital to analogue converter. It contains an 8 bit D-to-A converter, using an advance design of R-2R ladder network and an array of precision bipolar switches, which results in full 8 bit accuracy. The inclusion of an 8 bit binary counter on the chip and the addition of an external comparator enables analogue to digital conversion. A logic input select switch is incorporated, which determines whether the precision switches accept the outputs from the binary counter or external inputs, depending upon whether the control signal is respectively high or low. Use of the on-chip 2-5V precision voltage reference is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted. The ZN425E gives an analogue voltage output directly from pin 14, therefore the usual current to voltage converting amplifier is not required. A buffer amplifier is necessary, however, in order to remove the offset voltage and to calibrate the converter.

The problem of converting a binary number into an analogue voltage is solved by the following simple solution: a voltage is generated for each bit position of the binary number, the value of this voltage being proportional to the binary weighting of the bit. For example, bit 0 will generate a voltage \( V(2^0) \); bit 1 will generate a voltage \( V(2^1) \); bit 2, a voltage \( 4V(2^2) \) and bit 'n' a voltage \( 2^n \times V \). The resulting voltages are added and the result is proportional to the original binary number. This is simply illustrated in Fig. 6.2. The D/A consists of 4 switches, 4 summing resistors in the proportion 1,2,4,8, an operational amplifier and a proportional feedback resistor. Resulting in gains of: \(-1/8, -1/4, -1/2, \) and \(-1\). With the switches in the open position, there is no input to the operational amplifier, therefore the output will be OV. The operational amplifier is in inverting and adding mode. Closing bit '0' switch results in the formula \(-\frac{V_{ref}}{8R} \) being applied = \( \frac{1}{8} \) V. By closing bit switch '1' a gain of \(-1/4V\) is added at the output. And so on. The 4 bit binary number represented by the 4 switches is converted into a voltage, which is the analogue representation of one of the 16 possible digital values that can be derived from this circuit.

In practical applications, a precision R – 2R ladder network and fixed reference voltage is employed, switching being carried out by f.e.t. transistors. A typical arrangement of an R – 2R network is depicted in Fig. 6.3. If a bit is set to logic '1', its associated f.e.t. switch is closed, connecting \( V_{ref} \) into the R – 2R network. It is clear from the previous example that in an 8 bit Digital to Analogue converter, Data Bit 7 would provide a greater contribution to the analogue output when set, than Bit 0. As the number increases, its contribution to the output is double that of the previous bit, the ladder being binary weighted. In an 8 bit converter, Bit 7 is weighted at 1/2, whilst Bit 0 is weighted at 1/256. Note, that whilst there are 256 stages of resolution in an 8 bit converter, this only realises 255/256Vref when all bits are set. As opposed to the circuits used in Figs. 6.2 and 6.3 to illustrate the operation of DACs, the ZN425E is a unipolar device, assuming all inputs to be positive and its output is always a positive value.

The conversion of an analogue signal into a digital quantity is always a sampling process, the instantaneous value of an analogue signal being read and stored as a binary number at different instances of time. In the circuit which is to be described later, the output port of the computer is connected to the DAC's inputs, the output from which is fed into a comparator. The analogue signal to be converted is fed into the other input of the comparator, whose output is fed back into an input port of the computer. The digital value from the computer is then scanned until a comparison occurs between the analogue input signal and the output from the DAC. The digital value at the output from the computer then represents the analogue input signal to the comparator at that instant of time. There are several methods of arriving at this value and we will discuss some of them in the following paragraphs.

SINGLE RAMP OR STEPWISE CONVERSION

This technique uses an upwards counting whose final value is controlled by the comparator output. The conversion starts at zero and the count is incremented until the output from the DAC compares with the value of the analogue input to the comparator. This causes the comparator output to switch to logic 0, which in turn inhibits the counter. The digital value now existing on the input to the DAC represents the analogue voltage at the input to the comparator. This can be converted from a digital value into an analogue value displayed on the screen by the writing of a short software routine. The disadvantage of this method is that whilst a near zero signal can be rapidly compared and converted, a full scale input requires 256 iterations.

THE TRACKING CONVERTER

In a tracking type ADC, the up-count is replaced by an up/down count. The condition of the comparator output dic-
states the direction of the count so that the DAC output can track the analogue input. The starting point for each conversion is the end point of the previous conversion. Obviously, the success or failure of this type of conversion depends on the frequency of value changes and the differential values of the changes.

CONVERSION BY SUCCESSIVE APPROXIMATION

The successive approximation technique of A/D conversion is probably the one most frequently used with microprocessors, as it is characterised by high speed, high resolution and low cost. This method of conversion, whilst being based upon trial and error principles, ensures a result in a finite number of steps. It involves making a preliminary guess at the analogue value and then, from the result of that guess, making a series of intelligent guesses, each based upon the previous result until a final conversion value is reached. In practice, for an 8 bit DAC, the number of iterations is always 8. The preliminary value sampled is always half the full scale for the converter or Bit 7 of the computer output port. The comparator output then indicates whether the input analogue signal is greater than or less than half the output port. The conversion time is therefore independent of the size of the computer word or the DAC word size. As stated earlier, in our case 8 iterations are needed to find the final value. The convert time is therefore independent of the size of the analogue quantity to be converted. In the event of the analogue value being in excess of the full scale value of the converter, the conversion stops at the full scale value.

EXAMPLE OF 8 BIT SUCCESSIVE APPROXIMATION

Initial Value | > (1) | < (2) | > (3) |
-------------|-------|-------|-------|
1 0 0 0 0 0 0 0 (2) | 1 1 0 0 0 0 0 0 (3) | 1 0 1 0 0 0 0 0 (4) | 1 0 1 1 0 0 0 0 (5) |
< (4) | > (5) | > (6) | < (7) |
1 0 1 0 1 0 0 0 (6) | 1 0 1 0 1 1 0 0 (7) | 1 0 1 0 1 1 1 0 (8) |

The result is 173/256 of the full scale value of the signal. If the full scale value of the input signal is expected to be 5 volts, this would be displayed on the screen through a software routine as 3.7890625 volts.

Whichever method of sampling is used, programming for ADC is carried out by putting an analogue signal into the non-inverting input of the comparator and another signal from the DAC into the inverting input of the comparator. On the signals becoming of equal value, the output of the comparator becomes 0 volts. The computer looks for this signal and on it being present, should stop the sampling from the DAC. The state of the DAC output at that stage indicates the value of the analogue signal input to the comparator. The direct output from the DAC via switch 1 with all bits set (255) is approximately 2.53 volts and near enough to FSR (2.56V) —1 LSB. With bit 7 set (128), the output is 1.28 volts etc. This makes a useful starting point. Should the FSR of the comparator also be adjusted to 2.53 volts, this makes initial experiments fairly easy. Using 4.5 volt batteries to power the board, the output from the 741 is approx. 3.8 volts and provision is made for linking this to the comparator by making a small underside link on the board from the base pad of Transistor 1, to the small pad provided. Also, of course, the switch can be left out and the output from the converter connected directly to both op-amp and comparator.

If CB1 Control—Bit 4 of the Peripheral Control Register (PCR) (37148) is used to input the output of the comparator into the computer. Bit 4 is set to logic “0”. The CB1 interrupt flag will then be set by a negative transition on the CB1 line. (The line goes from a logic High to a logic Low.) The PCR cannot be read directly. It is designed to set a flag (Bit 4 for CB1) in the Interrupt Flag Register (IFR) (37149) when a transition occurs in the CB1 line. Once the CB1 flag is set, it will stay set until cleared by a POKE to PORT B, which resets the CB1 flag bit.

Initial experiments should be carried out by following these lines:

Set DDR with all lines as outputs, POKE 37138, 255
Input a small, known, analogue value
Input values into I/O register
Set PCR—Bit 4, POKE 37148
If the IFR is set by a transition, PEEK(37149)
PRINT message on screen
Clear I/O register, POKE 37136, 0
Restart sampling.

The following listing is suitable for running the DAC from the keyboard with very quick response.

01 PRINT“Shift/CtrHome”:REM Clear screen
02 PRINT“To start the DAC function you must”
03 PRINT“enter a value 0 to 255 in the I/O register”: PRINT:PRINT
04 PRINT“Typing in a new value changes the status of the port”:PRINT:PRINT

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CIRCUIT DESCRIPTION AND CONSTRUCTION

The circuit is a combined DAC and ADC using the Ferranti ZN425E 8 Bit converter IC. When used in DAC mode, a 741 operational amplifier is used as a buffer in order to adjust offset voltage and calibrate Full Scale Reading. These functions are carried out by way of VR2 and VR1 respectively.

(a) The offset null is adjusted by setting all bits to OFF (Low) and adjusting VR2 until Vout = 0.000V.

(b) Calibrate with all bits set to ON (High) and adjust VR1 until Vout = Normal Full Scale Reading - 1LSB (FSR/256) e.g. Set f.s.r. to 2.5V - 1LSB = 2.49V. (Where 1LSB = 10mV.)

(c) Repeat stages (a) and (b).

A SPDT switch is provided at pin 14 of IC1 to switch the output of the ZN425E between the 741 (IC2) and the LM311N (IC3) comparator, which is used when in the ADC mode.

The author used a small p.c.b. type switch, but pads have been provided, so that for those who wish to use a toggle, a hole can be drilled and connecting leads taken from the switch to the pads.

The output of the comparator is taken to CB1, pin B of the I/O port. (Bit 7 Port 4 for Z80 PIO).

 Provision has been made for adjustment of offset voltage and normal full scale reading at the comparator with VR4 and VR3 respectively. These are adjusted in the same manner as described above. Once set there should be no need for re-adjustment, apart from periodic checks or following accidental displacement.

A small power transistor of the 2N3055/BF51 700mW, 1A n.p.n. type has been included at the output from the DAC circuit to enable small motors to be driven and bulbs to be lit up. Power is taken from the 5 volt rail which supplies the 741 and 311, the ZN425E being powered by the host computer. A -5 volt supply is also used by the 741 op-amp. This is taken from the negative side of two batteries connected in series, the centre, + - , point being connected to ground. Two short links are made on the component side of the board. These should not be mounted flush, because they are useful as a test point at the output of the converter and a ground rail for all tests. A test point is also provided at the output from the 741 op-amp. The DAC function can be tested at these points with a meter.

Pads at the front edge of the board include CB1 and CB2 in addition to +5 volts, Ground and Data bits 0 to 7. Notice that on the ZN425E, Data Bits are marked from 1 to 8, with in addition to +5 volts, Ground and Data bits 0 to 7. Notice that on the ZN425E, Data Bits are marked from 1 to 8, with Bit 1 as most significant bit (MSB) and Bit 8 as the least significant bit (LSB). The reverse value of bits from the I/O ports of a computer.

Whilst the author has used 2mm p.c.b. test points (except computer panels) for input, output and power sockets, large copper pads are provided so that the constructor can choose to use whatever type of connector is available or preferred.

No provision has been made for opto-isolation from the computer since the circuit is intended for use with external supplies up to 5 volts. Provided care is taken with the polarity of the external power lines and the analogue input to the comparator everything should work fine.

TESTING

After typing in the DAC program, test it with the "I.e.d.s and switches" board (Part 2), to ensure that you have copied the listing correctly. When satisfied that the program is working, record it and turn the machine off.

First tests on the board should be to ensure that there are no shorts or badly soldered joints. If satisfied, plug into the I/O port of the computer without the ZN425E on board. Load and run the DAC program, placing 0 value at the ports. Test that you have +5 volts on the correct rail. Now put in 128 and check that you have approximately +5 volts on Data Bit 7 (Bit 1 of converter). Next input 64 through to 1, each time checking for the +5 volt signal. If satisfied that your leads are connected correctly, turn off the computer, insert the ZN425E and start again. This time, connect your meter, digital if you have one, between the two links previously mentioned. Having read the instruction set for the DAC program type in RUN10 to start program without having to wait. On initialisation the output to the ports should be 00000000 and the output from the DAC also 0.00. Enter 255. The ports show 11111111 and the meter reads 2.53
Fig. 6.5. Printed circuit layout (actual size)

Fig. 6.6. Component layout

COMPONENTS . . .

Resistors
- R1 6k8
- R2 18k
- R3 15k
- R4 3k3
- R5 1k
All resistors 1W 5%

Potentiometers
- VR1, VR4 4k7 (2 off)
- VR2 10k
- VR3 22k

Capacitors
- C1 220n

Semiconductors
- TR1 BFY51 or 2N3053
- IC1 ZN425E AD/DA converter
- IC2 741 op. amp.
- IC3 LM311N comparator

Miscellaneous
- S1 SPDT p.c.b. mounting
- Sockets 2mm p.c.b. mounting
- Printed circuit board

 Constructors' Note
Printed circuit boards for this series are available from
Proto Design, 14 Downham Rd., Ramsden Heath,
Billerica, Essex CM11 1PU (0268 710722) and Bradley
Printed Circuits, 9 Harcourt Terrace, Oxford OX3 7QF
(0235 32681).

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that this interface only measures small voltages. In industrial
only a moderate challenge to the computerist.
comparator is working. Try other values. Programs in BASIC
adjust the FSR to 2.5 volts. Input 255 from the keyboard
That is, for no inputs there should be zero output. Put an
voltage at which a motor will run and before the glow of a
lamp becomes apparent.

It is assumed that you have set your offset nulls by now.
That is, for no inputs there should be zero output. Put an
analogue voltage of 3 to 5 volts at the analogue input and
observe the results. Don’t forget that there is a minimum
output for an input of 255 will be around 3.8 volts, for 128, around 1.9
volts etc. Connect a small motor or lamp at the output and
and the meter 1.28 (approx.). By changing over your meter
range you should get more accurate readings, but the

When happy that your DAC is working, turn to the output
or input of the 741 op-amp.

Having made the initial tests, experiments can now be
made in conjunction with a low range voltmeter, passing on
to small motors, 6 volt bulbs etc. Broken Christmas toys can
provide a useful source for some of these. Why not connect
up to a model car with a couple of wires. Not as good as
some of the small robots on the market, but a start in the
right direction. To test the ADC, a potential divider can be
made with a 10k linear pot. across a battery.

Test the ADC with 1-5 batteries, LDRs, transducers and
solar cells. If you have no solar cells, cut the top off a surplus n.p.n. power transistor. Do not use p.n.p. as some of these
are filled with a poisonous paste. Do not be disappointed
that this interface only measures small voltages. In industrial
applications, such as temperature control, the output voltage

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NEX T MONTH: The hardware for an EPROM programmer.
Lost Hope?

Those of us who had hoped for a constructive alternative to Thatcherite economic policy from a rejuvenated Labour party must be disappointed. The 'dream ticket' leadership has produced nothing new and the 1983 manifesto stays intact.

Of course there are vague statements about back-room boys (possibly girls, too) engaged in long-term planning and some new policies will have to emerge in time for the autumn party conference.

The snag is that economic recovery continues, as is now generally agreed, Mrs Thatcher's claim that There Is No Alternative (TINA) will appear to be more than justified. It will appear that her resolute approach has made British industry more competitive, more efficient. I say 'appear' because, at least in part, the US economy is the locomotive that is pulling the world out of recession, including Britain. Nonetheless it has been Thatcher toughness that has thinned out, if not entirely eliminated, gross deficiencies affecting economic performance.

So where does this leave Mr Kinnock? He can move to the right and try to out-Thatcher Thatcher, beating her at her own game. Or agree, as is his natural inclination, to retain his loyalty to full-blooded socialism. The first would be totally unacceptable by the trade unions, his party paymasters. The second is largely unacceptable by the electorate at the present time. Labour had hoped that the success of socialist France would have been the example to highlight the comparative failure of Thatcherism. Alas, even this hope has now disappeared in economic failure in France.

With the middle ground already occupied by the Liberal/SDP alliance and with the handicap of inexperience in government Mr Kinnock has a difficult future. The revelation that he, equally with Mrs Thatcher, shops at Marks and Spencer is no substitute for a realistic policy. Nor does his pledge to return the Elgin marbles to Greece if he gains power look like being a vote-winner.

ASMI

Recent runway collisions involving loss of life as well as aircraft is bound to stimulate new demand for Airport Surface Movement Indicator (ASMI) installations. ASMI is a very high definition radar system which concentrates entirely on ground movements. It surveys main and auxiliary runways, aprons, entry and departure lanes, and perimeter tracks. Definition is such that aircraft types can be identified by wing shape and size, tugs, tankers and other replenishment vehicles equally so. Even birds are detectable through fog and rain as well as darkness.

The high cost of such equipment has resulted in a sluggish market. Only those airports with very high international traffic density have so far been equipped, such as those at Heathrow, Rome and Paris.

Racial Avionics has now gone some way to easing the cost barrier by using a mass-produced existing output stage in their latest ASMI, the 18X. One is being installed at Australia's busiest airport at Sydney with follow-ons at London-Gatwick and Stockholm. The Sydney installation has another cost-cutting feature. The ASMI scanner is sited 1.5km from the control tower and the radar data is transmitted by fibre optic links, thus enabling existing cable trunks to be used without fear of external electrical interference or cross-talk with other services.

200kHz Switch

There seems no limit to ingenuity in extending applications to existing systems. A prime example is the novel idea of using the BBC's 200kHz broadcast transmitters at Droitwich, Burghhead and Westerglen to switch on and off our off-peak tariff electricity supply. Bad news maybe for existing time-switch manufacturers but a bright opening for the replacement device which will incorporate a narrow-bandwidth fixed-tuned radio receiver.

Switching to the off-peak tariff at consumers' premises will be by phase modulating the 200kHz carrier and, because of the narrow bandwidth of the receiver, reception will be possible even in basements of steel-framed buildings.

The new system has been developed by GEC Meters and technical trials have apparently been running for at least four years. Now the Electricity Council has signed a contract with the BBC and consumer acceptance is being evaluated on a sample of 1,500 consumers.

Don't assume that if this idea reaches fruition that the whole nation's off-peak electricity will be switched simultaneously. By signal coding, each electricity area board can operate its own switching regime. And within each area there can be as many as 256 groups of consumers which can be separately controlled.

For the electricity boards there is the tremendous advantage of flexible load control. For the consumer the extra goodie of, say, an afternoon boost to his water heater at off-peak rate.

Airborne

Marconi Avionics continues to demonstrate outstanding ability both in technology and marketing. After developing digital speech communications which had successful trials at the Royal Aircraft Establishment the company has won a £12 million plus order for production equipment. The new digital speech system is scheduled for air-to-air and air-to-surface duty in all Royal Navy aircraft and in RAF maritime reconnaissance Nimrods. It is the biggest order ever to be won by the Basildon plant.

The Rochester Distribution Centre also got off to a good start in 1984 with an order for submarine detection systems for the Royal Swedish Navy who have chosen the AQG 902 which won a Queen's Award for Technological Achievement last year. I don't often have an opportunity to thank the Soviet Union for anything but I do so on this occasion because their suspected submarine intrusions into Swedish territorial waters prompted Sweden to improve her underwater detection. The AQG 902 has already proved itself in Sea King helicopters of the Royal Navy.

Pioneer

Few of the younger generation will have heard of Sir Harold Bishop who died recently at the good age of 82. Apart from his first two years he spent the whole of his working life in broadcasting, first at 2LO run by Marconi Wireless Telegraph Company and in 1922 transferring with the station to the BBC. As an engineer he progressed upwards, eventually becoming BBC Director of Engineering leading a team of 5,000. He was connected with every major development in broadcasting, including television, and he and his colleagues in the BBC set technical standards which led and still lead the world to the benefit of UK electronics.

Sir Harold was a true pioneer. He was there at 2LO when it had a single microphone feeding a 500 watt transmitter in London's Strand with an aerial on the roof and only a handful of listeners. The latest BBC handbook estimates that there are now 1,300 transmitters in use around the world. How's that for explosive growth in a single lifetime? Apropos of the increasing pace of life today I was much taken with a comment from the US politician George W. Ball's autobiography, The increasing compression of events now means that by medieval standards I have lived at least five centuries'.

Cable

Britain is not the only country gearing up for the cable TV revolution. East Germany is reported to be speeding up plans for a network. Western observers are probably correct in assuming that this, far from increasing the number of programmes, is a restrictive move. Large numbers of East German viewers regularly watch Western programmes transmitted from Berlin. By installing cable and then banning TV aerials their minds would remain uncontaminated by Western influence.
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Fig 1. B.F
THE HALLEY COMET MISSION

Now that agreement has been reached by the agencies involved as to 'who does what', the general scheme of the mission may be said to be finalised. The three agencies involved are the European Space Agency, the Soviet Union and the United States of America. The general strategy of these three has also been reinforced by the Japanese with their two spacecraft: Planet and MS-T5. Thus, this is now a truly international undertaking. It is hoped that the mission's close look at Halley's comet will answer some of the age-old questions regarding comet composition and formation.

We have, since the last return of Halley's comet in 1910, developed the technology which may solve the puzzle, in a century that will see two returns.

A few of the important facts of the strategy will be helpful in getting the feeling for the mission. First, the position of the Nucleus of the comet must be established. At the moment we have to make an educated guess because the Halley Nucleus is only ten kilometres or so in diameter, and has never been seen from Earth. This is because although the Coma, that is the cometary atmosphere that surrounds the Nucleus, extends for hundreds of thousands of kilometres, and is so bright that the Nucleus is not discernible. Therefore the European Space Agency has asked the Soviet Union to use the Vega spacecraft to provide the latest information. This is because the launch date of the first Vega will be up to seven days before that of Giotto, the ESA Halley spacecraft. Giotto will then be able to plot the orbit and make its final manoeuvre. The final manoeuvre will be made about two days before the actual fly-by. The ESA want Giotto to intercept the comet's orbit at a point some 500 to 1000km from the Nucleus on the sunward side of the Nucleus. We shall be relying on the Soviet Union for the correction and monitoring data.

Comets are usually described as very primitive bodies that are formed of debris, the most popular theory is that this is from the debris which remained after the formation of sun-like bodies, and that it was mostly ice and dust. Whatever ideas exist at the moment, the encounter will certainly provide sound evidence on which to discuss this matter in the future. One of the matters creating much interest will be the puzzle of the way in which the Coma grows spectacularly as the comet approaches the Sun. There is also the interaction of the atmosphere of a comet with the Solar wind.

Solar heating causes the molecules to become sublimed out of the Nucleus, or as scientists happen to pass from solid to the vapour state as the comet is heated up. During the time that a comet is being subjected to changes of environment the various reactions that take place often give rise to the creation of a variety of compounds. The Nucleus is so small and its gravity so low that the Coma becomes enormous, and may be millions of kilometres in extent. Under these circumstances the mechanism which makes it appear so bright must be directly related to a considerable amount of dust being present; the extent of this must be important. The Solar wind's ultra-violet radiation ionises the neutral molecules and this creates a plasma that is swept up in a tail. The effect of this reaction is that the Solar wind and the embedded magnetic field creates large electric currents. This, in turn, generates an induced magnetosphere much larger than that of the Earth itself. There may be a bow-shock in the Solar wind that is ahead of the Nucleus, so that the comet experiences a bow-shock within its ionosphere.

The five spacecraft will have similar experiments on board which will be in addition to their routine assignments. Each encounter will therefore be carried out over a period of eight days in March 1986. The information will vary, thus giving the maximum data to pass to scientists. The actual tasks to be carried out, so far as the comet is concerned, are quite varied, but the broad details are set out here as they are known at the moment. It is certain, however, that there will be changes.

MISSION TASKS

The imagery from the Soviet Union spacecraft, Vega 1 and Vega 2, will be at two levels. A resolution of 180 metres is aimed at. For Giotto, however, this will be 50 metres at the Nucleus.

Identification of the composition of gases and dust particles of the comet and the confirmation and examination of the physical processes and chemical reactions in the Coma will also be carried out. Other tasks include measurement of gas production rates and the dust flux and the study of cometary plasma and Solar wind reactions.

SPACECRAFT DEPLOYMENT

The pathfinder will be the Soviet Union's Vega 1. This is to be launched in mid-December 1984. It will fly past Halley at a distance of 10,000 kilometres on March 6th 1986. Japan is sending their first spacecraft to escape the Earth's gravitational field; this will be the MS-T5. It will be launched in January 1985, and will cross Halley's path at about one million kilometres from the Nucleus. This will be on the 8th March 1986. Planet-A will be sent by the Japanese in the middle of August 1985 and fly past at 200,000 kilometres on March 7th 1986.

Vega 2 will be launched in late December 1984 and is planned to intercept the comet on March 9th, 1986, the distance from the comet being 3000 kilometres. The spacecraft involved deserve a general description.

The two Vegas are three axis stabilised Venera class spacecraft. They are modified for the Venus/Halley international mission. The modified features include an extended Solar array. There are other optical instruments and television cameras for which a special platform has been provided. The spacecraft will be fitted also with a multilayer dust shield to protect the most sensitive areas from potentially lethal dust.

The Venus part of the Soviet Union mission will be accomplished first. The spacecraft will fly past Venus in mid-June 1985, and each will eject a probe into the Venusian atmosphere.

The velocity of the encounter with Halley will be 78km/sec and each Vega will carry 129 kilogrammes of load for the Halley mission. About two and a half hours before the encounter with the comet, the Vega telemetry will be switched to 65 kilobits/sec data rate. Forty kilobits/sec of this will be required for the television monitoring.

The Japanese spacecraft MS-T5 was planned initially as a test vehicle for Planet-A. It was made as part of the Halley mission to overcome the payload problems. The MS-T5 will carry a magnetometer, solar wind detector and plasma wave probes. Planet-A will carry an ultra-violet imager and a magnetic particles detector. It is not expected that these craft will fly close to the comet Nucleus. They should, however, be able to detect the bow-shock when they exist, and may encounter the ionosphere boundary. These two spacecraft, each of which weighs 150 kilogrammes, will be launched by an M-382 rocket. They too are spin-stabilised craft and will spin at 5 rpm.

The Giotto has 10 experiments on board using 16 sensors which are to be switched on 4 hours before the point of closest approach. Because of the close approach the pointing accuracy must be held to within 1 degree. The spacecraft is spin-stabilised and will spin at 15 rpm. As it will be travelling in an unknown environment it will carry heat pipes to return the solar cells. This is in case the dust degrades the array. The actual velocity of fly-past is expected to be 68km/sec. At that time the Halley comet is expected to be somewhere about 0.89AU from the Sun and 0.97AU from Earth. The spacecraft will approach the comet from the antisun side. This means that the chance of being overwhelmed by dust is minimised and therefore increases the chances of its survival.

IMAGING

Four of the spacecraft of the Halley mission are carrying imaging instruments and will therefore pass to the Sunward side of the comet to avoid as much interference as possible. The only craft which does not is the ISEE-3. This is well equipped to observe solar wind interaction with a cometary atmosphere. It will, therefore, be possible to observe from the comet side of the Sun. The spacecraft is expected to cross the comet's tail at about 15,000 kilometres from the Nucleus.

Frank W. Hyde
Micro-Professor
MPF-1 Plus

SOME eighteen months ago I was fortunate enough to be asked to carry out a review of the Microprofessor MPF1; a low-cost Z80 based microprocessor learning aid. This basic system, of which over 4000 have been sold, consisted of a single-board fitted with a Z80 CPU, 2K ROM, 2K RAM, 36-key keyboard, and a display comprising six seven-segment LED indicators. The package was supported with documentation including a monitor listing, and a "User's Experiment Manual". Although I had a few minor reservations about the package, I was able to give it a firm recommendation and my overall conclusion was that it represented good value for money for those about to enter the world of microprocessors. I am now pleased to report that Multitech have produced a new and much improved version of the Microprofessor, known appropriately as the Microprofessor MPF-1 PLUS.

MICROPROFESSOR LEARNING AIDS

Hardware, software and documentation make up the trio of essential components in any microprocessor learning package. Whereas these items may appear at first sight to be quite separate and distinct, there is a high degree of interdependence. Indeed, if any one of the three is found to have serious shortcomings then this is likely to be to the detriment of the package as a whole. It is a great shame that some learning aids fail quite badly in this respect. Excellent hardware, for example, is of little use if the accompanying software and documentation are lacking in depth and clarity.

Hardware must be built to a high standard such that it is both reliable and durable. As far as possible all i.c. devices should be mounted in sockets which facilitate easy removal in the event of failure. Connectors should be both electrically and mechanically robust, and only first quality 'industry standard' components should be used. In addition, the printed circuit board should be neatly laid out and all major devices are socketed. The accompanying documentation should be properly structured and should cater for the complete newcomer as well as those having some previous knowledge. Texts should incorporate relevant examples and applications should be introduced where appropriate. A full commented monitor source listing should be considered essential.

FIRST IMPRESSIONS

Like its predecessor, the Microprofessor MPF-1 PLUS comes securely packed in a corrugated cardboard box and, inside, the unit itself is contained in a neat, if rather 'plastic', book-style case. The case, which measures 255 x 200 x 48mm (approx), is secured by means of a press-stud fastener and opens to reveal the microprocessor board in the right hand leaf and a recess in the left hand leaf. This latter space is designed to accommodate one or more of the various options available which include an EPROM programmer, speech synthesizer, printer/desassembler, and I/O board. A separate a.c. mains adaptor is supplied which operates from a 240V 50Hz supply and provides a nominal 9Voutput at 600mA. The mains unit is fully encapsulated and is fitted with an integral 13A mains plug.

A 49-key keyboard, which uses a conventional QWERTY layout, replaces the previous 36-key hex and dedicated function unit. Despite the relatively small size of the keys, there is plenty of clearance around them and they have a pleasantly reassuring positive action.

Another very significant area of improvement is the twenty-character fourteen-segment vacuum fluorescent display. This is angled for convenient viewing and replaces the six seven-segment LED displays of its predecessor. The display is bright and extremely easy to read even in difficult lighting conditions. The fourteen-segment display is naturally capable of displaying a much wider range of characters and symbols than its seven-segment counterpart.

CLOSER EXAMINATION

Close examination of the p.c.b. reveals the same high standard of construction common to all Multitech products. The screen printed p.c.b. reveals an area of improvement than previously. The breadboard area of the original Microprofessor is absent. This, however, is no great loss since breadboarding directly onto the MPF-1 p.c.b. cannot really be recommended since it invariably tends to be a 'one-off' operation.

Removal of the p.c.b. (it is simply a press-fit into the plastic book) reveals a battery holder designed to accommodate four UM3 dry batteries. This new facility provides back-up of the RAM such that, with the CMOS devices fitted, memory can be retained for up to twelve months. This was found to be a most useful facility, enabling partly...
The Microprofessor now uses an 8K ROM (2764) and has 4K static RAM (2 x 6116). An optional 8K BASIC ROM is available. FORTH is also planned for the MPF–1 PLUS but the ROM was unfortunately not available at the time of review.

DOCUMENTATION

In keeping with other changes, MPF–1 PLUS documentation is also vastly improved. The basic unit is supplied with three handbooks; a User's Manual, Experiment Manual, and a Monitor Source Listing. In addition, a Student Work Book is also available. The User's Manual contains chapters entitled Overview and Installation, Specification, System Description, Operating MPF–1P, Useful Subroutines, Text Editor, Assembler and Disassembler, and System Hardware Configuration. The English is still a little quaint in places however the manual is otherwise extremely good.

The 311-page Student Workbook also has some 'oriental' English and does contain a few rather obvious errors (why on earth don't Multitech get someone proficient in English to proof read their texts?). The manual is well structured, and includes questions or exercises at the end of each chapter. The Workbook is suitable for an absolute beginner and is also ideal for the individual who is not following a formal course of instruction. Chapters are included on Keyboard Familiarisation, Hand Assembly, Introduction to Hardware, Using the Text Editor, Using the Two Pass Assembler, and How to Read a Schematic. This last title is somewhat misleading as the chapter leaves a number of questions unanswered.

ASSEMBLER AND DISASSEMBLER

One of the main criticisms of the original Microprofessor was the absence of a resident assembler. This meant that all programs had to be hand assembled and entered in hex. This tedious process is prone to error and rarely used for serious software development. Multitech have recognised this fact and have included a two-pass Z80 assembler in the MPF–1 PLUS.

Programs are entered, using standard Z80 mnemonics, line-by-line from the keyboard and resident text editor. The programs are then assembled and the appropriate source code is generated. An unfortunate disadvantage is that the reverse process (i.e. disassembly) can only be carried out in conjunction with the companion printer module, PRT-MPF-1P. This unit contains the disassembler software in ROM and whilst one might argue that program disassembly is usually made direct to a printer, it would be nice to be able to disassemble on a

BASIC

The optional BASIC ROM is entered from the keyboard via 'CONTROL–8'. BASIC statements exceeding twenty characters in length are automatically scrolled left when the display is filled. When editing long program lines the overflow may be displayed by appropriate use of the left-arrow. It is, however, a little disconcerting to find that later use of the right-arrow does not restore the display (i.e. characters shifted to the left of the first display digit are lost!). Three characters, '(', ')', and '*', are used to indicate monitor, input, and command level.

The 8K BASIC is reasonably powerful and will accept hex as well as decimal inputs. Editing is somewhat crude and lacking in the facilities which are normally found in low-cost personal computers. Furthermore, since only one line is displayed at a time, a printer soon becomes almost essential for any other than the most elementary of programs.

The 181-page BASIC manual is quite acceptable and consists of a step-by-step introduction to Microprofessor BASIC. It is ideal for the beginner wishing to make a first step into programming in a high level language. By the time that you read this review, an alternative 8K FORTH ROM should be available. This should bridge the gap between BASIC and assembler and appeal to those wishing to explore this excellent control-oriented language.

PRINTER

The first Microprofessor option which most users will want to consider is the high speed twenty character thermal printer. I frankly admit that my first reaction on unpacking the unit was surprise and reinforcement of the commonly held conviction that one doesn't get very much for one's money these days! I am now prepared to admit that I was wrong since, despite its apparent simplicity, the unit does work extremely well. It is quiet and reliable in operation and the printed text is very pleasing. The printer is supplied with a roll of thermal paper, a connecting cable, and the necessary mains adaptor. The printer is accompanied by a brief but perfectly adequate manual.

INPUT/OUTPUT

One of the most commendable features of the Microprofessor system is the level of expansion which is possible. An option which will undoubtedly prove to be very popular with both the electronic enthusiast and the equipment designer is the I/O board. This exciting module facilitates connection to the outside world in a variety of different forms. The hands-on experience of microprocessor interfacing which can be gained from this board is second to none!

The I/O board is the same size as the basic Microprofessor p.c.b. and incorporates both serial I/O in the form of an 8251 programmable communications interface and parallel I/O in the form of the Z80–P10 (programmable input/output). Thrown in for good measure is the Z80–CTC (counter timer circuit) and a sizeable breadboarding area. A further 4K ROM and 6K RAM are also provided. Like the printer, the I/O board has its own mains power supply and connects to the CPU board using a short length of 40-way ribbon cable.

The MPF–1 PLUS with the PRT, EPB and I/O boards and manuals

SPECIFICATION

<table>
<thead>
<tr>
<th>CPU</th>
<th>Z80A</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAM</td>
<td>2 x 6116 CMOS static (4K total)</td>
</tr>
<tr>
<td>ROM</td>
<td>8K system monitor</td>
</tr>
<tr>
<td>DISPLAY</td>
<td>20 character 14 segment vacuum fluorescent</td>
</tr>
<tr>
<td>KEYBOARD</td>
<td>49-key 'QWERTY' layout</td>
</tr>
<tr>
<td>CASSETTE INTERFACE</td>
<td>165 baud serial read/write</td>
</tr>
<tr>
<td>LOUDSPEAKER</td>
<td>63mm (2.5 inch)</td>
</tr>
<tr>
<td>I/O</td>
<td>48 parallel system lines</td>
</tr>
<tr>
<td>SOFTWARE</td>
<td>Z80/8080 machine code plus resident line and two-pass assembler</td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td>240V 50Hz mains (plus four 1.5V dry batteries for memory back-up)</td>
</tr>
</tbody>
</table>

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Z80-P10, Z80-CTC and 8251 devices together with relevant data sheets for each device contained in an appendix. Applications discussed are respectively a traffic light system, clock, and an RS-232C selectable baud rate interface. Demonstration software is contained in ROM and entered by means of an appropriate monitor command and starting address.

CONCLUSIONS
The MPF–I PLUS is ideal for use both in the formal educational environment and for the individual working on his own. Hardware, software, and documentation have all been much improved. An alternative approach to learning assembly language programming involves the use of an assembler package based on a personal computer. Whilst the cost of such a package is commensurate with that of the Microprofessor (when one includes the cost of the microcomputer itself) it has several drawbacks as far as the electronic enthusiast is concerned. Firstly, if this is because few home computers are designed to extensive hardware development and, secondly, a computer designed primarily for the domestic and games market is unlikely to have the I/O capability of a machine intended for real-world control applications.

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DK Tronics graphics ROM board for ZX-81, including extra 2K RAM and defender tape. All for £15. N. J. Butters, 6 Lewis Street, Church Village, Pontypridd, Mid. Glam. Tel: (0443) 208305.

URGENT ULA chip for Z81 needed, up to £5.00; also graphic ROM for same needed, up to £10.00. C. Tuckwood (Chris), 19 Holmwood Avenue, Plymstock, Plymouth, Devon PL9 9JP.

WANTED Image intensifier tube Mullard type, XX1060 ideally. Must be in excellent working order, cash offered. M. Liffield, 11 Broadway, Rottbourne Cheney, Swindon, Wilts SN2 3BN.

PYE AM 25B crystal 4 metres 70-26 MHz TX RX, vgc £12. DX2001 receiver covers all bands to 30 MHz, £75 vgc. Mr. R. Pearson. Tel: Swansea BS28941.

WANTED Frame and plug or complete chassis CX1571 XY plotter for CD 1400 solatron oscillator. J. F. Radley, 28 Queen Street, Gedlington, Northants. Tel: (0536) 743524.

WANTED ASCII coded keyboard, upper and lower case plus positive strobe. Computer bits, etc. What have you? Cash waiting. Md Saunders, 10 Burncliffe Road, Thornaby, Cleveland. Tel: 0675 2LH.

COMPONENTS 16-5mm chassis punch, £2.50; timer display, £1.50, new. Many others, list large sae. No callers. G. A. Noble, 50 Croftth Road, Slough, Berks SL2 1HF.

ACE-Telecom Prestel TV converter (unwanted prize), new, still boxed, £45 o.n.o. Tel: (0482) 866566. Mr. E. Lovett, 3 Woodhall Way, Beverley, North Humberside HU17 7AZ.

ATARI 800, £190, 810 d/drive, £200. £50 interface, £100: also 80 col. printer, £260, or offers. Steve Nicholls, 18 Warwick Terrace, St. George’s Road, Barnstable, Devon EX32 7AR.

WANTED, please, pair Goodmans Asom L. S. chassis types 201/301. Also modern oscilloscope. Dual/1, would arrange collection. E. Bandwell-Jones, 15 Deer Park, Saltash, Cornwall PL12 6HE. Tel: Saltash 2144.

TEST equipment, including scope, for sale. Magazines, books, components. Work forces hobbyist to sell up!!! John Rinaldi—01-947 2020.

ELF II Micro expanded S/B based on 1602.jon. Steve Drew, 393 London Road, Ewell, Epsom, Surrey KT17 1TF.

SCOPE probe, XT1/XO switch. 4ft. lead with BNC plug. As new. £10 including postage. Tel: (0308) 897625. C. D. Swift, 373 London Road, Beverley, North Humberside HU17 7AZ.


SPEAKERS Pair Hi-fi, £45; Karlsbos: small £8, large £25. 3-manual organ, £195. N. J. Kolb, Elms Acre, Leaden Roding, Essex CM6 1QG. Tel: (0344) 777426.

PRE-WAR Ekco radio PB 289, press-button, motor tuned, £15. Isolating transformer, 500W 240V—240 C. T. 120V. W. Edwards, 2 Beach Road, Burton Bradstock, Bridport, Dorset DT6 4BZ. Tel: (0308) 866546.

UK101 12K RAM Bk Basic 4k WEMON 32 x 48 display, cased, £45 only. Tel: Chris Swift (0344) 777426. C. D. Swift, 373 London Road, Camberley, Surrey.

UK101 32 x 48 16x3 detailed manual, green screen vdu, software, £170. Tel: Reading 412885, after 6p.m. 501656 office. P. R. Border, 171 Halls Road, Tilehurst, Reading RG3 4TP.

HP-41C for sale, two single memory modules HP 82106A, £12 each. M. Williamson, 7 St. Andrews Road, Head Green, Cheadle, Cheshire, SK8 3ES. Tel: (061) 428 0656.

UK101 Computer (cased) + VDU 32x48, 24K RAM sound, speech, and lots more. Offers around £200. Mr. P. W. Mead, 4 Staverton Walk, Blandford, Dorset DT11 7TN. Tel: Blandford 55498.
all in your MAY issue!

TEST GEAR SPECIAL

FREE LOGIC DESIGN CARD NO. 3

PRACTICAL ELECTRONICS

MAY ISSUE ON SALE FRIDAY, APRIL 6th
THE 74121 is an integrated circuit monostable which can be triggered by either positive or negative edges depending upon the configuration employed. The device has complementary outputs and requires only two components (one resistor and one capacitor) to define the monostable pulse duration. The internal arrangement of the i.c. is shown in Fig. 7.1. Control inputs, A1, A2 and B are used to determine the trigger mode and may be connected in the following three ways:

(a) A1 and A2 connected to logic 0. The monostable will trigger on a positive-going transition at B.
(b) A1 and B connected to logic 1. The monostable will trigger on a negative edge applied to A2.
(c) A2 and B connected to logic 1. The monostable will trigger on a negative edge applied to A1.

It should be noted that, unlike some other monostable types, the 74121 is not retriggerable during its monostable period. This means that any input transitions received during the period of the output pulse will be ignored. Furthermore, in normal use, a recovery time equal in length to the monostable pulse should be allowed before attempting to re-trigger the device.

### PULSE STRETCHER USING THE 74121 MONOSTABLE

The following investigation involves using the 74121 monostable as a 'pulse stretcher’. As the name implies, a pulse stretcher is a device for elongating the duration of a pulse. A 74121 monostable is an ideal device to provide this function; it can be triggered by a pulse of fairly short duration and will continue to provide its fixed duration output pulse long after the input signal has reverted to its original state. The only requirement is that, to ensure reliable triggering, the input pulse should have a width of at least 50ns. For a 74121, the values of external timing resistor should normally lie in the range 1.5kΩ to 39kΩ. The minimum recommended value of external capacitor is 10pF; however, the maximum value is only dictated by leakage current of the capacitor employed. In practice this means that, if necessary, values of several hundred μF can be used. This results in a monostable device which can provide a very much wider range of monostable periods than the simple types discussed earlier. Typical values of monostable period for some common C–R values are given in Table 7.1.

In this particular example we are concerned with relatively long monostable periods, i.e. ones which we can detect using the I.E.D. indicators of the Logic Tutor. In practical circuits we will generally find that the monostable periods are a great deal shorter than this!

The circuit diagram of the pulse stretcher is shown in Fig. 7.2. The following links are required on the Logic Tutor:

- TRIGGER FROM S1

### Table 7.1. Typical values of CR and monostable period for the circuit of Fig. 7.1

<table>
<thead>
<tr>
<th>Resistance (R)</th>
<th>Capacitance (C)</th>
<th>Approx. Monostable Period (t)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10k</td>
<td>10p</td>
<td>70ns</td>
</tr>
<tr>
<td>2k</td>
<td>100p</td>
<td>150ns</td>
</tr>
<tr>
<td>10k</td>
<td>100p</td>
<td>700ns</td>
</tr>
<tr>
<td>2k</td>
<td>1n</td>
<td>1.5μs</td>
</tr>
<tr>
<td>10k</td>
<td>1n</td>
<td>7μs</td>
</tr>
<tr>
<td>2k</td>
<td>10n</td>
<td>15μs</td>
</tr>
<tr>
<td>10k</td>
<td>10n</td>
<td>70μs</td>
</tr>
<tr>
<td>2k</td>
<td>100n</td>
<td>150μs</td>
</tr>
<tr>
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<td>1.5ms</td>
</tr>
<tr>
<td>10k</td>
<td>1μ</td>
<td>7ms</td>
</tr>
<tr>
<td>2k</td>
<td>10μ</td>
<td>15ms</td>
</tr>
<tr>
<td>10k</td>
<td>10μ</td>
<td>70ms</td>
</tr>
<tr>
<td>2k</td>
<td>100μ</td>
<td>150ms</td>
</tr>
<tr>
<td>10k</td>
<td>100μ</td>
<td>700ms</td>
</tr>
</tbody>
</table>
practical electronics

provide a symmetrical square wave

clock operating at approximately

11kHz. The output of the clock is taken to a 74121 monostable which has a variable resistance connected as part of its timing circuit as shown in Fig.

7.3. The configuration and values employed produces a monostable period which is adjustable over a range of approximately 10:1 (30µs maximum to 3µs minimum approximately). The output of the monostable is repetitive since it is retriggered on the falling edge of each clock cycle (the clock cycle has a period of approximately 90µs which is, of course, smaller than the monostable period). The monostable output thus consists of a train of pulses having a duty cycle which may be varied by means of the variable resistor. Typical waveforms for the pulse generator are shown in Fig. 7.4.

Fig. 7.4. Typical waveforms for the pulse generator of Fig. 7.3

Now we will look at a problem. Suppose that a certain logic control system requires an input signal consisting of a logic 1 pulse for precisely the duration of one complete clock cycle. The input signal is to be obtained from a push button whilst the output signal should not be retriggerable until the push button is released and pressed again. The problem can be solved using the devices and techniques described earlier.

DE MORGAN'S THEOREM

De Morgan’s theorem is an extremely useful tool in the analysis and simplification of logic expressions. By applying De Morgan’s theorem it is possible to construct arrangements of logic gates using either NAND or NOR (or a mixture of both) to satisfy any desired logical function. Furthermore, the technique can help us to use the minimum number of logic gates. This process, which is essential in many practical applications, is known as “minimisation”.

In Part Six we mentioned that a particular pattern in the output column of a truth table could help us find an alternative Boolean expression for the gate concerned. It is worth looking at this again as a prelude to De Morgan’s theorem.

Table 7.2 shows the truth table for two-input NAND and two-input OR gates, arranged with their output columns side by side. It should immediately be obvious that, although the two output columns look almost the same, the three 1’s and 0’s in each column are not quite coincident. If, however, we were to invert the A and B inputs for one of the gates and then compare the truth tables again we would get two identical output columns, as shown in Table 7.3. We therefore conclude that the NAND function is identical to the OR function with both inputs inverted. Thus, for two

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>A+B</th>
<th>A•B</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
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<td>1</td>
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</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 7.2. Truth tables for two-input NAND and OR gates
AND (NOT B). Writing this in Boolean complement cancels, gives:
this is written:
A · B = ¬A + ¬B.
Complementing each side of the expression, and recalling that a double complement cancels, gives:
A · B = ¬A + ¬B.
Had we started with NOR rather than NAND gates, we would have obtained the truth tables shown in Table 7.4. This in turn yields the result that
\[
\begin{array}{c|c|c}
A & B & A+B \\
0 & 0 & 1 \\
0 & 1 & 0 \\
1 & 0 & 0 \\
1 & 1 & 1 \\
\end{array}
\]  
\[
\begin{array}{c|c|c}
A & B & A+\overline{B} \\
0 & 0 & 1 \\
0 & 1 & 0 \\
1 & 0 & 0 \\
1 & 1 & 1 \\
\end{array}
\]

Table 7.4: Comparison of truth tables for a two-input NOR gate and a two-input AND gate with inverted inputs

NOT (A OR B) is the same as (NOT A) AND (NOT B). Writing this in Boolean form gives:
\[
\overline{A + B} = \overline{A} \cdot \overline{B}.
\]
Similarly, complementing both sides gives:
\[
A + B = \overline{A} \cdot \overline{B}.
\]  
These two expressions, which jointly constitute De Morgan's theorem are, of course, exactly the same as those arrived at earlier. Whichever type of gate we start with the result is the same. So much for the theorem, now let's see what we can do with it!
Suppose that we need to construct a two-input OR gate but we only have two-input NAND gates available. De Morgan makes it simple; all we need to do is to invert each input, using NAND gates with the two inputs tied together to act as an inverter, and then apply the outputs to a third NAND gate, as shown in Fig. 7.5. If, alternatively, we had a quantity of two-input NOR gates and needed a two-input AND gate this could be easily achieved by means of the arrangement shown in Fig. 7.5. Readers wishing to put De Morgan's theorem to the test may like to try the following exercises based on the 7400 quad two-input NAND and 7402 quad two-input NOR gates.

**Fig. 7.5.** Two-input OR gate from two-input NAND gates

EXCLUSIVE-OR FROM NAND
This investigation shows how a two-input OR gate can be built using three of the four two-input NOR gates of a 7402 following the arrangement shown in Fig. 7.6. Insert the 7402 into socket A of the Logic Tutor (checking that pin 1 aligns with 'A1') and make the following connections:
A1 to A14 (A)
A2 to S3 (S3 acts as the A input)
A3 to A2
A4 to A13 (B)
A5 to S4 (S4 acts as the B input)
A6 to A5
A7 to 0V (OV)
A15 to D1 (D1 indicates the output)
A16 to +5V (positive supply)

Operating S3 and S4 whilst observing D1 should confirm that the combination behaves as an AND gate. D1 should only become illuminated when both S3 and S4 are producing logic 1.

EXCLUSIVE-OR FROM NAND
As a final example of the use of De Morgan's theorem, and of the technique of minimisation, let us assume that we need an Exclusive-OR gate but only have NAND gates available. (The 7400 quad two-input NAND gate is, in any event, far more plentiful than the 7402 quad two-input Exclusive-OR gate.) To make the example easier to follow we shall divide the task into several simple stages and draw the logic arrangement of each.

**Stage 1.** Write down the Boolean expression for the desired output. In this case we require the output, X, to be:
\[\overline{A} + \overline{A} \cdot \overline{B} \cdot \overline{B} = \overline{A} \cdot \overline{B} \cdot \overline{A} \cdot \overline{B}.
\]

**Stage 2.** Separate the expression into its constituent parts and identify the logical connective between them. In this case we have two expressions: A AND (NOT B) and B AND (NOT A) which are OR'd together to produce the final output, X. This allows us to establish the nature of the last logic gate (OR in this case), and we can then write down the Boolean expressions for its inputs, as shown in Fig. 7.7(b). We shall divide the task into several simple stages and draw the logic arrangement of each.

**Stage 3.** Repeat the process of Stage 2 again dividing the Boolean expressions into constituent terms or expressions. The A AND (NOT B) term, for example, can be produced by using an AND gate fed with inputs of A and B. Similarly, B AND (NOT A) can be produced by a further AND gate which, in this case, is fed with inputs of B and A.

**Stage 4.** By further repetition (if necessary) one should eventually arrive at individual terms (e.g. A, B, etc.).
Where these are inverted (e.g. \( \bar{A} \)) this can be easily achieved by means of additional inverter stages. Now draw the complete logic diagram, as shown in Fig. 7.7(d). Check that there are as many gates present as there are logical connectives (i.e. \( \land, \lor, \) and \( \neg \)) in the original expression. In this case there are five such connectives and we have numbered them below in the order in which they have been dealt with:

\[
\begin{align*}
A & \rightarrow S3 \\
A & \rightarrow \text{A1} \\
A & \rightarrow \text{A14} \\
A & \rightarrow S4 \\
A & \rightarrow \text{A4} \\
A & \rightarrow \text{A11} \\
A & \rightarrow \text{A7} \\
A & \rightarrow \text{A10} \\
A & \rightarrow \text{A12} \\
A & \rightarrow \text{A13} \\
A & \rightarrow \text{A15} \\
A & \rightarrow \text{A16} \\
B & \rightarrow S3 \\
B & \rightarrow \text{A1} \\
B & \rightarrow \text{A14} \\
B & \rightarrow S4 \\
B & \rightarrow \text{A4} \\
B & \rightarrow \text{A11} \\
B & \rightarrow \text{A7} \\
B & \rightarrow \text{A10} \\
B & \rightarrow \text{A12} \\
B & \rightarrow \text{A13} \\
B & \rightarrow \text{A15} \\
B & \rightarrow \text{A16} \\
\end{align*}
\]

\( \text{Stage 5.} \) Replace each gate by its De Morgan equivalent using NAND or NOR, as required. Remember that inverters may be produced by linking two, or more, inputs together. In this case we are constrained to using two-input NAND gates only, the result of using these connected to form the required OR, AND and inverters, is shown in Fig. 7.7(e). At this stage the logic gate arrangement may begin to look rather complex and it is, therefore, often a good idea to number the logic gates.

\( \text{Stage 6.} \) Simplify the arrangement arrived at in Stage 5 by removing all redundant gates (e.g. two inverters following one another) and then group together all of the inputs. In this particular example gates 4, 7, 6 and 8 are redundant. Sketch the final logic arrangement and, if desired, check by means of Boolean algebra following the logical inputs through, stage by stage, from input to output.

Readers may now like to check for themselves that the Exclusive-OR arrangement really does work! Since we shall require a total of five gates, two 7400's will be required. These should be inserted into sockets A and B of the Logic Tutor, taking care to observe the usual convention of pin 1 to 'A1' etc. The following links are required:

\[
\begin{align*}
\text{A1} & \rightarrow S3 \\
\text{A2} & \rightarrow \text{A1} \\
\text{A3} & \rightarrow \text{A14} \\
\text{A4} & \rightarrow S4 \\
\text{A5} & \rightarrow \text{A4} \\
\text{A6} & \rightarrow \text{A11} \\
\text{A7} & \rightarrow 0V \\
\text{A10} & \rightarrow \text{B2} \\
\text{A12} & \rightarrow \text{A2} \\
\text{A13} & \rightarrow \text{B1} \\
\text{A15} & \rightarrow \text{A5} \\
\text{A16} & \rightarrow +5V \\
\text{B3} & \rightarrow \text{D1} \\
\text{B7} & \rightarrow 0V \\
\text{B16} & \rightarrow +5V \\
\end{align*}
\]

\( \text{D1 should, of course, become illuminated when either S3 or S4 is producing a logic 1. It should not, however, remain illuminated when both S3 and S4 are at logic 1, or both at logic 0.} \)

**KARNAUGH MAPS**

Karnaugh Maps form the basis of a powerful graphical technique which can be used to minimise logic systems. The map simply consists of a number of cells linked together, each cell representing a unique logical condition. The number of cells in the map depends upon the number of variables present; a system with one variable will have two cells, a system with two variables will have four cells, a system with three variables will have eight cells, and so on. In general, a system with \( n \) variables can be mapped using \( 2^n \) cells. To put this into perspective let's consider a simple system with just two variables, A and B. The four cells of the map are arranged in two columns (A and \( \bar{A} \)) and two rows (B and \( \bar{B} \)), as shown in Fig. 7.8. The cell coincident with column \( \bar{A} \) and row \( B \) is equivalent to the Boolean condition (NOT A) AND (NOT B) or \( \bar{A} \bar{B} \).

\[
\begin{align*}
\text{Fig. 7.8. Karnaugh Map for two variables}
\end{align*}
\]

In terms of the truth table this corresponds to the input condition \( A = 0, B = 0 \). Fig. 7.9 shows all four possible input conditions together with their corresponding cells on the Map.

\[
\begin{align*}
\text{Fig. 7.9. Relationship between a Karnaugh Map and a truth table}
\end{align*}
\]
To show how the Karnaugh Map works, a useful exercise is to consider the pattern produced by some familiar two-input logic gates: AND, NAND, OR and NOR. These are shown in Fig. 7.10. The shaded area in each map is equivalent to a logic 1 in the output column of the respective truth table. Sometimes 1’s and 0’s are used instead of shaded and unshaded areas, respectively. In this series, we shall use shading exclusively, if for no other reason than it is a little clearer! The maps shown in Fig. 7.10 clearly show the complementary relationships which exist between AND and NAND, and OR and NOR. What else can we do with the maps?

![Fig. 7.10. Karnaugh Maps for AND, NAND, OR and NOR gates with two inputs](image)

A single shaded cell involves two variables. Adjacent cells can be grouped together and, by so doing, we can eliminate one of the two variables. Let’s take the OR gate for example. The three shaded cells can be considered as two adjacent pairs with one cell common to both, as shown ringed in Fig. 7.11. One of the pairs occupies all of column A, the other occupies all of row B. The shaded area is thus, as we might expect A OR B or, in Boolean, \( A + B \). We could, however, have represented the shaded area using the expressions for each of its constituent cells. The Boolean expression for this would be \((A \cdot B) + (A \cdot B) + (A \cdot B)\). Since the shaded area has remained the same we must conclude that:

\[
A + B = (\bar{A} \cdot B) + (A \cdot \bar{B}) + (A \cdot B)
\]

At first sight this result may not appear to be very useful and we may have easily arrived at it from the truth table. Let’s go on, however, to see the result of carrying out a similar exercise using a NOR gate. The shaded area is the opposite (complement) of that for the corresponding OR gate. It should be noted that the shaded area is coincident with the \(\bar{A}\) column and the \(\bar{B}\) row. It may thus be represented by \((\text{NOT } A)\) AND \((\text{NOT } B)\) or, in Boolean terms, \(\bar{A} \cdot \bar{B}\). We could, however, also represent it by \(\text{NOT } (A \text{ OR } B)\) or \(\bar{A} + \bar{B}\). Thus we may conclude that:

\[
\bar{A} + \bar{B} = \bar{A} \cdot \bar{B}
\]

If this doesn’t ring a loud bell—it should! It’s simply De Morgan’s theorem yet again.

Karnaugh Maps really come into their own when it is necessary to simplify complex logic arrangements. This usually occurs when we are dealing with gate circuits which have three, or more, inputs. A Karnaugh Map with three variables is shown in Fig. 7.12.

![Fig. 7.11. Grouping together adjacent cells in a Karnaugh Map](image)

![Fig. 7.12. Karnaugh Map for three variables](image)

Here there are \(2^3 = 8\) cells which we have arranged in two columns and four rows. (We could have used four columns and two rows, but the result is the same.) Note that \(B, \bar{B}, C\) and \(\bar{C}\) cover two rows each and an overlap is arranged so that all eight different logical states are included. Each of the eight cells has a unique Boolean expression in terms of the three variables, \(A, B\) and \(C\). Where two adjacent cells are grouped together, the result is a Boolean expression which eliminates one of the three variables, i.e. the resulting Boolean expression involves only two variables. Similarly, if four adjacent cells are grouped together the resulting Boolean expression involves one single variable only.

When dealing with adjacent cells it is important to note that the map is continuous in either axis. This means that it is possible to ‘wraparound’ the opposite ends to produce adjacent cells which may otherwise appear to be widely separated. Fig. 7.13 illustrates this point. Here we have grouped together two cells to form a two-variable expression: \(A \text{ AND } (\text{NOT } C)\) or, in Boolean form, \(A \cdot C\).

To conclude this section on Karnaugh Maps it is worth considering a simple example of their use. Suppose that we have been asked to provide a simple electronic system to assist in a voting procedure. There are to be three judges and a simple majority vote is required to determine a successful candidate. Each member of the judging panel is equipped with a switch with which he makes a simple ‘yes/no’ decision. If two, or more, of the judges vote ‘yes’ then a light is to come on. Let us suppose that the three judges are called Andrew, Brian and Charles. There are four conditions in which a candidate would be successful:

<table>
<thead>
<tr>
<th>Andrew</th>
<th>Brian</th>
<th>Charles</th>
<th>Boolean Equivalent</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO</td>
<td>YES</td>
<td>YES</td>
<td>A \cdot B \cdot C</td>
</tr>
<tr>
<td>YES</td>
<td>NO</td>
<td>YES</td>
<td>A \cdot B \cdot C</td>
</tr>
<tr>
<td>YES</td>
<td>YES</td>
<td>NO</td>
<td>A \cdot B \cdot C</td>
</tr>
<tr>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>A \cdot B \cdot C</td>
</tr>
</tbody>
</table>

Plotting the Boolean expressions on the Karnaugh Map gives the resulting area marked in Fig. 7.14. The shaded area comprises three pairs of adjacent cells, the Boolean expressions for which are: \(A \cdot C, B \cdot C\) and \(A \cdot B\). The output, \(X\), of our logic arrangement (corresponding to the entire shaded area) should thus be:

\[
X = (A \cdot C) + (B \cdot C) + (A \cdot B)
\]

This can be obtained from a three-
input OR gate preceded by three two-input AND gates in an arrangement similar to that of Fig. 7.15. Note that, had we not attempted to simplify the expression first, we might have ended up with a much more complex arrangement.

![Fig. 7.14. Karnaugh Map for the majority vote](image)

Fig. 7.14. Karnaugh Map for the majority vote

**BINARY COUNTERS**

In Part Five we showed how a D-type bistable could form the basis of a simple binary counter. With such a circuit, a single bistable stage produces, in any given time interval, half as many output pulses as clock input pulses, thus effectively dividing the input frequency by two. This concept can be extended in order to produce circuits which can count the number of input pulses. If several bistables are connected in tandem such that the Q output drives the subsequent CLOCK input, the state of the Q outputs is dependent upon the number of input pulses received. If we take the simple two stage arrangement shown in Fig. 7.16, for example, the state of the Q outputs in response to a number of clock input pulses, n, is shown below:

<table>
<thead>
<tr>
<th>n</th>
<th>Q1</th>
<th>Q2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>etc</td>
<td>etc</td>
<td>etc</td>
</tr>
</tbody>
</table>

![Fig. 7.15. Logic arrangement for the majority vote](image)

Fig. 7.15. Logic arrangement for the majority vote

**Fig. 7.16. Simple two-stage binary divider**

We have, of course, assumed that the initial state of both the Q outputs is logic 0. In practice this could be easily accomplished using the CLEAR inputs provided on the bistables. It should be noted that the pattern of 0's and 1's repeats itself after the third clock input pulse, i.e. the output state for a count of 4 is the same as that for a count of 0. Furthermore, if we just concentrate on the first four states (n = 0 to n = 3), the Q outputs are a binary representation of the number of input pulses, Q2 being the most significant bit (MSB), whilst Q1 is the least significant bit (LSB). The circuit thus effectively counts to 3 and then repeats itself. If we wish to know the state of the count (number of pulses which have arrived) all we need to do is examine the Q2 and Q1 outputs and convert back from binary.

A four stage binary counter is shown in Fig. 7.17. Here four J-K bistable elements have been connected in cascade. The J and K inputs of each stage are connected to logic 1, and the Q output of each stage is connected to the CLOCK input of the subsequent stage. The circuit will count 15 input pulses before reverting to an output state of zero and recommencing. Since there are 16 different output states (including 0000), the circuit forms a divide-by-16 arrangement. We shall now examine a practical divide-by-16 arrangement based upon the 7473 bistable.

**Fig. 7.17. Four-stage binary divider using JK bistables (NB All J and K inputs are taken to logic 1)**

**BINARY + 16 COUNTER USING TWO 7473's**

The circuit of the 7473 ÷16 binary counter is shown in Fig. 7.17. In order to enable operation as a binary divider, the J and K inputs are all taken to logic 1. So that the counter can be reset to zero at the start of counting, the CLEAR inputs are all linked together and taken to S3. A logic 0 from this switch resets the counter whereas a logic 1 permits normal counting (remember that the CLEAR input is "active low"). The 7473's should be inserted in sockets A and B carefully ensuring that pin-1 aligns with socket 1 in each case. The following interconnecting links are required:

- A1 to clock
- A2 to A6
- A3 to logic 1
- A4 to +5V (positive supply)
- A5 to A14
- A6 to B2
- A7 to logic 1
- A11 to D3 (D3 indicates the Q2 output)
- A12 to A7
- A13 to 0V (0V)
- A14 to D4 (D4 indicates the Q1 output)
- A16 to A3
- B1 to A11
- B2 to B6
- B3 to logic 1
- B4 to +5V (positive supply)
- B5 to B14
- B6 to S3 (S3 provides the reset facility)
- B7 to logic 1
- B11 to D1 (D1 indicates the Q4 output)
- B12 to B7
- B13 to 0V (0V)
- B14 to D2 (D2 indicates the Q3 output)
- B16 to B3 (Total of 24 links)

It should be noted that the l.e.d.s have been arranged in the conventional...
order with the most significant bit appearing on the left (D1) and the least significant on the right (D4).

S3 should be set initially to produce logic 0. D1 to D4 should now all be extinguished, indicating an output of 0000 in the reset condition. Wait until the clock goes to OV (I.e.d. off) and then press S3 again. This produces a logic 1 on the CLEAR line and counting should commence with the first falling (1->0) clock pulse. When this happens (at the point where the clock I.e.d. goes off again), D4 should become illuminated indicating a count of 0001 (binary 1). After the next clock pulse, and again on the falling edge, the count should increase by 1 to 0010 (binary 2). Note that all changes are initiated on the falling edge of the clock pulse. Carefully observe the subsequent binary counting sequence and confirm that the arrangement follows the timing diagram shown in Fig. 7.18 and the logic state table shown below:

<table>
<thead>
<tr>
<th>Clock pulse number</th>
<th>Q4</th>
<th>Q3</th>
<th>Q2</th>
<th>Q1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (reset)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>14</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>15</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

The counting sequence should then recommence with 0000. At any time, however, it should be possible to interrupt the counting sequence using S3 to reset the count to 0000.

**DECADE COUNTERS**

In many applications we require counters which are capable of counting to a base other than a power of 2. We might, for example, be concerned with packing items into boxes in batches of six, ten or twelve. At a particular stage in the process a counter would be required to check that the correct number of items are present before sealing the boxes. In order to do this, we can easily modify the basic binary counter such that a reset signal is automatically generated to clear the counter when a specific state of count has been reached.

Taking the decade counter (+10) as an example, let us imagine that an electrical component manufacturer produces 13A plugs using a simple automated assembly line. After the assembly process is complete, each plug is visually inspected on a moving conveyor belt, before being passed to the packing machine. The machine arranges the plugs into batches of ten and then seals them into a plastic container in which the wholesaler receives the plugs.

After inspection, the plugs can be detected by a photocell as they arrive at the packing machine. The photocell can be arranged such that, after suitable processing, a 0->1->0 pulse is produced as each plug passes by. This pulse is fed to the clock input of a counter which counts to ten before activating the heat-shrink sealing process. The state of the count corresponding to 10 (binary 1010) can be easily detected using a logic gate which not only initiates the sealing process but also resets the counter to zero (binary 0000). The counter is thus made ready for the next batch of 10 plugs.

The process is shown in block schematic form in Fig. 7.19. The circuit of a typical decade counter is shown in Fig. 7.20. This arrangement uses a two-input NAND gate to detect the count of 10 (binary 1010). Note that this is only a transitory state and the counter will be immediately cleared whenever Q2 and Q4 are both at logic 1. The counter thus has ten states (0 to 9) and counting will recommence with an output of 0000 immediately after resetting.

The +16 arrangement using two 7473's can easily be modified for use as a decade counter by adding an additional 7400 (fitted in socket C) and making the following links:

- C1 to D1
- C2 to D3
- C3 to B6 (remove the link from S3 to B6)

![Fig. 7.18. Timing diagram for the four-stage binary divider of Fig. 7.17](image_url)

![Fig. 7.19. Simplified block schematic of a batch counting system](image_url)
The decade counter should follow the timing diagram shown in Fig. 7.21 and obey the logic state table shown below:

<table>
<thead>
<tr>
<th>Clock pulse number</th>
<th>Q4</th>
<th>Q3</th>
<th>Q2</th>
<th>Q1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>10 (0)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>11 (1)</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>12 (2)</td>
<td>0</td>
<td>0</td>
<td>1</td>
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Please Note
In Part 6 Table 6.8 should refer to Fig. 6.8 and Table 6.9 should refer to Fig. 6.9. Table 6.10 should be ignored.

NEXT MONTH: We will be looking at an intruder alarm and also a traffic lights simulator.

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If you order goods from Mail Order advertisements in this magazine and pay in advance of delivery, it is the code's requirement that the advertiser should become insolvent or bankrupt, provided:

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2. You write to the Publisher of PRACTICAL ELECTRONICS summarising the situation not later than two months from the day you sent your order and not later than 28 days from the day you sent your order.

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We guarantee to meet claims from readers made in accordance with the above procedure as soon as possible after the Advertiser has been declared bankrupt or insolvent. This guarantee covers only advance payment sent in direct response to an advertisement in this magazine. If, for example, payment made in response to catalogues etc. received as a result of an advertisement, the code requires advertisers to fulfill orders within 28 days, unless a longer delivery period is stated. Where goods are returned undamaged within seven days, the purchaser's money must be refunded.

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Simply plugs into expansion port on your Spectrum

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1984 catalogue

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Full construction details in Projects Book 5.

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Full construction details in Projects Book 5.

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Despatch by return of post where goods available.
LOGIC SOURCES
The standard TTL levels for 0 and 1 are well defined. In many cases, a circuit will need to use one of these levels to either prevent or ensure particular circuit behaviour, e.g. to be certain that the RESET input of a latch is kept inactive. A logic 0 or 1 source (as appropriate) is then used to drive the appropriate gate input. Some of the standard ways of generating logic 0 and logic 1 are shown below. Also included is the number of standard TTL gates which can be connected to each type of source.

TTL SUPPLIES
TTL operates from a single +5V d.c. supply. At no time should the voltage at the i.c. supply pin exceed +7V. The supply should ideally be regulated to within 250mV of the nominal +5V, and the ripple should be less than 250mV. The greater the number of i.c.s in a circuit, the more important is the need for a well-regulated supply. When designing power supplies for TTL, there are three important requirements to be satisfied:

- A regulated supply of voltage.
- Low-impedance supply distribution.
- Effective supply decoupling.

These are all necessary characteristics if a TTL circuit's behaviour is to be unaffected by its power supply.

LOAD CURRENT
Designing a power supply unit (p.u.s.) for a TTL circuit requires a knowledge of the maximum current to be supplied. The TTL data books give supply figures in either mA or mW, quoted either per gate or per-package. Any mW figures should first be converted to mA by dividing by 5. The total current for each package is then worked out by multiplying any per-gate figures by the number of gates in the i.c. (whether or not they are actually used). Then total up the current for all of the TTL i.c.s, and add in any other circuit loads (relays, l.e.d.s, etc.). This gives the expected overall load current for the circuit. A useful p.u.s. design current is obtained by adding a safety margin of (say) 20% to this last figure.

PSUs FOR TTL
The most convenient p.u.s. for TTL essentially use a mains transformer, a bridge rectifier and an i.c. voltage regulator. This arrangement provides an extremely stable, protected supply at reasonable cost, using only a small number of readily available components. By selection of an appropriate transformer, bridge and regulator, the same circuit may be used for a wide range of applications. The circuit shown below is suitable for use with TTL circuits which impose a load of up to 1A.

SUPPLY DISTRIBUTION
Good power distribution is essential in any TTL circuit. The power supply wiring must have a low impedance at all frequencies up to around 35MHz (125MHz for Schottky TTL). This prevents sudden bursts of high speed operation in one part of the circuit affecting another area via the power supply lines. A low impedance supply requires both good distribution and good decoupling (see later). A number of simple rules will help avoid problems with supply distribution:

1. Use wide p.c.b. tracks for the main 0V and +5V rails.
2. The main 0V rail should ideally be at least 8mm wide.
3. The main +5V rail should ideally be at least 8mm wide.
4. Try to run the main 0V track around the edge of the board.
5. Keep connections between the i.c. and 0V short.
6. Use supply leads rated at 5-10 times the expected load.
7. Use connectors rated at 5-10 times the expected load.
8. Keep supply tracks and leads as short as possible.

Regulators = 78L05 (0.1A), 78M05 (0.5A), 7805 (1A), LM309K (1-2A), 78H05 (5A).