

PRACTICAL

ELECTRONICS

JULY 1984

90p

FIBRE OPTICS



Simple Logic Analyser

SLIDE DISSOLVE CONTROL
ADD ON SUB-WOOFER

'HANDS ON'
QL

Low-price robots from POWERTRAN

- hydraulically powered
- microprocessor controlled

The UK-designed and manufactured range of Genesis general purpose robots provides a first-rate introduction to robotics for both education and industry.

Each robot in the Genesis range has a self-contained hydraulic power source operated from single phase 240 or 120v AC or from a 12v DC supply. Up to six independent axes are capable of simultaneous operation and all except the grip axis have sensing devices fitted to provide positional control by a closed loop system based on a dedicated microprocessor. Movement sequences can be programmed by means of a hand-held controller or the systems can be interfaced with an external computer via a standard RS232C link.



GENESIS P101

The top-of-the-range P102 has dual speed control, enhanced memory and double acting cylinders for increased torque on the wrist and arm joints. There is position interrogation via the RS232C interface, increasing the versatility of computer control and inputs are provided for machine tool interfacing.

All Genesis robots are available either ready-built or in kit form. The latter provides not only extra economy but also valuable additional training as an assembly project.



GENESIS P102



HEBOT II Turtle-type robot

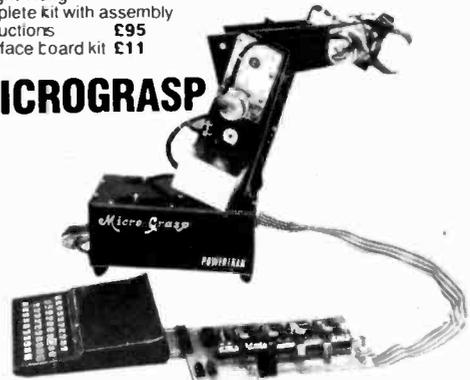
For a little over £100, Herbot II takes programming off the VDU and into the real world. Each wheel is independently controlled by a computer, enabling the robot to perform an almost infinite number of moves. It has blinking eyes, a two-tone bleep and a solenoid-operated pen to chart its moves. Touch sensors, coupled to its shell return data about its environment to the computer enabling evasive or exploratory action to be calculated.

The robot connects directly to an I/O port or, via the interface board, to the expansion bus of a ZX81 or other microcomputer.

HEBOT II

Weight 1.8kg
complete kit with assembly instructions £95
Interface board kit £11

MICROGRASP



A real programmable robot for under £300! Micrograsp has an articulated arm jointed at shoulder, elbow and wrist positions. The entire arm rotates about its base and there is a motor driven gripper. All five axes are motor driven and four of these are servo controlled giving positive positioning. The robot can be controlled by any microcomputer with an expansion bus – the Sinclair ZX81 being particularly suitable.

MICROGRASP

Weight 8.7kg, max. lifting capacity 100g
Robot kit with power supply £215.00

Universal computer interface board kit £57.00
23 way edge connector £3.00
ZX81 peripheral/RAM pack splitter board £3.50

GENESIS P101

Weight 34kg, max lifting capacity 1.8kg
6-axis model (kit form) £750
6-axis complete system (kit form) £1050

GENESIS P102

Weight 36kg, max lifting capacity 2kg
6-axis system (kit form) £1476
Powertran Cortex microcomputer self-assembly kit £295.00

Cortex 16 bit microcomputer

Goods subject to availability. All prices exclusive of V.A.T. and correct at time of going to press.



POWERTRAN cybernetics Ltd.

PORTWAY INDUSTRIAL ESTATE, ANDOVER, HANTS SP10 3PE. TEL (0264) 64455

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PRACTICAL ELECTRONICS

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No. 7

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OUR AUGUST ISSUE WILL BE ON SALE FRIDAY, JULY 6th, 1984
(for details of contents see page 17/8 of Micro-file)

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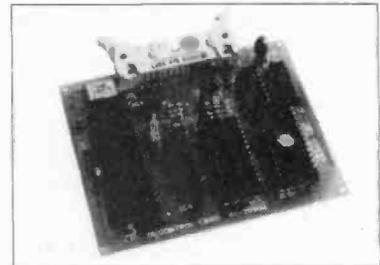
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Computer Products

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| | | |
|-----------------------------|----------|-------|
| C12 Computer Cassette | 21-00012 | 0.55 |
| BBC to Centronics Printer | 03-10019 | 7.25 |
| BBC to 25 way D Male | 03-10021 | 4.50 |
| 25 way D Socket | 10-25200 | 1.90 |
| 25 way D Plug | 10-25100 | 1.30 |
| Cover for 25 way D | 10-25322 | 0.93 |
| 20 up Eprom Eraser | 40-82100 | 31.25 |
| Z80 A Industrial Controller | 40-82000 | 49.95 |
| 6802 Industrial Controller | 40-68020 | 49.95 |
| 6502 Industrial Controller | 40-65020 | 49.95 |
| Z8 Basic/Debug Controller | 41-00904 | 50.00 |

Nicad Batteries & Chargers

Minimum life 600 (300 PP3 size) full charge/discharge cycles. Batteries must be charged from a constant current source only. All batteries are supplied only with a residual charge and should be charged before used.

| | | | | | |
|--------------------|-------------------|--------|----------|------|-------|
| AA | 1.2V | 500MAH | 01-12004 | 1.9 | 10.49 |
| C | 1.2V | 2.2AH | 01-12024 | 2.35 | 1.99 |
| D | 1.2V | 4.0AH | 01-12044 | 3.05 | 2.85 |
| PP3 | 8.4V | 110MAH | 01-84054 | 3.70 | 3.50 |
| CH1/22 PP3 Charger | 11mA for 16 hours | | 01-00159 | | 4.30 |

| | | | | | |
|------------------------------|--|--|----------|--|------|
| CH8/RX Multi-purpose Charger | | | 01-02204 | | 9.40 |
|------------------------------|--|--|----------|--|------|

Will recharge AA, C, D and PP3 size cells with automatic voltage selection. Will recharge following combination: 6x D, 6x AA, 6x C, 2x PP3, 2x D + 2x C, 2x D + 2x AA, 2x D + 1x PP3, 2x C + 2x AA, 2x C + 1x PP3, 2x AA + 1x PP3.

| | | |
|-----------------|----------|------|
| Battery Adaptor | 01-12001 | 0.96 |
|-----------------|----------|------|

Sold in pairs: one to convert AA size to C size and one to convert C to D size. Both may be used together to convert an AA to D size.

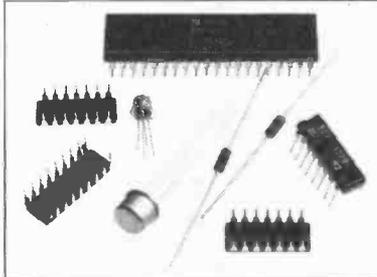
Semiconductors

Linear IC's

| | | | |
|---------|------------------------------|----------|------|
| LM301AN | DIL version | 61-03011 | 0.44 |
| LM308CN | DIL version | 61-03081 | 0.65 |
| LM311CN | Popular comparator | 61-00311 | 0.46 |
| LM324 | Low power quad op amp | 61-03240 | 0.67 |
| LM339N | Low power quad comparator | 61-03390 | 0.68 |
| LM346 | Programmable quad op amp | 61-00346 | 3.72 |
| LF347 | Quad Bi-FET op amp | 61-00347 | 1.82 |
| LM348 | Quad 741 type op amp | 61-03480 | 1.26 |
| LF351 | Bi-FET op amp | 61-03510 | 0.49 |
| LF353 | Dual version of LF351 | 61-03530 | 0.76 |
| LM380N | IW AF power amp | 61-00380 | 1.00 |
| NE555N | Multi-purpose low cost timer | 61-05550 | 0.45 |

for a better service.

| | | | |
|-----------|---|----------|------|
| NE556N | Dual version of the 555 | 61-05560 | 0.50 |
| uA741CN | DIL low cost op amp | 61-07411 | 0.22 |
| uA747CN | Dual 741 op amp | 61-07470 | 0.70 |
| uA748CN | 741 with external frequency comp | 61-04780 | 0.40 |
| HA1388 | 18W PA from 14V | 61-01388 | 2.75 |
| TDA2002 | 8W into 2 ohms power amp | 61-02002 | 1.25 |
| ULN2283 | 1W max. 3-12V power amp | 61-02283 | 1.00 |
| MC3357 | Low power NBFM IF system and detector | 61-03357 | 2.85 |
| ULN3859 | Low current dual conversion NBFM IF and detector | 61-03859 | 2.95 |
| LM3900 | Quad norton amp | 61-39000 | 0.60 |
| LM3909N | 8-pin DIL LED flasher | 61-39090 | 0.68 |
| KB4445 | Radio control 4 channel encoder and RF | 61-04445 | 1.29 |
| KB4446 | Radio control 4 channel receiver and decoder | 61-04446 | 2.75 |
| ICM7555 | Low power CMOS version of timer | 61-75550 | 0.98 |
| ICL8038CC | Versatile AF signal generator with sine/square/triangle OFs | 61-08038 | 4.50 |
| TK10170 | 5 channel version of KB4445 | 61-10170 | 1.87 |
| HA12002 | Protection monitor system for amps, PSUx, TXs etc | 61-12002 | 1.22 |
| HA12017 | 83dB S/N phono preamp 0.001% THD | 61-12017 | 0.80 |
| MC14412 | 300 baud MODEM controller (Eduro/US specs) | 61-14412 | 6.85 |



Microprocessor & Memories

| | | | |
|----------|--------------------------------|----------|-------|
| Z80A | Popular and powerful 8-bit CPU | 26-18400 | 3.40 |
| Z80AP10 | 2 port parallel input/output | 26-18420 | 2.95 |
| Z80A CTC | 4 channel counter/timer | 26-18430 | 2.90 |
| Z8671 | Z8 Micro comp. and Basic | 26-08671 | 17.50 |
| 6116-3 | 16K (2kx8) CMOS RAM 200nS | 26-36116 | 6.68 |
| Z6132-6 | 32K (4kx8) quasi RAM 350nS | 26-06132 | 15.00 |
| 4116-2 | 16K (16kx1) 150nS | 26-24116 | 1.59 |
| 2764 | 64K (8kx8) 450nS | 26-02764 | 9.50 |
| 2732 | 32K (4kx8) 450nS | 26-02732 | 5.70 |

Voltage Regulators

| | | | |
|------|-----------------|----------|------|
| 7805 | 5V 1A positive | 27-78052 | 0.40 |
| 7812 | 12V 1A positive | 27-78122 | 0.40 |
| 7815 | 15V 1A positive | 27-78152 | 0.40 |
| 7905 | 5V 1A negative | 27-79052 | 0.49 |
| 7912 | 12V 1A negative | 27-79122 | 0.49 |
| 7915 | 15V 1A negative | 27-79152 | 0.49 |

Transistors

| | | | |
|-------|---------------------|----------|------|
| BC182 | General purpose | 58-00182 | 0.10 |
| BC212 | General purpose | 58-00212 | 0.10 |
| BC237 | Plastic BC107 | 58-00237 | 0.08 |
| BC238 | Plastic BC108 | 58-00238 | 0.08 |
| BC239 | Plastic BC109 | 58-00239 | 0.08 |
| BC307 | Complement to BC237 | 58-00307 | 0.08 |
| BC308 | Complement to BC238 | 58-00308 | 0.08 |

| | | | |
|---------|---------------------------------|----------|------|
| BC309 | Complement to BC239 | 58-00309 | 0.08 |
| BC327 | Driver/power stage | 58-00327 | 0.13 |
| BC337 | Driver/power stage | 58-00337 | 0.13 |
| MPSA13 | NPN Darlington | 58-04013 | 0.30 |
| MPSA63 | PNP Complement to MPSA13 | 58-04063 | 0.30 |
| J310 | JFET for HF-VHF | 59-02310 | 0.69 |
| J176 | JFET analogue switch | 59-02176 | 0.65 |
| 3SK51 | Dual gate MOSFET-VHF amp | 60-04051 | 0.60 |
| 3SK88 | Dual gate MOSFET-Ultra to noise | 60-04088 | 0.99 |
| TIP31A | Output stage | 58-15031 | 0.35 |
| TIP32A | Complement to TIP31A | 58-15032 | 0.35 |
| VN66AF | V MOS Power FET | 60-02066 | 0.95 |
| ZTX3866 | E-line version 2N3866 | 58-03866 | 0.45 |
| 1N4001 | Rectifier diode | 12-40016 | 0.06 |
| 1N4002 | Rectifier diode | 12-40026 | 0.07 |
| 1N4148 | General purpose silicon | 12-41486 | 0.05 |

Silicon Controlled Rectifiers

| | | | |
|-----------|-----------|----------|------|
| BRY55-100 | 100V .8A | 52-55100 | 0.50 |
| C106DI | 400V 4.0A | 52-00106 | 0.70 |
| C122DI | 400V 8.0A | 52-00122 | 1.45 |

3mm Diameter LEDs

| | | | |
|-------|--------|----------|------|
| V178P | Red | 15-01780 | 0.15 |
| V179P | Green | 15-01790 | 0.16 |
| V180P | Yellow | 15-01800 | 0.18 |

5mm Diameter LEDs

| | | | |
|--------|--------|----------|------|
| CQY40L | Red | 15-10400 | 0.12 |
| CQY72L | Green | 15-10720 | 0.15 |
| CQY74L | Yellow | 15-10740 | 0.15 |

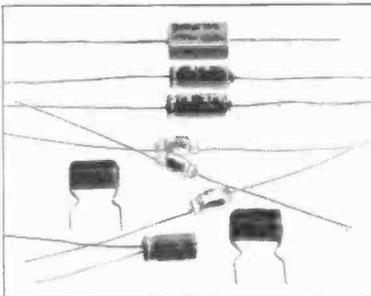
Infra-Red LEDs

| | | | |
|-------|----------|----------|------|
| CQY99 | Emitter | 15-10990 | 0.56 |
| BPW41 | Detector | 15-30410 | 1.51 |

Tri Colour LED

| | | | |
|------|---------------------|----------|------|
| V518 | Orange-Green-Yellow | 15-05180 | 0.60 |
|------|---------------------|----------|------|

Capacitors



Aluminium Electrolytics Radial PCB Mounting

| | | | | |
|------|------|----------|-----------|------|
| 10u | 16V | 05-10606 | Pack of 4 | 0.24 |
| 47u | 16V | 05-47606 | | 0.28 |
| 47u | 25V | 05-47607 | | 0.28 |
| 470u | 6.3V | 05-47705 | | 0.36 |
| 470u | 16V | 05-47706 | | 0.48 |

Tantalum Beads

| | | | | |
|------|------|----------|------|------|
| 1uF | 35V | 05-10501 | Each | 0.18 |
| 10uF | 16V | 05-10601 | | 0.28 |
| 47uF | 6.3V | 05-47601 | | 0.45 |
| 47uF | 16V | 05-47602 | | 0.92 |

Monolithic Capacitors

| | | | |
|------|----------|-----------|------|
| 1n | 04-10204 | Pack of 3 | 0.39 |
| 10n | 04-10304 | | 0.42 |
| 100n | 04-10404 | | 0.45 |

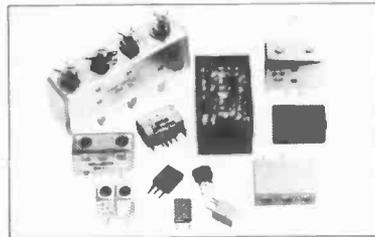
Low Voltage Disc Ceramic

| | | | |
|-----|----------|-----------|------|
| 1n | 04-10203 | Pack of 5 | 0.20 |
| 10n | 04-10303 | | 0.20 |

Polyester (C280)

| | | | |
|------|----------|-----------|------|
| 10n | 04-10305 | Pack of 3 | 0.18 |
| 47n | 04-47305 | | 0.24 |
| 100n | 04-10405 | | 0.24 |
| 470n | 04-47405 | | 0.51 |
| 1uF | 04-10505 | | 0.66 |

R F Components



Filters

CFU/LFB CFW/LFH SERIES

Miniature 455kHz filters. 1/P and O/P impedance 2K.

| | | | | | |
|-----------------|----------------------------------|-------|----------|------|--|
| | | -6dBW | -40dBW | | |
| LFB6/CFU455H | 6kHz | 18kHz | 16-45512 | 1.95 | |
| LFB12/CFU455F | 12kHz | 26kHz | 16-45515 | 1.95 | |
| LFH6S/CFW455HT | 6kHz | 14kHz | 16-45525 | 2.45 | |
| LFG12S/CFW455FT | 12kHz | 22kHz | 16-45528 | 2.45 | |
| CFM2455A | Mechanical IF Filters for 455kHz | | 19-45530 | 0.77 | |

Crystal Filters 2 Pole Types

| | | | |
|---------|---------------------|----------|------|
| 10M15A | 10.7 Centre Freq. | 20-10152 | 2.10 |
| 10M08AA | 10.695 Centre Freq. | 20-11152 | 3.49 |

Inductors

We offer the complete Toko range of fixed and variable inductors. Over 500 coils from audio to V.H.F. See catalogue for details.

Soldering Irons (Antex)

| | | | |
|-------|---|----------|------|
| CS240 | Iron 240VAC 17 Watts | 54-22300 | 5.20 |
| XS240 | Iron 25W 240V High heat capacity | 54-22500 | 5.40 |
| SK6 | Presentation pack of one XS-240 with ST4 stand | 54-22510 | 7.20 |
| MLXS | Handy 12V 15W soldering iron complete with crocodile clips and solder | 54-20004 | 5.60 |

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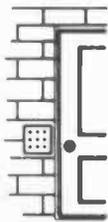
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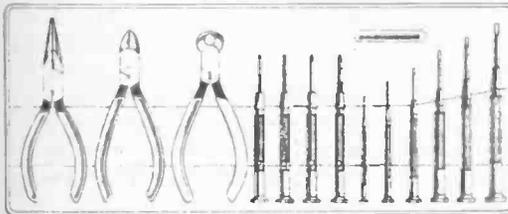
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COME ON SIR CLIVE

BACK in January, I attended the press launch of the new Sinclair QL. Remembering the problems with Spectrum and the long awaited microdrive, Sinclair was asked one or two questions on availability of the first units. The impression given was one of imminent production and no problems, we could place our order then and there for delivery within 28 days. At the time of writing it is nearly four months later and still no QL's have appeared.

PE was recently invited to send a representative to Cambridge and try out a QL for the day. The resultant report on this "one day wonder" is contained in this issue. The experiences of that day indicate that Sinclair still has some way to go before reliable, working QL's are available to the public.

Perhaps what worries me most about the whole affair is the "stringing along" that Sinclair have indulged in. I believe they have manufacturing problems with the QL microdrive, with pilot production resulting in a very small percentage of working units. I know that the operating system will not fit the memory space available. Sinclair have said they will sell early machines with a EPROM add-on and will later take back these machines to

be updated. I have also been told of a possible p.c.b. redesign, presumably to get extra ROM space, but questions on these matters have met with a "no comment" reply.

When our contributor Dr. Tony Berk visited Sinclair he was told that QL's would go out to customers the following week, yet the machine provided for him would not work properly, and had to be replaced. I was informed that the test machines were pre-production prototypes, so presumably no pilot production models were available only a week before the claimed sale date to the public! The state of affairs was similar with the manual which was in draft form and said to be substantially the same as the finished manual. At the same time I was told that finished manuals were expected from the printer "next week." Why then were the journalists not shown a final version? I cannot believe that the fully sorted version of the QL will be available for some time and I expect the add-on memory pack to take about a year to arrive (Sinclair will not quote a date)—this is a limitation as you will see from Dr. Berk's article.

The QL is aimed at the business man, will he continue to wait for delivery, will the machine prove to be reliable enough for business use and

how long will it take to get repaired when it does fail?

What does seem to be a great pity in all this is that a great British company is tarnishing its image — remember the Black Watch? Also the Psion software which seems to be so good, may never have the business use it appears to deserve.

It is easy to say after the event, but would it not have been better for Sinclair to advise customers of a problem and state that delivery of the new machine would not commence for six months. They could then finish prototyping the unit, sort out the production problems, test some working production models and have product ready for customers—most of which should have been done before the launch in the first place.

It is very worrying to receive a "no comment" reply on questions concerning major problems, so come on Sir Clive, tell your faithful public what is going on and when they can expect to buy a reliable QL off the shelf of their local retailer. I wonder if it will be before Christmas?



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Items mentioned are available through normal retail outlets, unless otherwise specified. Prices correct at time of going to press.

AMSTRAD'S GAMBIT

Amstrad, who will be best known to most readers for their range of hi-fi and television equipment, have now entered the personal computer market with a system which they claim will bring home computing within reach of almost every family in the country. The reason for this claim is that the CPC 464, as it is known, comes complete with its own monitor, a built-in cassette recorder, 64K of RAM and is priced at £229.00 including VAT.

The system is available in four basic options: A 64K unit with cassette and a green monitor (£229.00), a 64K unit with cassette and a colour monitor (£329.00), a 64K unit with a disc drive and a green

defined keys with up to 32 character strings; three screen modes, 40 columns by 25 lines, 320 x 200 pixels (normal mode), 20 columns by 25 lines, 160 x 200 pixels (multi-colour mode) and 80 columns by 25 lines, 640 x 200 pixels (high resolution mode); polyphonic sound using the GI AY8910 family of chips, three channels, 7 octaves are available each of which can be independently set for tone and amplitude with white noise being added as required for each explosion; a Centronics compatible parallel printer port; a joystick port to support two joysticks and an expansion bus connector for ROMs, modems, disc drives etc. All ROMs occupy the top 16K of memory and there are facilities in the firmware to call up to 240 additional 16K add-on ROMs.

A separate division of Amstrad called Amsoft has been formed to develop software specifically for the CPC 464 and already a range is available.

All models of the CPC 464 will be available from Amstrad's traditional stockists like Rumbelows, Dixons, Comet and Boots.

monitor (£429.00) and a 64K unit with disc drive and a colour monitor (£529.00).

The CPC 464 follows Amstrad's design philosophy as applied to their hi-fi tower systems in that they believe the consumer prefers a complete package with the absolute minimum of plugs and inter-connecting leads. This philosophy has resulted in the cassette recorder being built-in to the computer console and the monitors being fitted with power supplies instead of the computer so the one mains lead powers the computer, the cassette and the monitor.

If the CPC 464 is to be used with a television then an optional p.s.u. (MP 1) and modulator is required, although it should be noted that Amstrad will not be supplying the CPC 464 without either a green or colour monitor.

The major features of the system are: A Z80A microprocessor which has formed the basis of many home computer systems; 64K of RAM of which 42K is available to the user; a fast versatile Basic with extensions for graphics and sound; up to 32 user

BRITISH INGENUITY?

A study by the Director General of NEDC (National Economic Development Council), Mr. John Cassels, has identified serious weaknesses in the UK's engineering sector. United Kingdom R & D spending is markedly lower than that of its competitors, and more alarmingly, its R & D efficiency in terms of 'patents per pound' is worse than Japan and Germany, being only marginally higher than France's.

Also, long term growth is threatened by a skilled manpower shortage, particularly in the high technology sector—findings endorsed by Norman Tebbit and Sir Keith Joseph, the Education Secretary.

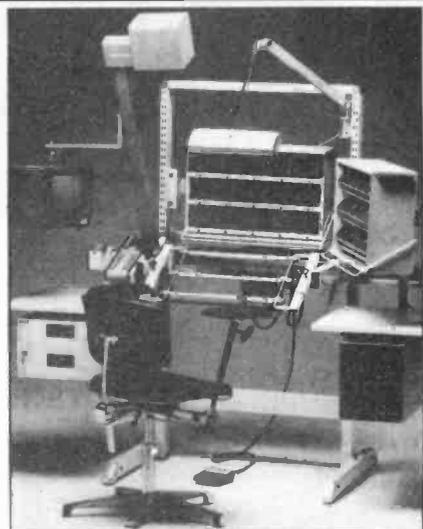
According to Engineering Industry Training Board research, the supply of newly trained engineers will have fallen to only half its 1979 level by 1986-87. Apprenticeship levels have subsided to all-time lows, and skilled personnel shortages are envisaged as the single most limiting factor in Britain's recovery in the technology revolution.

Electronics engineers have until more recently had to tolerate meagre pay in relation to their capabilities. So it's not surprising that many of today's graduates and school leavers, who were making their educational decisions at a time when the engineer's pay and prestige was at its nadir, chose to study other subjects. There is, perhaps, a hint of nemesis.

In the chair

At first glance this may look like the dentist's chair; it is in fact a constructor's dream (or is that nightmare).

System GWS is the product of a UK/Finland partnership, the modular design enables the assembly of workstations with the exact requirements of the operator. Most of the hardware is presently produced in Finland by GWS Metals. Martela, the UK half of the duo, hope to produce up to 40 per cent of the equipment when their new Milton Keynes factory opens later this year. A purpose built jig is the central feature of the system with 360 degrees of rotation available, it can be either manually or motor driven. Pools winners and other interested parties should contact Martela Contract Interiors Ltd, 210 High Holborn, London WC1V 7BP. (01-831 8771).



MARKET PLACE

SHRINKING WORLD

A digital video conferencing service between London and New York will start shortly. The new service will be set up jointly by British Telecom International (BTI) and AT&T Communications. Initially, it will operate between British Telecom's studios in London and other cities in Britain, and AT&T's studios in New York and 13 other American cities.

The decision to go ahead with the service was announced at the recent *International Teleconference Symposium*, held simultaneously in London, Tokyo, Sydney, Toronto and Philadelphia. It follows a decision giving the go-ahead announced by the US Federal Communications Commission.

More than 2,000 delegates worldwide attended the event, which was the first of its kind. Highlight of the week was a world session with



a live link-up between all five centres. Participants in this international forum on teleconferencing were able to see, hear and speak to their partners across the world by means of colour tv.

Five major areas of interest were studied: teleconferencing service objectives; potential demand; hardware and network developments; economics; and user impact.

The service will use a high-speed digital link between international exchanges in London and New York, providing full motion video and audio communications.

A British Telecom-developed coder/decoder (CODEC) codes and compresses the signals that make up the television picture, transmitting only the changes in picture content from one frame to the next. This technique reduces the bandwidth required to 2Mbits per second or less.

British Telecom is planning to provide terminals and CODECS for private use on purchase or rental terms through its VideoStream domestic videoconferencing service. These video terminals will incorporate television cameras, monitors, microphones and loudspeakers, enabling users to set up conferences from rooms in their own premises.

Bite-size batteries

Matsushita Electric Industrial Company Limited of Osaka, Japan, parent company of Panasonic U.K. Limited, have announced the introduction of the world's smallest pin-type lithium battery.

The 3 volt battery manufactured at Matsushita Battery Industrial Company Limited measures merely 2.2mm in diameter and 11mm in length and initially will be marketed for use in ultra-small fishing floats with l.e.d.s for night time fishing. The battery is expected to be widely adapted for use in many small electronic products.

Due to the rapid gains in i.c., LSI and VLSI technology the trend has been towards further miniaturisation in electronic equipment, therefore small high performance batteries have been in strong demand.

The new battery has been developed through use of Matsushita's ac-



cumulated technological expertise in the field of poly-carbon monofluoride lithium batteries.

To achieve mass production of the 2.2mm battery, the dimension tolerance had to be decreased to one-tenth of previous models, in the drawing process of the aluminium case and in the areas of plastic moulding technology, seal packing and assembling technology of the battery.

LOW COST ERASER

A low cost EPROM eraser is being marketed by Essex based Ground Control. The 'Uvipac' can erase up to three EPROMs or one CPU with on-board EPROM in 15 to 20 minutes. In order to achieve the small size of this unit, a low-profile p.c.b. mounting mains transformer was used along with a special type of discharge tube with reflector. The 'Uvipac'



measures 90mm x 80mm x 40mm. A fibre optic indicator is used to show that the unit is in operation. EPROMs are simply loaded onto the conductive foam supplied and inserted into the unit. The 'Uvipac' costs £21.45 as a standard unit or £24.95 with a built-in (15 min) timer. From Ground Control, Alfreda Avenue, Hullbridge, Essex SS5 6LT (0702 230324).

VIDEO PROMO

Pioneer (GB) Limited has introduced a major marketing drive to promote their LaserDisc video system, and will be opening 20 "LaserDisc Centres" in the UK. This follows RCA's decision to abandon their ill-fated Capacitive Electronic Disc (CED) format VideoDisc in the USA, which is sold in the UK by Hitachi.

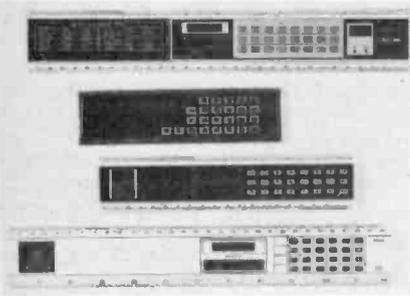
The LaserDisc format is, and will probably remain, the dominant system in video discs for some time. It is the only format which can actually give better picture and sound quality than both VCR and broadcast TV.

Over the last few years there has been a lot of confusion surrounding VCR, where there are still three competing formats. Video disc manufacturers are hoping to avoid this by setting a standard and presenting the video disc as a natural extension to the high quality audio discs already available.

Pioneer's "LaserDisc Centres" will be 'high visibility outlets' for the public to experience LaserDisc for themselves. This line of promotion has been taken as it is difficult to demonstrate the quality of LaserDisc, even on TV commercials. Although audio and video discs offer many advantages over cassettes and VCR, it will be some time before they become leaders in the audio-visual field. Disc prices for one thing must be reduced to attract buyers.

DUAL-RULES

It's now more than a year since Systema first introduced their 8 inch (200mm) Ruler-Calculator, and soon four additional models will be available. The designs are specially practical for moving down a column of figures during addition etc. The keyboards are well laid out and the displays conveniently positioned in the centre. They also prevent 'desk clutter' by serving as a measuring device and straight edge.



The first of the new members is the all metal RL-511 6 inch (150mm) model. Finished in black and gold the RL-511 has a full memory, per cent and square root keys. Fitted with long life batteries and supplied with a slip-in case it will retail for around £9.95.

Also introduced is the 12C. This 12 inch (300mm) Ruler-Calculator includes a time and date clock. Finished in white it features a large area for overprinting an advertising message. Supplied complete with batteries the Ruler 12C will sell for about £3 more than the RL-511.

The other two new models both have solar powered calculators and a battery operated built in clock. Finished in black and silver the R8C-Solar has an 8 inch (200mm) ruler and will retail for about £12.95. At the top of the range is the R12CT-Solar with a 12 inch (300mm) ruler incorporating a digital thermometer as well as a clock and solar calculator for around £15.50.

According to Systema all the above models will be available in many High Street shops this summer.

Robot Drive

Mitsubishi Electric Corporation has developed a direct-drive manipulator for next-generation industrial robots. The manipulator, combining a robot arm and an a.c. servomotor in a single unit, features an arm capable of moving over 6 metres per second, more than three times as fast as conventional manipulators. Movement of the arm is controlled by simply varying the electric current to the servomotor, in which powerful samarium cobalt magnets are used. The new manipulator with its improved precision will speed up complex assembly work and facilitate the use of (CAD/CAM) systems.

TI ADDS UP

The TI-66 programmable calculator from Texas Instruments comes in a horizontal computer-like case and provides the college student, engineer and science professionals with more than 170 scientific functions, large memory area and user-friendly programming features.

This calculator has arithmetic, logarithmic, trigonometric, statistical, polar to rectangular conversion features. It can have a maximum of 512 program steps or 64 data memories with each memory convertible to 8 program steps, with 9 levels of parenthesis and 6 levels of subroutines. TI say it can handle almost any problem.

When entering or reviewing a program the TI-66 displays readable alphanumeric abbreviations of the instructions and uses the same set of instructions as the TI-



58C/59 family of calculators. The constant memory feature retains data and program information even when the calculator is turned off.

The unit connects to TI's PC-200 thermal printer, giving it printing and listing capabilities. Additionally, programs written for the TI-58C can be used on this model—a bonus for 58C owners who are seeking to update their calculating equipment. High street availability is assured by TI at the competitive price of £44.99.

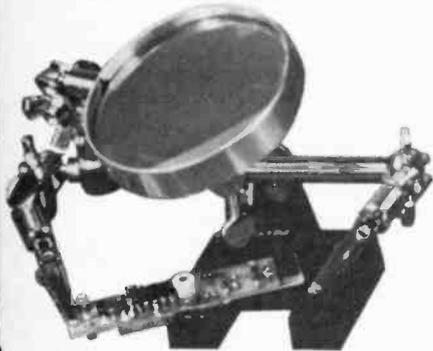
Helping Hand

For those who often find themselves short-handed (and long-sighted) in the workshop, Litesold have developed this helpful little magnifying device.

Supported on a solid, cast base, the 'Helping Hands' consists of a 115mm long support bar, fitted with two crocodile clips and a 5 diopetre glass lens. The support bar, clips and lens are all mounted on adjustable ball-joints, and can be set to any required position to hold parts and assemblies for cleaning, adjusting, soldering and many other jobs, whilst giving a clear, magnified view.

The Helping Hands is available at a special price of £7.45 which is inclusive of postage and VAT.

From Light Soldering Developments Ltd., Spencer Place, 97/99 Gloucester Road, Croydon, CR0 2DN, Surrey (01-689 0574).



LIGHT LOGIC

For some time now scientists and engineers have been investigating and developing optical systems such as lasers and fibre optics. Plans are now under way to build the world's first optical computer at Heriot-Watt University in Edinburgh. The project will be funded by the European Commission, with eight European universities making design contributions.

Optical computers use laser beams instead of electric currents to transmit and manipulate information, giving greater speed and versatility. Whereas modern electronic computers are based on digital logic using binary arithmetic, optical systems have no such limitations. Logic gates constructed using transistors can have only one of two stable states; however, its optical counterpart, the Transphasor, can operate on several different levels and thus give rise to a new breed of "computer logic".

Transphasors offer many advantages over the transistor such as speed (several hundred times faster), which is the ultimate limiting factor of a computer's power. They can also carry out different operations on several light beams simultaneously which is impossible using transistors. A conventional logic gate is made up from several devices but a single transphasor-like device will do the same job, which should eventually mean smaller packages.

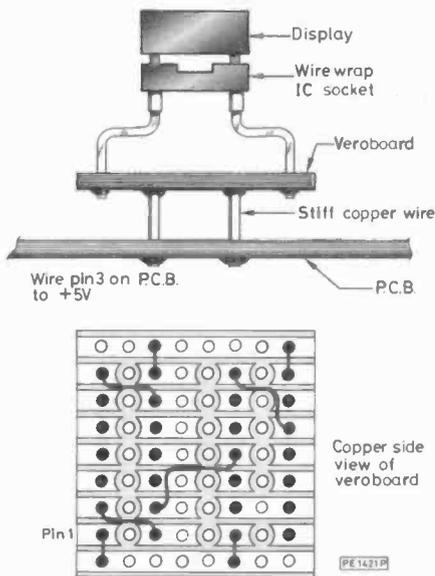
It will be a long time before any commercially viable optical computers become a reality, but the seeds have been sown.

MARKET PLACE

POINTS ARISING...

MICROSTEPPER April 1984

The predicted chip famine has struck! Suppliers of the Fairchild 9368PC display driver (IC3-8) have dried up, leaving a 45 week lead time. Still worse, there appears to be no pin compatible substitute available, so we have had to resort to a fix which allows the use of the 9370PC, the



not so hard hit complement designed for use with *common anode* displays.

If the 9370PC is used, each display (now common anode type) will require the illustrated adaptor socket. The pad for pin 3 of each display on the Microstepper board will need to be wired to +5V, or the adaptors could be incorporated on one continuous strip of Veroboard with its own +5V rail. Either way, pin 3 was not used in the original arrangement and so the modification to the p.c.b. at pin 3 can be ignored on reversion to 9368 operation. Wire-wrap type i.c. sockets will provide sufficient lead length for bending.

A supplier of the 9370PC is **Macro Marketing**, Slough, Bucks. (06286 4422).

Briefly...

According to the Japanese Ministry for Trade and Industry, semiconductor manufacturers in Japan are spending £4m a day on new plant and equipment. This compares with £2.7bn invested by the entire world in 1983, according to Bill McClean of Integrated Circuit Engineering. This probably explains why Europe is so far behind in the semiconductor field.

With each new generation of chip technology, new and more expensive production equipment is required. Unless present trends change, the Japanese will produce five times more leading edge products each year than Europe.

According to *Electronics Weekly* the UK business software market could be worth £900m by 1987. Significantly W. H. Smith the booksellers are turning their attention to this side of the market, in partnership with the US giants Softeam they hope to capture 25 per cent of the market.

A company called *Programmed Logic Services* has introduced a customising service covering all programmable devices around today. Not only can your PROM be fitted with your own program using the approved professional equipment and techniques, but *Programmed Logic Services* can also provide a development service.

Piece-part programming charges start from 5 pence, whilst development fees, including the cost of a prototype, may be under £100 for logic circuit implementation. Turnaround for programming and marking is about 72 hours, with an express service also available. *Programmed Logic Services*, Victoria House, London Rd., Cheam, Surrey SM3 8HY. (01-644 8095).

'Trips through space' courtesy of Rediffusion Simulation will be available in the CN Tower in Toronto this autumn. A 40 seat space capsule with hydraulic motion induction will take passengers on a 'Tour of the Universe' for C\$5 a head. The outside view will be generated by a computer and will be based on effects used in Hollywood.

Countdown ...

Please check dates before setting out, as we cannot *guarantee* the accuracy of the information presented below. Note: some exhibitions may be trade only. If you are organising any electrical/electronics, radio or scientific event, big or small, we shall be glad to include it here. Address details to Mike Abbott.

Welsh Amateur Radio Rally June 3. Barry Leisure Centre. C
 Software June 5-7. Earls Court, London. S1
 Scotex June 5-7. Royal Highland Exhibition Halls, Ingliston, Edinburgh. O5
 IBM Computer User Show June 12-14. Wembley Conf. Cntr., London. O
 Computer Fair June 14-17. Earls Court. K2
 Qualex June 19-21. Corn Exchange, Brighton. D4
 Mach (Machine Tool) June 19-29. NEC. Y5
 Compec North June 19-21. Belle Vue, Manchester. K2
 Promcon C & I (Control & Inst.) June 19-22. Earls Court. F4
 TMS 3617 Workshop (meeting) June 23. Electronic Organ Constructors Society, London. Y4
 Surface Treatment & Finishing Show June 25-29. NEC. M
 Office Automation Show June. Barbican, London. T1
 Leeds Electronics July 3-5. University. E
 PC User Show July 3-5. Cunard Int. Hotel, London. Q2
 Networks July 3-5. Wembley Conf. Cntr., London. O
 Cable July 10-12. Wembley Conf. Cntr., London. O

Education, Training & Development July 10-12. NEC. B2
 IBM System User Show Sept. 3-5. Olympia 2. Q2
 Laboratory Sept. 4-6. Barbican, London. E
 Amplifiers & Speakers (meeting) Sept. 8. Electronic Organ Constructors Society. Y4
 Testmex Sept. 11-13. Grosvenor Ho., Pk. Lane, London. E
 Personal Computer World Show Sept. 19-23. Olympia 2, London. M
 Building & Home Improvement Sept. 25-30. Earls Court, London. M
 Computer Graphics Oct. 9-11. Wembley Conf. Cntr., London. O
 Software Expo Oct. 16-18. Wembley Conf. Cntr., London. O
 Drives, Motors & Controls Oct. 24-26. Harrogate Exhibition Cntr. E
 P.c.b. Manufacture & UV Box Construction (meeting) Nov. 17. Electronic Organ Constructors Society. Y4
 Computers In The City Nov. 20-22. Barbican, London. O
 Data Security Nov. 20-22. Barbican, London. O
 B2 Brintex ☎ 01-637 2400
 C Barry College ☎ 0222 565656
 D4 Network ☎ 0280 815226
 E Evan Steadman ☎ 0799 26699
 F4 Morgan Grampian ☎ 01-855 7777
 K2 Reed Exhibitions, Sutton, Surrey
 M Montbuild ☎ 01-486 1951
 O Online ☎ 01-868 4466
 O5 Institute of Electronics ☎ 0706 43661
 Q2 EMAP ☎ 01-837 3699
 S1 National Computing Centre ☎ 061-228 6333
 T1 Cahners ☎ 0483 38085
 Y4 Percy Vickery ☎ 0202 423863
 Y5 Mach. Tool Trades Assn. ☎ 01-402 6671

Simple Logic Analyser

CHRIS ATKINS

PART ONE

THE circuit was designed and built for the extraction of data from microprocessors and computer circuits. It works very much in the same way as an expensive logic analyser, such as the Hewlett Packard or Tektronic analyser. It is very basic compared, but is very much cheaper to build. It differs most in the display format, in that logic analysers tend to use a c.r.t. or an external scope. This circuit displays a keyboard address and the data in that memory location. The word need not be a memory address, it could be any 16 bit word or less, which you would like to be compared. This would then strobe the display or provide a positive or negative trigger pulse for an oscilloscope.

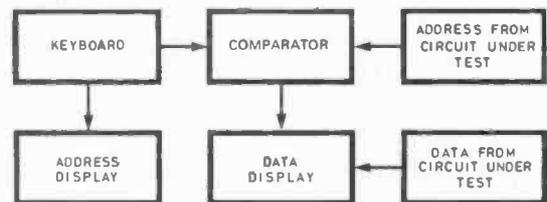
CIRCUIT DESCRIPTION

The word is generated by a keyboard which is fed into a 74C922 keyboard decoder (see Fig. 1.2). The four bit output is then connected to the input of a 74179 shift register – another three shift registers are then cascaded so a 16 bit word may be generated. The 74179 shift registers are clocked along by the data available pulse which is also derived from the 74C922 keyboard decoder. This pulse is inverted through a 7400 NAND gate and then fed into a serial shift register (7491) which when clocked serves as a delay dependent on the clock frequency. The clock is a 555 timer connected in the astable mode. This delay is needed so that the data is latched to the 74179 shift registers before being shifted on.

A reset switch has also been added so that all the shift registers may be cleared to zero. Displays are also connected to the outputs of the shift registers, these being TIL 311, which are hexadecimal displays with logic. The logic consists of a four bit latch which has a latch strobe input, a decoder and constant current drivers which also have a blanking input. These chips, although expensive, do away with a lot more logic. Full use of the latch strobe and blanking inputs is described later. The TIL 311s latch, decode and display the 16 bit word or address which is generated on the keyboard circuit.

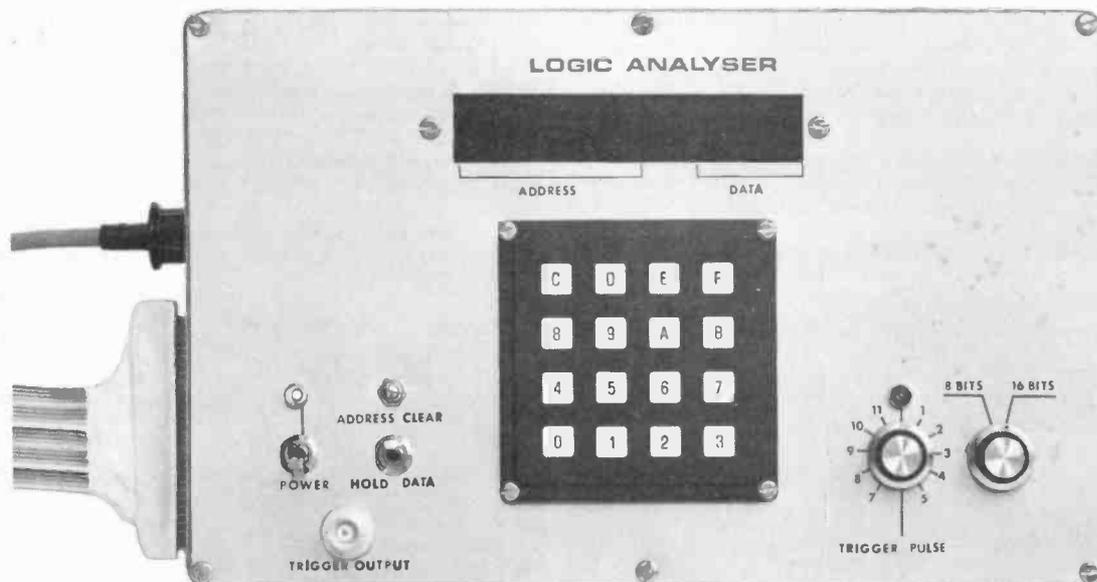
COMPARATOR

The comparator consists of four, four bit magnitude comparators (IC10–13). Sixteen lines from the shift registers are fed into one set of inputs to the comparators, and the sixteen bit address or word from the circuit under test is connected to the other set of



PE1537G

Fig. 1.1. Block diagram



TEST GEAR PROJECT

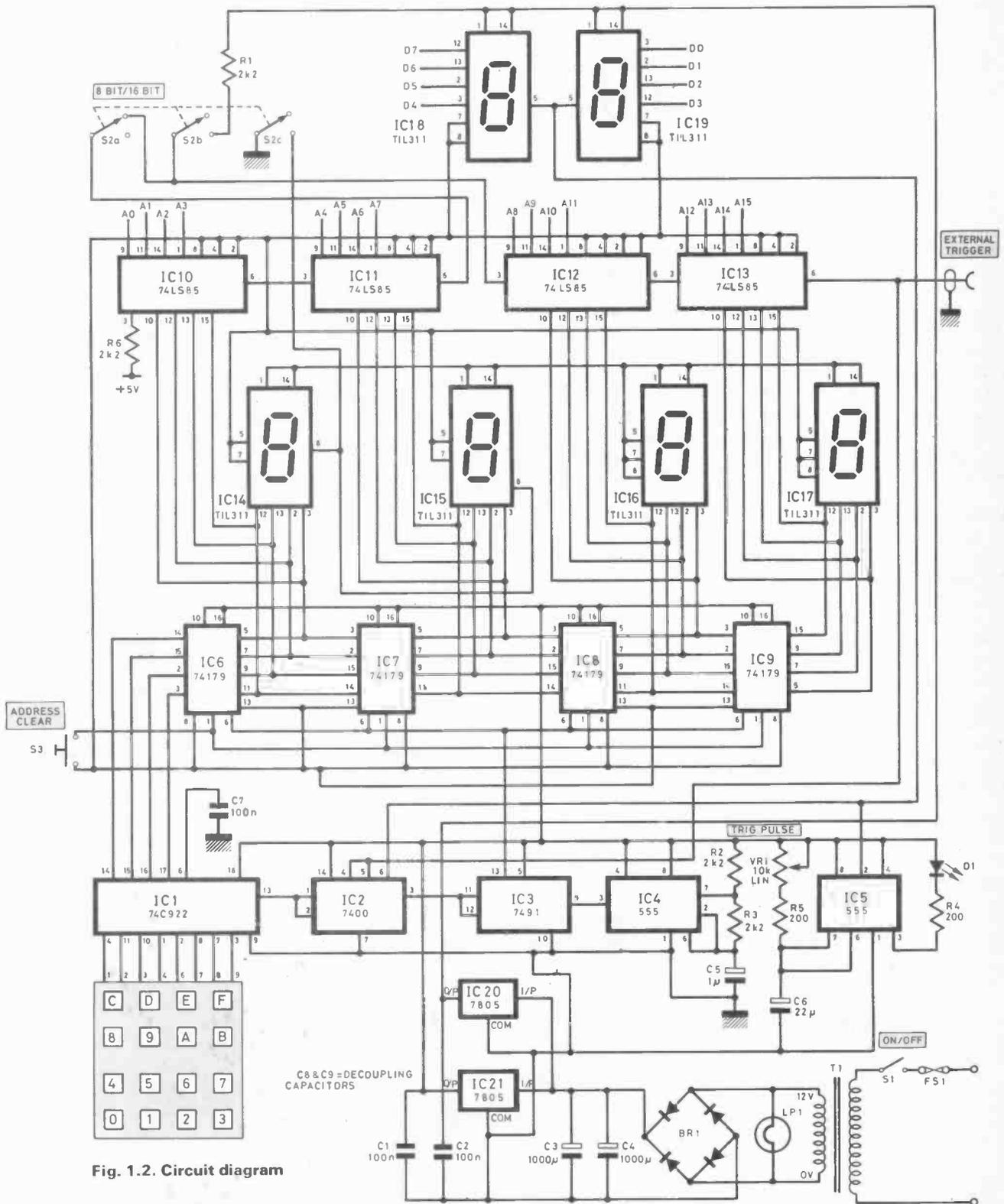
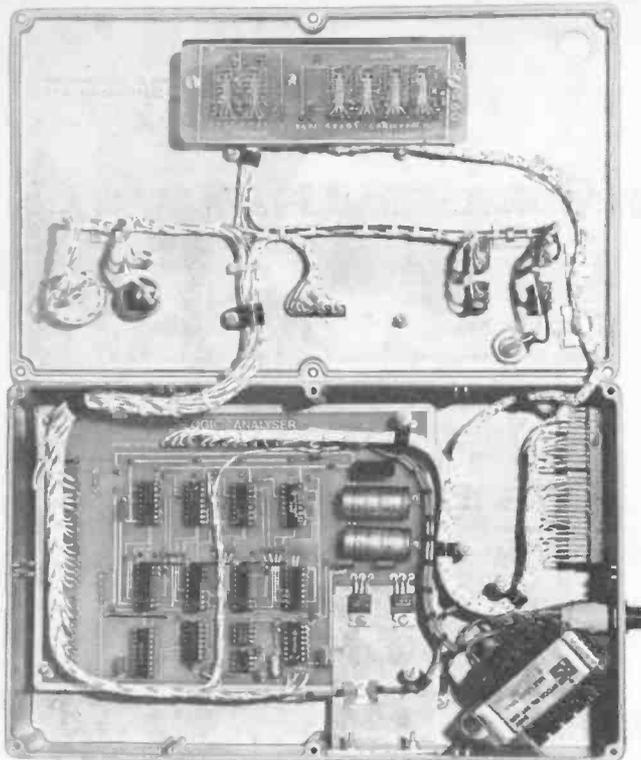


Fig. 1.2. Circuit diagram



Internal view of the analyser

inputs. When these two words are the same a positive pulse is produced. This is then inverted through a 7400 two input NAND gate. Outputs are taken here for positive external trigger pulses, so an oscilloscope may be externally triggered. The output from the 7400 is connected to the strobe input of the data displays. The data or eight bit word from the circuit under test is fed into the TIL 311 data display inputs. Also connected to the negative strobe line is a 555 timer connected up as a monostable; this has been done because of the high frequencies involved in a microprocessor or computer circuit when compared to the strobe pulse which is very small, so the operator is unable to tell if the reading he has is valid. By adjusting a potentiometer the pulse may be stretched so it can be seen. If the l.e.d. illuminates the operator knows his word is valid.

A switch has also been inserted that causes 8 bits or less to be compared instead of 16 bits. This is done by making pin 3 of IC12 high. The switch at the same instant disconnects the output of IC11 (pin 6) to IC12 and places a high on the blanking pins of the two most significant address displays, so the four address displays are reduced to two. This will be used for zero page of memory, and also for comparing smaller words. This has been done to save the operator's time when keying in numbers.

The external leads which are connected to the circuit under test may be fitted with probes but it was found to be easier to solder the connections to an i.c. holder and plug that into the existing i.c. holder and plug the micro in on top of that. All the design and development work was carried out on a 6802 and 6809 microprocessor at a clock rate of 1MHz.

PSU

The power supply uses a transformer which transforms 240 volts to 6 volts. This is then rectified and smoothed, and fed into two 7805 five volt regulators, one regulator for the displays and the other for the circuit power.

NEXT MONTH: Construction, including the display board.

COMPONENTS . . .

Resistors

| | |
|--------------------------|-------------|
| R1-3,R6 | 2k2 (4 off) |
| R4,R5 | 200 (2 off) |
| All resistors \pm W 5% | |

Potentiometers

| | |
|-----|----------|
| VR1 | 10k lin. |
|-----|----------|

Capacitors

| | |
|-------|--------------------------------|
| C1,C2 | 100n (104K) (2 off) |
| C3,C4 | 1000 μ /25V elect. (2 off) |
| C5 | 1 μ elect. |
| C6 | 22 μ /16V tant. |
| C7-9 | 100n ceramic (3 off) |
| C10 | 1n (102K) |

Semiconductors

| | |
|---------|---------------------------------|
| D1 | 0-1in. l.e.d. (yellow) |
| REC1 | In-line 4A/50V bridge rectifier |
| IC1 | 74C922 |
| IC2 | 7400 |
| IC3 | 7491 |
| IC4,IC5 | 555 (CMOS or bipolar) (2 off) |
| IC6-9 | 74179 (4 off) |
| IC10-13 | 74LS85 (4 off) |
| IC14-19 | TIL311 7-seg disp. (6 off) |

Miscellaneous

- Chassis plug (3-pin mains)
- Chassis mounting fuse holder & 2A fuse (FS1)
- 28+28 pin chassis socket (for Address & Data I/P etc.) plus polariser insert
- BNC chassis socket for TRIG O/P
- Min. toggle switch 1P2W (2 off) for POWER & HOLD DATA
- Min. push-to-c/o for ADDRESS CLEAR
- 12V lamp (mains pilot) + holder
- 20VA mains transformer with 0-12V sec.
- Main p.c.b. and Display p.c.b.
- Red filter for display window
- Diecast alloy case 274 x 170 x 55mm
- Alloy heatsink bracket to thermally couple IC20 & IC21 to case
- 3P2W rotary switch for 8/16 BIT
- Two knobs (for above and VR1)
- Nuts, bolts, wire, i.c. holders etc.
- Keypad: RS type 337-100 (or similar)

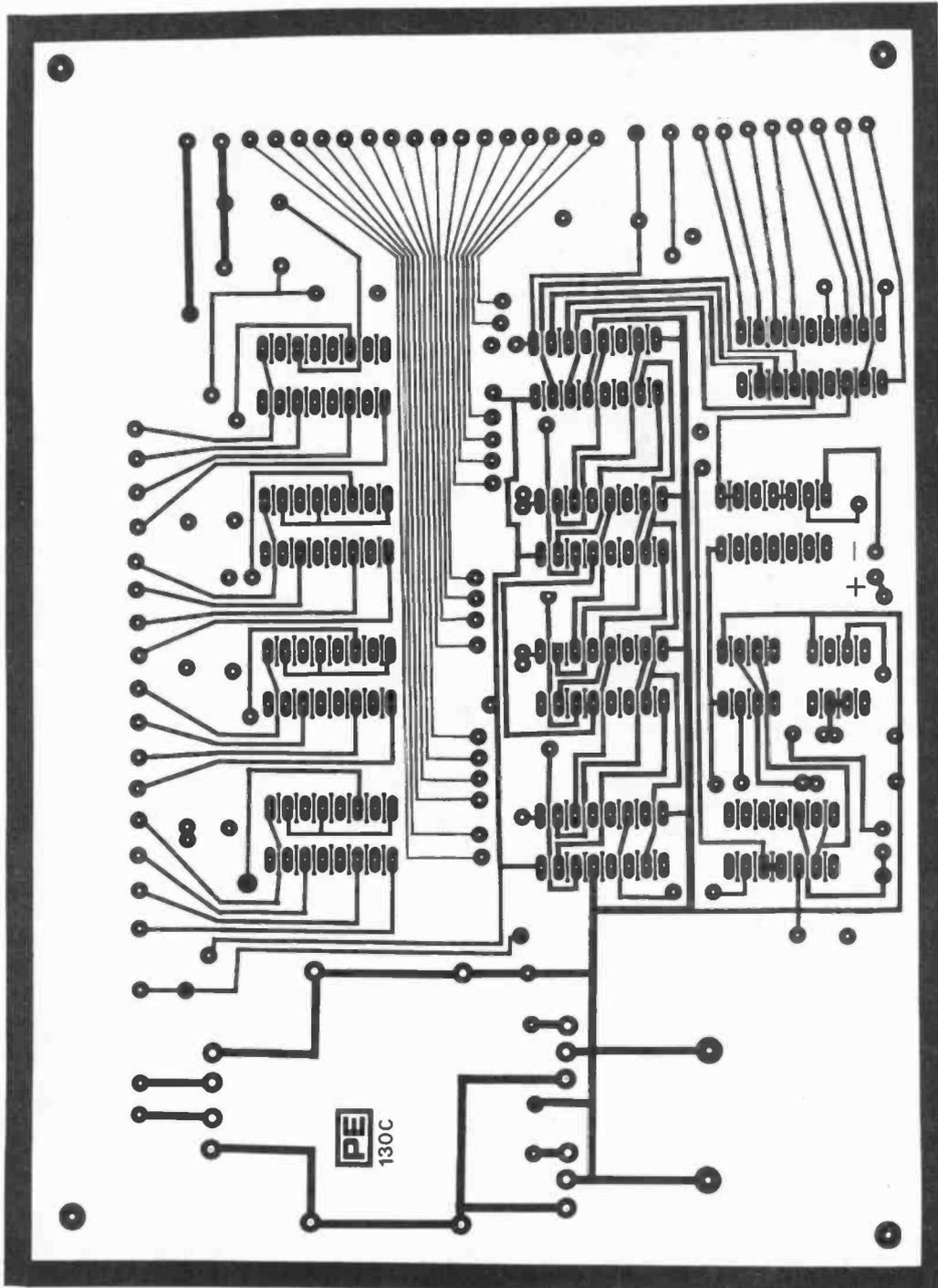


Fig. 1.3. P.c.b. layout (track-side)

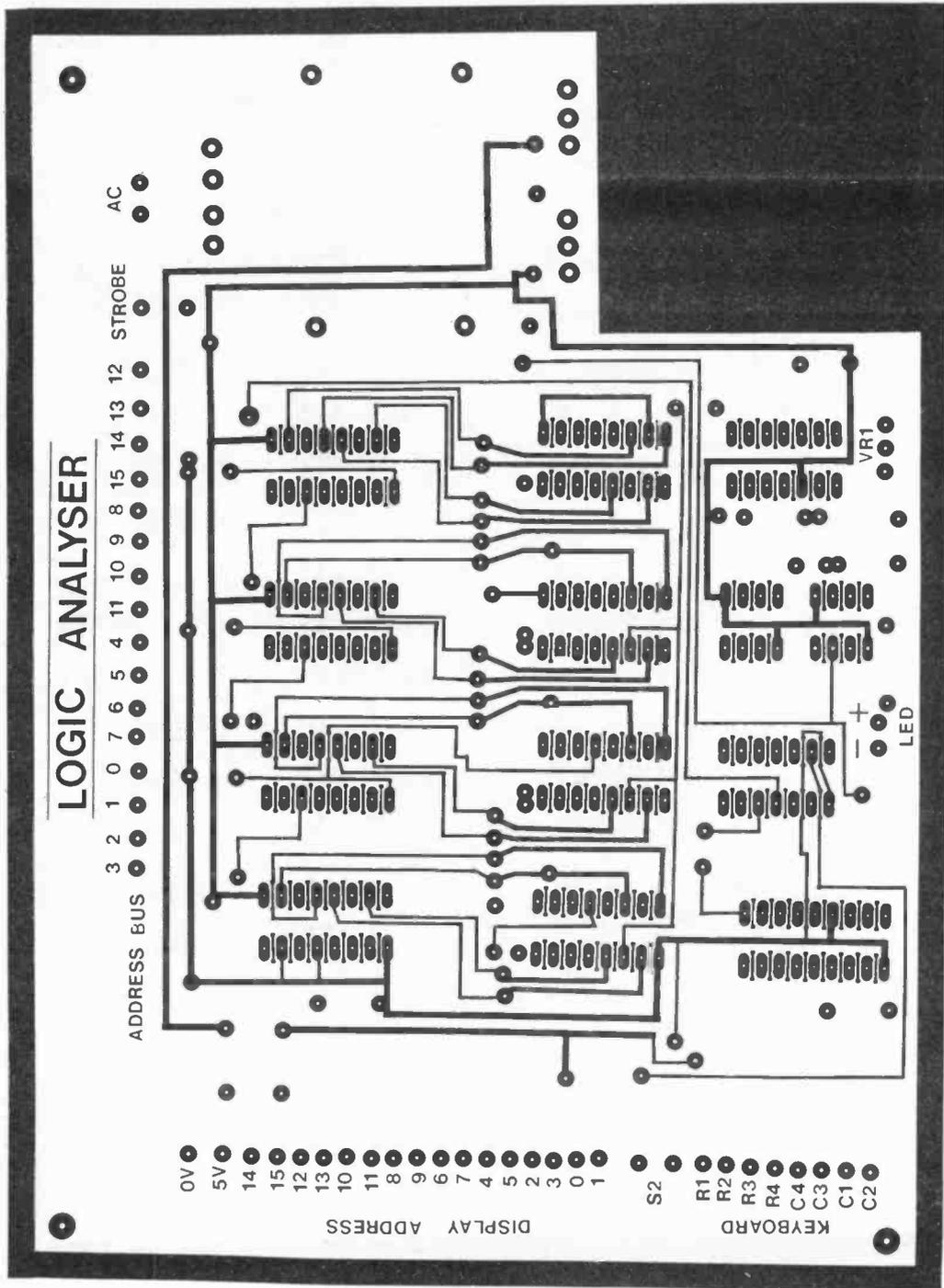


Fig. 1.4. P.c.b. layout (component-side)

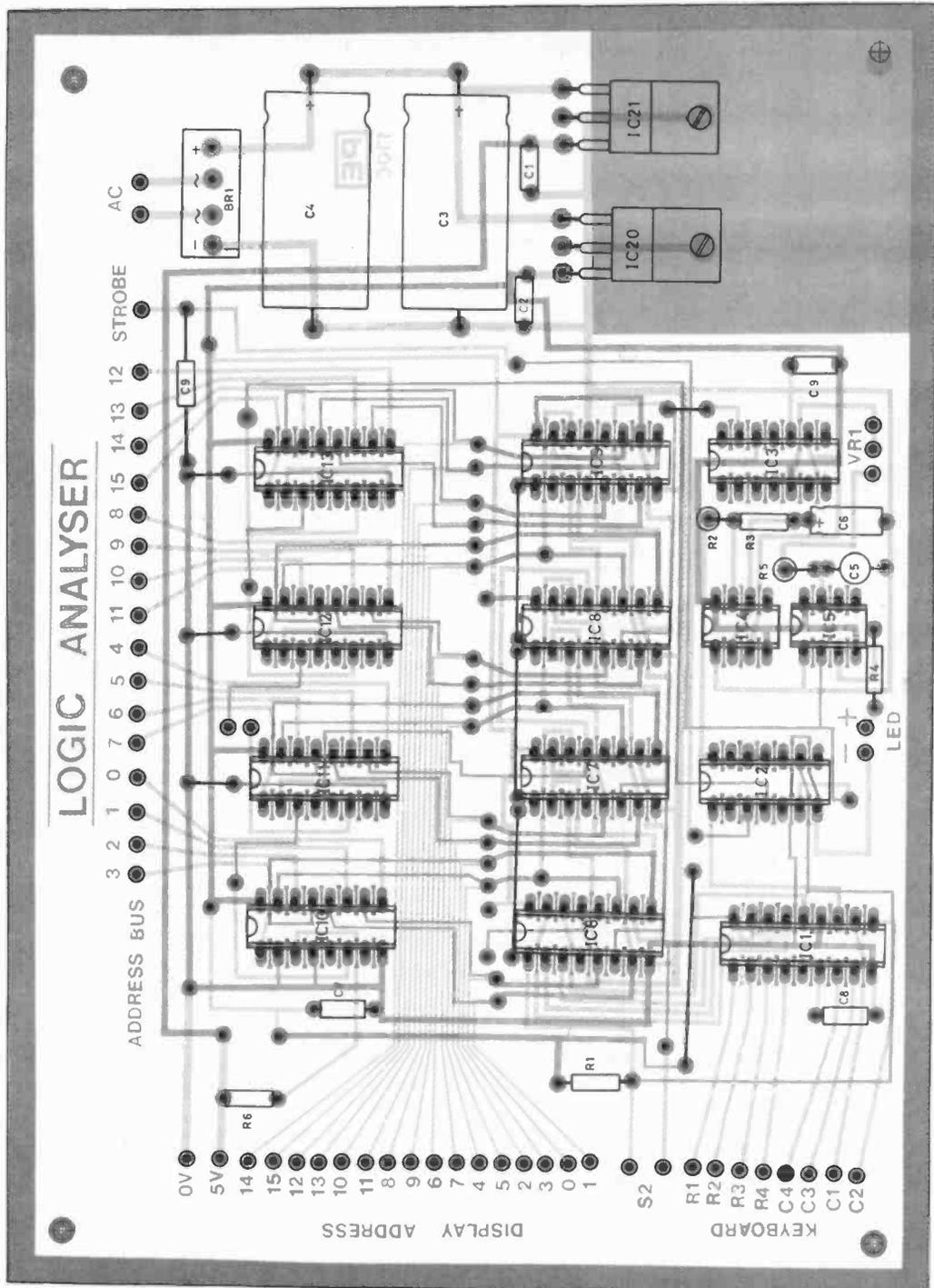


Fig. 1.5. Component layout (actual size)

EPROM DUPLICATOR

Prof. K. PADMANABHAN Ph.D MIEE & **S. ANANTHI**

NOW that the 2716 (2K x 8) and 2732 (4K x 8) EPROMs are available economically, it is advisable to replace the 2708s in older systems with one of these new EPROMs, to simplify power supplies and enhance the Read-only-memory capacity.

Professionally made equipment for EPROM duplicating is expensive and there is every reason for a simple instrument like the one described to find its place among micro-processors and home computers.

THE 2708/2716/2732 EPROM FAMILY

The 2708 EPROM is actually a second generation erasable read-only memory chip and is much superior to its predecessor, the 1702. The 1702 is a mere 256 byte type and it has rather difficult requirements for programming, such as Address complementing, a 45V program pulse etc. The 2708 fares better, because it is a 1K byte capacity and further, it requires no Address complementing and only a 27V pulse. It is also much faster than the 1702 for its memory access. However, the 2708 still needs three power supplies of +12, +5 and -5 volts, even for its normal reading mode. Most of the microprocessor based equipment built during the period prior to 1979 employed the 2708 EPROM only. Many readers may still be using them.

The 2716 EPROM which came after 1978 is much superior because it has a 2K byte capacity and works on a single +5V power supply. The TMS 2516 from TI is also an equivalent to the Intel 2716. For programming these chips, one needs a +25 volt supply, but it is just a steady 25V, unlike the pulse voltages needed for the 2708. For programming, a TTL level 5V pulse of 50ms has to be applied to the Programming pin 18. Further, it has the facility that one can program even a single byte at a time by one such pulse. The 2708 requires a series of pulses and one should apply them in sequence in order to program all the locations little by little. One pass through all address locations is defined as a Program loop. About 200 loops each with a 0.5ms pulse is needed to completely program all of its 1K locations. Individual locations also have to be programmed only by passing through so many loops.

Further, the 2708, because of its three power supplies, is prone to early failure due to power supply transients. In fact it requires that the -5V supply should be on first and switched off last in comparison with its other two +12 and +5 volt supplies.

The 2716 became available in 1979 and its price fell progressively, down to £3 or less. Since 1982, another chip, the 2732, of 4K byte capacity, has been available at or around £4. Now that the price has come down, these devices should soon replace the older 2708s.

For all these reasons, it is highly desirable that the 2708s in kits, computers and equipment should soon be changed to the 2716 so that single power supply working is possible. Two 2708s can now be replaced by a 2716: two 2716s can be replaced by a single 2732. A number of manufacturers now make these EPROMs. Hence the EPROM Duplicator described here will be well worth its construction, because it is simple in circuitry and needs no micro-processor.

CIRCUIT DESCRIPTION

Two sockets are required, one for the EPROM being copied to (marked 'B') and one for the chip being copied from ('A'), both of which should be 24-pin zero-insertion-force sockets.

Note that the data pins and address pins of both are connected in parallel, because, for any particular address location, the data from one goes into the other in the process of duplicating. However, if a 2708 is the source EPROM, then it has no A10 pin because it has only 1K byte addressing capacity. Instead, that pin no.19 in the 2708 happens to be a +12V supply. Further, pin 21 is V_{BB} which is a -5V in the 2708. If the source EPROM is also a 2716, then pin 19 is A10, the most significant address bit and pin 21 is V_{pp} which should also be +5V only.

So, a change-over switch S1 is used to copy from a 2708 or a 2716 chip in socket A. Since a 2708 has only 1K data bytes, and as the 2716 has 2K capacity in it, the data from the former could be copied either into the first or second half of the latter. In other words, two 2708s with consecutive address range can be copied into one 2716. Switch S2 selects which half of the 2716 in socket B needs to be copied, at the time. This S2 makes pin 19 (A10) either low or high and accordingly selects either the first or second half of it.

If socket B uses a 4K EPROM, the 2732, then it is possible to transfer two numbers of 2716 or four numbers of 2708s into it. Switch S3 selects either the first or the second 2K of the 2732. If the source EPROMs in socket A are 2708s, then switch S2 also has to be used.

IDEAL FOR COPYING DATA FROM ONE EPROM TO ANOTHER, FOR EXAMPLE, TO UPGRADE FROM AN OLD THREE-RAIL 2708 TO A NEW SINGLE-SUPPLY 2716.

As already mentioned, programming a 2716 or 2732 requires the application of a single 50ms pulse to pin 18 after applying the address and data to these pins. When the next address is chosen, data at that address of the source EPROM gets applied to the data input pins of the 2716. Again, another pulse is applied. This goes on until the entire memory has been programmed.

In order to sequence the address and apply the 50ms pulse after each address has settled, we require the remaining part of the circuit of Fig. 2. A clock generator is formed using a simple CD4011 astable circuit using two of its gates. The values of R2-C1 give a time of about 75ms, so that a series of rectangular pulses of 75ms half-period are applied, via a CD4049 inverting buffer to the clock input of a 12 bit binary counter CD4040. The CD4040 clocks during each negative-going edge at its clock input pin 10. The address information of the EPROMs changes at this instant, once for each pulse. So, during the positive-going swing of the oscillator output, the address gets changed every time (Fig. 1).

Note that the output of the CD4011 (pin 11) is also coupled via C2 to another CD4011 (2), which is connected as a 50ms monostable using two of its gates. So, at each negative-going edge of the 75ms clock, the 50ms pulse comes out and gets applied to the programming pin via one or two buffers, using CD4049. Thus, after the address has settled, considerable time is allowed before a 50ms pulse is given to the socket B at pin 18 to program the EPROM.

After going through a series of 2K clock periods, all of the locations will have been programmed with the corresponding data in the source EPROM. After completing 2K counts, pin 1 of 4040 goes high, which would make D2 glow via the CD4049 buffer, indicating completion of programming. Now switch S4 is opened to isolate the 25V programming supply.

Starting and Resetting is done by a pair of flip flops formed by the first 4011 i.c. When 'Reset' is pressed, it causes a high level pulse to be applied to the reset pin 11 of the 4040, so that the address bits start from 0 initially. The

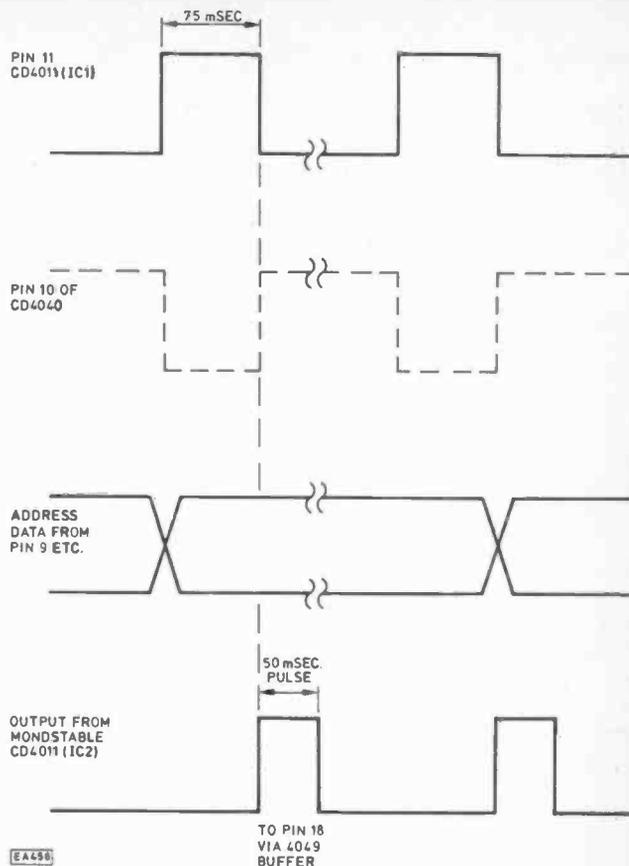


Fig. 1. Timing diagram

'Start' push switch makes pins 3 and 8 of the astable oscillator high so as to enable the clock oscillator. D1 glows to indicate that programming is in progress.

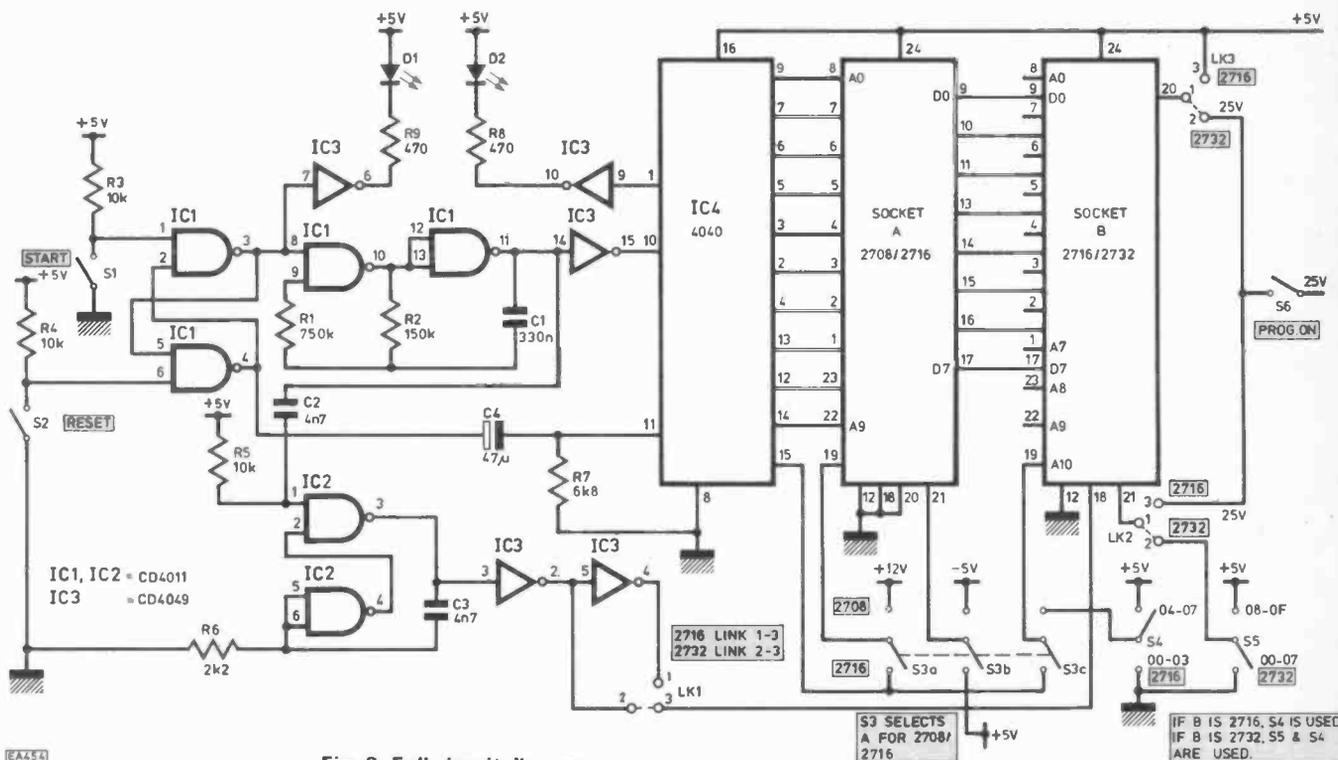


Fig. 2. Full circuit diagram

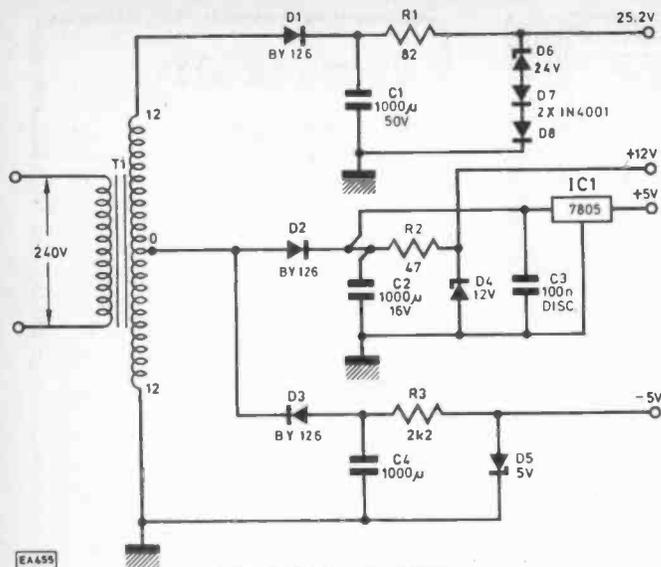


Fig. 3. Suggested PSU

USING THE DUPLICATOR

- 1) Insert Master or Source EPROM in socket A. It may be 2708 or 2716.
- 2) Select S1 for 2708 or 2716 of source chip and S2 for programming on to first or second half of the chip on socket B, if it is a 2716.
- 3) If the B chip is a 2732, select the first 2K part or second using S3.
- 4) Insert new or erased EPROM in socket B.
- 5) Keep S4, the programming power switch, open.
- 6) Apply power supply voltages, -5V first and then the +5V, +12V and +25V. For a source 2716, the -5V and +12V are not necessary.
- 7) Press Reset and then Start. D1 is now ON.
- 8) Close S4 at once. It takes about 4 minutes to go through the 2K locations. When D2 comes on, open S4. Switch off the power. Remove chip from socket B. It will have copied that part of A in it.
- 9) For programming the other half of the 2716 or 2732 as the case may be, proceed as above, with the switches S2 and S3 kept in the next position, as follows:

Source chip 2708. Source chip 2716.

- Copied on 2716** S₂ down-2708(i)
S₂ up -2708(ii) S₂ anywhere
- Copied on 2732** S₃ down:
S₂ down-2708(i) S₃ down-2716(i)
S₂ up -2708(ii) S₃ up -2716(ii)
S₃ up:
S₂ down-2708(iii)
S₂ up -2708(iv)

TABLE 1. Programming data of the EPROMs

| Pin Nos. | 2708 | 2716 | 2732 |
|-----------|----------------------------------|----------------------------------|----------------------------------|
| 1 to 8 | A ₇ to A ₀ | A ₇ to A ₀ | A ₇ to A ₀ |
| 9, 10, 11 | D ₀ to D ₇ | D ₀ to D ₇ | D ₀ to D ₇ |
| 12 | Ground | Ground | Ground |
| 24 | V _{cc} (+5V) | V _{cc} | V _{cc} |
| 23, 22 | A ₈ A ₉ | A ₈ A ₉ | A ₈ A ₉ |
| 18 | 27V low to high prog. pulse | 5V TTL low to high pulse | 5V TTL high to low pulse |
| 19 | -12V | A ₁₀ | A ₁₀ |
| 20 | +12V | +5V | V _{pp} = 25V |
| 21 | -5V | V _{pp} = 25V | A ₁₁ |

COMPONENTS . . .

EPROM PROGRAMMER

Resistors

- R1 750k
R2 150k
R3-5 10k (3 off)
R6 2k2
R7 6k8
R8, R9 470 (2 off)
All ¼W 5%

Capacitors

- C1 330n/100V polyester
C2, C3 4n7/60V disc cer. (2 off)
C4 47µ/16V aluminium elect.

Semiconductors

- IC1, IC2 CD4011 (2 off)
IC3 CD4049
IC4 CD4040
D1 red 0.1" l.e.d.
D2 green 0.1" l.e.d.

Miscellaneous

- 16-pin sockets (2 off). 14-pin sockets (2 off). 24-pin sockets (pref. z.i.f. type) (2 off).

Switches

- S3 3p2w
S4 1p2w
S5 1p2w
S6 1p1w toggle
S1, S2 Push-to-make switches (2 off)

CONSTRUCTION

The unit is assembled on a printed circuit board, single-sided type of dimensions 115 x 13mm, inclusive of the switches as needed. The p.c.b. layout is shown in Fig. 4 along with component and jumper locations in Fig. 5. Note that there are three links shown in the circuit of Fig. 2. One of these chooses the system to work for duplicating on 2716 EPROMs, while the other is for the later version 2732. The alternatives for these links are also marked on the component layout diagram, one of which should be chosen.

The two i.c. sockets A and B are inserted and soldered first. One of these, at least, should be a z.i.f. socket if regular use is intended for this unit. The CMOS i.c.s are to be handled with the usual care and sockets are needed for them too. The jumpers are connected carefully, after inspecting the same with the reference made to Fig. 2. The wiring to the switches is made underneath the p.c.b. The switches are mounted below. Supporting ebonite pillars are used on four corners. If you intend copying only on 2716 type EPROMs, no S3 is needed. The power supply points are brought out to a strip screw type connector mounted at one edge of the unit. The 25V supply should also be made through this. An external switch S4 in the 25V line is necessary, if the 25V p.s.u. does not have one in itself.

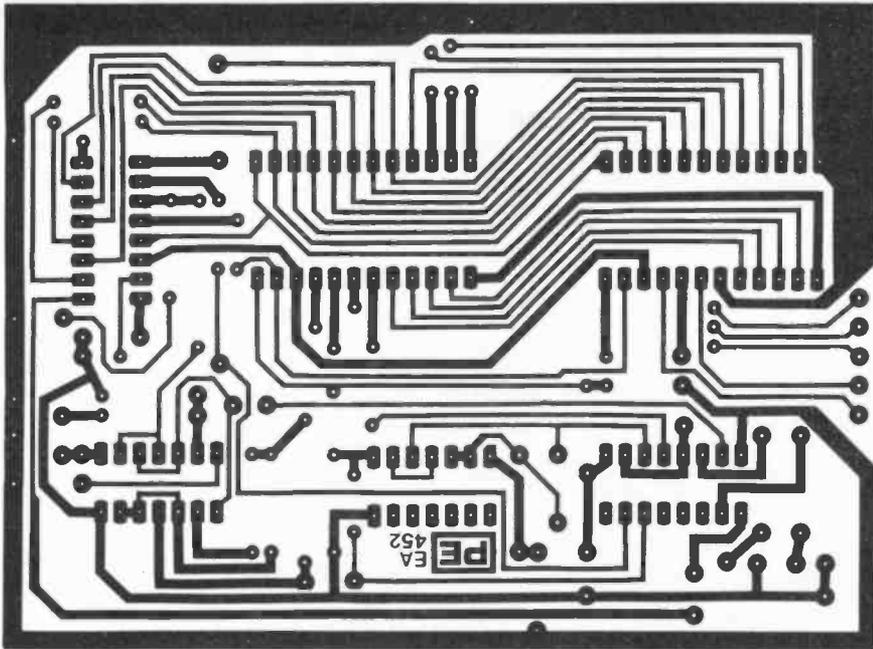


Fig. 4. P.c.b. track layout (actual size)

COMPONENTS . . .

SUGGESTED PSU

Resistors

| | |
|----|--------------------|
| R1 | 82 |
| R2 | 47 $\frac{1}{2}$ W |
| R3 | 2k2 |

Capacitors

| | |
|--------|-------------------------|
| C1 | 1000 μ /50V |
| C2, C4 | 1000 μ /16V (2 off) |
| C3 | 100n disc |

Semiconductors

| | |
|--------|----------------------|
| D1-3 | BY126 (3 off) |
| D4 | 12V/1W Zener |
| D5 | 5V/1W Zener |
| D6 | 24V/1W Zener |
| D7, D8 | 1N4001 (2 off) |
| IC1 | 7805 regulator |
| T1 | 230V/12-0-12V @ 0.5A |

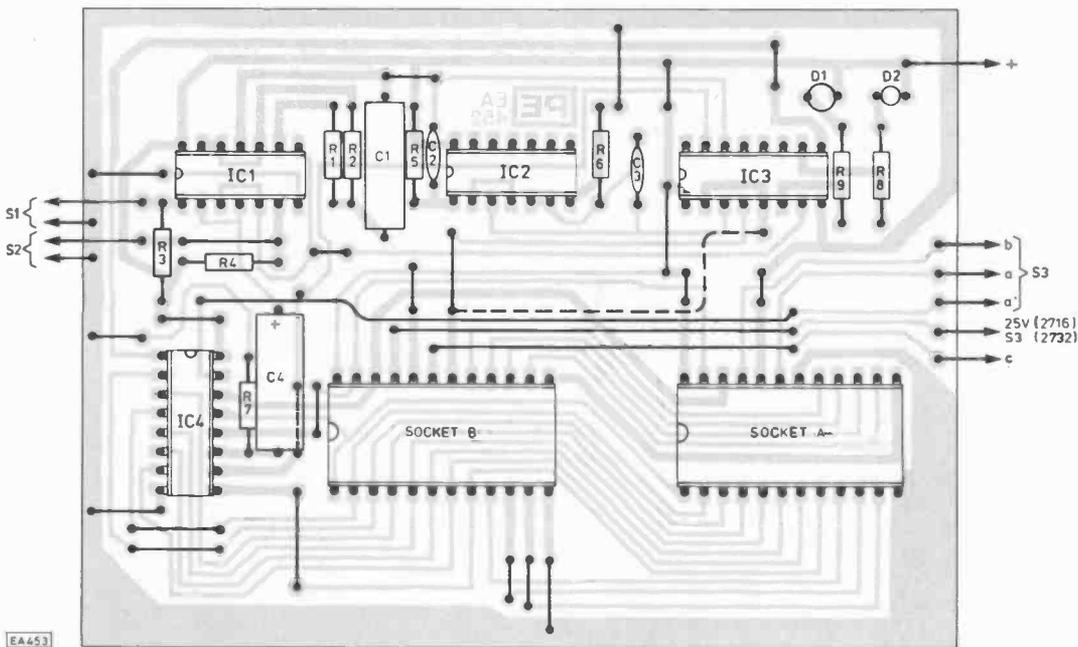


Fig. 5. Component layout of EPROM duplicator

TESTING

First apply 5V only to the unit, after just inserting the CMOS i.c.s, leaving the A and B sockets free. Pressing the start push button should enable the oscillator and at pin 11 of CD4011 (observe the waveform shown on Fig. 1). D1 should be ON. The 4040 should now be counting these pulses, as may be checked by scoping at its output pins 9 through 15. Pin 3 of the CD4011 should be producing a train of 50ms pulses. If not check the connection to pin 1 of it and also the wiring of R6 and C3.

Now check if the address pins of the EPROM sockets are all receiving the outputs of the CD4040. Pin 19 of socket A

will not receive it if S1 is up, selecting the same for a 2708 chip. Likewise pin 19 of socket B will not receive it if a 2708 chip is used for A.

Then check if the 12V and -5V points on the terminal connector maintain continuity with the pins 19 and 21 of socket A in the S1 switch's up position.

After about 4 minutes, D2 should light up.

If the above does not check out properly, carefully examine the p.c.b. for solder bridges, faulty solder joints or missing jumpers. Also check that the connections to switches are wired as per Fig. 2. ★

ADD ON Sub-Woofer

C.HARDCASTLE

THE Minimax II and GB3 bookshelf speakers, as most of you will know, have been the pre-eminent speakers in their class for over 10 years in the United Kingdom. They continue to sell well and remain as popular as ever.

They were conceived as a small speaker in which quality of sound was not sacrificed because of their small size and low price. Despite the compromise which necessarily had to be made to make such a small speaker sound good, Videotone were able to maintain a smooth frequency response and outstandingly low distortion. Due to their small size, and low distortion, they provided an exceptional stereo image. The one area of deficiency which they share with other small speakers is in the bass extension. Try as one will, the physics of a small cabinet limit the lowest frequency which can be generated in any given size.

To help overcome this, Videotone's engineers have designed a special sub-woofer to extend the bass response down to frequencies more normally associated with large, expensive speaker systems.

PHASE DIFFERENCE

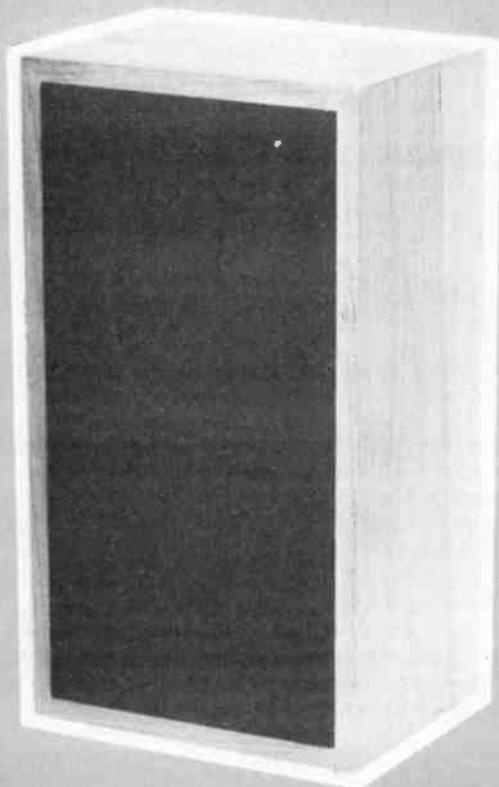
One of the great advantages enjoyed by speaker designers in the low frequency area is that the human ear cannot distinguish phase differences. As a consequence, low frequencies play a very small part in the area of stereo imaging and one bass speaker (sub-woofer) can be placed virtually

anywhere in a room without degrading stereo performance.

Knowing that a great number of *PE* readers have Minimax II and GB3 speakers from the *PE* special offer made in the September 82 issue, it was felt that there would be good interest in a sub-woofer to suit these speakers.

This sub-woofer can be built as a kit or bought as a completed unit. To this end, we have made the construction as simple as possible, consistent with the high quality performance required. Essentially a sub-woofer is a simple device as all the science and art is in selecting the appropriate bass drive unit and designing the cabinet and crossover to suit. Fig. 1 gives the basic construction details including dimensions and materials. We have selected a Coral Woofer, type 10L60, as having the best balance of sound to suit the Minimax speakers. Previously Videotone have used the same drive unit as the woofer in their GB3 speakers, retailing nowadays at over £400. This gives some idea of the quality of sound which we have aimed at. *The crossover has been designed to allow the sub-woofer to be connected across one channel of your amplifier* without giving a complex load. The crossover brings in the 10L60 smoothly to balance the performance of the Minimax II and GB3 and then the natural roll off of the 10L60 is used at the very low end.

Because of the complexity of the measurements involved in combining one woofer with two other speakers, we have not published frequency response curves. However, the design was refined by extensive listening tests on a wide variety of material and under different listening conditions. The result of using the sub-woofer in the manner described, is to extend the bass response of the M2 and GB3 down towards 20Hz in a satisfactory and cost effective way.



CONSTRUCTION

The sub-woofer can be purchased as a completed item or any of the major component parts may be purchased separately. Prices are listed along with the specification.

If the complete kit of parts is purchased, i.e. the Coral drive unit, the crossover and the cabinet, then simple assembly as in Fig. 1 is all that is required.

If, however, the reader wishes to make the cabinet then the information given in Fig. 1 should serve as a guide. The important factors to bear in mind are that the drive unit should be mounted centrally, and that the following basic dimensions should be used. The cabinet should measure 550mm high by 230mm deep and 300mm wide, it should be constructed from a suitable 19mm ($\frac{3}{4}$ ") board. All the inside surfaces should be damped with 1" acoustic foam.

The crossover unit Fig. 2 consists of a simple two element network of a 17.5mH inductor (L1) with an internal resistance of 2.2Ω (to prevent sharp impedance rising) and a $150\mu\text{F}$ capacitor (C1). These components should be mounted on the p.c.b. and fixed to the back of the cabinet.

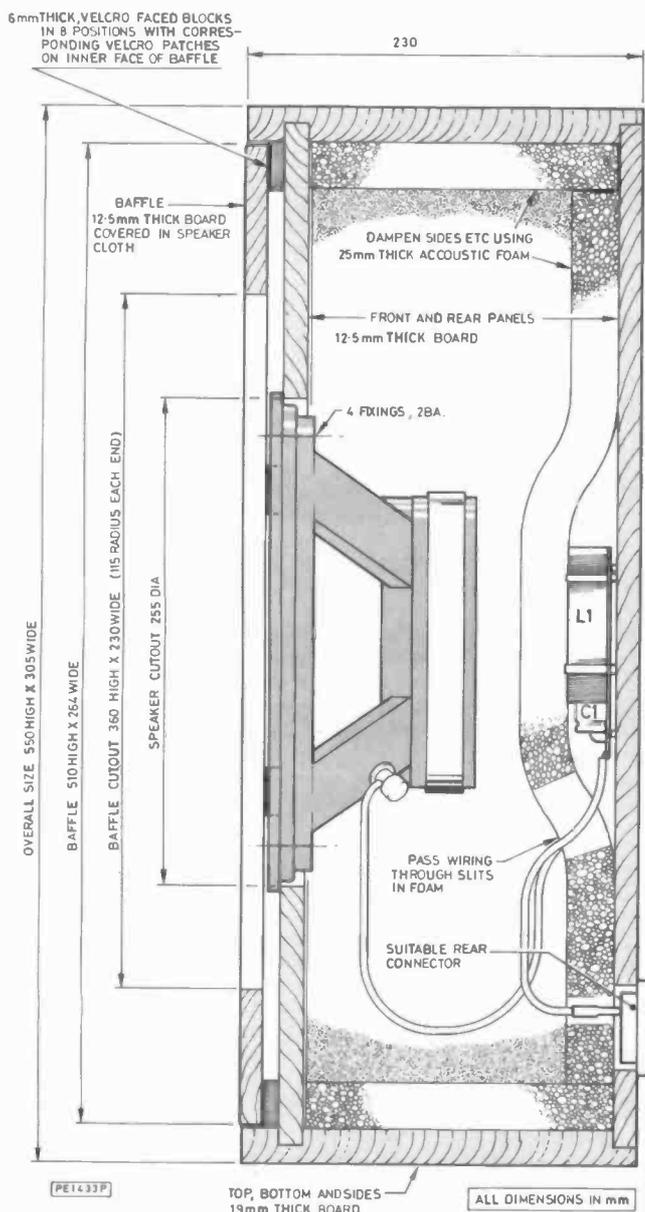


Fig. 1. Showing general construction information

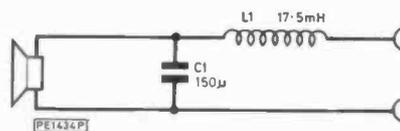
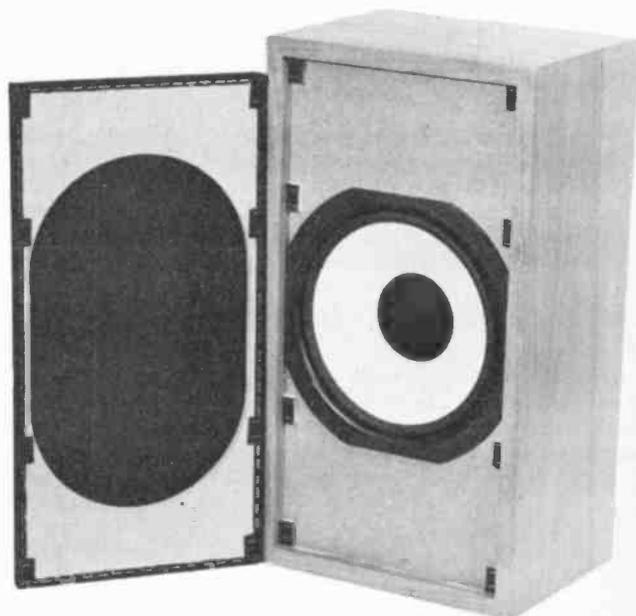


Fig. 2. The crossover unit consists of a simple two element network consisting of a 17.5mH inductor (internal resistance 2.2Ω) and a 150μF capacitor



The baffle can be seen here with the speaker cloth stretched over it and stapled in position on the back. The Velcro fixing method can also be seen

SPECIFICATION

General

Frequency response: 30Hz–100Hz
 Power Handling: 60W r.m.s.
 Sensitivity: 90dB 1W/M.

Coral 10L60 25mm Bass unit:

Impedance: 8 ohms
 Program Source Input: 60W
 Lowest Resonance Frequency: 28Hz
 Frequency Response Range: FO 5,000Hz
 Sound Pressure Level: 94dB/W-M
 Total Magnetic Flux: 160,000 Maxwell
 Weight: 4.5kg
 Effective Cone Radius: $a = 10.7\text{cm}$
 Effective Mass of Cone: $M_0 = 33\text{g}$
 $Q_0 = 0.33$

Prices: Drive Unit: £30-60.
 Crossover: £5.75.
 Cabinet: £12-65.
 Kit of parts: £49.
 Ready built unit: £69-95.

All the above prices include VAT and p&p. Cheques etc. should be made payable to **Perdix Components Ltd.**, Unit 4, Airport Ind Est, Biggin Hill, Kent.

SEMICONDUCTOR CIRCUITS

TOM GASKELL BA(Hons) CEng MICE

PROGRAMMABLE TIMER (ICM 7240)

THE use of counting and timing i.c.s is very widespread in electronics. Indeed, the vast majority of logic or control circuits contain many such devices, either as astable multivibrators (oscillators and clocks) or monostables (single shot timers) for altering pulse widths, and the like. Counting or dividing circuits are often associated closely with timers or oscillators as a practical means of adding extra ranges of timing, or adding extra flexibility to the way in which the timing is done. This month we feature the ICM 7240, a CMOS programmable timer i.c. containing just such an arrangement of timer and counter.

BASIC OPERATION

The block diagram of the ICM 7240 is shown in Fig. 2. The timing section uses a single resistor and capacitor, R_T and C_T , to determine the basic frequency of oscillation of the timebase. The timebase oscillator has a frequency of $F_c = \frac{1}{RC}$, i.e. a period $T_c = RC$.

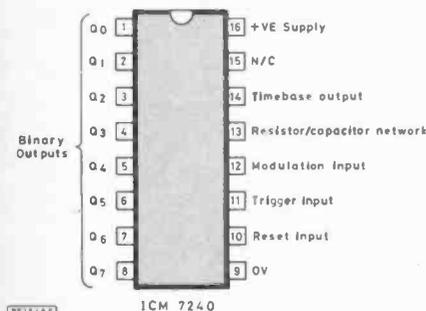
The timebase output is normally a logic 1 level with a series of narrow negative going pulses at the relevant frequency. These are fed out to pin 14 of the i.c., and also to an internal 8 stage binary divider. Hence, output Q0 is at $\frac{1}{2} F_c$, Q1 is at $\frac{1}{4} F_c$, Q2 is at $\frac{1}{8} F_c$ etc. Each output is an 'open drain' FET—a somewhat dubious term used to describe a FET with its drain taken out directly and with no internal loading! (It is the CMOS equivalent to an open collector transistor arrangement.) Hence, to achieve any kind of voltage swing, outputs Q0 to Q7 must be taken up to the positive supply rail with a suitable load resistor.

The operation of the whole i.c. is controlled by a flip-flop with reset and trigger inputs. These are loaded with internal 50k pull-down resistors, and hence do not require any external biasing if unused. Series 56k resistors

should be used at all times, as shown, to prevent possible internal damage to the i.c.; THIS IS VERY IMPORTANT. A positive (logic 1) pulse on the reset pin turns all outputs off (i.e. logic 1 if pulled up to the positive supply) and stops the timebase oscillator from running. This situation continues even after the removal of the reset pulse, until a positive pulse is fed into the trigger input. At this point the outputs are all turned on (set to logic 0) and the timebase oscillator starts running. If both reset and trigger pulses are applied at the same time the trigger pulse has priority and the circuit starts running. When power is first applied to the i.c. internal circuitry ensures that the device is forced into the reset state, awaiting its first trigger pulse. Both trigger and reset pulses should always be a minimum of 2.0µs in duration. Fig. 3 is a timing diagram for the i.c., showing the relationship between the control signals and the outputs.

MONOSTABLE AND ASTABLE OPERATION

The basic operational circuit for the i.c. is shown in Fig. 4. The timebase will start oscillating as soon as the trigger input is fed with a positive going pulse; to do this automatically when power is applied, take a capacitor from pin 11's 56k resistor to the positive supply, and a resistor from pin 11's 56k resistor to 0V. (Typically use a few tens of nF and a few kilohms.) With switch S8 in the open position, outputs Q0 to Q7 will change continuously in a binary sequence, and so the output of the circuit will be dependent on the settings of the switches S0 to S8. The outputs act in a 'wired OR' manner when connected together, because of their open drain output configuration. This means that if any of the binary outputs are turned on (i.e. logic 0), the output must be at logic 0 (a low level). Conversely,



ICM 7240

| Characteristics | Notes | Minimum Value | Typically | Maximum Value | Units |
|---|--|---------------|------------|---------------|--------|
| Supply Voltage | All specs measured at +5V unless otherwise stated | 2 | | 16 | V |
| Quiescent Current | See Fig. 2 { $C_T=100nF, R_T=10k$ $C_T=100nF, R_T=1M$ | | 300 120 | 700 500 | µA |
| Temperature Range | | -20 | | +85 | °C |
| Timing Accuracy | | | 5 | | % |
| Timing Drift | 0 to +70°C | | 250 | | ppm/°C |
| Maximum Frequency | | | 1.0 | | MHz |
| Timing Resistor | (R_T in Fig. 2) Recommended Practical Limits | 1k | | 22M | Ω |
| Timing Capacitor | (C_T in Fig. 2) Logic 0, sinking 3.2mA Logic 1, sourcing 1.0mA | 1000p | | | F |
| Timebase O/P Voltage | Pin 13 to 0V | 3.5 | 0.25 | 0.6 | V |
| Leakage Current | | | 4.2 | | V |
| Trigger Input Threshold | { +ve supply = +5V +ve supply = +15V | | 1.6 3.5 | 2.0 4.5 | V |
| Reset Input Threshold | { +ve supply = +5V +ve supply = +15V | | 1.3 2.7 | 2.0 4.0 | V |
| Maximum Output Sink Current | Pins 1 to 8 (Binary Output) | 3.2 | | | mA |
| Binary O/P Saturation Voltage | At 3.2mA O/P Current | | 0.22 | 0.4 | V |
| Binary O/P Leakage Current | | | | 1.0 | µA |
| Maximum Input Frequency When Using External Clock (Square Wave) | { Using O/P Q7 only (+256) Using any (or all) O/P's (Supply= +5V) | 2 | 6 13 | | MHz |
| | | | | 100 | kHz |

Fig. 1. Pin out and specification

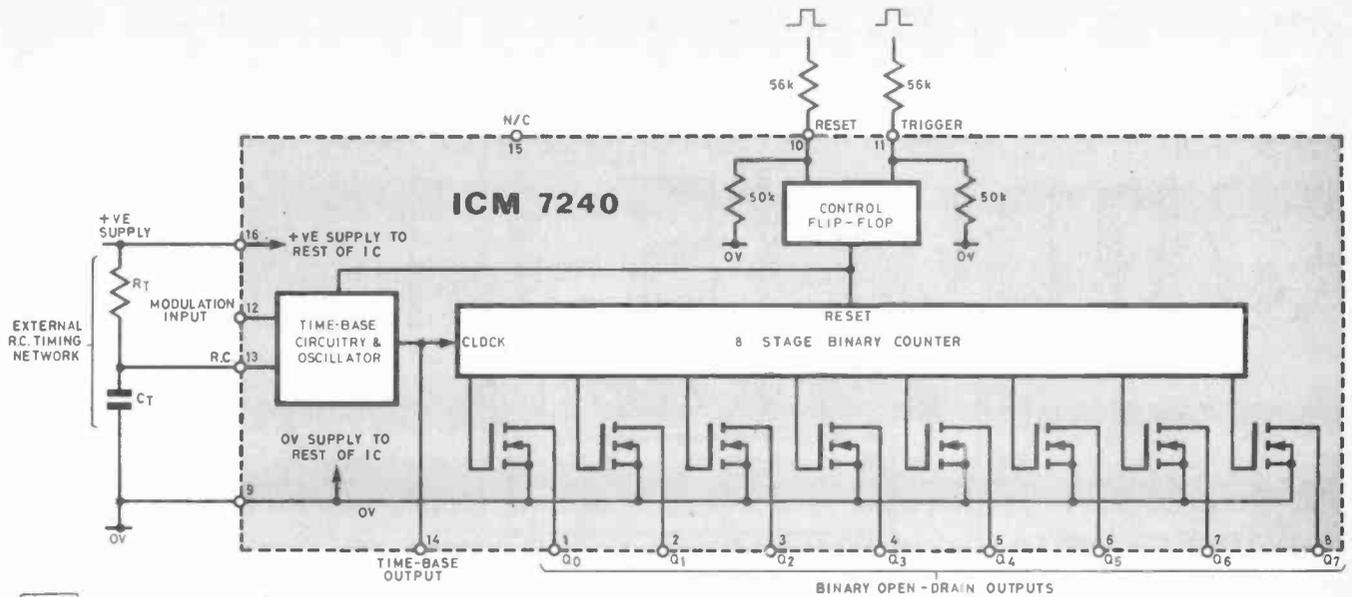


Fig. 2. Block diagram

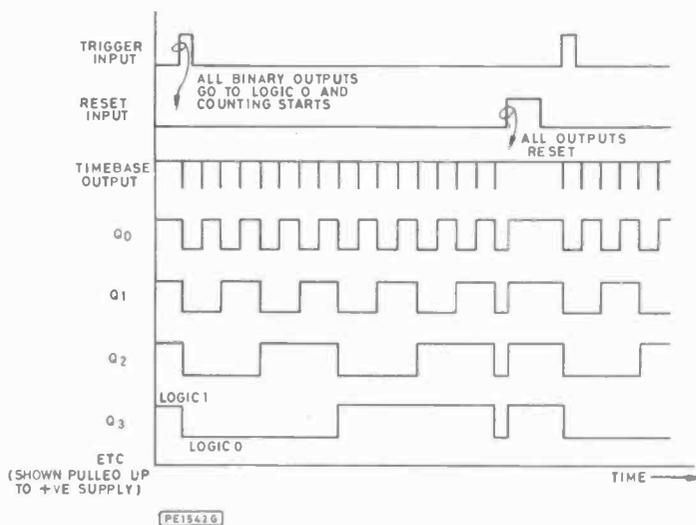


Fig. 3. Timing diagram

for the output to be at logic 1 (a high level), all the binary outputs must be at logic 1; or more accurately, turned off. Hence, the output waveform will be a simple square wave if only one switch is closed, or a complex mixture of square waves if several are closed. These output patterns will continue until the device is reset.

If switch S8 is closed we can use an appropriate combination of outputs to reset the i.c. For example, if S3 alone is closed (plus S8, of course), the i.c. will count normally for eight timebase periods, since for that time interval the Q3 output will be at logic 0. At the end of the eighth time period, however, output Q3 turns off, allowing RL to pull the output up to logic 1. This in turn resets the ICM 7240, turning it off until the next trigger pulse arrives. Hence, the output is a negative going (logic 0) pulse of a duration which is programmable by the settings of S0 to S7, which can

either be suitable switches or wire links, of course. Binary combinations of outputs can be used, so closing switches S0, S1, S3, and S4 gives a binary code of 00011011, for example. This corresponds to $16+8+2+1$; an output period of 27 timebase cycles. Note that the trigger pulse must be shorter than the monostable timing period required. Once triggered, all further triggers are ignored until either a reset pulse is fed into the i.c. or the timing period ends.

MORE SOPHISTICATED APPLICATIONS

As described, the i.c. allows for the generation of intervals from 1 timebase period to 255 timebase periods. It is very easy to cascade several i.c.s to produce dramatically long intervals; two i.c.s alone will produce output periods from 1 to 65535 timebase cycles! To couple i.c.s together in this way, connect both trigger inputs together (use a common resistor), connect both reset pins together (use a common resistor), and use a common output line for both sets of switches. Connect output Q7 (pin 8) of the first, i.e. least significant, i.c.

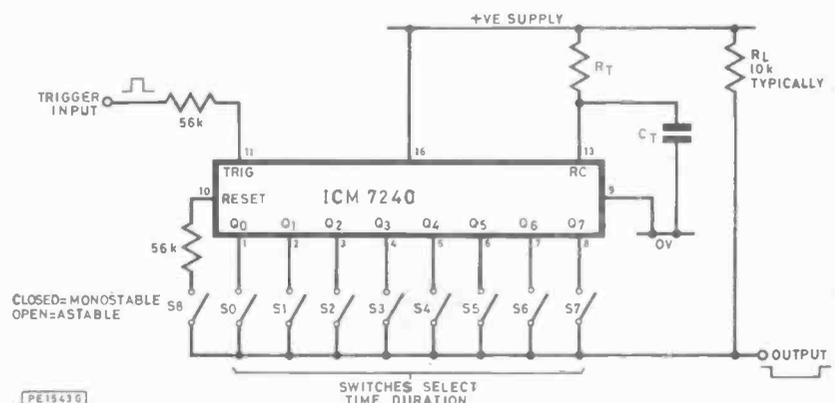


Fig. 4. Operation as astable or monostable

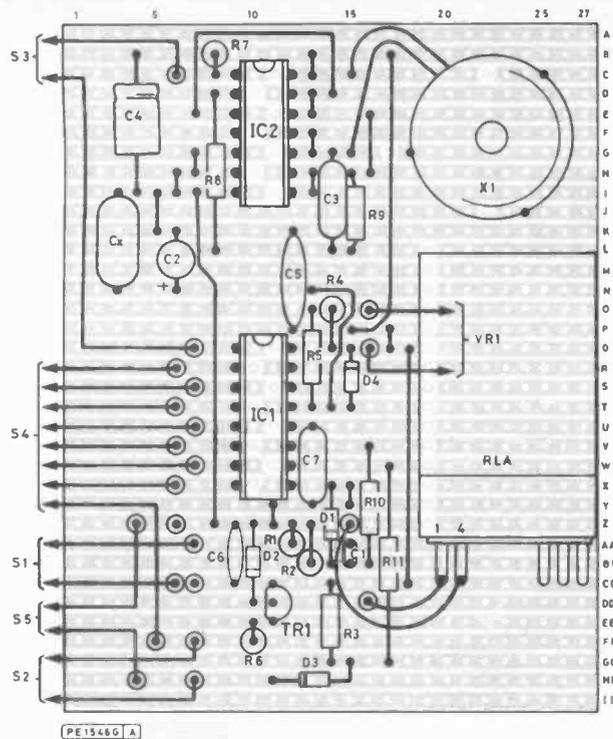


Fig. 6. Veroboard layout

law. Furthermore, VR1 must be a log law pot. This is all very important, since it allows VR1 to act as a fine trim control giving -1 stop at one end and +1 stop at the other, yet still being at zero, or 'normal', at the centre of its travel. Avoid changing any of these values, as

this could seriously affect the calibration of this pot. The exact 'normal' time duration is set by changing the value of C2, and adding extra capacitors as necessary, until the correct standard time interval is arrived at. (If required, the extra capacitors could be switched

in with a rear panel mounted d.i.l. switch.) Non-electrolytic or tantalum capacitors should be used if possible, to help ensure low leakage. C4, C5, and C6 decouple the power supply. D4 helps to protect pin 13 of IC1 if the power supply collapses suddenly, and C7 decouples the modulation input. If the circuit seems unable to stop timing, try adding more supply decoupling, or lower the supply voltage, since some i.c.s seem somewhat oversensitive at high supplies.

The least significant bit output, Q0, is taken via S3 to a simple tone generator formed by IC2 and piezo sounder X1. The resultant 'bleeps', nominally at once per second or so, help when 'dodging' and 'burning in' a print; techniques involving selective shading of the print for enhancement or special effect. Pressing S2 stops the exposure at any time, and switching on S5 turns the enlarger on continuously, to enable focusing prior to the printing paper being placed under the enlarger lens.

The project should be housed in a well-earthed metal case for safety, and fuses should be provided both on the incoming mains supply and the outgoing switched live to the enlarger. The 'normal' time period should be defined using standard negatives, chemical, and paper; this will typically be 10 to 20 seconds. Printing variations can then be readily accommodated using the f-stops on the lens, the f-stops on the timer, or both. Altogether, it's a much easier way of working in the darkroom!

The interesting and versatile ICM 7240 can be obtained from Watford Electronics. A similar, but not identical, bipolar device is also available; the μ A 2240.

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SLIDE DISSOLVE CONTROL

Peter F. Wells

THIS circuit uses a minimum of components and allows two projectors to be coupled together to give slide dissolve with automatic slide change on the dimmed projector.

With a little imagination this unit can be used to transform a rather dull slide show into a very interesting audio-visual presentation. When the prototype model was used with a synchronised cassette player, the results were quite stunning and have to be seen to be believed.

Only one half of the circuit need be described, as the other half is identical with the exception of the end connections to the slider potentiometer. These are reversed in order that the projector lamps are in antiphase to each other.

CIRCUIT DESCRIPTION

The circuit diagram of the Slide Dissolve is shown in Fig. 1. The power control circuit for both projectors consists of a bridge rectifier which carries the lamp current and a Darlington power transistor whose collector and emitter are connected directly across the d.c. connections of the bridge rectifier. The base current is controlled using the slider potentiometer, causing the lamp to fade as the transistor is gradually turned off. The inherent feedback within the bridge d.c. output, the power transistor and the slider potentiometer, ensures a linear fade between the two projectors.

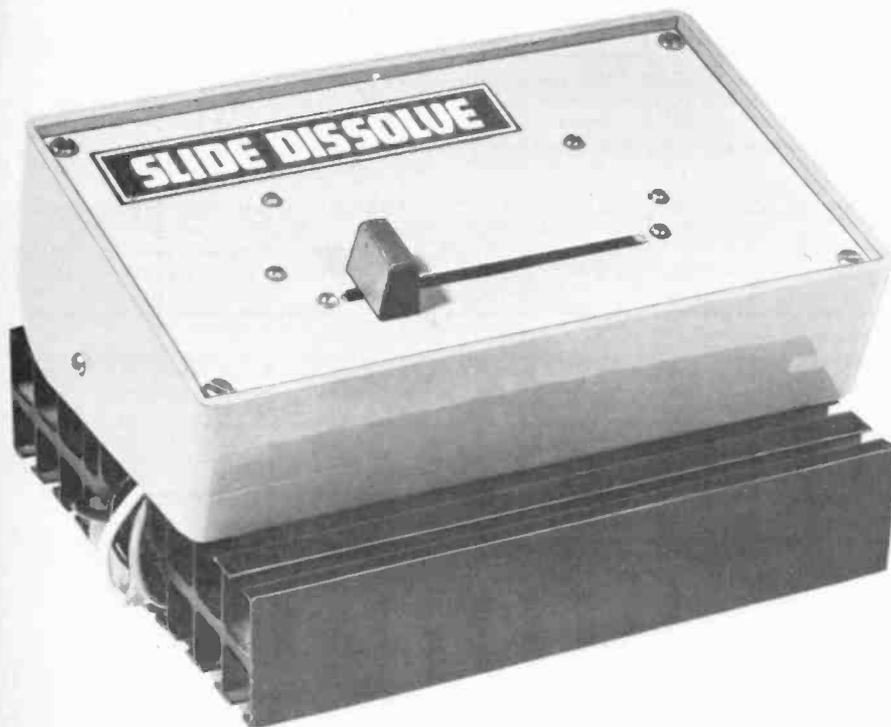
A lower cost alternative to the MJ3001 Darlington transistor is to use the more common 2N3055 with a BC108 or similar device, Darlington connected. As shown the fader is suitable for controlling two 24V, 150W projectors. If 300W projectors are used the transistors would need to be doubled up, but the 25A rectifier blocks need not be changed.

The micro switches are wired to operate the slide change solenoids in each projector. Most projectors require a pulse of current to increment the slide tray, with continuous current driving the slide tray in reverse. The single pulse is obtained from the depressed micro switch by allowing the slide change solenoid to energise via the capacitor charging current. As soon as the slider is moved to increase illumination on the second projector, the micro switch is released and the capacitor discharges through R1 and the normally closed contacts.

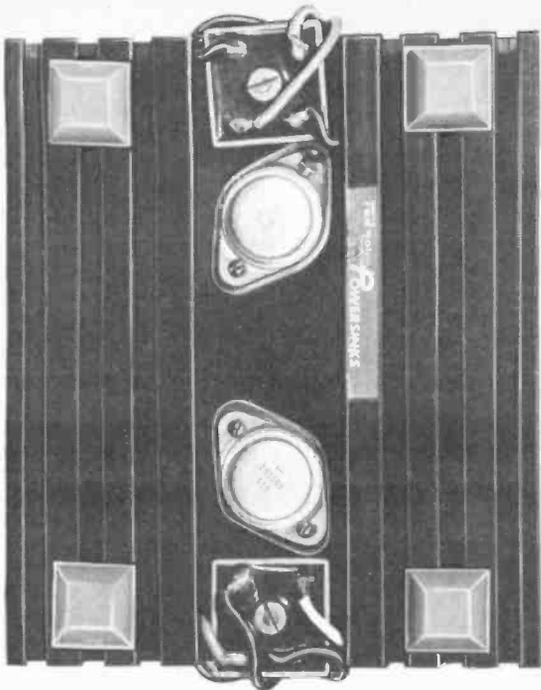
CONSTRUCTION

The bridge rectifiers and power transistors were all mounted on a standard heat shunt 152 x 130 x 32mm, 1.1°C/W (see photograph). The temperature of the shunt remains within reasonable limits as the major source of heat is generated within the bridge rectifier associated with the "on" projector. In this design, cooling was aided by placing the control unit so that the fan outlet blows air through the shunt.

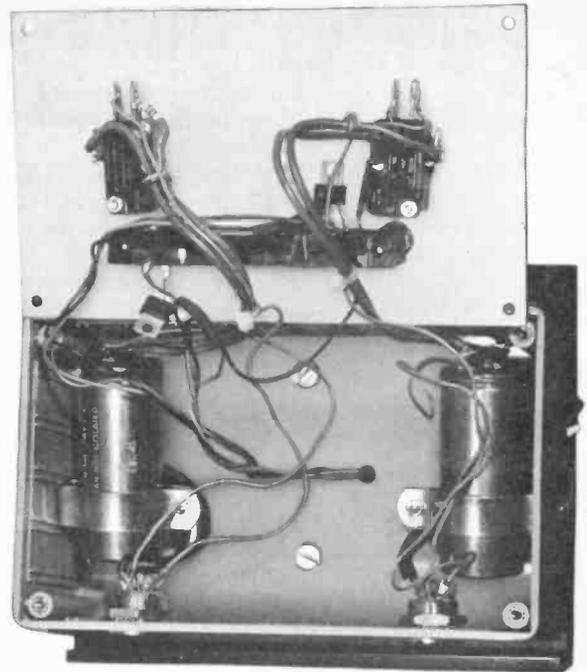
The two gang slider potentiometer was fitted into a suitable plastic box which was mounted on top of the heat shunt. The slider is arranged mechanically, to strike the micro switch lever at the end of travel in either direction as shown in Fig. 3. A plastic box was chosen to ease construction as slight problems may have been encountered when cutting the hole for the slider arm. The mounting holes for the micro switches and slider pot allow them to be bolted flat to the lid of the box, as shown in photograph.



A VERY PRACTICAL UNIT THAT WITH A LITTLE THOUGHT AND IMAGINATION COULD TRANSFORM AN ORDINARY SLIDE SHOW INTO AN INTERESTING AUDIO-VISUAL PRESENTATION.



Heat shunt assembly



Switch and slider potentiometer assembly

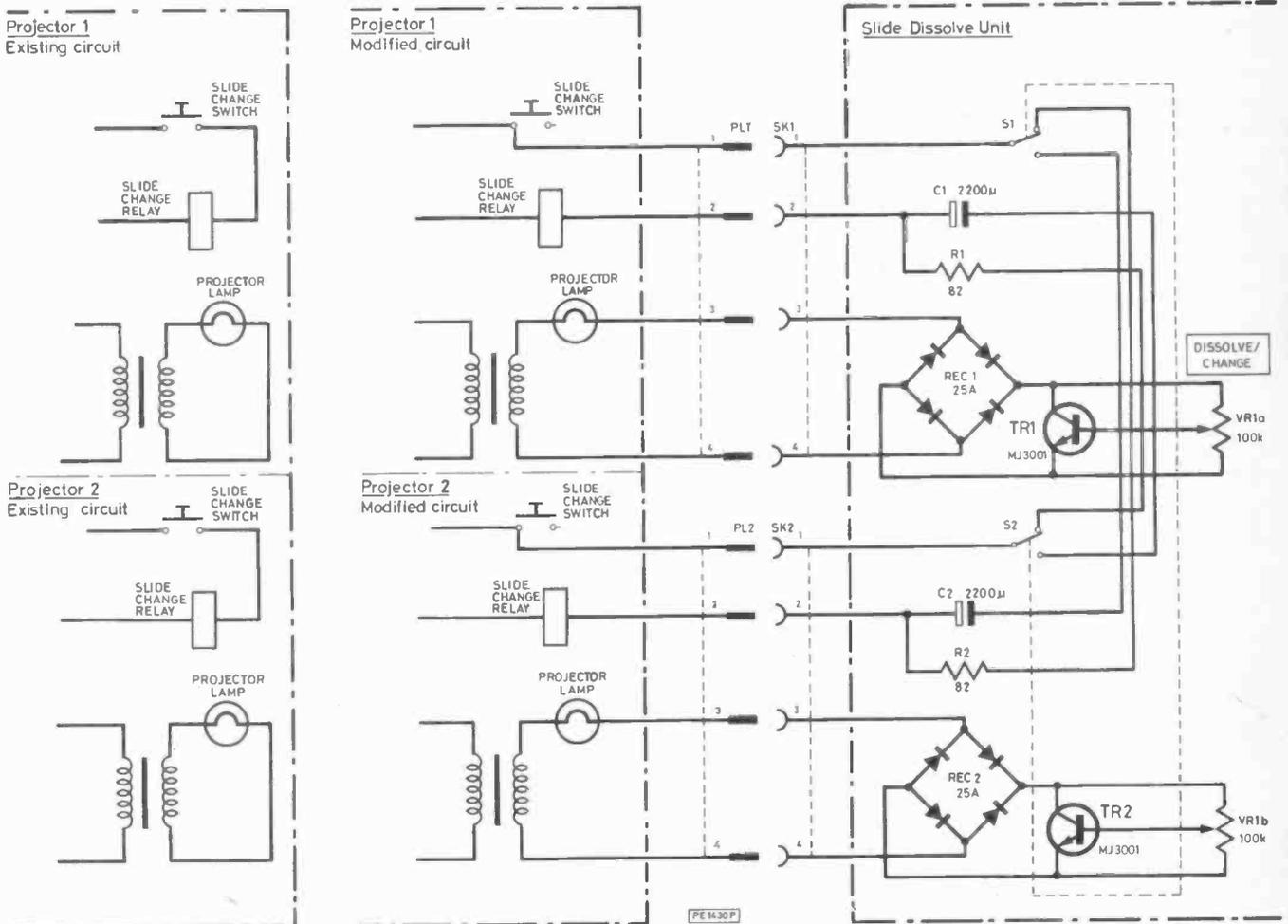


Fig. 1. Circuit diagram of the Slide Dissolve

All connections were made using 8 amp wire which was kept as short as possible to avoid any undue voltage drop. The wiring diagram is shown in Fig. 2.

Modifications to the projector wiring were made via 4 pin DIN sockets. The only connections to be made inside the projectors are a break in the feed between the 24V transformer, one side of the lamp, and the slide change push switch. If a single projector is to be used for conventional slide projection, a dummy DIN plug must be inserted with the lamp connections shorted out.

TESTING

The capacitors used in this design are 2200 μ , single ended types, but as the solenoid resistance may vary between manufacturers, it may be necessary to use different values.

When connecting the slide change wires to the capacitors and micro switches, the polarity must be determined with the projector switched on. A meter should be connected to the solenoid wires, which when the push button is pressed, will give an indication of the positive lead to be connected to the positive side of the capacitor. ★

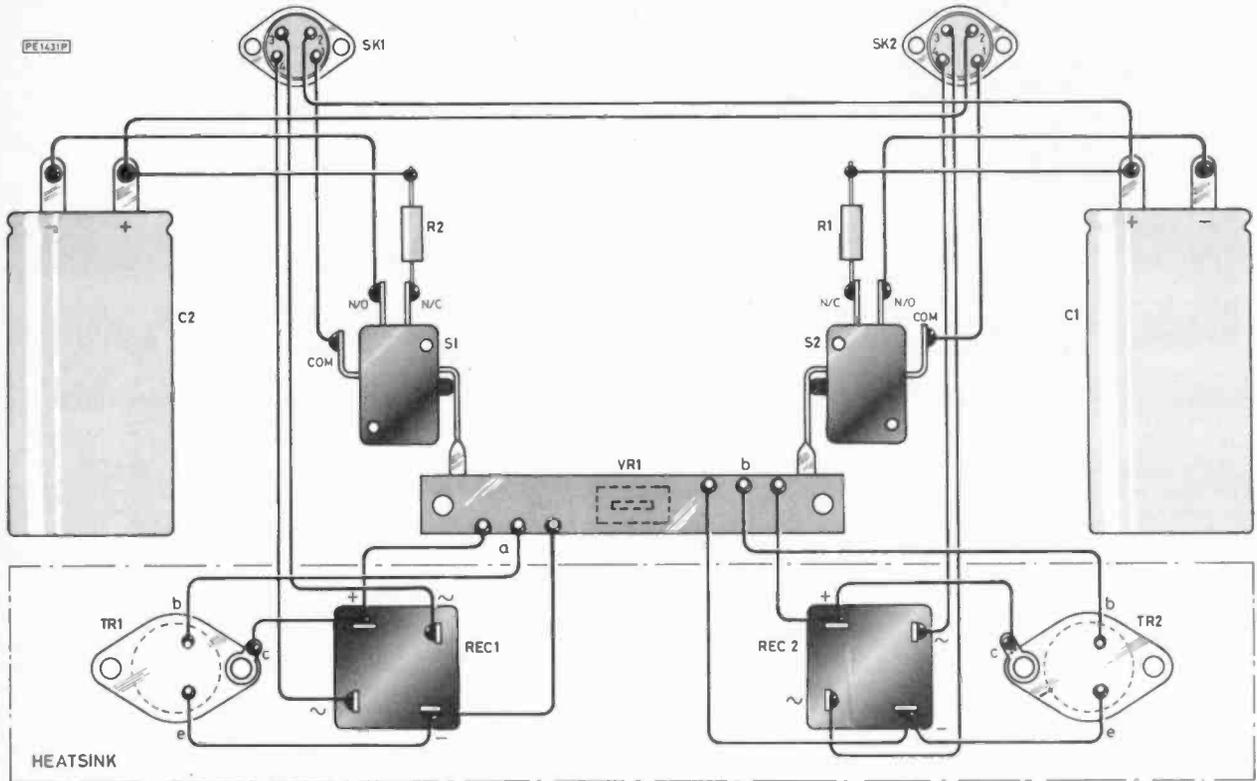


Fig. 2. Wiring diagram of Slide Dissolve

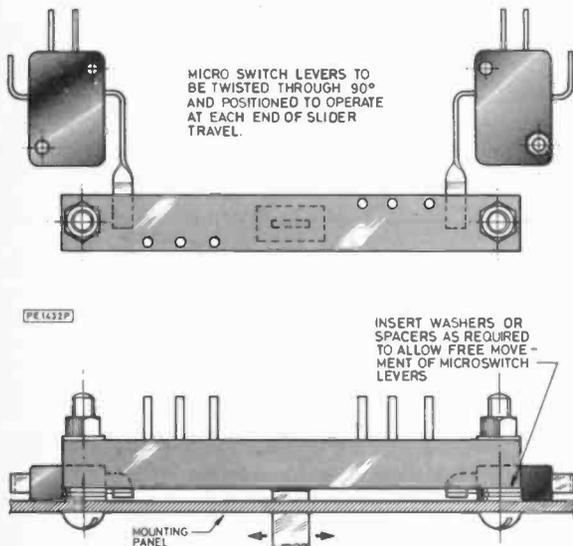


Fig. 3. Layout of slider pot and microswitches

COMPONENTS . . .

Resistors

R1, R2 82 $\frac{1}{2}$ W (2 off)

Potentiometer

VR1 100k slider dual gang

Capacitors

C1, C2 2200 μ 63V single ended (2 off)

Semiconductors

TR1, TR2 MJ3001 (2 off)

REC1, REC2 25A high power (2 off)

Miscellaneous

S1, S2 lever operated micro switch (2 off)

SK1, SK2 4 pin DIN socket (2 off)

PL1, PL2 4 pin DIN plug (2 off)

Heat shunt 152 x 130 x 32mm 1.1°C/W

T03 Mounting kit

PE micro~file

FILESHEET 17

R.W.Coles Z800

DESPITE their phenomenal success with the 8 bit Z80 microprocessor, Zilog came badly unstuck with the 16 bit Z8000 chip, coming a poor third to the Intel 8086/88 and the Motorola 68000. The choice of a Motorola 68008 processor for the new Sinclair QL personal computer by a design team which had previously produced three highly successful Z80 based designs (ZX80, ZX81, Spectrum) is symptomatic of the negative response to the Z8000 which has been demonstrated by most other system manufacturers who in the past have remained loyal to Zilog.

Some of the reasons for the failure of the Z8000 were analysed in detail in the relevant file articles, so there is no need to go over the gory details again. The good news is that Zilog have at last realised the error of their ways, and have introduced a new processor family which forms the subject of this month's file article and which is guaranteed to get all you Z80 fans drooling, even if the Z8000 left you cold!

Unlike the Z8000, the Z800 family is fully object code compatible with the Z80, which means that all existing Z80 and 8080 program code, including such things as the CP/M operating system and all the applications packages which run under it, will run unmodified on the new processor. Since users, quite understandably, are loath to part with all their *old* software just because they need extra power for their *new* applications, compatibility of this sort is very important, but it certainly isn't all that the Z800 has to offer.

When running old Z80 software, the new Z800 family will perform 4 to 5 times faster than its predecessor, and will make available at least twice as much memory space. When new applications software is written, however, and the full glory of the extended architecture and enhanced 16 bit instruction set of the Z800 is utilised, programmers will gain access to one of the most powerful 8/16 bit systems ever to become available.

Even the poor old Z8000 has not been forgotten, however, and although there is no direct software compatibility with that processor, versions of the Z800 will be available which interface to the 16 bit Z-Bus to provide an even greater level of performance for those systems not tied to an 8 bit Z80 style bus. In effect, the Z800 represents a bridge between Zilog's 8 and 16 bit systems, performing a similar function to that of the much earlier Intel 8088 in the 8086 family by offering complete software compatibility at the 8 and the 16 bit bus level.

In fact there will be four members in the Z800 processor family, two utilising a Z80 compatible 8 bit multiplexed data bus and coded Z8108 and Z8208, and the other two interfacing directly to the Z8000 style 16 bit Z-Bus, coded Z8116 and Z8216. (As with the Z8000 and Z8 families, there is no processor which is actually *coded* Z800, since this is merely a generic title.) Within each bus compatible pair the two available processors are divided into a "simple" and a "complex" version. The "simple" versions (Z8108 and Z8116) use a 40 pin package and consist of just a CPU with a restricted 512K byte address range. The two "complex" versions (Z8208 and Z8216) use a 64 pin package and offer the full 16M byte address range with numerous on-chip peripheral functions which in most other families require at least four additional packages.

To keep things simple, this file article concentrates on the two 8 bit bus compatible processors, since these are likely to be of the greatest interest to the many readers who are already familiar with the Z80. Featured on the file sheet is the Z8208 64 pin version, which includes all the additional peripheral facilities.

So what are we to make of this second 16 bit offensive from Zilog? There certainly is no doubt in *my* mind that the Z800 is the

processor that Zilog should have introduced back in 1979 when, instead, they introduced the Z8000. Had Zilog realised this at the time, the 16 bit market would have looked very different today, and Zilog would have had another winner on their hands, beating even the mighty Intel into second place.

Hindsight is a wonderful thing, of course, but at least Zilog have got it right now—or have they? Well, maybe not. They are very late with the Z800 and full production will not really be under way until late in 1984, long after the bulk of loyal Z80 designers have defected to the Intel, Motorola, or National camps. Introducing the right product for 1979 in 1984 is not a guaranteed recipe for success, and the great benefits which could have accrued from Z80 compatibility in the past will now be viewed by some as rather less than desirable. Remember the messy Z80 instruction set which was due in large part to the rigid insistence on 8080 compatibility? Well, Z80 code compatibility means that the Z800 has inherited every one of those idiosyncrasies, so it is unlikely to be viewed as a "nice" processor on its own merit.

On the credit side, the launch of the Z800 is a boon to all users of Z80 homebrew systems, since at last an upgrade path is available which does not involve throwing away all the old software. It will even be possible to build a small "daughter-board" with a Z8108, a crystal and an octal latch which can be plugged into any Z80 socket to provide an instant performance boost.

Also, it is only fair to note that all the peripheral functions available on the Z8208 and Z8216 could not have been integrated onto a single chip using 1979 processing technology, and many designers will welcome the Z800 just to get that kind of functional integration into their low-cost products. On the whole, I think the Z800 will be a limited success for Zilog, but what a pity they missed their chance of a real blockbuster!

REGISTERS

A glance at the file sheet will reveal that the Z800 family general register set is almost identical to that of the Z80, and that the only obvious change is the addition of an extra stack pointer so that "system" and "user" modes may be kept separate. The useful "primary" and "alternate" register file feature has been retained, as have the two index registers and the IR register pair, so there would appear to be no surprises.

Actually, however, there are quite a number of other changes which do not show up on the file sheet, but which offer a range of new and useful features to make the Z800 more acceptable to the more sophisticated potential customers of the 1980s, who now demand rather more from their chips than can be squeezed from the basic Z80 register set!

Apart from the extra stack pointer, the IX and IY registers have been modified so that they can now be accessed a byte at a time, and can therefore be used as pairs of general purpose 8 bit registers if required. Likewise, the Refresh register (R), although still in existence, is no longer needed for refresh purposes and is therefore available for the programmer to use as a general purpose 8 bit register. Dynamic RAM refresh is now controlled separately by a more sophisticated on-chip controller which generates 10 bit addresses compatible with the largest dynamic RAMs likely to be available during the life of the Z800.

Quite apart from these minor "tinkerings" with the Z80 set, though, the Z800 designers have also incorporated many brand-new features which have made it necessary to add a group of additional control registers (not shown on the file sheet) as follows:—

Bus Timing and Control Register: This 8 bit register can be set up by the programmer to select the required bus transaction timing parameters for I/O operations, high memory access, and interrupt daisy-chain response. The three two bit fields allow from zero to three wait states to be selected for each type of transaction, so that the system may be optimised to suit a particular hardware configuration. This register would normally be set up only once, during system initialisation.

Bus Timing and Initialisation Register: This 8 bit register is unusual in that it cannot be modified by the programmer, but only by external hardware connections made during reset. At reset, this register is either set to OOH (Wait input line low) or to the state of the AD bus lines (Wait input line high). By this means, a particular hardware configuration can inform the processor of its status during reset. There are two 2 bit fields and two single bit fields in this register, and these control clock scaling, wait states for low memory transactions, multiprocessor mode enable, and bootstrap mode enable, respectively. (Bootstrap mode allows the initial operating program to be loaded via the UART serial link after reset, so that slave processors can dispense with ROM based firmware.)

Interrupt Status Register: This 16 bit register contains various items of information about the status of interrupts, including which mode has been selected. (The Z800 has four modes, the Z80 has three.) Seven bits of this register are used as pending flags for the seven basic interrupt levels supported by the Z800.

Interrupt/Trap Vector Table Pointer: Twelve bits of this 16 bit register are used to select which 4K page is used to store the vector table required by the new Mode 3 interrupts and traps. Mode 3 operation is more powerful than any of the traditional Z80 modes, and is always used by the on-chip peripherals and the eight new error traps provided by the Z800.

Master Status Register: This 16 bit register contains a number of items of status information concerning the currently executing program and allows simplified nested interrupt handling. When an interrupt request is accepted, the Master Status Register, the address of the next instruction, and a 16 bit "reason-code" are pushed onto the system stack. New Master Status and Program Counter words are then fetched from the Interrupt/Trap Vector Table.

System Stack Limit Register: This 16 bit register performs the useful function of setting a lower limit on stack growth. An automatic error trap can be generated if this limit is exceeded.

Trap Control Register: Three of the eight traps, namely System Stack Overflow Warning (see above), External Processor Enable, and Inhibit User I/O, can be turned on or off by three bits in this register. The other five traps are not controlled by this register, although two of them, namely the Single Step and the Breakpoint-on-Halt traps, can be controlled via the Master Status Register.

In summary, Z80 users will be pleased with the compatible register set as shown on the file sheet, but they probably will not be so pleased when they have to wrestle with the intricacies of the new control register set, despite the powerful new options it provides!

Systems designed from scratch around the Z800 will, no doubt, protect the poor user from such frustrating features, by incorporating suitable system software to handle the control register problem.

ON CHIP PERIPHERALS

The Z8216 and the Z8208 (featured on the file sheet) both have an incredible array of built-in peripheral functions available, some of which are as complex as a microprocessor in their own right. Included on the chip are:—

- * 256 bytes of high-speed RAM (CACHE)
- * A Memory Management Unit (MMU)
- * An asynchronous serial interface (UART)
- * A four channel DMA controller (DMAC)
- * A four channel Counter/Timer (CTC)

These facilities are discussed individually below, but because of their complexity and the wide range of options possible, there is only room for a brief description here.

CACHE

The 256 bytes of on-chip RAM may be used either as general purpose read/write memory, mapped by the user, or as a high-speed data and instruction cache. The greatest performance advantages are gained in cache mode, since in this case the memory is used to hold up to sixteen separate 16 byte copies of areas of external (RAM or ROM) main memory, which may themselves hold instructions or data. In this mode the sixteen cache "lines" are continuously being refilled with copies of main memory up to 16 bytes long, which are built up while the processor executes a program. Each cache line is provided with a 20 bit address "tag" field and a 16 bit "valid" field. When data or instructions need to be fetched from memory, an address comparison with the sixteen tag fields is attempted, and if a cache "hit" is registered the code or data is fetched from the cache rather than from main memory. If a cache "miss" is registered then the cache controller uses a "Least Recently Used" algorithm to select one of the cache lines to be overwritten by the new data which has to be fetched from main memory.

The great advantage of the cache lies in the fact that most programs consist largely of tight "loops" of instructions or compact "tables" of data which are executed or accessed repetitively. If these loops and tables can be held in the fast cache memory area, they only have to be fetched once via the external bus. An analysis of typical Z80 programs has shown that most loops are less than 32 bytes long, needing only two cache lines on the Z800. Statistically speaking, the average cache hit rate could be as high as 90 per cent, giving dramatic improvements in execution speed.

If the programmer had to worry about controlling the cache, it probably would not be worth the trouble, but in the Z800 cache operation is transparent to the programmer. At reset, the memory is configured as an instruction-only cache, but this can be changed by the programmer via a special Cache Control Register to provide data-only or data-plus-instruction cache capability. A facility is also provided for burst-mode prefetching of instructions to allow even higher speed operation in some circumstances.

MMU

The Memory Management Unit performs a useful collection of tasks associated with memory addressing as follows:—

- Address expansion up to 16M byte.
- Separation of data and instruction memory.
- Separation of User and System mode memory.
- Write protection of selected memory areas.
- Virtual memory support via page fault traps.

At the heart of MMU operation are two sets of sixteen page descriptor registers that are used in address translation operations for the System and the User Mode respectively. The 16 bit logical address from the processor (the Z800 memory pointer registers are only 16 bits long remember) is divided into a 4 bit index field which is used to select a page descriptor register, and a 12 bit offset field which represents the address within a 4K byte memory page. The final 24 bit address value is then formed within the MMU by concatenating the 12 bit page frame address from the descriptor register with the 12 bit offset field supplied by the processor.

When all the descriptor registers have been set up by the programmer using a block move instruction, the processor has direct access to sixteen 4K pages in System mode, and sixteen 4K pages in User mode, making 128K bytes in all. To reach all other parts of the possible 16M byte memory map, the descriptor registers have to be rewritten.

The Valid bit indicates whether this descriptor has been set up to point to real memory, the Write Protect flag makes the page read-only, the Cacheable bit allows data fetched from this page to be placed in the cache, and the Modified bit is set whenever a write operation has been performed on this page. The other 12 bits are, of course, the most significant bits of the final 24 bit address value.

UART

The serial asynchronous receiver-transmitter provided on the Z800 chip seems to be the equal or better of any discrete UART chip which might otherwise be necessary. Transmission and reception can be performed independently with five, six, seven, or eight data bits per character plus optional odd or even parity. The transmitter can provide one or two stop bits and can provide a

GENERAL

This new 8/16 bit processor represents a second chance for Zilog to win back a share of the 16 bit market following the poor showing of the Z8000. It is unique in being a 16 bit device which is totally software compatible with its 8 bit predecessor - the highly successful Z80 - but this compatibility makes the Z800 a complicated, inflexible, processor available in four versions, offering Z80 or Z8000 bus compatibility and an impressive range of on chip peripheral functions, the Z800 would have been a smash hit if introduced in 1979 or 1980

REGISTERS & ON CHIP PERIPHERALS

| 15 PRIMARY SET | | 015 ALTERNATE SET | |
|----------------|---|-------------------|----|
| A | F | A' | F' |
| B | G | B' | G' |
| D | E | D' | E' |
| H | L | H' | L' |

| 15 | | 0 | |
|----|-------------------|---|--|
| I | R | | |
| IX | INDEX REG | | |
| IY | INDEX REG | | |
| PC | PROG. COUNTER | | |
| SP | USER STACK PTR. | | |
| SP | SYSTEM STACK PTR. | | |

MEMORY MANAGEMENT UNIT (MMU)

SERIAL CHANNEL (UART)

4 CHANNEL DMA CONTROLLER

256 BYTE CACHE MEMORY

4 COUNTER TIMER CIRCUITS

FLAGS

| | | | | | | | |
|---|---|---|---|---|-----|---|---|
| S | Z | / | H | / | P/V | N | C |
|---|---|---|---|---|-----|---|---|

PERFORMANCE DATA

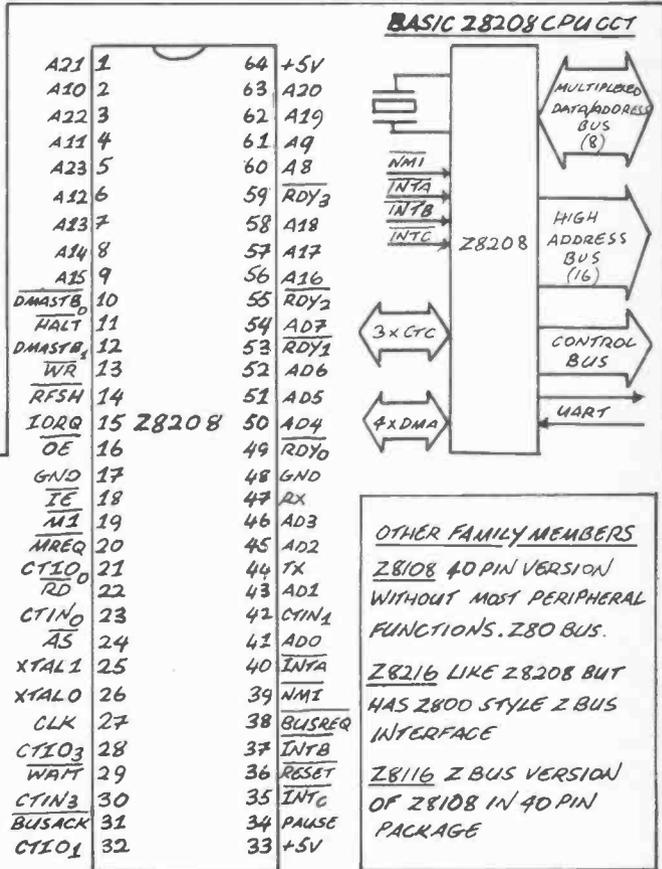
| | Z8208 |
|-------------------------|-----------------------|
| MEMORY ADDRESS RANGE :- | 16 M BYTE |
| I/O ADDRESS RANGE :- | 64K BYTE |
| CLOCK FREQUENCY :- | 10.MHZ* |
| POWER SUPPLIES :- | 5V |
| INTERRUPTS :- | NMI, INTA, INTB, INTC |
| *UP TO 25MHZ LATER | |

BENCHMARKS

| | Z8208 |
|----------------------------|----------------------------|
| ADD REG TO REG : | (Very dependent |
| O/P REG TO PORT : | on cache operation |
| MOVE FROM MEMORY TO MEMORY | and speed of memory used). |

INSTRUCTION SET AND SOFTWARE

The Z800 will run all Z80 code unmodified and is therefore compatible with CP/M. The instruction set has been extended to include additional 16 bit operations, and some new and powerful addressing modes have been added. The resulting set is messy but powerful, in true Zilog tradition.



OTHER FAMILY MEMBERS

Z8108 40 PIN VERSION WITHOUT MOST PERIPHERAL FUNCTIONS. Z80 BUS.
Z8216 LIKE Z8208 BUT HAS Z800 STYLE Z BUS INTERFACE
Z8116 Z BUS VERSION OF Z8108 IN 40 PIN PACKAGE

MANUFACTURERS

ORIGINATOR :- ZILOG

2ND SOURCE :- NONE ANNOUNCED, BUT PROBABLY MOSTEK AND SGS WILL SIGN UP.

SUPPORT CHIPS

THE Z8208 HAS MOST PERIPHERAL NEEDS CATERED FOR THE CHIP BUT CAN BE INTERFACED TO SLAVE PROCESSORS SUCH AS THE Z8070 FLOATING POINT MATH UNIT WHEN NECESSARY ALL Z80 AND 8080 PERIPHERAL DEVICES MAY BE USED SINCE THE Z8208 AND Z8108 USE A Z80 STYLE BUS.

Z800 INSTRUCTION SET

8-Bit Load Group

| Instruction | Operation |
|----------------|--|
| EX A,src | Exchange Accumulator A ↔ src |
| LD dst,src | Load Accumulator dst ← src |
| LD dst,src | Load Register (Byte) dst ← src |
| LD dst,n | Load Immediate (Byte) dst ← nn |
| * LDUD dst,src | Load in User Data Space (Byte) dst ← src |
| * LDUP dst,src | Load in User Program Space (Byte) dst ← src |

16-Bit Load Group

| | |
|---------------|--|
| EX src,HL | Exchange HL with Addressing Register src ↔ HL |
| EX (SP),dst | Exchange Addressing Register with Top of Stack (SP) ↔ dst |
| EX AF,AF' | Exchange Accumulator/Flag with Alternate Bank AF ↔ AF' |
| EX H,L | Exchange H,L H ↔ L |
| EXX | Exchange Byte/Word Registers with Alternate Bank BC ↔ BC' DE ↔ DE' HL ↔ HL' |
| LD(W) dst,src | Load Addressing Register dst ← src |
| LD(W) dst,src | Load Register Word dst ← src |
| LDW dst,nn | Load Immediate Word dst ← nn |
| LD(W) dst,nn | Load Immediate Word dst ← nn |
| LD(W) dst,src | Load Stack Pointer dst ← src |

| Instruction | Operation |
|-------------|-------------------------------------|
| LDA dst,src | Load Address dst ← address (src) |
| POP dst | POP dst ← (SP) SP ← SP + 2 |
| PUSH src | PUSH SP ← SP - 2 (SP) ← src |

Block Transfer and Search Group

| | |
|------|--|
| CPD | Compare and Decrement A ← (HL) HL ← HL - 1 BC ← BC - 1 |
| CPDR | Compare, Decrement and Repeat Repeat until BC = 0 or match: A ← (HL) HL ← HL - 1 BC ← BC - 1 |
| CPI | Compare and Increment A ← (HL) HL ← HL + 1 BC ← BC - 1 |
| CPIR | Compare, Increment and Repeat Repeat until BC = 0 or match: A ← (HL) HL ← HL + 1 BC ← BC - 1 |
| LDD | Load and Decrement (DE) ← (HL) DE ← DE - 1 HL ← HL - 1 BC ← BC - 1 |
| LDDR | Load, Decrement and Repeat Repeat until BC = 0: (DE) ← (HL) DE ← DE - 1 HL ← HL - 1 BC ← BC - 1 |
| LDI | Load and Increment (DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC - 1 |
| LDIR | Load, Increment and Repeat Repeat until BC = 0: (DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC - 1 |

8-Bit Arithmetic and Logic Group

| | |
|-------------|--|
| ADC (A),src | Add With Carry (Byte) A ← A + src + C |
| ADD (A),src | Add (Byte) A ← A + src |
| AND (A),src | And A ← A AND src |
| CP (A),src | Compare (Byte) A ← src |
| CPL (A) | Complement Accumulator A ← NOT A |

| Instruction | Operation |
|---------------|--|
| DAA (A) | Decimal Adjust Accumulator A ← Decimal Adjust A |
| DEC dst | Decrement (Byte) dst ← dst - 1 |
| DIV (HL),src | Divide (Byte) A ← HL - src L ← remainder |
| DIVU (HL),src | Divide Unsigned (Byte) A ← HL - src L ← remainder |
| EXTS (A) | Extend Sign (Byte) L ← A If A(7) = 0, then H ← 00 else H ← FF |
| INC dst | Increment (Byte) dst ← dst + 1 |
| MULT (A),src | Multiply (Byte) HL ← A × src |
| MULTU (A),src | Multiply Unsigned (Byte) HL ← A × src |
| NEG (A) | Negate Accumulator A ← -A |
| OR (A),src | OR A ← A OR src |
| SBC (A),src | Subtract With Carry (Byte) A ← A - src - c |
| SUB (A),src | Subtract A ← A - src |
| XOR (A),src | Exclusive OR A ← A XOR src |

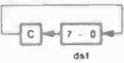
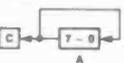
16-Bit Arithmetic Operations

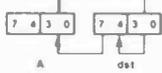
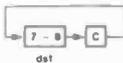
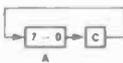
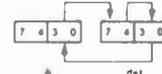
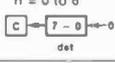
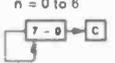
| | |
|------------------|---|
| ADC dst,src | Add With Carry (Word) dst ← dst + src + c |
| ADD dst,src | Add (Word) dst ← dst + src |
| ADD dst,A | Add Accumulator to Addressing Register dst ← dst + A |
| ADDW (HL),src | Add Word HL ← HL + src |
| CPW (HL),src | Compare (Word) HL ← src |
| DECW dst | Decrement (Word) dst ← dst - 1 |
| DEC(W) dst | Decrement (Word) dst ← dst - 1 |
| DIVUW (DEHL),src | Divide Unsigned (Word) HL ← DEHL ÷ src DE ← remainder |
| DIVW (DEHL),src | Divide (Word) HL ← DEHL - src DE ← remainder |
| EXTS HL | Extend Sign (Word) If H(7) = 0, then DE ← 0000 else DE ← FFFF |

16-Bit Arithmetic Operations (Continued)

| Instruction | Operation |
|----------------|---|
| INCW dst | Increment (Word) dst ← dst + 1 |
| INC[W] dst | Increment (Word) dst ← dst + 1 |
| MULTW [HL],src | Multiply Unsigned (Word) DEHL ← HL × src |
| MULTW [HL],src | Multiply (Word) DEHL ← HL × src |
| NEG HL | Negate HL HL ← -HL |
| SBC dst,src | Subtract With Carry (Word) dst ← dst - src - C |
| SUBW [HL],src | Subtract (Word) HL ← HL - src |

Bit Manipulation, Rotate and Shift Group

| | |
|-----------|---|
| BIT b,dst | Bit Test Z ← NOT dst(b) |
| RES b,dst | Reset bit dst(b) ← 0 |
| RL dst | Rotate Left tmp ← dst dst(0) ← C C ← dst(7) dst(n + 1) ← tmp(n) for n = 0 to 6  |
| RLA | Rotate Left Accumulator tmp ← A A(0) ← C C ← A(7) A(n + 1) ← tmp(n) for n = 0 to 6  |
| RLC dst | Rotate Left Circular tmp ← dst C ← dst(7) dst(0) ← tmp(7) dst(n + 1) ← tmp(n) for n = 0 to 6  |
| RLCA | Rotate Left Circular (Accumulator) tmp ← A C ← A(7) A(0) ← tmp(7) A(n + 1) ← tmp(n) for n = 0 to 6  |

| | |
|-----------|--|
| RLD | Rotate Left Digit tmp(0:3) ← A(0:3) A(0:3) ← src(4:7) src(4:7) ← src(0:3) src(0:3) ← tmp(0:3)  |
| RR dst | Rotate Right tmp ← dst dst(7) ← C C ← dst(0) dst(n) ← tmp(n + 1) for n = 0 to 6  |
| RRA | Rotate Right (Accumulator) tmp ← dst A(7) ← C C ← A(0) A(n) ← tmp(n + 1) for n = 0 to 6  |
| RRC | Rotate Right Circular tmp ← dst C ← dst(0) dst(7) ← tmp(0) dst(n) ← tmp(n + 1) for n = 0 to 6  |
| RRCA | Rotate Right Circular (Accumulator) tmp ← A C ← A(0) A(7) ← tmp(0) A(n) ← tmp(n + 1) for n = 0 to 6  |
| RRD dst | Rotate Right Digit tmp(0:3) ← A(0:3) A(0:3) ← src(0:3) src(0:3) ← src(4:7) src(4:7) ← tmp(0:3)  |
| SET b,dst | Set Bit dst(b) ← 1 |
| SLL dst | Shift Left Arithmetic tmp ← dst C ← dst(7) dst(0) ← 0 dst(n + 1) ← tmp(n) for n = 0 to 6  |
| SRA dst | Shift Right Arithmetic tmp ← dst C ← dst(0) dst(7) ← tmp(7) dst(n) ← tmp(n + 1) for n = 0 to 6  |

| | |
|----------|---|
| SRL dst | Shift Right Logical tmp ← dst C ← dst(0) dst(7) ← 0 dst(n) ← tmp(n + 1) for n = 0 to 6  |
| TSET dst | Test and Set s ← dst(7) dst ← FF |

Program Control Group

| | |
|-------------|--|
| CALL cc,dst | CALL If cc is satisfied then: SP ← SP - 2 (SP) ← PC PC ← dst |
| CCF | Complement Carry Flag C ← NOT C |
| DJNZ dst | Decrement and Jump if Non-Zero B ← B - 1 If B ≠ 0 then PC ← dst |
| JAF dst | Jump on Auxiliary Accumulator/Flag If Auxiliary AF then: PC ← dst |
| JAR dst | Jump on Auxiliary Register File in Use If Auxiliary File then: PC ← dst |
| JP cc,dst | Jump If cc is satisfied then: PC ← dst |
| JR cc,dst | Jump Relative If cc is satisfied then: PC ← dst |
| RET cc | Return If cc is satisfied then: PC ← (SP) SP ← SP + 2 |
| RST p | Restart SP ← SP - 2 (SP) ← PC PC ← p |
| SC nn | System Call SP ← SP - 4 (SP) ← PS SP ← SP - 2 (SP) ← nn PS ← System Call Program Status |
| SCF | Set Carry Flag C ← 1 |

Input/Output Instruction Group

| | |
|----------------|--|
| ↑ IN dst,(C) | Input dst ← (C) |
| ↑ IN A,(n) | Input Accumulator A ← (n) |
| ↑ IN[W] HL,(C) | Input HL HL ← (C) |
| ↑ IND | Input and Decrement (Byte) (HL) ← (C) B ← B - 1 HL ← HL - 1 |

Z800 INSTRUCTION SET

Input/Output Instruction Group (Continued)

| Instruction | Operation |
|-----------------|---|
| † INDW | Input and Decrement (Word) (HL) ← (C) B ← B - 1 HL ← HL - 2 |
| † INDR | Input, Decrement and Repeat (Byte) Repeat until B = 0: HL ← (C) B ← B - 1 HL ← HL - 1 |
| † INDRW | Input, Decrement and Repeat (Word) Repeat until B = 0: HL ← (C) B ← B - 1 HL ← HL - 2 |
| † INI | Input and Increment (Byte) (HL) ← (C) B ← B - 1 HL ← HL + 1 |
| † INIW | Input and Increment (Word) (HL) ← (C) B ← B - 1 HL ← HL + 2 |
| † INIR | Input, Increment and Repeat (Byte) Repeat until B = 0: (HL) ← (C) HL ← HL + 1 B ← B - 1 |
| † INIRW | Input, Increment and Repeat (Word) Repeat until B = 0: (HL) ← (C) HL ← HL + 2 B ← B - 1 |
| † OUT (C),src | Output (C) ← src |
| † OUT (n),A | Output Accumulator (n) ← A |
| † OUT[W] (C),HL | Output HL (C) ← HL |
| † OUTD | Output and Decrement (Byte) B ← B - 1 (C) ← (HL) HL ← HL - 1 |
| † OUTDW | Output and Decrement (Word) B ← B - 1 (C) ← (HL) HL ← HL - 2 |

| Instruction | Operation |
|-------------|--|
| † OUTDR | Output, Decrement and Repeat (Byte) Repeat until B = 0: B ← B - 1 (C) ← (HL) HL ← HL - 1 |
| † OUTDRW | Output, Decrement and Repeat (Word) Repeat until B = 0: B ← B - 1 (C) ← (HL) HL ← HL - 2 |
| † OUTI | Output and Increment (Byte) B ← B - 1 (C) ← (HL) HL ← HL + 1 |
| † OUTIW | Output and Increment (Word) B ← B - 1 (C) ← (HL) HL ← HL + 2 |
| † OUTIR | Output, Increment and Repeat (Byte) Repeat until B = 0: B ← B - 1 (C) ← (HL) HL ← HL + 1 |
| † OUTIRW | Output, Increment and Repeat (Word) Repeat until B = 0: B ← B - 1 (C) ← (HL) HL ← HL + 2 |
| † TSTI | Test Input F ← test(C) |

CPU Control Group

| | |
|--------------|--|
| * DI Int | Disable Interrupt If EI = 1 then MSR(i) ← 0 |
| * EI Int | Enable Interrupt If EI = 1 then MSR(i) ← 1 |
| * HALT | Halt CPU Halts |
| * IM p | Interrupt Mode Select Interrupt Mode ← p |
| * LD dst,src | Load Accumulator from I or R Register A ← src |

| Instruction | Operation |
|-----------------|--|
| * LD dst,src | Load I or R Register from Accumulator dst ← A |
| * LDCTL dst,src | Load Control dst ← src |
| NOP | No Operation |
| PCACHE | Purge Cache All cache entries invalidated |
| * RETI | Return from Interrupt PC ← (SP) SP ← SP + 2 |
| * RETIL | Return from Interrupt Long PS ← (SP) SP ← SP + 4 |
| * RETN | Return from Nonmaskable Interrupt PC ← (SP) SP ← SP + 2 MSR(0-7) ← IFF(0-7) |

Extended Instruction Group¹

| | |
|----------|--|
| EPUM src | Load EPU from Memory EPU ← template EPU ← src |
| MEPU dst | Load Memory from EPU EPU ← template dst ← EPU |
| EPUF | Load Accumulator from EPU EPU ← template A ← EPU |
| EPUI | EPU Internal Operation EPU ← template |

† Programmable as privileged

* Privileged instruction

¹ Refer to the Z8070 Z8000 Floating-Point Product Specification for the floating-point extended instructions

"break" output at any time. The receiver is protected by a spike rejection circuit, and has a sophisticated mechanism to ensure proper resyncing following a framing error. Both the transmitter and the receiver can be run under interrupt control, and can optionally use DMA channels for data transfer to and from memory without CPU intervention. CTC channel 0 is used to provide the baud rate clock.

One useful function of the UART is to receive an operating program downloaded from a master processor following reset. This bootstrapping option permits the use of ROM-less Z800 slave systems, and is selected via the Bus Timing and Initialisation Register mentioned earlier.

DMAC

The Z800 DMAC provides four Direct Memory Access channels which can each support the transfer of data blocks to and from memory or I/O without the need for processor control. Transfers on each channel can be performed between any two ports, including

memory to I/O, I/O to memory, memory to memory and I/O to I/O.

Two of the four DMA channels support the so-called "fly-by" mode of operation in which the DMAC generates a single 24 bit memory address and a handshake flag (connected to a specific high-speed I/O device) for each transfer operation. The other two DMA channels support "flow-through" operation, wherein two 24 bit addresses are generated for each transfer, one for the memory mapped source, the other for the destination.

All four channels may be operated in the Single Transaction, Burst, or Continuous modes, and memory or I/O addresses can be incremented or decremented following each transfer. Once again, this is a "no compromise" peripheral, equal to the best discrete devices currently available.

CTC

The Z800's four counter timer channels can be used in a broad range of applications, including event counting, interrupt or interval

timing, and clock generation. Three of the channels have external inputs and can be used in both timer and counter modes, the fourth can only be used in the timing mode. Sufficient options are available to satisfy almost all the timer/counter requirements yet invented for microprocessor systems, and as is usual with Zilog devices, simplicity has been sacrificed in the interests of achieving the highest levels of flexibility and performance. The CTC section of the Z800 manual alone occupies four very dense pages!

In summary then, the Z800 (in the form of its Z8208 or Z8216 versions) offers a powerful if somewhat bewildering array of on-chip peripheral facilities which will undoubtedly provide much more system power, and at a lower system cost, when used in personal computer type applications.

INSTRUCTION SET

One of the questions which springs immediately to one's mind on a first encounter with the Z800 data sheet is how on earth can a microprocessor with the register set of an 8 bit chip ever be expected to perform as a 16 bit processor, when even the accumulator is only 8 bits long?

The 8/16 bit version of the Intel 8086, the 8088, and Motorola's 68008 version of the 68000, each consist of a full 16 bit CPU on the *inside* interfaced via an 8 bit bus to the outside world. The Z800 on the other hand, seems at first sight to be an 8 bit processor on the inside, interfaced to the outside world via either an 8 or a 16 bit bus. Or in other words, the complete reverse of the Intel or Motorola approach.

The reason for this strange situation is that the fickle Zilog designers wanted a much higher level of compatibility with its earlier 8 bit processor than either Intel or Motorola. To get the required 16 bit capabilities they have therefore simply extended the Z80 instruction set, adding some new 16 bit facilities, and including a number of new addressing modes. In 16 bit mode, the HL register pair is used as an accumulator, and most available operations are register orientated.

You cannot make a silk purse from a sow's ear, of course, and the resulting 8/16 bit Z800 architecture is very inflexible and restricted compared with processors using the other approach, a price which Zilog and many users will be prepared to pay for compatibility with the huge existing Z80 software base.

Added to the old Z80 instruction set are a number of new 16 bit operations including multiply and divide, compare word, sign extend, negate word, and increment or decrement word. In addition, new instructions are provided to support system calls, test and set commands for use in multiprocessing, some new load control facilities, and, most important, interface instructions for Extended Processing Units (EPUs), such as the Z8070 floating point math unit.

To suit the Z800 for its role in today's more sophisticated software environment, four new addressing modes have been added to provide capabilities not dreamed of in the pioneering Z80 days, such as the manipulation of dynamic arrays and the ability to pass parameters on the stack.

Zilog claim nine address modes in all, five of which (Register, Immediate, Register Indirect, Direct, and Short Index) are either identical to, or extensions from, the old Z80 modes. The four new modes are as follows:—

Index: This is similar to Z80 indexed mode (now called short index) except that the 16 bit base address is provided by the instruction, and the 16 bit two's complement index value is taken from the HL IX or IY registers.

Program Counter Relative: Relative addressing was possible on the Z80 only in conjunction with the single JR instruction. This new mode provides for 8 or 16 bit signed displacements and may be used with many other instructions for the creation of position independent code.

Stack Pointer Relative: This mode allows parameter passing on the stack among other things, and computes the effective address of an operand by adding a 16 bit two's complement displacement to the stack pointer value. Data n levels down on the stack can therefore be accessed without upsetting the stack pointer, a valuable feature in high-level language applications.

Base Index: This mode provides for simultaneous stepping, in two directions, through arrays stored in memory. The effective address is computed by adding a 16 bit "base" stored in one of HL, IX or IY, to an "Index" stored in another of those three registers.

The result of these new instructions and address modes is a processor with a split personality. When running old Z80 application programmes it is a boring old 8 bit device, but when the programmer starts to write new code to take advantage of its latent 16 bit power, the Z800 becomes a fast and efficient processor, suitable for today's high-level language environment.

Better still, since it is not necessary to issue any 8/16 bit "mode change" instructions, old and new code can easily be mixed within a single program.

SOFTWARE

The Z800 is a very new device and does not have much software available which takes advantage of its improved 16 bit features. At this level, therefore, you are on your own!

On the other hand, thanks to CP/M and Sir Clive, there is a vast amount of "old" Z80 software available, which is a good starting point for any new design. Z80 software used on the Z800 will run much faster than before, particularly if the higher clock rate versions of the Z800 (up to 24MHz) are used. When all the new features are employed, and code optimised for the Z800 is run, the new device can achieve a peak throughput in excess of 5 million instructions per second (5 MIPS), and will provide a level of performance far in excess of that of its 8 bit predecessor.

To really take advantage of all that power in routine applications, though, the world needs an operating system such as Unix or 16 bit CP/M, reconfigured specifically for the Z800. So far as I know, no such software is yet available.

INTERFACING

As you would expect from such a modern processor, the Z800 runs from a single 5 volt supply and has an on-chip oscillator which only requires an external crystal. NMOS technology with advanced 2 micrometre design rules is used in the manufacture of the chip, and some new packaging techniques have also been employed.

The 64 pin versions (Z8208 and Z8216) use a dual in-line package with a 0.07 inch pin spacing rather than the more traditional 0.1 inch spacing, thus allowing a 64 pin DIP to fit into the same space as one of the old 48 pin packages like those used for the Z8000.

As mentioned earlier, there are versions available which suit either the 8 bit Z80 bus or the more sophisticated 16 bit Z bus, with the only advantage of the former being that a level of hardware compatibility is achieved for retro-fitting to existing Z80 systems. For all new designs the Z bus is preferable, since it doubles the throughput and provides more sophisticated interface features.

None of the Z800 family are directly pin compatible with either the Z80 or the Z8000, although plug-in compatibility can be achieved by using a small "daughter board" if the versions with on-chip peripherals are not used.

APPLICATIONS

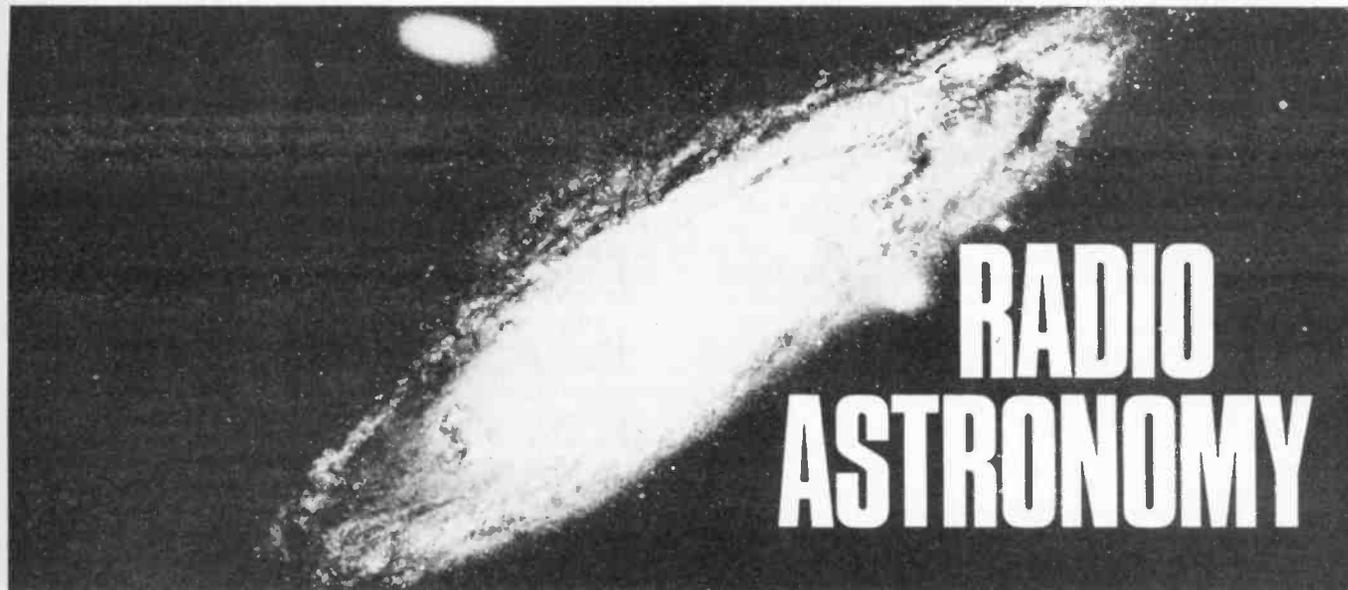
The Z800 is not a pretty processor, but like all Zilog designs it has plenty of raw power which may endear it to those obsessed with sheer performance.

System software designers will be pleased about the new instructions and addressing modes, but will probably prefer to use the much more elegant Motorola 68008 or National 16008 for new designs. Hardware designers will like the on-chip peripherals and the dynamic RAM refresh logic.

In my view, the only real excuse for using a Z800 is to take advantage of its Z80 compatibility in upgrading existing designs. Perhaps before long there will be plug-pin Z800 add-ons for machines like the TRS 80 and the Spectrum, a real bonus for owners of such systems, especially if someone also provides the necessary software support!

For most people, however, the Z800 will be just an interesting curiosity, appearing much too late to give Zilog the success they lacked with the Z8000.

all in the
AUGUST
issue!



In 1931 Karle Guthe Jansky mounted a make-shift aerial on an old Ford chassis and became the world's first radio-astronomer. This article takes a trip through the fifty-three year history of this fascinating subject and covers the basic principles right up to present day operating techniques.

**COMMODORE 64
RS232C INTERFACE**

This straightforward project will allow the Commodore 64 to drive a printer directly, or to communicate via a serial line with other machines.

**FIELD MEASUREMENTS
USING A CASSETTE RECORDER**

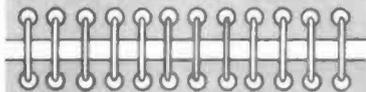
Any cassette recorder may be turned into a real-time data logger using V-to-F techniques. We describe the principles involved, and present a simple design.

PORTABLE CHESS GAME OFFER

PRACTICAL

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THE AUGUST ISSUE WILL BE ON SALE FRIDAY, JULY 6th



INDUSTRY NOTEBOOK

By Nexus



Elint

If the row over trade union recognition at GCHQ did little to enhance the reputations of the unions or government, it certainly alerted the general public to the existence and importance of electronic intelligence.

Sensational descriptions of GCHQ as being 'secret' and a 'spy centre' were done to death in the popular press. That GCHQ existed was no secret to anyone, including the Soviet Union. What is secret is the scale of activity and its efficiency in interception and code-breaking. And as a 'spy centre' it is no more than routine monitoring of the electromagnetic spectrum conducted by every major power, again including the Soviet Union, whose electronically equipped 'trawlers' operate world-wide and are in regular attendance at NATO exercises.

With all the recent fuss one could be excused for believing that monitoring and interception of signals was something entirely new and disreputable. The fact is that electronic intelligence gathering is as old as wireless and was practised in the Great War of 1914-1918 and has continued ever since. Before the days of wireless there was interception of wired telegraph traffic. Before that, interception of mail. It all still happens today.

The introduction of radar in the 1930's and its subsequent enormous growth brought in a new requirement for eavesdropping. There is no message content to intercept but by recording radar signals it is possible to categorise equipment in terms of frequency, pulse repetition rate and other characteristics and deduce application (surveillance, missile guidance or whatever) and devise appropriate jamming or spoof countermeasures.

Every new radar coming into operation is categorised by its characteristics and added to the existing library which can be stored in a computer. Comparison of a received radar signal with those stored in the library will throw up on an electronic display the type of radar and the threat it represents. In

a battle environment where a number of enemy radars as well as our own radars are operating the computer works out all the threats and lists them in priority. An extension of the system will automatically activate the appropriate defensive countermeasure. To deploy chaff, for example, fire an infra-red decoy or an anti-missile missile, or perhaps switch on a jamming signal.

Electronic warfare in constant refinement year after year is big business and by its very nature expensive. One way of keeping down costs is to adapt existing proven equipment designed for one environment to another. This approach appears to have been taken by Racal Radar Defence Systems in a recent contract to develop an automated ground-based Elint system for an unnamed central European country. Hitherto this company (formerly Decca Radar) was active only in the naval environment but there is no reason why naval Elint equipment normally deployed on the main mast and operations room of a ship should not be transferred to a mast on the ground and a transportable or fixed hardened ground shelter. The only problem would be siting the antenna array in the clear but we might guess that a central European country has plenty of nice mountains to choose from.

Another approach is by Marconi Space and Defence Systems which has just been reorganised into new systems companies rather than product divisions. MSDS advocate a step-by-step approach to inexperienced countries anxious to improve their defence capability. In this respect MSDS offer a Defence Operations Centre part of which would necessarily incorporate elements of Elint. A country in the Middle East has started with a modest £3 million of equipment to which can be added further modules.

The concept is one of 'build a little, test a little'. The user starts off with a simple system which is easily mastered. Operating and maintenance staff become familiarised with the new technology and operational procedures. The user can then move on from manual to automated operations and enhance his system progressively not only in line with increasing skills but also in line with possible changing operational requirements as military technology itself changes. Initial cost is comparatively low but the follow-on enhancements for a comprehensive Defence Operations Centre can add up to £50 million.

Vodafone

Racal Electronics Group, once the highest of high flyers in growth, together with impressive profits, has fallen from favour. Of course it would be ridiculous to expect growth to continue at 30 per cent into infinity but my private sources suggest that Racal will burst through the billion pound turnover barrier next year. Profits there will be, as in the past, but less sparkling than in the peak years.

The slowdown was not exactly unexpected. The acquisition of Decca and subsequent reorganisation was bound to have an effect. But this was a huge investment for

the future which is already beginning to produce dividends. The earlier acquisition of Milgo in the United States made a great contribution in profits until intense competition, coupled with the recession, provided a setback. The data communications interests are now seen to be recovering and Racal-Milgo has had a record year with a 240 million dollar turnover.

A lot will now depend on Vodafone. This is Racal's newly-coined word for its forthcoming portable and mobile telecommunications service, generically labelled cellular radio. Vodafone will involve vast investment before the service starts in 1985 and then returns will depend on public acceptance.

As with precedent, Vodafone will be a separate company in the Group with the name of Racal-Vodafone. Its head is Gerry Whent who is no newcomer to company start-ups. It was he who built up Racal-Datacom from nothing but an idea, to bring Racal into prominence in the exotic area of speech encryption. That was ten years ago in the unpromising circumstances of another miners' strike and the three-day week. Since then Gerry Whent has become a main board member in the Group as well as being appointed chairman and managing director of Racal-Vodafone. Racal has an 80 per cent majority in the new company with the US Millicom Inc holding 15 per cent of the shares and Hambros Advanced Technology Trust five per cent.

IC Boost

Semiconductor sales in the UK are expected to reach the magic billion pounds next year. The forecast is based on recent trends. Last year the figure was £600 million, 41 per cent up on 1982. Discretes grew 20 per cent while ICs topped 50 per cent. The Electronic Components Industry Federation reckons growth this year to be 12 per cent in discretes and 38 per cent in ICs. One factor perhaps not taken into account is that increased demand is pushing up prices as well as extending delivery dates so the magic billion may come even sooner.

Start-ups

Corby, no longer a famous steel town, is turning to sunrise industry. It has been chosen by Commodore as a main production site for Vic 20 and Commodore 64 home computers for world-wide sale. New jobs total 600 expanding to 1,000 by 1986.

The Italian semiconductor firm SGS is setting up a £1 million custom design centre at the existing HQ at Aylesbury. LTX, a US automatic test equipment maker, is starting a manufacturing and service centre for Europe in Woking eventually employing about 100 people. Japanese Sharp is investing in a £15 million plant to make VCRs at Wrexham, North Wales. Two hundred and forty will be working there next year, expanding to 630. Amdahl has settled on Dogmersfield Park, Hampshire, as their new European HQ. Investment is reported to be £10 million and will include R and D, the first time outside the US.

SO! At last, a look at the fabled QL from Sinclair Research. Unfortunately, to date, 'fabled' is the word. This article has been prepared after an afternoon near the end of April, over at Sinclair's Cambridge offices 'playing' with what I suspect is one of the very few QLs in existence. I should report, however, that there were three others in the same room, all being operated by journalists specially invited to partake of the forbidden fruit. We were not even allowed to see a manual before the event, and no glossies or any other material were presented to us on the day—just two remarkably thick and totally technical manuals, and a machine to discover for ourselves if there was a computer beneath the keyboard. As you will see: there was!

I had to copy all my information out long hand as we were not extended even limited photocopying facilities. Oh well, this is the rarefied dwelling of the Gods after all. A feeling which, I might add, even the plastic-domed and futuristic looking Sinclair premises seem to exude when first encountered. A fitting setting for what is probably the next gigantic (Quantum) Leap for the world of computer marketing—not to mention that of the bank accounts of those who have paid for their machines and are still waiting months after the 28 days promised delivery has run out.

Anyway, enough of the gripes, what about the computer?

The first detail that I would bring to your attention, if you have not looked into this machine, is that it is not, hardware-wise, a 32-BIT machine by most people's definition. The MPU data-bus is just 8-BITs wide, even though there are 16 and 32-BIT internal registers. The Motorola 68008 is the lower-end processor in a software-compatible family extending up through 8 and 16-BITs to 32-BITs. Like the 8088 and 8086 by Intel, the 68000 family allows a designer to use an 8-BIT MPU, for a simple version of a higher-BIT computer, as a sort of first stab at the larger computer-system market.

Having said this, all the software is upwards compatible, and apart from the slower speed of an 8-BIT machine, there are no other drawbacks, as one can still write the more sophisticated software of the mini-computer type of machine. Just the same, it is a little unfair to sell such a machine as a 32-BIT device with not the slightest qualification of any kind. Some people have already described this as just another extension of Sinclair's propensity for over (or forward) selling without any conscience. The point is that this machine is amazing for the price, and it should not be necessary to oversell it at all.

The hardware parameters of the QL are excellent. There are two serial ports, though the lack of a Centronics interface means that a bog-standard Epson-like printer will not fit straight onto the machine. The keyboard is the best that Sinclair has ever produced (a doubtful compliment), and the keys are easy to use, with a satisfying 'travel', though it is necessary to concentrate on

pushing the keys vertically, as too much sideways stress causes them to require more than normal force to close the switch. The feel is fine, and should be quite acceptable for the touch typists amongst you. There are 65 keys, including a CAPS LOCK (with no indicator as to its state!), but no SHIFT LOCK. A new key is the ALT key, which acts to allow fast deletion from the cursor position in the software packages. The keys autorepeat with quite a speed if you hold them down, and it takes a little getting used to, as the delay before autorepeat is very short, causing doubling of characters to occur rather easily. There appears to be 2-key rollover, but three characters would seem to be buffered by the keyboard, which is very pleasant when you become proficient at using the machine.

The screen is most comprehensive, and has three windows available for a number of uses. These windows are controlled by separate 'channels', the attributes of which are controllable by the user. When first switched on, the QL allows you to input the type of video output you are using. If an RGB monitor, the screen is 80 × 25; if a TV, with lower band-width, only 64 characters will appear horizontally. There are sockets in the back for both types of output. I was using a colour monitor, and have no way of assessing the quality on a TV. However, there is no reason to believe that this will be any different from other TV-based outputs. A vertical bar appears down the centre of the screen, dividing off two 40-column windows down to the 20th row. The lowest 5 lines are full-width command lines. The background colours and the sizes of the windows may be changed, if required.

The high-resolution graphics of the screen comes in two formats, 8 colours and 256 × 256 pixels, or 4 colours and 256 × 512—selectable by the user. The video takes up a total of 32K of the available 128K on the machine (see the memory map), and gives an excellent result, which is used to great effect by the software that comes with the machine.

MICRODRIVES

The most important single hardware feature of the QL is the pair of continuous-tape microdrives which are included. They contain of the order of 100K bytes, and have a quoted 'average access time' of 3.5 seconds. The loop runs at 30 inches per second, and takes around 7.5 seconds to make one complete revolution. If you have just passed a portion of the tape which your next command requires, the tape will have to loop around completely to retrieve that portion. This is a bit of a nuisance in the use of HELP screens, as explained later. Note that Spectrum microdrives and cartridges are not compatible with the QL. There is also no cassette port.



'HANDS ON'

QL

Dr. A.A. BERK

I have to report that during the day at Sinclair, all but one of us had trouble with the microdrives, and I actually had to have the machine I was working on changed for another, thereby proving that there are at least 5 machines in existence! I was privileged to be using a machine with serial no. 004, incidentally.

In order to assess the speed of microdrive functions, we tried backing up (copying) a complete tape. The machine I had took 16 minutes, one of the others never did succeed—showing an error after about a quarter of an hour, while a third machine completed the task in a little over five minutes. Unfortunately, therefore, I am unable to give a fair report on the efficiency of these devices. If they are reliable, they are slow, by the disk standards which will be used, no doubt, as a comparison. But they are of a different order entirely from cassettes, and are to be welcomed by any comparison—especially at the price. More microdrives can be fitted onto the machine, but one suspects that serious users will be awaiting the promised future expansion into floppies and hard disks.

MEMORY

The QLs which we were using had an extra ROM pack plugged into the back socket of the machine, and we were informed that this is how the first batch of machines will be delivered. This ROM contains the overflow of the QDOS operating system which is apparently shrinking but still does not yet fit into the machine's internal ROM space. It will eventually, we were assured.

The QL is designed as a multi-tasking and networking machine from the beginning, and if you wish to connect a number of them together, the network is up and running from the start, and will even allow Spectrums to be included in the Net. A network cable is included with the machine. Very useful for educational purposes, but not until there is a large peripheral memory source to share.

The 68008 can address up to 1 Mega byte of memory, and the map is shown in the following.

QL MEMORY MAP

| | | |
|-----------|------|---------------|
| FFFF | 256K | Expansion I/O |
| reserved | | |
| C000 | 512K | Add-on RAM |
| reserved | | |
| 4000 | 96K | Main RAM |
| RAM | | |
| 28000 | 32K | Screen |
| Video RAM | | |
| 20000 | 16K | Expansion I/O |
| reserved | | |
| 1C000 | 16K | QL I/O |
| I/O | | |
| 18000 | 32K | Expansion I/O |
| reserved | | |
| 10000 | 16K | Plug-in ROM |
| ROM | | |
| 0C000 | 48K | System ROM |
| ROM | | |
| 00000 | | |

As you can see, a very hefty 32K of the 128K available is taken up by the screen, and with the very sophisticated software available with the QL, one could run out of RAM quite quickly. There is to be a RAM add-on to the machine of half a megabyte, but we were told that this depends upon the supply of 256K dynamic RAMs—it is very difficult to know when this chip will be available, and it would be no surprise if this were at least a year away in production quantities.

Other hardware features include a buzzer on the machine which I did not manage to activate in the short time available, despite typing every conceivable variation of the characters given as an example in the manual, but it can produce a variety of sounds, including the Spectrum-like tones, which are purported to be accessible by a similar means.

There is also a battery backed-up clock, featuring a battery with a claimed life of 5 years. This provides both date and time, accessible from BASIC.

The serial channels have software selectable BAUD rates from 75 to 19,200, and are fed from a common clock, making the two channels equal in speed. CTS and DTR are used to handshake in hardware, and, as always with RS232, it is necessary to check the standards of the other device very carefully to ensure it talks the same way.

SOFTWARE

The four PSION software packages which come with the machine are an absolute *tour de force*. Time was when you bought a lump of machinery, and each software package you had—even BASIC and an operating system in some cases—would cost you a further few hundred (or more) pounds. Not so the QL. The software packages which are given away with this machine have been written with great care, and use the machine to its utmost. The general use of colour finally convinces me of the use of this previously doubtful luxury, and I would urge any serious user to buy a colour monitor to go with the machine from the start.

I would not recommend a TV as a serious output device for the machine, partly because I have rarely seen a good steady and readable TV screen, especially after hours of sitting in front of it, and partly for the simple fact that you cannot use the full 80 x 25 screen. The graphics will also be less impressive, and some of the features are frankly unusable with a TV. Perhaps the serious user who wishes to limit his outlay might start with a mono monitor, and graduate to colour later.

When you switch the machine on, the reset brings up the sign-on message, and you can autoboot into a program on a microdrive if you wish—this is an excellent and very thoughtful attribute. On switch-on, without a program booted, you can type in many operating system commands and a BASIC program if you wish. The BASIC is called SUPERBASIC (not written by PSION), and it was difficult to see that it differed so radically from normal to really be revolutionary.

The manual which I saw simply contained an alphabetic list of all the BASIC and operating system commands, with full, but sometimes incomprehensible definitions of their use. There were several cases where I could not easily work out how to use a function. The final manual will need a good contents, index and precis of operating system commands separated out from BASIC commands to ensure that the machine is easily usable. It was a nuisance to wade through the whole manual just to see how to run programs from a microdrive, only to find a technical definition of the commands which assumed I could use the machine already.

To give a flavour of the use of the machine, a typical (default) screen is shown in Fig. 1.

As you can see, there are three windows. The current BASIC program is shown in the top left section. The output from the program appears in the top right window, and commands appear at the bottom. The default background colours are White, Red and Black respectively. The screen shown also illustrates the simple editing facilities of the machine. A line is called into the command section using EDIT line number, and normal cursor movements used to edit it. When Enter is pressed, the new line replaces that in the List section.

Typical BASIC screen on the QL

```

10 REM benchmark ONE      HELLO
20 FOR I = 1 TO 500      HELLO
30 PRINT "HELLO"        HELLO
40 NEXT I                HELLO
                        HELLO
                        HELLO
                        HELLO
                        HELLO
                        HELLO
                        HELLO
                        HELLO

```

```

EDIT 20
30 PRINT "HELLO"
RUN

```

Fig. 1

The program shown is one of four (very rudimentary) benchmarks I tried. The other three are as follows:

```

10 REM Benchmark TWO
20 FOR I = 1 TO 3000
30 X = 45
40 NEXT I

10 REM Benchmark THREE
20 FOR I = 1 TO 3000
30 X = X + 1
40 NEXT I

5 X = .5

10 REM Benchmark FOUR
20 FOR I = 1 TO 3000
30 X = COS(X) ^ 3
40 NEXT I

```

In order to assess the speed of this machine, I tried three others. A BBC computer (6502), a Spectrum (Z80A) and an old Vector Graphics machine (Z80A) running MBASIC under CP/M. In some cases, X had to be set to zero in an extra line number 5, and for the Spectrum, brackets had to be placed around the COS function, instead of just around X. The BBC was in mode 3 (80 x 25 text). The times for all four machines are shown in Table 1. If you have a computer, it would be interesting to see how these compare.

In using BASIC, I found that very few abbreviations were allowed. You cannot, for instance, use '?' for PRINT. In addition, spaces seemed to be very important to the correct format of the statements—both of these would appear to be something of a step backwards. Lower case letters did not seem to upset the computer either in BASIC or in operating system commands.

GRAPHICS

Graphics are very accessible. Lines can be drawn between two points, arcs of circles can be drawn by giving two points and an angle through which the arc must rotate from one to the other—the two points could, for instance, simply define a diameter, with Pi specified as the angle. A complete circle, or an

ellipse, can be drawn, and coloured, at any coordinate point, of any size, and with any orientation of the major axis. Colouring of a rectangular block can also be performed, and the colours in general include a striking stipple effect between two contrasting colours. A coloured border can also be added to the window. The INK command allows the colour of the characters output by a program to be specified.

These types of graphics structures will be somewhat familiar to Spectrum owners. One of the major differences will be that on the Spectrum, only complete character slots could be specified as to colour, while the QL allows individual pixels to be specified—hence the rather large RAM section devoted to the screen. It is also possible to recolour all pixels of a given colour, and fill the inside of general non-re-entrant shapes. It would seem that the QL is well set-up for a Computer Aided Design application, and the turtle graphics, which effectively use the screen as a colour plotter, would be of great assistance.

The windows are also able to run separate programs simultaneously, though it will be interesting to see if the PSION software packages are not rather too large for any great use of this feature without add-on RAM.

If you wish to stop a program during execution, you hold down CONTROL and SPACE. CONTINUE then carries on with the next statement to be executed, while RETRY repeats the last statement again and then continues. The latter is very useful when errors are encountered, the line apparently in error can be retried again.

The QL BASIC allows PROCEDURES to be used, with local variables, and an interesting extended IF THEN and FOR structure, which allows, for instance, a block of statement lines to be executed upon the TRUE result of an IF statement.

String handling is excellent, with searches allowed for embedded strings within strings, etc. All the usual functions are allowed.

POKE can act on 8-BIT, 16-BIT and 32-BIT words, and CALL allows machine-code routines to be executed, as well allowing the program to set up parameters for the 68008's address and data registers. LBYTES allows a program or user to load a file from a microdrive to memory at any specified address. All the usual arithmetic and floating point functions can be used, with Real numbers being specified to 8 significant digits. Two useful commands are AUTO, for automatic line-numbering, and RENUM for renumbering a BASIC program.

PSION SOFTWARE

It is impossible after so short a time to do justice to these large and complex packages. The manuals which I was given were highly technical, and really asked for several days' reading with the machine nearby. The manuals which we were given did not have any simple precis, and the indexing was difficult to use on a first look at the packages. These were only photocopies of drafts, of course, but I was told that they were pretty near to the final versions. I hope they appear a little less formidable in their final form. The following gives some idea of the function of these excellent programs.

From the minute that one of these programs comes up, one has the feeling that the program writer has the user's needs in mind. It is possible to fiddle with the screen, and use it to some

BENCHMARKS

| Routine | QL | Spectrum | BBC | Vector |
|------------------|----------|-----------|-----------|-----------|
| Benchmark ONE: | 37 Secs. | 32 Secs. | 7 Secs. | 32 Secs. |
| Benchmark TWO: | 11 Secs. | 19 Secs. | 7 Secs. | 6 Secs. |
| Benchmark THREE: | 13 Secs. | 23 Secs. | 10 Secs. | 10 Secs. |
| Benchmark FOUR: | 34 Secs. | 493 Secs. | 146 Secs. | 127 Secs. |

Table 1

extent, immediately. They all have a number of levels, and HELP screens are copious, but will still need the manual for a full appreciation. One drawback is that if you are using the commands and the HELP screens continuously, there is an irritatingly long time to wait as the tape loops right back through to the HELP section each time.

The most useful of the packages will no doubt be QUILL. This is a word processing package, and it includes pretty well what you expect if you are used to WORDSTAR or any of the others. It seems to be nearly as good as any of the expensive machines' wordprocessors, with insert, amend, delete, global search and replace, etc. The use of colour is well thought out, and complements the display very well. It is not necessary, however, and a mono monitor would be perfectly acceptable for this program. Remember that no wordprocessor is any good without a printer, and this must be added to the cost if you buy a computer for this facility.

You can head each page with a title, to the left, right and centre, and you can insert page numbers, and control their values at will. You also have complete control over the four margins, you can left and right justify, merge files, and so on.

It is possible to share files with other members of the PSION packages which come with the QL. This is called EXPORTING and IMPORTING files, in the QL jargon.

EASEL is a package which allows 'business graphics' to be produced. It allows you to produce bar-charts, pie-charts, graphs, etc. from any numerical data available. You can also do some limited calculation on the data. EASEL really does need the colour and the graphics for its use, and though it is perfectly possible to use this sort of package in mono, the colour adds an important dimension.

ARCHIVE is a data-base program. It allows you, for instance, to keep a complete card-index in the computer with all sorts of ways of indexing, sorting, pulling subsets of the cards and so on. You are allowed to write procedures for the manipulation of the data on file, in a special data-base programming language. It is difficult to quickly assess a comparison with other data bases around, but this does seem to be very complete. Again, the use of colour and graphics is excellent.

The final program is ABACUS. As its name implies, it is a calculative program, and gives you a spreadsheet. If you are familiar with VISICALC or any other standard spreadsheet software, you will find ABACUS easy to understand. Again, the

HELP screens are excellent for making an initial stab at the program, but this really does need a careful look at the manual, with its examples, to achieve the best use. The essence of ABACUS is that columns and rows of numbers may be annotated, added up and generally worked upon as complete entities. This program is good, for instance, for the statistical analysis of lists of numbers. There are up to 256 rows by 64 columns. Also, files of such numbers can then be passed to EASEL for special types of display.

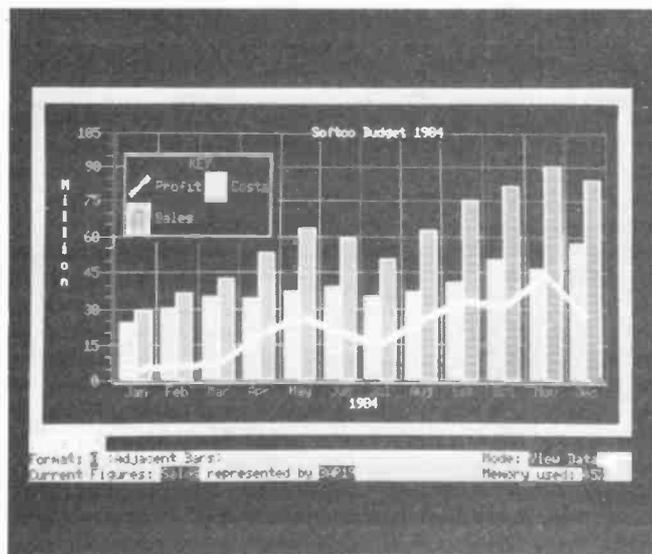
The manual examples given include a profit and loss account, a cheque-book reconciliation, and a cash-flow forecast. All of these are useful and often-used applications for this type of software.

ABACUS would be quite usable in mono, and with QUILL would give a business user an excellent initial system with a printer and mono monitor. A TV will produce a less than satisfying result. All this software is serious and business orientated, and should be used with the right equipment.

CONCLUSION

As stated at the start, this review has been written near the end of April, with the promise of machines still unfulfilled. While at Cambridge, we were informed that machines would be despatched at the end of the month (April!!!). It is difficult to assess both the supply of machines, and the state of the first machines which will be sent out. For instance, will the early machines be fully compatible with the final versions? When will final versions be available? And so on. It is also worrying that Sinclair Research has had people's money for so long. It suggests that there is a series of serious hitches in the production process, which may not be fully fixed yet. We shall have to wait and see.

However, when this machine does arrive, it is sure to be a runaway success. It is very much the latest type of technology. As to its use for business, it is clearly streets ahead of the many simpler machines being sold now (rather hopefully) as suitable for business use, purely from the point of view of its software. The microdrives have yet to be proven as a day-to-day-use technology for people who are not in the least bit interested in computing, but want a machine to perform with no fuss. It will be very interesting to view the state of affairs in a year's time, to see whether business users are praising or cursing the coming of this remarkable little machine. ★



A screen from the QL EASEL graphics package



QL Microdrive cartridge insertion

Patents Review

Copies of British Patents can be obtained from: The Patent Office, Sales, St. Mary Cray, Orpington, Kent (£1.75); and copies of Foreign Patents can be obtained from The Science Reference Library, 25 Southampton Buildings, London, WC2A 1AJ. (Prices on application.)

STEREO TV REBOUND

Sony is filing patents in Europe on a way of improving the system developed in Germany to provide stereo sound with television. This move has political, as well as technical, significance.

In Japan, stereo sound with television is transmitted using a multiplex technique, with the second sound channel modulated on a sub-carrier of the main sound carrier. Germany adopted a quite different approach, with an extra sound carrier rather than a sub-carrier.

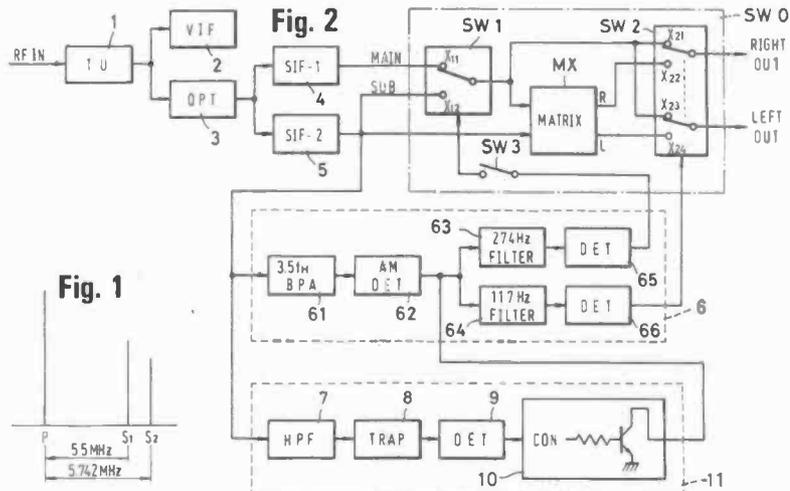
The official line was that this improves separation between sound channels. This is especially important when they are used to transmit two different languages, for instance the original and dubbed soundtrack for a feature film.

But the German move was really aimed at blocking the import of Japanese stereo TV sets into Germany. The Germans have tried to patent their two-carrier system. They planned to use the patents in the same way as they have used the PAL colour TV patents to shield European industry from Far East competition. But the plan has not worked out. This is partly because the two-carrier idea is old and the patents unlikely to be valid. Also, in Britain, the BBC has come up with a modified two-carrier system where the second carrier conveys stereo in digital code rather than analogue f.m. as is the case in Germany.

Perhaps most important, the German two-carrier system has not worked as well as expected. This is one reason why stereo sound in Germany has been slow to take off, with few transmissions and few sets sold, in chicken and egg fashion.

The Sony patent 2122458 (in Britain) provides a very useful background briefing on how the German system works and what is wrong with it. The patent then goes on to propose ways of improving it. It would be truly ironic if the Germans end up taking a licence from Japan on a way of making their own system work properly!

Fig. 1 shows the transmitted spectrum for Germany. The main sound carrier S1 is 5.5MHz above the video carrier P, the second or sub-channel sound carrier S2 is 0.242MHz further up. The receiver has to switch between three modes, mono, stereo for music and bilingual. This is necessary to preserve compatibility with existing receivers. The broadcast station has to transmit a mono sum on the main carrier for music and one language only for bilingual. So stereo decoding is different for



each mode. To switch the receiver, the second carrier is amplitude modulated with a 117Hz pilot tone for stereo, 274Hz for bilingual and 0Hz for mono.

Unfortunately interference can also switch the receiver. For instance when a video tape recorder is run in its "cue-and-review" or "picture search" mode it can generate a local modulation which fools the receiver into thinking it has received a broadcast switching tone. All kinds of anomalies can then result, for instance the receiver may try and amplify a non-existent signal and produce loud buzz in the loudspeakers.

The Sony solution is sketched in Fig. 2. The sound carriers are demodulated and fed to IF amplifiers 4-5. After frequency

demodulation, the signals are fed to switches SW1, SW2 and stereo decoding matrix MX. SW1 is controlled by a first pilot signal from detector 65 in bilingual mode. SW2 is controlled by a second pilot from detector 66 in stereo mode. SW3 gives manual channel choice in bilingual mode. Filters, 63, 64 discriminate the two types of pilot signal.

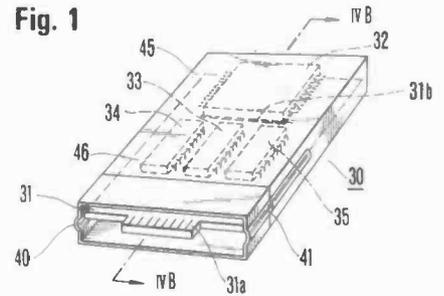
If the sub-channel sound carrier is absent or weak, the output at IF amplifier 5 has a strong noise component. Noise detector circuit 11, with high pass filter 7, trap 8, detector 9 and switching transistor 10 then ground the input of filters 63, 64. The pilot signal discriminator 6 is thus held in mono mode whenever the noise exceeds a predetermined threshold.

MEMORY CASSETTE

Hitachi is one of several Japanese companies still working on magnetic bubble memories. Recently the company promised samples in the spring and mass production by the end of the year. British patent application 2118383 from Hitachi confirms that the company has plans to use a bubble memory cassette as a replacement for conventional memory cartridges. Fig. 1 shows the general design. A cassette with bubble memory 32 sits between a pair of permanent magnetic plates to generate a bias field, with coils to generate a rotating field and read-write functions controlled by a CPU.

According to Hitachi existing memories are encapsulated in resin to keep all the parts in place but the resin may crack, especially when it gets hot. Also the resin ac-

Fig. 1



cumulates a static charge which can 'blow' the memory. So Hitachi now plans to use a cassette housing 45 made of aluminium and sealed with resin. This is strong, doesn't collect a static charge, and doesn't get hot. It plugs into a computer, like a ROM cartridge.

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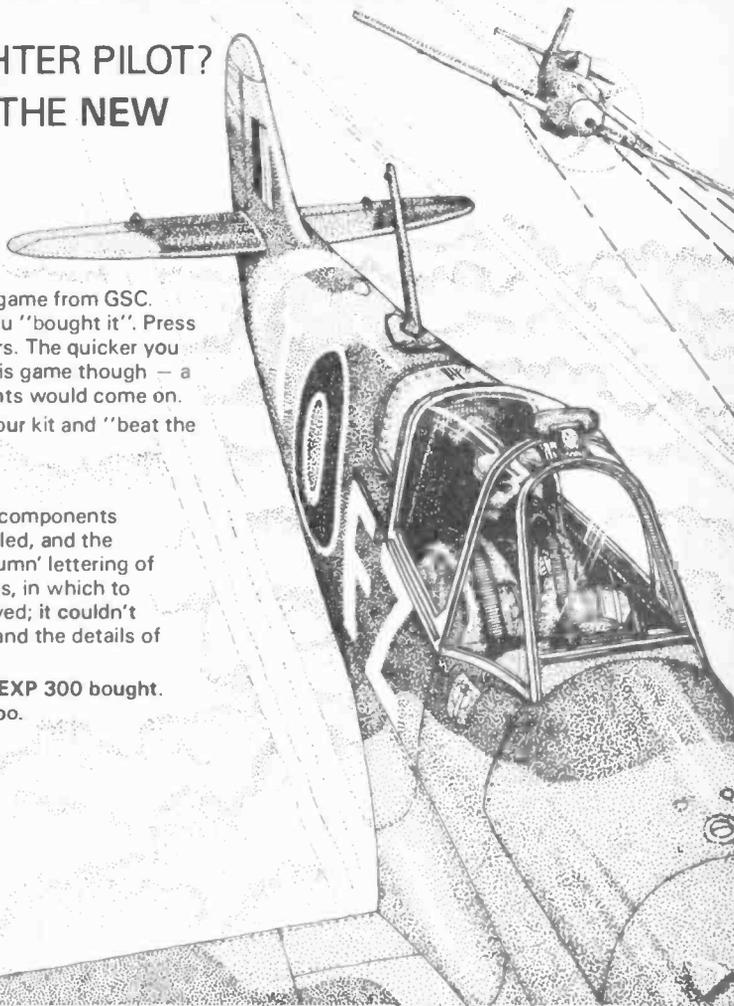
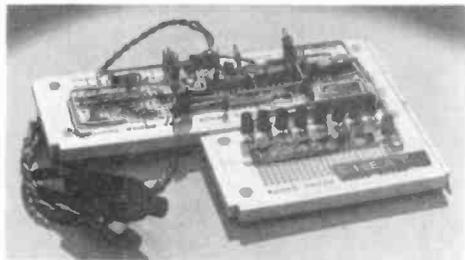
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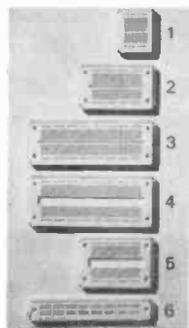
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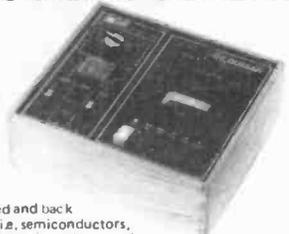
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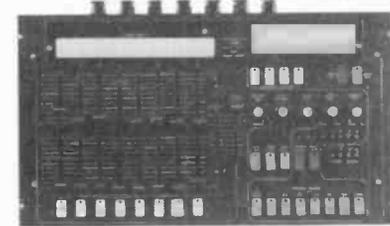
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V.T.'s views and opinions are entirely his own and not necessarily those of PE

WE'VE lots of things for which to thank the United States of America. There's chewing gum, for instance, the vacuum cleaner, pretty drum majorettes, Southern Comfort and bits of chicken in plastic boxes marketed by a military gent with an absurd beard.

But not everything that has come out of the land of the free and the home of the brave has met with the same unqualified welcome. Well, not from me at any rate. They include things like the calculated maiming of the Queen's English, peanut butter and strawberry blancmange sandwiches and, naturally, those twin opiates of the masses, Dallas and Dynasty.

Yet another import is Citizens' Band radio. And until a while ago, I couldn't make up my mind in which category to place it. But I think I have now, after having spent a day with a mob of mad-keen breakers down in rural Hampshire. One essential truth emerged from this excursion. CB radio is a total addiction. Just like golf or angling in the pouring rain—for fish which you hurl back anyway. In fact it would not be going too far to describe the cult as the cocaine of telecommunications.

CB has its origins in the US as far back as the late 1940s. It found its way across the Atlantic about seven years ago. The equipment available then was designed for a.m. reception and while this gave operators a world-is-your-oyster range, it was claimed, with some justification, that it seriously interfered with such essential services transmissions as hospital beepers and the like. It was therefore deemed illegal.

It was not until November 1981 that CB in the UK was made acceptable, respectable and within the law by licensing it at £10 a year and restricting its use to the f.m. band. Since then the Department of Trade & Industry has issued a Code of Practice which clearly lays down how breakers must behave. This Code of Practice covers such aspects as keeping conversations short to give everyone a fair share of the air time; cutting out some of the more ridiculous CB slang used in the US; being patient with newcomers; giving at all times on all channels priority to calls for help; leaving Channel 9 clear for emergencies; and, from March 5th 1984, restricting the operation of CB radio by children under 14 to parental control.

OK, said the dedicated DX-ers. All fair and reasonable. But this was really kid-stuff. What chance did it give for communication with mankind at large? However, one breaker told me that while stuck in a traffic jam at Hyde Park Corner he picked up—through a

fluke bounce off the ionosphere—a cab driver similarly incommoded in the heart of New York City. By the same phenomenon, said another breaker, he made momentary contact with a trucker late one night on a Nevada freeway.

All in all, the current situation has been accepted for the nonce by responsible fans and there are today about 255,000 licence-holders in the UK.

The DTI is unable to estimate the number of unlicensed sets in use. And it has no idea how many wallies continue to operate against the law on a.m. But it is apparent to me, after around 12 hours of concentrated listening, there are not a few.

Contrary to my earlier belief, CB radio is not a ruinously expensive hobby. A basic rig can be set up for around £50. But you don't have to stop there if you're really bitten. You

***"But unfortunately
you can't answer
for the wallies"***

can fork out anything up to £300 for ultra-sophistication.

Many DX-ers in a given area have set themselves up in groups, sharing experience and facilities. The chairman of the group I visited spelt out the approximate cost to an operator of this arrangement. Membership ranges from £1 to £5. QSL cards cost around £6 per 100. A group can rent a PO box for an annual fee of £32.50 if it's prepared to collect its cards. Delivery by the local Post Office costs double.

F.m. addicts have some 40 channels at their disposal over which they roam as freely as that bloke in the song roamed when looking for a bride. But, from my observations, the vast majority healthily respect the sacrosanct status of Channel 9. On the day I went exploring on the road with a mobile rig there were two calls for help. One from a breaker lost in the jungle of SE London. Another stranded with a puncture on the Hog's Back near Guildford in Surrey. Both were speedily succoured by fellow-breakers listening out.

However, don't think for a moment that dedicated breakers spend all their time glued

to their transmitters. In characteristic British fashion they have developed—certainly in the group whose guest I was—a strong social element. Dusty Bin (they all have these odd handles) told me how the Farnborough Valley breakers, through social functions and good works, have been able to present a CB rig to the local St John Ambulance and to raise cash for a cardiac arrest treatment machine for a neighbourhood hospital.

The tide of comradeship runs strong among those who rove the air. Just two examples: thanks to the help of other breakers, a blind operator (Magic Fingers) now has a vocal contact with a wider world. A severely spastic man, albeit with a marked speech defect, can now communicate with understanding breakers via his CB rig.

I get the impression that your genuine breaker bends over backwards to avoid any interruption of official transmissions. This is not his way of life. And, having clearly demonstrated this public-spiritedness, he looks to authority to liberate him at an early date from the nagging limit of purely f.m. operation. Greenskeeper—guess what he does for a living—said: "Every breaker worth his salt knows and respects the sensitive areas in the a.m. band and would avoid them like the plague. But, unfortunately, you can't answer for the wallies." Therein, as Shakespeare's Hamlet said, lies the rub. It's unfortunately true that in this, as in so many other areas, the activities of a small minority can blacken the name of the sensible majority.

And now for the other side of the coin. In spite of the seriousness of most of the breakers I met, I have the feeling that CB involves an awful lot of trivia. Let me offer some evidence.

While sitting outside a chip shop in North Ascot (Berks) we picked up the following conversation: First man: "OK, then I'll be round on Thursday night." First man's wife (I assume): "Oh no he won't." First man: "Oh yes I will." First man's wife (in background): "Will you kids hurry up in that bloody shower." Second man: "All right, then, I'll expect you when I see you." I couldn't, with the best will in the world, rate it as the pinnacle of intellectual exchange made possible by an advancing science.

On the other hand I listened enthralled, even though most of it went way over my head, to an in-depth technical discussion on transmission and reception data between a couple who between them seemed eminently qualified to collect a joint Ph.D. at the drop of a microphone.

So on that day-long finding, there appears to be two CB camps. On the one hand we have those who still seem to be fascinated by, if not slightly incredulous of, the possibility of communicating over long distances without any connecting wire in between. On the other hand there are those who see CB as yet another and exciting aspect of electronics in action. One which will—if and when authority permits—make possible cordial and useful contacts on a global basis. But one thing is undeniable. For both sides it is a form of fellowship. And this is summed up in a motto, dreamed up by my Hampshire mates. Their concept of CB relationships: "We are not strangers," they say, "but friends who have never met."

fibre OPTICS

D. STEWART

OPTICAL fibres have generated a great deal of interest and excitement in recent years because they are small, light-weight and cheap when compared to copper wire. The added bonus is that they have such a wide bandwidth, this will be necessary in our information society of the future. Already optical fibres are revolutionising military systems. Fibre guided torpedoes for instance are replacing wire guided torpedoes and fibre lengths of up to 5km have been used in rapid payout systems unreeling at speeds of 29 knots.

To understand optical fibre communications it is necessary to understand how a source generates suitable optical power, how this power travels down the fibre and how the detectors are used to collect the energy at the receiving end.

BACKGROUND

The fibres themselves are pure window glass with physical deformities removed and chemical impurities extracted. The problem with launching a ray of light into a fibre is that the ray is reflected out of the fibre and therefore energy is lost. The answer to this is to put a cladding on the fibre with a lower refractive index so that rays are reflected back into the fibre. Even then one has the problem of different rays travelling by different means. For instance a ray travelling parallel to the axis will arrive at the receiver faster than those that have been reflected along the way. These different modes of propagation are of course unsatisfactory and restrict the useful bandwidth.

The other limiting factor to optical fibre communication is that sources which generate the power, themselves emit energy at several different wavelengths leading to different modes of propagation and once again restricting the useful bandwidth. It is common to speak in terms of wavelength rather than frequency when referring to light-emission because then the wavelength can be more readily compared with the dimensions of the fibre down which it will travel.

There are three types of fibre (Fig. 1). In the monomode fibre the core is the smallest and supports only a single mode of propagation. To simplify matters let us assume that only a single ray of fixed wavelength light travels down the fibre, then there is no interference from rays of other wavelengths or rays arriving by reflections. This is the simple case and permits a very wide bandwidth.

At the other extreme is a multimode fibre with a 50 μ m core diameter as opposed to 2–8 μ m for the monomode fibre. As its name suggests it is capable of supporting more than one mode of propagation hence its bandwidth is limited. This in itself is not a drawback for a short route requiring a small bandwidth and in any case it is easier to launch power into a 50 μ m core than it is to launch power into the smaller 2 μ m core of a monomode fibre.

In-between these two extremes is the graded index fibre with a gently varying refractive index from core to cladding as can be seen from the refractive index profile, Fig. 1. This is achieved by choosing a pair of suitable glasses for core and cladding so that diffusion occurs between them in the manufacturing process.

In general the core refractive index is 0.5 to 2 per cent higher than that of the cladding.

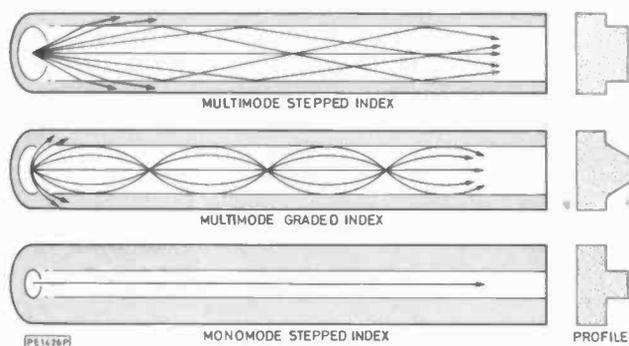


Fig. 1. The three basic types of optical fibre

MANUFACTURING OF FIBRES

There are several different methods of manufacture and some have become well established. Pyrex-like material or pure window glass (Silica) is used in fibres. To vary the refractive index, silica is doped with the oxides of germanium, aluminium, titanium or phosphorus.

Here we will look at the double crucible method and various vapour deposition methods.

Double crucible: Initially pure rods were produced from pure powders, and copper and iron were extracted from the platinum crucible hence contaminating the rods. A clever way of overcoming this is by RF induction heating. A 5MHz field couples with the molten glass at 1300°K hence the crucible is not the hottest part so a silica crucible can be used and cooled with gas or water. The melt is further protected from impurities in the crucible by a solid wall of pure glass which forms between the crucible and the melt because of the steep temperature gradient. The molten glass is homogenised by stirring the melt and bubbling with pure gas. The bubbles are then expelled by raising the temperature so that the bubbles escape from the surface.

The rods are then loaded into a double crucible for fibre pulling and again care must be taken not to contaminate the rods from the crucible.

Vapour Deposition Methods: (Corning method) using an oxygen flame a pure layer of silica is deposited on the inside surface of a tube to form the cladding. Then a layer of silica doped with titanium is deposited to form the core. The resultant preform is then collapsed and pulled into a fibre.

External deposition can also be used, where a soot containing fabrication materials is applied by a flame-hydrolysis method to a rotating mandrel, uniformly layer by layer. The rod is then collapsed.

LOSSES IN FIBRES

There are two main losses: Scatter and absorption.

Scatter is either 'Rayleigh Scatter' or due to defects in structure during manufacture. Rayleigh Scatter is caused by variation in the refractive index of glass over distances that are small compared to the wavelength of scattered light. These losses are typically 0.7 to 2dB/km at 850nm. Scatter due to structural defects are the results of bubbles of gas or unreacted materials and while these can be annealed out of bulk glass, it is more difficult to remedy fibres so great care needs to be exercised during processing.

Absorption occurs at infra-red and ultraviolet wavelengths. Absorption takes place when light beams interact with molecular vibrations within the fibres. Absorption is also due to small metal impurities like titanium, chrome, manganese, iron, cobalt, nickel and copper. These cause colours in glass, for example iron makes glass look green, chrome and titanium give rubies and sapphires their characteristic colours. The concentration and state of oxidation of these impurity ions will influence the absorption and, in turn, the manufacturing process will determine the state of these impurities. Manufacturing processes may also cause defects which show up as colour centres and these result in absorption and scattering.

JOINTING OF OPTICAL FIBRE

Joining is by means of fusion, sleeves, butt joints or lens terminations.

Fusion is carried out by butting the fibres together and using a hot wire as a heater.

Sleeves: A glass sleeve is collapsed around one fibre and the other fibre is cemented into the opposite end, Fig. 2.

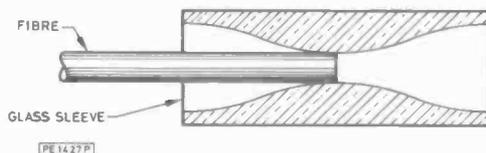


Fig. 2. Glass sleeve method

Another kind of sleeve is a 'V' groove sleeve and a special jig is used for aligning the cores using a microscope. For silica fibre, a pyrex sleeve 10mm long is used, and the protective coating of the fibre stripped back for about 15mm, then the ends are cleaved perpendicularly prior to sleeving.

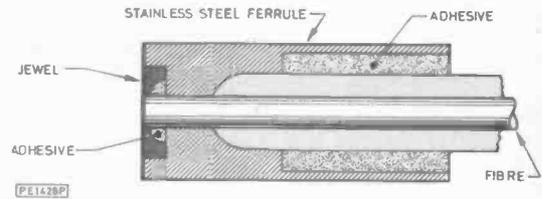


Fig. 3. Butt method

Butt joints can be made in a jewelled ferrule because hole sizes are more accurate in jewels than in metal. A stock of inexpensive watch jewels can be held with different hole sizes to match different fibre diameters. The fibre is then polished back flush with the end of the ferrule, Fig. 3.

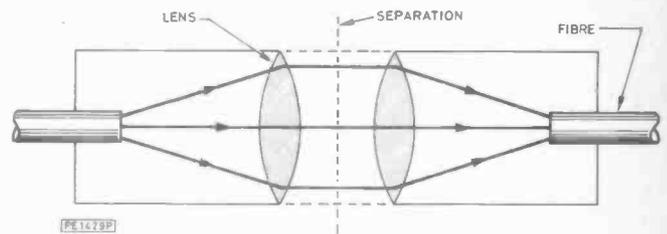
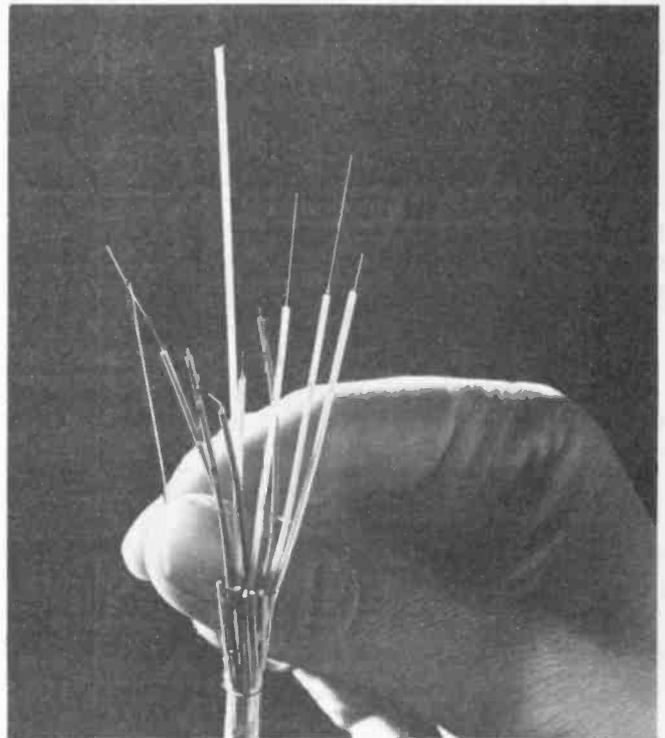


Fig. 4. Lens method

Lens termination, Fig. 4. The fibre is mounted at the focal point of the lens and accurately set in the factory. This is prepared in two halves, then accurate settings are not required in the field.



SOURCES

Sources used to launch power into fibres are either lasers or l.e.d.s. These devices are chosen because no other light source can be directly modulated at such high bit rates to give high output power with low drive current. For instance, a digital stream of 140 Mbit/s can carry 1920 channels of telephony. L.e.d.s. These are the same as the visual display l.e.d.s except that they operate in the infra-red range and the intensity of emission is many times greater.

The basic theory of emission is this: when the p-n junction in a semiconductor is forward biased, photon emission takes place due to recombination of hole electron pairs. The wavelength of emission will depend on the energy gap between the valence and conduction band in the semiconductor. Fortunately this emission is in the low attenuation region of the fibre hence it is transmitted with minimum loss.

For medium distances of about 10km and low bit rates (8Mbit/s) an l.e.d. and graded index fibre are used because the drive and control circuits are simpler. A light emitting diode can be made more efficient if a well is etched into the top layer and these high radiance diodes are called Burrus diodes.

Instead of emitting from an etched well in the top, edge emission can be caused and these edge light emitting diodes, e.l.e.d.s, are even more efficient. Furthermore they have a stripe etched on the top similar to lasers except that the stripe does not extend the full length of the chip. The semiconductor layers are the same as a laser so they are economical to manufacture.

Laser stands for Light Amplification by Stimulated Emission of Radiation and that is exactly what happens. A semiconductor junction is heavily forward biased creating a dense population of electrons in the conduction band and when a spontaneously emitted photon of energy (reflected by a mirror) meets an electron about to emit another photon, stimulated emission takes place. The two photons then stimulate the emission of further photons. The laser chip has vertical ends with mirrors deposited on them. Laser chips are in 'dice' form approximately 400µm square and bonded to copper heat sinks with indium solder which is soft and minimises strain. Lasers operate at 5mW output. Although lasers are much brighter than l.e.d.s, they are not linear, hence l.e.d.s are more useful if an analogue message is required to be transmitted.

The e.l.e.d. we discussed previously resembles the laser in that



By passing the chemical ingredients through a vacuum in the hollow centre of a super-heated tube of coarse glass, thin layers of the purest optical fibre glass are gradually built up

current is confined by the stripe to an insulated oxide layer but since the stripe does not extend the full length of the chip, its rear forms an unpumped absorption region. Light is generated and amplified in the stripe and since light is absorbed in the unpumped region no optical feedback takes place, hence no



On-site automatic jointing machine

lasing. Output power depends on stripe length, width and drive current, e.g. maximum output at 50mA requires a 70µm-length.

To summarise then and compare lasers with l.e.d.s: Both work by emitting photons, as electrons fall from the conduction band to the valence band but whereas l.e.d.s work by spontaneous emission, lasers work by stimulated emission. So lasers are brighter and the response is faster. Also the line width is narrower, increasing bandwidth. This is so because once lasing has started, photons stimulate emission of the same wavelength and this gain mechanism narrows the emitted spectrum to 1nm compared to 20nm for l.e.d.s. which are suitable for linear systems and at room temperature will last 10³hr and lasers 10⁵hr. Broad contact lasers need cooling and are operated in the pulsed mode only, whereas stripe lasers are operated continuous wave (CW). Optical feedback can be used with CW lasers but not with broad contact lasers.

Having obtained a suitable light source and manufactured a suitable fibre one other matter remains and that is to connect the two together. They can, of course, be simply butted together and a 50 micron fibre will fit admirably into the etched well of a Burrus diode or an e.l.e.d. can be butted to a suitable fibre. However there are losses from escaped radiation and if a lens is used between source and fibre the efficiency is improved.

DETECTORS

The most commonly used detectors are of two kinds: avalanche photo-diodes (APDs) or positive intrinsic negative (PIN).

Repeater spacing depends on the distortion and attenuation of the signal as it passes down the fibre. If there is no distortion then a sensitive detector can reduce the number of repeaters, hence the cost of a system.

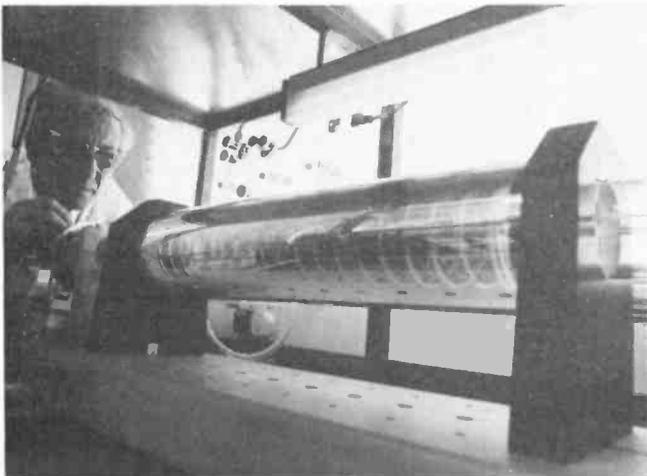
Basic detection theory. This is exactly the opposite of the action of sources where electrons are releasing light. Here packets of light are releasing electrons which flow in an external circuit, and light to electrical conversion has taken place.

Light travels in discrete packets of energy called photons. When a photon is absorbed, it excites an electron which moves from the valence band to the conduction band. This happens when the energy of the photon equals the band gap energy of the semiconductor.

When a photon excites an electron, a hole is left behind, so photons generate hole-electron pairs and in n-type material, electrons are the majority carriers, holes the minority carriers and vice versa for p-type material. In a reverse biased junction the majority carriers are prevented from flowing across the junction but the minority carriers are not prevented. Hence the reverse field clears the mobile carriers to their majority sides creating a depletion region at the junction.

PIN diodes: Absorption takes place in the "I" region which is low doped 10^{15} per cubic centimetre n type. The reverse bias extends the depletion region all the way to the heavily doped substrate and this is the reach through effect for fast collection of electrons. Although PIN diodes need a FET amplifier to amplify the weak signal, they have advantages like fast response even at 300Mbit/s. For operation at high bit rates diodes need fast response, high efficiency, low capacitance, and low dark current. The capacitance would reduce the transit time, and dark currents prevent the detection of weak signals. Capacitance can be decreased by increasing the I-region, but increasing the I-region too much increases leakage currents. In practice I-regions of $100\mu\text{m}$ and silicon devices of $200\mu\text{m}$ to $500\mu\text{m}$ length are manufactured.

Avalanche Photodiodes (APDs). In the 1970s silicon detectors were used at $0.85\mu\text{m}$ but in the present day the search is on for detectors to operate at $1.3\mu\text{m}$ and $1.55\mu\text{m}$. A detection limit is reached when the signal current at the receiver output equals the sum of the noise currents comprising quantum, dark current, excess shot and thermal. More important than the thermal noise is the signal to noise ratio for guaranteeing the required bit error rate. For example, to be assured of an error rate of 1 in 10^9 , at least 21 photons must be received for distinguishing a digital one. Here we might mention detector efficiency where for every 100 photons absorbed, between 30 and 90 electrons will flow in the external circuit and the quantum efficiency is said to be between 30 and 90 per cent. For a 10^{-9} error, an APD sensitivity of -49dBm would be required and -43dBm for a PIN-FET combination.



Laser-chips being made using liquid phase epitaxy; five or six layers of semiconductor compound are built up on the laser fragment using intense heat

The avalanche process needs to be initiated mainly by electrons to reduce excess noise and that can be done by making the junction as close as possible to the surface by using a shallow heavily doped n-type region (n^+). Also the edge of the junction will have a lower breakdown voltage due to the high field and requires a guard ring for protection. The guard ring has suitable doping and radius of curvature. APDs require reverse biases of 100V and dc-dc converters are used at repeaters.

Receivers. A detector converts photons to electrons and a receiver is a detector plus circuits to convert optical signals to the lower frequencies. The transimpedance input circuit of Fig. 5 is suitable for APDs and the high impedance circuit of Fig. 6 is used with the PIN-FET combination.

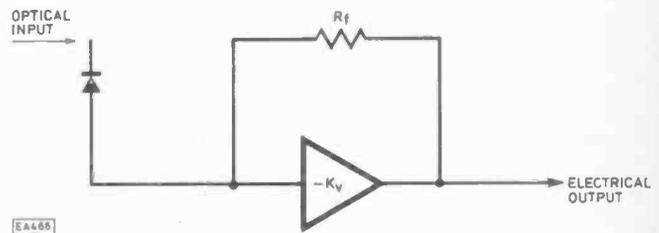


Fig. 5. Transimpedance input circuit

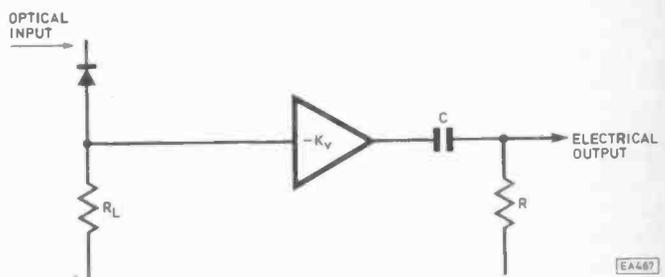


Fig. 6. High impedance input circuit

COMMUNICATIONS SYSTEMS

An interesting point to note about fibres is that the electric 3dB point in electrical circuits corresponds to the 1.5dB point in fibre and this is because the loss is a function of current rather than power.

Since lasers are non-linear just above and below threshold they are more suitable for digital systems than for analogue systems and a simple diagram of a communications system is shown in Fig. 7.

Work is going on to develop integrated optics similar to integrated circuits which replaced wire circuits. Integrated optic circuits are deposited in the same way as electric tracks by photolithographic processes, and in the future it is hoped to integrate sources, detectors, delay lines, and repeaters into a fibre optic cable very much the same as integrated signal processing is carried out in modern radios and televisions. A big advantage of switching optical signals without converting them to electrical signals would be in an environment of high electrical noise.

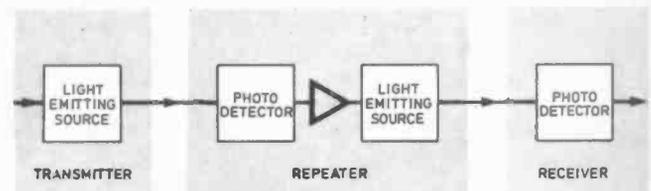


Fig. 7. Simple communications system

| Transmission rate Mbit/s | Repeater Spacing in km | |
|-----------------------------|---------------------------|---------------------------|
| | Coaxial dB/km 9.5mm | Optical fibre 1.3mm |
| 34 | 9.3 | 50 |
| 140 | 4.6 | 39 |
| 565 | 2.0 | 26 |
| 1200 | 1.4 | 20 |

Table 1. Transmission rates/repeater spacing (monomode)

| Wavelength μm | Attenuation dB/km | Bandwidth GHz/km |
|-----------------------------|----------------------|---------------------|
| 0.85 | 2.5 | 4 |
| 1.3 | 1.0 | 6 |
| 1.55 | 0.5 | 4 |

Table 2. Attenuation and bandwidth (graded index)

For graded index fibre the attenuation is 3dB/km at 0.85 μm and repeaters are spaced at 10km for a system operating at 140Mbit/s. But at 1.3 μm the attenuation is even less and there is a great deal of interest. Table 1 shows various transmission rates and the repeater spacing of 9.5mm coaxial cable compared with monomode fibre operating at 1.3 μm . It is easy to see the big saving in repeater costs.

Having compared coaxial cable with fibre let us compare the operation at different wavelengths for the same fibre. Table 2 shows the attenuation and bandwidth of graded index fibre operating at 0.85 μm , 1.3 μm and 1.55 μm . For these attenuation figures the repeater spacing for 0.85 μm , 1.3 μm and 1.55 μm will be 12km, 30km and 60km respectively showing the distinct advantage of operating at the longer wavelengths.

For monomode operation the repeater can be improved on the above figures but there is the difficulty of making good connectors and splices for efficient coupling since the cores measure only 2 μm to 8 μm .

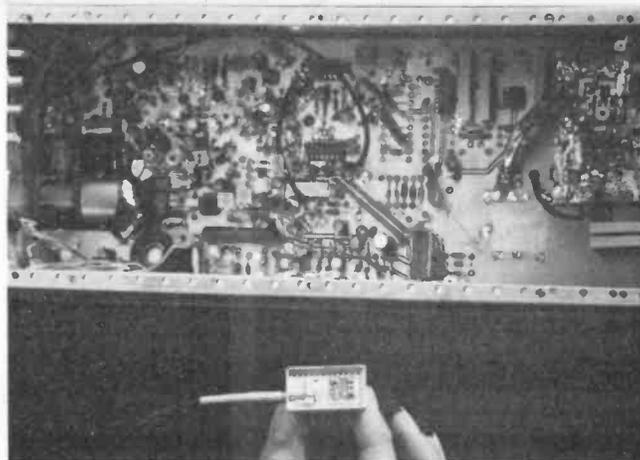
Submarine Cables. Naturally this area will be affected in the very near future providing once again cheaper links than satellite paths. For submarine cables operating at 1.55 μm , repeater spacing at 100km will be practical but to transmit a 300Mbit/s signal with the laser width of 7nm, fibre dispersion needs to be within 20nm of the laser wavelength. If this cannot be achieved then 1.3 μm carrying 300Mbit/s will need a laser width of 0.5nm, i.e. truly monomode.

The top frequency of a commercial route is 45MHz and a recent trial used 140MHz. Say we wanted 20,000 circuits at 3kHz, then the top frequency would be 180MHz requiring transistors with a cut-off frequency of 8GHz. The largest lightweight cable to date has a 1.7 inch diameter. With 180MHz bandwidth a 2.5inch cable would reduce both repeaters and the system voltage. Operating at 560Mbit/s, a 2 inch cable would need repeaters every 6km.

Broadband networks. Coaxial cables are heavy, bulky and affected by humidity and also need earthing to protect personnel from lightning if used by television crews, so here is an application begging to be exploited by optical cable. If a l.e.d. is used instead of a laser, the output can be directly modulated though the output may be 18dB lower than a laser. The repeater spacing would be 3km and for long distances an APD would be used instead of a PIN detector.

Broadband networks will offer three types of service:

1. CATV (Community Antenna Television) and high quality sound programs with no delay and zero blocking, that is, quickly and readily available.
2. Access to information with possible delay and blocking.



Prototype to present day transmitter size. This unit is capable of injecting up to 2000 calls simultaneously into a fibre

3. Point to point services like videophone with almost certain delay and blocking.

The price of fibre will fall in the next 5 years but coaxial cables costs will rise by about 5% per year. On 12km routes 34Mbit/s will be both economic and practical and the country will probably be wired up for cable TV, information services etc. in the same way as the telephone network.

Field Trial. A 40Mbit/s field trial took place from 1977-1980 between Hitchin and Stevenage. It was a 9km route with repeater spacings at 3km. A central steel member was used for strength and around this were four copper wires and three fibres. Altogether the cable was only 7mm in diameter.

The latest news is that repeaterless operation has been achieved over 100km at 140Mbit/s using a laser and monomode fibre. 140Mbit/s is capable of carrying 1920 telephone channels or one 625 line colour TV broadcast.

FURTHER APPLICATIONS

In closing it would be worthwhile to consider applications other than communications. Fibre can be used to look at and illuminate small, inaccessible areas both in industry and medicine. It can be used as a flowmeter by dangling the end in fluid and the fibre end will vibrate in sympathy with the flow, or as a flow detector to pick up variations in reflected light, and for analysing the fluorescence of materials by using the same fibre bundle as both an input and output medium.

Fibres have also been used in hydrophones for listening in water where one fibre is used as a reference and another is looped in the water to pick up stresses. The phase difference is analysed electrically. Fibres are a real boon in measuring high currents using non-conducting materials. A short length is coiled around the busbars and Faraday's principle used: the plane of polarisation of a light beam is rotated by a magnetic field depending on the field strength and length of path in the field.

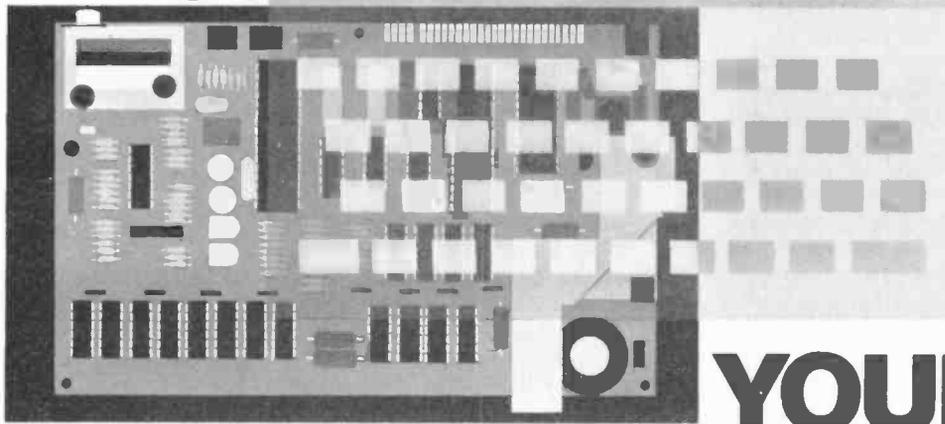
Other exciting possibilities remain to be exploited. For instance the same fibre can be used for transmit and receive directions by using two different wavelengths and employing a dielectric or prism to separate them at each end. Unlike computers, the optical fibre is not a tyrannical master waiting to exploit us but a very cheap and willing servant to this century's information society. In fact it's going to do everything we always dreamed of but were afraid to pay for.

ACKNOWLEDGMENTS

The author would like to record his gratitude to British Telecom for the supply of photographs used in this article.

JULY FEATURES...

Anatomy of



OWEN BISHOP IS THE ANATOMIST IN THIS MAJOR NEW SERIES. THERE ARE NOW TWO DOZEN OR MORE DIFFERENT PERSONAL COMPUTERS ON THE MARKET, OFFERING A SOMETIMES BEWILDERING VARIETY OF FEATURES. THE *ANATOMY OF YOUR MICRO* SHOWS WHAT THEY HAVE IN COMMON: CPU, ROM, RAM, I/O PORTS, AND EACH OF THESE SUB-SYSTEMS IS EXAMINED IN DETAIL.

IN THE FIRST PART, OWEN CONSIDERS THE LANGUAGE THAT THE MICRO ACTUALLY UNDERSTANDS: TWO DIFFERENT VOLTAGE LEVELS. HE THEN LOOKS INTO THE HEART OF THE COMPUTER—THE MICROPROCESSOR.

YOUR Micro

Car Lights Reminder

This unit warns the driver when daylight falls below a certain level and also if the ignition is switched off before the lights at the end of a journey.

ULTRASONIC Alarm System

Sets up an ultrasonic field reaching as far as ten feet from the transducer. Any movement within this field will trigger the alarm.

Electronic Lock

An electronic combination lock with a difference. Can be used to prevent unauthorised use of any mains operated appliance such as computers, videos and home-base CBs.

EVERYDAY ELECTRONICS and computer PROJECTS

JULY 1984 ISSUE ON SALE FRIDAY, JUNE 15

Alarm

G.E. LUMLEY

PART ONE

SYSTEM

THE Two Timer circuit is a flexible burglar deterrent which consists of three circuit boards and a warning unit.

The unit can be used as a stand-alone system or if an existing system needs to be updated with time controlled warning, then only the timing board need be used along with the p.s.u.

The three circuits are: Alarm Comparator, to sense intruders. Two Timer, to produce timing sequences for external warning device. P.S.U. to supply the above. It also provides a tell-tale monitor to determine whether or not the system has been activated during the owner's absence. The two periods i.e. the delay and the duration of operation are adjustable and independent of each other. An automatic reset is incorporated within the design so that, should the alarm be accidentally triggered, the process is not inexorable but can be aborted simply by removing the source of alarm. This applies whether the Two Timer is in the delay but triggered phase or whether it has advanced into the siren operating phase. This facility is overridden when the Comparator is operated in the 'Lock-On' mode inasmuch as removing the source of the alarm is ignored by the Comparator until 'Lock-On' is abandoned.

To keep the component cost low, standard NE556 timers are specified and give adequate delay times and reasonable current requirements. If reduced current demand and increased times are required the CMOS 7556 can be used.

CIRCUIT OPERATION

The circuit diagram of the Two Timer is shown in Fig. 1.1; an NE556 (dual NE555) is used to obtain two, independent, adjustable periods of delay. Both periods are initiated simultaneously by clamping TR1 base to emitter. This initiation signal is derived from the Comparator or if the Two Timer is used in conjunction with an existing system, by utilising its output relay to short circuit the Two Timer input terminals together. Any power supply present at the output of an existing system must, of course, be removed. A simple closed circuit is all that is required to activate the circuits.

Normally the trigger and reset pins of the two timing chips are held at -9 volts by virtue of TR1 being held in conduction and its collector 'bottomed'. (Timer pins 6 & 8 and 4 & 10). The timers are thus held quiescent and the two outputs (pins 5 & 9) are high. The associated l.e.d.s are therefore extinguished.

Should TR1 base be clamped by the introduction of an alarm signal from the Comparator, or other source, the timing cycles would commence. Timer number 1 consists of VR1, R3 and C1 and Timer 2 of VR2, R8 and C5.

Reference to Fig. 1.2 gives a pictorial indication of the sequence of events.

Period 1 provides the delay before the output relay closes and operates the external alarm. (Timer No. 1.)

Period 2 determines how long the siren operates i.e. the duration of the warning alarm. (Timer No. 2.)

With the constants given, the limits of the timers are approximately:

Period 1: 15 secs to 45 seconds

Period 2: 105 secs to 600 seconds

These times can be altered by changing the circuit constants but if the capacitor in the second timer is increased, it would be best to use tantalums in parallel. The very large tolerances of electrolytics may well give times differing from those quoted. Similarly, the leakage factors of electrolytic capacitors are very widely spaced, therefore, only good quality, low leakage components should be used. If the relay fails to open it is likely that the leakage of the capacitor C5 is too great.

The two outputs of the timer i.c. (pins 5 & 9) are coupled to the l.e.d. monitors via a push switch. The switch is optional and is intended to reduce current flow. These tell-tale l.e.d.s inform the user that the system has been triggered. The timer outputs are also connected to the two inputs of a 741 operational amplifier which is configured as a Difference Amplifier.

A difference amplifier follows a law of:-

$$e_{\text{Out}} = \left(\frac{R1 + R2}{R3 + R4} \right) \left[\left(\frac{R4}{R1} e2 \right) - \left(\frac{R2}{R1} e1 \right) \right]$$

when R1, R3, R2 and R4 are equal

the output, $e_{\text{Out}} = (e2 - e1) \frac{R2}{R1}$ in other words, the output is directly proportional to the differential of the two inputs.

When the inputs are equal, the output is low at pin 6 and when there is a difference between the two inputs, no matter in which direction, the output will be high.

When the timers are triggered simultaneously, as they are when TR1 base is clamped, the two timing capacitors commence charging. At this point in time both outputs are high, the 741 inputs are high (there is no difference) therefore there will be a low at pin 6 and TR2 will be cut off. When the first timer has tripped, one input to the 741 will go low (there will be a difference) and the output pin 6 will therefore go high. This state will hold until the second timing period

SECURITY PROJECT

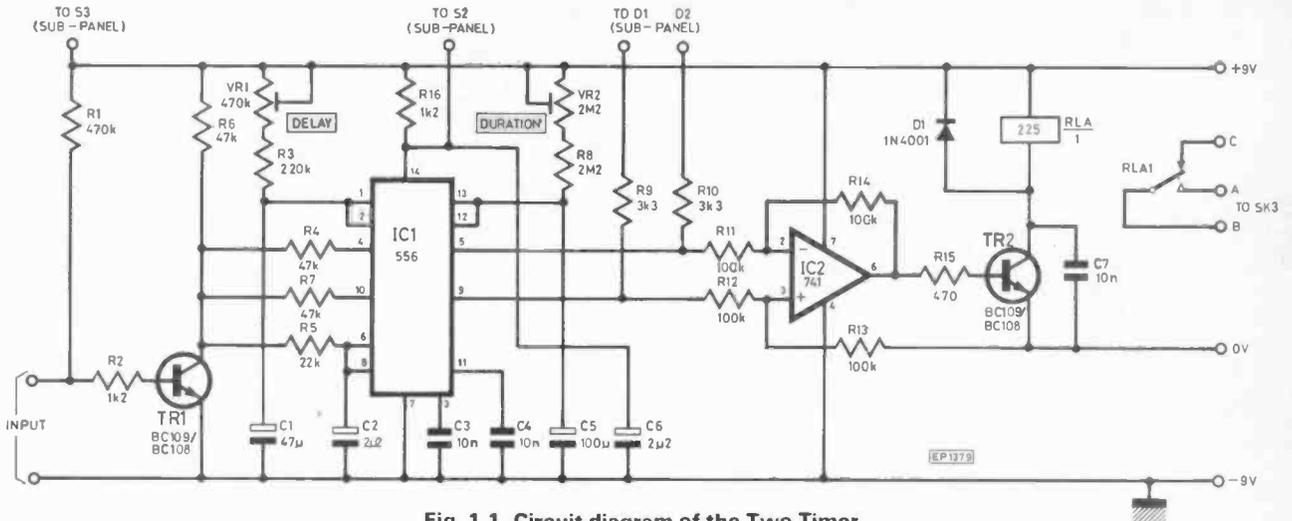


Fig. 1.1. Circuit diagram of the Two Timer

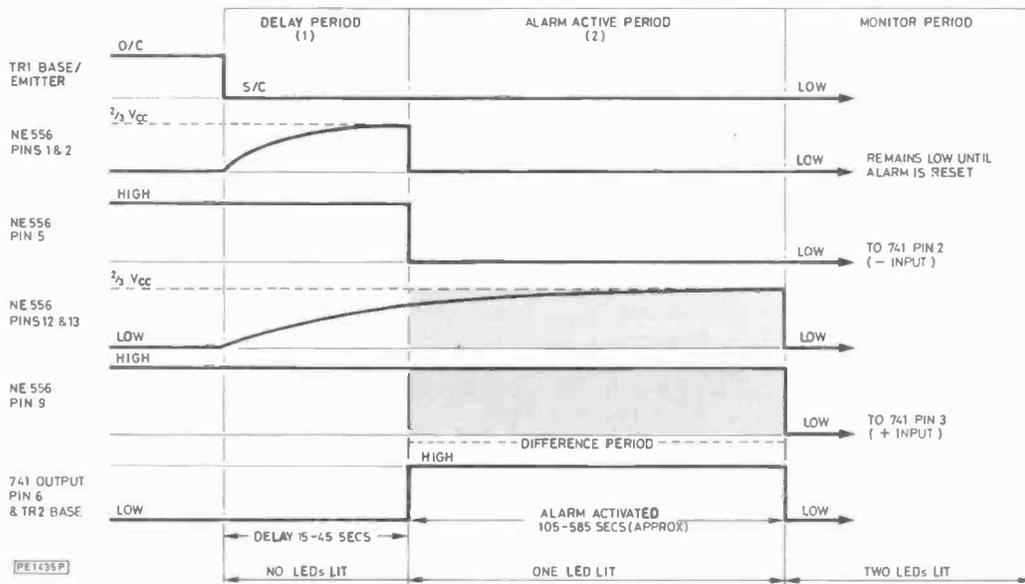


Fig. 1.2. Timing diagram of alarm system

COMPONENTS . . .

Resistors

| | |
|---|--------------|
| R1 | 470k |
| R2,R16 | 1k2 (2 off) |
| R3 | 220k |
| R4,R6,R7 | 47k (3 off) |
| R5 | 22k |
| R8 | 2M2 |
| R9,R10 | 3k3 (2 off) |
| R11,R12,R13,R14 | 100k (4 off) |
| R15 | 470 |
| All resistors $\frac{1}{4}$ W 5% carbon | |

Potentiometers

| | |
|-----------------|------|
| VR1 hor. preset | 470k |
| VR2 hor. preset | 2M2 |

Capacitors

| | |
|----------|-------------------|
| C1 | 47 μ |
| C2,C6 | 2 μ 2 (2 off) |
| C3,C4,C7 | 10n (3 off) |
| C5 | 100 μ |

Semiconductors

| | |
|---------|------------------------|
| D1 | 1N4001 |
| TR1,TR2 | BC108 or BC109 (2 off) |
| IC1 | 556 |
| IC2 | 741 |

Miscellaneous

14 pin d.i.l. low profile socket
 8 pin d.i.l. low profile socket
 Relay s.p.c.o. (225 ohm coil) (KUJTB Ambit)
 Veropins (as required)
 p.c.b.
 Siren 12V

has completed its cycle, whereupon the other 741 input will go low (once again there will be no difference). The output in pin 6 will now revert to its low state. The data at the two outputs of the 556 however will remain, therefore the l.e.d.s will both light if the button is pressed. The timer can be interrogated at any time, one l.e.d. lit indicating one timer has cycled, two l.e.d.s, both timers and no l.e.d.s indicates that nothing has yet happened.

The output of the difference amplifier is used to control the npn transistor TR2 in whose collector circuit is the output relay. This relay has contacts capable of handling 1A at 24V to switch on the warning device via SK3.

CONSTRUCTION

The p.c.b. design for the Two Timer is shown in Fig. 1.3 with the component layout shown in Fig. 1.4.

C5 must be a good quality, low leakage component or built up from tantalums (say $2 \times 47\mu$ or $4 \times 25\mu$). The specified electrolytic capacitors were $2 \times 47\mu$ low leakage types.

The inputs are taken to Veropins, as are the l.e.d. leads. The other side of the l.e.d.s, that is pin 14 IC1 is picked up separately via a push switch.

Although a plus and minus 9V power supply is used, the dropper resistor in the feed to the NE556 reduces this to a lower value, to stay within the specification of that i.c. The full 9V is necessary at the transistor TR2. The relay output is taken to a DIN socket (SK3).

Once again, just the usual precautions, check for solder runs, polarity of capacitors and the correct insertion of the i.c.s.

INTRUDER SENSING COMPARATOR

The Intruder Sensing Comparator detects changes in the external network of sensors whether they are magnetically actuated reed switches, pressure mats, micro switches or active devices such as ultrasonic doppler movement detectors.

The arrangement is such that any attempt to short circuit or cut the external network wiring will result in triggering the system, indeed a pair of wet fingers will suffice to trigger a properly adjusted system.

High gain, high input impedance, JFET input operational amplifiers are used to detect any change in the external network resistance and, having sensed such a change, subsequent circuitry is brought into operation to introduce warning signals in a strict sequence; firstly an internal warning, then by virtue of a second circuit board (the Two Timer) an interval, then an external warning for a defined period and ultimately, a tell-tale memory indicator to warn if the system has been triggered in one's absence.

A compensation system permits the user to open a normally protected door or window yet still maintain protection over the remainder of the house. There are eight compensators, thus up to eight of the sensors can be compensated for. The maximum number of sensors is ten although it is possible to increase this number if it is found necessary.

There are two modes of operation available at the user's discretion, they are:-

- (1) Auto-Reset or
- (2) Lock-on

An exit/entry delay is included and is adjustable from about 8 seconds to 80 seconds, which should cover most re-

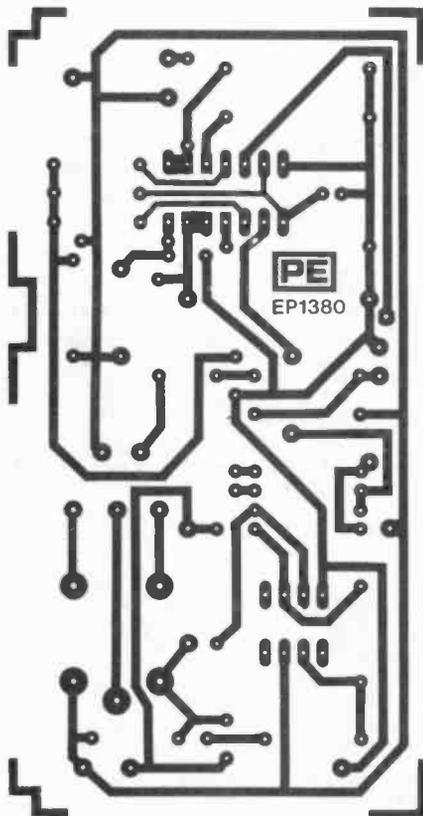


Fig. 1.3. P.c.b. design for Two Timer

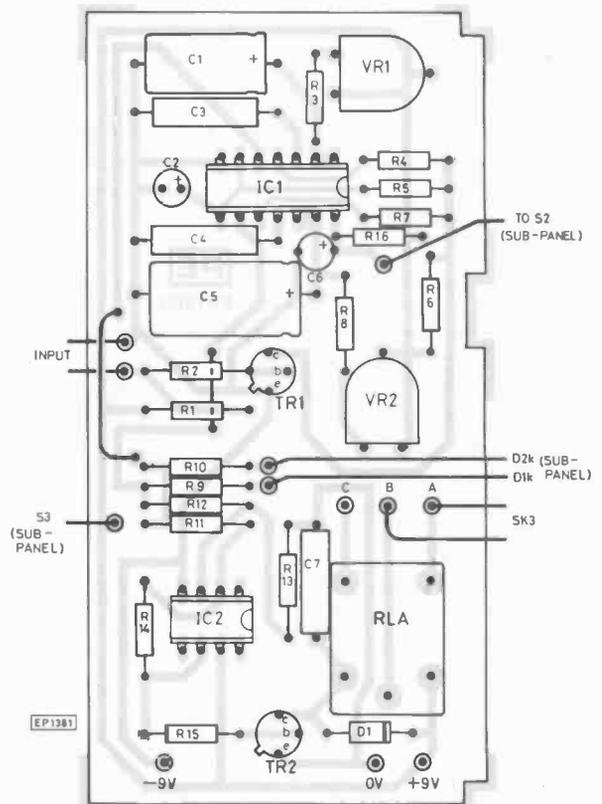


Fig. 1.4. Component layout

quirements. In order to permit the user to make exit, yet adopt 'Lock-On' mode whilst away from the premises, the 'Lock-On' is ineffective until after the expiry of the delay period. It is essential therefore, to leave the premises and close the door before the delay period has expired. Failure to observe this rule will mean the user is caught whilst making exit and, due to the delay period, if the mistake is not remedied, the sequence of events will cause the external alarm to sound, probably after the user has driven away. Upon return, when 'Lock-On' has been selected before leaving, failure to remedy the result of entering the premises under 'Lock-On' cover, will soon be made known by the sounding of the internal siren, thus the omission will be very obvious and remedial action taken before the external siren sounds to the annoyance of the neighbours.

The system includes annunciators which give indication of the progress of an input signal and the readiness of the system in normal circumstances.

- Alert & Ready is indicated by a green l.e.d.
- Intruder or Tamperer is indicated by a yellow l.e.d.
- Internal Siren on is indicated by a red l.e.d.

The output of the Comparator and the Two Timer is a relay in each case and therefore the choice of warning is at the user's discretion.

THE EXTERNAL NETWORK

The external wiring can be carried out in thin twin PVC insulated cable.

Each window or door or other area requiring protection is fitted with a suitable sensor. The essential requirement is that the sensor shall have normally closed contacts and these contacts shall complete a circuit which includes a resistor of specific value. These resistors are all of the same value which is determined by various relevant factors. Intrusion will open the contacts and exclude the particular resistor from the network. The sensors are wired in parallel and ten is the normal number although it is possible to increase on this maximum. Fig. 1.5 shows the requirements for a practical network. An increase on ten sensors is obtained by the 'extra reed switch in series' method as shown

in Fig. 1.4; then it must be remembered that anti-tamper facilities are forfeited on that switch and its associated wiring. Obviously, remedial action can be applied by concealing this section of wiring or running an extra loop.

The total of ten sensors is a function of the relationship between the ratio of the undisturbed network resistance, to that resistance when one sensor has been activated and, the degree of sensitivity available from the Comparator without running the gauntlet of false triggering due to electrical noise. Fig. 1.6. compares the effects of a sensor being activated, with the changes incurred by altering the value of VR1. It will be seen that with ten sensors as a maximum, open circuiting one of them produces a voltage change more than adequate to over-ride the voltage appearing across VR1 even when set to 100k, the most insensitive condition.

A lot depends on the local electrical atmosphere, a simple test will show whether there is a danger of spurious triggering. The proposed network is either installed or simulated. (The better test would be with at least the proposed wiring runs laid out in their approximate positions so as to include pick-up products). Then with VR2 set up (see setting up), VR1 can be adjusted in accordance with the procedure. Switch the Comparator to 'Lock-On' and leave it running for some time without the siren connected. Any spurious triggering will 'Lock' the system on and the l.e.d.s will indicate such an occurrence.

When reed switches are employed, use a simple bar magnet but avoid the magnets found in cupboard latches, they are multi-pole and difficult to use.

Wiring runs should terminate at a point where the electronics can be placed out of sight. The internal siren or bell should be sited away from the box and out of reach, thus location of the source of sound will not lead to the electronics. A good place in the average two storey house is high up in the stair well with the siren leads running through the loft.

OPERATIONAL PROCEDURES

The Compensators are used to substitute for an open sensor, one for one. All it does is put one resistor in when one has been taken out of circuit. Up to eight windows/doors may be opened since there are eight sections to the Compensator.

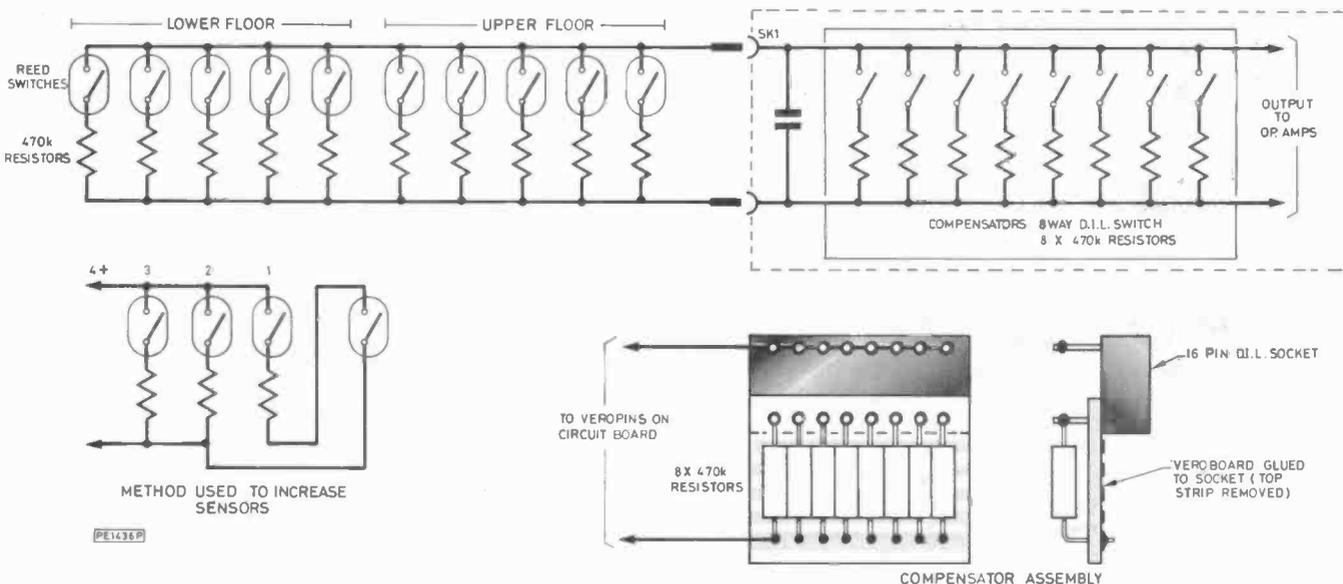


Fig. 1.5. Layout for a practical network

The two modes are self-explanatory. 'Lock-On' is useful when the premises are unattended unless pets are likely to interrupt any I.R. beams or ultrasonic movement detectors; 'Auto-Reset' is perhaps best when the house is occupied but protection desired. When it is necessary to open windows for instance and a compensator is used, 'Lock-On' is not the best mode of operation unless the compensator can be switched in before expiry of the delay. In the case of upstairs windows an alternative is to mount a miniature slide switch in the reed switch casing and use it to short circuit the reed switch when the window is open. This method does rather tend to negate the anti-tamper facility in that an intruder might just spot the switch. In any event, it is always possible to switch off the system until compensating adjustments are made. In the prototype installation, micro switches were used in the upper storey stations and a toggle included in the mounting bracket so that the micro switch could be held over by the toggle when the window was to be left open.

In a secret but adjacent position to the outer doors, a switch is recommended; together with its 470k resistor, this switch can be used whilst standing at the open door paying the milkman or perhaps whilst attempting to rid oneself of a persistent salesman. As a panic button such a secreted switch could also come in useful provided the delay set into the system was reasonable. This switch is simply shunted across the door sensor and can either contain its own 470k resistor or, if convenient, just shunt the micro switch or reed switch or whatever has been used as a sensor on the door.

Delay times are adjusted to suit the premises and the operator. A large house with tortuous passages and an owner who is no longer quick on his feet, might like to have a longer delay so that he can make an exit before expiry of the delay time, particularly if 'Lock-On' is to be used whilst off the premises. A suggested time scale for a normal house and operator could be:

- Exit entry delay . . . 15 seconds.
- Delay before external siren operates . . . 45 secs.
- Operating time of ext. siren . . . 180 secs.

This means that the delay set into the Two Timer will be 30 seconds plus 15 = 45 seconds after the triggering by opening a door/window and 30 + 180 = 210 seconds after, for the second period of delay, since all delay times are independent.

If 'Auto-Reset' is used, the sequence of events, i.e.

- (a) Trigger
- (b) Delay to internal siren commencing
- (c) Delay to Two Timer starting external siren
- (d) Period of external siren operating can be interrupted at any point in time by simply removing the cause, e.g. closing the open door or window.

If however, 'Lock-On' is selected, after the initial delay intended for exit and entry, removal of the cause will be ineffective and the only way to prevent the inexorable progress of the sequence will be to switch to 'Auto-reset' and remove the cause. 'Lock-on' can then be re-selected.

Since relay outputs are included in both the Comparator and the Two Timer, within the capacity of the contacts, external or internal lights can be activated.

When closing doors or windows which have been previously compensated for, remember to put out of circuit the appropriate compensator, otherwise the system will react to an attempted tamper.

All variable resistors are wired such that a clockwise movement increases the resistance; this means that in the case of delay controls, clockwise adjustment increases the delay. In the case of the width control, a clockwise adjustment increases the width.

It is necessary to lift the battery clips off the batteries if

the system is unplugged from the mains for a long period (say 12 hours) because of the possibility of a minute drain back through the power unit components.

Should the batteries become completely discharged, it is permissible to switch off at the On/Off switch whilst leaving the mains still connected. In this way a faster charge is achieved but as soon as the system stabilises it is best to put the system switch on.

CIRCUIT DESCRIPTION

The circuit diagram of the intruder sensing comparator is shown in Fig. 1.7. The input from the external network (see Fig. 1.5) is fed to the input socket and then to the dual JFET operational amplifiers of IC1. Each of ten sensors in parallel represent an equivalent resistance of 47k, all compensators being switched out (all eight d.i.l. switches at Off).

The two op. amps. are in a very high gain configuration, there being no feedback network. The network R1, R2 and VR1 holds pins 2 & 5 at fixed potentials, dependent on the setting of VR1 (Width Control). The inverting input of IC1a is held slightly above its fellow non-inverting input and the non-inverting input of IC1b is held slightly below its fellow inverting input. Pins 3 & 6 are held at whatever potential the external network dictates. Normally these pins 3 & 6 are at half Vcc so long as all sensors are normal and VR2 has been properly adjusted.

A second look at the input circuitry will reveal a situation where the input to pins 3 & 6 paralleled together consists normally of the resistive value of the external network as part of a potentiometer and the adjusted value of VR2 as the remaining part. VR2, having been adjusted to equal the parallel value of the external network, means that the potential at pins 3 & 6 is half Vcc, whereas the potential at pin 2 is slightly above half Vcc and that at pin 5 is slightly below. The difference, or 'Width' between pins 2 & 5 is determined by the setting of VR1. This in turn determines how big a change in the external network is needed to switch the op. amp. from one state to the other (see Fig. 1.6). The ratio of 'sensitivity' between the extremes of VR1 set to 25k and set to 100k (max) gives very nearly 4-1. Settings below 25k are possible but extra cognizance of electrical noise is required if 'glitches' are to be avoided; it does depend a great deal on the local electrical atmosphere.

Figs. 1.6a to 1.6e show the effects of disturbances to the external network and if referred to the 'Width' potentials of Figs. 1.6f to 1.6h it can be seen that very narrow 'Width' settings are unnecessary, unless more than ten sensors are to be installed.

The result of tampering can be seen at Fig. 1.6c, d & e and if the Truth Table of Table 1 is studied, the actual logic changes will be clear.

The output pins 1 & 7 of the dual op. amp. are connected directly to the inputs of a pair of NAND gates and via Inverter Buffers to the remaining pair of inputs.

The Inverter Buffers are part of a Hex. Inverter i.c. (IC2) and the NAND gates part of a Dual Input Quad NAND Gate i.c. (IC3). To follow the logic sequences, reference should be made to the Truth Table again (Table 1). An ALERT state, that is when the system is ON and set up, gives similar output voltages at pins 1 & 7 IC1, both being getting toward the low state. An INTRUDER state, that is when a door or window sensor has opened its contacts and its 470k resistor has been open circuited, produces a high at pin 7 whilst pin 1 stays low. This means that IC3a now has two low inputs and therefore its output will go high (pin 3 IC3a). Meanwhile, IC3b is receiving two high inputs at pins 5 & 6. The output at pin 4 therefore will be Low taking pin 13 IC3c with it.

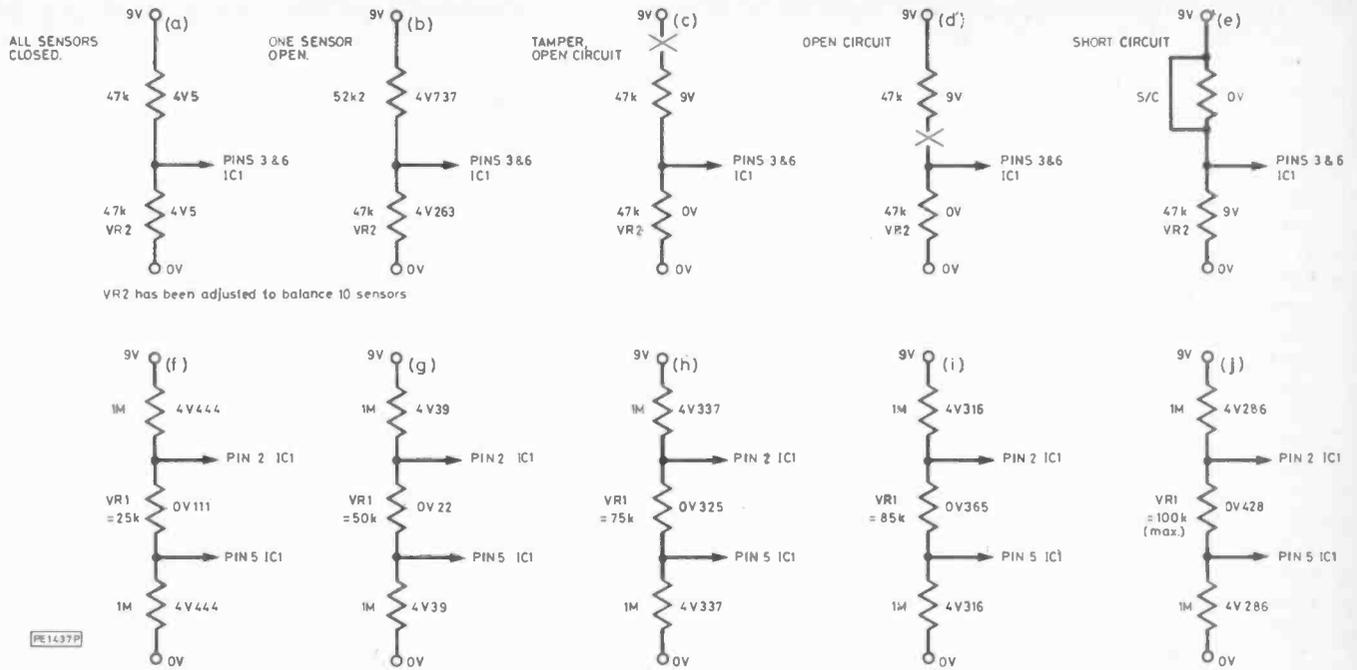


Fig. 1.6. The effects of an external network disturbance (top) and the effects of adjusting the width control (bottom)

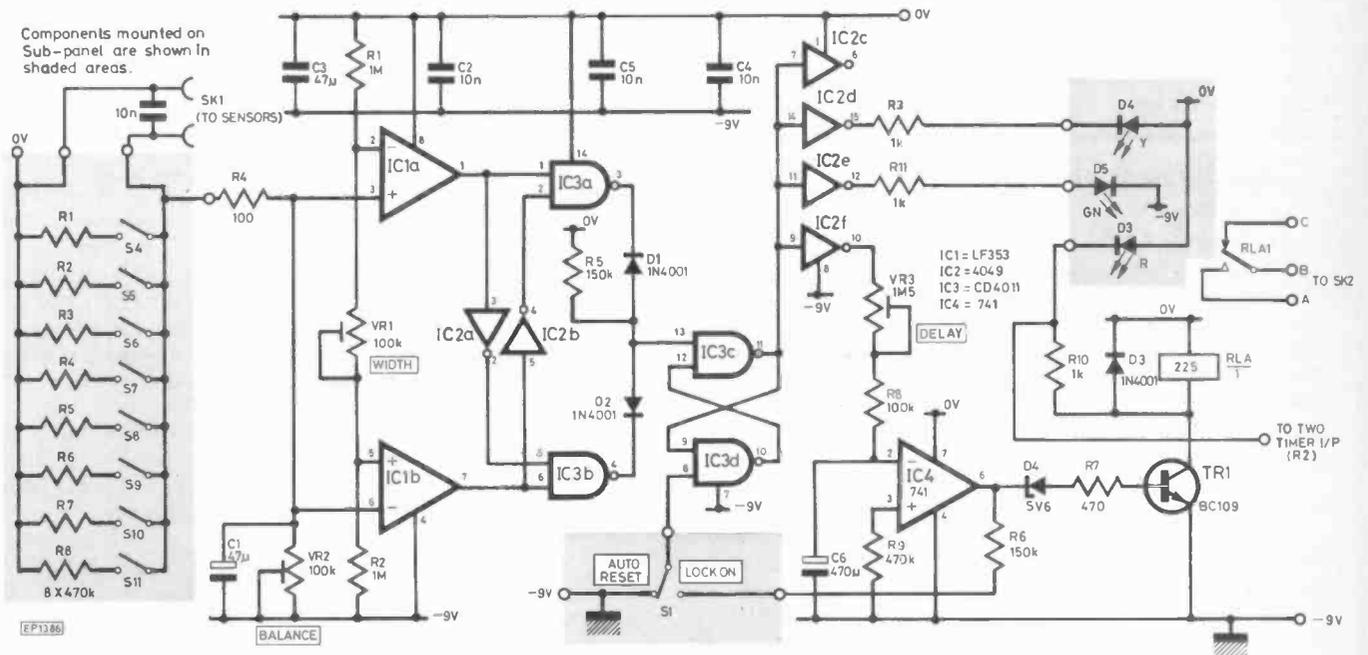


Fig. 1.7. Circuit diagram of the Intruder Sensing Comparator

| STATUS | IC1 a & b PINS 3 & 6 | IC1 a & b | | IC3a PINS | | | IC3b PINS | | | IC3c PINS | | IC2c d e f | | | IC2c d e f | | |
|---------------|-------------------------|-----------|-------|-----------|---|---|-----------|---|---|-----------|----|-------------|--|--|--------------|--|--|
| | D.C. Volts | D.C. | Volts | 1 | 2 | 3 | 4 | 5 | 6 | 13 | 11 | 7,9,11 & 14 | | | 6,10,12 & 13 | | |
| Alert & Ready | 4.25 | 1.85 | 1.85 | L | H | H | H | H | L | H | L | L | | | H | | |
| Intruder | 3.70 | 1.85 | 8.0 | L | L | H | L | H | H | L | H | H | | | L | | |
| Tamperer | 4.50 | 8.0 | 1.85 | H | H | L | H | L | L | L | H | H | | | L | | |

N.B.

As pins 6, 10, 12 & 13 of IC2 c, d, e & f switch low under influence of either Intruder or Tamperer, C6 discharges through VR3 and R8. At or near the point of discharge the high gain 741 switches to its output state.

In order to preserve correct polarities between the different boards, Vcc at the Comparator is in fact 0V as observed at the Power Supply Unit and at the Two Timer. Vee at the Comparator is therefore -9V.

Table 1. Comparator Truth Table. (Vcc 9V, Mode Auto-Reset)

Any attempt to Tamper with the external network will produce a high at pin 1 IC1a, therefore at 5 & 6 IC3b there will be a pair of lows and at 1 & 2 IC3a there will be a pair of highs. Thus pin 4 will go high and pin 3 low. It will be seen that whichever 'Emergency' state occurs, pin 13 (IC3c) is changed from high to low.

IC1 (a) & (b) along with IC3 (a) & (b) constitute a kind of discriminating bridge. It would be possible to distinguish between a short and an open circuit in the external network but there is little point. The important fact is that someone with probable malevolent intent is attempting to intrude (always assuming that inadvertent action is not the cause). When the network is disturbed pin 13 of IC3 (c) receives all inputs whether as a result of an o/c sensor or tampering with the wiring.

IC3(c) & (d) are in flip-flop configuration and one input, pin 8, is returned to either 0V or to a feedback resistor R6. The option is made by a slide switch S1 and this is the mode choice of 'Lock-On' or 'Auto-Reset'.

Pin 11 of the flip-flop section of the Quad NAND is the output and feeds the inputs of the four remaining Inverters IC2 (c to f), the other two sections being already used. These four Inverters provide:

- (1) An input to the delay circuit, VR3, R8, C6 & IC4.
- (2) Control of l.e.d. annunciator, Green for Alert & Ready.
- (3) Control of l.e.d. annunciator, Yellow for Network Disturbance.
- (4) Control of l.e.d. annunciator, Red for Internal Alarm (via TR1).

When all is normal and Alert, the output of IC2(f) pin 10, is high and therefore C6 will be fully charged. On receipt of an alarm signal, pin 10 falls and C6 starts to discharge through VR3 & R8. At a point near to complete discharge the 741

high gain operational amplifier will rapidly change its output potential from low to high. This changes the base bias of the BC109, TR1 which controls the output relay.

By adjusting the value of VR3, a suitable delay can be obtained, enough to make exit or entry without actuating the alarms. This delay inhibits both the closing of the relay and the effectiveness of the 'Lock-On' circuitry for the period set in by VR3.

It will be noticed that the coupling between the 741 output and TR1 is via a Zener diode. This is because a residual voltage exists at pin 6 even in the so called low state and this is sufficient to hold the BC109 in conduction, thus the relay would never open. The 5V6 trigger level of the Zener ensures that below this voltage the base of TR3 is low enough to cut off its collector current.

When an alarm state is sensed, and after the discharge of C6, IC3 output rises to more than 5.6 volts and TR1 is driven into full conduction. The relay closes and the Red l.e.d. is lit (most useful when setting up and the siren disconnected) and if 'Lock-On' has been selected, a feedback loop from IC3 output, pin 6, via R6, is taken to pin 8 of the flip flop via S1. This causes the flip flop to lock up until the loop is broken. This is done by sliding the switch S1 to 'Auto-Reset'. If the cause of the alarm is now removed, 'Lock-On' can be reselected.

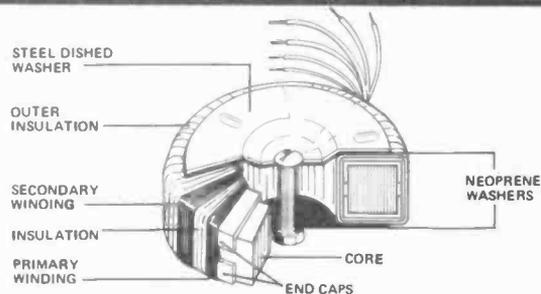
When the house is occupied, 'Auto-Reset' will allow entry and exit into the garden for instance, without triggering off the alarms and becoming a nuisance. Alternatively, interference with the external network when the house is vacated and the 'Lock-On' mode selected, will trigger the system.

NEXT MONTH: Comparator construction, interwiring and testing

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| 0x015 | 22+22 | 0.34 | 2x017 | 30+30 | 0.83 | 4x017 | 30+30 | 2.00 | 6x026 | 40+40 | 2.81 | 8x028 | 110 | 4.54 |
| 0x016 | 25+25 | 0.30 | 2x028 | 110 | 0.45 | 4x018 | 35+35 | 1.71 | 6x025 | 45+45 | 2.50 | 8x029 | 220 | 2.27 |
| 0x017 | 30+30 | 0.25 | 2x029 | 220 | 0.22 | 4x028 | 110 | 1.09 | 6x033 | 50+50 | 2.25 | 8x030 | 240 | 2.08 |
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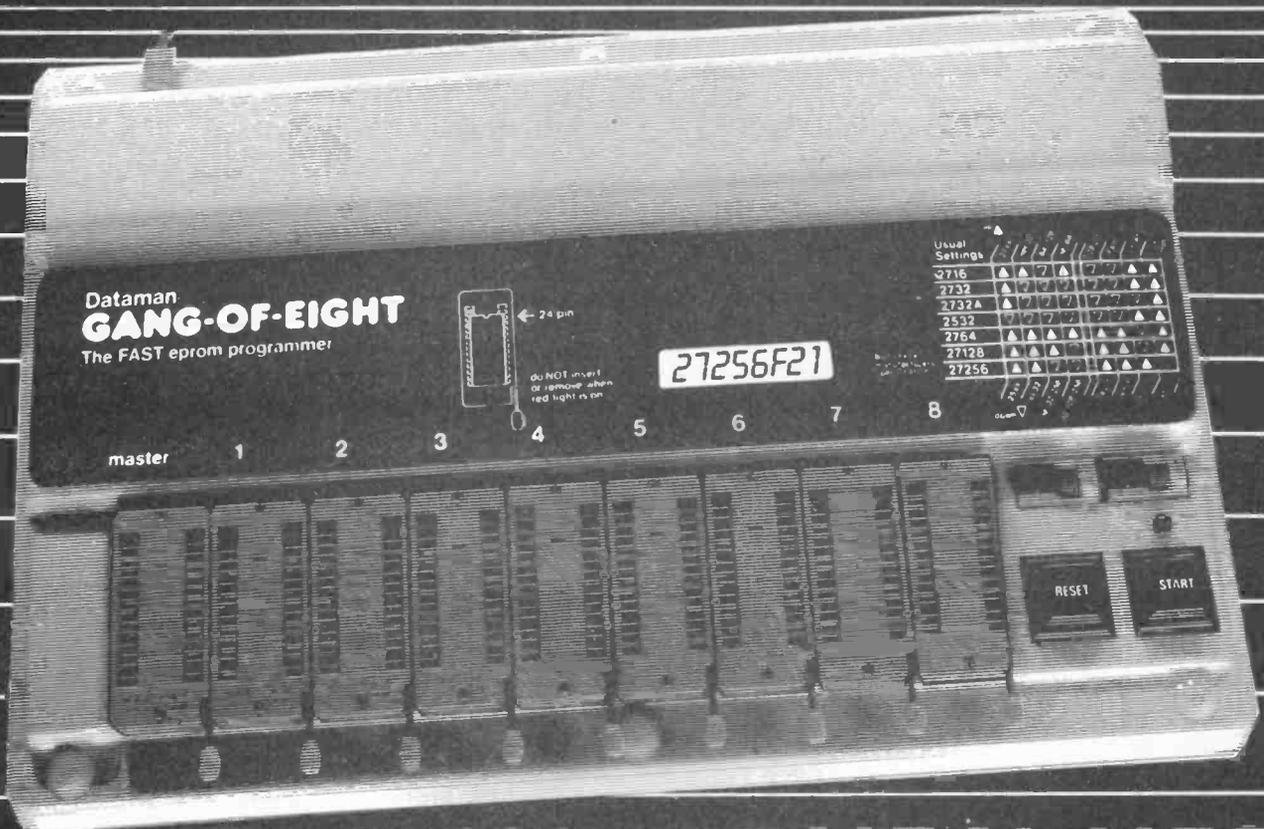
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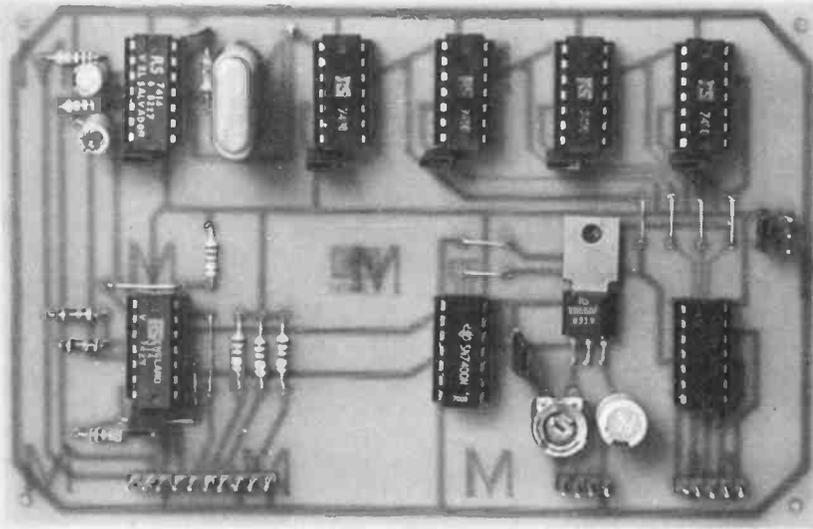
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This month's Digital Project deals with the construction of an oscilloscope calibrator. The unit provides signals which can be used for the calibration of both the timebase and the X and Y amplifiers of an oscilloscope. In addition, a range of standard output frequencies and periods are provided at TTL voltage levels. These outputs can be used to provide accurate timing of digital circuits and a means of calibrating digital measuring equipment.

SPECIFICATION

TTL OUTPUTS

Waveform: Square, unity mark to space ratio
 Frequency: Four outputs at 1MHz, 100kHz, 10kHz and 1kHz
 Period: 1 μ s, 10 μ s, 100 μ s and 1ms respectively

NORMAL OUTPUT

Waveform: Square, unity mark to space ratio
 Frequency: Switch selected 1kHz, 1MHz and 1kHz/1MHz
 Output impedance: 50 ohm (nominal)
 Output amplitude: 1V (adjustable from 0V to 2V approx.)

CIRCUIT DESCRIPTION

The circuit diagram of the Oscilloscope Calibrator is shown in Fig. 1. The various outputs of the unit are all derived from the same crystal controlled oscillator formed by IC1f and associated components. The 10MHz output of this oscillator is buffered by IC1e in order to minimise loading effects. This stage is then followed by four decade dividers, IC2 to IC5, which provide square wave outputs having frequencies of 1MHz, 100kHz, 10kHz and 1kHz respectively. The output from each decade divider stage is then buffered by inverting gates, IC6c to IC6f, which provide TTL compatible outputs having periods of 1 μ s, 10 μ s, 100 μ s and 1ms respectively.

The 1MHz and 1kHz decade divider outputs derived from IC2 and IC5 are also directly fed to the logic gate arrangement formed by the three two-input NAND gates, IC7a, IC7b and IC7d. This arrangement gates the 1MHz and 1kHz signals together according to the state of the two control signals applied to pins 2 and 5 of IC7. The output of the gate arrangement is then fed to TR1, a VMOS FET operated in source follower mode. This stage acts as a buffer and minimises loading effects at the output. VR1 is used to set the output level to exactly 1V peak.

The two control inputs to the control logic arrangement are derived from J-K bistables, IC8a and IC8b, and momentary operation push-button switches, S1 and S2. IC1b, IC1c and associated components are used to de-bounce the outputs of S1 and S2 respectively. L.e.d.s, D1 and D2, are used to indicate the mode of operation currently selected and D3 indicates that the supply is present and the unit is operational. Output waveforms corresponding to the four modes of operation are shown in Fig. 2.

CONSTRUCTION

The Oscilloscope Calibrator is built on a single sided p.c.b. measuring approximately 140 x 90mm, the copper foil layout of which is shown in Fig. 3. The corresponding component layout on the top surface of the p.c.b. is shown in

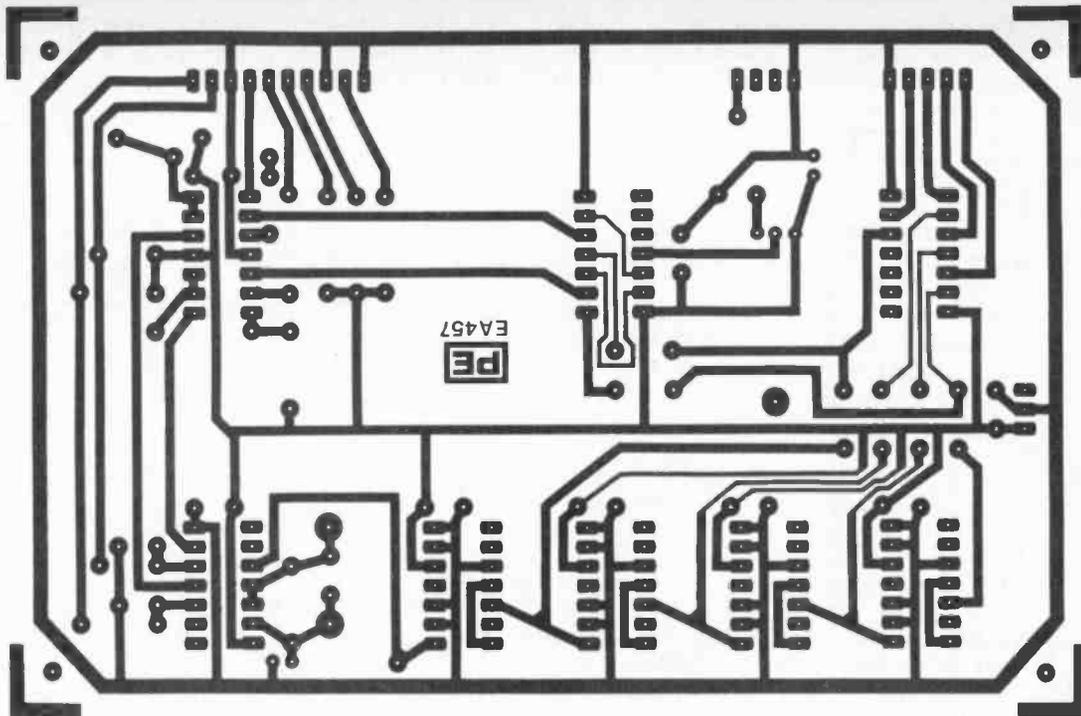


Fig. 3. P.c.b. design

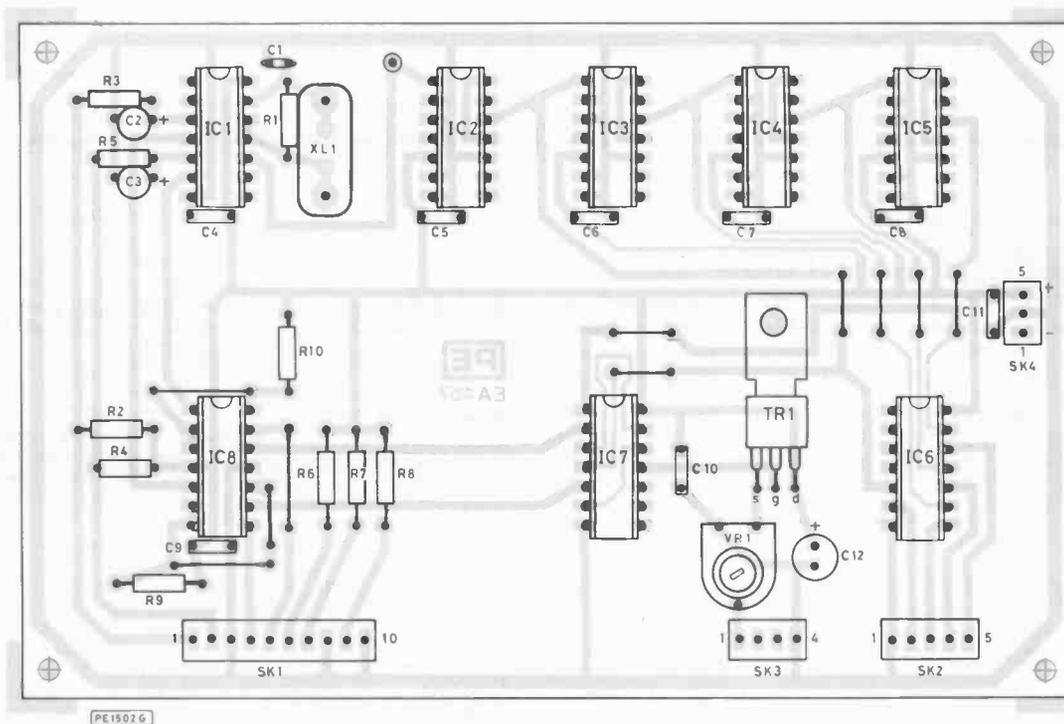


Fig. 4. Component layout

Once assembly is complete, the underside of the p.c.b. should be carefully checked for solder splashes, bridges between adjacent tracks, and dry joints. Finally, the i.c.s may be inserted in their respective holders, taking care to ensure the correct orientation of each device. Constructional details of the enclosure have not been given since this will undoubtedly be a matter of preference for the individual constructor.

A small diecast or ABS case will normally be found to be quite adequate in this respect. The momentary push-button switches and their respective l.e.d.s should be mounted on the front panel together with the four TTL output sockets and the 'normal' output, SK5. The choice of connector used for SK5 is again a matter for personal preference although use of a 50 ohm BNC type is strongly recommended.

Constructional details of a suitable power supply module were given in the January issue of *PE*; alternatively, for portable applications, power may be derived from three fresh 1.5V dry cells connected in series. These should be connected to the Oscilloscope Calibrator via a suitable miniature toggle or slide switch.

TESTING

Testing the Oscilloscope Calibrator requires the use of an oscilloscope and a digital frequency meter. The supply should first be connected to the Oscilloscope Calibrator, D3 should become illuminated and the waveform at the test point (TP) should be investigated. This should have a minimum peak-peak value of approximately 2.5V and a frequency of almost exactly 10MHz. If this is not the case check IC1f and associated components. Note that, at this point in the circuit, the waveform may not appear to be very square. Now transfer the oscilloscope and digital frequency meter to each of the four TTL outputs in turn. Check that a square waveform is displayed at each output. If this is not the case check each of the decade dividers in turn, IC2 to IC5, and IC6.

Finally transfer the oscilloscope and digital frequency meter to the 'normal' output, SK5. With S1 and S2 both 'off' (i.e. D1 and D2 both extinguished) the output should be 0V and no signal should be present. Now depress S1, D1 should become illuminated and the output should now consist of a 1kHz square wave output. VR1 should then be adjusted so that the output is exactly 1V pk-pk. Depress S1 for a second time (D1 should go off) and then depress S2. D2 should become illuminated and the output should now consist of a 1MHz square wave of 1V pk-pk. Finally depress S1 such

that both D1 and D2 are illuminated. The output waveform should now consist of a 1V pk-pk train of 500µs bursts of 1MHz signal, as shown in Fig. 1. This completes the testing procedure and the Oscilloscope Calibrator is now ready for use.

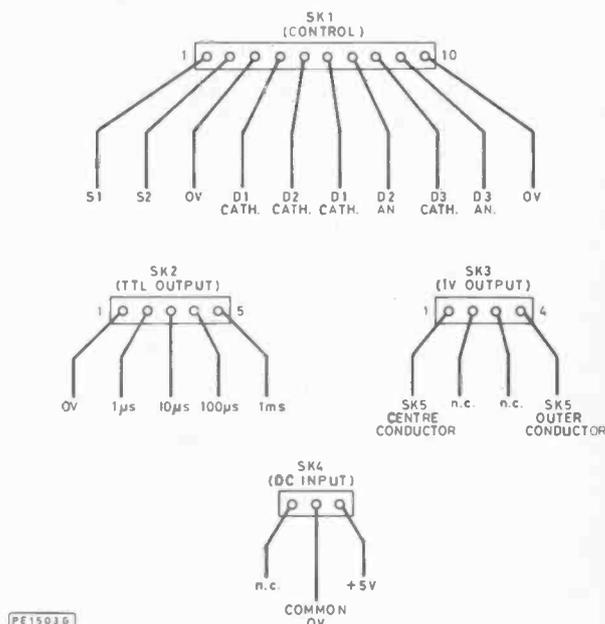


Fig. 5. Interconnections

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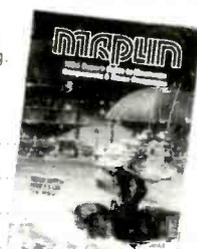
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