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size memory package - News, p7 Right: Brand new sections are being introduced on p14 and p37 Below: Products section starts on n52



The front cover comes courtesy of Varta Microbattery GmbH. Varta's new Cardpower battery addresses the powering needs of future smartcard applications.

Editor's c Always the bride

Technolo Top Ten

Insight Good architectur

Focus: S

Shedding The machine visi electronics and s

Match m

Christopher Macl that could lead to

ADCs: de Adrian Grindon g

mance from an A

FPGA so

Ever wondered h digital display de

Games Wireless

Heading toward

Circuit Ide

- Efficient ber
- 2V DC-DC o Sky box dro
- Replacing a
- Early warning

Letters

Products

February 2005	Volume 111	Number 1826
Editor's comme ways the bridesmaid	ent	3
echnology op Ten Tips		4
nsight bood architecture with grea	t timing	13
ocus: Second		14
hedding light (ne machine vision sector is ectronics and semiconduc	providing bright opportu	unities for the
Aatch made in ristopher MacLeod discus	sses the new advances ir	20 n biotechnology
DCs: demanc drian Grindon gives a detai ance from an ADC or DAC	iled overview of how to g	
PGA solution i ver wondered how to best gital display design? Bart B	select an FPGA with DSF	^o functions for your
Games		37
Vireless Colum ading toward auto-nursing		39
Dircuit Ideas • Efficient bench power s • 2V DC-DC converter • Sky box dropout zappe • Replacing a pulse relay • Early warning system • Simple mains power –	er /	40

47 52

1

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tion control. Operates in stand-alone or PCcontrolled mode. Up to six 3179 driver boards can be connected to a single parallel port. Supply: 9V DC. PCB: 80x50mm. Kit Order Code: 3179KT - £9.95 Assembled Order Code: AS3179 - £16.95 Assembled Order Code: AS3113 - £24.95

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Most items are available in kit form (KT suffix) or assembled and ready for use (AS prefix).



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able separately), 4 indicator LED 's, Rx: PCB 77x85mm, 12VDC/6mA (standby). Two and Ten channel versions also available. Kit Order Code: 3180KT - £41.95 Assembled Order Code: AS3180 - £49.95

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Enhanced "PICALL" ISP PIC Programmer



Always the bridesmaid ...

dedea+, a EU-sponsored R&D programme in microelectronics and nanotechnology, is meant to define the future of the European microelectronics industry. It is said that the technological potential of the microelectronics industry is such that its positive effects on the development of the economy's productivity are guaranteed for a long time in the future.

So, how come for several years now, Medea+ organisers and participants complain that the there's not enough money being ploughed into this and similar programmes (see news story on page 6)? Year after year, one and the same message emerges from Medea gatherings, and that is that other fields receive more public money than microelectronics programmes do. Agriculture is one big sticking point. It is always being mentioned as one area that seems to suck up most of EU's money, some €45bn of it. This year, it turns out that the tobacco industry is being sub-sidised with €1bn, a sum equivalent to what the information and communications techno-logy (ICT) field receives from the EU.

But, is Europe's success in the field of electronics just down to money or are there other reasons why Europe still lags behind the US and Japan in microelectronics development? Europe's lead - if the opportunity really ever existed - is further threatened by new countries. Taiwan and China are growing strong very rapidly in microelectronics development and manufacture. But going back to the old nemesis: the US - even today, with the continuously weakening dollar - seems to be doing a lot better in microelectronics than Europe. The same goes for Japan, a country that struggled for years to pick itself out of the economic doldrums it had entered into during the 90s. Europe, however, always appeared to

EDITOR: Svetlana Josifovska E-mail: s.josifovska@highburybiz.com EDITORIAL E-mail: EWeditor@highburybiz.com EDITORIAL ADMINISTRATION: +44 (0) 1322 611274 E-mail: EWadmin@highburybiz.com CONTRIBUTING WRITERS: Nick Flaherty, Matthew Peach, Keri Allan PRODUCTION EDITOR/DESIGNER: Jane Massey SUBSCRIPTIONS: Highbury Fulfilment Services, Link House, 8 Bartholomew's Walk, Ely Cambridge, CB7 4ZD. Telephone: +44 (0) 1353 654431 MANAGING EDITOR: Bill Evett • PUBLISHING DIRECTOR: Tony Greville

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be on the back footing to these two - 'always the bridesmaid never the bride'. It had always appeared sluggish in comparison, and just simply not as creative. Why is that?

Some industry executives I spoke to recently offered the answer that Japan and the US are both single countries and that Europe, with all its states, cannot be organised as a single entity and as such be as agile and responsive. But, is there more to it than that? Would you say that in addition to lack of money (for programmes, projects, small and medium sized firms, start-ups and even engineers) there is a lack of enthusiasm within European organisations, too? There is certainly a lack of aggressiveness, but is there, perhaps, a lack of creativity - or could that be, whatever creativity exists it is stifled?

Not that long ago, an internal EU report on productivity surfaced that admitted that, if the EU business model was the same as the that of the US, EU productivity would increase by 12%. At this year's meeting, the Medea+ executives agreed that closer cooperation between European R&D programmes and Brussels is necessary, as well as a clearer vision of the strategy for Europe in the field of micro- and nanoelectronics.

That is a good way forward, not only to negotiate more money for the programme and the industry in general, but to possibly acquaint politicians with what it is to be an engineer, what it takes to oil the wheels of creation and innovation and how to best nurture that environment to prime it for competitiveness. Maybe only then, we could make other countries' electronics industries start fearing Europe.

> Svetlana Josifovska Editor



Technology

Digital tool warns against system power failures

Power system designers can rest easier about failure risks thanks to a new power management software/hardware combination introduced by Canadian firm Potentia Semiconductor.

"In complex systems in applications like communications, computer, industrial and medical, there are a lot of power rails, a lot of different voltages - sequencing, high currents and so on, and power is a big risk of introducing failures into such systems." said Ian McGill, VP of business development at Potentia.

Potentia has a range of standalone ICs based on state machines only (no processors involved as McGill says, "BIOS makes customers nervous") that act as either isolators (PS1005/1006) where the input voltages are high, say 44V, or power controllers (PS2406) where they can "monitor" and "control" up to four different points off load (POL) at one time. For a higher number of POLs, cascading PS2610 chips will help. The software that sits above the system - PowerCentre Designer - then allows system developers to configure the



ICs for thresholds, delays and trim for each rail, to keep system failures down to a minimum but also remedy problems quickly.

There are several such points: first threshold voltage point can be adjusted according to the fail-safe voltage of the system: the second threshold voltage point can be adjusted to allow a different rail to 'fire up' after a given time; alarm- as well as faultthresholds can be set up,

where a rail is monitored for over-voltages over a certain period of time. Then there's a shutdown interlock that allows the system's rails to power down in reversed order to which they started, for full system safety.

"There are so many technical challenges in systems today that tools like ours are needed more and more. It's our belief that there's a transformation happening in the power management industry, from

time-consuming, hardwaredependent, black art, analogue design, to fast, configurable, knowledge-based tools that are digital," added lan.

In addition, the software contains a 'field analysis' capability that will help designers to fault-find more precisely within complex circuits.

Potentia's ICs contain 10-bit. 1% accuracy ADCs for each channel, which have also been developed by the firm, and non-volatile OTP memory.

Silicon lever may spell the end for viruses

AAA.

/iruses, bacteria and toxic V organic chemicals can be detected easier now thanks to a microscopic silicon device developed by researchers at US-based Cornell University.

The device consists of silicon paddles only 6µm to 10µm long, half a µm wide and about 150nm thick, with 1µm square

pad at the end. The experiment to detect pathogens revolves around pinpointing the natural frequency of vibrations that depend on its mass. Large array of paddles are mounted on a piezoelectric crystal and are made to vibrate at frequencies of 5-10MHz, When the frequency

matches the paddles' resonant frequency, they begin to vibrate. This can be measured by focusing a laser on them and noting the change in reflected light, a process called optical interferometry. A single silicon paddle weighs around 1.2pg and vibrates at frequencies around 10MHz. The virus used in the experiment weighs about 1,5fg. Adding just a few virus particles to a paddle is enough to change the resonant frequency.

The research could lead to simple detectors capable of differentiating between wide varieties of organic materials.

UK scientists break the world's time-measurement accuracy record

The UK's National Physical Laboratory (NPL) has found of new way of measuring time that is three times more accurate than any other method in the world.

The implications could be dramatic as they may lead to changing the way we measure time. In the nearer future, though, they are likely to enable improved levels of accuracy in deep space navigation and exploration.

"We are not there yet, but we know now that we have a working blue print that proves we can do it," said Professor Patrick Gill, who conducted the research.

Prof Gill and his research team used a strontium ion trap to create a stable optical

frequency that is [Photos: National Physical Laboratory, Crown Copyright 2004 – Reproduced with the permission of the controller of HMSO then measured. and Queen's Printer for Scotland]

To create the frequency, a single ion of strontium is trapped and isolated in a vacuum, and then chilled to near absolute zero (-273°C) with a blue laser beam (wavelength of 422nm). The laser "bombards" the ion with millions of photons, and as each is absorbed and reemitted causes the ion to lose a small amount of energy. Eventually, the ion "cools down".

A second mono chromatic red laser (674 nm) is then aimed at the cold ion and tuned to two very precisely defined energy states that it now has. Once

the laser is locked on to this precise energy - or frequency interval - it becomes very stable. This laser now provides the optical frequency that NPL believes will lead towards the world's most accurate clock. possibly able to measure the second down to one part in 1018. That is nearly a thousand times more accurate than the best clocks of today.

The very stable laser light is sent down an optical fibre to a nearby laboratory where its frequency is measured against a laser frequency 'comb'. These are very short pulses of laser light that cover infrared. level of accuracy.

stripped away).



Technology





Above: The ovens and electrodes of the NPL strontium ion end-cap trap, viewed in situ in a vacuum chamber

Left: The ultra-low-expansion glass cavity used to stabilise the 674 nm "clock" laser used in the world's most accurate opical frequency measurement

the spectrum from blue to

Each "tooth" of the comb is referenced to the Caesium fountain clock, which, as the current instrument defining the second, represents the highest

In July 2001, the first big breakthrough in time measurement was announced by US scientists at the National Institute of Standards and Technology (NIST). They created a prototype clock based on the optical frequency of a single mercury ion (an atom with one electron

The MultiBand OFDM Alliance Special Interest Group (MBOA-SIG) has completed its physical layer (PHY) 1.0 specifications and is now making them available to its members. The move enables many companies in consumer electronics, personal computing. mobile phone and the semiconductors husiness to finalise their standards-based ultra wideband (UWB) chip and board-level designs. This is particularly important to over 16 silicon developers that are now developing customer samples, and will result in pre-production interoperability testing. "We are proceeding quickly to ensure interoperable consumer products in mass production," said Stephen Wood, strategic marketing manager at Intel's R&D division and a member of the MBOA-SIG steering committee. O

Temple University in Philadelphia, US, has used functional magnetic resonance imaging (fMRI) technology to scan for lies. The scientists say that scanning the brain with fMRI has highlighted that when people lie activation occurs within seven brain areas, compared to four brain areas when neonle are telling the truth. Using fMRI as a lie detector is expensive, but in some cases. such as questioning terror suspects or in severe criminal cases, it could be worthwhile, says **Dr Scott Faro of Temple University.**

Taiwanese power supplies maker FSP Group, has formed a new technology company in Germany to compliment its portfolio range. The new firm is named Amacrox and among its new products will be computer peripherals, lenses for mobile phone cameras and MP3 transmitters. Amacrox is setting up sales offices in the US, the UK. China and Taiwan. It is establishing an R&D division and manufacturing centre in Shanghai to develop and make new products. A design facility and procurement centre has been set up in Taiwan. Ω

Today's MPU architectures fall foul of Moore's Law

oday's microprocessor architectures will no longer be suitable for system design when transistor scaling goes beyond100nm, said Hugo de Man. co-founder of Belgian research institute IMEC at the recent Medea+ gathering. "Power in today's computing is very inefficient - power dissipation doubles up every three years - it's an anti-Moore's Law. So, we need to think of other, new, architectures," he said.

Power savings can be made in various ways: through new technologies, new materials, better software programming, better tools, better distribution of instructions and data, localisation of memories and so on. Each step could deliver power savings of up to 30%. But, according to Prof de Man, the industry needs to make 14 steps in design and technology to make significant improvements. "That's a major architectural change."



Microprocessor power is Moore's Law in the wrong direction

Prof de Man has several ideas of how to move on, but it does mean abandoning the old, trusted ways. "First, get rid of the Von Neumann microprocessor architecture that's programmed in a classical way las transistors are used for more cache and not so much for computation]. We should use only fast and flexible architectures for parallel processing, and software 'washing' machines to save on

power. For that, we will require a new class of designers and architects, new methodologies and new tools."

Prof de Man also had a go at the EDA industry, which he claims is not doing enough now to prepare tools for the 45nm scaling that is expected in several years' time. "It takes ten years before concepts get into the EDA world. We need to get into it [building EDA tools] now but

there's no money in it for them [the EDA tool companies] now. So they are not doing anything about it."

When transistor scaling below 100nm, in addition to architectural problems, there are physics matters that need to be resolved, too. They have been cumulatively named 'the hell of physics' and consist of gate leakage, voltage headroom, increased gate variability, irregular lithography layout, signal integrity, global interconnect delays and others.

To be able to resolve all these issues. Prof de Man suggests to "lock up hardware and energy-aware software designers with 'nano' aware architects and start getting somewhere". This, it seems, will give rise to a new category of engineer. the so-called "silicon platform architect", who will be well versed in software programming, as well as mixed signal and RF design.

EU strong on R&D cooperation but not on funding

uropean cooperative R&D research like Medea+ is a success for Europe, claim government officials, even though little money is invested in the programme and countries like the US and Japan are still in the lead in microelectronics development.

.

"The Eureka formula bottom-up, lean and flexible organisation - has always been a strong asset in suporting Europe's economy," said Patrick Devedijan, the French Minister of Industry. He said that over €22bn of public and

private funding has already been used in Eureka projects of which Medea+ is one.

Controversially, the biggest bugbear for Medea+ participants and organisers is the lack of government money, which will adversely affect Europe's competitiveness in ICT (information and communication technologies). Half of the EU budget, or some €45bn, is spent on agriculture. In comparison, only €3bn per vear supports innovation and. of that, just a fraction - €1bn is spent on ICT. This is the

same amount with which Europe subsidises the tobacco industry.

"Is it right for the ICT industry to get less than the tobacco industry?" asked Doug Dunn, CEO and president of Dutch lithography equipment maker ASML. "Now is the time to act to avoid Europe becoming a 'qhost ship' on the ocean."

At this year's meeting, the Medea+ executives agreed that closer cooperation between Medea and Brussels is needed, as well as a clearer vision of the strategy for

Europe in the field of microand nanoelectronics. In addition, they conceded that more emphasis should be placed on SMEs.

Medea+ is a pre-competitive cooperation: It takes from one to 1.5 years for process technology and between two and 2.5 years for equipment to be brought to market after Medea. The top three participants in the programme, each with thousands of proposed projects, are France, followed by Germany and the Netherlands.

ELECTRONICS WORLD February 2005

'Easy' 32-bit processor created specially for FPGA designs

An Australian EDA company has launched its own, rovalty-free, 'easy to use' 32bit processor for FPGAs - the TSK3000

Altium develops design tools for FPGAs and circuit boards with its Nexar and P-CAD tools, and has teamed up with FPGA software tool developer Tasking to design a 32-bit Harvard architecture core with a five stage pipeline, combined with an 8-bit openstandard Wishbone interconnect bus. Wishbone is a system-on-a-chip (SoC) interconnect bus for portable semiconductor IP cores that allows flexible design methodology.

The aim is to provide a core for designers to use in FPGAbased reconfigurable systems, rather than SoC devices, supported by a compiler and debugger from Tasking, The main advantage is the ability to use one such processor core, and therefore one code base, across multiple types of devices. The processor can be used on any target FPGA



Tasking has provided the tools to support Altium's new TSK3000 processor

family with no licensing issues. So, one processor can be applied across multiple FPGA devices from different vendors in different projects.

"We think reprogrammable hardware will be a driving force over the next decade," said Klaus Pontius, European director of support at Altium. Unlike other processors for FPGAs such as Altera's Nios and Xilinx's MicroBlaze, the

anDisk 2

TransFlash

Pontius. Actel.

Tiny memory package hits big industry

Candisk has developed an **O**industrial version of its miniature TransFlash flash memory card with 256MB of storage. The original version was developed with Motorola for smartphones, but demand from the industry has led to an industrial version, necessary for applications where space is an issue and designs want scalable memory, where more memory can

connector. bits in each cell.

Technology

TSK3000 comes pre-synthesised and pre-verified. "We want to remove the barrier of VHDL or Verilog while allowing experienced designers to use HDLs if they want," said

Providing pre-synthesised IP means there are different versions of the core available for each of the main FPGA lines from Altera, Xilinx and

be added later using the same

The TransFlash package measures 11x15x1mm and is a third the size of current SD cards indeed, an SD card is used as the mechanical

carrier to link TransFlash to a PC. The current density is

256MB using Sandisk's 90nm NAND flash memory technology that stores four

The UK-based BTG is seeking an exclusive licensee for a technology on transparent cathodes in polymer organic light emitting diode (OLED) devices. The technology is based on US Patent 5,955,834 titled Light Emitting **Devices Utilising High Work** Function Electrode. BTG licensed it from the Ohio State University covering OLED technologies in the field of information displays. Now, it wants to license it to one OLED manufacturing company. BTG has already invested funding. equivalent to that of a seed-stage round by a third party investor. 0

Recent research from the UKbased City & Guilds has identified that many businesses find it difficult to cope with work placement schemes and are calling on the government to provide more support. The research states that 71% of UK businesses helieve there should be stronger government support to improve the current schemes. **Businesses also want tax breaks** to help them prepare the young for the workplace, better dialogue with schools and colleges, and stronger guidance on how to develop and run effective work placement schemes. However, up to a quarter of the questioned claimed that they've never found a way of making a work placement scheme successful.

O

A new Lean Manufacturing Initiative has been launched in Scotland to help local manufacturers. It aims to aid manufacturers in cutting costs. ncreasing quality and improving the bottom line. The initiative promises to save an average £150,000 in the first 12 months for each participating company, Other specialist advice on manufacturing best practice models, training opportunities as well as encourage networking and communication will also form part of the programme.

The main funding comes from the Scottish Executive and is delivered via Scottish Enterprise by the Society of British Aerospace Companies

CMOS process combines **logic and 30V transistors**

▲ nalog Devices (ADI) has Adeveloped a new chipmaking process that combines 30V devices with logic standard CMOS for the first time for industrial applications in noisv environments.

Traditionally, high voltage devices are built on 2µm to 3µm specialist processes such as bipolar, which limits the amount of logic that can be integrated onto the chip. Another way is to combine high voltage and standard CMOS die in the same package, which can be expensive.

In comparison, the iCMOS (industrialCMOS) process developed at ADI's plant in Limerick, Ireland, is a standard 0.6µm CMOS process that isolates the high voltage devices with wells of silicon dioxide. To date, the difficulty in building such devices was in developing a process that had both the wells for the 30V isolation and the 5V CMOS



devices, while keeping the area to a minimum for competitive reasons. Another issue was developing the modules for on-chip components such as capacitors.

Now the thickness of the wells can be varied, depending on the mix of devices needing isolation, and this is used in different process modules with different combinations of devices for various applications.

As such, 30V vertical bipolar transistors can be used alongside digital signal

Comparison in chip sizes when created with 30V.1um 24V and iCMOS processes

processing vertical CMOS transistors in different ways for data converters, switches and amplifiers.

The higher voltage gives larger input swings for analogue to digital converters (up to +/-10V), greater linearity for higher accuracy digital to analogue converters (up to 16-bits with 1 LSB), multiplexers with R_{op} of 3 Ω , 85% lower than previous devices. and amplifiers that are 60% smaller. ADI has launched a range of parts using the technology, including a

1MS/s, 12mW ADC with 8 +/-10V inputs that use standard logic to make them software selectable, rather than having to use a network of resistors to select the inputs.

As the process is in standard CMOS with different 'flavours' for different combinations of devices, it scales down to 0.25µm lithography and allows analogue devices to take advantage of the lower power and lower costs driven by Moore's Law, for the first time. The silicon dioxide wells may be relatively larger to provide sufficient isolation and reduced leakage current, but that is only for the high voltage devices that tend to be at the input or output of the chip.

As well as reducing the feature size to reduce the power consumption and cost. the company is also looking at a 50V version for even higher signal swings.

New touch for harsh environments

Because

the touch-

screen is a

standard

piece of

new kind of touch screen Atechnology that can be used on bigger screens and in industrial environments is now available from 3M.

The Dispersive Signal Technology (DST) measures the vibrations created in a sheet of class when it is touched. There are four piezoelectric sensors at the corners of the glass overlay on the screen, and a digital signal processor (DSP) uses this data to calculate the position of the touch. This means that the touchscreen can be used with gloves and

in rugged environments where the capacitative and resistive approaches are not so reliable. The current algorithm gives 1% accuracy.

3M demonstrated a 40in glass, it can also be used LCD with a DST touchscreen at Electronica in Germany for in a speaker. the first time in Europe. It is planning volume production has teamed in 2005. At the same time, it up with flat is evaluating the DSP used speaker for the screen, said Doug maker NXT Keller, product manager, with to integrate the performance of the DSP a speaker behind the glass. This means depending on what features they want to add to future the DSP has to filter out the products. vibrations created by the



The Dispersive Signal Technology (DST) touchscreen makes an appearance at a trade show

speaker when analysing the vibrations created by someone touching the screen.

DVB-H mobile TV silicon



Ceveral chipmakers are Odeveloping silicon for the new DVB-H (DVB-Handheld) standard that allows TV to be broadcast to mobile terminals such as mobile phones and personal digital assistants (PDAs).

The first to market is DiBcom, a Paris-based chip design firm. "As DVB- H is very close to DVB-T [DVB-Terrestrial], just adding the 4K mode, forward error correction and time slicing - so the design and development is guite straightforward and the DVB-H chip will benefit of the same advantages concerning portable and mobile performance," said Gerard Pousset, business development manager at DiBcom.

The company has demonstrated a laptop PC using its DIB3000-MC 2K/8K COFDM demodulator chip and a SmartMPEG chip from Fujitsu Microelectronics. With two antennas on a vehicle and the more complex 64QAM modulation, data rates can go up to 24Mbit/s at 250km/h. With a single antenna, the chip supports 16QAM modulation, with data rates of up to 18Mbit/s at up to 150km/h.

February 2005 ELECTRONICS WORLD

DiBcom demonstrates its DVB-H chip capabilities

The next step is to have a more cost-effective 4K version with 3409 active carriers specifically for DVB-H. The challenge after that is its integration into mobile phones.

UK silicon design provider Imagination Technologies is using its Universal Communications Coprocessor (UCC) multimedia processor core. which is also used for DAB chips and Digital Multimedia Broadcast (DMB) terminals, for its version of DVB-H. It will be ready in for terminals at the end of 2005. The UCC, developed by Imagination's Ensigma division, is essentially three processors, each with its own dedicated signal processing task. The Signal Conditioning Processor (SCP) performs IF to baseband conversion, while the Modulation and Coding Processor (MCP) performs data modulation and demodulation. The output from the MCP is a stream of soft decisions suitable for error correction. The data passes through the Error Correction Processor (ECP) before being decoded by the host processor. The DVB-H design also includes the link layer and demodulator for

DVB-H so all that is needed is a separate RF tuner chip and an applications processor to handle the video decoding. This allows the existing applications processor in a phone to be used. The designs will be ready by the end of this year. says Simon Hambly, mobile TV product manager at Imagination. "There's a great deal of interest in the solution." he said Texas Instruments will add

DVB-H capability to its DSPbased multimedia platform OMAP. It is a new single chip codenamed 'Hollywood' that combines the RF receiver. tuner and demodulator. Evaluation boards will be available at the end of 2005. samples in 2006 and full production will start in 2007. Philips Semiconductor aims to have a chip in the market early next year, as it plans to have terminals ready by the year-end, says Steve Turner, business development manager for consumer and multimedia products. It is working with Nokia on the trials in Oxford and Berlin and has demonstrated a tablet PC receiving DVB-H in Singapore.

Technology



Anti-Moore's Law

- Get rid of the classical Von Neumann microprocessor architecture
- Use only flexible and fast parallel architectures
- ► Create software 'washing' machines to reduce power
- ▶ Explore optimised memory hierarchy
- ▶ Introduce parallelism it's better to use 20 processors at 100MHz than one at 2GHz
- ► Exploit dynamic nature of algorithms to adapt VDD, fcl, IDDQ of processors
- ▶ Use tile-based GALS (global asynchronous, local synchronous) architectures with regular networks on chip
- ► Use error correcting communication techniques for networks on chip
- ▶ Create efficient software (co-design)
- ▶ Close the gap between system software and platform architecture including the programming environment, mixed-signal and even the RF link

This month's Top Ten Tips were extracted from a Medea+ lecture given by Professor Hugo de Man of the University of Leuven and cofounder of the IMEC research facility in Belgium. For more information see News Story on p6.

If you'd like to send us your top five or top ten tips on any subject you like, please write to the Editor at

EWadmin@highburybiz.com

Technology

Silicon on Sapphire moves into the mainstream

Peregrine Semiconductor is pioneering the use of sapphire substrates with standard CMOS process technology that tackles one of the largest problems in today's chips - leakage current. The fully depleted 200Å layer of Silicon on Sapphire (SoS) used in its UltraCMOS process has an immeasurable leakage current, says Rodd Novak, director of marketing at Peregrine. "It's less than a picoamp," he said.

This gives much higher isolation for higher voltages and higher swings, as well as letter linearity for RF elements such as phase locked loops



Bulk CMOS process versus the Perearine Silicon on Sapphire solution

and tuners. The company has just launched a 75Ω switch for cable TV boxes that provides

isolation of 70dB at 750MHz and ESD tolerance of iKV even in a non-powered state.

By combining two different nchannel transistors, the PE4274 switch can still pass current through the device at 0V, allowing other equipment, particularly games consoles. to be attached to the cable TV box and still operate even when the box is off. This level of isolation is only possible with SoS, says Novak.

The company, which has its own 6-inch fab in Australia. also has a deal with Oki Semiconductor, which is using the technology in two fabs in Japan for low power devices, as well as using it in its design centre in Provence, France.

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- Self Powered USB Interface no external PSU required
- 3rd Party application software support provided
- Hardware upgradeable over USB

The world of the telecom equipment makers is changing yet again, and now to enquif AdvancedTCA, says Fred Yentz

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he telecommunications industry today is beginning to seriously evaluate Advanced Telecom Computing Architecture (AdvancedTCA) compliant products. Acceptance of AdvancedTCA and the proliferation of solutions that conform to the standard is the result of work conducted by PICMG (PCI Industrial Computer Manufacturers Group), a consortium of more than 450 companies who collaboratively develop open specifications for high performance telecommunications and industrial computing applications.

In the late 1990s, the telecommunications industry was booming. This was also a period when the market was defined by infinite cash and an overabundance of opportunities. Acquisitions, mergers and takeovers were also rampant and left in their wake a plethora of proprietary platforms for organisations to manage. It didn't take long to realise that a new standard was needed to allow for common, modular platforms.

PICMG was maturing as a standards body and was, for the first time, joined by many of the industry's largest Telecom Equipment Manufacturers (TEMs). With more than 100 participating companies, PICMG set out to develop a new standard for next generation carrier grade communications equipment. The driving force were a more robust architecture, larger form-factors to accommodate more processing power and a consolidated view on management due to the parallel efforts of the Service Availability Forum (SAForum). Additionally, a new

standard would provide TEMs with more choice. AdvancedTCA was the promise of interoperable blades.

For users, it held the promise of better

interoperability, scalability and serviceability, which would lead to accelerated deployment of next generation services and ultimately improve time-to-money. As the AdvancedTCA specification matured, the industry began one of the largest corrections of all time. A precipitant drop in revenues and available cash. combined with enormous debt, resulted in a drastic transformation of the industry. The shakeout created a market that had been completely redefined. In this time of recovery, many TEMs focused their limited resources on quick upgrades to network elements and system boosts. These were small tweaks that offered incremental increases in performance

and function.

As TEMs adjusted to a renewed focus on return on investment and core competencies, AdvancedTCA offered

etary platform.

solutions. It would allow TEMs to spend critical resources on developing feature-rich applications and services rather than building the next compute or switch blade for their propri-

Even though TEMs improved some of their older network elements with speed and application adjustments, many of the architectures and platforms were in need of a significant refresh. Upgrading this variety of legacy platforms with fewer people due to massive downsizing was a monumental task. The most probable solution appeared to be AdvancedTCA.

It didn't take long for the industry to appreciate the value in a strong ecosystem made up of suppliers that provide both, AdvancedTCA-compliant building blocks and common platforms.

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Insight

GOOD architecture with great timing

Today, the world of interoperable solutions has opened up. Many AdvancedTCA-compliant solutions will be in test environments in 2005. However, once these solutions proliferate, TEMs will be faced with integrating different building blocks, from different vendors, to form complete systems. This will require significant time and resources, which are both in short supply. TEMs will need to rely on vendors to handle the integration and validation of various components, from a variety of suppliers and trust that they will deliver proven, tested, application-ready platforms.

TEMs may view this as a risky endeavor and be apprehensive to give up functions they have traditionally managed - in finite detail, to a new group of market and technology participants. Many will need to step up to the chal-

I TEMs may view this as a risky endeavor and be apprehensive to give up functions they have traditionally managed

lenge by hiring the best system architects and validation engineers, and investing in laboratories and equipment. Suppliers must become expert system architects, provide unequaled service and manage lifecycle and supply chain management functions with a keen eye on customer ROI.

AdvancedTCA was the brainchild of several movers and shakers in the telecom industry. The standard has matured through the telecom depression and emerged as a stable architecture with a strong ecosystem of technology companies, several of which have stepped up to the challenge of providing applicationready platforms.

Fred Yentz is services vice president at RadiSys and is based in the US.

Second hance

Regrouped and with a sharpened focus, ARC International hits the market place with a line-up of new platforms

By Svetlana Josifovska

RC International, the UK-based creator of reconfigurable microprocessor cores, is trying to turn its fortunes around. To achieve this, the firm has acquired new management and is launching a series of pre-configured platforms for key markets based on its cores.

The firm has been losing money for several years now. In its June 21, 2004 announcement of its results, ARC showed turnover of £10.7m and net loss of £20.7m, which increased 1% on the same period the year before. "ARC has not been a profitable company," confirms Derek Meyer, the firm's vice president of sales who joined it only a few months ago and used to work for MIPS Technologies, one of ARC's rivals. "The goal [with the new management] is to grow the company's profits."

Carl Schlachte is ARC International's new CEO. He joined in March 2004. With him, he brought a series of high-flying executives with technical and commercial background that has been trimmed at successful companies like ARM, MIPS, Texas Instruments and



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Cadence among others.

The management immediately divested the USB business that ARC acquired some years ago to re-focus solely on the firm's core competency that is reconfigurable processors and supporting tools. ARC still offers its range of highly flexible microprocessor cores. The code for these is delivered in C so that application designers can tune it to fit their requirements. They can modify the instructions sets or the memory configurations, unlike with ARM processors, for example, that offer fixed functions.

ARC's management also plans to keep the MQX realtime operating system (RTOS) that is used mostly in industrial applications. ARC acquired MQX when it bought Precise Software Technologies in 2000. This RTOS supports ARC and non-ARC processors.

What ARC is offering in addition to these solutions is a series of pre-configured licensable platforms for volume markets such as consumer electronics, for example.

ARC was formed in 1998 when it de-merged from the UK games and graphics chips developer Argonaut Software. Back then, its CEO was Bob Terwilliger, who when first saw what ARC can do said it was like spotting "diamond sparkling in the coal". Terwilliger left the company at the end of 2001. Since then the firm drifted. "On the business side, the company didn't bring people in from ARM and MIPS and others. They [the management of the day] didn't know about [the business of] CPUs and operating systems."

Even though it slipped off many customers' radar screens, Meyer says that ARC was still the second largest selling processor in 2004 with nearly 100 million units shipped and 100 licensees. The full potential of these licences, however, is yet to make an impact on ARC's balance sheet.

The number of registered configuration variations on the ARC 600 currently stands at 3600. "There's a strong correlation between configurability and high volume," said Maver.

Recent agreements with TTPCom and Broadcom will get the company further into the mobile phone market. "Broadcom already has an ARM and MIPS license but now they are taking an ARC licence, too. TTPCom will need it for their 2.75G baseband. This should put us in

even higher volumes," said Meyer.

ARC's portfolio consists of several configurable processors such as the Tangent-A4, Tangent-A5, ARC 600 and ARC 700. The ARC 600 and ARC 700 are 32-bit RISC processors that are available with or without DSP extensions - dual 16-bit or 24-bit multiply/accumulate/subtract. In addition, ARC 700 runs Linux, as well as other embedded operating systems (OS). This core is scalable up to 400MHz.

Users can profile the software programs they intend running on the processor, identify areas of the code that could be accelerated through hardware and add that to the processor. Examples of these types of instructions are bit manipulation functions, which are highly inefficient when handled by software. Speeding them up in hardware can yield improvements of up to 1000 times, depending on the programs and the level of extension used

To make configurability easier, ARC has expanded its ARChitect2 tool with the Extension Interface Automation (EIA) technology. EIA provides a graphical interface with which designers can create a library of processor components. Before the introduction of EIA, customers were given access to the ARC extension interface that is tied into the processor internals. Although this allowed flexibility, it required detailed knowledge by'the user.

EIA simplifies this complexity by allowing the designer to simply describe the function of their extension, which it then automatically connects to the processor internals along with the necessary support logic. It then generates the connections to the processor, including the models of the instructions for software tools, and describes the instruction to the compiler to allow it to be easily used. With EIA, implementation time is shortened from days to minutes.

Extensions can be described in Verilog and System C with which 95% of designers are familiar.

ARC's reconfigurable devices find their greatest fans in the digital consumer electronics, networking and storage applications space. That's why ARC went the extra mile to deliver a specific subsystem that will cut time-tomarket for some of these customers. The first in this series is the ARCsound Audio Subsystem. It consists of audio software, the ARC processor with custom audio extensions and a suite of hardware and software development tools. The total area of the module's footprint,



replaced with Linux if required, says Meyer. The subsystem conforms to MPEG-2/4 audio, MP3, WMA and AC-3 standards and uses a library of all the codecs. As Meyer says: "use them or don't use them, but they are there."

next level in our [IP] industry. Audio is the first step. Derek Mever, VP of sales, ARC International

and software, whilst competitors' [similar] platforms do not offer the software side of it, just the processing and the [audio] extensions. The "Pre-configured sub-systems are

Pre-configured sub-systems are the "Our solution includes hardware software is 'third party'," he added. the next level in our [P] industry. Audio is the first step the key is to fully understand which [elements] you need to deliver for a series of media related subsystems." The firm is planning other platforms, which, it says, will launch at the target market's "sweet spot". After all, application-specific solutions can generate three times more revenue than microprocessors alone. Building a pre-configured system - with certified software - will carry a greater premium, says Meyer.

So, what's next for ARC? "We'll need another range [of configurable processors] above the ARC 700 that runs Linux in 0.13µm CMOS implementation."

"The working trend to do is to bring a new microarchitecture every 12 months. But this is a pace faster than the embedded market can handle. You need compilers, software, tools - all sorts of things - to go with it. There are other ways to achieve performance without having to change the microarchitecture. You can do it with DSPs it is SIMD [single instruction, multiple data] based today but it may be the vector-type approach [next], for example."

"Sub-systems will clearly be an interesting business for IP companies."

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Block diagram of ARC 700 processor core

Electronics sheds light on the vision sector

-

With growth that is expected to continue at 20%, 40% and above (European, US and Asian forecasts, respectively) machine vision is providing bright opportunities for the electronics and semiconductor industries, says **Matthew Peach**



t the beginning of the 21st century, the vision sector is clearly transitioning from specialist custom solutions towards offthe-shelf packaged systems that are finding wider application. According to the Advanced Imaging Association, the key markets for vision systems are semiconductor manufacturing, electronics, transport, wood and food processing and pharmaceuticals.

Vision systems are the focus of intense research and development worldwide and the development objectives are bound up in the aims of product and system improvement in the electronics sector. As in microelectronics, vision system companies are working to solve the quintessential high technology challenge: reducing component size and power consumption while driving performance up and price down. At the same time, characteristics of hitherto diverse and disparate vision systems are becoming more streamlined as standards evolve, especially in the fields of communication protocol and connector technologies.

Machine vision (MV) is reaping the benefits from developments in other areas of the PC and electronics industries. Particularly, the 64-bit PCI Express bus specification, which is soon to be released, is a result of the pressure being exerted by the PC gaming industry. The 64-bit PCI Express bus raises data rates to 528MB/s with a theoretical limit of 660MHz dependent on hardware.

US firm Coreco Imaging, for example, has a range of boards: the X64 series, capable of interfacing with this new bus, and which can achieve high transfer rates for existing and new cameras. These boards, in turn, allow the current crop of highresolution cameras to realise their full potential, according to Colin Geer marketing manager at UKbased distributor Firstsight Vision.

The speed of the on-board processors, coupled with the advancing capability of associated software, is pushing many machine vision solutions into areas that were once the domain of "full-blown" PC systems. The latest DVT smart sensor range, for example, uses new DSPs, from the TMS320C6000 Texas Instruments (TI) series, that runs roughly at the speed of 500MHz.

Camera resolutions are also improving. The next generation of cameras is entering the market with 3, 5, 8 and even 22 Megapixel image sizes, with the prospect of higher resolutions yet to come. This is the other side of the same equation. With pixel resolutions reaching these levels, the hardware needs to be in place to manage the data generated, which is where the new interfaces will come into their own.

Image transfer protocols and interconnect technologies are proliferating. The Camera Link standard is an MV-driven protocol that has produced many benefits including far higher data transfer rates, up to 900Mbit/s, and it has simplified what was a confusing cabling situation by putting in place a defined interconnect standard. It includes standardised interconnects between cameras and frame grabbers and it is based on National Semiconductor's Channel Link LVDS (Low Voltage Differential Signalling) chipset for data transfer.

The other key communications protocols PC-toperipheral interconnect standards are Gigabit Ethernet, FireWire b (IEEE-1394b) and USB 2.0. These technologies are built on established PC industry standards and take advantage of the general impulse to increase the speed and simplicity of PC peripheral connection.

FireWire has been used in machine vision for some time now and there are many manufacturers of 'industrial' FireWire cameras, including Sony, Allied Vision Technology and Unibrain. These cameras include resolutions from standard CCIR/EIA up to 8 Megapixels. FireWire interface cards are available to cater for the machine vision market specifically in both the original and b versions.

USB 2.0 is also a method of connecting peripherals to PCs to enable data transfer rates of up to 480Mbit/s for devices such as external hard disks, video and printers.

This standard is being adopted for use in MV and there is a range of new products arriving on the market, such as the uEye. This camera range also demonstrates one of the other trends in the machine vision world for size reduction; the uEye has a physical size of just 25x25x20mm (the lens mount increases it to 25x25x32mm).

Gigabit Ethernet (GigE) is another technology that promises a revolution in device interconnection by using standard networking hardware and routing technology. Several manufacturers are already targeting the Gigabit Ethernet sector. Japanese-Danish cooperation JAI/PULNiX has several GigE cameras in the pipeline, saying it sees GigE as "an important future strategy". Another large camera manufacturer, Dalsa, also has a number of GigE products that are likely be released in the next few months, in addition to its Camera Link-to-GigE converter that is already available.

So how is electronic component integration occurring in MV systems? Terry Guy, marketing manager in Kodak's Image Sensor Solutions division says: "This trend toward a two-chip CCD solution continues with combining AFE, TG, and horizontal and vertical clock drivers into one device. Our KAI-0340 CDU employs an Analog Devices's AD9995 integrated analogue front-end (AFE) and timing generator (TG). This arrangement significantly reduces the size and complexity of the design by taking the specialised timing circuitry into the AFE."

Faster image transfer

German firm Baumer Optronic's new image processing sensors' improved processing speeds are being attained using the Baumer's own FEX (Feature EXtraction Processor) technology. FEX integrates image sensors, a lens system, illumination, the FEX pre-processing step, a microprocessor and industrial interfaces (I/Os. Ethernet, CAN and others). The 'pre-processing' stage uses FPGAs (Field Programmable Gate Arrays) to handle the parallel image processing. Baumer uses Xilinx FPGAs such as the Spartan 3 and Virtex in different versions of the system. Conventional image filters 'feed' the FPGAs with data to calculate the description of the objects and their characteristics - so called feature extraction - in real time. Once the image capture is complete, the data is then handled by a microprocessor. Most recently Baumer started



Opposite page:

Baumer's FEX-based smart vision sensor usesFPGAs for parallel image processing tasks

Vision

Below:

National Instruments's PCI Express frame grabber, PCIe-1429, uses the Camera Link standard. The board itself can acquire data at up to 800MB/s

17

Vision

Diagram of Pleora's iPORT IP device driver operation



using MicroBlaze, an embedded 32-bit RISC soft core from Xilinx that is Virtex compatible.

A new generation of smart vision sensors now becomes "plug and play", where the user does not have to define specific properties of the objects for inspection – such as smaller image details or fixed grayscale thresholds.

Camera design

Kodak's Terry Guy says that there are several notable areas in MV camera development. "Emerging new sensor package options, notably chip-scale packages for image sensors, will significantly reduce overall system size and cost. Image sensor subsystem elements are increasingly being integrated into multifunction ICs; high performance, economical embedded computing options can provide additional functionality without increasing size.

Japanese giant Sony reports that its MV camera customers are requesting smaller and smaller cameras for integration into space-limited systems such as automation and medical applications. These demands are linked with lighter cameras.

Mathieu Forget, Sony's product marketing manager, Europe, says: "With analogue cameras, we can consider that a kind of size limit has been reached with our current ultra compact XC series models. Our new digital 1394b-compliant platform will show a further reduction in the size from the previous generation cameras; it measures just 44x29x57mm. And our new digital Camera Linkcompatible cameras are the smallest in the market." At Vision 2004, Sony showed a prototype of smart camera that will bring an elegant, compact, all-inone solution to the company's portfolio.

Canadian company Pleora Technologies is integrating its iPORT IP engines that take imaging data in any format and convert it to IP packets for realtime delivery to PCs over standard GigE networks. The PT2000-CLM IP 'engine' is designed for highbandwidth vision applications that send imaging data to PCs for immediate processing, such as high-speed inspection systems used by manufacturers of flat panel displays and semiconductor wafers. The 'engine' streams Camera Link data at 200MB/s over standard GigE connections.

Marketing manager Wendy Doyle says: "Many camera manufacturers are integrating our IP engines directly into their cameras to create GigE cameras. Others are using the boxed versions of our IP engines beside their cameras. In either case, speciality connectors, such as Camera Link and LVDS, are no longer required. This approach reduces the cost and complexity of vision systems."

"At Pleora, we think Camera Link, LVDS, USB 2.0 and 1394b will ultimately be replaced by either GigE or its next generation successor, 10GigE. The Automated Imaging Association's GigE Vision Standard committee will soon release the first version of its standard, which will feed the already considerable market momentum for GigE connec-

ELECTRONICS WORLD February 2005

tivity in vision systems."

The protocols Camera Link, USB 2.0, FireWire and Gigabit Ethernet are bringing to a close the age of large connectors and bulky cable assemblies for vision systems. All of these interfaces share a common trait: the parallel data from an image system is serialised and sent at a high bit-rate over a modest number of wire pairs. The availability of highly integrated and high volume ICs to accomplish this serialisation/deserialisation process has made possible this change, and interfaces like these are likely to continue increasing in performance and decreasing in size and cost.

ASIC vision

The increasing costs of ASIC design make such devices practically cost prohibitive in MV systems in all but high volume products or the highest performance products, where cost is no object. For modest volumes, the off-theshelf availability of imagingoriented digital signal processors (DSPs) can provide a high level of functionality at a reasonable development LAN cost and power. The cost of FPGAs is coming down at the same time that their capabilities are growing. Therefore, implementing imaging functions in an FPGA, with or without a DSP, can be a good option as well.

National Instruments (NI) says that dedicated ASIC design for MV applications has become less and less common as FPGAs gain in popularity. The company points to a 2003 survey by UK firm Celoxica, the "Survey of System Design Trends", which says that system designers use FPGAs three times more often than ASICs. "With the release of NI's LabVIEW FPGA, our in-house designers and customers can reconfigure and customise FPGAs to fit their application," says vision product manager Kyle Voosen.

Four years ago, NI worked with camera manufacturers and other image-acquisition hardware providers to develop Camera Link. Even though Camera Link specifies transfer rates up to 680MB/s, most Camera Link image acquisition boards were based on the PCI bus, which provides about 100MB/s of bandwidth. Camera Link's full potential has finally been realised with the introduction of PCI Express.

Although PCI has enjoyed great success, it now faces a series of challenges, including bandwidth limitations, host pin-count limitations, lack of realtime data transfer services such as isochronous data transfers (where data is delivered within certain time constraints), and the lack of features required for next-generation I/O requirements, such as quality of service, power management and I/O virtualisation. As PCI clock frequencies have become inadequate in certain applications, the PCI derivates such as PCI-X and Advanced Graphics Port (AGP) have sought to provide bandwidth relief by increasing bus frequencies. Another proliferating connection protocol is highspeed USB (or USB 2.0), which has recently been added to the portfolio of Matrix Vision's camera

around 400Mbit/s.



range. By the introduction of the USB interface, the integration of new components in existing systems has been revolutionised, the company claims. USB 2.0 achieves data transfer rates of up to 480Mbit/s, at least as fast as the Firewire/IEEE1394 interface, which is typically

At the recent Vision show in Stuttgart a lot more technologies suggested that we are far from exhausting the range of possible machine vision solutions. The exhibition stands were groaning with possibilities and the potential applications were mind-boggling: adaptable illumination to differentiate components of similar colouring (Vision Light Tech from the Netherlands), economical video cameras to fit into mobile phones (Philips from the Netherlands) and vision systems to recognise the driver of a car and adjust the seat accordingly (Anafocus from Spain) are just a few. But wherever the industry heads next it will be inextricably wedded to the developments in the supporting electronics, materials and software. Undoubtedly, the machine vision market is definitely one to keep an eye on

Pleora's iPORT IP The driver streams image data into the PC using only a small fraction of the CPU. The 99% of its capability is available to support vision processing.

Vision

Biotechnology



Christopher MacLeod discusses the new advances in biotechnology that could lead to innovative devices

-111-

e are living in the midst of a quiet revolution. It's a revolution that's every bit as important and profound as the one in microelectronics. However, because it

hasn't started to affect our daily lives just yet, most of us are scarcely aware of it. It's a revolution in biotechnology.

In the last few years, scientists have discovered how to manipulate and fingerprint DNA - the very core of life itself. It can now be changed and reintroduced into other organisms, effectively creating new species of plants and animals. We have even mapped the human genome and cloned animals from adult cells - until recently the subject of science fiction. Development is proceeding at a breathtaking pace.

This technology more than any other will change our lives in the 21st century, mimicking the growth of electronics in the 20th. However, that change will only happen when biotechnology unites with our other great technological achievements - computing and nano- and micro-electronics. This article is about one way that might happen.

Wetware

At the moment biotechnology is still 'wet', done in laboratory test tubes by skilled technicians. The next stage of its development is to integrate it with the power of electronics and computing and move it out of the lab and into industry, the doctor's surgery and even the home - for it to become bioelectronics.

But, there is a practical problem. Up until now, biochemists and engineers have been living in their own separate worlds and their paths have seldom crossed. This means that there is a lack of communication and understanding between them. They, effectively, speak different technical languages and use different concepts, and very few people are trained in both disciplines. To understand how integration can take place we first have to understand the technology and what it can do.

The chemistry link

Our bodies, like those of all other organisms, are made from cells. Each cell is a living chemical factory. It takes raw materials from the outside world (air, light and water in the case of plants, and various foods in the case of animals) and manufactures complex products from them such as skin and hair, for example,

Each cell works in the same way. It has a built-in code - the DNA, which is continually being read by another chemical, called RNA. RNA, in turn, goes to make the chemical workhorses of the cell - the proteins. Figure 1 illustrates the process. It is the proteins that are the most important part

ELECTRONICS WORLD E February 2005

of the system. They do all the work in the cell: making new material, breaking up old and sensing and signalling changes in the cell's environment.

All proteins bind to other chemicals. Some synthesise new molecules by joining their component parts together or by breaking them up. Such proteins are called enzymes. They manipulate chemicals at the atomic level (Figure 2). The atoms that make up the protein have a particular physical shape, which is so precise that only the correct target chemical can fit into it. Often the shape is a type of "grove" in the atomic structure of the protein. Enzymes that synthesise new chemicals work by letting two simpler molecules attach to the protein in such close proximity that they bond together to form a polymer. This process allows the synthesis of highly complex and useful chemicals, which could not be made any other way because of the high energy and difficulty involved in forming the honds

Those which break down chemicals do the opposite, allowing a molecule to bond and then breaking it apart is shown in Figure 3.

Both this and synthesis are often helped by the thermodynamic movement of the protein or by a third chemical attaching elsewhere on the protein, which changes its shape, so ripping apart the bound molecule. Commonly, this third chemical is a substance that contains a "high energy" bond - one that has the capacity to release a large amount of energy when broken. The most common substance with this ability is called ATP (Adenosine Triphosphate). Figure 4 illustrates the idea.

Making electronic proteins

Since proteins are the key to biological systems, all sorts of possibilities open up if we can work out how to make controllable, artificial, ones. The logical way to try and do this electronically is on a silicon wafer. In theory, we could make binding sites on a chip as shown in Figure 5. The trouble is that the atoms that make up the binding groves of real proteins are far too close together to be fabricated using standard photolithography. Atom diameters are measured in angstroms (10⁻¹⁰m), whereas we can only routinely fabricate features of tens or hundreds of nanometers (10⁻⁹m).

However, there is hope and it's coming through research in the new science of nanotechnology. Already scientists have used Atomic Force Microscopes to manipulate and re-order the individual atoms of a silicon wafer - even 'writing' words with single gold atoms. Such technology is presently highly experimental and expensive. Only time will tell whether it becomes commonplace or not (or indeed, if it does, whether it's accurate enough to create active artificial proteins).







Biotechnology

Biotechnology





Fortunately, there is another alternative. We can combine existing protein chemistry with current electronics to produce a hybrid technology. It is perfectly possible to produce short lengths of protein molecule (called polypeptides) in the lab. These are too short to be used for much practical biochemistry, but exactly what is needed to produce bioelectronic chips.

The idea is illustrated in Figure 6. Here, the polypeptides are shown in-situ, on a chip. They can be bound to the chip by electrostatic forces between the atoms of the polypeptide and the pads of the chip (not shown). The geometry of the pad ensures that the positioning is correct and that different polypeptides can be assembled (by adding them at different times) and simultaneously placing the appropriate charges on the correct pads.

By monitoring the charge on the pads, we can see if a molecule has bound to the active site. By changing the charge we can alter the configuration of the polypeptides to act like an enzyme - splitting or synthesising the attached molecules. This may need the addition of bound metal atoms, to act as electroncarrying intermediaries in the system, a trick which nature herself uses in real proteins. Alternatively, the binding of another "high energy" molecule like ATP could change the configuration of the polypeptides. The simple formation of many thousands of pads and therefore sensors on a chip means that not all of them have to be successful for the chip to function.

Interesting applications

22

There are many obstacles to overcome before we can finally fabricate such systems successfully. Apart from the fabrication of the silicon and the synthesis of the polypeptides, we also have to provide an on-chip environment to ensure that the organic molecules stay in one piece once assembled. This means a pH-, contaminant- and temperature-controlled environment, which can prove a real challenge. However, the various pieces of technology are now in place to start experimenting with such systems.

And the applications are endless. Perhaps one of

the most obvious is in sensing. If we can synthesise binding sites for different chemicals, we can detect their presence by measuring changes at the anchoring pads. In theory, this would allow us to sense the presence of substances at molecular level. Obviously, such sensors could have many applications in environmental monitoring and medicine, particularly in the interface between man and machine.

A step beyond this is changing the configuration of the polypeptides by changing the electrical conditions at the pads or by bonding another chemical to the system. An application is the breakdown of unwanted substances into shorter chains. In this case, the substance binds to the assembly and a change in configuration brought about by changing the charge on the pads or binding rips it apart as explained before. The elimination of pollutants and production of hydrogen and oxygen from water are two examples.

Synthesis is the opposite of this and is probably more difficult to achieve. However, it's also the application with probably the most potential. It could allow us to make artificial versions of natural materials that are currently beyond our capabilities like skin or spider's silk (which is incredibly strong).

In the longer term, perhaps the power of ATP or similar "high energy" molecules could be harnessed to produce power for small machines in an analogous way to its use in living organisms, for example by "burning" carbohydrates. One can even envisage a time when we abandon the clumsy internal combustion engine for more biological forms of power (engines might end up looking more like bagpipes). After all, if a horse can get through the day on a few mouthfuls of oats and a human on a plateful of sandwiches, why can't we devise engines similarly capable? In the very long term even systems like fusion power might yield to a similar approach.

The final application worth mentioning is the manipulation of DNA itself (as well as the other chemicals of life). This could allow us to sequence and analyse DNA on chip and, perhaps, in the long term, even synthesise custom drugs in the surgery.

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In the mood for music? You will be with Mission's latest "mood-adapting" home theatre system, M-Cube. The 5.1 system consists of five individual cubed 'satellites' and a sub-woofer (with 250W amp and twin 8" drive units) that can be either mounted on the wall or standalone. The system comes with different colour fabric strips that wrap around the speakers to complement modern interior colour schemes and "match your mood", says Mission. "Never before have we dedicated as much time and development to how a product looks as well as how it sounds," said Jean-Marc Galiana, Mission's CEO. It uses DML (Distributed Mode Loudspeaker) engineering to create an even spread of sound throughout the entire room. From £1199, available from selected dealers

www.mission-cube.com

The latest in the Sanyo range of voice recorders is the ICR B170 device that doubles up as an MP3 player and data storage system. It is the first digital product to use an advanced built-in stereo microphone for high quality MP3 recordings. It can also play back WMA music. It stores data files directly from the PC, since it offers 64MB of memory.

No need to shout, says Nyko, the US firm that has developed SpeakerCom for the Xbox games console. It has an in-built speaker and microphone, it plugs straight into the Xbox controller and enables groups of people to talk to each other online, unlike the headsets which are limited to one-to-one conversations. The SpeakerCom is wireless and comes with volume control. As the controller powers it, there's no need for batteries or separate power sources. From £19.99 from Nyko distributors www.nyko.com

Gadgets



The ICR B170 can record over 8.5 hours mono and over four hours of stereo sound. By connecting it to the PC, files like Word, PowerPoint and Excel, and emails can be stored and carried around with it. The device allows discreet recording and listening of confidential information.

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Demanding performance from data conversion

Adrian Grindon of Future Electronics Europe gives a detailed overview of how to ensure the best performance from an ADC or DAC

n automotive electronics, particularly in an automatic breaking system (ABS) or electronic stability programmes (ESP), the quality of analogue and digital data conversion could literally mean the difference between life and death. Any delayinduced sluggishness or inaccuracy will reduce the ability of the electronics to safeguard the vehicle's occupants under emergency conditions. Although this is an extreme example, it does illustrate how data conversion quality can impact the end-performance of a digital, microprocessorbased application that is used to interface or control analogue electronics.

Conversion quality is ultimately dictated by the quality of the analogue to digital converters (ADC) and digital to analogue converters (DACs) used, and the supporting components and technical design employed in the signal chain.

Cost is also an issue as maximising quality within the commercial confines of a development. Product budget means looking for components that offer the best cost-performance value. In addition, understanding common sources of error in terms of layout and noise issues and other technical pitfalls will influence the efficiency of a design and the quality (thus cost) of associated components required.

This article will examine the most common sources of error found within ADCs and DACs (collectively referred to from now on as ADCs). We'll refer to sample devices from Microchip and National Semiconductor. Several sample application circuits will be discussed in detail.

It will also give advice on how to 'read between the lines' of datasheets to spot any obvious performance question marks.

Sources of error

Figure 1: Ideal A/D transfer characteristic

Analogue and digital conversion errors are best sub-categorised into direct current (DC) and

alternating current (AC) related errors. DC errors fall into one of four categories: quantisation errors, differential linearity errors, integral linearity errors, and offset and gain errors. AC errors generally relate to signal to noise and total harmonic distortion (THD) issues.

Quantisation is the most basic error. As illustrated by the simple 3-bit converter shown in Figure 1, input voltages are digitised into one of eight discrete levels represented by codes 000 to 111. Each code spans a voltage range of Vref/8 (for an n-bit converter this is calculated by the sum Vref/2n). The code size is generally defined as one least significant bit (LSB). If we assume that Vref = 8V, then the voltage change between each code would represent 1V. This means there is an error between the actual voltage giving rise to a specific code and voltage represented by that code. Usually, small 0.5 LSB offset is added to the input, this gives rise to a quantisation error of +/- 0.5 LSB about the ideal transition point. In the above example this would be +/- 0.5V.

Because Figure 1 shows an ideal converter, its





ELECTRONICS WORLD February 2005

code-to-code transition points are 1 LSB apart. In practical ADCs, however, this is not the case. This gives rise to differential non-linearity (DNL) errors. As illustrated in Figure 2, the transition between codes 010 and 011 has a DNL of 0 since it is exactly 1 LSB. The transition 000 001, however, has a DNL of + 0.2 LSB since it has a code width of 1.2 LSB. If the DNL error is specified as greater than +/- 1 LSB then it is possible that the converter may have missing codes. The code 100 never appears at the output because the converter has a DNL of 2.2 for the code value 101. It should be noted that if the DNL figure is not stated explicitly in the datasheet then it might be interpreted as the converter having 'no missing codes', implying that the converter has a DNL of better than +/- 1 LSB. For example, the Microchip MCP320X 12-bit converter range headlines the +/-1 LSB DNL in the datasheet.





Figure 2: DNL characteristic

system, the effect of a poor DNL may be to cause the system to 'hunt' (continuously oscillate about a setpoint and not settle into a steady condition). It also tends to degrade the signal-to-noise ratio (SNR).

Mathematical integral of DNL

However, it is not always necessary to choose an ADC with a +/-1 LSB DNL. A 16-bit converter with a +/-4 LSB DNL (i.e. 14 bits with no missing codes), for instance, would be adequate for a design requiring 13-bit resolution and could be cheaper than a 16-bit converter that has no missing codes.

Integral non-linearity (INL) is the mathematical integral of the DNL errors. This means an ADC with good INL guarantees good DNL. The INL describes the deviation of the converter from the ideal linear transfer function as shown in **Figure 3**. Manufacturers generally have two different methods of measuring INL, which can have important implications for the designer's 'end point' and 'best fit'.

With the 'best fit' method, a best-fit linear transfer function is derived from the device INL that balances the positive and negative deviations from the transfer function. This tends to yield



better INL figures than those given by the 'end point' method. In order to realise these figures in practice, however, the user must adjust each converter board for gain and offset not practical or desirable for most designers.

Figure 3: INL characteristic

For the end-point method, a linear transfer function is defined that connects the first and last code transitions. The INL is then specified as a deviation from this line. This gives a more conservative result but is more useful to the designer as it gives the worst case INL that can be expected by simply making adjustments to the two end-points. Companies such as National Semiconductor use the 'end point' method. Since neither INL nor DNL can be calibrated or corrected for, they are important parameters to observe when choosing an ADC to meet a specific error budget.

Gain and offset errors also occur within ADC converters but these can be calibrated out using a microcontroller. The offset voltage error is the deviation from the code transition points across all the output codes, usually measured at the first code transition point. It is worth noting that if the converter is to be used in a unipolar scheme, although this error can be calibrated out, it will result in some loss of dynamic range. Gain error defines the deviation of the part from the ideal analogue to digital transfer function. Determining the last code transition point and subtracting from it the value of the offset error can calculate its value. The gain error is also a function of the reference voltage being used, so it is important to note from the datasheet whether an internal or external reference is used to determine the gain error.

AAA

ADCs

Another figure sometimes stated is the total unadjusted error or absolute error. This is a specification of all sources of error, including⁴ linearity, gain and offset errors. It gives the designer a straightforward way of determining if a part will meet a specific error budget without need for further calibration.

Most datasheets will give specifications for the errors listed to allow the designer to choose a part to meet a given error budget.

AC signals

The previous errors are a measure of the DC performance of a converter. If the designer is to specify a part for use with AC signals, then a number of other electrical characteristics must be considered. The key specifications are SNR, signal-to-noise and distortion ratio (SINAD), THD, spurious-free dynamic range (SFDR) and effective number of bits (ENOB). The latter is a specificition that helps to quantify the dynamic performance.

SNR is the ratio of the output signal amplitude to output noise, not including harmonics and DC. There are three components to this quantisation: noise, noise generated within the converter itself and application noise. Quantisation noise is a function of the converter resolution. The noise within the converter is primarily a function of how well the input comparators function. Since this accuracy degrades at higher slew rates, it is worth noting the frequency at which the SNR is defined. The theoretical maximum SNR is:

> SNR max (dB) = 6.02n + 1.76, where n = converter resolution (bits)



THD is an indication of the linearity of the converter in terms of its effect on the harmonic content of a signal. It is the RMS value of the rootsum-square of the harmonics and noise relative to the root-mean-square (RMS) value of a sinusoidal input.

A more useful value to look for in the datasheets is SINAD as this is a measure of noise harmonics and distortion introduced by the ADC. In a perfect converter SINAD and SNR will be the same. It is possible to gain a more meaningful idea of the quality of a converter by converting the SINAD figure to effective number of bits (ENOB), although many manufacturers specify ENOB in the datasheets. The relationship is:

ENOB, as the name suggests, represents the number of bits resolution a perfect converter would have to give the same SINAD. Again, it should be noted that the sampling frequency and test conditions must be specified. ENOB will degrade as frequency approaches the Nyquist rate. A method of improving SNR is to oversample the signal of interest. The noise floor is reduced by 3dB each time the sampling frequency is doubled. SFDR is defined as difference between the RMS value of the desired output signal to the highest amplitude output frequency, which is not present at the input defined in dB. It is important to the designer as it illustrates the minimum signal level that can be distinguished by the converter.

Circuit design issues

Having understood how ADC datasheets define the errors within the semiconductor, it is now important to understand how poor circuit design can cripple converter performance. There is usually the requirement for some signal

> conditioning between the signal source and the ADC. Any resistors used will introduce noise. In order to minimise this, the values chosen should be as low as practical. Figure 4 shows a straightforward buffer circuit. The use of resistor packs should also be avoided, as the capacitance between devices is quite high and this can result in high frequency coupling into the signal path. The capacitance between the output side of the feedback resistor and resistors connected to the positive terminal of the op-amp can cause oscillation. This may manifest itself as a DC offset.

The selection of the op-amp is also important. The specifications of the



amplifier that will influence the system performance will be offset error voltage and the output noise figure. There are other subtle problems that can occur with signal conditioning buffers.

Figure 5a shows a buffer with a gain of 2. There are two potential problems here. First, the input of most sampling ADCs is a switched capacitor load. This type of circuit can output energy from the input pin so it is possible that this will cause the amplifier output to ring or oscillate. A wise precaution is to decouple the output with an RC network as shown in **Figure 5b**.

Second, operating the amplifier with a low gain can make it more susceptible to oscillation. This problem can be highlighted by attenuating the input signal and increasing the gain of the amplifier.

Inadequate power supply decoupling can also result in poor data-conversion performance. When the ADC outputs change state, the output drivers can draw high dynamic currents because they are suddenly driving capacitive loads. This can cause noise in two ways. Firstly, any currents that are sunk by the outputs pass through the substrate of the device (chip ground) and can cause a common mode as this voltage is effectively subtracted from the input when the conversion is made. Minimising the distance between ADC and microprocessor and using a series resistor can limit this

February 2005 ELECTRONICS WORLD



effect.

Secondly, if the outputs source current then these high currents can cause noise on the power supply pin. If the analogue and digital power supply pins are not adequately decoupled then this noise will couple into the analogue circuitry.

A good decoupling scheme

Figure 6 shows a good decoupling scheme for a National ADC12040. Choosing an ADC and buffer with a good PSRR (Power Supply Rejection Ratio) will also reduce this effect (but note that the PSRR degrades with increasing frequency).

The use of ground planes can also be beneficial in reducing noise, although care should be taken to ensure that breaks in the ground plane are parallel to the signal path. The clock used to drive the converter can also

The clock used to drive the converter can also cause problems to the unwary. The first way in which it can reduce performance is by coupling into the signal path, so take care to route it away from analogue signals. A more pronounced effect could occur if the clock has excessive jitter (i.e. it exhibits a cycle-to-cycle variation in duty cycle). This jitter can be caused by the poor layout, incorrect termination of the clock line and poor clock circuitry. It is wise to treat the clock line as a



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Figure 4: Simple

input buffer



Figure 6: Typical decoupling scheme for an ADC

Figure 7: Using a ratiometric technique to null out reference drift



Figure 8: Typical example of a reference circuit

transmission line and correctly terminate it. It is vital to do this if the delay caused by the length of track is greater than 6x the clock rise-time. The delay for FR4 board is typically 6ps per millimeter. This would mean, for example, that with a 2ns rise time, a clock line longer than 55mm must be considered a transmission line and be correctly terminated.

Reference circuit

The final circuit area to consider is the reference. The quality of the reference is fundamental to the system performance as the analogue input is compared against it. The obvious parameters to take note of are the initial accuracy, the temperature coefficient and the output noise. For instance, if the designer requires a 12-bit accurate system to function over a temperature range of -40°C7 to +85°C then a reference of better than 4ppm is required.

One technique that can alleviate the need for very low drift parts is to use a ratiometric measurement as shown in Figure 7. Here, the reference is used to feed the sensor together with the

ADC, which effectively cancels out any drift in the reference voltage as it affects both ADC and the analogue input.

Figure 8 shows a typical reference circuit that may be used to speed up low power ADCs such as the National ADC1175. The reference output is buffered to provide the low impedance drive required by the inputs of the ADC. The value of pull-up resistor is chosen to be low enough to ensure that the reference diode will have low drift over its temperature range.

Beware the pitfalls

Clearly, there are many potential sources of error when designing with ADCs and each can take its toll on the overall performance and cost of an application. Being aware of the common trouble hot-spots, however, means that they can be more easily identified and avoided.

This is crucially important because the impact of data conversion performance on most endapplications and products will have a direct influence on the likelihood of their commercial success.

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he majority of variable costs in a digital display today is the panel itself. For this reason, supply chain management is an important factor in digital display design. Also, there's a growing interest in the

ability to support evolving image processing algorithms and standards to address the needs of different geographies, over time. The goal of supply chain management is to ensure all components in the OEM end-product are procured at the lowest cost and are available to meet demand, while minimising inventory.

The earliest supply chain management decisions are made during system definition. At this point in the design cycle, a decision to proceed with a platformbased display design can reduce procurement costs significantly (Table 1). By supporting multiple panel sizes, OEMs can achieve higher volume discounts from one supplier. By supporting multiple panel vendor specifications, OEMs can create a competitive sourcing situation, which typically leads to lower prices. These two savings more than offset the increase in price due to the additional components required, such as an FPGA, to enable platform-based display design. In addition, multiple vendor support reduces risks to continuity of supply.

To maximise the savings and flexibility provided by a platform-based approach, system designers must select components for the system electronics, based upon the following criteria:

- Graphics processor requirements vary widely by geography-programmable support for multiple standards and formats throughout the world.
- Overall system I/O interface and control logic integration for support of bridging functions from existing designs/ASSP chipsets such as 802.11a or HiperLAN2 and customised user interface logic.
- Field re-programmability support for changing standards and incremental upgrades in image processing algorithms.

Evaluating the components

A key factor in system design is the balance of tradeoffs among CPU/software, ASICs, ASSPs and FPGA solutions, and determining which functions are best served by programmable solutions in a platform-based display design. In general, three circuitry requirements need to be evaluated in the selection of programmable components:

- RSDS (Reduced Swing Differential Signalling) and LVDS (Low Voltage Differential Signalling) support for the panel interface.
- DDR (Double Data Rate) SDRAM support for image processing memory.
- DSP functionality and performance for image processing functions.
- Figure 1 illustrates an FPGA solution that meets

111.

Bart Borosky of Lattice Semiconductives ideas of how to best select an FPGA with DSP functions for digital display de

these requirements. Inputs into the FPGA include a graphics processing chip and other ASSPs such as wireless Ethernet. Outputs include the panel driver circuitry and display timing generator. In addition, the FPGA block in the middle of the figure performs image-processing functions to support multiple panel vendors, sizes and geographical requirements.

For the input section, FPGAs help designers bridge ASSP functions to the graphics processor or system processor. Examples of bridges include wireless Ethernet (802.11a/g, HiperLAN2) and user interface control logic. Next generation displays and projectors may support wireless Ethernet via 802.11a or HiperLAN2, depending upon geography. In addition, customised user interface logic helps differentiate displays from competitors. Both functions are bridged / controlled with an FPGA solution.

February 2005 ELECTRONICS WORLD

over time.

This re-programmable image processing is facilitated by FPGAs that have embedded DSP. Some FPGAs with embedded DSP in the range of below \$10 support over 3,000 MMACs. This is less than 0.3 cents per MMAC - a cost-effective solution for image processing functions. Typically, FPGAs with embedded DSP functions include several blocks of multipliers, but some FPGAs also have embedded adders. subtractors and accumulators that can significantly increase image-processing performance. Although low-cost FPGAs typically operate at less than 300MHz-system clock frequency, the high DSP throughput (3,000 MMACs) can be achieved by performing multiple DSP functions in parallel in the multiple DSP blocks on the chip.

In addition, FPGAs can provide memory control and interface for the image processing frame buffer, which is often DDR SRAM. DDR memories capture data words both on the rising and falling edges of the system clock, effectively doubling the throughput over traditional SDR (Single Data Rate) memories at the same clock speed, DDR SDRAMs are often used for frame buffer memory, in which a large amount of cost-effective, faster speed memory is required to store entire frames for image processing.

Manipulating data

The DM data-masking capability of DDR SDRAM devices is used to simplify the manipulation of data for graphic display applications. Instead of performing READ-MODIFY-WRITE cycles to change part of a wide word, masked WRITE cycles are used in conjunction with the DM mask signals to enable and disable the writing of individual bytes within the wide word. Since the READ-MODIFY-WRITE cycle is replaced with a single WRITE cycle, the benefit to the system performance is obvious. Masked writes simplify changing selected bits in a block of data and increase the performance of tasks such as color management of the display. At lower (100MHz and below) clock speeds, the DDR memory controller interface is straightforward and can be implemented in an FPGA using the general-purpose I/O and logic capabilities. At higher frequencies, however, FPGAs with dedicated circuits are required to ensure a robust DDR memory interface. These dedicated circuits include special routing and DLL-based phase shifting for the DQS strobe,

For the image processing section, FPGAs provide scaling, aspect ratio conversion, colour space conversion, noise reduction and other DSP functions on the video frames to support multiple panel sizes and vendors. Some of these image-processing algorithms, such as sharpness enhancement, can be proprietary and lead to product differentiation, particularly with incremental improvements to the algorithms **FPGAs**

Table 1: Platform-based displa	design lowers	supply chain costs
--------------------------------	---------------	--------------------

	30 inches	32 inches	37 inches	42 inches	46 inches	Total
Price Per Inch	\$50	\$55	\$60	\$65	\$80	\$57
Panel Price	\$1,500	\$1,760	\$2,220	\$2,730	\$3,680	\$1,932
%Discount ¹	2%	2%	2%	2%	2%	2%
Panel Savings	\$30	\$35	\$44	\$55	\$74	\$39
Extra Component Costs ²	\$10	\$10	\$10	\$10	\$10	\$10
Total Savings Per Display	\$20	\$25	\$34	\$45	\$64	\$29
Annual Units Sold	100,000	50,000	50,000	25,000	10,000	235,000
Total Annual Savings	\$2,000,000	\$1,260,000	\$1,720,000	\$1,115,000	\$636,000	\$6,731,000
and the second second	30%	19%	26%	17%	9%	100%

Notes: ¹ Due to competition and volume discounts during procurement

²FPGA cost to support platform-based design

	ctrical characteristi	
Characteristic	RSDS	LVDS
VOD, Output Voltage Swing	+/- 200 mV	+/- 350 mV
RTERM, Termination	100 Ω	100 Ω
IOD, Output Drive Current	2 mA	3.5 mA
Content	RGB Data	RGB Data & Control

DQ data-valid circuits to signal the start of memory READ bursts, preamble and postamble detectors to correctly handle the DQS strobe as it exits and reenters tristate, and on-chip termination circuits to provide maximum signal integrity. Not all FPGA families contain these dedicated circuits and the cost and complexity of implementing high-speed DDR memory interfaces varies considerably, depending on the specific FPGA family.

During memory READ cycles, the DQ data and DQS strobe signals are driven edge-aligned by the memory device. To allow the FPGA to capture the data using the strobe, the strobe must be phase shifted by exactly 90 degrees relative to the data, then routed in such a way that it captures all data bits simultaneously. Since the DQS strobe is not a freerunning signal, a master-slave DLL approach can be used in the FPGA in which the master DLL is locked to the system clock and is then used to control a slave delay line that shifts the strobe by exactly 90 degrees.

Monitoring activity

The round-trip device and circuit board delays from the FPGA to the memory device, and back to the

AAA

FPGA, are usually unknown and can vary with temperature and voltage. The time from issuing a memory READ command until valid data arrives at the FPGA is therefore uncertain. A DQ data-valid circuit in the FPGA can be used to monitor activity on the DQS strobe and signal the start of a READ burst, and therefore the start of valid data. Generally, this requires some method of detecting the transition of the strobe from tristate to active at the start of the READ burst preamble.

Since DDR memories use SSTL and HSTL electrical interfaces that are parallel terminated to half supply, signals in tristate always float to the threshold voltage of the input buffer. This can result in spurious oscillation of DQ data and DQS strobe signals unless dedicated circuits are available to prevent this behavior. FPGAs may include dual threshold input buffers and minimum pulse width detectors to prevent oscillation of the DQS strobe prior to the READ preamble and after the READ postamble.

DDR SRAM and SDRAM devices use various combinations of single-ended and differential SSTL and HSTL electrical signalling. The clock inputs to these memories are differential, so the skew between the positive and negative signals must be minimised by

ELECTRONICS WORLD February 2005

Figure 1: Reconfigurable FPGA supports multiple panel sizes, I/O standards and



the FPGA output driver. Also, to ensure maximum signal integrity at the memory interface, FPGAs with on-chip series and parallel termination capability should be used to drive and receive the various signals that constitute the interface.

Current generation DDR memory systems use static parallel termination that is always present, either on the circuit board or on-chip in the memory controller. To reach even higher speeds, while reducing system termination power at the same time, newer generation DDR2 memory devices make use of switchable parallel termination and controlled output impedance drivers in both the memories and the controller. FPGAs targeted towards DDR2 applications may include these capabilities.

For the output section, FPGAs interface the image processing to the panel driving circuitry via LVDS or the newly emerging RSDS standard. LVDS and RSDS are low-noise, low-power, lowamplitude differential signalling methods for sending high-speed (gigabits per second) data transmission over copper wire. RSDS has a lower voltage swing and output drive current than standard LVDS, resulting in lower EMI and lower power consumption, as shown in Table 2.

Choose wisely

FPGA a possibility.

Supply chain management starts at the display system architecture level and is driven by OEMs' desire to reduce costs. In addition, system designers look to FPGA manufacturers for intellectual property and easy to use design tools to further reduce costs and speed time-to-market.



Choosing an FPGA that supports differential signalling standards such as LVDS and RSDS makes integration of the panel driving circuitry into the

FPGAs



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All tracks on this CD were recorded on DAT from cylinders produced in the early 1900s. Considering the age of the cylinders, and the recording techniques available at the time, these tracks are of remarkable quality, having been carefully replayed using modern electronic technology by historian Joe Pengelly.

21 tracks – 72 minutes of recordings made between 1900 and 1929. These electronically derived reproductions are no worse than – and in many cases better than – reproductions of early 78rev/min recordings some are stunning ...

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- The Volunteer Organist, Peter Dawson, 1913
- Dialogue For Three, Flute, Oboe and Clarinet, 1913
- The Toymaker's Dream, Foxtrot, vocal, B.A. Rolfe and his orchestra, 1929
- As I Sat Upon My Dear Old Mother's Knee, Will Oakland, 1913
- 8 Light As A Feather, Bells solo, Charles Daab with orchestra, 1912
- 9 On Her Pic-Pic-Piccolo, Billy Williams, 1913
- 10 Polka Des English's, Artist unknown, 1900
- 11 Somebody's Coming To My House, Walter Van Brunt, 1913
- 12 Bonny Scotland Medley, Xylophone solo, Charles Daab with orchestra, 1914
- 13 Doin' the Raccoon, Billy Murray, 1929
- 14 Luce Mia! Francesco Daddi, 1913
- 15 The Olio Minstrel, 2nd part, 1913
- 16 Peg O' My Heart, Walter Van Brunt, 1913
- 17 Auf Dem Mississippi, Johann Strauss orchestra, 1913
- 18 I'm Looking For A Sweetheart And I Think You'll Do, Ada Jones & Billy Murray, 1913
- 19 Intermezzo, Violin solo, Stroud Haxton, 1910
- 20 A Juanita, Abrego and Picazo, 1913
- 21 All Alone, Ada Jones, 1911

Star Wars Knights of the Old Republic II: The Sith Lords (KOTOR II) Xbox, PC

KOTOR II is the next chapter to the award-winning role playing game of 2003. With seven worlds to explore and a large degree of free choice, this game allows you to take the story in whatever direction you wish.

You begin 'neutral' as such, and your actions allow you to become either a Lightside character, or you can choose to give in to the Darkside and become an evil character

In order to survive, this game makes you use your brains as well as brawn, and for an RPG with so many options; the game is really in-depth when it comes to

choosing weapons, clothing and abilities. The controls are amazingly simple to get to grips with. Also, people new to this game will find it easy to pick up, so don't be put off if you missed the first one. Instead, look forward to choosing your destiny, and expect great value for money, because every time you play it you create a totally different experience.



Unreal Championship 2: The Liandri Conflict Xbox

Unreal Championship 2 (UC 2) has improved gameplay and abilities on the original. Players can chose from any of the 14 characters available from the 'Unreal' universe, and are pitted against each other in multiplayer mode via eight-person Xbox Live matches with gamers globally and, also, via system link games.

A new, two-part, single-player story mode has also been added, allowing players to choose from a

Nintendo DS



Nintendo's latest handheld console - the DS, offers a new type of experience, thanks to its new touch screen, voice recognition and wireless gaming capabilities.

Hitting European in spring this year, it still has the well-known buttons and directional pad, plus a stylus for the touch screen has now been added. The console's only downside is its size, which after the GBA SP, takes a little getting used to.

In addition to gaming, the DS comes with PictoChat, a function similar to texting, which uses the DS's wireless connection abilities for you to message up to 16 other friends. This allows you to draw, write and add to received messages, and could become a popular way of messaging friends! + + + +

Mercenaries PS2, Xbox

If you can see it - you can steal it, use it or blow it up sounds good!

Mercenaries is a third person combat-action game, set in North Korea where a coup has plunged the nation into chaos. As a lone mercenary, you're dispatched to track down regime fugitives before they launch a nuclear attack. Liven your action movie fantasies through combat and non-linear gameplay in large interactive environments. Motivated by cash, you can choose

alliances and get the opportunity to pilot 20+ ground and air vehicles, as well as 30+ deadly weapons. The action is complete with a havoc physics engine where the world is always active and you can affect everything within it. Great value for money, each fugitive

EyeToy: Chat



Chat uses your broadband connection to turn your PS2 into a videophone. The first of its kind on a console, it allows you to chat with other EyeToy users globally via text, voice, video mail and one-to-one video chat. The 'text chat' rooms allow 256 people to talk together, whilst voice chats allow for 16.





Games

variety of uniquely-skilled characters, and battle their way to the top.

As an evolution of the original, UC 2 now offers hand-to-hand combat as well as improved third party navigation, plus new adrenaline powers enable players to invoke powers for new offensive and defensive tactics. For a pick-up and blast-away title, this might be a worthy purchase for your collection...

The most important aspect of the DS's introduction is that its new capabilities will allow for a much wider scope of gameplay options, and it will be interesting to see what developers do with the machine.

provides a separate mission, meaning you'll need more than the odd evening or weekend to complete this!

> The main selling point of Chat is its video capabilities, which, in a nutshell, is like using a webcam on your PC, just transposed to the living room. It would be wrong to offer a console product without gaming capabilities, however, so when in video chat mode, you can challenge your friend to a game of Draughts, Chess or 'Naval War'.

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By Mike Brookes

vervone must be aware by now of the widespread use of heart pacemakers. Every day one reads of the quality of life improvement, occasioned from the implantation into the bodies of sufferers of small, long-life, battery-powered devices that regulate heartbeat.

If such implants require 'tuning', how many people really consider how this is achieved. The answer is, of course, very short-range radio (SRDs) since a wired connection is not practical. A 'programmer' is sited close to the implanted patient and a wireless 'dialogue' established between implant and programmer. No contact - no pain - no risk.

Today, things have moved on. With the continued development of sophisticated but low-cost integrated and miniature sensor/radios and the parallel improvements in battery technology, implanted sensors now exist that can monitor heart rate, blood pressure and even changes in blood vessels. They can detect changes in aneurisms and pick

up on other potentially fatal conditions. In parallel, a number of companies are developing equivalent 'stick on' radio 'patches'. These attach to patients' skin and continuously monitor physiological parameters and transmit them to a 'wrist watch' style monitor.

From the 'wrist watch', acquired data may be re-

It might seem obvious that such systems ought to operate on harmonised frequencies, with common operating procedures *****

transmitted via radio telemetry to remote databases in which individual patients/alarm limits will have been pre-programmed so that any potentially dangerous variation can be monitored and detected.

This gives the medical team the opportunity of taking preventative action.

The concept clearly has enormous implications. It is a powerful tool in assisting medical staff, but it also offers huge benefit to patients as it allows them mobility. Radio standards are already

in place to give a basis for

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Wireless column

Heading toward auto-nursing

manufacturers to develop suitable products and these, too, are under regular review to keep them in line with the pace of technological change. Within the European Telecommunications Standards Institute (ETSI), a

dedicated Task Group - TG30 - is working to develop Ultra Low Power (ULP) radio standards that encourage the

development of new products. There are a few snags, however. It might seem obvious that such systems ought to operate on harmonised frequencies, with common operating procedures to promote product interoperability and to ensure that 'on body' monitoring devices can be used freely in any country. This would not only aid medical staff in reducing training needs multiple incompatible products in an operating theatre seems not such a good idea, but would also allow much

areater freedom for patients. Such thinking is perhaps

naive. Medical device companies are under pressure to use proprietary and thus incompatible data transmission protocols to reduce liability to malfunction through interference. In addition, all SRDs operating frequencies have shared secondary occupancy. The current ULP band is shared with Radiosondes, for example. To be jammed by a weather balloon may seem bizarre but it is possible.

Real concentration on interoperability by manufacturers and harmonised spectrum availability from regulators is needed to guarantee the success of mobile "body area networking". For once, cost is not the issue!

> The Low Power Radio Association (LPRA) has several active members on the ETSI TG30 Task Group working on ULP standards.

> The LPRA is a European trade body that represents manufacturers and users of SRDs. It is active in the production of SRD radio standards and regulations.

Mike Brookes is LPRA's chair-

If Bluetooth, 802.11, Zigbee, UWB etc don't suit your wireless application – "easy-Radio" will.



Circuit Ideas

Efficient bench power supply



ariable power supplies V usually have poor current capability at low output voltages (unless you can tolerate the noise and complications of switch-mode regulators). To reduce the power consumption in the pass transistors and deliver the maximum current at low voltages, we can automatically switch two secondary windings from series to parallel when low voltages are required. The following circuit, Figure 1, does this without the normal DPDT switch or relay; it changes quickly as the voltage required comes close to the output of a single winding using the method outlined in

Fig. 2: One-switch Series/Parallel Changeover (Only for DC Supplies) (b) Series (Double Volts) (a) Parallel (Double Amps). +21 21v 216 A To Toy Vsupply supply 20.3V/5A 41V/2.5A +217v 21v

Figure 2. This is much simpler than Gregory Freeman's preregulator (Electronics World, April 1995, p336) but only provides a choice of two, instead of three, voltages to the regulator.

dropped quickly and efficiently when the regulator's output is low, as sensed by Tr3 in Figure In low voltage mode, Figure Although almost any regulator circuit could be used, the 2a, with the switch open (Tr1 in Figure 1 off), both supplies novel arrangement of a 723 IC (with similar internal resisin Figure 1 has some interesttances and diode voltage ing features, in particular the voltage difference circuit drops) share the current load

equally, giving a 20V/5A

ELECTRONICS WORLD February 2005

(shown in Figures 3), allows the

supply. When the switch is

closed, as Figure 2b shows,

D1 and D2 non-conducting,

doubling the output voltage.

switch after the rectifier/capac-

itor sections, voltage supplied

Using a power FET for the

to the regulator can be

the supplies are in series, with

power transistors (Tr5 and Tr6) to be connected directly to an earthed heatsink or chassis, and means the output voltage is continuously variable from 0 to VREF times (R1/R2); 723 circuits normally only provide variation from 2V to 7V or 7V to 37V. The three-transistor current booster also removes the 37V output restriction of that chip (it's VEE, and the series/parallel sensing transistor's emitter, are fed from half the possible supply voltage marked "0V" in Figure 2). Regulation performance depends on the matching of R1 to R4, and the tracks of

VR1; the internal resistance can be slightly negative.

The 723's own current overload sensing transistor (pins 2 and 3 in the 14-pin DIP) cannot directly be used with our circuit; we need an external transistor. By using an AC128 germanium transistor for Tr2 a wider range of cut-out currents can be set using the same 0.15Ω series resistor and its increased sensitivity to temperature can be advantageous.

Mark Aitchinson Christchurch New Zealand

2V DC-DC converter

With the advent of micro-processors requiring low-voltage, high-current supplies, many good low-Z components are now widely available.

This DC-DC converter makes use of them in a 2V design to run a 9W compact fluorescent lamp (CFL) from a single lead-acid cell. The circuit is a fairly standard, single-ended, forward

converter with resonant flyback. The frequency is selected so that the secondary winding capacitance provides the correct amount of tuning.

With optimum operation the FET sees a half-wave rectified sign wave drain waveform. The circuit works at a fixed duty, with the output regulation tracking the input.

The output voltage is approximately 300V DC determined by the 150:1 turns ratio. The transformer core is an ungapped RM10 in 3C85, or similar. The transistor drive is

strapped supply.

111

10A -000 110Q03 2 x 2200u 6 3V -0 74HC14 + 21 101 2k2

Supply From Fig. 2

"0v" V

Circuit Ideas

Fig. 3: Operation of Regulator Circuit



(+0.6v or -2 lv with respect to "Ov" from supply

provided by a 74HC14 hex Schmitt buffer with a boot-To guarantee the circuit starts, the 1000µF is charged from the battery via the

switch when the circuit is off. When first turned on, the

capacitor is connected in series with the battery to provide 4V start-up. This then guarantees start-up as logic FETs can still have thresholds as high as 2V.

Tight layout and low ESR capacitors are essential to efficiency. The FET used is a 5mΩ, 20V device. **Paul Bennett** Bristol UK



Circuit Ideas

Sky box dropout zapper



monostable, HCT123. This has

Our local hospital radio service uses a dedicated Sky Digibox for its news feed. The box is tuned to IRN News on the Hotbird 4 satellite but if the signal is lost due to bad weather, a thunderstorm or light shower anywhere south of Basingstoke, it doesn't always come back. When the hospital evening presenter announces. "Now here is the news from IRN", there is sometimes an awkward silence.

The IRN news service is located in "Other Channels" in the Digibox menu and can be restored by pressing "Services", "6" then "Select". We think there is a software fault inside the Digibox, as many other users have had the same experience. Clearly, an automatic way of doing this is desirable.

This circuit achieves that aim. Audio from one channel of the Digibox is fed to the two-stage amplifier Tr1 and Tr2. The collector of Tr2 triggers the retriggerable,

a time constant of about 30s (2 x 6.8µF with 4.7M resistor). As long as there are no audio gaps longer than 30s, the monostable Q output will remain high, holding the counter (HC4040) reset and disabling the HC4052. When a long gap is seen, the Q output will go low and the counter will start to count pulses from the HCT14 oscillator. The HC4052 outputs will also be enabled. The pulse rate of the oscillator is about one cycle every two seconds. (This must be long enough for the desired action to be performed by the Digibox, in our case for the audio to appear.)

The first two outputs from the counter, Q1 and Q2, go through the sequence 0,0 0,1, 1,0 1,1 then repeat. These signals drive the address lines on the HC4052, a dual 4channel analogue multiplexor/demux. The "analogue" outputs are used to fool a

butchered Sky remote control unit into thinking that the buttons have been pressed. The relevant outputs from the 4052 are wired straight to the pins of the remote controller chip. The analogue switches have an 'on' resistance of around 70 Ω and this is easily enough to simulate a pressed button on the remote control. See Figure 2 for a complete list of all keys and their corresponding connection to the controller chip (28 pin) in the remote control. The infra-red output from the Sky remote must be pointing (more or less) at the Digibox front panel. We use an SLx Link Eye from Grandata and plug this into the socket RF OUT 2 on the back of the Digibox. The "eye" is mounted next to the naked Sky remote controller on a piece of MDF board.

A HC4052 is like a dual-pole, four-way switch (the HC4051 is an eight-way, single-pole switch). There are many possibilities for key press

combinations. Multiple HD4052s or HC4051s could be used. A total of twelve outputs are available on the HC4040 counter.

Note that only one gate of the HCT14 is used - half the HC4052 and half the HCT123. thus leaving spare functions for ingenious use. The VEE pin on the 4052 needs to be grounded for this application. The Sky remote control is fussy about its 3V supply. Anything below about 2.8V gives a warning on the screen that the batteries need replacing, and at much above 3V it doesn't work at all.

Not all Sky remotes may conform to Figure 2 by the way. Sky+ has extra buttons for instance and may well be different inside. In this case, you'll have to work out the wiring of your remote control using a meter. You can buy Sky remotes and the SLx Link Eve from Grandata - Tel: 020 8900 2329.

I used components that were readily to hand for this project. It can probably be realised using fewer parts but has proved very useful indeed. It will be handy for any "unattended" Sky box applications. Patients in the Royal Berkshire Hospital now always get news instead of occasional silence. **Charles Coultas** Wokingham **UK**

Disclaimer: We are aware that proprietary equipment has been used in this circuit idea.We do not condone it and would do not take any responsibility for injury that may result from applying this information.

Replacing pulse relay



House elecrical wiring, occasionally, requires the use of a pulse relay, which is activated and deactivated by a press of a button. It will avoid going around with the relatively high voltage of the mains wiring, thus improving safety in

certain areas. Normally, there are purpose built relays but they are expensive and difficult to find. By using a few additional components and a relay with two sets of contacts. it is possible to get the same

operation without resorting to delicate electronic components. Just as its original counterpart, it draws no current when idle and is operated by a negative pulse. It draws power in the 'on' state, though.

Early warning system

A simple solution to the problem of washing machine hoses that go quietly in the night comes in the form of a battery, a transistor, a resistor and a piezo sounder (see Figure 2).

While Figure 1 uses only the two parts, a battery and a sounder, it lacks sufficient sensitivity to give reliable results.

Soft water makes a good insulator. Absolutely pure water will have a theoretical resistance of just over 18MQ, when measured with two electrodes placed 1cm apart. You can make a sensor for that but do not need to in this case.

The water from the tap. normally, will conduct well enough to pass the small amount of base current needed to turn on a transistor switch.

Connecting the circuit of Figure 1 to wires about 5-10mm apart in a little water gave an anemic tone. It passed less than 1mA, 0.001A.

February 2005 ELECTRONICS WORLD

The sound level meter registered around 72dBSPL; about the same loudness as polite conversation - a level unlikely to give an early warning.

In Figure 2, the $10,000\Omega$ resistor limits the base current to a safe level. If the leads touch each other or the water conducts exceptionally well, the base current stays within safe limits. It protects the emitter-base junction while allowing the transistor to turn on the collector load.

Less than 1mA of base current will drive a small-signal transistor, hard enough to turn on the sounder at practically full volume: in this case, over 80dBSPL. It has enough gain to drive the 102dBSPL sounders that draw upwards of 40mA, 0.04A. If you want to drive an extra heavy load, replace the sounder with a sensitive relay and get a bigger battery. The listed values will work at more than 12V. Keep the collector current under 100mA, 0.1A with this transistor. In workbench tests with a

30mA, the transistor showed about 200mV, 0.2V drop from collector to emitter. This particular relay has contacts rated at 10A. With a heavier-duty relay whose coil draws 60-70mA. the transistor showed just over a volt across it. Not guite as good saturation but it did not complain. Until something connects the two leads, the system draws no current from the battery. For an alkaline battery, expect shelf life of typically 2-3 years.

Circuit Ideas



The chosen relay has 5A contacts, good enough to switch most household appliances. However, the circuit can be modified for other relays and ratings. The resistors in series with the coil should have a value similar to the coil resistance. The other resistor should be twice the coil resistance. Relav voltage should be half the supply voltage. The capacitor's value is also proportional to the coil resistance: the higher the resistance, the lower the capacitor's value.

The charge/discharge cycle of the capacitors is responsible for the operation. Although the contacts are in the discharge



The shortest time between two consecutive operations of the button is from 0.5 to 1s, depending on the supply voltage. An unregulated 12V power supply of suitable power is required to feed one or more of these units. Domenico Di Mario Milan Italy

.



relay coil

that drew



Figure 1. Simple water sensor with piezo alarm

Long wires could pick up stray signals. The 0.1µF capacitor filters them out. This allows you to place the alarm in a convenient location and run the wires virtually any

Figure 2. Amplified water senso

practical distance When the

wires have become partially immersed in water, current flows from the battery through the base-resistor into the emitter-base junction. This causes a large current to flow through the emitter-collector circuit causing the Early Warning System to sound the alarm. This should get someone's attention to fix the water problem.

R1=10K

C1=0.1µF 15V Q1 = 2N39043-12V piezo sounder 9V battery

Evert Fruitman Phoenix USA

Circuit Ideas

Simple mains power improved



C1 ZD1 C.2 (N)Figure 2

 (\mathbf{L})

Simple mains power supplies, not isolated and using capacitive dropping, are scarcely new, but the circuits usually seen are actually somewhat flawed.

Let's look at typical standard circuit as shown in Figure 1. C1 - perhaps 0.1 to 1µF - is the actual dropper. It has capacitive reactance, and is in theory lossless. Capacitance of 0.22µF is a good starting value; this will pass some 15mA at 240V RMS (50Hz). allowing a practical load of say 5-10mA. R2 (several megs) bleeds charge from C1 in the absence of a supply to avoid unexpected shocks to the user. R1 – 47Ω or so – helps to suppress any transients, and also makes a good fuse if it's suitably rated.

The current passed by the capacitor flows through D1 on negative cycles, and through D2 and ZD1 on the positive ones, charging C2. Vcc is then close to the Zener voltage,

which will be perhaps 5.1V. C2's value will depend on allowable ripple; this circuit needs 470µF or more, assuming that a couple of milliamps is drawn from Vcc.

Supply circuits like this are often used in simple triac control applications, as shown. R4, perhaps 220Ω , limits the current from the PIC's output pin into the triac's gate (use a sensitive-gate type). This voltage will be pulsed with an "on" time of a few tens of microseconds: enough to operate the triac, but not enough to cause supply droop. R3 provides the PIC with zerocrossing information. Keep it high in value, and watch its voltage rating. A couple of 10M resistors in series is good. Obviously other components such as switches or optocouplers, LEDs, perhaps a VDR, and filtering and snubbing round the triac will be needed in actual applications, but we are really only interested in the power supply at the moment

≷r1

The bad news about the Figure 1 circuit is that ripple or cycle-by-cycle droop is greater than it need be, precisely because the Zener and the smoothing capacitor are in parallel.

Figure 2 is more efficient both in component use and performance. C1, R1, and R2 are unchanged, but ZD1 is put in D1's old position. Make it a 5.6V device for a nominal 5V rail. C1 should not exceed 1µF, which will put 75mA through the Zener: that's 250mW when averaged for forward and reverse half-cycles. As we saw earlier, 0.1 or 0.22µF gives quite enough to run a PIC.

the remaining diode and can only discharge through the target circuitry: it can be half its previous value for the same performance. One important point is that C1 must withstand the full

mains voltage continuously, so it must be appropriately rated to Class X or Class Y for safety.

e.g.

PIC

Load

Triac

R4

And the most important point of all: because it is connected directly to the mains, this type of circuit is potentially lethal! Never assume that the mains neutral wire is at earth potential, as it is supposed to be at least in the UK. If you must work on non-isolated mains circuits such as this, while they are live stand on an insulating mat or perhaps wear wellies, keep one hand safely in a pocket, and move wires only with the back of a finger (less important with AC, which doesn't cause muscles to clench).

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HANDYS

If you have any doubt as to the safety of the finished device, add more insulation. You have been warned!

Nick Cornford Berkhamsted UK

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C2 is now charged through

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Specifications

Switc	h posi	tion 1
Bandy	width	

Input resistance Input capacitance Working voltage

Switch position 2 Bandwidth

Rise time Input resistance 1M0 Input capacitance Compensation range Working voltage

DC to 10MHz $1M\Omega$ – i.e. oscilloscope i/p 40pF+oscilloscope capacitance 600V DC or pk-pk AC

DC to 150MHz 2.4ns $10M\Omega \pm 1\%$ if oscilloscope i/p is

12pF if oscilloscope i/p is 20pF 10-60pF 600V DC or pk-pk AC

Switch position 'Ref' Probe tip grounded via 9MΩ, scope i/p grounded



Go XP. ao!

Regarding Alistair McFarlane's article in the December 2004 issue ["Mixed spices part 2", p32]. firstly, there seems to be some misunderstanding on what information was transmitted to Alistair versus what was received or understood. Regarding the claims of hanging behaviour with SuperSpice, at no time was it suggested that there were issues with SuperSpice running on XP versus Win95/98, SuperSpice usually runs extremely well on any of these systems, and essentially, never crashes. Indeed, in five years, there have been maybe only one or two reports of a crash.

What I did note was that XP systems are far, far more reliable, by at least an order of magnitude, than the earlier systems, and as such I recommend that operating systems (OSs) prior to XP be replaced as soon as practical. The technicalities of Windows seem to be missed by so many. It is not debatable; XP is way ahead of the earlier systems. For example, the earlier OSs will run out of GUI memory and hard crash the whole OS once it uses up its scant 64KB of specialised reserved GUI memory. This is despite having 1GB of main RAM. This fact alone is enough to dispense with the older systems. There are many other technical issues that I won't go

into here, but the older OSs still sit on top of DOS.

Alistair mentioned that some vendors have indicated certain issues with XP and actually recommend staying with the earlier systems. This may be more due to 16-bit legacy code in their products then the merits of XP, or it may be ignorance on their part as, fundamentally, those that claim such matters are usually mistaken. So, whilst Alistair may not be certain about XP/98, I am. XP is the only realistic way to go today.

I am still unclear as to what the reason for Alistair's problems were, however, SuperSpice is specifically set up to produce results with minimum effort. Running examples is just a matter of pressing a button. After the run, graphs of the correct type and size will be displayed automatically. One possibility for graph size is that he inadvertently disabled the "lock graph size to window size" check box. This is a special feature to allow for graphs to be sized and placed anywhere on the schematic.

SuperSpice has been run on many systems, including Unix under an emulator. None of the issues Alistair mentioned have arisen on these systems. I have personally used SuperSpice for 1000s of hours, on many systems, with no hanging problems like Alistair's. My best guess here is that Alistair's system has a fundamental problem, either hardware or software. **Kevin Aylward** Anasoft Basildon, UK

Hot debate

With audio power amplifier distortion mechanisms currently hotly debated, I

Check the current I have comments on "The Catt anomaly" article in EW October 2004, page 38. The explanation by lan Hickman is very good, but I wish to take issue with his comments on displacement current, eg. "displacement current is not a flow of real



would like to add to it by proposing an audible distortion reducing mechanism I call 'class half-A'.

The idea is to trade some large-signal power handling in return for the elimination of small-signal crossover distortion. With a class AB power output stage, up to 25% of the stage's maximum power output may usefully be turned to partially bias the AB output stage as a small-signal class-A amplifier. Crossover distortion may thereby be removed from the dynamic range of small signals.

With a typical audio amplifier design, an output pull-down is a simple way to achieve this effect. A pull-down resistor tied between the output node and the negative supply rail is the crudest approach, but a constant current pull-down gives more usable class-A power. The pull-down current should be designed not to steal too much power when the output stage is giving its full pull-up voltage. For the more adventurous, it may be possible to adjust an amplifier's feedback to achieve a similar effect.

Allan Campbell Newcastle-upon-Tyne,

UK



current". My reasons are:

Letters

1) Maxwell's equations indicate that the displacement current is proportional to the rate of change of the electric field, has the dimensions of current and it generates a magnetic field identical to one that would be produced by a "real" current in a conductor. For example, consider a capacitor constructed from two parallel metal plates. When it is charging, the electric field between the plates is increasing in intensity. The changing electric field creates the displacement current, which is said to flow between the plates and is perpendicular to them. The magnetic field is perpendicular to the current and the lines of electric flux.

2) Ian and Ivor assume that a"real current" is the movement of charge carriers such as electrons. This has been taught by generations of physics teachers and is the accepted concept. But, I suggest that future developments may alter this viewpoint. Physicists from Einstein onwards (and possibly earlier) have been searching for the "theory of everything". I feel that, when this theory is devised, it may include a new definition of electric current.

The other point I wish to raise is lan's comment that, "the electrons may be moving at a snail's pace relative to the speed of light, but the disturbance just described propagates along the line at the speed of light".

I don't see how the "disturbance" can propagate at the speed of light when it is due to the movement of "snail's pace" electrons. If the disturbance of one electron is due to the movement of the one beside it, how can the disturbance propagate at the speed

Letters

of light? I feel that the "theory of everything" will produce a better explanation.

As I understand it, the most promising contender for the "theory of everything" is string theory. So electric current may be a flow of strings. Such a current may be able pass through dielectrics such a vacuum, air, plastic, etc. The movement of charge carriers may be simply because they are being pulled along by the "string current". As an analogy, consider a river of clear, slowly flowing (ie. non turbulent) water. The current is virtually impossible to see unless there is a marker of some kind such as a floating leaf or a colouring of the water by a blob of dye, etc. Len Cox Forest Hill Australia

A mistake of triac proportions

Thanks for the continually interesting and useful EW Circuit Ideas section. I must raise a concern about lan Benton's "Dual Rate Thermostat" as published in the December 2004 issue [p45].

No criticism of his circuit is intended. The triac CSR1 in the diagram seems (to me) to have been mistakenly drawn, with its main terminals transposed, putting the gate on the wrong end of the device. Correct operation requires that the trigger pulse flows from supply positive, through the triac's 'main terminal 1 to gate' region, via R5 to TR1's emitter. As drawn, the triac gate is at full mains potential with respect to the PIC positive supply, which looks to me incorrect and liable to damage the transistor and PIC. **Jeremy Jago** Nottingham, UK



Dare-devil

I was sorry to see some of the criticism of Graham's articles. Whilst I would have to agree that the writing style was at times repetitive, two verv important messages came out for me:

1) The "establishment" has paid far too little attention to First Cycle distortion one only has to see a plano note or a triangle being struck on an oscilloscope to see how sharp the first cycle edges can be. 2) In particular, the effect on speaker loading of the first cycle behaviour had not been obvious to me.

I would add that even at professionally organised gigs there seems to be a widely varying standard of ampilfication. By way of example, I have been fortunate enough to be at Eric Clapton concerts twice in the last few years. The first was the 'Reptile' tour, the second in May of this year. I particularly remember the brilliantly clear transparent PA of the first despite, perhaps unnecessarily, high soundlevels for the genre.

The second, though, I found to be definitely too loud and disappointingly muddled. I was sitting in the same seats in the same hall, yet there was a huge difference in the clarity. I would be most interested in an analysis of the equipment and speakers used for the two gigs. I would be particularly interested in such an analysis by someone like Mr. Maynard who seems to have genuine real-world experience and a drive to get to the bottom of

the differences he hears in that world.

How about it, Graham? **Chris Miller** UK

Unnecessary criticism

Having read Phil Denniss's long letter in the December issue of EW, in which he criticises (to put it mildly) Graham Maynard "Class A Imagineering" articles, I can't help feeling he was unduly harsh, dismissive and unfair towards Graham, Graham's writing does ramble on a bit, repeat itself and make tough reading, but it does manage to communidate his fervent enthusiasm for and belief in his message, which I gather has evolved through years of personal experience. I, for one, am intrigued by his theories and remain openminded

The human ear/brain takes a very big cue from the initial transient of any signal because it contains the directional information. in addition to information on how the sound was created. The memory of that initial instant is still important a long time (comparatively speaking) after it has passed.

Would that very information not be critical in the correct portrayal of a stereo sound stage?

So, Graham, I know it's been a marathon task for you, but unfortunately it's not quite finished. As a final conclusion, how about a double blind test using your best audio set-up, with results to appear in a future EW? I'm sure many, like me, will be eager to learn. Nick Ham Philips Power Semiconductors, Stockport, UK

Is this mere hypocrisy?

It saddens me to see the letter from Mr. Denniss following in the footsteps of Doug Self et al in expressing a point of view in such an aggressive manner. I've read "Wireless World" since the early 1960s and, throughout that time, the pointless argument between the objectivists and subjectivists has raged on the subject of audio equipment design.

I've spent nearly 40 years in the hi-fi and audio industries and been responsible for nearly 300 commercial designs. I was a founder director of Mission Electronics and Cambridge Audio, worked for numerous British, American and Japanese companies and, finally, semiretired after being Chairman of Wharfedale loudspeakers and Quad Electroacoustics. I also, incidentally, bear the responsibility of giving Doug Self his first job in the audio industry.

Let me first dispel the wrong assumption that the aim of a hi-fi audio designer (as distinct from a professional audio designer) is to create, say, the perfect amplifier. Not true. The aim of the designer is to create an amplifier that will sell. So, the really successful designer has to identify which measurable characteristics translate into manipulations of sound that people can identify and hopefully like. Sometimes, the designer may be unable to accept that this is what he is doing, but the fact remains that once they find that customers like a particular design, they stick to the formula or recipe that works. To give an example, in the 1980s and early 1990s I designed a hugely successful series of amplifiers for Rotel which, despite having a reasonably

flat frequency response, did emphasise the bass guitar and bass drum sounds so that a "foot tapping" sound was produced. And tap their feet was what the public did whilst buying the products in hundreds of thousands.

Some years ago, a wellknown magazine reviewer, who swears by the importance of measured performance, tested one of my products and found that it turned into a mediocre set of results. This left him with a quandary because he found that he just loved listening to his favourite music through this product.

I've always measured my products and, to this day, keep a set of audio precision equipment at home, but I also use those measurements to tailor the audible sound to suit the target market. And it works, because "my" proucts have received no end of "5 Star" reviews and awards from the consumer magazines. That doesn't mean that I cannot design an "accurate" product when I need to. The Quad ESL-989 loudspeaker significantly improves upon the performance of Peter Walker's original and brilliant work. Why? Because, again, that was what the market would respond to.

Certainly all this talk of "long established scientific knowledge" and "valid science" has about it the whiff of hypocrisy. I'm afraid that engineers have a poor reputation with the buying public. Remember the early transistor amplifiers, which had such low distortion, compared to valve amplifiers but then turned out to have crossover distortion and output stages which blew-up quickly (Ah, that smell of burning resistors)? Then, there was the "per-

fect" new medium of compact discs, perfect - once we'd sorted out some of the first generation problems. And the list goes on. Furthermore, anyone who has any involvement with the academic world knows well that results and findings are routinely "spun" to give either a more politically correct result or one which will facilitate the next round of funding. Alas, science is as corruptible as any other form of human endeavour.

Finally, I must take task with the comment that subjectivists "cannot or will not produce the slightest shred of credible evidence for their claims". I tend to stand with a foot in each camp but I can tell you that in the early 1980s a contingent of most of the "golden ears" magazine reviewers visited Abbey Road studios, where Decca kindly set up a double blind test with pieces of music simultaneously recorded on both analogue and digital recorders. The aim was to establish if we could identify any difference. The listening was performed in a rigorous manner and subsequently written up in "Hi-Fi for Pleasure" magazine, I can report that I achieved a statistically valid result in correctly identifying a difference most of the time. Unfortunately, the recordings I credited as being digital turned out to be analogue and vice versa. But then life is like that. Stan Curtis Ramsey

UK

I was puzzled by lyor Catt's opening paragraph in his article "Not me, guv" in the May issue of Electronics World. It closes with the assertion that "minimal area within the ((hysteresis) curve (of a mains transformer) indicates maximum remanent magnetism". I would have thought that minimal area within the curve would occur if the hysteresis loop could be made so thin that it became a line through the origin and there was no remanent magnetism at all. However, there is no need to invoke remanence to explain large switching-on surges in mains transformers. This has been explained before, in Wireless World, by Cathode Ray or Mixer, if I remember rightly. In a steady-state condition, the integral of voltage with respect to time during one half-cycle of the mains voltage changes the magnetising current in the transformer from its negative peak value to its positive peak value or vice versa. However, if the mains switch is closed at the beginning of a half-cycle, and the transformer behaves linearly, the current starts from zero and reaches twice the normal peak value. The current has a DC component that dies away with the usual time-constant of L/R. If the core saturates, the peak current will be considerably

greater.

111-

Letters

Continuing puzzle

It's not entirely true to say that switching-on surges have been ignored by the EMC community. Since 1993, the German NAMUR NE21 EMC standard for industrial process control equipment has stipulated that if a switching-on surge has a "half-life" longer than 5 milliseconds, its peak

value must not exceed 15 times the peak value of the nominal current consumption. All devices must continue to work with no loss of stored data after a 20-millisecond interruption of the supply. NAMUR stands for User Association of Process Control in Chemical and Pharmaceutical Industries. (If one reads it in German the derivation is equally obscure.)

The (US) Information Technology Industry Council specifies similar requirements for immunity to voltage interruptions and dips (see "Plug in: Safeguard AC Powerline Quality". EDN Europe, March 2004). IEC 61000-4-11 (for AC supplies) and IEC 61000-4-29 (for DC supplies) cover the methods by which the testing is done.

Ivor has in the past criticised the EMC community for use of jargon. Some readers may find the following explanations useful: "Symmetrical" refers to a test signal applied to a pair of wires in differential mode, but not necessarily balanced, and now sometimes called "line to line", "Asymmetrical" means common mode. "Unsymmetrical" means that the test signal is applied between the reference ground of the test set-up and an individual wire. The test is applied in turn to each of the wires connected to a port (input, output, supply etc.) of the equipment under test. Not surprisingly it is now sometimes called "line to ground". Confusingly, the latest (bilingual) version of NE21 has "unsymmetrisch" translated to "asymmetrical", presumably because the word "unsymmetrical" doesn't officially exist in English.

In the European Union, one also needs to master some

non-technical jargon. "New Approach" refers to a directive from the European Commission that describes only its essential requirements, leaving everyone in as much confusion as possible about what they have to do to demonstrate compliance with the directive. The "Technical Adaptation Committee" decides what a directive means, if the Commission, which issued it, doesn't know itself. "SLIM" or Simpler Legislation in the Internal Market, seems to mean legislation in which the same rule is applicable to everything, no matter what absurdities result or how many people's lives it complicates (the sort of thing George Orwell called Newspeak).

Examples include making the Automotive EMC Directive applicable to simple resistive loads such as map-reading lights and absorption refrigerators, and the current proposal to make the Low Voltage Directive applicable to extra low-voltage equipment. A third example would have greatly impressed King Canute's servant or Mr. Scott of the Enterprise, because it seems to demand a change in the laws of physics:

In the UK and much of Europe it has been normal practice for several years to run portable gas appliances from butane at 28 millibars gauge pressure or propane at 37 millibars to get similar performance with either gas. However, from this year, installations in caravans will have to comply with EN1949, which stipulates that the pressure will always be 30 millibars, and appliances will jolly well have to accept it. **Hugh Mirams** Oldham UK

50



Not synchronised

In the January's letter section, under the heading "Pendulum Conundrum" [p53], C Holwill asks how pendulums on quartz clocks maintain synchronism. Some time ago I was amused to observe one of these in action. The question is easily answered they aren't synchronised. Alan Robinson Holaate



Teaching students

The following is an attempt to answer one or two issues raised by Mr Trevor Skeggs under the title 'Powers that be' in the September issue Letters pages.

Most students studving engineering in particular will experience the problem of not immediately comprehending certain points, whether attending a course or reading a textbook. Unless positively and repeatedly encouraged to do so - which will not normally be the case - most students in a class are naturally reluctant to advertise their inability to understand particular points when first encountered. Where this is the case, students should take the matter into their own hands and help one another.

A student with a particular difficulty should feel free to ask other members of the class for an explanation during a break. If the class experiences a common difficulty, a 'brain storming' session over coffee can sometimes clear the matter up. A help line, whether by telephone or e-mail, can save hours of frustration and discouragement.

Obviously, assessed work handed in for marking must be the students' own: cheating is to be condemned as untrustworthy and ultimately selfdefeating. That said, engineering today is generally of such large scale and complexity that most people will work much of the time collaboratively as members of a team, so adopting a team approach to study usefully mirrors this fact and can also serve to improve social skills. If a point in class presents an initial difficulty, it is often helpful to consult several textbooks covering that point, whether in a library or a bookshop. Often, an alternative textbook will clear the matter up. Sometimes reading on ahead of the point of difficulty will reveal a subsequent explanation later in the text.

Modern technology increasingly and inescapably involves the application of mathematical physics in an engineering context, and thus abstract theory and the associated mathematics cannot be avoided. This makes it increasingly necessary to appreciate the key fact that mathematics centres on the recognition and appreciation of pattern, in the case of indices, that of a simple sequence as will be shown. Also, mathematics has to be rule-based to ensure consistency. Many mathematical operations, for example division, can be carried out in

more than one way, in this instance algorithmically using the 'long division' method or by employing logarithms. In many cases, there are three or more different ways to carry out the same mathematical operation. For specific inputs and to the same precision. every method must yield the same result for the mathematical consistency to be obtained, for reasons that are

self-evident. To take Mr Skeggs specific problem if an index of zero always yields unity, this is something many people have difficulty with on first acquaintance. The reason is that it arises from a mathematical pattern not always made explicit, in this case, the pattern being a simple numerical sequence. The matter can be made clear by setting out two identical sequences, one below the other, but having alternative format; the index form at the top, the rational form below:

10-2,	10-1,	10x,
101,	102,	103,
1/100,	1/10,	1,
10,	100,	1000,

The value in the upper sequence between 10⁻¹ and 101 has been written as 10x where x is assumed initially to be unknown. Clearly, the rule for generating the lower sequence is to multiply the previous value by ten to obtain the next value in order when moving from left to right. Similarly the rule for generating the corresponding upper index form sequence is to add one to the previous index when moving one place to the right, so: -2+1=-1, -1+1 =0, 0+1=1, 1+1=2 etc.

With this rule applied to the index sequence, it becomes

obvious that the necessary value for x is zero, i.e. x = 0. Thus the mathematical pattern in the index case is simply an integer sequence. From observation the mathematician defines 100 =1 for consistency.

The power of mathematics derives from its ability to generalise. In the above example, where the base equals 10, if the value 10 is replaced by the symbol b, the two identical sequences become:

b-2,	b-1,	b0,
b1,	b2,	b3,
1/bxb,	1/b,	1,
b,	bxb,	bxbxb,

Again, the lower sequence is obtained by multiplying the previous value by b, while the

upper index sequence is unchanged except for the substitution of base 10 by symbol b. Hence, the numerical value of base b is of no consequence: b could be equal to, say, the lottery magnitude number 7 294 628 and it would still be the case that 72946280 = 1. For generality, the mathematician again defines b0 = 1 and -b0 = -1 for consistency, whatever finite value b may take. On first acquaintance the notation 72946280 = 1 does not immediately strike one as being selfevidently true, and this is the cause of the difficulty when this sort of statement is first encountered. But, once the logic of the pattern-derived rule is laid out, the matter becomes obvious enough. Mr Skeggs should not

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February 2005 ELECTRONICS WORLD

Professor Silvanus P. do, another can". How very true! P. Welch Horsham IK

Corrections

AAA

In my circuit idea 'Precision Aweighting filter' published in the Electronics World

despair, most of us have been in the same position on many occasions. The celebrated

Thompson FRS, author of the textbook Calculus Made Easy, wrote a prologue containing a statement known to a generation of students: "Considering how many fools can calculate, it is surprising that it should be thought either a difficult or a tedious task for any other fool to learn how to master the same tricks. What one fool can

December 2004 issue on page 46 there are several minor corrections to be mentioned: 1. Figures 4 and 5: x-axis is frequency from 20Hz to 20kHz (log scale) 2. Figure 5: black trace = X; red trace = Y

Letters

3. Appendix 4.: a (B) is valid for non-equalised white noise only **Burkhard Vogel**

Stuttgart, Germany

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Ignios announces product Matlab's 64-bit Linux **System Weaver v1.0**

Ignios Ltd. a recent entrant in the embedded multicore System-on-Chip (SoC) market, recently announced the availability of SystemWeaver version 1.0. SystemWeaver addresses the software challenges of multicore architectures in the embedded IC market

It consists of the parameterisable, synthesisable System-Weaver IP core and the System-Weaver API. A SystemC model of the core and reference models of SystemWeaver-enabled SoCs are also included. The System-Weaver API provides a unified abstraction layer for complex

multicore devices. This abstraction allows embedded systems designers to develop and debug multicore applications more effectively, improving time to market.

The key underlying system management and communications functions are implemented natively in a SystemWeaver IP core that is integrated on-chip. SystemWeaver is compatible with existing and proposed interconnect, RTOS and processor technologies and requires minimal changes to the host chip architecture.

www.ignios.com

support

The MathWorks today announced new support for the Matlab and Simulink product families on AMD64 and Intel EM64T processors.

The MathWorks developed a version for the Linux x86-64 platform in response to the most frequent customer requests: large data set access and manipulation and optimal computational performance.

Matlab support for the x86-64 architecture removes the 4GB memory limit imposed by 32-bit operating systems that restricts the size of applications' data files. As a result,

users can work with much larger data sets.

"Often, customers make current platform decisions based on future application requirements. Many have indicated they plan on moving to x86-64 platforms," said Leslie Mehrez, Matlab marketing manager at The MathWorks.

Support for the 64-bit version of the Linux operating system on x86-64 processors is currently available with the recently released Matlab 7 and Simulink 6

www.mathworks.com

New video filter/drivers reduce board space

Fairchild Semiconductor has announced a new family of highly integrated video filter/drivers. They can replace as many as 80 parts to help designers lower pick-and-place design costs and reduce board space by up to 20% in video applications.

The new Fairchild FMS6143, FMS6145 and FMS6146 multichannel devices significantly decrease test- and design-time, and increase image quality in DVD, LCD, TV, set-top box and other digital consumer products. The 3-, 5- and 6-channel, 4th order filter/drivers improve image quality when used to replace discrete products in traditional 3rd

order passive solutions. Com-

pared to passive designs, they



Bridge chips simplify USB to serial connectivity

Intelligent USB to serial port bridge chips from Oxford Semiconductor provide serial port peripherals with the instant plug-and-play connectivity and high-speed data transfer of full-speed USB2.0. The single UARTOXUSB950 and guad UART OXUSB954 feature an integral 12Mbps transceiver and serial interface engine and support baud rates up to 230kbps.

Supported by a complete set of royalty-free USB host device drivers, the bridge chips create transparentinterfaces between USB and serial ports that require no firmware changes. For legacy applications, the OXUSB95x chips provide a simple means to upgrade peripherals from serial to USB communication. Power economy is assured by the integral USB suspend/resume function.

Handling USB transaction and control data processing is the bridge chip's advanced 16-bit microcontroller. Operating at 5MIPS and featuring 3kB of on-board RAM and masked ROM, the controller also offers the flexibility and processing power to enable development of peripherals able to process data before it is passed to the host PC. www.oxsemi.com



Products

provide better inband and stopband filter characteristics that reduce artefacts in video signals and result in higher image guality, By providing 8MHz cut-off frequency and 48dB stopband attenuation, these devices meet standard definition (SD) video requirements, while allowing them to be used as anti-aliasing or reconstruction 'video out' filter drivers. Internal diode clamps and bias circuitry enable the video filter/drivers to accommodate AC- or DC-coupled input signals.

The outputs on each device can drive AC- or DC-coupled single (150 Ω) or dual (75 Ω) coaxial cable loads

www.fairchildsemi.com



Industry's first singlechip 48-port GbE

Agere Systems launched what it claims is industry's first singlechip 48-port Gigabit Ethernet (GbE) switching chip and the lowest power GbE octal physical layer device (PHY) for enterprise networking equipment.

The solution uses seven chips - one switch system on a chip (SoC) and six octal PHYs - to build a complete 48-port GbE switch with two 10Gbit/s Ethernet ports.

The TruePHY ET1081 octal PHY has a power consumption of less than 500mW per port. Inherent in the TruePHY architecture is highly advanced cable diagnostics, with the precision and accuracy to pinpoint a break in 100m or more of standard CAT5 cabling,

The four new GbE switch-on-a-chip devices are part of Agere's ET4K family of switching silicon. The ET4000 supports 24 10/100/1000Mbit/s Ethernet ports and four Gigabit SerDes ports. The ET4100 supports 24 10/100/1000Mbit/s Ethernet ports, with four Gigabit SerDes ports and two 10Gbit/s Ethernet ports. The ET4001 supports 48 10/100/1000Mbit/s Ethemet ports and four Gigabit SerDes ports. The ET4101 supports 48 10/100/ 1000Mbit/s Ethernet ports, four Gigabit SerDes ports and two 10Gbit/s Ethernet ports. www.agere.com

TC-OCXO technology promises OCXO stability

C-MAC MicroTechnology has unveiled TC-OCXOs (temperature-compensated oven-controlled crystal oscillators), designed to deliver the high stability of an OCXO from a device with low power consumption, small size and light weight comparable to those of a TCXO. Capable of stabilities better than ±0.05ppm over the full operating temperature range, C-MAC TC-OCXOs will initially be aimed at mobile, battery powered and remote applications such as GPS, satellite comms, distress beacons and secure radio.

Ambient temperature variation is one of the main causes of frequency variation in a crystal oscillator. To overcome this, C-MAC TC-OCXOs use a hybrid combination of limited temperature control, by use of an oven, and further reduction of the remaining frequency error through C-MAC's proprietary Pluto temperature compensation ASIC. www.cmac.com



MultiSwitch can be powered by two sources

Riello Galatrek has launched a new product called MultiSwitch - an intelligent automatic transfer switch. It can be powered from two independent power sources to achieve standby power protection should one source fail suddenly. Up to eight separately connected network devices can be powered from its output sockets.

MultiSwitch is ideal for complex computer and Voice over IP (VoIP) networks requiring maximum uptime, and provides the added advantage of allowing users to monitor and control their connected devices.

The power sources to a MultiSwitch can be a combination of two independent mains supplies, uninterruptible power supplies or a combination of the two. Each source has to be rated to support the full load placed on the eight output sockets.

MultiSwitch can be installed with a single power source to allow the dual feed option to be activated at a late stage of growth of the network. www.riello-ups.co.uk

111

ELECTRONICS WORLD February 2005

Upgraded logic tool is comprehensive

The next generation of ispLEVER programmable logic design tool suite is now available from Lattice Semiconductor. The ispLEVER 4.2 release is a comprehensive upgrade and enhancement of the design tool suite's performance and functionality.



FPGA Fmax performance has been increased by an average of 22% and map, place and route run-times have been reduced by 24% for a typical design, lessening the demand on computing resources. Enhancements include an I/O Assistant for efficient placement of mixed I/O types, new Power Calculator and ispTRACY Logic Analyzer tools, a new Project Creation Wizard, major upgrades in static timing analysis, floorplanning and DSP design, and a significantly faster and more fully featured ModelSim Simulator from Mentor Graphics. The tool suite includes Synplicity's Synplify 7.7 as a standard feature.

http://www.latticesemi.com/

MCUs with 512k Flash

Supporting the industry migration from 8-bit to 32-bit microcontrollers (MCUs), Royal Philips Electronics announced the first five of a series of 32-bit MCUs with up to 512kB of onchip Flash memory. Philips's LPC2130 series establishes a new price/performance ratio for the 32-bit ARM7 segment. Designed for a wide variety of embedded system applications, including industrial control, computing peripheral and medical markets, the LPC2130 series offers the fastest Flash memory available on 0.18µm CMOS technology, ultra-lowpower operation and built-in error correction

On-chip Flash memory is a critical component in systems that require additional computing muscle and realtime response. The LPC2130 series (LPC2131, LPC2132, LPC2134, LPC2136 and LPC2138) uses 128bit-wide Flash memory. This enables four 32-bit words to be accessed in a single fetch, allowing the CPU to run at 60MHz (54MIPS) without waitstates

www.semiconductors. philips.com

40Gbit/s InP modulators ready now

The Centre for Integrated Photonics (CIP) has launched a range of electro-absorption modulators fabricated using indiumphosphide (InP). Available in 40Gbit/s and 10Gbit/s versions for either single wavelength or DWDM communications applications, the devices offer compelling advantages as building blocks for next-generation optical networks including low insertion loss, very small size, high bandwidth and low drive voltages.

A key feature of CIP's electroabsorption modulator (EAM) device design is low insertion loss, Figures of 4.5dB or 4dB typical for the 40Gbit/s and 10Gbit/s variants respectively provide good power margins for system design. This feature stems from novel structures employed in the devices including buried heterostructure geometry.

The 40Gbit/s version of the

device - 40G-SR-EAM - offers bandwidth of 32GHz, typical for high-quality error-free transmissions and a drive voltage of just 2.9V. These parameters compare well to modulators fabricated from lithium-niobate but result in a dramatically smaller footprint. The 10Gbit/s version of the device - 10G-LR-EAM - offers a minimum bandwidth of 10GHz and a drive voltage of 2.9V. Both devices are offered in a compact package with a K connector, or in chip-on-carrier form. The CIP has a long pedigree in optoelectronics, having previously been part of Corning, and before that. British Telecom's Photonic Technology Research Centre. The organisation has its own semiconductor fabrication plant and is able to create variants of the EAM devices with application-specific performance requirements.

111

Products



www.ciphotonics.com

New platform provides three times VXI switches' density

Racal Instruments has introduced the 1260-67M, six-position, single-slot VXI, modular, microwave, switch platform. With it users can specify up to twelve combinations of various 18GHz and/or 26GHz switches. thereby receiving up to three times the density of competing 26GHz VXI switch modules.

The 1260-67M platform provides a choice of eight switch types, including 18GHz and 26GHz 1x2, multi-throw and transfer switches. This modular approach means that there is no need to purchase separate C-size cards for each type of microwave switch needed in a system. The inherent modularity of the platform addresses sparing as well as upgrading. Should relay replacement be necessary, relays can be removed and replaced in less than five minutes, without removing the module from the VXI system. This approach not only facilitates the replacement of failed relays, but also enhances the field upgrade capability of this switch card.

Maximising system uptime, facilitating field upgrades and sparing and reducing MTTR are inherent significant features of this high-performance switch platform.

www.racalinstrumentsgroup.com



Double-decker PCB connectors

A new range of double-decker PCB connectors is now available from Camden Electronics. They are designed for use in applications where a high-density of connections is required. The



CTB9350DD series is available in two and three pole versions and are end-stackable. They interlock to allow any number of poles to be built up to customer specification.

The double-decker construction enables twice the number or poles to be connected in the same space as single decker versions. Pins are available in straight or 90^{0} , enabling cables to be connected in either orientation. Two versions are available with 5mm and 5.08mm pitch, respectively.

The connectors are moulded from UL94V0 green PA68 and feature tin-plated copper contacts rated at 12A for 450/750 operation. Insulation resistance is equal or greater to 5M Ω and dielectric strength is 2500V AC. PCB mounting hole diameter is 1.6mm. Maximum operating temperature is 125^oC.

www.camdenelec.com

CPCI Ventus chassis offers 80W/slot cooling

The new entry-level Ventus 12U, 21-slot IEEE1101.10-compliant chassis from APW Electronic Solutions provides 80W per slot cooling. Power consumption and system packaging density continue to rise inexorably, but for reliable long-term operation, maximum allowable silicon die temperature has remained stable at around 85°C.

Ventus chassis cooling is provided by APW's patented, hybrid serial/parallel fan arrangement. Three hot-swap, pluggable FRUs, each containing three separate fans, provide airflow of 850LFM (linear feet/minute) through all 21 slots with 70% obstruction in each slot position. Total system throughput of air is 255CFM (cubic feet/minute). In the event of a single fan failure, airflow is maintained at just under 800LFM per slot or 240CFM total. The chassis has positions for up to three, independently cooled, AC or DC input, 600W power supply units. These are hot swappable and can be populated as required to suit the power demands and configuration of the system.



Monolithic magnetic digital isolators designed for hybrids



Fully monolithic digital isolators, which have low power dissipation, can be used to replace opto-couplers in isolation functions, as line voltage window comparators or as isolated RS422 receivers, isolated relay drives and isolated wired-or alarms.

The couplers are failsafe and DC-stable but, unlike optocouplers, have no intrinsic wear out mechanism. The new range has floating coil input, which is simple to interface to any input voltage from 0.5V to 400V through a current limiting resistor. The series allows data rates of up to 40MBd and pulse width distortions of 7ns.

The MSOP package option makes this range one of the smallest isolators available. The isolator is also available in a single die for easy mounting on hybrids. The range offers isolation of up to 2500V rms in PDIP and SOIC packages and 1000V rms in an MSOP package.

There are two output configurations, CMOS and open drain for wire-or connection. Approval to UL1577 and IEC061010 is pending. www.rhopoint.co.uk

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1.83

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AT/HP 4191A 1000HHz Impedance Analyser AT/HP 4192A 13MHz Impedance Analyser AT/HP 4193A 110HHz Impedance Analyser FREQUENCY COUNTERS AT/HP 5345A 500MHz Frequency Counter AT/HP 5345A 500Hz Frequency Counter AT/HP 5350B 20GHz Frequency Counter AT/HP 5351B/001 26.5GHz Frequency Counter AT/HP 5351B/001 26.5GHz Frequency Counter AT/HP 5352B 40GHz Frequency Counter AT/HP 5352B 40GHz Frequency Counter AT/HP 5370A 100MHz Universal Time Interval Counter AT/HP 5370B 100MHz Universal Time Interval Counter AT/HP 3370A 100MHz Function Generator AT/HP 3312A 500MHz Frequency/Time Interval Analyser FUNCTION GENERATORS AT/HP 33120A/001 ISMHz Function Generator AT/HP 3315A 81MHz Function Generator AT/HP 3315A 50MHz Function Generator AT/HP 311A 20MHz Function Generator AT/HP 8116A 50MHz Function Generator AT/HP 8116A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator Time 8094A/001/002/003/004 600kHz Function Generator Philips PM5193 50MHz Function Generator Tek AWG2005 20MS/S Arbitrary Wavform Generator Fek AWG201/02 125MHz 250MS/S Dual Arb Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with D50 AT/HP 1660A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660A 500MHz Timing 100MHz State 136Ch AT/HP 1664A 18GHz Detector AT/HP 1664A 18GHz Detector AT/HP 11664A 18GHz Detector AT/HP 15689A 150MHz 50 Ohm S-parameter Test Set AT/HP 3587A 150Hz 50 Ohm S-parameter Test Set AT/HP 3587A 150HHz 50 Ohm S-parameter Test Set AT/HP 3587A 150MHz Network/Spectrum Analyser	GBP)	(
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AT/HP 5350B 20GHz Frequency Counter AT/HP 5351B/001 26.5GHz Frequency Counter AT/HP 5352B 40GHz Frequency Counter AT/HP 5352B 40GHz Frequency Counter AT/HP 5352B 100MHz Universal Time Interval Counter AT/HP 5370B 100MHz Universal Time Interval Counter AT/HP 5372A 500MHz Frequency/Time Interval Analyser FUNCTION GENERATORS AT/HP 3245A DC-IMHz Function Generator AT/HP 3120A/001 ISMHz Function/Arbitrary Waveform Gen AT/HP 3325B 21MHz Function Generator AT/HP 3325B 21MHz Function Generator AT/HP 3325B 21MHz Function Generator AT/HP 8111A 20MHz Function Generator AT/HP 8116A 50MHz Function Generator AT/HP 8116A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator AT/HP 8153 50MHz Function Generator Tek AWG2005 20MS/S Arbitrary Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D 500MHz Timing 100MHz State 136Ch AT/HP 1670D 500MHz Timing 100MHz State 136Ch AT/HP 1670D 500MHz Sto Ohm S Parameter Test Set AT/HP 1664A 18GHz Detector AT/HP 1664A 150 Ohm S-parameter Test Set AT/HP 35677A 200MHz 50 Ohm S-parameter Test Set AT/HP 35677A 150MHz S0 Ohm S-parameter Test Set AT/HP 35078 A 150MHz S0 Ohm S-parameter Test Set AT/HP 35077A 200Hz Set Ohm S-parameter Test Set AT/HP 35077A 150Hz 200 Ohm S-parameter Test Set AT/HP 35077A 150Hz 200 Ohm S-parameter Test Set AT/HP 35077A 150Hz 200Hz Detector AT/HP 850258 26.5GHz Coaxial Detector AT/HP 850258 26.5GHz Coaxial Detector	1150	
AT/HP 5351B/001 26.5GHz Frequency Counter AT/HP 5352B 40GHz Frequency Counter AT/HP 5352B 40GHz Frequency Counter AT/HP 5352B 100MHz Universal Time Interval Counter AT/HP 5370B 100MHz Universal Time Interval Counter AT/HP 5372A 500MHz Frequency/Time Interval Analyser FUNCTION GENERATORS AT/HP 3245A DC-1MHz Function Generator AT/HP 33120A/001 15MHz Function/Arbitrary Waveform Gen AT/HP 3325B 21MHz Function Generator AT/HP 3325B 21MHz Function Generator AT/HP 3325B 21MHz Function Generator AT/HP 8111A 20MHz Function Generator AT/HP 8116A 50MHz Function Generator AT/HP 8116A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator Tek AWG2005 20MS/S Arbitrary Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670D 500MHz Timing 100MHz State 136Ch AT/HP 1670A S00MHz Timing 100MHz State 136Ch AT/HP 1670A 18GHz Detector AT/HP 1664A 18GHz Detector AT/HP 1664A 18GHz Detector AT/HP 1664A 150 Ohm S Parameter Test Set AT/HP 1664A 150 Ohm S Parameter Test Set AT/HP 35677A 200MHz 50 Ohm S Parameter Test Set AT/HP 35677A 150MHz 50 Ohm S Parameter Test Set AT/HP 35077A 150Hz Sector Network Analyser AT/HP 85025B 0.01-50GHz Detector AT/HP 85025B 0.01-50GHz Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85027B 18GHz N-1 Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	3950	
AT/HP 53528 40GHz Frequency Counter AT/HP 53528 40GHz Frequency Counter AT/HP 53508 100MHz Universal Time Interval Counter AT/HP 53708 100MHz Universal Time Interval Counter AT/HP 53708 100MHz Universal Time Interval Analyser FUNCTION GENERATORS AT/HP 3245A DC-IMHz Function Generator AT/HP 33120A/001 15MHz Function/Arbitrary Waveform Gen AT/HP 3325B 21MHz Function Generator AT/HP 3325B 21MHz Function Generator AT/HP 3325B 21MHz Function Generator AT/HP 8111A 20MHz Function Generator AT/HP 8116A 50MHz Function Generator AT/HP 8116A 50MHz Function Generator AT/HP 8153 50MHz Function Generator AT/HP 8153 50MHz Function Generator Tek AWG2005 20M5/S Arbitrary Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D 500MHz Timing 100MHz State 136Ch AT/HP 1670D 500MHz Sto Ohm S Parameter Test Set AT/HP 35677A 150MHz 50 Ohm S Parameter Test Set AT/HP 35677A 150MHz 50 Ohm S-parameter Test Set AT/HP 35078 A 150MHz Network/Spectrum Analyser AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85027A 18GHz N-1 Directional Bridge AT/HP 85027A 18GHz N-1 Directional Bridge	1860	
AT/HP 5352B/005 46GHz Frequency Counter AT/HP 5370A 100MHz Universal Time Interval Counter AT/HP 5370B 100MHz Universal Time Interval Counter AT/HP 5372A 500MHz Frequency/Time Interval Analyser FUNCTION GENERATORS AT/HP 3245A DC-IMHz Function Generator AT/HP 3120A/001 15MHz Function/Arbitrary Waveform Gen AT/HP 3325B 21MHz Function Generator AT/HP 3335A 81MHz Function Generator AT/HP 8111A 20MHz Function Generator AT/HP 8116A 50MHz Function Generator AT/HP 8116A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator Tek AWG2005 20M5/S Arbitrary Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670D 500MHz Timing 100MHz State 136Ch AT/HP 1670A 500MHz Sto Ohm S Parameter Test Set AT/HP 35677A 200MHz 50 Ohm S Parameter Test Set AT/HP 35677A 150MHz 50 Ohm S-parameter Test Set AT/HP 35078 A 150MHz Network/Spectrum Analyser AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85027A 18GHz N-1 Directional Bridge AT/HP 85027A 18GHz N-1 Directional Bridge	2300	
AT/HP 5370A 100MHz Universal Time Interval Counter AT/HP 5370B 100MHz Universal Time Interval Counter AT/HP 5372A 500MHz Frequency/Time Interval Analyser FUNCTION GENERATORS AT/HP 3245A DC-IMHz Function Generator AT/HP 32120A/001 15MHz Function/Arbitrary Waveform Gen AT/HP 3325B 21MHz Function Generator AT/HP 3335A 81MHz Function Generator AT/HP 8111A 20MHz Function Generator AT/HP 8111A 20MHz Function Generator AT/HP 8116A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator Tek AWG2005 20MS/S Arbitrary Wavform Generator Tek AWG2005 20MS/S Arbitrary Wavform Generator Tek AWG2021/02 125MHz 520MS/S Dual Arb Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1660A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670A 500MHz Sto Ohm S Parameter Test Set AT/HP 1664A 180Hz Detector AT/HP 1664A 150MHz 50 Ohm S-parameter Test Set AT/HP 35677A 200MHz Sector Network Analyser AT/HP 3577A 5Hz-200MHz Vector Network Analyser AT/HP 35078 150MHz S0 Ohm S-parameter Test Set AT/HP 35078 150MHz S0 Ohm S-parameter Test Set AT/HP 35078 150MHz S0 Ohm S-parameter Test Set AT/HP 35078 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85027A 18GHz N-1 Directional Bridge AT/HP 85027A 18GHz N-1 Directional Bridge	2550	
AT/HP 53708 100MHz Universal Time Interval Counter AT/HP 5372A 500MHz Frequency/Time Interval Analyser FUNCTION GENERATORS AT/HP 3245A DC-IMHz Function Generator AT/HP 3120A/001 ISMHz Function Generator AT/HP 3325B 21MHz Function Generator AT/HP 3325B 21MHz Function Generator AT/HP 811A 20MHz Function Generator AT/HP 811A 20MHz Function Generator AT/HP 811A 20MHz Function Generator AT/HP 816A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator AT/HP 8004A/001/002/003/004 600KHz Function Generator Philips PM5193 50MHz Function Generator Tek AWG2005 20M5/S Arbitrary Wavform Generator Tek AWG2021/02 125MHz 250M5/S Dual Arb Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with D50 AT/HP 1660A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670Z 500MHz Timing 100MHz State 136Ch AT/HP 1670A S00MHz Timing 100MHz State 136Ch AT/HP 1670A 500MHz Timing 100MHz State 136Ch AT/HP 1664A 18GHz Detector AT/HP 35677A 200MHz 50 Ohm S-parameter Test Set AT/HP 35677A 150MHz 50 Ohm S-parameter Test Set AT/HP 35025B 26.5GHz Coaxial Detector AT/HP 35025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector	2950	
AT/HP 5372A 500MHz Frequency/Time Interval Analyser FUNCTION GENERATORS AT/HP 3245A DC-IMHz Function Generator AT/HP 33120A/001 ISMHz Function/Arbitrary Waveform Gen AT/HP 3325B 21MHz Function Generator AT/HP 3325B 21MHz Function Generator AT/HP 8111A 20MHz Function Generator AT/HP 8111A 20MHz Function Generator AT/HP 8116A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator AT/HP 804A/001/002/003/004 600KHz Function Generator Philips PM5193 50MHz Function Generator Tek AWG2005 20MS/S Arbitrary Waveform Generator Tek AWG2005 20MS/S Arbitrary Waveform Generator Tek AWG202 1/02 125MHz 250MS/S Dual Arb Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with D50 AT/HP 1660A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670D 500MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1670A 500MHz Timing 100MHz State 136Ch AT/HP 1664A 18GHz Detector AT/HP 1664A 18GHz Detector AT/HP 1664A 18GHz Detector AT/HP 1664A 150 MHz 50 Ohm S-parameter Test Set AT/HP 35677A 200MHz 50 Ohm S-parameter Test Set AT/HP 35025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector	1250	
FUNCTION GENERATORS AT/HP 3245A DC-IMHz Function Generator AT/HP 33120A/001 ISMHz Function/Arbitrary Waveform Gen AT/HP 3325B 21MHz Function Generator AT/HP 3325B 21MHz Function Generator AT/HP 8111A 20MHz Function Generator AT/HP 8116A 50MHz Function Generator AT/HP 816A 50MHz Function Generator AT/HP 816A 50MHz Function Generator AT/HP 804A/001/002/003/004 600kHz Function Generator Philips PM5193 50MHz Function Generator Tek AWG2005 20M5/S Arbitrary Waveform Generator Tek AWG2021/02 125MHz 250M5/S Dual Arb Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with D50 AT/HP 1652B 100MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1670A 500MHz Timing 100MHz State 136Ch AT/HP 1670A S00MHz Timing 100MHz State 136Ch AT/HP 1670B 500MHz Timing 100MHz State 136Ch AT/HP 1664A 18GHz Detector AT/HP 35677A 200MHz 50 Ohm S-parameter Test Set AT/HP 35677A 100MHz 50 Ohm S-parameter Test Set AT/HP 35025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85027A 18GHz N-f Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	1 500	
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AT/HP 33120A/OOI ISMHZ Function/Arbitrary Waveform Gen AT/HP 3325B 21MHz Function Generator AT/HP 3325B 21MHz Function Generator AT/HP 3335A 81MHz Function Generator AT/HP 8111A 20MHz Function Generator AT/HP 8116A S0MHz Function Generator AT/HP 8165A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator AT/HP 804A/001/002/003/004 600kHz Function Generator Philips PM5193 50MHz Function Generator Tek AWG2005 20M5/S Arbitrary Waveform Generator Tek AWG2005 20M5/S Arbitrary Waveform Generator LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1660A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660A 500MHz Timing 100MHz State 136Ch Ana AT/HP 1660A 500MHz Timing 100MHz State 136Ch AT/HP 167D/030 250MHz Timing 100MHz State 136Ch AT/HP 167DG 500MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1670A ANALYSERS AT/HP 1664A 18GHz Detector AT/HP 1664A 18GHz Detector AT/HP 1664E 0.01-26.5GHz Detector AT/HP 1664E 0.01-26.5GHz Detector AT/HP 35677A 200MHz 50 Ohm S-parameter Test Set AT/HP 35677A 150MHz S0 Ohm S-parameter Test Set AT/HP 35025B 26.5GHz Coaxial Detector AT/HP 35025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector		
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AT/HP 8116A 50MHz Function Generator AT/HP 8165A 50MHz Function Generator AT/HP 8904A/001/002/003/004 600kHz Function Generator Philips PM5193 50MHz Function Generator Tek AWG2005 20MS/S Arbitrary Wavform Generator Tek AWG201/02 125MHz 250MS/S Dual Arb Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1652B 100MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1670A State 136Ch AT/HP 1664A 18GHz Detector AT/HP 1664A 18GHz Detector AT/HP 35677A 200MHz 50 Ohm S Parameter Test Set AT/HP 35677A 150MHz 50 Ohm S Parameter Test Set AT/HP 35077A 51Hz-200MHz Vector Network Analyser AT/HP 35025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85027A 18GHz N-1 Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	1650	
AT/HP 8165A 50MHz Function Generator AT/HP 8904A/001/002/003/004 600kHz Function Generator Philips PM5193 50MHz Function Generator Tek AWG2005 20MS/S Arbitrary Waveform Generator Tek AWG201/02 125MHz 250MS/S Dual Arb Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1652B 100MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1662A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136 Ch AT/HP 1670G 500MHz Timing 100MHz State 136 Ch AT/HP 1670A State 136Ch AT/HP 1664A 18GHz Detector AT/HP 1664A 18GHz Detector AT/HP 1664A 150MHz S0 Ohm S Parameter Test Set AT/HP 3567A 150MHz S0 Ohm S Parameter Test Set AT/HP 3507A 500Hz StoChz Network Analyser AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85027A 18GHz N-1 Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	1150	
AT/HP 8904A/001/002/003/004 600kHz Function Generator Philips PM5193 50MHz Function Generator Tek AWG2005 20M5/S Arbitrary Waveform Generator Tek AWG201/02 125MHz 250M5/S Dual Arb Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1652B 100MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 68Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1670G S00MHz Timing 100MHz State 136Ch AT/HP 1670G S00MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1664A 18GHz Detector AT/HP 3507A 18GHz Detector AT/HP 3567A 150MHz S0 Ohm S Parameter Test Set AT/HP 3577A 5Hz-200MHz Sector Network Analyser AT/HP 3507B 150MHz S0 Ohm S-parameter Test Set AT/HP 3507B 150MHz S0 Ohm S-parameter Test Set AT/HP 3507B 150MHz S0 Ohm S-parameter Test Set AT/HP 3507B 26.5GHz Coaxial Detector AT/HP 85025B 0.01-50GHz Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85027A 18GHz N-1 Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	1895	
Philips PM5193 50MHz Function Generator Tek AWG2005 20MS/S Arbitrary Waveform Generator Tek AWG201/02 125MHz 250MS/S Dual Arb Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1650A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 68Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 68Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 68Ch Log Ana AT/HP 1670G 500MHz Timing 150MHz State 136 Ch AT/HP 1670G 500MHz Timing 150MHz State 136 Ch AT/HP 1670G 500MHz Timing 150MHz State 136 Ch AT/HP 1670G 500MHz State 136 Ch AT/HP 1664A 18GHz Detector AT/HP 1664A 18GHz Detector AT/HP 1664A 18GHz Detector AT/HP 35677A 200MHz 50 Ohm S Parameter Test Set AT/HP 3577A 5Hz-200MHz Sector Network Analyser AT/HP 35078 150MHz Network/Spectrum Analyser AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 0.01-50GHz Detector AT/HP 85027A 18GHz N-1 Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	1350	
Tek AWG2005 20MS/S Arbitrary Waveform Generator Tek AWG2021/02 125MHz 250MS/S Dual Arb Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1650A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1662A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136 Ch AT/HP 1670G 500MHz Timing 100MHz State 136 Ch AT/HP 1670G 500MHz Timing 100MHz State 136 Ch AT/HP 1674D 200MHz State 136 Ch AT/HP 1664A 18GHz Detector AT/HP 1664A 18GHz Detector AT/HP 1664A 150MHz 50 Ohm S Parameter Test Set AT/HP 3567A 150MHz 50 Ohm S Parameter Test Set AT/HP 3577A 5Hz-200MHz Vector Network Analyser AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85027A 18GHz N-1 Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	2950	
Tek AWG2021/02 125MHz 250MS/s Dual Arb Waveform Gen LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1650A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1662A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 150MHz State 136 Ch AT/HP 1674A 18GHz Detector AT/HP 11664A 18GHz Detector AT/HP 11664A 18GHz Detector AT/HP 1667EA 200MHz 50 Ohm S Parameter Test Set AT/HP 3567A 150MHz S0 Ohm S Parameter Test Set AT/HP 3577A SHz-200MHz Vector Network Analyser AT/HP 35025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85027A 18GHz N-1 Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	1750	
LOGIC ANALYSERS AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1650A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1662A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 150MHz State 136 Ch AT/HP 1664A 18GHz Detector AT/HP 11664E 0.01-26.5GHz Detector AT/HP 35677A 200MHz 50 Ohm S Parameter Test Set AT/HP 35078A 150MHz Network/Spectrum Analyser AT/HP 35025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Directional Bridge AT/HP 85027A 18GHz N-f Directional Bridge	5950	
AT/HP 1652B 100MHz Timing 35MHz State 80Ch with DSO AT/HP 1660A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1662A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 150MHz State 136 Ch AT/HP 1664A 18GHz Detector AT/HP 11664A 18GHz Detector AT/HP 11664E 0.01-26.5GHz Detector AT/HP 35677A 200MHz 50 Ohm S Parameter Test Set AT/HP 35678A 150MHz Network/Spectrum Analyser AT/HP 35025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85027A 18GHz N-f Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	3730	
AT/HP 1660A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1662A 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 150MHz State 136 Ch AT/HP 1670G 500MHz Timing 150MHz State 136 Ch AT/HP 1670G S00MHz Timing 150MHz State 136 Ch AT/HP 1670G S00MHz Timing 150MHz State 136 Ch AT/HP 1640A 18GHz Detector AT/HP 11664A 18GHz Detector AT/HP 11664E 0.01-26.5GHz Detector AT/HP 35677A 200MHz 50 Ohm S Parameter Test Set AT/HP 35689A 150MHz S0 Ohm S-parameter Test Set AT/HP 3577A SHz-200MHz Vector Network Analyser AT/HP 35078 150MHz Network/Spectrum Analyser AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85027A 18GHz N-1 Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	2150	
AT/HP 1660C 500MHz Timing 100MHz State 136Ch Log Ana AT/HP 1662A 500MHz Timing 100MHz State 68Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 150MHz State 136 Ch AT/HP 1670G 500MHz Timing 150MHz State 136 Ch AT/HP 1642A 18GHz Detector AT/HP 11664A 18GHz Detector AT/HP 11664E 0.01-26.5GHz Detector AT/HP 11664E 0.01-26.5GHz Detector AT/HP 35677A 200MHz 50 Ohm S Parameter Test Set AT/HP 35689A 150MHz Network/Spectrum Analyser AT/HP 35025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Detector AT/HP 85027A 18GHz N-f Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	2550	
AT/HP 1662A 500MHz Timing 100MHz State 68Ch Log Ana AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 150MHz State 136 Ch AT/HP 12423A SCSI Bus Preprocessor NETWORK ANALYSERS AT/HP 11664A 18GHz Detector AT/HP 11664E 0.01-26.5GHz Detector AT/HP 35677A 200MHz 50 Ohm S-parameter Test Set AT/HP 35677A 200MHz Vector Network Analyser AT/HP 3577A SH2-200MHz Vector Network Analyser AT/HP 35025B 26.5GHz Caxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector	2850	
AT/HP 1670D/030 250MHz Timing 100MHz State 136Ch AT/HP 1670G 500MHz Timing 150MHz State 136 Ch AT/HP E2423A SCSI Bus Preprocessor NETWORK ANALYSERS AT/HP 11664A 18GHz Detector AT/HP 11664E 0.01-26.5GHz Detector AT/HP 35677A 200MHz 50 Ohm S-parameter Test Set AT/HP 35678A 150MHz 50 Ohm S-parameter Test Set AT/HP 35689A 150MHz Vector Network Analyser AT/HP 35025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85027A 18GHz N-f Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	2350	
AT/HP 1670G 500MHz Timing 150MHz State 136 Ch AT/HP E2423A SCSI Bus Preprocessor NETWORK ANALYSERS AT/HP 11664A 18GHz Detector AT/HP 11664E 0.01-26.5GHz Detector AT/HP 35677A 200MHz 50 Ohm S Parameter Test Set AT/HP 35689A 150MHz 50 Ohm S-parameter Test Set AT/HP 3577A 5Hz-200MHz Vector Network Analyser AT/HP 3589A 150MHz Network/Spectrum Analyser AT/HP 3589A 150MHz Network/Spectrum Analyser AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025D 0.01-S0GHz Detector AT/HP 85027A 18GHz N-f Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	3750	
AT/HP E2423A SCSI Bus Preprocessor NETWORK ANALYSERS AT/HP 11664A 18GHz Detector AT/HP 11664E 0.01-26.5GHz Detector AT/HP 35677A 200MHz 50 Ohm S Parameter Test Set AT/HP 35689A 150MHz 50 Ohm S-parameter Test Set AT/HP 3577A 5Hz-200MHz Vector Network Analyser AT/HP 3589A 150MHz Network/Spectrum Analyser AT/HP 3589A 150MHz Network/Spectrum Analyser AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025D 0.01-S0GHz Detector AT/HP 85027A 18GHz N-f Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	4550	
AT/HP 11664A 18GHz Detector AT/HP 11664E 0.01-26.5GHz Detector AT/HP 35677A 200HHz 50 Ohm S Parameter Test Set AT/HP 35689A 150MHz 50 Ohm S-parameter Test Set AT/HP 3577A 5Hz-200HHz Vector Network Analyser AT/HP 3589A 150MHz Network/Spectrum Analyser AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025D 0.01-50GHz Detector AT/HP 85027A 18GHz N-f Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	100	
AT/HP 11664E 0.01-26.5GHz Detector AT/HP 35677A 200HHz 50 Ohm S Parameter Test Set AT/HP 35689A 150HHz 50 Ohm S-parameter Test Set AT/HP 3577A SHz-200HHz Vector Network Analyser AT/HP 3589A 150HHz Network/Spectrum Analyser AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025D 0.01-50GHz Detector AT/HP 85027A 18GHz N-f Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge		
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AT/HP 35689A ISOMHz S0 Ohm S-parameter Test Set AT/HP 3577A SHz-200MHz Vector Network Analyser AT/HP 3589A ISOMHz Network/Spectrum Analyser AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025D 0.01-S0GHz Detector AT/HP 85027A I8GHz N-f Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	435	
AT/HP 3577A SHz-200MHz Vector Network Analyser AT/HP 3589A 150MHz Network/Spectrum Analyser AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025D 0.01-50GHz Detector AT/HP 85027A 18GHz N-f Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	1895	
AT/HP 3589A ISOMHz Network/Spectrum Analyser AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025D 0.01-50GHz Detector AT/HP 85027A I8GHz N-f Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	1 500	
AT/HP 85025B 26.5GHz Coaxial Detector AT/HP 85025D 0.01-50GHz Detector AT/HP 85027A 18GHz N-f Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	3950	
AT/HP 85025D 0.01-50GHz Detector AT/HP 85027A 18GHz N-f Directional Bridge AT/HP 85027B 26.5GHz Directional Bridge	6250	
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I		Anritsu 68047C 10MHz-20GHz Synthesised Signal Generator	8525	341
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