

# ELECTRONICS WORLD

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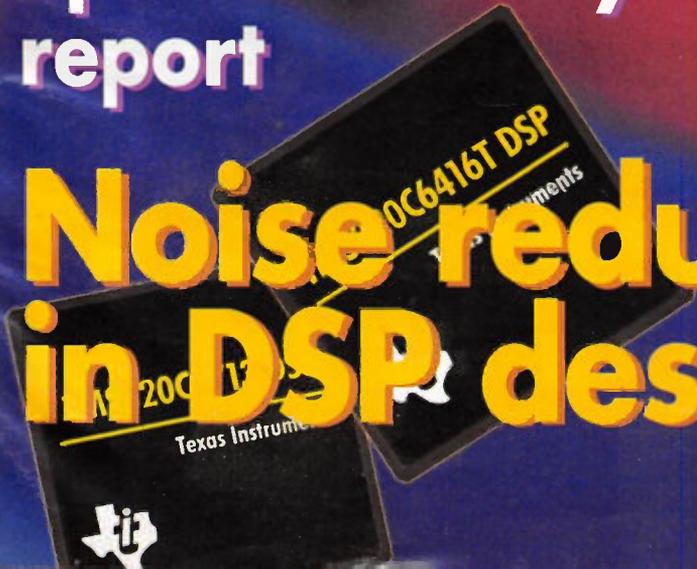


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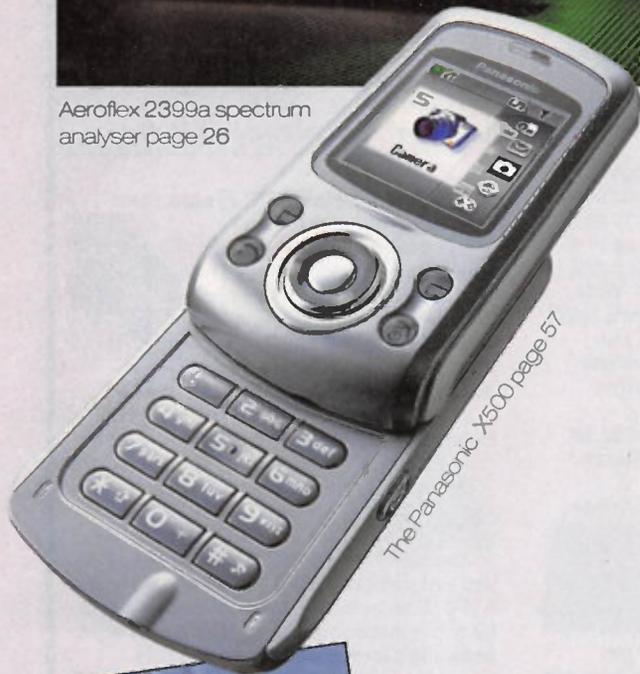
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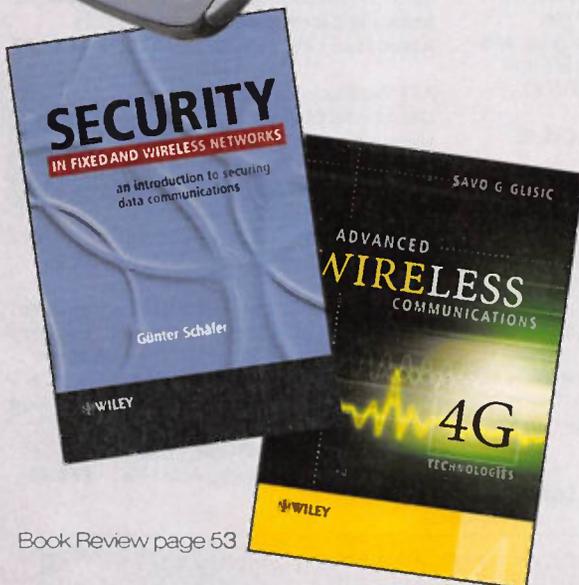
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 Kit Order Code: 3166KT - £14.95  
 Assembled Order Code: AS3166 - £24.95



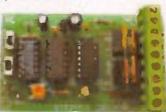
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#### NEW! Bi-Polar Stepper Motor Driver

Drive any bi-polar stepper motor using externally supplied 5V levels for stepping and direction control. These usually come from software running on a computer. Supply: 8-30V DC. PCB: 75x85mm.  
 Kit Order Code: 3158KT - £12.95  
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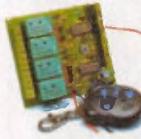
Most items are available in kit form (KT suffix) or assembled and ready for use (AS prefix).

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 Kit Order Code: 3145KT - £19.95  
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 Additional DS1820 Sensors - £3.95 each



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 Kit Order Code: 3108KT - £54.95  
 Assembled Order Code: AS3108 - £64.95



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 Kit Order Code: 3142KT - £41.95  
 Assembled Order Code: AS3142 - £51.95



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Uses serial port and any standard terminal comms program. 4 LED's display the status. ZIF sockets not included. Supply: 16-18VDC.  
 Kit Order Code: 3123KT - £29.95  
 Assembled Order Code: AS3123 - £34.95



#### NEW! USB & Serial Port PIC Programmer

USB/Serial connection. Header cable for ICSP. Free Windows software. See website for PICs supported. ZIF Socket/USB Plug A-B lead extra. Supply: 18VDC.  
 Kit Order Code: 3149CKT - £34.95  
 Assembled Order Code: AS3149C - £49.95



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# Time will take its course

“Designers do not spend enough time on the power sources at the outset of their designs,” you hear battery suppliers cry out (see ‘Specifying batteries early’ in this issue). Duracell has even commissioned a survey, involving some 150 design-companies across Germany, France and the UK to unlock the secrets behind the designer’s decisions of selecting and developing power supply systems. Its research has concluded that designers are not using most suitable power sources when developing the next generation of portable digital devices. Furthermore, according to the survey, the key driving factors during the design process are technology advancements (88% of respondents), followed by safety and legislation (51%), usage patterns (50%) and retailer demand (27%). Surprisingly, cost seems to be way down on the list.

The survey goes on to state that only 48% of designers are considering battery technology in the R&D phase. Of these, 55% design the device around the battery. But is that enough, considering the importance users place on long battery life for their portable devices?

Duracell, Varta and other battery suppliers now resort to marketing and the press to evangelise and convince developers of the importance of good power supply design and selecting the right battery source, when the design is still on the drawing board.

However, the situation, I must say, smacks of déjà vu. Only a few years ago, it

was the power supply makers that complained of exactly the same ailment that had afflicted the design community: Designers were not spending enough time and effort on creating the optimum power supply for their systems, instead leaving this task for the last moment.

Fortunately, what was once the blight of the power supply makers seems to be remedying itself. At board level, the use of so many different ICs, powered by different voltages, has given appearance to different power supply architectures. This in turn, requires a lot more knowledge – and, therefore, time – from the designers, from the very beginning of the design.

I wonder if the situation in the battery market is not likely to go the same way. As different technologies start appearing, each with its own specific power requirements and yet all of them belonging to the same portable solution, it is likely that engineers will start to think about batteries and power supplies from the word go.

And, in turn, as the market becomes more complex, there will be a bigger choice of batteries. From the designers’ point of view, it’ll be imperative to look at power sources much earlier in the design process.

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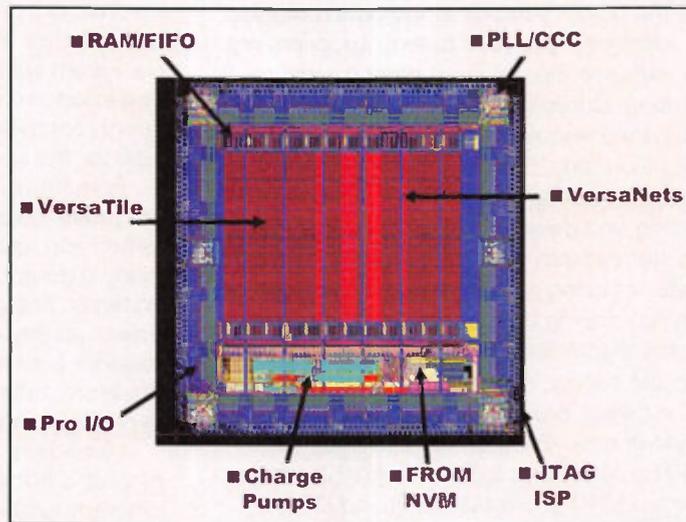
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# Actel launches flash-based FPGA with ISP

Flashless firm Actel, better known for its anti-fuse FPGAs, has launched a series of flash-based programmable devices with an ISP capability, in an assault on Xilinx and Altera's SRAM-based offerings. "Most of the FPGAs supplied today are SRAM-based or hybrids. But in our FPGAs we only use flash cells as the switching fabric. The flash cell does the programming and the switching," said Martin Mason, director of flash technology at Actel.

Actel's new proASIC3 and ProASIC3E families are the third series of flash-based FPGAs in Actel's product portfolio but this time they are offering in-system programmability (ISP), high gate counts and security features aimed at the industries that need these capabilities but at very low costs, such as automotive and consumer.

"You'd think that SRAM-based FPGAs are low cost, but that is not the case. Programming requires addi-



Die layout of the proASIC3 device from Actel

tional memory, which adds 75 cents to the bill-of-materials of SRAM devices. The FPGA is not live until the microprocessor powers up and clocks. So, for SRAM FPGAs you'll need some sort of clocking circuitry too, which also adds to the cost of the device. Then, any kind of noise of the power supply could affect the SRAM, so you'll need [a] brown-out [circuit]. You don't

need any of these with flash-based FPGAs," he added. The ProASIC3 families are also said not to suffer from errors in the configuration fabric - firm errors - as SRAM devices might do.

Actel's ProASIC3 devices offer operation of up to 350MHz, and meet the 64-bit, 66MHz PCI benchmark. Even though deemed 'value chips', selling at prices of below \$10,

the Actel FPGAs offer 1kbit of user flash memory on chip.

In addition to these features, Actel has maximised the benefits from having a non-volatile memory on board, by adding security capabilities. For example, the devices can be programmed with plain text, they can be programmed in-house with an AES key and then shipped to a manufacturer, or they can be re-programmed remotely in the field using AES encrypted programming file. "This opens up all sorts of opportunities to us, which will not be available to the SRAM devices.

Historically, the consumer space has not been dominated by FPGAs because of the security factor. Now that is likely to change with our families," said Mason.

The proASIC3 families will be made by Infineon in Dresden, Germany, in 130nm, 7-metal layer process technology.

The families come with their own set of development tools.

## Rose Electronics pins down remote 'cursors' with UltraLink phase 2

US-based developer of KVM (keyboard, video, mouse) solutions has announced the phase 2 of the UltraLink remote access-and-control system.

Rose Electronics's hardware, consisting of switches, routers and hubs, is augmented by the facility to allow authorised users to remotely access,

monitor and control servers or workstations via the KVM port, which could be an Internet Protocol (IP) or Cat 5 connection. This is UltraLink. However, up until phase 2, UltraLink used to suffer from practical problems, mainly related to the time discrepancy between the mouse click and the cursor position on screen, caused by

the remote access delay. By the time the mouse click was relayed to the monitoring server's screen, the position of the cursor on the monitored computer could have changed.

Rose Electronics's developers have devised a proprietary digital filtering and phase detecting algorithms that, in a nutshell, capture the cursor's

position first and send only that information across to the controlled server before the rest of the screen is captured, to pre-empt the cursor's movement before the mouse click arrives. The time delay in this instance is only 25ms, sufficient for tasks to be completed as intended without any practical 'gafts'.

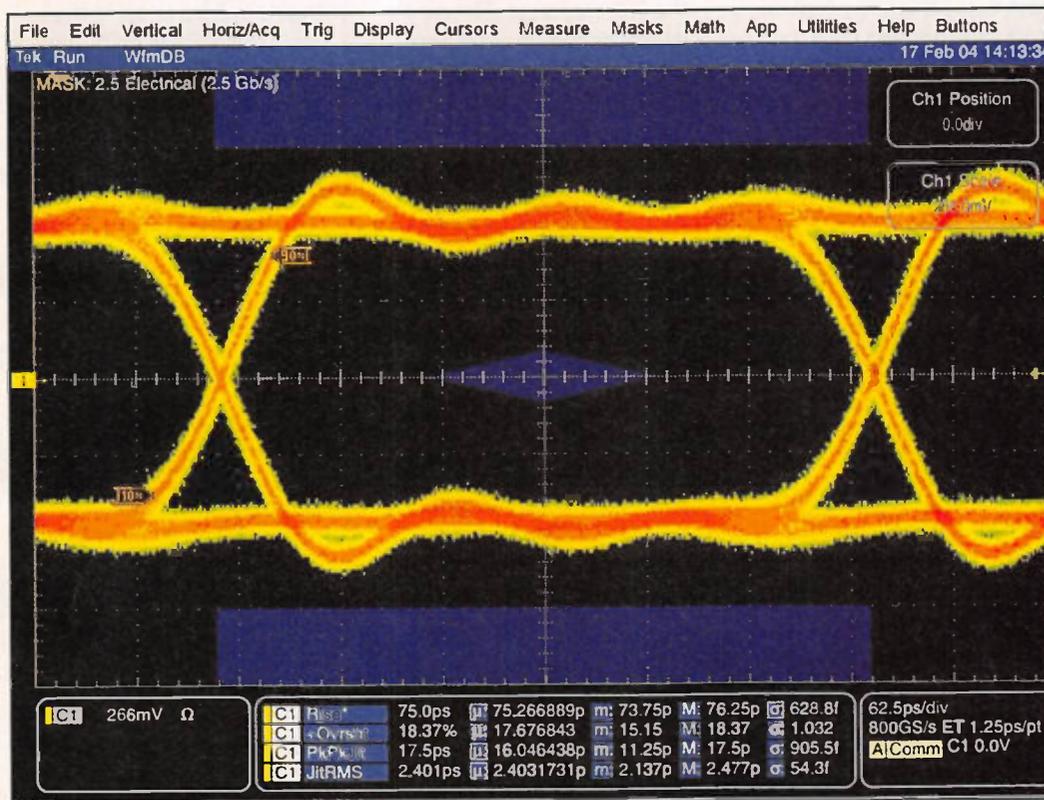
# Tektronix sets a new industry standard

Tektronix has introduced a new series of high-end oscilloscopes that promises to set the standard for the rest of the industry. The TDS6124C and TDS6154C have been launched in response to the changes seen in the ways and speeds that data is being transferred, especially with the proliferation of serial data applications that exceed

the hardware but the software too. So we had to focus on the complete solution."

The TDS6124C offers analogue bandwidth of up to 12GHz and the TDS6154C of up to 15GHz. Their performance is closely tied to IBM's SiGe technology at their core. Tektronix has used IBM's SiGe before, in its last series of oscilloscopes, but IBM's third

analysis tool for current and emerging serial data standards. They sample rates of 40GS/s on two channels simultaneously and up to 64M of optional record length on two channels (2M on four channels standard). This is equal to a time window of 1.6ms at full bandwidth and 25ps sample interval, which enables one of the best resolu-



10Gbps, such as 10Gig Ethernet, XFP/XFI and CEI (Common Electrical I/O).

"It's become very important to focus on serial data applications. Data rates have gone up exponentially," said John Jager, EMEA sales director of design and manufacturing at Tektronix. "To solve issues related to measuring such high data rates you not only need

SiGe process generation – 7HP – promises to deliver even better performances in the future.

The instruments are deemed the fastest real-time oscilloscopes in the world today, but also the most capable, offering not only the highest bandwidth, but also longest record length and timing resolution, lowest noise floor and a thoroughly comprehensive

analysis tool for current and emerging serial data standards. The random jitter noise floor is a typical 420fs.

TDS6154C can capture the first harmonic of the clock for serial data standards and the critical third harmonic up to 10Gbps. TDS6124C is able to measure rise times of 40ps within 3% accuracy.

The two instruments will sell at \$100,000 and \$125,000 respectively.

Microchip implants for arms have already received an acceptance from club goers. A Scottish nightclub – Bar Soba in Glasgow – is the first in the UK to offer this facility, which acts as a digital wallet and saves customers from carrying cash. Each VeriChip has a unique ID number, which allows entry to the club and an individual bar account. It is inserted by medical professionals and automatically scanned when the customer enters the bar.

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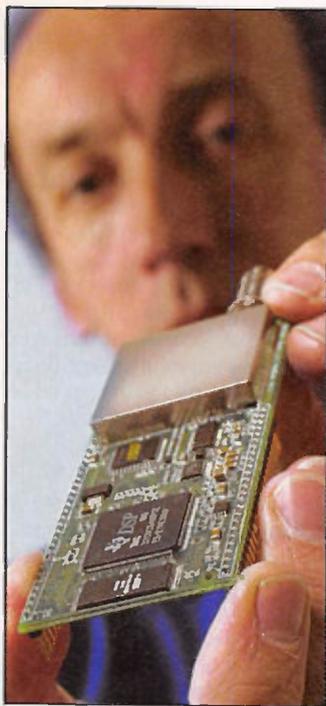
Lab-on-a-chip technology is finally making its mark within the MicroElectroMechanical Systems (MEMS) industry, according to In-Stat. Revenues of lab-on-a-chip devices are forecast to increase at CAGR of 31.2% through 2008, with unit shipments nearly quadrupling over the same period. The application earmarked for growth is the emerging field of clinical diagnostics, where lab-on-a-chip will allow physicians to diagnose infectious diseases, including certain cancers, much more rapidly than they're able to now.

Ω

TES (Technology Electronic Solutions), a full service electronic design and manufacture firm, has acquired Toulouse-based Component Analysis business from LCIE. Now TES will offer component analysis services to customers as a standalone service and as an integral part of its design and manufacturing services.

The group will be integrated into TES's CEACI (Centre of Evaluation of Information Security) group in Toulouse. CEACI provides services for the qualification of security products. It was formed in December 2004 through the acquisition of Thales Electronic Solutions (TES) business by a group of investors. The company employs over 600 people throughout France, Germany and the UK.

Ω



DAB module with Texas Instruments's chip

## Radioscape and TI to launch double-standard digital radio chip

Radioscape, London-based developer of digital radio software solutions has confirmed that it's working with Texas Instruments (TI) on the next generation of chips to deliver a combined Digital Audio Broadcasting (DAB), Digital Radio Mondiale (DRM), FM and AM receiver in one. Radioscape was one of the first companies to produce software-defined DAB modules, based on TI's DRE200 and DRE230 chips that use a DSP engine. The DSP handles all the algorithms necessary to mix down the RF

signal to an intermediate frequency (IF), digitise it, send it to the baseband hardware for synchronisation, demodulation, decoding, buffering and error-checking among other tasks.

Tackling DRM is slightly tougher, as it is a low-bit rate standard aimed at replacing the analogue signals below the 30MHz range. The modulation schemes used are 64 QAM in DRM and OFDM in DAB. DAB is broadcast in two bands: L-band (1452MHz to 1491MHz) and band III (174MHz to 240MHz).

"This will be a single DSP chip," said Nigel Oakley, RadioScape's VP of Marketing. "DRM makes things more complex, for a start you have four codecs at the outset, but we are confident that we will not experience any major snags in delivering this chip."

Although neither company confirmed which exact DSP engine will be used in the new DAB/DRAM chip, they conceded that such combined radio modules will be ready this year, and receivers on the market in time for Christmas 2005.

## Fully-differential amplifier promises high performance

Texas Instruments (TI) has unveiled a new generation of fully differential amplifiers for driving top-level performance analogue-to-digital converters (ADC). The 1.9GHz THS4509 device features fast settling time and low noise, which enable high performance from ADCs of speeds of up to 100MHz.

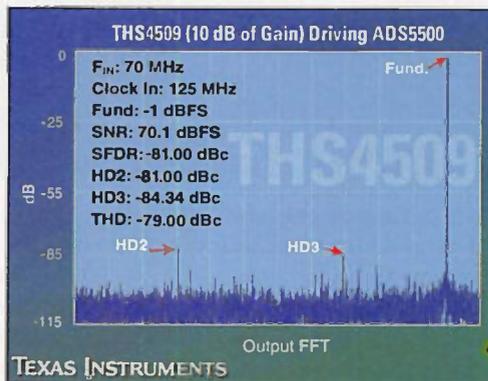
"High-speed amplifiers are the fastest growing segment of the amplifier market," confirmed Dr Carsten Oppitz, European business development manager at TI. "It will account for 30% of a \$4.6bn market in 2009. The key driving forces are wireless communication, medical imaging and high-end test and measurement markets."

TI's has used its high-speed BiCom-III complementary bipolar Silicon-Germanium

(SiGe) process (CMOS and bipolar), to deliver features such as low noise (2.0nV/rtHz), second- and third-order harmonic distortion at 70MHz of -80dBc and -87dBc (2Vpp into 200Ω load), respectively, and 1% settling time of 2ns with 2V output step.

This proprietary process allows integration of complementary NPN and PNP bipolar transistors, and hence the integration of digital logic in the high-speed devices. "High-speed amplifier is not an easy design. We used our BiCom III process

that allows the PNP transistors to have the same performance as NPN transistors – that's how good this process is," said Dr Oppitz. "This makes the THS4509 device a very fast amplifier and it is



Texas Instruments's fully-differential amplifier delivers the lowest noise and distortion

easy to use, as there's no complex compensation around it."

The THS4509 is not a single op-amp but a fully differential one: with differential inputs and differential outputs, which means getting away from two amplifiers that normally have to be balanced. Its architecture decouples the gain, output common-mode voltage and output impedance-matching issues from one another, enabling the designer to easily set them independently. In addition, the device will perform single-ended input to differential output conversion to enable DC-coupled data acquisition systems. Along with the noise and distortion performance, these features enable the designer to ensure accurate low-level signal measurements and high signal fidelity, while greatly simplifying the design process and reducing the overall solution size.

# Helped by modelling

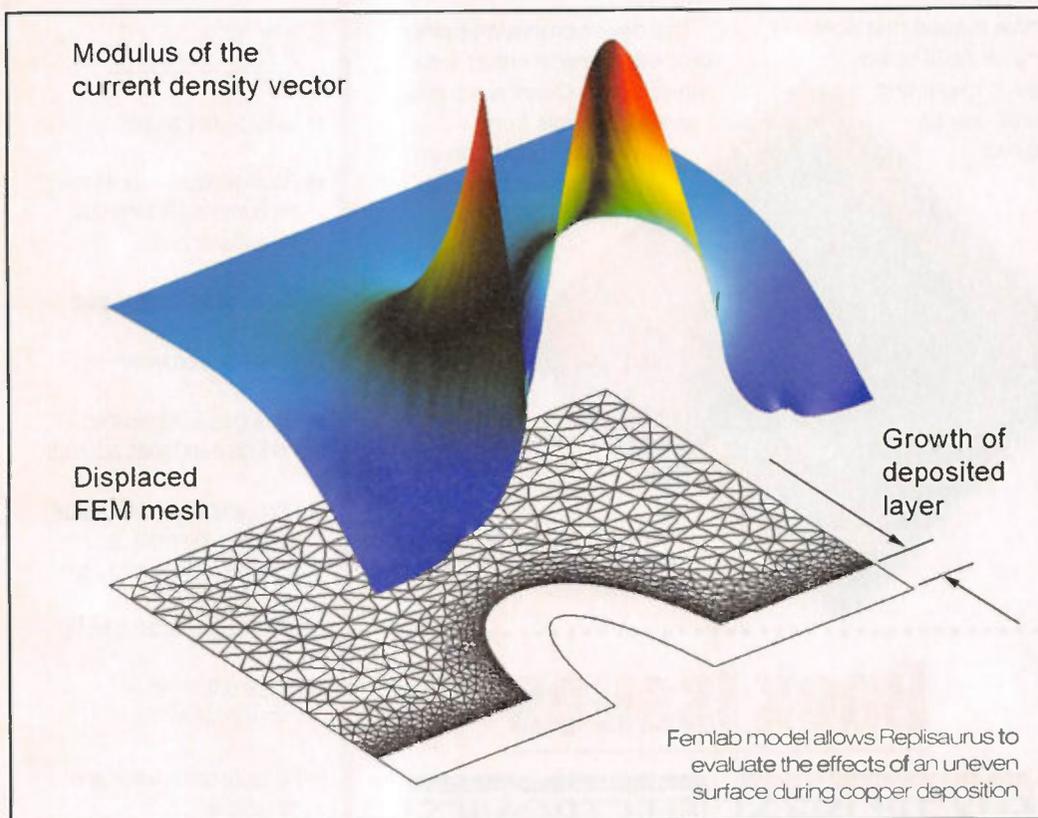
Replisaurus Technologies of Sweden has developed a unique alternative to the conventional photolithographic method of depositing copper contacts on flip-chip carrier substrates. Its electrochemical replication (ECPR) process deposits copper nearly 100 faster than conventional methods.

However, when faced with a problem of depositing copper

before committing to the time and expense of clean room trials.

The Femlab model allows for a large number of parameters such as different voltage levels, warping, substrate unevenness or different electrolyte properties. The estimations were sufficient to let Replisaurus R&D staff know whether any of their ideas were worth pursuing.

Today, it is one of the most cost-effective means of dealing with packaging and thermal issues of high-density, high-power ICs. Typically, a final wafer-processing step deposits solder beads on the chip pads, so the die package must itself have pads with positions that align with the beads. Creating these carrier substrates with photolithography can involve almost as



within cavities, where it is impossible to install monitoring instrumentation, or dealing with imperfections on the metallisation cathode, Replisaurus turned to Comsol's mathematical modelling package Femlab to optimise its technique. The software allowed the company to simulate hundreds of different process variations

"Femlab helped us to explain the phenomena we've seen in the lab," said Mikale Fredenberg, R&D manager at Replisaurus. "The information has been invaluable in debugging the process and is now helping us to refine the technique for commercial operations."

Flip-chip technology eliminates wire bonds between the silicon die and the package.

many manufacturing steps as when creating the IC itself. Replisaurus reuses a patterned master electrode as a template and provides for direct metallisation on a variety of substrates. This process can only take up to five minutes to complete. This compares to nearly 120 minutes in conventional photolithography-based metallisation.

The WiMax Forum selected Cetecom Spain as its official certification laboratory. Cetecom will act as an independent body by testing and certifying WiMax Forum member companies' products to ensure they meet the WiMax conformance and interoperability standards. "Preparation of the test lab is the last step in the process before we begin accepting equipment for certification," said WiMax Forum president Ron Resnick. Cetecom was chosen for its extensive range of testing and compliance services, including its experience in GSM/GPRS, EDGE, W-CDMA, Wi-Fi and Bluetooth among other wireless standards.

Ω

The Federation Against Software Theft (The Federation), which lists McAfee, Oracle and Sx3 as some of its members, is planning to introduce a new 'kitemark' for software licensing in the effort to tackle the growing direct and indirect software theft. The new 'kitemark' is intended to provide purchasers with a consistent and transparent agreement, to reduce any potential licence compliance confusion. John Lovelock, director general of The Federation, said: "We recognise that the industry must be proactive in helping end-users to comply with copyright laws. Software users will then have a simple and straightforward set of guidelines setting out exactly what their rights are."

Ω

A new global not-for-profit trade association has been launched that will work toward harmonising global standards and regulations in the fast developing powerline communications market. The Universal Powerline Association (UPA) brings together major players in the Powerline Communication (PLC) field to jointly work on industry standards and promote the worldwide deployment of interoperable and coexisting PLC networks for all markets and all applications. UPA has already made a move toward a networked, digital future with a 200Mbps power line product. The Association will work closely with other standardisation bodies such as the IEEE, ETSI, CENELEC and CISPR.

Ω

## New architecture is at the heart of Altera's structured ASIC

FPGA supplier Altera has used a patented technology dubbed HCell macros to deliver its next generation of structured ASIC devices – HardCopy II.

Paul Hollingworth, senior director at Altera, would not disclose the details of the architecture but he said that “each HCell has less than 15 transistors and there are no registers or multiplexers”.

Altera has been one in the growing number of companies pushing the concept of structured ASIC to designers. It says that the development of ASIC type designs is much cheaper and easier by using an FPGA board for prototyping, simulation, debugging and verification of a design, which can then easily be “mapped” onto a HardCopy device. The chip customisation is at the metal layers level, where each customer can hardwire the design as the last step. HardCopy II is made in 90nm process technology, allowing

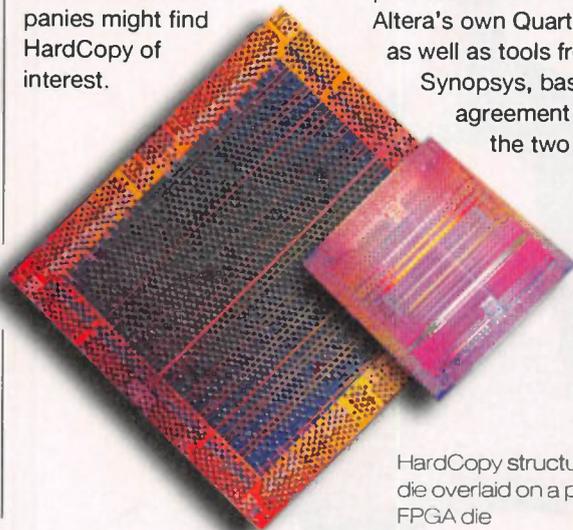
1 million gate designs. For each HardCopy II device – available with different gate counts, DSP blocks, RAM sizes, number of PLLs and user I/O – Altera offers several different versions of its FPGAs to start the development on. “You can use different prototyping vehicles to utilise the number of gates the designer needs,” said Hollingworth.

“We thought that only smaller ASSP companies might find HardCopy of interest.

Now we've found that even the larger guys – \$5bn ASSP firms – like to use HardCopy,” he added.

The logic elements in FPGAs are normally 4-input look-up tables (LUTs), but the structured ASICs are defined in standard cells. When mapping the design from an FPGA to HardCopy, the ratio of gates to LUTs is typically 12.

The development/mapping process is made easier with Altera's own Quartus II tools as well as tools from Synopsys, based on an agreement between the two firms.



HardCopy structured ASIC die overlaid on a prototype FPGA die

## ELECTRONICS WORLD

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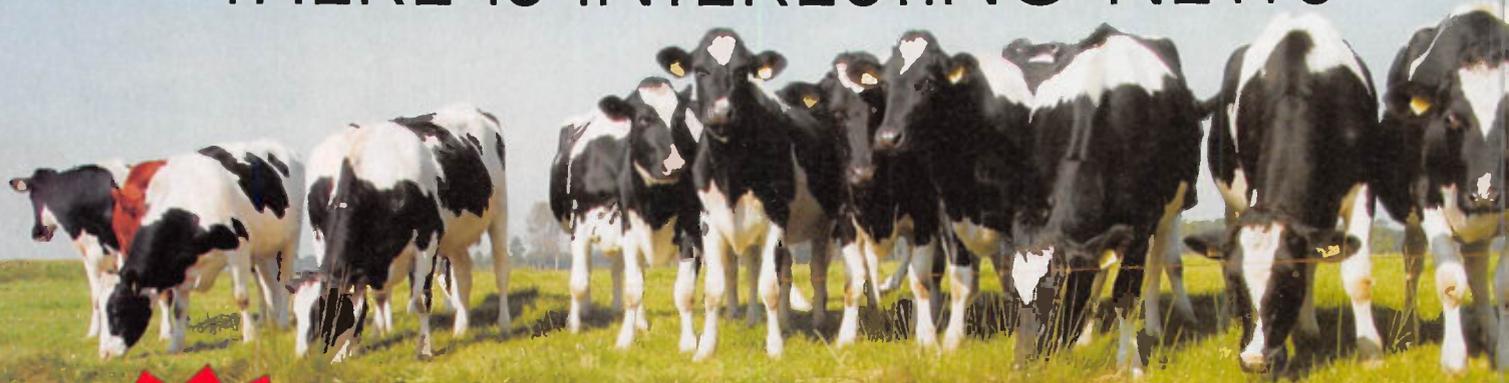
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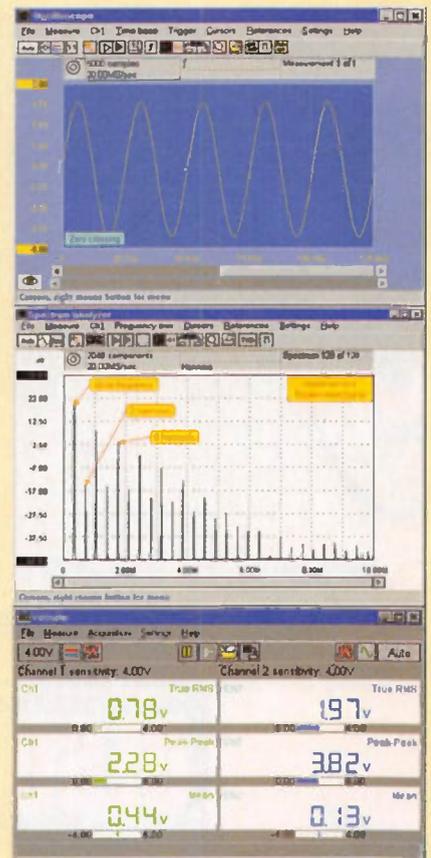
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# Specifying batteries early

Thinking of the batteries to use as soon as you start thinking of the design you'll be developing is of crucial importance, claims Gordon Clements of VARTA Microbattery

How important to the performance of a car is the capacity, efficiency and form-factor of the fuel system, as well as the type of fuel used? At what stage in the design of a car would these issues be specified?

Most designers would agree that these decisions are important enough to be considered at the outset of the design. However, this is not always the case, which could end in poor product performance and, potentially, expensive product recalls and damaged reputations. It is, therefore, vitally important to carefully consider the following key issues at the beginning of the system design.

The first decision a system designer has to make is whether the battery should be rechargeable or not. This decision is usually governed by the capacity required and the cost of the overall system. It must also be remembered that, while primary batteries are relatively low-cost, the end-user will not take kindly to replacing them on a weekly basis. Some applications may also be constrained by the lack of external charge. This is true, for example, in gas metering applications, security and remote sensing applications.

Each battery chemistry system has a defined system voltage. For example, NiMH = 1.2V; Li-ion = 3.7V; Lithium polymer = 3.7V. The designer must

decide his system voltage requirement and, where necessary, arrange cells in series in order to achieve the required level. The overall capacity required will determine the product lifecycle and will be determined largely by what the end-user will deem acceptable. This can vary enormously since the end-user of a laptop PC will quite happily accept a three-hour lifecycle, while the mobile phone user will not accept anything less than eight hours. This is the most important issue to consider, and can be the most difficult to ascertain due to the complex and multifunctional nature of many products. However, if the wrong chemistry is selected, which subsequently cannot deliver the power, the product is in trouble.

A crucial question in the design process is, how much space is available to accommodate the battery and the form-factor that is most suitable? Form-factor is largely defined by the

ergonomics of the end product and, in most applications, weight and distribution can be critical. If weight is the key differentiator for the end product, then Lithium polymer technology is the best solution. This is also true where the thickness of the end product is an important matter too, since Lithium polymer cells are available at thickness sizes of less than 3mm while conventional Lithium ion is rarely available under 5mm thick.

In small handheld devices in particular, it is becoming increasingly common for the battery to be embedded in the system, rather than be removable, either for offline charging or replacement. It would appear that there is virtually no replacement market for batteries in the

mobile phone arena. Moreover, even where a product has inherently greater value to the consumer, such as a PDA, the market for replacement batteries is relatively small.

Most battery technologies perform better when subjected to complete charge/discharge cycles. However, few products lend themselves readily to this regime. Environmental issues are an equally important consideration, particularly in relation to temperature, as this will have a dramatic effect on the efficiency of charge and there are many possible combinations here

As with charging regime, the environment in which the battery is discharged, particularly with respect to temperature and humidity, will have a big impact on

.....  
*“ Most battery technologies perform better when subjected to complete charge/discharge cycles, however, few products lend themselves readily to this regime ”*  
 .....

the performance and life expectancy of the battery.

It is important to define at the very outset of system design the features that are absolutely necessary to the success of the end product and the features that are merely desirable.

With the numerous battery design considerations possible, it is imperative that the whole area of battery requirement is examined fully at the very beginning of any design, as failure to do so can result in failure to deliver the product to market or, at a minimum, to unnecessary delays.

*Gordon Clements is General Manager at VARTA Microbattery GmbH.*

# Adding USB can be easier than you think

There is a lot of help available for adding USB functionality at the design stage, with some chips needing no specialist USB knowledge.

Steve Rogerson looks at the possibilities

When USB first appeared, it seemed a straightforward technology, a hierarchical method of connecting peripherals to a PC, and little more. But as the technology has matured, so its applications and uses have grown, creating design headaches for the makers of all the different products that now have to be USB compliant. The result has been an array of chips that use ingenious ways of creating USB connectivity or boosting USB performance.

The original USB design was a host-to-peripheral technology. The peripherals' USB communications were simple because they were designed as peripherals. Likewise, the host connectivity was more complex, but that didn't matter because just about every host was a PC and could handle such complexity. This took off as a successful connectivity technology because it worked.

The problem for USB designers started with the growth of intelligent peripherals such as cameras, PDAs and cell phones. No longer was the connection just required between them and the PC but these peripherals would want to talk to each other without going via a PC.

The change is likely to hit high-street products this year but dates back to the so-called On The Go (OTG) supplement to the USB 2.0 specification,

published in December 2001. This changes the master-slave topology of USB by letting a peripheral act, often temporarily, as a host.

"OTG is USB for mobile devices, so you can use your PDA as a host to some other device," explained Mark Saunders, USB product line director at EDA tools supplier Mentor Graphics. "This will let you connect, say, a PDA to a camera or either of them to a printer, or add a keyboard and mouse to a PDA. Or connect PDAs to PDAs."

This, however, has brought with it a number of design problems. With the PC based system, new devices would come with a driver that could be installed on the PC, but the software installed on PDAs is not in the same league as on a Pentium based system and so writing drivers for it and getting them certified has created a bottleneck for this technology.

"OTG is a step in the right direction," said Saunders, "but there will be problems for a while because these devices do not have Pentium processors."

Saunders believes that the easiest way for designers of such products to add USB functionality to their chips is opting for reusable IP (Figure 1). This route, he said, suits USB OTG applications because the configuration options vary depending on the device – a mouse and a PDA have very different

needs. Such configuration options include number of endpoints, their direction and the FIFOs, the number and size of which affects the amount of memory required by the system. If this is too high than that can mean an external device or the use of a large chunk of on-chip RAM, not desirable for the space and cost sensitive devices being talked about.

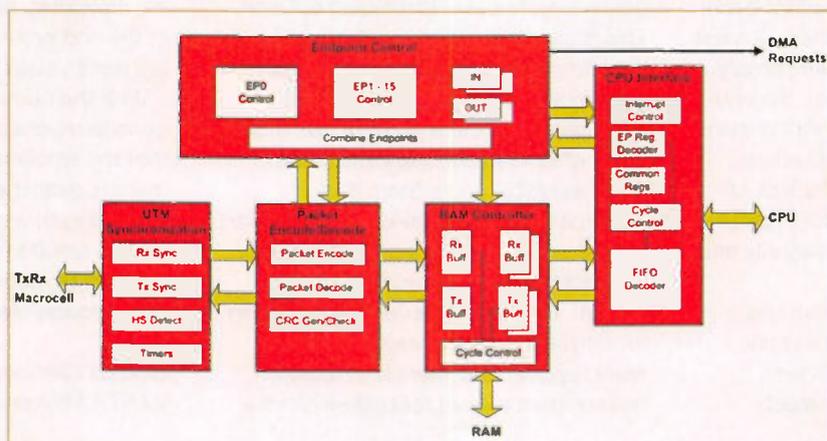


Figure 1: Mentor Graphics' MUSBHSFC core provides a USB 2.0 controller for high and full speed functions

Also, when building USB into a chip, it often runs at frequencies that are not necessarily the same as other sections. USB has a significant analogue component, which creates problems on an otherwise digital chip. There are also potential leakage problems with the technology.

Some companies get round this by using two chips with the digital logic in an ASIC and a discrete component for the analogue part. Though this can all be built into one chip, doing so could considerably reduce yield.

"The larger chips are almost always all-digital with high yield," said Jerry Johnston, a product line manager at Fairchild Semiconductor. "USB is not analogue but like analogue, and that is hard to do in the larger chips."

Nevertheless, there are companies taking that route. This is because for high volume applications, the cost of such an extra chip can be extreme, but that has to be set against the risks of integration.

"On a cell phone," said Saunders, "the extra chip is a major factor on cost and size in a market where they are trying to be cheap and small. For something less high volume, it can make sense to take the USB off chip. In time, the technology will become less risky and people will integrate it more commonly."

In the meantime, there are simple (less than 16 pins) transceiver devices available that can sit off-chip and take the USB data (which is not necessarily voltage compliant) and the I/Os for the USB line and convert that into the USB signal so it can connect with other USB devices.

One of the key advantages in such a set-up is the control of electrostatic discharge. Typically, the large 100-plus pin chips can have ESD problems. Using a transceiver protects the sections that are most vulnerable from the outside world. This is because the larger chip can be at 0.15 $\mu$ m or smaller, whereas these transceivers will be a little bit more robust at 0.35 $\mu$ m or 0.8 $\mu$ m. Though this is an extra chip, without it an additional device is often needed anyway to protect the main chip from ESD.

And some of the larger chips struggle to support a USB interface built in because of the processes with which they are made. USB uses a 3.3V bus, which is quite large for them.

"ASICs that are built on a small process often don't have the ability to handle 3.3V," said Johnston.

Adding such a transceiver should not be a difficult process. If the ASIC supports the use of such a transceiver, then it can be just dropped in. "USB has been around for eight years or so, but the market for these transceivers started to grow in the past two or three years," said Johnston. "Speed to market is one reason because using a transceiver makes the design process quicker."

Another advantage is flexibility. The needs of portable devices such as PDAs, MP3 players, cameras and so on differ and incorporating such changes in the main chip can be expensive, whereas altering the smaller extra chip is less so, and, as Johnston mentioned, quicker.

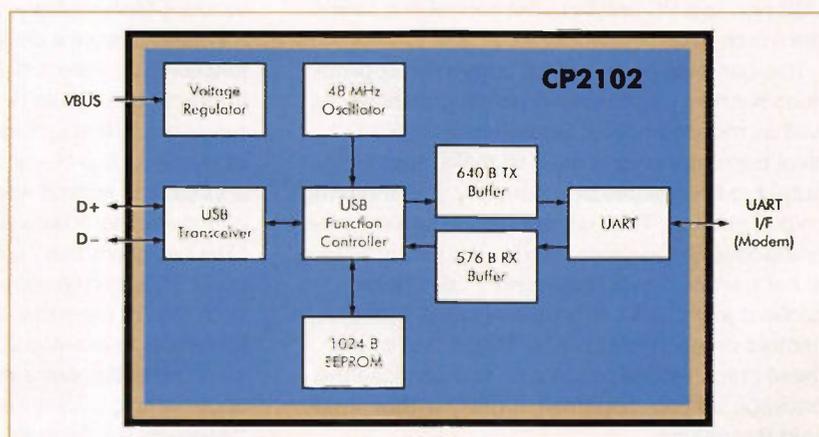
"In the portable world of phones, PDAs and so on, you need flexibility in the design," he said. "In one model they may want a high speed device, in another a low speed one is all they need."

Another way to protect USB devices from unwanted signals in the outside world is to use a switch product. When open, they let the USB signal through easily but when closed they offer protection. The main use for such chips would be in portable devices such as cell phones where there can often be ESD events between the devices and external plug-in connectors. The switch will absorb the ESD events, protecting the internal ASIC.

Another application would be a notebook computer with a docking station. Here the switch can reduce cost because the docking station would no longer need its own USB hub. It also simplifies the USB host controller inputs in the notebook.

The use of such switches is likely to grow as the high-speed USB 2.0 installations become more common. "High speed signals are quite susceptible to interference," said Johnston. "This also means it is important to keep signaling paths short. Size really does matter in these cases. Long traces can be dangerous to high speed signals."

These switches provide flexibility in terms of circuit layout. Though taking up more space than integrating the functions within the ASIC, they are



**Figure 2:** USB bridges, such as the Silicon Laboratories CP2102, can convert UART signals into USB

**Figure 3:** The Silicon Laboratories F32x microcontroller with integrated USB functionality

so small that for many applications it doesn't matter. "It is a choice," said Johnston. "There is no clear line that says you should always have it inside or outside. The designers like it outside because it gives them flexibility."

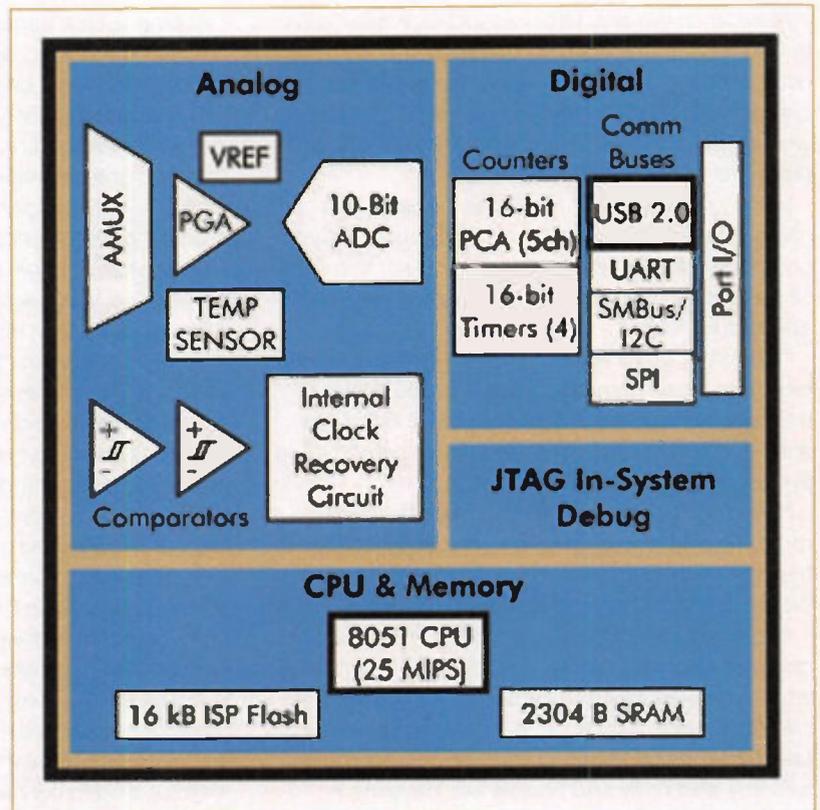
USB is also extending out from its PC base into the embedded world, but the designers who write embedded code are not used to writing drivers for Windows and other PC-type operating systems. This has led to bridge products that take an embedded UART connection and convert the signal into one compatible with USB, see Figure 2.

"This means they don't have to write the USB code for Windows," said Ross Bannatyne, marketing director for Silicon Laboratories.

A common application would be a control system running processes in a factory. A USB connection may be needed so it can be upgraded via a PC or data from it can be downloaded to a PC. Similarly, in the medical world, it can be useful for downloading captured data for analysis.

Typically, the bridge products are for upgrading legacy systems that use RS232, once the standard for PC communications but now most modem PCs no longer even have an RS232 port. "Using one of these bridges means they don't have to change any software at any end," said Bannatyne. "The drive software that comes with them makes it look like a USB port to a PC and from the controller it seems like a com port."

This can also be an aid for consumer applications such as joysticks and pointing devices, as well as mobile phones. Sometimes, an RS232 level translator chip is used to make sure the output is compatible but, normally, just the bridge chip is needed. This 5x5mm device can even be embedded in the cable head so by just attaching it, it will work. "If you buy such a cell phone cable, it just looks like a normal cable with connectors on each end, but, in fact, it has one of these chips embedded into it. You can lose the package up your fingernail, it really is that small," said Bannatyne.

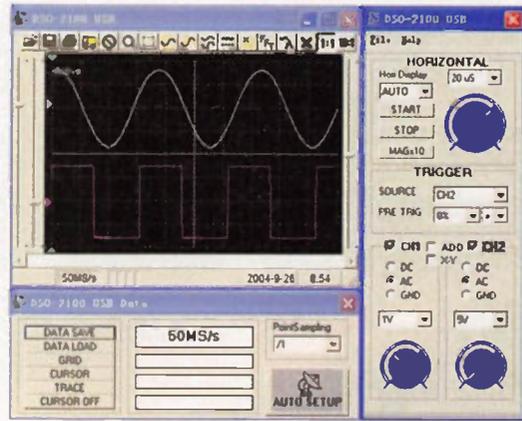


Versions of these bridges are available for particular baud rates so they can fit in with applications that require customised speeds.

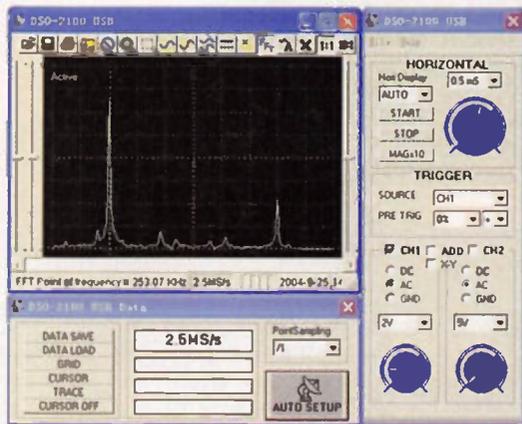
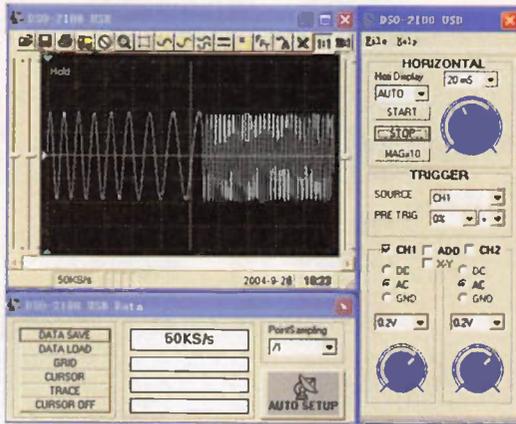
Also aimed at making life easier for designers are microcontrollers with USB functionality built in. This capability looks like any other integrated function on the chip, so all the designer has to worry about is the data in and out and not how the USB part works. "We want to make it as easy as possible so you don't have to be an USB expert," said Bannatyne.

This integration has the usual advantages of saving a separate chip, such as smaller footprint and lower power consumption. Adding an on-chip oscillator means there is no need for an external crystal. Such a chip is shown in Figure 3 and includes flash memory, digital I/O, clock and so on.

Whatever route a designer takes to add USB functionality, there is help available from the USB Implementers Forum ([www.usb.org](http://www.usb.org)). This is an active group that provides engineering support. Also available is USB design software to help write applications without worrying about the USB communications between the PC and the host. "The designers don't need to mess with any USB code. They can create a USB application without such kind of expertise. We are trying to make it easy for people to develop USB applications using standard microcontrollers without having to worry about writing USB drivers or messing with Windows," said Bannatyne.



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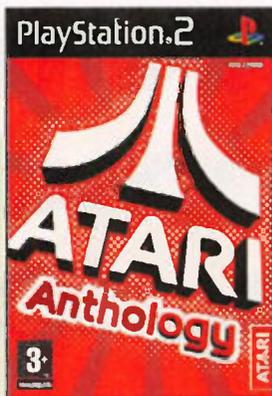
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- Self Powered USB Interface - no external PSU required
- 3rd Party application software support provided
- Hardware upgradeable over USB



## ATARI ANTHOLOGY

Xbox, PS2

★★★★☆

If you're old enough to remember the likes of Pong or Asteroids, you're going to love this collection of games from the Atari classics vault.

Age and technology advances aside, this will be either a game you play religiously or hardly ever, but what it does offer is value for money. With almost 40 games and variants of each game updated for the 21st century, you'll find yourself getting addicted all over again and waiting that little longer to make dinner, just so you can beat your previous high score.

Although not for everyone, Atari Anthology does bring classic arcade gaming to a new generation of gamer. Love it or hate it, at the very least, it's gaming the way it used to be.

## OUTLAW GOLF 2

Xbox PS2

★★★

Outlaw Golf 2 is a continuation of last year's original, with the added extra of online play for both consoles. The biggest difference year is the price. At only £19.99, there's no more complete a sports title on either format.

Improved graphics, visuals and character animations make it extremely



impressive. Each character can have more than 60 different animations for swing and the obligatory beatings!

The game's one failure, however, is its control system. There's no real feel of control over the character in either swing or putting mode, which makes the game incredibly difficult to get into and even more so to master.

## MARIO POWER TENNIS

GameCube

★★★★☆



Forget 'Game and Watch', it'll be 'Game, Set and Match' with Mario's latest sporting foray. Mario Power Tennis (MPT) is an arcade-style game where you play as one of 14 Nintendo characters across eight themed courts, ranging from Mario's factory to DK's jungle. This is a great pick-up-and-play game for people of all ages and ability.

Its simple controls allow you to beat down friends and family in multiplayer mode, or take on the single player

challenges of tournaments.

Character choice allows for varying strength, reach and speed, plus each character has two special moves that range from moves that propel them across the court in time to stop a shot, to special serves that help ace the opponent.

No Mario game would be complete without a multitude of extras and its wacky mini-games allow you to hone your skills and unlock extra features, characters and additional games.

## MECHASSAULT 2: LONE WOLF

Xbox PS2

★★★

MechAssault was a huge hit across the US, however, but the picky Europeans seemed wanting more from the original and so now it's back - with a vengeance. With a refined and improved interface,

proprietary graphics engine and immersive gameplay, 'mech' games just might start making an impact on us. With the promise of more downloadable content than we can get our hands on, you're sure to play this game more than just occasionally. Add to that the online Conquest mode that puts you in an all-out war to control the inner reaches of

the galaxy, which you have to defend and expand against real people in the real world. Addictive has a new definition.

Mech games won't appeal to all, so perhaps, Mechassault 2 might be best rented before buying.

# Wideband spectrum analysis using advanced DSP techniques

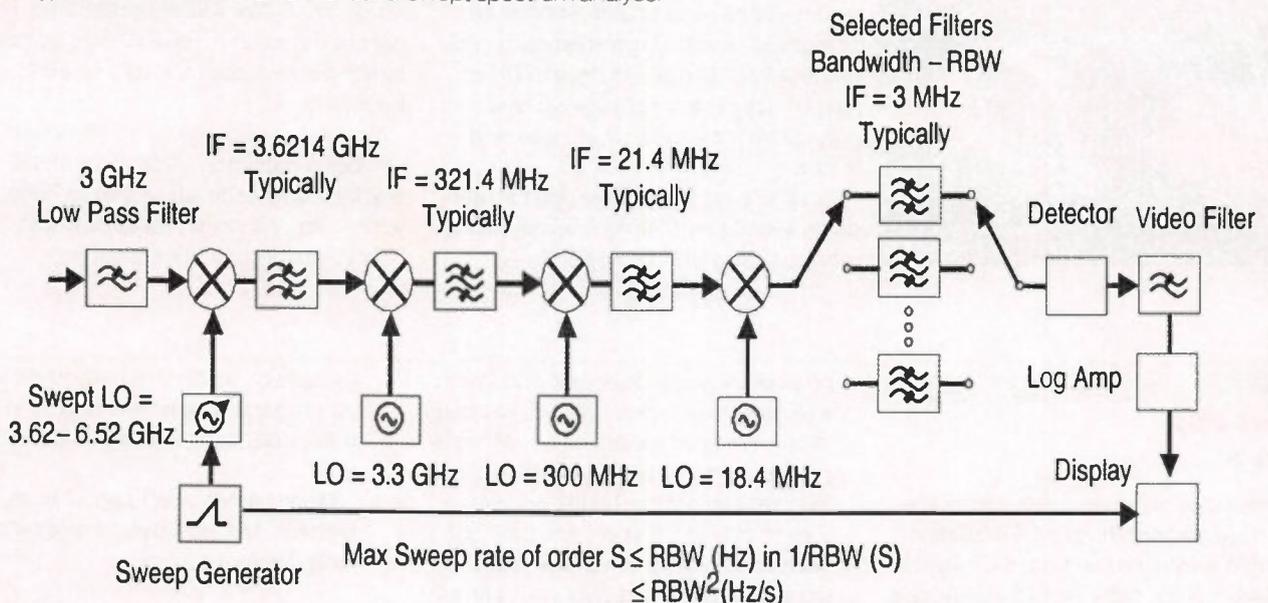
**John Lillington**, chief technology officer at RF Engines, identifies the main signal processing architectures that can be used to implement modern spectrum and signal analysis systems

Modern spectrum analysers come in a variety of different forms with widely different characteristics and price tags. It is often difficult for those unfamiliar with the terminology of spectrum analysers to understand and compare the detailed specification sheets for different classes of analyser. This is partly because the evolution of conventional swept analysers and FFT analysers have followed very different paths, aimed at different

application areas. The traditional swept spectrum analyser, for example, has, from an early stage, been aimed at RF and microwave system measurements. With the use of analogue techniques, it has been capable of performing very high frequency measurements with modest Resolution Bandwidth (RBW) requirements, down to the sub-kHz region. Digital signal processing (DSP) techniques and, in particular, Fast Fourier Transform (FFT) analysers have come from the other direction, being inherently

limited by available analogue-to-digital converter (ADC) technology, in terms of speed and dynamic range. Until recently, such techniques have been limited mainly to audio rate analysis, especially in acoustic and vibration analysis. This is because such techniques have been based on block processing (i.e. collect a block of sampled data, process, collect the next block etc.) - a different approach and terminology compared to the more continuous, throughput nature of analogue systems.

Figure 1: Typical architecture of a conventional swept spectrum analyser



One of the key limitations has been that of the dynamic range available from ADCs. High quality swept analogue analysers have been capable of Spurious Free Dynamic Ranges (SFDR) well in excess of 100dB for many years and, until recently, ADCs have simply been unable to compete except at very slow sample rates. This is why FFT analysers have been largely relegated to the audio arena.

All of this is changing rapidly, mainly due to pressure from the wireless communications community so that 16 bits with SFDR up to 100dB is now commercially available up to at least 5MS/s, 14 bits and 90dB SFDR up to at least 100MS/s. Even in the GS/s region, 10 and 12 bits are becoming readily available and this trend will accelerate, so great is the demand for DSP techniques at ever higher frequencies.

The benefit to spectrum analysis has been obvious in several areas. These are the replacement of traditional analogue RBW and Video BandWidth (VBW) filters in swept analysers with greatly improved characteristics, and the introduction of FFT techniques to improve the speed of measurements, particularly at lower RBWs. More recently, the introduction of real-time, wideband spectral analysis techniques has allowed, for the first time,

true spectral analysis of wideband burst-mode signals. These are increasingly used in communications and radar systems, and measurement of this type of signal with conventional spectrum analysers is extremely difficult, if not impossible.

## Conventional swept spectrum analyser

The two most difficult and expensive elements of such architectures (Figure 1) are the filter bank required to select the RBW and the microwave swept Local Oscillator (LO). It is standard practice to use a 1:3:10 sequence to achieve a wide range of RBWs (10Hz, 30Hz, 100Hz, 300Hz etc, up to 3MHz and above). This requires 12 different RBWs and, for the narrower RBWs, presents a very difficult filter design. In fact, for RBWs below 300Hz, it is common to go to digital techniques using a further down-conversion to a lower IF (say, 4.8kHz). This is why spectrum analysers with narrow RBW capability are also very expensive.

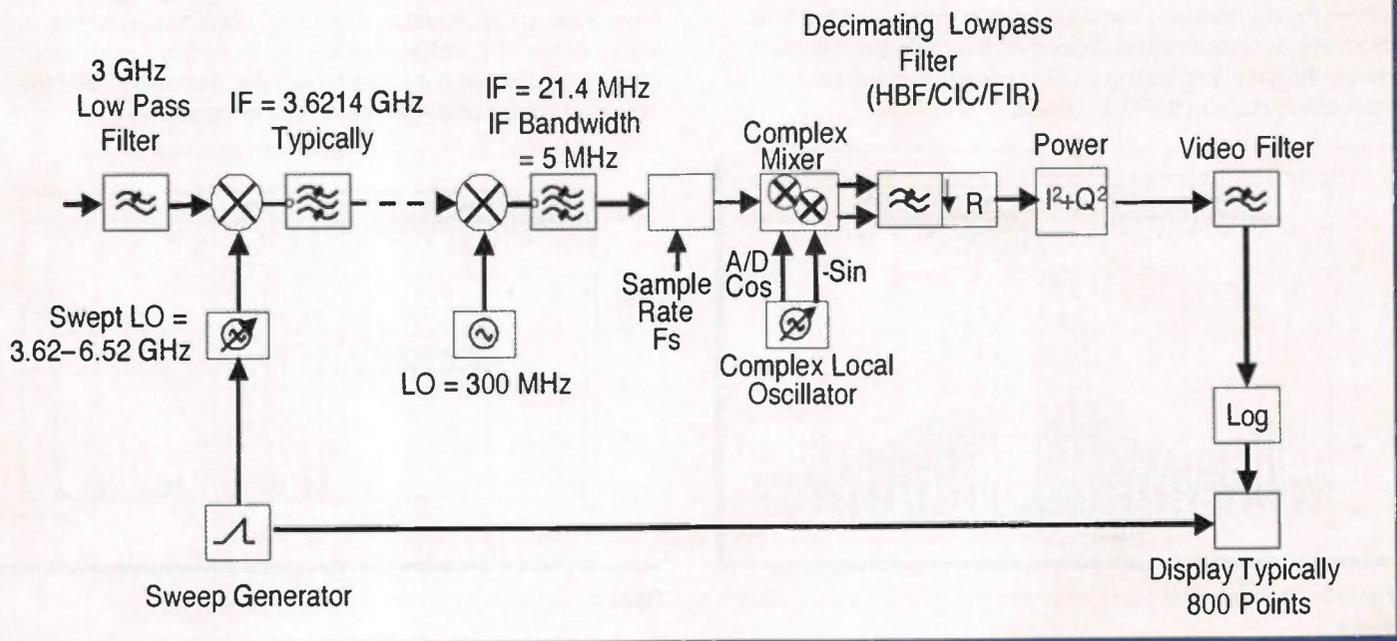
The swept LO also presents a difficult design challenge. The narrower the RBW, the more accurate the frequency sweep and, hence, the lower the oscillator phase noise has to be. It is normal, in more expensive analysers, to use a

synthesised source to achieve these objectives. For now, we will mainly consider the IF design issues since the requirement for a high quality swept LO will exist regardless of the exact nature of the IF design. It should be remembered, however, that the narrower RBWs that are achievable using digital techniques will require the use of very high quality LOs throughout the system from both centre frequency accuracy and phase noise viewpoints.

In Figure 2 the final IF section from Figure 1, from 21.4MHz onwards, is replaced by some form of digital down-converter (DDC). Firstly, the IF needs to be digitised at a suitable sample rate,  $F_s$ . There are a number of factors to take into account when making this choice, including ADC performance and anti-alias filter requirements. Further decimation of the sample rate is necessary to allow the narrower RBW filters to be realised, followed by complex to power conversion ( $I^2+Q^2$ ), video filtering and optional logarithmic conversion. All of this may be carried out in hardware (FPGA or ASIC) or in a combination of hardware and embedded software as described later.

The main advantages of using DSP techniques over the analogue approach are improved filter shapes (true

Figure 2: Modified architecture using digital downconverter IF replacement



Gaussian), more accurate and repeatable RBW and VBW values, a wider range of programmable RBW and VBW values and much easier formation of very narrow RBW values (down to 1Hz). The main limitation is the performance (signal-to-noise and SFDR) of the ADC.

The complex mixer following the ADC in Figure 2 is intended to provide a fixed down-conversion from the IF (21.4MHz) to complex baseband (I&Q). This can be done with a relatively simple process, especially if there is a simple relationship between the IF and sample frequencies (e.g.  $IF = F_s/4$ ). The down-conversion frequency could be variable which, although requiring more resources, could have certain advantages.

One possibility is to allow the sweep oscillator, which provides the first frequency conversion, to have a much coarser frequency step. In a high specification instrument, this will be a low phase-noise synthesiser-based design with a sweep of several GHz and a resolution of less than 1Hz, which results in an expensive design. This can be simplified if the synthesiser is only required to provide a coarse step (1MHz) and the fine sweep is provided in the digital IF ( $\pm 0.5$ MHz in less than 1Hz steps). In principle, this is quite easy to achieve, using standard NCO down-converter techniques, but the system designer needs to be aware of the limitations this imposes on the overall instrument performance.

## Non-realtime and realtime FFT analysers

The FFT is well established and provides a very economical solution to the spectral analysis problem. It can be viewed either as a method of transforming a block of data in the time domain to frequency domain or as a bank of filters with a response dependent on the weighting applied to the time-domain data. Figure 3 shows the equivalent set of filters (only four shown) for the particular case of a 32-point FFT with Kaiser weighting.

For some applications, it is only necessary to acquire a limited block of sampled data and transform it in 'slow time' using, for example, embedded software FFT. This might apply to cases where the signals are known to exist over long periods of time. Normally, such techniques depend on a recycling architecture where the same processing block is used to perform each successive stage of the FFT process.

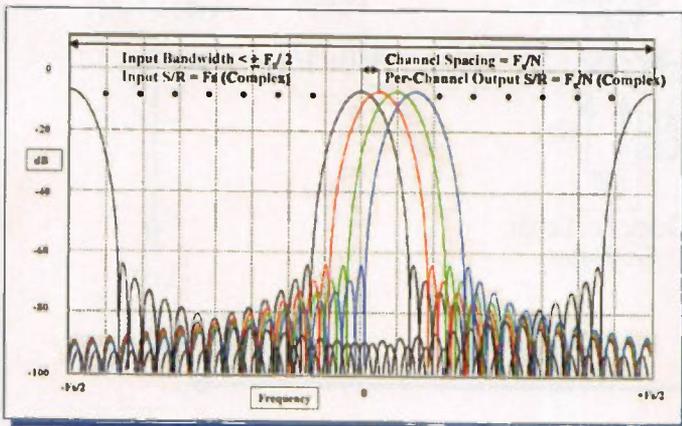


Figure 3: Equivalent filter bank using N-Point FFT (N=32) with Kaiser weighting

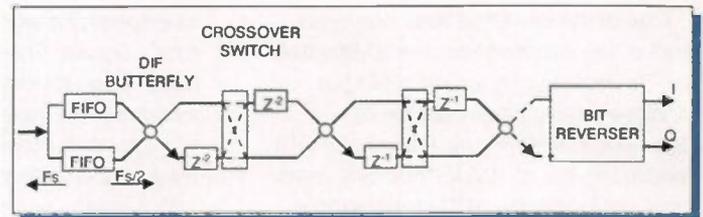


Figure 4: Example of pipelined FFT structure

For more complex signals, with time varying or transient characteristics, the use of real-time techniques becomes more desirable. The ability of the FFT processing to be able to keep up with the flow of input data, without any gaps, requires a significant increase in processing power. This is because, instead of using a recycling structure, a pipelined process is used whereby each successive stage has a dedicated processing block, organised as a pipeline (see Figure 4).

As might be expected, for an N stage process (FFT size = 2N), the throughput rate is N times that of the recycling process described above.

With a real-time system, any filtering must also take account of the transient effects since the assumption of steady-state signals is not valid (see below).

## Realtime analysers with highly selective filter banks

So far, we have only discussed FFT architectures with simple windows – that is, windows such as Kaiser and Blackman-Harris that are of the same length as the FFT itself. The degree of selectivity and bandwidth control is quite limited with this method. As can be seen from Figure 3, simple windowing can reduce the spectral sidelobe levels, but only at the expense of broadening the main lobe, giving less selectivity for closely spaced signals and increasing the Effective Noise Bandwidth (ENB).

Techniques exist that allow much sharper and narrower filters to be formed. An improvement to the filtering performance can be achieved by the use of polyphase filter banks ahead of the FFT, rather than the use of simple "windowing" of the time-domain data. The technique, generally called the "Weight Overlap and Add" or WOLA, or its subset the

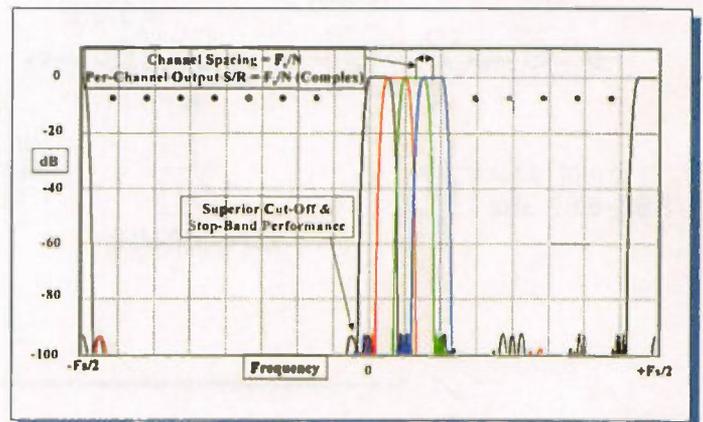


Figure 5: Typical 32 bin polyphase DFT or PFT filters

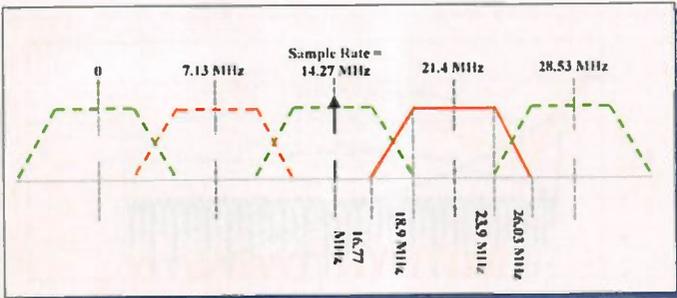


Figure 6: 21.4MHz IF with 5MHz bandwidth, under-sampled at 14.27MSPS

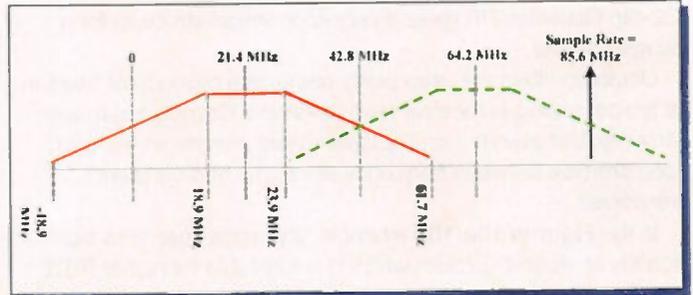


Figure 7: 21.4MHz IF with 5MHz bandwidth, sampled at 85.6MSPS

“Polyphase DFT”, is becoming more established and is certainly very efficient where large, high-quality filter banks are required. A typical 32-bin filter bank is shown in Figure 5. The improved filter shapes, compared with Figure 3, can be seen clearly.

There is a novel form of processing, known as the Pipelined Frequency Transform (PFT), which uses a different approach. Based on a “tree” structure, successive splitting and filtering of the frequency band is used to achieve a progressively finer resolution of the broad band. Advantages include the availability of simultaneous outputs from successive stages, which are at different frequency resolutions and also the ability to independently tailor the filters for different frequency bins. Furthermore, if certain frequency bins or blocks of spectrum are not required, it is simple to exclude them from the processing, leading to greater efficiency.

There is a price to be paid for this. Firstly, it requires significantly more processing power. Secondly, high selectivity in frequency corresponds to a greater latency in the time domain. This is important where transient signals are to be measured.

## Swept spectrum analysers

Here, we are considering a 5MHz bandwidth IF, centred on 21.4MHz. The same principles will apply to higher bandwidth systems at higher IF frequencies.

Dealing first with the question of sample rate, according to Nyquist,  $F_s$  needs to be at least twice the signal bandwidth. In practice, to allow for practical filter cut-off rates, at least 2.5 times is required. The resultant sample rate of at least 12.5MHz, together with an IF centre frequency of 21.4MHz is feasible and is named an ‘under-sampled’ system because the sample rate is less than the IF frequency.

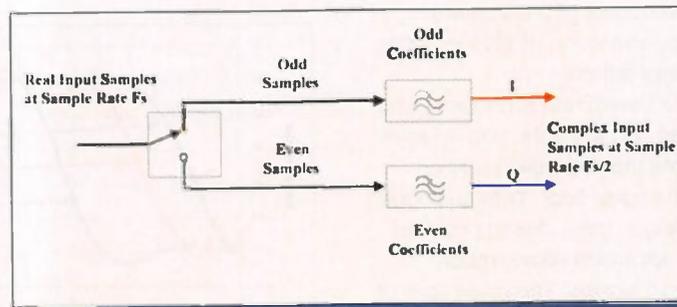


Figure 8: The halfband filter in down-convert and decimate-by-two form

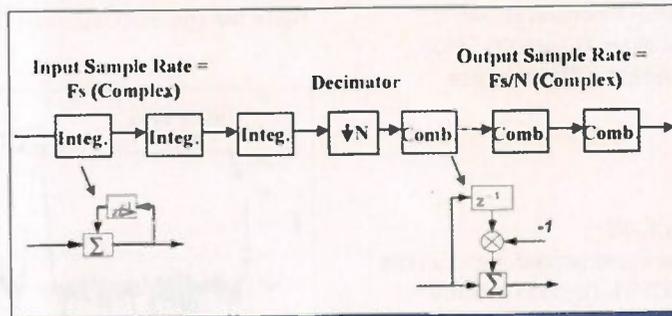


Figure 9: Schematic of a 3-stage CIC filter

There are, however, inherent problems with this plan.

Firstly, the IF filter needs to have a very sharp cut-off to avoid the alias regions centred at 14.27MHz and 28.53MHz. Various frequency plans are possible including sample rates, for example, at 17.12, 28.53, 64.2 and 85.6MS/s. The higher sample rates significantly ease the analogue anti-alias filter problems but at the expense of faster ADC’s with potentially lower SNR and SFDR as well as higher speed requirements. Figure 7 shows the case for 85.6MS/s where it may be seen that the filter transitions for the anti-alias filter, centred at 21.4MHz, are considerably easier to achieve than those shown in Figure 6.

## Down-conversion, decimation and filtering

Another benefit of the plan of Figure 7 is that the IF is now exactly equal to  $F_s/4$  which means that a very convenient and simple form of down-converter can be used to convert the real IF I&Q baseband. This takes the form of a Halfband filter in  $F_s/4$  down-convert and decimate mode and is a well-established technique. Figure 8 shows the simplified form.

Referring again to Figure 2, the initial down-conversion is followed by some form of decimating filter structure. This can be a combination of several different types of filter including cascaded integrator comb (CIC), decimating FIR and polyphase structures. For a spectrum analyser requiring a wide range of RBW values from, say, 5MHz down to 1Hz, then a very high degree of decimation is required. This may be quite simply achieved by the use of a higher order CIC filter followed by a simple Gaussian FIR filter, which may also have some decimation.

The great advantage of the CIC filter is that it is a highly efficient ‘multiplier-less’ structure, capable of very high integer decimation. An example of a 3-stage CIC is shown in Figure 9. It has been found that a five stage CIC followed by a 16-tap or

32-tap Gaussian FIR gives a very economical structure for a single channel.

Gaussian filters are used partly because a cascade of filters in a typical analogue receiver tend towards a Gaussian response anyway. But even better, Gaussian filters provide a very good compromise between frequency selectivity and transient response.

In the Figures 10a/10b example, the worst case alias side-lobe is at around -87dBc, which is acceptable for higher RBW values since this level will be at or below the system noise level.

## Results for typical swept system

Figure 11 shows an example of the output of a complete swept IF, including power and Log conversion. It also includes the effects of system noise and quantisation.

Using the usual 'rule of thumb', the sweep rate is chosen to be  $0.5 \cdot RBW^2$ . Two signals 1.5MHz apart and at 20dB relative levels can be easily distinguished here. Note that the true Gaussian shape is maintained right down to the noise floor. With analogue RBW filters, there would be much longer 'tails', due to practical filter design showing that the digital approach allows much better discrimination of closely spaced signals. The noise floor of around -100dBFS is about what would be expected for an ADC running at 85.6MS/s with an ENOB of 12 bits.

A complete core including all the DSP functions shown in Figure 2 has been implemented on a Xilinx XC2V1000 FPGA. This includes all control and data interfaces. The resource requirements are:

- Logic = 75%
- Memory = 42%
- Multipliers = 70 %

The power estimate for this core is 1.2W.

For lower cost systems, this can be implemented, for example, on a Xilinx Spartan 3 device. For a XC3S1000, the resource requirements would be:

- Logic = 61%
- Memory = 70%
- Multipliers = 83%

bearing in mind that the Spartan device has more logic but less memory and multipliers. Also, the power estimate of 413mW is much lower mainly due to the more advanced process used in the Spartan devices.

## Swept system with coarse front-end step and fine digital sweep

As discussed above, the front-end synthesiser could be significantly simplified if the fine sweep is carried out in the digital IF, leaving the microwave synthesiser to provide coarse frequency steps. Using a step of 1MHz, for example, it seems logical to use a  $\pm 0.5$ MHz sweep in the IF local oscillator. Unfortunately, this does not allow for the transient effects in the RF and digital filters, caused by the abrupt frequency change.

Figure 12 shows a floating-point simulation of the first 500 samples of a standard swept IF system. Figure 13 shows the same span but using coarse steps of 1MHz, together with a fine digital sweep of  $\pm 0.5$ MHz. The transient effects caused by the

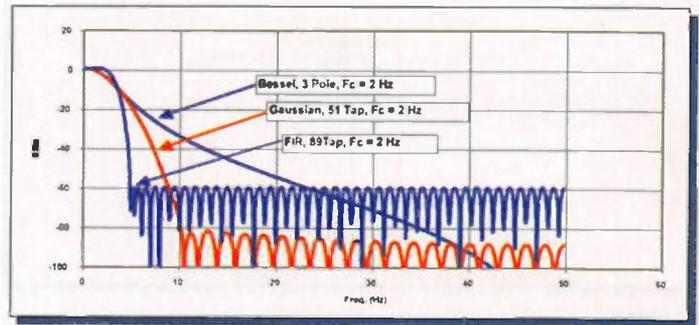


Figure 10a: Frequency response of different filter types

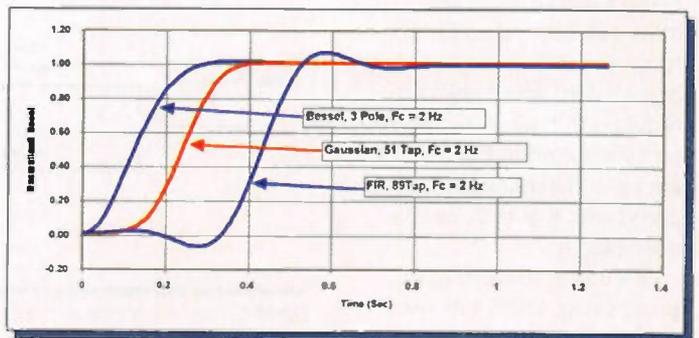


Figure 10b: Transient response of different filter types

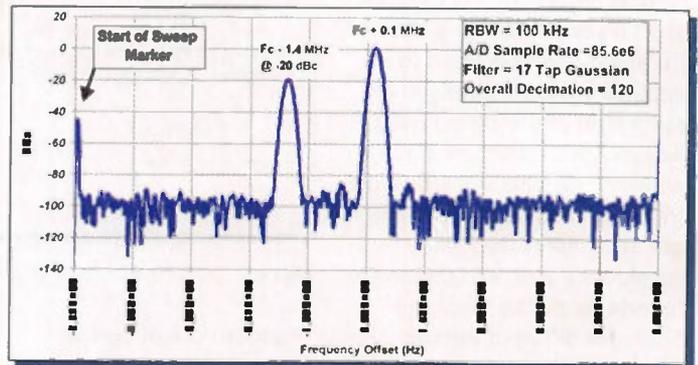


Figure 11: Swept results for span = 10MHz, decimation = 120, RBW = 100kHz, sweep rate = 5e9Hz/s

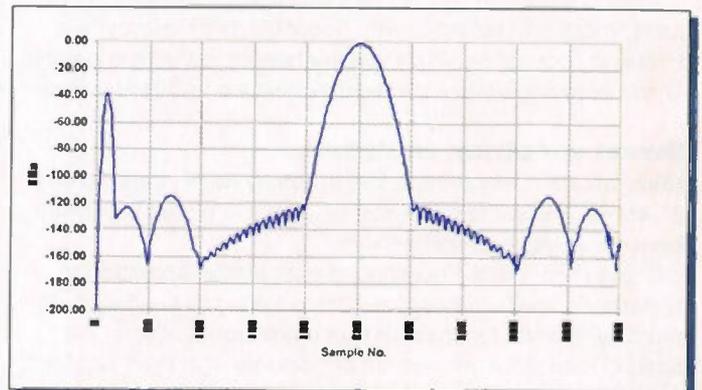


Figure 12: Floating-point simulation of standard 300kHz RBW swept system

1MHz steps are clearly seen and are due to both digital and analogue filter fill-up time. In effect, the corrupted data during the glitches cannot be recovered so the system, as it stands, is not workable.

One solution is to extend the IF sweep so that the transients occur outside the  $\pm 0.5\text{MHz}$  range. The effect of this is shown in Figure 14. A 60% 'over-sweep' has been used such that the digital IF sweep extent is now  $\pm 800\text{kHz}$  but at the same sweep rate. The glitches are still present but it now becomes possible to extract the 'good' data and reconstruct a clean signal. For the example chosen, extracting 48 samples out of each 76-sample block and 'joining' them, results in a clean signal, as in Figure 12.

It is obvious that more time is required to complete a sweep (60% more in this example). In addition, there is added complexity due to issues of timing and data extraction that need to be dealt with. Another important side issue is that it is normal to use some form of analogue bandpass pre-filtering ahead of the ADC to minimise third-order intermod effects from large signals, just outside the RBW filters. With a 1MHz stepping system, it will be necessary to have a flat passband of at least 1MHz ahead of the ADC. This will prevent the use of pre-filters so that the technique is only applicable where system cost is more important than performance.

With swept analysers, it is normal to provide a range of video filters to reduce displayed noise. It is important to distinguish

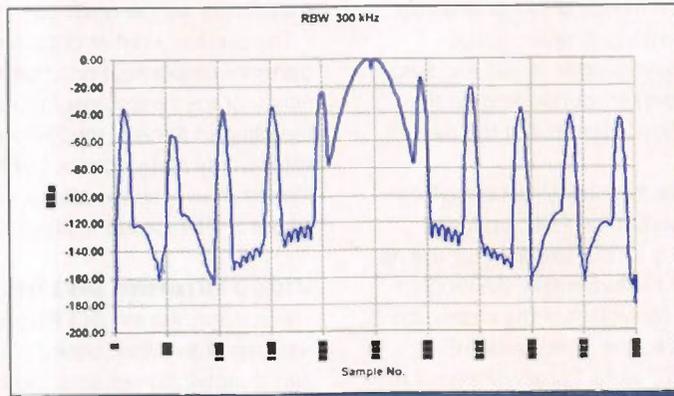


Figure 13: Effect of using 1MHz coarse steps and  $\pm 500\text{kHz}$  digital IF sweep

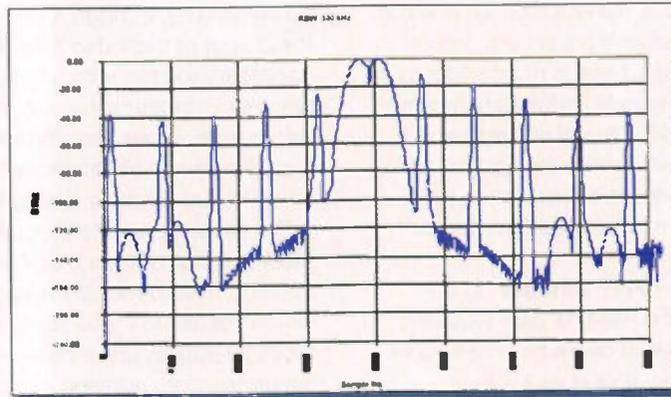


Figure 14: Effect of using 1MHz coarse steps and  $\pm 800\text{kHz}$  over-sweep

between the effects of the RBW and the VBW filters. Looked at from a frequency discrimination viewpoint, the Gaussian RBW sets the spectral selectivity and rejection of out-of-band signals. From a noise viewpoint, the RBW filter sets the equivalent noise bandwidth (ENB) and hence the noise floor of any particular measurement.

The VBW filter does neither of these things since it operates on the power of the signal. The VBW filter is required to reduce the noise variance of the signal and, as illustrated in the example of Figure 15. As can be seen, the 10kHz VBW filter does not change the response shape or the average noise floor but it does greatly reduce the noise variance, increasing the chances of detecting a small signal close to noise. It is necessary to reduce the sweep rate to an approximate value of  $0.5 \cdot \text{RBW} \cdot \text{VBW}$  (compared with  $0.5 \cdot \text{RBW}^2$  for the case without VBW filtering).

The critical properties for the VBW filter are its effective ENB and the transient response. Unlike the RBW filter, the frequency stopband performance is not very critical. A similar structure to the RBW filter may be used involving a CIC and Gaussian filter, which gives a wide range of possible VBW values. A lower order CIC and less FIR filter taps will be required in this case.

## FFT and filter bank based realtime analysers

The RF front-end for an FFT or filter bank analyser does

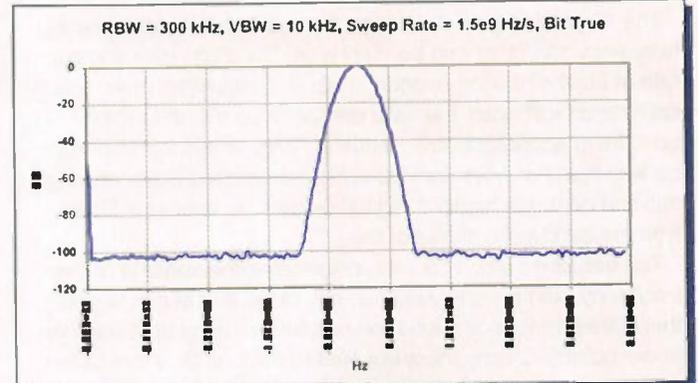
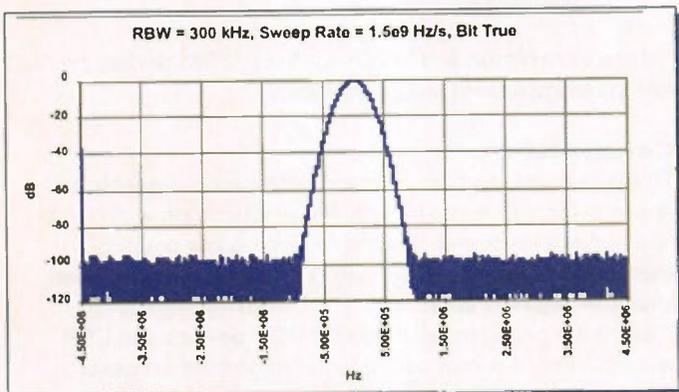


Figure 15a (left) and 15 b (right): Comparison of 300kHz RBW, with and without 10kHz VBW, span = 9MHz, sweep rate = 1.5e9Hz/s

require different characteristics from that of a swept analyser. The microwave synthesiser can be made simpler since, although the ability to set the centre of a span is still required, the frequency step can be much coarser, depending on the minimum span of the instrument. Also, there is not the same need for a linear frequency sweep.

On the other hand, a reasonably flat frequency response from the RF and IF stages is required ahead of the ADC, up to the maximum span of the instrument. Any amplitude ripple or roll-off will result in inaccuracy of the power measurement. Although it can be improved by calibration and correction of the data in the DSP, this becomes difficult to achieve over a very wide RF bandwidth. It is generally considered that FFT analysers have a lower accuracy than the best swept analysers mainly because the latter maintain a fixed centre frequency after the first frequency conversion.

The wide input bandwidth required at the ADC causes another problem when both large and small signals are present within the FFT band. Unlike the swept system, there is no pre-filter to prevent the IMD3 products of larger signals limiting the dynamic range. With swept systems, it is possible to adjust the gain of the RF chain dynamically as the signals sweep through the RBW filter. With the FFT, the gain must be set to a fixed value, determined by the largest in-band signal, which causes a potential reduction in dynamic range.

There is a crossover point at which the FFT will start to out-perform the swept system because the effect of gain switching causes transients that look very similar to oscillator phase noise.

The whole subject area of FFT techniques is vast with a multitude of algorithms for programmable DSP implementations and a number of COTS ASIC implementations readily available. The intention here is to restrict the discussion to wideband, pipelined hardware solutions, particularly those that are suitable for FPGA realisation.

One of the challenges facing the designer of a wideband, real-time FFT spectrum analyser is how to make the displayed results look similar to that of quality swept analysers. The designer has three basic parameters with which to control the effective RBW. These are the sample rate ( $F_s$ ), the transform size ( $K$ ) and the window function (e.g. uniform, Blackman-Harris, Gaussian etc). In addition, the degree of over-sampling can be important for real-time applications

The sample rate will determine the maximum instantaneous frequency span that can be displayed. For a complex sample rate of  $F_s$ , the maximum span is also  $F_s$ . However, given practical filter cut-off rates, the valid display span (i.e. the region containing acceptably low frequency alias levels) will generally be less than  $F_s$ . A typical value might be around 80%, although this can be much higher if digital, rather than analogue filters limit the bandwidth ahead of the FFT.

The transform size,  $K$  points, determines the spacing of the frequency points,  $F_s/K$ . Another way of looking at it is to note that a finer frequency resolution requires a longer time sample (more points). Clearly there is a limit to the practical size of the FFT that can be performed depending on sample rate, available silicon and memory bandwidth. Also, visually, there is little value in attempting to display more than about 1000 points so that

transforms will generally be in the range up to 2048 points.

The window is what determines the effective filter shape and transient response. For a real-time FFT system, the discussion of filters for the swept spectrum analyzer is equally applicable. It is tempting to think of the FFT as being a block process, dealing with steady state signals. For the real-time system and transient signals, however, the effects of different filters apply equally to swept or FFT-based analysers.

## Video filtering and block averaging

The output of a single FFT process will, like the swept analyser, have associated noise due to system thermal noise and quantisation effects. Some form of smoothing, similar to the video filter in swept systems, is required. In theory, it would be possible to place a video filter after the FFT. One approach would be to pass a frame of FFT, after forming the power ( $I^2+Q^2$ ), through a video filter. Since the sample rate of the output of the video filter will be decimated, it would be necessary to start with a larger FFT length. This would rapidly become impractical for very narrow VBW's and high decimation values. An alternative approach would be to filter each frequency bin across a number of FFT frames. This could be achieved as a weighted average of  $N$  frames.

The simplest approach, however, is simply to average  $N$  blocks, either using a block average or a sliding window average. The former is the easiest to compute and yields very similar results to more complex forms of filtering. In particular, block averaging using power-of-two is the easiest since it simply involves addition of power and a binary shift to achieve the division.

An estimate of a typical implementation, based on an actual "place-and-route" in a Xilinx FPGA may be helpful. The following resources apply to a 1024 point windowed FFT including complex down-conversion, input buffering, block averaging up to 256 frames and 32-bit floating point output. The ADC rate is 105MS/s at 14 bits.

To achieve this requires the following resources from a Xilinx X2V3000 FPGA (speed grade -5):

Logic = 36%  
Memory = 17%  
Multipliers = 20%

If this were placed and routed in a Virtex 2 Pro device, the ADC rate could increase to around 200MS/s.

## Conclusions

This paper has given an overview of the various spectrum analyser techniques with particular emphasis on wideband and real-time systems. It has also given some practical examples of complete DSP-based systems that have been implemented in FPGAs.

Given the great strides made in FPGA devices and DSP architectures, it is now possible to realise core-processing requirements of modern analysers in this way. This ranges from the simplest swept digital IF process to the most complex real-time filter bank based analysers.



# Selecting a spectrum analyser to suit your needs



Aeroflex 2399a spectrum analyser

Purchasing a spectrum analyser can be a costly exercise so it is important to evaluate requirements and expectations before placing an order, says **Bryan Harber**, product manager at Aeroflex

Historically, spectrum analysers were very expensive units and the province of a few 'expert' users. But today, spectrum analysers operating up to 4GHz are relatively inexpensive and nearly as commonplace as digital multimeters.

However, an analysis of the key parameters and architecture of spectrum analysers will help to ensure that the purchaser gets the right product at the right price.

Let's start with the simplest definition of a spectrum analyser: "A radio receiver with a swept local oscillator that displays frequency against amplitude on a Cartesian display".

# Spectrum analyser types

## Key parameters

The important parameters are listed here in a sensible order that can be applied to most cases; some will argue for other ways to rank the parameters. Also discussed is how spectrum analyser architectures affect some of the parameters and therefore the decision process.

➤ **Frequency** – The frequency range parameter is top of the list because this probably has the greatest effect on a key decision-making point – price! First, consider the lowest frequency of operation required and compare it to typical spectrum analyser frequency range specifications. Usually, the lowest specified frequency of operation will be between 9kHz and 100kHz, exceptionally 100Hz or even 'DC'. At the high frequency end, the range is limited by the mixing system and the need to provide adequate filtering.

There are three types of architecture employed in most spectrum analysers that are in current use:

The up/down-converter with multiple IFs – the most common low frequency system operating from a few kHz to maybe 3GHz or 4GHz. The harmonic mixer – employed almost exclusively for microwave spectrum analysers. Two versions, preselected and non-preselected, are available for operation up to 100GHz, although the highest frequency preselected mixers are limited to around 60GHz by coaxial connector systems. The highest frequency types are in waveguide.

➤ **Level range** – This will be specified by the manufacturer as "maximum input power handling, normally that of the input attenuator". Typically this is between 100mW (+20dBm) and 1W (+30dBm). The minimum level will usually be specified as the noise floor; occasionally, the minimum settable top of screen reference level will be stated.

➤ **Noise floor** – The spectrum analyser noise floor is normally described in product data sheets as "Displayed Average Noise Level" or DANL and it is the on-screen lowest noise level that can be obtained under a specified set of conditions. For example, "DANL is -115dBm between two fre-

quencies with resolution bandwidth (RBW) set to 1kHz and a video bandwidth (VBW) of 10Hz with 0dB input attenuation at 25°C". The RBW is particularly important here since we know that thermal noise is given by  $kTB$  where,  $k$  is Boltzman's constant,  $T$  is operating temperature and  $B$  is the detection bandwidth (RBW in a spectrum analyser).

In a 1kHz RBW at 25°C this equates to -144dBm and implies that the noise figure of the spectrum analyser in the above example is 29dB. This is quite normal for spectrum analysers that are usually optimised for signal handling rather than sensitivity. When comparing spectrum analysers from different manufacturers, care should be taken to compare DANL specifications on a normalised basis. Naturally, manufacturers want to show their lowest noise floor and will often specify DANL in the narrowest filter available. For example, if the spectrum analyser above has a 10Hz analogue filter then the DANL could be quoted as -135dBm in 10Hz. Other manufacturers normalise to a 1Hz bandwidth showing this as -145dBm.

All 3 values used in the above example result in the same normalised value so it is necessary to carefully extract the conditions specified.

➤ **Display range** – This is simply a statement of the product of the vertical scale range and the graticule size, normally either eight or 10 graticule steps and 10dB/division, although exceptionally, some analysers with only eight graticule steps offer 20dB/div which implies 160dB of display range. This may appear to be of benefit but see dynamic range below.

➤ **Dynamic range** – It is this parameter that causes most confusion for users; this is probably due to a misunderstanding of the accepted definition for dynamic range. The commonly accepted definition states "the ratio of the largest signal that can be handled without distortion and the analyser noise floor". This was originally a definition for high performance radio receivers and can equally well be applied to spectrum analysers.

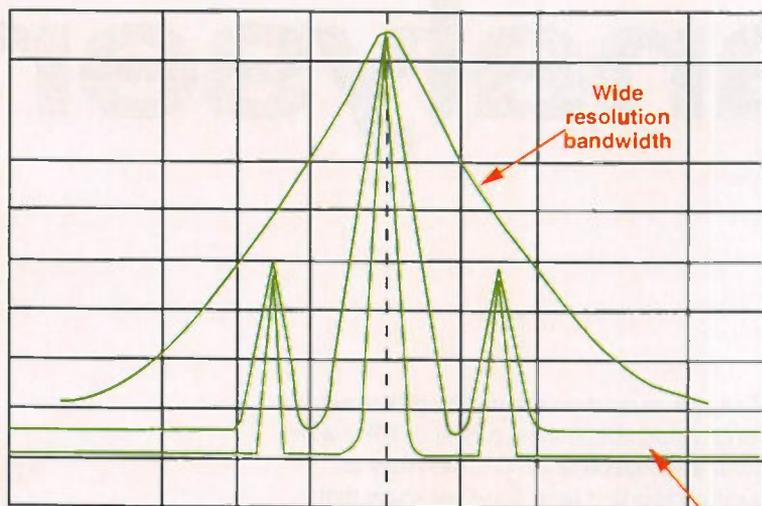


Figure 1: Resolution bandwidth

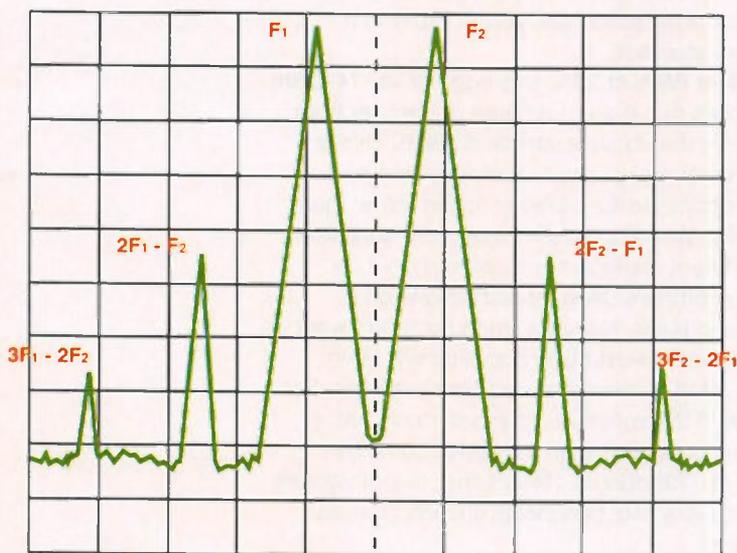


Figure 2: Two tone intermodulation analysis

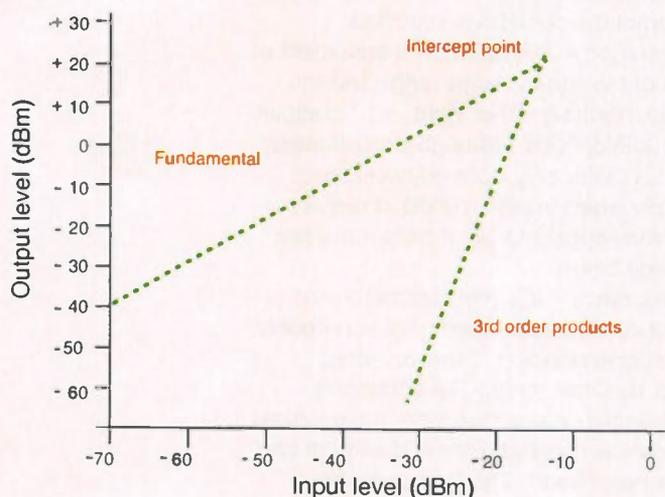


Figure 3: Intermodulation Intercept point

The problem is that this definition is often corrupted to make the analyser appear better than is actually the case. Both parts of the definition should apply at the same instant in time but often the large signal part of the definition is taken to be at some more favourable (higher) point so that the total range appears greater. Alternatively, with the input attenuator set for large signal handling, the noise floor definition is moved to that with no attenuator, again creating a larger ratio than is really possible.

### ➤ Resolution bandwidth (RBW)

Resolution bandwidth is the bandwidth of the IF filter, which determines the selectivity of a spectrum analyser. A wide resolution bandwidth is required for wide sweeps whilst a narrow filter is used for narrow sweeps. By using narrower resolution bandwidths the instrument can resolve the sidebands. The penalty for high resolution is a slower sweep speed. Wide filters are thus used when the display needs to be updated rapidly or when wide modulation bandwidths are to be displayed.

The minimum resolution bandwidth of a spectrum analyser is a key measure of ability to measure low level signals adjacent to high level signals and also to provide the lowest displayed noise floor.

### Frequency accuracy

There are three related frequency accuracy specifications within a spectrum analyser: reference frequency accuracy, centre frequency accuracy and span accuracy. The reference frequency accuracy is that of the internal standard frequency oscillator (or external standard, if selected). A spectrum analyser has a swept local oscillator and there are potentially three modes of operation and each has a different frequency accuracy specification:

➤ Free run mode is an analogue sweep used for wide spans with probably little better accuracy than  $\pm 5$  to 10% of total span.

➤ "Lock and roll" mode is the more commonly employed mode for wide spans in a modern spectrum analyser. As its name implies, the swept oscillator is locked to the reference at the start of the sweep to accurately set the start frequency, the oscillator is then swept in analogue mode to the stop frequency. An accuracy of  $\pm 3\%$  or better of span is typical in this mode.

➤ Lock or "Lock-Lock" or stepped sweep mode is the most accurate mode of operation where each frequency point in a stepped sweep is close to the "in-lock" condition. The mode is usually only employed for small spans of between a few MHz out to a few tens of MHz. In this mode the accuracy

cy is normally written as that of the frequency standard in proportion to the actual frequency or in ppm (parts per million) at the centre frequency.

## Level accuracy

Most modern spectrum analysers employ an internal calibration signal to correct for changes in the gain of the IF amplifiers with the objective of maintaining a constant level accuracy. During factory calibration of the spectrum analyser, the manufacturer will usually connect a signal source and power meter system to characterise the input level and frequency response characteristics, assuming that these do not change subsequently. Even with this type of system used over 50 or 60dB of input range, the input level accuracy of a spectrum analyser remains dominated by the input match. A typical input VSWR for a low frequency spectrum analyser at the highest frequency is around 1.5:1 and for a microwave spectrum analyser can be greater than 3:1.

## Distortion and spurious signals

### > Residual signals

A spectrum analyser can display a signal on the screen even though no signal is present at the input. Instrument designers endeavour to eliminate this undesirable phenomenon but these residual responses as they are known are present in all spectrum analysers to a greater or lesser extent. Residual responses occur because within a spectrum analyser there are a number of local oscillator frequencies whose frequencies and harmonics mix with each other to produce signals which can fall within the IF bandwidth. These then appear as apparently real signals on the display.

Residual responses can create significant measurement problems so it is important to purchase an instrument with a very good specification. Residual responses of a quality instrument are typically less than -110dBm. Some instruments can have inferior specifications or, in some cases, the residual responses are not even quoted at all.

### > Input related spurious signals

Active RF and microwave systems frequently generate non-harmonically related signals that need to be identified and measured. Tracking down and then reducing the level of unwanted spurious signals is a very common application of a spectrum analyser. Unwary spectrum analyser users can experience problems with such a measurement if they are unaware of the limitations of the instrument.

The problem of internally generated harmonically related distortion products has been described but the spectrum analyser itself can produce spurious responses. It is essential to ensure that

the instrument itself does not generate a signal seen on the screen. Instrument-generated spurious signals can either be residual responses that are an inherent limitation of the design or they can be caused inadvertently by the operator if the instrument is overloaded. Image responses and multiple responses are also encountered in microwave spectrum analysers if a preselector is not used. Modern spectrum analysers have a spurious response specification of typically -120dBm to -110dBm. To be absolutely certain that a signal is not internally generated, it may sometimes be necessary to replace the signal being analysed with a known pure signal and to study the difference.

### > Second harmonic distortion

A spectrum analyser can be used to measure the amplitudes of the fundamental and even very low-level harmonics. Sometimes, however, it is necessary not only to quote the level of the harmonic distortion products, but also to give the total harmonic distortion; this can be calculated from the following equation:

$$\text{THD (\%)} = 100 \times \sqrt{(A_2)^2 + (A_3)^2 + \dots + (A_n)^2} / A_1$$

Where:

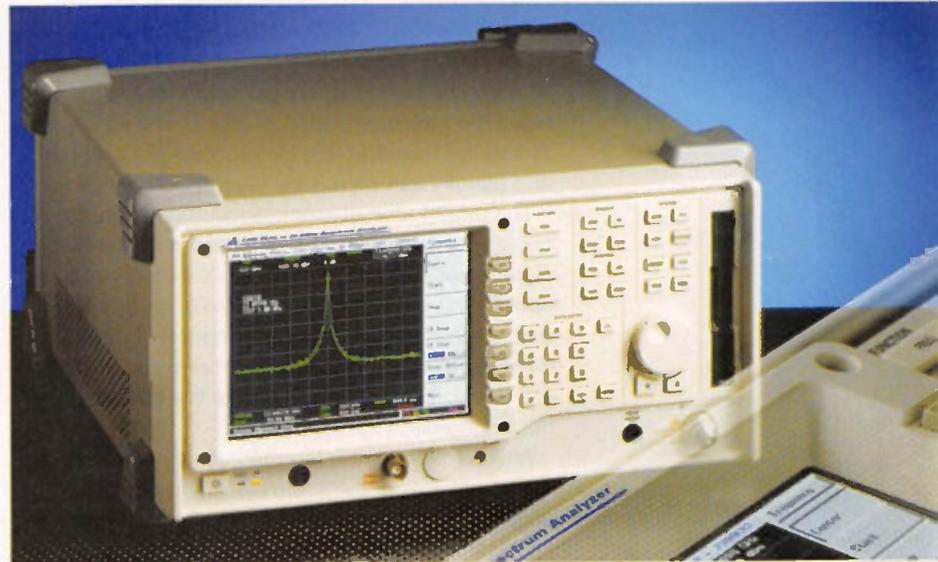
THD = Total Harmonic Distortion

A1, A2, A3 and An = Amplitudes of fundamental, 2nd, 3rd and nth harmonics.

### > Intermodulation distortion

Measuring the harmonic distortion caused by a device is not a very discriminating measurement. A more searching method is to use two or more test signals and to measure the intermodulation products that are generated at the output of the device under test. By using more than one test signal the device is receiving signals that are closer to the more complex signals that are generally encountered in practical systems. Two separate signal

Aeroflex 2395 spectrum analyser



generators are needed, the signals are combined together and fed through the device under test.

Great care must be taken when making measurements or they may be invalid. Both signal generators must have low harmonic content. If this is not possible then a low pass filter should be inserted at the output of the generator. The combiner should be a linear device with good matching.

Another problem is that any non-linearity in the output amplifiers of the signal generators can produce intermodulation. Further problems can arise if the ALC detector at the output of one signal generator also detects the signal from the other signal generator. For these two reasons, it is good practice to insert an attenuator between the signal generator output and the combiner. In some circumstances, this may not be practical because the signal level may then be too low. For higher frequency measurements an isolator is recommended to improve measurement integrity.

A typical spectrum analyser display of a two-tone intermodulation test is shown in **Figure 2**, annotation has been added to explain the origin of the intermodulation products. Signal generator 1 has a fundamental frequency of  $F_1$  and signal generator 2 has a fundamental frequency of  $F_2$ . Nonlinearity in the device under test will cause harmonic distortion products of frequency  $2F_1$ ,  $2F_2$ ,  $3F_1$ ,  $3F_2$  etc to be generated. The spectrum analyser will record these harmonic products but the significance of the intermodulation test is that the non-linearity causes the harmonic products to mix together to generate additional signals. Numerous intermodulation products can be generated but the most commonly encountered ones are known as the third order and fifth order products.

Third order products have frequencies of  $2F_1 - F_2$  and  $2F_2 - F_1$ . Fifth order products have frequencies of  $3F_1 - 2F_2$  and  $3F_2 - 2F_1$  etc. Even order products such as  $F_1 + F_2$  and  $F_2 - F_1$  are also encountered but are generally less significant since the intermodulation products are widely separated from the two frequencies ( $F_1$  and  $F_2$ ) and usually can be readily filtered out.

The amplitudes of intermodulation products change according to the amplitudes of the test signals applied and it is therefore necessary to specify the level of the test signals. It can be difficult to compare the performance of different devices however, if they were measured at different levels. The solution is to use the concept of an intermodulation intercept point.

An intercept point is the theoretical point at which the amplitudes of the intermodulation products equals the amplitudes of the test signals, **Figure 3** shows the concept. There are two lines on the

graph. The fundamental line shows a linear relationship between the input and output signals but the line has been extrapolated beyond the output level of +5dBm since at such levels the response becomes non-linear. Input and output signal levels have also been plotted for the 3rd order products and the line is extrapolated. The two lines meet at the intermodulation intercept point.

The slope of the intermodulation product line is equal to the order, that is the 2nd order lines have a slope of 2:1, the 3rd order lines have a slope of 3:1. Practically, this means that as the level of the test signal is reduced by 10dB then the 3rd order product will theoretically drop by 30dB, provided that the device is operating in a linear mode.

## Sweep speeds

A spectrum analyser must be swept sufficiently slowly to allow the signal level in the narrow resolution filters to settle. Two difference responses are shown, the errors produced when sweeping too fast are clearly illustrated.

Modern instruments incorporate microprocessor control to always give the correct speed. Under certain conditions, where high resolution is required, the sweep speed may need to be as slow as 100 seconds, digital storage is thus essential.

Manual sweep speed controls are provided on modern instruments to over-ride the automatic selection. Sweeping faster than the optimum can be useful to carry out a rapid uncalibrated search for spurious signals or to study the effects of rapidly changing transient signals. The operator must however be aware of the errors that can be generated.

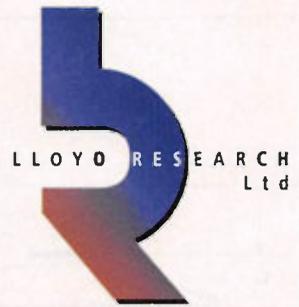
## Other features and facilities

Perhaps the most common optional feature offered with most spectrum analysers up to 3GHz or 4GHz is that of a tracking generator. This allows the spectrum analyser to be used as a selective scalar network analyser. Other possible uses include a fault location or TDR facility for cable testing in cell site maintenance applications. Note that microwave spectrum analysers generally either only offer a tracking generator over a limited lower frequency range or do not have the facility at all.

Adding an optional tracking generator to a spectrum analyser usually increases the price by 25% so careful consideration to the likely application should be given before purchase.

Other optional features include EMC pre-compliance testing by adding quasi-peak detection and filters.

Many software features are to be found either as standard or as options and these include channel power, adjacent channel power ratio, occupied bandwidth, harmonic distortion, limit masks and zero span time domains.



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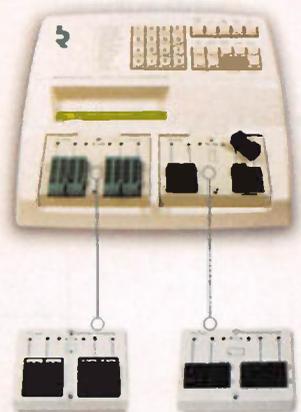
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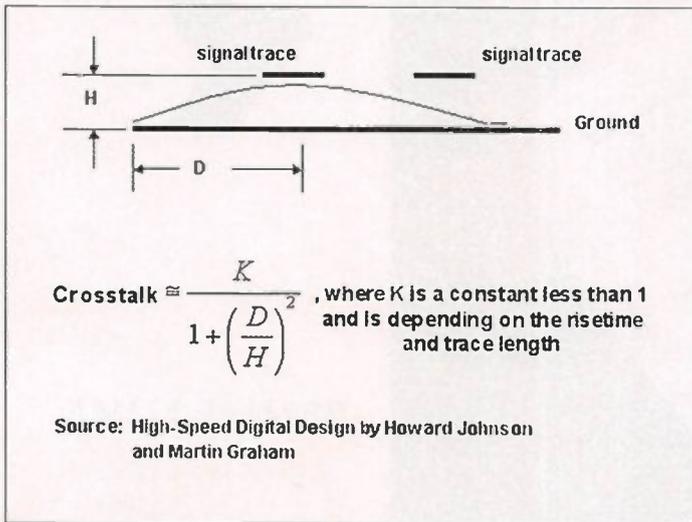


Figure 1: Doubling traces minimises crosstalk

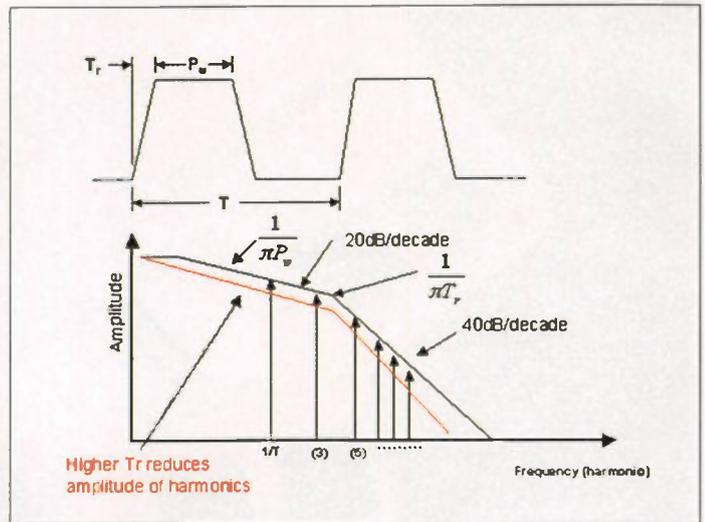


Figure 2: Slowing the rise-time reduces harmonic content

High-speed DSP system design is becoming increasingly sophisticated with higher clock rates and signalling speeds. As a consequence, there are an increasing number of noise sources. The clock rates (1GHz) and signalling speeds (500MHz) of current high-end DSPs lead to considerable harmonics with PCB traces acting as antennae. The resulting noise degrades audio, video, graphics and communications performance, as well as posing problems in achieving FCC/CE mark certification. It is critical for high-speed DSP designers to recognise and address possible causes and apply good high-speed design practices in order to combat power noise. This article outlines the importance of crosstalk, phase lock loops (PLLs) and decoupling/bulk capacitors in noise reduction.

**Combating crosstalk**

Crosstalk is an important, often overlooked, source of noise. In high-speed systems, signal ground paths vary depending on the frequency of an operation. For low-speed signals (<10MHz) the current returns to the source via the ground path of least resistance (i.e. shortest path).

Above 10MHz, the situation is different. Current returns on a ground path of least inductance, which is generally not the most direct path. Significantly, the return signal spreads out with a current distribution (Figure 1) that means, return paths of adjacent signals can easily overlap, leading to crosstalk.

There are several techniques to reduce crosstalk: trace spacing, adding a ground wire, reducing harmonic content and trace-termination techniques.

On high-speed DSP systems, doubling the trace spacing between signals, from one to two trace-

# Reducing power noise in high-speed design

Dr Thanh Tran, senior member of IEEE, analyses the best way to tackle noise in high-speed design

widths, reduces loop overlap and produces a four-fold reduction in crosstalk. For differential signals (e.g. Ethernet or USB), the recommended spacing that produces the signal pair with the required matched impedance should be adopted. In addition, critical signals (i.e. clocks) should be shielded by either routing the signal on an inner layer between the power and ground planes or using an image plane (ground plane) on the layer immediately below critical signals.

A ground wire should be included in parallel when adding a signal wire to a reworked board. This supplies a high-speed current return path and produces the smallest area in the current loop. This extra path ensures that, the return current does not create large loops and pick up noise.

When combating crosstalk, it is important to appre-

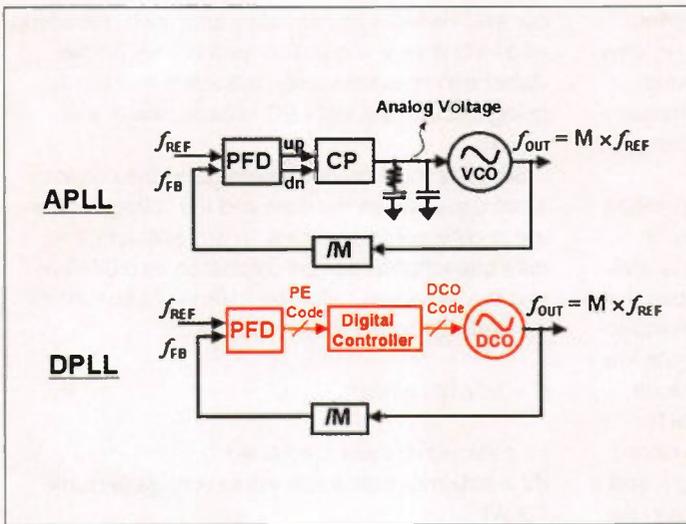


Figure 3: Analogue and digital PLLs

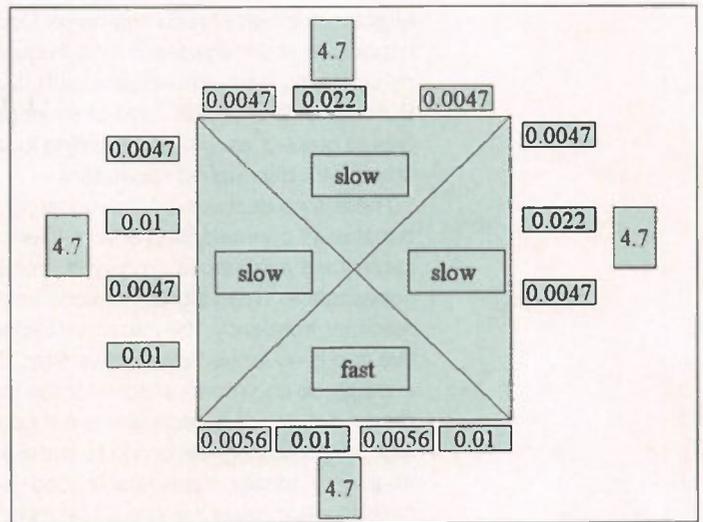


Figure 4: OMAP5910 DSP capacitor values

# Power noise in DSP system

Technical staff at Texas Instruments  
DSP designs

...ciate that fast edges create more harmonic energy and, therefore, interference. Slowing the rise time ( $T_r$ ) by adding series-termination resistors on traces, for example, is an effective way to reduce this harmonic content. Moving the noise amplitude curve towards lower frequencies better attenuates harmonic components (Figure 2).

A trace can act as a transmission line (i.e. when rise time ( $T_r$ ) < 2 x propagation delay ( $T_p$ )). It is, therefore, a good idea to keep traces as short as possible. If it is essential to have a trace line long enough to act as a transmission line, it is important to terminate the line, using series (a resistor in line with the output driver) or parallel termination (a resistor to ground at the load). If a resistor matching the trace's PCB impedance is used, transmission-line reflections and ringing can be reduced.

## Phase-locked loops

Phase-locked loops (PLLs) are another important source of noise. Both analogue and digital versions are increasingly being used in some DSPs (Figure 3). A pi filter is effective at removing high-frequency noise when isolating a power supply feeding a PLL. Removal of low-frequency noise (<1MHz) is less effective and requires the inclusion of a multistage filter network. In fast switching circuits, however, a low-dropout (LDO) regulator is more appropriate because these devices are designed to have a high power supply rejection ratio (PSRR) at low frequencies. If the design runs in a noisy environment (e.g. automotive, electrical/mechanical devices) with considerable low frequency transients, a high-PSRR regulator should be selected.

Analogue and digital grounds tend to be kept separate to isolate digital noise from analogue sections. This is fine for low-speed circuits. For high-speed circuits (e.g. video sections), however, separate grounds should be avoided. Fast switching currents take the smallest current loop and an isolated ground prevents the current from finding this path. As a result, an alternative path to the source will be found, which ultimately leads to a potential difference, current flow and radiation. Shorting the analogue and digital grounds together at the digital data entry point will provide a direct path without affecting the low-frequency signals. The signals seek the physically shortest return route to the source rather than the shorted path.

## Capacitor applications

The appropriate application of capacitors is an

effective method of reducing noise. Decoupling capacitors shunt unwanted high-frequency energy by supplying a low-impedance path to ground. Bulk capacitors can be used to shunt low frequencies to ground, as well as providing local charge storage for decoupling capacitors.

There is no best value for decoupling capacitors because of counteracting effects. Generally, a capacitor's impedance drops with frequency and capacitance. When signal frequencies exceed the resonant frequency, the capacitor becomes inductive and is no longer an effective filter. Despite low impedance and more charge storage to reduce droop, a high-value capacitor is not optimal for high frequency signals owing to a lower resonant frequency. Ideally, if practicable, both a high- and a smaller-value capacitor should be included on the power supply ground. If not, a 0.01 $\mu$ F capacitor is an acceptable compromise. Relatively large bulk capacitors should be used that combine to at least 10 times the total decoupling capacitance in a given region.

At 100kHz, for example, a 100 $\mu$ F electrolytic has an equivalent series resistance (ESR) of around 0.6 $\Omega$ , compared to around 0.12 $\Omega$  for the same value tantalum, making the latter preferable for bulk capacitors. Ceramic rather than polyester capacitors are better for decoupling. At 1MHz, for example a 0.1 $\mu$ F ceramic has an ESR of around 0.12 $\Omega$ , compared to 0.11 $\Omega$  for a 1.0 $\mu$ F polyester capacitor.

Decoupling capacitors should be placed on the bottom of the PCB next to the device pins. Alternating between the core and the I/O values will minimise the distance from any lead to its capacitor. For a high-speed DSP, a decoupling capacitor should ideally be placed on every power pin. If space does not allow this, as many as possible should be placed around the device. An effective method of decoupling a complex DSP is to draw two imaginary lines from opposite corners to create an X (Figure 4). Then analyse each of the four regions separately. To get the bulk capacitors close to the decoupling capacitors, place them on the top of the board. This positioning minimises traces (and thus current loops), while reducing radiation and parasitic inductance.

Let us take the OMAP5910 DSP from Texas Instruments as an example, particularly the region containing a digital PLL and an external memory interface (Figure 4, left region). The device has 13 core-voltage pins and a peak core-current consumption of 170mA (average 13mA/pin). The three core-voltage pins in the region containing the digital PLL and external memory interface draw 39mA. To be sure accuracy, when determining capacitor size, it is advisable to add a 100% margin, i.e. 78mA. It is also necessary to estimate the peak I/O

current. Taking a conservative approach, assuming all 54 I/O lines in the region switch 4mA (as per datasheet) simultaneously, this leads to 216mA going through the eight I/O voltage pins in this region.

Supplies must be decoupled using the correctly sized capacitor as the core and I/O voltages operate at different frequencies. In this example, the core capacitance can be calculated as 0.0078 $\mu$ F and the capacitance for the 216mA I/O current as 0.022 $\mu$ F, using the following formula:

$C = I(dV/dt)$ , where

$I$  = peak current just calculated

$dV$  = maximum allowable ripple voltage (assume 10mV)

$dt$  = the risetime (assume 1ns, typical of the OMAP5910)

i.e. the core capacitance,  $C = 78mA \times (1ns/10mV) = 0.0078\mu F$

In the OMAP5910 BGA package, there is enough space for four capacitors per region, not one for each core power pin. To decouple the core voltage pins, therefore, it is best to select two capacitors with a total value of 0.0078 $\mu$ F (arrange two 0.0047 $\mu$ F ceramics for the shortest distance from the pins to ground).

Switching frequencies must also be taken into account. This section of the core switches at 150MHz, while its eight I/O pins switch at 75MHz. The other two capacitor-positions can be used to decouple the I/O-voltage pins (i.e. two 0.01 $\mu$ F ceramics with a self-resonant frequency above 75MHz, providing 0.022 $\mu$ F).

### The value of bulk capacitors

In this example, the DSP's total core-voltage current is 338mA. Using the previous formula, capacitance is calculated as 0.0338 $\mu$ F. As bulk capacitance should ideally be 10 times the decoupling capacitance this gives approximately 0.39 $\mu$ F. Apply the same procedure for the I/O voltage, and you get a capacitance of 0.84 $\mu$ F, giving a total of 1.23 $\mu$ F. One bulk capacitor, each providing 3.075 $\mu$ F (1.23 $\mu$ F divided by four then multiplied by 10), should be added to each region. The smallest bulk-capacitance value currently available as a surface-mount device is 4.7 $\mu$ F, which works well in this example. Tantalum bulk capacitors should be selected, if possible, failing that a surface-mount electrolytic.

The decoupling and bulk capacitor values for each of the four regions can be calculated in this way and are shown in Figure 4.



# Hardwired and going strong

Hardwired MPEG4 part 10 decoders steel the thunder from programmable engines in the new generation of TV and DVD-type systems

By Nick Flaherty

**B**roadcom and Conexant, US chip makers are battling to be the first to develop and ship hardware decoders for the new MPEG4 part 10 coding technology, also known as AVC (Advanced Video Coding) and H.264.

The technology is being used by broadcasters to squeeze more TV channels into existing spectrum and to provide high definition (HD) TV more cost effectively than previously. It will also be used for high definition DVD systems that use the Blu Ray and HD-DVD standards for high capacity disks, HD personal video recorders (PVR) and TV systems that use IP protocols to send standard definition (SD) TV over broadband networks.

All of these require a decoder, which so far has been provided by programmable engines such as the DM64 digital signal processor (DSP) from Texas Instruments (TI) and the BSP16 VLIW engine from Equator Technologies. Both of these will support set-top boxes (STBs) with end costs of under \$100 and provide flexibility for new and changing decoder technologies.

However, the Broadcom part aims to bring the system costs down below those currently possible with the programmable versions, and the chip is being used in reference designs for an HD DVD, HD PVR and HD STBs. The decoder is based on technology acquired from Sand Video, a Boston-based start-up that Broadcom bought early last year. Broadcom has taken some of that technology, moved it into hardware and added other system

blocks, such as an audio decoder and interfaces around the central decoder. The chip can now handle two channels of SD video using the MPEG2 technology or one channel of HD video. This means boxes can be used for existing MPEG2 services as well as HD services. "The idea is a cost-effective solution," said Brian Sprague, marketing director at Broadcom. "We don't see any reason why this will cost any more than your basic free-to-air or satellite set-top box [\$50] and potentially less," said Sprague.

The key has been to put as much as possible in hardware. This is potentially more difficult than it might seem, as there are different variants of the standard and there is a different standard from Microsoft that has become popular with some operators, particularly in IPTV, that also needs to be supported. That is one reason why the programmable decoders have been used so far. Another reason is that current HD systems in the US, from satellite operators such as Voom, DirecTV and EchoStar, use the current MPEG2 HD standard (main level at high profile or ML@HP) and 1080i

displays, which means they need to be supported too.

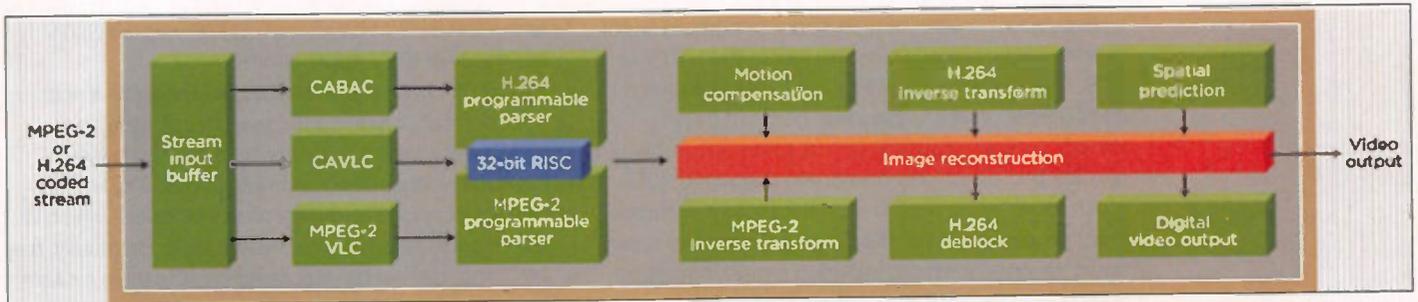
At the same time the European

.....  
“ This is a new ball game because these systems don't exist yet  
– you have a whole new concept of user interface. ”  
.....

Brian Sprague, marketing director, Broadcom

Broadcast Union (EBU) has specified that HD broadcasts should use MPEG4 part 10 with 720p progressive screen technology as the baseline for HD broadcasts in Europe. This contrasts with the only HD broadcaster in Europe, Euro1080, which is using MPEG2 ML@HP and 1080i, with decoder boxes from French consumer electronics company Thomson, using the previous generation MPEG2 HD decoder chips from Broadcom.

But other broadcasters are also looking at the MPEG4 technology to squeeze more out of today's standard definition video. Using AVC on existing 525-line SD resolution video can reduce the bandwidth requirement from the 2.5-6Mbit/s of MPEG2 down to 1Mbit/s. This makes it viable for transmission over IP networks that are using DSL technologies to send data over twisted pair telephone cabling.



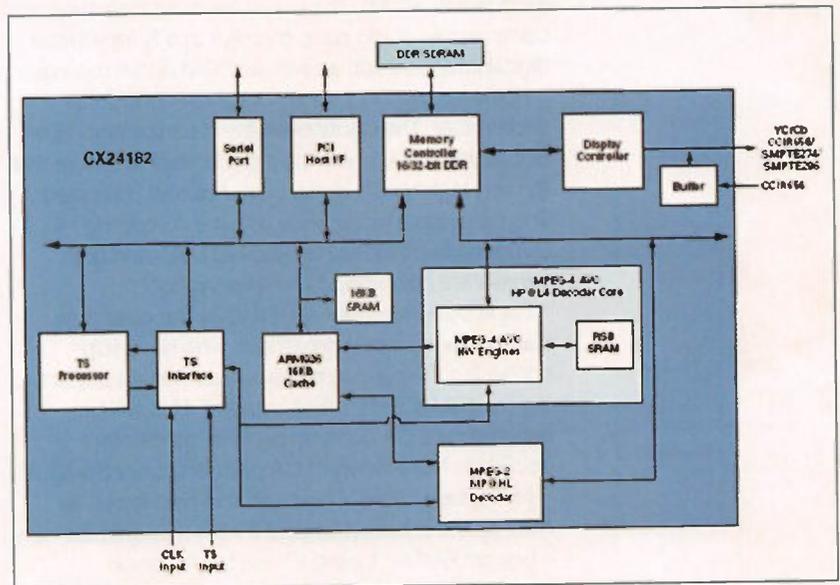
Above: Block diagram of Broadcom's AVC core

While these DSL networks can handle up to 8Mbit/s, reducing the bandwidth extends the reach of the service and allows the operator to reach more customers and hence bring in more subscribers. Operators such as Video Networks in London and FastWeb in Italy are currently running commercial IP over DSL services with MPEG2 and looking seriously at moving to AVC. So a decoder has to be able to handle a range of compression technologies, both in SD and HD systems.

The AVC approach (see 'MPEG4 part 10 coding') is also used in Microsoft's coding technology. Originally called Windows Media9 (WM9), and optimised for progressive screens such as PC monitors, this has evolved to a specification presented to the US Society of Motion Pictures and Television Engineers (SMPTE) to be a more open protocol and called VC9 to distance it from the Windows technology. The latest version has now been optimised for interlaced TV screens and is converging with the technology in AVC, with the new name of VC1. "We do see VC1 as important and we have to support it," said Sprague. "We have been tracking it and we have to have a software selectable approach. Some of the hardware has to change and we need a new firmware driver."

To handle both standards and all the different profiles within them, the Broadcom 7411 chip has a mix of hardwired and software functions. The basic functions involved in decoding such as the inverse Discrete Cosine Transforms (iDCT) are all implemented in hardware, along with the variable length coding, Context-based Adaptive Binary Arithmetic Coding (CABAC) and deblocking filter. The CABAC block handles the decoding of the entropy data in the AVC stream. This is done differently in VC1, which uses Context-based Adaptive Variable Length Coding (CAVLC), and there are two separate decoders in the chip to handle them. The deblocking filter is also in hardware, but with programmable parameters to allow different deblocking algorithms to be supported. Meanwhile, the software functions are implemented in a RISC engine. This is commercial core from ARC International – the A600 configurable core. The device handles the syntax of the MPEG stream to determine which hardware decode

Below: Block diagram of the Conexant AVC decoder



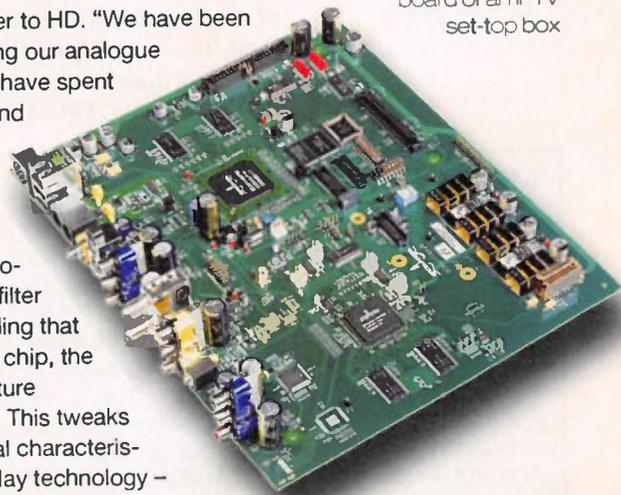
blocks need to be used and in what order. This gives the flexibility to handle different profiles and different versions, at a smaller estate and lower cost.

This is especially important in HD DVDs, says Sprague. "This is a new ball game because these systems don't exist yet – you have a whole new concept of user interface."

Broadcom is no stranger to HD. "We have been pioneering in HD, sampling our analogue HD decoder in 1999. We have spent years making analogue and SD digital video look good on analogue HD TV sets," said Sprague.

Broadcom has developed key display technologies such as a 3D comb filter and motion adaptive scaling that are used in a companion chip, the 7038, that includes a picture enhancement processor. This tweaks the picture to the physical characteristics of the particular display technology – LCD, plasma, DLP or rear projection.

The BCM9731 reference design board of an IPTV set-top box



However, this level of picture enhancement is not needed in the decoder, as this sits in the HDTV or STB. There is a scaler in the 7411 that includes a deinterlacer on both channels, horizontal and vertical scaling, cropping and chroma unsampling, and 3:2 pull-down and on-screen display, but it is much more basic design than the picture enhancement processor. What is fully programmable is the audio processor, which includes a multi-standard audio decoder core, supporting MPEG-4 high-efficiency AAC (AAC+), MPEG-4 AAC (ACC-LC), Dolby Digital Plus (Enhanced AC3), Dolby Digital (AC3), MPEG-1 Layer I, II, III (MP3) and pulse code modulation (PCM). The audio decoder also supports compressed audio pass-through to a Sony/Philips digital interface out, as well as PCM audio mixing.

However, the 7411 does not handle conditional access (CA). The CA functionality is particularly important for HD DVD, where the studios want to ensure that the very high quality digital output cannot be copied. This has been a major issue with the competing HD DVD standards of Blu Ray and HD DVD, and both formats are now using 128-bit encryption.

CA is also important for IPTV, as the operators want to be sure that only those who have subscribed to the service receive it, as well as protecting the content from illicit copying. This will be handled by a CA companion chip, as different operators have different CA partners, says Sprague.

At the same time, Conexant has developed an AVC decoder based around a core it acquired when it bought Belfast-based IP vendor Amphion Semiconductor in June last year. Conexant's \$20 CX2418X uses the ARM 926EJ-S synthesisable core with a Jazelle co-processor for handling Java applets. This is running alongside the Amphion CS7050 decoder core. It uses variable block size motion estimation to improve the coding efficiency and the quality of the video output. The implementation requires less than 300k gates and 24Mbytes of external system memory, which allows the 2418x family to use 32Mbytes of system memory. There is a range of devices in the family, from the CX24182 that handles AVC HP with an HDTV interface, down

to the 24181 that handles AVC MP with an SDTV interface for IPTV applications.

In HDTV, both these devices sit alongside a host decoder that is running the system software and middleware, which adds costs to the end solution. However, it does allow a simple upgrade to HDTV without having to re-qualify all the software, which is a time consuming and expensive task. Eventually, the AVC decoder will be integrated into the main system chip alongside a MIPS or ARM host processor.

Other manufacturers are also looking at hardwired decoders. Korean firm LG Electronics is planning to use the Optimode digital signal processing extensions to the ARM family of processors for an AVC decoder for HDTV that will retain reprogrammability to accommodate multiple video decoding standards.

Optimode adds a configurable data path to the ARM core, along with additional DSP instructions, so that engines can be tuned to the specific requirements of different algorithms such as VC1 and AVC. This means that control and DSP code is written in the same environment and debugged and tested on the single core.

"Conventional signal processing approaches no longer serve our customers' rapidly changing technology demands, as they do not address the performance and reprogrammability needs of our video encoding and decoding product lines," said Dr. Seung-Jong Choi, vice president of the Digital TV Labs at LG Electronics.

The next step in digital TV is coming from AVC. Equipment makers are already looking for cost-effective decoders. Until recently, the programmable DSPs have been the only way to provide the decoding capability. But now that standards and profiles are more settled, the availability of the Broadcom BCM7411 and the Conexant CX2418x family in the second quarter of this year will bring the cost of AVC IPTV standard definition decoders down to the same levels as today's STBs, and HD decoder boxes down in cost, making them more appealing to a larger market. It will also open up the new area of high definition DVD players.

## MPEG4 part 10 coding

MPEG4 part 10 coding or Advanced Video Coding (AVC) has been developed by the international standard bodies such as MPEG and the ITU (which calls it H.264), and, like MPEG, includes different profiles: the Main Profile (MP) and the High Profile (HP). Because it is MPEG-based, it can be used within existing MPEG2 transport streams, so the transport layer of the AVC decoders needs to be able to handle MPEG2. This is not a problem, as the processing power for AVC is more than enough to handle MPEG2 decode as well.

The High Profile reduces the bit rate by a further 10% over the

other profiles by changing the macro blocks that are used for coding the image from a block of 4x4 pixels to a block of 8x8 depending on the complexity of the scene. With scenes that are not overly complex, the 8x8 blocks provide more efficient coding, reducing the bit rate. But the decoder has to recognise the profile and be able to decode 8x8 blocks. This is handled in the syntax processing engine in the chip. Programmability is via firmware updates so that the box will be able to handle future variants while still using the same underlying processing elements implemented in hardware, on the chip.



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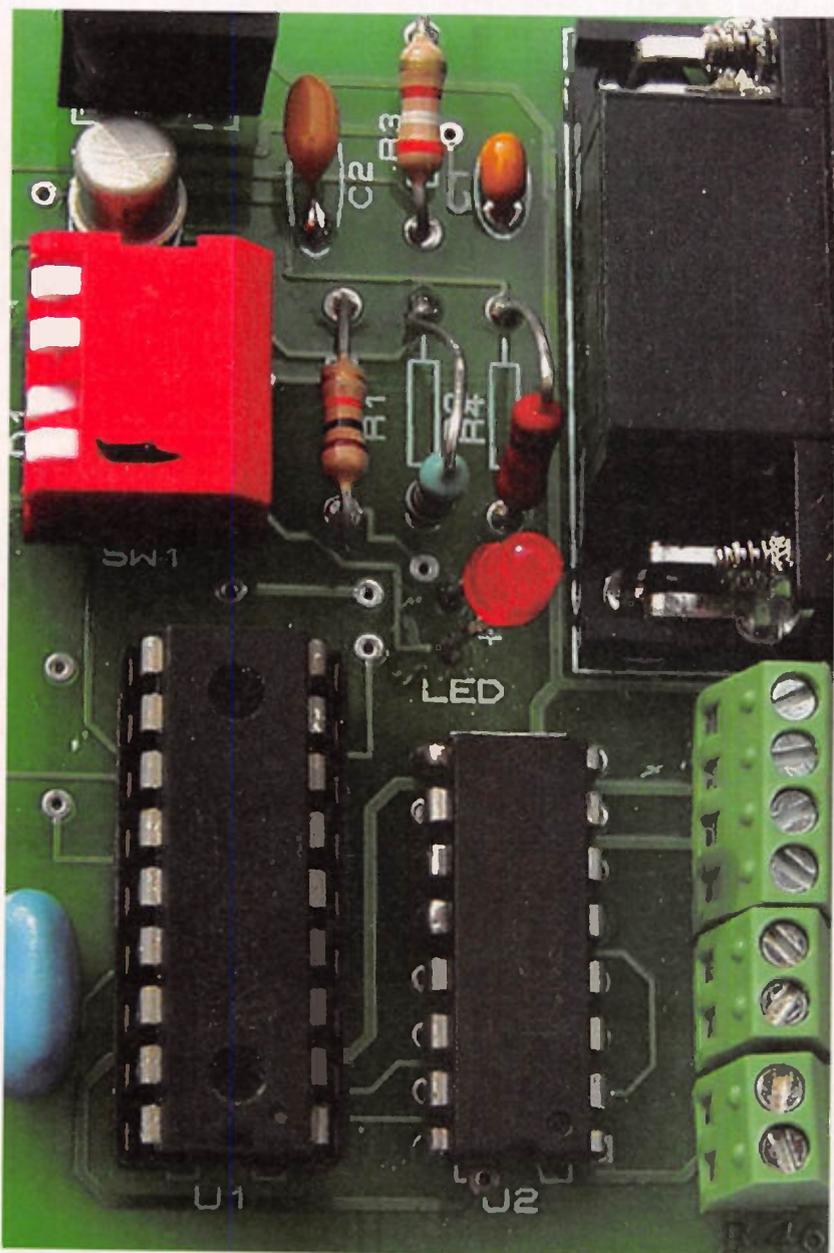
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# PIC-based autonomous stepping motor controller



Dogan Ibrahim designs a PIC-based autonomous stepping motor controller with commands that can easily be received over a serial line and stored in the MCU's EEPROM memory

Stepping motors are electro-mechanical devices that convert electrical pulses into discrete mechanical movements. A conventional motor has a free running shaft and rotates continuously as long as power is applied to the motor. The shaft of a stepping motor rotates in discrete steps when electrical pulses are applied to it in the correct sequence. The direction of the motor shaft rotation is related to the sequence of the pulses. The speed of the rotation is related to the time between the input pulses and the length of rotation is directly related to the number of pulses applied.

The stepping motor, therefore, allows simple open-loop control of the distance, direction and velocity of a motor shaft. If desired, a closed-loop feedback may be applied around a stepping motor with an encoder, but stepping motors are usually used without any feedback loops.

## Pros and cons of stepping motors

Stepping motors have the following advantages over the conventional motors:

- Motor shaft position can be controlled very accurately using digital input pulses and in open-loop mode. This type of control eliminates the need for expensive sensors and control circuitry. The position is known by keeping track of the number of applied input pulses.
- It is possible to operate the stepping motors at very low speeds.
- They are very reliable since there are no brushes and, as a result, these motors have very long operational lives.
- Their speed can be easily controlled by varying the frequency of the applied pulses.
- The motor has full torque at standstill, as long as the windings are energised.
- Excellent starting and stopping responses.

However, stepping motors also have disadvantages:

- Their cost is usually higher than the cost of conventional motors.
- They are not easy to operate at very high speeds.
- They are usually available for low torque applications.

### Controlling a unipolar stepping motor

There are basically three types of stepping motors: variable-reluctance, permanent magnet and hybrid motors. This project is not about the stepping motor technology, but about controlling the speed, direction and the step size of a unipolar stepping motor using a PIC microcontroller. A unique feature of this project is that the circuit can operate in either remote mode, programming mode or stand-alone mode. In remote mode, external input pulses control the motor. In programming mode, rotation commands are received from the RS232 serial port and these commands are stored in the non-volatile EEPROM memory of the microcontroller. In the stand-alone mode, the motor rotates under the control of a PIC microcontroller by following the commands in its EEPROM memory and without using any external pulses.

Unipolar motors are easy to control and a simple 1-of-n counter circuit can be used to generate the required stepping sequence. A driver transistor can be used for each winding. One of the most commonly used drive methods is 1 phase full step, also known as the "wave drive", where the motor windings are energised one at a time as shown in Table 1. The motor can be driven by using a MOSFET power transistor for each coil winding, as shown in Figure 1.

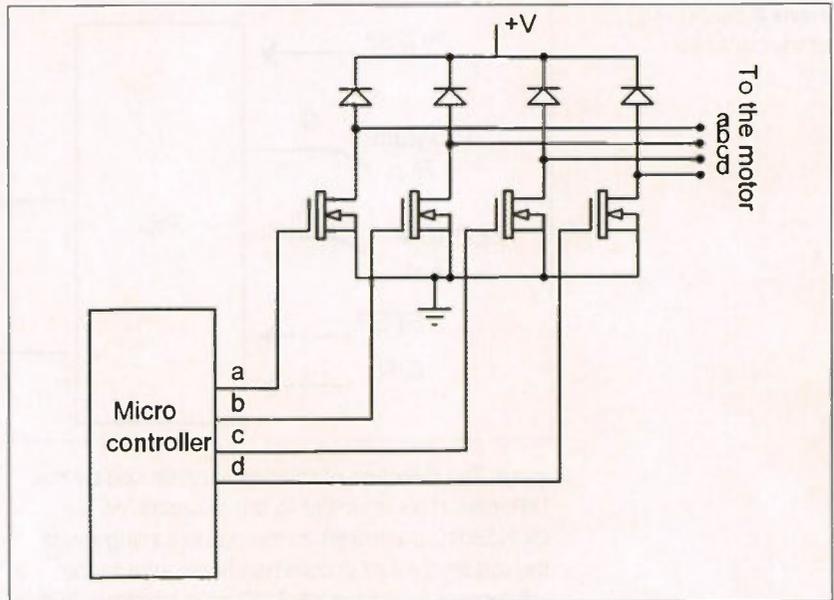
Unipolar motors can also be driven by using integrated circuits, such as the UCN5804B. This chip operates with voltages of between 6V and 30V. It contains a CMOS logic section for the sequencing logic and a high-voltage output section to directly drive a unipolar stepping motor. As shown in Figure 2, the motor is connected directly to the chip. Pulses are applied to the STEP input of this chip and the chip generates the correct sequence of signals to drive the motor. The DIR logic input of the chip controls the motor direction.

### The method applied

Although the integrated circuits such as the UCN5804 simplify the stepping motor control process, there are applications where we may want to generate pulses to control the rotation of a stepping motor on a stand-alone basis. For

**Table 1: One phase full-step drive**

Step	A	C	b	d
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1



**Figure 1:** Driving a unipolar stepping motor

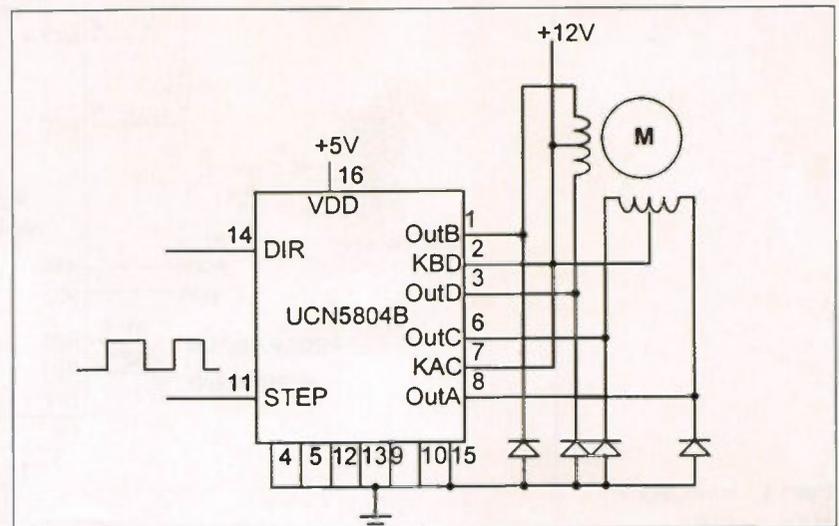
example, we may want to rotate the motor 500 steps clockwise, then after a delay of three seconds, rotate 2000 steps anticlockwise, then after a delay of two seconds rotate the motor another 50 steps clockwise and then stop. One way of achieving such an operation may be by using a microcontroller and a UCN5804 type chip, where the microcontroller can be programmed to generate the required pulses for the UCN5804.

The method used in this project is based on using a low-cost PIC16F84 type microcontroller and a ULN2003A type driver to control the rotation of a unipolar stepping motor. Figure 3 shows the block diagram of the controller.

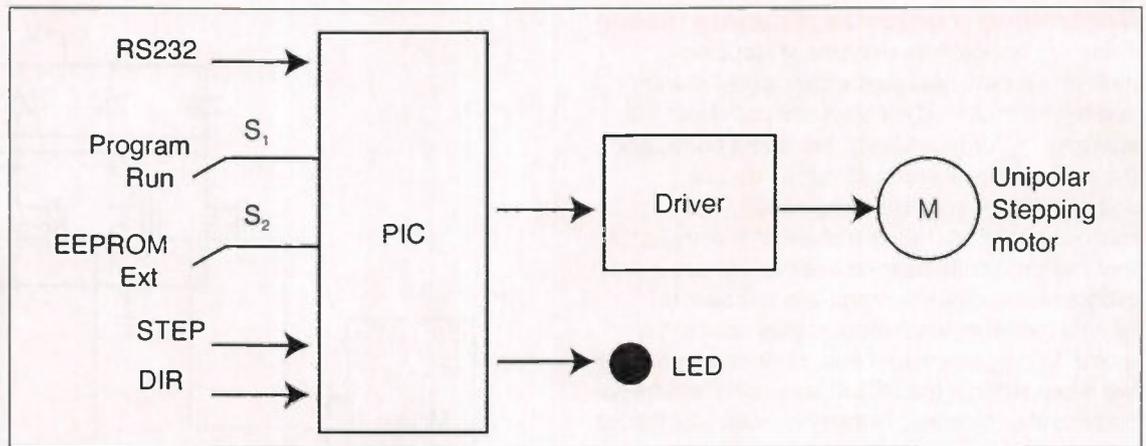
The controller is operated in three modes: remote-run mode, programming mode and stand-alone run mode.

In the remote-run mode the motor rotates one step on each application of a pulse to the STEP

**Figure 2:** Controlling a unipolar motor using a UCN5804 IC



**Figure 3:** Block diagram of the controller



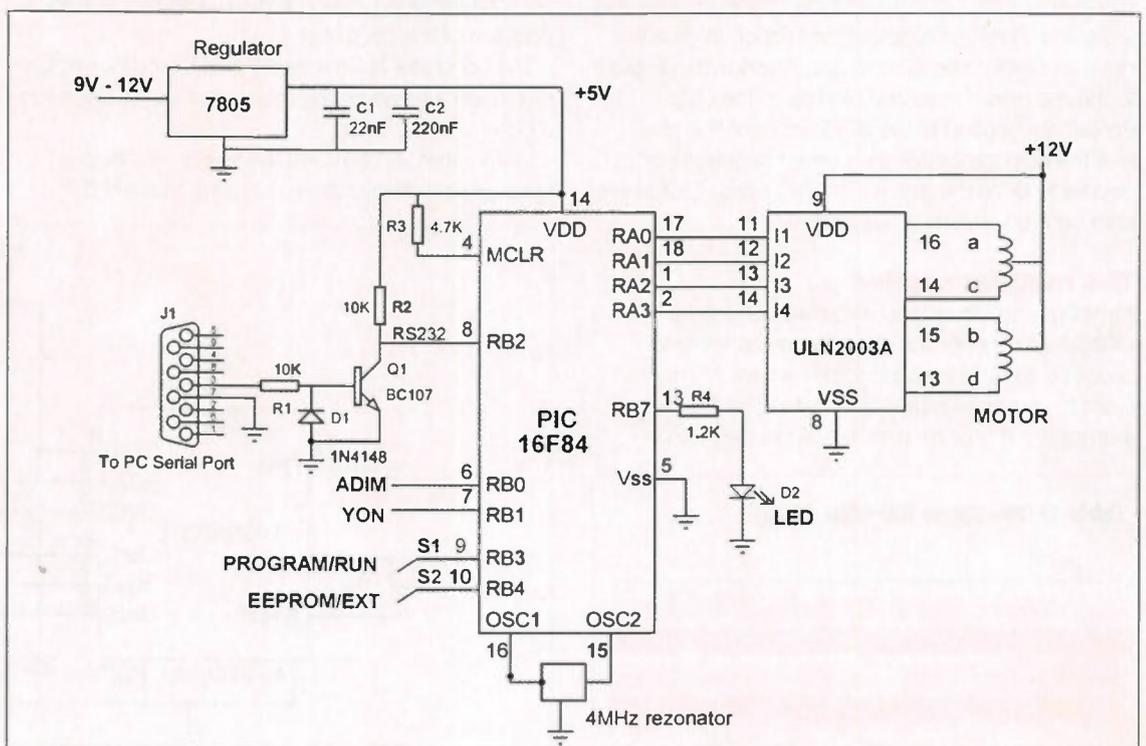
input. The direction of rotation is controlled by the DIR input (This is similar to the operation of UCN5804B controller). In the programming mode, the required rotation commands are sent to the microcontroller using a RS232 type interface. In this project, a PC is used to send the required rotation commands to the microcontroller. The received commands are stored in the non-volatile EEPROM memory of the microcontroller. When the microcontroller is in the stand-alone-run mode, the motor is controlled from the command steps stored in the EEPROM memory of the microcontroller.

The circuit diagram of the controller is shown in **Figure 4**. A PIC16F84 microcontroller, operated with a 4MHz resonator, is used at the heart of the controller. Ports RA0-RA3 are configured as outputs and they drive the inputs of the ULN2003A. The

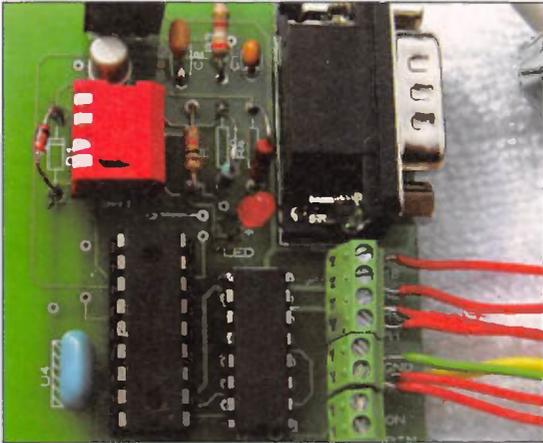
output of the ULN2003A drives the stepping motor directly. RB2 input of the microcontroller is configured as a serial RS232 input and a transistor-diode circuit is used to convert the RS232 signal levels to +5V. A pushdown two-way DIL switch is connected to RB3 and RB4 inputs. The mode of operation is selected by these switches as shown in **Table 2**. S<sub>1</sub> selects the programming or the running mode. When in running mode, S<sub>2</sub> selects operation from

**Table 2: Selecting the mode**

S <sub>1</sub>	S <sub>2</sub>	Mode
0	X	Program the EEPROM with motor commands
1	0	Work from commands in EEPROM
1	1	Work from external pulses



**Figure 4:** Circuit diagram of the controller



the internal EEPROM or from external pulses. RB0 and RB1 are the STEP and the DIRECTION inputs. The motor turns by one step each time a pulse is applied to the STEP input when the controller is in the remote-run mode.

The circuit of the controller is built on a small 6.5cm x 5.5cm double-sided PCB, as shown in Figure 5. A small LED is connected to bit 7 of PORT B. This LED flashes for a second when the controller is in the programming mode and when a valid command set is received from the serial port. The circuit is designed to operate stepping motors with a current of up to 500mA, at +12V.

### Software

The software is in two parts: the microcontroller software, which runs on the PIC microcontroller, and the PC software that is used to download commands to the microcontroller via the PC serial port.

The microcontroller software was developed using the Hi-Tech PICC Lite C compiler. This compiler is distributed free by Hi-Tech Inc and it can be used to program PIC16F84 and PIC16F877 chips. Using a high-level language for the development of a microcontroller system has the advantages of being easier to develop and test the code, as well as easier to maintain the code. See Box 1.

The commands start with character 'S'. Then the stepping angle and the delay between steps is sent. Next, blocks of five bytes are sent to specify the required rotation. The first two bytes are the number of revolutions. The direction of rotation is then specified, followed by the required delay between the commands. A '#' character is sent to indicate the end of data. The LED is flashed for a second to indicate that data has been received with no errors.

The PC software was developed using Visual Basic. The program uses the Microsoft MSComm ActiveX component to send out serial data. The program consists of a single form as shown in Figure 7 which is used to enter the required motor commands. On this form, the user enters the

stepping angle of the motor, the delay required between each step and the serial port number used. Required motor control steps are then entered as the number of revolutions, the direction (0 or 1) and the delay after the command (in ms).

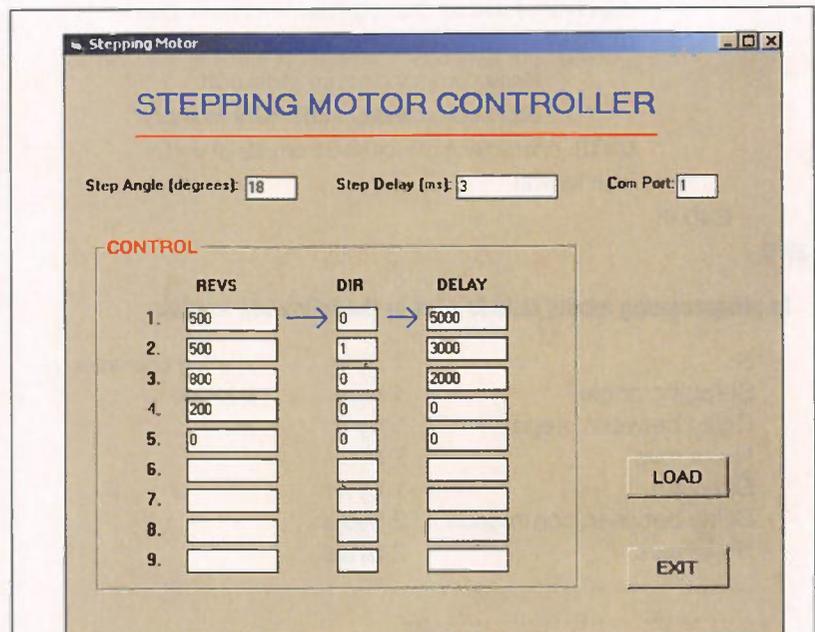
Nine steps are reserved for the user to enter the motor control commands but this number can be increased by modifying the program, if desired. In the example given in Figure 7.

### Conclusion

The design of a PIC microcontroller based autonomous stepping motor controller has been described. The controller has the advantage that the control commands can easily be received over a serial line and stored in the EEPROM memory of the microcontroller. With a PIC16F84 microcontroller, up to 12 control commands can be stored in the EEPROM memory. A larger PIC chip, such as the PIC16F877 will allow up to 50 control commands to be stored in its EEPROM.

Figure 5 (Left): The stepping motor controller

Figure 7: A typical run



The following control commands are given:

Motor stepping angle: 18  
 Delay between steps: 3 ms  
 One serial port used for programming  
 Turn 500 revolutions clockwise  
 Wait for 5 seconds  
 Turn 500 revolutions anti-clockwise  
 Wait for 3 seconds  
 Turn 800 revolutions clockwise  
 Wait for 2 seconds  
 Turn 200 revolutions clockwise  
 Stop

**Box 1: The operation of the microcontroller code is described as:**

**BEGIN**

Configure I/O ports

**IF** RUN mode = 1

**IF** EEPROM mode = 1

**DO FOREVER**

Wait for an external pulse on STEP input

Rotate the motor by one step

Wait required amount between steps

**ENDDO**

**ELSE**

**REPEAT**

Read commands from the EEPROM

Rotate motor according to the command

**UNTIL** there are no commands in EEPROM

Wait forever

**END IF**

**ELSE**

Wait until character S is received from serial port

**REPEAT**

Read commands from serial port

Store commands in EEPROM memory

**UNTIL** character # is received from serial port

Wait forever

**END IF**

**END**

**In programming mode, data is sent in the following format:**

S	1 byte	starting character
Stepping angle	1 byte	degrees
Delay between steps	1 byte	ms
No of revs	2 bytes	
Direction	1 byte	
Delay between commands	2 bytes	
No of revs	2 bytes	

.....  
 .....  
 #

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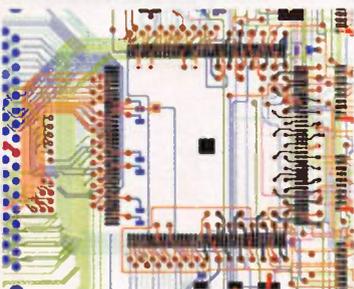
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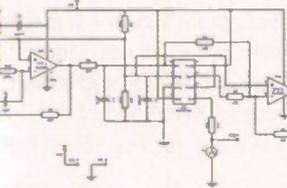


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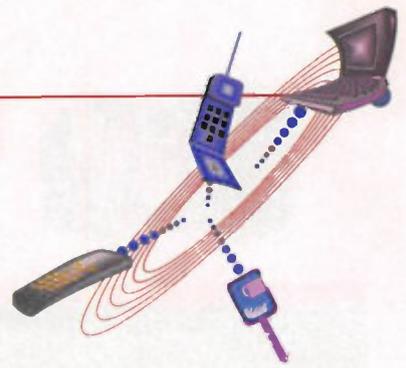
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# Object lesson in patience

By Mike Brookes

Retail giants have been waiting – ever more impatiently – for the production of new extended range of radio frequency identity (RFID) tags for use in their supermarkets.

The new tags depend on the use of UHF spectrum in the 865-868MHz band. To gain access to this, a new radio standard was needed, without which the RFID manufacturers could not proceed with development or marketing. The procedure leading to the publication of the standard EN 302 208 is an object lesson in patience and impatience.

Radio standards, including those for short range devices (SRDs) begin life as a proposal from industry or government to ETSI (European Telecommunications and Standards Institute). In this case, initial proposal was put to ETSI RP08 (General Short Range Devices Committee) in 2001. Due to reorganisation in ETSI, the development of the standard was given to a new task group TG34, chaired by the Low Power Radio Association (LPRA) council members.

ETSI task groups comprise members from the industry and the EU administrations, meeting three or four times a year in venues all over Europe, to draw up the text of the standard and conditions for use. Progress follows a more or less fixed pattern. The draft standard is presented to other more senior

cause destructive interference. This is an ideal stage for opponents to throw 'spanner in the works', to delay or even destroy the new standard.

Assuming successful conclusion, usually with reservations, the studied standard is returned to ETSI for further mullings and modifications until, eventually,

appear in CEPT/ERC recommendation 70 03, which is a sort of bible for the SRD industry. At this stage, it might be thought that this is the end of the road, but 'No'.

Suddenly, EU administrations that have followed the development of the standard for years, find that it is incompatible with some arcane use of the spectrum in their state and cannot agree to it. This immediately wrecks the harmonisation effort that would enable uses of the new standard unhindered access to all EU states and, if not resolved, leads to further costs and delay to the industry, suppliers as well as users.

For EN 302 208, after four years' effort, this is exactly where we are. Vive la EU!

.....  
“ Suddenly, EU administrations that have followed the development of the standard for years, find that it is incompatible with some arcane use of the spectrum in their state ”  
.....

committees for open consultation and when it is in a sufficiently advanced state, is sent onwards to the ECC (European Communications Committee) working group.

Here, it is mullied over and usually sent to yet another ECC group, WGSE (Working Group Spectrum Engineering) for compatibility tests. These are theoretical studies to determine whether or not equipment designed to the proposed standard will operate harmoniously with other occupants of the band or

it is released by ETSI to public enquiry. Public enquiry (PE) is yet another period of 'baited breath', waiting for approval from sources that, until this point, have never shown any interest. This can be a 'mine-field' zone.

After a successful PE, the emergent standard is then prepared for publication in the OJ (Official Journal of the European Union – a publication listing all new decisions, standards etc) and simultaneously conditions of use are considered. For SRDs these

The LPRA (Low Power Radio Association) is a European trade body that represents manufacturers and users of short range devices (SRDs).

It is active in the production of SRD Radio standards and regulations.

Mike Brookes is LPRA's chairman.

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**Is ultimate testing needed?**

Mike Law (*Letters*, January 2005) is absolutely right to say that the ultimate test of audio amplifiers is to put a signal in and compare it with the signal out, suitably attenuated, using a differential amplifier.

Speaking as one who has done this, however, I can assure you that the test is very difficult to make any sense out of. The problem is one of interpretation. Even such a simple test as comparing two interconnect cables of different LCR characteristics will give a residual typically as little as 50dB down in the top octave of audio, due to phase shifts of a very few degrees and amplitude attenuation of a few hundredths of a dB. One assumes that these are trivial and devises a first-order approximation to a correction (this can be done in analogue or digital domains, depending on the test attempted). The digital domain has the usual advantages, not least, that it saves a lot of soldering. The result will be an improved null.

There will certainly still be effects that seem to be linear and perhaps should be compensated out. We can proceed iteratively, constructing simple filters that compensate for these 'unimportant' factors. At some point, real distortion becomes evident, but what to make of it?

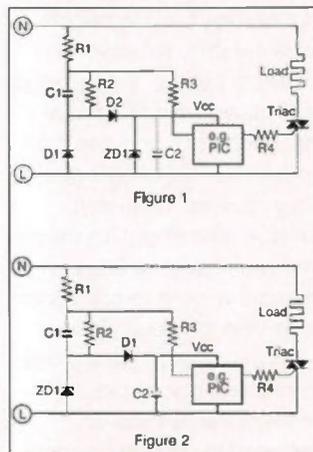
If we're using real music as a stimulus we can judge it by ear but that gives no guarantee at all of a sensible weighting because masking and related effects completely alter the relative importance of various kinds of distortion at various frequencies and levels in the presence of the 'wanted' signal. If spectrum analysis is what we're after, sinusoidal excitation in the traditional manner is much easier.

Only when an amplifier is so linear that its distortion drops right down into noise is this kind of nulling test really conclusive. In that (rare!) circumstance, a series of ordinary distortion measurements across the band would have told us the same answer a lot quicker. It's an interesting approach, but it involves a considerable amount of work.

**Richard Black**  
London  
UK

**Simple mains power – improved**

In my Circuit Idea in the February issue, I managed to swap the Live and Neutral connections, thus contravening the Low Voltage Directive that prohibits switching of the neutral line. Here are the revised diagrams with the correct markings and tracks.



**Nick Cornford**  
Berkhamsted  
UK

**DIY power station**

I would like to know how to set up a standby power station. I purchased a 1500W inverter and two 100A/hr batteries so I have 24V in and 230V out. OK so far, but how to automate it all?

What I need is a good

reliable auto-switching circuit that will detect mains failure and switch over (24V at up to 70A) also 240Vac at the same time so as to isolate the inverter when not in use, plus a charging circuit (switch-mode 24Vdc out at up to 20A). It has to be fool-proof.

I would also like to include a wind or solar back-up system. The inverter I have is not the best because it only gives 230V pk-pk not rms, and is square wave out, which on load produces loads of RF hash. I have tried filtering it with limited success.

Another thing I have yet to grasp is how to feed excess power back into the grid? At best it could only feed the same phase back to the local transformer. When the supply is designed to be one way how can you pump against the flow? What of the need to synchronise the wave forms and what if the generator slows down? Will it back-feed from the supply due to reduced output voltage? (No diodes can be used here).

I can't find a good book on the subject and I do not have access to the Internet at this time.

**Ian Johnson**  
UK

**Do not risk electric shock**

Towards the end of Nick Cornford's article (*EW*, February, p44) is the statement "less important with AC, which doesn't cause muscles to clench". IEC 60479, which is the authoritative document on the physiological effects of electric current, considers three levels of current:

- Threshold of reaction – minimum value of current that causes involuntary muscular contraction;
- Threshold of let-go –

above this threshold a person gripping the source of current would be unable to release the grip;

- Threshold of ventricular fibrillation.

**Typical values for 50Hz AC and DC are:**

	AC	DC
Reaction	0.5mA	2.0mA
Let-go	10.0mA	No definable threshold; only making and breaking current leads to painful and cramp-like contraction of the muscles
Fibrillation	For shock durations less than 200ms	The current values for AC and DC are about the same. For longer durations the values for DC are considerably higher than those for AC.

Do not risk electric shock at 230V, whether AC or DC. The limiting values for Safety Extra Low Voltage (SELV), which are considered safe to touch, are much lower.

**Ted Smith**  
Wilmslow  
UK

**Remember Nyquist?**

I am extremely puzzled by some of the statements that have been made recently about transient distortion in audio amplifiers. It is as if the protagonists have never heard of black-box theory or of all the work carried out by Bode, Nyquist and others on linear systems.

Linear system theories state that the transient performance and the sine-wave response of

linear systems can be exactly derived from their mathematical transfer functions. The only proviso is that all the system elements must remain within linearity at all times. In other words, there must be no non-linearities caused by such things as slew-rate limiting. Any good audio amplifier should never get anywhere near being slew-rate limited when fed with any audio program material.

From the above it follows that all amplifiers that have a flat amplitude response and zero phase-shift over the whole audio band will have exactly the same audio transient performance. There will be no discernable difference between the input and output waveforms when fed with signals that are restricted to the audio frequency spectrum. The problems arise when tone-burst tests are tried. Here we have to be very careful indeed when interpreting the results. An audio sine-wave tone-burst waveform, unless its output is fed through an audio-bandpass filter, has appreciable out-of-audio-band components. At the high-frequency end of the spectrum the effects arise at the abrupt start of the sine-wave burst. Until the time when the input has risen to about 10% of its peak value, the input waveform approximates very closely to a ramp function. To accurately amplify this signal at the very beginning of the ramp demands virtually infinite bandwidth! If, however, we feed such a test signal through a filter that restricts the output to within the audio spectrum, then it will be seen that there is no abrupt change from zero to the linear ramp, there is a gradual change from one to the other. The

audio amplifier will then track this waveform flawlessly.

We must always remember what we are trying to do and that is to reproduce as accurately as possible all signals within the audio spectrum. If we look at the program material available to us, whether FM, compact disc, digital radio, tape, vinyl etc, it is all bandwidth-limited before we get it. Because of microphone frequency responses, studio amplifier responses, finite sampling frequencies for digital, etc, there is virtually no program material that includes frequencies above about 30kHz.

Incidentally, subjective testing of amplifiers etc is fraught with difficulty. In A/B tests it is imperative that the listeners do not know which device is which, when comparing systems. Indeed, they should not be presented with straight A/B tests. It is much better to make the tests more like a random sequence such as ABABABB or AABABBA. In addition, it is imperative that the output audio levels are identical in both cases as, otherwise, even only 0.5dB difference will skew results in favour of the louder sound.

If anyone is really concerned with HF transient response of Hi-Fi systems, then they need to look at the impedance curves of tweeters. It is the current through a tweeter that provides the driving force, yet in a typical dome tweeter, above about 2kHz, this current lags the voltage by some 45 degrees and the impedance rises by some 3dB per octave. This causes major transient distortion within the HF audio spectrum. The possible effect of an amplifier stabilisation output inductor, such as that which so seems to worry

Graham Maynard, is virtually non-existent in comparison with normal tweeter impedance variations.

**Dr Arthur Bailey**  
Ilkley  
UK



### Time off school

The recent research from City & Guilds regarding problems with work placement schemes (reported in *EW*, February, p7) restates a problem that has been known for many years. When Britain had a meaningful engineering base, we had apprenticeships that ensured young people were carefully selected and correctly trained. Today, most youngsters on work placement schemes only see it as time off school or college. They have no interest in learning anything. This means that you require at least one member of staff to constantly supervise the youngster.

I have prepared work placement training schemes for professional associates, designed to make the young aware of what industry is about. One of these was shown to a placement officer, who rejected it. I then discovered that this officer had no qualifications or experience in engineering.

On another occasion I was asked by a government agency officer to take on a person on a work placement scheme. It gave me great delight to ask if they had any candidates with

a minimum of 1st degree level qualifications to work in an engineering and management consultancy.

**David W. Purnell**  
Newport  
UK

### Current knock-on effect

Can the apparent discrepancy between the snail's pace of an electron (Len Cox, *Letters*, February) and the speed-of-light energy transfer through a conductor be likened to Newton's cradle?

For example, when a ball bearing is raised at one end of the string of suspended ball bearings and released, the just-released ball bearing travels a short distance (to the next ball bearing) and then stops. However, the energy transmitted through the train of ball bearing appears to travel remarkably fast, as the ball bearing at the end of the row soon moves due to the transfer of energy to it. You could say that the average speed of an individual electron is slow, (if I recall correctly the mean free path = 4mph) but it can be fast for short periods of time.

**Andrew Ainger**  
Harpenden  
UK

### Hickman's reply to Len Cox

Len Cox raises issue with my dismissal of displacement current as non-existent on two counts. Firstly, it is there in Maxwell's equations. Earlier theories are often overtaken by later work - the existence of phlogiston was once a seriously proposed theory. Secondly, he proposes that a "real current" may not necessarily involve the movement of charge carriers such as electrons (or holes). He goes on to say that he cannot see how electrons moving at "a snail's pace" can be responsible for a

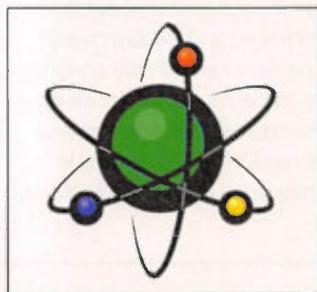
"disturbance" (the interface between stationary and moving electrons) propagating at the speed of light. I can very easily explain that by a simple analogy. Imagine a series of point masses of 10 grams, spaced out along a line from left to right at intervals of 1cm. Imagine each is tethered to its neighbour to the right by a light inextensible string of length 1.001cm. At time  $t = 0s$ , the leftmost mass commences to move to the left at 1cm/s. At time  $t = 1s$ , 1cm of slack in the strings has been taken up. Thus at this instant, the thousandth 10gm mass, way down the line to the right, just starts to move. So the disturbance is propagating at 1000cm/s, although all the moving masses are travelling at only 1cm/s. The light inextensible string is an analogy of the net force on an electron whose neighbour on the left is very slightly further away than on its right.

I do not believe that "displacement current" creates a magnetic field. Consider a resonant vertical quarter wave dipole in free space. The current flowing into the terminal of the upper element returns from the lower. One can either assume (rather simplistically) that this flows via the  $73\Omega$  characteristic impedance of the dipole, or that it arrives at the lower terminal via displacement current. Consider the latter possibility. A changing voltage exists between the two elements, reaching a maximum at the tips, its spatial distribution is well known. This should cause displacement currents to flow in the vertical plane, in the space surrounding the antenna. To determine the field at a distance  $r$  from the centre, at an angle  $\theta$  to the horizontal plane, one simply sums (integrates) the contribution

from the current in each short (infinitesimal) element along the length of the antenna. One does not take into account any field due to the supposed displacement current.

I am satisfied that the explanations in my article are sound and adequate from practical electronic engineering's point of view.

**Ian Hickman**  
Waterlooville  
UK



**Transmission lines and the Catt anomaly**

I agree with Len Cox (Letters, EW, February, p47) that Ian Hickman's explanation is good, but feel that some of the difficulties arise because of assumptions made. Any model is just that – a model, and when real observations don't quite fit we need to look at the assumptions or approximations made in designing the model.

The first thing I take issue with is the assumption of a perfect switch, switching in zero time. Some semiconductor switches can respond in nanoseconds, perhaps even picoseconds, but even if a switch could switch 600V at 1A in 1ps, a wavefront would have moved 0.3mm, which is enormous on the atomic scale.

The second assumption that electrons are effectively at rest, I also take issue with. A conducting gas of electrons, roughly 1.5 per atom in

copper at room temperature, individually move with speeds of  $10^5$  to  $10^6$ m/s but have a net drift rate of zero, in the absence of an applied electric field.

If the transmission line is made of  $1mm^2$  conductors, for  $300\Omega$  the spacing is roughly 7mm, close to that of lighting cable. In a 1m length there are  $8.49 \times 10^{22}$  atoms per conductor. For a 1A current to flow, the net drift rate is  $4.9 \times 10^{-5}$ m/s.

A 1A current in two parallel conductors 7mm apart gives rise to a force of  $2.86 \times 10^{-5}$  N/m, with a very small drift rate. Increasing the current by ten times increases the force by a factor of 100, due to the fact that the force is proportional to the product of the current in the two wires. However, the drift rate has only increased 10 times. My contention is that individual electrons moving at speeds up to  $10^{10}$  times greater must influence one another and at atomic distances these influences must be very great indeed.

If streams of electrons in parallel conductors are travelling in the same direction at the same speed, why is there a force of attraction between the two conductors? Should we not also see a similar effect for two electron beams in a CRT? Yet, I always understood that mutual repulsion of like charges caused beams to diverge. There is also the influence of positively charged copper ions in the cable and an almost zero net charge.

I believe that the wavefront propagating close to the speed of light happens because there is this close mutual coupling and because individual electrons are moving very fast.

This brings me to another poser. It is assumed that electromagnetic waves propagate through a vacuum. How can we know and what do we mean by vacuum? The best vacuum we can create has many thousands of atoms/ $m^3$  and we cannot assume these have no effect. Is deep space free from particles? The only way we can detect electromagnetic waves is by their interaction with matter, so we cannot simply assume that they self sustain. It is more likely that atoms/electrons are briefly given greater energy, which is then coupled at the speed of light to adjoining atoms. Electric and magnetic fields are visual models that we use to explain action at a distance, but we define distance by relationship to the velocity of E/M waves.

This is something of a circular argument in scientific constant derivations. Distance is defined by using the velocity of light (electromagnetic waves), time is defined by the vibrations of an atom, but then we use electromagnetism to couple the two. Notice that gravity (i.e. the presence of matter) also has an influence on both the velocity of light and the passage of time. This I believe is where Len Cox is right, the theory of everything somehow holds it all together, but as yet we don't know how.

**Ray G. Lee**  
Gateshead  
UK

**The sound of music**

We need an amplifier capable of driving real loudspeakers to create the illusion of real musicians with real instruments in real space. This is clearly not easy and is probably not likely to be arrived at only with

measurements such as total harmonic distortion. The measurements need to include the perception of the auditory sounds and space.

There are many poorly understood elements to these perceptions, but significant light has been shed on them by von Békésy (Sensory Inhibition, for which he won the Nobel Prize) and Albert Bregman (Auditory Scene Analysis). The latter author has shown that the ear and brain organise perceptions by grouping sounds (not just frequencies), usually by using transient changes as /zeit-geibers/. Although he doesn't write about the fidelity of sound reproduction, he (and von Békésy) provide much food for

thought on possible mechanisms that might make our hearing very sensitive to distortions of transient or short-lived signals. For example, when equally loud signals consisting of continuous sound are fed first to one ear and then the other, the perception is that of the volume of the new signal in one ear being louder than the previous one in the other ear. This appears to be an example of sensory inhibition (temporal) of the kind von Békésy wrote about. The point is that, for a transitory period, sound appearing in an ear appears to be louder than its continuation. The ear may be more sensitive to the transient change and possibly to its accuracy of

reproduction in the case of music signals.

Graham Maynard provided some clues on what we might additionally measure on our amplifiers driving real speakers and, I hope, others can follow these up. Like with any scientific hypothesis Maynard's work is testable.

Fourier transforms are very useful in analysing amplifiers, but because they infer one mode from the other, they are not sufficient to explain all that goes on in music where both temporal and frequency elements are constantly changing to make music. When we may be interested in accurately reproducing both time and frequency related elements and

their interactions, we may need to examine both simultaneously as Bregman has suggested.

Our engineers need measurements to perfect designs, the users of which care mainly about the illusion of musical reality they create. The challenge is to apply the scientific cycle (hypothesis, test, new hypothesis) to the perception end of the system as well as to the electronic.

Thank you for almost 50 years of enjoyment and stimulation in *EW*, and thanks to Graham Maynard for his insights and challenges.

**Mick Carrick**  
Melbourne  
Australia

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This box consists of a cream base with a PCB slot, a cover plate to protect your circuit, a black lid with a 12 way edge connector and 12 screw terminals built in (8mm pitch) and 2 screws to hold the lid on. The cream bases have minor marks from dust and handling. Price £2.00 + VAT (= £2.35) for a sample or £44.00 + VAT (= £51.70) for a box.



866 battery pack originally intended to be used with an orbitel mobile telephone it contains 10 1.6Ah sub C batteries (42x22dia) the size usually used in cordless screwdrivers etc.) the pack is new and unused and can be broken open quite easily £6.46 + VAT = £8.77



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# Decibel meter

Here, I am describing a decibel meter to obtain gain of two powers in terms of voltages. It consists of two log amplifiers A1, A2 of LM 324 as shown in the figure.

The outputs of these amplifiers go to a differential amplifier A3. The output of A3 goes to a non-inverting gain amplifier A4. The gain of A4 is adjusted with a positive temperature coefficient thermistor and a resistance to give gain of the two powers as output.

The thermistor compensates the variation in emitter saturation current  $I_s$  with temperature. The standard 0dB is taken as 0.77V equal to dissipation of 1mW power in 600Ω resistor. The voltage  $V_{ref}$  forms input of the A2 amplifier. In comparison,  $V_1$  forms input to the A1 amplifier.

**Calculations:**

Amplifier output

$$A1 = \frac{kT}{q} \cdot \ln \left( \frac{V_1}{R_1 I_s} \right)$$

$$A2 = \frac{kT}{q} \cdot \ln \left( \frac{V_{ref}}{R_1 I_s} \right)$$

$$A3 = \frac{kT}{q} \cdot \ln \left( \frac{V_1}{V_{ref}} \right)$$

Where  $k$  = Boltzmann's constant,  $q$  = electronic charge,  $T$  = absolute temperature °K,  $kT$

Emitter saturation current  $I_s = 10^{-13}A$ , the value of  $\frac{kT}{q}$  at room temperature of 300°K is 0.026V.

Therefore  $R_1 \times I_s = 12k\Omega \times 10^{-13}A$

**Practical values:**

Amplifier A1 output = - 0.52V (Here,  $1 = 1V$ ,  $V_{ref} = 0.77V$ )

Amplifier A2 output = 0.51V,

Differential amplifier A3 output = 0.01V

Amplifier A4 output = 3.5V (numerically equal to power gain)

By calculation A4 output =

$$V_i \left( 1 + \frac{R_f}{R_t} \right)$$

(with usual meanings)

$$= 0.01 \left( 1 + \frac{26.7K}{80\Omega} \right) V$$

$$= 3.348V$$

Amplifier A4's gain is adjusted by constants =  $\frac{20 \times 0.4343}{0.026} = 334$

The constants are obtained by following standard relations:

$$\text{Power in dB} = 10 \log_{10} \frac{P_2}{P_1}$$

$$\text{Power in dB} = 20 \log_{10} \frac{V_1}{P_1}$$

(In terms of voltages with impedance match)

$$\log_{10} x = 0.4343 \ln x$$

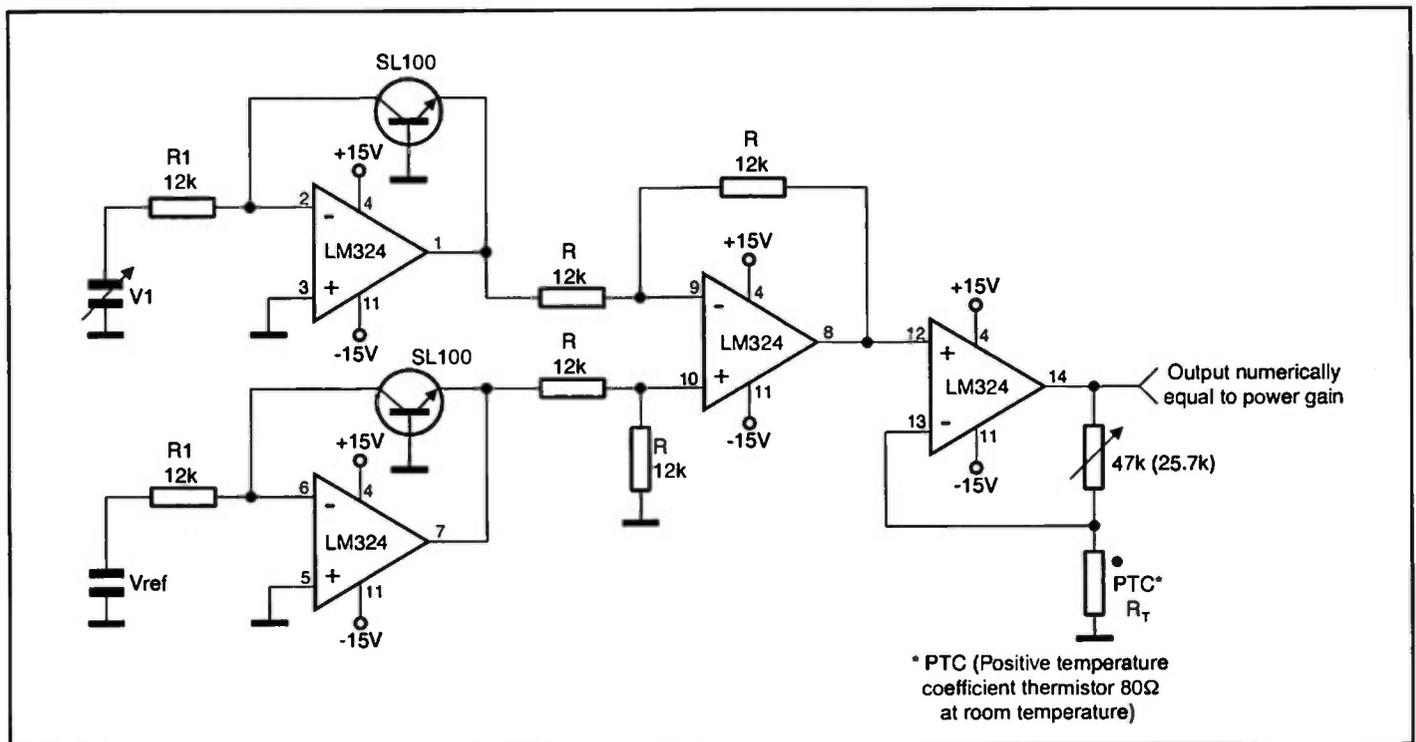
$$\frac{kT}{q}$$

at room temperature of 300°K = 0.026V

Thus the dB meter is constructed with one chip of LM 324.

The cost of the circuit comes to about £1.

**V. Gopalakrishnan**  
Bangalore  
India



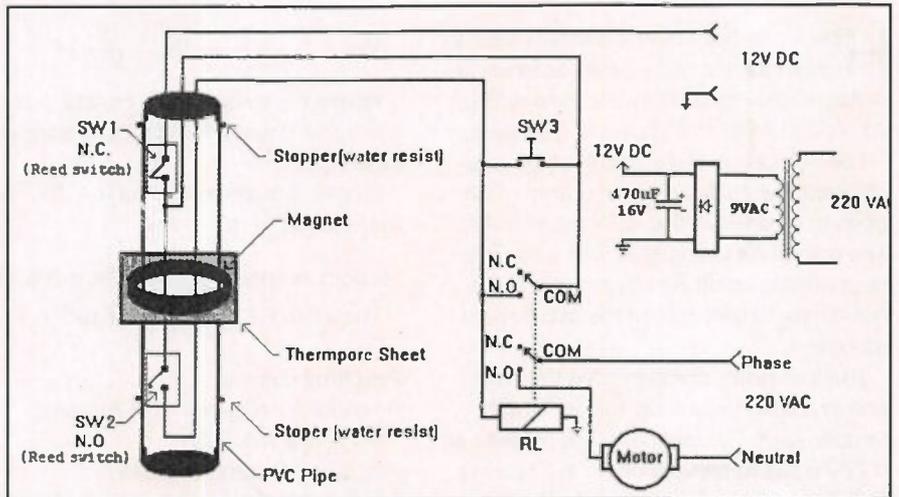
# Automatic water level controller

This is a simple and inexpensive solution of controlling water level of an overhead water tank. The circuit is very simple and very easy to fabricate. SW1 (normally closed) and SW2 (normally open) are miniature reed switches that are enclosed in PVC pipe. Two ends of the pipe are made waterproof by sealing them with a waterproof sealant.

A magnet removed from an old speaker is mounted on thermo pore sheet, which can float on the surface of the water. The magnet can move up and down with the water level and can actuate the reed switches. When the water tank is fully empty, the magnet seats itself on the stopper (as shown in the figure) and SW2 is closed. A 12V power supply is connected to the coil of the relay RL by passing through SW1 and SW2. The relay is energised and phase is connected to the motor of the water pump through one

common terminal of the relay.

When the pump starts to fill water into the tank the magnet moves upward with the water level. When it leaves its seat, SW2 opens but the power supply is still connected to the coil of the relay through the second common terminal of the relay RL. When the magnet reaches the SW1, it opens the SW1 switch and second path of the power supply reaching the coil of the relay is also disconnected. The relay is de-energised, switching off the pump. When water drains from the tank, SW1 is again closed but the power supply



does not reach the coil of the relay. On further draining of the water, SW2 is closed and the relay energises again, thus switching on the water pump again. This process repeats again and again.

The pump does not run continuously but in intervals. The interval depends upon the separation between the reed switches. However, you can switch on the pump

manually by pressing the momentary switch SW3.

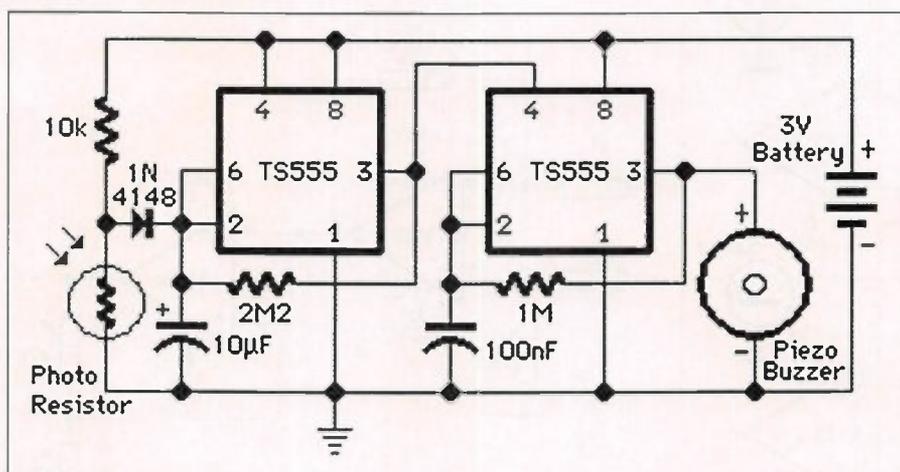
RL = DPDT relay (one pole is used in logic control and one is used to switch ON/OFF the motor), coil voltage = 12Vdc, contact rating depends on the load.

SW1, SW2 = miniature reed switches  
**Muhammad Mateen**  
 Islamabad  
 Pakistan

# Fridge door alarm

My circuit idea is a simple fridge door alarm powered by 3V battery that also allows safe operation even when its voltage falls down to about 1.3V.

The circuit should be placed in the fridge near the lamp (if any) or close to the opening. With the door closed, the interior of the fridge is in dark, the photo

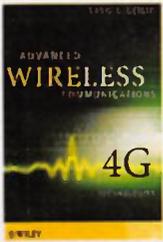


When a beam of light enters from the opening, or the fridge lamp lights, the photo resistor lowers its resistance (<2k) stopping the charging current.

Therefore the first IC, wired as an astable multivibrator, starts oscillating at a very low frequency and after a period of about 24s its output pin (#3)

goes high, enabling the second IC. This chip is also wired as an astable multivibrator, driving the piezo sounder intermittently at about 5 times per second. The alarm is activated for about 17s then stopped for the same time period and the cycle repeats until the fridge door closes.

The timer ICs must be TS555CN or equivalent CMOS types. Stand-by current drawing is 150µA.  
**Flavio Dellepiane**  
 Genova  
 Italy



### Advanced Wireless Communications

Savo G Glisic

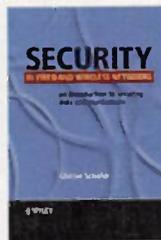
John Wiley & Sons

When I was young I was studying a degree in Electronics at Northumbria University. I was very enthusiastic and wanted to go on to do post graduate research in telecommunications. The reason I never have done is actually because I don't understand the complicated mathematics necessary for modern engineering. If I did, I would be able to understand this book.

If you, like me, are a lesser mortal and not a top telecommunications professional working in the field, borrow the book from a library and read the first chapter. The first chapter of this book is a good introduction to CDMA, OFDM, ATDMA, UWB and all the techniques used in modern wireless Internet, mobile telephony, digital radio and TV. It doesn't actually mention digital radio and TV but will take away the sense of mystery when people use terms like OFDM. Perhaps the publisher could bring out the first chapter in paperback, for those who are simply curious about telecommunications or whose job does not require a very advanced level of understanding. If they did, it would be as good as some small paperback books that are actually on the market.

The first chapter of the book is well worth reading but was as much as I understood. Don't pay a great deal of money for this unless you really understand telecommunications – at an advanced professional level. In the right place, which is a university research laboratory, I am sure this book would be a precious Bible of telecommunications. If you are an inventor who wants to actually design new kinds of OFDM and CDMA transmitters and receivers, in all the years since I graduated I have never seen a book that contains such full explanations – no question is left unanswered, no stone is left unturned. Unfortunately, it is difficult to understand. The mathematics is at a very advanced level. If  $\cos(\omega t)$  is as much as you actually remember from your degree course, borrow the book from a library but don't buy it.

Malcolm Lisle



### Security in Fixed and Wireless Networks

Günter Schafer

John Wiley & Sons

Security in computer and mobile phone networks is a big issue nowadays. Not only can a hacker hear your conversation on a mobile phone, he can

also work out your location. Hackers on the Internet can get into your computer files, read data that might be of a very personal nature, perhaps even discover your credit card number and, while they're at it, might decide to immobilise your computer.

Security over a wireless network is even more of a problem. The signal from an Internet hotspot may travel for anything up to a hundred yards. A criminal could rent a flat near a pub and convince hundreds of people that they were logging into their bank accounts when they were actually logging into a dummy site that would store all their details on the criminal's computer. Solving these problems is crucial to people feeling confident enough to do business over the Internet.

This book explains how mobile phone network security works, how Internet firewalls work, how wireless computer systems can be made secure and reveals some of the limitations of such systems, their problems and how they are being improved.

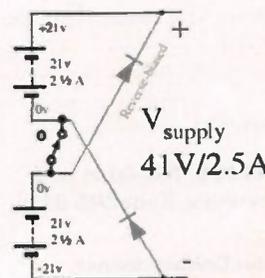
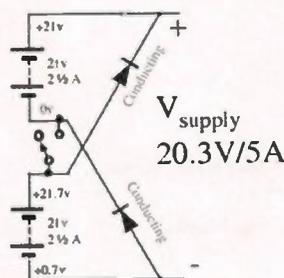
There's a great deal to learn about modern mobile phone systems, the Internet and mobile computer networks – how they work, not only how to protect them – from reading this book. This book is a good introduction for people who don't have good expert knowledge of present day systems. The book is at a reasonable technical level that most people would understand with some effort. There is some mathematics, but the explanations are simple enough. It is possible to miss out a few things that are difficult to grasp and still carry on reading the book.

Malcolm Lisle

## Correction: Efficient bench power supply – EW February 2005 pp40

I'm sorry to say I accidentally reversed the bottom diode in both Figure 2 circuits, making Fig 2(b) an unpleasantly efficient diode destruction circuit. The polarity is correct in the full circuit, Figure 1. My thanks to Ans Vill for spotting the mistake.

Mark Aitchinson  
Christchurch  
New Zealand



Send new circuit ideas to:  
The Editor, Electronics World,  
Highbury Business,  
Media House, Azalea Drive,  
Swanley, Kent BR8 8HU  
or email to:  
[ewcircuit@highburybiz.com](mailto:ewcircuit@highburybiz.com)



## Industrial LCD monitors



PremierView-ABB is the latest release in the range of legacy monitors from display manufacturer Calibre UK. It is designed to connect direct to ABB Mod300/ Tesselator control systems giving excellent image quality.

PremierView-ABB automatically detects the graphics mode in which the ABB system is operating. An on-screen menu system is provided to allow the installer to further optimise the image quality, if necessary.

There are two sizes available – 18.1" and 15". Both provide bright, sharp high contrast images from legacy ABB graphics systems.

Both models are industrial quality metal cased display units with standard 75mm VESA mountings on the rear for use with an optional desk stand and very sturdy side mounting points for console mounting. They are fitted with anti-glare, anti-scratch protective front windows as standard.

PremierView-ABB is based around Calibre's proprietary PremierView4 LCD driver technology with high performance scaling algorithms that work without comprising image quality of resolution, Irrespective of the signal resolution implemented.

[www.calibreuk.co](http://www.calibreuk.co)

## AIMS Interferometer – for MEMS



The AIMS (Adaptive Interferometric Metrology Systems) Interferometer, manufactured by Interferomet Ltd, is a new high precision metrology instrument combining fast, simple set-up with a robust technology.

The instrument can function in non-contact mode as a non-destructive displacement measurement system ideally suited to MEMS materials and devices, wafer fabrication and most high-precision manufacturing applications and nanopositioning solutions. It also enables easy calibration of small precision motion devices. The system can measure displacements of the order of 10nm, varying at a rate of 100Hz or more, with sub-nanometric accuracy.

AIMS employs an innovative

common-path optical configuration, ensuring that the instrument is inherently stable and is unaffected by mechanical changes.

The reference and measurement beams are aligned automatically and the need for dead path error compensation is minimal. The instrument may be used as a standalone system or integrated with other hardware.

The Interferometer uses fixed and moving cube-corner retro-reflectors in conjunction with the beam-splitter head and electronics. So only two simple alignments are required before use: the superimposition of the reference and measurement beams to form interferograms, which must then fall onto photodetectors.

[www.nanopositioning.com](http://www.nanopositioning.com)

## DIN-rail system terminal blocks

The Morsettitalia DIN-rail system from Elkay Electrical has a full range of fuse terminal blocks that are lighter and very cost-effective.

There are 14 models in the Euro fuse DIN-rail range from standard fused, diode, LED and disconnecter blocks. They are suitable to conductor sizes from 0.5mm<sup>2</sup> to 16mm<sup>2</sup> allowing for current carrying capacity from 6.3A to 32A to be used.

The fuse terminal blocks have an easily accessed fuse carrier on the top of the block. This allows easy exchange of the fuse



when necessary.

LED indicators are also available to clearly show when the fuse has failed.

Morsettitalia Euro fuse terminal blocks

come with a full range of accessories including supports, end plates, sliding clamps, copper bars and end brackets. All are designed for use with standard symmetrical DIN rails, resulting in a more compact terminal than normal. Testing organisations that approve the products include the CSA, UL, VDE, IMQ, SEV and KEMA.

[www.elkay.co.uk](http://www.elkay.co.uk)

## USB DEVICE WITH BIOMETRICS

Trek 2000 International launched the first USB portable storage device with the latest biometric capabilities – the ThumbDrive SWIPE.

The device requires the user to swipe their finger across the sensor for verification to access data stored in the device. With the SWIPE, the user has the option of either allowing access via fingerprint verification or password verification. The two key features of the SWIPE technology are its embedded data encryption and embedded cryptography functionalities.

"ThumbDrive SWIPE is developed with the first swipe biometric fingerprint authentication solution," said Rachel Lewis, sales manager at Trek 2000's UK arm ThumbDrive UK. "It is the most secure portable storage device to date – the act of swiping the finger ensures that fingerprints can not be taken from the device and copied – it will be highly suitable for executives who need to transport highly confidential, sensitive or valuable data."

The ThumbDrive combines flash memory technologies with the ubiquitous USB connection to create a self-contained drive and media package the size of a thumb. It plugs directly into the USB port of any computer and can store virtually any digital data from documents, and presentations, to music and photos. Since ThumbDrive acts just like a hard drive, files can be dragged and dropped onto it as well as created, edited, deleted and formatted.

[www.thumbdrive.uk.com](http://www.thumbdrive.uk.com)

## Humidity-resistant lead-free solder

Henkel's electronics group has launched a lead-free solder paste with a resistance to humidity. Multi-core LF318 is a halide-free, no-clean, pin-testable formulation that promises broad process windows for both printing and reflow. The product has been developed to appeal particularly to multinational manufacturers wishing to qualify a single solder paste that offers reliable, repeatable performance within the assembly environment,



under any climatic conditions.

LF318 achieves a consistently high degree of coalescence upon reflow, even after 72 hours at 27°C and 80% relative humidity.

In testing to IPC ANSI/J-STD-005 and JIS-Z-3284 standards, the LF318 displays very good resistance to slump. The main benefits of specifying LF318 are evident during printing and assembly: low paste wastage – the result of superior tack life and an open time greater than 24 hours – and resistance to component movement during high-speed placement, through its high initial tack force of 2.0g/mm<sup>2</sup>.

[www.henkel.com](http://www.henkel.com)

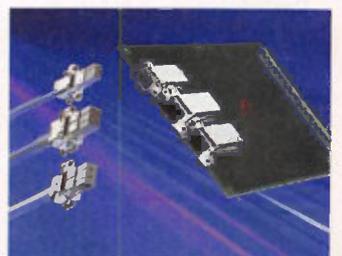
## Ethernet interface tackles telecom rigours

Comprising right angle headers and cable plugs, the SOFIX front I/O interconnection system from FCI has been designed to comply with telecom standards for building practices (IEC60917-2-2 and IEC60297-3). It has also been designed for 20 years lifetime in accordance with Telcordia GR-1217-CORE. Fully shielded down to PCB level, SOFIX is suitable for the distribution of data of up to several Gbit/s, as well as power.

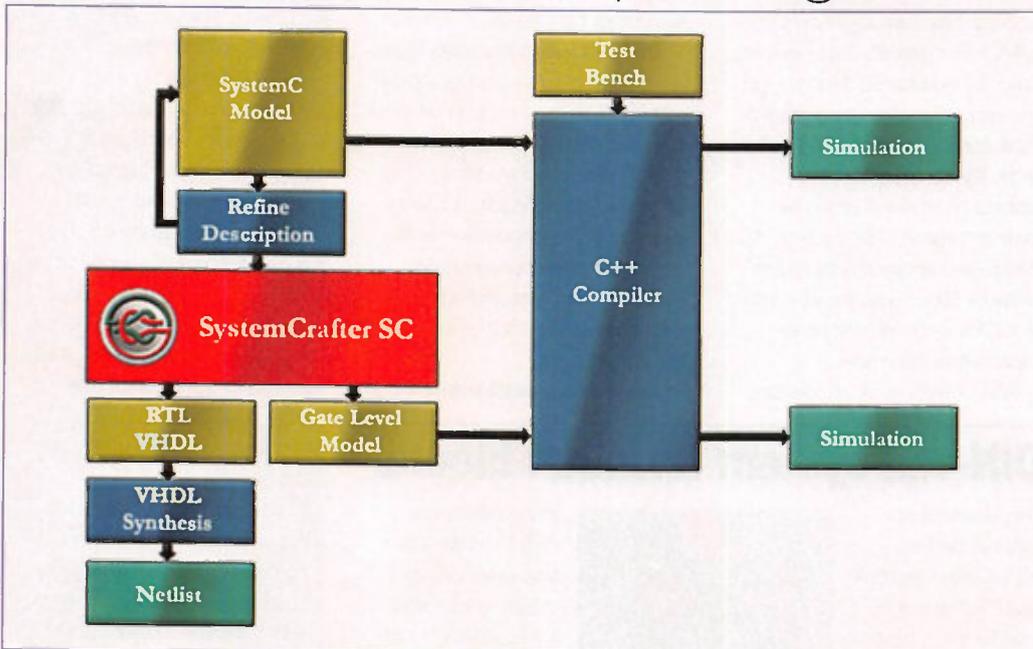
SOFIX PCB connectors are provided as a three-part kit, consisting of a right angle header, metal shield cover and associated spring contacts. The robust connector assembly ensures system ground integrity is maintained between card, front panel and cable plug. Two sizes of high-density connector suit standard 15mm and 20mm pitch card slots.

For a 15mm card slot, the 2x4 position SOFIX connector supports both 10/100 BaseT and 1000 BaseT requirements. With a pitch of just 17.5mm, the connectors can provide up to 45 lines per 10cm of linear board length. Two connectors are provided for 20mm card slots, a 4x6 position connector handling up to 96 lines per 10cm of linear board length, and a 1x2 position power connector. Signal line connectors are available in pin-in-paste versions to facilitate fully automated assembly.

[www.fciconnect.com](http://www.fciconnect.com)



## SystemC synthesis package



Orange Tree Technologies and SystemCrafter announced the SystemCrafter package for SystemC development. The package consists of the SystemCrafter SC compiler, for the synthesis of SystemC to VHDL, and the ZestSC1 FPGA development board. The list price for the compiler is \$995, and the package of compiler and board is \$1490. The two firms say this is a breakthrough in price for

SystemC synthesis technology.

SystemC is a worldwide standard for modelling hardware and software systems using the C/C++ language with a library for hardware constructs. As well as allowing hardware and software to be simulated in the same framework, it is also more compact than VHDL or Verilog. It is faster to write and more maintainable and readable, and can be compiled into an executable

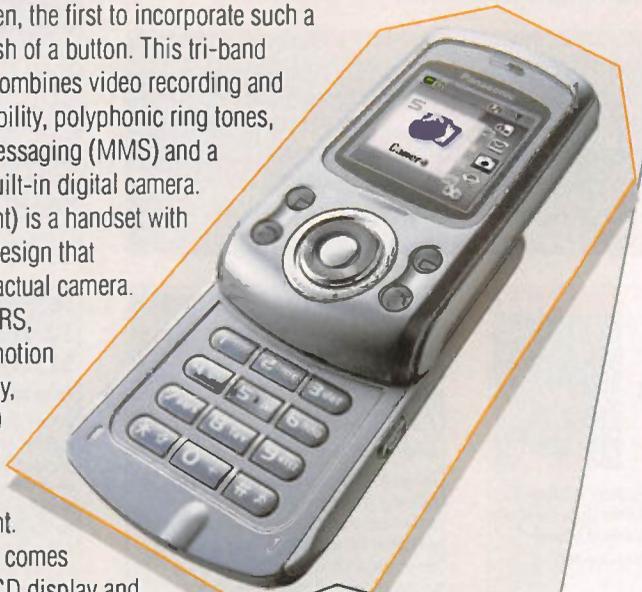
specification for fast simulation.

SystemCrafter SC automatically synthesises hardware designs written in SystemC to VHDL. The VHDL can then be used with commonly available tools to target Xilinx FPGAs. This enables engineers and programmers to design, debug and simulate hardware and systems using their existing C++ development environment.

[www.orangetreetech.com](http://www.orangetreetech.com)



If you choose either the left or right phone, they are still a Panasonic. The X300 (left) is a mobile video camera phone with a pop-up screen, the first to incorporate such a screen at a push of a button. This tri-band handset also combines video recording and playback capability, polyphonic ring tones, Multimedia Messaging (MMS) and a CMOS VGA built-in digital camera. The X500 (right) is a handset with a small slide design that resembles an actual camera. It supports GPRS, incorporates motion JPEG capability, Java MIDP 2.0 and features a VGA camera with photo light.



The X500 also comes

with Multimedia Messaging (MMS), 65,536 colour TFT LCD display and up to seven hours of talk time as standard.

From under £130 from the high street

[www.panasonicmobile.com](http://www.panasonicmobile.com)

A flying object it isn't, but this portable digital radio – the Aviator 10M – is a first for BT in a new range of digital home communications products. "With our expertise in DECT technology proven, we are hugely excited to be able to introduce the BT Aviator DAB radio," said Gary Tubb, CEO of BT Home Communications. The DAB set also offers the ability to receive standard FM radio stations. Among its other features are a 10-minute record and playback facility, a playback of MP3 files from standard SD and MMC cards, an alarm clock and a digital text display screen that allows the listener to view information about the station they are listening to, including its name, type of music and title of the track.

Retails at under £130

[www.bt.com/shop](http://www.bt.com/shop) or call 0800 102800



"Black rocks", says Altec Lansing, the audio system specialist that has just launched the inMotion iM3 Black Limited Edition. This is a special version of its iM3 portable audio system for iPods that is custom-designed to match the black enclosure of Apple's iPod U2 Special Edition. The iPod U2 is merely placed in the dock of the black iM3, and you get a sound system that, the firm says, looks like a piece of modern black sculpture. The speakers sit on either side of a built-in iPod docking station, which also doubles up as a synchronisation, file transfer and recharge device. The unit provides more than 24 hours worth of playback on four AA batteries. The speakers use a highly efficient digital amplifier that powers four full-range micro drivers and patented MaxxBass technology, which creates quality bass without a subwoofer.

Retails from \$179.95 in Apple stores

[www.store.apple.com](http://www.store.apple.com)

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## TCP/IP EMBEDDED INTERNET APPLICATIONS

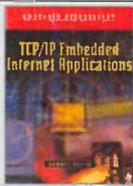
**Edward Insam**

This text highlights an engineer's approach to Internet protocols and applications, reducing R&D time for engineers. The book aims to be the main design guide for the cutting edge of Internet-enabled electronic products and systems.

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Published in UK

Code 1-878707-99-X

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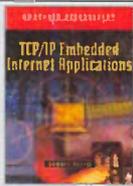
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This self-study text introduces digital electronics from first principles, before going on to cover all the main areas of knowledge and expertise. It covers the practicalities of designing and building circuits, including fault-finding and the use of test equipment.

Feb 2000 ▲ 302 pages ▲ Glossary ▲ Index  
PB ▲ Published in UK

Code 0-7506-4583-0

**£18.99**



## NEWNES DICTIONARY OF ELECTRONICS

**S W Amos; R S Amos**

Aimed at engineers, technicians and students working in the field of electronics, this dictionary provides clear and concise definitions, including TV, radio and computing terms, with illustrations and circuit diagrams.

4th edition ▲ Mar 2002 ▲ 394 pages  
100 illustrations ▲ PB ▲ Published in UK

Code 0-7506-5642-5

**£12.99**



## NEWNES GUIDE TO TELEVISION & VIDEO TECHNOLOGY

**Eugene Trundle**

An exploration of television and video technology. It covers the fundamentals of digital television (satellite, cable and terrestrial) and digital video, as well as providing a grounding in analogue systems.

3rd edition ▲ Feb 2001 ▲ 432 pages ▲ Index  
PB ▲ Published in UK

Code 0-7506-4810-4

**£17.99**



## NEWNES GUIDE TO DIGITAL TV

**Richard Brice**

Covering all aspects of digital television, this text encompasses the electronics of the equipment, data compression, television production, servicing and the different transition methods - terrestrial, satellite and cable. The text has been updated with developments since the 2000 edition.

2nd edition ▲ Oct 2002 ▲ 304 pages ▲ Index  
45 illustrations ▲ 15 photographs ▲ HB  
Published in UK

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## PRACTICAL ELECTRONIC FAULT FINDING AND TROUBLESHOOTING

**Robin Pain (Design Engineer, Cotag International Ltd)**

A text using simple circuit examples to illustrate principles and concepts fundamental to the process of analog and digital fault finding. It aims to help the reader tackle any job, from fixing a TV to improving the sound of a hi-fi. A digital multimeter and oscilloscope are needed for these jobs.

Apr 1996 ▲ 284 pages ▲ Index  
50 line illustrations ▲ PB ▲ Published in UK

Code 0-7506-2461-2

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## PRACTICAL ELECTRONICS HANDBOOK

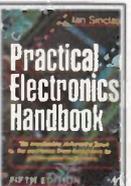
**Ian Sinclair**

A collection of all the key data, facts, practical guidance and circuit design basics needed by a spectrum of students, electronics enthusiasts, technicians and circuit designers. It provides explanations and practical guidance, and includes new sections on SHF techniques and intruder alarms.

5th edition ▲ Feb 2000 ▲ 571 pages  
Illustrations ▲ PB ▲ Published in UK

Code 0-7506-4585-7

**£16.99**



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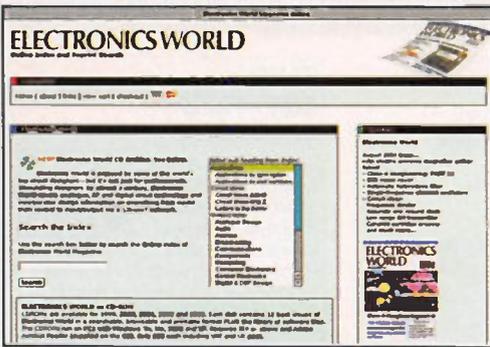
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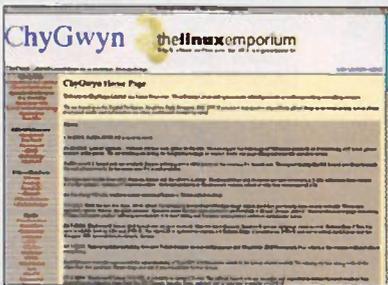




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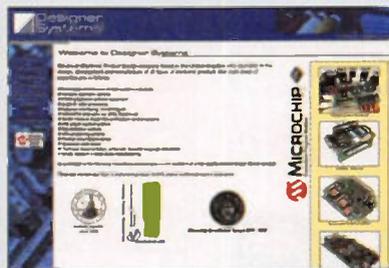
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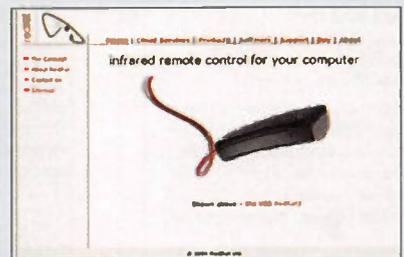
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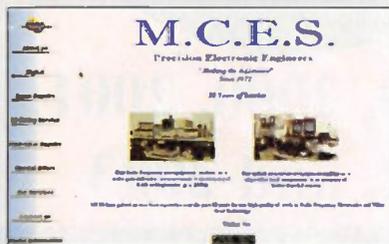
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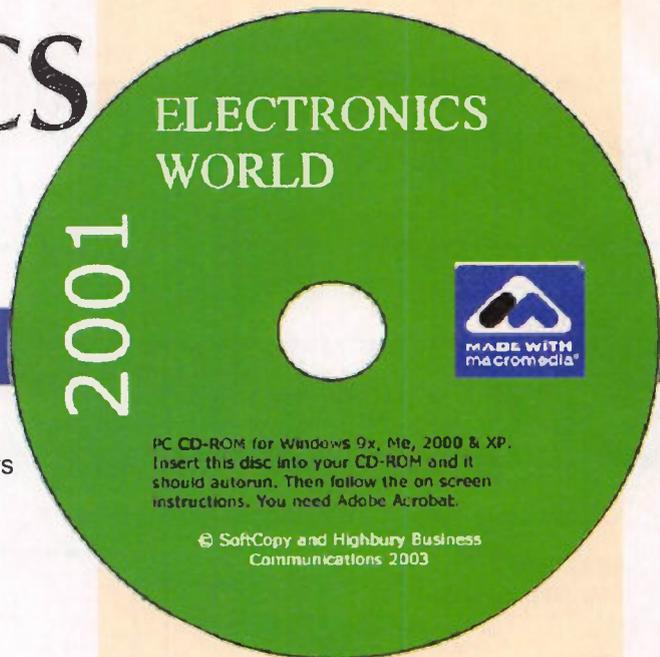
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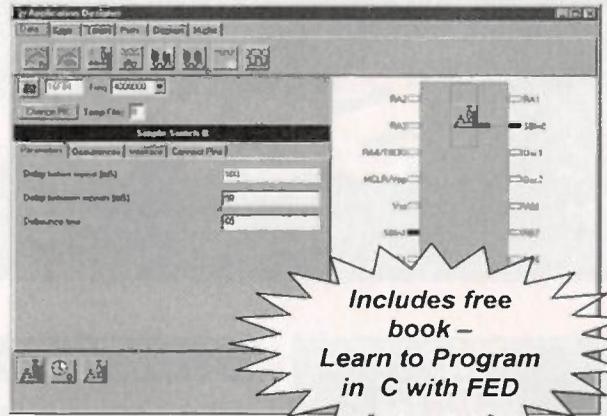
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AT/HP 8594E/041 2.9GHz Spectrum Analyser	4500	149
AT/HP 8595E/004/021/101/105 6.5GHz Spectrum Analyser	6750	204
AT/HP 8596E/041/053/140/151/160 12.8GHz Spectrum Ana	11950	365
AT/HP E4403B/A4H/B72/049 3GHz Spectrum Analyser	6250	225
Anritsu MS2651B 3GHz Spectrum Analyser	3950	186
Anritsu MS2711B/05 3GHz Handheld Spectrum Analyser	3650	132
Anritsu MS610B 10kHz-2GHz Spectrum Analyser	2150	65
Anritsu MS710C 10kHz-23GHz Spectrum Analyser	6500	195
Marconi 2392 9kHz-2.9GHz Spectrum Analyser	2750	83
R&S FSEA30/B4/B5/B7 20Hz-3.5GHz Spectrum Analyser	14750	585
R&S FSP3 3GHz Spectrum Analyser	10450	425
R&S FSP7/B1/B3/B4 9kHz-7GHz Spectrum Analyser	16950	685
<b>SIGNAL GENERATORS</b>		
AT/HP 83711A/1E1 1-20GHz Synthesised CW Signal Gen	7950	239
AT/HP 83712B/1E1 0.01-20GHz CW Generator	13950	575
AT/HP 8648C 9kHz-3.2GHz Synthesised Signal Generator	5500	224
AT/HP 8657A 1GHz Synthesised Signal Generator	1600	46
AT/HP 8657B/001 2GHz Synthesised Signal Generator	2350	71
AT/HP E4432A 3GHz Synthesised Signal Generator	6950	278
AT/HP E4433A/1E5 250kHz-4GHz Synthesised Signal Gen	7950	239
AT/HP E4433B 250kHz-4GHz Signal Generator	10000	485
Anritsu 68047C/2A/16 10MHz-20GHz Synth Signal Generator	10950	395
Anritsu MG3601A/02 1GHz Signal Generator	1600	46
Marconi 2031 2.7GHz Synthesised Signal Generator	3650	146
Marconi 2031/01/07/08 2.7GHz Sig Gen + Dig Vector Mod	4950	147
National VP-7201A 500kHz RC Oscillator	485	15
R&S SMH 2GHz Synthesised Signal Generator	3650	146
R&S SMHQ3B/B1/1/11/12/14/... 3.3GHz Vector Sig Generator	11950	359
<b>WIRELESS</b>		
AT/HP 8920B/1/4/7/13/14 1GHz Radio Comms Test Set	3950	119
IFR 2967/12/16/21 Radio Comms Test Set With GSM & TACS	5950	179
Marconi 2935 GSM Test Set [Tri Band]	4950	179
Marconi 2945/05 Radio Comms Test Set	5950	150
Marconi 2955B 1GHz Radio Comms Test Set	3500	124
Marconi 2966A/1/12 1GHz Radio Comms Test Set with GSM	5850	176
R&S CTD55/B5 GSM GO/MOGO Tester	1850	95
Racal 6103/001/002 Digital Mobile Radio Test Set	3950	159
Racal 6113/01/02/04E/52 Base Stn Tester (GSM 900/1800)	3350	155
W&G 4106 GSM/DCS1800/PCN1900 Mobile Phone Tester	2250	70
Wavetek 4107 Mobile Phone Test set - Triband	2750	83

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