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Contents

For the Arthur C Clarke
"Past and Present" supplement
See centre pages

October 2005

Volume 111

Number 1834

Editor's Comment	3
True pictures lie in the aggregate	
Technology	4
Top Ten Tips	9
Insight	10
Colin Hunter looks at the history and future of powerful supercomputers	
Focus	12
Caution: lead-free reflow may cause damage Keith Gurnett and Tom Adams	
The Buzz of ZigBee	14
Dr Faiz Rahman analyses this new communications technology	
Designing wireless chips	18
Designing a modern radio frequency (RF) ASIC. Jürgen Hartung	
2.5GHz radio demonstration circuit	22
...with a two-stage power amplifier chain, a broadband low-loss SPDT switch and an ultra-low-noise amplifier in the receive chain J S Lee, R Remba and M J Bailey	
Simple microwave filters	26
Paolo Antoniazzi and Marco Arecco	
No MMIC? No WLAN	30
Susan Curtis of the Institute of Physics discusses new developments of millimetre-wave monolithic microwave integrated circuits (MMICs)	
DIY	36
Taking a computer apart is easy enough. Boris Sedacca shows you how...	
Gadgets	41
Tips 'n' tricks	42
PICmicro: Microcontroller CCP and ECCP – the series continues	
Letters	45
Wireless Column	47
Vive l'indifference. Mike Brookes	
Circuit Ideas	48
<ul style="list-style-type: none">• Nearly ideal parallel resonant circuit – computer controlled• Three-way electronic appliance timer• Simple indicator circuit for pin 8 on a Scart socket	
Book Review	55
Products	57

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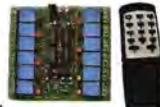
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True pictures lie in the aggregate

There's been quite a debate going on recently instigated by a research market analyst. And as in any case of a "hedge dispute", this one has two sides too. Malcolm Penn, founder and CEO of industry analyst house Future Horizons says that today's chief executive officers of semiconductor firms do not have the 'guts' for the business compared to their equivalents of the 1970s. He calls the new crop of CEOs "risk-averse", lacklustre and good for "brewing beer or making cream crackers, where the business trends are easier to predict". During his presentation on the state of the industry – present, past and future – Penn reminisced of yesteryear, when, he says, the chip business was full of vigorous characters with street-fighting spirit – "strong leaders", he says; when Jerry Sanders of this world were captains of the industry.

Penn went on to say that today's chip bosses are only interested in the bottom line and how to keep the company coffers full without investing in the future. They have become meek under the pressure of financial burdens and expectations of immediate returns. As a side effect, they are not investing in R&D, which typically generates products for future returns.

Unsurprisingly, his provocative comments were matched with opposition. The defence says that today's semiconductor bosses are a second generation of CEOs. Whilst the first generation were playing with their own money – as young entrepreneurs eager to make their mark on the world – the second generation are looking after somebody else's money instead – that of the shareholders – hence, the lack of 'playfulness' with it. The first generation set up private companies that grew into the public conglomerates of today, and with that came the appearance of 'sluggishness', as CEOs are aware that no shareholder would be willing to invest in a firm where the top man is risk-prone with funds.

This attitude is further compounded by another big influence on the world's financial scene – Wall Street. One Wall Street analyst, Philip Coburn, was recently quoted as saying: "It is no longer accept-

able to Wall Street for companies to make longer-term strategies designed to pay back four or five years in the future." Penn names this school of thought "the Coburn dictate" and a "recipe for death for silicon companies".

The second prong in Malcolm Penn's attack on the semiconductor business is along the lines of lack of innovation. He says that, "the products today are not leading technology products like before".

The opposition disagrees yet again. They say the technology on the micro scale of the 70s could not do what 90nm or, indeed, 45nm technology could do today. They say "That's true innovation". "When I was at school," says Derek Mayer of processor cores supplier ARC International, "my 'mini' computer was 0.75DMIPS and sold for \$750. Today, you get a processor core with a performance of 800DMIPS and that sells for single-digit dollars. "That's innovation!" he says.

What about the proliferation of wireless technologies that didn't use to exist in the 70s? The opposition continues. These devices enable not only communications but true 'from office to office' environment. A small computer costing hundreds of dollars in the 70s could not match the technical performance of small portable device today that carries gigabytes of memory and gigahertz of processing power – in a miniature packaging.

But, some see these trends as progress rather than radical innovation. Progress is an inevitable result of product development. So, the first transistor was innovative, the first IC was innovative, everything from then on is just a development of doing what's already been done before.

This dispute, as disputes go, is likely to remain in place: everybody is entitled to their opinion. But one thing remains certain: Each era has its own innovations, ups and downs and leading characters. As suggested by Meyer, the trick, then, would be to probably look at the "aggregate [of an era] to see the true picture".

Svetlana Josifovska
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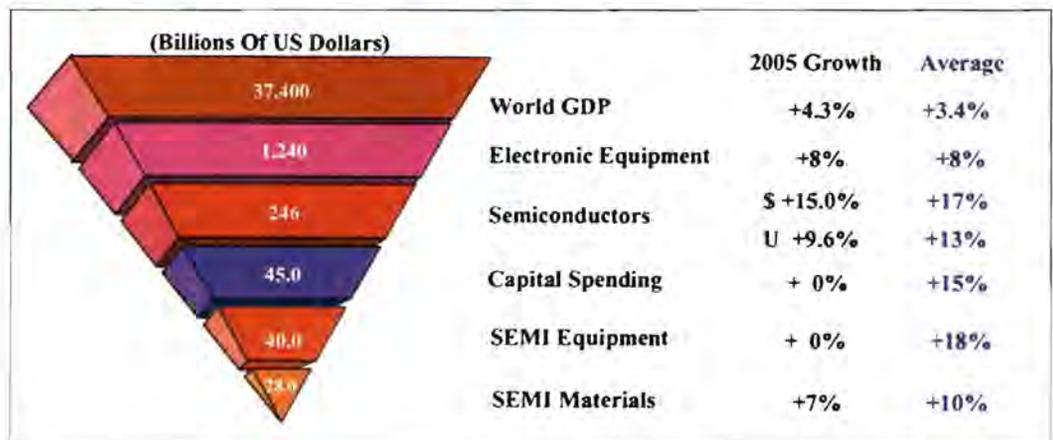
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Chip industry is doing well, but not its captains, says analyst

The semiconductor industry is doing well, with a projected growth rate of 15% for 2005 rising to 20% in 2006, but at the same time, it is losing its competitive edge. This was the message from Malcolm Penn, founder and CEO of market analyst firm Future Horizons, at a recent industry event.

"The world economy is decent, there's no near-term [fab capacity] overheating in prospect, the inventory burn has finished and unit demand is good. Q3 is set to be the strongest quarter ever for unit shipments. We are approaching the 10 billion ICs per month run-rate. We've never seen such figures before. Fab capacity is tight and getting tighter. All these are good signs for the industry," said Penn.

However, this summary was immediately followed by a scathing remark on the new crop of semiconductor bosses. "People have forgotten how to compete in this industry. They are not taking enough risks. If you don't take risks, the company will die."



"Today, you don't have the guts the strong leaders had in the 70s; the Jerry Sanders of this world. Today's CEOs don't have the stomach for it. This industry needs the street-fighting spirit," he added.

What Penn wants to see instead is increased investment in R&D and more radical innovations. "The products [today] are not leading technology products like before. CEOs should put money in R&D. Instead, they have closed research centres – even though they are sitting on billions. What a pathetic way to

look after your money. Laying R&D people off is not smart. You should tell them to go and invent something to bring profits in five years' time, instead."

This goes in the face of a recently prevalent Wall Street dogma, which discourages firms from making long-term strategies that might pay back four or five years in the future. Penn branded this a "recipe for death for silicon companies", who take up to two years to build a fab and a further year or so to see the first results from them.

However, the silicon industry disagrees with Malcolm Penn's comments. "Try and tell those engineers working 20 hours a day that they are not inventive," said Derek Mayer, vice-president at ARC International, a fabless designer of MPU cores. "I am in London, my office is in California and I am sealing a deal with a sales person in Taiwan with my email-enabled handset – whilst at dinner! If that's not innovation, then I don't know what is. Nobody could imagine in the 70s that this was even possible."

• Nanowatch • Nanowatch

Carbon nanotubes will soon be used in injections to help treat broken bones. When injected into the bone, carbon nanotubes will act as an artificial scaffolding to allow new tissue to grow around it. They are one of the toughest materials around; less likely to be rejected by the patient's body and easier to handle than having grafts, says US researchers.

Innos and the University of Southampton will conduct R&D into dopant diffusion suppression in semiconductors. This work will carry

on from a pioneered new technique that uses optimised fluorine implants to completely suppress boron transient enhanced diffusion in silicon and silicon-germanium, and significantly reduce boron thermal diffusion.

Bio-Nano Sensium Technologies, a joint venture between Toumaz Technology and Advance Nanotech has launched its first working platform of a wireless healthcare monitoring system. This is an ultra low-power body implant, which detects ECG, blood oxygen, glucose, body temperature, motion and

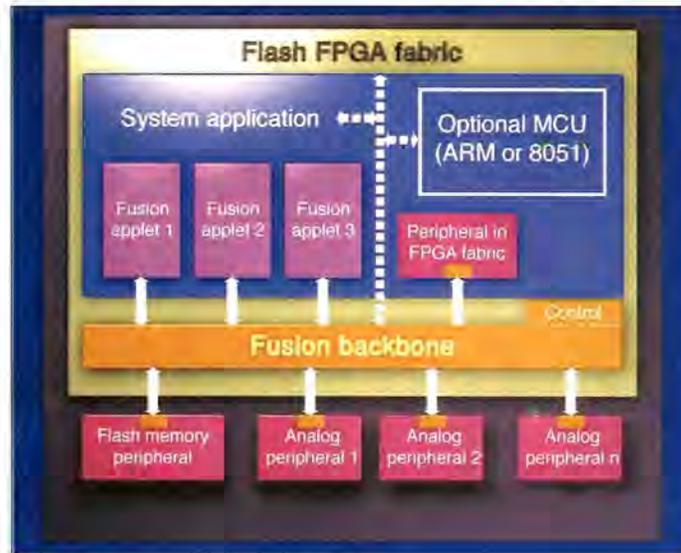
mobility, and wirelessly transmits any "problem event" data to network nodes.

Innos has further expanded its team with the appointment of a Commercial Integration Engineer and a Process Engineer. They will be responsible for interfacing directly with clients and overseeing research projects completions at the Innos cleanroom facility in Southampton. Riccardo Varrazza is formerly of Ericsson Telecomunicazioni Italy and Enrico Gili of the STMicroelectronics (ST) R&D facility in Crolles, France.

Actel advises Fusion for a “true” mixed-signal programmability

Actel has, for the first time in industry, combined analogue functionality with FPGA fabric, non-volatile memory and an MCU core in a single, monolithic device. With its Fusion technology, the firm promises to bring “true programmability to mixed-signal solutions”, for areas that have traditionally been served only by discrete analogue components and mixed-signal ASICs.

Although known for anti-fuse technology, Actel has used its flash-based FPGA fabric for this programmable system chip (PSC). For the analogue functionality, it used high-voltage transistor technology, which helps with the noise immunity, so the analogue section of the chip can be better isolated from the digital section. The FPGAs can be connected directly to high-voltage input signals, with no need for external resistor



Actel Fusion silicon physical view

divider networks. This reduces component count and increases accuracy.

The PSC offers a scaleable number of fixed, analogue peripherals that connect to the Fusion “backbone”, which is

implemented in the FPGA fabric, as are the system applications’ building blocks (applets) and the soft MCU core (for now, ARM7 or 8051-based). The FPGA can also be used to create additional

peripherals, if wanted. Nevertheless, they are still treated equally by the system, regardless of whether they are hard-wired or soft IP.

The Fusion ‘backbone’ is a flexible bus, which controls the communications between peripherals but also, with the help of an in-built IP, configures them based on information stored in the embedded flash.

The PSC will allow designers to work at a very high or very low level of abstraction. Analogue block settings can be re-configured to perform different functions by downloading data from the embedded flash memory. The initial Fusion family members will be general devices for accuracy rather than speed. However, the company plans to introduce specific, vertical applications devices in the near future.

The government is not doing enough on RoHS

The Department of Trade and Industry (DTI) in the UK is failing to support the electronics industry with guidelines on the RoHS (Restriction of the Use of Certain Hazardous Substances) compliance despite the directive’s imminent start, say industry representatives. At a recent electronics assembly event, organised by NPL, an R&D and measurement organisation partly funded by the DTI, several industry representatives openly voiced their concern and disappointment that there’s a lack of specific RoHS guidelines so close to the directive’s starting date – July 26, 2006. Whatever little

information is available has been described as “nebulous”.

“Products manufactured now will be shipped and used well after the July 1 2006 date, when the RoHS was meant to start. It would be useful to get some guidance from the DTI now. We need to know how the compliance works. To say ‘follow reasonable steps’, as the DTI advises, is not enough. The industry needs proper guidance and what it needs to do,” said one industry event-participant.

James Lingard from the DTI, who also attended the NPL-organised event said: “There’s not enough awareness – we are doing the best we can. We

are also working closely with the EU on this.”

According to the DTI, the EU guidance document should help in the “significant ‘gray areas’” that exist in specialised or industrial sectors, however, “ultimately, only the courts can give a definitive answer” and that companies “should consult a lawyer”. Ligard added that the DTI is committed to working with

industry on compliance.

But, industry representatives were difficult to placate, at least during the event, stating: “We don’t want to be your test-case, because you [at the DTI] have ‘fuzzy’ thinking [on this issue].”

RoHS aims to reduce the use of hazardous substances during manufacture. It seeks to restrict lead, mercury, cadmium, hexavalent chromium and certain brominated flame-retardants in electrical and electronics components and equipment.

TTI Europe has already launched RoHS-compliant chip ferrite beads suitable for high-power applications



Schaffner is looking for buyers for its test equipment and systems businesses. The Schaffner group has recently evaluated its strategic position and has decided to concentrate its resources on its already highly successful EMC components business to further enhance its market position. Paul Dixon, Schaffner Ltd's managing director said: "Seventy percent of our business is component sales and we need to continue to invest in new products and processes to maintain our market leading position for the long term. We have had a very positive response to this decision from our major test equipment customers and while we find the best partners for our Test Systems Division to join it will be business as usual for sales, support and service."

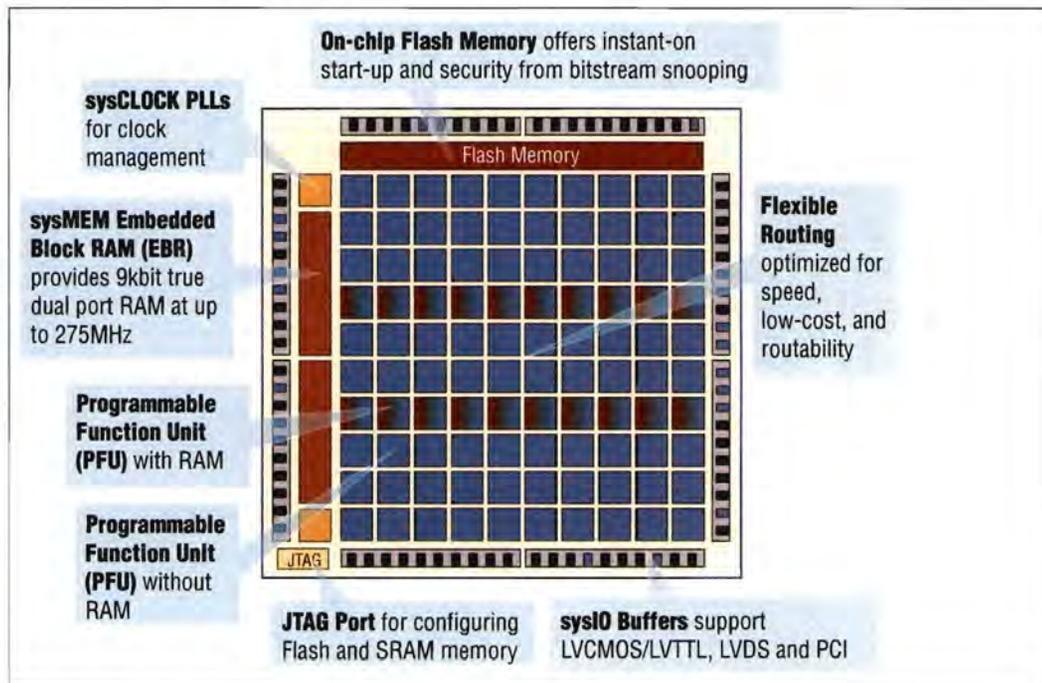
Ω

The Ilfracombe-based power supply specialist Lambda has been bought by Japanese giant TDK for £134m. The agreement includes Lambda's entire North American and European operations, as well as Invensys's (Lambda's parent company) current 58.2% shareholding in Denset Lambda KK. The combination of TDK's existing power supply business with that of Lambda will create the second-largest power supply manufacturer in the world, with the largest market share in the industrial power sector by some considerable distance.

Ω

Cambridge-based Bluetooth leader CSR is acquiring UbiNetics's software business for \$48m. UbiNetics is also based in Cambridge and specialises in communication protocol software for mobile phone manufacturers. By acquiring UbiNetics's R&D expertise, CSR hopes to accelerate its existing software developments in Bluetooth, Wi-Fi and UWB (Ultra Wide Band). UbiNetics has been developing protocol stacks for GSM, GPRS, EDGE, WCDMA (UMTS) and HSDPA since 1999. CSR now plans to use this IP to provide multimode software to handset makers and to "bundle" UbiNetics's cellular multimode and HSDPA stacks with its existing wireless protocol and DSP software.

Lattice launches "crossover" programmable logic



Lattice MachXO block diagram

Lattice launched a new family of re-programmable devices aimed at the "crossover space" between CPLDs and low-capacity FPGAs. The so-called MachXO family offers the high pin-to-pin speed of CPLDs but with the high pin-to-logic ratio, flexibility and distributed memory of an FPGA. It also features an instant 'on' capability enabled by combining flash and SRAM memory.

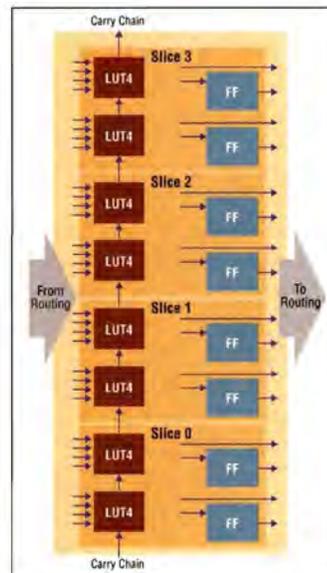
At power-up, the configuration is automatically loaded to the SRAM (which configures the 4-input look-up table, or LUT, fabric) in under 1ms. If there's re-programming to be done, the configuration is loaded to the embedded flash via the JTAG, whilst the logic continues to operate normally out of the SRAM.

With these features, the family is aimed at control, bus bridging, bus interfacing and

signal distribution functions, much like the CPLDs are. However, the LUT-based architecture 'borrowed' from the FPGAs allows more features and, yet, lower cost-per-gate logic. LUTs offer good performance and the 4-input LUTs offer better area efficiency.

In addition, MachXO features a low standby power sleep mode – up to 100 times less standby power than in FPGAs, for example. "Power is critical in all devices. We can carry microamps of current," said Stan Kopec, vice president at Lattice.

Initially, there will be four devices in the family, of different sizes and I/O counts. The larger devices offer embedded block RAM, which can be configured as single and dual port, or FIFO memory. The larger devices also have PLL clock circuitry



Lattice MachXO programmable function unit (PFU)

and PCI and LVDS I/O, typically found in traditional FPGAs.

Two of these devices – the MachXO256 and MachXO640 – are available immediately.

Components are getting smaller and trickier

The 0201 and 01005 component sizes are the tiniest around but also create the biggest headaches for the electronics industry. They can now go through the eye of a needle, but that's not such a good thing when it comes to their storage, transport, pick and place, and even legend markings, says Peter Grundy director of the electronics manufacture consultancy PG Engineering.

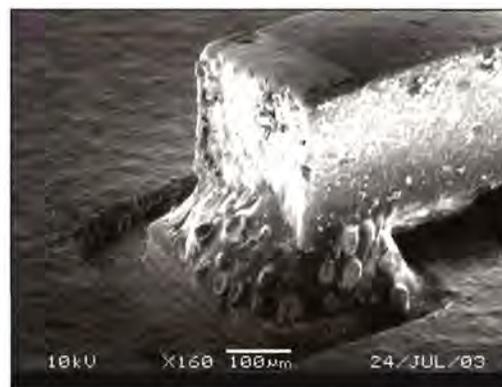
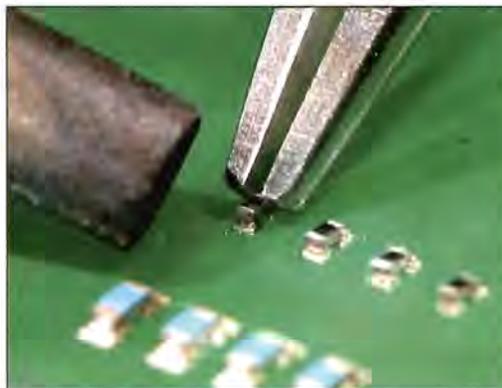
The nominal dimensions of the 01005 resistor are 0.12 x 0.2 x 0.4mm, whilst for a capacitor 0.2 x 0.2 x 0.4mm. "If you are a designer, there are characteristics that will be very important to you, like the power rating, the dielectric, the resistor tolerance and so on, but the design requires small [components]. The tiny devices have limitations – they do not have all the possible values, tolerances, dielectric variations etc."

"Then there's the handling [of them]. Tiny capacitors in particular are difficult to handle: which position to put them in, how do you print the legend on them?" asked Grundy.

The whole nightmare begins at the tape and reel end. The standard 4mm paper pitch makes for a very inefficient use of tape to package these devices in. Paper purity is also highly important in avoiding contamination from fibres. The industry is already considering 2mm pitch and punched paper, as embossed plastic is too loose to house such tiny components.

Connecting such small components is another problem. "How do you define the gap between the pads, what size soldering ball do you place on them without risking bridging and how do you connect them?" Grundy carried on. "There are also the limits of the stencils. The apertures are so small, they get blocked with debris, dust particles and all sorts very quickly." Hence, the pad area must be bigger than wall area of stencil aperture at least in the 1.5:1 ratio, with a maximum stencil thickness of 0.1mm for such devices.

Debris and blocking are also a problem for the nozzles of the pick and place machines. During pick-up, the component can easily be incorrectly fetched or it can turn in the wrong direction, making placement tricky. Nozzles for the 0201 and 01005 have gaps of 80µm. And, as luck would have it, some of these components would need reworking. "You can just about work with the 0201s, but it's not easy – it's a



Passive components are getting smaller and smaller, also difficult to rework

significant problem," said Grundy.

Grundy's suggestion is to consider embedded passives instead. "Now more than ever, it's important to consider embedded [components], especially with applications like ZigBee, Bluetooth and others around. Designers should strongly consider using this route – it's a much better way than [using] standard components."

The CEO of Quantum Research Group, Hal Philipp, has been granted both US and European patents for a technology that eliminates ambiguity between adjacent keys in touch keypads. The technique, known as Adjacent Key Suppression (AKS), uses an iterative technique that repeatedly measures a detected signal strength associated with each key, compares all the measured signal strengths to find a maximum signal change, then determines from which user-selected key that signal change comes from. AKS then suppresses or ignores signals from all other keys as long as the signal from the selected key remains above a nominal threshold value.

Ω

Imagination Technologies of Bristol, the UK, has launched a programmable shader graphics family for wireless applications, dubbed PowerVR SGX. It is claimed to be a highly efficient tile-based architecture, which fits into small silicon areas and delivers higher performance and higher image quality but at lower power consumption than competing technologies. PowerVR SGX uses a unified scalable shader engine, which combines vertex shader and pixel shader features in a single scalable processing unit. The shader technology enables realism and advanced features when rendering 3D objects. It also makes 3D effects more programmable.

Ω

Scientists at the University of Southampton have set up a network to develop a better understanding of how human memory works and how it might be augmented by technological developments. The network is supported by the Engineering & Physical Sciences Research Council (EPSRC) Memories for Life project and includes around 30 UK academics from the fields of psychology, neuroscience, computer science, information science and sociology, who will come together over a two-year period, in the hope that cross-fertilisation of ideas across the disciplines can lead to a more effective use of human and computerised memory.

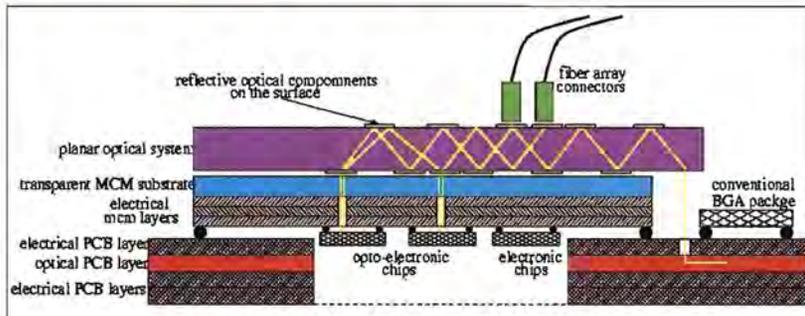
Faster computers project will show demo at ECOC

A joint industry and university project that uses optoelectronics to improve the speed of desktop computers looks set to show its first working prototype at ECOC, the largest fibre-optic communications event in Europe, taking place in Glasgow this year, between

September 25-29.

The Holms (High-speed Opto-electronic Memory System) project was created to deal with a latency problem in high-speed computers, caused by processors running at gigahertz speeds having to go off chip to access memory at such a slow rate that the processors spend a lot of the time doing nothing.

Heriot-Watt University, Siemens and ETHZ run the



Architecture of the system being built by the Holms project

project jointly, with help from Hagen University, ILFA, Thales and Supelec.

The research has led the scientists to use different types of optical communications. For distances up to 2m, traditional optical fibre is used. Under 1m, the system uses free-space integrated optics, perhaps the most exciting part of the project.

This is basically a slab of glass with tens of thousands

of optical channels that can be manipulated in free space.

It is similar to a multilayer PCB in that channels can pass along the surface or through the glass creating a three-dimensional mesh.

The final section connects the fibre with the electronics. From optical to silicon, standard modulator and detector array technology is used. From silicon to optical, vertical cavity surface emitting lasers are

used.

Each part of this system has been demonstrated separately and Siemens hopes to have the optical PCB at the centre of the system commercially available, perhaps by late next year. "We are working in stages," said John Snowdon, a senior lecturer at Heriot-Watt

University. "By [the time] ECOC [starts], we hope to have all the bits together and be able to show the whole thing working."

He said that freedom the optical PCB gave was the most exciting part of the project.

"The low latency is very sexy," he said, "but the free-space optical section could enable a whole new way to look at computer architecture."

Scattering improves analyser accuracy

The Brillouin scattering effect, named after the scientist Leon Brillouin, is helping improve the accuracy of optical spectrum analysers.

Usually a signal analyser is limited to seeing a peak in the signal under test between 50 and 100pm, but to go deeper into the signal and see the different spectral components would need a narrower filter. The light that is backscattered

in the waveguide – known as the Brillouin effect – could help generate such a filter. "You can generate a filter in the waveguide with a resolution of 0.08pm," said Juan Luis Vadillo, marketing manager at Aragon Photonics. "This filter can be used to split the signal under test into slices 10MHz wide."

Aragon will be showing an analyser using this technology at ECOC.

Plastic fibre breaks novelty image

Technology once only thought suitable for Christmas trees and other novelty applications is set to make a breakthrough in the video surveillance market.

Plastic optical fibres were once considered only useful for toys and gimmicks because of the high attenuation of plastic. But four years ago, the first breakthrough was made when Daimler-Chrysler started to use the technology for data communications in its cars.

Now Luceat is taking this a stage further with a system that will let video images

from any camera and to any monitor be transmitted clearly for up to 250m and, potentially, up to 400m.

"Scientists never took it seriously because it would only work for short distances," said Alessandro Nocivelli, Luceat CEO.

"But in surveillance, the maximum distance is often less than 200m. We use simple LEDs rather than lasers. The system cost is less than one fourth the equivalent over glass fibre."

The system is in prototype now and will be launched in time for ECOC.



Conference: 25th – 29th September 2005
 Exhibition: 26th – 28th September 2005
 Scottish Exhibition Conference Centre,
 Glasgow, Scotland
www.ecoc-exhibition.com



Colin Hunter looks at the history and future of powerful supercomputers

Supercomputing is fast becoming a household term in many industries, where the need for high-performance computing (HPC) – or supercomputing – has skyrocketed in the last decade. This is due to a revolution in both, architectures and usage models, that is culminating in the emergence of an amazing new machine – the cluster workstation, also known as the personal supercomputer.

Personal supercomputers represent an evolution that begun decades ago in the direction of both the powerful and the personal. The move toward widespread supercomputing is partly due to the massive amount of data being continually collected and analysed and partly due to better characterisations of the challenges industries face. More importantly, advances in basic computer technology have brought tremendous computing performance within the financial reach of industries that previously would not have considered the benefits of massive number-crunching capability.

Of the top 500 supercomputers in the world today, more than half are now dedicated to industry, including the sciences, finance, web service, aerospace modelling and even entertainment and animation. Just a decade ago, the vast majority of HPC technology was dedicated to research and academic pursuits.

Clusters are groups of individual computers networked together in such a way that they behave as one large computer for certain tasks. Cluster workstations, and clusters in general, are based on open standards and commodity hardware.

Clusters based on x86 (PC) technology are fast becoming the de facto standard for high-performance computing.

By their flexible nature, clusters can take advantage of all new technologies and continue to re-invent themselves. Open-source software is also the rule, particularly the Linux operating system. This lowers entry, maintenance and customisation costs dramatically and represents a strong departure from traditional supercomputing technology.

“By their flexible nature, clusters can take advantage of all new technologies and continue to re-invent themselves”

Traditional supercomputers required a separate dedicated room with special wiring and air conditioning and, often, a fleet of maintenance personnel. These systems had to operate on a “time-share” usage model. Those who needed computing cycles had to wait in line – or compete with others – to get access. Time-share systems enable organisations to centralise resources, but they naturally create conflict among groups who need access at the same time. Current mid-range clusters (between 10 and 100 nodes) also operate on the time-share usage model.

In the early 1980s, individual high-performance machines began to proliferate. These machines were called ‘workstations’. By themselves they were not as powerful as the hulking minicomputer down the hall, but they could be operated and maintained by one person. If the computer crashed, it took only one

person’s work with it. Workstations rapidly became a standard by virtue of their vastly improved usage model.

This same evolution is taking place in the HPC community, with computing resources tailored for the individual scientist or developer rather than a group – a personal approach to supercomputing. For example, the Orion cluster workstation leverages low-power commodity x86 components to create a twelve-node cluster on a single board. This provides a very low-power, homogeneous alternative to “back-room” clusters, which are often made up of very different machines, individually powered. The ‘deskside’ workstation combines eight Orion boards to provide a 96-node cluster in a single case. The DS-96 fits unobtrusively under a desk, powered by a single plug in a standard wall socket with no special cooling considerations and it draws less power than a hairdryer.

With this knowledge of the limitations of individual processors, computer science has embraced multiprocessing technology – solving the problem with more hands instead of bigger ones – and promises to do so well into the future as hardware costs fall. Industry and research continue to present challenges that can be met by high-performance computing. The emergence of clusters and open-source software, combined with the demand for ease-of-use embodied in the workstation usage model, clearly puts personal supercomputing on the crest of the technology wave.

Colin Hunter is the founder, president and CEO of Orion Multisystems, based in the US.

CAUTION:

lead-free reflow may cause damage

Warping, delamination and flaking are just some of the potential damages that could happen to your FR4 laminate during lead-free reflow

By Keith Gurnett and Tom Adams

At the turn of the century, when serious planning for Pb-free solders was just getting underway at thousands of companies, engineers were looking at a menu of dozens of possible alloys to replace conventional tin-lead (SnPb) solder. Most of the potential replacement alloys required reflow temperatures higher than the reflow temperature of SnPb. As costs, legislation and market forces drove the replacement process, the long menu of alloys was narrowed down to a handful that perform well in most applications.

It was also thought at the time that the equally conventional FR4 boards might be largely replaced by boards made from more expensive materials, such as polyimide, that would be less likely to suffer damage at the higher reflow temperatures. But as the technology of Pb-free processing has evolved, the vast majority of applications have retained FR4 as the laminate material, in part because of FR4's much lower cost, in part because engineers have had long and detailed experience with FR4, and in part because FR4 can generally pass through the higher-temperature Pb-free reflow without significant damage.

In some applications, however, FR4 does sustain damage. The type and extent of damage is not easily predicted from temperature data, and engineers looking for thermal damage are far more likely to be testing components and solder joints rather than the board itself. Overall, not enough is known about how FR4 behaves in the Pb-free environment.

Gail Tennant, team leader in Regional Supplier Engineering at contractor electronics manufacturer Celestica in Canada represents her firm in an industry consortium seeking to learn more. "One of the key things that we've seen in the industry is that there's not really any specifications on what lead-free means," she says. "Some suppliers think it means 245 degree temperature, but some are testing to 260 degree temperature."

One of the goals of the consortium, she adds, will be the definition of tests that laminates need to pass for Pb-free usage. Tests will enable users to compare one laminate to another for use in the small process windows that Pb-free reflow dictates.

The types of damage that can take place in an FR4 board as a result of thermal excursion are several. For some types of damage, the damage mechanism and the long-term impact of the damage on product reliability are fairly well understood; for

other damage types, much less is known. Six types of damage are discussed here.

▲ Damage to coatings on the top surface of the board. Several coatings are used on FR4 boards – matte tin, bright tin, tin over nickel, gold over nickel, palladium, palladium over nickel, silver and various Organic Solderability Preservatives (OSPs). Hot Air Solder Leveling (HASL) is another frequently used finish. These coatings perform multiple functions: they serve as a barrier to migration, prevent oxidation of the copper, protect the board from mechanical damage during handling and identify points that will be soldered.

These coatings may respond to the high Pb-free reflow temperatures by breaking, lifting or dimpling. These changes, in turn, may permit moisture to enter the board and may accelerate further peeling. These types of damage are visible in open areas of the board, but may escape detection if they occur underneath mounted components. HASL will reflow for a second time during the assembly reflow phase and has

the potential to break the final top coating on the board.

Although these coatings have lengthy histories in SnPb applications, they are now being studied anew to characterise their behaviour in higher-temperature Pb-free environments.

▲ Delamination within the board structure. Delaminations or separations between the horizontal layers of the board are a fairly common response to exposure to higher temperatures. They are more likely to occur if contaminants were present during the manufacture of the board, or if the board has taken up moisture in sufficient quantities. Board delaminations can largely be avoided if the board is baked before assembly, but baking is too expensive and time-consuming for most applications.

One of the early indications that board delaminations were occurring during Pb-free reflow came from acoustic microscopy. Acoustic microscopes are often used to image the internal structure of mounted components, where heat-related delaminations on a somewhat smaller scale may occur. By targeting a slightly lower depth, engineers have been able to identify delaminations in the top layers of the board itself, since delaminations and other internal gaps – whether in a component or in a board –

“One of the key things that we've seen in the industry is that there's not really any specifications on what lead-free means”

Gail Tennant, team leader, Celestica

give high-amplitude acoustic reflections. Some board delaminations, of course, create a bubble that can be seen optically at the board surface, but acoustic inspection additionally finds delaminations hidden from optical inspection.

"We see board delaminations fairly frequently," notes Ray Thomas, director of Sonoscan Applications Laboratory in the US. "They are basically similar to defects that occur in the interposers of BGAs and CSPs. It appears that the higher reflow temperatures, along with the moisture level in the board, have a great deal to do with board delaminations. The acoustic image may also reveal the delamination of board coatings from the top of the board."

One of the reliability risks from board delaminations is that small or shallow delaminations may, at the time of manufacture, not yet have caused an electrical malfunction. Traces and vias within the board may still be intact. It is the nature of delaminations, though, to expand and contract with thermal cycling, and to grow larger over time, with the result that even a relatively innocuous board delamination can lead to an unanticipated electrical failure.

▲ Warpage of the board. Already a familiar phenomenon at conventional SnPb reflow temperatures, warpage is likely to be more pronounced at the higher Pb-free temperatures. The problem is most damaging in fine pitch technology, where the signal lines are carried out on thin traces and the power lines on much thicker traces. Fine-pitch boards are becoming more common and generally involve multi-layer circuits.

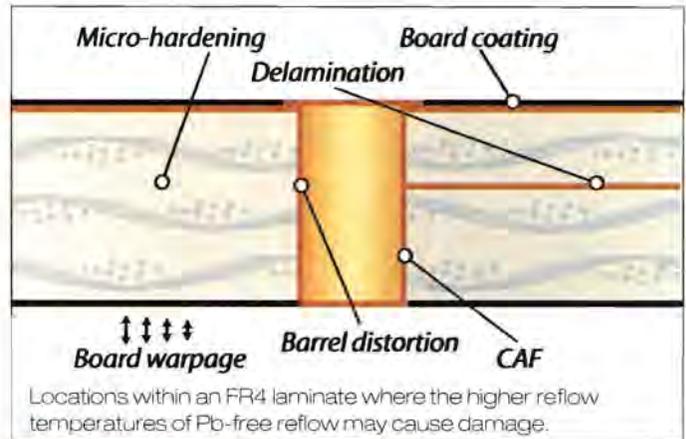
Board design can be used to limit warpage. For example, if two thick trace planes are both placed on the same side of the board, they can cause bowing and twisting of the board because of the uneven distribution of coefficient of thermal expansion; the two planes cause the board to act somewhat like a bimetallic strip. Placing one trace plane on each side of the board limits this effect. The use of thinner glass fibres in the glass-epoxy mix of the laminate itself can also help to control warpage, although the cost of the board may be somewhat greater.

▲ Growth of conductive anodic filaments (CAF).

The growth of these filaments, which (like tin whiskers at the component level) cause shorts, depends on two factors: the quality of the bond between the glass fibres and the epoxy in the board, and the presence of moisture.

In Pb-free reflow, the danger is that the higher temperatures may degrade the epoxy-glass bond, without necessarily causing other damage that is immediately apparent. In the presence of moisture, an electrolytic cell forms; the cell in turn promotes the growth of a copper filament along the interface between the epoxy and the fibres.

CAF is most frequently observed in dense, multi-layer boards, and typically occurs where copper barrel plating meets the glass reinforcement fibres of the glass-epoxy laminate. Like delaminations within the board, CAF is typically an insidious, slow-acting phenomenon that has the potential to cause sudden field failures. It can be accelerated, though, by impurities that may be present during board manufacture, by pH level and by the application of voltage in the operational mode. CAF may also be associated with an earlier delamination. "If you disturb the laminate with a delamination, over time, you will see it grow a CAF," notes Tennant.



▲ Damage to copper barrel plating. When the temperature of the laminate rises above the laminate's glass transition temperature (T_g), the coefficient of thermal expansion (CTE) of the laminate increases markedly. Fundamentally, CTE changes operate in all three dimensions, but because of constraints imposed by the woven, layered structure of the board, nearly all movement is in the vertical dimension.

A hole that is plated with either electro or electroless copper is thus subjected to vertical stress. The problem is compounded by the fact that holes are somewhat difficult to plate uniformly. The narrow diameter of the hole restricts current flow and chemical reactions during plating – meaning that it is difficult to achieve a consistent wall thickness along the entire length of the hole, and that the thinnest and weakest part of the copper plating is likely to be near the centre of the board.

If the vertical CTE stress during high-temperature Pb-free reflow is sufficiently great, a copper barrel may be stretched until it ruptures. If the rupture is permanent, the board will probably fail electrical tests and, therefore, be scrapped. When the board cools, however, the two barrel sections may re-establish electrical contact, so that no electrical fault can be identified by testing. In the field, the ruptured barrel may eventually manifest itself as an intermittent failure. Intermittent failures are notoriously difficult to diagnose and may even be labelled as software problems. The actual failure cause – the ruptured barrel – is likely to be identified only if temperature testing is carried out, something that is not often done on boards.

Very small diameter holes in boards using high density interconnects are sometimes formed by mechanical drills. These drills may leave ridges; the ridges, in turn, accentuate the unevenness of the plating and make rupture even more likely. Laser drills avoid this problem because they leave no ridges.

▲ Micro-hardening of the laminate. This phenomenon has been identified, but its impact on reliability is not yet well understood. At Celestica, Gail Tennant is researching the problem. "When the FR4 laminate is heated above its T_g , as may happen during Pb-free reflow, the laminate is temporarily softened," she observes. "When it is cooled below its T_g , small areas may have become brittle." The consortium of which Celestica is a part is investigating the risks that micro-hardening may pose for handling and performance.

ZigBee is emerging as a very suitable standard for wireless digital data interchange between embedded computing devices. Dr Faiz Rahman analyses the technology

Wireless communications are fast displacing wired connections in all kinds of information exchange appliances. Now, it appears as if it is the turn of embedded computer systems to go wireless.

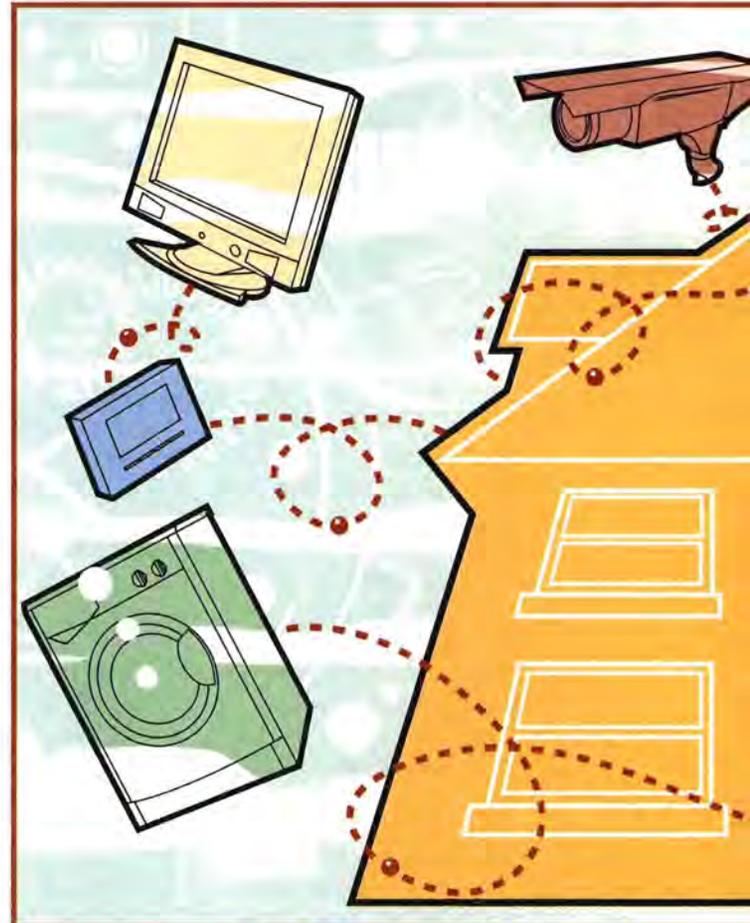
Traditionally, computers have exchanged data with each other and other digital equipment over legacy interfaces such as the IEEE 488 parallel port, RS232C and other serial ports as well as the widely deployed Ethernet connections. Recently, other higher speed communication channels have emerged to satisfy demands for higher bandwidth data transfers. These standards, like the Universal Serial Bus (USB) and the IEEE 1394, popularly called FireWire or i-Link (by Sony), are external serial buses, which are capable of several tens of megabits per second data transfer speeds. All of these interfaces require cables for connecting equipment together. For those occasions where external wiring would be impractical or inconvenient, there are now established radio frequency (RF) interconnection standards like Bluetooth and Wi-Fi (Wireless Fidelity), as well as emerging RF standards like Z-Wave, WiMax (Worldwide Interoperability for Microwave Access) and Wireless USB.

These standards are still maturing and increasing their penetration in the consumer electronics domain. However, localised computer systems are also found in all kinds of other applications that have little or nothing to do with conventional computers. Such systems with embedded processors range from washing machines and microwaves to cars and industrial tools. Often, such equipment has its own communication needs.

Whereas one day, conceivably, our microwaves and washing machines might need the ability to communicate with other electronic systems, for instance in the context of a smart home, some of the other systems with embedded processors have existing requirements for external communications. In fact, devices like medical electronics, surveillance systems and industrial shop floor tools, all require the ability to communicate either with their peers or with larger computer systems. So far, such systems have relied on wired interfaces, running standard protocols for communication with other systems. Wiring, however, accounts for more than three-quarters of the cost of distributed sensor networks and thus a wireless system would bring great financial benefits.

Microprocessor and microcontroller based systems have utilised a variety of schemes like the Serial Peripheral Interface (SPI), Serial Communications Interface (SCI), Inter Integrated Circuit (I2C), CANBus (Controller Area Network Bus) and others for digital information exchange. But, just like in the personal computer arena, things are changing in the embedded world as well. There is a growing realisation that in many circumstances such systems can benefit greatly from an ability to communi-

The Buzz



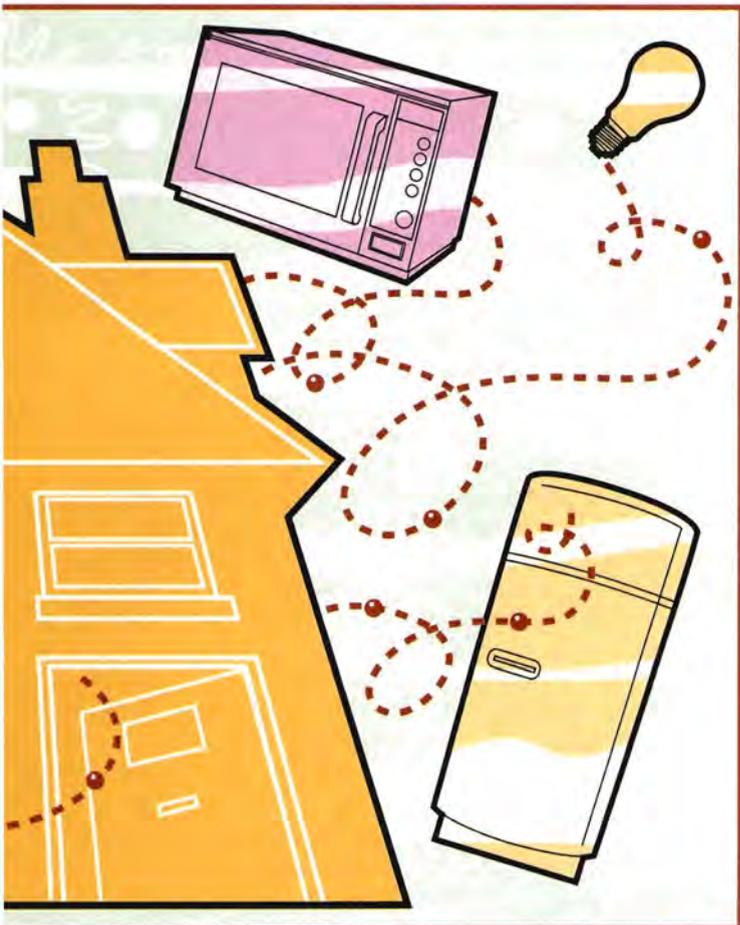
cate data wirelessly. Such a development would, for instance, obviate much of the wiring between industrial process monitoring systems and their control computers.

Given the recognition of this need, several companies began to develop their own proprietary RF communication systems, designed for embedded control applications. This led to a number of competing protocols that were quite incompatible with each other. In order to address the issue of platform independent communications, an industrial alliance was formed a few years ago to develop an industry-wide standard that could serve the entire market for wireless digital data interchange between a variety of embedded computer systems.

This alliance, called ZigBee after the zig and zag motion exhibited by honeybees during out-of-the-hive communications, was initially founded by Honeywell, Invensys, Mitsubishi Electric, Motorola, Philips and Samsung in San Ramon, California, but has since been joined by more than a hundred and fifty other companies. Participants now include semiconductor companies, wireless IP providers, hardware manufacturers and Original Equipment Manufacturers (OEMs).

It is understood that the best approach is to develop an industry-wide open communications standard that makes true

of ZigBee

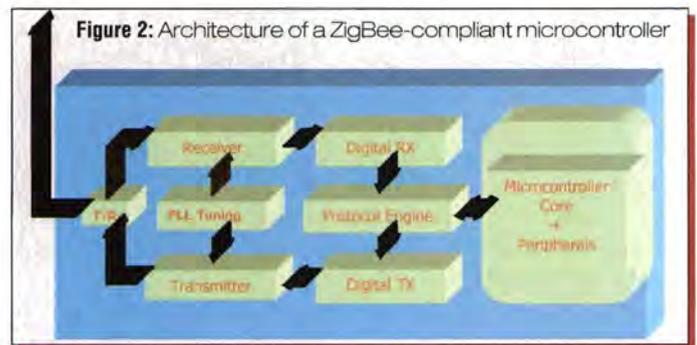
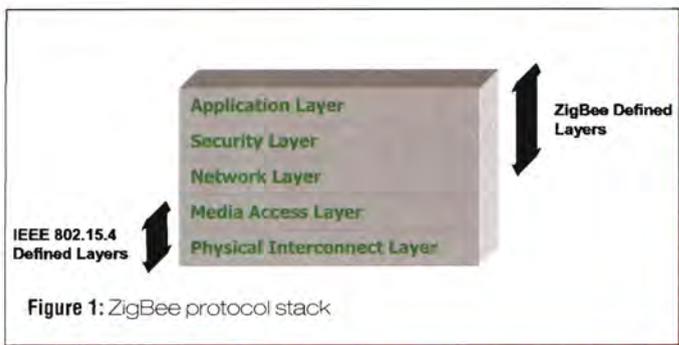


worldwide product interoperability possible. The goal of the alliance has been the incorporation of embedded RF functionality in a very wide range of communication-dependent products.

The ZigBee alliance has developed a standard communication protocol that could be used for interprocessor RF communications. This standard is based on the recently approved Institute of Electrical and Electronic Engineers (IEEE) wireless standard called 802.15.4 and also incorporates features of a defunct RF communication standard called HomeRF Lite. In terms of the Open System Interconnection (OSI) reference model, the original IEEE standard defined the lower level physical radio while the ZigBee modifications define the upper level logical and application layers, as shown in **Figure 1**. This protocol is meant for relatively low data-rate communication over a limited area but it could connect a very large number of nodes together. The technologies and architectures employed are geared towards very low power consumption implementations so that even low-cost, non-rechargeable battery powered nodes could be accommodated. In fact, battery life in many ZigBee connected systems could approach the shelf life of the batteries used.

Designed to support a group

The ZigBee wireless network has been designed to support as many as 254 distinct nodes, forming a relatively fine-grained wireless web. Each network, in addition, will have a master or, in ZigBee terms, Full Function Device (FFD) with the authority to control network traffic and negotiate network-to-network data exchanges. The master will feature a complete set of communication overseeing capability, implemented as a complete ZigBee protocol stack. The slave nodes, also called Reduced Function Devices (RFDs), could be designed with limited ZigBee functionality and thus feature a limited stack but with the ability to execute peer-to-peer communications. This way, there could be numerous, self-contained, extremely



low-powered and low-cost slave nodes that could be deployed, for example, to form a distributed sensor network over a limited geographical area. An FFD will require about 32kB of memory to accommodate the ZigBee protocol stack, while an RFD will need around 4kB. In actual implementation, conventional microcontrollers will be modified by the addition of a separate ZigBee peripheral comprising of a communication engine and an RF front-end to create a ZigBee-enabled microcontroller, as seen in **Figure 2**. Companies like Atmel have already come out with such microcontrollers. Atmel calls its chip Z-link, which is basically a modified microcontroller from the company's line of 8-bit AVR RISC processors. This device, part-numbered AT86ZL3201, is a combination of a RISC microcontroller core and a multi-band radio with a complete ZigBee stack, up to the security layer, as shown in **Figure 1**.

Other companies are developing stand-alone ZigBee radio chips that could be used with existing microcontrollers to provide them with RF networking capabilities. All of these ICs are based on the popular and cost-effective Complementary Metal Oxide Semiconductor (CMOS) technology. An example is Chipcon's CC2420 ZigBee-compliant RF transceiver IC, fabricated with a 0.18µm CMOS process. Low power operation, however, does mean that the range of operation of one ZigBee network is limited to less than 100 meters. The exact operating distance in any particular installation will depend on transmission power and environmental characteristics, and thus, does not form part of the ZigBee specifications. Multiple ZigBee networks could be interconnected, spanning longer distances and supporting more than 65,000 nodes in star, cluster or mesh networks. The mesh networking capabilities of ZigBee will probably enable new applications, like ambient temperature control systems. Furthermore, by interconnecting networks over the Internet, locally wireless but globally distributed systems could be realised. The standard supports three data rates: 20kbps, 40kbps and 250kbps.

At this time, ZigBee is defined for tri-band operation. The unlicensed 868MHz and 915MHz bands are targeted for use in Europe and North America respectively, while the higher frequency 2.4GHz band will be used worldwide for higher data-rate operations.

All transmissions are based on a digital scheme called Direct Sequence Spread Spectrum (DSSP). The low bands are specified to use Binary Phase Shift Keying (BPSK) modulation, while the high band is specified to use Offset Quadrature Phase Shift Keying (O-QPSK). Use of DSSP scheme ensures that ZigBee is relatively immune from external RF interference. This is a key requirement for the acceptance of any wireless network in noisy industrial environments.

Furthermore, spread spectrum technology also provides data security by making it harder for intruders to

access information covertly. The specified modulation schemes are proven techniques for the efficient generation of transmit signals and provide a low energy route to convert information from the raw digital format (baseband) to the RF domain. This makes ZigBee one of the most energy efficient communication technologies in the marketplace today.

Key hallmark points

Low power consumption and high data-security are two key selling points for this standard. ZigBee enabled devices could sleep for times ranging from seconds to hours and, therefore, can have very small communication duty cycles. This results in very small average power consumption, which is a hallmark of this technology.

Being thrifty with power, repositionable ZigBee wireless switches are expected to replace fixed electrical switches in homes in a few years' time. After the initial network forming activity, where devices identify themselves as communication nodes, ZigBee microcontrollers in slave roles could lie dormant until either they have data to communicate or are actively queried by the system master. A typical timeline of activities is shown in **Figure 3**. As seen here, a slave device can wake up and be active in just 60ms. The first time slot is taken up in registering and configuring a slave device. Next, the slaves are brought out of their sleep state and, finally, a data exchange takes place.

Like all other modern digital communication systems, ZigBee also works by exchanging data packets called frames. The four basic frame types are: Data, Acknowledgement, Command and Beacon. These, respectively, carry actual data, data reception acknowledgement, commands to media access controller and calls to wake up sleeping nodes. The data frame can have

a variable number of bytes up to a maximum of 104. Apart from the raw

data (called the payload), the

data frame also carries frame control information, a

sequence number to

enable data tracking,

recipient device

address and a

frame-check

sequence to ensure packet integrity.

The acknowledgement

frame is a

short data packet that is sent immediately

after data

reception as a receipt of data frame. The

command frame is used

to control and synchronise

slave nodes and to configure

their operation as part of the whole



Figure 4: ZigBee chipset from Freescale Semiconductor

network. The task of periodically waking up sleeping nodes in order to query them goes to the beacon frame. These carry address information and only the device with the matching address is brought to full wake-up state; all other devices go back to sleep after receiving the beacon frame.

Being a packetised digital data communication technology, ZigBee benefits from previous developments in the field of data security. The network is self-forming and immune to failures of a few slave nodes as data can get to its destination over multiple paths. The standard itself is based on an Ethernet-like Carrier Sense Multiple Access with Collision Avoidance (CSMA-CA) front-end protocol that ensures data integrity over a distributed network. Other provisions for security include support for 128-bit encryption and options for guaranteed communication time slot for devices that must get access to a network quickly, for example alarm systems and medical monitoring devices.

The ZigBee standard

The ZigBee standard was ratified in December 2004 and the alliance, now comprising members in more than two dozen countries, is stronger than ever. These companies, that range from chip manufacturers to software developers and

communication system providers, periodically carry out interoperability testing to ensure that the protocol specifications are being uniformly implemented by all potential vendors. This is in preparation for a large scale launch of compatible products.

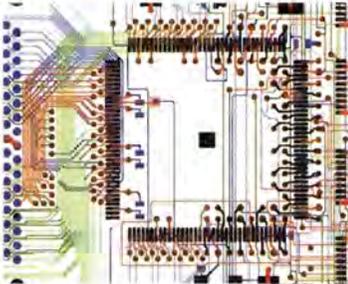
ZigBee enabled devices and systems have been making their initial commercial appearance throughout 2005. The initial target markets are in building automation through Home Area Networking (HAN) but later product offerings will also include networked shop-floor automation systems. In a major development, US chip maker Freescale Semiconductor recently released a ZigBee chipset and a development system that could be used to create prototype applications (Figure 4).

Such design kits enable system developers to concentrate on the end applications rather than struggle with the implementation of the embedded radio system. Other companies are also busy introducing their own development kits and reference designs. All the signs are there that ZigBee is slowly but surely permeating the world of embedded wireless applications. Gradually, this standard is expected to become as ubiquitous as the more well-known data interchange standards that are in use today.

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Designing wireless chips

Designing a modern radio frequency (RF) ASIC is one of the most audacious challenges in electronics design, as Jürgen Hartung from Cadence Design describes

RF IC designers face several significant challenges. Large RF ICs, such as wireless transceivers, comprise a full range of on-chip functionalities that, in particular, stress functional verification solutions.

In addition, high-speed requirements make RF circuits extremely sensitive to the effects of parasitics, including parasitic inductance, passive component modelling, as well as signal integrity issues.

Thus, the essence of the RF IC flow is the ability to manage, replicate and control post-layout simulations and effects, and to effectively use this information in a timely fashion at appropriate points through the design process.

RF IC design also requires specialised and unique analysis techniques specific to RF design. These vary between frequency domain and time domain analysis methods, chosen on the basis of circuit type, designer comfort level, circuit size and design preference. Ultimately, this requires a seamless environment that facilitates choice in simulation method.

Integration trends have also affected the RF IC world, which used to be viewed as a separate, almost standalone entity.

Today, many RF ICs contain at least the analogue-to-digital converter (ADC), digital-to-analogue converter (DAC) and phase-lock loop (PLL) functions, as well as a digital synthesiser, which is created through the digital environment and integrated on-chip. In some cases, RF content is being added to large systems-on-chip (SoC), as design groups attempt a single-chip solution.

Other design teams are integrating RF content by using system-in-package (SiP) techniques, which leads to similar verification issues as RF IC and SoC methodologies. These advanced issues demand an RF IC solution that must:

- > Optimise simulation time
- > Facilitate verification
- > Enable detailed analysis at the block and chip levels
- > Manage and facilitate simulation with full parasitics
- > Enable analysis (noise, IR, EM) early and often in the flow
- > Include layout automation that can be used at appropriate points in the design
- > Enable several levels of passive modelling throughout the design process

All of these requirements must be met through a single environment that not only facilitates the job of the RF IC designer, but also integrates with the

other domains such as analogue/mixed-signal (AMS) and digital design. This environment must include both front-end and back-end perspectives at multiple abstraction levels, so that design collateral can be passed back and forth, facilitating verification/implementation from either point of view, independent of physical integration strategies.

The first place to start describing an RF IC flow is from a more global methodology perspective and context. The ACD methodology is shown in **Figure 1**. This describes a process geared towards mixed-signal design, which takes design tasks and parallelises them, allowing for a top-level perspective, for parasitic and analysis functions performed early and often, and which, ultimately, enables the design to progress with as much information as is available at any given point in time.

Predictability is the driving force behind the ACD methodology. The need for predictability is driven by two primary concerns: schedule, which must be met from the beginning of the design process, and performance requirements, which must be met to achieve first-pass success and which require silicon accurate methodology.

Schedule requirements: top-down

To meet schedule requirements, RF designers need a fast design process that supports thorough simulation and physical design. The top-down design process, when applied to both simulation and physical design, is the approach that facilitates a fast design process. The design process is comprised of many tasks and many of today's chips contain multiple blocks from multiple design domains. Thus, it is imperative to design in as many of these blocks and perform as many tasks as possible in parallel, using as much of the top-level IP as possible throughout the process. This leads to the concept of design evolution, where all a design's IP is utilised as it matures through the design process.

Using this concept, multiple abstraction levels – from high-level design through detailed transistor-level design – are combined to support a mixed-level approach that targets detailed design to only the point(s) needed for a given test. This also enables designers to use top-level information for block design and to subsequently re-verify the blocks in the top-level context.

Performance requirements: bottom-up

To achieve the required design performance, RF designers need a design process that is silicon accurate. Silicon accuracy relies on base design data, such as device models that support accurate simulation and technology files that support physical verification and analysis.

Test chips, which are often comprised of critical structures that are known from past designs to be highly sensitive, are also used in this process to verify the feasibility of a process and the accuracy of its corresponding Process Design Kit (PDK).

Often, a design group will need to add components to the PDK to support a particular design style. Device models may need to be expanded to combine or add corners, or to facilitate statistical modelling or other approaches the design team requires.

This silicon-accurate data is driven through the design process through detailed transistor-level analysis, including layout extraction. The calibration of these lower-level silicon-accurate results to higher levels of abstraction ensures that designs will meet performance requirements. This comprises the bottom-up portion of the ACD methodology.

Meeting in the middle

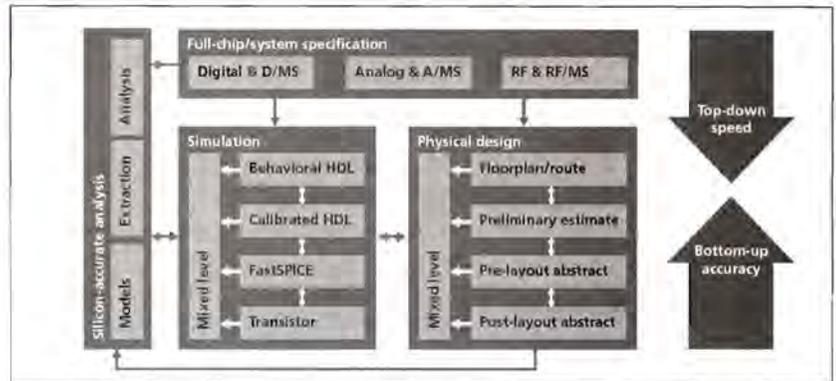
In practice, the top-down and bottom-up processes work in parallel, producing a 'meet-in-the-middle' approach. This approach balances the need for a fast design process with silicon accuracy, which ultimately produces a predictable schedule and leads to first-pass silicon success.

The ACD methodology can be applied to a complex integration or to a particular domain area. The methodology for each domain applies the meet-in-the-middle approach, combining top-down speed with bottom-up silicon accuracy.

Figure 2 shows the Virtuoso RF IC flow. The top-down process starts with HDL modelling for the entire RF IC. This includes all RF blocks, along with any analogue content and/or digital blocks. The first step is to model behaviorally the full chip within a top-level testbench, which would verify some system tests such as error vector magnitude (EVM) or bit error rate (BER).

This step initially verifies the partitioning, block functionality and the ideal performance characteristics of the IC. This behavioral setup then serves as the basis to facilitate mixed-level simulations, where blocks can be inserted at the transistor level and verified in a top-level context.

This full-chip setup can serve as the regression template to enable continuous verification as blocks mature, creating a continuous evolution approach through the entire design process. This is very important, because any problems can be detected at the earliest stage possible, when time still remains to fix



the problem, and because blocks can be designed in parallel according to individual schedules.

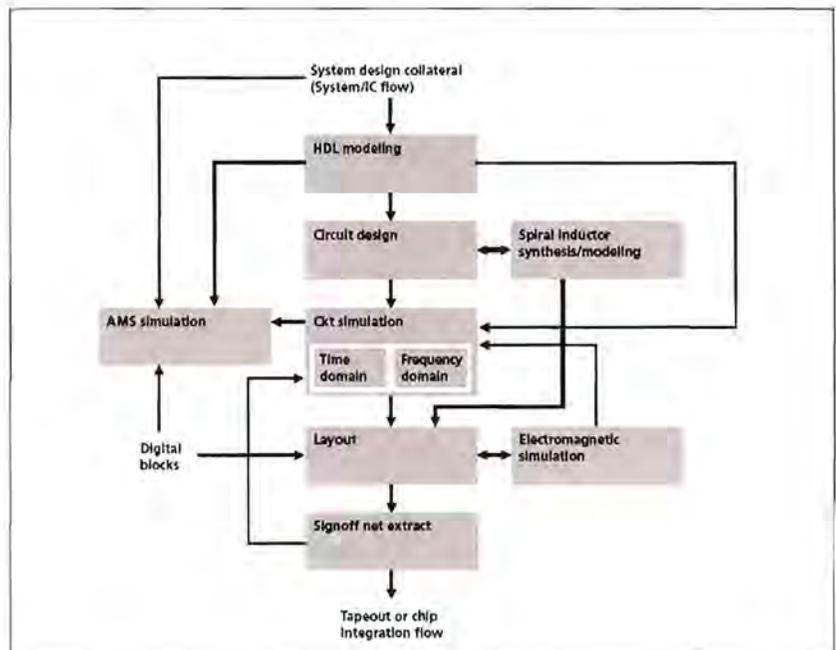
Next in the flow: a preliminary circuit is designed, enabling early circuit exploration and a first-cut look at how the design meets performance specifications. This early exploration leads to a top-level floorplan, which for RF ICs is very sensitive to signal integrity concerns, and block-level interconnect design and parasitics. At this stage, it is possible to synthesise passive components such as spiral inductors to specification and to do an initial placement of these on the chip.

This enables two key activities: the creation of early models for spiral inductors that can be used in simulation before the block-level layouts are complete, and the initial analysis of mutual inductance between the spirals. Component models of each inductor can be generated within this context for use in the simulations.

Next, simulation is performed using the designer-preferred method, either by frequency or time domain. This choice depends on the circuit, type of

Figure 1. Block diagram of the ACD methodology

Figure 2. The Virtuoso integrated circuit (IC) design flow



simulation and amount of design data to be simulated, and is a judgment call by the designer. A single process design kit and associated environment enables a smooth determination and selection of the simulation algorithm desired.

Results are presented through a display, appropriate for the selected simulation type. As circuits are completed at block level, they are verified within the top-level context with behavioral stimulus and descriptions for the surrounding chip. Simulation setups are created and kept in a specification-driven environment, which enables effective management of numerous simulations and views of each block.

The full simulation environment will comprise several views of the same circuit. These are likely to include a behavioral view, a pre-layout transistor-level view, several views of parasitic information (one view may have resistance and capacitance (RC) only, one view resistance, inductance and capacitance (RLC), one view RLC plus substrate, etc.), and perhaps a back annotated behavioral view.

The specification-driven environment provides the means to manage all these simulations, pick the appropriate views of each block or sub-block and manage the runtime versus accuracy trade-offs for the simulations that are being performed. This provides an effective mechanism to set up the continuous regressions that support the ACD methodology.

Blocks maturity

As blocks mature, more transistor-level information may be required to test RF/analogue and RF/digital interfaces. These tests will require the use of a mixed-signal simulator capable of handling analogue, digital and RF descriptions, and a mix of behavioral-level and transistor-level abstractions.

Runtime versus accuracy trade-offs can be made through simulation options; the designer can send the transistors to a FastSpice simulator, or keep the transistors in a full Spice mode. This configuration is highly dependent on the circuit and sensitivity of the interfaces. The ability to manage these configurations effectively is important as they must be repeatable.

Layout automation (automated routing, connectivity-driven layout, design-rule-driven layout and placement) can be used judiciously. The advantages to using layout automation are that it is tied to the schematic and Design Rule Checking (DRC) rules and that it enables productivity gains. Analogue-capable routers can help with differential pairs, shielding wires and enable manual constraints per line.

This enables a physical design process that can become just as repeatable as the front-end process. The time and overhead, expended to set up the initial tools, are made up as iterations are created through the design process. Engineering Change Orders (ECOs) are performed more effectively if a

repeatable layout process is in place. The repeatability of an automated layout process is weighed against the requirements of highly sensitive circuitry, which demands a manual approach.

As layouts are completed, ElectroMagnetic (EM) simulation can be used to provide highly accurate models for passive components. For example, several spiral inductors may be selected as highly critical and a target for EM simulation. These EM simulation models can be swapped in to replace the models that were created early in the design process, and can be mixed and matched with the existing models.

This gives the designer full control over the spiral modelling process and, again, enables the ability to trade-off runtime versus accuracy. Net-based parasitic extraction becomes a key element of the process as layouts emerge.

Parasitic extraction

RF design is highly sensitive to parasitic effects. The ability to manage different levels of parasitic information is paramount, as the designer can describe the amount of parasitic information to include for each area, line, or block. Less sensitive interconnects may require RC only, where more sensitive lines may require RLC.

Lines with spirals attached can be extracted fully with RLC plus the associated inductor component, and substrate effects can be added for those lines that are the most sensitive. Again, those lines that contain a "full" extraction can be mixed and matched with the component models for passive components that were created earlier.

Managing drawn inductors through the parasitic extraction process is an important aspect of a complete design flow and warrants special consideration. In fact, one can consider inductor creation to follow the meet-in-the-middle methodology. Early in the design process, these inductors are drawn (or synthesised) using a top-down model. As the design progresses and layouts mature, the bottom-up process enables more refinement. At this bottom-up stage, full parasitic effects – including substrate – are included for the inductor as well as the surrounding circuitry, using the same parasitic methodology as the rest of the circuit. This enables more accurate representation of these critical components.

Circuit designers need the ability to choose the method most appropriate in the up-front process: a quick, quasi static equation-based solver, or a slower, more accurate 2.5-3D EM full-wave numerical solver. Both can complement the design process from inductor synthesis to final check. There should be reasonable agreement between the methods for well-characterised semiconductor processes in the lower frequency regimes.

The full-wave EM solutions are better for complex shapes and higher-frequency harmonics. But all circuits do not have these needs. The full parasitic check at the end serves as the signoff, net-based extraction, and models from these various solvers can coexist with the extracted data. Discrepancies may arise and understanding them is an important step, as a variety of situations depending on process information and setups could impact the models and simulation results. In this case, there is great value in having multiple simulation runs from different stages and using various techniques to ensure accuracy.

Finally, as blocks are completed, the initial behavioral models can be back annotated for key circuit performance parameters, which can provide a more accurate HDL simulation. While this back annotation will not account for every effect, it can add more realistic performance information at a very small runtime cost, enabling faster high-level verification and, perhaps, reducing the amount of full transistor-level verification required.

For further information access:

www.cadence.com/community/virtuoso/

Wireless design challenges

New wireless applications are shifting to human-machine, human-goods and goods-machine communications. A large number of new short-range wireless applications have to support interactions between machines, reading sensors or controlling actuators at remote nodes. Example for these emerging wireless devices include:

- Control of machines and devices in the process and automation industry;
- Logistic Radio Frequency Identification (RFID), which includes transportation, terminals and warehouses;
- Smart home appliances, remote controlled;
- Medical monitoring health conditions (Wireless Body Area Network or WBAN);
- Environmental monitoring, such as smart dust or other ambient intelligence;

Mobile phone designers continue to combine wireless communication technologies and devices in the same subscriber unit. These mobile phone engineers squeeze as many radios as they can into a handset.

For example, GSM/PCS/PCN/EDGE/GPRS already operates in multiple RF bands (800MHz, 900MHz, 1.8GHz and 1.9GHz). Most handsets also support global positioning satellite (GPS) for location-based services, newcomer digital radios and at least one variety of 802.11(WLAN) for tapping into Internet hot-spots. In addition, they also support Personal Area Networks (PAN) as Bluetooth, and often include infrared as well.

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A 2.5GHz radio demonstration circuit

J. S. Lee, R. Remba and M. J. Bailey from Filtronic Compound Semiconductors present a 2.5GHz WMAN radio demonstration circuit with a two-stage power amplifier chain, a broadband low-loss SPDT switch and an ultra-low-noise amplifier in the receive chain

Wireless Metropolitan Area Networks (WMAN) using the IEEE 802.16/ETSI HyperMAN standard will soon be positioned for commercial deployment to deliver broadband wireless access, spearheaded by the WiMAX Forum of telecommunications operators and equipment suppliers. Trial deployments are planned for later this year and industry analysts expect network deployments to accelerate in 2006.

The 802.16 standard is an adaptive protocol that covers applications in the 2-11GHz frequency range and is meant to complement the Personal Area Network (PAN) standards such as Bluetooth (802.15) and Local Area Network (LAN) standards such as Wi-Fi (802.11a/b/g). The 802.16 standard supports fixed, portable and 'nomadic' users and is envisaged to provide a number of services, such as backhaul connection for Wi-Fi hotspots, broadband connectivity for industrial and educational campuses and as an alternative to digital cable or DSL for the 'last mile' broadband service to businesses and residences. The standard offers non-line-of-sight service and can deliver up to 280Mbps service to base stations, using a spectrally efficient modulation (3.8bit/Hz). The air interface standard combines high-data-rate QAM (quadrature amplitude modula-

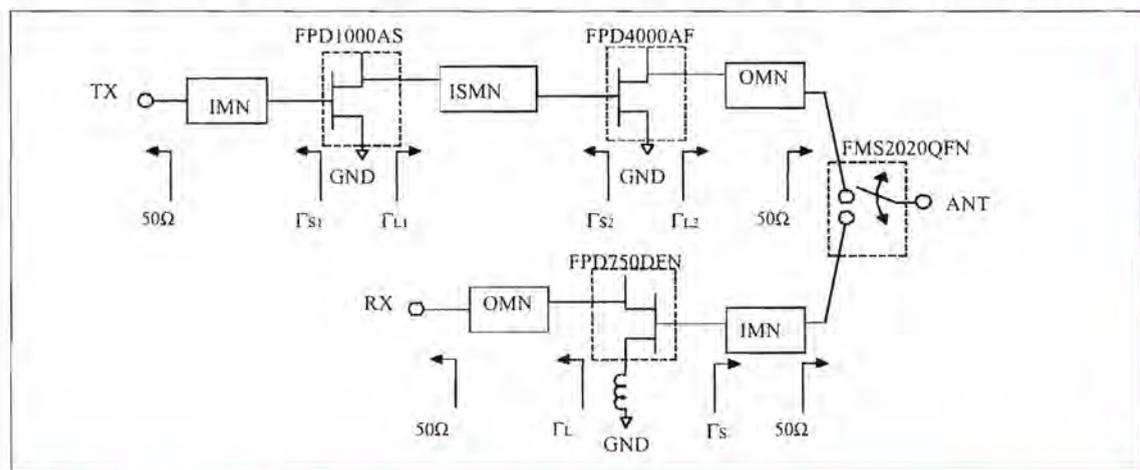
tion) with multi-tone OFDM (orthogonal frequency division multiplexing) and, consequently, the transmitter power amplifier must be very linear to avoid distortion due to the RF carrier's peak-to-average envelope variation. This presents new challenges to the radio design engineer.

The radio demonstration circuit

This 2.5GHz WMAN radio demonstration circuit is intended to allow potential users to explore various power-amplifier operating conditions, in order to optimise the unit for specific linearity and DC power requirements. Future versions of the basic circuit will include a number of sub-circuits to handle bias sequencing and switch control, as well as designs at higher power levels, to 20W.

The circuit was designed, fabricated and tested using Filtronic Compound Semiconductors pHEMT process technology. A two-stage linear power amplifier is combined with a single-stage low noise amplifier and a pHEMT-based broadband packaged SPDT switch to validate design procedures and demonstrate the basic performance specifications for a radio transmit/receive front-end. The power amplifier is designed to provide a linear 28.5dBm output power, with less than 2.5% EVM (error vector magnitude) when an 802.16 modulation is

Figure 1: Block diagram of the demonstration radio. IMN = input matching network, ISMN = interstage matching network, OMN = output matching network, and Γ_{SL} = source and load impedances as seen by the devices



applied. The receive path was designed to provide at least 13.5dBm of input intercept point (IIP3) performance, referenced to a standard two-tone measurement technique. A block diagram of the demonstration radio is shown in **Figure 1**.

Demonstration radio design

The Filtronic model FPD1000AS packaged pHEMT device was selected for the transmit (TX) path driver stage and the FPD4000AF as the output stage, with the radio designed to provide at least +28.5dBm linear power with less than 2.5% EVM, using standard 802.11/802.16 modulations. Experience has shown that amplifiers need to be operated 7-8dB below the "linear" power level, traditionally defined as the output power at 1dB gain compression (P_{1dB}). For amplifiers operated in Class A mode, the Output 3rd-order Intercept Point (OIP3) is classically 10.6dB above the P_{1dB} power level, although pHEMT devices can show non-classical linearity behavior. Since the intermodulation distortion performance for cascaded amplifiers follows the relationship:

$$(IP_T^n)^{\frac{(n-1)}{2}} = \sum_{i=1}^x (IP_i^n g_{(i+1,x)})^{\frac{(n-1)}{2}}$$

where: IP_T^n = cascaded intercept point, n^{th} -order (linear units)

n = distortion product order

IP_i^n = intercept point of the i^{th} stage (linear units)

$g_{(i+1,x)}$ = total gain following the i^{th} stage (linear units)

For a two-stage cascade, this relationship for 3rd-order intermodulation products becomes:

$$(IP_T^3)^{-1} = (IP_1^3 g_2)^{-1} + (IP_2^3)^{-1}$$

The typical IP3 performance for the driver (FPD1000AS) is 42dBm (15.8W), and for the output stage (FPD4000AF) it is 48dBm (63.1W). The gain achieved by the output stage is about 10.5dB (11.2). Thus, the cascaded IP3 is approximately 46.5dBm, a theoretical degradation of only 1.5dB. Actual results were 46-50dBm across the band. This is 12-14dB above the P_{1dB} power level, typical non-classical behavior for pHEMT devices in a 20% fractional bandwidth design.

A convenient engineering 'rule of thumb' for cascaded amplifier design is to ensure that a driver stage's output IP3 is at least 6dB greater than the input IP3 of the driven stage. If this guideline is observed, there will be less than 1dB of intercept point degradation of the output stage.

Another caution needs to be observed in cases where the output stage does not have particularly good gain performance: the driving stage must then be selected carefully so that it does not begin to

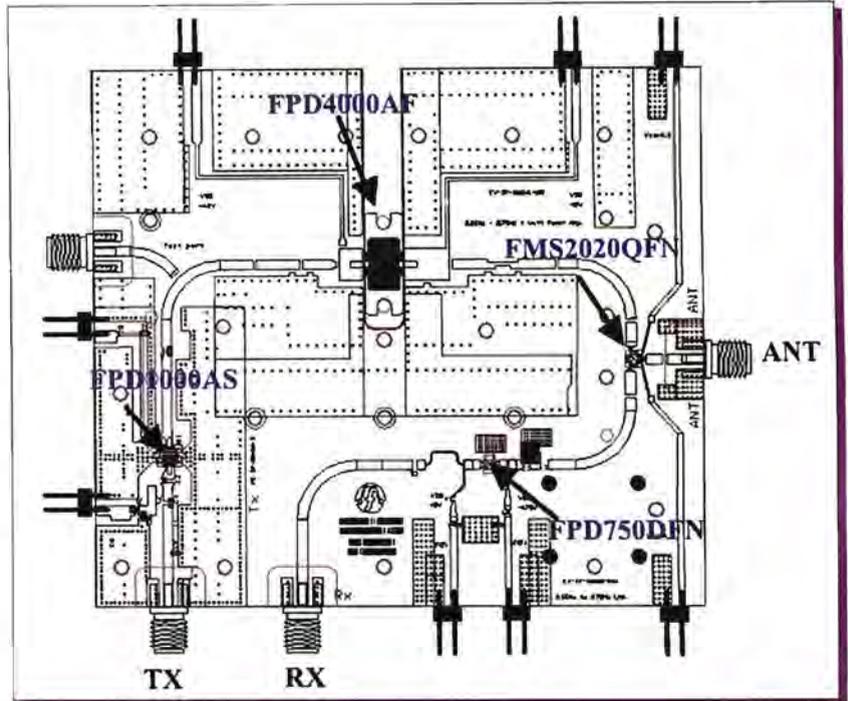


Figure 2: Board layout, overall dimensions are 10.2x8.6mm

compress before the driven stage, otherwise the cascaded pair will not attain its best P_{1dB} performance.

The receive path (RX) intermodulation performance is determined principally by the low-noise amplifier stage, since the switch's output IP3 power level exceeds 38dBm. A common difficulty with other device technologies is that the optimum DC bias current levels for good noise performance is too low to simultaneously provide for a reasonable IP3 level. This is not the case with pHEMT technology, which offers extremely low noise figure performance while maintaining very good IP3 levels, thereby extending the dynamic range of the receiver.

In this case, the noise figure of the FPD750DFN device is less than 0.8dB and the radio's input noise figure is as low as 1.2dB, which includes the loss of the TX/RX switch. The output IP3 of the low noise stage is 25dBm when biased at 3.3V/60mA and, thus, the input IP3 of the radio's RX path is at least 13.5dBm. Assuming a typical receiver noise floor of -174dBm/Hz (Nyquist noise), the receiver's operating bandwidth of 500MHz (87dB) and the noise figure achieved in the demonstration radio, the noise floor is $-174 + 87 + 1.2 = -86$ dBm. The dynamic range of the RX path is, therefore, nearly 100dB.

The radio circuit board layout is shown in **Figure 2**. All three stages use a common source amplifier configuration and are stabilised using a shunt gate bias resistor and bypass capacitors. This stabilisation technique improves the stability factor for frequencies below the passband. In the first TX path stage, the FPD1000AS pHEMT device's input is conjugately matched for maximum gain. An inter-stage matching network between the first and second TX

path stages provides the optimum Γ_{L1} (output match) for the output of the first stage. The output match presented to the first stage is designed to provide an optimum power match for that stage and the network also provides a conjugate match for the input of the second stage, the FPD4000AF pHEMT device. This interstage network is effectively composed of two sub-networks to simplify the design process. The second stage's output matching network transforms a standard 50Ω impedance into the optimum load for best power and intercept point performance. Both amplifier stages are operated in Class AB mode, with a quiescent operating current that is about 30% of the IDSS (maximum drain-source current). The TX path 2-stage amplifier can be operated from Class C (lowest current) to Class A (highest current, about 50% of IDSS), depending on the specific needs of the user. **Figure 3** presents the performance of the TX path.

Selected for LNA design

The FPD750DFN pHEMT device was chosen for LNA design. Source degeneration is used (by adding inductance) to simultaneously match the device for lowest noise figure and maximum associated gain. The inductance is realised by distributed element, a shorted length of microstrip line. The output matching network provides for optimum gain to again achieve the lowest possible noise figure performance. While the input noise figure is degraded by the passive loss of the switch, obtaining as much gain as possible from the low noise stage will minimise the effect of additional passive losses that occur after the active stage. **Figure 4** presents the performance of the RX path.

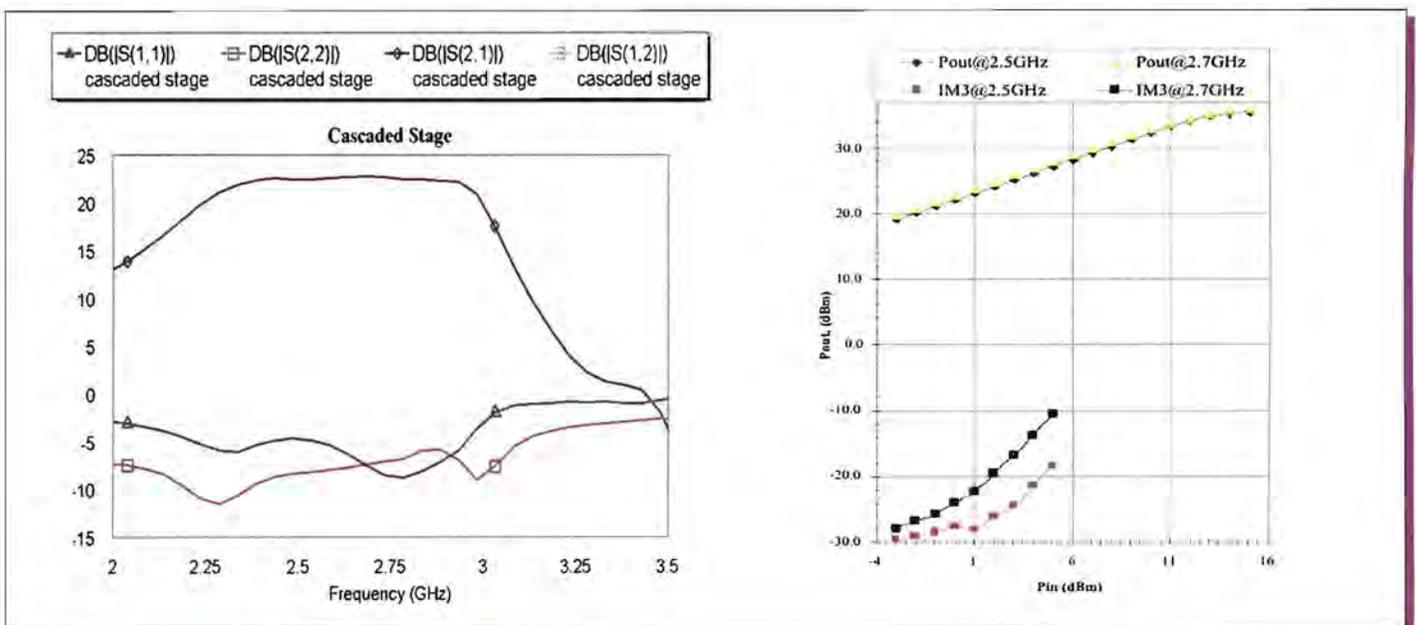
The circuit board is fabricated using 0.762mm thick substrate and mounted onto an aluminum heat

sink, shown in Figure 2. The substrate is Rogers 4003 material and the board includes both plated through-vias and filled plated through-vias for grounding. The circuit media is microstrip, but includes lumped elements as well; there is a test port between the first and second TX path stages. In the present version, each stage requires separate bias connections for both the gate and drain bias, since the depletion-mode pHEMT technology requires a negative gate-to-source voltage to establish the proper operating current level. The user must manually apply control voltages for the switch. Additional versions are currently being designed that include DC-to-DC voltage conversion (to eliminate the need for a negative voltage supply), bias sequencing (to ensure the devices are biased on/off properly) and simplified control circuitry for the switch. Although the depletion-mode pHEMT devices require a negative gate voltage (in this dual bias design), the combination of excellent gain, superior linearity and very low noise performance offers the designer the opportunity to achieve superior performance. **Table 1** provides a summary of the prime performance specifications and attributes of the demonstration radio circuit.

Device and Process Description

The three active devices used in this product are very similar and all use the same critical gate technology. The epitaxial layers for all three devices are grown on 150mm diameter substrates, based on a standard AlGaAs/InGaAs/AlGaAs pHEMT differing in Hall sheet charge and Schottky layer thickness. All are based on a dry etch stop technology to achieve highly repeatable threshold voltages. In summary, the parts are fabricated using the fol-

Figure 3: Performance of the transmit (TX) path. The left-hand plot shows small-signal gain and input, output return loss, as a function of frequency in GHz. The right-hand plot shows output power and 3rd-order intermodulation product levels as a function of input power.



lowing process steps. Device isolation is achieved by either ion implant isolation or standard wet mesa etch. Ohmic contacts are formed with a AuGeNiAu system, alloyed near 400°C. The N+ recess is a dry, selective etch process, which helps minimise parasitic resistances. The stepper-based optical gate process is a nitride-assisted T-gate structure utilising a dry (plasma assisted) recess etch. The RX path device, the FPD750QFN, utilises a 0.25µm gate length low-noise pHEMT structure (with $f_t \approx 50\text{GHz}$, a frequency performance of merit), and the TX path devices use a 0.5µm gate length power pHEMT structure ($f_t \approx 20\text{GHz}$).

All devices are based on a Ti/Pt/Au system (for gate and first metal layer) and an electroplated Au for the interconnection layers. Backside processing consists of highly uniform thinning ($\pm 5\mu\text{m}$ variation across the wafer) and either plated back with through vias (power FET), evaporated metal (low-noise FET), or no metal at all (switch). All devices are passivated with layers of PECVD silicon nitride. The switch devices are manufactured with essentially the same processing steps and consist of meander-gate pHEMT devices that are optimised for low loss, high isolation and linearity. The switch process is further optimised for lowest manufacturing costs.

Device uniformity for these process families is quite excellent. For example, a typical cross-wafer gain variation (5th to 95th percentile range) for a three stage 8-14GHz MMIC amplifier using the 0.25µm process is less than 1dB (28dB small-signal gain). This uniformity represents a substantial improvement for pHEMT manufacturing capability and allows design engineers to consider biasing alternatives that are significantly less expensive. Given the threshold voltage variation, complex

Table 1: Performance of the demonstration mode

Parameter	Results
Operating Bandwidth	2.3 – 2.8GHz
TX Small-Signal Gain	22 ± 0.5dB
TX Power at 1dB Gain Compression	35.5dBm
TX Output 3rd-order Intercept Point	38 ± 2dBm
RX Small-Signal Gain	11 ± 1.0dB
RX Input 3rd-Order Intercept Point	13.5dBm
RX Noise Figure	
2.3 – 2.5GHz	< 1.25dB
2.5 – 2.8GHz	< 1.75dB
TX-RX Isolation	25dB
DC Power < 8.5W	

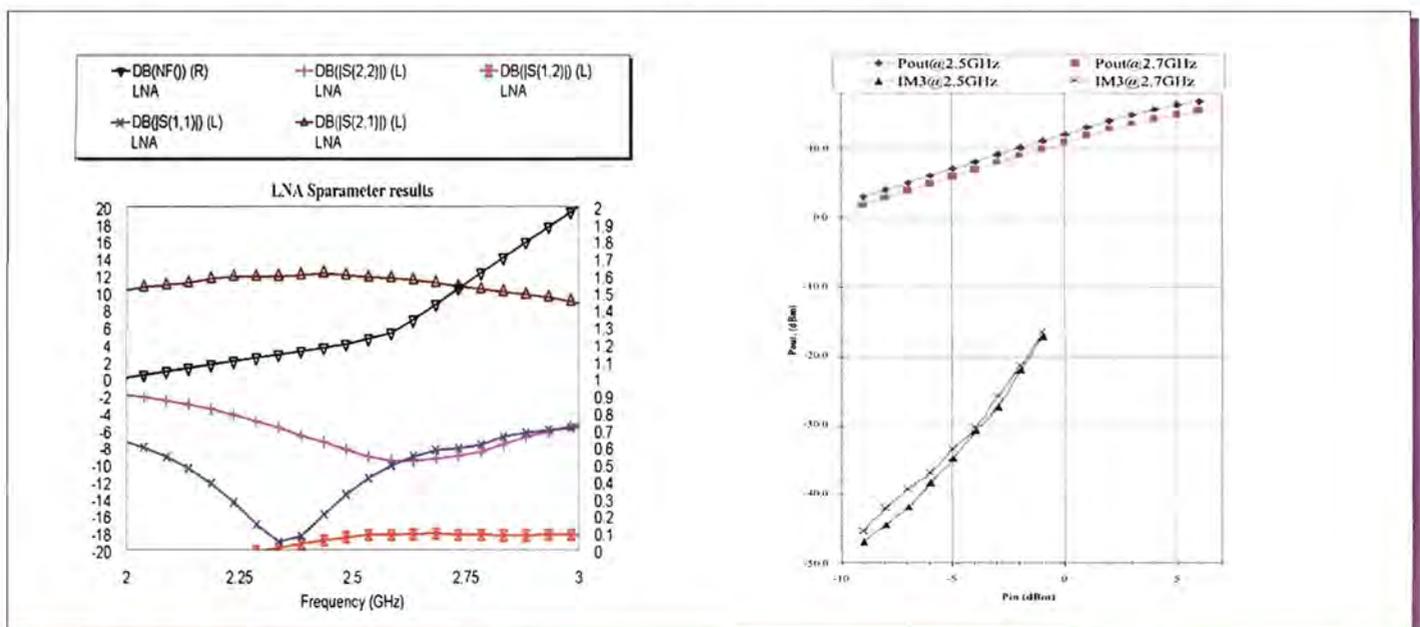
active-bias networks are normally used to ensure consistent device operating current. The uniformity achieved in Filtronic's pHEMT family of devices virtually eliminates the need for such complex bias circuits and simpler networks (such as dual-bias or self-biased) can be used instead, at considerable cost savings.

Summary

A 2.5GHz WMAN demonstration radio has been designed and characterised. This radio front end circuit is intended to allow system designers the means to optimise device performance for particular requirements and is based on straightforward circuit design methodology. Additional design variants are planned to include bias circuit upgrades, as well as higher output power transmit amplifier chains. The radio is intended to meet the demanding linearity and efficiency requirements of the 802.16 WMAN standard.

Figure 4: Performance of the receive (RX) path.

The plot left shows the small signal gain, noise figure and input, output return loss as a function of frequency in GHz. The other plot shows output power and 3rd-order intermodulation products as a function of input power.



Simple microwave filters

By Paolo Antoniazzi and Marco Arecco

In a professionally designed filter, ideally, only synthesis is required. When constructed, the prototype achieves all the desired characteristics. In practice, this does not happen. Prior to the PC simulation era, the recourse was to build and modify a prototype to achieve the desired filter characteristics. This is still the way for building many non-professional filters, as in the microwave amateurs' field, using small copper cavities realised through standard "Pipe Cap" (see **Figure 1a**).

Different resonance modes can be used with a cavity. Most interesting for amateur radio use is the TM_{010} mode, where the resonance frequency depends only on the inner diameter (D) of the cavity. Practically, $f = 229.56/D$, where D is in millimeters and f in GHz.

In **Figure 2**, the E (electric) and H (magnetic) fields in the cylindrical cavity are shown. We can see also from **Figure 3** that, with $D/L = 1$, very high values of Q are theoretically possible, but this is not compatible with the necessity of avoiding spurious modes (as the TE_{111}), because the adjustment screw normally used (see **Figure 1b**) acts to the modes (TM_{010} and TE_{111}) in a different manner.

As an example, with $L = 14\text{mm}$ (cylindrical cavity height) and $D = 20\text{mm}$, we have $f_{TM_{010}} = 11.48\text{GHz}$ and $f_{TE_{111}} = 13.85\text{GHz}$, with the spurious mode TE_{111} only still 2.37GHz away. Unfortunately, the highest Q of resonator cavities can't be reached when using small heights and, therefore, the selectivity of the filters is lower. One way is to use a precision TM_{010} machined cavity with a tuning screw limited to the fine tuning function. In a copper

cavity with $D = 21.5\text{mm}$ and $L = 14\text{mm}$ the resonance (TM_{010}) is at 10.67GHz with a calculated Q = 9516. The nearest spurious mode is at 13.47GHz (TE_{111}).

It is useful to be able to predict these frequencies, in order to gain insight into the spurious performance of a filter. The easiest way to predict these modes is to use a mode chart as shown in **Figure 4**. The "Dominant Mode" of a cavity is the lower frequency at which it can resonate.

To prevent the secondary modes resonance, the TM_{010} cannot be excited in the whole D/L range reported in Figure 3, but only in the part of the graph where the ratio $D/L > 1$. At $D/L \leq 1$, the dominant mode becomes the TE_{111} . Practical values of the D/L ratio to be used are 1.4-2.4 for TM_{010} and 0.45-0.5 for TE_{111} modes.

The TE_{011} is not a dominant mode so care must be taken to choose a coupling system that does not excite the other possible modes that could resonate within the frequency tuning range of the cavity. Interestingly, the unloaded quality factor Q_u is about three times greater than that of TM_{010} or TE_{111} cavities.

Another advantage of the TE_{011} is that there is not axial current. This means that the end plate can be free to move without significant loss due to the current that flows in parallel to the circular caps of the cylinder. With $D/L = 1.5$, the diameter of the TE_{011} cavity is about two times that of a TM_{010} cavity.

If more professional design is needed, waveguide filters are the solution.

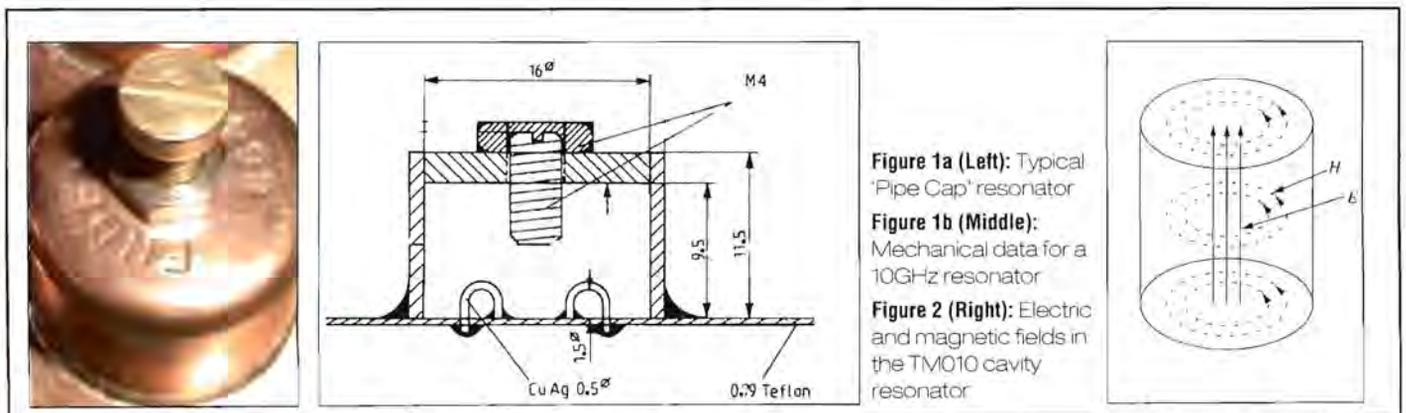


Figure 1a (Left): Typical "Pipe Cap" resonator

Figure 1b (Middle): Mechanical data for a 10GHz resonator

Figure 2 (Right): Electric and magnetic fields in the TM_{010} cavity resonator

Waveguide filters

There are several types of filters that can be used to perform the job of separating RF and LO or image frequencies, but most are either difficult to construct or have losses that are unacceptable. From a construction point of view, the waveguide approach is attractive and, at 10GHz, these filters are relatively small.

There is a website where you can verify the filter:

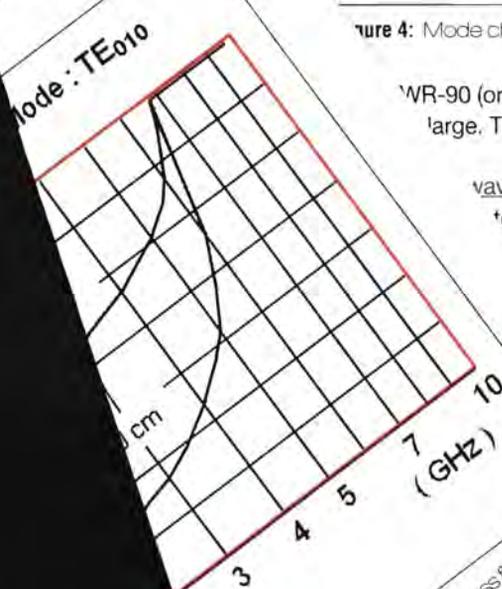
www.wavetech.com/IRISHTML/iris2p.htm

Bandpass structures consist of propagation of standard waveguide (see Figure 5) as half-wavelength resonators, via discontinuities in the guide (see Figure 5) or posts.

These structures employ iris-coupled resonators. You will see a pattern similar to that of a resonator filter. The waveguide width and the iris material are chosen as with other filters. It is a designer's job to have tuning capability and tolerance variation.

defined by the distance between the posts.

is the same length. To all these having the same continuation to the guide is calculated using the rectangular



Response of the simple bandpass filter of Figure 9
ELECTRONICS WORLD ■ October 2005

CAVITY MODES COMPARISON AT 10GHz

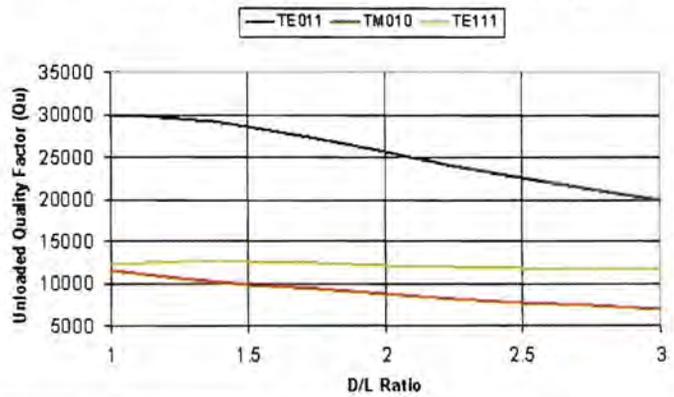


Figure 3: Unloaded Q of TM₀₁₀ microwave cavities

MODE CHART FOR RIGHT CYLINDER
(f in GHz, D in mm)

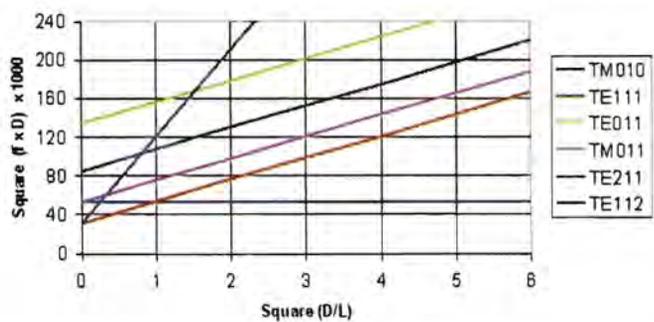


Figure 4: Mode chart for MW cavities

WR-90 (or WG-16 in UK) where the side "a" is large. The real-time software is available

www.wavetech.com/IRISHTML/iris2p.htm

changing simulation method with 13 in the analysis.

response and the input/output of the filter are shown in the bandpass filter of this type

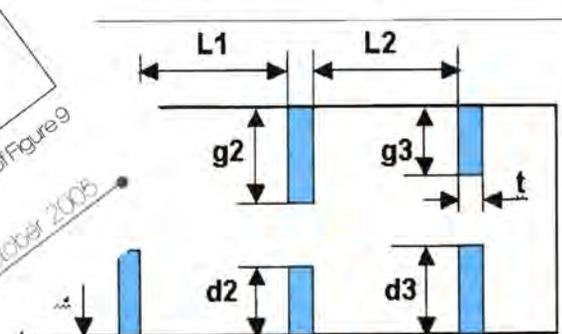




Figure 7: On-line design data for the 10.4GHz filter

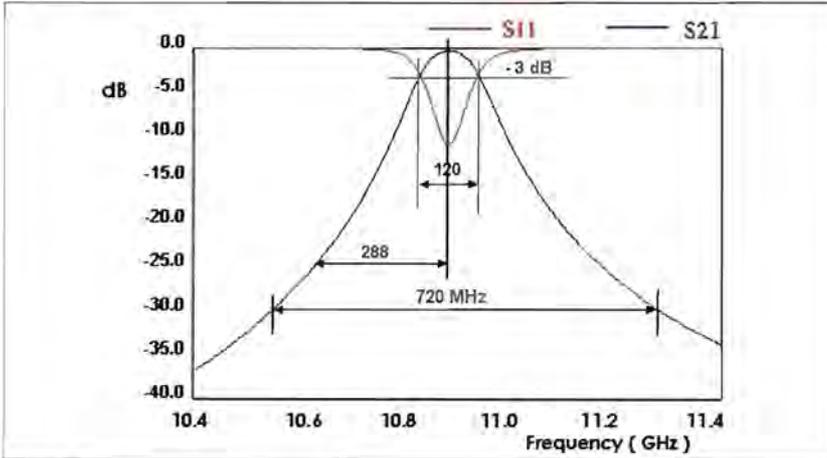


Figure 8: Calculated response of the filter

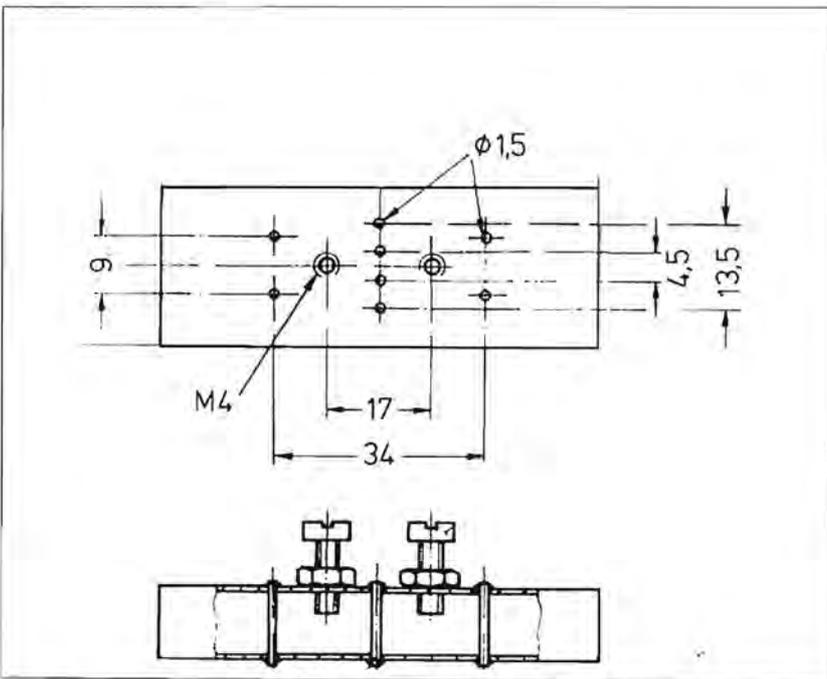


Figure 9: Single-stage waveguide bandpass filter using posts

has a -3dB bandwidth of about ±60MHz and 25dB attenuation at ±288MHz.

For the filters using posts, we include only a simple example from DC8UG. The most important mechanical dimensions of the filter (without waveguide flanges) are shown in **Figure 9** and the pass-band response is in **Figure 10**. This filter is only a didactical realisation for beginners and is normally not suited for 10GHz local oscillator filtering.

High-pass filter

A very easy method to manufacture a high-pass filter lies in the use of a standard waveguide, of a defined length, in the cut-off region (see Table 1). If the involved guide has a different size than the used one, suitable adapters are used to match the source and load.

The equation that describes the shape of the waveguide attenuation, in decibels, under the cut-off frequency is:

$$A = 54.5 (d / \lambda_c) \sqrt{1 - (\lambda_c / \lambda)^2}$$

where λ_c is the cut-off wavelength, λ the working wavelength and d is the guide diameter. To apply correctly the above formula, all dimensions must be expressed using the same units. Take note that the total attenuation obtained is directly proportional to the waveguide length.

The cut-off wavelength can be calculated using the following that is applicable to a rectangular waveguide:

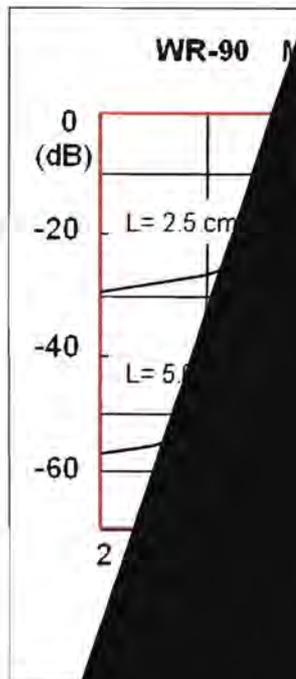


Figure 10

$$\lambda_c = 2a$$

where "a" is the largest dimension of the guide cross-section that is considered to operate with the TE₁₀ mode. However, a new equation is applied to the circular waveguide if operating in TE₁₁ dominant mode:

$$\lambda_c = 3.412a$$

In this case, "a" becomes the waveguide radius. An example is shown in **Figure 11** using a WR-90 waveguide (X-band = 8.2 to 12.5GHz). The considered lengths are about one and two inches (2.5 and 5.0mm).

Simple measurements

In **Figure 12** we can see the simple setup used for our measurements, which include a Marconi 6058B microwave generator and 6587 RF signal leveller, plus a well-known HP 431B power meter. Two WR90-to-coaxial adapters (HP model X281A) and a 10dB - 18GHz SMA fixed attenuator are the

only other components of the tests circuit. An HP waveguide attenuator - model X382A - and a 10dB waveguide directional coupler model X752C (with 40dB directivity) was used for analysing the filters' input/output matching. All these components are available today at very low-cost on the surplus market.

WAVEGUIDE CHARACTERISTICS					
Type	Inner Window (mm)	Dominant mode	λ_c (mm)	f_c (GHz)	Frequency Range (GHz)
Rectangular	a x b				
WR-90	22.86 X 10.16	TE ₁₀	45.7	6.56	8.2÷12.5
WR-75	19.05 X 9.53	TE ₁₀	38.1	7.87	9.8÷15.0
Circular	diameter				
WC-94	23.83	TE ₁₁	40.7	7.38	8.5÷11.6
WC-80	20.24	TE ₁₁	34.5	8.69	10.0÷13.7

Figure 11: Calculated response of high-pass, using WR-90 in the cut-off zone

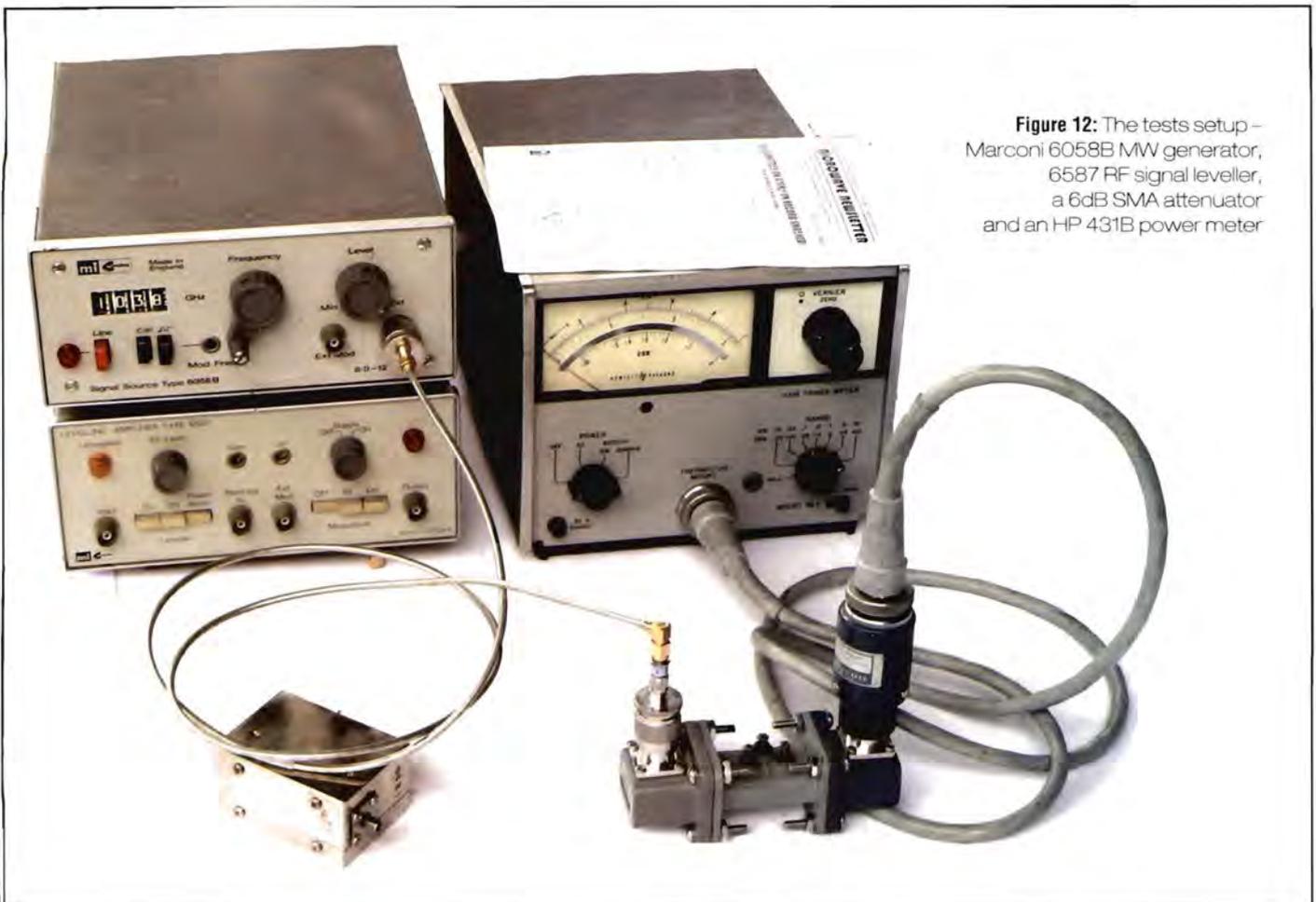
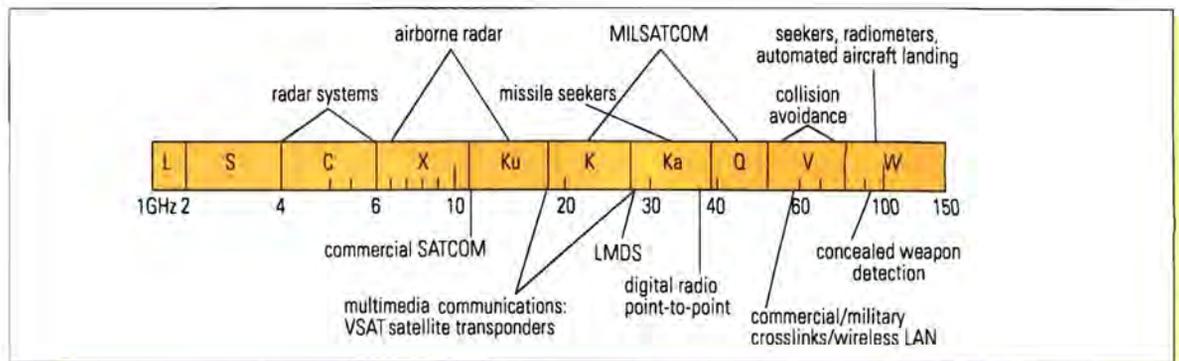


Figure 12: The tests setup - Marconi 6058B MW generator, 6587 RF signal leveller, a 6dB SMA attenuator and an HP 431B power meter

No MMIC? No WLAN

Susan Curtis of the Institute of Physics discusses the issues revolving around new developments of millimetre-wave monolithic microwave integrated circuits (MMICs)



Any maturing electrical technology is characterised by a trend toward smaller size, lighter weight, lower cost and increased complexity. Microwave technology is no exception: for the past 20 years engineers have been developing microwave integrated circuits that replace bulky and expensive waveguide and coaxial components with smaller, cheaper, planar components.

These integrated circuits incorporate passive elements such as transmission lines, resistors, capacitors and inductors as well as active devices such as diodes or transistors. The simplest approach exploits transmission lines to provide connections between discrete transistors and passive components that are wire-bonded to a substrate. However, the objectives of smaller size and lower cost are best achieved by monolithic microwave integrated circuits (MMICs), which combine active and passive components on a single semiconductor substrate. MMIC technology allows total microwave subsystems such as receiver front-ends and radar transmit/receive modules to be integrated onto a chip just a few millimetres in size.

Gallium arsenide (GaAs) has traditionally been the substrate of choice, because it is suitable for realising both high-speed transistors and low-loss passive components. Today's MMICs can operate at frequencies ranging from 1GHz up to 100GHz and beyond, with the most advanced technologies now able to achieve operation up to 200GHz.

Applications for millimetre-wave MMICs
The economies of scale enabled by MMIC technology have been crucial for driving rapid progress

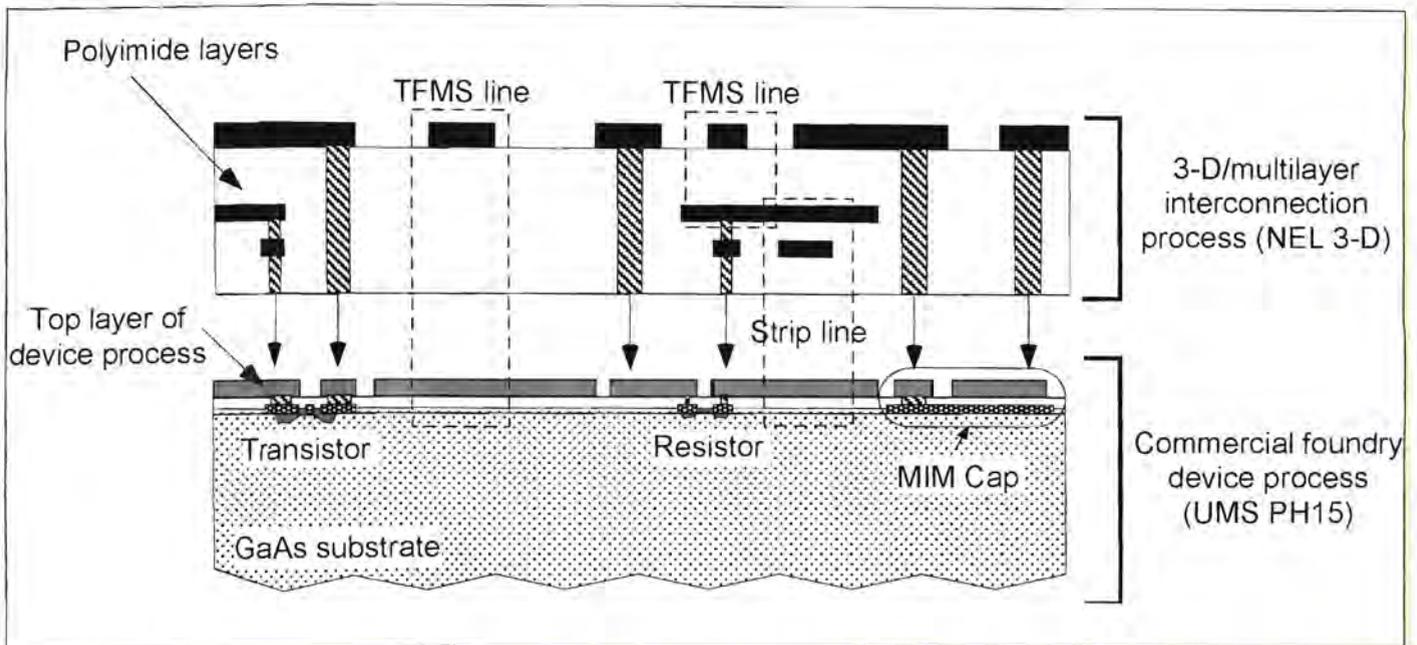
in the mobile communications industry. Cellular handsets, wireless basestations and wireless local-area networks all rely on MMICs operating at 1-2GHz to send, receive and amplify voice and data signals, and there is no doubt that the *global revolution* in wireless communications would not have been possible if MMIC technology had not matured enough for wireless networks to become an economical alternative to extensive routing and laying of coaxial or fibre-optic cables.

Now, however, designers and engineers are working to extend the operating range of MMIC solutions to address new applications at frequencies of 100GHz and beyond, which correspond to wavelengths of a few millimetres. A new report from Institute of Physics Publishing, 'Commercial Applications for Millimetre-Wave MMICs' (www.technology-tracking.com), provides an in-depth analysis of this growing trend, combining core content on the latest technological innovations with a frank assessment of the commercial drivers at play in this emerging market.

The report points out that MMICs operating at these millimetre-wave (mm-wave) frequencies offer several major benefits over their low frequency counterparts. For a start, the higher operating frequencies enable more information to be encoded in the signal, which make mm-wave solutions ideal for high-bandwidth, high-capacity communications systems. High-frequency MMICs also work well for applications requiring narrow antenna beams or high spatial resolution in a compact size, since the shorter wavelengths of mm-waves enable the use of smaller receiver and transmitter elements.

The latest developments in circuit design have

Frequency bands in the microwave part of the electromagnetic spectrum. Commercial and military uses of microwave signals extend from a few gigahertz up to 100GHz



enabled microwave engineers to improve the performance of mm-wave MMICs, while commercial foundry processes are now available for fabricating chips operating at frequencies of up to 100GHz. Further optimisation of circuit designs will reduce both the cost and size of millimetre-wave components, which is expected to drive a steady growth in this market. Indeed, industry figures estimate that the market for commercial mm-wave MMICs will grow from \$163m in 2003 to \$400m in 2007. According to the report, several key areas are already showing significant commercial activity.

Key areas for mm-wave MMICs

– **Terrestrial broadband:** Transceivers for fixed-wireless broadband systems now represent the largest commercial market for mm-wave MMICs. Sales of radio frequency components for mm-wave radios totalled \$40m in 2003 and that figure is set to rise as vendors introduce next generation systems offering higher data rates and longer transmission ranges. Systems operating beyond 70GHz are now being developed to deliver data communications at speeds of up to 10Gbit/s.

– **Satellite communications:** Two-way satellite communication at 12-18GHz already represents a significant commercial market for microwave MMICs, while next-generation systems operating at 26-40GHz will be deployed over the next two years. Unit shipments of mm-wave MMICs for this application are expected to exceed 500,000 in 2005 and could reach 1.5m in 2006 and beyond.

– **Automotive applications:** Automotive radar at 76-77GHz is widely anticipated to be the next big application for mm-wave MMICs. Radar-based systems

providing adaptive cruise control have already been fitted to luxury cars, while falling component costs look set to open up the mid-price car market. Automotive-radar applications could account for 4.5m mm-wave MMICs by 2007, while total mm-wave MMIC usage in this market could approach 100m per year by 2010.

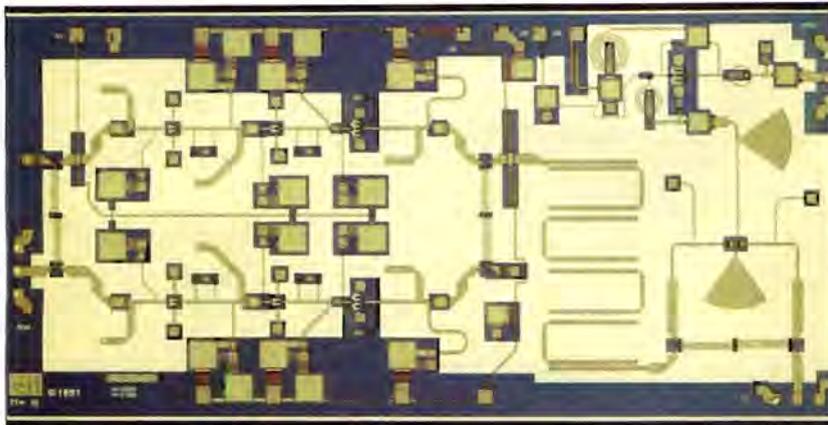
– **Military systems:** Defence applications kick-started the development of MMIC technology and the growing need for sophisticated electronic and communications systems on the battlefield is driving demand for high-performance MMICs operating at high frequencies. The largest market lies in airborne electronic warfare equipment, but mm-wave MMICs are also being deployed in phased-array radar systems and could be used to equip soldiers with advanced communications and electronic warfare systems.

Facing challenges

There is no doubt that mm-wave MMICs offer serious potential in the commercial market-place, but the report's authors contend that the big challenge for MMIC suppliers is to deliver packaged and tested parts that meet the performance, cost and size criteria demanded by commercial end-users.

These challenges are already being addressed at the chip level by the major developers and manufacturers of mm-wave MMICs, including TriQuint and Northrup Grumman in the US and United Monolithic Semiconductor in France. As a result, it is now generally agreed that the latest generation of MMIC manufacturing processes can deliver the gain and bandwidth performance required for applications at frequencies of up to 100GHz.

A MMIC receiver integrates active and passive devices on a single substrate



Left: Multilayer MMICs exploit multiple layers and dielectric and gold metallisation to form passive component planes above the surface of the chip.

Right: The next few years will see rapid growth in the use of SiC wafers as a substrate for electronic devices based on SiC and GaN

At the same time, intense R&D activity is continuing to improve the performance of MMIC technologies, in particular to deliver more power and better low-noise characteristics over a wider frequency range. Much of the innovation stems from conventional compound semiconductors, with new device architectures based on GaAs and InP now emerging to provide better power performance at mm-wave frequencies.

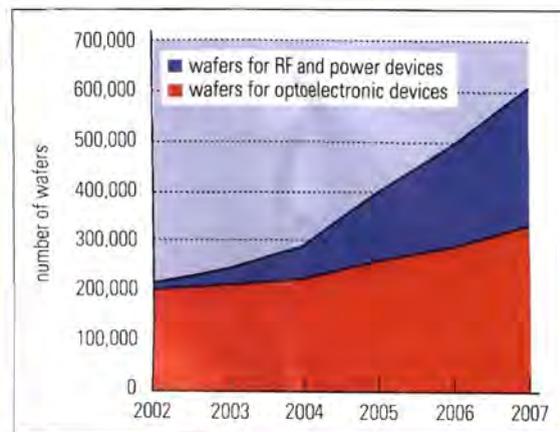
Emerging technologies

New technologies include GaAs-based metamorphic HEMTs (mHEMTs), which are rapidly emerging as easy-to-manufacture devices that match the high-frequency performance of InP HEMTs. MHEMTs exploit a special buffer layer that shifts the lattice constant by up to 5%, allowing InP HEMT structures with high indium content – originally developed to extend the high-frequency performance of HEMT devices – to be grown on GaAs substrates.

According to the report, mHEMT wafers with high quality and good surface morphology have been demonstrated using buffer layers made from both InAlGaAs and AlGaAsSb. Foundry services are now available for 0.15µm mHEMT low-noise processes on four-inch wafers and 0.15µm power processes on six-inch wafers, while the first mHEMT MMIC products are also appearing on the market. The first application of the technology is likely to be in low-noise amplifiers, although mHEMT technology has also been investigated for high-efficiency power amplifiers operating above 20GHz.

Interest is also growing in the use of InP HBTs for high-performance applications, since these devices deliver unparalleled current densities at frequencies of a few hundred gigahertz. Researchers at the University of Illinois in the US have reported the fastest InP HBT to date, with a cut-off frequency of 509GHz and F_{max} of 219GHz.

Thanks to funding from the Defense Advanced Research Projects Agency (DARPA) in the US, InP HBT foundry services are now available from Vitesse Semiconductor. However, InP remains an



expensive material system that requires specialist fabrication techniques and challenges remain in scaling the device dimensions further, reducing the power consumption and enabling greater integration. As a result, InP HBTs are likely to be reserved for applications that require their superior power performance, such as military radar and communications systems.

At the same time, other materials systems are starting to challenge the dominance of traditional compound semiconductors for mm-wave applications. For example, silicon-germanium (SiGe) technology, which exploits the same manufacturing processes as silicon-based CMOS, is rapidly emerging as a low-cost alternative to InP devices for low-power applications requiring operating frequencies of up to 100GHz.

Today, SiGe HBTs can be found in telecommunications equipment, ranging from wireless handsets and basestations, through to wireless LAN chipsets and transceivers for optical communications at 10-40Gbit/s. The latest foundry service offered by IBM exploits 0.18µm feature sizes to achieve operating frequencies from 40 to 100GHz, while work is continuing on developing manufacturing processes for SiGe HBTs operating at up to 200GHz. One key advantage of this technology is that it allows analogue, digital and RF functionalities to be integrated into a single chip using existing CMOS fabrication plants.

Applications for SiGe HBTs

Potential applications for SiGe HBTs range from high-speed communications systems at 60GHz and beyond to automotive radar systems at 77GHz. Both of these commercial applications require low-cost RF components and SiGe is likely to offer the required performance at a lower cost than compound-semiconductor solutions. The major limitation of current SiGe HBTs is that their breakdown voltage is limited to about 3.6V, which means that they cannot be used for applications requiring high power inputs.

ELECTRONICS WORLD

OCTOBER 2005

"Thank you, Arthur C Clarke" ...

In October 1945 'Wireless World' magazine published a scientific paper by a young Englishman, Arthur C. Clarke, which first explained how a radio transmitter placed in outer space, 36,000km from earth, could provide communications links between distant parts of our world. Three such 'satellites' could, therefore, provide global coverage.

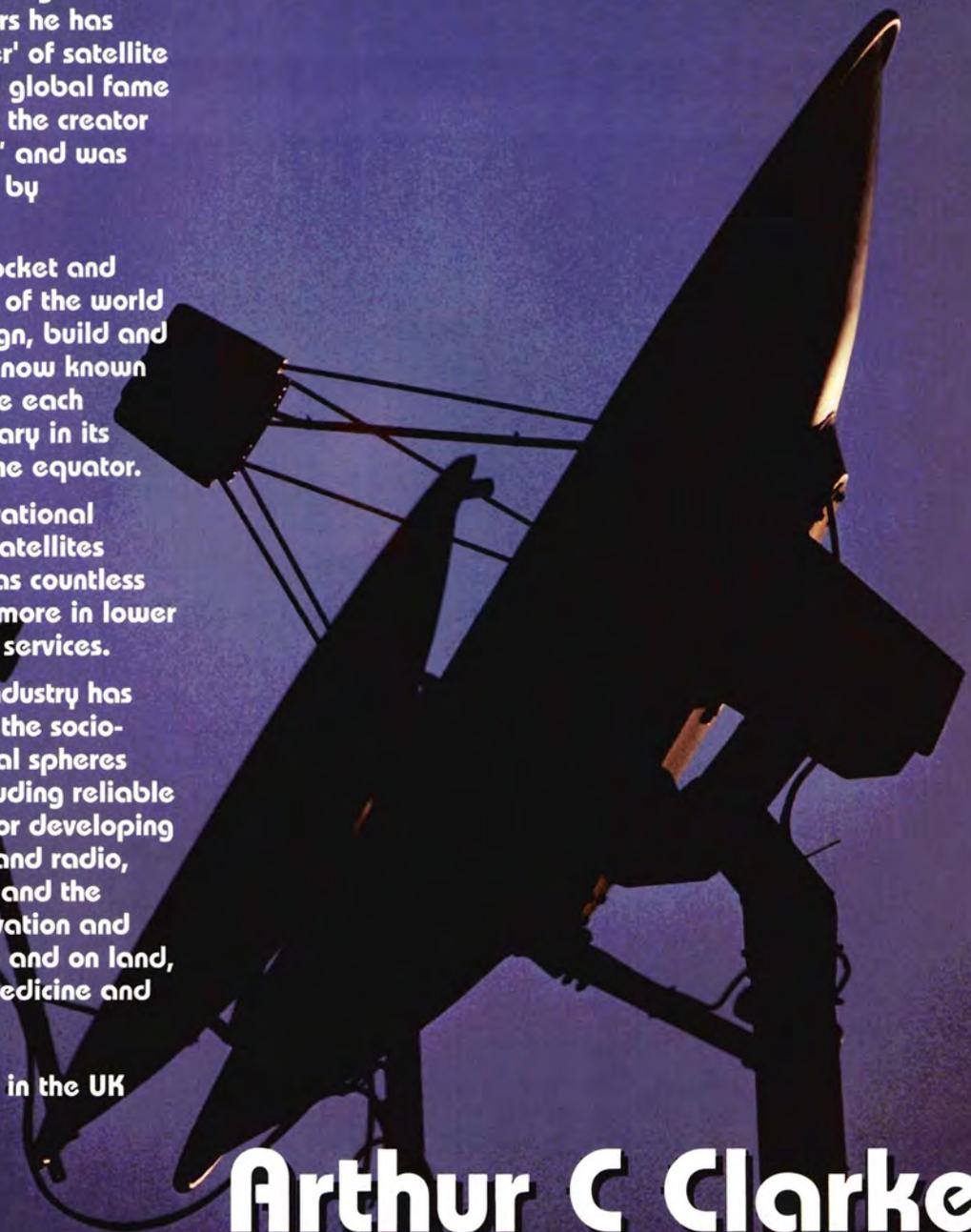
Today, Arthur C. Clarke at 87 is still a prolific writer, living and working in Sri Lanka. In the intervening years he has been hailed as the 'godfather' of satellite communications. He achieved global fame in Hollywood and beyond as the creator of "2001 – A Space Odyssey" and was rewarded with a knighthood by Queen Elizabeth II in 1998.

Over the last 60 years, the rocket and telecommunications scientists of the world have discovered how to design, build and launch satellites into what is now known as "The Clarke Orbit" – where each satellite is effectively stationary in its designated location above the equator.

There are now over 300 operational commercial communications satellites spanning the globe, as well as countless military satellites and many more in lower orbits, providing a variety of services.

A multi-billion dollar space industry has evolved, which has impacted the socio-political, economic and cultural spheres with benefits to mankind including reliable telecommunications services for developing countries, satellite television and radio, weather forecasting, Internet and the global economy, earth observation and monitoring, navigation at sea and on land, global tele-education, tele-medicine and much more...

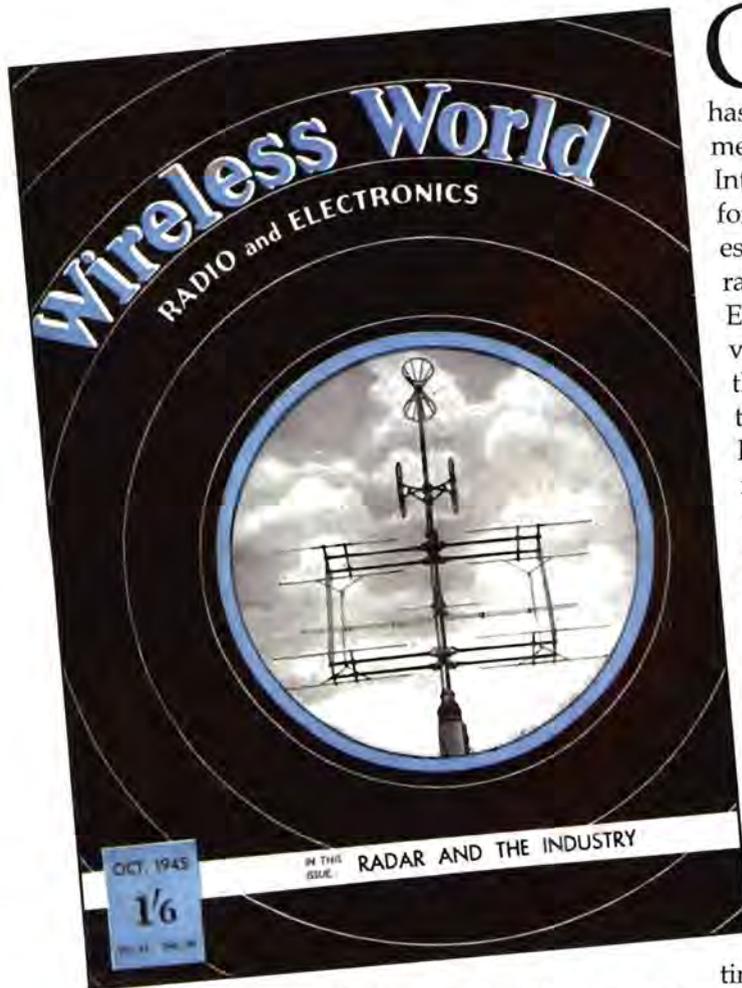
Peter Marshall, ACCF Director in the UK
(www.clarkefoundation.org)



Arthur C Clarke
Past and Present
COMMUNICATIONS SPECIAL

Peacetime uses for V2

V2 for Ionosphere Research?



ONE of the most important branches of radio physics is ionospheric research and until now all our knowledge of conditions in the ionosphere has been deduced from transmission and echo experiments. One of the more modest claims of the British Interplanetary Society was that rockets could be used for very high altitude investigations and it will not have escaped your readers' notice that the German long-range rocket projectile known as V2 passes through the E layer on its way from the Continent. If it were fired vertically without westward deviation it could reach the F1 and probably the F2 layer. The implications of this are obvious: we can now send instruments of all kinds into the ionosphere and by transmitting their readings back to ground stations obtain information which could not possibly be learned in any other way. Since the weight of instruments would only be a few pounds—as compared with V2's payload of 2,000 pounds—the rocket required would be quite a small one. Its probable take-off weight would be one or two tons, most of this being relatively cheap alcohol and liquid oxygen. A parachute device (besides being appreciated by the public!) would enable the rocket to be re-used.

This is an immediate post-war research project, but an even more interesting one lies a little farther ahead. A rocket which can reach a speed of 8 km/sec parallel to the earth's surface would continue to circle it for ever in a closed orbit; it would

become an "artificial satellite." V2 can only reach a third of this speed under the most favourable conditions, but if its payload consisted of a small one-ton rocket, this upper component could reach the required velocity with a payload of about 100 pounds. It would thus be possible to have a hundredweight of instruments circling the earth perpetually outside the limits of the atmosphere and broadcasting information as long as the batteries lasted. Since the rocket would be in brilliant sunlight for half the time, the operating period might be indefinitely prolonged by the use of thermocouples and photo-electric elements.

Both of these developments demand nothing new in the way of technical resources; the first and probably the second should come within the next five or ten years. However, I would like to close by mentioning a possibility of the more remote future – perhaps half a century ahead.

An "artificial satellite" at the correct distance from the earth would make one revolution every 24 hours; i.e., it would remain stationary above the same spot and would be within optical range of nearly half the earth's surface. Three repeater stations, 120 degrees apart in the correct orbit, could give television and microwave coverage to the entire planet. I'm afraid this isn't going to be of the slightest use to our post-war planners, but I think it is the ultimate solution to the problem.

ARTHUR C. CLARKE

British Interplanetary Society.



Evolution of global communications:

The post A.C. Clarke era

Professor Barry G Evans looks back, sixty years hence, to examine the realisation of Arthur C. Clarke's predictions in terms of global communications and the role that satellite communications has played therein.

By Barry Evans

The visionary Wireless World article by Arthur C. Clarke of sixty years ago is justly credited as the origin of satellite communications and specifically of the geostationary earth orbit. Three satellites appropriately placed in the equatorial plane orbit, at 36,000km altitude could, as Clarke suggested, via terrestrial relay provide global communications.

In 1945, at the time of the paper, global communications only existed in terms of broadcast short-wave radio and via HF communication hops in the 3-30MHz region. The latter relied on total internal reflection within the ionospheric layers for radio waves with angles of incidence greater than some critical angle. This was termed "sky-wave communication" and was the only means of transoceanic communications at that time. It was very unreliable, being dependent on the forecasting of the state of the ionosphere, which varied both on a daily and on a longer term, sun-spot period, basis. Bandwidths were small in today's terms and only allowed for a few voice channels to be transmitted.

In the early 1940s the demands of world warfare had provided radar systems using low microwave frequencies in the 1-3GHz range and consequent components that would enable point-to-point microwave relays covering 10s of km for communications. At about the same time, the first broadcast systems in the VHF/UHF (100s MHz) spectrum were being implemented for the distribution of television, which had been invented in the war years and was now being exploited. These lower (than microwave) frequencies were used as the attenuation was less, resulting in larger broadcast area coverage, and simple wire antennas and receivers enabling cheaper domestic terminals. It is interesting to note that it was very much in this context, of TV broadcasting, that Arthur Clarke wrote his paper. The broader-band television signals (5-6MHz) could not be delivered via HF communication systems and he considered that a network of terrestrial broadcast transmitters fed by microwave relays would not be economic or extendable globally.

His answer was to suggest use of another WW2 technology – intercontinental rockets. He foresaw that such rockets, given adequate propulsion, could escape the earth's gravity and become a low orbiting satellite relay (what we now call a LEO satellite). His extension to higher altitudes produced the GEO satellite and the global coverage concepts. He also predicted the use of solar cells to provide the power for such satellites; batteries to overcome eclipse periods, altitude control and large reflector antennas for spot beam coverage – all of which are in use today. We note that this was all to provide efficient broadcast and communications coverage which was more power efficient and environmentally friendly – nothing much has changed.

Global communications

Communications over land evolved using multi-pair cables and

analogue techniques (fdm) driven by user demands for telephony in the 1940/50s. Lower loss coaxial cables were introduced in the 1950s and these, together with microwave radio relay links, provided the major long distance connections. Despite Clarke's suggestions, broadcast of AM and then FM radio as well as television, also developed using a network of broadcast transmitters fed by the radio relays. Between various land points, HF was still being used alongside submarine cables, which originated in the 1920s for telegraphy using cable pairs but were again replaced by coaxial cables in the 1940/50s as cable design improved. The first major transatlantic cable (TAT1) was introduced in 1956 using coaxial cables and analogue fdm transmission, with a capacity of just 36.4kHz telephone channels, followed by many other submarine cables.

Satellites came of age in the 1960s, when rocketry had developed to enable launches into the earth orbit. Major studies were introduced in the early 60s into which orbits to use, and Intelsat (the first International Satellite Consortium) settled upon the GEO (Clarke orbit), with the first launch in 1964. It was in 1968 when three such satellites were placed over the major oceans and Clarke's prediction became a reality after 23 years.

However, the use was for point-to-point connections between large (30m diameter) earth stations connected into the national telecommunication networks. From this time on, there was a choice between satellite and submarine cable for connections of land and HF communications was on the wane.

Two other important developments took place in the 1960s. The first was the implementation of PCM (pulse code modulation), which heralded a change from analogue to more efficient digital communications, and the second was the development of optical fibre communication systems, which provided much lower loss and greater bandwidth than cables. Thus, in the 70s/80s telecommunication networks gradually changed from analogue to digital (including the switching systems) and optical fibre replaced cables and radio-relay in all but the extreme geographical areas where still some radio exists today.

The first submarine digital optical transatlantic cable (TAT8) was introduced in 1988 with a capacity of 8000, 64kbps telephone channels and saw the gradual demise of point-to-point satellite communications. Although developments of higher power satellites with multiple spot beams (predicted by Clarke) in GEO kept pace with submarine cables for a time, the much greater bandwidth and widespread deployment of submarine cables would always provide a lower cost per bit than by satellite. Satellites did enable developing countries to establish national and international telecommunication systems much earlier than would otherwise have been the case and, thus, played an important role in their economic development.

Within telecommunication systems, satellites will always find a role in diversification of routing and as back-up for cases



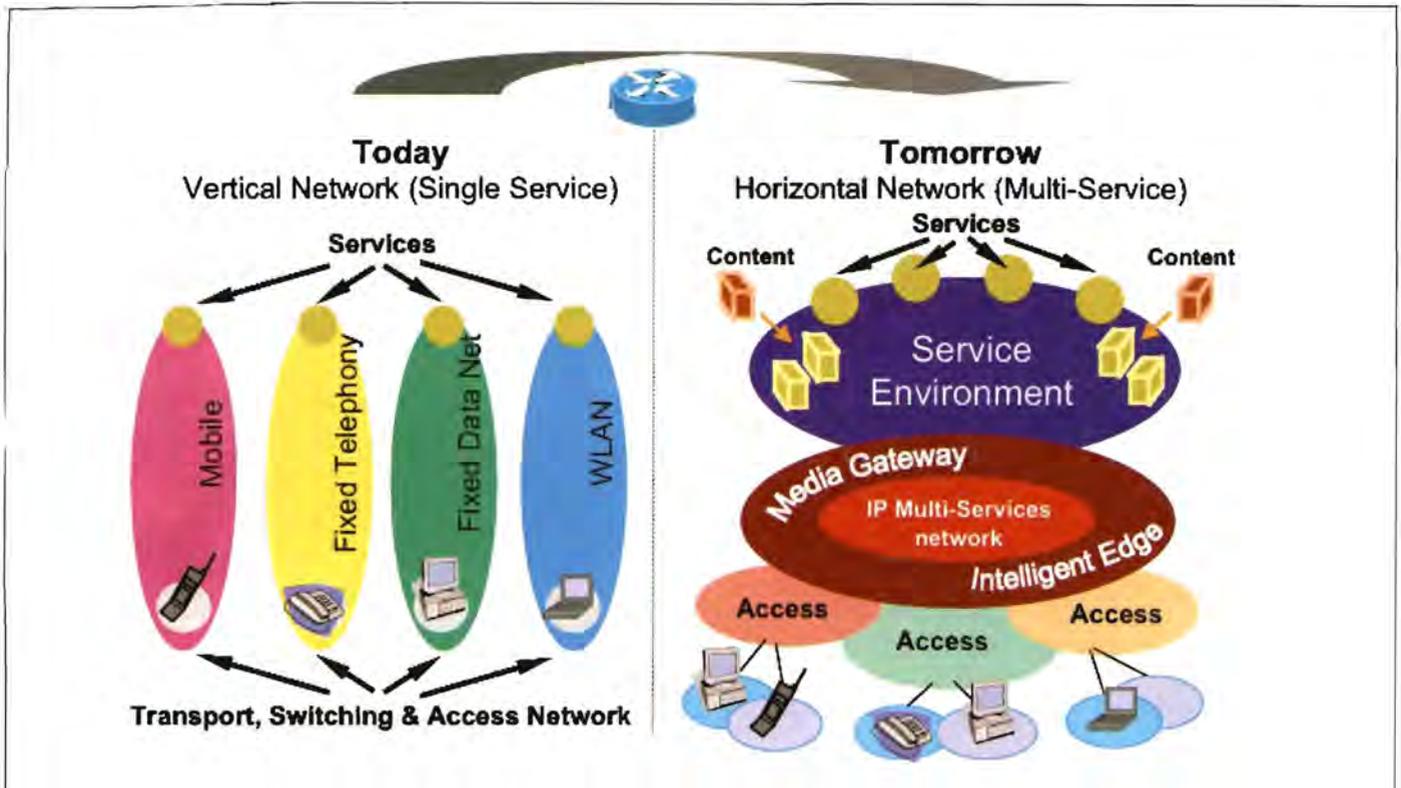


Figure 1: Move from single service to IP-based multi-services

when submarine cables are out of service for long repair periods. Perhaps the 1960-80s were the heyday of point-to-point satellite communications. Thus, today our modern fixed telecommunications systems are all digital, dominated by optical fibre transmission with satellites playing mostly a subsidiary role.

Broadcast and mobiles – a role for satellites?

In Clarke's original paper, the driver for satellites was broadcast services. It wasn't until the 1977 World Administrative Radio Conference (WARC 77) plan that allocated orbit slots and fixed frequency channels to each country that broadcast satellites were seen as an economic possibility for television broadcast. The plan was linked to a move from analogue television towards digital but the full digital compression technology was not available and a half way standard called MAC (multiplexed analogue components) evolved. The MAC standard and WARC77 plan was never really implemented to any great extent, due to delays in VLSI chip production, and satellite television only went ahead in the early 80s using higher power fixed satellites in Ku-band (around 12GHz) to 60cm domestic dishes, still using analogue techniques and frequency modulation. In Europe, Sky television was the driver operating satellites out of Luxembourg, in a mode reminiscent of the earlier Luxembourg commercial radio station.

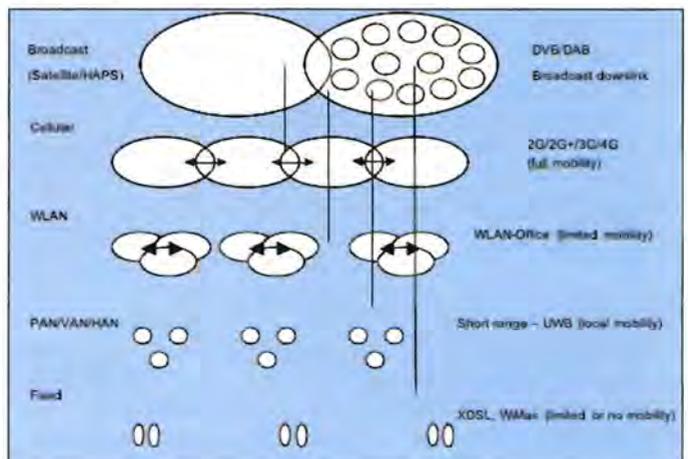
Around this time, there was considerable momentum for a UK television coverage satellite - Unisat, to operate within this plan, but it never materialised and, thus, an opportunity to realise one of Clarke's predictions vanished.

The next major step came in the late 90s with the introduction of full digital compression and transmission standards (MPEG2/DVB-S) and satellites, capitalised on their customer market to secure 80% of digital television distribution via satellite in Europe, outpacing cable rivals. Radio broadcast via satellite did not really emerge until the early 2000s with Digital

Audio Broadcast (DAB) standards and Digital Audio Radio Service (DARS) in the US. Today, Worldspace operates GEO satellites covering Asia, the Caribbean and the Americas and two new commercial ventures XM Radio and Sirius Satellite Radio, operating GEO and highly elliptic orbit satellites (HEO) respectively, have achieved success with US coverage for vehicles. These latter systems augment direct satellite coverage with terrestrial repeaters (gap-fillers) in urban areas in an integrated delivery mechanism.

This review would not be complete without mention of mobile communications, which didn't feature at all in Clarke's original paper. Indeed, extrapolating from his concerns regarding a network of broadcast transmitters it would not appear that he would have supported the idea of a larger network of base stations and terrestrial cells. On the other hand, he might have seen this as an opportunity for satellites. Interestingly, mobile satellites developed at the same time as terrestrial mobiles via the Inmarsat system, but have only been successful

Figure 2: Layered networks



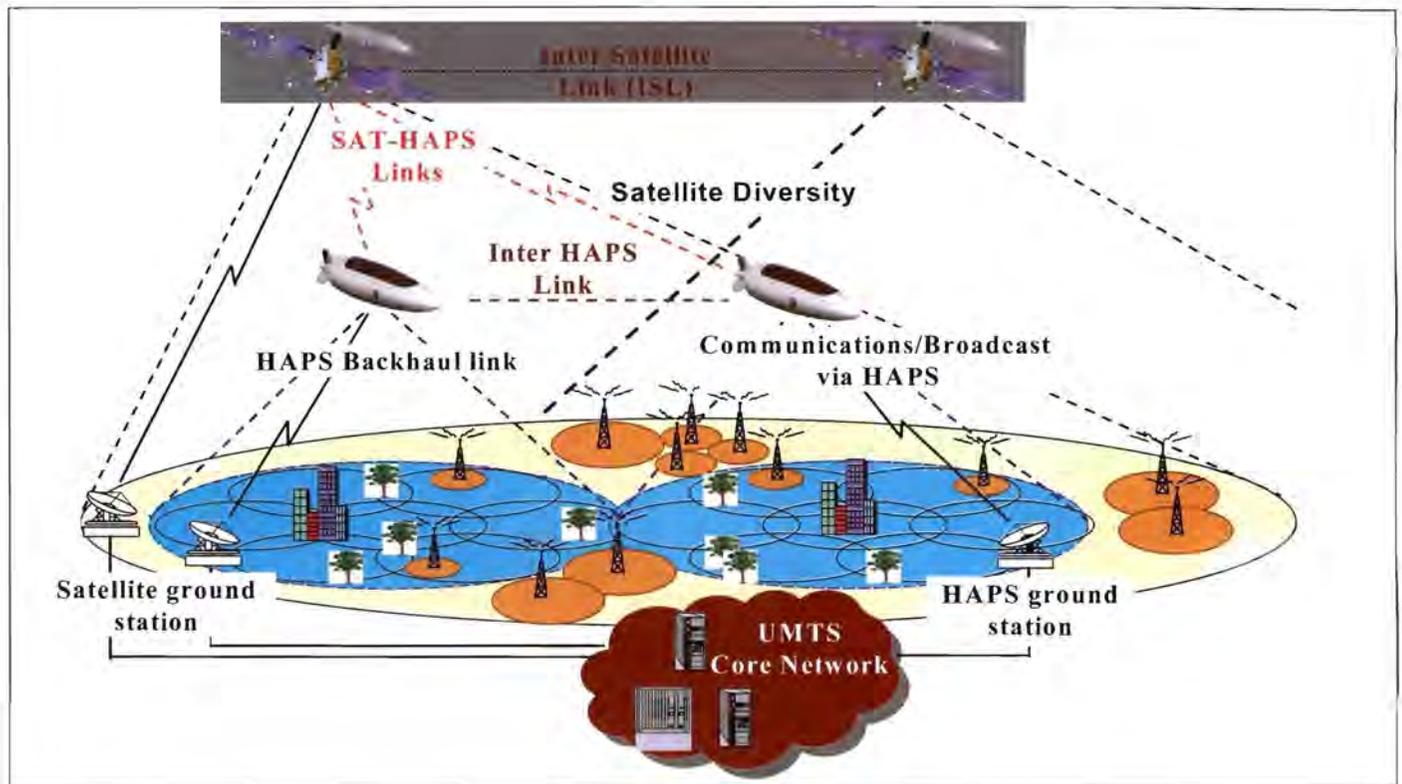


Figure 3: Possible integrated system architecture

in the niche areas of maritime and aeronautical, where terrestrial cannot compete. In the late 90s and early 2000s, when satellites tried to compete head-on with terrestrial mobile, via the use of satellite constellations – Iridium and Globalstar systems of LEO satellites (48-66), they failed economically to do so.

The future

Today's services are dominated by packet (IP) mode and Internet services, with delivery mechanisms that are becoming more radio based. As shown in Figure 1, today's vertical, service-orientated networks will evolve into tomorrow's horizontal, Internet multi-service based architecture. The latter has an all IP core network with a variety of access networks, which will mostly be radio based. Figure 2 demonstrates how such a scenario may be depicted in terms of a layer structure and indicates where satellites can play an important role at the top broadcast, wide cell coverage, providing mobility. To preserve quality of service whilst allowing seamless movement between networks, integration between satellite-cellular, Wi-Fi, personal area networks (PAN) and WiMax fixed radio will be necessary. The advantage of satellites has, and will always be, their wide area coverage. However, their power and spectrum efficiency has been shown to be inferior to terrestrial systems, despite Clarke's predictions – in fact, between 50-100 times improvement would be required for comparability with terrestrial. The future for satellites thus lies in integration with terrestrial and not with competition.

A possible scenario is shown in Figure 3. This depicts an all IP network with end-to-end connections and guaranteed quality of service. There is complete integration between terrestrial fixed, cellular and hot-spot connections with dynamic ad-hoc routing between networks. The interconnected satellite layer provides the wide coverage larger cells and the mobility management between the various networks. A subsidiary layer of intermediate sized cells is provided by high altitude platforms

(HAPS), located at around 20-25km in the stratosphere to deal more efficiently with hot spot areas and relieve the demands on terrestrial infrastructure, as well as collection for lower power sensor networks and broadcasting to urban areas. All networks are vertically and horizontally connected as indicated in Figure 2, and seamless and secure handover between them is provided. This is a possible vision of the future circa 2020.

Conclusions

It would appear that for broadcast television and, to a lesser extent, radio that satellites have succeeded but in mobile communications they have only done so in niche areas of sea and air coverage. Satellites still feature in global core networks on a point-to-point or multicast basis but, mainly, in a supporting role to terrestrial delivery. As mobility demands and multimedia services increase, the concept of integration between satellite and terrestrial delivery will become more attractive but to be realised will need a culture change on behalf of operators.

In the longer term, satellites will continue to play a role in global communications but it may only become significant with the realisation of smaller more efficient, cheaper satellites and launchers.

Professor Barry G Evans is from the Centre for Communication Systems Research at the University of Surrey.





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Geostationary weather satellites

Satellites have evolved to offer almost continuous surveillance of the entire planet.

By Pat Norris

GOES-N – first in a new US series

Satellite observations have revolutionised weather forecasting. In the UK, for example, satellite data now provides about 70% of the information used in the core weather forecasts while incurring only 50% of the data collection costs. On a global scale, satellite data provides the only source of information for most of the southern hemisphere and for remote areas of the northern hemisphere. The European Centre for Medium Range Weather Forecasting (ECMWF) has reported a steady improvement in its forecasts for both hemispheres, but satellite data has radically improved the southern hemisphere forecast to the point where it now matches that of the northern hemisphere.

Thanks to satellites, instead of discrete observations scattered over the surface of the earth, mainly in the more populated areas and major trade routes, scientists now benefit from almost continuous surveillance of the entire planet. Where three or four weather ships covered the entire North Atlantic and Pacific Oceans, launching instrumented balloons twice each day, meteorologists can now receive atmospheric measurements at intervals of 50km or so over the entire globe. Instead of having to infer the shape and movement of weather systems from a few widely scattered observations, they can now enjoy a bird's eye view of the planet and see the movement and evolution of storm systems in animated sequences on a computer screen. This revolution is accomplished by two classes of meteorological satellites, which have many applications beyond pure meteorology.

The first images were in monochrome – shades of grey like a black-and-white photograph – obtained using daylight as the source of illumination. Such imagery is still useful but has been supplemented by a range of other developments. Infrared (IR) imagery ensures data continuity even through the hours of darkness. This is based on the thermal emissions of the clouds and can be used to derive the temperature and, therefore, the height of the cloud tops. IR and visible light images may be combined in a multi-spectral image. Areas that are simultaneously bright in the visible part of the spectrum and cold in the IR are deep cold rain clouds. They can be colour-coded to indicate the likely intensity of precipitation.

Other spectral channels may be added to the multi-spectral toolbox. Water vapour images show where clouds may develop and, as dry air is indicative of descending motion, provide information about the local dynamics of the atmosphere. Images from the spectral region in the near-IR, where visible light and the IR overlap, may be used for specific purposes

such as the identification of fog or forest fires, or used in various combinations with other imagery.

Further insights can be gained from viewing animated sequences of images from geostationary meteorological satellites. The powerful personal computer systems now widely available at reasonable cost are more than adequate to display movie-like animations of the evolving weather patterns over periods of hours, days, weeks or longer. This gives fresh insight into the dynamics of the atmosphere, including the development of weather systems and the general planetary circulation.

Geostationary versus polar orbiting

From their fixed vantage point, geostationary meteorological satellites can generate frequent images, typically every 15 or 30 minutes, of the full earth disc, or more frequent images of smaller areas. Images are useful over an area extending up to 70° north and south of the equator, and out to 70° east and west from the sub-satellite point. Image quality is reduced at the greatest distances because of the curvature of the earth, but useful quantitative products can be extracted from the images at distances of at least 55° great-circle-arc from the sub-satellite points. Sequences of images allow cloud movements to be tracked, providing information on winds at various altitudes. These satellites are the key source for timely information on rapid weather development, and the monitoring of tropical storms and large mid-latitude weather systems.

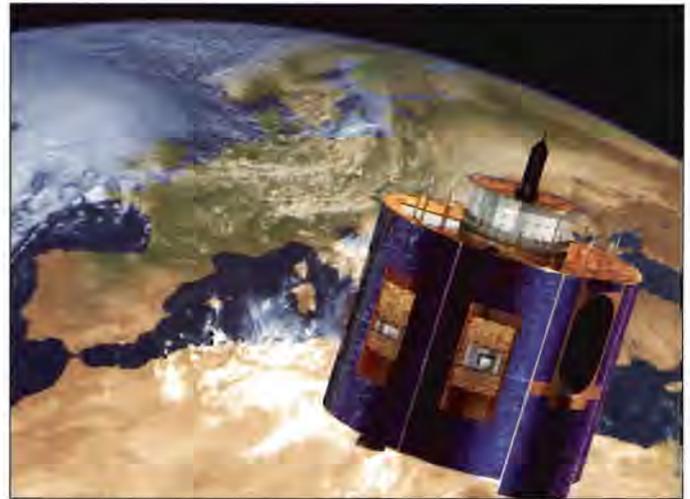
The polar orbiting satellites do not appear stationary from the ground. In contrast, their orbits are inclined at about 80° to the plane of the equator and they circle the planet about 14 times each day at an altitude of about 850km. The plane of the orbit remains almost constant, so that as the earth spins on its axis the tracks of successive orbits are displaced further to the west. In any period of 24 hours each satellite can view the entire planet, once during daylight and once at night. For most polar meteorological satellites the orbits are chosen to be sun-synchronised, which means that the plane of the orbit keeps a constant angle with the sun throughout the year, thus ensuring that the satellite passes over a given location at the same local (sun) time each day.

The geostationary satellites carry a narrower variety of instrumentation than the polar satellites and can observe the planet in less detail, but much more frequently. These complementary characteristics ensure that a constellation of five geostationary satellites and two or three polar systems fulfil basic operational requirements.





Japan's MTSAT-1R new generation satellite



Europe's Meteosat 2nd generation satellite [Credit: ESA-D. Ducros 2002]

First geostationary weather satellites

Although the first two geosynchronous satellites (Syncom-2 and Early Bird) carried exclusively telecommunications payloads, the third, ATS-1, launched on 7 December 1966 also carried a meteorological payload. Following further successful tests on ATS-3, the first prototype operational geosynchronous weather satellite, SMS-1, was launched on 17 May 1974 and the first operational satellite, GOES-1, on 16 October 1975. Europe and Japan added further satellites in 1977 - Meteosat-1 and Himawari (GMS-1), respectively - and the global network of such satellites was augmented by India's Insat-1A in 1982, Russia's GOMS (Elektro-1) in 1994 and China's FY-2 in 1997 in addition to further US, European and Japanese satellites at regular intervals.

Geostationary weather satellites pose some specific design challenges. The large telescope and camera dominates the satellite to the extent that some early designs were dynamically unstable - in the case of the US's SMS and early GOES series, and of Europe's Meteosat and Japan's initial GMS series, having to eject the apogee boost motor case when empty in order to become dynamically stable.

Current satellites have evolved along two distinct paths, with Europe and China continuing to build spin-stabilised satellites, while the US starting with GOES-8 in 1994, Japan with MTSAT-1R in 2005 and India now use 3-axis stabilised satellites. Satellite mass has risen from 600-750kg for the 1970/80 satellites to the 3.2 tonne GOES-N due for imminent launch as this article is being written.

International collaboration

The world's weather satellites are coordinated under the auspices of the World Meteorological Organisation, itself affiliated to the United Nations. The satellites are coordinated on a purely voluntary basis by members of the Coordination Group for Meteorological Satellites (CGMS). Members include Eumetsat for Europe, the US, Japan, Russia, China and India.

Although the geostationary satellites and systems of the

various CGMS members differ in design, several of their key technical and operational characteristics are coordinated, including:

- data dissemination is interoperable between the systems
- remote data collection platforms are interoperable
- image characteristics are similar
- meteorological products derived from the images conform to agreed standards.

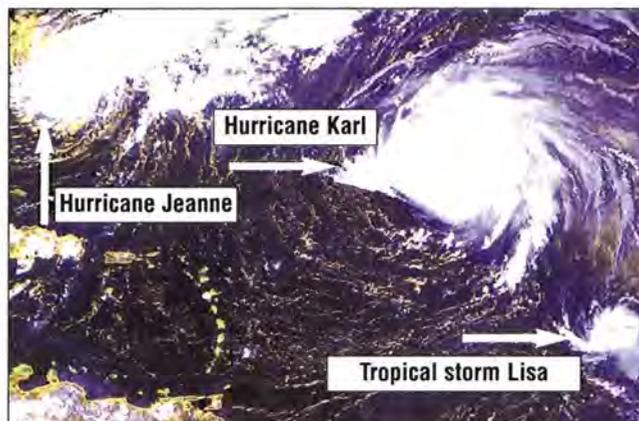
Weather forecasters therefore have access to a truly global data set on a 24 hour a day basis.

Payloads - now and in the future

With one exception, the current geostationary weather satellites capture imagery in four or five visible and IR spectral bands. The imagery has a resolution of 1-5km, the visible imagery being slightly higher resolution than the IR. The US satellites also carry an 18-channel IR sounder, which help to monitor and predict the particularly violent weather events, such as tornados.

The exception referred above to is Europe's Meteosat Second Generation (MSG) series, the first of which was launched on 28 August 2002. MSG images cover 12 spectral channels, similar to the AVHRR images taken by many polar

orbiting systems. The US is now studying the design of a similar system that would follow the current GOES N-Q series. Europe, meanwhile, is studying a Meteosat Third Generation (MTG) concept, which is likely to involve 3-axis stabilised satellites with significant new payload features - first launch would be 10-15 years from now.



Hurricanes Jeanne and Karl and tropical storm Lisa: GOES-12, Sept 21st, 2004 [Credit: NOAA]

Pat Norris is Business Development Manager at UK systems integrator LogicaCMG, and was involved in supply of ground facilities for the Meteosat Second Generation and MTSAT-1R systems.





Galileo satellites will carry Europe's first generative (primary) navigation payloads designed and built by EADS Astrium in the UK

Galileo

Europe's satellite navigation system

The Galileo project is making big promises for the wellbeing of Europe.

By Gerrit Beyer

Sir Arthur Clarke's geostationary orbit is not the only orbit for satellites. As every application has its optimum orbit altitude, inclination and shape, it really is 'horses for courses'. Earth observation satellites are normally in low polar earth orbits; communications and broadcasting satellites are mostly in geo; high latitude communications spacecraft are often in highly elliptical inclined orbits; and navigation satellites are primarily in intermediate circular inclined orbits.

The latest and probably the most advanced of satellite navigation systems is the one proposed by the EU, called Galileo.

Galileo is a joint initiative by the European Space Agency (ESA) and the European Commission (EC) to develop and launch an independent constellation of 30 civil controlled navigation satellites. From 2009, Galileo will enable users to pinpoint their location with high precision and guarantee a service anywhere in the world. Being fully interoperable with, but operated independently from, the US-owned Global Positioning System (GPS), Galileo will provide significantly enhanced accuracy and signal integrity. The new system is also designed to accommodate the demanding requirements for safety-critical applications, for example in the field of air transport, and promises to be a catalyst for transport, telecom and the IT sectors.

Galileo is Europe's largest high-technology project and is expected to contribute substantially to Europe's social and indus-

trial integration. The satellite constellation, consisting of 30 spacecraft, supported by a worldwide network of ground stations, is planned to be fully operational by 2009. The satellites will be positioned in three 56° inclined orbits at altitudes of 22,900 kilometres to provide highly accurate timing signals to support a seamless, global navigation network, complementing the US GPS.

Reaching agreements

In May 2003, the governments of the participating European member states agreed to proceed with the development and validation of the first four satellites of the Galileo system. A preliminary contract for the In-Orbit Verification (IOV) phase was awarded to the European consortium Galileo Industries in December 2004. The IOV phase, jointly funded by the EC and ESA, encompasses the development, manufacture and launch of these four flight models together with the establishment of essential ground segment elements.

Galileo Industries had already signed a contract worth €72m for the Galileo System Test Bed (GSTB V2B) satellite in July 2003, while Surrey Satellite Technologies Ltd took on the smaller GSTB V2A contract. These early prototypes will be precursor and test missions for Galileo and Europe's first satellites entirely dedicated to navigation. Their primary purpose is to secure the global radio frequency filings and, in the case of GSTB V2B,



demonstrate and validate all payload technologies previously developed under the Galileo programme. The first satellite will be launched on a Soyuz rocket in December 2005.

The development and manufacture of the large and highly complex space-based Galileo infrastructure is a stimulating challenge for European industry. The European consortium Galileo Industries was established in 2000 as a joint venture by Europe's leading space companies, with EADS Astrium as its largest shareholder, to act as the industrial prime contractor to deliver the Galileo infrastructure, budgeted at €3.5bn in total. The other Galileo Industries shareholders are Alcatel Space and Thales of France, Alenia Spazio of Italy and the Spanish consortium Galileo Sistemas y Servicios.

Following approval of the system in May 2003, Galileo Industries is rapidly becoming a truly integrated company with its head office in Munich, Germany, responsible for the global system architecture. In 2004, an engineering office was established in Rome, Italy.

EADS Astrium is a principal shareholder and will support the implementation of the Galileo system as per following:

■ EADS Astrium Germany's Ottobrunn site is focusing on the design and development of the space segment and its 30 satellites, and is playing a major role in overall systems engineering and in elements of the mission's ground segment.

■ EADS Astrium UK's Portsmouth site is responsible for the design and manufacture of the complex navigation payload and is also leading the management and system engineering for the ground control segment.

■ In France, EADS Astrium's Toulouse site plays a major role in Galileo's mission ground segment, and

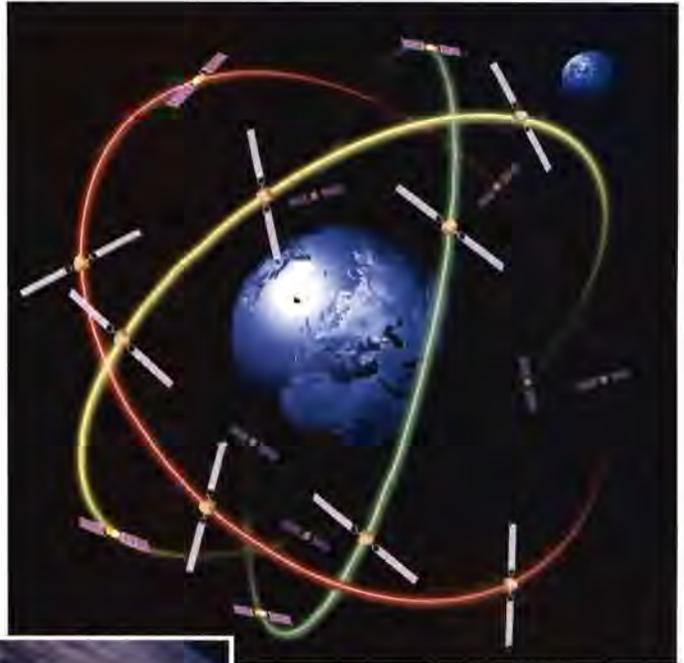
In Spain, EADS Astrium and its affiliated companies are also participating substantially in the programme.

■ In addition, technical experts nominated by EADS Astrium from across all the countries are taking key positions within Galileo Industries to support overall management and system engineering tasks contracted to the joint venture.

Innovative funding

After completion of the in-orbit validation phase, the procurement and operation of the overall system is to be financed through a Galileo concession company on a public-private partnership (PPP) basis. This is the first time that the EC and ESA will adopt the innovative PPP approach to finance a space technology project. The concessionaire will bring together public and private investors from the finance and telecommunications communities together with other interested parties, to procure, deploy, operate and maintain the system and to collect the revenue particularly from the high-integrity value-added services.

In partnership with Inmarsat and Thales, EADS SPACE Services formed the iNavSat consortium to compete for the role of the concessionaire, or Galileo Operating Company, the entity that will deploy and operate the constellation over a 20-year



Galileo will have 27 operational spacecraft and three spares in three 56° inclined circular orbits



Between six and eight Galileo satellites could be launched on each Ariane 5

period. The Galileo Joint Undertaking (GJU) announced in June 2005 its acceptance of a joint bid by iNavsat and Eurely. Both teams have now jointly begun negotiations with the customer, which are expected to last at least until the end of the year.

In February 2003, a call for expressions of interest was launched to allow private sector companies to apply and prepare for the call for tenders.

In October 2003, the Joint Undertaking launched a call for tenders for the one, two (or possibly more) consortia interested in operating and marketing Galileo.

In February 2004, three consortia were selected as bidders. This included the iNavSat Consortium with EADS SPACE Services. In parallel with these consortia, the Joint Undertaking prepared the contents and the scope of the concession contract. The Commission will remain responsible for the public service requirements i.e. the quality, availability, integrity and continuity of the services and the safety requirements.

After the withdrawal of one of the consortia, the GJU was left to select its preferred candidate from the remaining two. In May 2005, unable to decide between the two offers, the GJU opted to pursue a joint approach and in June accepted the combined iNavsat Eurely bid. The combined bid "showed a significant reduction in the financial contribution from the public sector and an increase in the foreseen commercial revenue". This decision should now allow the concessionaire to be fully operational in time and to effectively plan for the deployment phase.

Market conditions

Satellite navigation and precise timing technology is increasingly used in the industrial, public and consumer sectors. The overall decrease in cost and size of the receivers will continue to drive market development towards high volume applications and increasing levels of integration of satellite navigation tech-



nologies with communications networks, geographic information and complete transport systems will result.

The global turnover for satellite navigation products in 2001 amounted to €15bn and is expected to rise to €140bn by 2015. In 2001, approximately 30% of the global revenues were generated in Europe.

As an enabler, Galileo can demonstrate space technology and can be an innovative driver for user- and consumer-oriented solutions, as entrepreneurs continue to develop new applications to serve the growing market. It is estimated that satellite navigation technology will secure or create in excess of 100,000 jobs across Europe.

Satellite navigation and positioning and timing services are a vital element in many socio-economic sectors. Management and control of all modes of transport, communications networks and many other utilities are expected to benefit from satellite navigation.

By integrating positioning information with communications, typically in handheld terminals and mobile phones, Galileo will enable many new location-based services to be introduced. Users will not only be provided with the exact details of their position, but will also be able to receive on-demand information about nearby restaurants, hotels, petrol stations and others. This combined location/transmission technology will also be of great benefit for personal safety as emergency services will be able to accurately locate callers who are unable to give their precise positions.

Galileo has been designed to serve all transport domains: air, sea, road and rail. Applications include route planning, traffic and fleet management, in-car navigation, driver assistance, congestion and collision warning, and management of emergency situations in the air, on land and at sea. Thus, Galileo will lead to increased efficiency, safety and security and will directly contribute to reduced traffic congestion and travel times.

Galileo's high-integrity global timing system, based on highly accurate atomic clocks, will facilitate the interconnection and synchronisation of a wide range of services from electricity sup-

ply and telecommunications networks to complex banking systems. The introduction of combined position and timing information will also make data encryption and electronic signatures for e-commerce even more secure. Insurance companies will be able to use the technology to trace and follow high value goods.

In addition to the navigation and positioning of vessels, Galileo signals can help to accurately locate and monitor fish resources and can assist the authorities in ensuring that vessels operate in their designated areas. Galileo can also contribute significantly to crop yield monitoring and precision farming, allowing effective resource management to safeguard the agricultural environment.

Various applications are currently being implemented to combat vehicle theft, monitor offenders on bail and patrol maritime borders against illegal trafficking. Satellite navigation can also be used to keep track of registered cargos and dangerous goods. Tracking and tracing applications will increase the efficient use of resources in large-scale security operations to ensure public safety and security at events such as the Olympic games or summit meetings.

The crown jewels

Galileo is a highly significant programme for the whole of Europe as it delivers valuable supplementary means of independence from GPS. It offers a huge market potential and its advanced technology is a definite catalyst for further innovation in Europe.

Galileo will be the first radio satellite navigation system fully under civil control, securing maximum service availability and reliability.

The system will allow, also for the first time, the implementation of integrity alerts and will enable users to enter into a contractual service agreement with the Galileo operator.

Gerrit Beyer is Business Development Manager for Satellite Navigation Systems at EADS Astrium Ltd.



EADS Astrium Ltd has already built and delivered the payload for GSTB V2B, due for launch by early 2006





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“TO INVESTIGATE THE REACH AND
IMPACT OF HUMAN IMAGINATION,
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The Foundation was created in 1983 as part of World Communications Year and is dedicated to promoting the extraordinary contributions made by Arthur C. Clarke to the world - as a scientist, science fiction writer and renowned 'futurist'. Through Clarke, we have a door, slightly ajar, inviting us into an awesome adventure. In him, the human imagination has traveled far in many forms. How does that happen? How far can it go? How does it converge in single individuals, enabling insight, creativity and brilliant results along multiple paths? How does the mind become motivated at just the right moment in history? How can nations identify and enhance that creativity and expose it to avenues of ethical progress?

To search for answers to those questions and more, the mission of the Arthur C. Clarke Centre at the University of Nevada, Las Vegas, will be to investigate the reach and impact of human imagination: to explore its sources; to weigh its consequences in human development, including in the advancement of science, literature, and the arts; to examine and predict how creativity intersects with historical moments; to discover and encourage individuals of all nations and ages, gifted with exceptional insight; and to match those capabilities to humanity's most critical responsibilities.

For further information on the Foundation and its activities, see:

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Scientific exploration using

Science inspires us; exploration of the Earth from space allows looking at the planet globally; while space science gives an outward look - toward the stars and other worlds. The goal is to observe, question, measure and monitor in order to understand, to predict and manage.

By Bernhard H Foing

The ability to launch spacecraft has changed our lives. The greatest innovations have been new views of the world. Scientific exploration of the Earth from space has been a key to better understanding of our home planet: its interior, surface, magnetosphere, atmosphere and climate, resources, active Earth, global biosphere and so on.

Earth observation satellites remain in place for long periods of time, so they can highlight gradual environmental changes. Archived satellite data shows us the steady clearing of the world's rainforests, an apparent annual rise in sea level and depletion of the ozone layer by atmospheric pollution. This long-term monitoring of the Earth's environment enables a reliable assessment of the global impact of human activity and the likely future extent of climate change.

As part of ESA's Living Planet Programme, the Earth Explorer missions encompass a new strategy for observing the Earth from space, designed to address critical and specific science issues using innovative technology. There are currently six Earth Explorer missions:

CryoSat (launch scheduled for September 2005) will determine variations in the thickness of the Earth's continental and marine ice cover, then test and quantify the prediction of diminishing polar ice due to global warming.

GOCE (Gravity and Ocean Circulation Explorer, planned launch 2006) will provide the data-set required to accurately determine global and regional models of the Earth's gravity field and geoid. This will advance research in areas of ocean circulation, physics of the Earth's interior, surveying and sea-level change.

ADM-Aeolus (Atmospheric Dynamics Mission, planned launch 2007) will provide novel global wind-profile observations and information to improve weather forecasting.

SMOS (Soil Moisture and Ocean Salinity, planned launch 2007) will provide global maps of soil moisture and ocean salinity to increase understanding of the Earth's water cycle and contribute to climate, weather and extreme-event forecasting.

Swarm (planned launch 2009) is a constellation of three satellites to study the dynamics of Earth's magnetic field to gain new insights into its interior and climate.

EarthCARE (Earth Clouds Aerosols and Radiation Explorer, planned launch 2012) is a joint European-Japanese mission that aims to improve the representation and understanding of the Earth's radiative balance in climate and numerical weather forecast models.

In early 2005, ESA released the latest opportunity for scientists to submit ideas for future Earth Explorer missions.

Global monitoring for environment and security

Global monitoring for environment and security (GMES) is led by the European Commission (EC) and ESA to support Europe's goal of sustainable development and global governance, in support of environmental and security policies. GMES supports many service elements, including land cover and for-

est monitoring, the marine, coastal and polar environments, maritime security, risk management, food security, atmospheric monitoring and humanitarian aid.

Planetary monitoring requires global international co-operation. An example is the use of Earth observation science to improve current water management practices (e.g. in Africa or in Asia), enabling the identification and sustainable exploitation of underground aquifers, better management of wetlands, enhancing food security and epidemiology research into links between outbreaks and environmental factors. Earth observation can be developed as a territorial management tool, enabling improved development planning, resource mapping and mitigation of natural hazards, therefore, protecting the habitability of our home planet.

We also need to understand where we are in space and time in the universe. The night sky glows in microwaves with the very first light ever released into space, some 100,000 years after the Big Bang. Space telescopes are time machines, allowing us to use this fossil light to see the birth and development of the young universe: the Big Bang, first stars and galaxies, stellar and galactic evolution and the origins of solar systems.

The violent conditions in the early universe or at the edge of black holes are a laboratory in which to study astroparticle physics at energies beyond laboratory accelerators and physics beyond quantum and Einstein relativity laws. Some future space missions will question the laws of fundamental physics and the universe. One will test the equivalence between an inertial mass and gravitational mass. Another mission, such as LISA, will track - for the first time - the elusive 'gravitational waves' predicted by General Relativity, giving birth to a new kind of astronomy that no longer looks at light, but detects tiny ripples (less than 1nm over million km) of space-time due to gravity.

Solar system exploration

Solar system exploration focuses on understanding the Earth's relationship with the Sun and other planets. Study and monitoring of the Sun is necessary to assess our analysis of the Earth's changing climate. The Sun's light helps to maintain our world's temperature, but it also produces a magnetic field that shields us from deadly cosmic rays from deep space.

The discoveries of proto-planetary disks around other stars and the detection to date of more than 150 Jupiter-type exoplanets provide evidence that formation of extra-solar systems may be common throughout the universe. In coming years, the COROT mission, planned launch 2007, will be able to detect both giant and terrestrial planets (super Earths) during 150 days of continuous high-precision, simultaneous, photometry of 5000 stars. Nasa's Kepler mission will look for transits by Earth-sized planets in Earth-like orbits. ESA's Gaia astrometric mission, planned for launch in 2011, will measure the stellar reflex motion to detect tens of thousands of jovian exoplanets.

Intriguing presence of organic molecules

Biogenic elements such as H, C, N, O, S, and P are widespread



space technology

in our galaxy. The existence of organic molecules in interstellar and circumstellar environments, their incorporation into potential planet-forming disks and subsequently into solar system material has been successfully investigated over the last decade. Extraterrestrial delivery of organic matter and water by comets and asteroids may have triggered the emergence of life on Earth and possibly on Mars. Common interest in the origin and distribution of life in the universe has led to a new scientific discipline: astrobiology. Astronomical telescopes and space missions contribute to the investigation of possible habitats in our solar systems, the search for exoplanets and the link between falling extraterrestrial matter and the origin of life on Earth. Key astrobiology questions being addressed include:

- How do solar and stellar systems form? (ISO, Herschel, SMART-1, Rosetta, Bepi-Colombo, Gaia);
- Geological evolution of terrestrial planets (living planet, Mars-Express, SMART-1, Venus-Express, Bepi-Colombo)
- Interstellar complex organic chemistry (ISO, ISS/EXPOSE, Herschel, Rosetta)
- Co-evolution of Earth-Moon, effects of impacts on life (SMART-1, Bepi-Colombo)
- How to detect other solar systems and habitable zones (COROT, Gaia, Darwin)
- Early Earth and alternative environments (Huygens/Cassini, Mars-Express, Venus-Express)
- Signature of biosphere and photosynthesis (Earth Explorer missions, Darwin)
- Water on Mars (orbiter instruments on Mars Express and Exomars lander)
- Search for organics and life on Mars (Mars Express, ExoMars lander and future Mars sample return)
- Astrobiology in low-Earth orbit (survival of organics in space and human studies on ISS)
- Terrestrial life beyond the Earth (life sciences and human missions on the Moon and Mars)

Several space missions investigate extraterrestrial organic chemistry and search for extra-solar systems and traces of life. ESA's Infrared Space Observatory ISO (1995-1998) has revolutionised our understanding of gas and dust in interstellar and circumstellar space. Nasa's SIRTIF mission is continuing this research, and the airborne observatory Sofia will be launched in the near future.

ESA's Herschel Space Observatory (due to be launched in 2008) will be the only space telescope covering the far infrared to sub-millimetre range of the spectrum (from 80 to 670 microns). It will be located 1.5 million km from Earth. For at least three years, Herschel will contribute to astrobiology by studying the formation of early galaxies, stars and planets.

The James Webb Space Telescope, JWST (NASA/ESA) will be able to penetrate the dusty envelopes around newborn stars using the infrared part of the spectrum. JWST will also study small objects, brown dwarfs and Jupiter-sized planets that are not mas-

sive enough to become stars. JWST's high resolution will also make it possible to see how extra-solar planetary systems form.

Placing Earth into context

By studying alien Earth-like worlds, such as the Moon, Mars, Venus, or Jupiter's or Saturn's moons, we can place our own Earth in context.

How do rocky planets form and grow? Models assume accretion from embryo planetesimals from different parts of the solar system. The Moon and Mercury carry a physical and chemical record of the early bombardment of the inner solar system not visible on Earth. The physics of impact processes can be investigated on different scales, making use of remote sensing, in-situ and sample data.

The Nasa/ESA Cassini-Huygens mission continues to explore Saturn and its rings. In January 2005, the European Huygens probe measured the properties of Titan's atmosphere, including organic molecules and nitriles, thought to resemble those of the young Earth. High-resolution images provided evidence of a methane river cycle on Titan's surface.

It will also be interesting to study the Jovian system for clues on the formation of the solar system. Jupiter's moon Europa probably hosts a subsurface water ocean beneath its outer ice crust. Europa seems to have an internal energy source provided by tidal friction through its interaction with Jupiter, which could keep water in liquid state below the crust and would, therefore, provide key ingredients for life. This would make a great laboratory for deep oceanic exploration.

ESA's Rosetta mission launched in March 2004 is planned to rendezvous with comet Churyumov-Gerasimenko (CG) in 2013-2015. More than 20 instruments on the orbiter and lander will obtain data on cometary origin and the interstellar-comet connection, yielding insight into the origin of our solar system. Rosetta will study the comet's nucleus and environment for two years, with distant observations leading to close observations (~ 1km distance). Comets are relics of planet-formation processes in our solar system and are thought to contain the most pristine chemical record, since they spend most of their lives in the cold outer part of the solar system. Knowledge of their composition is a key astrobiological objective in order to understand what material was delivered to the early planets by cometary impacts.

Earthly connections

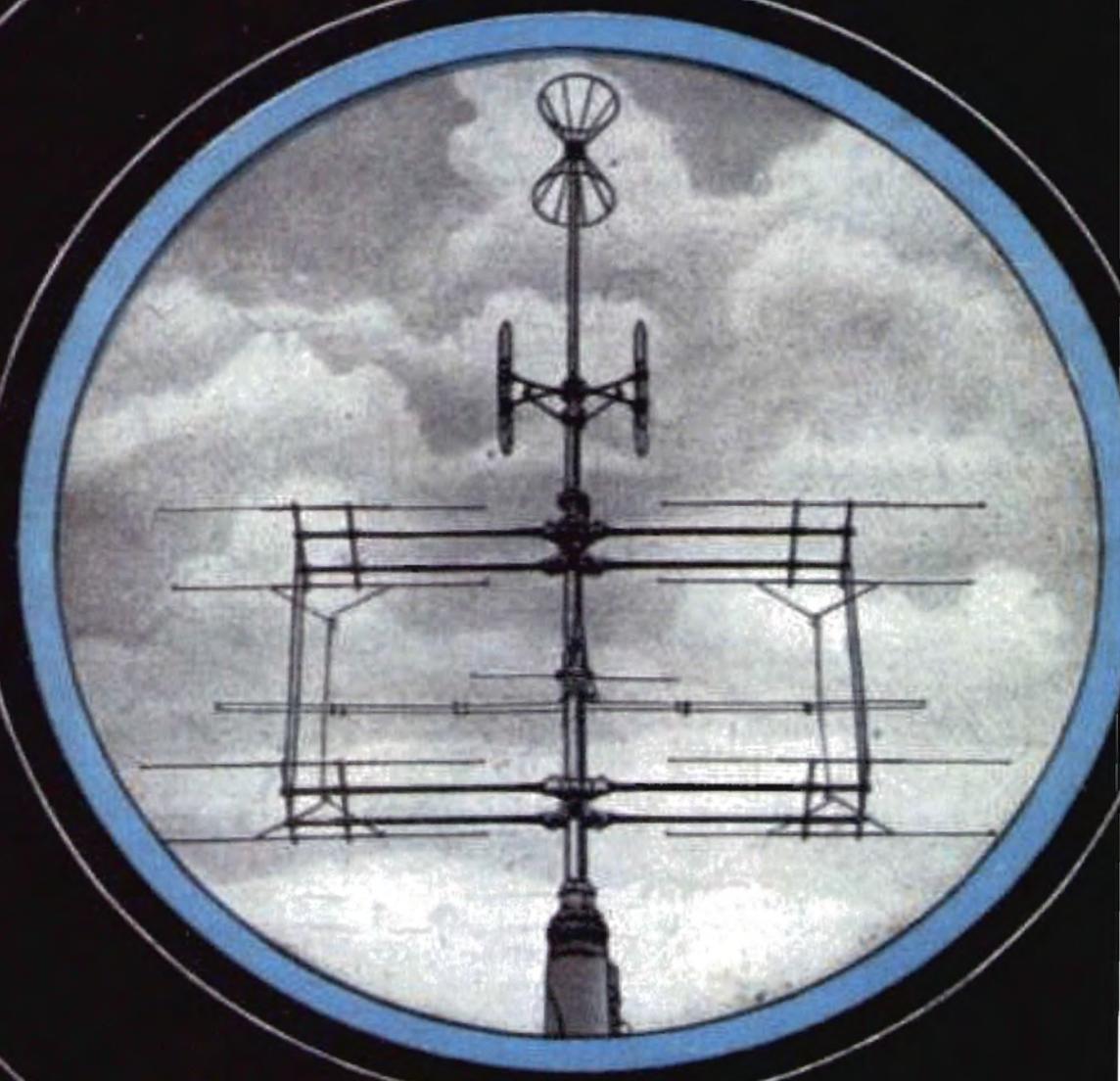
We have to nurture awareness of the universe/solar-system/earth/life/human-society connection. To bring people to space, scientific, technical, economic, legal issues should be presented and debated with the public, to engage citizens in key questions relevant both for space exploration and to keep alive the values of our Earth.

Bernard H. Foing is Chief Scientist at the ESA Science Directorate.



Wireless World

RADIO and ELECTRONICS



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1/6

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IN THIS
ISSUE:

RADAR AND THE INDUSTRY

For high-power performance, device designers are turning to wide-bandgap materials, in particular silicon carbide (SiC) and gallium nitride (GaN), which have the potential to increase the power performance of MMIC power amplifiers by a factor of 10. These materials offer much higher breakdown fields and saturated electron velocities than GaAs, as well as far superior thermal conductivities. As a result, power devices based on these materials are expected to operate at high frequencies with high power density and efficiency, while also being able to withstand large voltages and currents.

The potential of these wide-bandgap semiconductors has been recognised for some time, but the materials and processing technologies have only recently reached a level of maturity where device performance can be tested and demonstrated experimentally. Progress in this area has largely been driven by a strong market for light-emitting diodes and lasers based on GaN and AlGaN grown on SiC substrates, and these developments are now feeding through to RF device applications.

The report points out that substrate technology has been a particular challenge in the development of wide-bandgap electronic devices, since the high melting points of these materials prevent them from being produced in high volumes using the techniques traditionally used for silicon and GaAs.

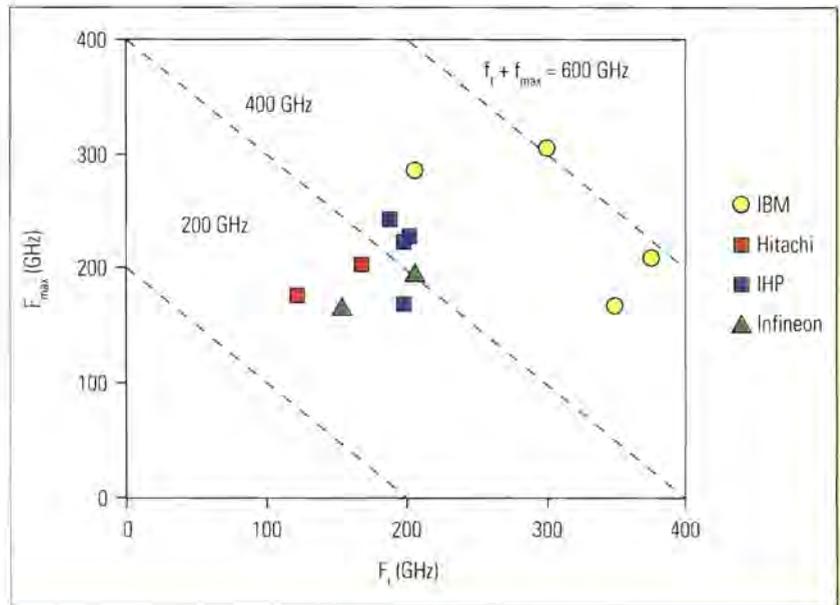
Wide bandgap, mature substrate

Of the wide bandgap materials, SiC offers by far the most mature substrate technology, although cost and reliability issues still remain.

SiC wafers are most commonly grown using a physical-vapour transport process, in which extremely pure SiC source material is evaporated onto a seed substrate. To obtain high quality substrates, it is critical to control the thermal gradients within the deposition chamber accurately and to minimise the presence of electrically active impurities such as boron and nitrogen. Another issue is that SiC naturally forms more than 200 different crystal structures, but only two of these – 4H and 6H – are useful for electronic devices. As a result, the growth conditions must be controlled to ensure the formation of the required crystal type.

Three-inch semi-insulating SiC substrates are now commercially available from Cree and other companies for about \$700 each, compared with less than \$10 for six-inch GaAs wafers. Efforts are also continuing to prevent the formation of so-called micropipes during crystal growth, which reduce the usable area of the wafer and so decrease device yields.

To achieve operation at high frequencies, GaN transistors are usually grown on SiC substrates to deliver cut-off frequencies of up to 110GHz. GaN has primarily been used to produce AlGaN/GaN



HEMTs, but there has also been some work on HBTs, HFETs and MESFETs. Another option that is now being pushed by Nitronex of the US is to grow GaN devices on low-cost silicon substrates. This has so far been impossible because of the large lattice mismatch between GaN and silicon, about 18%, as well as a significant difference in thermal properties, which strains the interface between the two materials. Nitronex has solved these problems by growing a buffer layer between the silicon wafer and the GaN epi-layer to absorb and dissipate the tension. The company claims to have developed a stable, uniform and repeatable processing technology based on standard silicon processes and now offers four-inch epi wafers on a commercial basis.

Most GaN results to date have been measured on discrete devices and the development of a GaN MMIC technology remains at an early stage. However, several groups have built GaN MMICs that show promising performance and Cree offers prototyping services on three-inch SiC wafers for research groups wanting to test the performance of the technology.

Alongside these innovations at the chip level, more detailed and accurate simulation techniques are allowing circuit designers to understand and predict the complex electromagnetic behaviour that arises in MMICs operating at high frequencies. This helps to optimise the performance of mm-wave MMICs and reduce the risk associated with developing a new fabrication process.

Cost factors

Despite all that, cost remains a major obstacle for commercial applications of mm-wave MMICs. Further optimisation of mm-wave circuit designs are

The latest results for SiGe HBTs produced by IBM, Hitachi, IHP and Infineon show impressive F_t/F_{max} values

likely to reduce both the chip area and cost of MMIC solutions, while MMIC foundries claim that they could introduce price structures that would allow significant rate reductions for high-volume orders. But the report reveals that the biggest issue remains the cost of packaged mm-wave transceivers, which are often about five to six times as expensive as bare MMIC die. Only by reducing packaging and assembly costs can the mm-wave community hope to achieve high-volume sales of MMIC devices and transceivers.

This critical objective requires innovation in two key areas:

Material cost: most existing MMIC packages are made from milled metal, which is both expensive and heavy. Package designers are now investigating alternative materials, including ceramics, plastics and polymers. These low-cost, lightweight materials have already proved successful at low frequencies and some, in particular low-temperature co-fired ceramic (LTCC) materials, are showing considerable promise at higher frequencies. Multichip modules, which incorporate several MMICs in a

single package, also offer significant potential for reducing the size, weight and cost of complete mm-wave subsystems.

Automated assembly: current processes for assembling mm-wave MMIC-based transceivers are labour intensive and hand-tuning is often required to achieve the desired performance. Techniques now being investigated to enable the mass production of mm-wave MMIC modules include flip-chip bonding to connect the MMIC to the subassembly reliably and repeatably, and the introduction of automated pick-and-place machines to position the MMICs in a module and for automated bonding. The trend towards multichip modules will also lead to reduced assembly costs.

These developments will be crucial to achieving affordable MMIC solutions at mm-wave frequencies. Good communications between the foundries, the module makers and the system manufacturers will play a critical role in helping suppliers to better meet the needs of their customers and, in so doing, reduce unit costs, deliver the required performance and speed up time-to-market.

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How to: dismantle a PC

Taking a computer apart is easy enough
Boris Sedacca shows you how...



Dismantling

The screws of the PC's case are at the side panels (see Figure 1).



Figure 1: Rear view of a PC case

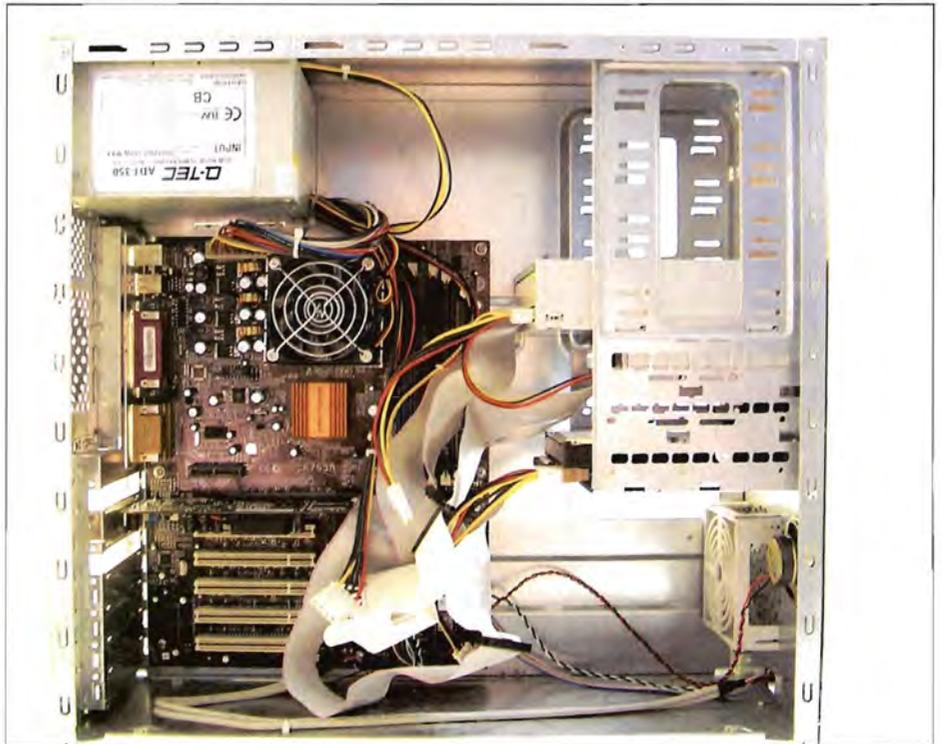
The case shown above is a midi tower case, with bags of room to work in. If you're working with a mini tower, you might find a flexible extension useful, as shown in Figure 2.



Figure 2: Tools useful for dismantling PCs

When you have unscrewed the side panels, the inside of the PC should look as in Figure 3.

Figure 3: Inside of a PC case



There are many types of cases on the market. The motherboard complies with the specifications for the ATX system case. The board can support one floppy diskette drive and four enhanced IDE drives. Ensure that your case has sufficient power and space for all the drives that you intend to install.

Most cases have a choice of I/O templates in the rear panel. Make sure that the I/O template in the case matches the I/O ports installed on the rear edge of the motherboard. This motherboard has an ATX form-factor.

The first component to unscrew is the power supply (top left in Figure 3). The

screws for this are usually located at the rear of the case, near the top of where the side panel screws were removed.



Figure 4: Power supply

You'll have to be particularly careful when removing the CPU, heat sink and fan assembly. **Figure 5** shows a spring lever that releases the heat sink and fan.

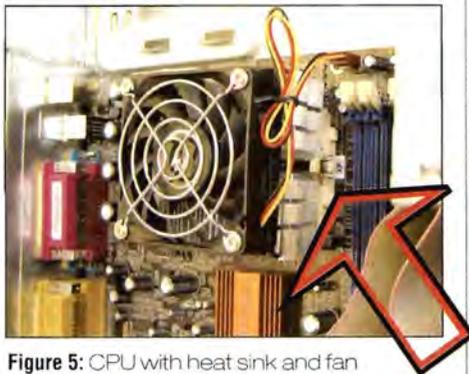


Figure 5: CPU with heat sink and fan

You will need a flat-head screwdriver for this – as you push down, you need to lever out the clip to release it. The fan has leads with a connector that plugs into a matching socket on the motherboard for supplying power.



Figure 6: Heat sink and fan – outside the box

Now you can see the CPU package sitting in its zero insertion force (ZIF) socket on the motherboard. This is an AMD Athlon. The big messy blob of white

thermal paste in **Figure 7** almost covers the CPU chip.



Figure 7: CPU in a ZIF socket with a visible white thermal paste

The lever needs to be raised as shown in the photo below in order to release the CPU package. This particular socket is known as Socket A, or Socket 462 for the number of holes corresponding to the number of pins on the processor package. Note that there is a hole missing on two of the corners to make it impossible to fit the processor the wrong way around.

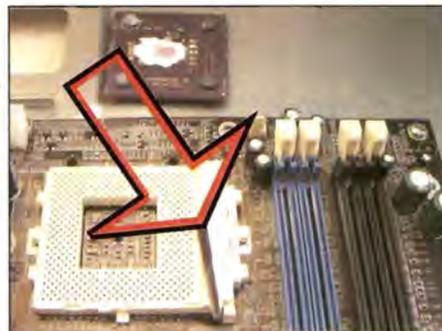


Figure 8: Another take of the board

Then you need to remove the AGP (Advanced Graphics Port) as well as other cards, including the AMR (Audio Modem Riser) and PCI (Peripheral Components Interconnect) cards. The motherboard has five 32-bit PCI expansion slots, one AGP slot and one AMR slot.



Figure 9: AGP card

The AMR slot is an industry standard slot that allows for the installation of a special audio/modem riser card. Different territories have different regulations regarding the specifications of a modem card. You can purchase an AMR card that is approved in your area and install it directly into the AMR slot.

The screw for each card is near the bottom of the case where the various card slots are located on the motherboard.

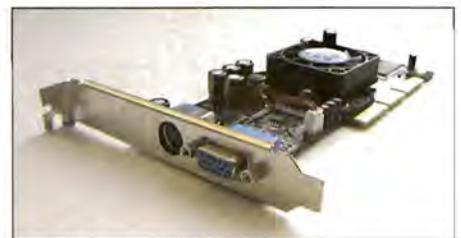


Figure 10: AGP card outside the box

Next, you need to remove the various drive cables, first from the motherboard sockets and then from the drives' sockets. This is not as easy as it looks, particularly where the socket has securing lugs, (see **Figure 11**) where the diskette cable goes into the motherboard socket. The motherboard has two sockets for a primary and secondary IDE channel interface (IDE1 and IDE2).

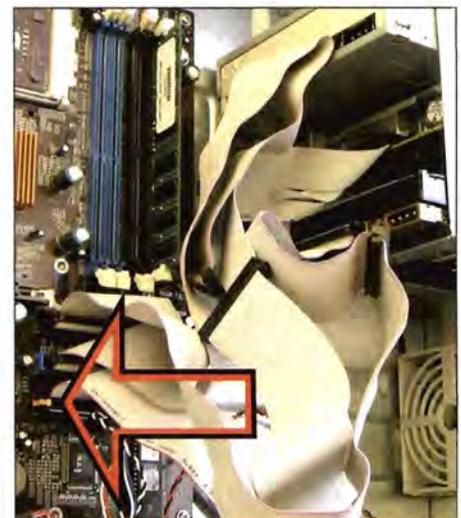


Figure 11: The amazing 'maze' or drive cables

With the drive cables removed, you should now see (from top to bottom) the CD drive, the diskette drive and the hard disk drive. There should be at least one mounting screw on each side of the CD drive to avoid vibration, and although some people mount the diskette and hard

disk drives with only one single screw, this is not best practice.



Figure 12: A 'top to bottom' view of the drives

The CD drive will come out through the front bay of the case by first levering out the plastic bay cover with a screwdriver, while the other drives are removed from inside the case.

Then you need to remove the memory from its slot – this should be easy because there are usually levers on both sides of any memory socket. There is also a notch or two that prevents you from putting memory back into a slot the wrong way around. The motherboard has two 168-pin DIMM slots for SDRAM memory modules and two 184-pin DIMM slots for DDR memory modules.



Figure 13: Drives and memory

Finally, you need to disconnect all the remaining case leads from the sockets on the motherboard. Some features are implemented by cabling connectors on the motherboard to indicators and switches on the system case, and to the speaker (black/red cable). These include:

- Hard Drive Activity LED
- Power /Sleep/Message Waiting LED
- Reset Switch
- Power Switch



Figure 14: Case leads

Provided it is supported by the motherboard (this one does), some cases may have optional front-panel USB ports as shown in **Figure 14** with the dual white leads and/or front-panel audio sockets for microphone and headphone.

The front panel microphone/speaker out header on the motherboard allows the user to connect a microphone and speakers or headphones from the front of a case, although this case does not provide leads for it.

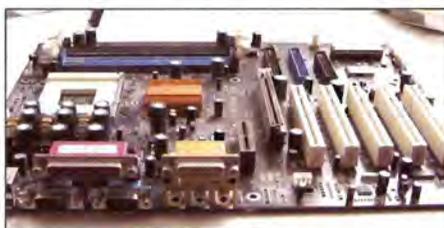


Figure 15: Elite K7S5A motherboard

At last you can remove the screws securing the motherboard to the case.

The Elite K7S5A motherboard seen in **Figure 15** has a Socket-A processor socket for the type of AMD K7 processors. You can install any one of these processors on the motherboard. The motherboard supports front-side bus speeds of 200/266MHz.

This motherboard uses the SiS 735 chipset, which supports a 4x specification AGP slot for graphics display, DDR interface and Ultra DMA 33/66/100 function. The motherboard has a built-in AC97 codec, provides an AMR slot to support audio and modem applications, and has a built-in 10BaseT/100BaseTX network interface.

In addition, the main board has an extended set of ATX I/O ports, including PS/2 keyboard and mouse ports, two

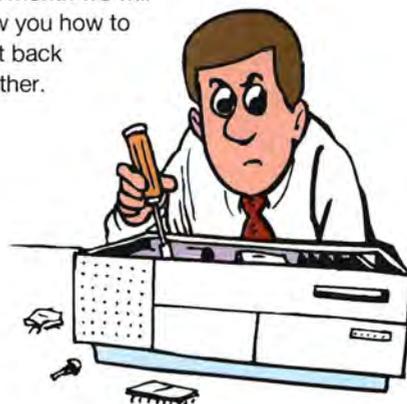
USB ports, a parallel port and two serial ports. Two extra USB ports can be added using the Extended USB module that connects to the motherboard. The board is ATX size and has power connectors for an ATX power supply.



Figure 16: The standoffs for mounting the motherboard

Figure 16 shows the bare case with the standoffs required to mount the motherboard. Most cases have several screw holes for standoffs that correspond to the holes on the motherboard.

That's it. You are now ready to work backwards and re-assemble the PC. Next month we will show you how to put it back together.



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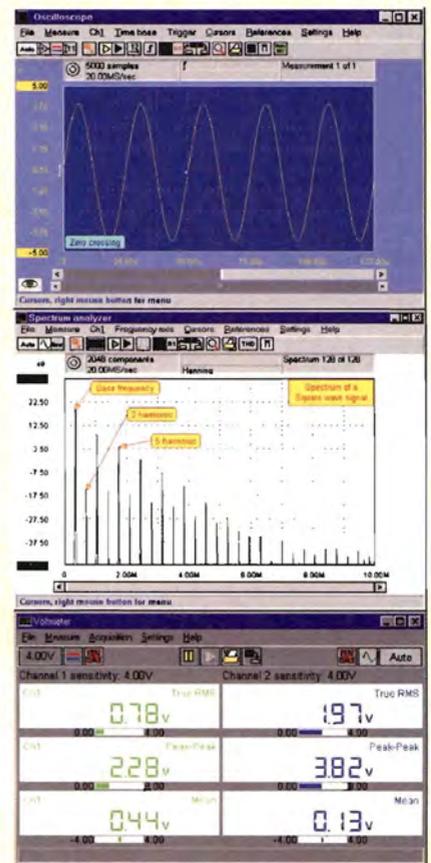
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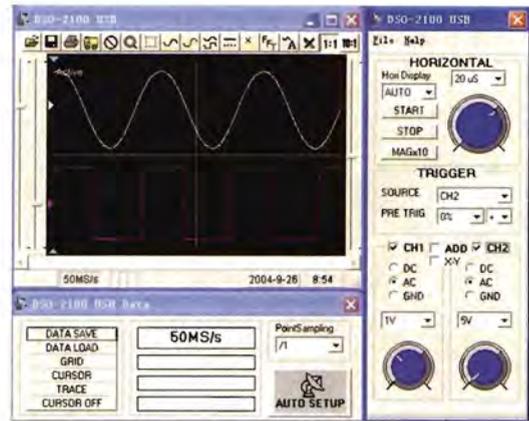
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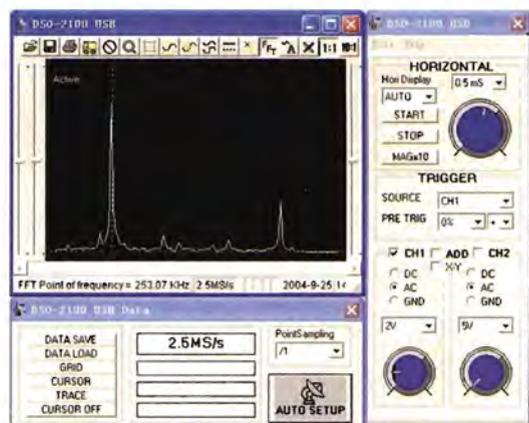
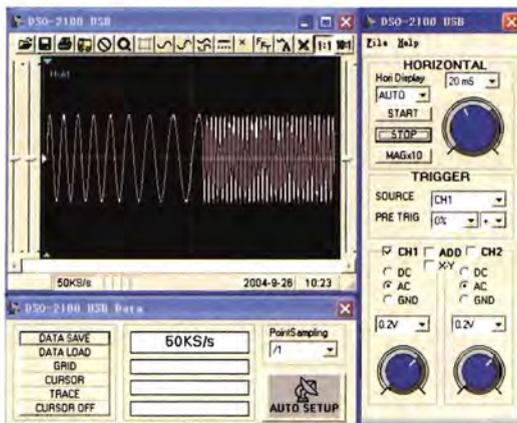


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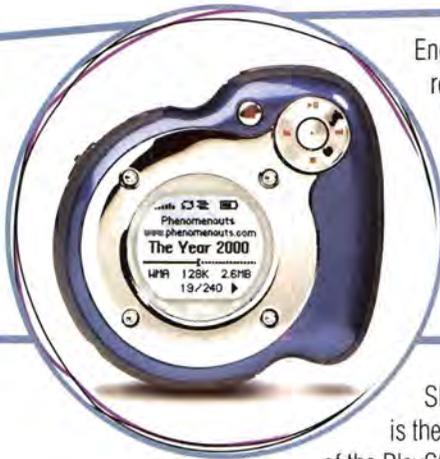
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Engineered for sports enthusiasts, the Rio Forge MP3 player incorporates ruggedness and durability required for highly physical activities, bringing an end to music skips.

The device includes sports clip earphones, a stopwatch, lap timer and a sports case with armband, so that the player won't get 'jogged' around as you do.

Rio Forge comes with 512MB of memory, as well as an expansion memory slot that lets you add up to an additional 1GB if you wish. With fast music-transfer abilities and a simple management system you will get an ease of use. **Around £129**

www.rioaudio.com

Sleek and sexy, the PSP is the first portable member of the PlayStation family, allowing you to play games, listen to music, watch videos etc, all from one compact machine. It features a 4.3", widescreen TFT LCD that displays on a 480 x 272 pixel high-resolution screen, and comes complete with a range of input/output connectors such as USB 2.0 and 802.11b Wireless LAN. Users can easily connect to the Internet and play online via a wireless network of up to 16 people. Expect a broad range of digital entertainment content to be distributed on Sony's new Universal Media Discs (UMD). This high-capacity optical disc is the next-generation compact storage media, and although only 60mm in diameter, it can store up to 1.8GB of digital data. **Around £179**

www.yourpsp.com



The first of its kind, the iPlayer+, brings together all aspects of digital television into one set-top box; including high-end functionality such as SMS services through your television, with Wi-Fi compatible video and audio streaming from portable or PC devices. With the optional Phantom+, the iPlayer+ also becomes a personal video recorder. With multiple outputs in audio and video, the iPlayer can be used as a central hub for your entertainment centre, feeding directly to or from a standard PC and also offering future services such as video on demand.

Around £89.99

www.iplayer.co.uk

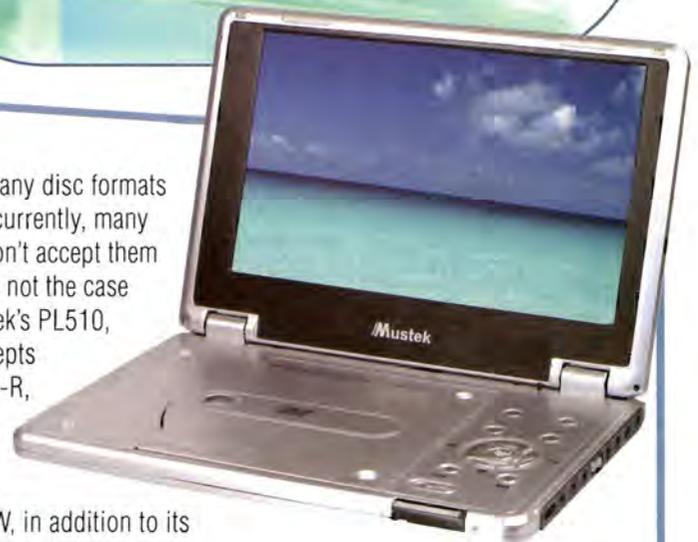
With so many disc formats available currently, many players won't accept them all. This is not the case with Mustek's PL510, which accepts DVD, DVD-R, DVD+R, DVD+RW, CD, CD-R and CD-RW, in addition to its SD/MMC card slot reader.

This player offers all you could possibly want from portable entertainment, allowing you to watch video, listen to music, or even show off your holiday photographs on the flight home. Its design is great, with a sleek look, 10", colour, TFT LCD, widescreen display and compact carry-case. It has built-in stereo speakers, but if you can't sleep whilst the others doze off, you can plug in two sets of earphones to keep you entertained quietly.

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PICmicro: Microcontroller CCP and ECCP

TIP 1: Measuring the period of a square wave

- 1: Configure control bits CCPxM3:CCPxM0 (CCPxCON<3:0>) to capture every rising edge of the waveform.
- 2: Configure the Timer1 prescaler so Timer1 will run TMAX1 without overflowing.
- 3: Enable the CCP interrupt (CCPxIE bit).
- 4: When a CCP interrupt occurs:
 - a) Subtract saved captured time (t1) from captured time (t2) and store (use Timer1 interrupt flag as overflow indicator).
 - b) Save captured time (t2).
 - c) Clear Timer1 flag if set.

The result obtained in 4a is the period (T).

Note: TMAX is the maximum pulse period that will occur

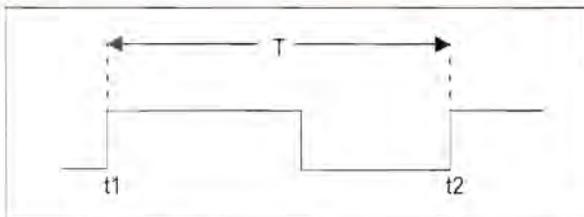


Figure 1: Period

TIP 2: Measuring the period of a square wave with averaging

- 1: Configure control bits CCPxM3:CCPxM0 (CCPxCON<3:0>) to capture every 16th rising edge of the waveform.
- 2: Configure the Timer1 prescaler so Timer1 will run 16 TMAX1 without overflowing.
- 3: Enable the CCP interrupt (CCPxIE bit).
- 4: When a CCP interrupt occurs:
 - a) Subtract saved captured time (t1) from captured time (t2) and store (use Timer1 interrupt flag as overflow indicator).
 - b) Save captured time (t2).
 - c) Clear Timer1 flag if set.
 - d) Shift value obtained in Step 4a right four times to divide by 16 – this result is the period (T).

Note: TMAX is the maximum pulse period that will occur.

The following are the advantages of this method as opposed to measuring the periods individually:

- Fewer CCP interrupts to disrupt program flow
- Averaging provides excellent noise immunity

TIP 3: Measuring pulse-width

- 1: Configure control bits CCPxM3:CCPxM0 (CCPxCON<3:0>) to capture every rising edge of the waveform.
- 2: Configure Timer1 prescaler so that Timer1 will run WMAX without overflowing.

- 3: Enable the CCP interrupt (CCPxIE bit).

- 4: When CCP interrupt occurs, save the captured timer value (t1) and reconfigure control bits to capture every falling edge.

- 5: When CCP interrupt occurs again, subtract saved value (t1) from current captured value (t2) – this result is the pulse-width (W).

- 6: Reconfigure control bits to capture the next rising edge and start the process all over again (repeat steps 3 through 6).

TIP 4: Measuring duty cycle

The duty cycle of a waveform is the ratio between the width of a pulse (W) and the period (T). Acceleration sensors, for example, vary the duty cycle of their outputs based on the acceleration acting on a system. The CCP module, configured in capture mode, can be used to measure the duty cycle of these types of sensors.

Here's how:

- 1: Configure control bits CCPxM3:CCPxM0 (CCPxCON<3:0>) to capture every rising edge of the waveform.

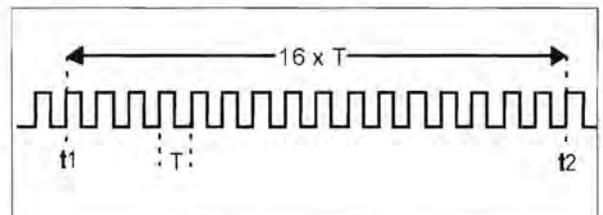


Figure 2: Duty cycle

- 2: Configure Timer1 prescaler so that Timer1 will run (1) without overflowing.

- 3: Enable the CCP interrupt (CCPxIE bit).

- 4: When CCP interrupt occurs, save the captured timer value (t1) and reconfigure control bits to capture every falling edge.

Note: TMAX is the maximum pulse period that will occur.

- 5: When the CCP interrupt occurs again, subtract saved value (t1) from current captured value (t2) – this result is the pulse width (W).

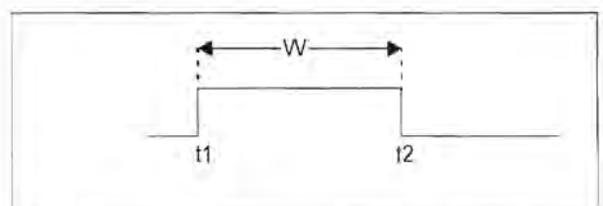


Figure 3: Pulse width

- 6: Reconfigure control bits to capture the next rising edge.
- 7: When the CCP interrupt occurs subtract saved value (t1) from the current captured value (t3) – this is the period (T) of the waveform.
- 8: Divide T by W – this result is the duty cycle.
- 9: Repeat steps 4 through 8.

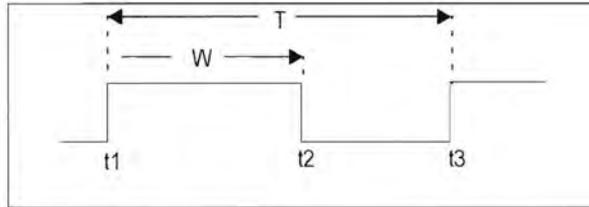


Figure 4: Period measurement

Win a PICkit2 Flash Starter kit



Electronics World is offering its readers the chance to win a new Microchip PICkit 2 Flash Starter Kit. The new PICkit 2 Flash Starter Kit enables engineers, students and anyone with an interest, to easily begin development and experimentation with PIC microcontrollers. The PICkit 2 follows the very successful PICkit 1 offering improved ease of use, faster programming and greater flexibility.

The PICkit 2 Starter Kit connects to any personal computer via full-speed USB 2.0, which allows firmware upgradeability, and requires no additional power supply for the programmer or target application board. The PICkit 2 comes with a set of easy-to-

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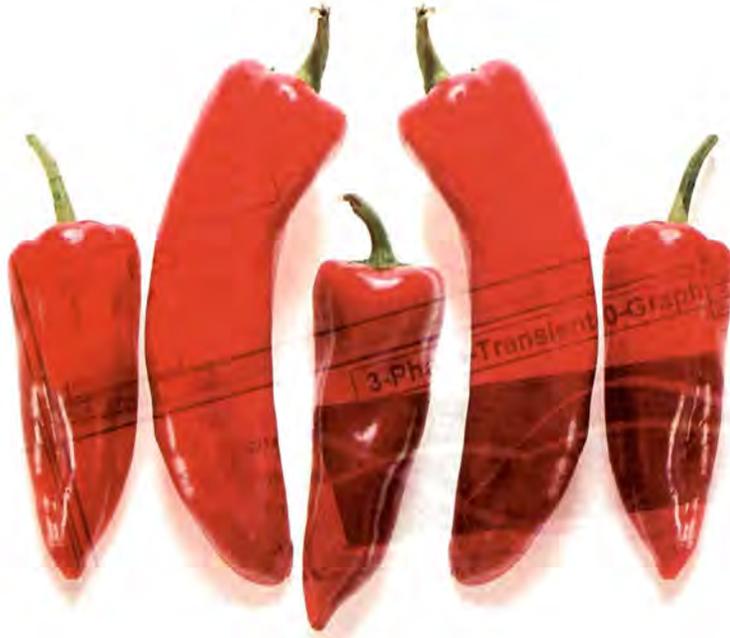
The kit includes the programmer, USB cable, CDs and an 8/14/20-pin evaluation board. Initially, the programmer supports 33 different low pin count, Flash PIC microcontrollers. For additional information visit the Microchip Web site at www.microchip.com/tools

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Good news on EMC?

The article on the "New Harmonics Standard" by Muhamad Nazarudin (EW, August 05, p14) contains a mixture of good news and bad news for equipment designers.

The good news is (quoting the article) that "the Class D current waveform envelope requirement has now gone. The migration to Class A would mean a reduction on the (potentially significant) cost of complying with the stricter class D."

In other words, the requirement limits have been increased, allowing higher levels of current transients to become acceptable, relaxing the design requirements and allowing manufacturing costs to be reduced.

The bad news is that the test requirements have become more complex, and the bulk of the article is devoted to a description of the additional measurements that need to be performed. The introduction of the New Harmonic Standard will inevitably lead to an increase in the cost of compliance testing.

However, even the 'good news' has a sting in the tail. If equipment is released onto the market, which creates higher levels of current tran-

sients on the 50Hz supply, then, inexorably, over a period of time, the level of interference on the supply will rise. Everyone will suffer.

Hence, the effect of introducing the new compliance standard will be twofold:

- The cost of verifying compliance will rise;
- The quality of the 50Hz mains supply will deteriorate.

This is not a development that can be greeted with a joyful welcome.

Ian Darney

*Bristol
UK*



The heat is on for all of us

Those who suffer sleepless nights when the weather heats up should cast a thought to the welfare of valuable electrical and electronic components housed in tightly packed panels when seasonal temperatures climb.

The increased power of modern devices has naturally created greater heat dissipation. At the same time real estate constraints have seen electrical panels becoming ever more densely populated. Given these trends, sharp rises in the ambient temperature – even the UK's occasional heatwaves – could be enough to shorten the lifetimes of individual components or even provoke premature failure.

The need for better cooling regimes in electrical enclo-

tures, VDI server and patch panels, electronic control boxes and the like has never been greater. Components such as relays, thermal overloads and contactors need to be kept cool to ensure their continuous and reliable performance. Once confined only to clearly defined high power installations, forced cooled or refrigerated enclosures should now be considered for broader applications.

While there are several solutions available to enclosure specifiers, calculating the thermal management requirements of a panel can be confusing, but consulting an enclosure specialist early in the design process should help.

Unfortunately, still all too often, the electrical or electronic kit is stuffed into a box that is sourced at the final stage from the first available supplier. This is irresponsible and gives poor service to the end user, but it does go on.

Perhaps, think of it this way, if one designed an ideal working environment for the electrical design team, it would be unlikely to be a greenhouse!

Richard Beighton

*Swindon
UK*

Mind your language

As resellers, many businesses struggle to carve a definition for themselves in terms of their key differentiators against the competition. It seems to have become commonplace to label your business a 'value-add' reseller and one that 'goes the extra mile', regardless of what the offering is. But what does this really mean? Are you a simply a box shifter labelling yourself as something more or do you deliver true value add to your customers?

Much of this debate comes down to one big question – what is value-add? Some would argue it is about service but that then leads to the next question: Does service still truly exist or is it dead? Communication trends have led many businesses away from the traditional phone/face-to-face route and more towards automated voice systems and helpdesks, email and online communication. Such communication has come under severe scrutiny over the last couple of years and businesses are beginning to wise up to the notion that people like to deal with people.

The perception of value against cost and risk differs from one organisation to the next but I argue that, either way, businesses need to decide where they fit into the value-add definition and focus on their real USPs. Perhaps true value-add is about recognising your business' strengths and focusing on these rather than branding yourself with the age-old value-add badge? There's food for thought.

Phillip Coombes

*Crowthorne
UK*

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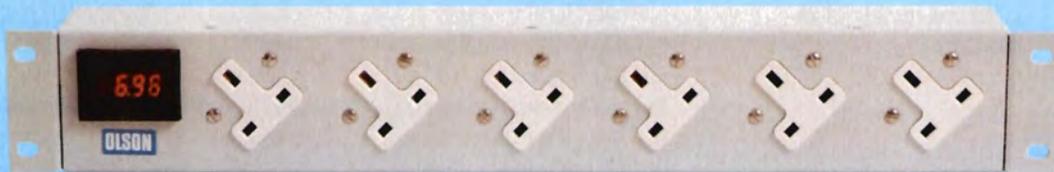


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Vive l'indifference

By Mike Brookes

Summer is with us and with the holiday mood nothing much in the short-range devices (SRD) world is happening – or is it?

Over the past few months, we have been exhorting the SRD industry to consider the future seriously in an atmosphere of spectrum pricing and rapid developments in this technology.

Regulators (radio administrations) have a real problem. They are under tremendous pressure to lease/sell any spectrum that becomes available, for example through technological advances, while the fastest growing sector in communications is that of the SRDs, which, historically, has enjoyed licence (cost) free secondary occupation of radio spectrum.

This is a great scenario for the SRD industry, but a real poser for administrations who cannot see any revenue benefit from allowing SRDs access to more spectrum than now. Thus, the pressure is on for industry to make the most effective use of currently available spectrum through reduction of "application specific" spectral bands, with the use of ever more intelligent radio chipsets that can 'hunt' for

interference-free bands.

While this might sound a great idea – a move towards 'generic' use of spectrum, certain sectors such as in social alarms, fire alarms and medical users will throw up their hands in horror at the thought of other SRD users moving into "their bands".

Strenuous requests for 'protected spectrum' are likely to be met with cynicism. There are too many examples where, for the best possible reasons, spectrum has been allocated on an exclusive basis and the market has responded – ungratefully – by no take-up.

“Regulators have long memories and will be very cautious in creating future 'ERMES'”

The ERMES band, recently re-designated, is a classical example. There was much 'egg on the face' of regulators who considered that they were doing the industry a service, only to find that their 'gift horse' was truly looked in the mouth and rejected. Regulators have long memories and will be very cautious in creating future 'ERMES'.

This was the first band ever designated under the auspices of EU frequency harmonisation and hailed as a triumph of the new cooperative policies being adopted to bring European use of radio spectrum together.

ERMES was to be used for wide area paging. What actually happened was that one or two EU states implemented it, but the vast majority didn't – thus making a nonsense of the "trumpeting".

The reason for its general failure was that technology moved on and the massive uptake of mobile phones effectively made ERMES redundant. Now, radio administrations are very wary about dedicating any spectrum to an application, preferring instead to provide a "highway", which users get on to according to their requirements.

For several months, through Electronics World magazine, we have been exhorting the industry to make positive moves in identifying new areas of spectrum that would be attractive for SRD applications – in a generic sense. We have pointed out that the European situation is very different to that pertaining in the US, where there is no history of varying spectral use by disparate States and that as a consequence, allocation of 20MHz sectors to SRDs is a non-starter.

At the time of publication of this article, the clamour of SRD

manufacturers eager to state their claims on spectrum for the future has been a resounding silence. The ECC Working Group (Frequency Management) Project team FM 43 is due to make its critical report on the 'Strategy for the Future of SRDs in Europe' by the end of 2005. The final report, which will determine the future policy within the European Union for the development of the SRD industry, will be presented in early 2006. Radio administrations are hard at work ensuring that the strategy is comfortable for them.

So far, the industry has not responded with equal enthusiasm. It is summer and most thoughts are on beaches and bars. Unfortunately – like a tsunami – unawareness is no guarantee of escape from the consequences.

Contact from any company involved in the SRD industry – as a manufacturer or user is welcomed. Please contact Electronics World magazine or the Low Power Radio Association (LPRA) at info@lpra.com

The LPRA (Low Power Radio Association) is a European trade body that represents manufacturers and users of short range devices (SRDs).

It is active in the production of SRD Radio standards and regulations. Mike Brookes is LPRA's chairman.

Wireless Software Solutions Firmware revision 2.1 Jan 05

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Nearly ideal parallel resonant circuit — computer controlled

Well known formulae for resonant frequency f_r and quality factor Q of the classical resonant circuit RLC are:

$$f_r = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

and

$$Q = R\sqrt{\frac{C}{L}} \quad (2)$$

If both of them, elements L and C are tuned in such a way that their product is changed but their quotient is constant, the resonant frequency will change but the Q factor will remain constant. This interesting case cannot be used in RLC techniques but can be applied to resonant parallel circuit consisting of FDNR* element D and resistor R_4 . In **Figure 1**, Bruton [1] FDNR circuit (inside the dashed line), the resistor R_4 and coupling capacitor C_c are shown. At the bottom of **Figure 1** is shown a digital interface that controls this resonant circuit by parallel port of the PC computer.

Equations 1 and 2, [2] for the circuit from **Figure 1**, can be written as:

$$f_r = \frac{1}{2\pi\sqrt{R_4 D}} \quad (3)$$

and

$$Q = \frac{\omega_r D}{C_p} = \sqrt{\frac{D}{R_4}} \quad (4)$$

where coefficient D is:

$$D = \frac{C_1 C_2 R_1 R_3}{R_2} \quad (5)$$

Equations 3 and 4 are similar

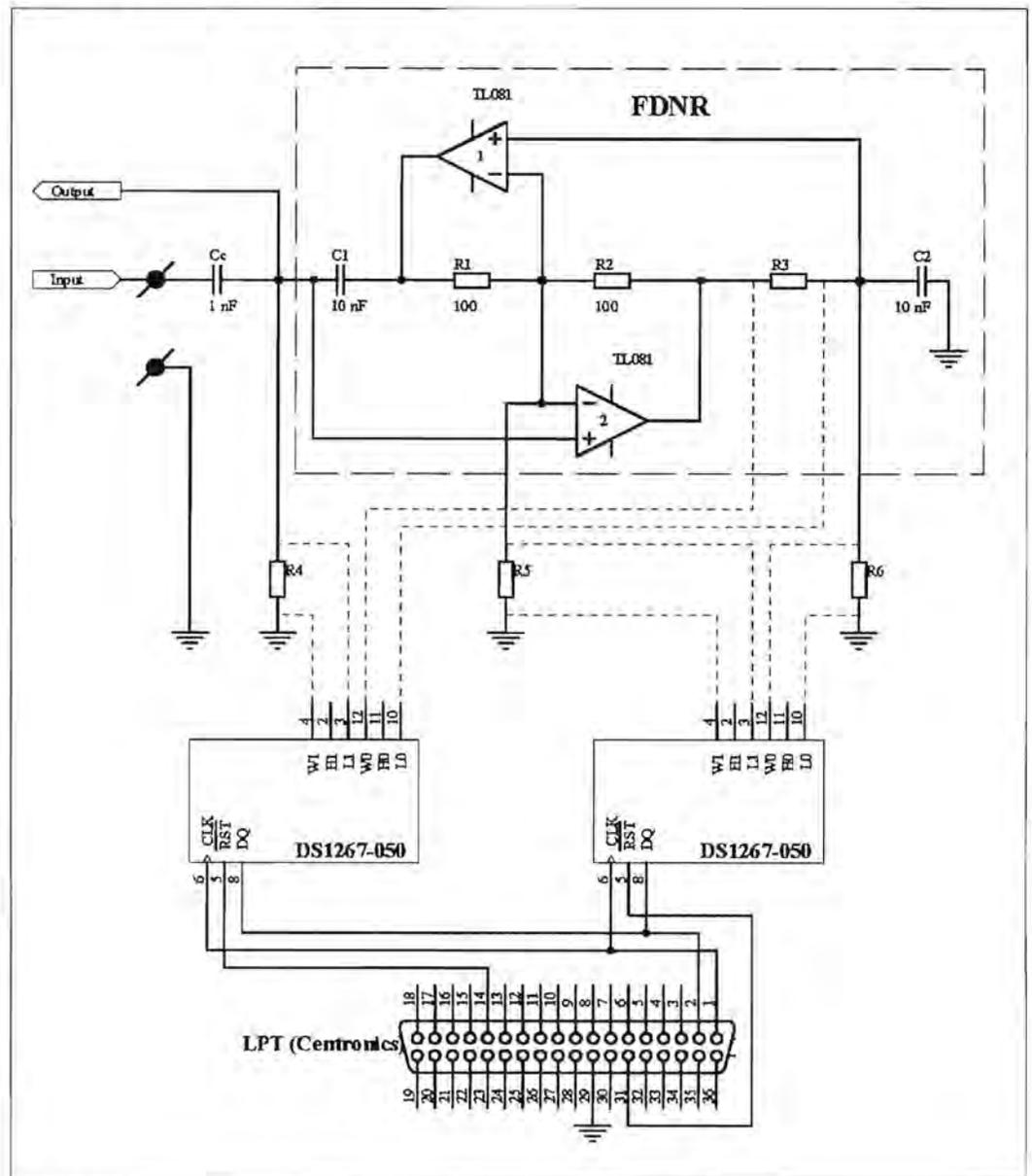


Figure 1: Scheme of the parallel resonant circuit with the digital interface

to 1 and 2. To tune the resonant frequency without the influence on the Q -factor the resistor R_4 must be simultaneously changed with the coefficient D , which can be done by changing the resistors R_4 and R_3 . We assumed that $R_4 = R_3$

and they are both simultaneously changed.

Parasitic capacitance C_p , which is included in Equation 4, appears at the input terminals of the FDNR circuit due to losses of the capacitors C_1 and C_2 and owing to the product of

gain and bandwidth of the operational amplifiers. Since the value of capacitance C_p changes with frequency and its sign becomes negative at the high frequency region, there is a need to add a positive and a negative capacitance to com-

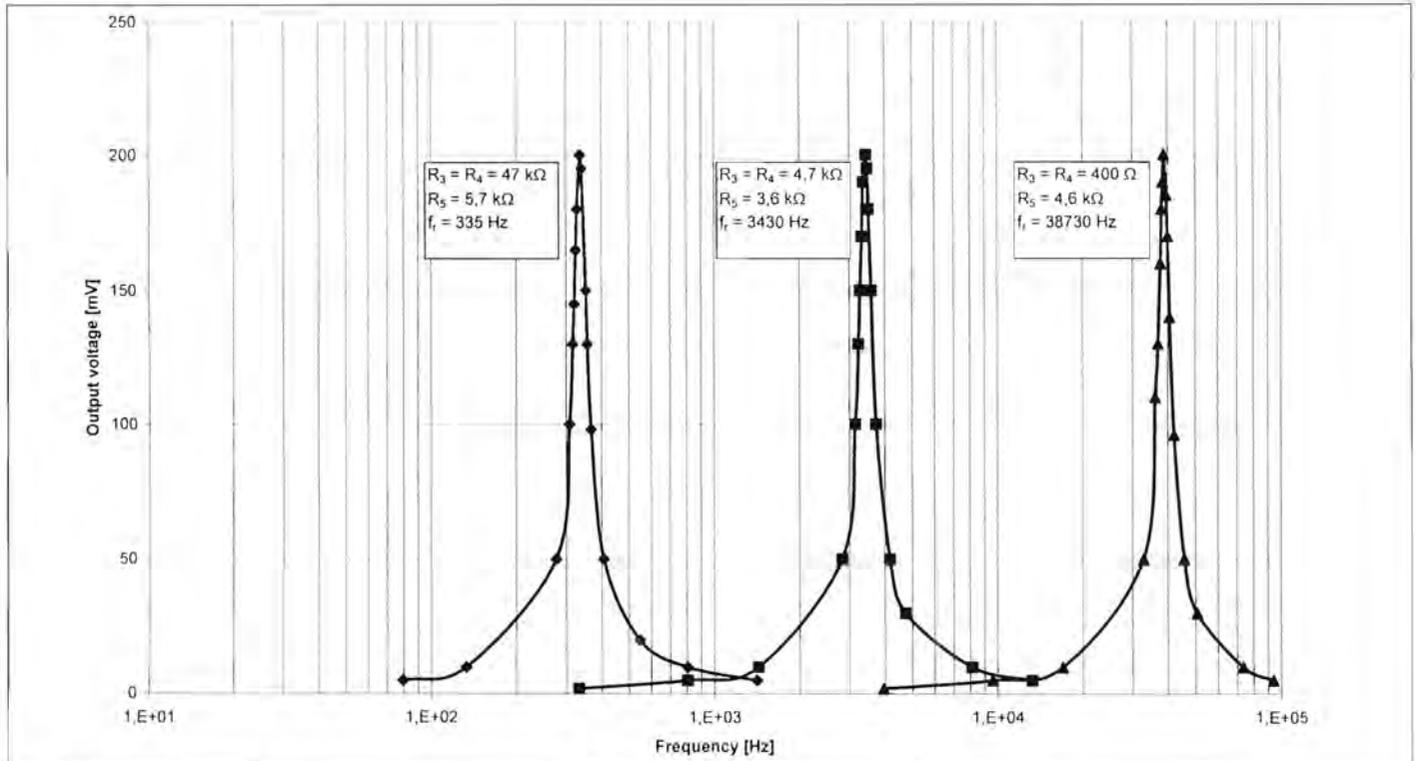


Figure 2: Some measured transfer characteristics of the circuit.

pensate the changes of C_p . Resistor R_5 proposed by Senani [3] gives the negative capacitance C_{ad} . Resistor R_5 proposed by Senani gives the negative capacitance C_n . Finally, the quality factor Q is described as Equation 6:

$$Q = \frac{\sqrt{\frac{C_1 C_2 R_1}{R_2}}}{C_c + C_p + C_{ad} + C_n} \quad (6)$$

Capacitance C_c should also be added to the other capacitances, which exist in the denominator of Equation 6, if the circuit is excited from a source with a small output resistance.

By matching the values of the resistances R_{ad} and R_n , the sum of the capacitances $C_p + C_{ad} + C_n$ can be set to zero. Then if $R_1 = R_2$ and

$C_1 = C_2 = C_i$, the Q-factor is $Q = C_i / C_c$ and, for example, if $C_i = 10\text{nF}$, $C_c = 1\text{nF}$ and $Q = 10$ then the output voltage equals the input voltage (200mV), but the Q-factor calculated without the capacitance C_c tends to infinity as in an ideal resonant circuit.

At the end, three or four resistors are needed to tune this circuit. They are: R_3 and R_4 , for changing the resonant frequency with a constant quality factor, R_6 for the decreasing Q value at high frequency region, and R_5 for increasing the Q value to keep a constant value of the Q factor elsewhere. These resistors can be substituted by two double digital potentiometers, controlled from the parallel port of the PC computer or microcomputer. Eight bit double potentiometers DS 1267 (50kΩ) are controlled by three digital signals: control

signal RST, clock CLK and data DQ, which can be realised by a simple computer program.

Measured transfer characteristics of this circuit are shown in Figure 2. Resistor R_6 was not used in this case.

Application of it is recommended when the circuit is working near an unstable region of a frequency, for

example near 100kHz.

Lech Tomawski and Marcin Górnicki
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Note:

*FDNR, Frequency Dependant Negative Resistance;
 $Z(s) = 1/s^2$; $D [As^2/V]$

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