ELECTRONICS WORLD

DECEMBER 2005 £4.50

The Unsung Heroes:

Circuit Protection and Safety Devices

Conductive Adhesives – New Flip Chip Technology?

Squeezed but not Squashed: 16-bit MPUs

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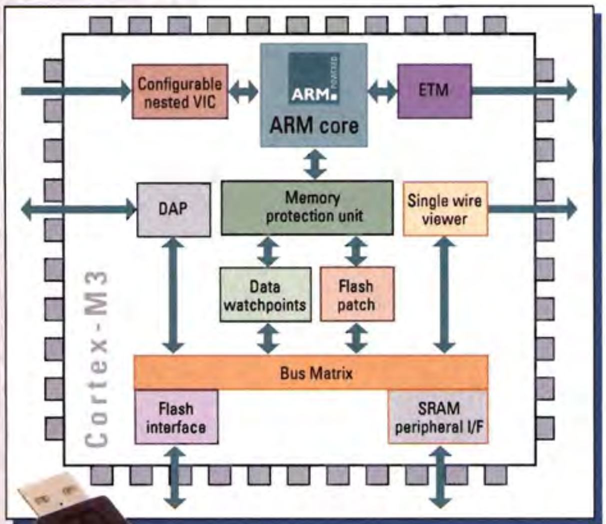
December 2005 Volume 111 Number 1836



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Front cover image supplied by Raychem Circuit Protection

Rising Star

One area that has been quietly chugging along in the background – without too much fuss, as in wireless communications, and without the glitter of consumer electronics – is automotive electronics.

Even though the growth curve of new cars produced is almost flat, the electronics content in them is exploding. We happily drive our cars, taking things for granted but rarely do we appreciate how much engineering goes behind all of that.

Electronics requirements in the automotive sector are great and varied. From analogue devices and systems' perspective, there's a need for many sensors, high-voltage components and high-precision devices. In the digital field, as usual, requests revolve around microcontrollers, digital logic and non-volatile memory, among others. The under-bonnet area is a harsh environment, with high vibration levels and a wide temperature range. The temperature range for in-vehicle electronic devices is being extended to accommodate those variations and such systems nowadays also come with ESD and EMC protection.

Smart power is being added to many new car systems. Smart power is the ability to integrate high power and high voltage at silicon level to devices, but it is relatively new for this sector.

Electronics is becoming more prevalent but also more novel in all aspects of the vehicle: for the engine, driver safety and comfort, in-car infotainment systems, wiring for all type of ECUs (electronic control units) and in-vehicle networks, brakes, headlights, tyres, guidance systems, car entry and security, transmission and gearbox control, heating and ventilation, not to mention ever more strict exhaust emission regulations to be met and a lot more besides.

All of these require sensors. In 2001, the automotive sector used some 1.2 billion sensors; in 2008 that figure is expected to exceed 2 billion units. In the cockpit area alone, there are a dozen or more application areas: from mirror glare and dashboard sensors, to seat weight and pedal positioning sensors. Similarly, the need for motor control grows increasingly in cars too. Some luxury models have up to three motor control units – in the headlamps alone! This means that they can sense and adjust the lighting level of the headlights if a car, for example, goes round a bend or potentially blinds other road users.

Innovation and engineering continue in the automotive field, even though this sector remains relatively quiet and does not brag about its achievements.

Maybe it's too quiet for such interesting developments. If electronics and engineering make a difference in our world, then why not shout about it?

Svetlana Josifovska
Editor

To all of those who are eagerly anticipating our next year's feature list so they can contribute with technical content to Electronics World magazine, here is the list of subjects that we will endeavour to cover in depth. As usual, we will be happy to hear from you whether you have a feature, circuit idea, top ten tips or, indeed, a book review – on any electronic engineering subject – that you'd like to share with the rest of the engineering community.

JANUARY	Semiconductor Fabrication and Electronics Manufacture	**JULY**	Data Acquisition and Analysis
FEBRUARY	Design for EMC	**AUGUST**	Industrial Electronics
MARCH	Displays Design	**SEPTEMBER**	Automotive Design
APRIL	Software Development	**OCTOBER**	Battery Technologies
MAY	System Power Design	**NOVEMBER**	Designing with MPUs and MCUs
JUNE	Communications Techniques	**DECEMBER**	RF and Microwave Design

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PRINTER: William Gibbons Ltd • **ORIGINATION:** Impress Repro A1 Parkway, Southgate Way, Orton Southgate, Peterborough, PE2 6YN
NEWSTRADE: Distributed by Seymour Distribution Ltd, 86 Newman St, London W1T 3EX. • **PUBLISHING DIRECTOR:** Tony Greville
If you are experiencing problems getting copies through your newsagent, please call Debbie Jenner on +44 (0) 1322 611210

ISSN 0959-8332

Electronics World is published monthly by **Nexus Media Communications, Media House, Azalea Drive, Swanley, Kent, BR8 8HU** Nexus Media Communications is a trading name of Nexus Holdings Limited. Registered in England. Registered Number 5346404. Registered Office: Hanover House, 14 Hanover Square, London W1S 1HP

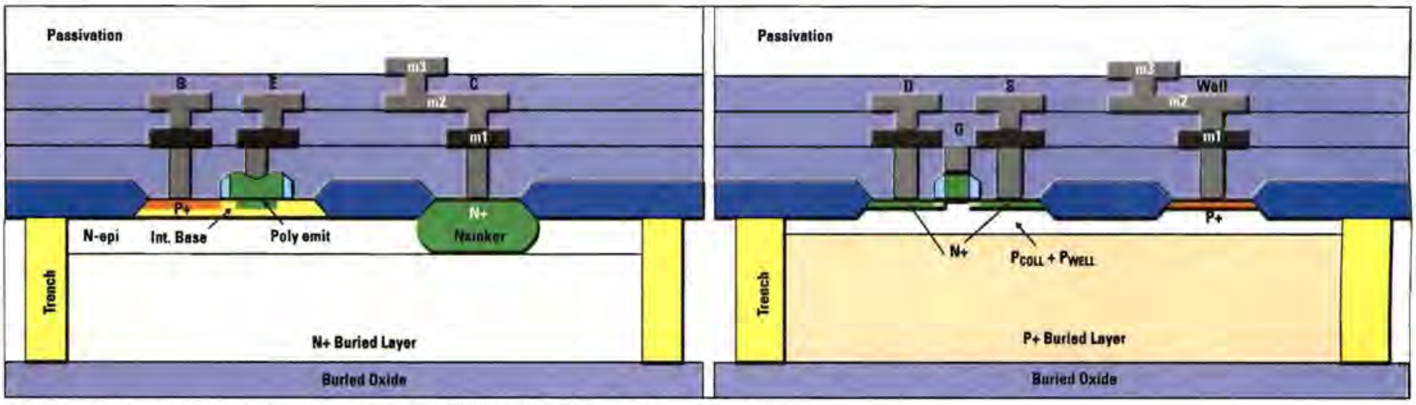


Diagram of the transistors created with SOI BiCMOS by National Semiconductor

National Semiconductor launches analogue process for precision amps

National Semiconductor has developed a silicon-on-insulator (SOI) BiCMOS process for a new generation of high-precision amplifiers. Dubbed VIP 50, for Vertical Integration PNP in 0.5 micron CMOS feature sizes, the process is a combination of Silicon on Insulator (SOI) and CMOS technology.

SOI is typically used for high-speed processes but, on this occasion, National Semicon-ductor's team used it for precision as it reduces the capacitance on the collector of the bipolar transistor by a factor of 10. It lowers parasitics, but also a lot less energy is wasted on powering up and powering down of the device.

The transistors are isolated by a 1-micron thick layer of buried oxide and trenches. This isolates them from noise but also prevents a transistor to go into a latch-up mode when in saturation caused by leakage currents.

"This process is latch-up proof and this is good for reliability," said Erroll Dietz, vice president of the amplifiers products group at National Semiconductor.

The bipolar transistor (NPN, PNP) could have a supply voltage of up to 12V, even though it can be tweaked for voltages of up to 30V.

Although, typically, a PNP transistor is a lot slower than an NPN one, National improved it to match the NPN's speed to 4GHz.

"We also matched the resistance," said Dietz. "We trimmed it to the low value as needed." To trim the resistance, National has "whittled away" the metal links. A coating die on the transistor packaging further ensures that the resistance is not going to be disturbed after it has been trimmed at the wafer fabrication level.

In addition, the firm optimised the process for low 1/f noise (<1Hz), which is important for precision analogue signal conditioning applications.

"We've optimised the MOS transistor to have noise significantly lower than that of other CMOS. Now that performance is better than that of JFETs. The corner frequency is higher than in [conventional] bipolar transistors but you can deal with that via the base current," said Dietz.

The company has already used this process to announce several products – the LMP7711 and LMP7701 precision amplifiers, LMV651 and LMV791 low-power op-amps, LPV511 nanoamp and LPV7215 nanoamp comparator. According to Dietz, there are over 20 products in the pipeline to be launched in the near future.

Look! No hands

Tractor manufacturer John Deere is using satellite-guided steering technology in its latest generation of tractors.

GreenStar AutoTrac SF1 offers 13-inch pass-to-pass accuracy to help operators make consistent straight passes through the field. The system uses three common components: receiver, display and a mobile processor with a key card. The StarFire iTC SF1 receiver, the GreenStar display and the mobile processor with an AutoTrac SF1 KeyCard were developed with Wind River's software on board.

The GPS-guided tractor doles out the exact amount of pesticide with accuracy, taking moisture measurements as it goes along. Thomas Evensen, chief technology officer at Wind River, said that the tractor cabs are even fitted with TV sets to stop the operators getting too bored by not having to steer.

Customers have the ability to upgrade to higher steering accuracy by using additional software to update to four-inch pass-to-pass accuracy.

Acquired simulation 'engine' strengthens AWR's design suite

Applied Wave Research (AWR) has strengthened its Microwave Office RF and microwave design package with a highly optimised RF simulator, faster electromagnetic (EM) simulator, an open EM Socket II interface for third party tools integration and an optional network filter synthesis.

"Our Microwave Office design suite has been very successful; we have 500 customers and 6000 seats. The key to this success is the architecture, which delivers more concurrent data flow rather than serial. This means that developers get their designs faster," said Ted Miracco, executive VP at AWR.

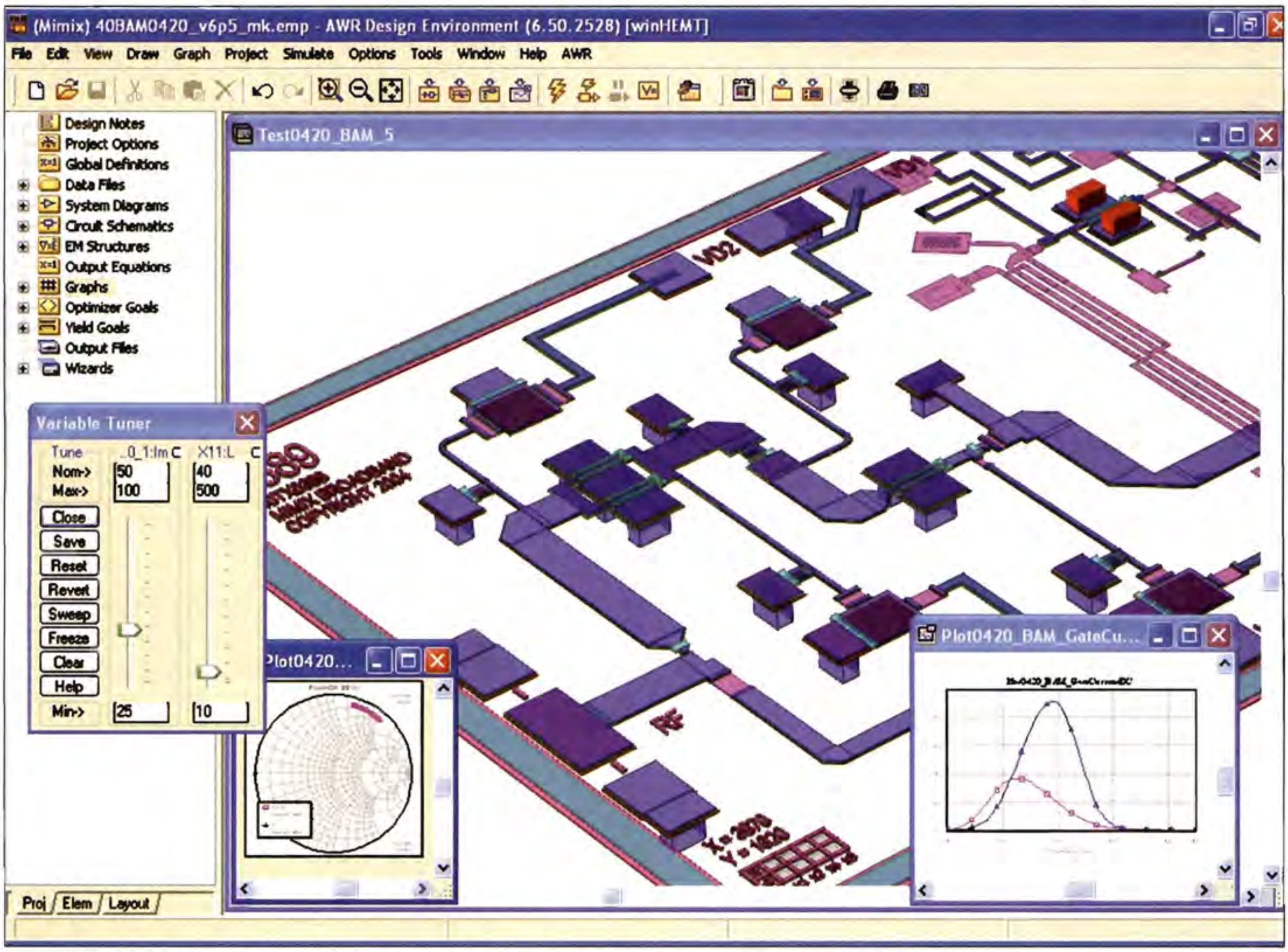
Microwave Office 6 boasts a new simulation engine that has been acquired when AWR purchased Finnish firm APLAC Solutions. APLAC used to work for Nokia and its simulation technology has already been approved by foundries in the US and Asia. "We integrated their simulator with our user interface. We both had simulators but we've all been using different tricks. We found that their [simulator] algorithms were more optimised."

In addition, AWR entered into an agreement with Nuhertz Technologies to use its filter synthesis software that covers most of the filters.

AWR demonstrated the approach for a unified data model, which is only now being discussed heavily in the EDA domain, a few years ago in its first Microwave Office suite. It was also one of the first EDA tool suppliers to offer open source code, so that developers can easily change things around but also integrate their own algorithms into it.

AWR's customers split into three groups: the military, commercial users and academia.

According to Miracco, there's a growing number of design-starts for WiMax and 4G in the US.



Microwave Office 2006 design suite is integrated with APLAC's foundry-approved circuit simulation technology

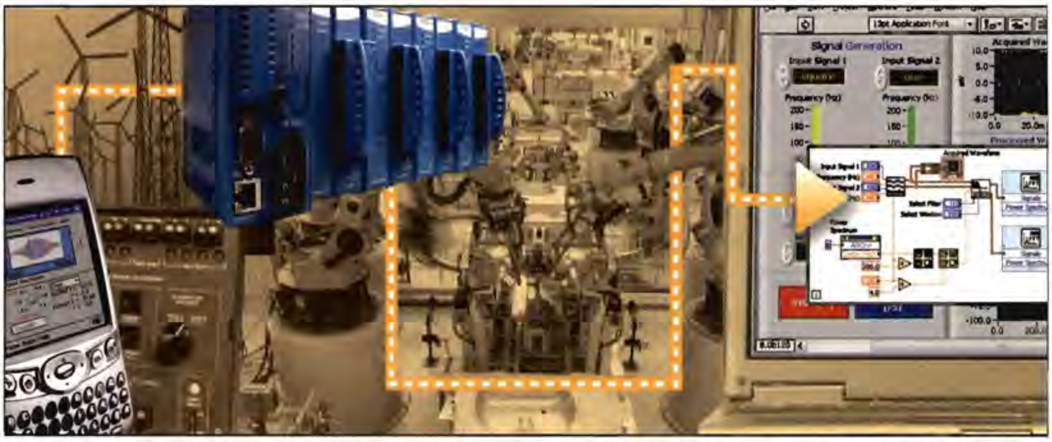
A new study from the University of Edinburgh and Pennsylvania State University suggests a solution to one of the biggest challenges facing the optics and electromagnetics sector – how to produce near-perfect lenses cheaply. Researchers have devised a very simple method of producing materials which bend light the 'wrong' way – a significant development as lenses with minimal distortion can be made from flat slabs of these negatively-refracting materials. According to the study, negatively-refracting materials can be produced by blending two granular substances together. Neither of the two granular substances can refract negatively by themselves, but a homogeneous mixture can.

Ω

IP video services in Asia Pacific are ramping up and will grow by nearly 80% annually through 2010, reports In-Stat, with revenues reaching $4.2bn by 2010. China, Japan, India and South Korea will account for the majority of regional growth. In deregulated markets like Japan and South Korea telecom companies can offer IPTV and VOD services freely. In China, incumbent carriers are heading toward obtaining IPTV licenses to provide such value-added video offerings. Among the major IP-based video service providers leading the market in the region are Yahoo!BB, Korea Telecom, Chunghwa Telecom, China Telecom, China Netcom, SingTel and Atlas Interactive India.

Ω

The latest figures released by UCAS show an increase in the uptake of science and software engineering in UK universities. However, there is still work to be done if the UK is to avoid a future skills crisis, transform into a knowledge-based economy and compete on a global scale, says the IEE. Although the figures show a positive overall rise in sciences, the engineering and computer science disciplines, which are so crucial to the UK industry, are either declining or not increasing at the rate that is required.
The uptake of electronic and electrical engineering is consistently low and specialist areas, such as power engineering, are still receiving only a quarter of the number of applicants needed to sustain the industry.



With LabView 8 engineers can interface with and synchronise remote intelligent devices and systems

New LabView promises ease of use for large projects and teams

National Instruments (NI) has announced a major upgrade to its popular LabView series of virtual instrumentation software. LabView 8 contains new tools for distributed intelligence as well as tools to manage and deal with large systems and project teams.

"We are beginning to see more processes in the systems (test or control systems) and on more platforms," said Ian Bell, technical marketing manager at National Instruments. "LabView 8 offers an enhanced ease-of-use and speed of use."

With LabView 8 engineers can interface with and synchronise remote intelligent devices and systems such as real-time processors and FPGAs. The platform also has a "shared variable" on board that allows simplified communication between the project team members. As such, the engineers can use the same graphical platform for simple data transfer, deterministic real-time communication and network synchronisation with integrated alarms, events and data logging.

"Shared variable is an architecture that we are going to build on. It'll be a part of a more deterministic model," added Bell.

In addition, LabView 8 has an instrument driver finder. Before, developers had to locate instrument drivers via the web, now with LabView 8 this is automated and easier. Users can automatically recognise connected instruments and search, download or install the appropriate driver from the 4000 plus that are available on the NI Instrument Driver Network.

According to Bell, LabView 8 has had more than 100 features added to it to deal with the larger set of developers that NI wants to reach, such as in embedded design and prototyping, industrial monitoring and control and automated test and measurement among others.

Intel is banking on new video applications

Intel has launched a range of video processing systems in the belief that future telecom revenues will come video services. "We believe video will drive revenues and customer loyalty for operators," said Tim Moynihan, director of product marketing at Intel. "We see video mail, video messaging, video portals, video blogging, infotainment, push to video and real-time video streaming as the applications that will become very important," he added.

The newly launched Intel systems, which are aimed at enterprises for video over IP applications, include the NetStructure Host Media Processing V1.5 for Linux and Windows. The systems sit in the space between video processing and video servers. "NetStructure Host Media Processing is software-based. As such, it offers higher density of channels – up to 400 of them – and a better performance," said Moynihan. "You can use the extra channels to improve the richness of your applications, such as [offering] video for example."

Suntek in China is already operating video portals and video messaging, handled by video servers.

DSP goes head to head with processors in digital video

Texas Instruments (TI) is aiming to replicate the success it has had in the GSM mobile phone market in the video world with its newly launched Da Vinci "platform". It combines an ARM core with the latest digital signal processing (DSP) core for a variety of applications, from portable video through surveillance systems to standard definition TV over phone lines and even high-definition TV (HDTV).

This is a similar approach to the OMAP platform TI launched several years ago for mobile phones that now dominates the market with a single software and development infrastructure, making it simple for companies such as Nokia, Symbian and Motorola to develop operating systems to a standard set of APIs.

The key to its success, says Jean Marc Darchy, DSP systems director for Europe at TI, will be the software. "The aim is to provide a lot of the software components such as Linux and WinCE and a series of others that are targeting the embedded system world. We are providing the middleware and the user interface capabilities so with the first device will be a [complete] solution."

Other players are also coming with innovative architectures. US start-up Telairity has developed T1P2000 that combines five independent vector/scalar cores, a video controller and a DRAM controller supporting an I/O bandwidth up to 5.3Gbit/s in the SoC.

A US start-up called WISchip International, is aiming to take on Da Vinci, too. Its DeCypher8100 decoder uses three MIPS cores with a mixture of programmable elements and hardwired accelerator blocks for functions such as CABC, ME and DCT, all linked via a 32-bit bus switch. This can handle one HD channel up to 1080 progressive and an SD channel for picture in picture, recording on a VCR or distribution around the home.

Another innovative approach comes from French firm Neotion. It has patented the idea of using an MPEG4 AVC module in a CAM module. This is the slot in the back of a TV or payTV set-top box that can take a PCMCIA card with hardware for conditional access.

The mobile phone is prepped to become the new portal for information

"In the near future, your phone will be where you go for information," said Tod Sizer, director of Wireless Research at Bell Labs.

"Today, it is only used for communication (voice and texting), but in the near future the information [that it will provide] will be unique to each person – tailored for their individual needs. This will be their personal virtual network and yet accessible to any device. There will be agents in the phone that will manage that network," he added.

This is the future envisaged for the mobile phone by Bell Labs. Train timetables, theater and cinema listings, restaurant directions, your child whereabouts, the health of your elderly relatives are just some of the possibilities that could be included in that 'customised information'. According to Bell Labs's Sizer, the mobile phone will have a push-to-view option that will offer an interactive video channel too.

In order to achieve such a flexible virtual network for each mobile phone on the planet, Bell Labs is turning to frequency and protocol agile cognitive radio techniques. "Much of the spectrum is [currently] underused," said Sizer. "These [techniques] are an effort to use up that spectrum. This will require a new generation of wireless devices capable of dynamic spectrum coordination. Such devices will be able to select between which spectrum channels to use and which to leave alone."

The FCC in the US and Ofcom in the UK are already getting involved. In the UK, the recently revised EN 300 22, which will be on the statute books by the beginning of 2006, now incorporates, for the first time, the use of LBT (ListenT) and AFA (Adaptive Frequency Agility) techniques.

System studies and prototyping are already taking place at US defence and aerospace firms Mitre, General Dynamics and others.

A new product is being developed that will allow thoroughbred horse breeders and trainers to remotely analyse a horse's performance during training. The system combines a GPS receiver with biological and environmental sensors into a single lightweight package carried by the horse. The device can simultaneously monitor the horses performance, physiology and environmental conditions. This can be displayed in real time to the rider or transmitted live to anywhere in the world. Bespoke software delivers highly accurate analysis of a horse's performance and fitness, as well as assistance in managing and quantifying the effect of training regimes. The system has been developed by UK engineering consultancy Cambridge Design Partnership.

Ω

A portable mil-spec 3G network has been launched by 3Way Networks. The hand-portable UMTS system is capable of supporting up to 100 user devices. The equipment is based on the 'network on a card' principle. It packs a complete 3GPP Release 5 compliant system with radio network, switching and packet elements into a 30 x 56 x 80cm ruggedised case. Called DBX-m, the system supports a range of applications including disabling third-party 3G networks, providing home calling facilities for armed service personnel or acting as a basestation with enough bandwidth to support a spectrum of remote sensing applications, from battlefield sensors to multi-media UAV communications.

Ω

Toshiba has announces a gallium nitride (GaN) power FET with power output of 174W at 6GHz. The device is said to surpass the operating performance of the gallium arsenide (GaAs) FET widely used in basestations for terrestrial and satellite microwave communications. Toshiba achieved this breakthrough performance enhancement by optimising the epitaxial layer and chip structures for 6GHz-band operation and by adopting a four-chip combination structure to minimise heat build-up. Toshiba plans sample releases next year.

FPGA designers get a graph-based tool from Synplicity

EDA tools supplier Synplicity has applied a brand new approach to physical design of programmable logic in its latest FPGA synthesis tool – Synplify Premier. This is a graph-based, push-button synthesis flow that promises big benefits.

Pre-existing wires, switches and placement sites used for routing an FPGA are represented as a detailed routing resource graph. Mapping, optimisation and global and detailed placement and routing have been combined into one routine to identify fast routes and assign them timing estimates. Distance is, effectively, represented as a parameter of delay and availability of wires. This results in a full-chip placement and physically optimised netlist, which is then used with the vendor's FPGA routing tool.

This process, Synplicity claims, reduces the number of design iterations, typically associated with place and route. "In FPGAs the shortest route is not necessarily the best one and our tool selects the best route," said Andrew Haines, marketing director.

Traditional FPGA flow, where RTL feeds into synthesis, and the resulting netlist splits into floorplanning and place and route, is hitting limits as FPGAs grow in complexity and functionality. The EDA industry has embarked on other optimisations but with limited results. Synlicity claims its tool will top that with a performance imrovement of between five and 20%.

"We have beta tested it [the new tool] for Xilinx's devices," added Haines.

Synplicity customises its tools for each product line of each FPGA vendor and Xilinx's FPGAs will be the first to gain this tool. Support for others, like Altera and Actel, will follow in the near future.

TOP 10 TIPS

RoHS compliance

- **Don't play the part number lottery**. Use distributors that are changing part numbers. This is the only way to ensure compliant and non-compliant parts are identified and properly segregated. Distributors that aren't changing part numbers rely on 'flushing through' stock – an approach that will leave engineers unsure of whether they are using compliant or non-compliant products in design. It's absolutely essential to know what suppliers are shipping.
- **Traceability is key**. Ensure distributors are providing complete documentation and, where appropriate, material testing. A blanket declaration of compliance on product lines is not enough. Distributors should be able to show a full audit trail at item level for each RoHS compliant component to ensure stock is risk-free. Personalised Certificates of Compliance for each individual component will show due diligence if the authorities come knocking.
- **Go online to access the latest RoHS products**. Compliant product listings are continually being updated as new stock becomes available in the marketplace. Only distributors that can get RoHS products to market quickly can truly support engineers through the changing legislation. The web is the fastest way to source the latest RoHS components.
- **Find out about products that are coming soon**. Build compliant components into the design cycle by making design decisions in advance of stock availability. Having a clear timeframe on when products will be available is essential in order to do this. To be sure of when components are in stock look out for distributors that offer the option of an email notification service.
- **Understand the impact of RoHS**. Getting to grips with all the issues doesn't need to be difficult. Use distributors that have in-house RoHS experts who can discuss the legislation and help it make sense. Distributor user groups and RoHS seminars are proving popular events across the country and provide the opportunity for engineers to find out about the latest RoHS developments.
- **Benefit from a step-by-step guide**. The details of the legislation regarding lead-free soldering, maximum concentration values and homogeneous materials can get very technical. Find a comprehensive guide that will provide clear reference material on these key issues.
- **Keep informed**. As the legislation evolves, it's important to keep abreast of changes. As well as updates from the DTI, there's a wealth of material available from organisations like ERA Technology, an independent consultancy providing RoHS compliance and reliability advice.
- **Access to technical support**. Readily available advice from a technical support desk with engineers specially trained in RoHS should be a core offering from distributors. Being able to pick up the phone or email a query goes a long way to helping smooth the transition to RoHS.
- **Testing**. Find out what safety checks a distributor has in place to ensure components have been tested. Random testing, based on a stringent risk analysis process, is recommended as part of due diligence. The term "know your supplier" often crops up in the guidelines that accompany the RoHS legislation. The use of a trusted supply source is of vital importance.
- **Look for quality assurance** – peace of mind in the transition to RoHS is key. Distributors can only provide comprehensive support if they are embracing all areas of the legislation. Quality can be assured through a commitment to changing part numbers, the provision of a broad range of support services and a wide offering of RoHS components.

This month's Top Ten Tips were supplied by Gary Nevison of Farnell InOne. Farnell InOne runs a dedicated website www.rohs.info, which covers everything engineers need to know about RoHS as well as the latest news on the directive.

Next generation storage solutions

for media and entertainment applications

It's time for broadcasters, network operators and content providers to start relying on off-the-shelf type of storage systems, says **Per Sjöfors**

The business of broadcasters, network operators, studios or content providers requires a considerable amount of high-speed data storage. In an ideal world, this data storage needs to be completely integrated, easy to use and scalable, as well as available 24/7 for its entire staff.

Currently, many broadcasting and postproduction facilities suffer from a fragmented storage infrastructure. Storage decisions are often tactically made, dictated by the storage needs of a single workstation or a group of workstations. As workstations and servers are added over time – many on different computer platforms and with different operating systems – the storage infrastructure becomes increasingly fragmented. This leads to a storage infrastructure characterised by "islands of storage" with each "island" serving a single workstation or group of workstations. Typically, this may include some shared storage for editing or for video servers using SAN (Storage Area Network) technology, where the storage is accessed using expensive Fibre Channel, while direct attached storage is used in most other cases. Network Attached Storage (NAS) is sometimes added to the typical infrastructure as an archival type storage system.

With multiple workstations and servers, with either direct attached storage or part of a SAN, it becomes difficult for operators to locate files. Once they are located, the transfer of large video and audio files from a certain workstation to a second workstation takes a long time, as files concurrently crisscross the network – while operators just wait. Even worse, this file transfer operation may disable the source workstation from doing actual paid-for work.

Likewise, routine support and maintenance becomes a nightmare in an environment that includes storage subsystems from multiple vendors with multiple operating systems, using different storage technologies. Each operating system and storage technology has its own management application and requires the maintenance staff to be fully trained and experienced for multiple applications. Not only does this force maintenance staff to take more time to learn multiple applications, but it also increases the risk for potentially damaging mistakes.

> *"In an "island of storage" environment, the overall storage utilisation factor is typically low and unbalanced – with certain storage systems operating at near full capacity while others are close to empty"*

In an "island of storage" environment, the overall storage utilisation factor is typically low and unbalanced – with certain storage systems operating at near full capacity while others are close to empty. This type of inefficiency is completely inconsistent with the corporate striving for high work-effectiveness.

A simple and elegant solution to the issues identified above is the addition of a next generation NAS system, a grid storage system that improves efficiency, enables better and controlled access to assets, leverages scaling of storage, load balancing and backup features, while at the same time substantially reduces the overall spending on storage capacity and storage maintenance.

From a capacity and access bandwidth point of view, these systems allow users to add capacity or bandwidth anytime the need arises – even while the system is in full operation – eliminating costly downtime and the need to involve the facility's technical resources for system reconfiguration and balancing. Similarly, adding users to a next generation NAS is as simple as attaching a workstation to the network, requiring virtually no systems integration.

With technology giants spending hundreds of million of dollars to develop ever faster and more efficient computer and networking technologies, a next generation NAS system must be designed to take advantage and leverage this development. The solution then, is to create a system that is totally software-based and will automatically increase storage system performance with any new hardware technology. Costs will be further kept low by the use of off-the-shelf standard hardware components.

Secure, always-on, access to the data on the storage system is paramount in today's environment. Service interruptions, whether in creation or distribution of content, will be expensive and must be avoided. The architecture of a next generation NAS system, therefore, will need to be fully redundant, with failover capabilities, automated self-healing and include regular call-out and 24/7monitoring functions – no matter how small or how large a system might be.

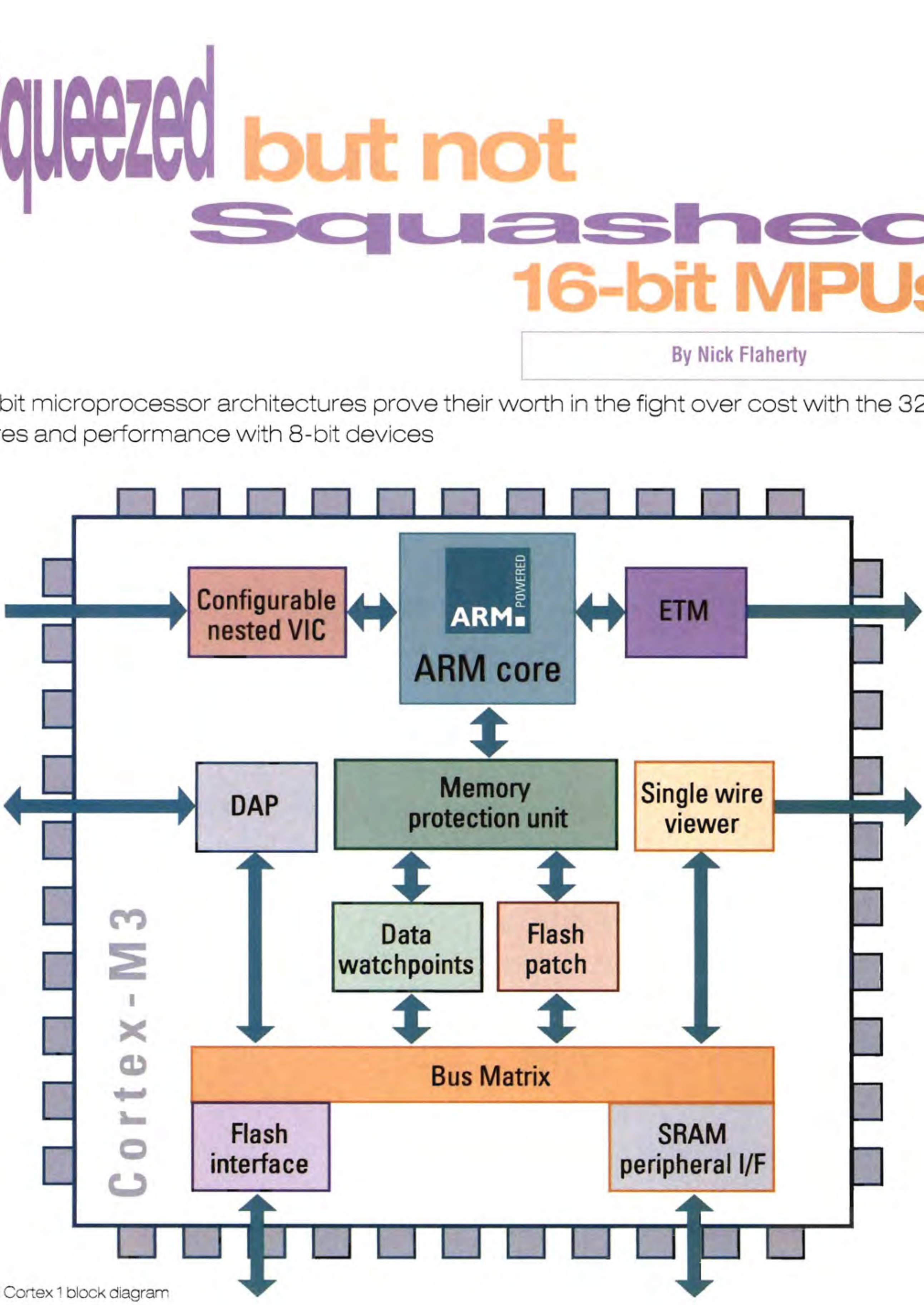
The "right" storage strategy will enable M&E operators to improve operational efficiency, maintain a high availability to assets, whereas a "wrong" strategy is costly to implement, even costlier to manage and may severely impact a company's bottom line.

Per Sjöfors is vice-president of business development of Exanet

Squeezed but not Squashed 16-bit MPUs

By Nick Flaherty

16-bit microprocessor architectures prove their worth in the fight over cost with the 32-bit cores and performance with 8-bit devices



ARM Cortex 1 block diagram

16-bit microprocessor architectures are seen as squeezed between the small size and cost of 8-bit and the performance of 32-bit cores, but there has been a resurgence of interest in the technology from several directions, particularly in motor control and automotive applications. As a result, 16-bit controllers are predicted to have the fastest growth of all three types of processor.

This is being driven by costs and increasing performance from new process technologies, opening up new areas that previously were not accessible to 16-bit controllers.

Traditional low-cost 8-bit controller designer Microchip is moving up into the 16-bit market, while ARM is moving into the 16-bit market with its Cortex microcontrollers.

Microchip sees the 16-bit market growing slightly more than the 32-bit market at 21% in 2004, but from a bigger base of $4bn, rather than the 20% growth of the $3bn 32-bit market. Alongside this is the $2.5bn digital signal processor (DSP) market, which is growing at 17%, driven by applications in the medical and industrial fields, instrumentation, as well as emerging technologies such as biometrics in fingerprinting, iris scanning and facial scanning, says Will Strauss, founder of market researchers Forward Concepts.

Similarly, there are significant opportunities for 16-bit devices in motor control, particularly when combined with DSPs. "That has big potential but it is small right now," said Strauss, as well as robotics, pattern recognition, efficient power supplies and uninterruptible power supplies (UPS).

To tackle these markets, the new Microchip 24F and 24H controllers are the same 16-bit core as is the digital signal controller, without the multiply accumulate unit and the DSP engine, and giving 16MIPS and 40MIPS respectively at 30Hz. This allows designers to create a range of products, starting at the low end and then moving up to multimedia applications such as speech interfaces and wireless links with the same instruction set and the same development environment.

These MCUs will start general sampling in January next year for applications ranging from remote controls, air conditioning controllers and toys, through factory automation and remote monitoring and diagnostics, to climate control and ignition controllers in automotive applications. The same tools can then be used with the DSC parts that add signal processing for noise cancellation and voice over IP applications.

The ARM Cortex-M3 processor contains the company's smallest core (33,000 gates at 50MHz in a 0.18μm process) and integrates in many close system peripherals through a closely coupled switch matrix. While it is pitched at 32-bit designs, it uses the Thumb2 instruction set that mixes 32-bit and 16-bit instructions to keep code memory size down.

Cambridge Consultants has also developed its third generation of the XAP processor with this firmly in mind. The previous generations of 16-bit engines are used in devices such as the Bluetooth single-chips from Cambridge Silicon Radio (a spin-off from Cambridge Consultants).

"The simplest architecture is when the address and the data space are the same, so there's more of a need for something that is logically Von Neumann but physically Harvard," said Alastair Morfey, chief designer. "What we see going forward is people need to be able to run much bigger pieces of software that could be done on a project basis and re-used [later]."

Software is the driving force behind XAP3 as well as the new 16-bit parts from Microchip. "We are trying to make it so that software programmers can be lazy and do big projects on a processor that is small," he said. "Our goal is small and low power, and therefore cheap."

For XAP3, Cambridge Consultants takes the step up to a 32-bit architecture, but with a twist. The processor core is designed to handle both 32-bit instructions and 16-bit instructions transparently; there is no "mode" that has to be set as in the ARM Thumb instruction set. More than that, however, the architecture is set to make things easier for the project developer. A relative program counter (PC) with different global pointer values and each of these with its own stack area, supports multiple programs in memory different locations at runtime, rather than all of them having to be linked during the compilation stage. This means that the different parts of the project can be updated, uploaded and run independently.

> *"The simplest architecture is when the address and the data space are the same, so there's more of a need for something that is logically Von Neumann but physically Harvard"*
> ***Alastair Morfey, chief designer, Cambridge Consultants***

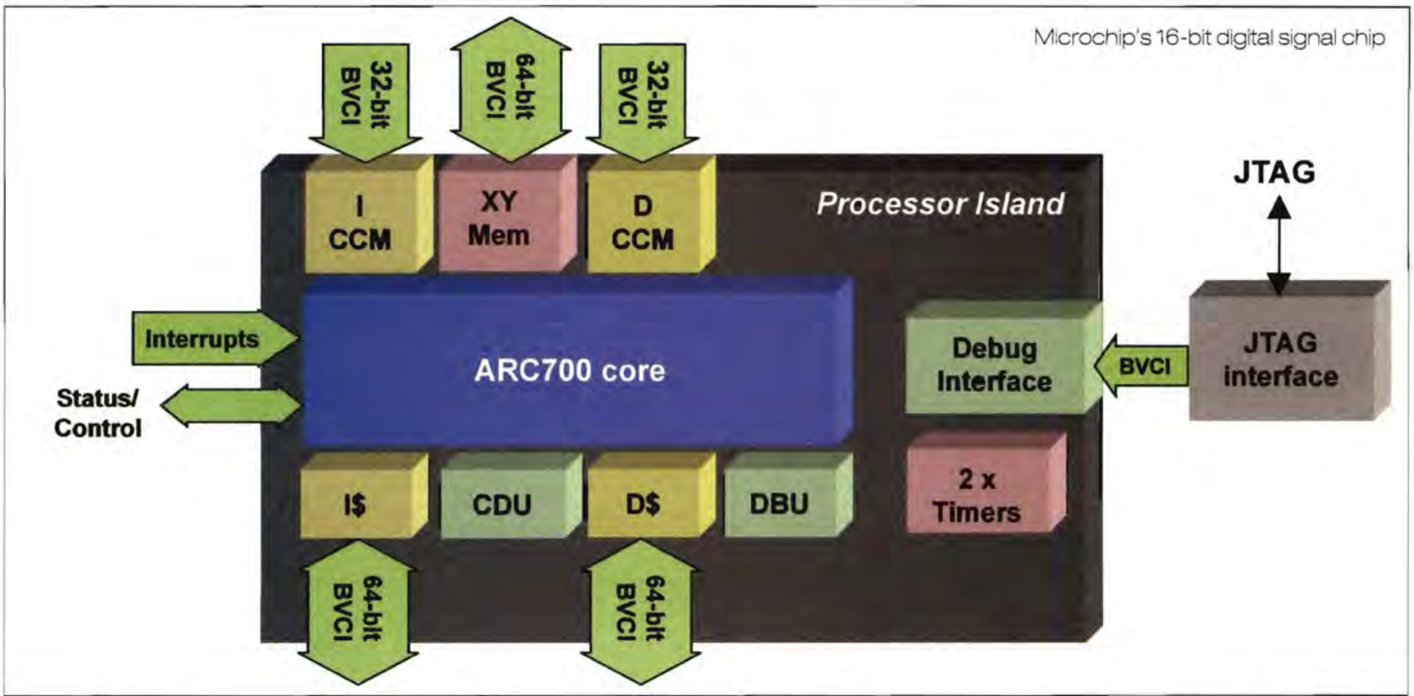
The instruction set has been optimised to compiler conventions, for example, acknowledging that registers are not symmetrical and are used for different tasks such as stack pointers, link registers, passing arguments and returning results. This means that some instructions can only access certain registers, which helps to increase the code density. Similarly, frequently used instructions such as load, store and move are implemented in 16-bits rather than 32-bits; a bit at the front of the instruction determines the length. This cuts the address space from the 4Gbytes of a traditional 32-bit engine to 2Gbytes, but that is still a dramatic improvement on 16-bit systems with a 30% improvement in code density over 32-bit systems.

The assembler determines which instructions are 16-bit and which are 32-bits, depending on the complexity and the address space required.

Moving to 32-bits also opens up to more operating systems. "We have done a clean compile of UC Linux and we expect to port the Nucleus real-time operating system, but not yet," said Morfey.

The team is developing two versions of the core. XAP3a has a single bus, making it a Von Neumann engine, while 3b has pipelining for more performance and could be Harvard architecture, while maintaining the single memory for data and instructions. The 3a core is just 50,000 gates.

At the same time, configurable processor core developer ARC International has also increased the performance of its 32-bit embedded core in the drive to run high-level operating systems. It has ported the ThreadX operating system to its



Microchip's 16-bit digital signal chip

700 series of cores, and boosted their performance to match that of DDR2 DRAM memories at 533MHz.

The firm is working on a fully configurable approach to adding operating systems to the core, which will dramatically increase its popularity.

The performance boost comes from changes to the RTL of the hardware pipeline, particularly the branch prediction unit and the memory management. The design team profiled large amounts of existing code on the core, and changed the design to eliminate stalls in the seven stage pipeline. This results in the 750D reaching 533MHz and 813MIPS on a 130nm process, taking up just 1.4mm^2 and using 0.14mW/MHz.

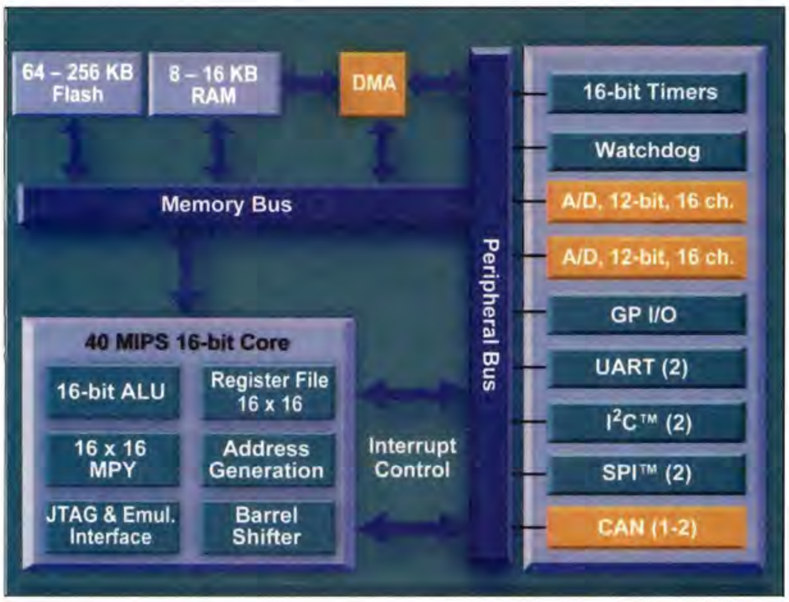
The port of ThreadX is important in giving system developers a standard real-time operating system (RTOS) to work with. While ARC has its own proprietary RTOS, some potential users have been reluctant to move to it. The combination of the RTOS and higher performance will take ARC into applications as the main CPU, not just the companion chip, said Derek Meyer, vice president of sales and marketing at ARC.

However, porting a standard operating system to a configurable core is not simple. As the system-on-chip developer can add instructions and registers to the core, these may have to be taken into account by the RTOS. As a result, ARC has defined a base core functionality that will run the RTOS, and any additions are handled by the compiler and the API programming interface.

The next stage is to allow the vast majority of configurable options to be fully supported by the OS, which means having the OS compiled alongside the core, says Meyer.

Smaller size and tighter code memory is an increasingly important trend, and designers are taking several different routes. Part of the solution depends on what the existing code base is, but moves to Thumb2, which is not backward-compatible with the original ARM instruction set or the original Thumb, mean that there is more of a level playing field with these 16/32-bit engines. If performance is important, then adding customised instructions to the optimised ARC core speeds up key applications and still allows standard operating systems to be run.

So even though 16-bit is seeing resurgence in dedicated devices, the 32-bit cores will be difficult to shift from their place. This is challenged from 32-bit architectures finding ways to provide smaller code size with the high levels of performance and full operating systems.



ARC750 core

Lightning Still Strikes: But Some Challenges Are New

ESD, EMC and other issues continue to affect circuit design but how to go about protection when performance and speed of operation as well as standards evolve? **Chris White** of Raychem Circuit Protection explains

As the drive towards integration and solid-state technologies continues, designers focus ever more closely on delivering higher speed, higher performance and more features, in ever-shrinking device and system footprints. For consumers and engineers alike, this progression is often accompanied by the implicit assumption that electronics is increasingly and inherently robust: an impression that is bolstered by talk of designing for increased reliability, particularly in consumer markets where a reputation for quality is seen as a distinct competitive edge.

In such an environment it is very easy to forget that electronics, far from being tough and resistant to damage, is often delicate and vulnerable. Even in the 21st century, lightning still strikes, power cables still come loose and circuits remain vulnerable to faults in the devices and assemblies connected to them.

The bad news is that a whole host of new threats can be added to this range of traditional perils. Components based on advanced semiconductor manufacturing processes are sensitive to ESD (electro-static discharge). Electronics is increasingly deployed in environments, which would have been unimaginable 10 or 20 years ago: these include conditions of high temperature or humidity, situations involving exposure to dust, water or solvents and circumstances that involve high levels of shock and vibration.

This state of affairs is worsened by the changing feature set of the electronics itself and the different techniques for realising those features. The trend towards low-voltage operation means that high currents are encountered more often. And users' expectation to be able to "hot swap" and "hot plug" equipment carries dangers of voltage spikes and sudden charges and discharges.

As a result, circuit protection techniques have had to move forward just as quickly as the equipment that they protect. To the old style one-shot fuse has been added an array of options including gas discharge tubes (GDTs), multilayer and metal oxide varistors (MLVs and MOVs), polymeric ESD suppressors and polymeric positive temperature coefficient (PPTC) devices.

The increased range of options reflects not just changing electrical needs, but also a change in function. Whereas the traditional fuse is basically a safety device designed to protect the user, many of the new components are equally important in protecting the equipment itself from damage caused by associated circuits: or in preventing the equipment from causing such damage to interconnected assemblies. This is increasingly important in a world where connectivity is taken for granted. Most equipment today needs to talk to the outside world via some standard interface or another. Such non-safety standards implicitly specify necessary levels of protection, by defining how system components may interact correctly and what happens when things go wrong.

Necessary levels of protection

The two main fields of development in circuit protection today are in ESD suppression and "resettable fusing" via PPTCs. ESD is of particular concern at the moment, because new standards such as USB 2.0, DVI (Digital Video Interface) and HDMI (High-Definition Multimedia Interface) specify extremely high-speed signals that can be degraded by the capacitive loading typical of most existing protection strategies.

IEC-61000-4-2 is now almost universally accepted as the most relevant standard for ESD immunity. It specifies a testing regime that simulates the damage caused by an ESD event from the human body, according to a human body model (HBI). Common regulatory requirements, including those in the EU that lead to the award of a CE mark, specify that equipment should conform to IEC 61000-4-2 Level 2, with contact and air discharge test voltages of 4kV. In practice, most manufacturers opt for Level 4 testing, in which the contact and air discharge voltages are 8kV and 15kV respectively. The waveform used for testing rises to its peak voltage (and a maximum current of 30A) in less than 1ns, decaying to 50% amplitude within 60ns.

Whatever ESD protection mechanism is chosen, it needs to suppress this waveform sufficiently to prevent damage to the equipment. This is commonly achieved using a simple, low-cost Zener diode. Such an arrangement will clamp the voltage to a few Volts, with a response time which will be deemed satisfactory at around 1ns. The penalty for such an implementation is a fair amount of leakage current and a high capacitive loading (50pF or more) on the rails which are being protected.

Such a performance penalty is acceptable in applications such as the audio path of a mobile telephone, RS232 serial port, keyboard or mouse interface. Standard transient voltage suppression (TVS) diodes provide similar performance but with higher clamping voltages, for use in automotive applications, general electronics and white goods. MOVs and standard MLVs, meanwhile, exhibit higher capacitance (at least 100pF), but generally have faster response times (in the sub-1ns range).

Addressing higher-speed applications

Higher-speed applications such as USB 1.1, Ethernet and LCD drivers require lower capacitive loading of below 10pF and can, therefore, be served only by low-capacitance components such as specially-designed TVS diodes and MLVs. The former provide low-to-medium clamping voltages, modest current leakage and response times of 1-5ns. The latter clamp at over 100V and suffer from higher leakage current, but can achieve the sub-nanosecond response times required in some applications.

Protection of the fastest devices on the market today, however, requires a different class of components. Standards such as USB 2.0, IEEE 1394 and DVI impose severe restrictions on the acceptable capacitive loading. DVI transmitting equipment, for instance, can operate at up to 1.65Gbit/s; HDMI typically operates at a rate of 750Mbit/s. These specifications put designers in a bind, because transmission speed is not optional: the usual consequence, then, is to sacrifice a degree of ESD resistance. This risks damage to the sensitive chips that the protection scheme is intended to safeguard, but also puts additional stress on the protection component itself.

The new USB 2.0 protocol provides a further case in point. It allows for data transfer rates of up to 480Mbit/s and supports plug-and-play hot swappable installation and operation. These factors make low-capacitance ESD protection of the bus essential.

Polymeric ESD suppressor devices

Polymeric ESD (PESD) suppressor devices are one recently developed solution to this problem. The mode of operation of such a device is relatively simple: conductive particles are dispersed in a non-conductive polymer within the body of the component. The polymer maintains a separation between each conductive particle which acts like a "spark gap". For this reason, PESD devices have both very low leakage current and very low capacitance. However, a high-voltage ESD pulse that exceeds a certain trigger voltage will cause the gaps to spark-over, creating a path of very low resistance. It is this mechanism which leads PESD devices to typically exhibit higher trigger voltages than clamping voltages: the energy needed to start the process is higher than that required to maintain it.

PESD devices provide exceptionally low capacitance (typically 0.25pF). Advanced devices such as those recently announced by Raychem can also offer trigger voltages of around 100V and clamping to a few tens of Volts. These are improvements on key specifications which to date have limited such devices' usefulness. A further important parameter is their performance in transmission line pulse (TLP) testing: and IEC 61000-4-2 specifies that devices must withstand at least 100 ESD "strikes", with a typical figure of 500. Engineers should be aware of the performance impact of multiple strikes when selecting such components.

As with most of the common techniques for ESD suppression, designing with PESDs requires the engineer to adhere to certain best-practice guidelines. Data signal ground and V_{bus} transients need to be suppressed for proper operation, typically via a separate MLV. Conversely, good design practice suggests that it is wise to avoid tying the data signal ground line to the chassis ground line at the board level, suggesting the use of decoupling capacitors between V_{bus} and chassis ground to minimise EMC issues. Finally, as with all ESD suppression devices, PESD components should be installed as close as possible to the source of the potential ESD event.

PPTC circuit protection devices

Polymeric materials are also making an impact in the most familiar of all circuit protection applications, fusing. PPTC devices protect assemblies in the same way as a traditional fuse, effectively going open-circuit when subjected to an over-current (or over-temperature) condition. However, unlike a traditional fuse, when the fault condition is removed and the power is cycled, the PPTC returns to its normal conducting state. Each device is typically specified by a "hold" current, which is the minimum current that the device will pass without tripping at 20°C.

Like PESD suppressors, PPTC circuit protection devices are made from a composite of semi crystalline polymer and conductive particles. However,

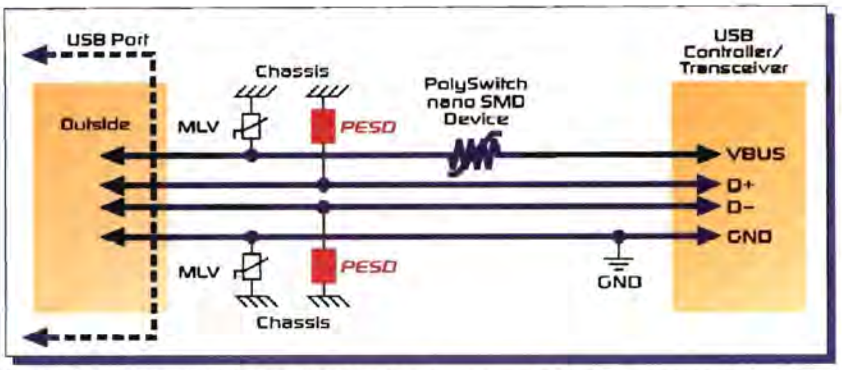


Figure 1: Typical USB 2.0 circuit protection design using PESD suppressor devices

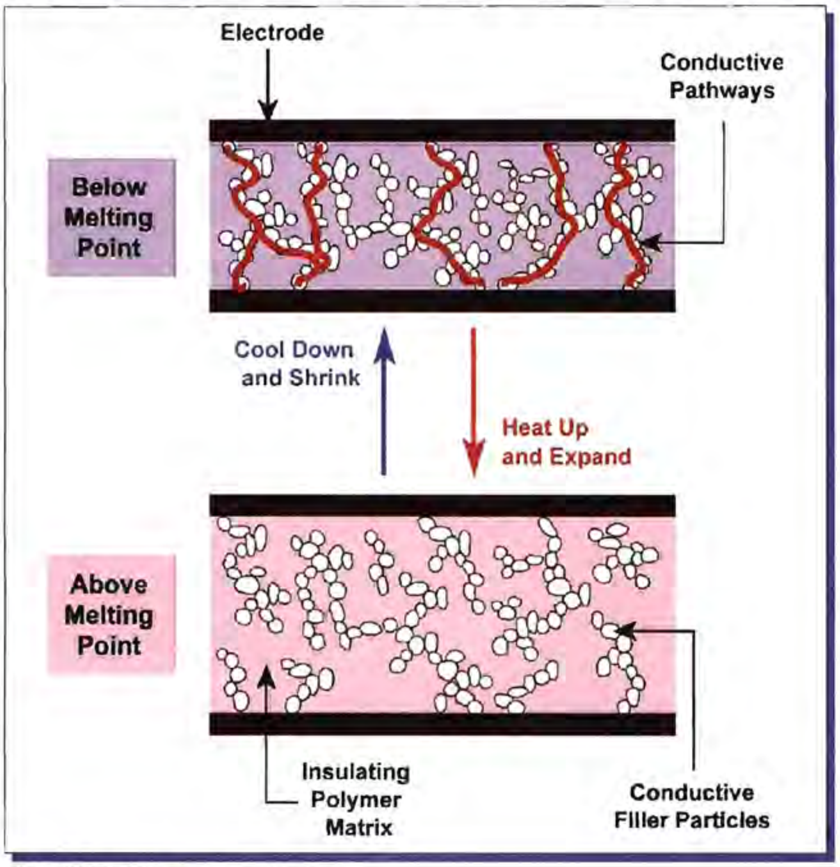


Figure 2: PPTC crystalline structure

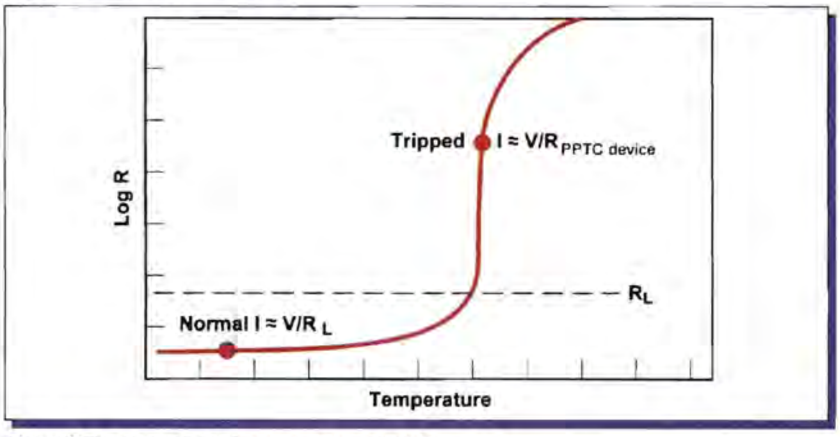


Figure 3: Typical operating curve for a PPTC device

whereas PESD devices are normally non-conducting, PPTCs are normally conducting devices. At room temperatures, the conductive particles form low-resistance networks in the polymer (see **Figure 2**). But if the temperature rises above the device's switching temperature (T_{SW}), the crystallites in the polymer melt and become amorphous. The increase in volume during melting of the crystalline phase causes separation of the conductive particles and results in a large non-linear increase in the resistance of the device.

Because the "fusing" process is temperature-dependent, it can be triggered either by high current passing through the part, or by an increase in the ambient temperature. This means that a PPTC component can be used both as over-current and over-temperature protection. For instance, in a power supply it can be physically located on the transformer windings so that it will trip if input voltage sag conditions cause an increase in transformer power dissipation and, hence, heat dissipation – even if the increase in current is insufficient in itself to trip the device. Similarly, in a switch-mode power supply, the device can be mounted in contact with critical heat-generating parts such as the MOSFETs.

The resistance of a PPTC typically increases by three or more orders of magnitude (see **Figure 3**) and the device will remain in its latched (high resistance) state until the fault is cleared and power to the circuit is removed – at which time the conductive composite cools and re-crystallises, restoring the device to a low resistance state. This resettability provides more than just a cut in the need for service calls and maintenance costs: since it is not necessary to provide access for fuse replacement, it also allows a reduction in board space. There may also be safety advantages because service personnel do not need to access areas which contain potentially uninsulated terminals carrying line voltages (or higher).

Simpler design?

From at least one point of view, designing with PPTCs is simpler than using traditional fuses. The latter can be blown by momentary transients, causing nuisance failures: it is, therefore, often necessary to set the fuse rating much higher than the system operating current to avoid such events. Under these circumstances, the fuse is more appropriately viewed as a safety device than a circuit protection device, since it will likely be too highly rated to prevent the level of current that might damage the more sensitive system components and ICs. The PPTC, in contrast, can be specified with a trip point much closer to the actual operating current of the system, providing better protection of the electronics and helping to prevent damage when, for instance, external load components fail.

Five other parameters are relevant when considering the use of a PPTC device. The first and most basic of these is maximum voltage capability, since the system voltage is fixed. Next are two measures of current: hold current and trip current. The former is the highest continuous current that the device is guaranteed to pass without tripping at standard operating temperature, and the latter is the minimum current that will trip the device. It is important to consider the derated hold and trip currents (**Figure 4** shows a typical characteristic) at the product's designed-for operating temperature, because, as we have already noted, PPTC devices are thermally activated.

The final two quantities that need to be considered in specifying a PPTC are time to trip and resistance. The first specification will be dependent upon the amount of fault current through the device and the system operating temperature. The higher the temperature at the time of fault, the faster a PPTC device will trip (see Figure 4 for a 265VAC rated PPTC device). Resistance is generally specified at 20°C, in terms of minimum, nominal and maximum values: not as a tolerance percentage as would be the case with standard resistors.

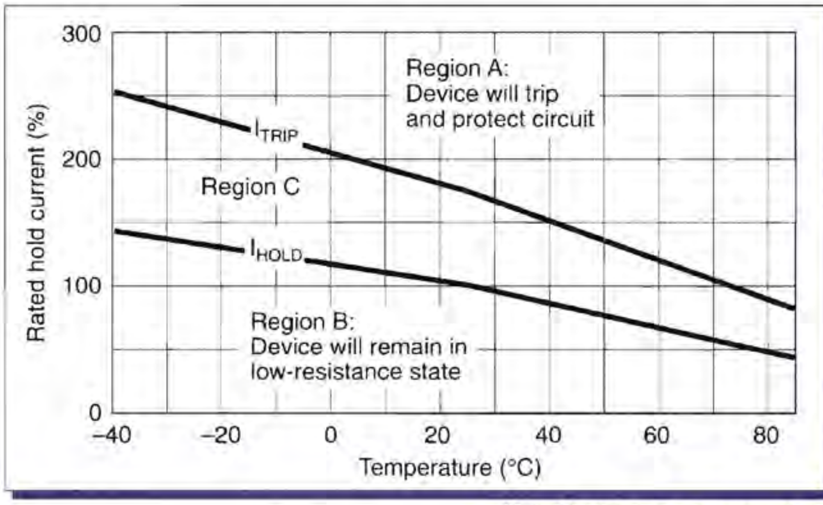


Figure 4: IH and IT vs temperature

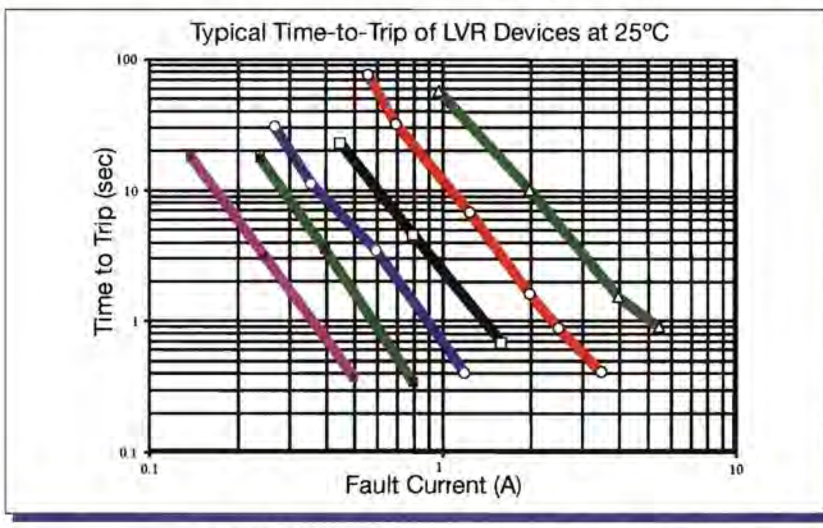


Figure 5: Time-to-trip curves for a 265VAC-rated PPTC device

Radical changes ahead

Increasing performance and speed of operation – and changing standards – often mean radical changes in the technologies required to implement systems. But sometimes these changes are more subtle. Just as the advent of USB 2.0, DVI and HDMI has led designers to rethink their strategies for ESD protection, the widespread introduction of broadband communications has brought about major changes in the requirements of telecommunications infrastructure, including equipment that is installed outdoors or on the customer's premises.

In this field, one of the major circuit protection challenges is to build in resistance to overvoltage faults of the type caused by lightning on or near line plant and short-term induction from – or worse, contact with AC power lines. To emphasise the fact that things have not stood still, even in this relatively well-established application, the ITU has within the last two years revised its testing requirements for such situations. Given modern high-speed transmission rates, the challenges are not dissimilar to those encountered with ESD protection on high-speed lines: to devise effective ways of shunting away extremely large voltage spikes without compromising the system's ability to transmit and receive at high speed.

In contrast to the case of USB 2.0 and DVI, however, this is one area where it has proved possible to evolve established technologies to accommodate new requirements. The use of GDTs and thyristors continues to represent the best solution in such applications. GDTs are used in parallel with the components they are protecting. In the event of a voltage surge, they switch from their normal high-impedance state to a very low impedance state. GDTs have extremely low capacitance and, so, are suitable for use on high-speed lines such as ADSL and VDSL. Thyristors are valuable in similar applications for their very low on-state voltage and relatively small form-factor when compared to devices of similar energy-handling capacity.

It seems likely that circuit protection and safety devices will remain in the "unsung hero" category of electronics components for the foreseeable future. However, advancements in the speed and power of our systems are possible only for so long as these particular devices can continue to develop and ensure robustness and safety. All of the semiconductor advances in the world are useless if the components are regularly "zapped" by ESD, and the only conclusion can be that future products look like needing more protection, not less.

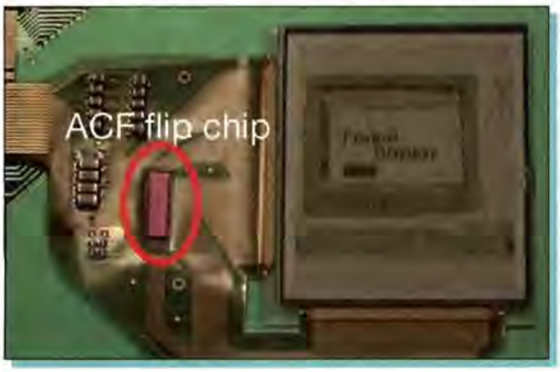
Moisture Effects On The Reliability of ACF interconnections

Chunyan Yin, **Hua Lu** and **Chris Bailey** from the University of Greenwich, London, and **Yan-Cheong Chan** from City University of Hong Kong present a paper on the moisture effects on new technologies deployed in flip chip packaging

The major trend in the electronic products today is to make them smaller, faster and cheaper, while at the same time more friendly, functional and reliable. One of the key technologies that are helping to make these goals possible is electronics packaging and assembly, especially low-cost flip chip technology. Up until now, eutectic tin-lead solder has been the main material used in flip chip technology. However, the use of lead in the electronic devices is becoming a more and more serious concern for the consumers and the manufacturing industry, due to the harmful impact of the alloy on the environment. Therefore, many research activities are now focused on the alternative interconnection materials to tin-lead solder in electronic packaging industry.

What is ACF?

Anisotropic conductive films (ACFs), more appropriately referred to as anisotropic conductive adhesive films (ACAFs) have been introduced as a promising flip chip interconnection material due to their potential in achieving high density I/O interconnection, low processing temperature and relatively mild impact on the environment. In particular, devices with flip chip on flexible substrate (FCOF) using ACFs are now widely used in smart cards, disk drives and driver chips for LCDs. A typical prototyped LCD product using ACF flip chip technology is shown in **Figure 1**.



ACF consists of adhesive and randomly distributed conductive particles. There are several kinds of ACFs available in the industry, according to the type of particles. The ACF filled with Ni/Au coated polymer particles are now commonly used in the fine pitch connections due to the relatively higher connection reliability and more uniform distribution of conductive particles. The detail structure of this kind of conductive particle is shown in **Figure 2**. The diameter of the tiny particle can be as small as 3.5μm.

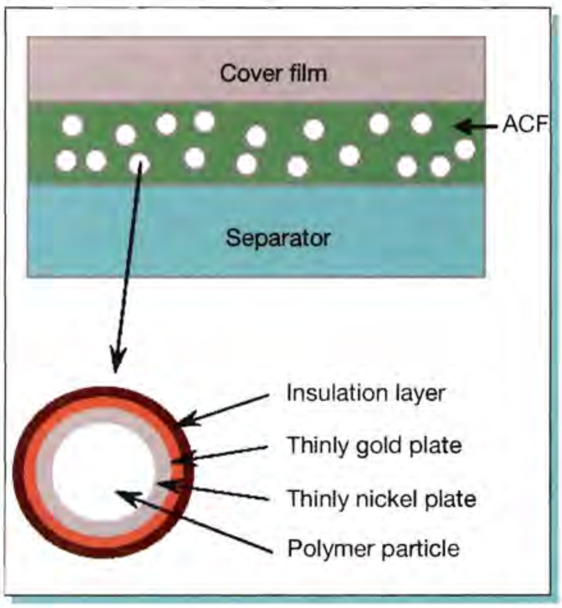


Figure 1 (Left): Prototyped LCD using ACF flip-chip technology

Figure 2 (Right): Detailed structure of Ni/Au coated polymer particle

Flip chip bonding process using ACF

Compared with soldering, the ACF assembly process is simplified since there is no need to use flux, stencil printing and re-flow ovens. It consists of the following three steps which are illustrated in **Figure 3**:

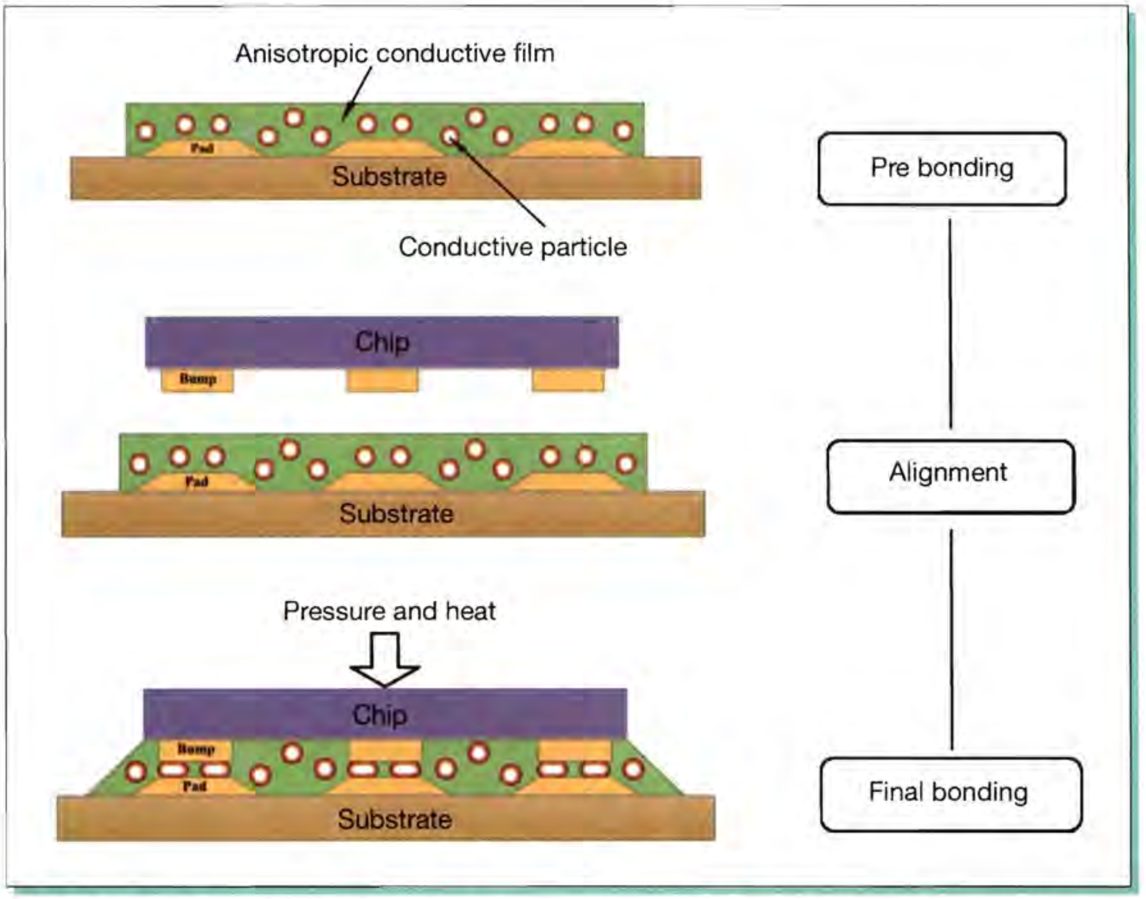


Figure 3: Flip chip bonding process using ACF

- **Pre-bonding**: The transparent layer on the surface of ACF is removed and the ACF is laminated onto the surface of the substrate, a 0.2-0.3MPa pressure is applied over the bonding area for 3-5 seconds at 90-100°C. After that, the separator layer is removed.
- **Alignment**: The IC chip is then aligned to the substrate by using the marks on the chip and substrate. Since the ACF is always used for fine pitch applications, there is a high requirement with the alignment accuracy.
- **Final bonding**: after the alignment, the heat and pressure will be applied at the back of the chip. Subject to the heat and pressure, the adhesive is permanently cured and attaches the IC to the substrate. Some particles will be trapped between the metallisation and deformed to get a good contact. The electronic conduction along the vertical direction is then achieved.

During the ACF flip chip bonding process, the control of bonding parameters such as the bonding pressure, bonding temperature and bonding time, are very important for achieving reliable ACF joints. For example, during the bonding process the bonding pressure is required to be high enough to displace the excessive adhesive so that single particles can be captured between the metallisations and get deformed. However, a very high bonding pressure is not expected since it may cause the crash of the conductive particles. In the meantime, the adhesive gets cured under the heat absorption during the bonding process. The cured adhesive can hold the deformation of the particle after the bonding force is removed. A proper temperature should be applied in order to make the adhesive start curing at the right time and proper curing degree can be achieved at the end of the bonding. A minimum curing degree is required to provide a certain level of mechanical and electrical performance in the adhesive system. Besides the bonding pressure and bonding temperature, the bonding time also needs to be controlled to make sure that there is enough time for the particle to be deformed and the adhesive to be cured.

Electrical conduction mechanism

Electrical conduction through ACFs is achieved by the mechanical deformation of tiny conductive particles contained within the cured adhesives. During the bonding process, the insulation in the vertical direction where the balls are trapped is pushed away, allowing the Ni/Au layer on the particle to conduct electricity between the IC and the substrate, while not shorting in the plane directions. Once the adhesive gets cured, the particles are locked in compressed state. The elasticity of the

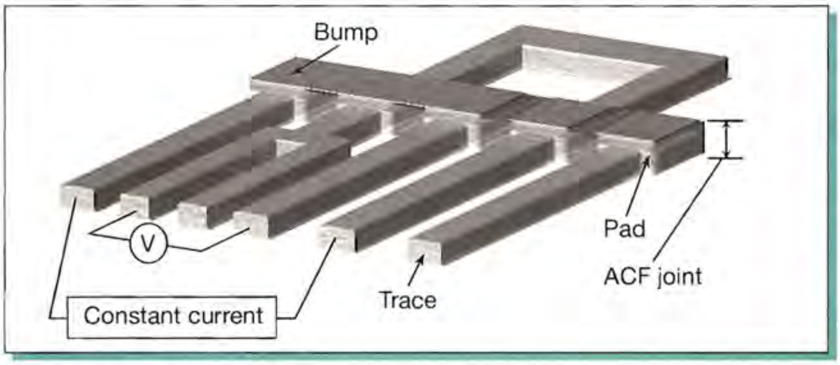


Figure 4: Contact resistance measurement of ACF joints

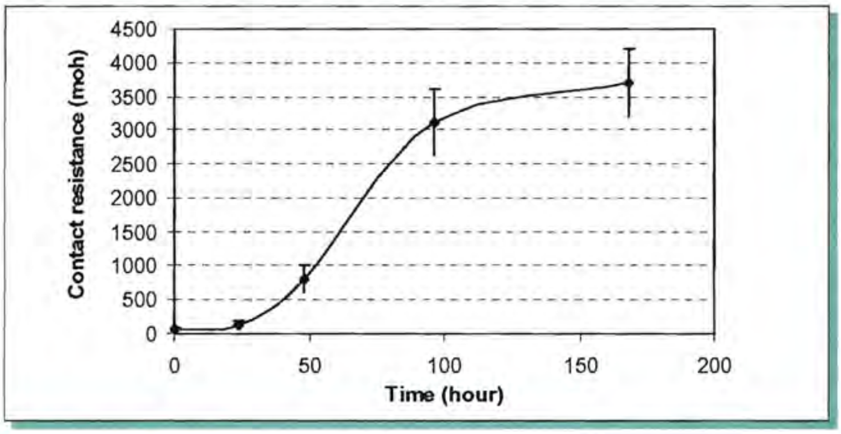


Figure 5: Joint resistance during the autoclave test

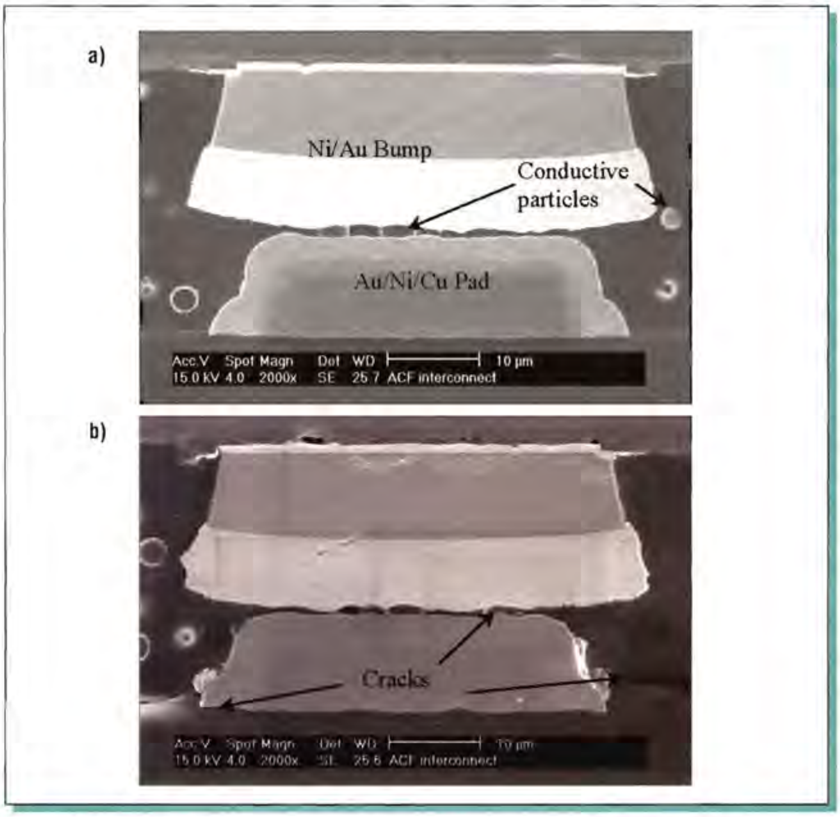


Figure 6: SEM photos showing the ACF interconnections with conductive particles (a) before autoclave test (b) after 48 hours autoclave test

compressed trapped particles causes them to constantly press outward on both contact points, helping to maintain good electrical connections. There are several factors which could affect the electrical performance of ACF joints, such as the deformation degree of the conductive particles, the curing degree of the adhesive and the particle uniformity, dispersion etc.

The joint resistance is always used as the indicator to evaluate the electrical performance of the ACF joints. A popular method to measure it is the four-point probe method. Its typical schematic circuitry is shown in **Figure 4**. In the test, 1mA constant DC current was applied to the circuit and the voltage was read from the Hewlett-Packard multimeter. The joint resistance can be obtained simply by using Ohm's Law, $R = V/I$. The joint resistance measured here is the total of the resistance of the bonding electrodes, the contact resistance between the conductive particle and bonding electrodes, and the resistance of the conductive particles. Therefore, for the same bonding electrodes and the same kind of ACF, the variation of the joint resistance can reflect the changes in contact resistance between the conductive particles and bonding electrodes, which is always used to indicate the reliability performance of ACF joints.

Reliability issues

In spite of the increasingly important role of ACFs in the assembly of electronic products, there are still concerns about the reliability of any device with ACFs in it. After all, when compared with solder interconnect material, ACFs are new materials with many unknown properties. Among the many factors that affect the reliability of ACF devices, moisture is one of the most important ones. Previous studies have revealed that the reliability of ACF is strongly affected by moisture and it is even thought of as the dominant factor in ACF flip chip failures.

The autoclave test under 121°C, 100%RH, 2atm conditions for up to 168 hours was used to evaluate the moisture effects on the reliability of ACF flip chips. The joint resistance was measured using the four-point probe method at 0h, 24h, 48h, 96h and 168 hours during the test, and the result is shown in **Figure 5**.

As shown in **Figure 6a**, conductive particles have good contact with the conductive metallisation surfaces before the autoclave test. But as shown in **Figure 6b**, the conduction gap between the conductive particles and the metallisation was clearly visible after the 48 hours autoclave test. The formation of this conduction gap signals a loss of the contact area and this leads to an elevated joint resistance.

Computational modelling procedure

For a better understanding of the experimental results, computer modelling methods were also used to analyse the moisture effects on the reliability of the ACF interconnections. The simulation of the ACF flip chip was carried out using a multi-physics software package Physica.

ACF bonding is a complicated process that involves heat transfer, fluid flow and solid deformation. In order to simplify the analysis, the stress created in the bonding process is assumed to be negligible. This means that the model is stress free at the reference temperature. Another simplification that has been made concerns the vast range of length-scales in an ACF flip chip. While the thickness of the particle metallisation is about 50nm, the die is 11mm in length: the ratio of the two is approximately $1{:}10^5$! In addition, there are thousands of conducting particles is in a typical ACF joint. All this means that an 'exact' model which includes all the particles and interconnections is simply not achievable with today's computer technology.

Therefore, a 3D macro-micro modelling method was used to predict the moisture diffusion and moisture-induced stress inside the package. At the package level (macro model), a coarse mesh was used to predict the displacement and moisture concentration through the assembly. At the ACF joint level (micro model) a finer mesh was used that captures the detail of an ACF particle. The macro model is shown in **Figure 7**. Only one quarter of the package was simulated due to the symmetry of the ACF package. The micro model which includes one ACF joint with one pre-deformed particle in the centre is shown in **Figure 8**. The macro model was used to predict the moisture diffusion and the displacement of the whole package. The displacement extracted from the macro model was used as the boundary condition of the micro model and the detailed stress analysis was performed using the micro model.

During the autoclave test, moisture from the environment diffuses into the flip chip. The transient moisture diffusion process obeys the Fick's Law of Diffusion (see **Equation 1**).

$$\frac{\partial C}{\partial t} = D\,\frac{\partial^2 C}{\partial x^2} + \frac{\partial^2 C}{\partial y^2} + \frac{\partial^2 C}{\partial z^2} \qquad (1)$$

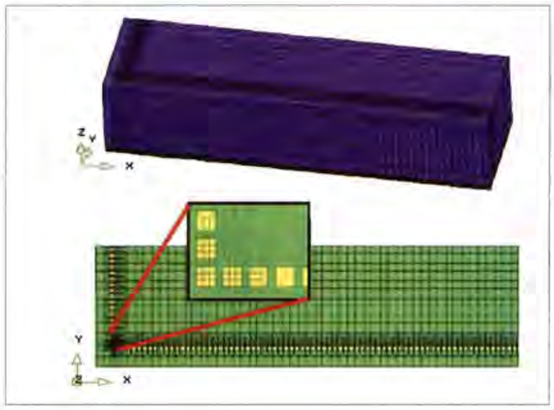
Where C = the moisture concentration,
D = the moisture diffusivity.

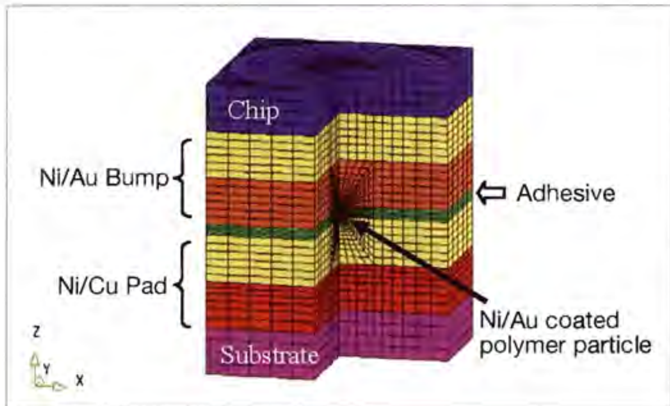
Unlike temperature, which is continuous at material interfaces, moisture concentration is discontinuous because the saturated concentration varies for different materials. This problem can be solved by using the wetness faction approach.

In the process of moisture diffusion and changes in temperature, hygroscopic stresses and thermal-induced stress are generated due to the mismatches in coefficient of moisture expansion (CME) and coefficient of thermal expansion (CTE). Assuming that the mechanical, thermal and moisture induced strains are independent, the mechanical stain is the total strain less the thermal strain due to temperature excursions and the hygro strain due to the moisture absorption.

$$\varepsilon^{mechanical} = \varepsilon^{total} - \varepsilon^{thermal} - \varepsilon^{moisture} \qquad (2)$$

The stresses can then be calculated from **Equation 3**.





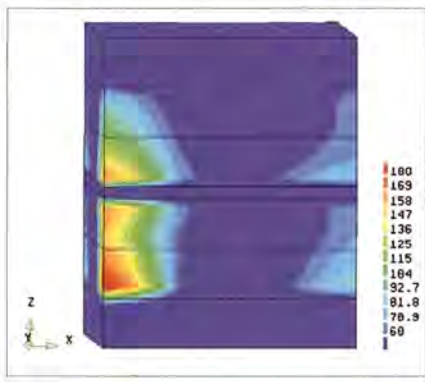


Figure 7 (Top): The mesh of the macro model
Figure 8 (Centre): The mesh of the micro model
Figure 9 (Bottom): Pattern of the Von-Mises stress distribution

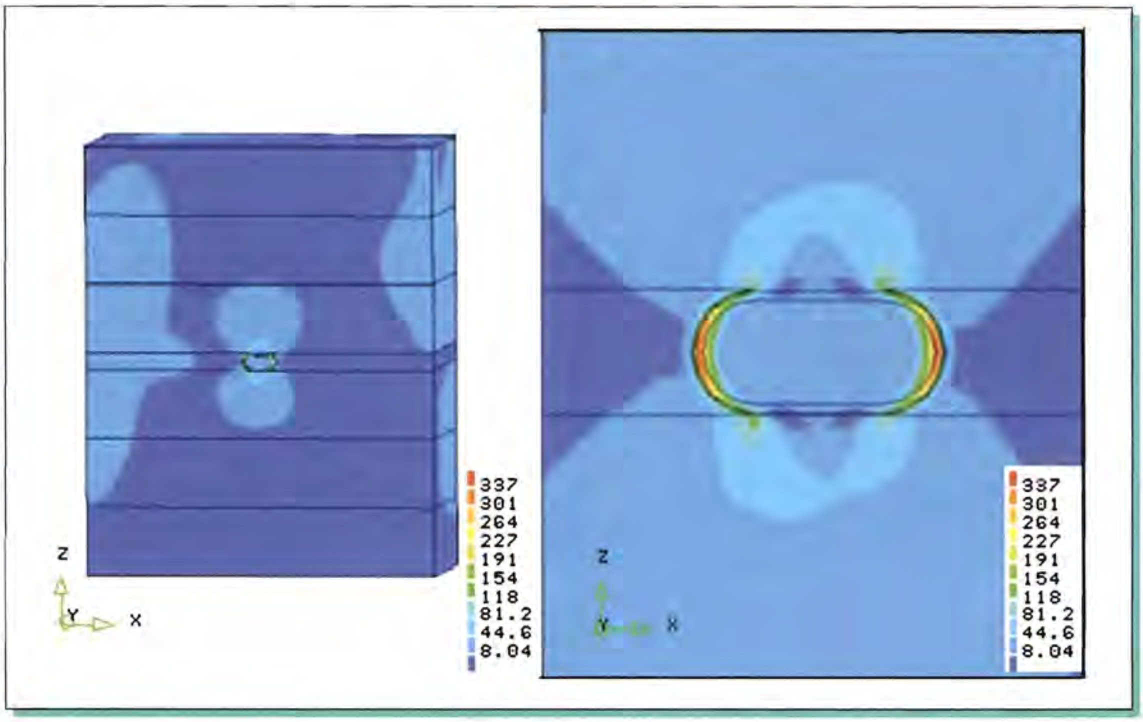


Figure 10: Pattern of the tensile stress distribution

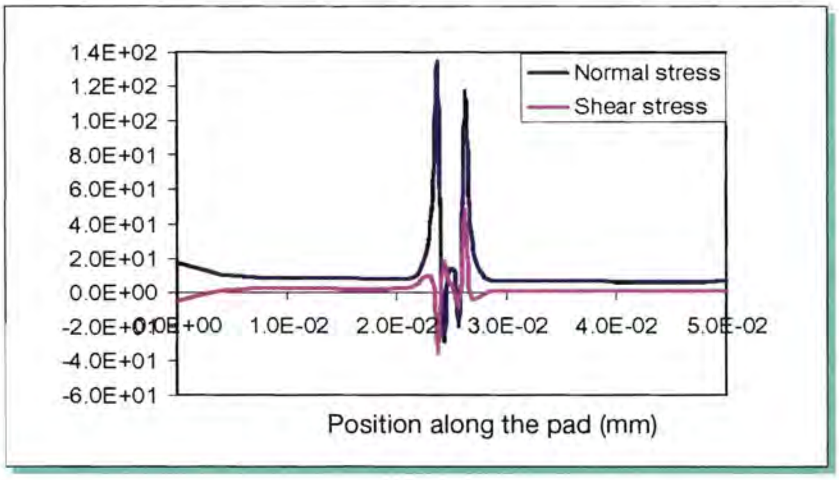
$$\sigma_{jk} = \lambda\varepsilon_{ij}\delta_{jk} + 2\mu\varepsilon_{jk} - \frac{E}{1-2v}(\alpha\Delta T)\delta - \frac{E}{1-2v}(\beta C)\delta_{jk} \quad (3)$$

Where λ, v, E and μ are the Lamé constant, Poisson's ratio, Young's modulus and Shear modulus respectively, β is the CME, α is the CTE, ΔT is the temperature change, and C is the moisture concentration.

Modelling results

The Von-Mises stresses distribution in this ACF joint due to the moisture absorption is shown in **Figure 9**. Stress concentration was found at the interfaces between the adhesive and bump/pad. The stress level is especially high at the corner where the pad, the flex substrate and adhesive meet. This is the location where micro cracks were found at the beginning of the autoclave test. The cracks can propagate along the flex/pad interface to detach the pad from the substrate or along the interface between the adhesive and substrate pad to join the conduction gap. The existence of these two forms of delamination was observed in the experiment. The normal stress distribution around the conductive particle is shown in **Figure 10**.

Figure 11: The interfacial stresses due to moisture absorption



The interfacial stresses along the top surface of the substrate pad are presented in **Figure 11**. It was found that the loading condition around the conductive particle is mostly tensile. The shear stress is not significant even though the modelled ACF joint is located at the corner of the flip chip. This means that the ACF swelling effect pushes the die upwards, resulting in higher stresses at the interface between the conductive particle and metallisation. The electric connection between conducting particles and the surrounding metallisation are formed through the contact pressure caused by the elastic/plastic deformation of the particles. This contact pressure is maintained by the residual stress in the adhesive. The loss of the electrical contact may occur when the adhesive expands in the vertical direction.

The temperature effect was analysed as well. The temperature induced stress was not as significant as the moisture-induced during the autoclave test. The moisture-induced swelling effect is concluded to be one of the major causes of the ACF joint failures during the autoclave test.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Novel Devices for Novel Circuits

Multigate devices using multiple surfaces are promising to continue the transistor's scaling down. This opens many opportunities for novel circuits says **Leo Matthew**, principal research and development scientist at Freescale Semiconductor

Planar CMOS technology has revolutionised the electronics industry over the last few decades. Moore's Law charted out the rapid and predictable miniaturisation of devices, which has allowed the semiconductor industry to make new products with added functions in each new generation of technology. Most commercial products are now in the 90nm technology node as defined by the ITRS, with work on 65nm and 45nm nodes progressing rapidly. This predictable scaling is now reaching its limit and has forced the industry to look to novel device architectures beyond the 45nm technology node.

Despite all these years of digital CMOS innovation and scaling, we have only scratched the surface of the semiconductor substrate. The planar CMOS devices – the workhorse of digital applications used in modern electronic systems – have a channel only on the surface of the silicon. These devices have a single gate on the surface of the silicon to modulate the channel. Scaling of these planar devices has now begun to hit its limits for power, noise, reliability, parasitic capacitances and resistance. New device architectures using multiple sides of the semiconductor and not just the planar surface offer a path to overcome these performance limits. In addition, these non-planar CMOS devices enable new circuits previously not possible with single gate CMOS devices.

A better switch

The fundamental function of a transistor in a digital system is to be a switch, to conduct as much current as possible when on and to shut down when off. The limits of planar CMOS technologies make this fundamental operation impractical as gate lengths and supply voltages are scaled down. The current in the on state is reduced when the device sizes are scaled down, due to reduced mobility of the electrons and parasitic resistances among other effects. The leakage currents increase when the device is turned off. This, substantially higher leakage current can drain batteries quickly making many mobile applications difficult to engineer (**Figure 1a**).

The fundamental limiting factors to scaling a single gate planar CMOS transistor are the leakage through the gate and the effect of the drain taking control of the channel, making it difficult to control the switch using the gate (**Figure 1b**). This is known as short channel effect.

In a multigate device, the channel of the device is controlled (gated) from multiple sides and the body of the device where the channel is formed is made ultra-

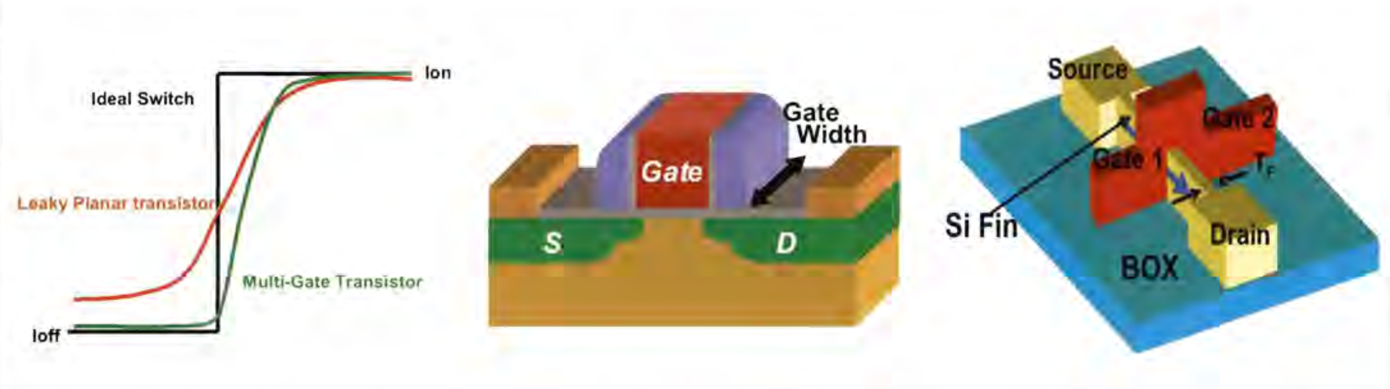
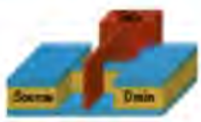
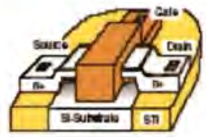


Figure 1a (Left): Ideal switch vs a good switch and a leaky switch

Figure 1b (Centre): The planar Mosfet, where the gate is only on the surface

Figure 1c (Right): Multigate-FinFET gate controls many sides

	Multiple Gate MOSFETs				
	N-Gate (N > 2)		Double-gate		
Device					
Concept	Tied gates (number of channels > 2)	Tied gates, side-wall conduction	Tied gates planar conduction	Independently switched gates, planar conduction	Vertical conduction

thin so the gate bias controls the channel more efficiently from those multiple sides (**Figure 1c**).

These multigate devices, like the planar Mosfet, still have a single gate electrode. However, this single gate electrode wraps around many sides and controls the channel from those multiple sides. Among these devices are the Mesa Isolated FET, DeltaFET, FinFET, TriGATE, MigFET and others.

In all of them, a single gate electrode controls the channel from multiple sides, yielding better control of the device. Also, the leakage is lower when the device is shut down and it conducts more current when it is turned on. A version of these devices, where the gates are separated and are independently controlling the channel, is called MigFET (multiple independent gate FET). Some novel circuits that could be feasibly constructed with this device are discussed later.

Challenges and solutions

While individual transistor structures have been demonstrated to behave better as switches than the existing planar transistors, manufacturing a complete product using these devices still has many challenges. Such challenges include process technologies, design methodologies and new compact models to represent these devices.

➢ Process technologies

The multigate device architecture requires two basic technologies that are substantially new compared to the existing process. One is the process to make very thin silicon body of the order of 20nm and the second is the process to fabricate identical gates on at least two sides of this very thin silicon. Various process technologies have been proposed to fabricate such a structure (**Figure 2**).

While many processes have been identified to make a very thin silicon channel, a process that easily allows gates on both sides of this channel that are aligned to each other has been provided only now on a structure called FinFET (**Figure 2b**). Currently, most research efforts to make multigate devices involve such structures.

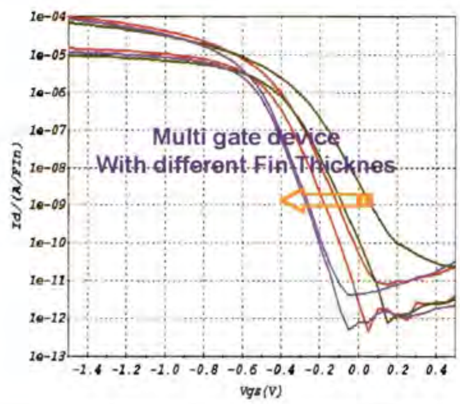
While devices with sub-20nm silicon body and gates less than 40nm in length have been demonstrated, there are still manufacturing challenges to make a product with millions of such transistors.

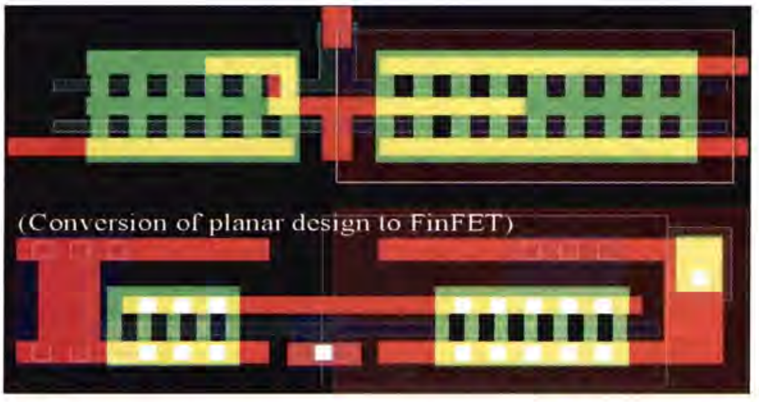
For example, the challenge to fabricate very thin silicon body has been met by process optimisations such as trimming the silicon and using non-conventional masking procedures, and dimensions as low as 10nm have already been demonstrated. The other challenge is to pattern gates over tall topography. Process changes and

Figure 3a (Left): A TEM cross-section of a FinFET with metal gate

Figure 3b (Centre): A SEM 3D view of the FinFET device

Figure 3c (Right): Characteristics of a metal gate electrode PM





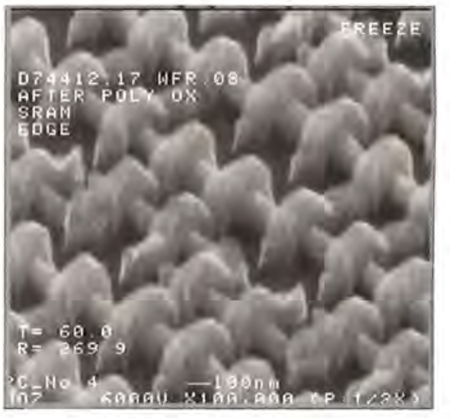


Figure 4a (Left): Planar logic gate converted to a FinFET layout. Tools to convert and generate these devices are needed

Figure 4b (Right): An array of SRAM cells patterned over 100nm topography

optimisations have been successfully used to demonstrate these gates over very large areas as in the SRAM cells area shown in **Figure 4b**.

While these novel devices make progress, new materials are also researched such as new gate materials. Incorporating these is crucial to gain the maximum benefits out of the novel structures. The use of metal gates instead of conventional polysilicon gates will allow less parasitic resistance and poly depletion effects. Although patterning these metal gates on FinFETs with traditional oxides is a challenge, they have been demonstrated using new process techniques (**Figure 3**).

➢ Design

There is substantial investment to integrate these novel devices in existing designs. It is of general view that any new technology should be able to seamlessly convert or use the existing design infrastructure. All multigate device technologies need some level of re-design to optimise the products and to incorporate new process conditions. The vertical devices, such as FinFETs, can be modified using existing design tools by converting one or more design layers. An inverter using 90nm silicon-on-insulator (SOI) design converted using an automated tool is shown in **Figure 4a**.

Such design conversion methodologies need to become part of standard EDA (Electronic Design Automation) tools to make novel devices mainstream.

Compact models

The multigate devices that control the channel from multiple sides devices are new to circuit and system designers. These devices need to be modelled to understand and predict the physics and functionality of the circuits. Compact computer models are used in design of circuits with semiconductor devices. SPICE models that represent these devices are just beginning to be developed for use in simulators.

There are new physical characteristics that now need to be incorporated into these device models. The University of Florida's Double Gate (UFDG) model is one of the earliest to address this need. The model incorporates the physics of quantum-mechanical effects that are inherent in very thin body devices.

Other effects, such as the resistance modulation with bias, parasitic effects and the use of multiple independent gates are also incorporated in it. Compact models such as UFDG allow circuit and system designers to model the systems and study

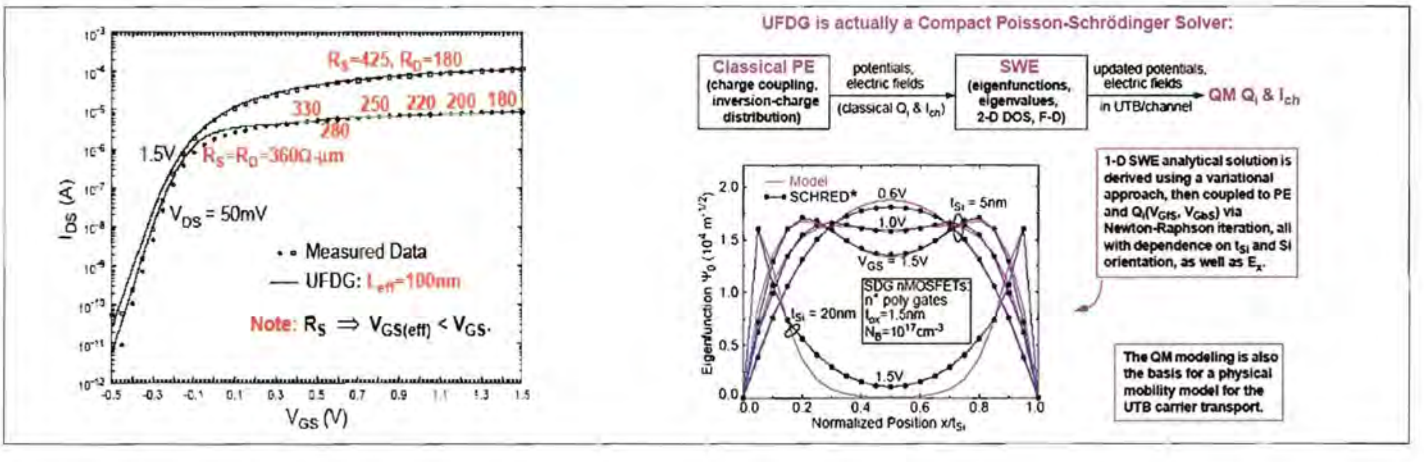


Figure 5: The compact models for double-gate devices need to consider new effects due to the second gate's very thin silicon body. UFDG is a physics-based model used for prediction and new designs

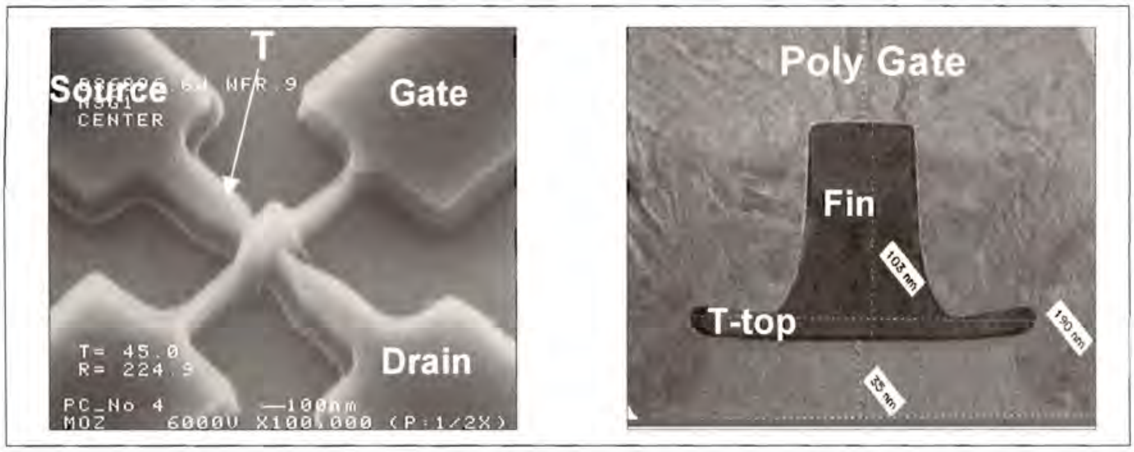


Figure 6a and 6b: The ITFET has a channel that is shaped like an "inverted T". This structure provides the advantages of both planar and vertical thin body devices

the tradeoffs for the new devices in systems but, also, innovate new circuits that are feasible due to the new device structures.

This is "IT"

The multigate device architectures are rapidly evolving. The FinFET with all its advantages still has one significant drawback – the region between the fins is not used as part of the switch. A new family of devices that uses both, the vertical and horizontal regions of the silicon, has been proposed and demonstrated for the first time. This device is called ITFET. Its vertical and horizontal thin body regions are shared like in an "inverted T" shape (see **Figure 6b**).

The ITFET offers maximum surface area utilisation on the wafer for the channel and allows optimisation of crucial circuit elements such as the SRAM-based cache that is ubiquitous in all modern digital CMOS products.

The MigFET

In a MigFET, multiple gate electrodes control a thin silicon channel using multiple gate electrodes that are separated from each other (see **Figures 8a** and **8b**). This class of devices allows new circuits and applications that were usually impractical or impossible in planar CMOS applications, where there's only one gate on the surface. Many new applications have been proposed and demonstrated using these devices such as MigFET-based 4T/6TSRAM, MigFET RF mixer, MigFET FPGA, MigFET 1T dynamic memory and others.

New logic circuits with a better switch

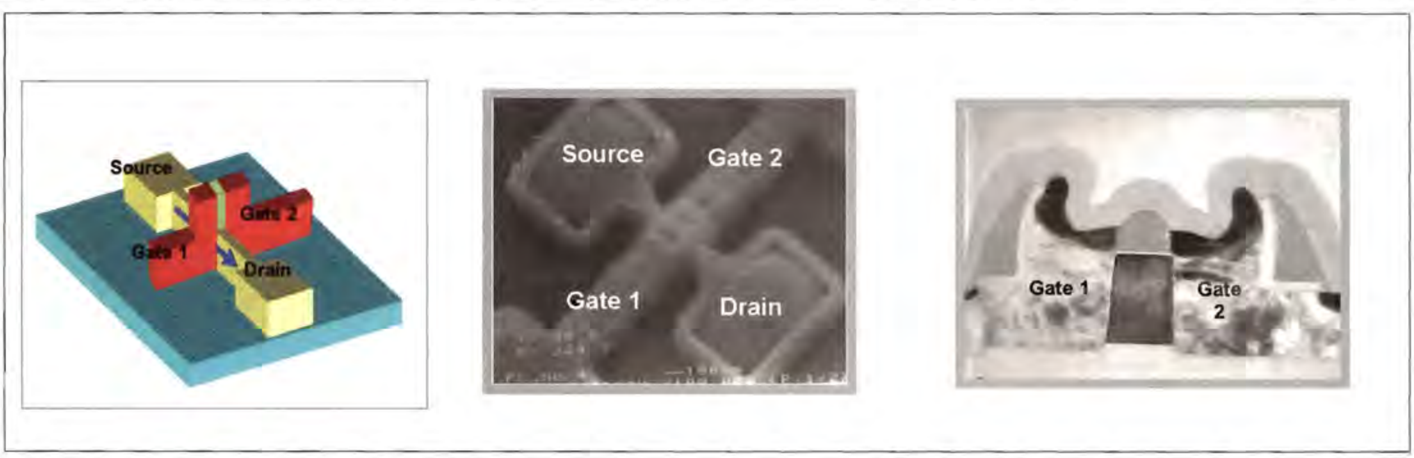
The excellent I_{on} and I_{off} characteristics of the multigate devices allow future scaling of traditional circuits for a few generations. Even this is not sufficient for certain low power applications, such as pacemakers, hearing aids and some self-powered logic devices. While sub-threshold logic has been proposed as a low power circuit alternative, it's not been widely used due in part to the limitations of the single gate devices. The multigate devices with their steep turn-on characteristics and extremely low leakage currents promise to be the ideal device to make these systems practical.

New analogue circuits

➢ **RF applications**

While digital CMOS logic leads the process technology roadmap for computing applications, the communications applications have a substan-

Figure 8a: The MigFET has independent gates on either side of a thin channel. A schematic, SEM view and TEM cross-section through it are shown



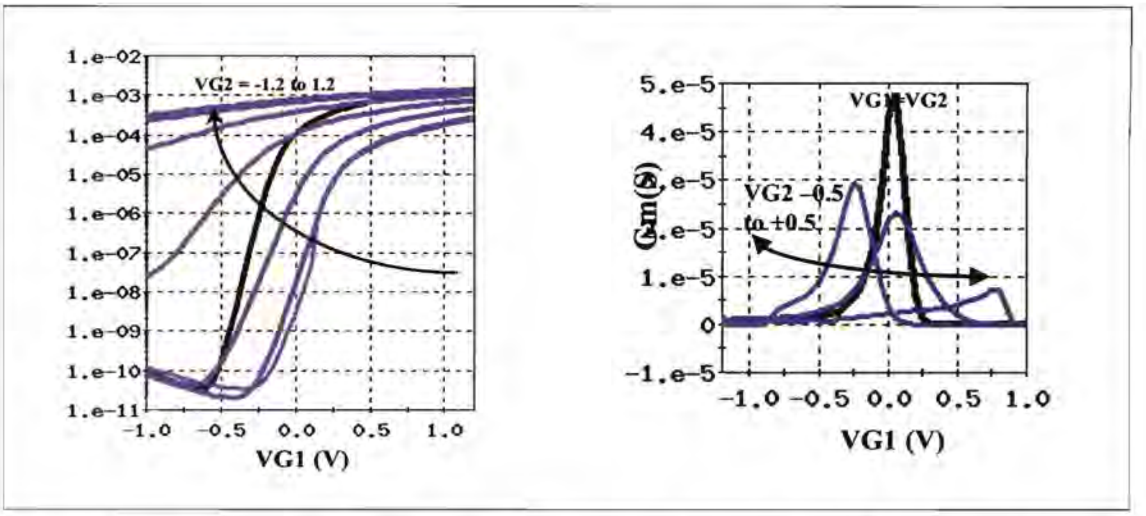


Figure 8b MigFET with two independent gates, where both gates modulate the device performance separately. Normal transistors have one gate and only one of these characteristics (in black) is possible

tial mix of analogue components that are integrated in the CMOS logic or as standalone products. The double gate device architecture allows better scaling of these analogue applications and new functions that were not possible with single gate transistors. Just as in CMOS logic, the fundamental switch is improved by the double gate architecture for analogue applications. The double gate architecture offers better gain and can be used as a better mixer, amplifier or VCO.

➢ RF mixers

The mixer is a very crucial analogue component used for frequency conversion. Wireless systems typically consist of multiple such mixers. They are integrated with the CMOS logic when possible, but with the difficulty encountered in scaling and matching the analogue devices. These devices are often forced off-chip, which in turn increases cost and complexity.

The MigFET has been studied for mixer operations and promises to be an excellent device to allow analogue scaling as the digital devices continue to shrink. It offers the unique feature of having two independent gates modulating the channel. These gates allow new modes of operation such as an RF mixer, for example. In this operation shown in **Figure 9**, the RF and LO signals used in the mixer are fed to the two gates and the corresponding mixed output is obtained. This has been demonstrated and simulation of such new circuits suggest that these devices have substantial gains up to 100GHz, which will substantially improve future wireless performance and reduce power consumption.

Novel implementations of a simple MigFET mixer have been simulated and its double-balanced counterpart has been also simulated using the double gate compact UFDG model. For the former, a small RF signal and a large LO signal applied to the two gates of a single MigFET, yield mixing via the charge coupling between the gates. Getting good conversion gain and linearity from the MigFET, while still satisfying small-size/low-voltage/low-power requirements for specific applications, can be achieved with optimal biases of the two gates and good design of the transistor. The double-balanced mixer uses four MigFETs and generally offers better conversion gain, linearity and superb port isolation, with the compromise of larger power consumption and area.

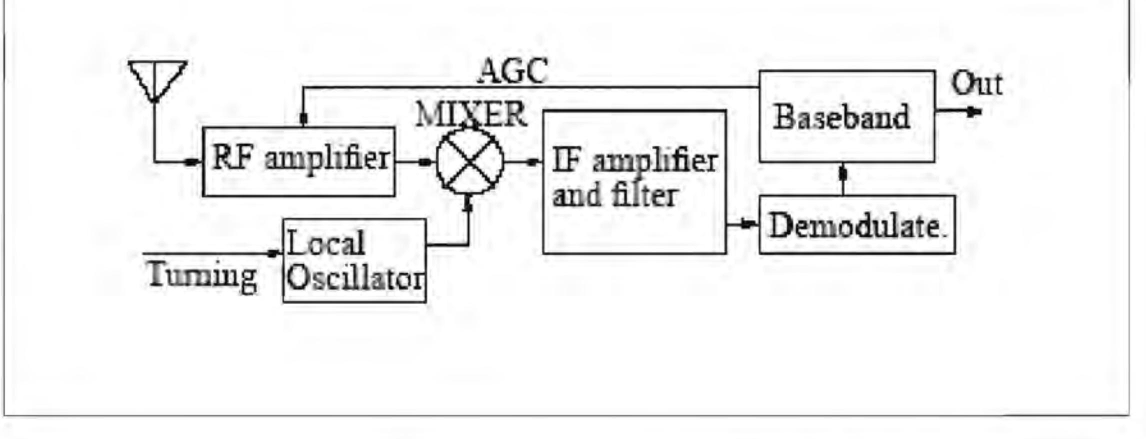


Figure 9 Wireless systems use various analogue components that can be enhanced by multigate devices. The transceiver shown has a mixer, which currently use multiple transistors can be replaced by MigFETs

New memory circuits

Substantial part of any system now is memory. High performance logic typically uses SRAM, where large data files are saved in non-volatile memory (NVM) or dynamic RAM. All three memory types can be improved using these devices in novel configurations that were not practical in single gate planar technologies.

➢ **SRAM with dynamic feedback**

Intrinsic variations and the challenging leakage control in today's planar silicon Mosfets limit the scaling of SRAM. The 6T and 4T FinFET-based SRAM cells designed with built-in feedback achieve significant improvements in the cell Static Noise Margin (SNM) without area penalty. Up to 2x improvement in SNM can be achieved in 6T FinFET-based SRAM cells. A 4T FinFET-based SRAM cell with built-in feedback can achieve sub-100pA per cell standby current and offer the similar improvements in SNM as the 6T cell with feedback, making them attractive for low-power, low-voltage applications.

➢ **1T ZRAM – high density integrated dynamic RAM**

The DRAM is one of the densest devices in the semiconductor industry. Current dynamic RAM processes are so different from planar CMOS technologies that it is usually not cost-effective to integrate these DRAMs with CMOS. The MigFET device has some floating body characteristics that enable it to be used as a 1T (one transistor) RAM, called the ZRAM. These 1T ZRAM devices are made possible because of the unique features in vertical MigFET devices, such as the additional independent gate electrode. And since the device is essentially a transistor, but can be operated as a RAM, it could be integrated with similar CMOS logic devices in products that can take advantage of large on-chip storage.

➢ **Multigate flash memory**

Non-volatile memory devices have now become widely used in automotive, communication and multimedia products. The non-volatile nature of these memories makes them very attractive in such applications.

Multigate devices allow their further shrinking. The

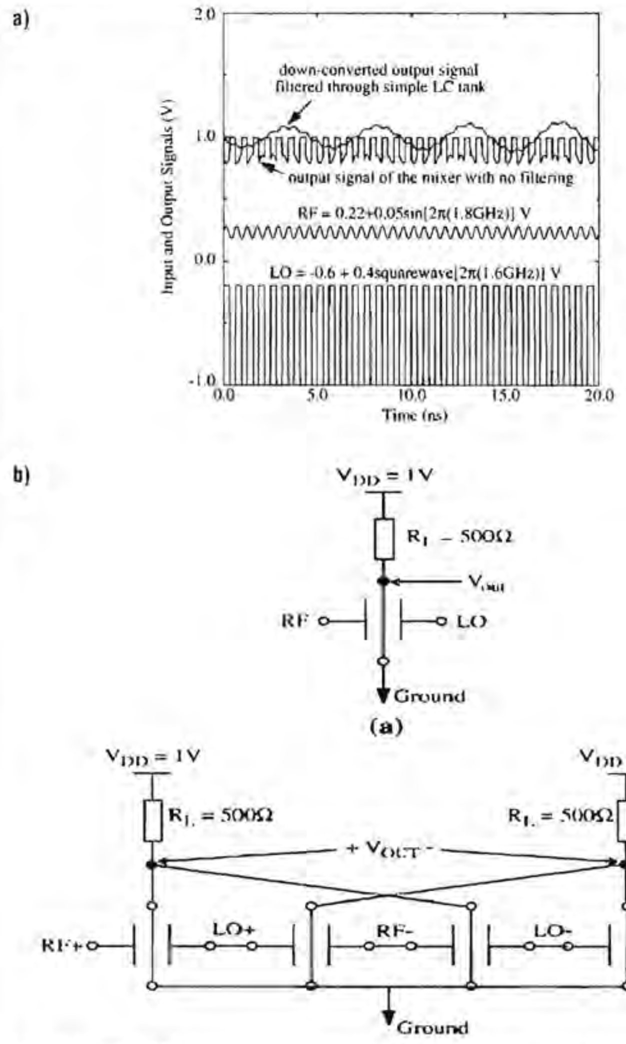


Figure 10a and 10b: Mixer schematics: (a) mixer using one MIGFET; (b) double-balanced mixer using four MIGFETs. Note that RF+/RF- and LO+/LO- are antiphase signals

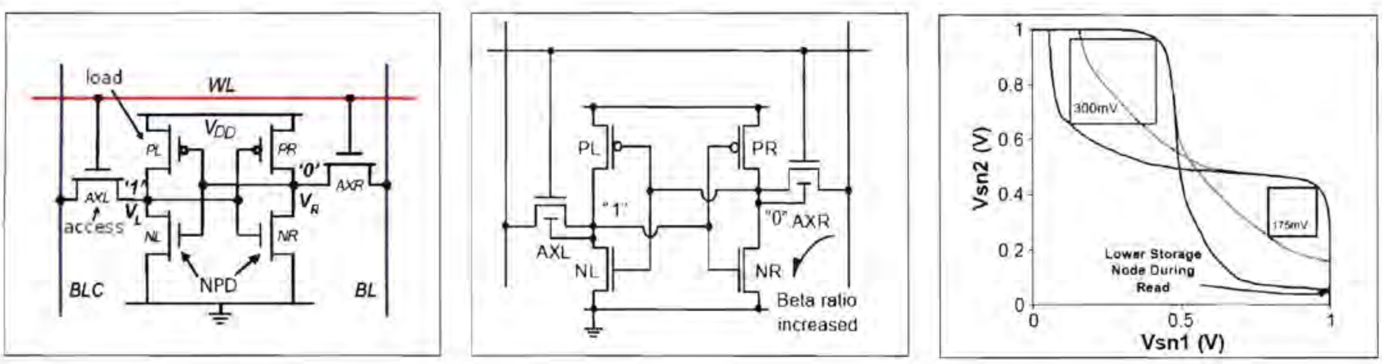
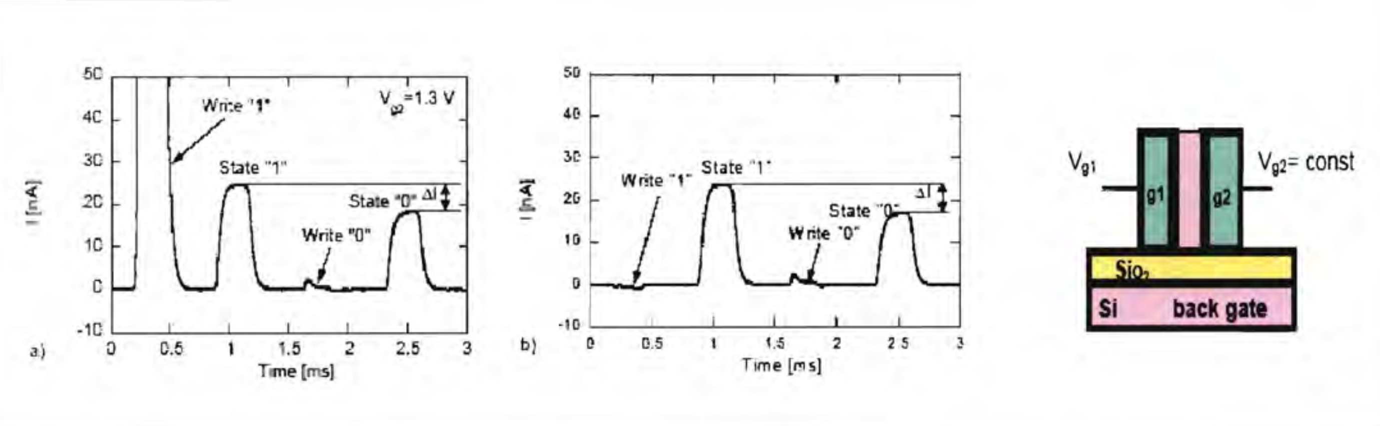


Figure 10c: The 6T SRAM cell can be substantially improved with MigFET feedback



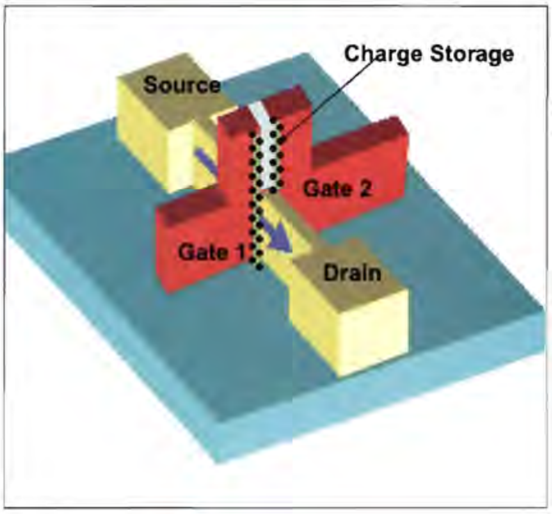


Figure 11 (Above): The MigFET device used as a DRAM. The channel between the two gates can be held floating to store data using the first gate and read using the second independent gate

Figure 12 (Right): The MigFET flash device has storage elements under both gates and can store multiple bits in each device

Figure 13: The multigate devices can be used to improve all device functions – logic/memory/analogue

sidewalls of the multigate transistor can have charge storage layers, such as silicon nitride or silicon nano-crystals. The performance of conventional charge storage layers, such as poly, can also be enhanced since they can now be formed on both sides of these vertical devices.

In combination with the multiple gate option, these devices can store multiple bits in a single transistor, increasing density and performance.

Looking ahead

With CMOS scaling reaching various limits, multigate devices offer an alternative path to increase the functions/unit silicon by providing better transistors for existing circuits and making new applications feasible.

A hypothetical product that would take advantage of most of the devices discussed here would include single-gate electrode multigate devices to reduce leakage and improve switching performance. For high performance static memory, the ITFET can be used with 6T SRAM with feedback, but would need to include a large on chip 1T ZRAM and embedded multi-bit multigate flash memory. The analogue and I/O subsystems will take advantage of the better gain and noise immunity of the multigate architecture in some circuits, such as a balanced MigFET mixer, for example.

Summary

Rapid and predictable scaling of planar CMOS devices is becoming difficult. New device structures are researched to replace the planar CMOS devices. Multigate devices using multiple surfaces are promising to continue scaling and even make new circuits feasible. These devices can provide new and better characteristics across all logic, memory and analogue device functions.

The challenges in making these devices to enter mainstream products are many but rapid strides in process, design and modelling in the last few years have delivered substantial progress.

Advancing Chip Packaging Technologies

Andy Longford of PandA Europe provides a view of the expected directions for microelectronic packaging at chip level that ties in current developments to the needs envisaged by emerging technology roadmaps

The requirements for packaging semiconductor devices have become a new technology driver for the electronics 'final manufacturing' industry. Emerging packaging technologies, currently ball grid arrays (BGA) and chip size packaging (CSP), continue to develop to meet the needs of electronic systems, driven by the trend for "smaller, faster, cheaper" devices. Yet, many of the industry-generated forecasts and roadmaps expect a multitude of options to be developed in order to meet the demand of an industry that requires ever more complex devices that exhibit both higher reliability and lower cost.

These new packages inherently utilise printed circuit board (PCB) technologies rather than the semiconductor leadframe technologies and bring to chip packaging many challenges that are beyond existing PCB capability. This gap is now creating the interest for wafer level packaging (WLP) in every type of device from diodes to DRAMs.

Packaging directions

There are three aspects that are key to the development of new packages:

- Development of package "substrate" technology
- The requirements of MEMS for application specific packaging
- The move to provide all the aspects of interconnection (Level 1 packaging) at the wafer processing stage.

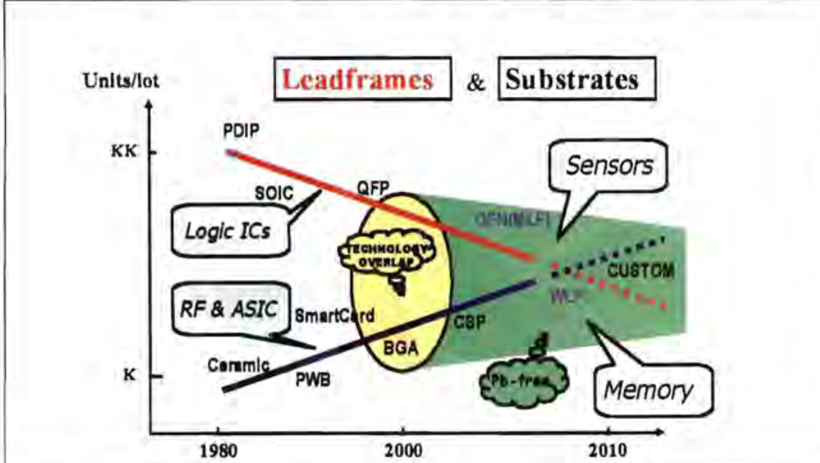


Figure 1: Development of substrate technologies

The chart in **Figure 1** indicates the past and future changes in this industry.

Lot sizes are reducing, as products have a much shorter life and because there are a number of different packaging options for the same chips, depending upon application, customer and prices need. The smartcard was one of the first to use very advanced (even by today's standards) PCB technology and this was really the start of the new technology shift.

As this overlap occurred and also brought with it the start of the lead (Pb)-free requirement, package development technology entered a new era. PCB developments suited the high pin-count options, offering low 'real-estate' footprints and low-cost tooling to get new chips to market quickly, in a type of package that was ready for production, even though volumes might be quite low. This trend was also a self-perpetuating driver, as it allowed many more chips to get to market, providing many more 'new' products, even though they might have limited life or no significant volume. The mobile phone 'killer'-application pushed hardest, needing much less package height and smaller footprint packages, and enabled a wide variety of BGAs. Inevitably, this led to the CSP packages to come to market. This trend is now supported by market figures from SEMI. They estimate that the market for laminate and flex substrates will be valued at over $4.5bn in 2007, compared to a leadframe market of less than $3bn. The forecast also shows a 15% growth in the market for ceramic packages from 2005 to 2007.

It is envisaged, as shown by industry forecasts later on, that WLP will be similarly self-perpetuating. The future expectation sees only the need for WLP chips, driven by the mobile phone and memory products, and application-specific packaging, driven by the MEMS sensors and other custom markets.

One of the key roadmaps, published in 1997 by NetPack, indicates many of the new package types that are just now coming out. However, it did not foresee the drive to WLP or the introduction of the new industry standard the QFN (quad flat no-lead) package.

In 2004, WLP became the most challenging technology for our industry. The advances in small ball size and flip chip have enabled the on-chip, on-wafer capabilities that will drive WLP forward.

The QFN package (**Figure 2**) has evolved as an interim solution to CSP, to overcome the problems associated with solder ball attach, substrate imperfections and manufacturability.

It reverts back to metal lead frame technology and

Figure 2: QFN package technologies

overmoulding, which gives additional features of power management, thermal performance and 'in situ' test capability. It removes the need for underfill and X-ray inspection at the board assembly stage, offering significant cost saving down the line.

The other key advanced technology that has emerged as a result of the developments in these packages is wafer scale packaging (WSP), a variant of WLP. Wafer scale will see development of variants of CSP, Chip on Chip (CoC) and integration of a range of different technologies at the wafer processing stage.

Technology drivers

The next generation chips will always push for innovative package designs that can handle more complexity and get board real-estate reductions. Inevitably then, the push for WLP is the ideal match, but there are many issues affecting yield, manufacturability and cost that have to be overcome. The development of such technologies is, as yet, too costly for volume applications, so for the next few years, the existing advanced package technologies will be pushed to get better performance at lower cost.

As application potentials develop, so package cost becomes the driver. In turn, low cost package solutions are becoming the drivers for new technologies such as 'last-mile' fibre optic telecom systems, 3G phones, Bluetooth, MEMS and sensors. However, only the development of standard package formats will ensure that costs are kept down.

Emerging technologies will need innovative package design that will perform well in high-speed and RF type applications, yet provide shielding against interference. The ability to manufacture high yielding products is a big driver for large chips, as yield loss due to package failure is unacceptable. Whereas opto, RF and power devices will push for smaller thermally efficient solutions, requiring package reliability in high stress environments. All of these will have to be within a 10% margin of the overall device cost.

The development of RFID tags (**Figure 3**), which utilise the tag itself as the package for the chip, is an example of innovative design and process providing a low cost (less than one US cent) package.

Figure 3: RFID baggage tags by Siemens

Application specific packages

The roadmaps for package technologies beyond current high-volume standards are based around the application needs. MEMS, opto/photonics and RF devices are expected to ramp up in volume in the next few years, driven by automotive, medical and communications markets. Hence, there are numerous programmes underway to find cost-effective solutions for manufacturing, packaging and interfacing such devices.

MEMS devices, typically sensors, are a key example of how applications are pushing the technologies to create cost-effective packaging. This market is expected to grow with a CAGR of around 17% over the period 2005 to 2008. It is being driven by major applications in automotive markets, where for example, some 100 sensors are now incorporated into a Mercedes A Class vehicle. However, package costs can be up to 80% of the cost of a MEMS device, so developing novel interposer technologies in order to achieve cost-effective, standard type packaging is key.

Innovation is required to adapt devices, if possible, into existing technologies. Matching application to package requires some form of interposer technology to encompass the function, whilst allowing standard interface connections. Such an

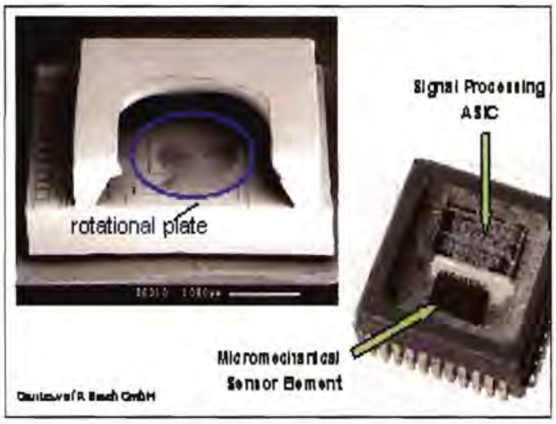


Figure 4: Bosch accelerometer device

example is shown in **Figure 4**. German firm Bosch has developed interim wafer level packaging for the MEMS unit, which is then linked to the control IC in a "standard" plastic package.

Many other companies are adopting similar techniques for road tyre pressure-sensing devices (TPMS) and opto control. MEMS gyros and accelerometers are being used in phones and laptops, as well as in vehicle airbag systems. Mobile phones use MEMS microphones and will utilise new RF MEMS security devices. MEMS are used for inkjet printing, medical blood sensing, micro medical 'on-chip' labs and many more developing applications. Most are in need of special package design, based upon standard package type with innovative interposer technologies, but many will be incorporated into modular system packages, once known as hybrids, but today known as System-in-Package (SiP).

Packaging evolution

BGA/CSP type products, however, are currently the preferred package options for handheld and other small form, feature-rich products that require high complexity and high I/O count. Memory products, in particular, are driving these package developments. The need for memory density is almost exponentially increasing and, as such, the need for stacked chips packages is evolving. The example shown in **Figure 5** is a 1.4mm thick package, with I/O count of up to 1024.

All currently produced mobile phone handsets use memory devices that have at least a two-chip stack package. The memory device makers are looking at much higher density needs in much smaller form-factors, and the likes of AMKOR, ASAT, CHIPAC and other top subcontract assembly houses are working closely with device makers to develop suitable stacked chip packaging technologies.

However, the two key areas of development, now creating the most interest, are SiP with organic substrates and WSP. The future scenarios see the

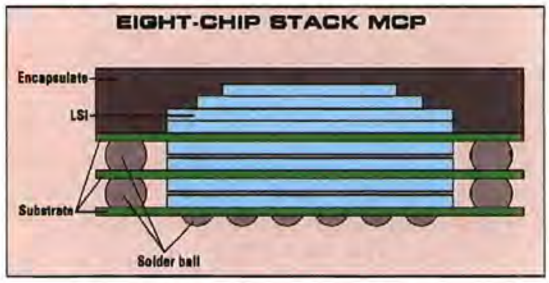


Figure 5: Stacked chip BGA package format

move through 2D and 3D system integration, where the packages have multifunctional layers, embedded passives, integrated sensors and micro interconnects as shown in **Figure 6**. The trend will push the 3D concepts to very thin, multilayer technologies, which have aspects approaching that of wafer fabrication.

Wafer scale packaging itself will continue to develop as more and more applications move through CSP into flip chip and then to CoC technologies. Some forecasters are looking at the future combination of sensor devices and control IC circuitry in nanoscale that will eventually produce intelligent electronic 'dust' or 'smart-dust'. In Figure 6, this is indicated as 'e-grain' technology and conceptual work is well underway for it to become reality.

Market trends

In a review of reports published by IC industry analysts, chip packaging will undergo a number of significant changes in the next five years. The overall growth of the market will (of course) be similar to the chip industry between 13% and 15% CAGR. This equates to a market unit increase from the 2003 figure of 85 billion units to around 143 billion units in 2008.

The advanced package technology reviewed is

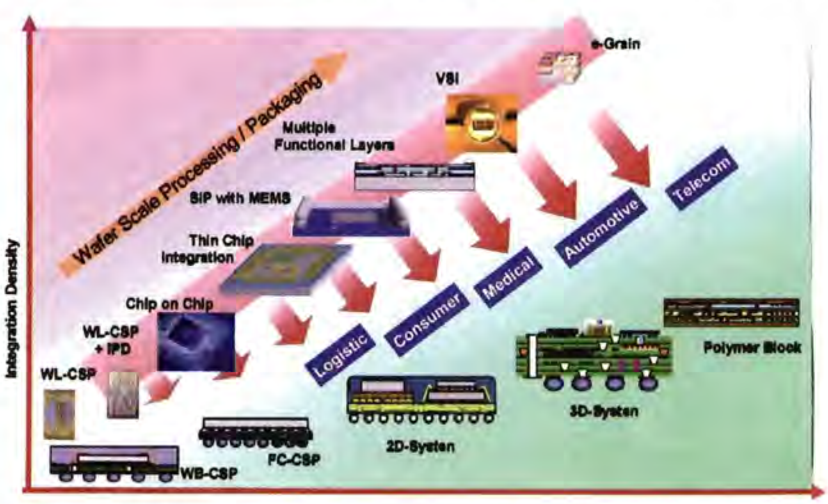


Figure 6: Advanced package trends [Source: TUB & FhG-IZM, - ISS Berlin Feb 2005]

covered mainly by the applications. The analysts see that the market for photonics will drive the need for new technologies, as will MEMS and RF.

MEMS devices will increase from a current 500 million unit market to 4.5 billion in 2008 and photonics will rise like a Phoenix from the ashes in mid-2006 to account for some three billion package units by then. Other significant applications will be flip chip package technologies, often being direct chip attach (DCA) and new SiP technologies (see **Figure 7**).

The memory market, using FC, DCA and wire-bond technology, will dominate stacked chip package growth, which is expected to be close to two billion units per year by 2008.

Without a doubt, WLP will be the strongest growth technology to evolve in the second half of this decade. The expected growth will be from around one million units globally in 2003 to some one billion units in 2008. It is the smallest IC package size as it is a true CSP and offers the lowest cost per I/O because the interconnections are all done at the wafer level in one set of parallel steps. It has the lowest cost of electrical testing and burn-in, as both these processes are done at the wafer level. The need for underfilling with organic materials around the solder joint is eliminated and the short interconnections enhance electrical performance. But the simple fact that it does require a fab-like processing facility will initially see only key market take-up and, hence, a limitation to actual available volumes in the next few years.

Downstream challenges

The manufacturing processes being developed for emerging package technologies do need to be aware of the issues of downstream handling, both for test and board assembly. For example, the size of pitch of I/O reducing below 0.3mm (300nm) will create alignment problems in handlers. Lead-free finishes on pins and ball array contacts can be problematic for test probes and Pin 1 markings will be lost when chips are flipped into DCA or stacked package applications.

The need to do die level test or system level test may have to be decided at the design stage, because when new high-density CSP and BGA stacked packages are used, and especially the use of CoC technology, access to device interconnections will not be possible.

For MEMS, opto and RF devices, static and dynamic tests will be required. MEMS devices will require additional media (pressure, gases, liquids etc) to enable functions to be tested. This means slow throughput and higher cost. Opto devices need additional care, hermeticity, clean surfaces and three-dimensional alignment, in order to accurately assess functionalities. Photonic alignments (fibre and chip detectors) need to be dynamically set during the test phase, unless package development can get in-built location features to sub-micron accuracies.

Wafer level packaging will use full clean-room processing and testing accordingly, before dicing and insertion into applications. The marking issues and Pin 1 detection, will be just some of the challenges for handling all the stages of this technology. However, using standard wafer processing and test data protocols, WLP will ideally be adapted to fast automatic assembly applications, excluding the need for additional packaging. In fact, this level of packaging will effectively become the standard "no package" option, wherein the wafer fab (foundry) will ship tested wafers directly to the end user.

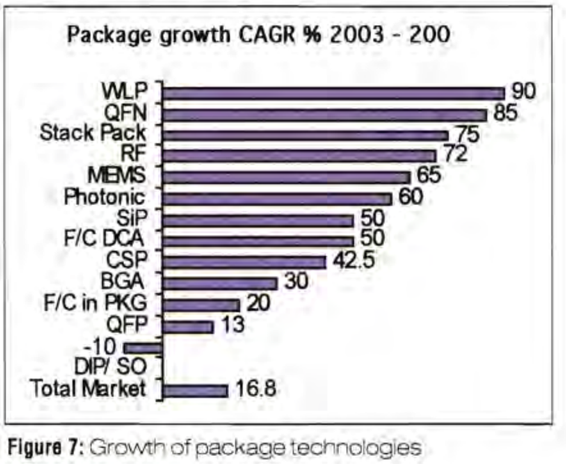


Figure 7: Growth of package technologies

Packing it in

It is clear that in the long term, the new and emerging packaging technologies are in danger of exploding in options and cost. The industry drivers need to work closely with all aspects of the manufacturing, from chip design through package design and test issues. They must also consider the system issues, which require an understanding of the handling and board system constraints of future applications.

The market is continually demanding advanced packaging technologies to deliver even smaller devices that will match the need of faster chip-speed applications but will continue to be a cheaper option than before. The chip packaging, also known as 'back-end' or 'final manufacturing' industry, will require the development of significant new 'standard' final manufacturing, that is in packaging, assembly and test processes, in order to achieve the desired faster time-to-market at lower cost. It is likely that the WLP ultimate goal of "fab, test and ship" will be the only viable future solution.

The Led Head MG504:

A Photographic Enlarger Light Source Using LED

One of **Huw Bevis Finney** hobbies is photography, another is electronics. Here, he presents his photographic project that uses light emitting diodes

To aid my printing I purchased an RH Designs Analyser. This is used to measure the light on the enlarger baseboard and calculates the exposure and grade required. It was used for a while with multigrade paper and filters (see 'Black and White Multigrade Printing') and performed well.

Light emitting diodes (LEDs) would make a good illumination source for an enlarger. However, until the advent of the high brightness ones, this was impractical and still a bit dim, even with a side-by-side array of LEDs.

LEDs' advantages include low heat output, long life, constant colour and small size. When high intensity LEDs became widely available I decided to make a light source for my then current enlarger using four (two green, two blue) LEDs from Lumileds.

Recently, I started using a much larger camera and enlarger so it was back to filters for contrast control until I designed and built the subject of this article the 'Led Head MG504'.

Enlarger and light source

Simply put, the requirements of an enlarger and light source are "to project a sufficiently bright image of the negative onto the sensitive paper with even illumination". Traditionally, this has been done in two ways – condenser and diffuser.

The condenser approach was used in my first LED enlarger project, but as the size of the negative increases so does the size of the condensers, and at 5" x 4" these would be over 6 1/2" diameter and cost a small fortune, so for this project a diffuser is used. The diffuser has one main drawback, however and that's inefficiency. Only a small percentage of the light generated is used to form the image, this means a lot of LEDs: 12 blue, 18 green and two red LEDs. At £4 a piece, they work out at about half the cost of a decent pair of condenser lenses alone.

The reason for using different number of LEDs revolves around the paper; the paper is more sensitive to blue light than green and 12 LEDs is the minimum needed to give an even illumination. The two red ones are for a 'safe' illumination to allow for positioning of the paper, which does not have to be even, just visible. To put the brightness of these LEDs in perspective, the original light source supplied with the enlarger was a diffused one using a 250W halogen bulb; the Led Head has equivalent exposure times.

The electronics

The LEDs used have a maximum current rating of 350mA and drop about 3.5V. Having a 24V 2A power supply available led neatly to three green and two blue strings of six LEDs in series and the two red LEDs in another. The worst case current is when all the blue and green LEDs are on at full brightness; the reds can't be on in this mode (see 'The switches' right) and have 50mA for the rest of the electronics, which is 1.8A.

The current is handled by six linear sinks, the three green and two blue ones controlled from PWM outputs on the PIC via low pass filters, with the red directly from an output pin. A 7805 is also included to supply the +5V rail. The output transistors are mounted on the metal chassis of the unit with isolating pads for heatsinking. The 7805 is also mounted on the chassis without a pad to connect 0V to chassis. All of this is on the rear PCB.

The old saying "if it needs more than three chips then throw a PIC at it" holds here: the control of the whole system is done by a PIC16F877 microcontroller. It is much more powerful than required but has enough I/O pins, the latest Microchip offering of In Circuit Debugging (ICD) built in and it only costs a few pounds.

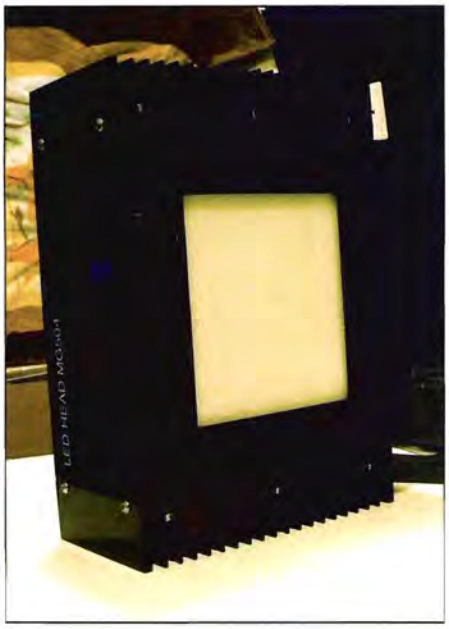
On the subject of ICDs, I wholeheartedly recommend that anybody thinking of using PIC micros gets the Microchip ICD system. I have no connection with Microchip other than being more than happy with their products.

The micro reads the three front panel switches, monitors the remote (more of which later) and foot switch inputs, and drives the display and the two PWM outputs. The display is one of HP's four digit dot matrix types. To indicate the switch functions I used some rectangular area LEDs and, using Letraset, labelled them; normal front panel lettering is a bit hard to see in a darkroom. In addition, switching increases the brightness of the LED associated with the switch.

The switches

The switches are on-off-on SPCO type and function as follows:

- Right hand up, auto mode (see lower down);



Far left – A shot of the diffuser surface when lit, this is with the room lights on demonstrating the enormous light output of the LEDs. The camera used attempted to expose correctly for the whole scene leaving the room black

Left – Showing the diffuser surface which when in use points down towards the negative to be enlarged

Lower left – A view of the front of the unit showing the grade display digits and selector switches with illuminated legends.
Also includes the IDC socket far left

Bottom – The LedHead on my DeVere 504 enlarger, ready for use

- Right hand centre, manual mode, exposure via external foot switch;
- Right hand down, manual mode, expose.

Manual mode:

- Middle centre, red off, focus off;
- Middle down, focus light on, overridden by expose;
- Left up, increase grade;
- Left centre, no action;
- Left down, decrease grade.

Auto mode:

- Middle up, red on;
- Middle centre, red off;
- Middle down, left up, left centre and left down, no function;
- Grade setting, focus and expose light controlled via serial interface.

A couple of clarifying points are required here. Focus light, for this I turn on all the blue and green LEDs at full brightness, giving a brighter image for focusing. Expose light, the blue and green LEDs are set to differing brightnesses depending on grade.

Remote control

The RH Designs Analyser displays the grade required and also times the exposure for a conventional enlarger via a relay. It is left up to the user to insert the correct filter for exposure and remove the filter when measuring the light on the baseboard.

To save time, I designed a small PCB to fit under the 40pin DIL of the processor in the analyser, which decodes the display (using another PIC), detects the safelight and expose relay drive signals and sends this data in a serial stream. The format of the data is low=idle then 1 high start bit, a low sync bit, 4 bits describing the grade (1 to 13 for 00 to 5 in 0.5 steps) and two bits indicating focus and expose. This is sent out at 1.024ms per bit with a 3:1 idle to data ratio, making data recovery easy. Getting 'into' the analyser was quite easy. RH Designs furnished me with a circuit diagram of the unit and helped out whenever I had a query. I wish they had done a serial out, there are a couple of pins left on the micro, after all.

In use

I have been using the Led Head for some time now and I can't see myself going back to filters. Surprisingly, even though this is a 5x4 head, it copes with 35mm film (36x24mm) without excessive exposure times. Some of the lower light available when enlarging 35mm is offset by the larger aperture of lenses used here.

Black and White Multigrade Printing

To fit the density range (peak to peak signal) of different black and white negatives on to the printing paper, the contrast range (gain) of the paper must be chosen. The choice of paper contrast range is called the 'grade', there are two main methods of getting the grade required.

Paper is obtainable in different grades, usually 1 to 5 in whole grade steps, and as variable contrast paper. Obviously, stocking all the grades, surface finishes and all the sizes in fixed grade paper is at best a compromise and, given Murphy's Law, the one you want won't be in stock. Variable contrast paper, however, only has to be stocked in sizes and finishes. The variable contrast is achieved by controlling the colour of the light reaching the paper.

One system (Ilford 1950's) used two sensitive layers on the paper, a high contrast (high gain) layer sensitive to green light and a low contrast (low gain) one sensitive to blue light. This had the problem that black at the extremes of the contrast range was made of one layer only, so the blacks where less intense compared to the middle contrast black.

The current system from Ilford uses a mixture of three emulsions, all with full blue and varying green sensitivities, blue light affects all at once giving high contrast and green light affects them one by one leading to a low contrast image. Filters are obtainable which, when placed in the light path of the enlarger, give the contrast required.

Great opportunities lie ahead for the SRD industry

By Mike Brookes

December being the month for reflection and celebration is also a good time to review developments in the Short Range Device (SRD) world.

The most far-reaching change in the world of radio standards and regulations for SRDs has been the practical completion of the overhaul of the creaking generic standard EN 300 220. This has been as excellent workhorse for several years but was in need of upgrading to stimulate a new breed of devices.

EN 300 220, now in two parts (not three as earlier), has completed its public enquiry and resolution stages and should be on the statute books by the beginning of 2006. It incorporates, for the first time, the use of LBT (ListenT) and AFA (Adaptive Frequency Agility) techniques. These move SRDs away from the old concept of fixed spectrum, defined channel use to that of greater spectrum efficiency – but less certainty.

SRDs using LBT will be applied initially in an extended band 863-870MHz. No detailed channel plans will be incorporated and equipment will be permitted to act in narrow band (to 25kHz) or wideband (to 200kHz), in roles using the LBT facility to detect interference on an initially selected channel and the AFA facility to hop to another unused channel. The channel width used will depend on the required data rate.

Simultaneously, the overall European 'controller' of radio regulation (ECC – European Communications Committee) frequency management sub-group has agreed the necessary changes to accommodate the revised standard incorporated in a revision, shortly to be published, of the CEPT/ERC Recommendation 70-03 – the "essential manual" for all SRD users and producers.

Following hot on the heels of these changes will be the revolutionary facility of SDR (Software Defined Radio) also known as Cognitive Radio. SRDs incorporating SDR will be enormously versatile, being able to interpret both optimum spectrum use and 'channel width' to meet data transmission rate demands.

Chipsets are already available on the market incorporating LBT/AFA and are in advanced development to incorporate SDR. More importantly, from the user or integrator viewpoint, they are extremely low cost – less than $5.

> *"The increasing use of digital techniques in audio systems is blurring the division between data and audio"*

Their advent gives some headaches – with LBT/AFA the duty cycle concept becomes moribund, as does the, until now, untouchable concept of protected channels, since the new units can hop to avoid interference. Added to this, the increasing use of digital techniques in audio systems is blurring the division between data and audio. Combined systems using the flexibility of auto-adjustable data rates and optimised data compression algorithm/protocols to make audio intelligible in non-100% channel usage scenarios are inevitable.

A further development calculated to cause the rapid evolution of new SRDs is the advent of super lightweight long-life batteries, again at low cost and high reliability. The availability of very low cost SRDs coupled with such power gives the 'fit and forget' sectors of the SRD industry just the conditions needed for explosive product development and growth.

Whereas until now, except for radio car keys, volume SRD products have been rare. However, these will now be progressively the norm with RFID, auto-metering and medical device systems not far behind.

Undoubtedly, problems will arise from high population density of SRDs in the future – but what great opportunities for entrepreneurs to make this industry the success of the next few years.

The Low Power Radio Association is a European trade body that represents manufacturers and users of short range devices (SRDs).

Mike Brookes is LPRA's chairman.

Various PIC microcontrollers

TIP 1: Switching off external circuits/duty cycle

All of the low power modes in the world will not help your application if you are unable to control the power used by circuits external to the microprocessor. Lighting an LED is equivalent to running most PIC microcontrollers at 5V – 20MHz. When you are designing your circuitry, decide what physical modes or states are present and partition the electronics to shutdown the part of the circuitry that is not needed.

EXAMPLE:

The application is a long duration data recorder. It has a sensor, an EEPROM, a battery and a microprocessor. Every two seconds, it must take a sensor reading and scale the sensor data.

Solution 1 and 2 (see schematics on this and adjacent page)

The system shown in **Figure 1** is very simple and, clearly, has all of the parts identified in the requirements. Unfortunately, it has a few problems in that the sensor – its bias circuit and EEPROM are powered all the time. To get the minimum current draw for this design, it would be advantageous to shut down these circuits when they are not required (see Solution 2). Here, I/O pins are used to power the EEPROM and the sensor. Because the I/O pins can source 20mA, there is no need to provide additional components to switch the power.

TIP 2: WDT alternative wake-ups

Most applications control the power of the microprocessor by periodically going to SLEEP. There are two ways to wake up a sleeping PIC microcontroller:

1: Receive an interrupt

2: Wait for the watchdog-timer

The nanoWatt PIC16F/18F devices have a low current watchdog timer (WDT) that draws 2-3μA. Additionall, the PIC18F devices can also dynamically turn on/off the WDT for even more current savings.

TIP 3: Stretched dog

The WDT is commonly used for waking up a sleeping PICmicro MCU. The longer the PICmicro MCU stays asleep, the less power most applications will take. Therefore, it is appropriate to have a watchdog time-out duration that is long enough for your application. If the application requires data samples once per minute, then the WDT should wake-up the PICmicro MCU once per minute. Newer PICmicro microcontroller devices, such as the PIC18F1320, have an extended WDT that allows the watchdog period to be stretched up to two minutes.

TIP 4: Power budgeting

Power budgeting is a technique that is critical to predicting current consumption and battery life. See **Table 1** opposite.

The following example shows the power budget for Solution 2 in Tip 1.

Computing battery life

Typical coin battery	Capacity mAH	Live (H)	Life (Years)
CR1212	18	3446808.511	393.47
CR1620	75	14361702.13	1639.46
CR2032	220	42127659.57	4809.09

After completing a power budget, it is very easy to determine the battery size needed to meet the application requirements. If too much power is consumed, it is easy to determine where additional effort needs to be placed to reduce the power consumption.

TIP 5: Undirectional brushed DC motor control using CCP

Figure 1 shows a unidirectional speed controller circuit for a brushed DC motor. Motor speed is proportional to the duty cycle of the Pulse Width Modulation (PWM) output on the CCP1 pin. The following steps show how to configure the PIC16F628 to generate a 20kHz PWM with 50% duty

Solution 1

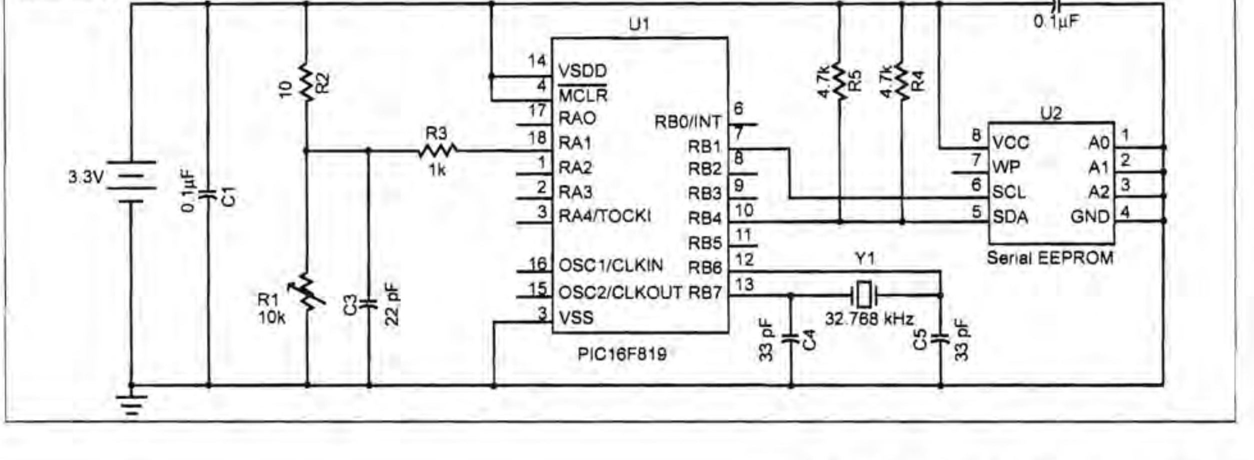


Table 1

Operation Modes	*Time in Mode (mS)*	*Current in Mode (μA)*	*μAmS in Mode*	*Description*
Sleeping	1989	1	1989	Waiting to read the data
CPU		1		
Sensor		0		
EEPROM		0		
Sensor Warm-up	1	166	166	Stabilising the sensor
CPU		1		
Sensor		165		
EEPROM		0		
Sensing	1	213	213	Reading the sensor
CPU		48		
Sensor		165		
EEPROM		0		
Scaling	1	48	48	Scaling the sensor data
CPU		48		
Sensor		0		
EEPROM		0		
Storing	8	2048	16384	Writing 2 bytes (4mS per byte)
CPU		48		
Sensor		0		
EEPROM		2000		
**μAmS	18880			
converting to mAH	5.2μA			

cycle. The microcontroller is running on a 20MHz crystal.

Step 1: Choose Timer2 prescaler

a) FPWM = FOSC/((PR2+1)*4*prescaler) = 19531Hz for PR2 = 255 and prescaler of 1

b) This frequency is lower than 20kHz, therefore a prescaler of 1 is adequate.

Step #2: Calculate PR2

PR2 = FOSC/(FPWM*4*prescaler) - 1 = 249

Step #3: Determine CCPR1L and CCP1CON<5:4>

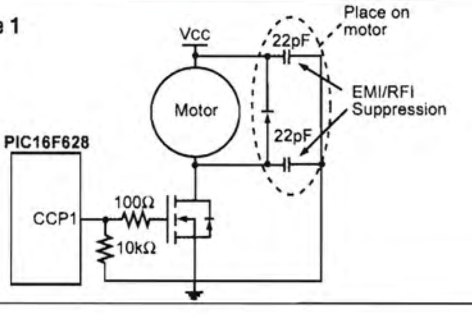
a) CCPR1L:CCP1CON<5:4> = DutyCycle*0x3FF = 0x1FF

b) CCPR1L = 0x1FF >> 2 = 0x7F, CCP1CON<5:4> = 3

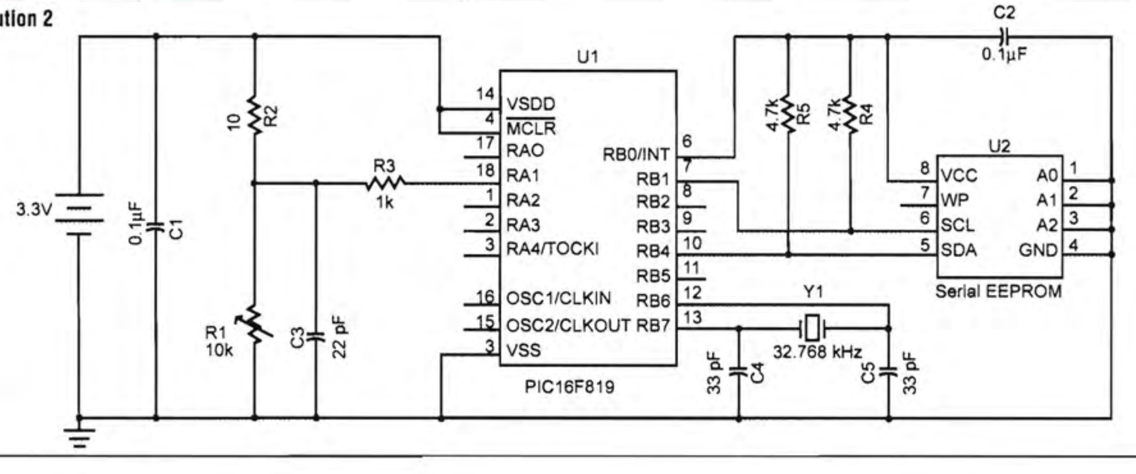
Step #4: Configure CCP1CON

The CCP module is configured in PWM mode with the least significant bits of the duty cycle set, therefore, CCP1CON = 'b001111000'

Figure 1



Solution 2



Win a PICkit2 Flash Starter kit

Electronics World is offering its readers the chance to win a new Microchip PICkit 2 Flash Starter Kit. The new PICkit 2 Flash Starter Kit enables engineers, students and anyone with an interest, to easily begin development and experimentation with PIC microcontrollers. The PICkit 2 follows the very successful PICkit 1 offering improved ease of use, faster programming and greater flexibility.

The PICkit 2 Starter Kit connects to any personal computer via full-speed USB 2.0, which allows firmware upgradeability, and requires no additional power supply for the programmer or target application board. The PICkit 2 comes with a set of easy-to-understand tutorials that allow users to learn at their own pace. In addition, the PICkit 2 can easily plug into development boards via In Circuit Serial Programming (ICSP) technology.

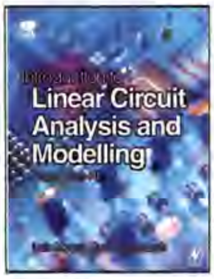
The kit includes the programmer, USB cable, CDs and an 8/14/20-pin evaluation board. Initially, the programmer supports 33 different low pin count, Flash PIC microcontrollers. For additional information visit the Microchip Web site at www.microchip.com/tools

For the chance to win a PICkit 2, log onto www.microchip-comp.com/elecworldpickit2 and enter your details into the online entry form

Introduction to Linear Circuit Analysis and Modelling - From DC to RF

Luis Moura, Izzat Darwazeh

Elsevier (Newnes)



This is a good textbook for students of electric or electronic engineering. It can also be read by anyone interested in learning the theoretical basics of circuit analysis, from DC to RF.

The authors start with the very foundations of electric circuits and move on to advanced topics such as Radio Frequency (RF) concepts and techniques, statistical concepts, noise in electric circuits etc. Their goal is to explain how electrical networks are modelled inside a simulation tool, to get the best results from it.

Each chapter comprises examples, for a better understanding of each presented argument, and exercises.

The mathematics is very clear, and there is just enough of it to develop the subject. A companion website provides all the solutions for final problems, examples with SPICE and MATLAB to practically show what has been explained in the text, additional teaching material, a list of errata and further developments on many arguments.

Chapter One introduces voltage and current, passive components, sources. Then it shows first circuits, Kirchhoff's laws and networks main theorems.

Chapter Two is a nice trip around complex numbers and their exponential and trigonometric forms.

No surprise in discovering that **Chapter Three** is about the frequency analysis. Phasors, transfer function, Fourier series and transforms, Bode diagrams: they all are explained in sequence.

Chapter Four deals with analysis in the time domain and introduces the Laplace transform.

The so-called two-ports are treated in **Chapter Five**, along with their representations. The authors show Z, Y, Chain sets of electrical parameters, introducing the automatic matricial analysis, which stays at the foundation of any circuital simulator. During the talk about two-port network analysis, Miller theorem shows all its usefulness.

Chapter Six is about amplifiers. In about fifty pages, one can find almost all the important things: what are band and gain for an amplifier, what is the low-frequency, high-frequency and middle band response. Then, there are the four small-signal models for amplifiers in mid-band: current-amp, voltage-amp, transimpedance-amp and tranconductance-amp.

Later in the chapter, one will encounter the op-amp and its main arrangements, and the concepts of reaction.

The next argument involves devices for the linear electronics: the P-N Diode, the BJT, along with its non-linear Ebers-Moll model and its linear hybrid model, the Greek Pi model and others.

Then, the Mosfet holds the scene, with its large-signal model and its low-frequency, small-signal model.

Carrying on, a high-frequency model for an active device is also explained. The common-emitter amplifier is introduced; the approximate method of time constants is used to determine its band.

At the end of this chapter, there are the differential pair and the current mirror.

Chapter Seven treats RF. The transmission line is described and modelled. You can read about standing wave, lossy lines, microstrip lines and others. At this point, the S-parameters are introduced and associated with power on the line. The Smith chart is showed and its usage explained in detail.

The last chapter is **Eight**. It focuses on noise in electric circuits. It goes incredibly deep in the subject. It's interesting to read not only for students, but also for many engineers already working in this field.

Before introducing the argument of noise, the authors intend to teach the basics of random variables and stochastic processes. This is the part of the book in which the maths becomes heavy. However, all the functions and parameters used in the book are in the Appendices, for an easy consultation.

This text can be very useful. It is easy to read, despite its richness and comprehensiveness. In this one book you will find what you'd normally find in three:

- Linear circuit analysis
- Two-ports and amplifiers, and a description of active devices
- Good treatment of RF and noise.

Maria Flora Torretta

Op-Amp Applications Handbook - Analog Devices

Edited by Walt Jung

Elsevier (Newnes)

If I had to get rid of all my technical books except one, which would I keep? This book would have to be very high on the list. So why would anyone need a reference book on op-amps? Well, despite all the media hype about the digital age, when it comes to interfacing, we still live in a fundamentally analogue world. It is hard to find a digital product that doesn't feature an op-amp somewhere, but with so much emphasis on digital technology, the theory of op-amps is often overlooked by modern students. This book will help to fill the knowledge gap.

The book is not merely a vehicle for pushing Analog Devices Inc's products, and although these obviously feature, it is much more broadly based than that and reference is made to major contributions from other manufacturers, especially in the historical context. Each chapter is followed by a short and useful bibliography. Although the book features contributions from a number of sources over many years, it does not fall into the discontinuity trap like so many compilations. It is very structured and readable, and the information flows smoothly from one chapter to the next – a tribute to the editor, Walt Jung.

The first section covers op-amp basics, including a comprehensive discussion of all those irritating imperfections that the less experienced among us might choose to ignore. Circuit diagrams are clear and usually accompanied by the relevant equations so it is easy to see critical information at a glance without having to read through the text. The discussion on noise is as good as I have seen anywhere. A host of test circuits are included for determining various parameters such as input bias current, bandwidth and slew rate. These all help to keep things in context and focused. I particularly liked the treatment of single supply and rail-to-rail amplifiers, and the constraints these impose on the designer, not all of which are obvious at first sight. The section concludes with a section on high-speed op-amps, and if you are old enough to think that op-amps can't be used at RF then think again!

The book moves on to discuss 'speciality' amplifiers. Included in this section are instrumentation amplifiers, programmable gain amplifiers and isolation amplifiers, all of which should be familiar to these involved with data acquisition. Two op-amp and single supply instrumentation amplifiers are covered in detail as well as the more traditional three op-amp configuration.

From speciality amplifiers we progress neatly to probably the most important section for digitally motivated engineers – using op-amps with data converters. This is the section where we consider the problems of interfacing between analogue and digital technology; both input (ADC) and output (DAC) conversion are covered. The all-important error-budget analyses are here, and quantifying data converter dynamic performance with SINAD (Signal-to Noise-And-Distortion ratio), SNR (Signal to Noise Ratio) and ENOB (Effective Number of Bits) is covered with delightful clarity.

The rest of the book looks into the some traditional op-amp applications such as sensor interfacing for a variety of different sensors, signal conditioning and analogue filtering with useful practical examples. The more recent op-amp applications in video signal processing are also covered in detail. The section on active filters includes a number of worked examples and very useful summary of all the main filter types with circuits and design equations.

A study of op-amps would not be complete without some mention of passive components as bad choices here can be ruinous to an otherwise excellent circuit design. For those new to the game there is a very helpful – and perhaps enlightening – capacitor comparison chart, and some good tips on assembly techniques.

The book concludes with an entertaining history of op-amp development by Walt Jung. This is the part of the book where I guess the thermionic enthusiasts will find most of their stimulation, although thermionic circuits do crop up throughout the book. I'm old enough to have used some of the solid-state hybrid devices mentioned here back in the late 70s, and the part numbers were disturbingly familiar. I did use a hybrid parametric (varactor) amplifier once, and this was excellent and probably as good as the ME1400 (thermionic) electrometer valve it replaced, but I hasten to add that I don't quite recall thermionic op-amps. The technology has thankfully moved on.

This book is a thorough study of operational amplifiers and covers in depth just about every application you can think of. It replaces half a shelf of my hitherto favourite texts and it is destined to become a standard work. I can heartily recommend it.

John W. Wood

The Sony Cyber-Shot M2 is a stylish still and movie camera which features 5.1 effective mega pixel resolution, a 2.5-inch Hybrid LCD screen, Carl Zeiss Vario-Tessar folded-path 3x optical zoom lens and high-quality MPEG-4 recording. As well as excellent images, it also allows 'casual' movie-shooting capabilities, with a capture of up to 50 minutes of good quality footage on a Memory Stick PRO Duo.The charge is supplied by InfoLithium battery. Unique to Sony, the camera features the Pocket Album and Slide Show plus Movie functions for playback on the Hybrid LCD screen. It also features PictBridge, the standard for printing directly to photo printers. The camera comes with its docking station, which makes charging and connecting to a PC, printer or TV a lot simpler.

Around £399

www.sony.co.uk

If you're looking for a small, inexpensive handheld console, then check out the new Game Boy Micro; the smallest Game Boy ever created. Thinner than a mobile phone, the Micro is only four inches wide, two inches tall and 0.7 inches deep. Not only extra slim, it also weighs an astonishing 2.8 ounces, or about the weight of 80 paper clips, making it Nintendo's lightest console ever. Even so, it has the same processing power and plays the same games as the Game Boy Advance SP.

The most notable feature, apart from the vastly reduced size, is its 2-inch backlit screen, which is brighter and sharper than any previous Game Boy screen. Plus, for the first time ever, users will be able to adjust the brightness of the screen to adapt to indoor lights or outdoor sunshine.

www.nintendo.co.uk

For people always on the move, the travel mouse might be quite a useful addition to the 'out of office' kit. Allowing you to stay productive on the move, it is a compact, easy to use mouse with a two foot retractable cord. Simple to get started, it has a plug and play set up and is fast and easy to use. Easy enough to just drop in your pocket, the mouse weighs only 0.08kg and is 4cm wide, making it the perfect solution for the mobile businessman.

Around £11.99

www.apc.com/gb

The Memorex Mini TravelDrive is a flash-based portable storage device just 2.25 inches long, 0.85 inches wide and 0.33 inches thick. Available in 256MB, 512MB, 1GB or 2GB capacities, it can be used for taking photos, music, video or important work files with the user wherever he or she may go, and it is compatible with the Windows, Mac and Linux operating systems. This product stands out because it comes complete with SecureTD software that allows the setting of a password to prevent unauthorised access to files. This works by creating a partitioned area on the Mini that does not appear until access to it is unlocked by entering a preset password.

Around: £29.99 for 256MB, £49.99 for 512MB, £89.99 for 1GB and £179.99 for 2GB

Available from the high street

Piezoceramic transformer

If there is a need to feed very low power devices you may resort to infrared optocouplers, solar cells, batteries or low power transformers, although the latter might be rather oversized for the intended purpose. Eventually, with the exception of solar cells and batteries, all of them draw power from the mains so it might be convenient to use a piezoelectric transformer if the power required is in the range 0.1 to 0.3mW. **Figure 1** shows an easy implementation of such a transformer.

Two piezoceramic sounders are glued back-to-back so that the mechanical movement of the first, the primary, is transferred to the second, the secondary. The AC output voltage can be used as it is or rectified in order to feed micropower electronic equipment or trickle charge small back-up batteries.

The actual implementation requires two ceramic sounders with high intrinsic capacitance: sounders with 80 to 110nF are readily available and usually come as 50mm discs. Two of these discs are cut down to 35mm in order to have a more compact unit and a lower stray capacitance between primary and secondary. A layer of double-sided adhesive tape is laid on the larger plate of each sounder in order to assure proper electrical insulation between primary and secondary. The sides of the sounders are then pressed against each other and the transformer is ready to operate.

Table 1 shows the measured output under several loading conditions: the AC output was measured with the load directly across the output terminals as shown in **Figure 2** while the DC output was measured with a full wave rectifier in place.

The measured DC voltage refers to a Schottky bridge rectifier but the use of standard 1N4004 diodes will only show a modest 6-8% voltage decrease.

Measurements were taken with the transformer operating in free air, without any holder, but a proper mechanical layout would require the transformer to be firmly held by the edge of the disc. This improves the transfer of mechanical energy to the secondary thus obtaining the additional benefit of a 15-20% voltage increase.

Care must be exercised during testing as the unit is directly connected to the mains and in some countries it might be convenient to split the primary resistor in two halves, one on each leg of the supply line in order to minimise feed-through of high voltage spikes across the stray capacitance – around 180pF – between primary and secondary.

The unit was stress tested by decreasing the primary resistor down to 56kΩ: the output voltage increased by 55% but the transformer did get slightly warmer after a few hours. Behaviour of ceramic sounders at mains frequency is not documented and it could be risky to run the transformer with a resistor lower than 100kΩ.

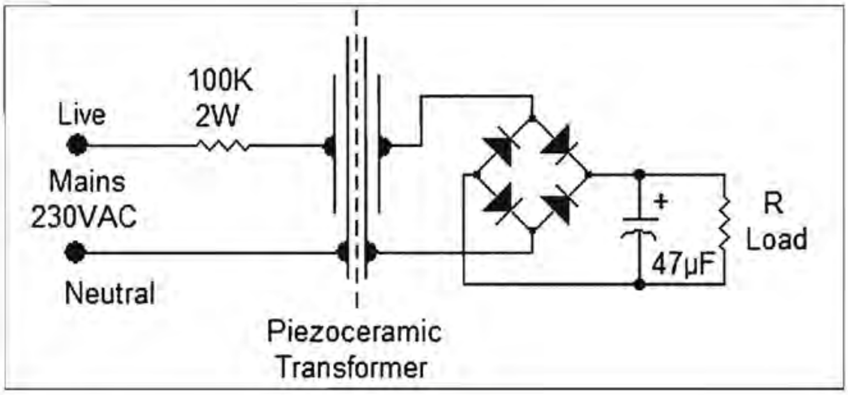


Figure 1 (Left): Circuit diagram

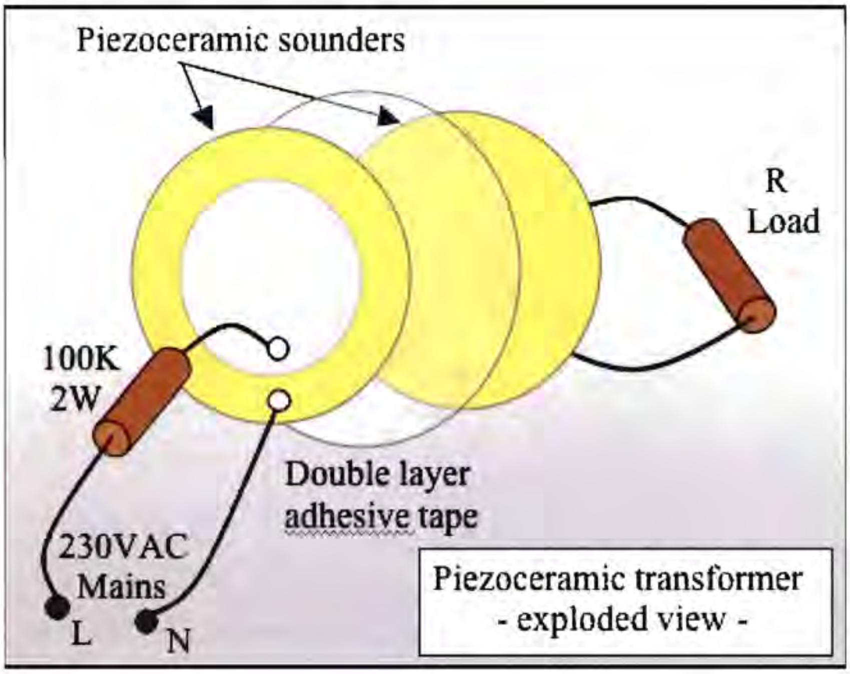


Figure 2 (Below)

Table 1

R Load	*VAC*	*VDC*
1 MΩ	5.48	7
100 kΩ	5.1	4.67
47 kΩ	4.22	3.29
22 kΩ	2.77	2.06
10 kΩ	1.41	1.1
4.7 kΩ	0.68	0.56

Useful link:
Piezoelectric transformers:
www.linear.com/pdf/an81f.pdf

D. Di Mario
Milan
Italy

Simple amplitude modulator

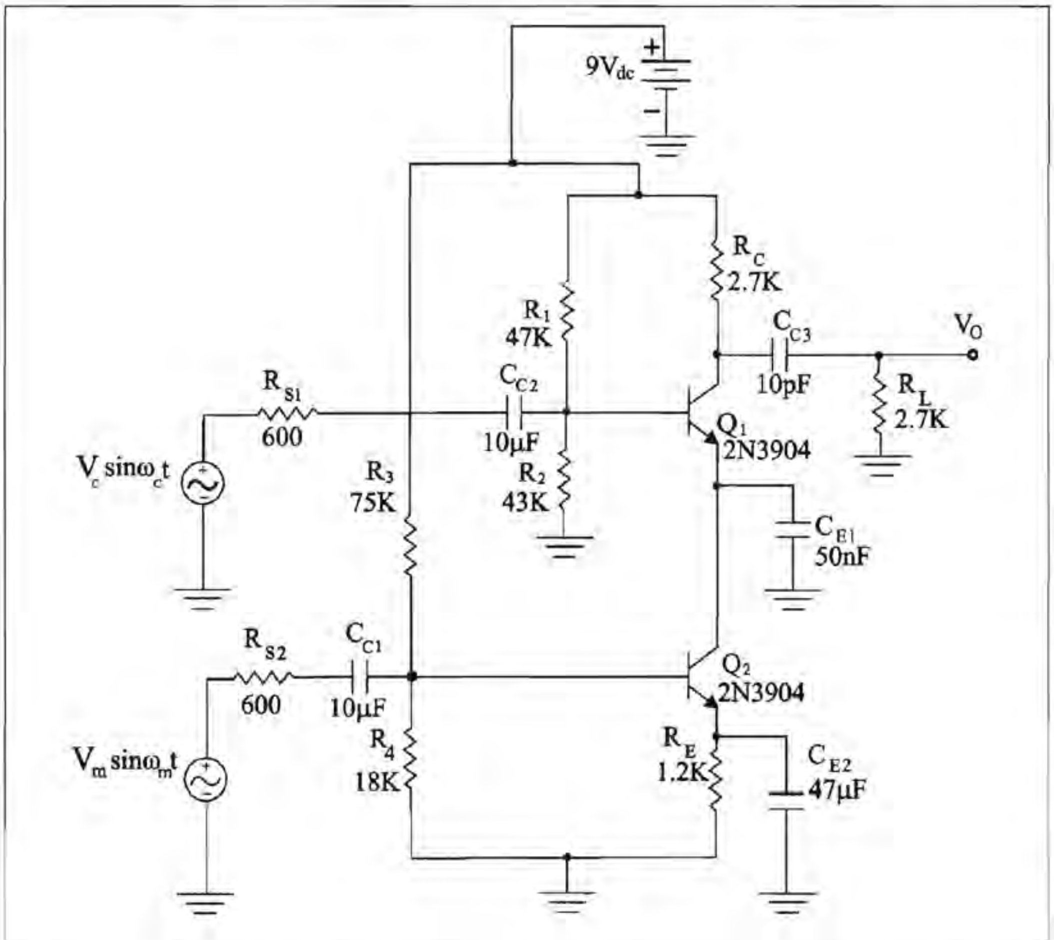


Figure 1: Simple AM circuit with a minimum number of elements

The simplest method of amplitude modulation (AM) is by using a four-quadrant analogue multiplier. The design of these multipliers is based on the structure of Gilbert cell; however, some of their characteristics limit their practical use. Among them are typical supply voltages and currents. **Table 1** shows the typical supply voltages and typical supply currents for some of the well-known four-quadrant analogue multipliers. Sometimes, the required power supplies of these ICs do not correspond with and are greater than the designed supply for other parts of the circuit. Also, the supply current of these ICs is high and this limits their use in battery-powered systems. Thus, we need a simple and flexible amplitude modulating circuit with simply modifiable characteristics that may easily be designed for any specific application. **Figure 1** shows a simple AM circuit with minimum number of elements. R_1 R_2 and are the biasing resistors of Q_1. The carrier signal is applied through C_{C2} to the base of Q_1. The carrier frequency is set equal to 1MHz. R_{S1} is the internal resistance of the carrier signal source. This source "sees" Q_1 as a common-emitter amplifier, because the impedance of C_{E1} is negligible at the carrier frequency. Therefore, the amplitude of the output voltage will be proportional to the product of V_C and g_{m1}. If g_{m1} changes proportionally to V_m, then amplitude modulation will result.

The biasing of Q_2 is provided by R_3 and R_4. The modulating signal with a frequency of 1kHz is applied through C_{C1} to the base of Q_2. R_{S2} is the internal resistance of the message signal source. Since at the frequency of modulating the signal C_{E2} bypasses R_{E2}, Q_2 is a common-emitter amplifier for the message signal. Thus the collector current of Q_2 is proportional to the amplitude of V_m. The value of C_{E1} is selected such that its impedance at the frequency of f_m is much higher than the impedance seen from the emitter of Q_1. Therefore, C_{E1} is nearly a short circuit for the carrier signal and nearly an open circuit for the message signal. This makes the emitter current of Q_1 proportional to the amplitude of the modulating input. As g_{m1} is proportional to the emitter current of Q_1, the amplitude of V_o will have a changing behaviour like the message signal.

Figure 2 shows the result of simulating this AM circuit with PSPICE 9.2. This circuit uses only a single battery and its supply current is about 1mA. Thus, it has superior performance in comparison with the four quadrant analogue multiplier ICs mentioned in Table 1. The amplitude modulated signal resulted from the practical implementation of the circuit of Figure 1 is shown in **Figure 3**.

The most important parameter of an AM circuit is the modulation index, denoted by m. The changing behaviour of m with R_2, R_4, R_C, R_E, C_{E1}, C_{E2}, and R_S ($R_S = R_{S1} = R_{S2}$) is shown in **Figures 4, 5, 6, 7, 8, 9** and **10** on pages 51 and 52.

Therefore, the modulation index may be tuned by a wide variety of circuit elements. The carrier frequency of commercial AM broadcasting is in the range of 535kHz to 1605kHz. **Table 2** shows the necessary changes in the value of C_{E1} for proper operation of the circuit at these frequencies. Necessary changes in the value of for other frequencies of the message signal are given in **Table 3**.

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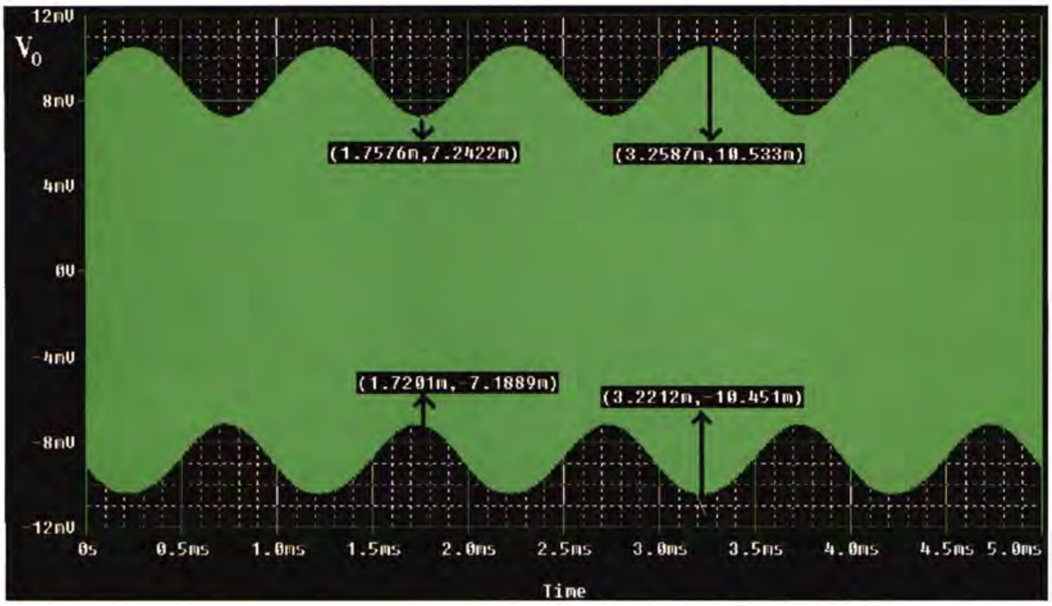


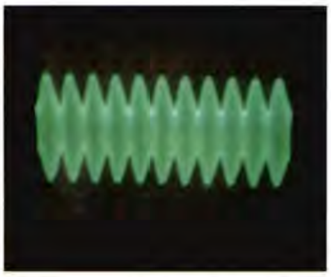


Figure 2 (Left): The output voltage of the AM circuit in Figure 1 resulted from simulating it with PSPICE

Figure 3 (Above): The output voltage of the circuit of Figure 1 that resulted from the practical implementation

TABLE 1: Typical supply voltages and currents

Device IC	Supply Voltage	Supply Current
MC1495	±15V	6mA
AD633	±15V	4mA
CA3091	±15V	6mA
AD534	±15V	4mA
ICL8031	±15V	6mA

TABLE 2: Necessary values of C_{E1} for different values of f_c

f_c (MHz)	m	C_{E1}, nF
	0.26	14
0.5	0.3	22
	0.33	43
	0.26	7.5
1	0.3	12
	0.33	22
	0.26	4.8
1.5	0.3	7
	0.33	20

TABLE 3: Necessary values of C_{E2} for different values of f_m

fm (kHz)	m	CE2, µF
	0.26	6
1	0.3	10
	0.33	25
	0.26	1.45
4	0.3	2.3
	0.33	4.8
	0.26	0.8
7	0.3	1.2
	0.33	2.4

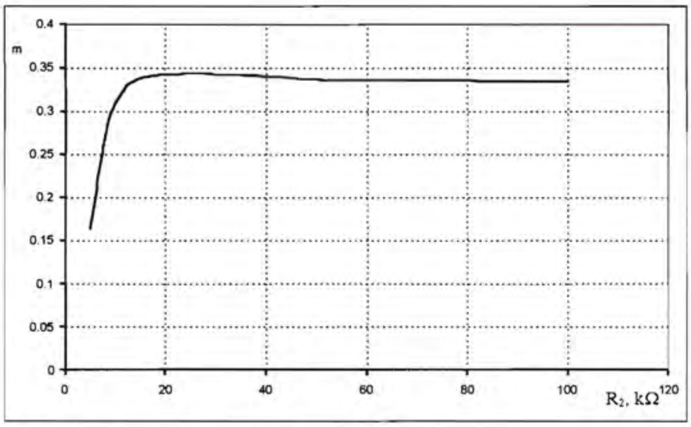


Figure 4: The changing behaviour of m with R_2

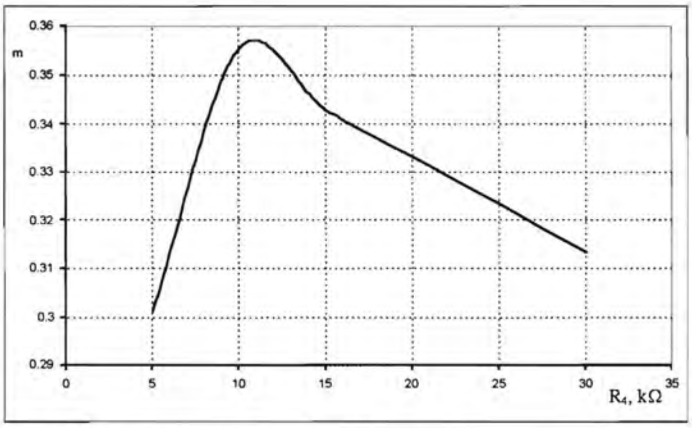


Figure 5: The changing behaviour of m with R_4

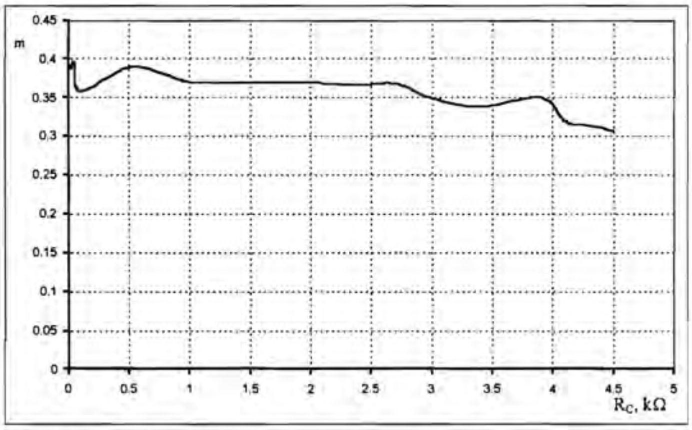


Figure 6: The changing behaviour of m with R_C

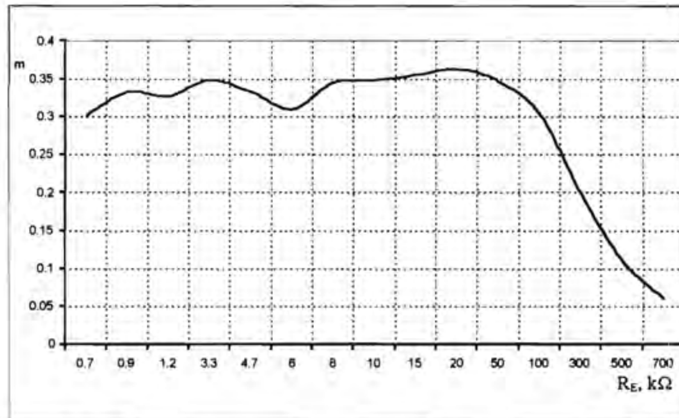


Figure 7: The changing behaviour of m with R_E

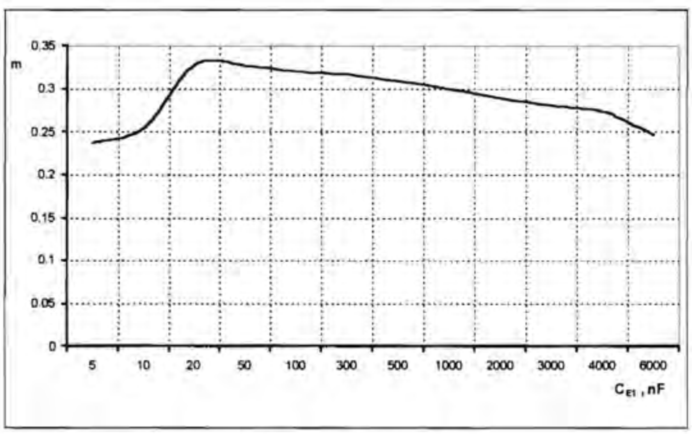


Figure 8: The changing behaviour of m with C_{E1}

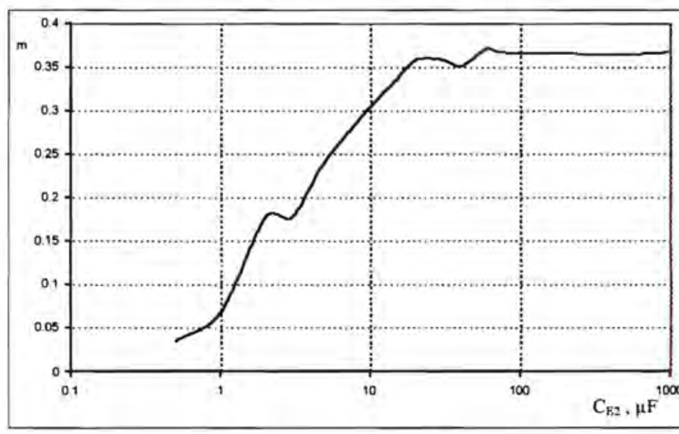


Figure 9: The changing behaviour of m with C_{E2}

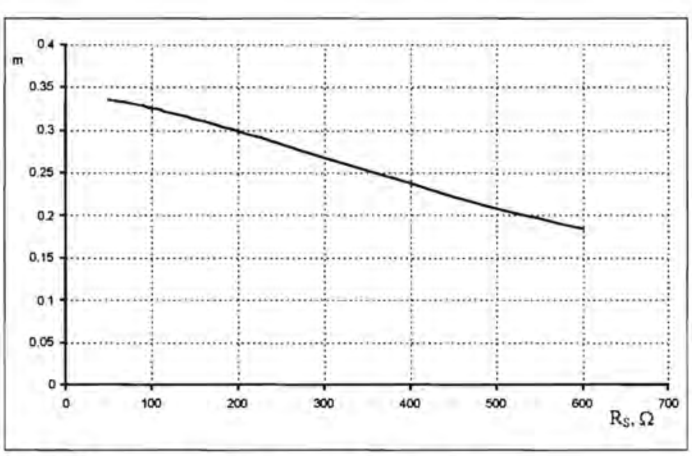


Figure 10: The changing behaviour of m with R_S

Using a power transistor as a high power zener diode

The purpose of this circuit is to use a power transistor as a high power zener diode. A high power zener diode is not only expensive but also hard to find. Anything above 10W in power is very difficult to obtain.

Figure1 shows the circuit enables a power transistor to be used as a zener diode.

To obtain the specific reference voltage, a power transistor is tested using the circuit shown as **Figure 2**. As a guideline the DC power supply is set at 15V or higher.

R1 should be around 1K.

M1 is a DC voltmeter set to the voltage range required.

As a benchmark, a Motorola TIP31C was found to obtain a reference voltage of 9.0. This may vary due to different manufacturer and production batch. A Motorola 2N3055 was found to have a reference voltage of 11.60.

The zener diode in this case for a TIP31C is 40W and a 2N3055 is 115W with adequate heatsink applied as normally required for the power transistor.

Michael Ong
City Beach
Australia

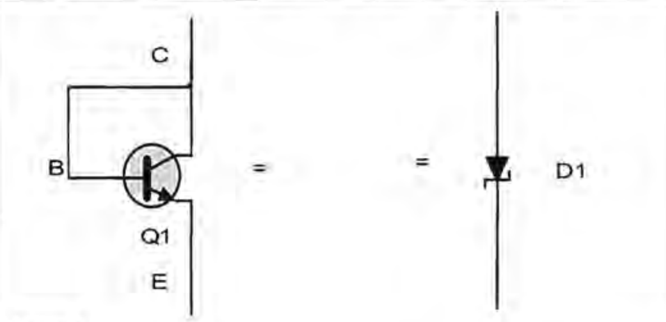


Figure 1

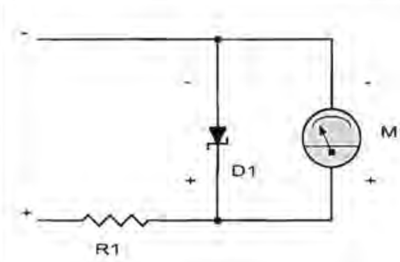


Figure 2

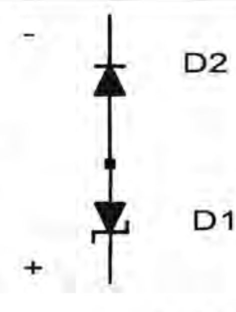


Figure 3

DSP-based stethoscope reference design

AMI Semiconductor (AMIS) announced the availability of a reference design and support material for a complete DSP-based electronics stethoscope. The design incorporates AMIS's BelaSigna 250 DSP-based audio processing device. This allows for digital recording or cardiac and pulmonary sounds into non-volatile memory, as well as it offers enhanced user interface and minimal CPU usage.

Among its features are amplification and equalisation – low delay, frequency-specific amplification for improved and faster diagnosis in noisy environments; recording a playback, easy-to-use controls, including half-speed playback mode for detailed review of pathologies that may be otherwise difficult for physicians to diagnose; low power, wireless capability and others. There's a button selection for bell, diaphragm and extended modes, with volume control, battery monitoring and low-power indication.

According to AMIS, the reference design allows for improved accuracy in assessing and classifying cardio-respiratory pathologies for medical professionals.

www.amis.com

High frame-rate smart camera models

Sony Europe's Image Sensing Solutions Division has lauched a smart camera range, with the XCI-SX1 being the first in the series. It integrates an image sensor and frame grabber with a powerful on-board processor running the industry-standard open-source Linux operating system.

The XCI-SX1 smart camera has been introduced to meet the increasing demands in smart cameras, especially in the machine vision market. Unlike conventional machine vision cameras, images captured by the XCI-SX1 are processed within the camera and the processed data is directly transmitted to a PC over a network. It provides a flexible hardware platform for OEMs, systems integrators and end users who require systems to follow the ever-changing industry trends by quickly and cost-effectively developing and implementing a range of machine vision applications, without changing specific hardware infrastructure.

A Windows-compatible version is also part of this range.

www.sony.com

Pioneer-NTB for System Verilog

Discovery Pioneer-NTB is a new System Verilog testbench automation tool from Synopsys. It promises to increase verification productivity and improve the quality of complex system-on-chip and IP designs.

The tool allows easy-to-use connections to third-party VHDL, Verilog and mixed-language simulators, allowing engineers to adopt a single, standards-based, advanced verification infrastructure in mixed-simulation environments.

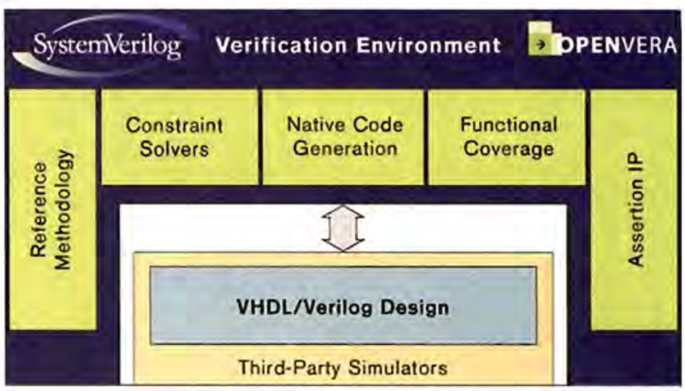
Pioneer-NTB compilers and engines are built on Synopsys Native Testbench environment with support for the IEEE P1800 System Verilog and OpenVera hardware verification language.

According to Synopsys, Pioneer-NTB's architecture simultaneously optimises testbench, functional coverage, assertions and verification IP from the recently announced Synopsys VCS Verification Library into a single executable.

The assertion IP library includes a variety of interfaces and protocol standards including PCI, AMBA 2 AHB and APB, 802.11a/b/g, AGP and SMIA. Additional standards such as PCI X2.0, PCI Express, USB 2.0, DDR2, OCP 2.0, LPC and CoreConnect will be added with later releases.

The assertions can be debugged with the Pioneer-NTB graphical debug and analysis environment.

www.synopsys.com



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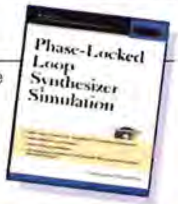
By Cory Clark

National Instrument's LabVIEW graphical programming language allows engineers to create instruments in software -- at tremendous cost savings compared to purchasing the actual hardware. LabVIEW virtual instruments can make DSP (digital signal processing) work faster and less expensively -- making it particularly valuable to engineers working on cutting-edge communications systems. This resource provides engineers with step-by-step tutorial to using LabVIEW to create virtual instruments to handle the most sophisticated DSP applications. CD-ROM contains sample LabVIEW virtual instruments and colour images from the book.

May '05, Hardback

£45.00 Code MCG 0071444920

PHASE-LOCKED LOOP SYNTHESIZER SIMULATION
By Giovanni Bianchi



Phase Locked Loop frequency synthesis is a key component of all wireless systems. This is a complete toolkit for PLL synthesizer design, with MathCAD, SIMetrix files included on CD, allowing readers to perform sophisticated calculation and simulation exercises. Describes how to calculate PLL performance by using standard mathematical or circuit analysis programs

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DIGITAL ELECTRONICS DEMYSTIFIED
By Myke Predko

Written by renowned digital guru Myke Predko, the primary focus of this self-teaching guide is on digital electronics and logic, demonstrating how functions are designed and interfaced to other devices. Readers can perform experiments with the technologies discussed in the book for under £5! The author includes two circuit design problems per chapter.

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By Theodore Wildi

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By Robert Strangeway, Owe Petersen, Richard Lokken and John Gassert

This succinct yet thorough treatment of DC and AC circuits analysis effectively communicates the concepts and techniques of circuit analysis with a focused practical style that keeps students motivated. Starting at a level that students can grasp, the text continues with clear, focused explanations that advance students to the desired level of proficiency.

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By John J. Craig

For senior-year or first-year graduate level robotics courses generally taught from the mechanical engineering, electrical engineering, or computer science departments. Since its original publication in 1986, Craig's Introduction to Robotics: Mechanics and Control has been the market's leading textbook used for teaching robotics at the university level. With perhaps one-half of the material from traditional mechanical engineering material, one-fourth control theoretical material, and one-fourth computer science, it covers rigid-body transformations, forward and inverse positional kinematics, velocities and Jacobians of linkages, dynamics, linear control, non-linear control, force control methodologies, mechanical design aspects, and programming of robots.

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COOL CIRCUITS
By Marc E. Herniter

For courses in Introduction Circuits, Circuit Analysis, Electronic Circuit Design and Analysis, and Electronics. This book attempts to answer the questions, "Why are we doing this?" and "What is this used for?" when applied to analog electronics. Since most students do not see where or how analog electronics fit into their lives, this book discusses several demonstrations and design examples with the express purpose of showing students some of the cool things that can be done with analog electronics.

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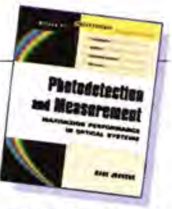

Using basic theory, fully-worked calculation, cicuit snippets and rules-of-thumb, this book conveys the know-how of good opto-electronic design, from low-noise receivers to synchronous detection "TRY IT" topics provide light-hearted demonstrations of key points. The grad student starting in photonics and the engineer optimising on opto-electronic product will benefit particularly!

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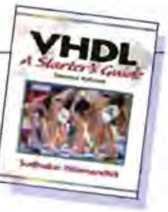
By Sudhakar Yalamanchili



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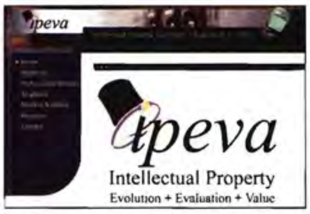

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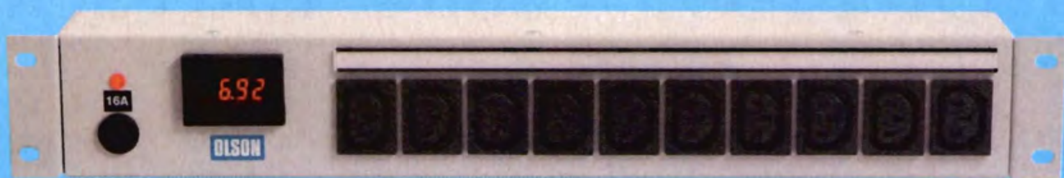

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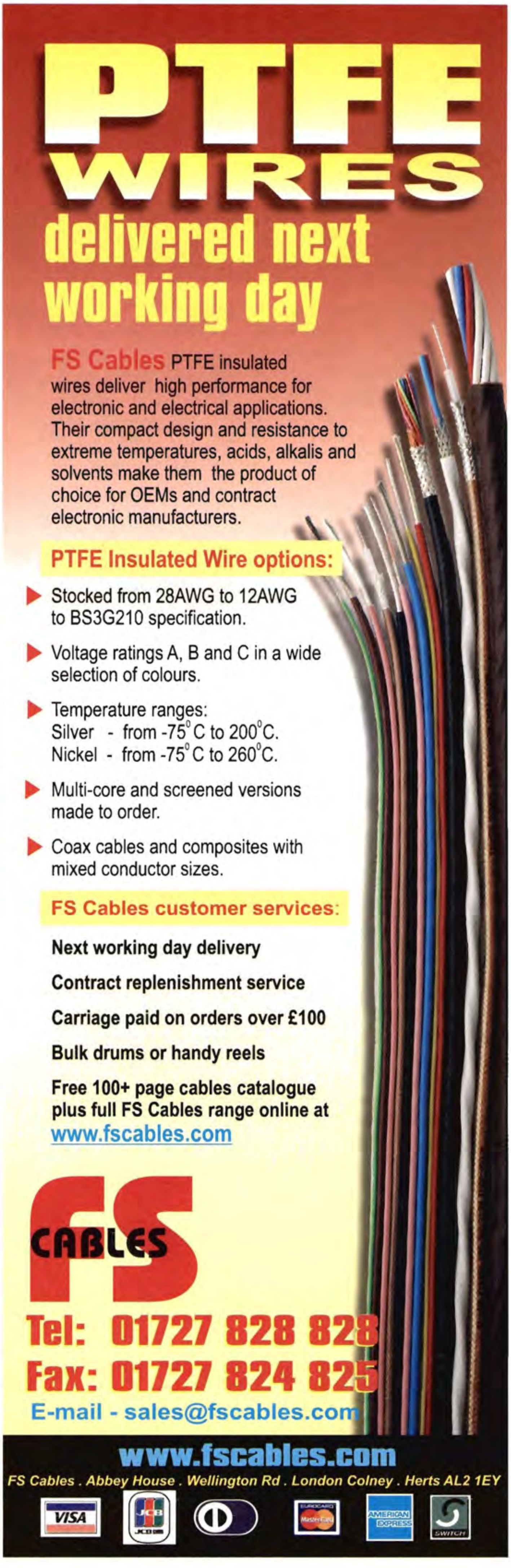

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Racal 6103/001/002/014/420/430/04T Digital Mobile RTS	4250	128
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Gfx Aug 03