VOLUME 113, ISSUE 1852

9 770959 833110 04

APRIL 2007 £4.60

ELECTRONICS WORLD

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"The **secret** to **success** is to know something nobody else **knows**."

Aristotle (384 BC - 322 BC)

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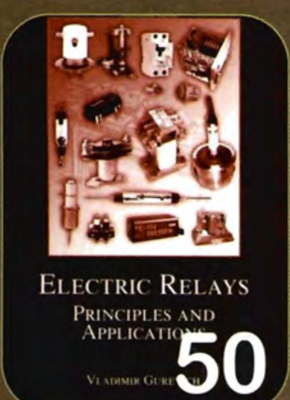

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Here are just a few of our controller and driver modules for AC, DC, unipolar/bipolar stepper motors and servo motors. See website for full details.

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Drives any 5, 6 or 8-lead unipolar stepper motor rated up to 6 Amps max. Provides speed and direction control. Operates in stand-alone or PC-controlled mode. Up to six 3179 driver boards can be connected to a single parallel port. Supply: 9Vdc. PCB: 80x50mm.
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Assembled Order Code: AS3179 - **£19.95**

NEW! Bi-Polar Stepper Motor Driver

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Supply: 8-30Vdc. PCB: 75x85mm.
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Controls the speed of most common DC motors (rated up to 16Vdc/5A) in both the forward and reverse direction. The range of control is from fully OFF to fully ON in both directions. The direction and speed are controlled using a single potentiometer. Screw terminal block for connections.
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Assembled Order Code: AS3166 - **£25.95**

DC Motor Speed Controller (100V/7.5A)

Control the speed of almost any common DC motor rated up to 100V/7.5A. Pulse width modulation output for maximum motor torque at all speeds. Supply: 5-15Vdc. Box supplied. Dimensions (mm): 60Wx100Lx60H.
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Kit Order Code: 3140KT - **£46.95**
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Individually control 12 on-board relays with included infrared remote control unit. Toggle or momentary. 15m+ range. 112x122mm. Supply: 12Vdc/0.5A
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NEW! USB 'All-Flash' PIC Programmer

USB PIC programmer for all 'Flash' devices. No external power supply making it truly portable. Supplied with box and Windows Software. ZIF Socket and USB lead not included.
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Assembled Order Code: AS3123 - **£34.95**

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SUBSCRIPTION RATES:
1 year: £46 (UK); €120 (Europe);
$145 (US & worldwide)

PRINTER: William Gibbons Ltd

NEWSTRADE:
Distributed by Seymour Distribution Ltd,
2 East Poultry Avenue, London, EC1A 9PT
+44 (0) 20 7429 4000

PUBLISHING DIRECTOR: Wayne Darroch

SAINT JOHN PATRICK PUBLISHERS

Personalising mobile phones

Recently I attended a forecast seminar for the semiconductor business. Among his various presentations, the industry analyst touched on a very interesting subject – how mobile phones are becoming more like car models every day.

We all choose our vehicle depending on what we want to do with it: family saloons to lug the family and the shopping around in; a sports car to flash it about and enjoy the speed; a van to carry bulky stuff in, or large four-wheel drives to schlep the smallest babies in.

Equally, we are seeing the emergence of phones that can offer video delivery, TV broadcasts, email, high-quality music or just voicemail and SMS. Mobile phones appear to be developing to fit different market segments.

However, the more complicated they get, the longer it takes for them to boot up too. There's nothing more annoying than trying to make a *quick* phone call, just in that very convenient gap when you are in between two successive trains, only to end up waiting several minutes to be able to dial out – and miss the train.

It is not surprising that it takes a long time, considering how much processing power has been crammed into that small space. These are small but very powerful machines. Things are likely to get even more complicated with mobile TV reception, too.

I had the chance to preview one of these mobile TV handsets – the Lobster, a phone made by HTC for BT's mobile TV service. Even though the picture was jerky, broken up and frequently disappearing, I found that TV delivered on to a mobile handset is intriguingly addictive; even more so when waiting for the picture to come back (it's that expectation that the image will appear any second...).

Poor images are nothing new, however. We all got used to the FM reception on our yester-year TVs and VCRs. Many probably still remember the dad, in an embrace with the antenna, trying to get the best TV picture. Or the numerous cartoons created around the families' youngest members juggling antennas close to the TV set for a better reception.

Now the loss of image has been personalised to each one of us (with the help of the mobile phone) and we can jiggle the handset about until tomorrow, if needed.

Either way, we shall have to consider this progress. In our world, everything is getting personalised: web pages, shopping experiences, TV programmes, so why not mobile phones too.

Svetlana Josifovska
Editor

Electronics World is published monthly by **Saint John Patrick Publishers Ltd,** Unit AG4 Block A, Hartley Buildings, Green Walk, London SE1 4TT.

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Total Recall freeze-frames design bugs

Synplicity has launched a new technology, which it says "it's a big leap forward in how people do verification".

The verification technology, called Total Recall, runs alongside a simulation program (and at FPGA hardware speeds) checking for bugs. If it identifies a bug, it stops to analyse and fix it – either in software or hardware (at the RTL level), whilst the simulation continues.

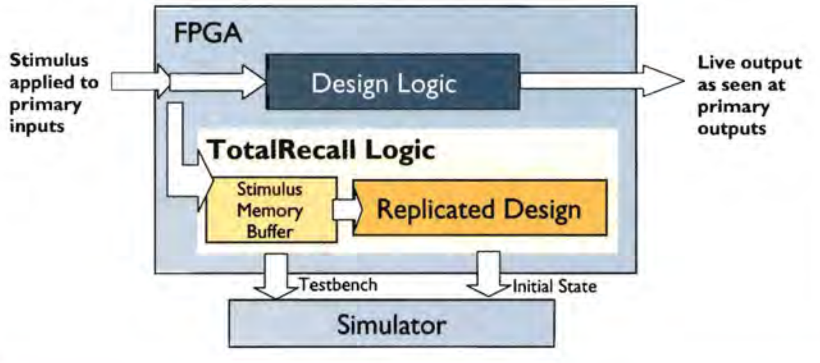
According to John Gallagher, senior marketing director at Synplicity, the Total Recall technology works for non-deterministic bugs found in live running hardware. "For this class of bugs and other rarely occurring bugs, it is almost impossible to verify that changes made to the RTL code have truly fixed a bug. Total Recall allows this – and rapidly," he added.

As more companies have started to use multi-FPGA prototyping, the conventional verification methods, such as assertions, are becoming slower. Total Recall, however, has assertions synthesised into the hardware, which increases the speed with which they can be tested.

The technology works by capturing all the signals within a design prior to the point at which an error occurs. The complete design state, along with an automatically generated test bench, can then be exported to an HDL simulator where the sequence can be replayed as many times as it takes to understand and fix the problem.

Synplicity hopes to license the technology to other companies.

Total Recall analyses the complete design state, replaying it as many times as it takes to understand and fix a bug



Olympics and Asia will influence the next semiconductor boom, says SEMI president

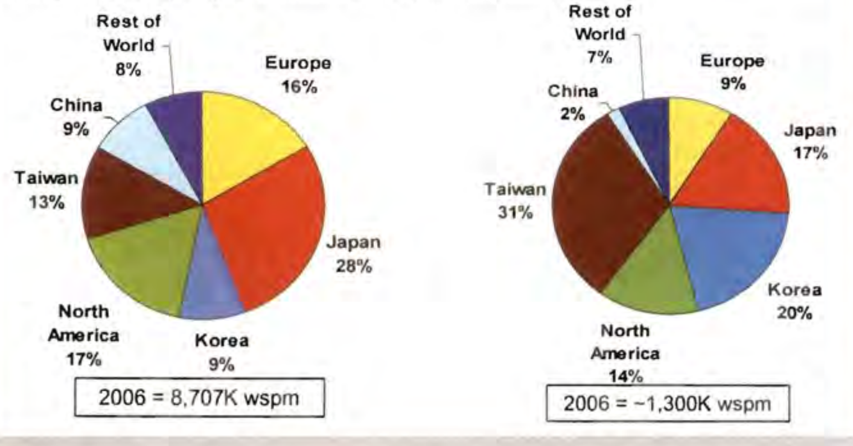
Year 2008 is likely to be a boom year for the semiconductor industry – if we read historical trends, says Heinz Kundert, the current president of SEMI Europe.

"The presidential elections [in the US] and the Olympics are always good years for the semiconductor industry," he said.

However, this may yet change since the US does not seem to play a major part in influencing the economy as it used to over the past 30 years. Kundert said that, nowadays, it is the Asian countries with the Chinese "dynamism" that are the big economy influencers instead.

"China accounts for 1.4% of the total worldwide production of semiconductors in the world [today]. In a year's time this could go up to 2.4%. However, this is still a fraction and they [the Chinese] have to prove that they can make semiconductors profitable," he said.

2006 global fab capacity of 200mm fabs (left) and 300mm fabs



Europe's fab capacity has remained at a steady 16% for the production of 200mm wafers over the past six years to 2006. However, Europe is now increasingly looking more toward producing semiconductors for the photovoltaic (PV) industry for solar panels, which requires large quantities of silicon. Some 60% of known equipment suppliers for this business are European and of that 40% are German.

"In Europe, the semiconductor industry has successfully diversified into PV," said Kundert.

Tektronix launches the fastest scope yet

Front panel of the DSA72004, 20GHz per channel oscilloscope from Tektronix

Tektronix continues to push the boundaries of its instruments, which it further proved with its latest launch of the DSA70000 series of oscilloscopes, where the top model (the DSA72004) offers a bandwidth of 20GHz, sampling rate of 50GS/s and record length of 200MB on all four channels simultaneously.

"The world has now moved on to second and third generation of serial data – and multiple lanes of it too – and this brings a whole set of engineering challenges: crosstalk, EMI, jitter, noise and so on," said Chris Martinez, design and manufacturing director at Tektronix. "Most of these challenges need better tools than what is used today – so we introduced the DSA70000 series."

The new digital serial analyser oscilloscopes capture the fifth harmonic of the clock to get a cleaner signal 'eye' and a better amplitude definition. A DSP is used to "clean up" the bandwidth, which in analogue terms is 16GHz. "The DSP is user-configurable, so a developer can choose 20GHz or a low-noise setting of 18GHz," said Trevor Smith, marketing development manager at Tektronix, EMEA.

At the heart of the instrument is IBM's 7HP silicon germanium (SiGe) technology, which offers peak performance for applications requiring high speed transfer of data, low noise, high linearity and low power consumption. Tektronix introduced this process to its instruments just under a year ago.

Nanoimprint lithography system developed in Canada

A technique for the fabrication of metallic nanostructures in pre-patterned substrates has been developed by a group working at the National Research Council, Boucherville, Quebec, and should speed the production of three dimensional moulds for nanoimprint lithography. This laser technique may also be used for forming nanostructured substrates for biochemical sensing.

Nanoimprint lithography is basically a very attractive process for the patterning of ICs with extremely high component densities, but the production of the required mould can be very difficult. Moulds can be formed by slow electron beam patterning or by photolithography, but these are very costly processes.

In nanoimprinting, a mould is pressed into a thermoplastic polymer that has been heated above its transition glass temperature. The topography of the mould is thus passed to the polymer, which can be used as a resist for the subsequent lithographic processing of an underlying substrate. The new laser assisted nanotransfer printing does not use resists, but effectively replaces the patterning, deposition and lift-off steps of normal lithography with a single step. Laser pulses selectively heat a source of donor material so that it melts and bonds to the desired locations on an acceptor substrate. Both substrates in laser assisted nanotransfer printing are patterned so that some regions will not accept the donor material. Hence, the resolution is limited by the size of the features on the donor material and not by the spot size of the laser.

The workers tested the principle by using photolithography and reactive ion etching to produce 40nm deep, 100-micron diameter microwells in a SiO_2 layer on a silicon wafer. A quartz plate coated with chromium micro-dots 80nm in diameter and 35nm high was pressed against the silicon and exposed via the back side with 266nm radiation from a laser. The nano-dots were transferred to those regions of the substrate in contact with the quartz plate. It is important that the laser provides the short pulse width required for spatially well-defined surface melting, but with minimal heating of the substrate.

Samsung Electronics has created the first LCD panel that can produce independent images on each side of a mobile LCD display. Samsung's new double-sided LCD can show two entirely different pictures or sets of visual data simultaneously on the front and back of the same screen. Other conventional double-sided LCDs can only show a reverse image of the same video data.

This new development is expected to replace two display panels with one, thereby reducing overall thickness of mobile products by at least 1mm.

Samsung has based the new technology on its proven double-gate, thin-film transistor (TFT) architecture.

* * *

A technique which will allow silicon wafers to be stacked accurately and inexpensively in 3D structures has been developed by researchers at the University of Southampton.

To date, the major challenge when stacking silicon wafers has been to align one wafer to another, matching all the features. At the moment, big machines are being used and the process is being carried out optically, with a path that is long and introduces errors.

At Southampton University, however, researchers have used a passive alignment technique and achieved alignment as precise as 200nm. The alignment features consisting of convex pyramids and concave pits can be fabricated and chip scale specimens can be successfully bonded after the microfabrication process.

* * *

NEC Electronics has introduced a 55nm cell-based IC, with a significantly lower power consumption, suitable for portable devices.

The cell, CB-55L, is based on NEC's UX7LS process technology, which demonstrates a 40% power reduction from the previous 90nm CB-90M cell. CB-55L also offers more than double the density of previous devices and offers very high reliability by resolving parameter variations often encountered at advanced process technology nodes.

Other of the cell's features include high reliability, reduced turnaround times and a comprehensive IP library optimised for portable devices. IP macros such as USB2.0, JPEG, DDR/DDR2 required for digital cameras, camcorders and other battery-operated applications will also be added to the device.

IMEC develops germanium PMOS devices

IMEC, the Inter-University Microelectronics Centre in Leuven, Belgium, has investigated the use of germanium for future pMOS devices of nanoscale dimensions. It provides a high mobility channel material that is said to be potentially better than strained silicon, but previous results using it have been limited to either long channel or to ring shaped devices.

IMEC has employed enhance-ment techniques, including strain, to obtain excellent hole mobility in long channel devices of up to 2.7 times higher than the universal hole mobility in silicon and high drive currents for short channel devices. The shortest gate length was reported as 125nm.

IMEC fabricated the pMOS devices by using a silicon compatible process with 200mm diameter germanium on silicon wafers made by ASM. The uppermost germanium layer on the wafers was deposited by epitaxial growth directly onto the silicon. An extremely thin 0.6nm epitaxial silicon layer, partially oxidised after its formation, provided passivation for the germanium surface. The silicon passivation layer was immediately capped by a 4nm thick dielectric layer of hafnium oxide deposited by using an ASM Pulsar reactor, which was followed by a 10nm layer of tantalum nitride and an 80nm layer of titanium nitride deposited by physical vapour deposition.

The effective oxide dielectric thickness was only about 1.2nm resulting in a gate leakage less than $0.01A.cm^{-2}$. In a typical device of dimensions 10 x 10µm, a peak carrier mobility of $315cm^2/Vs$ was achieved. The drain current of 670µA per micron is claimed as a record for a gate length of 190nm and a Vd of –1.5V.

IMEC intends to further improve the device performance by implementing strain, optimising the ion implantation and reducing the gate length even further. The results, reported at the IEEE International Electronic Devices Meeting in San Francisco, California, are part of an IMEC core programme on sub-32nm CMOS in collaboration with the companies Infineon, Intel, Micron, NXP, Panasonic, Samsung, ST Microelectronics, Texas Instruments and TSMC.

FOREMOST project will integrate 45nm CMOS technology

A MEDEA+ project known as FOREMOST aims to maintain the European lead in CMOS IC manufacture by developing and demonstrating advanced process modules and transistor architectures. These will include a full 45nm mode technology for use in industrial 300mm wafer fabrication plants by 2010.

Running from January 2006 until June 2008, the project incorporates both CMOS logic and DRAM/Flash memory technologies. Currently, the major manufacturers mass produce DRAM memory chips with 90nm node technologies.

The DRAM work in FOREMOST aims to develop new devices for the peripheral transistors required for future double data rate standards and novel transistor structures for DRAM cell arrays. The arrays are related to new CMOS logic that will require three dimensional structures in due course. FOREMOST intends to let manufacturers propose the most advanced logic techniques even ahead of the International Technology Roadmap for Semiconductors (ITRS) predictions to boost the European industry. It will directly impact high complexity component performance and reduce the cost per function.

A process ready for integration is expected to be achieved by the middle of 2008. The project involves 22 partners from eight countries.

World's fastest transistor

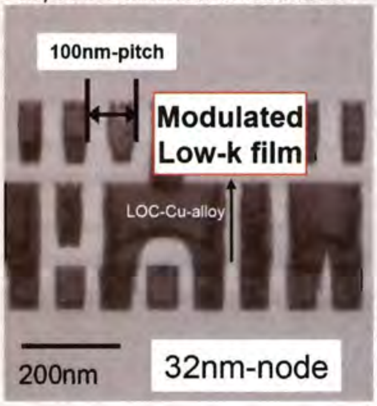
A heterojunction bipolar transistor based on InP and InGaAs has been operated at a frequency of 765GHz at room temperature (25°C) and at 845GHz when it was cooled to –55°C. The device was developed by Milton Feng at the University of Illinois, Urbana-Champaign. It is said to be some 300GHz faster than transistors built by other researchers.

The transistor employs a pseudomorphic grading of the material composition in the base and collector regions. This grading of the semiconductor composition enhances the electron velocity, thus reducing both the current density in the device and the charging time. The researchers have improved the device fabrication process to achieve smaller transistor features with a base region only 12.5nm in thickness. This vertical scaling of the device dimension reduces the distance that the electrons must travel and thus increases the device operating speed. The collector size was also reduced laterally to reduce the device capacitance, so that it can charge and discharge more quickly.

It is hoped to increase the transistor operating speed still further and also to reduce the current density to the absolute minimum value possible, so as to reduce the junction temperature and improve device reliability. The work was funded by the US Defense Advanced Research Projects Agency (DARPA) and carried out in the Micro and Nanotechnology Laboratory of the University.

32nm interconnect developed

New co-polymerised low-k film was developed in 32nm-node interconnects



A new low-k dielectric technology based on a plasma co-polymerisation technique has led to the development of the first 32nm node multilayer interconnect for large scale integrated circuits (LSIs). In advanced LSI devices, the number of interconnects between transistors increases with device complexity, while the amount of space between interconnects decreases owing to miniaturisation. The resulting line proximity tends to produce increased parasitic capacitance, which can cause longer delays to signals.

One solution to these problems involves the use of a porous low-k (low dielectric constant) material to minimise parasitic capacitance, such as the organic silica films with low polarisability that are already being used in 90nm node LSIs. The known porous low-k materials could not provide adequate mechanical strength plus insulation reliability at the 32nm node and beyond. NEC has developed a technology to overcome these issues that also brings the advantages of high performance and low power consumption required for the next generation of network servers and mobile terminals.

The plasma co-polymerisation technique provides continuous control of both the dielectric constant and of the mechanical strength during the growth of the low-k films, by changing the supply ratio of two types of precursor chemicals without breaking the vacuum.

NXP, the former semiconductor arm of Philips, has announced that it will terminate its involvement in the Crolles2 Alliance upon the expiry of the initial contract term at the end of this year. The two other parties in the Alliance are Freescale and STMicroelectronics (ST).
The partners, including fab giant TSMC, have successfully collaborated on advanced CMOS, differentiating options, packaging development, libraries and memories, as well as 300mm manufacturing.

* * *

Year 2007 is expected to mark the rise of both mobile email and back-up and restore for mobile devices in the mass market, says Synchronica, a synchronisation and device management solutions supplier based in the UK.
This is due to the advent of industry standards, lower cost devices and falling service plan costs. Until now, mobile email has been mainly limited to the approximately six million BlackBerry subscribers worldwide who can afford to buy an expensive device and are willing to accept a costly data plan.

* * *

Polymer Vision and Innos have established the world's first production facility for organic, semiconductor-based, rollable displays (see below). Manufacturing will begin this year. Polymer Vision has spent the past three years processing displays in its own pilot facility in Eindhoven. Its process technology will now be transferred to Southampton, UK, where Innos has already started installing equipment in its newly built cleanroom.
Rollable displays offer the opportunity to create unique design form-factors and the additional advantage of low power.

ClearTune filtering technology hoped to clean up mobile TV act

Microtune, the developer of tuners for handheld mobile TV systems, has used a filtering technology from its cable division and applied it to mobile TV tuners to guarantee an interference-free picture.

The techonology is called ClearTune and is currently undergoing the patenting process.

ClearTune offers in-band suppression and rejection of an undesired signal that cannot be stopped by external filters, but it works in conjunction with them as they attenuate the out-of-band carriers. As such, it significantly reduces the impact of the mobile phones' GSM 900MHz power amplifier signal that generates a blocking signal inside the phone. It can reject the GSM carrier and suppress other unwanted signals, which could come from TV stations, cars and other mobile phones – some of which over 45dB more powerful than the wanted signal – and affect the picture's clarity. By attenuating large nearby signals, the tuner can better decode the desired signals.

"With the conventional receiver architecture the LNA saturates in the presence of strong in-band carriers, and the GSM carrier is the biggest adjacent channel that a handset designer must content with. As soon as this happens, the sensitivity of the receiver collapses," said Phil Spruce, handheld marketing manager at Microtune. "The cellular industry does not know this yet. We know this from our cable business and we've applied it to mobile TV. With ClearTune, there's no sensitivity collapse." As such, the TV image will not disrupt or disappear if a call or SMS comes through to the handset.

Although ClearTune will not add any benefit for close-in interfering signals, it does so for far-away interfering signals of over 50MHz – an aspect that seems to be overlooked in the industry.

Microtune will not disclose the architecture of ClearTune just yet. However, Spruce said that this is a direct conversion technology "incorporated around the low-noise amplifier [LNA]".

ClearTune has already been applied to a multi-band DVB-H tuner, in a system-in-package version. However, Microtune plans a wafer-level, chip-scale package, where the tuner, demodulation and memory will be packed into an even smaller space.

The devices are being made by IBM in a SiGe and BiCMOS-process.

Mobile TV reception with and without ClearTune technology

Cellular v TV reception

Cellular phone receivers operate in narrow frequency bands, typically 25-35MHz. To reduce interference in these systems, designers can put a filter in front of the receiver and effectively eliminate potential interferers across a broad spectrum.

In contrast, a TV receiver has a wide band. As a result, it is not possible to use a single fixed filter and reject the interferers. In stationary TV sets, this is typically overcome with specialised filtering techniques and/or increasing linearity significantly, but the resulting tuner consumes over 1W of power.

For the DVB-H standard for mobile TV reception, the tuner must select either a single 5, 6, 7 or 8MHz channel out of the entire band of channels (for example, countries using an 8MHz channel separation will have a total of 48 channels present in the pass band of the tuner for UHF band IV-V). The rest of the frequency spectrum in the UHF band IV-V will be made up of an unknown combination of analogue (such as PAL), and/or DVB-T television signals at potentially large amplitudes relative to the desired DVB-H signal.

All of these other television signals are seen as interfering signals in the receiver.

DATABASE ATTACKS

Enterprise database infrastructures, which often contain the crown jewels of an organisation, are subject to a wide range of attacks. The most critical of these are listed here, followed by recommendations for mitigating the risk of each.

Excessive Privileges: When users (or applications) are granted database privileges that exceed the requirements of their job function, these privileges may be used to gain access to confidential information. For example, a university administrator whose job requires read-only access to student records may take advantage of excessive update privileges to change grades.

The solution to this problem (besides good hiring policies) is query-level access control. Query-level access control restricts privileges to minimum-required operations and data. Most native database security platforms offer some of these capabilities (triggers, RLS, etc), but the manual design of these tools make them impractical in all but the most limited deployments.

Privilege Abuse: Users may abuse legitimate data access privileges for unauthorised purposes. For example, a user with privileges to view individual patient records via a custom healthcare application client may abuse that privilege to retrieve all patient records via a MS-Excel client.

The solution is access control policies that apply not only to what data is accessible, but how data is accessed. By enforcing policies for time of day, location and application client and volume of data retrieved, it is possible to identify users who are abusing access privileges.

Unauthorised Privilege Elevation: Attackers may take advantage of vulnerabilities in database management software to convert low-level access privileges to high-level access privileges. For example, an attacker might take advantage of a database buffer overflow vulnerability to gain administrative privileges.

Privilege elevation exploits can be defeated with a combination of query-level access control and traditional intrusion preven-tion systems (IPS). Query-level access control can detect a user who suddenly uses an unusual SQL operation, while an IPS can identify a specific documented threat within the operation.

Platform Vulnerabilities: Vulnerabilities in underlying operating systems may lead to unauthorised data access and corruption. For example, the Blaster worm took advantage of a Windows 2000 vulnerability to take down target servers.

IPS tools are a good way to identify and/or block attacks designed to exploit known database platform vulnerabilities.

SQL Injection: SQL injection attacks involve a user who takes advantage of vulnerabilities in front-end web applications and stored procedures to send unauthorised database queries, often with elevated privileges. Using SQL injection, attackers could even gain unrestricted access to an entire database.

Query-level access control detects unauthorized queries injected via web applications and/or stored procedures.

Weak Audit: Weak audit policy and technology represent risks in terms of compliance, deterrence, detection, forensics and recovery.

Unfortunately, native database management system (DBMS) audit capabilities result in unacceptable performance degradation and are vulnerable to privilege-related attacks – i.e. developers or database administrators (DBAs) can turn off auditing. Most DBMS audit solutions also lack necessary granularity. For example, DBMS products rarely log what application was used to access the database, the source IP addresses and failed queries.

Network-based audit appliances are a good solution. Such appliances should have no impact on database performance, operate independently of all users and offer granular data collection.

Denial of Service: Denial-of-service (DoS) may be invoked through many techniques. Common DoS techniques include buffer overflows, data corruption, network flooding and resource consumption. The latter is unique to the database environment and frequently overlooked.

DoS prevention should occur at multiple layers including the network, applications and databases. Database-related recommendations include deploying an IPS and connection rate controls. By rapidly opening a large number of connections, connection rate controls can prevent individual users from consuming database server resources.

Database Protocol Vulnerabilities: Vulnerabilities in database protocols may allow unauthorised data access, corruption or availability. For example, the SQL Slammer worm took advantage of a Microsoft SQL Server protocol vulnerability to execute attack code on target database servers.

Protocol attacks can be defeated by parsing and validating SQL communications to make sure they are not malformed.

Weak Authentication: Weak authentication schemes allow attackers to assume the identity of legitimate database users. Specific attack strategies include brute force attacks, social engineering, etc.

Implementation of passwords or two-factor authentication is a must. For scalability and ease-of-use, authentication mechanisms should be integrated with enterprise directory/user management infrastructures.

Exposure of Backup Data: Some recent high profile attacks have involved theft of database backup tapes and hard disks.

All backups should be encrypted. In fact, some vendors have suggested that future DBMS products may not support the creation of unencrypted backups. Encryption of online production database information is a poor substitute for granular privilege controls.

Although databases and their contents are vulnerable to a host of internal and external threats, it is possible to reduce the attack vectors to near zero. By addressing these threats you will meet the requirements of the most regulated industries in the world.

This month's Top 10 Tips were supplied by Amichai Schulman, co-founder and CTO of Imperva, a developer of database and web application security and compliance products.

Imperva will be exhibiting at Infosecurity Europe 2007, which is taking place at London Olympia between 24th and 26th April 2007 (www.infosec.co.uk)

If you want to send us your top five or ten tips on any engineering and design subject, please write to the Editor at EWeditor@nexusmedia.com.

It's all about the Bits

Dave Welch, Chief Strategy Officer and Jeff Ferry, Director of Communications at Infinera explain the benefits of a new network architecture comprising digital optical networks

The digital optical network offers a new platform for telecom operators, with new features, flexibility and excellent economics. Access to data travelling through the network enables an operator to manipulate it, adding or dropping traffic, switching, grooming and other functions. This enables the operator to add value for his customers, increasing their revenues, profitability and business growth opportunities.

Digital optical networks are enabled by large-scale photonic integration. Large-scale Photonic Integrated Circuits (PICs), incorporating up to 50 optical devices on a single monolithic substrate, enable dramatic improvements in the performance of long-haul optical networks. In the first commercially available architecture, a pair of photonic integrated circuits provides 100 Gigabits/second (Gb/s) of DWDM capacity. A transmit PIC incorporates ten 10Gb/s lasers, modulators and other devices. A receive PIC incorporates ten receivers. Analogous to the electronic integration of transistors onto a silicon chip first achieved half a century ago, photonic integration enables dramatic savings in space, cost, power consumption, reliability and scalability as compared to traditional DWDM networks that are built from large numbers of discrete components.

Fibre connections are the greatest source of problems in a DWDM network. Traditional DWDM networks use a large number of components connected by fibre. Photonic integration eliminates up to 97% of fibre connections by making connections on-chip or on the system backplane, leading to a great improvement in system reliability and uptime. As of November 2006, commercially deployed PICs have logged six million hours of field operation, carrying live traffic with no PIC failures.

PIC architecture yields significant benefits in cost by eliminating the costly packaging required by discrete components. PIC architecture also provides benefits in scalability. Each pair of PIC chips provides bandwidth of 100Gb/s, enabling network scalability in increments ten times larger than the prevailing 10Gb/s rate in long-haul DWDM networks. Fast and simple scalability is valuable for networks trying to cope with fast-growing and unpredictable demand driven by the new wave of Internet applications such as video and music sharing.

Photonic integration has enabled a new network architecture known as Digital Optical Networks. Reduced cost and footprint of the PIC-based system enables more frequent deployment of Optical-Electrical-Optical (OEO) conversion, for access to and manipulation of the digital data in the network. This enables important features such as performance monitoring, protection and restoration for greater network uptime. Other value-added features include switching, grooming, add/drop of traffic and advanced video-oriented features such as multicasting. A digital optical network is also able to provide support for packet-centric functions and architectures such as Ethernet and Gigabit Ethernet transport, and GMPLS network intelligence.

While the current generation of PICs operate at 100Gb/s on a chip, there have been successful demonstrations of a 400Gb/s PIC and, in March 2006, of a 1.6 Terabit/second PIC. The 400Gb/s PIC employed demonstrated in 2005 employed 10 DWDM channels each operating at a 40Gb/s data rate. The 1.6Tb/s PIC employed 40 channels of DWDM, each operating at 40Gb/s. As evidenced by the 1.6Tb/s demonstration, PIC technology has the capability to scale both by scaling the TDM line rate or by scaling the WDM channel count on a fibre. Experience with PIC design indicates that the PIC is at an early stage and is likely to see a significant growth in data rate as well as functionality, with future potential to add other functions to today's PICs.

WHILE THE CURRENT GENERATION OF PICS OPERATE AT 100GB/S ON A CHIP, THERE HAVE BEEN SUCCESSFUL DEMONSTRATIONS OF A 400GB/S PIC AND, RECENTLY, OF A 1.6 TERABIT/SECOND PIC

In summary, a new network architecture consisting of digital optical networks has been enabled by large-scale photonic integration. This digital architecture brings significant benefits to network operators in terms of features, flexibility and enhanced opportunities to realise new revenue streams, while reducing costs and increasing reliability. Increases in the performance and capabilities of future PICs can be expected to make the digital architecture still more powerful and more competitive as compared to traditional DWDM architectures.

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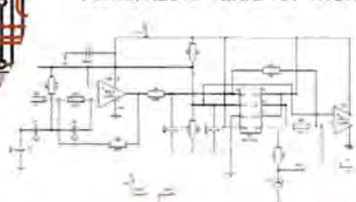

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DIE SINGULATION...

...Lasers could be the way

BY KEITH GURNETT AND TOM ADAMS

Synova's new 300mm (12 inch) wafer dicing system incorporating a maintenance-free fibre laser

For a good many years, the dicing of wafers, or singulation into individual die, was more or less an inexpensive afterthought of the costly – and rapidly advancing – front-end processes. Design rules might go to 65 nanometers, but you still have to dice up the wafer into individual die.

True, there were incremental improvements in sawing and in scribe-and-break, still the two most widely used methods. Perhaps a decade ago lasers began to nibble at the market share, but lasers were generally considered too expensive. Mechanical methods had achieved high reliability, were much cheaper initially and their consumable elements – diamond blades and scribing tools – were generally very cheap as well.

Several forces are now at work to change this peaceful scenario. Not all manufacturers will be affected, at least not in the short term, and mechanical dicing methods will remain widely used. But there are at least four factors that are making chip makers in diverse corners of the industry think twice about their dicing choices. These are thin wafers, street width, redistribution of insulating layers and native substrates.

The Transition To Thinned Wafers

Dick Toftness, vice president for advanced process development at Xsil Ltd, estimates that the use of chips less than 150 microns thick – less than a third of conventional silicon thickness – is growing by more than 25% per year. The move toward miniaturisation, in other words is now taking advantage of the Z dimension. The impetus comes from mobile phones and numerous other applications, where saving space is critical and chip stacking becomes a necessity. Toftness regularly sees production wafers thinner than 80 microns and even down to 20 microns.

Thinning becomes a dicing concern because the mechanical methods of thinning don't handle very thin wafers well – but lasers do. And because of the way they remove material, lasers can dice thinned wafers very quickly. Higher speed means higher wafer throughput, and higher throughput might diminish costs enough to make a laser system attractive.

Street Width And The Advantage Of A Narrower Kerf

The kerf is the cut made by the laser and is typically narrower than can be achieved by a diamond saw and more controllable than scribe-and-break. The material that is removed during dicing amounts to wasted real estate in terms of the total area of the wafer. If the chip maker can narrow the kerf, he can likewise narrow the streets that run between the die. And if he can narrow the streets, he can place more die on the surface of the wafer.

The space advantage of narrower kerfs is most pronounced when the die are small, because there are more die and the streets occupy a relatively larger area of the wafer. There is a correlation between the minimum laser-cut kerf width and the thickness of the wafer; usually the ratio is about 1:10. But this means that on a 100-micron thick wafer, the best laser system can run a kerf that is only 10 microns wide. If you have a fairly large wafer with hundreds of tiny chips, being able to reconfigure the wafer to accommodate a kerf that is only 0.01mm wide gives a tremendous productivity boost.

Redistribution Of Insulating Layers

One of the methods that chip designers are using to get to 65 nanometers and below is the incorporation of low-k dielectric layers in the chip circuitry. Many different materials are being used for these inner-layer dielectrics, but most of them are nanoporous polymers, usually about one to two microns thick. Understandably, these materials are mechanically fragile and don't tolerate rough handling during production.

Their fragility tends to give the edge to laser dicing methods, where mechanical forces are minimised. A laser still has the potential to cause damage, typically by causing overheating that puts stresses into the silicon that can lead to cracking, but controlling the thermal parameters of a laser is fairly easy.

Native Substrates And The Proliferation Of Exotic Substrates

Wafers such as gallium arsenide (GaAs) and silicon carbide (SiC) have been in production for many years and are the substrates of choice in applications where silicon doesn't perform well – most notably high frequency, high-power applications. Each has its own dicing problems. Wafers made of GaAs, for example, are famously brittle; once GaAs begins to crack it tends to keep on cracking. Silicon carbide is extremely hard. Dynatex, one of the key makers of mechanical dicing equipment, has a scribe-and-break system dedicated to SiC and other similarly hard materials.

But the desire for ever more advanced high-frequency systems has taken off recently. The military, for example, badly wants X-band radar systems, which are beyond the frequency limits of silicon and require gallium nitride (GaN) chips. GaN is an unusual material: it operates best at junction temperatures of 300°C, far above the 180°C limit of silicon junctions, and can handle high frequencies and high power. It is a prime candidate to replace the silicon power amplifiers currently used in mobile phone basestations because of these qualities and because it generates more sharply-defined channels.

But in one way GaN is an oddity: there are no GaN wafers, at least not crystalline wafers similar to silicon, GaAs and other wafers. You can grow wafers of silicon and GaAs and other substrate materials, but no one has yet been able to grow a GaN wafer by a viable, repeatable method. Instead, GaN is being deposited onto wafers of diamond, sapphire, silicon carbide and, even, onto wafers of plain silicon. GaN is also being deposited onto GaN – not onto a grown crystal, but onto a bulk form of GaN. Research is even going on to deposit GaN onto a silicon layer that in turn goes onto a diamond substrate. The reason: silicon is a well-known, friendly material, and diamond is the most efficient material for removing heat, in this case, the 300°C heat of the GaN.

Few, if any, of these substrates are likely to be cut by mechanical methods. The production costs are too high to risk chip-out, and some of the materials, such as diamond, are just too hard. So they are being diced by various laser methods. While the total volume of all of the GaN substrate varieties will never be very large, these challenging materials draw attention to laser dicing methods.

All of the laser dicing systems ultimately vapourise the target material, but there is a great deal of variation in the way the various systems approach the task. The Swiss firm Synova combines the laser with water. The laser beam is confined inside a high-pressure water-jet which, remarkably, can be as much as 6cm long. The laser removes the silicon or other wafer material, while the water jet removes the debris particles and provides cooling. The wafer is heated, but only very locally and very briefly.

At the moment, the narrowest laser beam being used with the system has a 22 micron diameter and can produce a kerf 28 microns wide. Research is underway to reduce the beam diameter to around 10 microns.

A very different approach is used by Advanced Laser Separation International in the Netherlands, whose system uses an optical grating that splits the laser beam into separate parallel beams in order to limit heating. The separate beams follow each other down a street during cutting. Depending on the application, the number of separate beams may range from three to 50. Each beam vapourises a small amount of material; the wafer then cools slightly before the arrival of the next beam. The beams may be from 15 to 100 microns apart.

The narrowest kerf the system can cut is 10 microns on thinned wafers. More typical are kerfs from 20 to 30 microns (the kerf is typically one-tenth of the wafer thickness), but the widths are so small that they permit more die on each wafer.

One ordinarily thinks of the streets on a wafer as being straight and running from one side of the wafer to the other, but it isn't always the case. Some wafers contain hexagonal die; as a result, the streets are torturous zigzags. How do you cut something like this? You might do it with a saw, but the streets would have to be so wide that they would waste a great deal of real estate.

Xsil makes a laser whose strong points are high speed and very tight spatial control. As you might expect, the laser has a very sophisticated optical system, but it cuts the short zig-zags of the hexagonal die at high speed. Because it can handle the short cuts, the chip maker can greatly reduce the width of the streets and use the recovered space – about 30% of the whole wafer – to pack in more die.

Manufacturers of more conventional wafers with straight streets are finding that the speed and precision of the system are useful in other ways. For example, they can first dice the wafer and then immediately go back and cut isolation trenches on individual die.

THERE ARE AT LEAST FOUR FACTORS THAT ARE MAKING CHIP MAKERS IN DIVERSE CORNERS OF THE INDUSTRY THINK TWICE ABOUT THEIR DICING CHOICES: THIN WAFERS, STREET WIDTH, REDISTRIBUTION OF INSULATING LAYERS AND NATIVE SUBSTRATES

HOW FAR WILL IT GO: when only the longest range will do

by Myk Dormer

Low-power ISM band modules are well established in a wide variety of short range, high and low data-rate applications. They are often referred to as SRDs (Short Range Devices), so it is commonly assumed that these solutions are usable only over very limited distances.

But it all depends on what you mean by 'short range'. Simple, wideband ISM implementations rarely exceed 100m. Popular 2.4GHz network devices don't even approach that figure – and rarely need to. But there is a sub-set of low power radio tasks where longer ranges are desirable.

Alarms and high-value asset-tagging systems need to cover extensive industrial sites, agricultural monitoring, and control devices frequently need ranges exceeding a kilometer; maritime telemetry calls for even longer ranges. While there are existing infrastructure-based wireless systems (such as GPRS, or even ARGOS), or high-power licensed band radios that guarantee far longer ranges by design, there is a lot that can be achieved with very simple ISM modules, provided a few simple considerations are taken into account.

So what defines range? The range expected of a radio link is the point at which the path loss between the aerials equals rx_sensitivity – tx_power (the 'link budget'). A margin for fading and uncertainty, of usually 10-20dB, is normally added to the path loss.

From the path loss model (see footnote) we can see that the path loss is proportional to $10 \times \log(1/d^4)$, where 'd' is the range in meters. As a rough rule, this suggests that to double the range, it is necessary to improve the link by about 12dB.

1. Start with an RF-friendly design. The most sensitive receiver is totally wasted if all it can pick up is noise from the processor, power supplies and displays. The first step is to provide adequate shielding, decoupling and avoidance of EMI generation.

2. Keep the data rate as low as possible. Range is all about receiver sensitivity, which, in turn, relates to channel bandwidth. For a given transmitter power and system noise figure, a 64kbit/s link will have a lower sensitivity and hence inferior range to a 1kbit/s link.

A lower data rate will also allow the use of narrow-band radios with higher sensitivity and better rejection performance than simple wideband modules (refer to Note 2). To make best use of very low data rates, special techniques must be employed, processing the AF output before squaring, or in some cases the IF signals. Some implementations use DSP techniques to achieve sub-10Hz effective band widths and sensitivities better than –150dBm.

3. Use an efficient decoder. For a given level of received signal-to-noise ratio, the data error rate (and hence usable sensitivity) can vary markedly for different decoder algorithms. Edge triggered, asynchronous decoders (such as simple UARTs) require a much 'cleaner' baseband signal than a good biphase (Manchester) decoder. Tone decoders (slower modem devices, DTMF devices) offer even better performance at the price of more hardware and much slower communication.

4. Choose your band carefully. Different nations have different regulations and different permitted power levels. Selecting the band permitting the highest output power is part of, but not all, the issue:

Path loss increases with frequency, proportional to $-10 \times \log(1/f^2)$, which means that (assuming the same aerial gain, transmit power and receiver sensitivity) a 173MHz VHF link will see 14dB lower path loss than an 869MHz one. In other words, a 10mW, 173MHz link will have similar range to an 80mW 458MHz one, a 250mW 869MHz one, or a (hypothetical) 2W system at 2.4GHz.

But lower frequencies require larger aerials for a given aerial gain performance, which can be an issue in the mechanical design of the product. (An 869MHz whip aerial is 9cm long. The same 1/4 wave antenna at 173MHz is 43cm).

A good rundown of the available UK frequency allocations can be found at **www.ofcom.org.uk/static/archive/ra/publication/ra_info/ra114.htm** and **www.ofcom.org.uk/static/archive/ra/publication/ra_info/ra365.htm.**

“It all depends on what you mean by 'short range'. Simple, wideband ISM implementations rarely exceed 100m”

5. Pay attention to the aerials. The best radio on earth won't give good results if it's sited down a manhole, or uses an inefficient aerial.

For long range links, plan to use a good quality helical (not a compressed 'stub' design) or a quarter wave whip as a minimum. If space (and cost) constraints permit, then a true dipole or a 5/8 wavelength design will offer superior performance.

But pay especial attention to radiated power limits in the chosen band, which will prohibit the use of an antenna with more than unity (0dBi) gain at the transmitter. The receiver antenna can, however, have as high a gain as circumstances permit. On fixed links even highly directional 'Yagi' arrays can be used, with gains sometimes exceeding 20dBi.

6. Height matters! Mount the aerials as high up as feasible. Referring to the path model again, the loss is directly proportional to $-10 \times \log((Hr \times Ht)^2)$.

Mounting the aerials 2m above ground level will improve the path loss by 12dB and double the expected range. A 4m elevation of both (the height of a first floor window ledge) should quadruple the range.

7. Test is everything. At the risk of labouring a point I've made before, only a practical test of your application in the eventual environment will confirm for certain your design assumptions. Egli's model is only an approximation, and path losses can be much less (over sea or rivers for instance) or far higher (in buildings, around tall structures, in difficult terrain). Interference can ruin receiver performance. An error in aerial mounting can reduce transmit power.

Go out and try it.

Note 1: Referring to the Egli irregular terrain path loss model, expressed in dB terms:

$$\text{Path gain (dB)} = 32.4 + 10 \times \log(1/d^4) + 10 \times \log(1/f^2) + 10 \times \log((Hr \times Ht)^2) + Gt + Gr$$

F = frequency in MHz
d = distance in meters
Gt, Gr = transmit and receive antenna gain (dBi)
Ht, Hr = height above ground of transmit and receive aerials

Note 2: Practical data rate testing: Using a CTR44 biphase coder/decoder pair and a –120dBm (for 12dB sinad) narrowband receiver (a Radiometrix LMR2-433-5).
Reliable (sub-1% data error) signalling at:

4kbit/s	–116dBm
2kbit/s	–118dBm
1kbit/s	–120dBm
500bit/s	–122dBm
250bit/s	–124dBm
125bit/s	–126dBm
62bit/s	–127dBm

Without reducing the post-detection AF bandwidth, no improvement beyond –122dBm is seen. The 250, 125 and 60bit/s figures are achieved with the reduction in filter bandwidth to 300, 150 and 75Hz respectively. At data rates below 50bit/s, the receiver's data extractor (an 'average and compare' circuit) is no longer functional.

Simple communications theory predicts a 3dB improvement in S/N (and hence signalling sensitivity) with each halving of bandwidth. This is not seen here, as the FM demodulator and the data squaring comparator introduce non-linear transfer functions into the signal path.

For a description of a practical 30bit/s example see also Application note 003: Long range low speed telemetry at:
www.radiometrix.co.uk/apps/apnt003.htm

Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd
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The secret is in the TUNER

PHIL SPRUCE, MARKETING MANAGER FOR HANDHELD DEVICES AT US-BASED MICROTUNE, ANALYSES THE DESIGN TECHNIQUES NECESSARY TO DELIVER A TROUBLE-FREE TV RECEPTION ON A MOBILE HANDSET

Mobile TV is gaining momentum as network operators begin to rollout commercial services and to expand field trials across more and more countries. For manu-facturers, however, considerable technical issues need to be taken into account when adding mobile TV capability to handsets and portable devices. For example, it is imperative to have a constant picture and audio – regardless of environ-mental interference factors – and the TV receiver must operate at low power. The digital video broadcast-handheld (DVB-H) standard has made an effort to address the issues of low signal levels, interference and power, but still more issues remain. For instance, in order to meet consumer expectations for mobile TV, the service must offer high reliability and quality, and meet the cost expectations of the market.

Design Selection Checklist

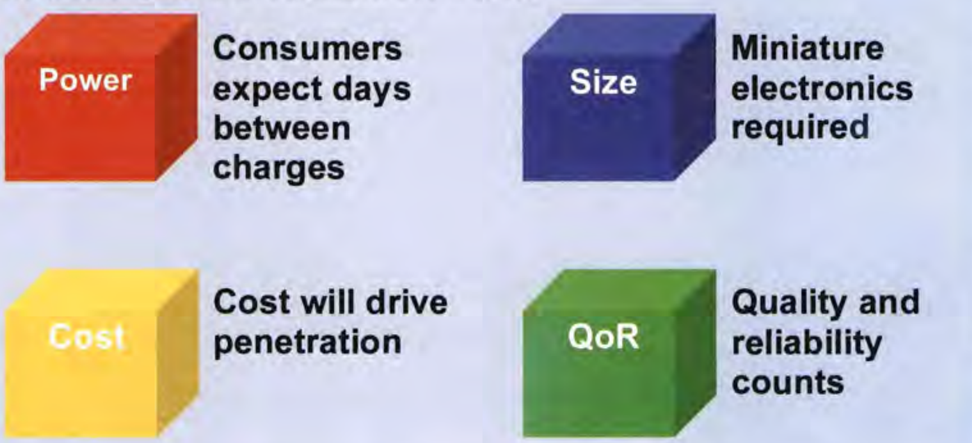
There are four key design criteria for a successful mobile TV platform power consumption; size of the complete solution; quality of reception (QoR) – ensuring that mobile TV always has a picture and sound; and cost.

The issue facing handset manufacturers is that there isn't a single standard that specifies the necessary performance for mobile TV in the real world. For instance, The Mobile and Portable DVB-T Radio Access Interface Specification (MBRAI) for DVB-H addresses how mobile TV reception will work, but does little more than specify conditions for laboratory testing.

The MBRAI specification covers general radio perfor-mance, but does not address performance issues in the real world. For instance, for quality mobile TV reception, the tuner needs at least 20dB additional rejection at higher frequencies to reject a mobile phone's own GSM carrier. MBRAI simply restricts the number of higher frequency channels that can be used. It is up to the tuner manufacturers to identify and solve these technical issues, and it is up to the handset vendors to ensure that they select the tuner with the right level of quality to ensure a successful mobile TV application.

So, what does all of this mean for the technical parameters of the tuner and demodulator that are the heart of the mobile TV functionality? And, how do you select the technology that will make or break the mobile TV application?

Figure 1: Building blocks for a successful DVB-H device



Power And Interference

In the early stages of mobile TV development, the key technical concerns were interference and power. In response, the industry worked to develop the DVB-H standard to address these first hurdles. Based on the pervasive Digital Video Broadcasting-

Figure 2: *DVB-H cell phones bring broadband TV into a narrowband system. DVB-H tuners must tune over a wider frequency range, as illustrated below by the European UHF band. The tuner must retain high-signal integrity, while preserving battery life*

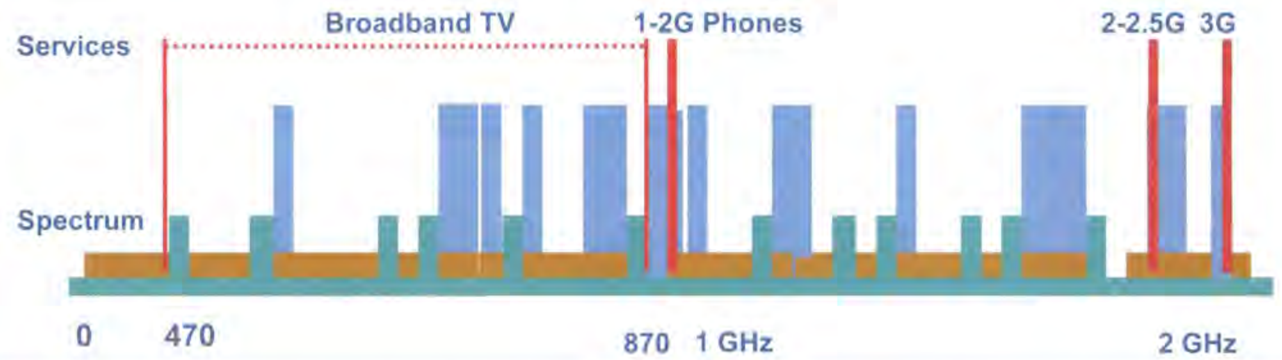
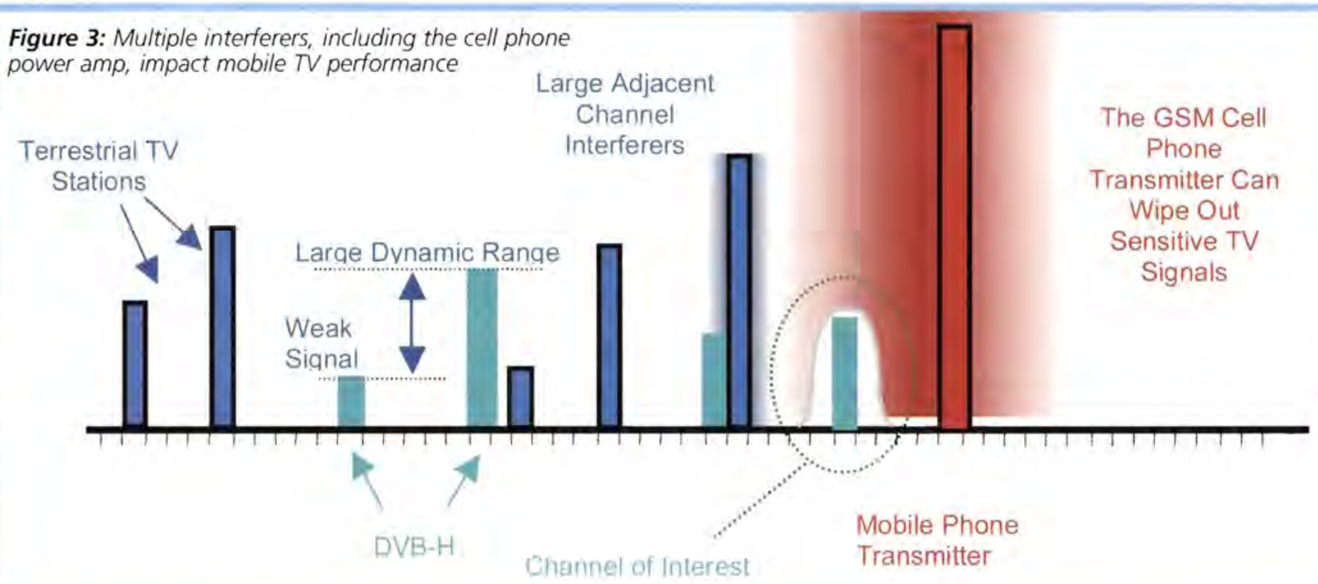


Figure 3: *Multiple interferers, including the cell phone power amp, impact mobile TV performance*



Television (DVB-T) open industry standard for digital broadcasting, DVB-H uses time slicing, modulation techniques and error correction to overcome issues of power and interference.

Enabling up to four hours of TV viewing on a single battery charge, time slicing allows the handset to support a range of TV content without severely draining the battery or impacting the ability to receive cellular calls. With time slicing, each TV program is broadcast at a different point in time, so, when a user selects a program, the handset only receives that TV signal and can power down in between transmissions of that channel's content. In the end, the mobile handset will have three modes of operation: communications, TV and standby. All will drain the battery to some degree, therefore, they need to be optimised for low power. Current industry estimates expect consumers to use their portable devices for two to four hours of talk, two to four hours of TV viewing and a few days of standby time on a single charge. In the end, the biggest drain on the power budget for mobile TV is now the backlight on the screen, which can consume between 200mW and 300mW.

In addition to time slicing, the DVB-H standard specifies the use of Coded Orthogonal Frequency Division Multiplexing (COFDM) modulation. COFDM uses subcarriers which are responsible for transmitting small amounts of information. So, if one carrier is lost or destroyed during transmission due to some type of interferer, then only a small amount of the signal payload is lost. Error correction specified in MBRAI will enable the lost data to be recovered. However, if the received signal is very small or the local interferes are very large, then many of the carriers can be lost. In this instance the error correction will not be able to reconstruct the lost data.

A high-performance tuner will greatly improve the chances that a transmitted signal will be decoded by the receiver, but at the expense of slightly higher tuner power. It is left to individual vendors to choose a receiver that will function in a challenging operating environment that is crowded with interferers. The quality level of the tuner and demodulator has a direct impact on reliability, signal quality and cost. And, it ultimately can determine the success or failure of the application.

Reliability

In the early days of mobile phones, dropped calls were annoying but accepted as a limitation on the system. Technology has moved on. Today it has become

***Figure 4:** Building blocks for a successful DVB-H tuner*

unacceptable to drop calls. With mobile TV, consumers will expect the same quality of reception and high reliability as a conventional TV. They will not accept picture corruption or audio drop-out, so the TV signal reception must be constant, regardless of whether the user is on a train, downtown, or at home.

One challenge to mobile TV reliability is the operating environment. Depending on where the handset is located, it may receive a very large or very small signal; both can be challenging for a tuner to discriminate. To be successful, the tuner needs to have a broad dynamic range and have the ability to discriminate the wanted signal from adjacent TV channels or other in-band interference, which could even be a mobile phone's own transmissions.

Mobile phone receivers operate in narrow frequency bands, typically 20 to 30MHz. To improve reliability in these systems, designers can put a narrow band filter in front of the receiver and effectively eliminate potential interferers across a broad spectrum. In contrast, a mobile TV receiver has a wider bandwidth. The first DVB-H tuners will need to tune across the UHF band IV-V frequency range (470MHz to 860MHz) with 6MHz, 7MHz or 8MHz channel bandwidths in Europe, and the L-band 5MHz channel at 1670MHz to 1675MHz in North America. The situation is particularly challenging in Europe, where the spectrum is fragmented by country and cellular transmitters are often spread into the same bands as mobile TV.

As a work around, the DVB-H standards committee has reduced the usable bandwidth for mobile TV within the allocated band up to 702MHz, but there are a number of companies that would like to use the higher frequencies. Clearly, truncating the available spectrum is only a short-term fix and a new tuning technology is needed.

For signal reliability, handset manufacturers need to select a tuner with the ability to discriminate the desired DVB-H signal. That in itself is quite a challenge for any application. One way to improve tuning for mobile TV is to use new on-chip filtering techniques.

Developed using expertise in cable set-top box, traditional television and automotive TV systems, Microtune's ClearTune technology, which is implemented in its Mobile MicroTuner chips, offers in-band rejection of an undesired signal that cannot be stopped by the external filters. Such a technology enables in-band filtering on both sides of the desired carrier and it will significantly reduce the impact of the mobile phones GSM 900MHz power amplifier (PA) signal that generates a blocking signal inside the phone. It can reject the GSM carrier, suppress other unwanted signals and provide improved performance. The technology helps to ensure that neither audio nor video signals are lost, which has a direct impact on perceived quality.

Quality

Quality of the mobile TV experience may not be very important for a user of a low-tier handset, where voice calls are the priority and an added feature that works marginally well is acceptable to the customer. However, for the consumer who wants mobile TV, maintaining the picture and audio quality will be critical to the application's success. Typical users of high-end smart phones and feature-rich phones expect their features to work well. For designers and vendors working in the mobile TV space, satisfying these discerning customers will be critical to the application's ultimate success or failure. In this case, the picture quality must be very good and the performance must meet or exceed the hype. As a result, it is important to select a high-quality tuner and demodulator for this type of high-end application, anything less would risk failure.

To comply with the DVB-H standard, the tuner must select a single 6MHz, 7MHz or 8MHz channel out of the entire band of channels. The rest of the frequency spectrum in the UHF band IV-V will be made up of an unknown combination of analogue and/or digital TV signals at potentially large amplitudes relative to the desired TV signal. The receive system in the handset will need to handle maximum signal levels up to –25dBm or higher without distortion, as well as amplifying signals near to the thermal noise floor.

The tuner must handle this large dynamic range of desired signals in the presence of many other distorting signals that could be much stronger than the desired minimum signal level. The undesired signal power to the desired signal power ratio can be > 45dB and as much as 56dB for certain conditions. This means that the receiver needs to be able to amplify the desired signal in the presence of an interfering signal that is > 45dB higher. If it cannot do that, the tuner cannot deliver the performance necessary to ensure a quality end-user experience.

Features Affecting Cost

As with all applications, the total solution price for mobile TV functionality is expected to drop with market penetration. Early bill of materials (BOMs) ranged from $14 to $18, with the industry looking for the cost to drop to $5 by 2008, when DVB-H is likely to be a standard feature in many handsets.

In addition, reducing the footprint of the mobile TV functionality will impact cost, but it is also necessary due to the shrinking real estate inside of next-generation handsets. In order to support additional features, these handsets might have more Flash memory, a hard drive, MP3 capability, PVR functionality, location services, Wi-Fi, Bluetooth and FM radio.

Any new function has to be small. The complete DVB-H function needs to be squeezed into a space smaller than 10 x 10mm.

Don't Skimp On The Tuner

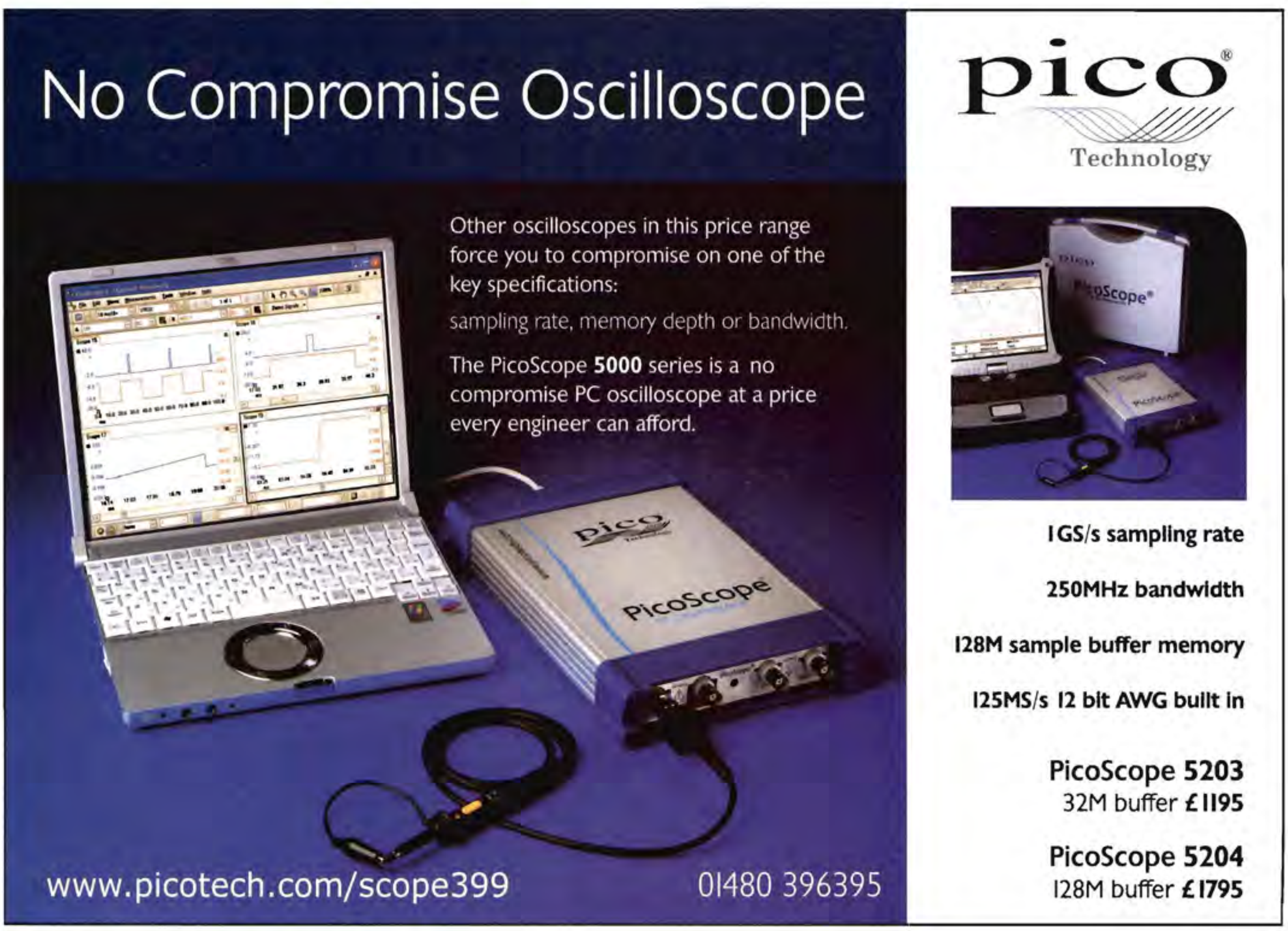
When selecting a tuner for mobile TV, manufacturers need to look for one that was specifically designed for this application and make sure it was designed with on-chip filters and low-noise amplifiers that prevent interference. There are several main priorities (in order of importance) when selecting a tuner.

Quality of reception is most important of all. If the user experience is bad in the early years of mobile TV launch, it can lead to poor adoption, criticism from the media and users and, ultimately, delayed penetration into the high volume mobile phone market.

Cost must be low in order to enable penetration into low-end handset markets. Look for a tuner that offers small size and low height.

Equally, the power consumption of the tuner is very low compared to other functions and does not have a big impact on the power budget.

Skimping on tuner quality could be a fatal mistake for handset designers adding mobile TV functionality to next-generation devices. Dropped TV programs, loss of picture and audio are the likely outcome for users of mobile TV applications that use a low-end tuner.



MANAGING POWER

WHAT ARE THE POWER DIFFERENCES BETWEEN WIMEDIA, BLUETOOTH AND WI-FI? BILLY BRACKENRIDGE, PRODUCT ARCHITECT AT STACCATO COMMUNICATIONS EXPLORES FURTHER

Power consumption has always been a major concern for engineers designing wireless devices. In the recent past one could get away with a simplistic approach – "Bluetooth is for applications where power consumption is of primary importance and Wi-Fi can handle everything else".

The successful use-cases for Bluetooth and Wi-Fi were fairly limited. Bluetooth provided the link between a handset and a Bluetooth earpiece. Wi-Fi connected laptops with Internet access points.

A new class of digital wireless interconnect will begin appearing on the market in 2007. WiMedia is an implementation of ultrawideband technology standardised by the WiMedia Alliance – a consortium of more than a hundred companies large and small that have joined forces to promote a standard radio.

The use cases for WiMedia are expected to be much wider than Bluetooth and Wi-Fi have seen to date. WiMedia is the basis for several different wireless schemes.

Certified Wireless USB allows a wireless link to replace USB cables. This standard is backed by the USB Implementers' Forum. Bluetooth 3.0 is a faster implementation of Bluetooth backed by the Bluetooth SIG; and WiNet is a scheme for extending 802.3 frames over WiMedia links. This standard has been developed by the WiMedia Alliance. It may be adopted by the Internet Engineering Task Force as a standard at some future date.

There has been some interest in carrying IEEE 1394 over WiMedia radios, but the group behind this has not been active recently. In addition, there are proprietary schemes using the WiMedia radio.

Applications are expected to range from streaming video between a set-top box and a display, to portable media players discovering one another and sharing files. WiMedia will be employed to allow handheld devices to display video on TV and PC screens (see **Figure 1**). As technology matures, we expect to see WiMedia support multi-gigabit streams and low-cost devices such as mice and keyboards.

WiMedia cannot prosper as a business unless it is built on a solid technical foundation. Power management, particularly for battery powered devices, poses unique engineering challenges.

A Rising Tide Lifts All Boats

To some extent we are all prospering on the improvements in process technology for making integrated circuits. With WiMedia this is not accidental. WiMedia is based on a technique called Multiband Orthogonal Frequency Division Multiplexing (OFDM). Early ultrawideband radios used impulse techniques that could be implemented with simple analogue circuits. These schemes were rejected in favour of OFDM because planners knew that the digital approach would become more flexible and cost-effective as technology evolved. OFDM can only be implemented in digital circuitry.

It takes tens of millions of transistors to implement a WiMedia radio. The first generation radios seen today require about 600mW at peak power consumption. As CMOS process technology evolves,

Figure 1: *UWB provides the inherent flexibility and bandwidth for handsets to interface directly with larger displays such as TVs*

CONSUMPTION in WiMedia Devices

this figure will drop. Several years ago, OFDM seemed impractical to some, but today it is practical and performance will improve significantly as the next decade brings improvements in CMOS process technology.

Integrated circuit designers will practice their art and all of us will benefit, but there is plenty the system designer and software engineer can do to improve the power efficiency of systems built around the WiMedia radio.

Better To Transmit Than Receive

Normally radios consume the most power when transmitting, but WiMedia is unique in that it consumes more power listening than it does transmitting. Receiving means a signal is present and Wi-Fi uses a bit more power receiving than 'listening', which is where a signal is not present.

In a WiMedia radio, listening is the most expensive mode in terms of power consumption. WiMedia radios work by digitising the radio signal at a high sample rate and looking for patterns of energy over a wide area. Power-constrained devices can't afford to listen for long periods of time. Transmitting requires slightly less power than listening. These patterns of power consumption differ fundamentally from earlier radios such as Wi-Fi and Bluetooth. While these other radios attempt to minimise the amount of time that is spent transmitting, software running in the WiMedia MAC attempts to limit the time spent listening.

Stand And Wait

Wi-Fi, Bluetooth and WiMedia all have similar concepts of standby or ready modes. Power saving schemes attempt to either completely turn the radio off or enter some sort of standby mode.

When active, WiMedia radios announce their presence by beaconing every 65ms. This would be considered excessive for Wi-Fi, where only the access point beacons and clients listen for a transmit opportunity to be assigned by the access point. With Wi-Fi it can usually be assumed that the access point is mains-powered. In contrast, WiMedia may be deployed in situations where all devices are living off limited battery power.

The 65ms beacon period allows all WiMedia devices which share a beacon period to share a microsecond accurate clock. In the WiMedia universe, time is divided into 256 MAS (Medium Access Slots). Each MAS represents 256 microseconds. WiMedia radios can turn themselves on or off to listen or transmit at a time accuracy of one microsecond.

The combination of a high resolution timer and fine granularity of allocation of bandwidth implies that WiMedia radios are capable of implementing sophisticated power saving schemes by managing traffic patterns.

Certified Wireless USB, WiNet and Bluetooth 3.0 all are based on the WiMedia radio, but each application anticipates different usage scenarios. Each approaches power management differently.

Certified Wireless USB: The Host Does The Most

Conventional USB was designed so that devices could be very simple. Most of the burden is placed on the host. This is particularly important for timing. Mice are polled every eight

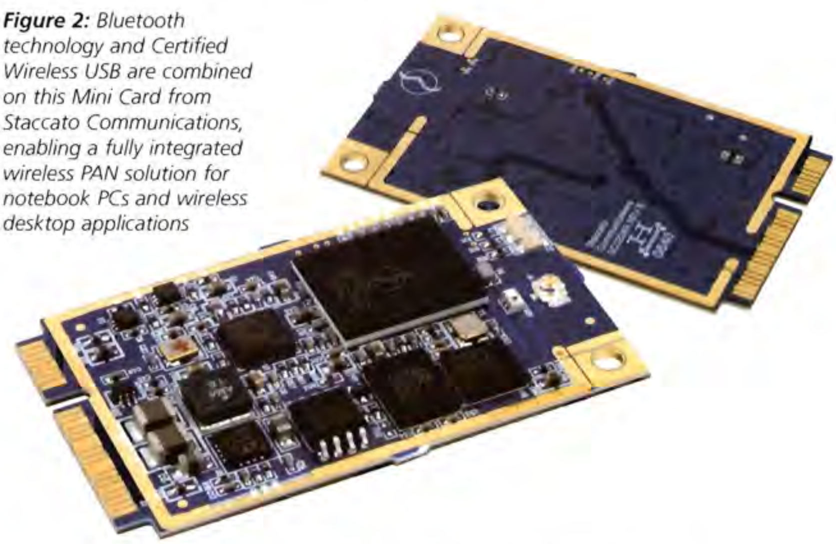


Figure 2: *Bluetooth technology and Certified Wireless USB are combined on this Mini Card from Staccato Communications, enabling a fully integrated wireless PAN solution for notebook PCs and wireless desktop applications*

milliseconds. If the polling interval isn't regular or accurate, mouse movement will appear jerky or unresponsive.

Certified Wireless USB has expanded on this model to include hooks for power savings. The host knows exactly when it is going to poll a device and tells the device in advance when this will occur. This way the device can go to a low-power state and wake up just in time to transfer data.

The mechanism to do this is called a Micro-scheduled Management Command (MMC). MMCs contain microsecond accurate time stamps that point to a linked list of transaction groups. Transaction groups bundle together several writes and reads. This way the device wakes up at a pre-arranged time and receives data from the host and then immediately transmits data back to the host. Before the device goes back to a low power state, it reads the time stamp from the MMC so it knows exactly when it must wake up again.

This allows the host to be completely in charge of bandwidth and link management. It can choose bit rate and transmit power levels appropriate to the situation. Devices can remain in a low power state (not listening) whenever they are not actively engaged in transfers.

If a device needs to turn itself off completely for a period of time, it can petition the host to go into a sleep state. If the host grants the request, the device can sleep,

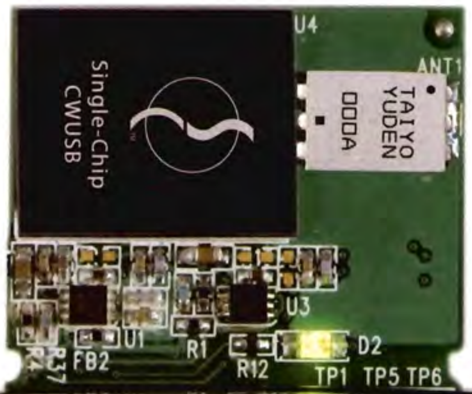


Figure 3: *Staccato SDIO-enabled PDA*

waking up every few seconds to check to see if there is work to be done.

WiNet: An Anchor In An IP Storm

WiNet is the WiMedia defined way to carry IEEE 802.3 frames and, therefore, Internet protocols over the wireless link. WiNet introduces the concept of a WiNet Service Set or WSS, which is a named group of devices that share a security relationship. WSS was designed to make it easy to form secure ad hoc networks, where devices can discover each other and form securely encrypted links.

WiNet includes the concept of a bridge that is similar to a Wi-Fi access point. Unlike Wi-Fi, Certified Wireless USB and Bluetooth there is no 'master'. All WiNet devices are peers.

All active devices are required to beacon, that is announcing their presence in a beacon group. Sleeping devices can miss the beacon period for several seconds before they are considered disconnected from the WSS. Obviously, all devices can't go to sleep at once. Somebody has to stick around and beacon so that everyone can keep their clocks synchronised. This node is called the anchor. WiNet devices advertise in their beacon whether they have limited power or not. If a mains-powered device is available, it will become the anchor. If not, responsibility to be anchor will be shared among peers and transferred every few minutes to another node.

WiNet can be used to provide Internet access. Bridges can easily link to Ethernet, Wi-Fi or any IEEE 802.3 networking technology. There can be several bridges in a WSS, but the usage case for WiNet is expected to be primarily for ad hoc networking.

To date, there has been very little ad-hoc networking. Ad hoc networking is where devices come together and assign themselves 'ad-hoc' network addresses rather than rely on a managed server to keep track of Internet addresses. Microsoft's new media player Zune is an excellent example of ad-hoc networking, but it is a closed system. Many people are complaining that Zune doesn't allow file downloads from the Internet or 'DJ' mode where music can be streamed in real time to a group of listeners.

WiNet is an open, (soon to be) published specification for secured ad hoc networking that includes a robust scheme for power management appropriate for battery-powered devices. With an open specification everyone is free to innovate and we expect to see new ways of sharing media that go far beyond what Wi-Fi has done to date.

Bluetooth 3.0: By Version 3 We Got It Right

The Bluetooth SIG has adopted WiMedia as the basis for Bluetooth 3.0. Technical details of the implementation have not been released by the Bluetooth SIG working group, but the study group which recommended adopting WiMedia publicly announced some guidelines.

Bluetooth 3.0 will be backward-compatible with the standard's earlier versions. This means there will be two radios side by side or two radios built into the same chip or module. Staccato Communications has demonstrated a USB Mini Card Slot device (see Figure 2) that includes Staccato's Ripcord single-chip CMOS WiMedia radio sharing an antenna with a Bluetooth device. Because the UWB radio and Bluetooth radio don't interfere with one another, both radios can operate simultaneously using the same antenna.

WiMedia and Bluetooth are complementary from a power usage perspective. WiMedia is the most power efficient means for moving bits in terms of Joules per bit. (For those who have forgotten their secondary school physics, a Joule is a watt second or the work done to produce power of one Watt for one second).

WiMedia achieves this efficiency because its high transfer rate allows it to transmit many bits in a short period of time. On the other hand, Bluetooth is more efficient at keeping a link open as it is able to wake up every few seconds, send a short message and go back to sleep.

The Bluetooth SIG expects to use conventional Bluetooth in its standby mode keeping the WiMedia radio completely off until such a time as it is needed to transfer a file or stream video or audio.

Today, Bluetooth has a significant advantage over WiMedia in standby or sleep modes in that it is a simpler radio and can be implemented in a fewer number of transistors. Bluetooth in its standby modes consumes only a few microwatts of power.

There are two techniques of achieving low power states for digital circuitry, clock gating and power gating. With clock gating, you turn off the clock driving the circuitry and current usage drops, but there is still leakage. When there are millions of

A NEW CLASS OF DIGITAL WIRELESS INTER-CONNECT WILL BEGIN APPEARING ON THE MARKET IN 2007

transistors, leakage becomes significant. With power gating, you turn off power to selected sections of the chip and no current is used.

Chip designers believe that, over time, the low transistor count advantage of Bluetooth's simpler radio will go away as power gating techniques become more sophisticated. Today, the latest generation of Wi-Fi chips designed for portable devices match Bluetooth power consumption in low power modes. First generation WiMedia draws more power in low power modes, but chip designers believe that over time this differential will diminish.

Power To The People

WiMedia's biggest advantage in power savings comes from its ability to transfer at high data rates. When listening or transmitting it uses about the same amount of power as other radios, but because it can move bits so fast, it doesn't have to be on as long.

This is particularly important in laptops where running the CPU requires significantly more power than just running the radio. When moving large media files, such as a full-length motion picture, this speed advantage translates to long battery life for laptops and smaller batteries for mobile phones and media players.

With more than $250m invested in start-up venture capital, many people are betting on the success of WiMedia. The first products will be cable replacement for USB. This isn't a particularly challenging area from a power management perspective. Devices like printers, hard drives and hubs are externally powered today and will remain that way. If WiMedia is to sell in really huge volumes, it must prosper in environments where power is at a premium such as PDAs, mobile phones, digital cameras and portable media players (**Figure 3**).

There is significant work to do in developing the next generation products that will define the wireless revolution to come, but the plans are in place and the foundation has been built.

THE WIRELESS CHALLENGE

WIRELESS INNOVATORS NEED TO FULLY UNDERSTAND THE TIME IT TAKES TO BRING A PROTOTYPE – THEN A PRODUCT – TO MARKET, BUT ALSO SEE THE TRUE POTENTIAL OF THE ROLE UNIVERSITIES AND ACADEMIA CAN PLAY IN THE INNOVATION PROCESS, SAYS DR ALEC READER, BUSINESS DEVELOPMENT DIRECTOR AT INNOS

We all come into contact with hundreds, perhaps thousands of every-day examples of how wireless technology is applied in our environment, with glimpses of what is to come. The boundaries do not stop at commonplace objects such as mobile phones, handheld games consoles, headphones and Bluetooth connectivity – one day everything we see or do will have an element of wireless technology.

The Barriers To Market

In the UK, many innovators of wireless technologies – especially those with an avant-garde or unconventional approach – face considerable challenges when pushing their concept through to the mainstream market. Not only the business basics – funding, organisation etc, but also in terms of attaining economies of scale, acquiring the right expertise, reducing risk, increased consumer demand for integration with incompatible technologies, maintaining quality and, also, the constant struggle in reaching a point where mass manufacture is viable. It is generally believed, though somewhat cynically, that those with money and whose business it is to push new products to market will prioritise based on what will make the most returns the fastest. Anything out of the norm opposes little chance in the real world. However, this does not have to be the case and this misjudged view is changing.

Rapid Prototyping To Bridge The Gaps

The first step on the path to mass manufacture is a working prototype; it is also one of the most prominent roadblocks. The wireless market is fast paced and constantly changeable and consumer demand is the lynchpin. Take for example the latest mobile phones – consumers continually expect them to incorporate increased functionality (i.e. Blue-tooth, GPS, Internet etc) yet maintain a small size. The components that power many of these functionalities need to evolve, through continual design modification and also preserve economies of scale. The fabrication processes required for transistors and RF CMOS – the core of integrated circuits (ICs), which power mobile phones, handheld PCs and other wireless devices, are heavily dependent on many sequential precision-manufacturing steps. These steps consequentially lead to long manufacturing cycle times and high costs. The whole reiterative process for prototype manufacture can frequently take more than one year and, by the time the project is completed, it is already outdated. However, UK businesses are now beginning to question this once accepted norm.

With Europe as the world leader in the hotly debated RF CMOS product development sector, the UK is estimated to own about 40% of the world's RF CMOS design capability. It is in a strong position, but staying ahead of the game means it is crucial that future problems, opportunities and barriers are identified at the outset, in order to drastically decrease fabrication time and cost and ultimately improve marketability. Most of these companies are fabless, i.e. they don't have their own silicon fabrication capabilities, so they must approach a specialist manufacturer. Yet anyone who has worked with the large fabrication houses (fabs), where the vast majority of this manufacturing is done, will recognise that the relationship is very much one-way traffic, whereby these trends are rarely, if ever, highlighted to the customer.

Typically, new RF CMOS ICs are developed from original circuit designs. Developing these into working products requires a number of iterative manufacture steps, during which prototype circuits are manufactured and tested. The traditionally held view is that the only way to test a new circuit is to manufacture a bulk lot at the fab (typically located in Asia), ship them home and test them, then, if necessary, follow with an investigation to identify the reason for failure, modify the design and start the cycle again. This ultimately leads to the requirement for the

THE WIRELESS CHALLENGE

One handset can handle more than two or three wireless standards

Bluetooth headset

manufacture of further prototypes, but all this takes time (typically 18 months for a full cycle) and time costs money.

Of course the trick to fill this gap between the innovator and the fab is to get the prototype right before it is shipped and this insight, be it research, development, prototype creation or purely consultancy, needs to be home-grown to ensure the competitive advantage is maintained. If prototyping cycle times can be accelerated to a few months, using a home-grown company with right expertise and tool sets to fabricate the prototypes, an innovator can increase their chances of success. Risk of failure is significantly reduced, thus the innovator not only saves costs in avoiding having to ship and wait for prototypes – that are potentially unworkable and geographically distant, but ultimately the design is improved and competitive advantage is maintained.

Maintaining Quality

If an innovator is reducing its prototyping cycle times, it has already given itself an edge in terms of keeping up with consumer demand. However, the fast-paced nature of the wireless market can put significant pressure on innovators to maintain quality. With product lifecycles shortening (some wireless devices last mere months on the market before being replaced with improved or cheaper designs) and the selling price of products in continual decline, then maintaining quality is king. For the small to medium sized innovators this is exacerbated when you try to keep a very flexible research environment, whilst cultivating a quality culture.

Quality is the result of achi-eving the right blend of skilled people, equipment and tools, appropriate materials, defined procedures, understanding client needs and wants and proven quality monitoring processes. Yet many of these processes have been developed over the years by big companies and remain the preserve of big companies, who have the expertise and resources to write and implement them. The small innovative company rarely has this luxury but, in order to compete, is still reliant on the delivery of a quality product.

With product life-cycles declining, the speed to market of new products is vital to success. It is imperative to identify and remove the barriers between departments – including the fab, in office and shop floor processes and equipment bottlenecks. Removing these barriers will frequently improve other aspects of the process and improve quality. Also, time should be taken to listen to the customer and understand what they regard as a value add, using this to effectively remove unnecessary steps that slow the processes down.

Quality of wireless products also comes under the microscope when an innovator is looking at reducing marginal costs of manufacturing each prototype or device. One material, such as silicon, may very well be sufficient for a university student to complete a prototype device and write a thesis, however, when the innovator takes into account consumer expectation of quality, as well as keeping costs low, another, cheaper material, such as polymer, could be used to the same or similar effectiveness.

Integration Of Incompatible Technologies

Wireless technology faces another emerging challenge in order to meet consumer pressure. This lies with the limited – and still learning – expertise available to enable the integration of seemingly incompatible technology. For a long time we have recognised the numerous market applications and increased functionality that come with being able to create a device which uses wireless communication (RF CMOS), but also incorporates a self-powering element and a sensor. This is very much the Holy Grail of many wireless and MEMS innovators. Of course these technologies are as far removed from each other as chalk and cheese, and integrating these onto one chip is a very complicated and expensive process. The resultant prototype is, of course, high in added value.

An example of such an application is a self-powering, self-communicating sensor, comprising of a MEMS energy-harvesting device, a sensor and an RF CMOS IC. Temperature in horticulture is critical; so consider an owner of a vineyard monitoring the temperature of the grape vines. If the temperature falls below a certain point, the harvest will be killed and revenue for the season will be lost. These integrated devices could be placed at various points across the vineyard, which powered by the movement of the vines, can create a temperature map by sensing the environment. Information from the devices can be transmitted via radio frequency to a receiver in the corner of the vineyard. If the temperature is nearing critical, the owner could be alerted via text message for example, and they could then take steps to rectify it.

Encouraging Innovation

The wireless market itself also faces a considerable challenge in keeping itself fed with new ideas. So far this article has addressed what could put a stopper in the works for an innovator or innovative company, but with all these problems to resolve, some innovators and companies can be put off attempting to enter the race to market and opt for licensing out their patents to other companies instead. The market risks developing a gaping hole in the volume of new ideas and innovations, however, the UK's university network is bulging with fresh approaches to technology and brand new ideas, something which industry has yet to fully embrace.

The same problem is apparent in getting an IC design from a university to a commercial market, perhaps even bigger in that it relies on funding from the government and unless a company is spun out, little or no working capital will be available to get it off the ground. It is unlikely to have access to a fabrication house and the innovator is effectively stopped from exploiting anything new. The university culture is to research a project, develop a concept, publish the results and forget about it. Too many developments of proposals in universities won't make it to the manufacturing stage because they aren't interested in getting it to mass manufacture, selling it to a company to exploit or licensing out the IP. It is then that a gap appears between academia and industry – no willing supply, no demand and little or no communication.

There is certainly no lack of ideas in the wireless arena from universities and research institutions, this is not the problem; the faltering demand from industry due to misunderstanding of the importance of academia to high-technology business and the resultant poor communication are the down-fall. What can be done to bridge this gap in understanding?

A recent Higher Education white paper stated that 80% of UK businesses had absolutely no relationship with universities, whereas it is more likely to be the other way around in the US, where developing academic relationships is heavily practised. A mutual understanding is essential, something which is severely lacking in the UK. Universities and businesses need to actively engage to improve understanding and the transfer of information and technology. To facilitate this exchange of information, an intermediary with knowledge, expertise and understanding of both sides, as well as the wireless market for example, should work to improve the relation-ship and ensure a solid 'chain' from concept of a simple 'eureka' moment through to manufacture at the fab.

The Gaps Are Closing

We are still in the middle of a maturing wireless industry, but with a long way to go in terms of culture and finally achieving that straight path to market. Industry must fully recognise that steps can be taken to maintain low costs in wireless prototype manufacture within the UK whilst maintaining quality and reducing risks, bridge gaps of understanding between design houses, fabs, universities and companies, and still keep up with consumer demand. However, the gate is also finally open for many innovators to realise the potential they suspect of their product and start experiencing revenue streams from what started life as an idea on a piece of paper.

MEASUREMENT METHODS *for a* NEW RF *and* MICROWAVE CALIBRATION SOURCE

Figure 1: *9640A instrument mainframe and levelling head*

The signal sources used in RF and microwave calibration applications are usually general-purpose signal generators, not optimised for calibration requirements. Many generators widely regarded as best suited for calibration use are now obsolete. Performing measurements to evaluate the performance achieved against aggressive target specifications during development, as well as testing products in the manufacturing process, present a variety of technical challenges:

- Identifying methods capable of providing low uncertainties over the range of values required;
- Lack of traceability for certain parameters;
- Identifying alternative techniques suitable as cross-checks to validate the chosen methods.

Appropriate methods are also required for users to carry out routine re-calibration with readily available equipment.

Obtaining high signal purity is important for many calibration applications, often requiring the use of external filters. In the Fluke model 9640A signal source, which has been developed specifically for RF and microwave calibration, low levels of harmonic and spurious content are achieved by the use of appropriate filters within the output signal path. It also features internal analogue modulation capability. Frequency modulation (FM) is generated within the frequency synthesiser at rates up to 300kHz and amplitude modulation (AM) is generated within the output amplification and levelling circuits at rates up to 220kHz.

Level

Measurement requirements include level (RF power), output VSWR and modulation. RF level is measured as an absolute value at a reference frequency, followed by frequency response (flatness) measurements relative to the value at the reference frequency. For the reference point (100kHz), an AC Voltage Measurement Standard measures the RMS voltage developed across an accurately known 50Ω termination, and the corresponding power level is calculated. An RF power meter and power sensor head is used for the high frequency measurements.

This is a commonly used technique, capable of extremely low uncertainty traceable measurements, if appropriately calibrated power sensors with correction data are used. However, it cannot provide sufficiently low uncertainty below about –50dBm. Measurements can be made at lower levels by taking advantage of the linear amplitude response of a modern spectrum analyser [1]. The linearity of such an instrument is almost exclusively determined by the A/D converter used to digitise its IF signal for subsequent processing in the digital domain. Measured analyser linearity errors are generally much less than the estimated uncertainty of the test (< 0.02dB for a 70dB range). At each of the required measurement frequencies, the spectrum analyser is normalised against the UUT output, as measured by the power sensor at –47dBm and without changing analyser settings, measurements are made over a 50dB range down to –97dB. The spectrum analyser is then re-normalised at –97dBm to make measurements down to –130dBm.

Although the general approach is an established technique, additional considerations are important in achieving the low measurement uncertainties required. The power sensors used for measurement of levels above –10dBm employ thermal detectors and are inherently linear over the range of input powers applied. However, at levels below –10dBm thermal sensors are unable to provide sufficiently repeatable accurate results and diode-based sensors are used down at –50dBm.

Diode power sensors are inherently non-linear devices. At low levels, they respond to the RMS value of the input signal and at higher levels, they act as peak detectors. The design of the accom-

IN THIS ARTICLE, **PAUL C. A. ROBERTS** OF FLUKE PRECISION MEASUREMENT DESCRIBES MEASUREMENT TECHNIQUES DEVELOPED FOR DESIGN EVALUATION, MANUFACTURING TEST AND ROUTINE USER RE-CALIBRATION OF A NEW SIGNAL SOURCE DESIGNED SPECIFICALLY FOR RF AND MICROWAVE CALIBRATION APPLICATIONS

panying power meter includes linearity compensation to produce an overall linear power measurement response. However, a small residual error remains, usually described by a linearity specification for the power sensor and power meter by its manufacturer. In this case, such residual errors are too large to be ignored.

This residual linearity error has been found to be frequency dependent and varies between individual examples of the power sensor model used, but is typically up to 0.02dB (0.4% expressed in terms of calibration factor). In practice, a correction is applied. The frequency-dependent linearity correction is determined by measurement in-house and is combined with the correction for the sensor frequency response obtained by sensor calibration at an external calibration laboratory.

Output VSWR

Having knowledge of the output impedance of the 9640A model (source match) is important not only to confirm specifications, but also to allow users to estimate mismatch uncertainty contributions in their applications. The measurement techniques generally used for passive components cannot be used for an active levelled source. If those methods are used, they are likely to give erroneous misleading results.

In operation, any reflections caused by a mismatch between the source and the load will be at the signal frequency, and the levelling circuit will detect the combined effect of the output signal and the reflection. The methods appropriate for passive devices do not give appropriate conditions to correctly measure the equivalent source match. (They can be, and are, used successfully on the output ranges where the output step attenuators are switched into circuit, because the attenuators sufficiently isolate the levelling circuits).

Because active levelled source match measurements can be difficult to perform, most equipment manufacturers do not include source VSWR tests in their published performance verification procedures or application notes. At the time of this work, it was also not possible to identify a calibration laboratory offering an accredited (ISO17025) measurement service for source match of a generator. The chosen method uses a return loss bridge, as shown in **Figure 2**.

A signal generator injects a signal with a small

Figure 2: *Source VSWR measurement*

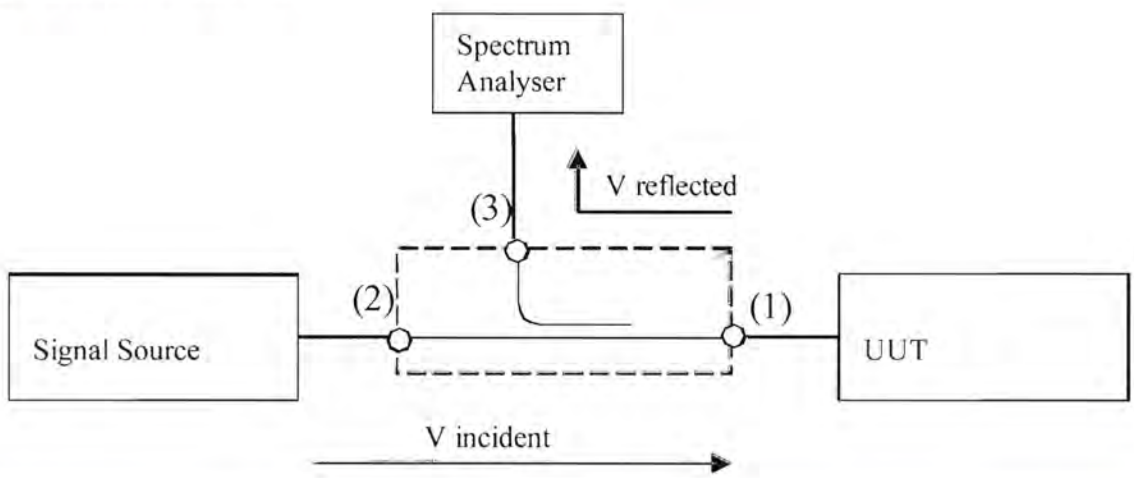
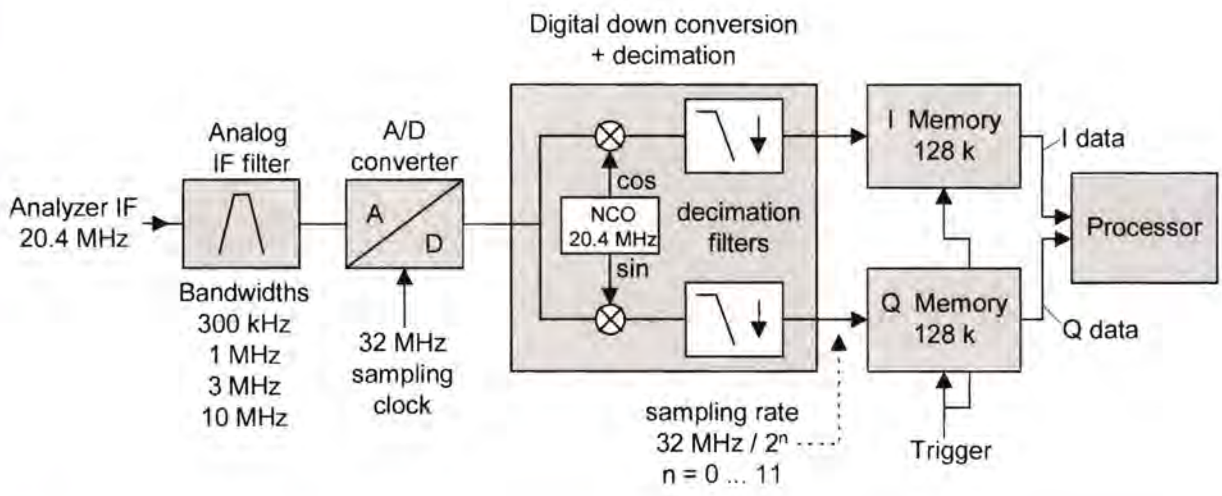


Figure 3: Spectrum analyser signal processing



fixed frequency offset, say 10Hz, from the UUT output frequency. The UUT output and reflected signals will add and subtract at a rate of 10Hz. This signal is detected with a spectrum analyser set to 'zero span' mode, using the cursors to measure the maxima and minima of the amplitude variations with time. A reference level is also measured with the UUT replaced with an open and a short. Voltage Reflection Coefficient and, hence, VSWR is calculated.

Modulation

AM and FM design goals of accuracy better than 0.1% and distortion < 0.05% (–66dB) are difficult to measure with traditional methods. Measurements are made using a spectrum analyser featuring a measurement demodulator (the Rhode & Schwarz FSMR). The demodulator uses digital signal processing to extract the required signal characteristics from data obtained by digitising the IF signal, illustrated in **Figure 3** [2]. By sampling (digitisation) at the IF and digital down-conversion to the baseband (I/Q), the demodulator achieves maximum accuracy and temperature stability. Accuracy and stability are maximised by minimising the analogue circuitry prior to the IF analogue to digital converter, for example by using only the widest bandwidth (10MHz) IF filter.

Obtaining valid and accurate AM measurements depends on setting the spectrum analyser/ measurement demodulator mixer level with appropriate choice of its RF input attenuator settings. The mixer is inherently a non-linear device, used to shift the input signal in frequency while preserving its amplitude characteristics. If the input signal level at the mixer is too high, the signal will be compressed and distor-ted, resulting in AM depth measurement errors and incorrect THD readings.

Making valid and accurate frequency modulation measurements is dependent on setting the measurement demodulator bandwidth appropriately. Insufficient bandwidth will exclude some modulation sidebands resulting in inaccu-rate FM deviation measurements, and excessive bandwidth will increase wideband noise in the demodulated signal.

For AM and FM, measurements of modulation rate, depth/deviation and distortion are made. For example, for distortion measurements, the demodulator is configured to display the signal's audio spectrum and its THD measurement algorithm is used to determine the total of the harmonic content present in the required bandwidth. Analysis of the inherent error sources within the spectrum analyser and measurement demodulator suggest extremely accurate modulation measurements should be obtained; much better than its manufacturer's published specifications suggest.

The Bessel Null or Disappearing Carrier method is a method for FM deviation measurement based on FM theory and is potentially very accurate. It can be used to validate measurement capability. The amplitude of an FM signal remains constant, but the amplitude of the spectral content at the carrier and sideband frequencies is related to the modulation index by the Bessel function. At certain values of modulation index, the amplitude of the signal at the carrier frequency and of the sidebands nulls to zero and this condition can be observed on a spectrum analyser. It is generally easy to provide a modulating signal with an accurately known frequency and as the modulation index value is determined mathematically by the Bessel function, this technique can be used to accurately determine the FM deviation of a signal and, hence, evaluate the measurement performance of both the measurement demodulator and the 9640A. For example, tests of FM deviation accuracy carried out with a 100MHz carrier modulated at 125kHz deviation at 23.113kHz rate (corresponding to the third carrier null) gave agreement between the Bessel Null method, the 9640A and the measurement demodulator of < 0.02%.

Apart from use of the Bessel Null technique for FM deviation measurement, it has not been possible to identify methods or other laboratories, which can provide sufficiently low traceable uncertainties to fully evaluate the potential performance of the measurement demodulator for other modulation parameters. However, some work is being undertaken to investigate alternative techniques based on direct digitising of the modulation signal with fast sampling, but at present, it is too early to discuss details in this article.

REFERENCES:

[1] Rhode & Schwarz application note *"RF Level Test System +20dBm to –130dBm"*

[2] Operators Manual, Rhode & Schwarz FS-K7 Measurement Demodulator

FLUKE developed its new signal source (model 9640A) specifically for RF and microwave calibration applications, providing high-purity precision level outputs covering a wide amplitude range over an extended bandwidth, with precision modulation capability.

Its frequency range is from 10Hz to 4GHz, at amplitudes from +24dBm to –130dBm. The instrument has been designed to generate the signals necessary for the most common RF and microwave calibration applications. It provides inherent accuracy without the need to monitor or characterise the output with additional equipment during use, such as measuring of the output amplitude with a power splitter and power sensor, monitoring of the achieved modulation levels with a modulation analyser and others.

In order to facilitate delivery of the output signal direct to the load or Unit Under Test (UUT) input and minimise performance degradation due to cabling and interconnections, the instrument has an external levelling head (see **Figure 1**). Signals are generated in the mainframe and fed to the levelling head containing the level detector and attenuator circuits.

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Exploring Termination Options

IN THIS ARTICLE, KANNAN SRINIVASAGAM AND JAYASREE NAYAR ANALYSE SIGNAL INTEGRITY OF TRANSMISSION LINES; DIFFERENT FACTORS AFFECTING SIGNAL INTEGRITY, CAUSES FOR SIGNAL DISTORTION AND METHODS TO REDUCE DISTORTION AND IMPROVE SIGNAL INTEGRITY ARE ALSO DISCUSSED

Specialised high-speed memory products optimise memory performance for a variety of networking systems. With the emergence of these high-speed memories, signal integrity has become a concern. Data that used to be transferred at 50-100Mbps has now increased to 250Mbps or even higher.

This article provides an introduction into transmission line and signal integrity basics and provides details on how distortion of these signals can be minimised.

Transmission Line Basics

Transmission lines are connections between a transmitter and a receiver capable of carrying a signal. At low frequencies, a wire or a printed circuit board (PCB) trace may be an ideal circuit without resistance, capacitance or inductance. But at high frequencies, alternating current (AC) circuit characteristics dominate causing impedances, inductances and capacitances to become prevalent in the wire. As signals are transmitted over high speed, even the shortest passive PCB trace will suffer from transmission line effects. Any specific trace on a PCB is considered a transmission line if the time to traverse the length of the transmission line is greater than six times the rising edge of the signal. When both are described in terms of trace length:

$$L_{line} > L_{edge}/6$$

Where L_{line} = length of the transmission line, L_{edge} = length of the rising edge.

For example, if we consider a rise time T_r = 1ns, then based on FR4 dielectric, where propagation delay is approximately 180ps/inch, then the length of rising edge (inch) is:

$L_{edge} = T_r/(\text{PD per inch}) = \sim 6$ inches
Therefore, a line that has a length (L_{line}) greater than L/6 = 1 inch will be considered as a transmission line.

Signal Distortion At The Receiver

High-frequency signals are subject to losses along transmission lines, which interfere with the receiver's ability to interpret the information. Transmission lines must be designed to minimise distortion of the signals at the receivers. In order to minimise signal distortion on a T-line, a system designer needs to understand the causes of distortion.

Distortion in a transmission line arises mainly due to:

- Reflections and ringing
- Crosstalk
- Shifts in reference-levels (power and ground bounce)
- Switching noise due to currents across impedance of the PCB power distribution systems.

This article concentrates on signal distortion due to reflections and crosstalk and how they can be minimised in a system.

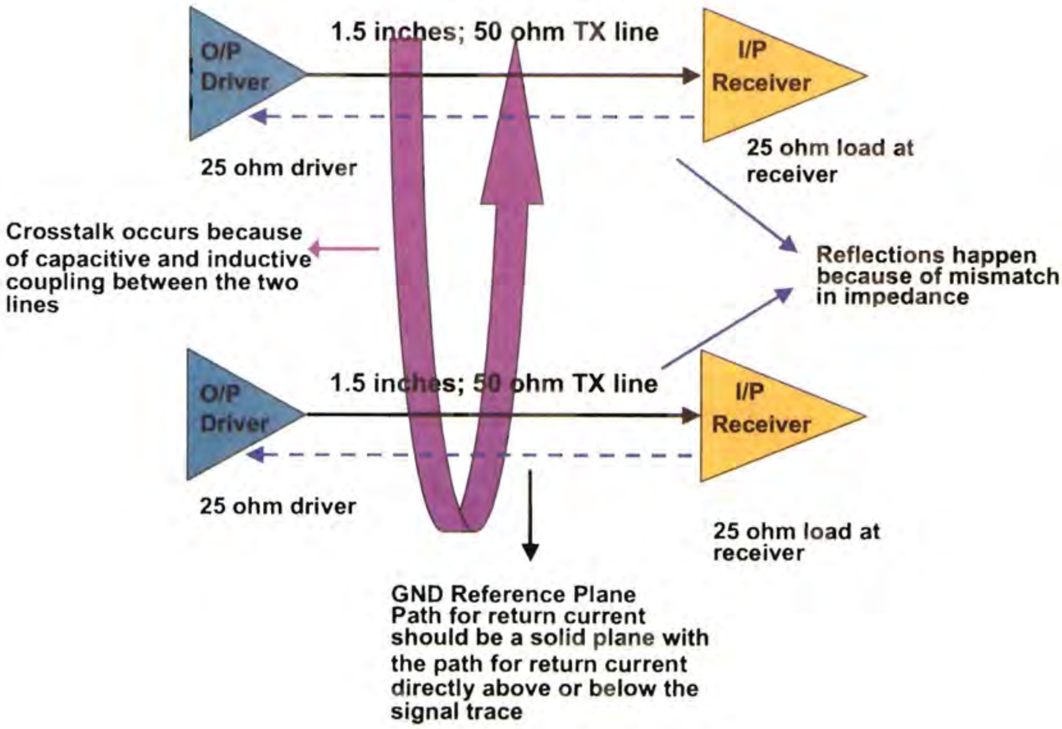
Consider a simple interface where two output drivers (25Ω) of a memory device are driving two input buffers (25Ω) of any logic device. Assuming a rise of 1ns, FR4 board material and the trace length of 1.5 inches, we can conclude that the trace is a transmission line.

Based on this example the different distortion effects that can occur at the receiver are shown in **Figure 1**.

Reflections And Ringing

As mentioned earlier, one of the problems on a T-line is reflections and ringing. This is mainly due

Figure 1: *Different signal distortions on transmission lines*



to the impedance of the transmission line changing. When a driver launches a signal onto a transmission line, the initial voltage will propagate down the line until it reaches the end. If the end of the line exhibits impedance different to the impedance of the transmission line, a portion of the signal will be reflected back down the transmission line toward the source. The amount of the signal that is reflected back is determined by the reflection coefficient as described in the equation below.

If both ends of the line exhibit impedance discontinuities, the signal will reflect multiple times back and forward on the line, with the reflections getting smaller each time until the signal will eventually settle to its final value.

At any point in the transmission line the resultant wave is the superposition of the original wave and all the reflected waves. Reflections should be avoided as they can cause false triggering of logic.

Figure 2 contains the equation used to calculate the amount of energy reflected and overall effect of the signals at the source and the receiver. The measure of the amount of signal reflected back is provided by the reflection coefficient.

The reflection coefficient can be calculated by the following formula:

Reflection coefficient = $(Z_L - Z_O)/(Z_L + Z_O)$

Where Z_L = Load impedance and Z_O = characteristic impedance of the transmission line.

A reflection coefficient of 0 results when the load impedance is matched with the characteristic impedance of the transmission line, implying that there are no reflections of the signal back to the source.

Crosstalk

Crosstalk is another cause of distortion in a transmission line. It is mainly due to mutual capacitance and inductance between neighbouring traces. Crosstalk will change the performance of a transmission line by modifying the effective Z_0 and propagation velocity of that line. It will induce noise onto other lines, which will further degrade signal integrity and reduce noise margins.

Inductive coupling occurs due to the interaction of return current loops (explained below) of two neighbouring signals. Inductive coupling is more predominant than capacitive coupling.

As a signal travels through a trace, it creates a magnetic field. It also reacts to magnetic fields within its path. Therefore, the trace acts as both a field generator and as an antenna. The voltages that external fields cause are proportional to the strength of the external fields and the length of the trace that is exposed to the field. The trace that causes crosstalk is termed the "Source" or "Aggressor" and the trace that is affected by the first is called the "Victim".

Mutual Inductance L_m will inject a voltage from a driven line onto any "victim" trace that is in close enough proximity to be encompassed by its magnetic field. L_m will inject a voltage noise onto the victim line proportional to the rate of change of current on the driver line. Since the induced current is proportional to the rate of change, mutual inductance becomes very significant in high-speed digital applications.

Mutual Capacitance

Mutual capacitance, C_m, is the coupling of two conductors via the electric fields. C_m will inject a current onto the victim line proportional to the rate of change in voltage on the driver line. These two factors become significant in high speed board design (fast edge rates = fast change of I and V).

Return Current

One of the absolutely fundamental truths in electronics is that current flows in a closed loop. On a PCB signals propagating down, traces must have a return path for the current to form this closed loop. In high-speed PCB board design the return current signal will be on the plane directly below the signal trace; this is the path of least inductance and results in the smallest current loop possible.

In high-speed designs, it is important that this current loop be kept as small as possible, for signal integrity and EMI (electromagnetic interference) considerations. A large loop will be susceptible to EMI and interference from other signals, as well as radiating EMI itself.

If any slots or holes exist in the ground plane underneath the signal trace, the return current

Figure 2: *Different signal distortions on transmission lines*

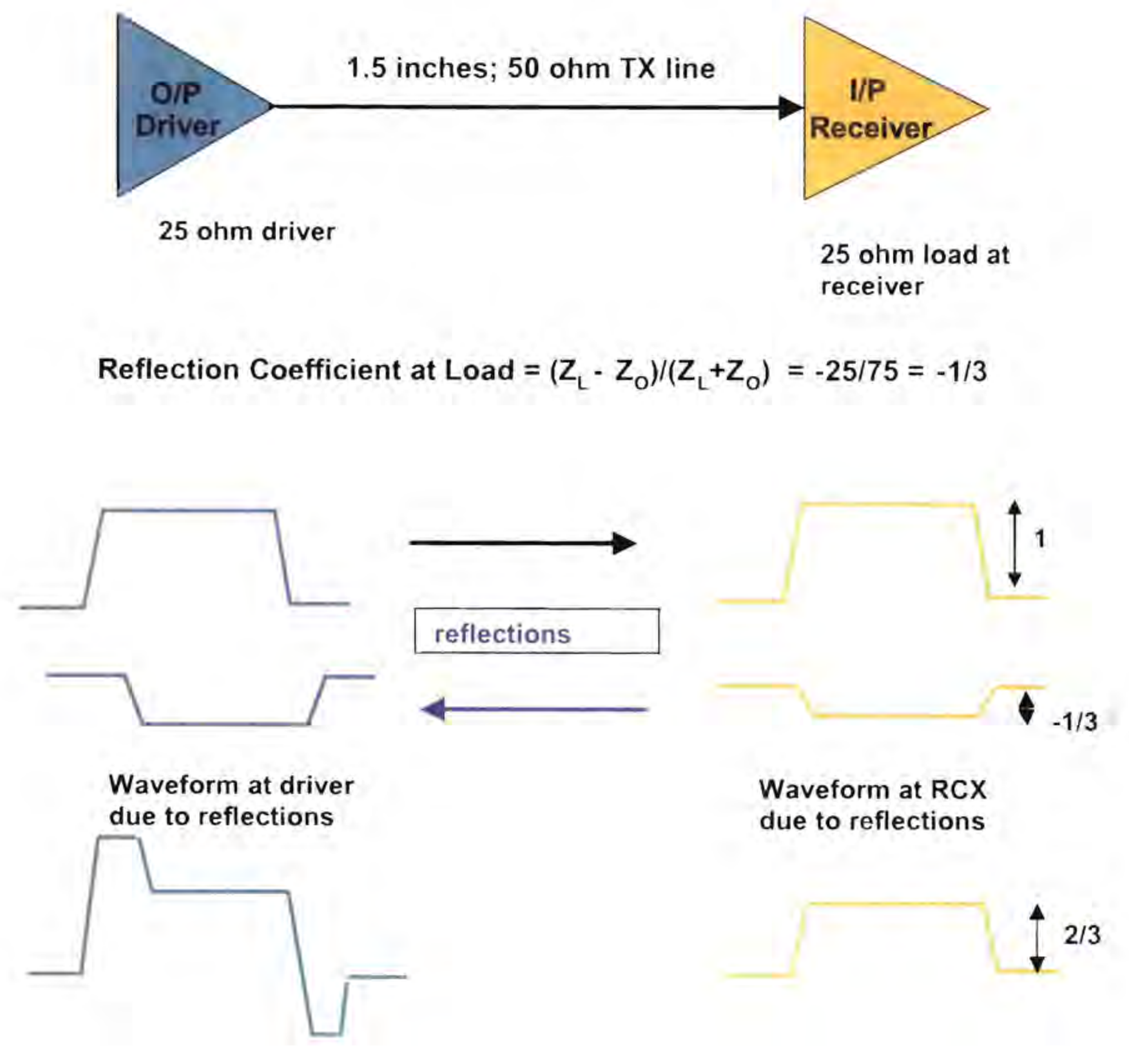


Figure 3: Reflections that can occur in a transmission line

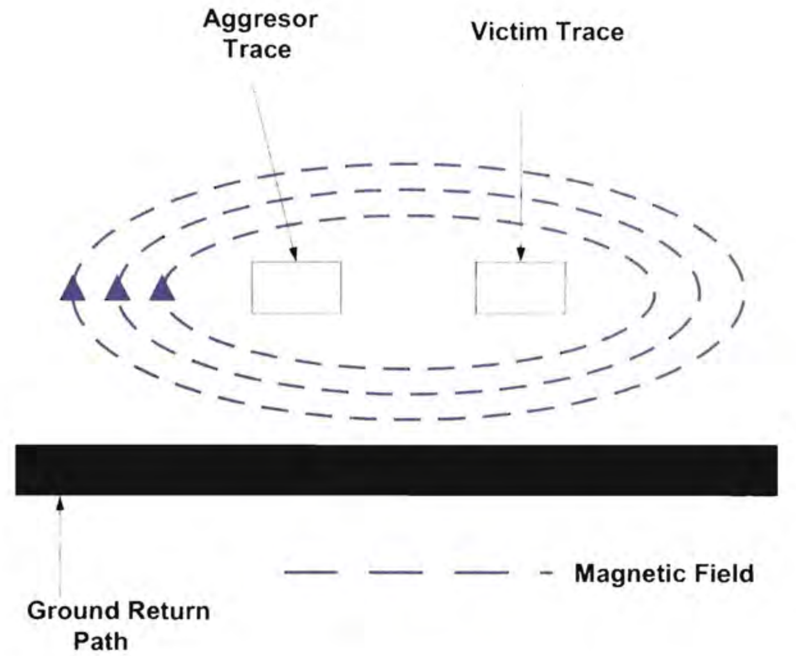
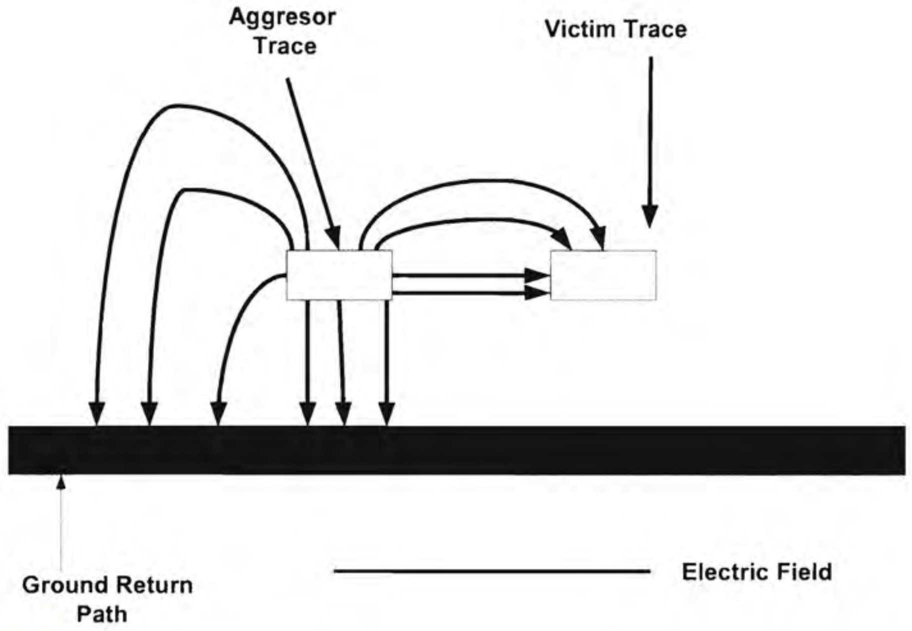


Figure 4: Interference caused by two adjacent transmission lines



must find a path around the hole, thus increasing the loop size and degrading signal quality and increasing EMI. This is why ground and power planes should be kept as solid as possible. Also, the current return path of signals that cross between routing layers that use different reference planes can result in the formation of large loops. This should be avoided as much as possible.

Every signal path has a return path. All signals must have a current return path; this will be the path of least inductance: the ground plane underneath the signal trace. Whenever there is voltage change, there is a corresponding current change in each section of the line and the current flows through the distributed capacitance back towards the source. When a signal is transmitted from an output driver to an input buffer, the forward current flows through the signal conductor and the

Figure 5: *The electric and magnetic fields of a transmission line*

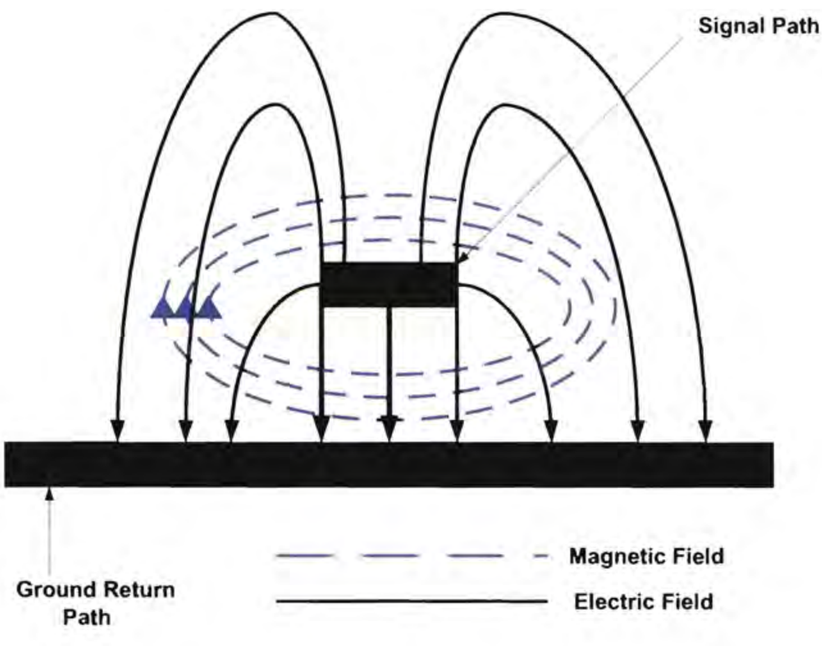
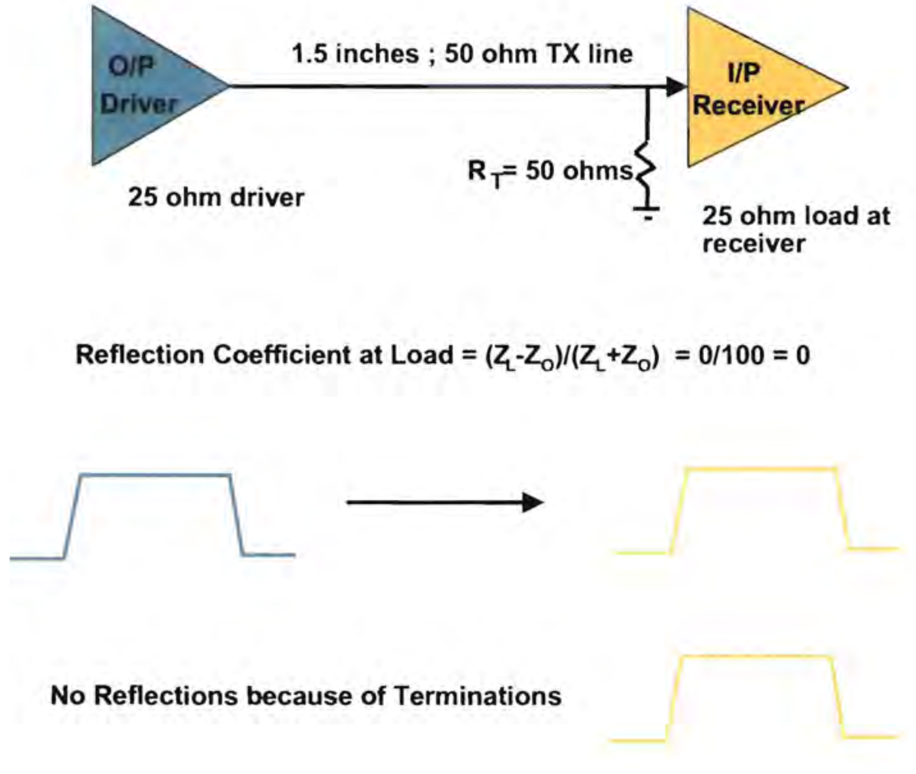


Figure 6: *Effect of termination on reflections in a transmission line*



return current flows through the reference plane. For high frequency signals, the return current is the path of least inductance. For good signal integrity at the receiver, the return current path should be directly above or below signal trace and should have a solid ground reference plane.

Reducing Signal Distortion

The following methods can be used to reduce the signal distortion and improve signal integrity.

Termination: Based on the discussion above regarding reflections, we saw that the energy gets reflected back because of impedance discontinuities at the receiver. In order to reduce or eliminate this reflection, one factor that can be taken into account is to absorb the energy before it is reflected. Terminations of a transmission line can be used to accomplish this. Energy can travel in either direction along a transmission line. Therefore, it may be necessary to terminate both ends of a transmission line to properly absorb any energy travelling on it.

Figure 5 shows the effect of termination on reflections in a transmission line.

There are different options available for terminating high-speed interfaces. Several of them are discussed below.

1) *Series or source termination*: In this method the termination resistor is connected in series with transmission line. It should be placed as close as possible to the source. The value of the source termination resistor depends upon the output impedance of the driver. Refer to **Figure 6** for series or source termination.

$$R_d + R_s = Z_0$$

Where Rd is the output driver impedance, R_s is the series termination resistor and Z_0 is the impedance of the transmission line.

In this termination method the reflected wave is absorbed while returning back to the source – one method if implementation is with an external resistor. Another

Figure 7: *Series or source termination*

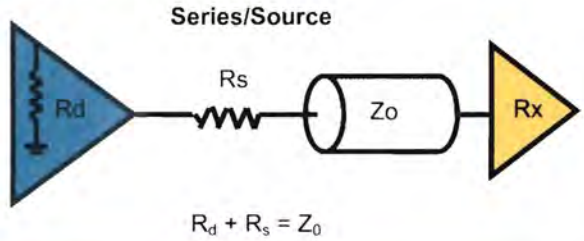


Figure 8: *End or parallel termination*

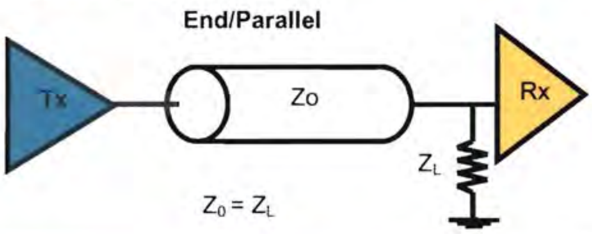


Figure 9: *Source termination in a multi-drop bus*

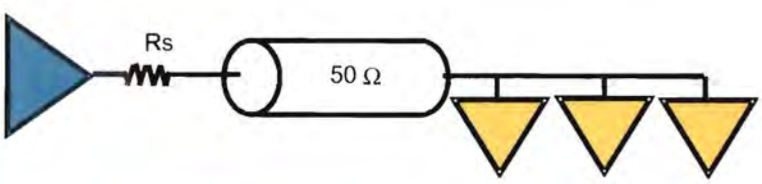


Figure 10: *End termination in a multi-drop bus*

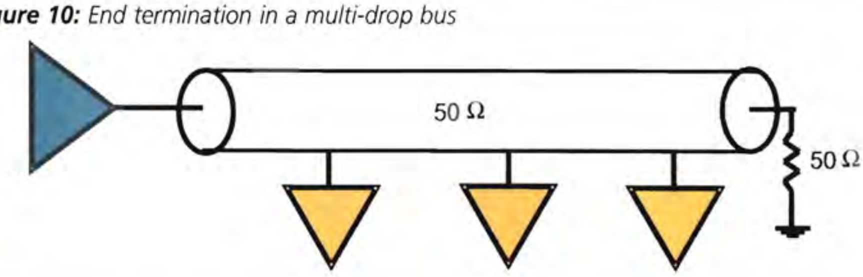


Figure 11: *Series termination in a bi-directional bus*

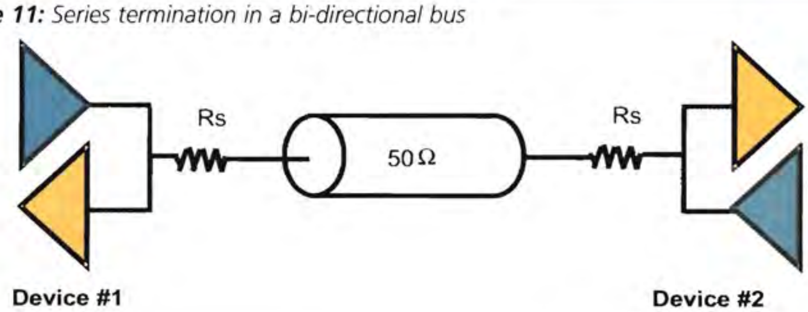
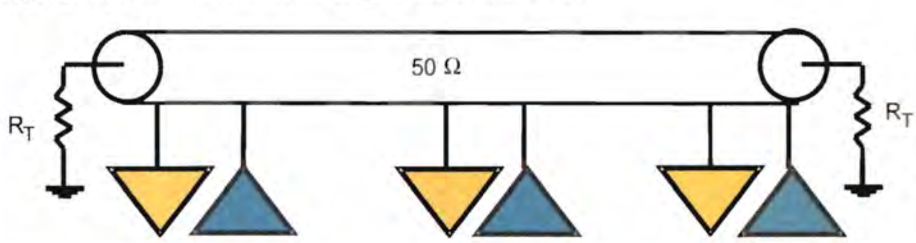


Figure 12: *Termination in multi-drop bi-directional buses*



method of implementing this kind of termination is to use the variable impedance option available in some high performance devices. In this method the impedance of the output driver can be varied through the drive strength of the driver through the value of the resistor tied to a specific pin of the device driving the signals. This eliminates the need for any external resistor thus saving board space. The advantage is that it cancels out reflections at the source and prevents high currents, but the disadvantage is that a voltage drop exists (for external series resistor) that causes problems with noise margins.

2) *End/parallel termination*: In this method the termination resistor is connected as a pull-down resistor at the end of the transmission line. The value of the termination resistor should match that of the transmission line. No reflections occur as the entire load is matched to the transmission line impedance. Refer to Figure 6 for end or parallel termination.

The advantage of this method is that the constant power consumption is eliminated. However, the disadvantage is that additional resistor at the load. Another advantage is that this method requires more board space.

3) *Special cases for termination:*

a. Multi-drop

b. Bi-directional

Multi-Drop Bus

For a multi-drop bus (transmission line driving more than one load), one of the following methodologies can be followed, depending on the loading conditions, to achieve best signal integrity.

If the loads are at the end of the transmission line then source termination would be the best option.

If loads are distributed along the line, end termination would be the best option. A termination resistor of 50Ω is desirable to avoid impedance mismatch.

Bi-Directional Bus

For bi-directional buses, the transmission lines need to be terminated in both directions to preserve the signal quality of the line. For point-to-point bi-directional buses, series termination would be the best option.

For multi-drop bi-directional buses, terminating the far ends of the line in both directions would be the best option.

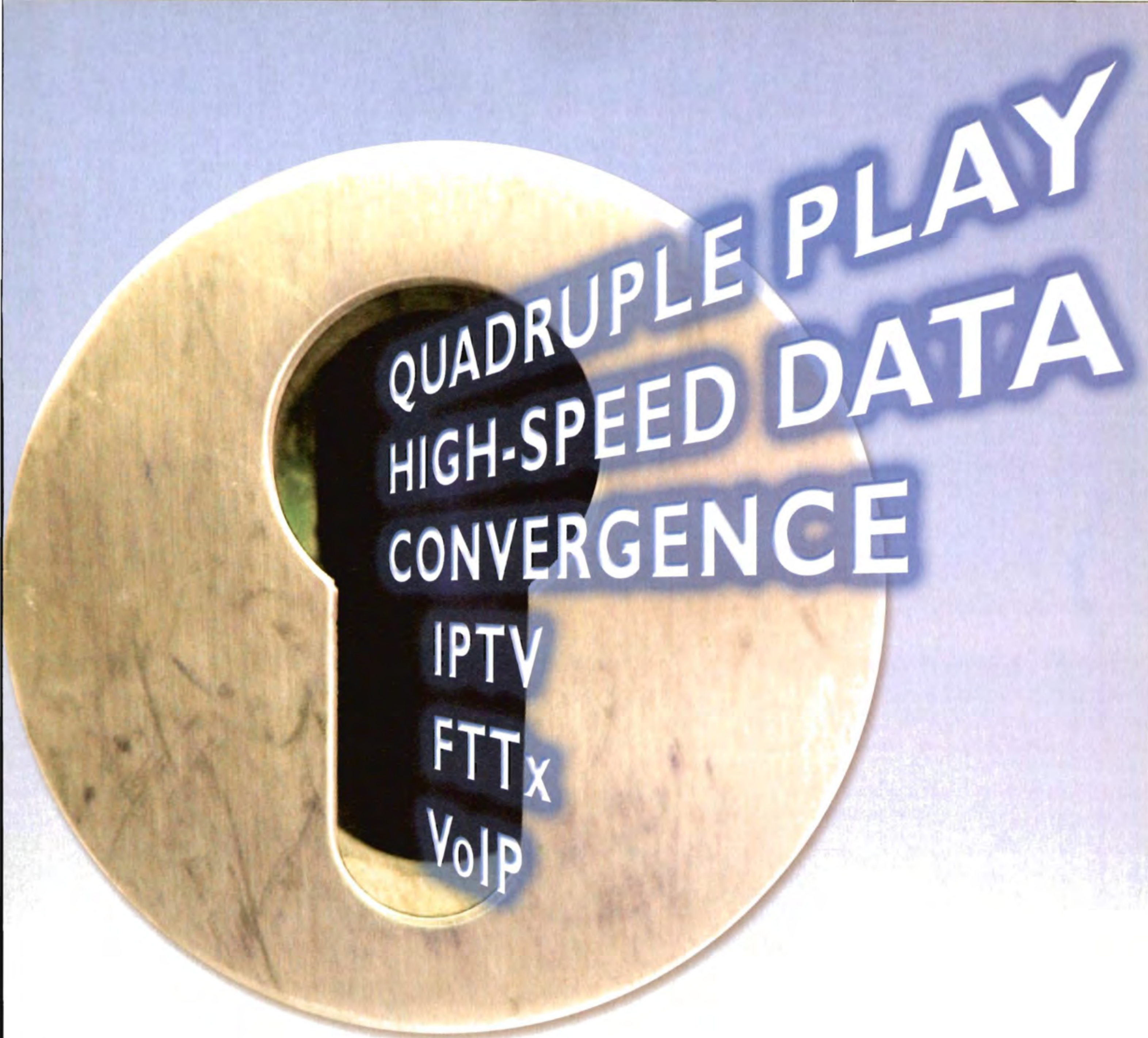
Conclusion

Signal integrity in high-speed memories is a major concern because system speeds and clock edge rates continue to increase. It is imperative that a system designer understands the issues related to signal propagation and quality.

REDUCING CROSSTALK IN PCBs

For reducing crosstalk in PCBs, the following design practices are recommended:

1. Increase the separation between the victim and the aggressor (best way). Crosstalk falls proportional to $1/D^2$ (D = Sep Distance).
2. Solid GND plane which provides a clean, unobstructed, least inductance path for the return current.
3. Adjacent signal layers not separated by reference planes – one layer orthogonal to another to reduce capacitive coupling between layers.
4. Lower laminate height (H) by moving the traces close to the plane.
5. Implementing stripline traces rather than microstrips. This is because coupling is a linear function of spacing in microstrip traces and approximately a square function of spacing in stripline structures. This separation alone accounts for a two or four-fold reduction in crosstalk. Hence, stripline has lower crosstalk compared to a microstrip.
6. Choice of slower edge rate devices provided speed requirements are not high enough.
7. Guard traces between signal traces. This will be a good option only if the guard trace is the primary current return path. A guard trace consists of a single grounded trace between source signal trace and the victim trace. The guard trace shields or guards the victim trace from the source trace.



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MOSFET-BASED HIGH-CURRENT DC POWER SUPPLY

I. HAKKI CAVDAR OF KARADENIZ TECHNICAL UNIVERSITY IN TRABZON, TURKEY, CREATES A HIGH-CURRENT DC POWER SUPPLY BASED ON POWER MOSFETS AND A STANDARD THREE TERMINAL VOLTAGE REGULATOR

Regulated DC-power supply design for high output currents is still a critical and difficult problem. The basic methods of increasing maximum output current of a 78xx standard three terminal regulator are: parallel-connected, multiple three-terminal regulators, 1A - 78xx devices [1], the use of an external bypass element such as BJT [2] and the use of an external bypass element such as P-channel power mosfet [3]. Parallel-connected multiple 78xx devices work well, but at high output currents, for example at 50A, fifty 78xx units should be used, which may not be the most economical and its size might be a problem.

The bypass BJT and 78xx is also a critical design, as the BJT is a current-controlled element, and the bypass current depends on the load resistance. This design may be used only for constant load resistance, i.e. constant output current. The output voltage cannot be regulated for various output currents.

Because the load resistance varies, the output current also changes and so does the DC-operating point of the BJT. In fact, a DC power supply must work for any large output current levels. Controlling the output current of a BJT is not easy. The first important parameter here is hFE, which can be between 50-100 for power BJT. As such, for large power outputs, the input base current must be controlled in small steps.

The power mosfet is another solution as a bypass element for the 78xx. Controlling a power mosfet is a lot easier as it is a voltage-controlled element. The output current can be controlled by the VGS voltage. The VGS controlling process is the important step in realising a high-current power supply that uses a bypass power mosfet and the 78xx. In literature you can already find a P-channel power mosfet design for a bypass 78xx device at 15A fixed output current [3]. This design works well with at 15A output load current level. It requires to use current sensing resistances with very low impedances – 10mΩ and 100mΩ – due to using a P-channel mosfet. On the variable loads (i.e. variable output current values), this design should be adapted to the given output current levels.

Design Of High Output Current Power Supply

This study aims to provide a general solution for a high current supply with realisable elements, for any output current. The configurations of the power mosfet and 78xx for P and N channels are shown in **Figure 1.** An N-channel mosfet may be selected as: 1) they are used more conventionally in high current applications, and 2) the ID = IS current is controlled by VGS voltage for both, so both need another secondary voltage source to contol VGS.

For a P-channel mosfet, VGS varies in the negative region, and for an N-channel mosfet VGS varies in the positive region. In Figure 1, for conventional

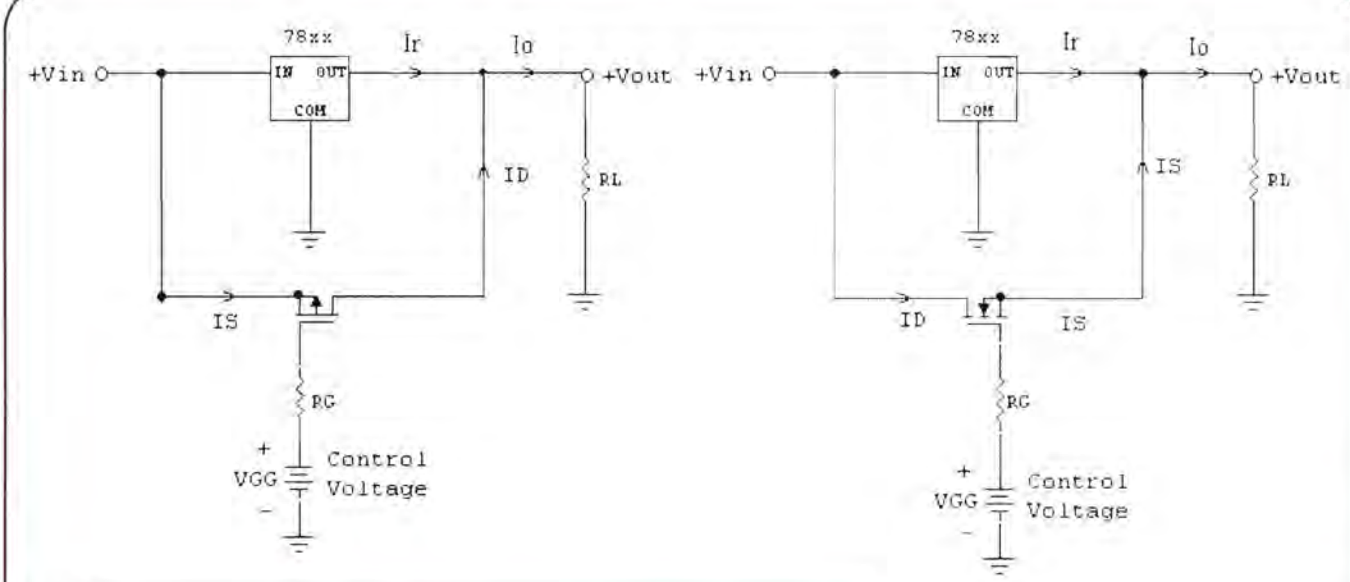


***Figure 1:** (a) P-channel mosfet and 78xx (b) N-channel mosfet and 78xx*

mosfets, VGS varies between 2V and 20V, and -2V and -20V for the N and P channel respectively. For enhancement mosfets, the threshold voltage is 2V. If we apply this data to the Figure 1 configurations, then:

$V_{GS} = V_{GG} - V_{in}$; where for a P-channel mosfet VGS should be negative
$V_{GS} = V_{GG} - V_{out}$; where for an N-channel mosfet VGS should be positive.

So, a P-channel mosfet needs a second bi-directional power supply due to a full control VGS voltage. On the other hand, here VGG must be applied to G or made common to the G and S terminals. If VGG applies between G and common, VGS is calculated by the equation above. Vin is not a regulated voltage, it changes and so does VGS. Note that ID may not be stable.

Another way for a P-channel mosfets is to apply VGG between the G and S terminals. This is also difficult, because in power supply design, working before regulation is not the more effective choice. In order to obtain the required VGG voltage, small resistances on the high current lines should be used. However, the N channel needs only positive power. Secondary power supply is more easily obtained (see the notes below). And for the N-channel VGG is applied between G and common, which is very suitable. Finaly, N-channel mosfets are more usable compared to P-channel mosfets.

Methods Of Generating Second Voltage Sources

1) *Using an independent, small size, second power source.*

   This is the best option and is relatively stable as the secod supply requires very little power. The required signalling and reference voltages are obtained from this supply, therefore this should be a highly regulated power supply. For designing the main high-current power supply at the 50A–100A level, second voltage source is not expensive.

2) *Using voltage multipliers from the main transformer.*

   A second power supply may be obtained from main transformer secondary coils using the second bridge diodes. After that, voltage multipliers may be used to improve the required VGG voltage level. Its only advantage over method 1 is that it does not need a second transformer. However, it does need many other components, such as diodes, capacitors etc.

3) *Using a large voltage transformer as a primary source.*

   In order to provide the second supply, secondary voltage of a primary transformer may be selected high for VGG. So, a required second voltage may be obtained using a small bridge diode and other elements. This method does not need a second transformer but, using a large secondary voltage at the main transformer causes large power loss. It also creates a heating problem and the power efficiency decreases. For example, for a 20A, 12V supply, VGG max must be 34V. To be controlled on a full scale, we need 34V transformer voltage at the primary source, so this means VDS = 24V and a loss of 480W. Equally, max input voltage is 30V, which is a limitation. If we use the 7812, we must use a 30V transformer, so we may control VGS max 18V, otherwise we may not be able to work at max ID currents.

4) *A second voltage may be obtained using a transformerless power supply with a small power.*

   There are many methods for this, but they need a good user-phase isolation, otherwise serious damage could be caused.

Figure 2 shows the block diagram of the mosfet and 78xx high current power supply. The critical

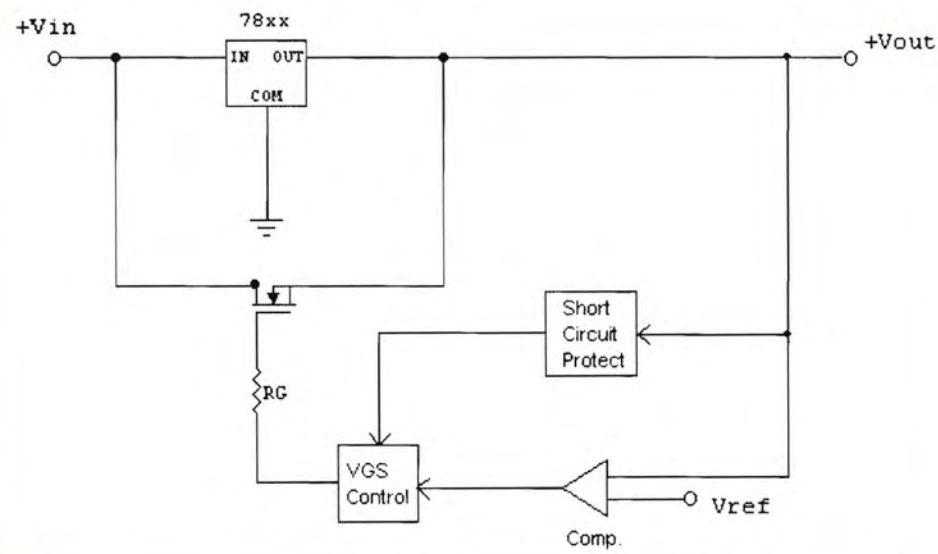


Figure 2: *Block diagram of high-current regulator with 78xx and N-channel mosfet*

point of this design is the VGG-controlled voltage method, as explained earlier. A voltage comparator uses a clean reference voltage with Vo as reference and the actual voltage as their inputs. At the output 1s and 0s are produced logically, and this data drives a transistor to enable or disable a charging or discharging of a capacitor. The capacitor voltage applies to the mosfet's gate and VGS is obtained. If the load changes, the output voltage drops at high output currents, but this is detected and VGS will increase so ID also increases and the output voltage will stablise rapidly. A short circuit protection system is added to the power supply. If VGS is zero, this will also be the cut-off region and, hence, no ID current. To do this, a second compa-rator may be used.

A second comparator uses two inputs: actual Vout and the a low voltage near zero. If Vo is zero, this means the output is a short circuit, and comparator 2 produces a 1. The VGG voltage capacitor is then discharged. Finally, VGS goes to zero and the mosfet channel is closed.

Figure 3 shows an application circuit for a given output voltage at 20A. This modular design is examined for different fixed output voltages at 20A using different 78xx such as 05, 08, 10, 12, 15 and 24. All of them will work satisfactorily. The best side of this design is that it is modular and in a compact form. Designing for any voltage and output current levels is easy and it only takes choosing a few additional components. On the other hand, IRFZ34 may be used because it is a conventional component and a cheaper N-channel mosfet. This may work up to 29A, but it could also be used up to 20A reasonably and safely.

All supplies for given output currents may be designed with the same mosfet using parallel connections for VGS. For example for 50A output current, three IRFZ34 or an equivalent may be used in parallel, or you can choose a 50A single mosfet. U3 and U4 are the LM311 voltage comparators: output voltage regulation and the short circuit protection respectively. Classical op-amps may be used instead of LM311, but LM311 offers good performance on the voltage comparison side and does not need a dual polarity power supply. C5 is the VGG charge and discharge capacitor, Q2 is the switching transistor, U2 is the second supply regulator. The other resistors and diodes are used to obtain the well-known biasing or voltage levels in the circuit. Here, an independent small size power supply is used as the second power source. T2, D5, U2, C3 and C4 are used on the second, small-size supply.

U3 is a voltage comparator. One of its inputs is connected to to the reference voltage, which is the same value as the output voltage, and it is obtained from U2. The other input is connected to the output of the regulator Vo.

U3 is used to adjust the gate voltage of Q1. The gate voltage of Q1 is equal to the voltage across C5. The voltage across C5 depends on Q2, whether it's in cut-off or saturation. If Q2 is at cut-off, C5 wants to charge via R1, so the gate voltage of Q1 increases. If Q2 is at saturation, C5 wants to discharge over R3 and Q2, C-E, so the gate voltage of Q1 decreases. U3 decides that the gate voltage should be increased or decreased by controlling the two U3 inputs.

The main aim of this regulator circuit is to provide a constant output voltage under variable loads, i.e. variable output currents. Therefore, at high output current levels, the drain current of the bypass element, the mosfet, should be controlled, because ID is approximately equal to the output current. If ID is controlled at the level of the required output current, the output voltage of the supply will be stable and constant at the designing point. While this supply operates at the constant output voltage and output current, if high current is required, U3 produces a logic 0, so Q2 cuts-off, the voltage across C5 increases via R1, hence the gate voltage of Q1 increases, ID increases and the output voltage increases up to the desired value.

This creates a constant output voltage and current. If lower output currents are required, while working with stable voltages and currents, U3 produces a logic 1 signal; Q2 saturates and the gate voltage decreases via R3 and Q2-CE. The process of charging and discharging of C5 is very fast as the time constant of C5 is only a few hundred miliseconds.

U4 is used in short circuit protection. If the output terminals are short-circuited, Vo drops rapidly to zero, U4 produces logic 1, Q2 goes to saturation and C5 fully discharges. The gate voltage of the mosfet will also be zero and Q1 goes to cut-off; ID = 0, only U1 will be active, but standard three-terminal regulators have short circuit protection system, so its output will be zero. Therefore, the important components T1, Q1, D1...D4 etc are protected against damage.

Conclusion

The design specifications and a selection of different output voltage and currents guide table are shown on **Table 1**. All of these have been tested in our lab. It is well known that three terminal voltage regulators produce some fixed output voltages such as 5V, 8V, 10V, 12V etc. If a power supply is needed outside any of these given values, the LM317 adjustable voltage regulator could be used.

The interesting point about this design is there's no need for a large capacitor at the output terminals; the large output capacitors should be used at conventional regulators in order to reduce the rms ripple voltage and correct the ripple factor due to variable loads. But, in this design, the ripple factor is close to 1 without the need for a large output capacitor due to a mosfet controlling the gate voltage and ID.

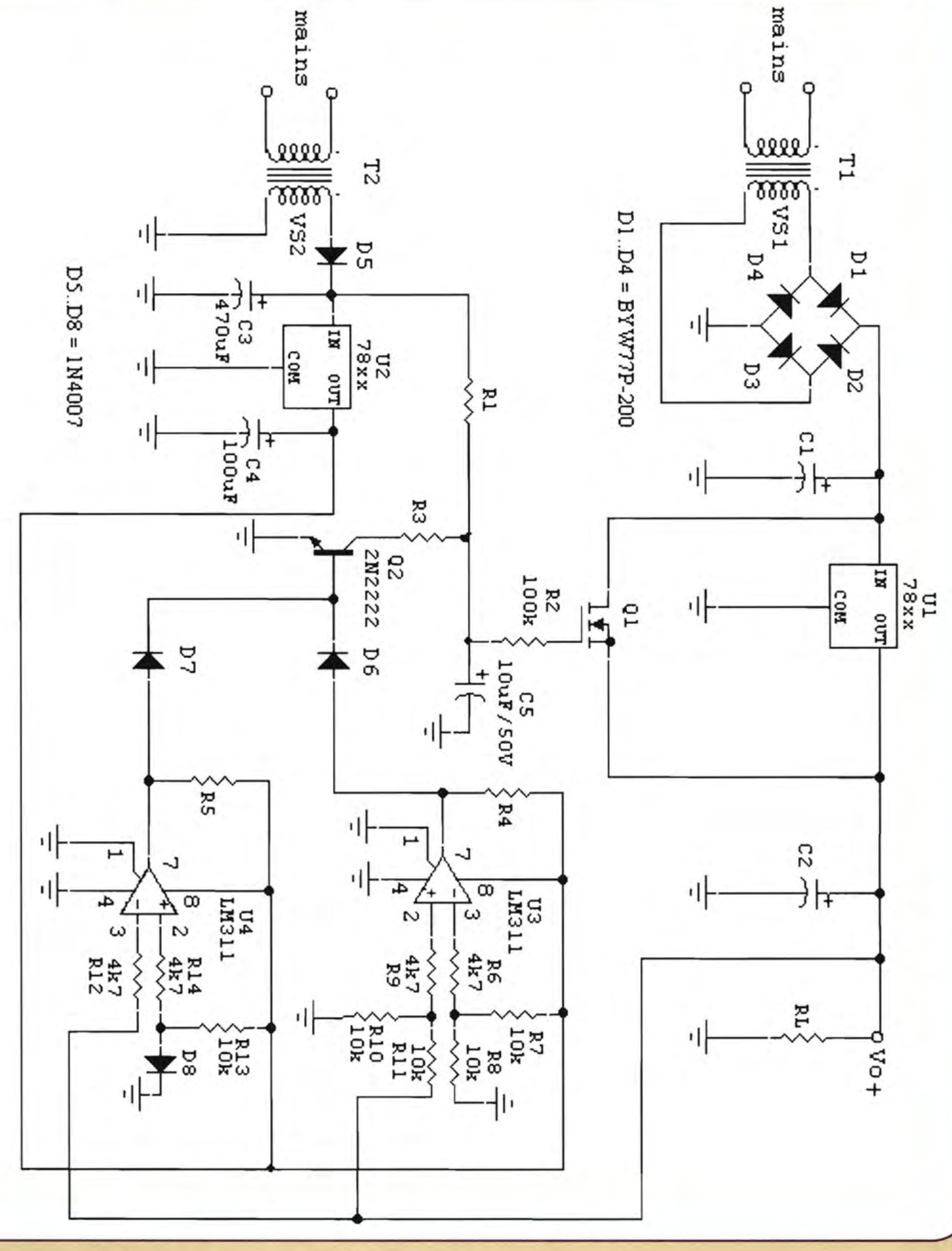
Other design suggestions include:

1) U1, Q1 and D1...D4 must be cooled down using suitable cooling platform, additionally or alternatively. Also, a small fan may be used.
2) U1, Q1 and D1...D4 should not be located on the PCB, they should be close to each other and the required connections should be made via cables. Used cables, especially carriers of high currents (mosfets S and D and the output cables) should be selected suitable for the current levels. During experimentation, when we used thin cables at the 20A output currents, we experienced voltage drops of between 0.5V and 1V over the cables, which affects the output voltage regulations.

Table 1: *Selection quide of the components for different output voltages at 20A max output current*

	5V	8V	10V	12V	15V	18V	24V
T1-Vs1 total power	10V 250 W	12V 300 W	15V 350W	18V 400 W	22V 500 W	25V 600 W	30V 750 W
T2-Vs2 total power	18V 2W	20V 2W	22V 2W	24V 2W	30V 2W	32V 3W	35V 3W
U1=U2	7805	7808	7810	7812	7815	7818	7824
Q1	IRFZ34	IRFZ34	IRFZ34	IRFZ34	IRFZ34	IRFZ34	IRFZ34
C1	22 mF 50V	22 mF 50 V	22 mF 50 V	22 mF 50V	22 mF 50V	22 mF 50V	22 mF 63V
C2	4700 µF 16V	4700 µF 16V	4700 µF 16V	4700 µF 25V	4700 µF 25V	4700 µF 25V	4700 µF 50V
R1	100K	120K	150K	180K	200K	200K	220K
R3	4,7K	5,6K	6,8K	8,2K	10K	12K	18K
R4=R5	10K	10K	12K	15K	18K	18K	22K

Figure 2: An application circuit of a modular power supply at standard output voltages for 0-20A output current



3) Over 20A, mosfets must be connected in parallel for every additional 20A. This connection is also well-known.
4) Vout output voltage sample for the comparators should be taken from the actual output point at the circuit board as soon as possible. This is necessary to prevent errors at the output voltage due to the drop of voltages at the cables.

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Precision Time Constant Measurement And Display

Time constant of any physical system is an important parameter in assessing its dynamic performance. In case of passive networks, although the time constant is evidently known for simple RC and RL networks, it is not directly available for complex RLC networks or distributed RLC networks such as transmission lines. Also, the time constant of transducers such as thermocouple is not readily available for analysis of its dynamic behaviour. Furthermore, in popular electromechanical devices like a DC motor, the time constant is to be determined experimentally. This article describes an experimental method of determining precisely the time constant and displaying it in decimal form.

The time constant of a distributed passive network could be estimated based on the basic principle relied in simple RL or RC network. Taking RC network as a model for determining the time constant, there are two possibilities (as shown in **Figure 1**), also known as a low pass circuit (Figure 1a) and a high pass circuit (Figure 1b).

The time constant 'τ' for both circuits is the same (product RC) but the transient responses are different. The experimental determination of the time constant from the step response should be adjusted with the circuit for the two categories. The timing diagram showing the step response of these two circuits is given in **Figure 2**.

In the case of a low pass circuit, the time constant is the time taken for the response to reach 63.21% $(1 - e^{-1})$ of the steady state output. This duration is to be measured by comparing the response at 63.21% level. On the other hand, for the high pass circuit, the response starts with maximum at the beginning and falls to zero level exponentially. The time constant is the time taken by the response to reduce by 63.21% from the maximum. Therefore, the marking level for the comparator in this case is 36.79% (e^{-1}).

Figure 3 shows the schematic of the experimental circuit which identifies the low pass or high pass nature of the circuit under test, establishes automatically the

Figure 1a

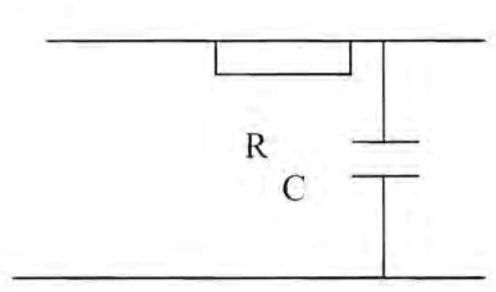


Figure 1b

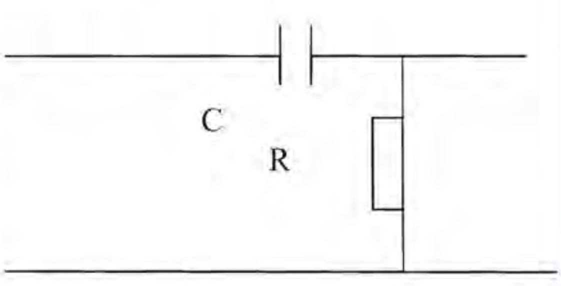


Figure 2a

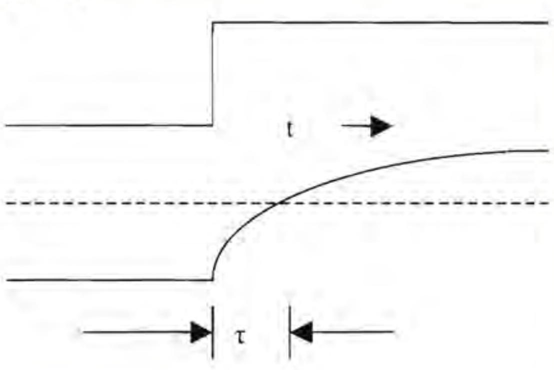


Figure 2b

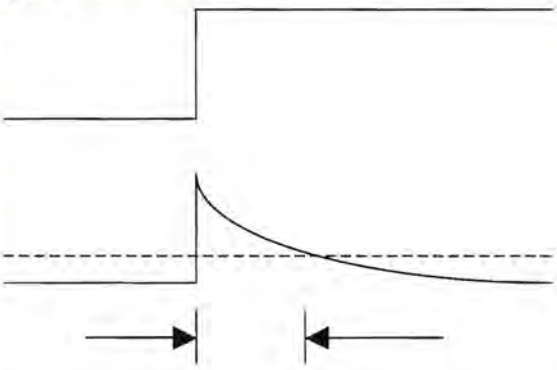
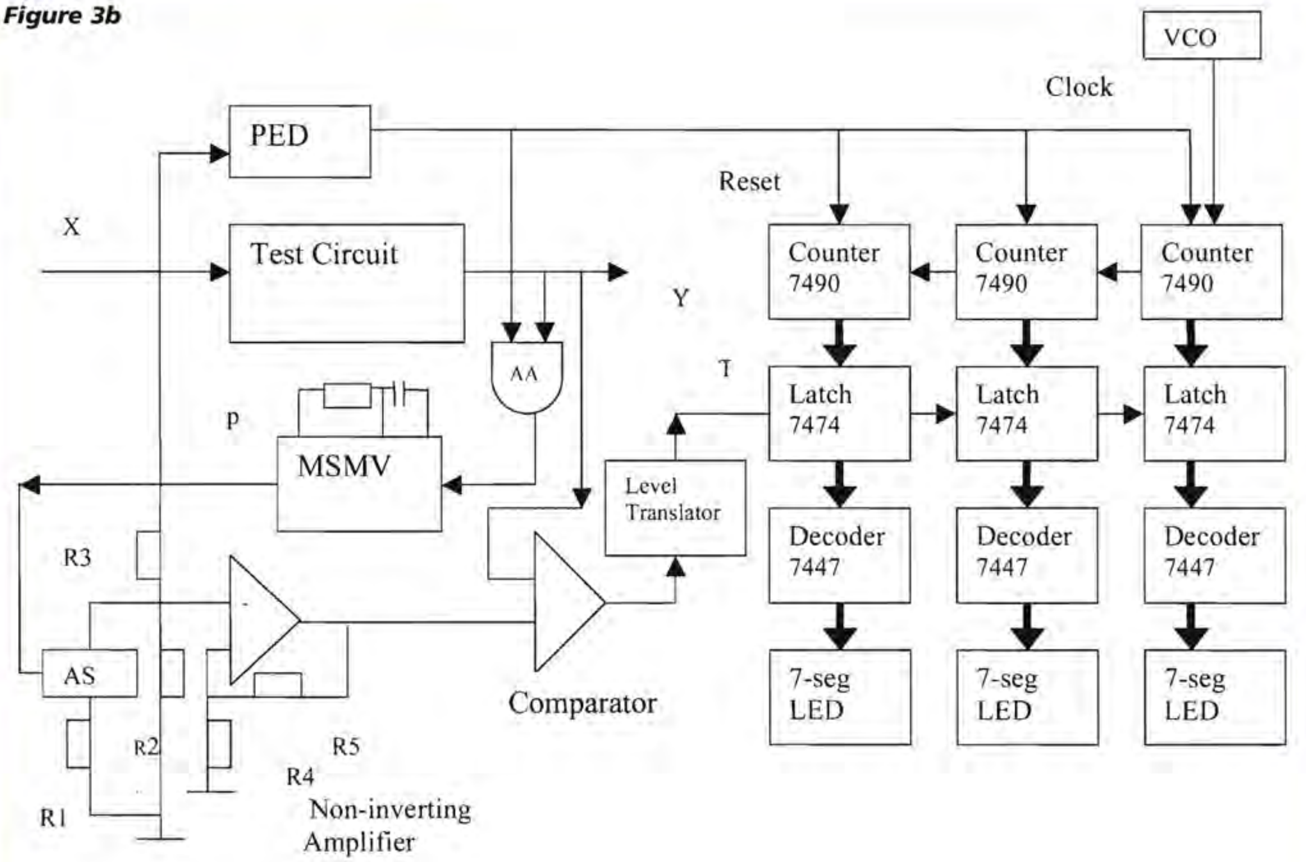


Figure 3b



reference levels, measures the time duration which takes to reach the marking level and displays the period in decimal form in LEDs. A counter stage comprising a chain of three BCD counters (7490) counts the clock for a period starting from the step input and the marking instant in the response. At the marking instant the counter data is latched (7474) to the BCD to 7-segment decoders (7447) which, in turn, displays the decimal data in the 7-segment LEDs (FND507). The comparator responsible for producing the trigger input to the latch has two inputs: one from the response of the circuit under test and another as the reference input. The reference input to comparator is to be set automatically as 0.6321 times the step magnitude, or 0.3679 times of the step magnitude, depending upon the nature of the circuit used for the test.

The testing starts with applying a 5V step input indicated as X to the testing circuit. The Positive Edge Detector (PED) finds the starting edge and resets the counter stage to start the counting. PED also triggers a Monostable Multivibrator (MSMV, 74121) in the case of the high pass circuit being used as a testing circuit, where the response Y being high opens the AND gate (AA). Triggering MSMV doesn't happen for the low pass circuit, where the response Y is low.

The reference input to the comparator is derived from X through a potential divider connected to a non-inverting gain amplifier. The potential divider formed by R3 and R2 develops the 0.6321*X in the case of a low pass circuit test. In the case of a high pass test, MSMV is triggered which, in turn, switches a resistance R1 by the analogue switch AS, which becomes in parallel with R2 and reduces the reference to the comparator as 0.3679*X.

The reference voltage obtained for low pass case is:

Figure 4

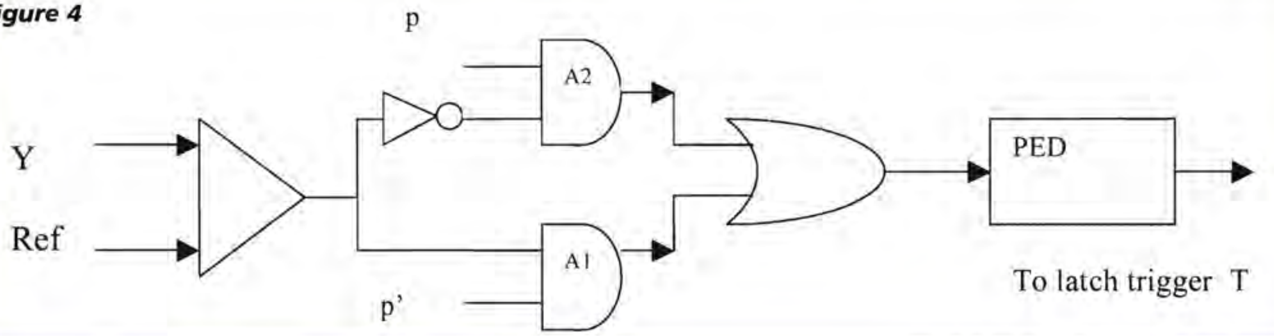


Figure 5

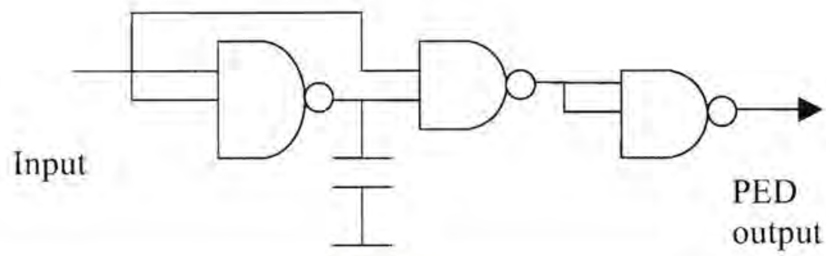
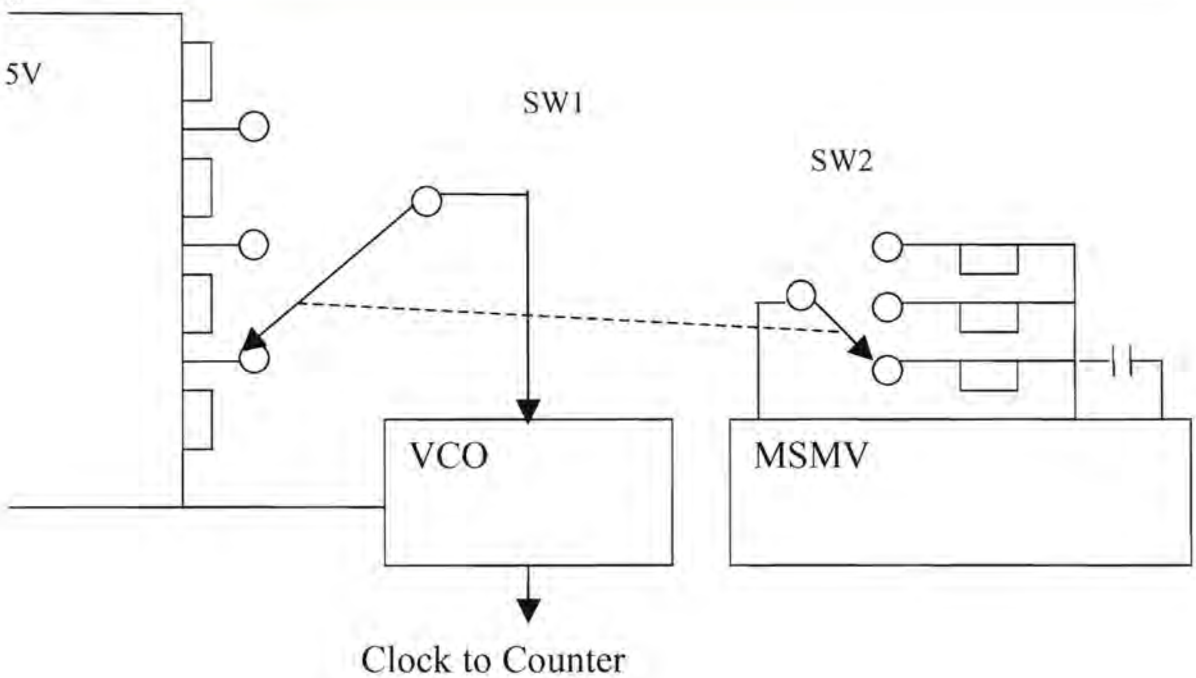


Figure 6



Vrl = 0.6321*X = X (R2/(R3+R2)) (1)

When R1 is switched on, the reference for high pass is obtained and is given as:

Vrh = 0.3679*X = X*(R1*R2/ (R1R2+R2*R3+R3*R1)) (2)

The gain of non-inverting amplifier is = (1 + R5/R4) (3)

By setting R5 as 0Ω its gain turns out to be +1. (4)

By choosing a value for the resistance R2 or R3, the other can be obtained from **Equation 1**.
By using these two values, R1 can be obtained from **Equation 2**.
Typical values obtained are R2 = 10K, R3=5.82K, R1= 5.1227K, R5=0Ω and R4 = 10K.

When the test circuit is a low pass circuit, the comparator output is initially low and goes high while marking. On the other hand, when a high pass circuit is used as a test circuit, the comparator output is initially high and goes low while marking. A level translator logic shown in **Figure 4** is used to obtain the trigger signal for the latches.

When low pass circuit is used Y is 0 and MSMV is not triggered giving 0 as p. When Y reaches 0.628*X comparator output becomes 1, making the OR gate output as 1. PED gets the edge for the latches. In a similar way, it works for a high pass circuit also.

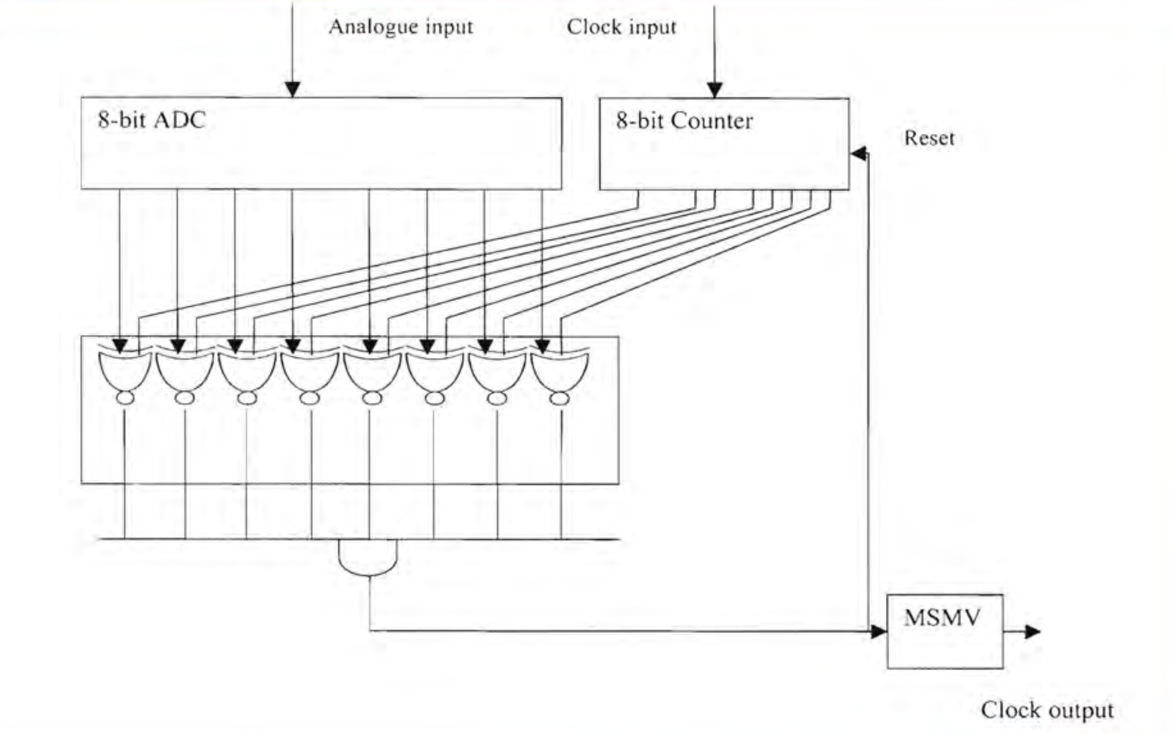
The PED is realised using NAND gates and a small capacitor as shown in **Figure 5.**

Time constant measurement range and its setting

Although we can have a wide range of measurement with the present circuit, we used three ranges: 1ms, 100ms and 10s. The user can manually select any one range into operation. **Figure 6** shows the time constant range selection circuit. By operating the switch SW1 the user can select one of the three voltages to the VCO generating clock to the counter stage. As the MSMV duration used in Figure 3 should be adapted to the measurement time, another switch SW2 ganged to SW1 selects the corresponding resistance to the MSMV for the desired duration.

The circuit of VCO for this application is shown in **Figure 7**. The analogue input chosen by the user is given to an 8-bit ADC generating appropriate digital word. The clock input is given to an 8-bit binary counter (2 x 7493) and when the counter data word reaches the ADC word, the AND gate output goes high resetting the counter. At this instant an MSMV is triggered to produce an extended pulse. The time difference between the successive pulses in the train produced by MSMV

Figure 7



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depends on the analogue value given to the ADC. Thus, when the analogue input is low resetting this occurs quickly, creating a high clock frequency output.

Time constant of a transducer

Any transducer capable of generating electrical voltage proportional to physical parameter could be tested with the above circuit; for example, a tempe-rature transducer – say a thermistor, and check out the steps involved in the measurement. An instrumentation amplifier connected to the thermistor has gain and offset arrangement facilities. The gain and offset are adjusted such that it gives 0V for room temperature and 5V for a temperature of, say, 95ºC. The appropriate time constant range is chosen into operation. The water bath is heated to the reference temperature of 95ºC and is ready for making measu-rement. Although the test circuit is missing, the step input X is applied to the rest of the circuit. Simultaneously, at the instant of step edge the transducer is dipped into 95ºC bath and this should be made synchronously. As the test circuit is absent, the output Y needed in the circuit is provided by the transducer amplifier. The circuit works and displays the time constant.

Time constant of a 5V DC motor

A 5V DC motor is chosen as an example, as it doesn't need an extension circuit for measurement. Other motors need additional adjustments. The motor needs to be connected with a tacho generator which would produce a voltage of 5V at rated RPM obtained for a 5V DC input to the motor. It is to be noted that when the RPM is low, the tacho generator output will also be low accordingly. The time constant of the motor is the time it takes to reach 0.6321 of the rated RPM for a step input of 5V applied to the motor.

The test circuit now is the motor with a tacho genera-tor and the output Y is taken from the tacho generator. Assuming all of the other elements are the same, the time constant of the motor is measured and displayed.

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Special focus: China RoHS

Now that RoHS is law (as of 1st of July this year), there are more questions than ever about how to cope with it. Recent research showed that the UK wasn't prepared for the deadline. Only 12% of design engineers, buyers and MRO engineers were fully compliant in readiness, ahead of RoHS officially coming into force. Whilst 37% of respondents revealed that they were "close to becoming compliant", a further 28% confessed that they had only just "started to become compliant".

There's still clearly a lot that needs to be done by the design engineering community but the main thing for engineers to realise is that they aren't alone in their quest to become compliant. Wide ranges of support services exist to help people along the way, such as those on offer at www.rohs.info. The fact that the deadline has passed means that it is even more important to access the help that exists.

The research – which was conducted amongst 263 UK design engineers, buyers and MRO engineers – shows that distributors are playing a vital role in ensuring compliance is achieved. Around 46% of those surveyed had chosen to approach a distributor for reliable RoHS support, followed by 22% who preferred to directly approach the manufacturer. Interestingly, only 9% have been relying on the government for RoHS support.

By its nature, online support is the fastest way to find out about the latest RoHS complaint products. Signing up to automatic email notification or online 'Bill of Materials' conversion services are effective ways to get new part numbers for old non-compliant components and upgrade to the latest RoHS offerings. But being able to speak to experts is also proving key for engineers who have achieved compliance.

Whilst 53% of respondents from the research considered online technical help and support services to be either "extremely" or "very" important, 39% also considered telephone technical help and support services to be "extremely/very important". There are still many grey areas around the new legislation that people are unsure about – exemptions and due diligence are just two of the 'hot potatoes'. Being able to access expert opinion over the coming months on these issues will be hugely important as the real effects of RoHS start to take place.

There are still many questions that need answering about the scope of the legislation and it will be essential to keep on top of the products that are under review for exemption. A recent example of this is semiconductor evaluation boards. Distributors and manufacturers alike believed these to be out of scope but the National Weights and Measures Laboratory, the body responsible for policing RoHS, has decided they're in.

It often isn't clear if a product is within the scope of RoHS or not. The situation for many types of industrial product will depend on how they are used. Equipment that is not dependent on electricity is also excluded such as gas boilers and petrol lawnmowers.

Q: What substances does China RoHS restrict?

A: As in EU RoHS, China RoHS restricts the levels of lead, cadmium, mercury, hexavalent chromium, PBB and PBDE, with the possibility of others being added. Deca-BDE is excluded.

Q: What are the main requirements of China RoHS and how do these compare to EU RoHS?

A: The EU RoHS directive states that the six restricted substances (as above) must not be present in homogeneous materials at above the maximum concentration values, unless covered by an exemption. China also adheres to this and all Electronic Information Products (EIPs) must be marked to indicate whether any of the six substances are present or not.

Q: I know that the EU does not require products to be marked as RoHS compliant, is this the same in China?

A: China RoHS will have pollution control marks, which will indicate recyclability. There will be one mark, symbol one (green preferred) for when no RoHS substances are present, and another, symbol two (orange preferred) for when a RoHS substance is present in at least one material. In the case of the latter, a number is required in the centre of the logo indicating the Environmentally Friendly Use Period. This depicts the anticipated number of years before any of the hazardous substances are likely to leak out of the product, potentially causing harm to health and the environment. Where symbol two is used a disclosure table is also required showing which substances are present and where they are located in the product.

Q: Does China have an equivalent body to the UK's National Weights and Measures?

A: While the Ministry of Information Industry is in overall charge of the management and co-ordination of China RoHS, other authorities will cover areas such as certification and testing, inspection and compliance and inspection of imports.

Q: What are the maximum concentration levels permitted of the restricted substances?

A: Concentrations of Pb, Hg, Cr (6), PBB or PBDE are > 0.1 % and > 0.01 % of Cd by weight in homogeneous materials. China RoHS also takes into account metal coatings as well as small products regarded as single homogeneous materials.

Q: What are the rules for obtaining exemptions to China RoHS?

A: 'The Catalogue' of priority products, when published, will highlight any exemptions as well as the implementation date for compliance. It will also state which substances are 'banned' by product and could include some not currently covered in EU RoHS.

Q: What is China's RoHS stance on compliance of non-electrical products?

A: Unlike EU RoHS, where products are excluded if the finished product sold to the end user does not depend on electricity, all products are included if listed as EIPs, including CDs and DVDs. China RoHS also covers products such as batteries, medical, test equipment and components that are not currently within scope of EU RoHS.

Gary Nevison is chairman of the AFDEC RoHS team, board director at Electronics Yorkshire and head of product market strategy at Farnell InOne. As such he is our industry expert who will try and answer any questions that you might have relating to the issues of RoHS and WEEE. Your questions will be published together with Gary's answers in the following issues of Electronics World. Please email your questions to EWeditor@nexusmedia.com, marking them as RoHS or WEEE.

Book Review

Electric Relays - Principles and Applications
Vladimir Gurevich
Taylor & Francis

This massive book is a sort of Encyclopaedia of relays and is number 130 in a vast series of technical reference books in the Electrical and Computer Engineering series from Ohio State University. The author is obviously a relay expert and, from the hints we glean from the text, his life is a story in itself.

He inherited his passion for relay technology from his father, who appears to have been an engineer in the heavy power industry of the former USSR. At some point, the family must have emigrated to Israel, and Vladimir (now 50) has become part of the power generation industry there. His rather grand claim to have founded a new branch of engineering, in high-voltage relays, must have some foundation, because he is now published internationally and has 116 patents to his name, some dating from his early 20s.

THE AUTHOR IS OBVIOUSLY A RELAY EXPERT AND, FROM THE HINTS WE GLEAN FROM THE TEXT, HIS LIFE IS A STORY IN ITSELF

The Russian origins of this text are clear throughout; it is extremely thorough and the 1300 illustrations are clear and well annotated. However, a large proportion of the relays shown as examples of their type are Russian in origin and have a touch of, sometimes eccentric, obscurity about them. The author has retained a fond affection for Soviet technology, which comes over as a sort of golden age of relay development. The translation improves as the book progresses, implying that some of the earlier material has been in preparation for many years. There are some glorious phrases at times: where we might say that two points were in intimate contact, Vladimir's relay contacts "strongly snuggle up to each other". And it took me a while to realise that "technological diversity" is, in fact, Russian for "manufacturing tolerances" – an interesting slant on the former USSR's no-blame culture in its leading industries. For all this, however, the book remains very readable and quite fascinating in the sheer expertise which the author has of the subject.

Chapter 1 is a brief history of relays – I had no idea that the name derives directly from the post-horse relay stations of the Wild West, but it makes sense. The author throughout the book emphasises the historical development of relay technology and does it very well, giving full credit to all the various inventors in many countries over the years.

Chapters 2 to 4 cover the magnetic and contact systems available across the board and the external design factors important in manufacture and use. The book then moves on in chapters 5 to 9 to detail the various different functions and styles available, as we ordinary engineers might meet them: reed relays, high-voltage relays, electronic, time and thermal relays. The coverage is excellent.

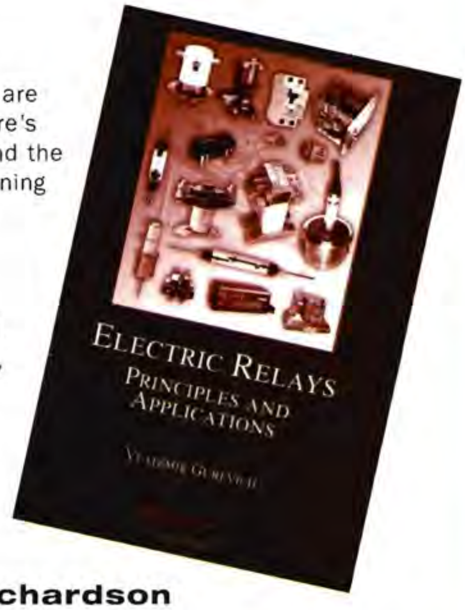
It is in chapters 10 to 14 that the author really comes into his own and his passion for the subject is revealed in his detailed knowledge of power distribution engineering, which is where he has patented many of his designs. Here we learn about protective relays, power and power directional relays, differential and distance relays, and relays to control mains supply frequency. Some of these devices are the size of a small building and the book's very clear description of their working principles is impressive. They are hugely complex, and the power directional devices and the distance relays, in particular, demand considerable concentration to understand their function properly.

Chapter 16 tidies up with a brief description of fourteen less familiar types of relay otherwise not covered – things like the weird and wonderful magneto-hydro-dynamic relay and the Buchholz gas-detection relays. There's also a neat circuit for an earth-leakage trip that is useful for anyone who can't get an off-the-shelf solution.

Chapter 14 is an anomaly. It is headed "*Microprocessor Based Relays: Prospects and Challenges*", but in fact it is a thorough-going condemnation of the intrusion of computers into the field of relays. At first sight, this looks like simply the resentment of a man who spent his life patenting some pretty sophisticated and expensive devices and who hates to see all his hard work suddenly rendered obsolete by some anorak with a keyboard on the grounds of economy. But the author presents his case well. Certainly, a lot of low-level switching jobs can be done by a PIC chip and some bigger tasks tackled by an embedded industrial PC. But as the voltages and the currents rise – and in power generation we are talking about hundreds of KV and thousands of amps – then the computer actually produces a slower response than a dedi-cated relay. This is partly because it needs an interface relay anyway, but mainly because the software can detect many types of fault condition only by comparison with previous readings and this takes at least two passes round the loop. The tens of milliseconds difference could be very costly indeed in a vital high-power circuit-breaker. The author also makes the valid point that some fault conditions may not arise for 30 years, and there are still in service, in power systems all over the world, many vital relays that have not once been tripped but still remain fully serviceable. This long-term stability is an area in which computerised systems are as yet unproven – 99.9% up-time simply isn't good enough.

All in all, this book is a technical tour-de-force. It is intended as a design aid for engineers and the strong emphasis on working conditions, materials and reliability make it useful in this capacity. But for most of us who aren't in power engineering and for whom the manufacturer's data sheet is entirely adequate, this is still a nice book to own: the history and the sheer technical detail are fascinating; there's a lot to learn and the style is entertaining and, at times, surpri-singly passionate.

You won't manage to read it at one sitting, but you will certainly keep returning to it for its wealth of knowledge.



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Agilent (HP) 4192A L/F Impedance Analyser (13MHz)	£3500
Agilent (HP) 4193A Vector Impedance Meter	£2750
Agilent (HP) 4274A LCR Meter	£1750
Agilent (HP) 4275A LCR Meter	£2750
Agilent (HP) 4276A LCR Meter	£1400
Agilent (HP) 4278A Capacitance Meter (1KHz / 1MHz)	£2500
Agilent (HP) 5342A Frequency Counter (18GHz)	£850
Agilent (HP) 5351B Frequency Counter (26.5GHz)	£2250
Agilent (HP) 5352B Frequency Counter (40GHz)	£3950
Agilent (HP) 53310A Mod. Domain An (opt 1/31)	£2750
Agilent (HP) 54600A / B 100 MHz Scopes from	£700
Agilent (HP) 54810A Infinium Scope 500MHz	£2995
Agilent (HP) 8116A Function Gen. (50MHz)	£1500
Agilent (HP) 8349B (2- 20GHz) Amplifier	£1750
Agilent (HP) 8350B Mainframe sweeper (plug-ins avail)	£250
Agilent (HP) 85024A High Frequency Probe	£1000
Agilent (HP) 8594E Spec. An. (2.9GHz) opt 41,101,105,130)	£3995
Agilent (HP) 8596E Spec. An. (12.8 GHz) opt various	£6500
Agilent (HP) 89410A Vector Sig. An. Dc to 10MHz	£7500
Agilent (HP) 89440A Vector Signal Analyser 2MHz – 1.8GHz	£7750
Agilent (HP) 33120A Function/Arbitrary Waveform Generator 15MHz	£850
Agilent (HP) 53131A Frequency Counter	£750
Agilent (HP) 53181A Frequency Counter	£750
Agilent (HP) 4284A Precison LCR Meter	£5750
Agilent (HP) 6031A Power Supply (20V – 120A)	£1250
Agilent (HP) 6032A Power Supply (60V – 50A)	£2000
Agilent (HP) 6671A Power Supply (8V – 200A)	£1350
Agilent (HP) E4411A Spectrum Analyser (9kHz – 1.5GHz)	£2995
Agilent (HP) 8924C CDMA Mobile Station Test Set	£3000
Agilent (HP) E8285C CDMA Mobile Station Test Set	£3000
Agilent (HP) 54520A 500MHz 2 Channel Oscilloscope	£1000
Agilent (HP) 54645D 100MHz Mixed Signal Oscilloscope	£3000
Agilent (HP) 8713B 300kHz – 3GHz Network Analyser	£4500
Agilent (HP) 8566B 100Hz – 22GHz High Performance Spec. An.	£7000
Agilent (HP) 8592B 9kHz – 22GHz Spectrum Analyser	£6250
Amplifier Research 10W1000B Power Amplifier (1 GHz)	£4700
Anritsu ML 2438A Power Meter	£1400
Rohde & Schwarz SMY01 9kHz – 1040 MHz Signal Generator	£1750
Rohde & Schwarz CMD 57 Digital Radio Comms Test Set	£4250
Rohde & Schwarz XSRM Rubidium Frequency Standard	£3750
Rohde & Schwarz CMD 80 Digital Radio Comms Test Set	£3500
R&S SMIQ-03B Vector Sig. Gen. (3 GHz)	£7000
R&S SMG (0.1 – 1 GHz) Sig. Gen.	£1750
Tektronix THS 720A 100MHz 2 Channel Hand-held Oscilloscope	£1250
W&G PFJ 8 Error & Jitter Test Set	£4500
IFR (Marconi) 2051 10kHz-2.7GHz) Sig. Gen.	£5000
Wayne Kerr AP 6050A Power Supply (60V – 50A)	£1850
Wayne Kerr AP 400-5 Power Supply (400V – 5A)	£1300
Wayne Kerr 3260A+3265A Precision Mag. An. with Bias Unit	£5500
Wayne Kerr 3245 Precision Ind. Analyser	£1750
Wayne Kerr 6425 Precison Component Analyser	£2000
Wavetek 9100 Universal Calibrator (Opts 100 / 250)	£9000
Various other calibrators in stock. Call for stock / prices	

8-pin FLASH PICmicro Microcontrollers

Microchip continues to provide innovative products that are smaller, faster, easier to use and more reliable. The Flash-based PICmicro microcontrollers (MCU) are used in a wide range of everyday products from smoke detectors to industrial, automotive and medical products. The PIC12F/16F family of devices with on-chip voltage comparators merge all the advantages of the PICmicro MCU architecture and the flexibility of Flash program memory with the mixed signal nature of a voltage comparator. Together they form a low-cost hybrid digital/analogue building block with the power and flexibility to work in an analogue world. The flexibility of Flash memory and a comprehensive development tool suite, including a low cost In-Circuit Debugger, In-Circuit Serial Programming (ICSP) and MPLAB ICE 2000 emulation, make these devices ideal for just about any embedded control application. This series of Tips 'n' Tricks can be applied to a variety of applications to help make the most of discrete voltage comparators or microcontrollers with on-chip voltage comparators.

TiP 1: LOGIC – INVERTER

When designing embedded control applications, there is often the need for an external gate. Using the comparator, several simple gates can be implemented. This tip shows the use of the comparator as an inverter.

The non-inverting input is biased to the centre of the input voltage range, typically VDD/2. The inverting input is then used for the circuit input. When the input is below VDD/2, the output is high. When the input is above VDD/2, then the output is low.

Values for R1 and R2 are not critical, though they must be equal to set the threshold at VDD/2.

Some microcontrollers have the option to connect the inverting input to an internal voltage reference. To use the reference in place of R1 and R2, move the input to the non-inverting input and set the output polarity bit in the comparator control register to invert the comparator output.

Note: Typical propagation delay for the circuit is 250–350ns using the typical on-chip comparator peripheral of a microcontroller.

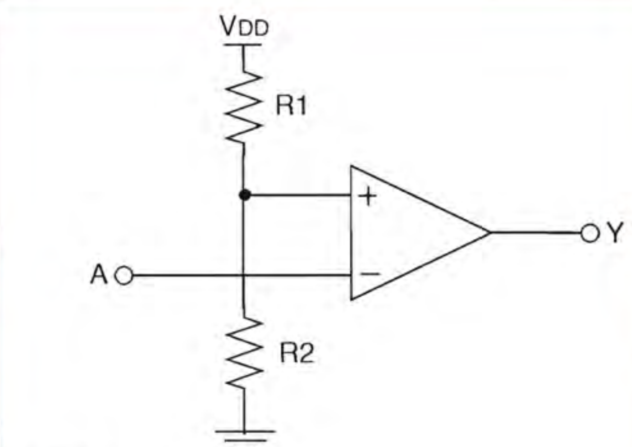

***Figure 1:** Inverter*

TiP 2: LOGIC – AND/NAND GATE

This tip shows the use of the comparator to implement an AND gate and its complement the NAND gate (see **Figure 2**). Resistors R1 and R2 drive the non-inverting input with 2/3 the supply voltage. Resistors R3 and R4 average the voltage of input A and B at the inverting input. If either A or B is low, the average voltage will be one half VDD and the output of the comparator remains low. The output will go high only if both inputs A and B are high, which raises the input to the inverting input above 2/3 VDD.

The operation of the NAND gate is identical to the AND gate, except that the output is inverted due to the swap of the inverting and non-inverting inputs.

Note: Typical propagation delay for the circuit is 250–350ns using the typical on-chip comparator peripheral of a microcontroller. Delay measurements were made with 10k resistance values.

While the circuit is fairly simple, there are a few requirements for correct operation:

1. The inputs A and B must drive from ground to VDD for the circuit to operate properly.
2. The combination of R1 and R2 will draw current constantly, so they must be kept large to minimise current draw.
3. All resistances on the inverting input react with the input capacitance of the comparator. So, the speed of the gate will

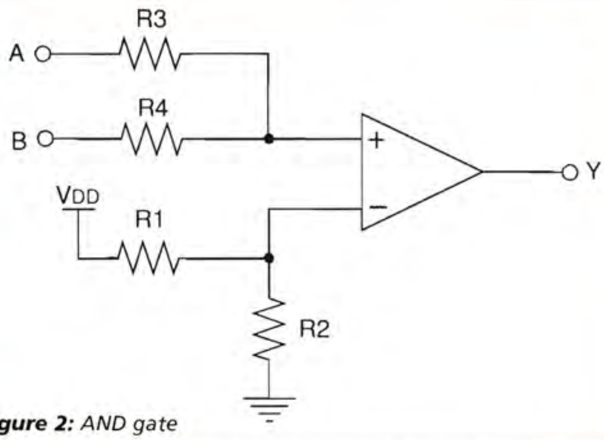

Figure 2: *AND gate*

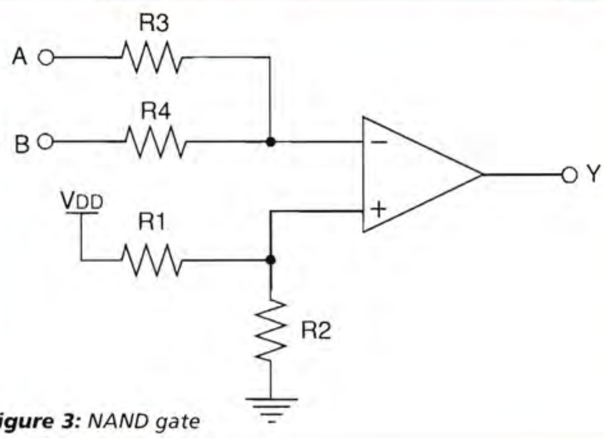

Figure 3: *NAND gate*

be affected by the source resistance of A and B, as well as, the size of resistors R3 and R4.

4. Resistor R2 must be 2 x R1.
5. Resistor R3 must be equal to R4.

Example:

- VDD = 5V, R3 = R4 = 10k
- R1 = 5.1k, R2 = 10k

TIP 3: LOGIC – OR/NOR GATE

This tip shows the use of the comparator to implement an OR gate and its complement, the NOR gate.

Resistors R1 and R2 drive the non-inverting input of the comparator with 1/3 VDD. Resistors R3 and R4 average the voltages of the inputs A and B at the inverting input. If either A or B is high, the average voltage is 1/2 VDD and the output of the comparator is high. Only if both A and B are low does the average voltage at the non-inverting input drop below 1/3 the supply voltage, causing the comparator output to go low. The operation of the NOR gate is identical to the OR gate, except the output is inverted due to the swap of the inverting and non-inverting inputs.

Note: Typical propagation delay for the circuit is 250–350ns using the typical on-chip comparator peripheral of a microcontroller. Delay measurements were made with 10k resistance values.

While the circuit is fairly simple, there are a few requirements for correct operation:

1. The inputs A and B must drive from ground to VDD for the circuit to operate properly.
2. The combination of R1 and R2 will draw current constantly, so they must be kept large to minimise current draw.
3. All resistances on the inverting input react with the input capacitance of the comparator, so the speed of the gate will be affected by the source resistance of A and B, as well as the size of resistors R3 and R4.
4. Resistor R1 must be 2 x R2.
5. Resistor R3 must be equal to R4.

Example:

- VDD = 5V, R3 = R4 = 10k
- R1 = 10k, R2 = 5.1k

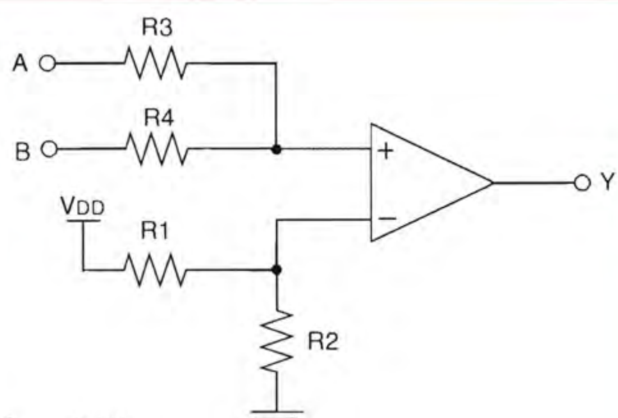

Figure 4: *OR gate*

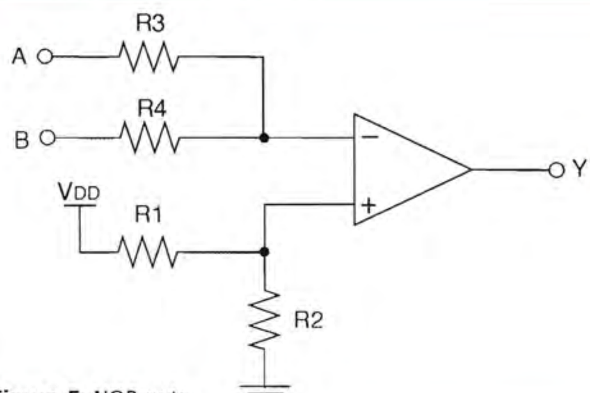

Figure 5: *NOR gate*

TIP 4: LOGIC – XOR/XNOR GATE

This tip shows the use of the comparator to implement an XOR gate and its complement the XNOR gate.

The operation is best described in three sections:

1. Both A and B inputs are low. With both inputs low, the inverting input is held at .7V and the non-inverting is held at ground. This combination results in a low output.
2. Both A and B inputs are high. With both inputs high, the inverting input is pulled up to VDD and the non-inverting input is equal to 2/3 VDD (the average of VDD inputs and GND). This combination also results in a low output.
3. Input A or B is high. With one input high and one low, the inverting input is held at .7V and the non-inverting input is equal to 1/3 VDD (the average of a VDD input and GND). This combination results in a high output.

Note: Typical propagation delay for the circuit is 250–350ns using the typical on-chip comparator peripheral of a microcontroller. Delay measurements were made with 10k resistance values.

While the circuit is fairly simple, there are a few requirements for correct operation:

1. The inputs A and B must drive from ground to VDD for the circuit to operate properly.
2. All resistances on the both inputs react with the input capacitance of the comparator, so the speed of the gate will be affected by the source resistance of A and B, as well as, the size of resistors R1, R2, R3 and R4.
3. Resistor R1, R2 and R3 must be equal.
4. Resistor R4 must be small enough to produce a 1.0V, or lower, voltage drop across D1 and D2.

Example:

- D1 = D2 = 1N4148
- R4 = 10k, R1 = R2 = R3 = 5.1k

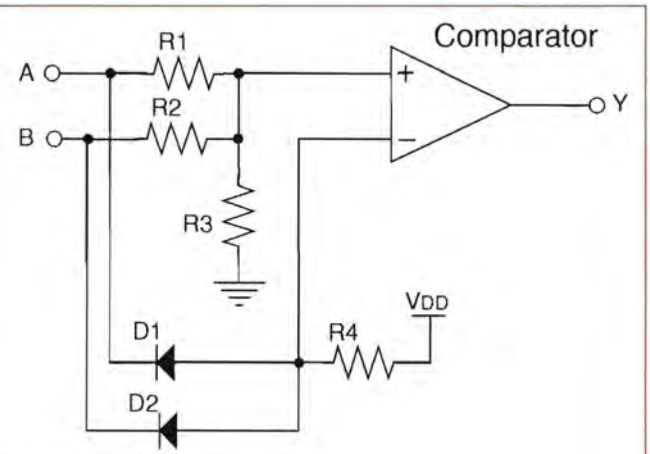

***Figure 6:** XOR gate*

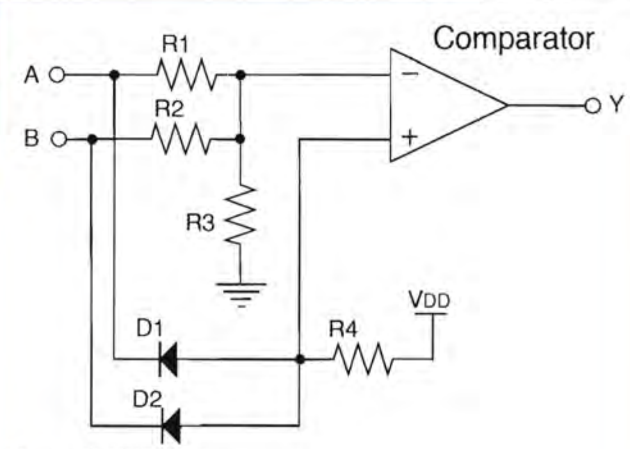

***Figure 7:** XNOR gate*

TIP 5: LOGIC – SET/RESET FLIP-FLOP

This tip shows the use of the comparator to implement a set/reset flip-flop. The inverting and non-inverting inputs are biases at VDD/2 by resistors R1 through R4. The non-inverting input also receives positive feedback from the output through R5. The common bias voltages and the positive feedback configure the comparator as a bistable latch.

If the output Q is high, the non-inverting input is also pulled high, which reinforces the high output. If Q is low, the non-inverting input is also pulled low, which reinforces the low output. To change state, the appropriate input must be pulled low to overcome the positive feedback. The diodes prevent a positive state on either input from pulling the bias of either input above VDD/2.

Note: Typical propagation delay for the circuit is 250–350ns using the typical on-chip comparator peripheral of a microcontroller. Delay measurements were made with 10k resistance values.

While the circuit is fairly simple, there are a few requirements for correct operation:

1. The inputs set and reset must be driven near ground for the circuit to operate properly.

2. The combination of R1/R2 and R3/R4 will draw current constantly, so they must be kept large to minimise current draw.
3. R1 through R4 must be equal for a VDD/2 trip level.
4. R5 must be greater or equal to R3.
5. R1 through R4 will react with the input capacitance of the comparator, so larger values will limit the minimum input pulse width.

Example:

- Diodes = 1N4148
- R1 = R2 = R3 = R4 = 10k
- R5 = 10k

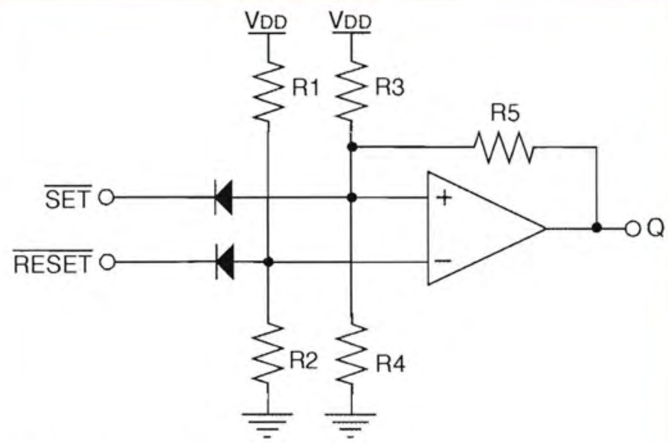

Figure 7: *Set/reset flip-flop*

Win a Microchip 16-bit Explorer Development Board

Electronics World is giving its readers the chance to win a Microchip 16-bit Explorer Development board. The Explorer 16 is a low cost, efficient development board to evaluate the features and performance of Microchip's 16-bit PIC24 microcontroller and dsPIC33 Digital Signal Controller (DSC) families, coupled with the MPLAB ICD 2 In Circuit Debugger, real-time emulation and debug facilities speed evaluation and prototyping of application circuitry. The Explorer 16 features two interchangeable Plug-In Modules (PIMs), one each for the PIC24FJ128 GA010 and the dsPIC33F128GP710 DSC.

It features both PIC24FJ128GA010 microcontroller and dsPIC33F128GP710 Digital Signal Controller PIMs, alpha-numeric 16 x 2 LCD display, interfaces to MPLAB ICD 2, USB and RS-232, includes Microchip's TC1047A high accuracy, analogue output temperature sensor, expansion connector to access full devices pin-out and bread board prototyping area, PICtail Plus connector for future expansion boards and full documentation CD includes user's guide, schematics and PWB layout.

For the chance to win an Explorer board, log onto **www.microchip-comp.com/ew-explorer16** and enter your details in the online entry form

Flat Panel Displays –

By Chris Williams, UKDL

The world of flat panel displays (FPDs) appears to draw heavily on conventional semiconductor technology to deliver many of the fine display products that are in the shops today, yet, the manufacturing processes are far apart. Today, semiconductors are routinely manufactured with multiple millions of transistors of identical performance and with individual topographical dimensions of significantly less than one micrometer. Most semiconductors are built on crystalline wafers and the active layers of the semiconductor are formed in the epitaxial layers that are complex depositions on top of the basic crystal lattice structure.

The FPD structures that use semiconductors are quite different. Semiconductors are required to form the circuit of electrical switches in the active matrix backplane. The active matrix thin film transistor backplane (Am TFT) is used to drive the liquid crystal display (LCD) that is assembled on top of it. Am TFT LCDs are used in laptop computers, desktop monitors, LCD TVs and, increasingly, in mobile phones and PDAs.

What is the function of the (Am TFT) transistor in an LCD display and why is it so different from the standard silicon chip?

Every display manufacturer has its own in-house design rules and guidelines that are generally secret. To avoid breaking any confidences on individual manufacturers' data, I can use a simple generic model. This isn't how you would design a circuit for manufacture, but it shows the principles involved.

The active matrix thin film transistor is built onto the rear glass of the LCD unit. When the transistor is turned on by applying a voltage to the transistor gate, electrons will flow through the transistor and into the charge storage capacitor. This charge will then create a differential voltage between the top plate of the capacitor and the inside surface of the top plate of glass forming the LCD cell. This electrical field is applied across the LC fluid that is trapped between the two surfaces, and this field will cause a perturbation to the transmission of light through the LC cell. As the charge that flows through to the storage capacitor is increased or reduced, the field across the LCD cell also increases or reduces and the amount by which the light transmission will be affected varies. This simple principle is at the heart of every active matrix LCD on the market today.

So where do the problems come from?

When conventional semiconductors are manufactured, the devices are 'grown' on wafers of crys-talline material that will be between 50mm and 300mm in diameter. The deposition processes are conducted in vacuum chambers at high temperatures. When active matrix LCDs are manufactured, the semi-conductors must be grown onto a glass substrate that may be as large as 2 x 2m.

This requires a whole new set of manufacturing principles that were pioneered at Dundee University in the 1960s. They showed how to create transistor functions by depositing amorphous silicon onto glass. Amorphous silicon does not have the same crystalline purity of conventional silicon and, as a result, the performance is much lower, but it can be deposited onto very large areas of glass and subsequently patterned into transistor structures.

Today, we have active matrix LCD TVs that are 60 inches diagonally in screen sizes. We see a screen image and we can comment on its colour fidelity, ability to show video without motion blur and whether we see strange artefacts, but hidden to our view is a world of fantastic engineering that has solved a large number of problems.

There is at least one thin film transistor fabricated at each sub-pixel position. For an HDTV LCD with resolution of 1920 x 1080 pixels, the actual number of sub-pixels is three times higher, since one colour pixel = (1 x red + 1 x green + 1 x blue) sub-pixels. There are a minimum of 1920 x (3) x 1080 TFT transistors = 6,220,800 transistors on the screen of an HDTV LCD TV set. Remembering that the field across the LC cell can be varied by controlling the charge current to the capacitor, which affects how much the LC cell modulates the light passing through it (which controls the greyscale), then it is clear that the colour that appears at each pixel is the same if the same driving voltage is applied to the transistors; so the transistors must have identical switching characteristics. These switching characteristics are defined during the manufacturing process, so it has to be ensured that at every position across the glass plate where depositing and processing this material is taking place is a consistent, repeatable and reliable process.

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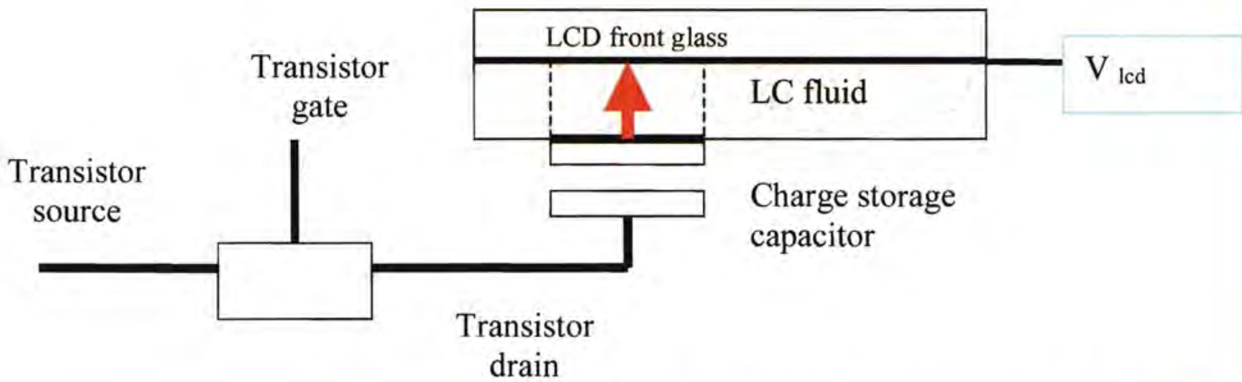


Basic structure of the active matrix TFI LCG unit

Furthermore, this amorphous semiconductor material has to "age" in a controllable and well-defined way. If some transistors age more quickly than others, then the amount of current they pass to the storage capacitor will change differentially over time and the colour that is expected at every pixel will not be delivered by the screen. Some pixels will perform as expected, but others that have aged more will have passed less charge to the capacitor, resulting in a smaller field than needed and the displaying of an inaccurate colour at that position.

Even the metalisation that is used to make the contacts within the LCD cell is a problem. As the display sizes have increased over time, the length of the metal tracks that are used to interconnect the thin film transistors have increased and, as the screen resolutions have increased, the width of these tracks have reduced. Longer, thinner tracks result in unwanted problems – increased track resistivity and increased power losses down the longer tracks. This has the simple effect of reducing the power input to all of the transistors that are furthest away from the point at which power is supplied into the track. For the design of a 60-inch LCD TV, the transistors positioned at the pixels in the top left hand corner will have to get the same amount of power per unit time as the transistors at the bottom left hand corner and bottom right hand corner. Again, if resistive power losses along the track itself reduce the power input to the transistors, so when the transistors are on, less charge will be passed to the storage capacitor than expected in any particular period of time, and the LC cell will not modulate the light correctly.

Manufacturers want to have tracks that have as low impedance as possible – less than 1Ω/square is an ideal target for sheet resistance. But using current materials that are deposited at moderate temperatures, the achievable impedances can be much higher than this, with sheet resistances of 5, 15, 50 or even more than 100Ω/square being quite common. Addressing this problem has been expensive and requires electronic compensation for the known reduced performance of the transistors furthest away from the source of power, as well as continuing research into new materials to offer improved performance in the first place.

These technology challenges increase tremendously when we look to create active matrix backplanes using organic as well as inorganic semiconductors deposited onto flexible plastic substrates.

Chris Williams is Network Director at UK Displays & Lighting KTN (Knowledge Transfer Network)

Processor Module Features Dual-Core Xeon

Concurrent Technologies has announced a high performance Advanced Mezzanine Card (AdvancedMC), a double-width, full-height, processor module suitable for AdvancedTCA, MicroTCA and proprietary platforms. The AM 100/20x uses the dual-core Intel Xeon processor to provide high performance processing, and the Intel 3100 chipset, which combines server-class memory and I/O controller functions into a single component.

The AM 100/20x module supports the dual-core Intel Xeon processor LV @ 2.0GHz or the dual-core Intel Xeon processor ULV @ 1.66GHz. By using appropriate operating systems and applications software, a computing performance increase (for the same clock frequency) of up to two times a single-core Intel Xeon processor is achievable. The Thermal Design Power (TDP) for the Dual-Core Intel Xeon Processor LV @ 2.0GHz (667MHz FSB, 2MB shared L2 cache) is 31W versus 35W TDP for the single-core LV Intel Xeon processor @ 2.0GHz (400MHz FSB, 512kB L2 cache); the dual-core Intel Xeon processor ULV @ 1.66GHz (667MHz FSB, 2MB shared L2 cache) with a TDP of 15W gives a remarkable increase in performance/Watt.

The Intel 3100 chipset, a single chip embedded server chipset, interfaces up to 16GBytes DDR2-400 ECC memory with a peak memory bandwidth of 3.2 Gigabytes/s.

www.gocct.com

Drop-In Processors For Video SOC Design

Tensilica introduced four new Diamond Standard VDO (ViDeO) processor engines customised for multi-standard, multi-resolution video in System-on-Chip (SOC) designs. These are Diamond 381VDO, Diamond 383VDO, Diamond 385VDO and Diamond 388VDO. They are targeted at mobile handsets and personal media players (PMPs).

They are fully programmable to support all popular VGA and standard definition (SD, also known as D1) video codecs with resolutions up to 720 x 480 (NTSC) and 720 x 576 (PAL) including H.264 Main Profile, VC-1 Main Profile, MPEG-4 Advanced Simple Profile (ASP) and MPEG-2 Main Profile, each of which is available from Tensilica. Lower resolutions such as QCIF, QVGA, CIF and VGA are also supported.

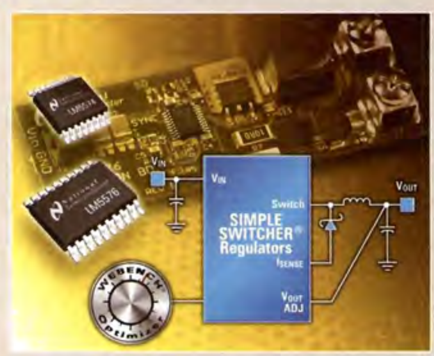
The Diamond Standard VDO engines host all the key video processing functions in software on the cores – including the network abstraction layer, picture layer, slice layer, bit-stream parsing and entropy decoding and encoding. This includes the computationally demanding CABAC (Context Adaptive Binary Arithmetic Coding) decoding in the H.264 Main Profile decoder. It is implemented in a separate and complex non-programmable hardware block as it necessitates more than 700MHz of general CPU workload, which significantly increases power consumption. By implementing CABAC in instruction set extensions, Tensilica was able to create a low MHz and power efficient version of CABAC in less than half the area of a typical CABAC hardware block.

www.tensilica.com

Flexible Switcher Buck Regulator Family

National Semiconductor has added six more high-frequency buck regulators to its Simple Switcher product family.

The new regulators are based on a patented emulated current mode technology, which provides a load transient response in low duty cycle applications, not addressable by traditional current mode control. To reduce EMI, a frequency synchronisation pin allows multiple ICs from the family to self-synchronise or to synchronise to an external clock. The new regulators guarantee robustness with cycle-by-cycle current limit, short-circuit protection and thermal shut-down.



Emulated current-mode control overcomes traditional current-mode control's noise susceptibility by emulating the buck switch current signal, which is then used for current-mode control. The emulated buck switch current signal is the sum of an emulation ramp current and the sampled diode current just before switching occurs. Avoiding direct buck switch current measurement minimises the effect of switching noise, while maintaining the benefits of the current-mode control.

The six products included in the new line are the 0.5A LM5574, 1.5A LM5575 and 3.0A LM5576 buck regulators, which feature an input voltage range from 6V to 75V and adjustable switching frequency between 50kHz and 500kHz; and the 0.5A LM25574, 1.5A LM25575 and 3.0A LM25576 buck regulators, which feature an input voltage range from 6V to 42V and adjustable switching frequency between 50kHz and 1MHz.

www.national.com

High-Gig Pattern Generators

Agilent Technologies introduced the J-BERT N4903A 7Gb/s and 12.5Gb/s pattern generators with complete jitter injection capabilities. With them, serial high-speed ports with all types of jitter can now be quickly and accurately simulated.

The J-BERT N4903A pattern generators enable fast and accurate testing by simplifying worst-case jitter tolerance testing with built-in and calibrated jitter sources for random jitter, periodic jitter and bounded uncorrelated jitter. They also emulate inter-symbol interference (option J20); test robustness against differential-mode or single-mode noise (option J20) and inject commonly used spread spectrum clocks.

Complex training sequences can be set up easily with the pattern sequencer and 32MB pattern memory; all types of clock and data rate ratios can be generated with the sub-rate clock outputs. The generators cover all popular data rates between 150Mb/s and 7Gb/s (option G07) or to 12.5Gb/s (option G13).

The instruments give accurate results based on excellent signal performance with 20ps transition times (20-80%) and 9ps peak-peak jitter. They provide scaleable functionality, which allows the user to add complete J-BERT functionality over time with error detector, CDR and complete jitter tolerance test.

www.agilent.com/find/jbert

720MB/s VXS Data Recorder

VMETRO expanded its Vortex range of high-speed data recording solutions with the introduction of the Vortex M6000 VME/VXS recorder. Supporting dual 4Gb/s or quad 2Gb/s Fibre Channel ports, this high speed recorder is able to achieve 720MB/s recording performance in a single 6U VXS (VITA-41) slot. The Vortex M6000 recording engine provides an effective platform for a number of applications in industrial inspection systems, medical scanners and Intelligence, Surveillance and Reconnaissance (ISR) applications such as Signal Intelligence (ELINT/COMINT), as well as Software Defined Radio (SDR), Synthetic Aperture Radar (SAR), Moving Target Indicators (MTI) and many other high-speed data recording needs.

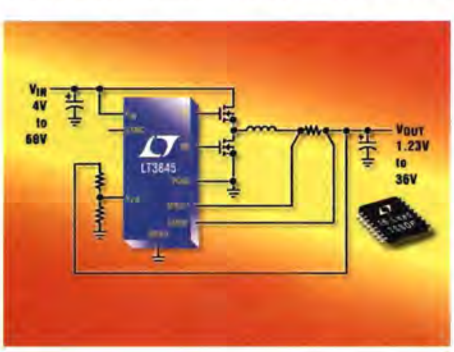
The Vortex recording engines are the common foundation of all of VMETRO's Vortex data recording and playback solutions. The Vortex M6000 VXS/VME data recording and playback systems include fourth generation hardware platforms designed to provide the highest possible streaming data throughput from the I/O interface to the storage system.

Its features include VME/VXS (VITA-41) recording, playback and analysis solutions, dual 4Gb/s or quad 2Gb/s Fibre Channel interfaces and customisable I/O through XMC/PMC sites utilising PCI Express or PCI-X/PCI. The systems are available in open (customer programmable) or targeted versions. They can be pre-programmed web-browser GUI for all recorder functions. VxWorks and Linux support is also available.

www.vmetro.com

60V Input DC/DC Synchronous Controller

Linear Technology has announced its LT3845, a 4V to 60V input range, synchronous DC/DC step-down controller with adjustable operating frequency of between 100kHz and 500kHz. At higher frequencies users can implement a smaller inductor and capacitors, or at lower frequencies they can optimise the efficiency of the circuit. For noise-sensitive applications, the LT3845 can be synchronised to an external clock from 100kHz to 600kHz. The minimum 4V input maintains operation during automotive cold cranking and the 60V maximum input withstands inductive load dump peak voltages. In addition, the output voltage can be adjusted over a wide range from 1.23V to 36V at load currents up to 20A. Applications include 12V and 42V automotive, 48V telecom supplies, heavy equipment systems, avionics, industrial controls and distributed power systems.



The LT3845 is a current mode controller with an integrated biasing regulator that drives N-channel MOSFETs. Current mode operation provides fast line and load transient response, as well as cycle-by-cycle overcurrent protection. The integrated regulator provides IC power directly from the input supply without the need for a separate bias voltage. It maintains high efficiency at light loads with its Burst Mode operation and 120μA quiescent current, a feature required in many automotive and battery-supplied input applications.

Other features include short-circuit protection, adjustable soft-start, thermal shutdown and precision input undervoltage lockout. The LT3845 employs adaptive overlap control, which maintains a constant dead time, preventing shoot-through switch currents, independent of the type, size or operating conditions of the external MOSFET switches.

www.linear.com

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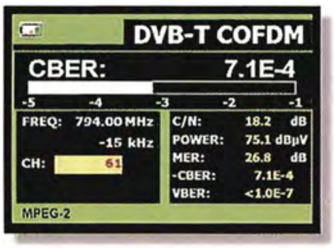

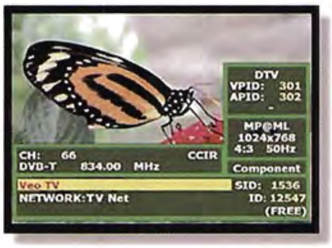

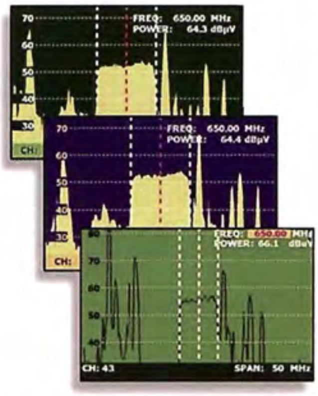

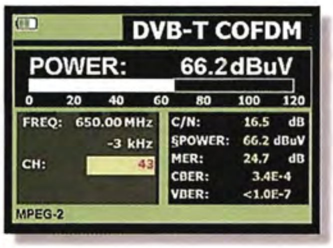

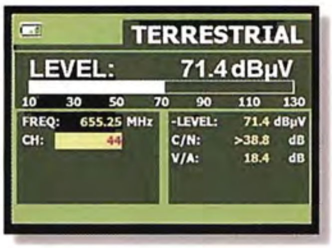

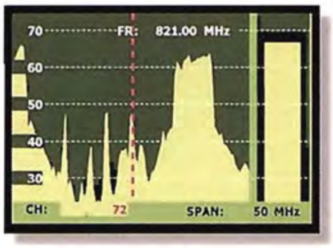

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