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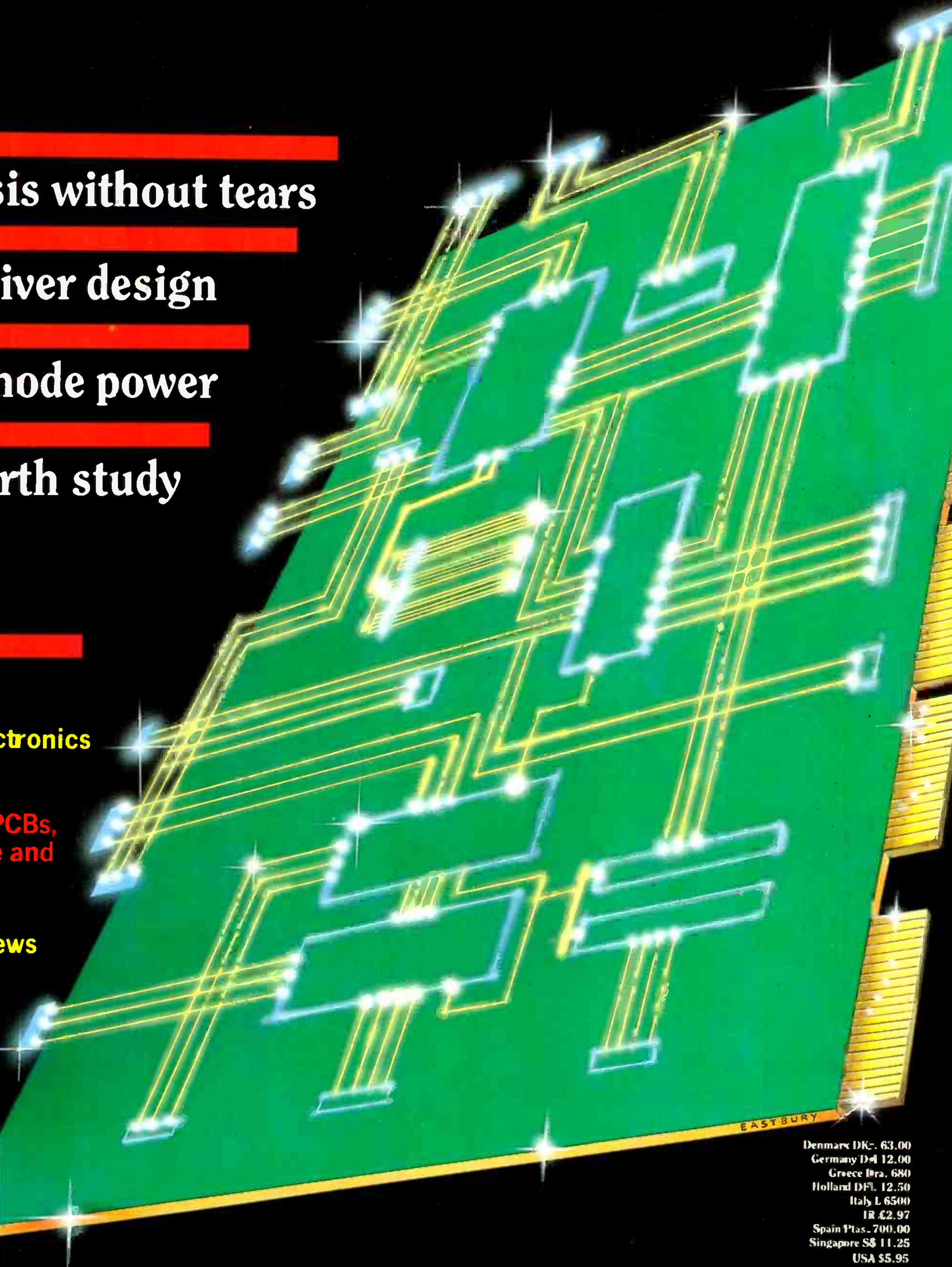

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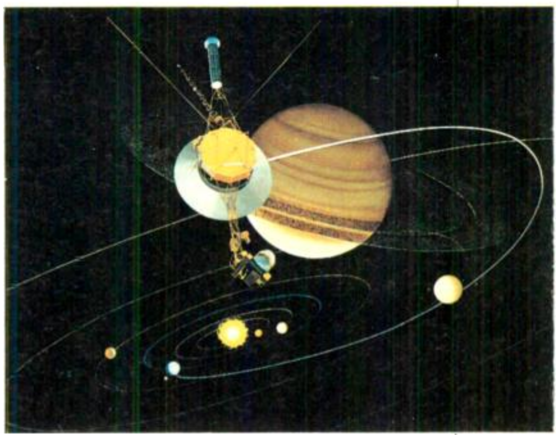
JULY 1989 VOLUME 95 NUMBER 1641

In the next issue. New Wave Microwave. The August issue of Electronics & Wireless World will present a series of articles charting the rise and rise of microwave technology. The advent of satellite broadcasting has changed the price structure of microwave technology dramatically. Microwaves belong exclusively to the military no longer.



From Neptune, on 30 watts: Voyager-2 cruises into Research Notes, page 648.

Special offer to E&WW readers: for details of this 20MHz oscilloscope and the digital multimeter which comes with it, turn to page 650.

Typical PC-based cad station with PCB design in progress, using PADS-PCB from Microtel which is to be described in a future issue.

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No business in show business

The UK's largest electronics show, British Electronics Week, is over for another year. We hope that it will be the last. Opinion, perhaps, but a widely held one if the results of a straw poll among the people who attended and exhibited was anything to go by.

One couldn't possibly deny the sheer scale of the "Week" as the organizers like to call it. It occupies virtually the entire floor-space of Olympia for its three day duration. It has swallowed up the old ECIF event, much of Internepcon and a few others besides. One couldn't possibly think of not exhibiting or attending, or could one?

The opinion of the largest exhibitors: "We spend £50 000 putting the stand together and we don't really know what we get for the money". Of course they don't. They exhibit for the image. They've already identified the major business prospects with a field sales force.

The smaller companies have to pay upwards of £4000 for their stands. They look for "good" enquiries and try not to think about the additional costs involved in keeping highly qualified people cooped up on a stand for a few days, touting for custom from visitors walking the aisles.

Then consider opinions from the visitors themselves. Some will work for large companies who can afford to send people down to the bottom half of the country. Others live in the South East and can reasonably endure the miseries of a short journey to Olympia. The remainder of the electronics industry has to do without the dubious benefits of British Electronics Week.

The event has now reached such a size that, unless you organize a visit very carefully, you have little hope in seeing all that you really wish to see and of meeting all the people you would really wish to meet. The situation has elements of Catch 22. You've got to know what you want to see before you see it but you can't know what you want to see until you have. The earlier, smaller venues offered a showcase; the design engineer looking for ideas could wander around and see everything, not missing anything. The only consequences a visitor can now guarantee are mental numbness and aching feet.

The answer may lie in the staging of small, specialist shows, preferably on a regional basis. This merely reflects the way in which electronics professionals work. Most concentrate within a particular design area; for example, digital, micro, linear. The problems in attending distant venues remain and it seems unrealistic to expect small companies to exhibit at more than a couple of shows in any year.

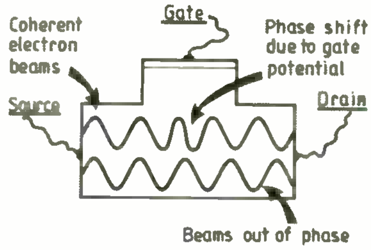
It could be that you have just picked up the answer in the magazine you are now holding. The UK's technical press leads the world in its variety, specialization, content and readership. *Electronics & Wireless World* plans more than its fair share of coverage for electronics professionals.

Super-fast transistor out in the cold?

Quantum electronics is a subject that's guaranteed to make many of us feel we're beginning to lose touch with reality. Its main contention – that electrons are waves – somehow doesn't seem to square with the familiar mental image of little black balls threading their way through atomic lattices. And despite the fact that most of us were treated to liberal doses of the wave/particle duality of electromagnetic radiation at school, its analogue in electron behaviour seems remote.

Small wonder then that most of today's devices exploit only the particle character of the electron, relying as they do on diffusion or charge density modulation. Tunnel diodes and quantum-well devices are among the few exceptions. Yet theoreticians have known for some time that quantum effects hold out a tremendous potential for increased performance; in simple terms, waves are faster and cleaner than particles.

One of the most interesting proposals recently discussed (Appl.Phys.Lett. Vol. 54, No 350) is a design for transis-



tors based on quantum interference between parallel waves of electrons. It's a bit like holography, in which small phase changes between two coherent beams of light lead to interference patterns or holograms. In the case of the quantum transistor, the effective path length of one of two electron beams would be modulated by applying a voltage to a gate electrode. The two sets of waves arriving at the drain would then interfere constructively or destructively, depending sensitively on the gate voltage.

So beautiful is the concept that you might be forgiven for wondering why you can't order such devices off the shelf especially as their speed and noise performance would be exceptional by any standards.

The first major obstacle is that such a device would require a pair of electron beams with a high and consistent phase coherence. As yet this hasn't been unequivocally demonstrated in solids, the problem being that electrons continually interact with impurities, dislocations and lattice vibrations to prevent any sort of coherence, except over extremely short distances.

Many theoreticians are now of the opinion that these difficulties can either be allowed for or eliminated by operating the device at a temperature close to absolute zero. Gerhard Fasol of the Cavendish Laboratory (*Nature* Vol. 338 No 6215) thinks that the phase coherence length for electrons in gallium arsenide heterojunctions should be of the order of 5μm at 0.1K – a temperature too low even for liquid helium. So Sol's quantum interference transistor, whilst miraculous in theory, would be impracticable at present.

Brew your own chips

If ultra-low temperatures are difficult to achieve, then ultra-tiny dimensions may prove the easiest route to exploiting quantum effects in electronics. Certainly there's a greatly renewed interest in low-dimensional structures such as quantum wells and super-lattices. But what about semiconductor particles in which quantization occurs not just in one dimension, but in three?

In very small colloidal particles, less than 100nm in diameter, size quantization results in a new class of materials with properties intermediate between those of a single atom and those of a bulk solid. Confinement of electron-hole pairs leads to an increased conduction band-gap and hence interesting new properties.

But if this sounds like another example of over-funded physicists tinkering around with bizarre and useless states of matter, it's worth noting that Nature may have already learned to exploit quantum semiconductors.

C.T. Dameron *et al.* from the University of Utah have shown (*Nature* Vol. 338, No 6216) that two varieties of yeasts can biologically synthesize cadmium sulphide crystals on this almost sub-microscopic scale. They do it ostensibly to get rid of cadmium, a substance that is normally poisonous in its bulk form, by transforming it to quantum-sized crystals in which form it is stable and harmless to the yeasts.

When such crystals were extracted from the yeasts, the Utah researchers found that they were perfectly uniform in size and had extremely consistent physical properties.

Further research has shown that, far from being biological rarities, quantum-sized semiconductor crystals are probably quite common in nature.

More interesting still is the possibility that cells such as yeasts might be harnessed by man to grow the raw materials for a whole new class of electronic devices, especially solar cells, lasers and other optical devices. In fact it doesn't go beyond the bounds of reasonable speculation to imagine electronics raw materials that are brewed for their precise application as you or I would tailor other yeast by-products. . . a tin of Bootsbury's ReadiBrew and a good fermentation lock.

Ear on the universe

A sub-millimetre-wave telescope with a 10 metre diameter dish antenna has been designed to scan the heavens through what, up till now, has been a closed window. It's a joint venture between the Max-Planck-Institut für Radioastronomie in Bonn and the University of Arizona.

Normally radio waves of less than a millimetre are strongly absorbed by water vapour in the atmosphere; so to work effectively the new telescope is to be installed next year on the 3300m summit of Mount Graham, some 150km from Tucson, Arizona. This places it above the bulk of the vapour and will enable it to get a clearer picture of millimetre emissions from space.

The telescope, manufactured by two German firms, is reported (*Deutscher Forschungsdienst* Vol. 28 No1/89) to be virtually complete and ready for testing. The antenna surface is made from carbon fibre-reinforced material which deviates no more than 0.015mm from a true paraboloid at any point.

When installed and working, the sub-millimetre wave telescope will be used by astronomers to gain insight into what takes place inside optically-dense clouds of interstellar matter where, it's thought, stars are born.

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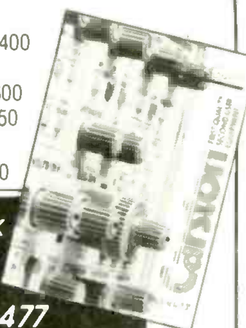

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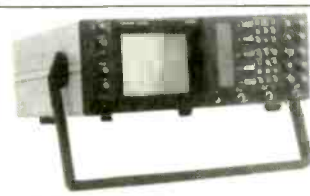

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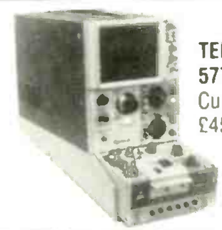

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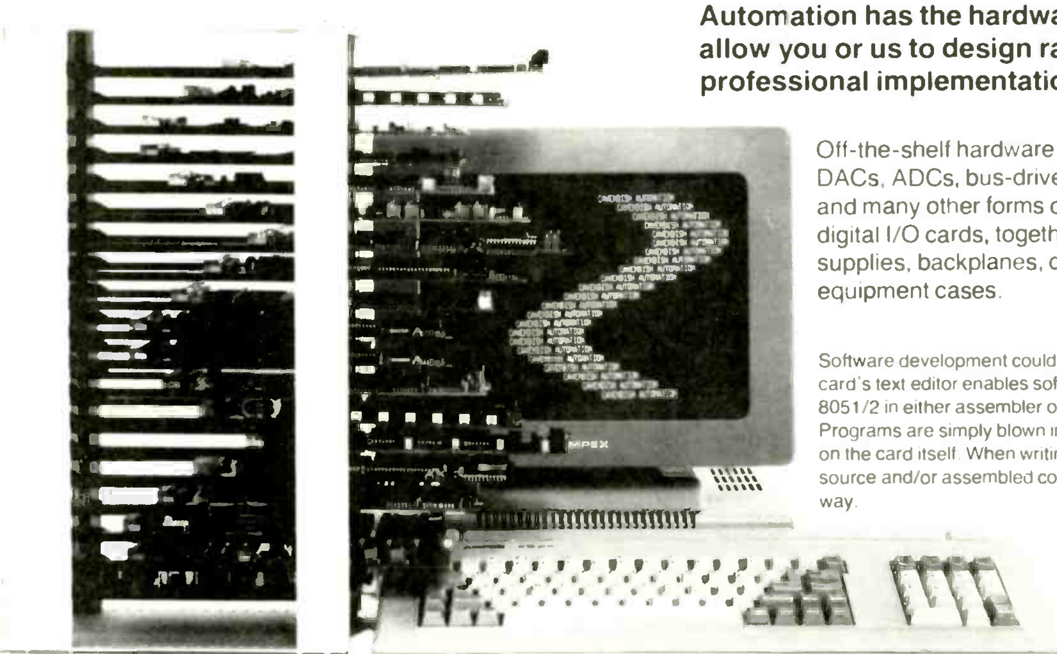

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Engineering in the blood

For those of us who feel squeamish at the thought of a spider crawling up our legs, how about a creepy-crawlie that gets inside the body and swims about in the blood stream? It's not a bad dream, nor even a good Hitchcock movie, just a sober project dreamed up by Professor Iwao Fujimasa and a team of engineers at Tokyo University.

If you recall the micro-robots being devised by the Massachusetts Institute of Technology for cleaning windows then this is just the same principle scaled down another couple of orders of magnitude. Fujimasa, whose work is being taken very seriously by companies like Toyota and Hitachi, believes that within ten years it will be possible to create micro-robots that can be injected into the body and which will be able to swim through the bloodsteam to the site of some obstruction or lesion. There they'll perform an operation by remote control and then swim away when the job is complete. So seriously is this bizarre prospect being taken that the Japanese Ministry of International Trade and Industry (MITI) is expected to contribute about £20 million to get the work under way.

In engineering terms the obstacles are phenomenal. Today's chips are much too large for the control and communications aspects of the micro-robot; sensors and power supplies are even more so. But the truly amazing prospects are those of micro-miniaturizing mechanical parts such as motors and gears. In the USA, gear trains have already been cut at sub-millimetre size by lithography, but the Japanese are actually planning to make micron-sized moving parts.

Fujimasa is confidently predicting that by the end of next year he will have a proto-type micro-robot capable of travelling around in the body and communicating its whereabouts. Later, but still within the foreseeable future, he expects to be able to add simple sensors for doing reconnaissance jobs around our innards. Thereafter it will be on-board micro-lasers to zap our clots and beam up our tumours. Utterly incredible, but it doesn't half give you a creepy feeling. . .

Digging for cosmic answers

Europe's deepest mine shaft, the 1100m Boulby potash mine in North Yorkshire will be the site of a feasibility study to detect the so-called missing mass or 'dark matter' of the Universe. This material, which could comprise anything from tiny black holes to as-yet undiscovered subatomic particles, is thought by cosmologists to make up 90% of the Universe.

The reason for setting up the experimental detectors in a potash mine is quite simply that the depth of earth will form an effective screen for the showers of spurious particles produced by cosmic radiation which would otherwise 'blind' the equipment. Even at 1100m the researchers, from six British universities and the Rutherford Appleton Laboratory, plan to line their 500m^3 experimental cavern with further layers of specially-developed screening materials, possibly of lead or salt.

If this preliminary study proves that the search for 'dark matter' is worth pursuing and if the necessary funds are forthcoming, then a full-scale experiment will get underway later this year. Special detectors will be developed to measure the recoil of an atom when its nucleus is hit by particles of the hypothetical dark matter.

Boulby mine isn't by any means the deepest in the world, nor is this the only attempt ever made to find the missing mass of the Universe. Nevertheless if it succeeds, this work will go a long way to unravelling one of cosmology's greatest mysteries.

Research Notes is written by John Wilson of the BBC World Service science unit.

Busking under the bridge?

Physical scientists throughout the ages seem to have enjoyed a certain dalliance with the musical arts, notably men like Herschel and Borodin. Even today, great minds expend vast amounts of energy and hours of computer time trying to re-compose Bach or make a perfect bassoon from old wardrobe panels.

One gentleman of this kind, who I confess has escaped my attention until now, was no less than Sir Charles Wheatstone (popularizer of the Bridge*). Sotheby's, whose annual sale of scientific instruments on May 5 was to have included nearly 50 items of Wheatstone memorabilia, ample evidence of his musical pursuits. Lot 16, an automatic harmonium chord transposition assembly, was accompanied by lot 27, a patent bellows fiddle. Or would have been, had not the whole Wheatstone collection been withdrawn from the sale following a legal dispute about its ownership. So you could still have a chance to bid when the matter is settled.

But new to me was the realization that this great Professor of Experimental Philosophy was also the inventor and perfector of . . . .the concertina!

* See Pioneers: Charles Wheatstone, master of telegraphy, *E & WW* April 1987

Some of Wheatstone's first bridges were on stringed instruments such as this Wheatstone & Co. Harpe-Lute of 1810-1815, Lot 18 in Sotheby's sale catalogue. By the age of 14, in 1816, young Charles was already working at his uncle's music business at 436 Strand, London, where this and other instruments were made and sold.

From Neptune, on 30 watts

After an incredible twelve-year journey through interplanetary space, America's Voyager-2 will rendezvous with Neptune on August 24. Already this hardy little spacecraft has sent back to Earth some amazingly detailed pictures of what is currently the most distant planet in the solar system.

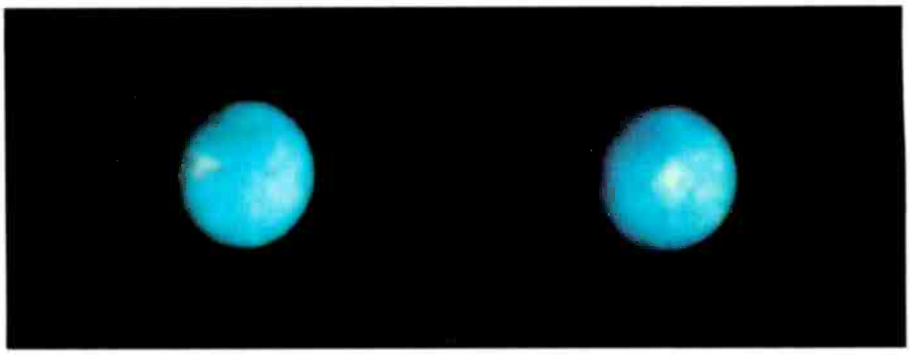
When Voyager-2 was launched by NASA in 1977, the main object of the mission was to explore the two great planets Jupiter and Saturn and their various moons. Needless to say, even that involved an extraordinary feat, not just of planetary ballistics but also of data storage and transmission, especially when you consider that the radio range from Saturn is about 2×10^9km.

Saturn, however, wasn't to be the last planetary encounter for Voyager-2. Early in 1986 it went on to explore Uranus, together with its rings and five major moons. Uranus is so far away that, since its discovery 200 years ago by William Herschel, we've learnt very little of this distant world except that it has a 'horizontal' axis of rotation and more-or-less rolls its way around the Sun!

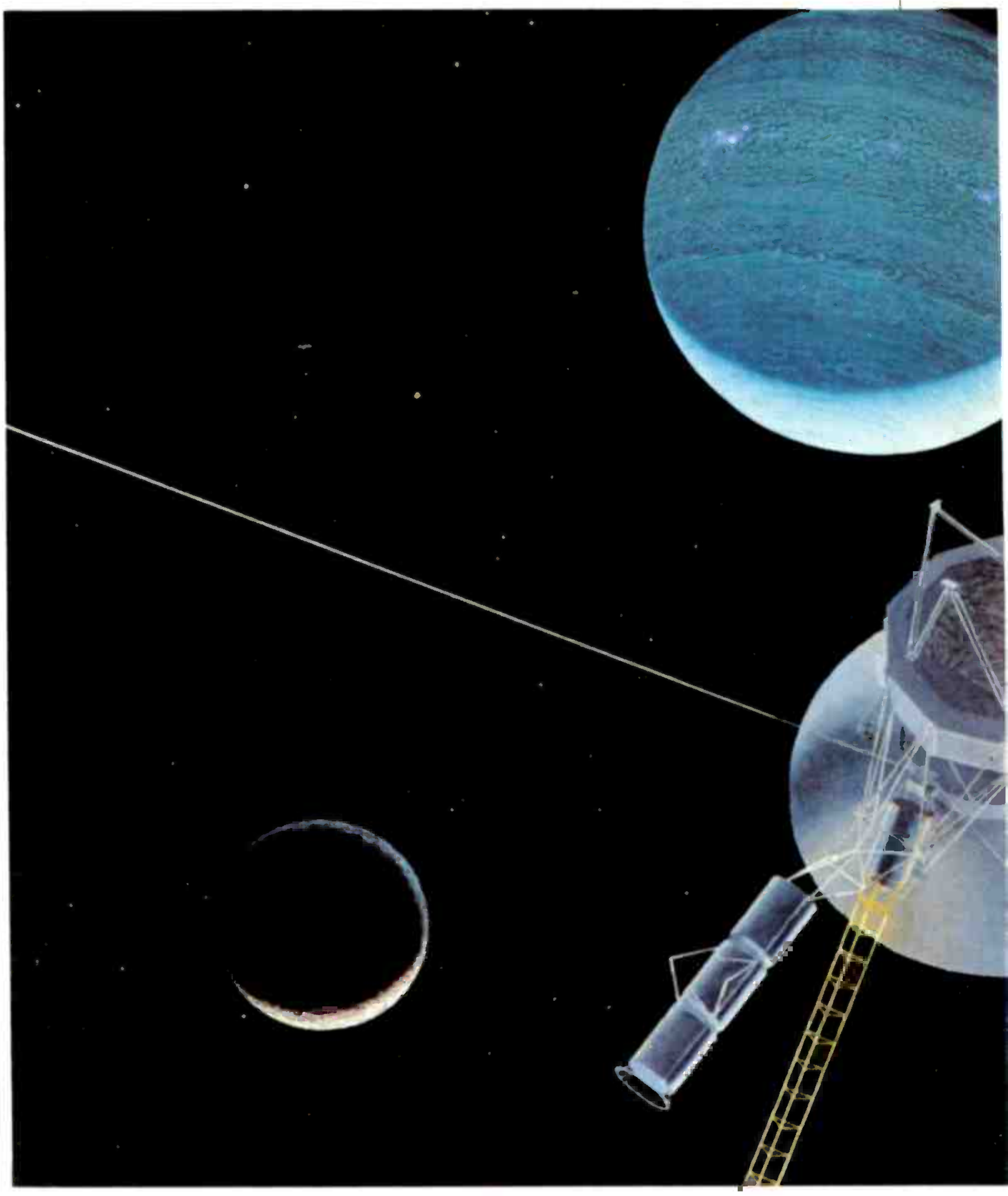
What NASA never dared suggest at the time of its launch was that Voyager-2 could theoretically make its way to the very edge of the Solar System and encounter Neptune (Pluto is currently orbiting inside Neptune's orbit). Yet, thanks to a rare planetary alignment that happens only once every 177 years, it was simply a matter of juggling with trajectories – a sort of interplanetary game of snooker. 'Simply' is perhaps the wrong word, for NASA likens the required degree of accuracy to that of hitting an atom from a distance of a few hundred metres.

Neptune is at present 4.5×10^9km from the Sun, a distance at which it's over four hours' journey by any form of electromagnetic radiation. Any communication from NASA's deep space tracking network therefore takes around twice that time to be acknowledged. Two-way communication is achieved on S-band and X-band using two highly duplicated systems feeding two separate antennas.

The S-band transmitter consists of two redundant exciters and two redundant RF power amplifiers of which any combination is possible. Only one exciter-amplifier combination operates at any one time. Selection of the com-



Above: colour images of Neptune by Voyager-2, taken two hours apart, from about 309 million kilometres away. Note the movement of the bright cloud feature which is consistent with a 17-18h rotation period. Below: NASA painting shows Neptune and its moon Triton just after Voyager's fly-by on August 24, 1989.

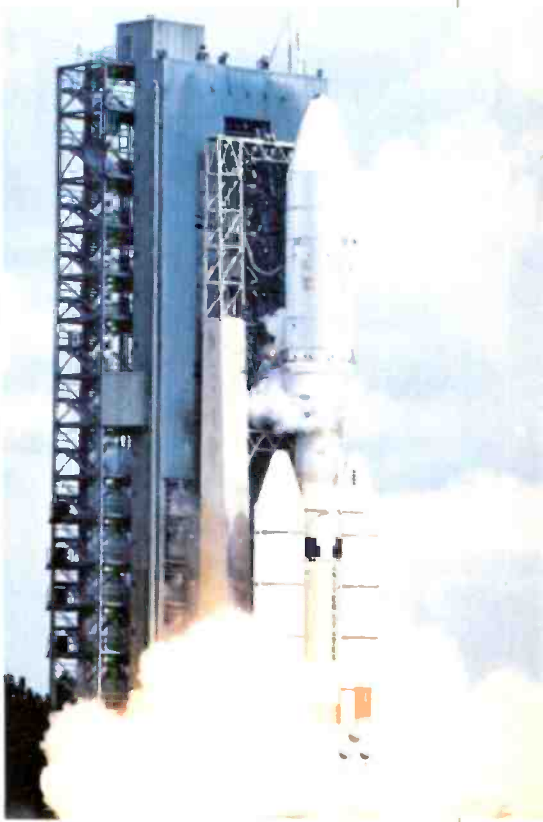


bination is by onboard failure detection logic within the computer command subsystem (CSS), with ground control backup. The same arrangement of exciter-amplifier combinations makes up the X-band transmitting unit.

One S-band and both X-band amplifiers employ travelling wave tubes. The second S-band unit is a solid-state amplifier. The S-band transmitter is capable of operating at 9.4 watts or at 28.3 watts when switched to high power and can radiate from both antennas. X-band power output is 12 watts and 21.3 watts. X-band uses only the high gain antenna.

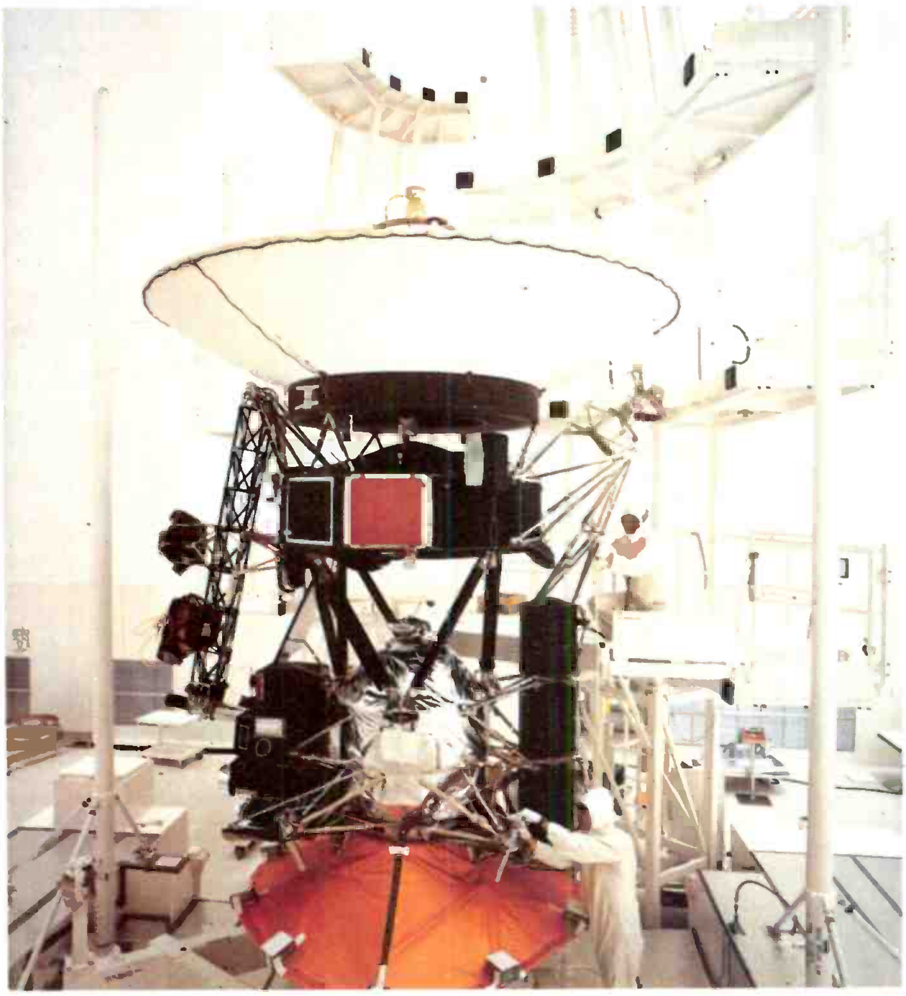
All data is sent in digital form, slowed down when necessary by means of a belt-driven magnetic tape drive. Even then, full resolution television pictures from Saturn required a frame read-out time of 144 seconds. As received on Earth, the data rate varies from 40bit/s to 115kbit/s depending on its nature and the range of the craft. Slow it may seem, but it's no means feat to receive anything at all from a 30 watt transmitter at a range of four-and-a-half billion kilometres!

With only a few months and a few hundred thousands kilometres left to go to Neptune, NASA are keeping their fingers firmly crossed for Voyager-2. If the promise of these early pictures is anything to go by, one could soon be in for some spectacular shots from a distant world where the summer temperature rarely rises above −220°C. ■



Right: Voyager-2's launch aboard a Titan/Centaur-7 on August 20, 1977.

Below: test model of Voyager-2 being checked in the Kennedy Space Centre's industrial area.



10W flyback converter

Multiple-output SMPSs must often provide independent auxiliary current sources for control and monitoring. The Siemens TDA 4814 uses a triangular current characteristic in self-oscillating flyback converters

J. NATTRAS and S. WRIGHT

The flyback converter principle permits low-cost control of several auxiliary output voltages over a wide supply voltage range. Both applications shown in **Fig. 1** have three outputs each protected against overload and short-circuit. A 12V output powers the control and monitoring logic of the main SMPS primary. Since no electrical isolation is needed, it is further used for the power supply and control of the TDA 4814 controller. An isolated 15V output supplies the control and monitoring circuitry of the SMPS secondary and a tightly toleranced and isolated 5-V output supplies any TTL logic.

One of the converters shown exhibits an input-voltage range of 100 to 450 V, whilst the other will only operate at inputs greater than 250 V because of its undervoltage monitor: a thyristor is triggered via an additional isolated output to overcome the on-resistance and permit smooth capacitor charging at switch-on of a high power switched-mode power supply.

TDA 4814 controller

Controlling the outputs with the TDA 4814 ensures protection against overvoltage and short-circuit. This is achieved by using the on-chip operational amplifier to control the first 12V output, the remaining outputs being indirectly controlled by transformer winding ratios. Good coupling is required to ensure voltage stability. The tolerances required at the 5V output are achieved by designing the winding for a 7.5V output and adding a fixed voltage regulator. The switching transistor in the primary side is driven directly from the chip.

Switching transistor. Maximum drain-source voltage $V_{DSmax} = V_{INmax} + V_R$, where V_R is the flyback or demagnetisation voltage, in this case 150V. Hence $V_{DSmax} = 450 + 150 = 600$ V.

However, this does not account for the voltage transients which occur at switch-off. Hence, the BUZ 78 SIPMOS transistor (V_{DSmax} = 800 V, $R_{DS(on)}$ = 8 ohms, I_D = 1.5 A) was selected as a suitable device.

Transformer. The winding details shown in **Fig. 2** show how the primary and secondary windings are interleaved in layers. The EC35/17/10 transformer core (N27) is large enough to take six windings while providing the required creepage paths. Good coupling is obtained when the start of each winding is on the same side, enabling the electric field to be built up geometrically in the same direction.

Start-up. Resistors R_2 - R_4 provide the necessary standby current with minimum input voltage: with maximum input voltage (450 V) there is no overloading.

The standby current is that required by the standby function of the TDA 4814 (maximum 0.5 mA). The undervoltage monitor (TAE 1453) requires a further 2 mA.

The TDA 4814 becomes fully operational once its threshold voltage has been reached. An auxiliary trigger signal, possibly derived from the undervoltage monitor, starts the flyback converter which then draws the required current from the first winding.

Auxiliary trigger. The auxiliary trigger signal is provided by the internal start logic, which functions as a diac with a 20V trigger voltage. The signal at Q START is coupled via R_{18} to the detector input, this signal being suppressed in normal operation by the low-impedance signal from the detector winding.

Power unit. With SIPMOS transistor Tr_1 conducting, current rises linearly from zero and is measured via a series resistance. When a peak-current value given by the control amplifier is reached, transistor Tr_1 is blocked. At this time, the potential at the detector input is high, maintaining the transistor-off state. Once the transformer has completely discharged the stored energy to the secondary side, the detector winding changes polarity and Tr_1 is turned on once again.

In the event of a short-circuit, the voltages at the output windings will be low. The detector winding is designed such that these low voltages are sufficient for reliable triggering.

Current detection. Low-pass filters C_{10}, R_{11}, C_4 and saturation choke L_4 are included to reduce the influence of parasitic currents when the load current is low. This leads to continuous operation even at low loads and supply voltages below 300 V. A bias voltage of about 100 mV at the comparator input (R_{10}, R_{11}) eliminates the problem of negative voltages originating from the charging currents of the SIPMOS capacitances.

Voltage limiting. The interleaved primary transformer windings give a wide tolerance to load distribution at the output windings. However a resistor-capacitor-diode network is included to limit transients which may occur at switch-off.

Smoothing. AC capacitors C_{11}, C_{14} and C_{17} help to reduce the effects of high dI/dt on the output electrolytics. Even so, high-frequency ripple will occur due to the equivalent series resistance. Small I-core chokes (L_1, L_2, L_3) are included to smooth this high frequency ripple. As an example, under full load at output 1, ripple is reduced from 200 mV at C_{12} to 7 mV at C_{13}.

Undervoltage monitoring. Inclusion of an undervoltage monitor (IC_3) in the flyback converter permits repetitive

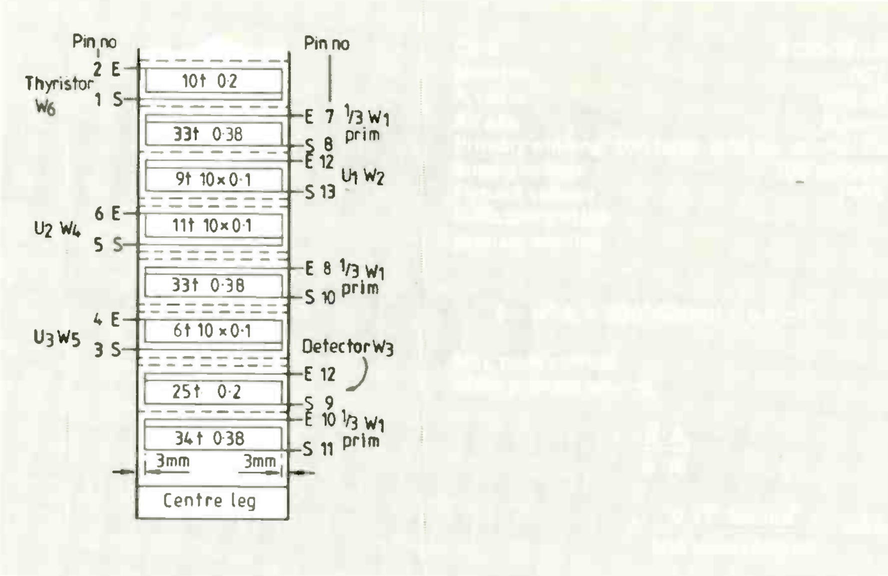
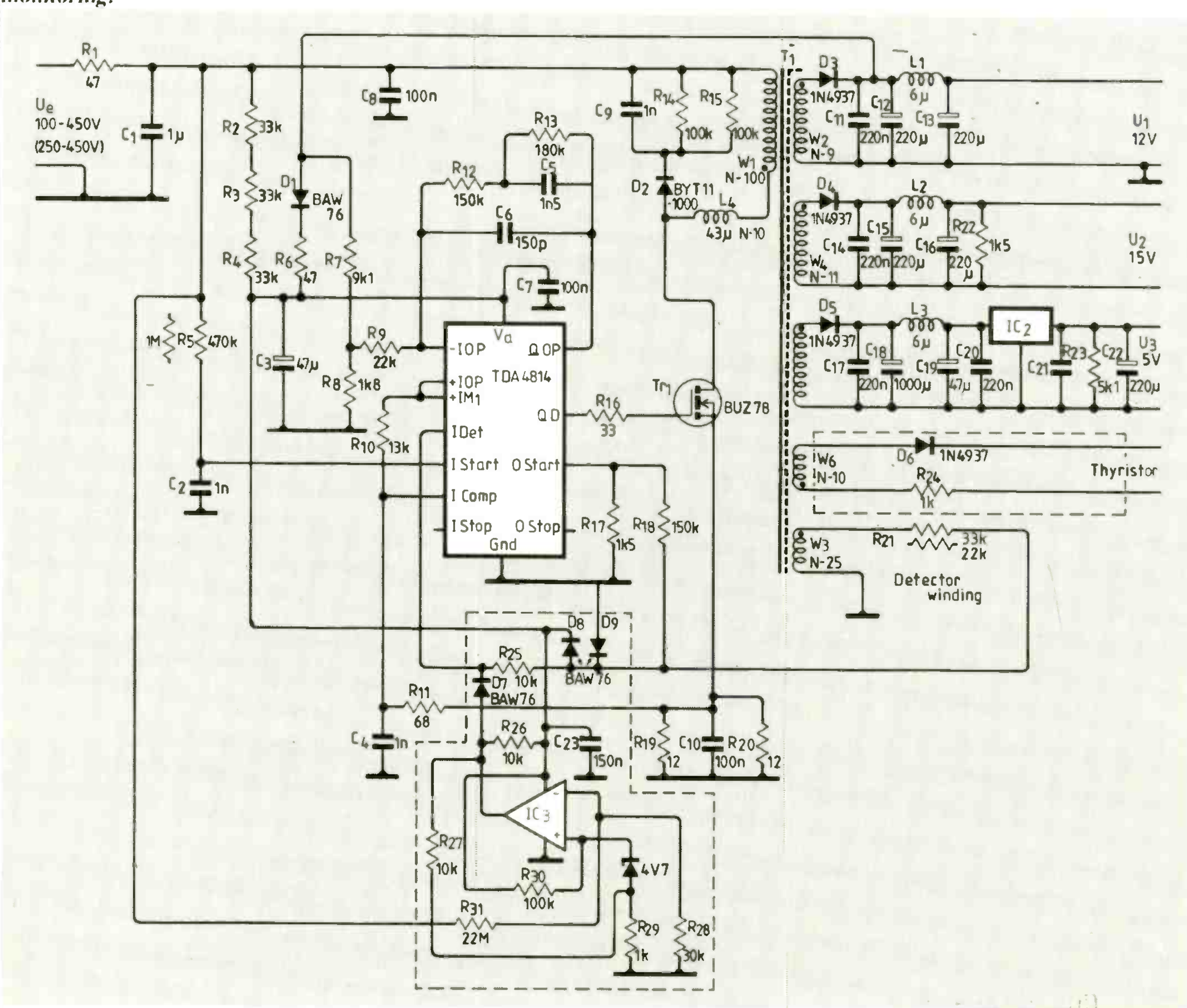


Fig. 2. Winding details of the transformer.

Fig. 1. Converter using TDA 4814 has auxiliary supply and extended supply voltage range. Shaded circuitry provides undervoltage monitoring.



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triggering of a thyristor via an additional secondary winding (W_6). The thyristor is used to bridge the on-resistance for the current-limited charging of the SMPS primary smoothing capacitor. It would be triggered after switch-on once a minimum input voltage (e.g. 250 V) has been reached. Thyristor gate current is defined by R_{24}.

The TAE 1453A is well suited as the undervoltage comparator due to its low power consumption. A small hysteresis is provided by R_{27} and R_{29}, whilst D_{10} is required as an additional reference, since the reference output of the TDA 4814 is inactive during standby. At an input level greater than 1.6V, the comparator will block switching transistor Tr_1 via the detector input of the TDA 4814.

Diodes D_8 & D_9 limit the voltage from the detector winding to the operating voltage of the TDA 4814. This ensures reliable switch-off by the undervoltage monitor under any condition at the detector winding. A low level at the comparator output will not affect the trigger voltage due to the inclusion of diode D_7.

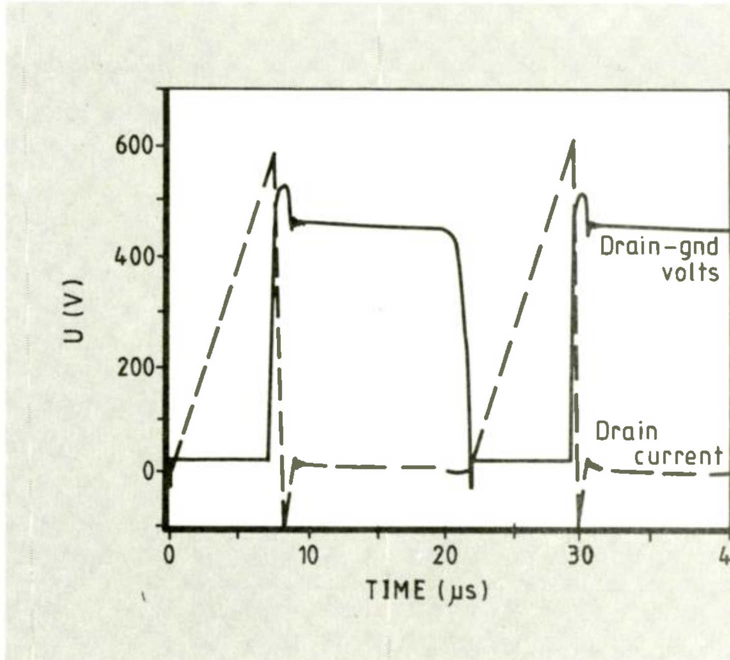


Fig.3. Transistor switching performance in full-load operation at 300V supply voltage.

Performance of the flyback converter

Use of the TDA 4814 control IC in the flyback converter shows a reliable performance under all supply voltage and load conditions (**Fig. 3**). Good coupling of the windings by interleaving is indicated by excellent individual control characteristics, despite the need for creepage paths of a minimum of 5 mm. Continuous operation up to 300 V input is possible with the inclusion of base load resistors (R_{22}, R_{23}). At higher input voltages and with no further change in base load, intermittent duty will occur during which the output voltages will remain within given tolerances.

The function of the base load is to limit the output voltage in the no-load condition. However, the available base load is sufficiently small that with a no-load condition at output 2 and other outputs heavily loaded, the upper tolerance threshold may be exceeded. Hence, for more critical applications, an increase of the base load may become necessary. A good transformation performance is achieved when output 1 delivers at least 10% of the rated power.

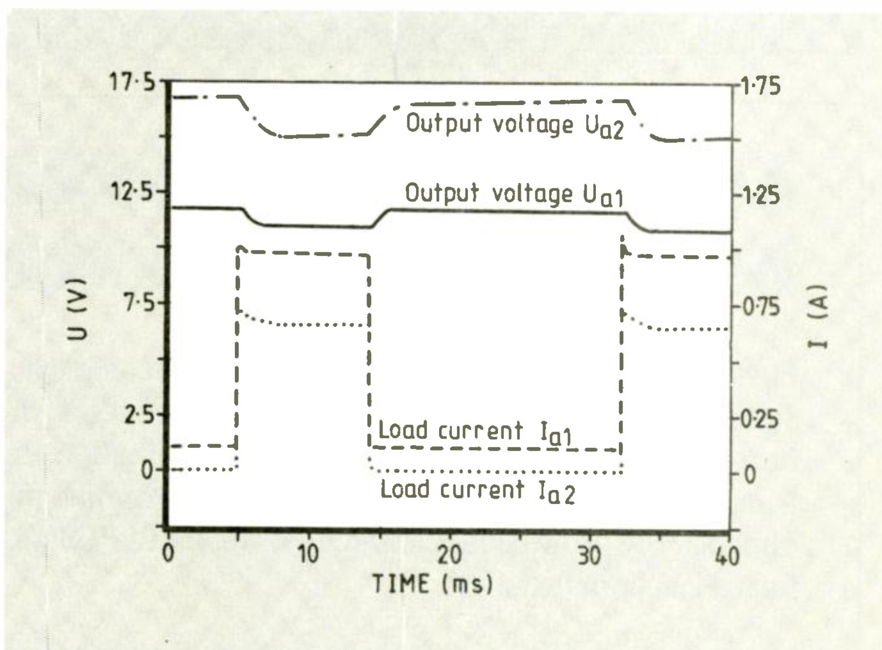


Fig.4. Dynamic performance of the converter with abrupt load changes.

The internal resistance of filter choke L_1 (0.2 ohms at 20°C) will influence the control performance of output 1. Taking the voltage directly from output 1 would clearly worsen the indirect control of the remaining outputs and produce control instabilities which may occur as a result of further phase rotation in the control circuit. By further improving the overall performance of the controller the deviation of the steady-state output could be reached during load changes. However, this has not been pursued here as the dynamic performance would be greatly affected by abrupt load changes.

These two application circuits demonstrate how versatile auxiliary power supplies can be built at low cost. ■

The authors are both with Siemens Ltd Electronics Components Group.

Remote sensing from space

By the turn of the century, remote-sensing satellites could well eclipse comsats in their importance to the growing global community. Jeremy Cavanagh describes sensing techniques which are providing information about the Earth on a scale not previously possible.

Space-based remote sensing has its origins in military reconnaissance, weather forecasting and the Gemini-Apollo space programmes. Early in the space age, the military in America and the USSR recognized the potential for spying upon one another from space. So today we have secret Shuttle payloads, public debate over the UK Government's attempted Zircon programme and veiled boasts that such satellites can read a car number plate from 200 miles or so up. More useful was the deployment of cameras, from 1960 on, to photograph the Earth's weather, so revolutionizing forecasting. Finally, beautiful full colour photographs of the Earth's surface were taken from space during the first Gemini space missions and followed by the Apollo mission's 'Planet Earth in a void' photos.

The detail and colour of these photographs awakened people to the potential of looking at Earth from space. Space-based remote sensing now has applications in pollution control, agriculture, resource assessment, climatology, land use, archaeology and oceanography.

What is sensed?

Several frequency bands in the visible and infrared spectrum are available, together with microwave frequencies (Table 1). Using the visible and infra-red spectrum depends upon the Earth's being a 'black-body' radiator. A black body emits all the energy it absorbs (emissivity = 1). The Earth emits energy received from the Sun, also a 'black body'.

The wavelength at which the maximum energy is emitted depends on the temperature of the body. This is found from Wien's displacement law, $\lambda_{max} = a/T$. For the Earth this is approximately 10μm at 288K surface temperature, which is in the thermal infra-red band.

Planck's radiation law E = hf gives the relationship for emission of radiation (E is the radiant energy and f its frequency; h is Planck's constant). This equation for all wavelengths emitted per unit area translates to $E = T^4 \sigma$ W/m.

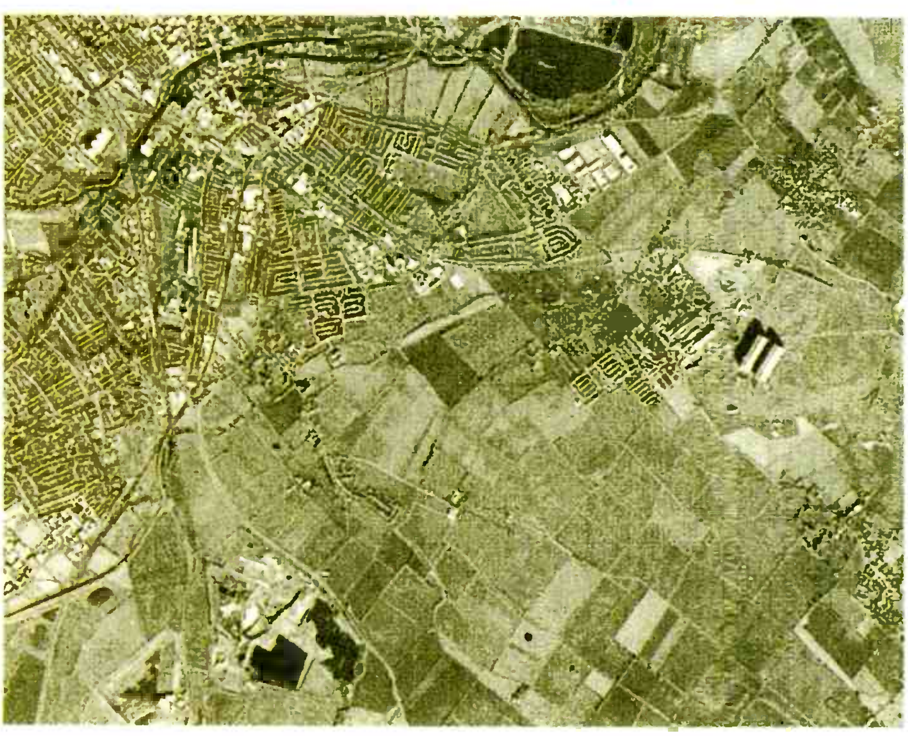
However, not all wavelengths of visible to far infra-red pass through the Earth's atmosphere: different gases absorb different wavelengths.

- Oxygen (O_2 and O) absorbs wavelengths shorter than 0.1 μm while ozone absorbs wavelengths from 0.1 to 0.3μm and 0.32 to 0.36μm.
- Carbon dioxide absorbs at 2.5μm, 4.5μm and 15μm.
- Water absorbs at 0.6, 2, 3 and 6μm. So sensors used in remote sensing are designed to 'look' between these bands.

Orbits

You want to have the opportunity to gather information from anywhere on the globe. Two orbits allow this, the first being the geostationary orbit of 36 000km distance. From this height, a sensor such as a camera can image a large amount of the Earth's sphere, which the satellite faces 24 hours a day. Changes across large areas of the Earth's surface can be followed and the extent and impact seen as fast as the data can be transmitted received and processed. This is particularly valuable for weather satellites. The ESA Meteosat weather satellite, operated by the Eumetsat organisation, has scanners operating in the visible to thermal infra-red bands and a sensor for water vapour. It can image weather patterns 55° north and south of the Equator.

The second orbit is the near-polar orbit which, at a height ranging from



Above: London and the Thames estuary, in false colour (Landsat thematic mapper). Left: Bedford and the giant airship hangars at Cardington (Spot image, 10m resolution). Previous page: Gulf of Suez (Landsat); width represented is about 90km.

Table 2. Some remote sensing satellites – current and planned.

Satellite	Country	Launch	Orbit	Applications
Landsat 5	USA	1984	Near-polar*	Land use, vegetation, geology, geomorphology, hydrology
Landsat 6	USA	1993	Near-polar*	
SPOT	France	1986	Near-polar*	Land use, agriculture, cartography, exploration
Meteosat 2	ESA	1981	Geostationary	Meteorology, environment, vegetation
Insat 1	India	1B-1982	Geostationary	Meteorology, communications, direct broadcast
Meteor series	USSR	From 1969	Geostationary	Meteorology
Space Shuttle Imaging Radar (SIRB)	USA	1984	Low Earth Orbit	Geology, geomorphology, soils, land use, oceanography
Radarsat	Canada	1993?	Near-polar	Ice monitoring, land applications
ERS1	ESA	1990	Near-polar	Meteorology, oceanography, land applications, climatology and environment, marine biology, land and sea ice
Columbus Polar Orbiter Platform	ESA	1993-4?	Near-polar*	Meteorology, climatology, pollution and environment, ocean ice, ocean colour, land use, search and rescue, precise positioning, space plasma, solar research, oceanography, land use, astronomy, materials science

* Sun-synchronous orbit

500 to 1500km above the Earth's surface, allows swaths to be scanned in far greater detail than is possible from the geostationary orbit. If the satellite is carrying passive sensors operating in the visible to near infrared portion of the spectrum then a sun-synchronous polar orbit is desired. In this orbit the satellite maintains the same angle to the Sun over a particular part of the Earth's surface all the time. So Landsat 5 always crosses the Equator at about 9.30a.m. local time and northern latitudes around 10.00a.m. The polar orbit allows the satellite to re-scan the same spot on the Earth's surface every 18 days, giving an opportunity to note changes on a regular basis. Landsat 4 and 5 were designed with an attitude-pointing accuracy of 0.01° and a stability of 10^{-6} degrees per second.

Sensors

In remote sensing, two types of sensors are used: passive and active.

The most widely-used passive sensing instrument to date has been the scanning radiometer. This consists of a single detector and a scanning mirror. The mirror scans the field of view and focuses radiation on to the detector. The mirror's scan represents a line consisting of pixels the size of the detector. An image is built up by the forward motion of the satellite.

Different detectors are used for different bands. Hence the Landsat series used a multi-spectral scanner by which five bands were imaged. The scanning mirror would focus the radiation on to a point and then that light was split up and conveyed by light-pipe to the appropriate detector for each band; 64 levels of grey were allowed for, with a grey-scale reference built in at the end of the mirror's movement. Similar are the thematic mapper and the Nimbus-7 coastal zone colour scanner.

Charge-coupled devices have been used on the French Spot-1 (CNES) satellite since its launch in 1986. Known as HRV (high resolution visible), the sensor package consists of two sensors constructed of 15 000 CCD elements each set out as three 3000-element arrays for three bands and one 6000 array for a fourth band. The CCDs are limited to operating in the visible and near infra-red spectrum. In panchromatic mode the ground resolution is 10×10m with a 60km field of view, giving great resolution. For multi-spectral mode, the two sensor packages are operated together giving a ground resolution of 20×20m. CCDs do not suffer from the noise caused in scanning

radiometers by oscillations in the movement of the scanning mirror across the field of view. However, thermal and unshielded radiation noise can affect the image.

Active scanners. Microwave radar techniques are coming into wider use with the employment of synthetic aperture radar (SAR). Radar is not affected, of course, by bad weather over the Earth's surface.

The back-scattered return depends on factors such as the dielectric of the surface (e.g. wet or dry soil), the roughness or texture of the surface and its angle in relation to the pulse transmitted.

To achieve a ground resolution of 25×25 metres, SAR uses two techniques. A very short radar pulse is transmitted for resolution along a (typically) 100km swath. The forward motion over the ground of the satellite synthesizes a much larger antenna than the satellite carries. SAR is side-looking radar, i.e. it does not look under the spacecraft straight down to the Earth's surface, but *off-nadir* to the side of the spacecraft.

Remote sensing by active microwave sensors is already eclipsing passive scanners for oceanography and future European satellites such as ERS-1 (ESA L-1989/90) are concentrating on microwave techniques. The difficulties in using an imaging SAR radar are the extremely high data rates (approximately 100Mbit/s) and the need to process this data in real time. This calls for the development of a SAR processor for use on board the spacecraft.

Thetford and the Little Ouse, on the Norfolk-Suffolk border. This and the other Spot image are copyright of the Centre National d'Etudes Spatiales (CNES) – see panel opposite.

Other active scanners based on radar techniques used on remote-sensing satellites are

- The scanning multichannel microwave radiometer flown on Seasat (1978) and the Nimbus-7 weather satellite. The SMMR can measure the temperature of the ocean surface. Seasat, operating for only four months in 1978, generated so much data about the ocean wave motion and its global effects that it is still being analysed today.
- The radar altimeter operates at Ku band and uses a 20μs pulse to obtain precise measurements of the altitude of a satellite plus information about the Earth's surface.
- The Active Microwave Instrument intended for use on ESA's ERS-1 (1990) operates at 5.3GHz using vertical polar-

Table 1. Satellite sensors and their capabilities.

Sensor	Mode	Band	Resolution (m)	Data rate (Mbit/s)	Quantization (levels)	Ground swath width, km
Thematic mapper	Passive	7: visible to infra-red	30	80.34	256	185
Multi-spectral scanner	Passive	4: visible to Infra-red	82	15	64	185
HRV	Passive	4: visible to near Infra-red	20	25	256 (DPCM)	60
SAR	Active	Ka to L	25	100	–	
AMI SAR	Active	6.3GHz	30/100			80-100

ization for two modes: SAR image and SAR wave, for detailed monitoring of ocean areas including mapping and the spectral analysis of ocean waves, mapping of ocean/sea ice boundaries and the imaging of land surfaces.

These sensors concentrate on imaging wide swaths of the Earth's surface. However, of increasing importance is vertical sounding of the atmosphere. NOAA weather satellites carry a high resolution infra-red radiation sounder; a stratospheric sounding unit; a microwave sounding unit; and an Earth radiation budget sensor. These are used to increase our knowledge of the structure and mechanism of the Earth's atmosphere, which is of vital importance to our understanding of the 'greenhouse effect'. It was a weather satellite that first detected the depletion of ozone over the Antarctic.

Data transmission

A scanner on a satellite can generate a huge amount of data. For example the thematic mapper generates 277Mbyte of data per scene at 256 levels per pixel and seven bands! This has to be transmitted, received and stored multiplied by the number of scenes taken per day over a particular country. Spot (see Table 2) makes use of DPCM for reducing the rate of data transmitted — 25Mbit/s for its HRV in panchromatic mode.

The TM was carried on Landsat in a low Earth orbit so that it was possible to access the satellite from the ground only for relatively short periods of each day. If a particular organization needed information from Landsat then it could rely on its country's Landsat receiving station (there are 17 around the world) or it could buy the data from the commercial organization Eosat in the USA. However NASA has deployed its TDRSS communication satellites at 41°W and 171°W respectively in geostationary orbit to access almost in real time the data transmitted from Landsat.

This huge amount of data generates problems in storage and processing. In Britain this is carried out by the National Remote Sensing Centre at Farnborough, which makes its services available on a commercial basis.

Image processing

Organizations can buy raw data or take advantage of facilities at the NRSC to look for particular items of interest. Large organizations such as mining concerns, universities, or Government bodies may have their own systems for processing and using data. Among the image-processing systems run by the NRSC are Gems, an interactive system using 'Gemstone' algorithms for image analysis. Also used is the LS-10 image processing system which is microcomputer based and not as extensive.

Three techniques can be applied to raw data from a satellite to arrive at the information wanted. The first two are to compensate for distortions introduced by the satellite system.

Geometric distortions are due to the spacecraft's imperfect movement and orbit. Pitch, roll and yaw of the spacecraft, and changes in altitude and velocity affect 'fitting' the image to existing cartographic information. This involves modelling the spacecraft's orbit and backing this up with measurements of the spacecraft's position. Data from such sensors as Spot's HRV is suitable for 1:50000 scale maps with 40-metre contours as Spot can produce stereoscopic images.

Radiometric distortions are more complex because they depend on scene and sensor. For example Spot's HRV sensor package has a vertical stripe occurring seven pixels 'down' the image, of about 3% in brightness variation on both sensors. HRV-1 also has less spatial resolution than HRV-2. This can be dealt with in a straightforward manner because it is readily quantifiable. Other effects may be less easy to deal with: for example, haze or sub-pixel sized clouds affecting brightness, which need an estimation of their effect and occurrence.

Processing is pixel-based. Some of the techniques are

- image enhancement, involving contrast and edge-correction. Further enhancing takes in spatial and directional filtering of the data numbers making up the image. This takes the frequency spectra of the information to identify detail in an otherwise uniform image segment or scene. Such details can then be highlighted for display on a monitor, allowing the operator to pick out such items as dried-out river beds;
- density slicing, where pixels in one or more bands are identified as being close in value or density. So pixels representing water bodies may all be assigned a colour;
- enhancing areas of interest such as a stretch of vegetation and bare soil by taking ratios of different wavelengths that have a more consistent variation for vegetation than for soil;
- principal components analysis, a technique for finding a set of variables from the image data that are independent of each other. These components are separated out for display on a colour monitor.
- multispectral classification, which makes use of the differing reflectance curves of different surfaces having each a separate reflectance curve according to the spectral band of the sensor used.

The emphasis in developing interactive processing systems is on GIS (geographic information systems). In the form of an interactive data base, GIS combines space and aerial remote sensing data with ground truth and historical information, all fitted to cartographic data.

The future

More and more countries are setting up their own RS programmes as planning of resources becomes dependent on the multi-level knowledge RS can provide. This is shown by the numbers of countries building or planning their own RS satellites; Japan, Brazil, India, China. Canada is planning Radarsat for sea/ice studies; Britain, having maintained a consistent effort in such matters pulled out of this project after participating in the planning stages. In Europe, ERS-1 is being planned for 1990, while the ambitious Columbus space platform is being designed with every conceivable sensor device for both Earth and space remote-sensing in time for the year 2000. ■

Photographs for this feature were kindly supplied by Nigel Press Associates, of Edenbridge, Kent. The NPA group specializes in acquisition, digital image processing, interpretation and mapping from satellite imagery for environmental and resource surveys. NPA is the UK representative of Spot Image SA. Further information from NPA on 0732-865023.

NPA

The author wishes to acknowledge the information and time given by personnel from the NRSC and Imperial College's Centre for Remote Sensing.

Precision analogue signal processing

As digital signal processing advances in speed and accuracy, ever-increasing standards are demanded from analogue systems to keep pace. Improvements are sought in device parameters such as higher CMRR, lower offset voltage and current with lower temperature coefficients, etc. These are achieved with well-thought-out circuit designs together with ingenious techniques employed during chip layout and manufacture to optimize performance to a given process.

Most analogue designers will tell you that reaching the stage of having verified the circuit performance with a Spice simulation run is the easy part; the longest and hardest task is to translate that theoretical chip into a fabricated device that measures up to expectations.

Transistor matching. Mismatching between transistors causes problems and is the result of fabrication process variations, including mask resolution, doping level non-uniformities etc. The use of large area transistors reduces these process parameter uncertainties but at the expense of silicon 'real-estate'. This compromise can be overcome by using a common centroid layout approach, a technique which can be employed in matching the transistors of a long-tail pair to minimize input offset voltage. Instead of simply two BJTs, four are laid out symmetrically, as shown in **Figure 1**. Opposite pairs are paralleled so that diffusion gradients across the chip and also thermal gradients tend to be equal in both halves of the long-tail pair; the effects then cancel.

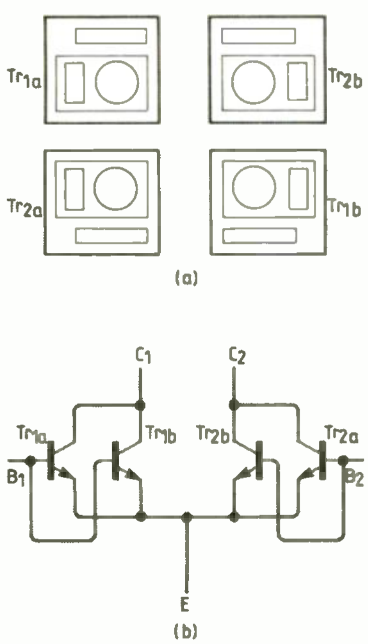


Fig. 1. Matching techniques for BJTs: (a) common centroid layout; (b) paralleling transistors to create a well matched long-tail pair.

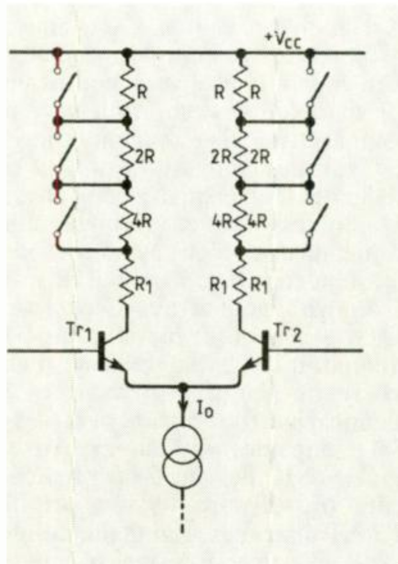


Fig. 2. On-chip resistor trimming of long-tail pair loads.

On-chip resistor trimming. Linear analogue designs rely almost exclusively on the linear current-voltage relationship of resistors. Despite their diminishing numbers in today's generation of ICs they are still an extremely important circuit element. Parameters such as closed-loop amplifier gain, CMRR of instrumentation amplifiers etc. are generally set by accurately-defined resistor ratios; and on-chip resistor trimming is an important production engineering facility needed in the manufacture of precision analogue ICs.

Two methods of resistor trimming are used, laser trimming and the selective short-circuiting or open-circuiting of trimming links in the circuit. Both techniques may be fully automated, but this individual device attention adds considerably to the chip costs. Direct laser trimming is the more accurate but more expensive method.

Manufacturers of high quality analogue products have invested heavily in developing laser trimming expertise, which forms an integral and important part of their design and manufacturing base.

The second method of on-chip trimming involves creating shorting links, using a technique called 'zener-zapping', or opening fusible links across fixed-value resistors. **Figure 2** shows the resistive load of a long-tail pair made up with a binary weighted series of resistors. Trimming is done at the wafer probing stage (as it is for laser trimming) and the offset is measured and reduced to a minimum by computer driven-signals to either short-circuit or open-circuit the trimming links.

Both of these transistor matching and resistor trimming techniques are employed in the OP-27 (PMI) op-amp, which features a typical offset of 10mV and a maximum of 25mV.

AUTOMOTIVE ELECTRONICS: WHAT'S NEXT?

The market for automotive electronics in general is only just beginning to open up, with predictions that 25% of the cost of the average car will be in electronics by the mid 1990s. This presents the designer with quite a challenge, as the environment is relatively harsh. Equipment must be able to withstand the −40°C to +125°C temperature range and not be affected by vibration or electromagnetic interference.

The wiring harness in a car has increased dramatically in size over the last decade and there always seems to be yet another accessory to add. An attractive alternative to the present wiring system, which requires a separate power line to each electrical/electronic device, fed generally via the dash-board controls, is to wire each device to a common power ring. The device is fitted with a so-called intelligent power switch that is activated only upon receipt of a uniquely coded signal, which may be sent via the power ring. Texas Instruments' development programme for a range of intelligent-power switches is nearing completion and they will be launched later this year. As always seems to be the case with new developments, the industry is not in total agreement as to the protocol to be adopted for these multiplexed wiring systems. We shall watch the debate with interest!

Flexible alternative for analogue asic

Recently Exar has revolutionized the approach to semi-custom analogue design with the introduction of its Flexar linear arrays. The concept is intriguing. The architecture of the Flexar-array is based on a cell which is repeated throughout each array in series. This permits the duplication of the circuit layout, anywhere within an array or on related arrays, with unchanged characteristics. This repeated cell structure simplifies design compared with traditional semi-custom linear arrays.

Each cell contains three 'twinsistors' flanked by two groups of resistors. The 'twinsistor' is a versatile multi-functional and multi-purpose component that can be configured, with appropriate connection of its nine contacts, into over twenty different active and passive functions including an n-p-n transistor, a p-n-p transistor, a diode, a resistor, a capacitor etc. The 'twinsistor' is a composite device comprising a dual-collector p-n-p merged with a dual-emitter, common-collector n-p-n.

In addition to the 'twinsistor' there are two other composite elements, referred to as 'padstor' and 'twinbooster'. Both are multi-functional and multi-purpose devices programmed by the particular interconnections made.

The 'padstor' is located around the perimeter of the chip and is a bonding pad merged with a five-emitter n-p-n and a large area p-n-p. Not only can it drive loads when configured as a n-p-n or p-n-p, but it can also be used as a large value capacitor for frequency compensation, a high voltage high current clamping diode and a resistor network.

The 'twinbooster' is the third element in the Flexar-array stable and this device provides high power drive capability. It has a 32-emitter n-p-n, merged with a lateral p-n-p containing four collectors and three large emitters. The 'twinbooster', not available on all Flexar-arrays, is intended for coping with high current output demands; it can handle loads of up to 500mA as an n-p-n and 25mA as a p-n-p.

There are two Flexar-arrays: the Beta series launched in 1986 and now the Delta series, with the additional benefits of thin-film resistors, Schottky diodes, easier-to-use components and higher frequency operation to 1GHz. With Delta, Exar aims to challenge full custom-design. The fast turn-round, typically six months shorter than full custom, with very low comparative development charges, low-risk designing and low unit cost make the Delta chip a strong alternative to full-custom for high-volume applications, such as automotive, consumer and disc drive markets.

As with gate-array development, when a successful module has been created, it is easy to replicate it elsewhere on the chip because of the identical matrix structure of the array. For companies without expertise in analogue IC design, Exar provides a suite of software to run on IBM PC/AT machines, giving the designer so called 'soft cell' designs of standard analogue circuits that have already been characterized and verified. Soft cells available from Exar include most analogue system blocks — op-amps, comparators, phase-locked loops, peak detectors, precision rectifiers etc. Software is also available for experienced designers to develop their own analogue circuits, with schematic capture, simulation and layout.

A further advantage of the Flexar system of semi-custom IC development is that it is perfectly feasible to design mixed-mode analogue and digital circuits on the same chip and relatively easy to do so.

Though at present Exar is the only company to offer an analogue asic facility, based on what could be termed an uncommitted linear array approach, it is likely that competitors are looking rather jealously at Exar and will be seriously reviewing ways of producing something similar!

Both the Flexar series are BJT arrays, which makes sense for many analogue applications; however it would be particularly useful to see an equivalent linear-array master-chip developed based on mosfet technology rather than BJT, since this would provide better packing density and compatibility with so many of the recent developments in digital electronics. Such a device would be ideally suited for mixed-mode analogue and digital applications.

Do vertical p-n-ps indicate a BJT revival?

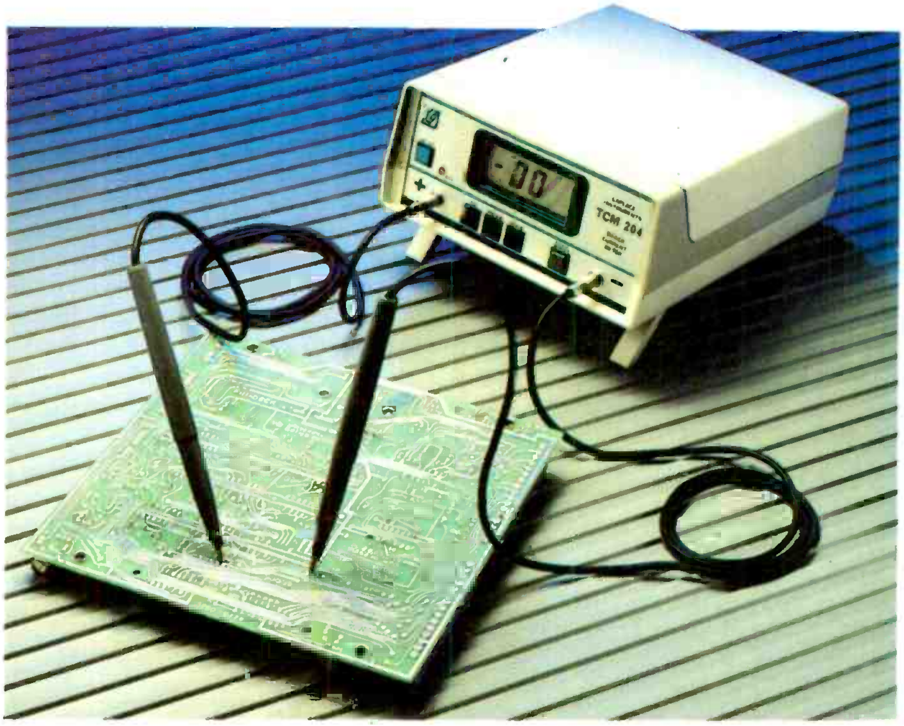
Discrete designs with BJTs became so much more versatile with the availability of complementary p-n-p and n-p-n devices. Unfortunately, IC processes are predominantly either p-n-p or n-p-n, with n-p-n devices preferred because of their higher frequency performance due to the higher mobility of electrons in silicon than of holes. On a p-type silicon slice, principally intended for vertical n-p-n devices, p-n-ps are realized as lateral transistors; inherent in this structure is a device with poor β and f_T. This imbalance between the performance of n-p-n and p-n-p transistors has led designers into using convoluted tricks to keep the signal path to n-p-n transistors so as not to degrade performance. However, it is undoubtedly true that IC design would be much simpler and better if p-n-p transistors were available with comparable performance to n-p-ns.

Several manufacturers, including PMI, Texas Instruments and Analog Devices, have reported technical developments enabling isolated high-performance vertical p-n-p to be realized on a P-type silicon slice. This gives the designer the freedom to use elegant complementary n-p-n and p-n-p structures previously possible only in discrete circuit designs. Although this is a relatively recent development, several new devices are already appearing on the market that make use of this new freedom to use symmetrical complementary topologies, such as the new CLC401 current-feedback op-amp from Comlinear.

So much of what is new in electronics is driven by semiconductor process developments. The consequences of this particular advance herald a BJT renaissance, and we shall soon see a range of new analogue circuit designs coming forward that exploit this development to the full.

Analogue Action is written by Dr John Lidgey of Oxford Polytechnic.

Non-destructive PCB current test



An outstanding piece of electronics design has resulted in a non-destructive method of current measurement in a PCB track. An instrument based on the technique will measure current in the range 1mA to 1A without breaking a track or lifting a component leg as demanded by conventional measurement methods.

The Track Current Meter, designed by the small British company Laplace Instruments, uses a combination of special measurement probes, chopping differential amplification and current nulling to determine current flow irrespective of conductor thickness.

The meter comprises two basic circuit sections: an highly sensitive DC amplifier measuring the voltage drop along a section of PCB track due to the current flowing in the conductor under test; a reference current generator controlled by the output of the DC amplifier which injects a current of a magnitude and direction sufficient to cancel out exactly the voltage drop measured in the conductor. The instrument provides a readout of the mirror current which is equal and opposite to the current flowing in the track.

While the operating principle is as simple as it is novel, the measurement of DC potentials in the microvolt range has required some ingenuity on the part of the designer, David Mawdsley. The instrument requires twin contact electrode probes. An inner spring-loaded point measures potential while an outer fixed point provides the current injection. Successful measurement also requires a combination of polarity chopping followed by an averaging circuit. It is worth noting that the instrument allows equipment under test to remain fully operational and that current measurements are unaffected by current flowing in adjacent tracks.

David Mawdsley's company intends to sell the TCM-204 for £485.

Cellular explosion

A report published by *The Economist* Intelligence Unit says the growth in the cellular market has exceeded even the most optimistic forecasts: 1988 saw a total of 500 000 subscribers to the cellular networks generating a gross income of £600 million. The Unit goes on to predict that the subscriber base will triple to 1.5 million by 1992, creating a billion pound industry.

The report, entitled Retail Business Special Market Survey, says that cellular will face increasing competition from other systems such as telepoint and radio paging. It claims that radio pagers have already caught on as a cheap method of alerting people, possibly with a simple message passing facility. It predicts two million users by 1995 rising from an existing base of 600 000.

The report sums up with an assertion that current systems and equipment will be obsolete by the end of the century, being replaced by integrated fax, voice and data transmission terminals.

A computer called horse

It is now possible to buy a multiprocessor system off the shelf using a system based on VME running Unix V. Called Equus, the prototype was developed by harnessing four Vitesse graphics systems from Cambridge Microcomputers with a rack of twelve 68030 processor cards. An ethernet link connects these to six Sun workstations and four Sun file-servers providing a standard interface to the system.

Equus is an operating system environment which runs computationally intensive applications across any number of distributed parallel processors. At its simplest, it allows the user to add extra processors into a single processor computer.

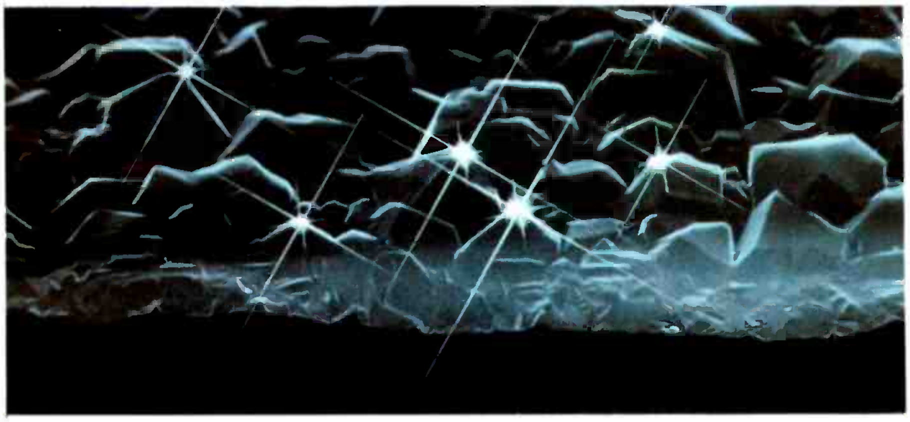
The system uses dynamic reallocation of resources while the program is running. The designers claim this to be a significant departure from transputer-based systems which cannot allow reconfiguration.

Diamond window on the world

Researchers from Plessey's Caswell facility have developed a process to manufacture diamond film in layers over two inches diameter and 5μm thickness.

The synthetic diamond layer makes a durable and transparent window for IR detection in missile targeting systems and burglar alarms operating in the 0.4 to 12μm region. According to the workers involved in the development of the process, the polycrystalline layer offers superior transmission properties to natural diamond because it produces less scatter than a single crystal.

Manufacture involves the deposition of carbon from low-pressure methane gas plasma at temperatures below 800°C, a very low temperature in comparison to those normally employed in the manufacture of synthetic diamond. The individual crystals measure in the region of 2 to 3μm.



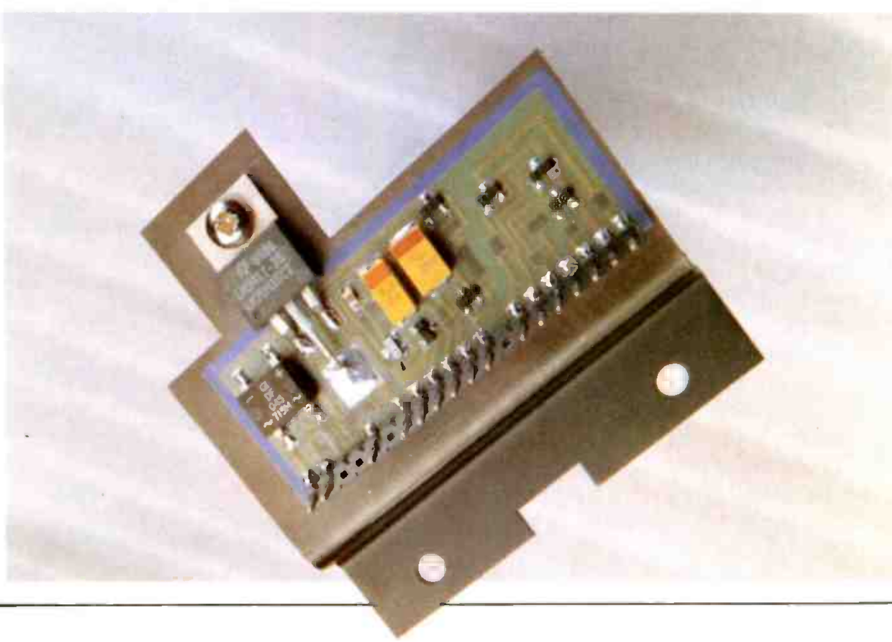
Semiconductors on steel

A hybrid production process developed by the comms chip manufacturer Mitel uses stainless steel as the substrate medium. It offers all the benefits of the traditional ceramic based product but has the added advantages of heat dissipation, strength and electromagnetic shielding, says the company.

Mitel says that the key to the technology is a dielectric material which matches the steel substrate to the thick film ink system.

Hybrid thin film circuits can now be built with multiple layers of circuit connect using a new fabrication process from AT&T.

The process uses successive layers of polymer laid down on a conventional ceramic substrate which also acts as a thermal header. Each layer can contain a mix of standard thin film elements such as tantalum nitride resistors, fabricated capacitors and inductors. The increased amount of interconnect – based on gold – allows a much improved packing density. The low-loss dielectric makes the process suitable for microwave and high frequency applications.



Calling the

According to its designers, the Northern Ireland Fire Brigade's new computerized call-out system is the most advanced in Britain and possibly in the world. From a central control room in Lisburn, County Down, operators can despatch staff and resources to incidents occuring anywhere in the province's 5200 square miles. At present, the brigade responds to more than 25 000 incidents per year, ranging from house and factory fires to road accidents and the occasional terrorist episode. Altogether, 59 fire stations and their vehicles are linked to the system, by telephone, private wire and VHF or UHF radio. Data communications are the dominant means of passing information to fire stations, but voice channels are available simultaneously over the private wire and radio circuits.

At the brigade's headquarters, the operators who receive alarm calls from the public are supported by a 350Mbyte gazetteer of the province. With this, fires can be located accurately from the incomplete or garbled details given by an over-excited caller, or even from the number of a telephone call-box alone. When there is any doubt, the software offers a list of sound-alike addresses

fire brigade

Seen here is one of the control positions at Northern Ireland Fire Brigade's headquarters at Lisburn. Equal opportunities note: the giant wall-map status display, part of which is visible at top right, has 5000 lamps. All of them were wired up in the space of four days by a man with only one arm. He did his own cable-forming.

from which the operator can select the most probable. Also available on-screen is the Harwell chemical database: firefighters tackling a chemical spillage can receive directly from it a print-out of the special information they need. Touch-screen controls are extensively used, for rapid operation without mistakes.

Two Data General Eclipse minicomputers manage the system (one is on stand-by) and there is a third for training purposes. Two "shadow" control rooms are available in case the main one has to be evacuated. The system was designed and installed by International Aeradio (IAL), a subsidiary of British Telecom. IAL's next project of this kind, an even bigger one, will be in operation shortly – a call-out system for the London ambulance service.

Personal cell-phone

Motorola's pocket-sized 9800X is the smallest cellular radiotelephone yet. Though it weighs only 305g (including a slimline NiCd battery pack) it offers features to match much larger models. Among them is a facility to recall stored telephone numbers using names.

Channels covered include the full ETACS assignments, and the unit can be registered on both UK networks at once. RF power output is 0.6W and a continuous talk time of 30 minutes is possible (or 75 minutes with the standard battery, which brings the weight up to 350g). A range of accessories includes a car fixing kit and a mains power unit.

Within the 9800X, all main components are mounted on a single printed circuit board – RF components on one side, logic and audio on the other. A metal interlayer provides an isolating screen. The display is an alphanumeric led type: Motorola doesn't consider its relatively heavy power consumption a problem since for most of the time it is blanked. Some 80% of the semiconductor devices are special types sourced by Motorola itself.

The telephone will be available this year in versions for all 900MHz analogue cellular systems; the British model is ready now and carries a price tag of £2295.

RS-232 multimeter

A five-digit multimeter from Fluke can be used under computer control using a built-in RS-232 interface. It accepts ASCII commands, interpreted by internal rom, which can control range, functions and calibration. A standard PC could be used to provide full remote control of multimeter function.

An optional software package allows the instrument to be incorporated into an automated testing environment. Captured data can be transferred into standard PC applications packages such as dBase or Lotus 1-2-3. The RS-232 port can also be used to address an external printer for hard copy.

The model 45 multimeter provides all the conventional multimeter functions. Additionally it has a dual display enabling comparative testing to be made. It costs £459.

LCD digitizing tablet

The Japanese company Mitsubishi has combined an LCD display with a touch-sensitive panel to create a self-indicating digitizing tablet. The screen/tablet comprises an array of 640×400 pixels spread over an area 230×145mm.

Working with a pressure stylus, the operator can display images as they are digitized. An external computer connects to the unit by a standard RS-232 port.

World's fastest synthesizer?

This is what Lyons Instruments claims for a direct digital synthesizer manufactured by the US company Sciteq. It says that the unit will hop over a bandwidth of 300MHz in less than 20ns, maintaining phase-continuous switching.

Based on GaAs technology, it uses a central clock running at 640MHz to produce a frequency range of DC to 300MHz with a resolution of just under 10Hz. The specification indicates a phase noise of −105dBc/Hz at 100Hz offset when running at an output frequency of 150MHz.

Hermetic optics

Hughes Aircraft has developed a hermetic packaging technique for optical fibre pigtails. The fibre lead-in uses a multi-layer jacket produced by first coating the silica fibre with aluminium as the fibre is being drawn. The aluminium layer then receives coatings of nickel and gold to aid the soldering process.

DIY PLD

Brian J. Frost concludes his introduction to programmable logic devices with a design example and a look at PLD design tools.

As an actual design example, consider a simple four-bit binary up-counter. The design equations are easy to appreciate once the basic rule of operation of the counter is clear. There are two rules for counting, which for an up-counter are

1. The least-significant bit must toggle on each clock.

2. Higher bits must toggle only if the bits are lower order are all 1, otherwise they must remain unchanged.

From rule 1, implementing the least-significant bit is simply a question of changing the pal D-type flip-flop operation into a T-type, or toggling, flip-flop. If the Q output of the flip-flop is connected back to its D input it will toggle on each clock pulse and since we have this feedback into the array, this provides our bit 0 of the counter. We usually need a reset facility as well, so the equation for this bit 0 would read

q0.d = !reset & q0;

Here the D input to the flip-flop for this bit is signified by the extension ".d" to the actual output pin name "q_0", and that the state of the actual output pin is used as an input on the right. Thus if Reset is not true, each new output state after a clock pulse will be the inverse of the last state. Should Reset go true, it takes precedence and sets the D input to 0, thus clearing the flip-flop to the reset condition on the next clock.

From rule 2, the next higher bit, bit 1, must toggle only when bit 0 is a 1. Control over this toggling is achieved by presenting its D input with either its own output (so it does not change) or its own output inverted (so that it *does* toggle). The decision for this "toggle or not" is based on the state of the previous bit, q_0. This control over an inversion is conveniently represented by the exclusive-Or function which can be expanded into Ands and Ors if required. Here we shall let the logic compiler do the expansion for us and use the symbol $ for the exclusive-Or function. Thus the definition for q_1 becomes

q1.d = !reset & (q0 $ q1);

For bits 2 and 3, the principle is identical and their equations just add another term each time:

q2.d = !reset & ((q0 & q1) $ q2);
q3.d = !reset & ((q0 & q1 & q2) $ q3);

Note that Reset has appeared in all equations.

PLDs – WHY YOU SHOULD BOTHER

Programmable logic devices are set to move into areas where conventional logic has seemed inviolate, and although traditional logic families are likely to exist for many years yet, the developing PLD technology will be regarded by more and more designers as the less painful solution to their design problems once their initial learning phase is complete. The wider acceptance of such devices that follows this learning will fuel in turn the generation by manufacturers of ever more innovative PLD products and design tools.

From this sequence it might seem that we could go on adding more bits to the counter very easily, but a limitation arises from the number of product terms to which each equation expands. When compiled for the basic pals, each bit in a binary counter will require one product term per control function (e.g. Reset, Preset, Hold etc.) plus a number of product terms equal to the binary order plus 1, limiting the popular pals to around eight bits. This limitation can be avoided either by using special pals that have exclusive-Or gates available placed before the D-type flip-flop, or by partitioning the counter into several shorter counters and interlinking them via a "count enable" signal.

The philosophy behind this example of a simple binary up-counter is applicable to all counter designs, and a down-counter can be designed just as easily by reversing rule 2.

However simple the principles I have just outlined, a justifiable comment is that to create a simple counter in this manner seems rather more painful than just picking a readily available TTL part. But because counting is so common a requirement, a number of example counter designs are supplied with any logic compiler and it is more usual to modify one of these examples to your requirements than to create a new design each time from the ground up. The reward of a PLD-based counter design is the ease with which one can incorporate additional features over those found in the TTL standard designs; for example, counters with control inputs that allow them to shift their contents left or right as well as count. This is the area where pals become particularly useful, since many of the complex MSI/LSI functions with high numbers in the TTL range turn out to need extra signal conditioning logic before they can be used within your application. A PLD can be programmed to provide just the signal polarity that you require and becomes even more attractive when pins need to be re-arranged to suit a PCB layout.

For those like myself who can exist for really quite a long time without feeling the need to write a boolean equation, ways have been developed in which high-level syntax can be used with common logic compilers to express these counting operations in a much more direct way by regarding counting as one defined sequence of a state machine.

State machines

A state machine is any logic system that proceeds through a defined sequence of states under the influence of external inputs, its previous state, and a clock. Much software executes in this way, with its sequential instruction-controlled flow and its programmability working together to provide a very flexible tool.

A logic-based state machine can provide the same level of flexibility as a software routine but at a much higher speed where the control "branching" is performed not by software testing of input bits, but by logic states that follow sequences dependent upon inputs at the time the sequencer was clocked.

As an example of the application of a PLD-based state machine, a very high-speed data acquisition system may require an A-to-D converter to have its result awaited, transferred into local ram followed by an auto-increment on to the next address and a re-triggering of the A-to-D for the next measurement. Cycle rates below 1μs would not be possible using a software technique, yet a logic state machine can be programmed from a list of the A-to-D control signals (trigger, busy, read, chip select etc.) and the memory control lines to issue these in a fixed sequence at very high speed. A clock of 50MHz would not be excessive.

Because of the usefulness of state machines for counting and sequencing applications, many logic compilers provide syntax for their definition. The CUPL notation is

```
PRESENT name__of__present__state
IF input__1__true
   NEXT name__of__state__P
IF input__2__true
   NEXT name__of__state__Q
```

One can see the similarity to the If...Then expressions of high-level languages.

To see how easy this makes the expression of a counter design, **Fig.10** shows a decade counter with control inputs for up, down and clear, and with a carry output.

The design starts with declaring the pin numbers to use for inputs and outputs together with their names and polarities. Then follows a definition section where each state of the 10 possible counts is given a name (S_0, $S_1 \ldots S_9$) and the the names Up, Down and Clear are defined.

The actual design is in the Sequence statement where each "present" state is shown leading to one of (in this case) three possible "next" states, corresponding to incrementing, decrementing or clearing the counter.

How much TTL to replace

Deciding on partitioning – where a design needs to be split up into smaller logical blocks – can be difficult. And perversely, the flexibility of PLDs can make it more so. With traditional TTL design, circuitry grew around the available parts; and partitioning concerned only which parts of the design were to be split on to other circuit cards within a card frame.

With PLDs, partitioning is not only about fitting a larger design into more than one device, but it is important not to lose the PLD's flexibility in so doing. For example, consider a simulated, proven design which fully occupies one 16L8 pal, i.e. all 10 inputs and eight outputs are used. A decision, based on whether any further features are likely

```
/**  Inputs  **/

pin 1          = clk;        /* Counter clock          */
pin 2          = clr;        /* Counter clear input    */
pin 3          = dir;        /* Counter direction input */
pin 11         = !oe;        /* Register output enable  */

/**  Outputs  **/

pin [14..17] = [Q3..0];      /* Counter outputs        */
pin 18 = carry;              /* Ripple carry out       */

/** Declarations and intermediate variable definitions **/

field count = [Q3..0];       /* declare counter bit field */
$define S0 'b'0000           /* define counter states */
$define S1 'b'0001
$define S2 'b'0010
$define S3 'b'0011
$define S4 'b'0100
$define S5 'b'0101
$define S6 'b'0110
$define S7 'b'0111
$define S8 'b'1000
$define S9 'b'1001

field mode = [clr,dir];      /* declare mode control field */
up = mode:0;                 /* define count up mode */
down = mode:1;               /* define count down mode */
clear = mode:[2..3];         /* define count clear mode */

/** Logic Equations **/

sequence count {             /* free running counter */

present S0     if up           next S1;
               if down         next S9;
               if clear   next S0;
present S1     if up           next S2;
               if down         next S0;
               if clear   next S0;
present S2     if up           next S3;
               if down         next S1;
               if clear   next S0;
present S3     if up           next S4;
               if down         next S2;
               if clear   next S0;
present S4     if up           next S5;
               if down         next S3;
               if clear   next S0;
present S5     if up           next S6;
               if down         next S4;
               if clear   next S0;
present S6     if up           next S7;
               if down         next S5;
               if clear   next S0;
present S7     if up           next S8;
               if down         next S6;
               if clear   next S0;
present S8     if up           next S9;
               if down         next S7;
               if clear   next S0;
present S9     if up      next S0;
               if down         next S8;
               if clear   next S0;
               out  carry;         /* assert carry output */
```

Fig. 10. Configuring a decade counter. This one has a carry output and three control inputs – up, down and clear.

to be required, must be made as to whether this implementation of the design is satisfactory, since if additional outputs are required, the resulting additional IC would display a modification no more attractive than a TTL design. Further outputs can be added by using a larger pal device – for example the 24-pin 20L10 with 10 outputs – and leaving the extra two unconnected.

Another solution is to lay out a PCB to take a 24-pin 0.3 inch wide package with V_{cc} to pin 24, to earth pin 12 as if for the larger pal devices, but then to earth pin 10. This footprint will accommodate either 20-pin or 24-pin pals with no PCB modification and with only one lost input on the larger device.

Designs often require more than just a few extra pins on one device. A good designer will partition a PLD design such that not only are uncommitted inputs and outputs available within each of the several PLDs, but that logic functions are grouped within each PLD so as to minimize interconnections and to contain the "domino effect" of any future changes to the design within as few PLDs as possible. Such a reduction of the interconnections between the PLDs is well repaid, not only through a tidier design, but because each interconnecting link frees two PLD pins. Consideration must also be given to the end use of the design: for example, a prototype system should offer many more spare connections than a final, tested design aimed at minimizing cost.

Larger counter designs eat up the available architecture of PLDs because the higher order count bits require more product terms (Ors) than the device has. In this case if a PLD with larger internal organization is not feasible the counter design will need to be split between devices.

One technique which sometimes pays off is to make sure that you have spare TTL functions available which the pal cannot provide. For example, a combinatorial pal is supplemented with an external uncommitted flip-flop that can be roped in should it be required, ensuring that Murphy is frustrated at an early stage in the design.

Interestingly, software techniques can provide pointers toward good PLD partitioning. There are a number of parallels between a well-structured, modular piece of software and a well-partitioned PLD design. Good software has individual modules (each PLD) with well controlled parameters (signals in and out) without complicating cross-linking and changes in the main flow (such as Goto).

Fortunately, as with software writing, any partitioned design – however inelegant – will function once debugged, and the experience that defines your own future partitioning rules is quickly achieved. The choice of PLDs is then wide: number of devices, their size, number of pins, power consumption, technology and of course cost.

As with microprocessor programming, having the right tools makes for efficient use of PLDs. PLDs are now almost universally designed using software tools and programmed on specific hardware. Both merit a closer examination.

Software design tools

The early days of programmable logic were often spent with a dedicated programmer box which applied the necessary programming voltages to one specific type of part and where the device program was often entered using manual switches. Although apparently cost-effective, this approach was only acceptable for devices with a small number of bits to be programmed and it could still lead to errors in programming. Even then, the user still had to code his logic requirements into the bits to be programmed, further increasing the risk of incorrectly translating the equations into fuses to be blown.

A few years ago, software tools began emerging which would accept a simple document file written with the required PLD logic equations and, acting much like any other software language compiler, would translate these equations together with a knowledge of the intended PLD into the bits that required programming. This had the advantage that the user could specify names for pins, vastly increasing the readability and documentation of a design as well as allowing a fast-turn-around to minor changes.

Today, these software packages fall into three basic categories:

1. Shareware. Several manufacturers have developed software that supports their devices and in some case also supports general architectures, so allowing its wider application. Examples are AMD/MMI's "PALASM" and Signetic's "AMAZE", which are available for basically the cost of the discs. The quality of such software is quite high and offers many of the facilities of the traditional up-market CAD packages.

2. Non-specific general purpose logic CAD software. To cover as many as possible of the PLDs in the marketplace, several software packages cover a wide choice of devices, for example CUPL and ABEL (see the reference list last month for more details). The libraries of these packages are regularly updated with new designs as they become available, and their relatively high cost is attributed to features such as power-

PLDs – THE FUTURE

Programmable logic devices have a very bright future. Many popular devices have been with us for a long time, but their volume of use is increasing rapidly; most general distributors' catalogues now include them.

At the same time, manufacturers of conventional logic families have realised that there will come a time when users choose a PLD route for their design and therefore they need to be positioned ready to offer in that market. As a result, several alliances have now been formed between high-volume logic semiconductor manufacturers and the often smaller, more innovative PLD manufacturers. The programmable logic marketplace is likely to become much more competitive.

The greatest potential would seem to be for UV or electrically erasable devices which are rapidly increasing in their internal density. This increasing capacity benefits the user in two ways. Firstly, new device configurations can be designed that are very flexible in the logic functions that they replace: for example, registers can be buried within the device, freeing pins for i/o tasks. Secondly, devices can be designed as "supersets" of existing smaller fixed architecture parts. As an example of the latter, one device that is gaining much present popularity is the 16V8. This 20-pin device, usually electrically erasable, can be programmed to act as one of 20 or more dedicated pal devices; i.e. it can mimic combinational or registered pals including devices that have mixed outputs (16R4 etc). It does this by offering a programmable output cell on each output pin that is defined when the programming equipment loads the type of device to be used, allowing users with existing pal logic designs to use the 16V8 with no modification. Marketed as Generic Array Logic, or GAL, it adds another buzzword to the logic vocabulary.

For the future it seems likely that within two or three years PLDs will evolve into standard larger architectures and grow until they reach, and pass, the complexity level at which ASICs were being offered some two or three years ago. This will allow whole PCBs of conventional logic to be replaced by just one PLD; and it will be then that design verification techniques such as logic simulation learnt now on the simpler PLDs will return the greatest rewards.

Another area showing significant growth is that of PLDs designed specifically around certain functions that end-users tend to repeat often. As an example, the new IBM Microchannel bus architecture used in the

ful logic minimization, "hot-line" support, thorough simulation etc. Many packages also incorporate conversion utilities enabling designs made using other software to be converted.

3. Other manufacturer-specific software. Some PLDs with newer architectures are so specific that their manufacturers have written software dedicated to them which exploits the advantages inherent in their design. In many cases (PLD sequencers for example) this software is also available as shareware at low or zero cost. In other cases the manufacturer has chosen to incorporate software intended to aid the user in entering his requirements, for example where devices from the TTL family can be specified: the software then converts these to the PLD design.

Some software packages permit the graphical entry of TTL components in circuit diagram form, and so present a very friendly user interface. This diagram is then converted into logic equations by the software and on into a fuse map for the intended PLD. Whilst this is an excellent process for straightforward designs, remember that there is no substitute for an understanding of the processes involved in fitting the design to the PLD, and that you will certainly need such an understanding should problems occur.

In all case though, the eventual output is a JEDEC file that contains information in the form that can be read by the device programming equipment.

Programming equipment

Many devices for programming PLDs are on the market and on the surface they appear similar to eprom programmers. Indeed their task is a related one, to set individual bits in the device being programmed to states as defined by a downloaded pattern file.

Unlike eproms though, PLDs differ widely in pin connections, programming algorithms and technology; and this forces many manufacturers to dedicate an item of programming equipment exclusively to certain types of PLD. One reason for this is that bipolar pals (such as the 16L8) and other devices based on fuse technology can require up to 0.5A to fracture the fuses in a manner guaranteed to meet the manufacturer's specification. By contrast, the erasable PLDs now appearing use eprom and earom technology in c-mos where the programming process requires raised pin voltages that must be restricted in their slew rates to avoid the risk of c-mos latch-up. The significant difference in programming electronics that this demands has led to lower cost programmers designed either for "pal programming" (probably bipolar fuse types) and "EPLD programming" (the newer erasable types). This makes it very important to examine their specification in detail to establish which devices they *cannot* program, since this limitation may not be discovered until later.

Several manufacturers specialize in "universal programmers". These are sophisticated devices that are designed to handle PLDs with a wide range of pin voltage, current and slew-rate requirements and which are configured internally to suit the specified device. Such equipment usually handles eproms, eprom-based microprocessors and proms as well.

Which tools are best?

Unfortunately the answer to this question is not a simple one, since your particular requirements reduce the options available.

None of the tools currently available, however full of windows, menus and circuit diagrams, releases the end user from the need to understand the basic principles involved, and there will always be a need for an adequate understanding of how your design is actually overlaid on the architecture of a given device. Although this understanding is only fully tested when errors are reported to you by a software or programming process, it does help you to avoid creating errors in the first place.

Software that allows schematic entry does tend to look very attractive since the circuit diagram concept is immediately recognizable to the user; but be aware that unless the error reporting incorporates really positive suggestions about curing problems – almost to the extent of doing it for you – you are still not spared the basic learning curve. As a result, regard such software for what it is – a convenient "front end" for user entry.

If you have no previous experience of PLDs, or equipment or tools for handling them, the need for a learning curve makes the low-cost shareware approach quite adequate as a starting point. PALASM from AMD/MMI for example, is available from several distributors for under £20 and supports all the common pal devices. But it has enough features to allow you to decide more objectively on purchasing a more comprehensive software package (such as CUPL or ABEL) once your needs are clearer.

Again, the cost of programming hardware can be kept low with the purchase of a programmer that is designed only for simple pal devices. Straightforward programmers designed for serial connection to a PC are readily available for under £400. ■

latest PCs requires significantly more interaction between the main processor and an expansion card that uses the bus. Several manufacturers such as Altera have tailored PLDs to Microchannel bus applications where the PLD contains "hard" non-programmable circuitry that implements the defined bus functions and registers but also contains "soft" programmable features such as decoder outputs, interrupts and handshakes that the end user can customize to his own use. In this way not only are many traditional ICs saved, but so too is the effect of designing-in quite complex bus specifications.

Other PLDs with a bright future are those designed for sequencing. These can be thought of as similar to a reduced instruction set processor, but with very little memory: they are designed to perform small but fast sequencer loops to control a subsystem of logic. The common requirement for counting, jumping and testing at speeds in excess of software capability has resulted in several manufacturers offering PLDs that are specifically designed to be flexible in this mode, and often come with their own assemblers and software tools.

Another example of a PLD device that is increasing in popularity is the logic cell array, or LCA, manufactured by AMD. This device is an array of configurable logic blocks, each one containing some combinatorial logic, a flip-flop and control logic. A PLD design using this device is based on programming the required logic within the blocks and also the routeing used to connect signals from input pins, through logic blocks and out again. The flexibility of this architecture comes from the ease with which logic can be cascaded without using valuable package pins, so "burying" logic within the device. There is an increase in propagation delay using this technique, since the internconnection is performed using relatively high-resistance silicon "wires" instead of metal, but development is concentrating on minimizing this.

An interesting development for the future is that of devices that can be programmed in-circuit. This relatively new concept relies on equipment that can connect to one or two reserved device pins and load a fuse map into the PLD using a serial technique. As well as being a useful prototyping aid, this has the advantage that devices can be flow-soldered with the other PCB components without having yet been programmed. It also allows PCB devices to be field-upgraded without the need to design them into sockets.

ACTIVE

ASIC

C-mos arrays. Three new members of the HDC family of 1 micron arrays are the HDC003, 006 and 011, offering 3000, 6000, 11 000 gates respectively The HDC technology allows over 70% gate use Its channel-less sea-of-gates architecture offers 300ps delays (with a fan-out of two), combined with unprecedented I O counts in minimal chip dimensions Motorola, 0296 395252

A-to-D and D-to-A converters

16 channel A-to-D-to-A 12 bit converter. The PC-30A plug-in board for the IBM PC provides both A-to-D and D-to-A conversion with a conversion time of less than 1 microsecond, plus parallel I O and a timer The 12 bit A-to-D converter and 16 channel multiplexer has a typical conversion time of 35 microseconds A sample-and-hold circuit is used between the multiplexer and the converter Amplicon Electronics 0273 5700220

Eight-bit, 200Msample/s flash converter. The monolithic AD770 provides an eight-bit output at 200Msample/s with 250MHz full-power and 400MHz small-signal bandwidths, which allow low-distortion sampling of 100MHz Nyquist-frequency signals Additional benefits include accurate sampling of high-frequency signals without an external sample/hold, fast settling when a high-speed external sample/hold is used and sampling of signals beyond the Nyquist frequency Analog Devices, 0932 253320

Data acquisition board. The DT2809, an IBM PC XT AT-compatible data-acquisition board can measure the outputs of eight different sensors or transducers within 20ns of one another, and is capable of 16-bit resolution (±% accuracy) The analogue-to-digital converter performs a calibration each time the board is powered up Data Translation, 0734 793838

Eight-bit D-to-A converter. The Plessey Semiconductors 8-bit D-to-A converter (ZN438) has input latches to facilitate updating from a data bus and a buffer amplifier to give low analogue output impedance Other features include a 1 25 microsecond settling time to ±½ LSB, trimmable 2 5V bandgap reference, microprocessor TTL and 5V c-mos compatibility and commercial and military temperature ranges RR Electronics 0234 270272

Discrete active devices

Tuning diodes. MSI Electronics announces its High Q surface-mount and stripline packaged single-chip and back-to-back abrupt-type tuning diodes. Minimum reverse voltage is 31V and they are available with a 4V capacitance from 1 8pF to 100pF The 2C3113A series Q values are from 1000 to 125 Elyon Electronics 0883 47916

Linear integrated circuits

Bipolar op-amp. The AD708 dual bipolar op-amp features 25 microvolt maximum offset voltage and 0 3 microvolt per degree Celsius maximum offset voltage drift Maximum offset voltages and drifts are matched to within 25 microvolts and 0 3 microvolts per degree Celsius respectively Analog Devices, 0932 25320

Fast current-feedback op-amp. The PMI OP-260 offers slew rates of 1000V/microsecond at unity gain, 500V/microsecond at a gain of 10, and draws a supply current of only 4 5mA per amplifier Bandwidth is 90MHz Current-loop amplifiers are used in exactly the same way as voltage-feedback amplifiers, but offer major performance advantages Jermyn Distribution, 0732 450144

Hybrid dip VCO. Vectron model VC-373 is a non-crystal-controlled, voltage-controlled oscillator providing a TTL output at any centre frequency in the 1MHz to 90MHz range; HCMOS output is available up to 40MHz Deviation is ±10% standard with octave deviation optional Linearity is ±10% Lyons Instruments 0992 467151

Memory chips

ASIC memory. PUMA II is an asic ceramic memory which can carry flash prom, eeprom, UV eprom and static ram and be configured by the user to provide up to four megabits of memory in 8 16 or 32-bit wide words Memory configurations are changed through "select" pins which enable users to access each of the 32-pad sites in any order by using the chip-select pins as address lines Hybrid Memory Products 091-258 0690

C-mos 64K prom. The CY7C266 by Cypress Semiconductor is a high-speed, low-power c-mos 64K prom that offers standard eprom pinout With a maximum access time of 55ns the CY7C266 dissipates 440mW, which drops to 35mW when deselected The device is arranged as 8192×8bit and is housed in a choice of packages which can be equipped with an erasure window Pronto Electronic Systems 01-554 6222

CD-rom. Digital's RRD40 Compact Disc rom stores up to 600Mbyte on a 12cm platter and is available in table-top form for SCSI and Q-bus systems or as an embedded unit for SCSI systems Access time averages 0 5 seconds and the standard Philips/Sony data format is employed Rapid Recall, 0494 457388

Optical devices

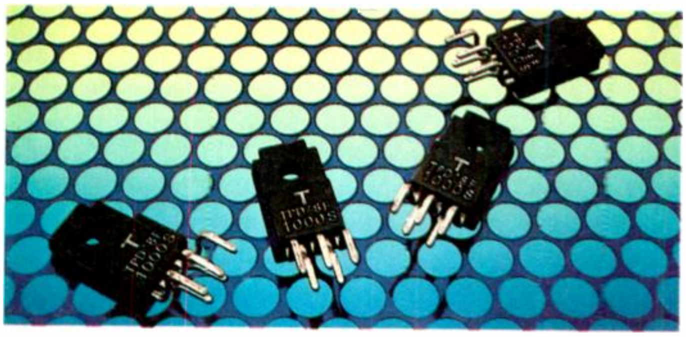
Infra-red emitter. The TSIP 5201 has a viewing angle of 40 and offers 520mW SR of radiant intensity when driven with a 1 5A pulse of 100 microseconds duration Spectrally matched to silicon photo-transistors and photo-diodes, the device has a wavelength of 950nm AEG (UK) Ltd, 0753 872120

Retro opto switches. The VTR22 series of devices consist of a gallium arsenide led with a phototransistor or photodarlington so mounted that each optical axis is perpendicular to the face of the retro package A retro opto switch normally sees no light when an object passes within the device's field of view the infra-red from the led is reflected back to the photodetector Pacer Components 0491 873077

Power semiconductors

Intelligent power device. The TPD1000S is a high-current monolithic power IC which has the control IC and vertical output mosfet on a single chip It features a high-sided power mosfet output switch for grounded loads The TPD1000S has a V_{DS} of 60V, and I_F of 4A and a $R_{DS(on)}$ of 0 22Ω Typical operating current is 2mA at 12V and microprocessor drive compatability is assured Toshiba Electronics, 0276 694600

TPD 1000S smart power from Toshiba



PASSIVE EQUIPMENT

Passive components

Standard size, SM mica capacitor. This retains the advantages of mica over NPO ceramic, with the added benefit of SMT Two package sizes SM01 7 3×1 4mm and SM02 7 3×5 8mm, line up with industry-standard landscape sizes for tantalum chip capacitors Height above the board is 2 8 and 3 5mm respectively A capacitance range of 4pF up to 2000pF is made in voltages between 63 and 1000V DC Ashcroft Technology, 0493 853957

Surface-mount trimmer pots. The TRG042 series of cermet trimmer potentiometers by Tocos is designed for surface mounting The resistance of the devices, which measure 3 8×4 5×2 2mm, ranges from 500Ω to 500kΩ and they have a resistance tolerance of ±30%. Mechanical travel is 250 and maximum operating torque is 300gcm BDL 06285 30607

Leadless electrolytic capacitor. The NAC series of leadless, surface-mounted, cylindrical electrolytic capacitors are available in preferred values from 0 1 to 220µF with working voltages from 4 0 to 50V DC and an operational temperature range from −40 to +105 C The series is packaged in a cylindrical aluminium casing measuring only 4×6mm for values from 0 1 to 47µF, and 6 3×6mm for values between 4 7 and 220µF Bowmar Instrument, 0932 851341

Metallized-film capacitors. Panasonic has two new ranges of miniaturized film capacitors: the ECQ-B series polyester film/foil and the ECQ-V series stacked metallized film capacitors At 63V DC, the two ranges together offer a range of 0 0001 to 1 0µF HB Electronics, 0204 386361

Interference-suppression capacitors. Metallized-paper capacitors by RIFA are intended for use in across the line (X1 and X2) and line to earth (Y) applications, especially where high pulse voltages of more than 1 2kV can be experienced The PME 271E range offers capacitance values from 0.01µF to 0 22µF and are rated at 300V AC (X1) RIFA-EVOX (UK) Ltd, 0203 653100

Low-voltage electrolytics. Two ranges of low-voltage electrolytic capacitors, the EKR and EKX series have been designed for use in switched-mode power supplies Both series are polarized, radial-leaded devices and are available in values from 10 to 2200µF Voltage ratings of 10, 16, 25 40 or 63V DC can be specified, and the capacitors have particularly low impedance over the frequency range 10-100KHz Steatite Roederstein, 021-643 6888

RF attenuators. A range of high-power RF attenuators, covering the 0-2 5GHz frequency band is available in standard attenuation values of 3 to 60dB at 12 to 20W They are available with type "N" connectors – Model 8212 or "BNC" connectors – Model 8211 Impedance is 50Ω Telonic Instruments, 0628 73933

Connectors and cabling

Capacitor collet sockets. A complete line of open-frame capacitor sockets for devices with 0 3in (7 62mm), 0 4in (10 16mm), and 0 6in (15 24mm) row-to-row pitch gives a choice of either 0 1µF or 0 33µF capacitor as standard The use of capacitor sockets is a protection against momentary voltage surges, and eliminates the need for a separate capacitor on the PC board Aries Electronics (Europe), 0908 260007

Terminal blocks. The CTB1300 series of flame-retardant, plug-in interlocking terminal blocks can be plugged flush to the PCB, either horizontally or vertically, on to the 5mm pitch pin strip. They are rated at 6A, 250V AC and accept up to 2 5mm² wires. Camden Electronics, 0727 64437

High tension connector. This 2mm touch-proof connector has a test voltage of 5kV and is rated at 15A The recommended operating temperature range is between 70 and −10 C The socket, manufactured from brass, machined and gold-plated has a deep insulating shroud giving a breakdown voltage to VDE standards of 9.5kV. Multi-Contact (UK) 01-575 7070

Displays

Graphics plasma displays. These displays consist of an AC gas-discharge plasma panel, including memory function, with bistable characteristic and driver circuitry The neon orange display is presented against a black background and provides a brightness of 110cd/m² with a contrast ratio exceeding 20 1 FPF8050HRUM features a display matrix of 640×640 dots with an effective display area of 211mm×132mm and the FPF8050HRUK, a 640×640 dot matrix unit. Fujitsu Microelectronics, 0628 76100

Instrumentation

Digital multimeter. Gold Star model DM 7241 is a 4½ digit instrument with a DC voltage accuracy of 0.05%, all ranges having full overload protection It measures alternating and direct voltage to 750V and 1000V to 10µV resolution, and alternating and direct current to 20A with a resolution of 0 1µA Resistance measurement goes from 10mΩ to 20MΩ. Alpha Electronics, 0942 873434

Digital panel meter. The DPM-8100 can be used either as a conventional voltmeter, providing AC DC amperes and volts read-out, or recalibrated to display engineering units such as height, pressure and flow rates. It provides automatic zero and polarity indications, crystal-control for noise rejection, display hold capability and true differential or single-ended input Anders Electronics, 01-388 7171

Programmable attenuator controller. A high-speed series of control processors is now available for micros in conjunction with Flann programmable attenuators and phase shifters Setting times for the attenuators of 1 2 seconds for 0-60dB and 70ms for 50-60dB are achieved Phase shifters can be repositioned from 0 to 360 in 320ms Flann Microwave Instruments, 0208 77777

Handheld multimeter. The GDM 1 11 is a 3½-digit, handheld multimeter which includes capacitance measurement as one of its eight functions The multimeter, which also includes diode testing and semiconduct h_{FE} measurements, has a basic DC accuracy of 0 5% The 29 ranges, which include DC voltage up to 1kV and DC/AC current up to 10A are selected by a single rotary control Probes are included in the purchase price of £49 95, and an optional carrying case is also available Global Specialities, 0234 217856

Digital storage oscilloscope. The SO40 25MHz microprocessor-controlled digital storage oscilloscope, which has an analogue real time display, has two input channels and a storage capacity of 4×2K or 1×8K. All four of the stored signals can be displayed simultaneously Grundig Electronic, 0911 7330-1

Clip-on ammeter. The 2000 AC is a basic, wide-range, Hall-effect instrument Designed to be hand-held, its jaws clip round a conductor to enable measurement of the current carried The design of the jaws permits current measurement on circular conductors of up to 48mm diameter or 22×60mm rectangular section. Three current ranges are provided: 0-20A, 0-200A and 0-2000A Accuracy is ±1% of range The frequency range of the instrument is 15Hz to 3kHz Heme International, 0695 20535

Digital/analogue oscilloscopes. Tektronix 2230, 2221 and 2220 are the first digital storage oscilloscopes to include non-storage measurement to 100MHz (2230) and 60MHz (2221/2220). As a DSO, the 2220 supports sample, peak-detect and average modes; the 2221 and 2230 also support accumulated peak detect. All three models have a sampling rate of 20Msample/s with 8-bit vertical resolution, and in repetitive storage mode of up to 2Gsample/s. IR Group, 0753 580000

Waveform tester. A multi-channel waveform analyser that simplifies a wide range of measurements in mechanical and electromechanical applications, the Tektronix 2510 is designed to perform complex waveform analysis. Features include record lengths to 256K points and card modular expansion up to eight acquisition channels per analyser. Additionally, a simple spreadsheet-style user interface fully integrates control of waveform acquisition, storage, analysis and data management. Tektronix UK, 06284 6000

Pen recorder. The Hioki 8601 battery-powered pen recorder offers single-channel, inkless recording on a 15m-long pressure-sensitive paper roll. The four chart speeds are 1 and 2cm/s and 1 and 6cm/minute. Zero can be positioned at any point on the 20mm wide recording paper. Seven input ranges give 100, 200 and 500mV and 1, 2, 5 and 10V full scale sensitivity. Frequency response is 80Hz and the input resistance a fixed 1MΩ. Universal Instrument Services, 0533 750123

Power Supplies

1000W power supply. Powermag A1000 is a 1000W single-output, switch-mode power supply in a 5×8×10 in standard package. Outputs include 5V, 12V, 24V and 48V DC. Advance Power Supplies, 0279 55155

DC-DC converters. A series of economically-priced miniature DC-DC converters, with both single and dual outputs, is manufactured by SCI (Semiconductor Circuits Inc.). The DPU series of single and dual-output unregulated converters offers efficiencies up to 80%; short-circuit protection; an operating range of −25°C to +71°C with no derating; and an LC input filter to reduce the reflected ripple. Pascall Electronics, 01-979 0123

DC/DC converter. Vicor "Megamodules" are compact, chassis-mounting converters available in ratings from 50-600W, which can be combined to achieve multi-kilowatt power ratings. With an operating frequency of up to 3MHz and efficient thermal packaging, the overall efficiency of the Megamodules reaches 85% and their power density is up to 27W per cubic inch, depending upon the model. Powerline Electronics, 0734 868567

Production test equipment

Component test system. A bench-top component test system, the CT1000, offers functional and parametric testing of linear components including op-amps, comparators, voltage regulators and opto-couplers. The user sets the test limits and conditions using simple menu-driven software running on the system PC which controls the instrumentation and processes the test results. Antron Electronics, 0252 737191

Radio communications products

HF/SSB transceiver. The 2230 synthesized, 100 watt HF/SSB transceiver is engineered for mobile, portable and fixed-station service in hostile, bush and desert environments. Combining keypad frequency entry with rotary-switch selection of 15 memory channels, the AEL 2230 operates in USB/LSB, CW, AM and FSK modes. The keypad may be detached from the front panel, with operation then as a conventional channellized transceiver on up to 15 spot frequencies. AEL Communications, 0293 785353

Switches and relays

Alternative to dip switches. Alfa Bridge is a low-profile, 2.54mm-pitch jumper, which can be used as a low-cost alternative to dip switches. The jumpers simply slide over a pair (or more) of pins from the unshrouded header. The pin passes through the jumper, allowing jumpers to be stacked up and cross matched. It is available in three versions, single, in-line and bus-bar, from 2 to 20 positions. Digitran, 00763 61600

Programmable waveguide switches and drivers. A series of programmable waveguide switches and drivers is designed for use in instrument, laboratory or ATE applications. The switches, with an optional 2 or 3 channel rotor, offer high repeatability and reliability. A precision stepper motor provides programmable switch positioning via a switch driver unit. Flann Microwave Instruments, 0208 77777

Metric rotary switches. Metric versions of the Grayhill Series 50/51 rotary switches have a 4mm×25mm shaft, and are rated for 200mA at 28V DC, or 150mA at 115V AC, for 25000 cycles. The Series 50 features a 36° angle of throw with up to two poles, the Series 51 a 30° angle of throw with up to four poles. Both series are available in solder-lug and PC-mount versions. Highland Electronics, 04446 45021

Sealed diaphragm switch. The Series 14S has a seal design using a membrane, which effectively excludes dust, liquids and airborne contaminants from the electrical contacts. It features ITW's registered Butterfly contact mechanism to provide high reliability and a current-carrying capability of 20A at 480V AC. The contacts themselves consist of a high mass of solid silver with a semi-refractory design. ITW Switches, 0705 694971

Heme 2000 AC clip-on current meter

Transducers and sensors

Optical transducers. Type DP500 is a series of high-resolution, non-contacting, optical panel-mounting encoders, named "Digipot". Designed to convert input rotation and direction into real-time digital data, the DP500 encoder offers extremely low torque and the ability to cope with continuous speeds up to 10 000 rev/min, providing 500 pulses per revolution to generate 14 40 code changes every full rotation. Control Transducers, 0234 217704

Load cell. The ELF-500 series of load cells from Entran could be the smallest in the world, with a diameter of 0.5in and a thickness of 0.110in. The devices are available in tension, compression or both modes and offer measuring ranges from 1lb up to 100lb. Temperature compensation covers the range of 0°C to 60°C, but can be extended. These low-deflection devices provide outputs of up to 250mV FS, measuring static or dynamic forces at frequencies to 20kHz. Entran, 0344 778848

Rotational impulse-signal emitter. Designed to convert shaft revolutions into electrical signals, the model G080 rotary impulse emitter is a small, mechanically driven electrical contactor which produces electrical impulses in accordance with the gearing arrangement between the driven shaft and the contact breaker. IVO Services, 0959 64884

Temperature transmitters. The SEM 151 series of temperature transmitters now includes 0-200°C versions as standard. The units are designed for use with two or three-wire platinum resistance detectors to BS 1904 or DIN 43760. Status Instruments, 0684 296818

COMPUTER

Computer board level products

PCBus isolated extender board. The PC-54 isolated extender board finds application in PCB development and trouble-shooting. It provides a socket on its top edge which duplicates the IBM motherboard socket, but is fully buffered from it. The bus protects the host PC while checking experimental or production boards. Amplicon Electronics, 0273 570220

PC AT frame grabber. The DT2862 arithmetic frame grabber is an IBM PC AT-compatible board that can capture, process, and store up to four 512×512×8-bit images from standard video or slow-scan devices in real time (1/25 second). It has 1Mbyte of on-board memory, a built-in 8-bit arithmetic logic unit, and high-speed data ports for direct connection to dedicated processor boards. Data Translation, 0734 793838

Data communications products

Serial communications controller. An enhanced c-mos version of the industry-standard 8530 serial communications controller that doubles the speed of the previous generation, the 85C30 is designed for use with 8- and 16-bit microprocessors. AMD (UK), 0483 740440

Arcnet network cards. The Arcnet PC communication range includes the ARC-100 Arcnet interface in both star and bus topology as well as active and passive hubs. All interface cards plug into PC/XT/AT and 386 machines and are fully compatible with Novell and other major software packages. The ARC-100 is a short card and includes a 2Kbyte multi-packet buffer with I/O address and interrupt, selectable via links. Blue Chip Technology, 0244 520222

Development and evaluation

VME I/O prototyping. Using an on-board 68000 processor, the XVME-080 and XVME-081 prototyping systems enable designers to develop application-specific I/O modules with local intelligence at reduced cost. The on-board intelligence ensures that the system processor is not overloaded in I/O-intensive applications. Dean Microsystems, 07357 5155

PC based simulator for H16. This simulator/debugger allows software for the 32-bit H16 microprocessor to be developed on an IBM PC or compatible system. The SO16SIMPC allows H16 programs to be developed, tested and debugged before any target hardware has been developed, allowing hardware and software design to progress in parallel. Hitachi Europe, 0923 246488

Interfaces

Intelligent VME analogue I/O. The BVME 650 module is a high-performance VME board, providing an intelligent DMA interface for A-to-D and D-to-A conversion. The 6U module provides 32 input and four output channels, each with 12-bit resolution. It is capable of continuous conversions through its DMA controller: either via on-board ram or via the VME system memory. BICC-VERO Electronics, 0703 266300

D-to-A and digital I/O for PCs. The DADIO, produced by Scientific Solutions, can be used in any personal computer with a standard IBM PC bus, such as the IBM PC, XT, AT, and PS/2 model 30. It contains four independent, double-buffered, 12-bit digital-to-analogue converters in addition to 24 I/O lines, which can be programmed in groups of eight. Frontline Distribution, 0256 463344

Programming hardware

Eprom programming. The XP2M supports all current 24-, 28-, 32-, and 40-pin eproms, eeproms, flash eproms and micros as standard, and has the ability, with optional add-on modules, to cover bipolar proms and pals. GP Industrial Electronics, 0752 342961

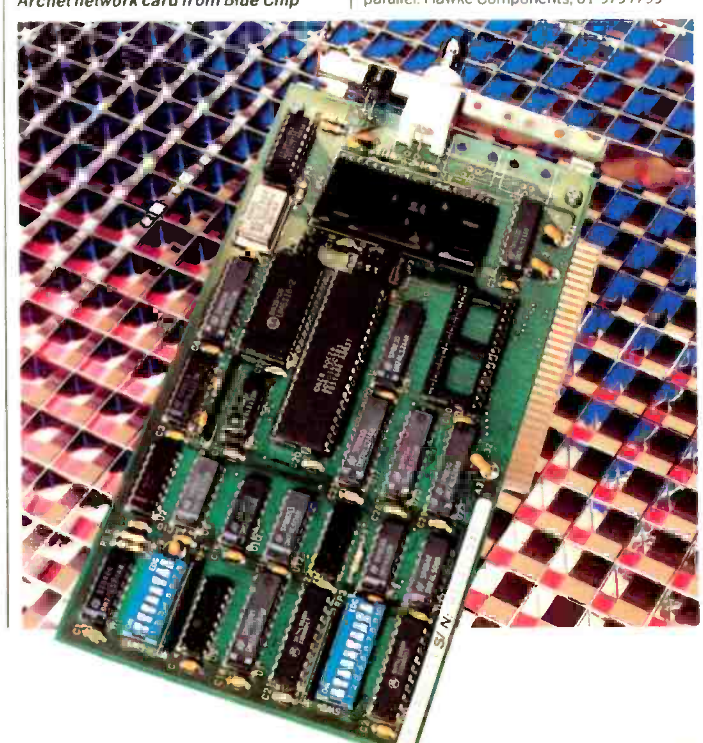
Software

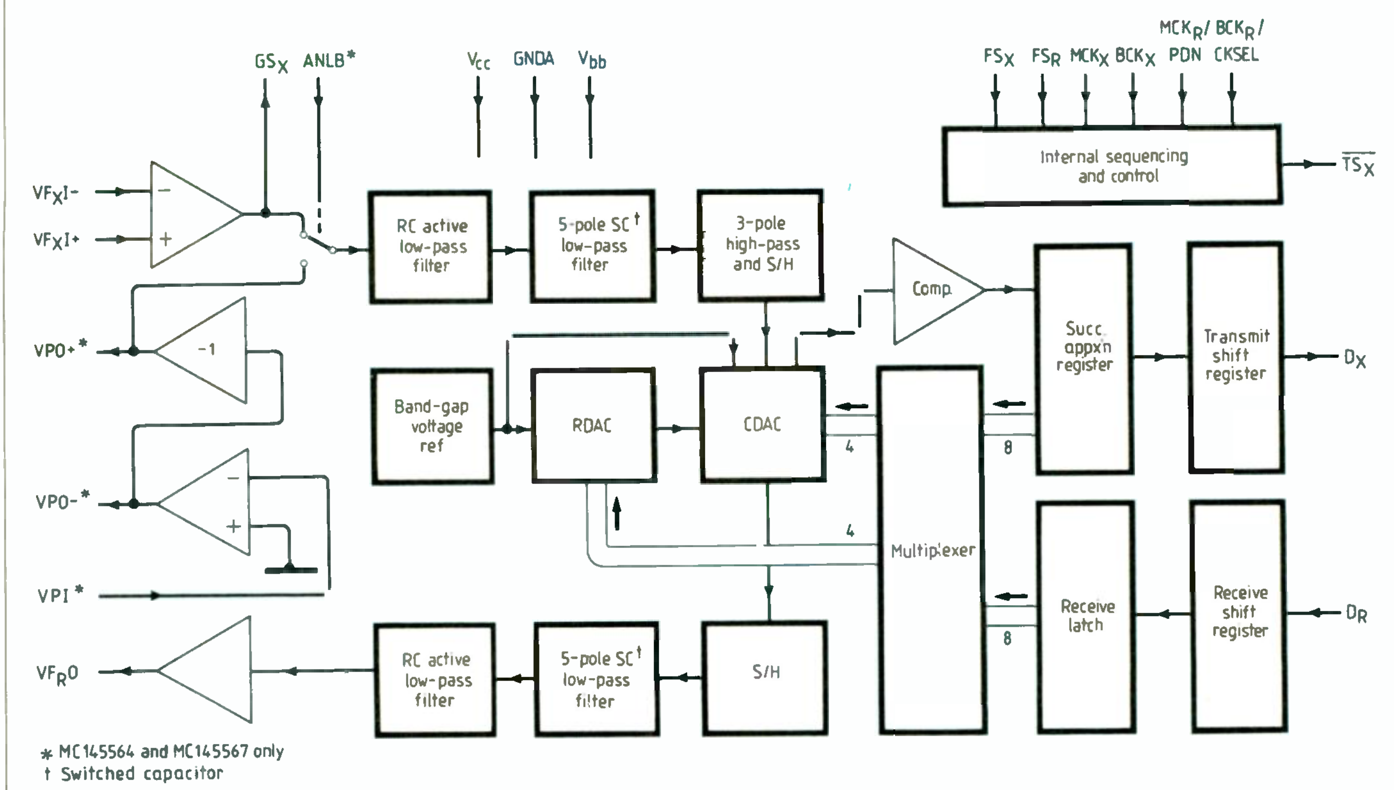
PADS-PCB design system. Version 3.0 of the PADS-PCB PC-based cad system includes many enhancements, among which are networking, high resolution, a 30% increase in autorouter speed, and advanced placement capabilities. A major advantage of Version 3 is that it enables the user to set up a single file server and library node, accessible by all micros on the network. Export Software, 0242 222307

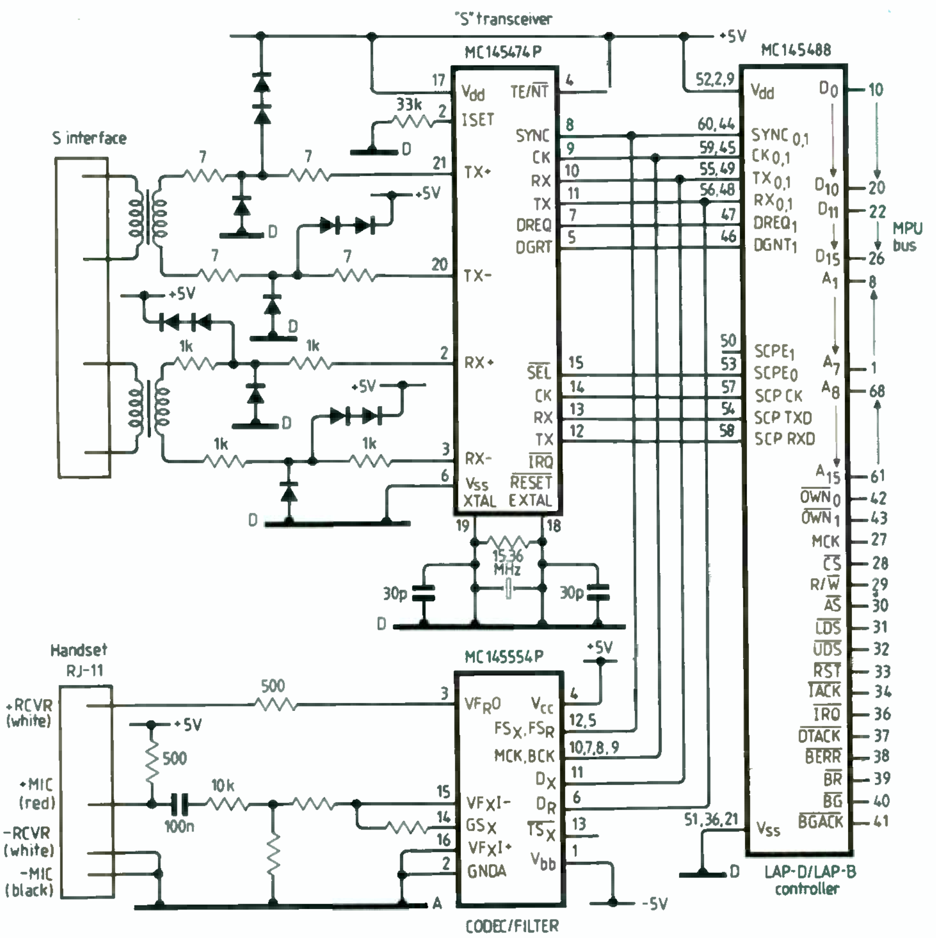
Task-oriented processors

Transputer-performance graphics. The QTVIO MicroVAX-resident graphics and image-processing module is one of the QT Series of transputer-based Q-bus subsystems which allows MicroVAX users to make full use of the transputer. Suitable for both PAL or NTSC cameras as well as PAL, NTSC or non-interlaced monitors with refresh rates of up to 60Hz, the system may be expanded to 24-bit RGB image processing by running three QTVIOs in parallel. Hawke Components, 01-979 7799

Arcnet network card from Blue Chip







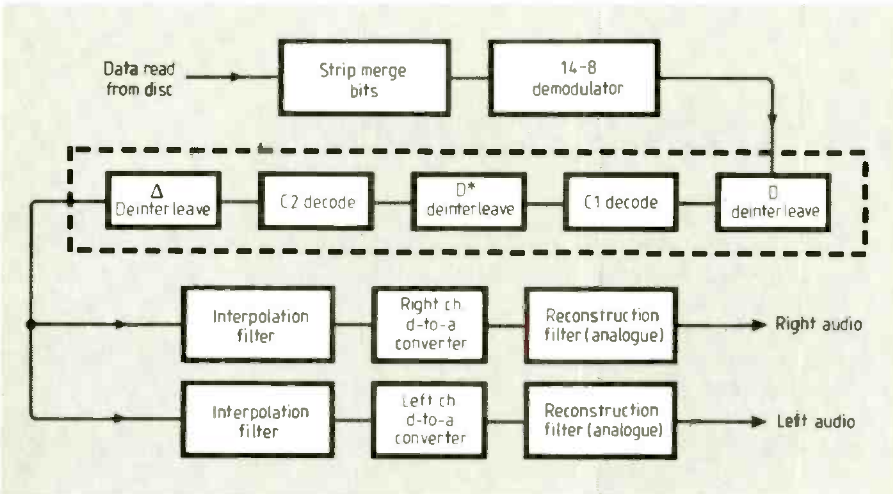
PCM codec filter

This ISDN voice/data terminal is from an advanced data sheet on Motorola's MC145554 series pulse-code modulation codec filters. Each device in the family performs voice digitization and reconstruction as well as the band limiting and smoothing required in PCM systems.

There is no specific description of this circuit in the note, but there are details of how the 145554 operates and further circuits for an ADPCM transcoder and a single-party channel unit. *Motorola, Macro Marketing, Burnham Lane, Slough, Berkshire. 06286-4422.*

Why is a compact-disc player like a satellite modem?

In an article with a title like the one above you would expect to find a fair comparison between a CD player and a satellite modem. AMD's DSPatch Newsletter No 10 contains such an article but satellite modems are hardly mentioned; the only mention comes in the last paragraph which tells you that data can be corrupted by both random and burst errors in satellite communications channels and CD pick-up systems alike.



However, details of how the CD player data system works make up for the over-adventurous title. Cross-interleave Reed-Solomon coding, data framing and oversampling are all outlined in the article. There is also a run-down of advantages that accrue from using the ADSP210 family DSP chips and a note that there is an entire section on multi-rate digital filtering in the ADSP210x Family Applications Handbook, Volume Two.

Other articles in the newsletter describe a 16bit PCM audio d-to-a converter, disk-drive head positioning using a digital signal processor and high-resolution data conversion in general. Below is an extract from the newsletter on an interesting signal/array processing system called SP20 and manufactured by Sigmet and Lassen Research. The SP20 is capable of between 20 and 400Mflops depending on its configuration so it is suitable for radar and image processing applications.

High-speed signal array processing

Signal processing has traditionally required the speed associated with hard-wired electronics which, by their nature, are inflexible, fixed-program systems. The SLR SP-20 signal/array processor takes full advantage of this technology: it has computational rates an order of magnitude higher than comparable systems, yet supports a general-purpose architecture capable of high performance in a variety of applications.

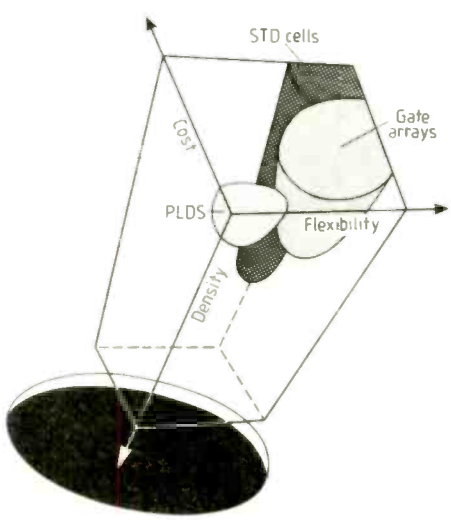
The SP-20 is designed for performing repetitive, computationally-intensive algorithms for applications such as remote sensing (e.g., radar, lidar, sonar, satellite), image processing or numerical modelling. Use of an SP-20 together with a low-cost to mid-range host computer, yields the performance of a much more expensive system.

Analog Devices, Station Avenue, Walton-on-Thames, Surrey KT12 1PF. 0932-232222.

Choosing a PGA

Suggestions on how to choose the right programmable gate array are given in AMD's brochure Programmable Gate Arrays – The Perfect Solution for the Imperfect World. Among subjects broached are cost, why user programmable devices are useful, why you should program your own devices rather than let them be programmed by the vendor, and risks and compromises associated with PGAs.

There is also a table of devices available from AMD in the brochure and notes on software, PGA design and the design cycle. *AMD, The Genesis Centre, Garrett Field, Science Park South, Birchwood, Warrington WA3 7BH. 0925 828008.*



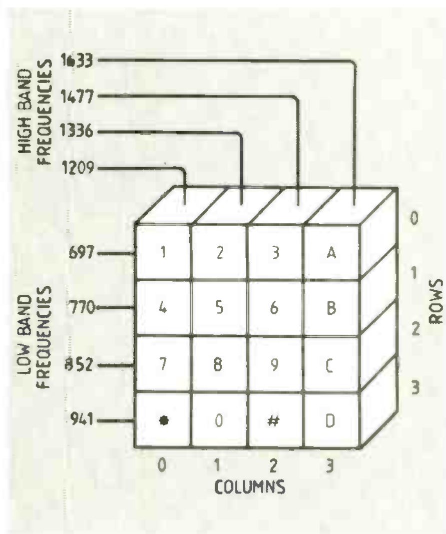
Many trade-offs exist between semicustom solutions

Dual-tone multiple frequency on a microcontroller

Assembly-language software for producing DTMF on COP820C/840C controllers is listed in Application Note 521 from National Semiconductor.

Since the 820/840 controllers only have one timer, the problem with producing DTMF on them is that three different times need to be handled – the two selected frequencies and the 100ms DTMF duration. One, or possibly two, of the timings can be handled by the timer but the remaining one or two need to be dealt with in software.

The solution described in the note consists of 78 bytes of code together with 32 bytes of look-up table. It relies on dividing the 100ms duration by the half periods for each of the eight frequencies and then examining the respective high and low-band quotients and remainders shown in the table. *National Semiconductor, The Maple, Kembrey Park, Swindon, Wiltshire SN2 6UT. 0793-614141.*



	Freq. 0.5P Hz	Half period in µs	Half period	100ms/0.5P Quotient	Remainder
Low	697	717.36	717	139	337
band	770	649.35	649	154	54
freq's	852	586.85	587	170	210
	941	531.35	531	188	172
	1209	413.56	414 (256+158)	241	226
High band	1336	374.25	374 (256+118)	267	142
freq's	1477	338.52	339 (256+83)	294	334
	1633	306.18	306 (256+50)	326	244

Statistics and anti-statistics

Is there a relationship between particle physics and politics? Just as a nuclear particle has its counterpart, an anti-particle, each statistic produced by a politician leads to the appearance of an anti-statistic, and quantum theory ensures that two statistics relating to the same subject can never be the identical.

This was evident during a debate which expressed concern at the trade deficit in electronics, and the increasing skills shortages in high technology, when Paddy Ashdown, the Democrats' leader, began to focus a beam of anti-statistics on to the Government benches.

In 1979 there was a trade surplus of 0.5% of GDP in high-technology products, which by 1989 had become a deficit of £2.19 billion. Between 1971 and 1985, out of five major OECD countries, only the UK's percentage of GDP spent on R&D dropped (from 1.8% to 1.5%, whilst civil R&D dropped from 0.73% to 0.5%); in terms of patents, the UK's share has fallen sharply (26% of all European patents in 1963; to 16% by 1985), and the UK is the only OECD country whose numbers of applications for USA patents has fallen. In terms of skills, by 1993, the UK will be short of 100 000 IT staff, and that the UK rates 17th out of the top 20 OECD countries for the number of those staying in full-time education over the age of 16 (the Japanese have 95% stay-on rate, the UK 32%); and for every 10 000 population of the top OECD countries, the UK has the fewest scientists and engineers working in R&D.

"Too selective", said the Government, which unselectively noted that recent high-tech investments by Fujitsu, Toyota and Bosch amounted to £1.2 billion. Indeed, capital investment in a high-tech industry such as chemicals was £1.4 billion, the trade surplus on electronic radars was £700 million, capital investment in IT was up by 44%, and in 1988, IBM alone added £2 billion to the positive side of the trade equation. With respect to the skills shortage, 5000 extra technical graduates would be produced by the engineering and technology programme, and YTS now has a technical component.

With so many statistics, claims and counter-claims, the hectic final stages resulted in Eric Forth, the minister responsible for technology, describing the Democrats' leader as "glib", "waving something which was halfway between a wand and a panacea" and offering "fraudulent proposals". It all goes to show that when statistic and anti-statistic collide, cold fusion releases much energy in the form of heat.

Parallel thought processing

An intriguing conundrum concerning Fylingdales early warning station surfaced during an exchange between Archie Hamilton, Minister of State for the Armed Services, and Labour's Andrew Bennett. How was the Minister sure, Bennett asked, that the USA would provide all information from the early warning station to the UK authorities, if the USA thought that a UK government would independently fire its Trident missiles? No problem, replied the Minister, we receive information in parallel, "so there is no question of one nation having it and giving it to the other".

But what about the interpretation of data? Although there was a principle of mutual corroboration, no guarantee was given to the House that such corroboration would result in an agreed interpretation of events. Thus, it is theoretically possible for the UK's interpretation to be so different from the USA's that the UK might want to fire off its Trident independently. Mmmmm!

More support for defence exports

Defence exports from the UK over the last three years have totalled £13 billion and electronics forms a significant part of that total. Could the UK export more if the resources of the Defence Export Services Organisation (DESO) and embassy staff abroad were more effectively used?

The answer from a recent National Audit Office Report[1] is a definite 'yes'. Its study showed that DESO's and embassy staff did not usually have sufficient business or marketing experience, and that high staff turnover in DESO made communications between staff and exporter difficult. Resources, the NAO found, were targeted at the larger companies, with the result that there was too little support for the smaller company in defence electronics. To assist exporters further, DESO should computerize its complex and cumbersome manual database. Both embassy and DESO should, the NAO reported, apply specific performance measures to ensure that their effectiveness and efficiency was not impaired.

The NAO managed one unsubtle hint; it noted that exporters "welcomed the NAO's own survey", and "such surveys should be a regular feature" of DESO's and the attachés' future work.

[1] National Audit Office, Report by the Comptroller and Auditor General, 'Minister of Defence: Support for Defence Exports', HC 303, ISBN 0 10 230389 4, £5.60 from HMSO.

Notes on the House are by Chris Pounder.

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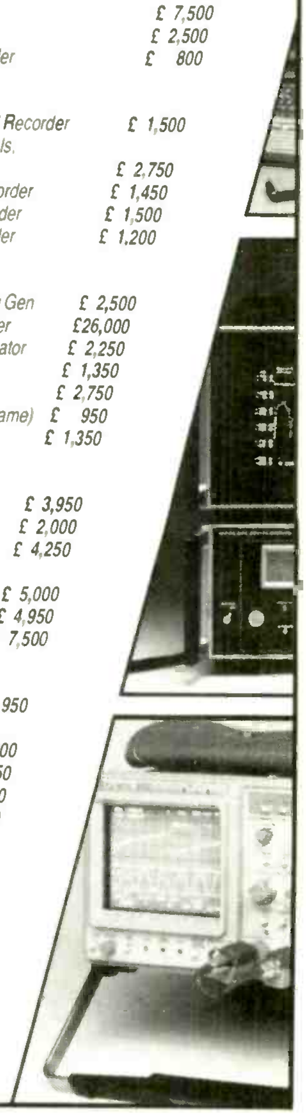

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FFT ANALYSIS WITHOUT TEARS

FFT analysis is a powerful tool which, nevertheless, conceals a number of traps for the unwary. David Mawdsley of Laplace Instruments exposes them and shows how to tame FFT analysers

There has been a virtual explosion in the use of FFT techniques and equipment within the past 10 years in almost all branches of engineering and science. The driving force has been the availability of very powerful FFT instruments at steadily reducing prices as the cost of computing power and speed drops.

But what about the expertise to drive these instruments? Most practising engineers and technicians were trained in an era when the Fourier series was only mentioned in passing and FFT analysers were almost unheard of. To make matters worse, most magazine articles and academic courses approach the subject from a mathematical or theoretical point of view. Although this approach is obviously important and is indeed essential in some areas, it is not really what the engineer wants to know when struggling to decide which instrument to buy, or how to obtain the best results, or how to interpret results.

This article is based on an intuitive, non-mathematical approach to explain how FFT analysers work, how to choose the right one for your application, and how to get the best out of it.

SIDE EFFECTS

FFT analysers are powerful and useful machines, but as with powerful drugs, their use can have potentially destructive side effects which must be anticipated and allowed for. Examples are leakage, the picket-fence effect, and aliasing.

In frequency analysis, aliasing is not just an minor irritant or nuisance: it can be a source of major errors and must be completely avoided. This is because aliases cannot in general be distinguished from 'real' signals in the frequency domain. It is therefore vital that proper anti-aliasing filters are used for all serious FFT analysis.

To understand the other side effects, it is important to grasp two basic concepts about how the FFT analyser operates. Firstly the basis of the FFT technique is derived from the discrete Fourier transform, or DFT. The important word here is discrete. It means that the process works on discrete samples of the signal and displays the results in the frequency domain as discrete points, so the results are not in the form of a continuous spectrum, but as points or 'lines' with gaps in between.

The second point is that the analyser works on only a short length of the signal. This is called windowing, because the analyser sees the signal through a window, and cannot see anything either side of the window. Now the Fourier technique assumes that the signal is continuous. To satisfy this requirement, the windowed signal is assumed to repeat itself continually, i.e. the windowed signal fully represents the true signal and therefore repeating it continuously should not be a problem;

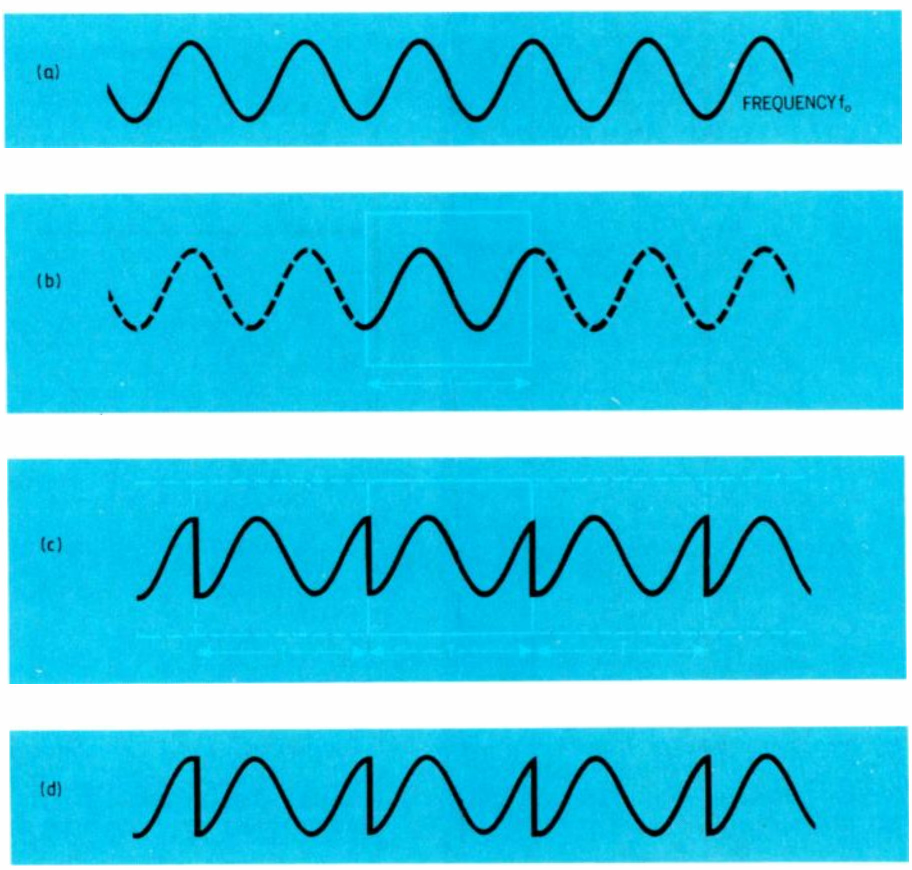


Fig. 1. Windowing. The signal at (a) is seen through a "window" at (b). If the signal is repeated for ever, as at (c), the signal seen by the FFT analyser is that shown at (d).

or should it? (**Fig. 1**). In general, major discontinuities exist at the window edges, are assumed to be part of the true signal and are therefore transformed into the frequency domain, leading to false results. What form will this distortion of the results take?

A simple way to visualise the effect is to look at the discontinuities in the apparent 'signal' as a modulation of the original signal. The effect appears every window width T and its frequency is therefore 1/T. Now, modulation causes sidebands in the frequency domain, appearing at f ±F, so one would expect to see similar effects on the FFT results. This is precisely what happens. The effect of windowing is to cause shoulders or sidelobes to appear either side of the peaks. Some of the energy in the signal is leaking away into these sidelobes, which is where the term leakage comes from. How can this effect be prevented?

WEIGHTING

One way would be to avoid the discontinuities by arranging for the window length to be an exact multiple of the signal period. The problem is that (a) most real signals contain more than one fundamental frequency and (b) on most analysers the window length is not adjustable. This means that we have to accommodate these discontinuities in some way. In practice, the effect is suppressed by using 'weighting'.

Weighting is a function applied to the samples of the signal prior to processing by the FFT algorithm. So far, all samples have been considered equal, and have a weighting of one. This is called rectangular weighting. Other weightings have been derived which reduce the importance of the samples at the edges of the window, and correspondingly increase the importance, or weight, of the samples toward the middle. Many such weightings exist, the most common being Hann, flat-top and Hamming.

The effect of these weightings is to

- reduce the discontinuity to zero
- modulate the signal by the 'shape' of the window
- reduce the sidelobe height in the frequency domain, and
- increase the effective bandwidth.

Increased bandwidth? This needs a little explanation. The bandwidth we are talking about is that of each point in the frequency domain. In a perfect system, each point would represent a perfect band-pass filter of very small width and with virtually brick-wall characteristics either side. However, in practice the

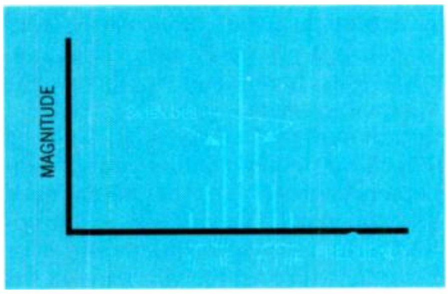


Fig.2. Leakage due to windowing. Energy from the signal F_0 has "leaked" into the side lobes.

filter has a finite width and a finite cut-off slope, which characteristic determines the selectivity of the system.

Now the time and frequency domains have an inverse relationship. If we look at the window shapes in the time domain, it is clear that the maximum effective window width is obtained with the rectangular window. All other windows can intuitively be seen to have a reduced effective width (think in terms of the 3dB points). Reduced width in the time domain is equivalent to increased width in the frequency domain. So the effect of windows other than rectangular is to increase the bandwidth of each frequency point. Therefore this effectively reduces the ability of the FFT analyser to resolve close components. It also reduces what is called the picket fence effect.

To understand this, recall that the FFT process is discrete. It calculates the frequency content of a signal in terms of discrete points in the frequency domain. So, for instance, if we have a 400-line FFT analyser working on a 20kHz span, then there will be a line every 50Hz, at 50, 100, 150Hz. What happens if a single frequency of, say, 125Hz is present? In a perfect system, it would not appear because it falls between two frequency lines. This is the picket-fence effect, so called because we do not see the frequency domain fully, but only as narrow slots separated by areas we cannot see properly. In reality, because each line has a finite bandwidth, and these overlap, frequencies which fall between lines are seen as components in the adjacent line, but at reduced magnitude. The wider the bandwidth of the system, the less reduction in magnitude is seen. Rectangular weighting gives a worst-case reduction of 3.9dB, whilst Hann gives 1.4dB.

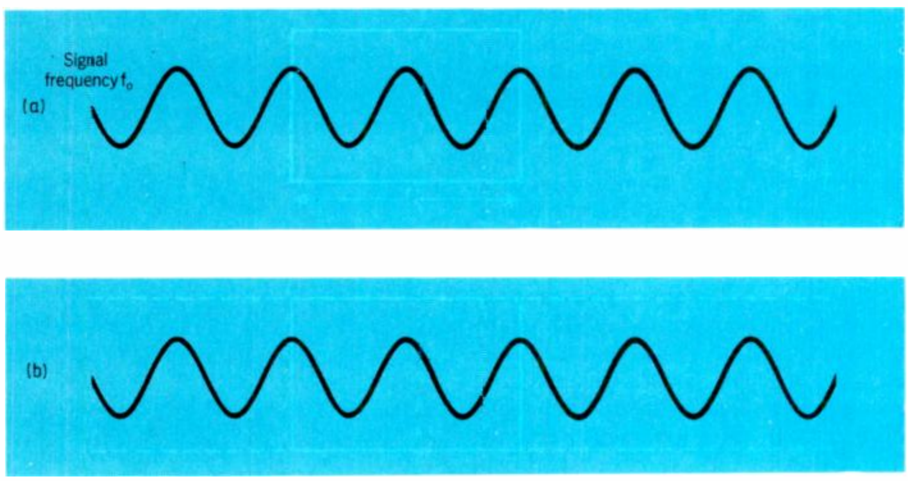
Thus you can see that the selection of the right equipment, the correct modes, weighting and other controls, are vital to ensure the integrity of the results.

Vibration analyis. As an example of the use of weighting, consider the ultimate vibration generator – the helicopter.

Take a lightweight structure, balance a very powerful engine somewhere near the top of it and connect it to a gearbox with many power take-off points, all requiring different gear ratios. Put a huge fan on top of all this, which takes virtually all the power of the engine to drive, and has variable angle of incidence and long, flexible blades as well. Attach a long stick to the back, put another fan on the end of it and drive it from the gearbox via a long shaft with another gearbox at the far end. Hang various accessories all over it (antennas, landing gear, missiles, some crew members, etc.) and fly through the air at speeds in excess of 100mile/h. What happens. . .?

Well, imagine driving a car fitted with all-steel wheels. Bits fall off. The crew cannot read their instruments. Ancillary equipment fails. Critical equipment fails. The fatigue life of the machine suffers.

Fig.3. In the special case of the window length being an exact multiple of the signal period, as in (a), repeating the window recreates the original signal.



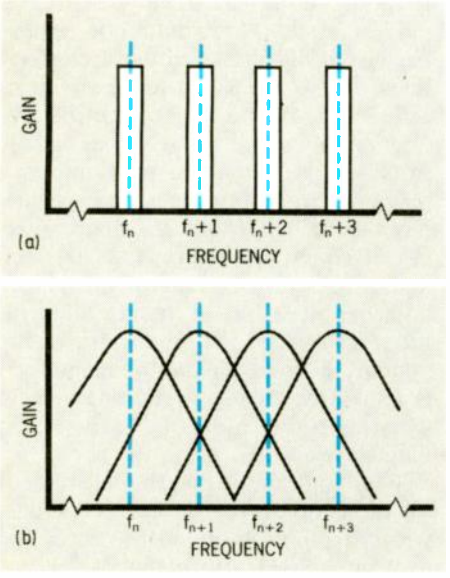


Fig.4. The idealized band-pass filter at (a) is, in practice, more like that shown in (b).

Question: what can be done about it?
Answer: eliminate each possible source of vibration.
Problem: how to detect which of the hundreds of possible sources are the significant ones?
Answer: do a frequency analysis of the vibration.

The helicopter is a fixed-speed machine. The engine and rotors run at a constant speed within a tolerance of around 1% and, in general, each source has its own characteristic frequency. Helicopter manufacturers issue charts showing those frequencies for all their models. By checking vibration frequencies against those charts, the sources can be immediately located. By extending this principle to do vibration analyses periodically and monitoring the results for trends, an early warning of any problems in bearings, gearboxes or rotors can be detected. The next generation of helicopters will almost certainly have an FFT-based monitoring system built in, complete with accelerometers to measure vibration and electronics to perform continual in-flight FFT analysis and warn the pilot of any significant changes in the vibration spectrum. Such equipment is already in use on a limited scale with some manufacturers.

But what are the practicalities of performing vibration (frequency) analysis on helicopters today? The starting point must be a vibration transducer. These days, small piezoelectric accelerometers are almost universally used for all vibration measurements. Tri-axial units are available which will give outputs in all three axes simultaneously if you have the equipment to cope with three channels. Obviously, equipment which is portable, small and battery-powered is essential. Lugging 19inch-rack equipment on and off helicopters has been done, but it's not to be recommended. One perfectly viable option is to use a special data logger or recorder to record the vibration on the helicopter and perform the analysis later when back at base. To define the requirements for the analysis itself we must look initially at the type of signal being analysed. The signal tends to be noisy and consists of the following components:

- Steady components from engine, gearbox etc. often at a relatively low level (amplitude).
- Fluctuating steady signals (!), signals which are of fixed frequency but can vary in amplitude significantly over periods of several seconds. The main rotor vibrations and aerodynamic effects are examples of this type.
- Random noise caused by aerodynamic buffeting, mechanical and electrical equipment etc.

Next, look at the results needed. Obviously the main objective is to detect and accurately measure the amplitude of all significant vibration components. On helicopters some of these are quite closely spaced. Some are harmonically related, but many are not. Amplitude is important and it needs to be output scaled in units of (typically) velocity. Things which are not so critical are the detection and measurement of low-level components, wide dynamic range or frequencies above 10kHz.

These requirements dictate that we use the analysers in the following way.

The effect of random noise is reduced to an insignificant level by using averaging in the frequency domain. Any steady signals, even if completely buried in noise, will be revealed if sufficient averages are performed. Because the signal is essentially stationary, linear averaging is used.

Those signals which vary with time can be averaged out to provide a steady, meaningful level. Again linear averaging is used with up to 128 updates.

The requirement to measure amplitude directly in terms of engineering units means that linear vertical scaling is used. Logarithmic scaling would complicate such measurements and its main advantage, increased dynamic range, is not required.

Because amplitude measurement is critical in this application, the window function (i.e. weighting) used should be one which minimizes the picket fence effect. Suitable weightings are therefore those which give a wide bandwidth.

In certain cases, the frequency resolution may not be sufficient to separate closely-spaced components. In these cases frequency zoom may be necessary to increase the resolution. The penalty for using zoom is time. For instance, zooming to give a resolution of 0.1Hz with 32 averages means waiting for five minutes before getting one result (and helicopters cost several hundred pounds per hour to fly).

As you can judge from the above, getting the right results is not just a case of buying the fanciest piece of kit in the catalogue, plugging in and watching the screen. FFT analysis is a powerful machine, but you have to know how to drive it or you will end up in a spin. ■

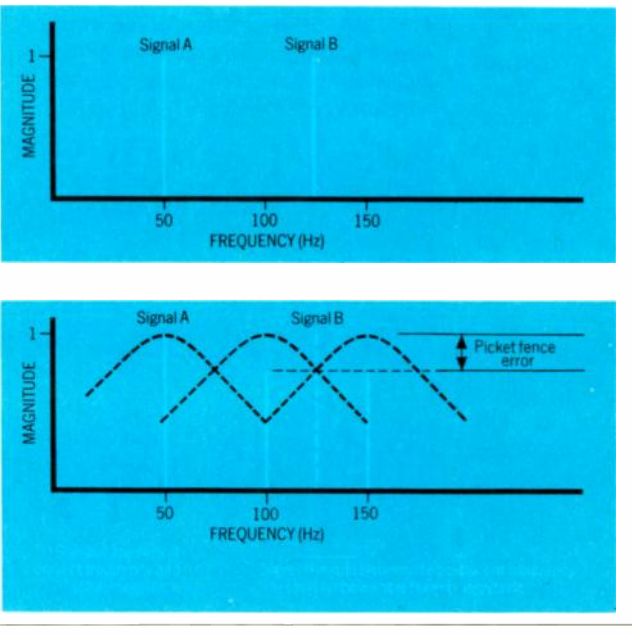


Fig.5. The picket fence effect. Signals falling between the lines, such as the 125Hz signal (above), could not be seen if each line was infinitely narrow. In practice, the lines have bandwidth, as below, and show the signal in each of the adjacent lines at reduced amplitude.

Cold fusion

Radical scientific discoveries have a propensity for creating scepticism, and the Fleischmann and Pons fusion cell is certainly no exception. During the early 1900s, Bohr, Einstein and others suggested that atoms could be stimulated to emit energy, but it was 1960 before the first laser appeared!

If the cold-fusion device fails to deliver its promise, the purge of ridicule might also inhibit the discovery of an 'avalanching' effect for radioactive decay! Many physicists will insist that the natural rate of radioactive decay cannot be influenced by external means. However, nuclear dogma has enjoyed frequent reinterpretation over the years, particularly after Mossbauer's discoveries in 1958.

Nuclear avalanching will resolve the fission waste problem, by converting long-lived isotopes into compact power sources, whilst simultaneously transforming fuel slugs into safe non-active elements. The nucleonic turn-key for this process will be found within the observed phenomena of nuclear physics and the technique will change our world more radically than cold-fusion experiments!

C. Bruce Sibley
Waddington
Lincolnshire

Crossed-field antenna

Allow me to congratulate Messrs Kabbary, Hately and Stewart (*EWW*, March 1989, pp 216-218) on their very amusing April Fool article! It's a pity it was published a month too soon.

They have almost persuaded one that a simple modification could make the humble dipole into a super-efficient radiator. Like good conjurors they cleverly hid their trick: firstly, by concentrating on the H-field produced by displacement currents, they made one almost forget that ordinary currents also produce H-fields; secondly, by setting up an analogy between addition and the logical Or (top of p.217) they made one almost forget that terms might cancel as well as add. Hence, the reader was made to overlook the possibility that the H-field due to the current in the feed-wire to the upper D-plate of their crossed-field antenna (Fig.6.) might cancel the field due to the displacement current between the D-plates.

Unfortunately they seem to have missed the best trick of all. If, by rephasing one of the drives, we phase-reverse one of the factors making up the Poynting vector S, then we change the direction of S itself. So, instead of having power flowing outwards, we can make it flow inwards. Thus we shall have an inexhaustible source of energy which might make even Professors Fleischmann and Pons green with envy!

William G. Chambers,
Department of Electronic and Electrical Engineering,
Kings College,
London.

Ohm tune

I note from *E&WW* May p449 Martin Eccles' report on the declining value of the standard Ohm.

This does not bode well for Mrs Thatcher's Ohm ownership policy!

C.J. Harris,
Weoley Castle,
Birmingham.

Anti-gravity and cold fusion

As David Williams (*EWW* Letters, p. 415, April, 1989) says, it certainly is reasonable to dispute the anti-gravity claims, if one has not seen the demonstration of the phenomenon. To witness a heavy flywheel subjected to a gentle forced precession and lifted by Professor Eric Laithwaite's little finger in a smooth non-vibrating fashion has overcome my incredulity. To have the result confirmed by two separate precision weight measurements, one mechanical (the Strachan machine) and one electronic (the Kidd machine), is confirmation that Professor Laithwaite is not superhuman. It is due time that those interested in the technological opportunities provided by this phenomenon brought it under their own scrutiny, as there is little to be gained by interested onlookers, including myself, giving vent to their personal opinions.

However, until authority rules on this subject, it may help to draw attention to something else that has a possible connection and has just hit the news, namely the cold-fusion process discovered by Professors Fleischmann and Pons.

Rather than venture my own opinions, I point to the 1966 edition of a book written by Professor Sir Harrie Massey, F.R.S., entitled 'The New Age in Physics' (published by Elek Books). The title was probably about 25 years ahead of events. On page 149 he discusses anti-gravity and says:

> 'One possibility, which cannot be ruled out at the present stage, is that of a repulsive force of gravity between matter and anti-matter. We cannot yet say whether a piece of matter exerts a gravitational attraction or repulsion on a piece of anti-matter – we do not know whether anti-protons tend to fall downwards or upwards. The nature of the force of gravity is still so obscure that no reliable answer can yet be given from theory.'

A few lines further, on p.150, he discusses 'The New Aether' and the presence of negative mass protons and neutrons as well as mu-mesons in the vacuum itself.

Now having regard to my article on 'Anti-gravity electronics' in the January 1989 issue of *EWW*, readers will see that I questioned the universal validity of Newton's Third Law of Motion (as related to the law of conservation of momentum). I have received many letters from professors and others, taxing me on these opinions. But let us see if the book can shed light on the subject. I quote from his chapter entitled 'The Strangest One of All' at page 253:

> 'This is by no means an isolated example. These two features are present in all beta-radioactive phenomena – there is an apparent disappearance of energy and the conservation of angular momentum appears to be violated. Attempts were made for many years to detect the energy which was not taken up by the product nucleus and the emitted electrons, but all without success... It was natural to enquire whether, in beta-decay phenomena, the conservation of momentum also breaks down. This is difficult to investigate because of the small energy taken up by the product nucleus. Nevertheless it was established in later experiments that this further conservation rule also appeared to fail.'

Readers may wonder about the 'isolated example' just referred to. It concerned the decay of the triton into helium 3 and an electron. The energy shed to the electron did not fit the Einstein formula for the loss of mass involved in this nuclear process. The triton is formed by two deuterons fusing to create a triton and a proton. Note also that two helium 3 nuclei can fuse to decay into two protons and helium 4. There are no neutrons involved.

The point of interest is that the cold-fusion process reported by Professors Fleischmann and Pons is stated to occur with negligible neutron production. This, then, means that the decay process raises the mysterious issues of energy balance and force balance just discussed and we do see our entry into a 'new age in physics', an age in which we can face up to the prospect of anti-gravity and new aether technology. However, sceptics relying on what they have been taught, without reference to what is accepted as inexplicable, will need to be dragged into that new age. Sadly, that drag effect does comply with Newton's law and sets up opposing forces which resist those trying to drive us forward.

Finally, concerning 'cold fusion', is it not curious that *EWW* published an article by Carl D. Adams as recently as January 1988, on what is effectively 'cold fission'? Had 'cold fusion' been predicted as well, critics would have pointed to the very substantial energy needed to bring deuterons close enough to fuse and said that it was impossible for this to work at normal temperatures. I would then have drawn attention to my discussion of the deuteron binding energy in my 1969 book 'Physics without Einstein' (Sabberton, P.O. Box 35, Southampton), because I show that electrons can bind protons together in an atomic nucleus. This is also the theme of my paper 'The Theoretical Nature of the Neutron and Deuteron' at p. 129 of the *Hadronic Journal*, July 1986. It does not surprise me, therefore, to hear that deuterons can be fused in a palladium cathode, bearing in mind the presence of free electrons in a metal conductor and the background vacuum activity of those elusive mu-mesons.

H. Aspden,
Department of Electrical Engineering,
The University
Southampton.

Feedback and fets in audio power amplifiers

I am surprised that, in the above article by Ivor Brown in February 1989, the Otala criterion[1,2] for the prevention of transient distortion in amplifiers is still being used. (Erno Borbely also used this criterion in a mosfet power amplifier design[3].) This criterion requires that the open-loop bandwidth of an audio feedback amplifier be at least equal to the upper audio frequency limit (usually 20kHz). This criterion, which was introduced by Otala in the early 1970s, caused something of a revolution in feedback amplifier design, with many manufacturers moving to reduce negative feedback in their amplifiers to satisfy this criterion.

However, by the late 1970s and early 1980s, it was shown both theoretically and experimentally by Jung, Cordell and others[4-7] that open-loop bandwidth and feedback factor have no direct bearing on the transient distortion performance of an amplifier, and that the relevant parameter is the amplifier's slew rate. Specifically, to avoid transient distortion (slew-rate limiting), the slew rate of an amplifier must be greater than or equal to the 'slew rate' of the highest-amplitude, highest-frequency sine-wave signal that must be transmitted at the output of the amplifier. Since distortion progressively increases as the slew rate limit is approached, the amplifier's slew rate should be somewhat greater than the minimum value to minimise distortion products.

In conclusion, consistent with the normal stability requirements, large amounts of negative feedback can be applied around an amplifier, thereby securing the benefit of reduced harmonic distortion. It is time that this "high feedback is bad, low feedback is good" philosophy be laid to rest. Otala was wrong. Let us not perpetuate his error.

Stephen Gift,
Trinidad and Tobago Telephone Co.
Port of Spain,
Trinidad, WI.

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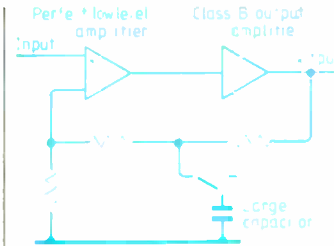
3. Borbely, E., High-power, high-quality amplifier using mosfets, *Wireless World*, pp 69–75, March 1983.
4. Jung, W.G., M.L. Stephens, C.C. Todd, Slewing Induced Distortion and Its Effect on Audio Amplifier Performance with Correlated Measurement Listening Results AES Preprint No. 1252 presented at the 57th AES Convention, Los Angeles, MAy 1977.
5. Cordell, R.R., Another View of TIM, *Audio*, pp 38–49, February 1980, pp 39–41, March 1980.
6. Garde, P., Transient Distortion in Feedback Amplifiers, *J. of the Audio Engineering Society*, Vol. 26, No 5, pp 314–321, May 1978.
7. Cherry, E.M., Transient Intermodulation Distortion – Part 1: Hard nonlinearity, *IEEE Transactions on Acoustics, Speech and Signal Processing*, vol. ASSP–29, No 2, pp 137–146, April 1981.

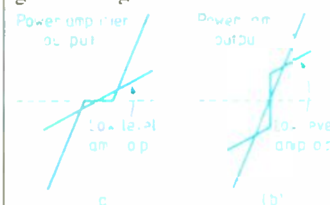
In his letter in the May 1989 issue, Douglas Self appears to state that the only detrimental effects caused in audio amplifiers by the use of large amounts of negative feedback and "heavy dominant-pole compensation" are due to slew-rate limitations. These he dismisses as a "non-problem".

I do not agree with this view and ask you to consider the amplifying system shown in **Fig.1**. Assume that the low-level amplifier is perfect and introduces no distortion, and that the output amplifier is operated in class B. This an



extreme case, but it will serve to illustrate my argument.

Consider the switch in the lower position, so that there is overall DC feedback on the system to stabilise the operating conditions, but, owing to the very large capacitor, no signal feedback. With a sinusoidal input, the output waveform will appear as in **Fig.2(a)** as the input goes through zero. Now throw



the switch and increase the input signal level to obtain the same output amplitude, and assume that the presence of the signal feedback removes all crossover distortion from the output. If this is to happen, the output from the low-level amplifier must look as in **Fig.2(b)** with an infinitely fast step in the waveform, implying that this part of the circuit must have infinite bandwidth and slew-rate.

In practice, operating in class AB, the crossover distortion will not be as severe, but since it occurs during only a small part of each signal cycle, the output of the low-level amplifier with its correcting "steps" will have to contain frequency components much higher than the signal frequency. If the frequency response of these stages is falling in the audio range due to a dominant-pole compensation network, this cannot happen. Therefore, effective cancellation of the crossover effects in the output stages is not possible.

As I say in my article in the February 1989 issue, bipolar output stages generate a lot of high-order harmonics when operated in class AB. The limited-bandwidth feedback will become less well able to reduce them as the order is increased. In practice, they do fall in amplitude as the frequency increases, which tends to compensate for the reduced effect of the feedback; hence the frequently seen spectrum with all the odd "crossover" harmonics appearing to have about the same amplitude.

In a system with a large loop gain, the feedback will always attempt to make the output an exact but enlarged copy of the input. With limited bandwidth in the low-level stages this becomes increasingly more difficult as the frequency rises. In an attempt to provide the necessary correcting steps, some relatively large transient signals may appear in the early stages. With poor design involving low-current stages and large compensating-capacitor values, slew-rate could be a problem.

In my design, the use of fets considerably reduces the crossover distortion problem and also enables a wideband low-level amplifier to be used, so that the full amount of feedback is present throughout the audio range. In this situation the distortion created in the output stage is not too important, as it is effectively removed by the feedback. With a voltage gain of about ten in the output stage, its THD exceeds the 0.1% figure quoted by Mr Self for his circuit. However, his design uses bipolar drivers which appear to operate in class AB and so will not help the crossover situation. With no information about the rest of the circuit, comparison is not possible.

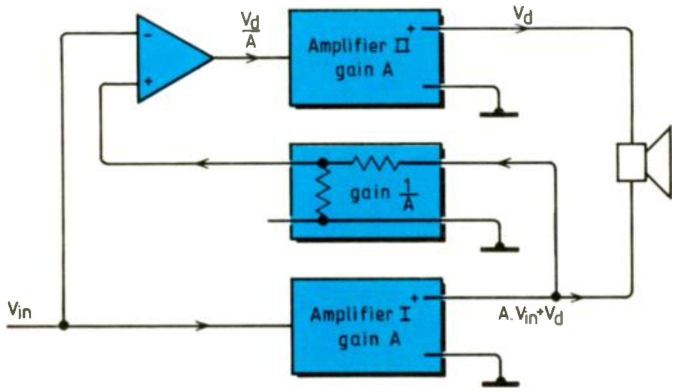
Further articles on my design are in preparation to include circuit details of the prototype together with experimental waveforms and spectra. With the Editor's permission these should be published in due course.

Ivor Brown,
Department of Electrical Engineering and Electronics,
Brunel University.

Feed forward

In your February issue, Ivor J.A. Brown writes in his paper "Feedback and fets in audio power amplifiers" about the feed-forward principle: "Addition of the inverted error signal to the output of the main amplifier is not easy to arrange."

However, this principle, also known as 'adding of the missing part' can very well be arranged in an audio power amplifier. All you have to do is to connect the loudspeaker to the 'plus' (or 'hot') connectors of two amplifiers. The loudspeaker is then driven by the difference of the two power signals. Mr Brown's Fig. 3 can then be implemented as illustrated here.



In this design, amplifier II, although it is only handling small signals, has to deal with large loudspeaker currents and will probably be as expensive as main amplifier I. However, a symmetrical circuit can be designed in which two equivalent amplifiers each deliver 50% of the power to the loudspeaker, while at the same time each amplifier produces a signal that compensates for the distortion produced in the other amplifier, using the principle of 'adding of the missing part.'

Peter van der Wurf
Bosrand
Geldrop
Netherlands

Ball-bearing motor

The ball-bearing and shaft configurations described in Stefan Marinov's April article do have features which could be expected to make them operate as motors. Take, for example, an arrangement with a rotatable outer cylinder, two ball races, and a fixed shaft of two insulated sections, with a voltage applied between its ends.

If the outer cylinder is initially clamped, current flowing axially along the shaft, well removed from either race, will have a fairly uniform azimuthal distribution, but near the race will be channelled towards the points of contact of the ball bearings. If now the outer cylinder is steadily rotated, the channels will try to follow the movement of the points of contact, i.e. they will swing in the direction of rotation, but with a time lag. Thus they become somewhat curved, by an amount which is greater, the greater the speed of rotation. As a result the current develops a circumferential component near the race, which gives rise to an axial magnetic field over the space occupied by it. This interacts with the radial currents flowing through the individual ball bearings, producing a torque on the race whose sense is such as to make it rotate faster. Consideration of the currents along the outer cylinder shows that they are distorted so as to have a local circumferential component flowing in the opposite sense. The axial field produced by this also tends to make the race rotate faster. Thus, if the outer cylinder is now allowed to rotate freely it will begin to speed up, and as it does so the driving torque will increase further.

On this interpretation there is no electromagnetic torque acting on the outer cylinder, which moves instead in response to the rolling friction between it and the individual ball bearings. The balls rotate as they roll, so that at every point on each ball there is a current oscillating in both magnitude and direction at a frequency a few times the frequency of rotation of the outer cylinder. This could be a significant factor in limiting the ultimate speed of the motor. The mechanism outlined is one which allows the motor to run on AC.

C.F. Coleman
Grove,
Oxfordshire.

I was most amused by Stefan Marinov's article and your report, and decided it was a phenomenon that could only be observed on the 1st April!

My copy of *EWW* didn't arrive until after that date and by the time I'd reached the article it was the 8th April; nevertheless, I was so intrigued that I decided to try it with a couple of ball bearings ex EMI tape recorder pressure roller. Yes, indeed – to my surprise it worked until the connecting wires to the car battery melted with clouds of rubber and PVC fumes.

I tried then on my welding transformer. Again, yes, and it ran until things got too hot for comfort: the race outer shells had tempered to a light straw colour but it still ran freely when cool.

Whilst it is an interesting phenomenon I can't see it having a serious future, but it does alert us to the nearly instantaneous thermal deformation in moving machinery that few people have ever considered to date.

Ralph L. West,
Villereal,
Lot et Garonne,
France.

Anti-gravity electronics

I wonder if many of your readers remember the Dean Drive of the early 1960s? This was the subject of USA patent No. 2,886,986, entitled "System for converting Rotary motion into Unidirectional motion."

It was a purely electromechanical device, employing timed reciprocal shifting of centres of revolution. In the computer world, there were rumours of an electronic version. But of that possibility, neither papers nor articles ever became public. Public interest faded when some (US government?) agency, took a belated second look at the Dean Drive, and it just dropped out of sight. As I understand the situation, under USA patent law, all patents are investigated for possible "defense" use. The Dean Drive had originally passed as innocuous, perhaps potty.

Some time later, I did see a possible utilisation. It was during one of the early near-space-walk experiments, when space was still considered to be news-worthy. An astronaut was shown to be using a power tool to drive a bolt head. There was no rotary reaction, but contra-rotating weights could assist there.

The significant point was the way that the astronaut did not move backwards. He had no means of forcing the tool to stay on the bolt head! "007" back-pack jets were not then being used. In my circle, it was assumed that the Dean Drive was being used.

This patent was brought to public notice by a series of articles in the magazine *Astounding Science Fiction*, which is now called *Analog Science Fact and Fiction*, and continues to publish new and speculative sicence. The Dean Drive was the cause of lots of speculation and comment in "Brass Tacks" – the letters page… regarding its use as a space drive, and other more terrestrial applications.
Philip Lonsdale,
Hillbrow,
Republic of South Africa.

Motion through the ether

Though in his May article E.W. Silvertooth doesn't say in so many words that Special Relativity cannot account for the Sagnac effect, he manages to leave the strong impression that it can't. In fact it is normally interpreted in terms of the Doppler Shifts generated in radiation reflected from moving mirrors (including beam splitters).

If the Sagnac ring is to provide a practicable system for measuring rates of rotation, then the difference between the phase shifts for beams travelling clockwise and counter-clockwise round the loop must be virtually unaffected by any linear motion common to all parts of the system, i.e. to the beam splitter, source, and phase-shift detector, as well as to the mirrors (see the inset box on page 438). This property certainly holds if Special Relativity is valid. However, the expression for the differential phase shift derived from ether theory (calculation supplied) contains a term linear in V_1/c, the component of the common velocity along the line joining the two mirrors. In other words, if a laser gyro based on a Sagnac ring is mounted in an aircraft with its plane horizontal and with the mirror-to-mirror path perpendicular to the heading of the aircraft, then according to ether theory the gyro would be expected to respond not only to rotation of the aircraft about its vertical axis, but also to any sideways drift it might show relative to the ground arising from the presence of a cross-wind. Some gyro!

Silvertooth states that ring-laser gyros are now in use for navigation. If so, his own interpretation of his measurements is certainly untenable. The effects he observes relative to the direction of anisotropy of the 4 K residual radiation from the "big bang" are large, in marked contrast to the results of the recently reported experiment by Riis *et al*, which sets a very low limit to the anisotrophy of the velocity of light in the laboratory relative to this direction. In principle, the Silvertooth experiment is the more direct of the two, but unlike the other it involves a mechanical translation in which the movements of the photocathode of the photomultiplier D1 and of the offset reflecting mirror M4 (p437) must match to within a fraction of a micrometre. Still it's hard to imagine a systematic error in the drive mechanism linked to the stellar rather than the solar day.

He refers to errors in navigation systems controlling satellite communication, and I remember Dr Murray making a similar point in this journal some years ago. If such errors are believed to exist, it is perhaps time the systems were described in the open literature in sufficient detail for outsiders to consider them.
C.F. Coleman,
Grove,
Oxfordshire.

Reference

E. Riis, L.A. Andersen, N. Bjerre, and O. Poulsen, *Phys. Ref. Letters* 60 (1988) 81-84

Whether E.W. Silvertooth's claim to have disproved the theory of relativity (*E&WW*, May, 1989) is confirmed or not, the underlying principle of the apparatus he describes is certainly the origin of number since it is of exactly the same form as the Tower of Hanoi problem. Clearly, as multiple (optical) path propagation under spread-spectrum conditions, the same mechanism will be found literally everywhere one looks. Since the Tower of Hanoi problem can be stated in terms of Gray (reflected binary) code, it follows that the visible environment is already coded in binary. Moreover, this, and similar problems are related to Hamiltonian pathways and therefore represent minimal-energy solutions. This leads on to the supposition that phase is quantized which, on reflection, seems to have been a massive error of omission in theoretical physics.
B.E.P. Clement,
Crickhowell,
Powys.

Radio data system

I write to thank you for publishing the above articles (February and March, 1989). They have enabled me to identify the source of interference which has been ruining the reception of stereo radio in my home and car.

It appears that the 57kHz data signal is getting into the stereo decoder, with disastrous results. The interference is heard as a rushing noise very like the sound of steam escaping from a boiler safety valve.

It is annoying that the BBC should be allowed to transmit RDS in a manner which is not compatible with existing, recently purchased receivers. I am certain that I am not alone in having to endure this curse and I suggest two possible methods of putting an end to the nuisance.

The first alternative is that the BCC should cease transmitting RDS and not resume until it has developed a means which is compatible with existing equipment. In default of this, you should publish a circuit for a filter to remove the offending signal before the multiplex stereo gets to the stereo decoder.
Andrew Cowper,
Northfleet,
Kent.

I was sorry to hear of the reception difficulties experienced by Mr Cowper, which he attributes to the transmission of RDS. I think, however, this is very unlikely to be the source of his problem.

Compatibility is, for the broadcaster, a very important aspect of any new development and was an essential element in the development of RDS. RDS conforms to well established CCIR provisions from supplementary sub-carriers: both older and newer receiver designs, almost without exception, are compatible with this enhanced feature of FM transmissions.

The impairment described by Mr Cowper can result from a number of other causes. In areas which are very generously served with FM signals, such as Northfleet, receivers can suffer from overloading which results in intermodulation products being generated. Severe multipath reception can also result in effects similar to those described. Without specific details of the receiver, or the aerial installation used, it is not possible to identify the specific cause with certainty.

However, for a fixed installation, careful attention to aerial type and positioning would be worthwhile and, in the case of possible overload, the use of an attenuator could be beneficial.

Should he be unsuccessful in overcoming his reception difficulties, which I am confident are not caused by RDS, I would be pleased to receive more details from him and offer what further assistance I can.
Mick Gleave,
Assistant Head of Engineering Information Department,
BBC

RDS is an agreed European Broadcasting Union and CCIR standard, and is designed to be completely compatible with reception on existing non-RDS radios. Since 1987, the IBA has so far installed RDS encoders at 31 independent local sites, after first having carried out extensive tests to ensure compatibility. From our experience, we are not aware of any problems having resulted to listeners with existing mono or stereo receivers.

I would suggest that the difficulties being experienced by Mr Cowper are likely to be due to receiver overloading in the presence of large numbers of strong signals (Wrotham is just a few miles away). Stereo reception is much more prone to the effects of signal overloading than is mono. Whatever the cause, I am confident that it is not RDS!
Paul Gardiner,
Principal Engineering Information Officer,
IBA.

Phase-locked VFO for VHF

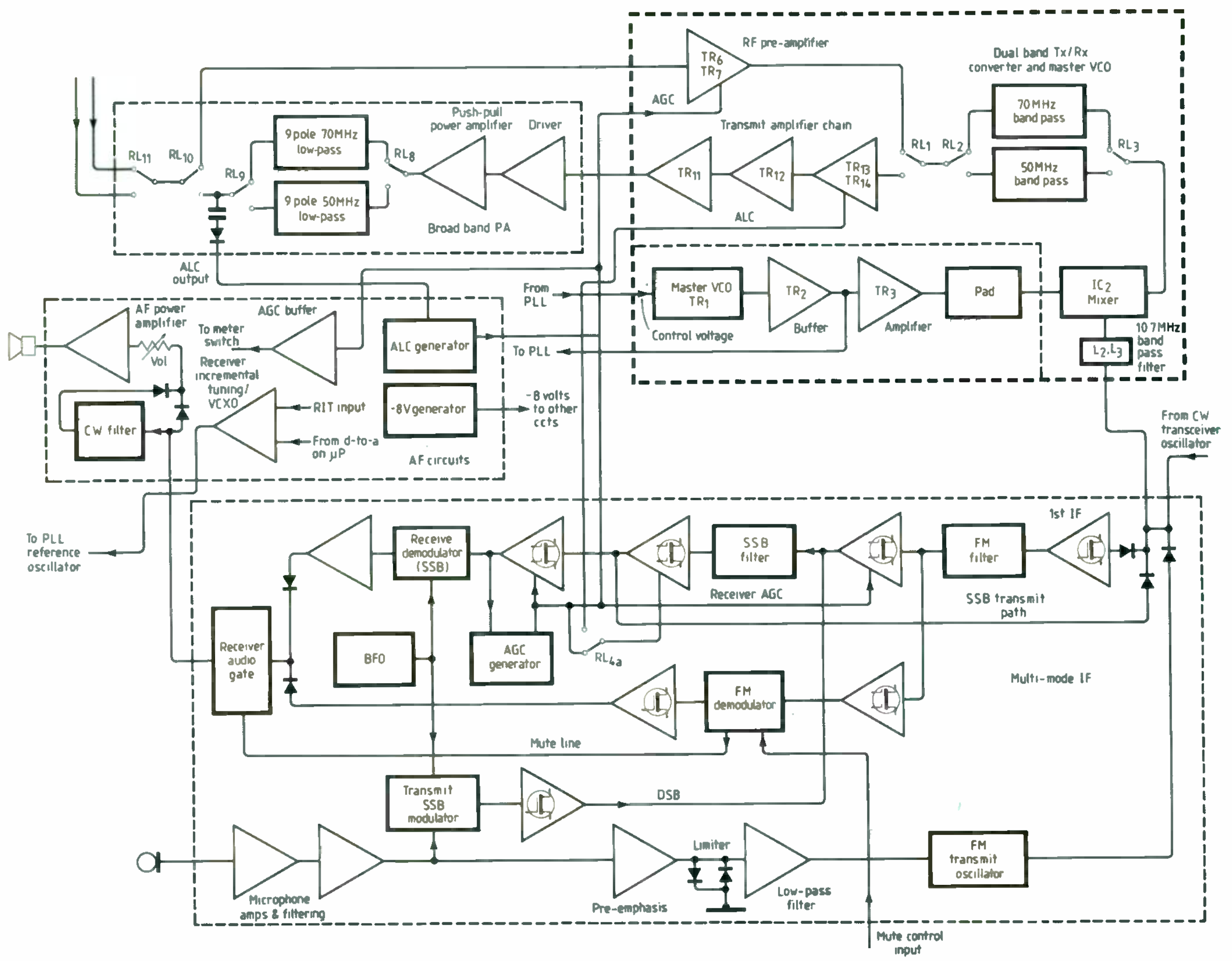
Tim Forrester describes an advanced oscillator which forms part of a dual-band, multi-mode VHF transceiver.

The initial requirement was to produce a transceiver which could receive anywhere between 50 and 70.5MHz, and transmit in the bands 50 – 52MHz and 70 – 70.5MHz.

Inevitably, a microprocessor was included to do all the house-keeping work such as scanning the controls, driving the synthesizer, frequency display, and band switching etc. From the outset the design was about producing a transceiver with excellent radio performance, and not about a radio with average performance but with an all-singing, dancing microprocessor system (as is often the case).

First of all, I decided that the tuning must have the "feel" of a VFO, i.e. the minimum tuning step size from the synthesizer must not be greater than 20Hz. Any step size greater than this is too easily detected by the ear. To be

Fig. 1. Dual-band transceiver for 50MHz and 70MHz. The phase-locked oscillator and microprocessor control stages are outlined in Fig. 2. Aim of the design was to produce a transceiver with excellent radio performance.



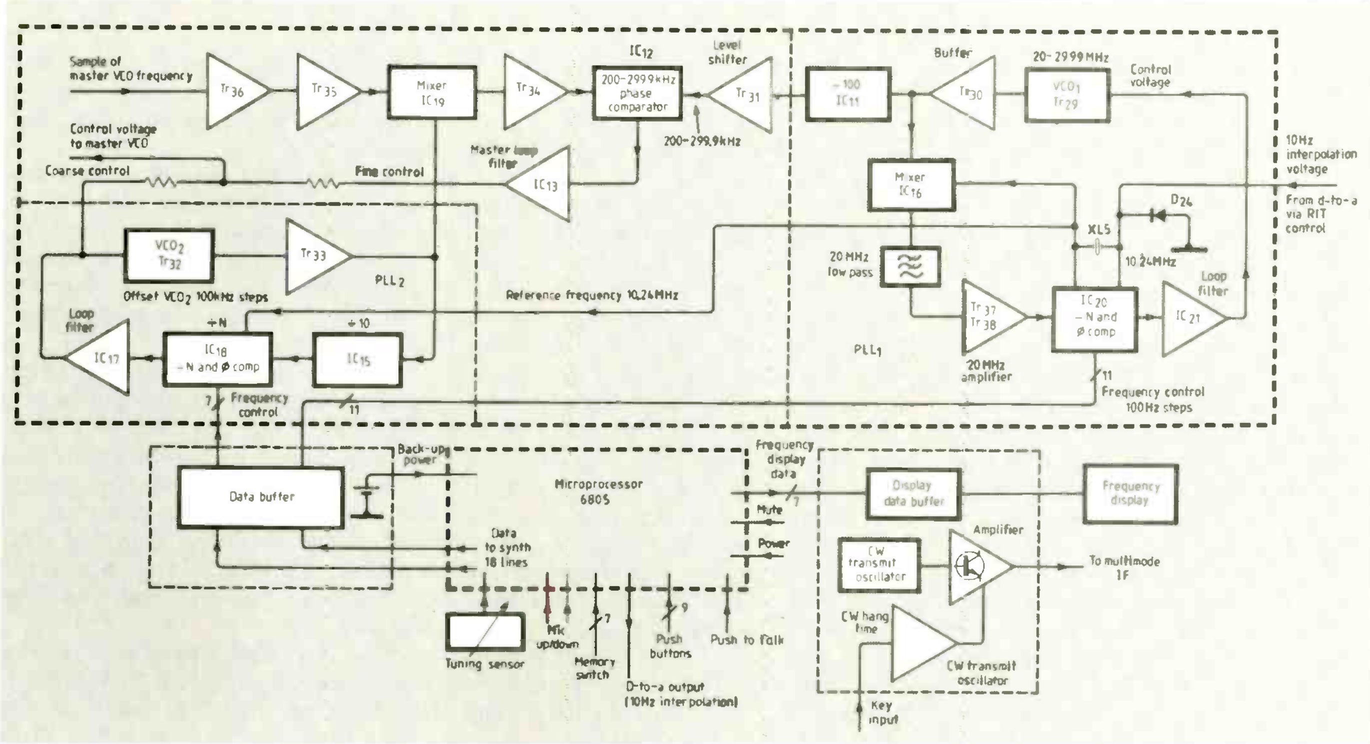
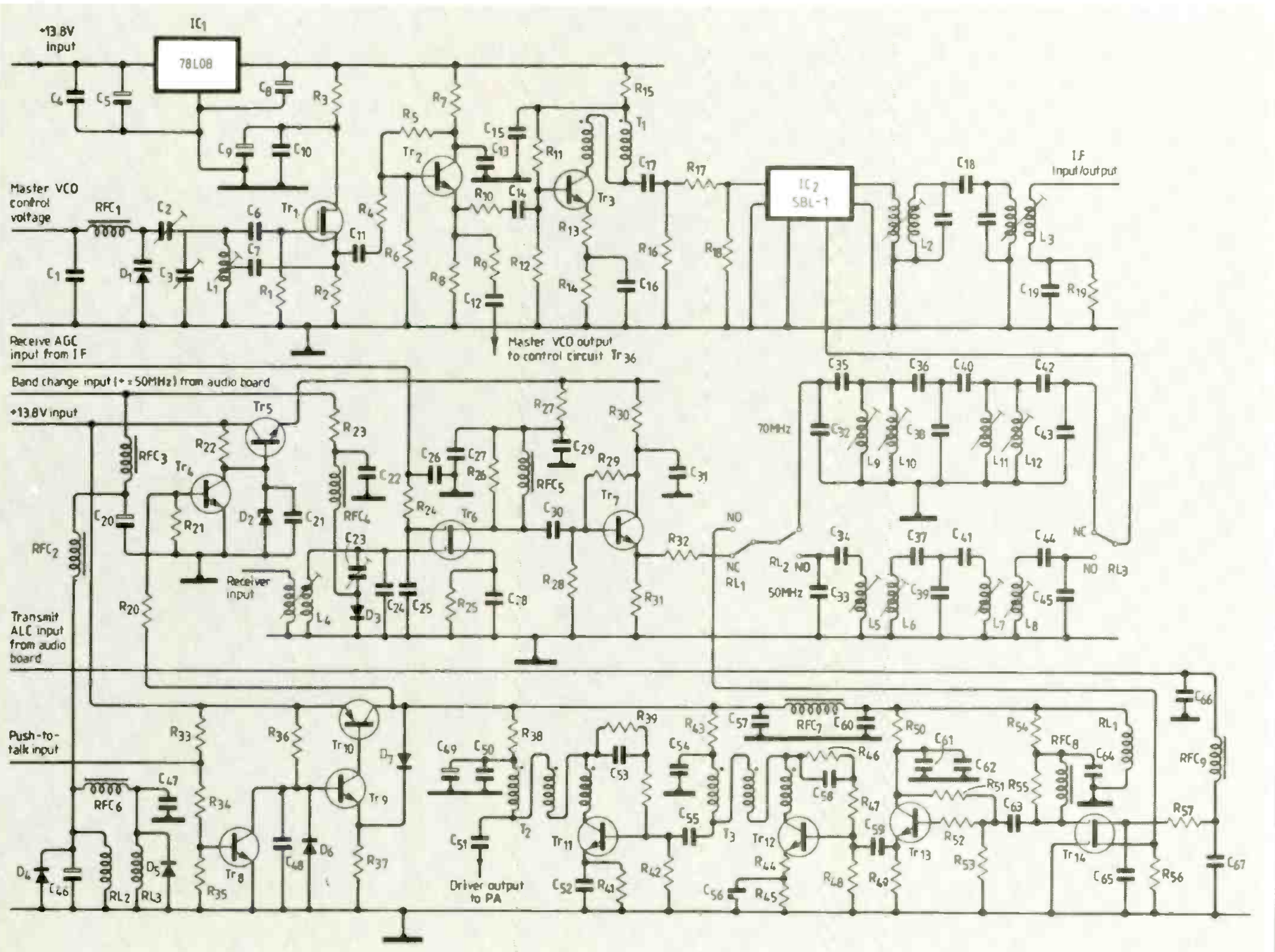


Fig.2. PLL, microprocessor and CW transmit oscillator for the dual-band transceiver. The processor is a 6805.

Fig.3. Dual-band transmit-receive converter and master VCO.



sure of a smooth VFO-like tuning response, I eventually decided upon a resolution of 10Hz as being a good compromise between complexity and resolution.

In the early stages of the design of the PLL, I considered a direct digital synthesis (DDS) approach. This would have had the benefits of very low phase noise and a very good tuning resolution, perhaps down to 1Hz step size. Unfortunately, though, at the time of starting the design the cost of fast digital adders and the other associated digital circuits made the use of a DDS oscillator prohibitively expensive. However, the cost of chips for DDS is falling rapidly. Plessey Semiconductors has announced an integrated circuit DDS device, which is capable of operating at up to 500MHz with a switching time of something around 10ns. No doubt devices such as this will eventually replace most conventional PLLs; but at present this particular device costs about £600 and is not yet freely available as a production item.

In this design the PLL would, ideally, enable the radio to operate over the range of 50MHz to 70.5MHz, with no gaps in the coverage. However, to keep the design simple to align, and to avoid the use of tracking filters and other complications in the actual RF signal path, I decided to restrict the coverage to just the amateur bands. Thus the PLL could operate at around 60MHz and use low-side injection for 70MHz operation, and high-side injection for 50MHz operation.

An additional benefit of restricting the tuning range was that the PLL had only to cover 3.4MHz in total to tune both the 50 and 70MHz bands. This enabled the PLL's performance to be optimized over a narrower bandwidth, thereby making its overall design easier. If the PLL had been required to work over the entire tuning range of 50 to 70.5MHz, inevitably some circuit parameters (such as VCO sensitivity) would have varied, causing the phase noise and/or the lock-in time to degrade.

For these reasons, combined with the need for tracking filters (to remove the unwanted in-band image response caused by the 10.7MHz first IF with its continuous coverage from 50 to 70MHz), I have restricted the tuning range so as to be able to use easily-adjustable bandpass filters to select the desired product from the mixer.

Trade-offs

Designing a PLL with a resolution of 10Hz and good phase noise performance is not too difficult if cost and complexity are not limiting factors. However in the present case certain compromises had to be made. The first was in the method of obtaining the 10Hz resolution.

It is fairly easy to design a synthesizer with a step size of say 10kHz, with reasonable performance, without resorting to complex multiple loops. This design, however, needed a resolution of 10Hz, which could not be achieved by a simple single-loop design.

After looking at several different schemes I decided on a basic digital PLL resolution of 100Hz, and to achieve 10Hz resolution by interpolation. This interpolation is achieved by slightly shifting the PLL's reference crystal. To understand how the resolution of 10Hz is obtained, it is best to break the operation of the PLL into sections **(Fig.2)**.

PLL1 is a conventional PLL operating between 20MHz and 29.99MHz in 10kHz steps. The only oddity in the design is the mixing down of the VCO signal from Tr_{29} with the 10.24MHz reference signal. The purpose of this mixing process is to enable IC_{20} to operate on the signal directly without the need for a prescaler. The output of this PLL is divided down by 100 in IC_{11} to produce a signal of between 200 and 299.9kHz in 100Hz steps. This signal is used as the basic 100Hz digital increment in the PLL and is fed to IC_{12}, a

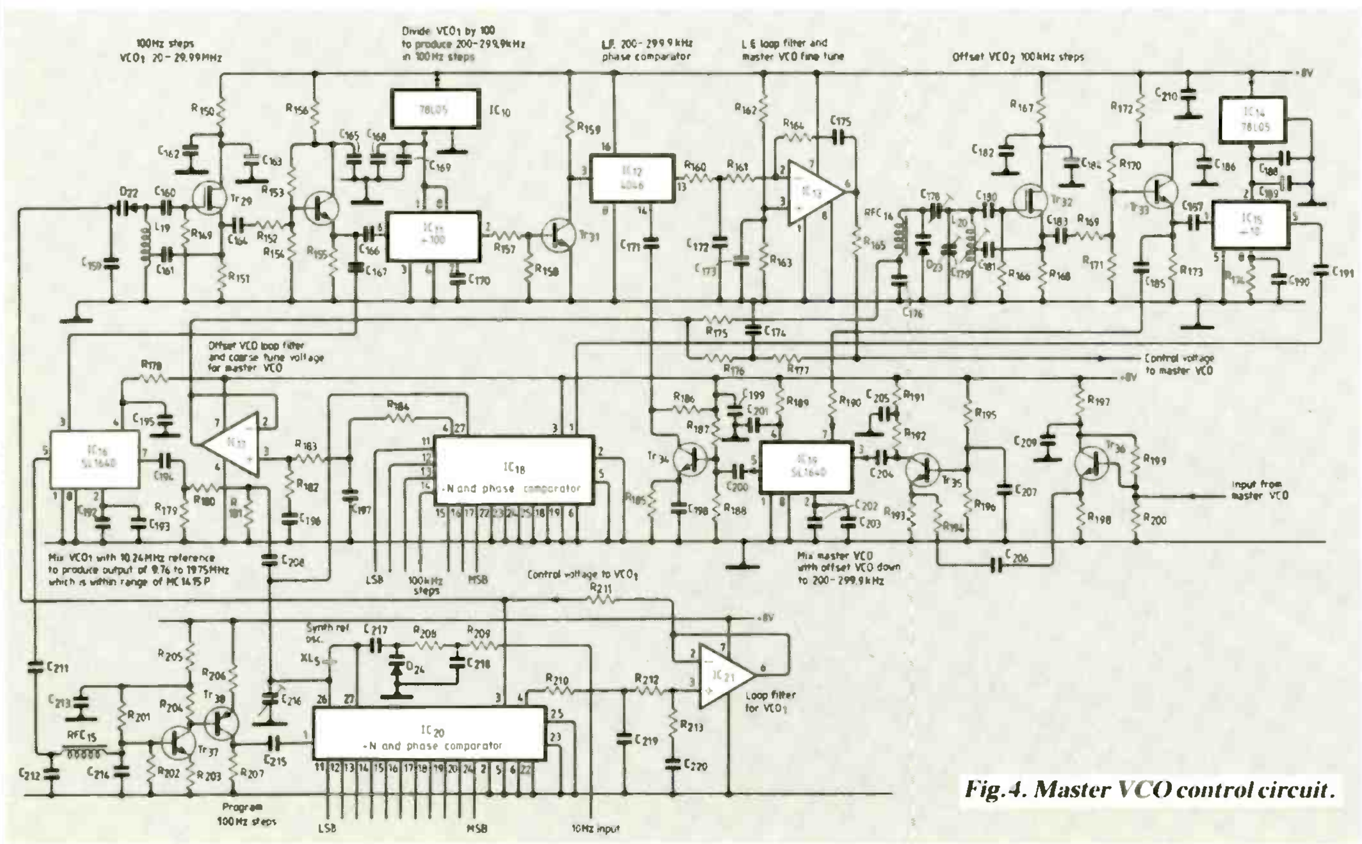


Fig.4. Master VCO control circuit.

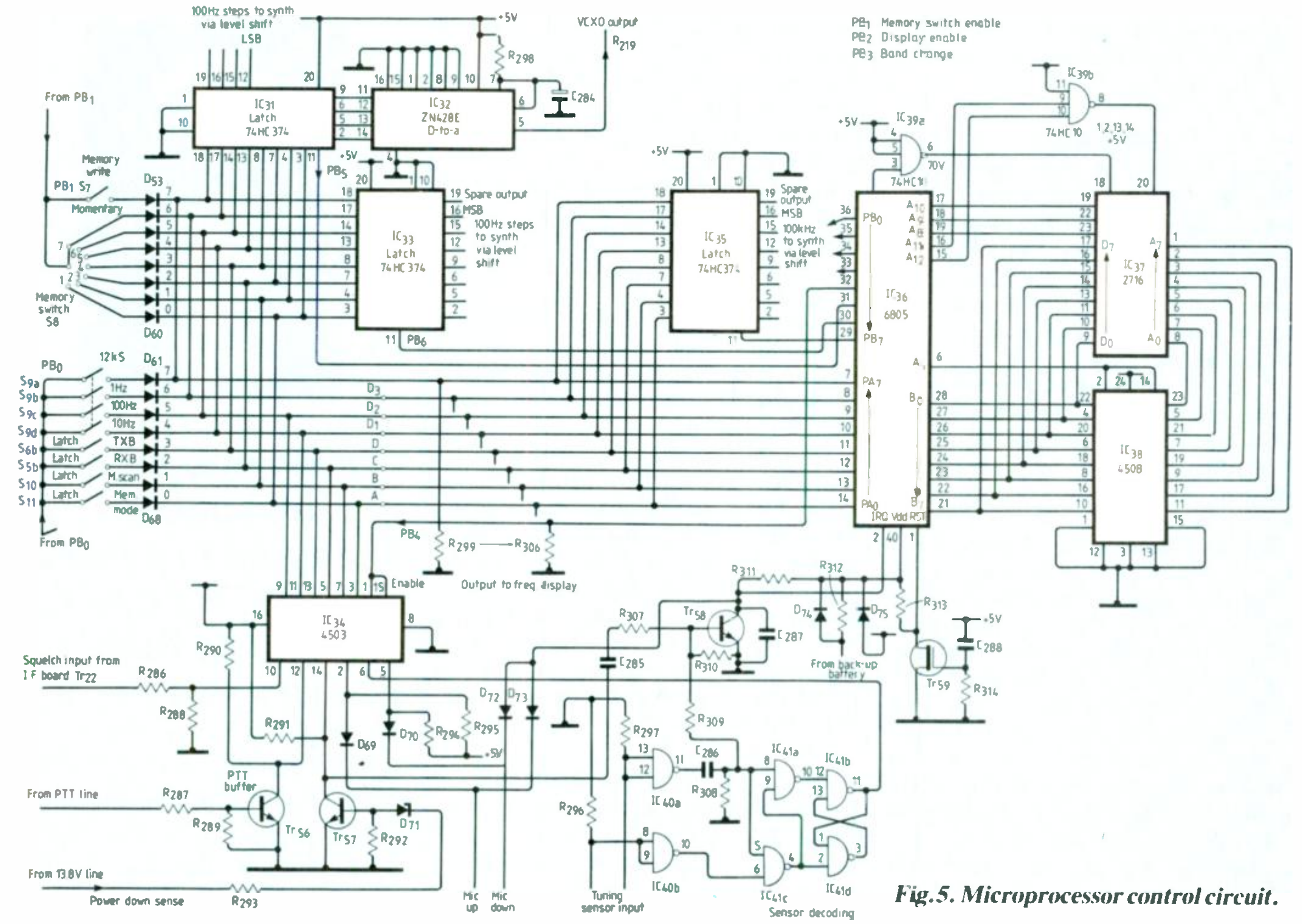


Fig.5. Microprocessor control circuit.

low-frequency phase comparator operating in the range 200 to 300kHz.

PLL2 is another conventional PLL, but this time operating in 100kHz steps; it uses the same 10.24MHz reference as PLL1. Transistor Tr_{32} is a VCO operating in the 60MHz region, whose output is split between IC_{15} and IC_{19}. The output to IC_{15} is divided by 10 to be within range of IC_{18}, which is the divide-by-N and phase comparator device. PLL2's frequency is chosen such that it heterodynes with the master VCO to produce a signal in the range of 200 to 299.9kHz. For instance if the offset PLL is set to 61.5MHz, and reference frequency set by PLL1 is 200kHz, then the master VCO has to be on 61.7MHz to be in phase lock. If the frequency of the 200kHz reference (generated by PLL1) were to change by, say, 100Hz, then the master VCO would have to change by 100Hz to track it.

To ensure that the master PLL locks up quickly, a steering voltage from the VCO in PLL2 is applied to the master VCO such that the 200kHz phase comparator has only to fine-tune the frequency. This steering voltage from the offset VCO also ensures that the master VCO is within the capture range of the 200–299.9kHz phase comparator.

The final 10Hz resolution is obtained by slightly varying the crystal reference frequency of 10.24MHz. An analogue control voltage is used to change slightly the bias voltage on D_{24}, which in turn shifts the reference frequency; this voltage is generated by an eight-bit digital-to-analogue converter on the microprocessor circuit board. As only a total of only 10 voltages are required (0Hz to 90Hz shift), only the four most significant bits of the D-to-A are used.

Control of the PLL

This method of heterodyning the master VCO with another PLL to produce a signal in the region of 200kHz for phase locking has been used for several years. But with the advent of single-chip PLL devices such as the Motorola MC145150 series, it has become increasingly easy to implement, thereby avoiding the masses of discrete logic which would have been previously needed.

Programming the PLL oscillator to the desired frequency is achieved by 18 parallel lines from the microprocessor via level shifters to IC_{18} and IC_{20}. Parallel programming is adopted in preference to the more usual serial method to make initial testing of the PLL easy without the need for a special serial interface. If serial programming is preferred, to lessen interconnections and improve overall reliability, then IC_{18} and IC_{20} could be replaced with IC type MC145155. A serial driver routine would then have to be added to the microprocessor program, because the number crunching in the processor is all parallel arithmetic.

With a design such as this, combined with an IF offset of 10.7MHz which can be on either side of the local oscillator, there is no easy or direct relationship between the eventual operating frequency of the radio and the data required to program the synthesizer. It would be possible to design some form of discrete logic circuitry to drive both the PLL oscillator and the frequency read-out, but this would be rather complex and inflexible. A much better solution would be to use a microprocessor.

Indeed, using a microprocessor allows a much greater flexibility in both the design and implementation of the control functions.

Software

The processor is a Motorola 6805, which offers good facilities for control functions, while at the same time being easy to program. In addition, since the processor can be single-stepped through its code, it is easy to debug the code by simply monitoring the state of the address and data lines.

Processor control was initially broken down into a number of basic modules which would form the basis for driving the synthesizer and frequency read-out. Subsequent subroutines would make use of these driver routines.

Any module or subroutine would have to restore the conditions of the processor's internal registers, before passing control back to the parent routine. Data would be passed between modules by each routine taking an input from one location in ram, processing it as required before writing it to its particular output location. This method could be considered wasteful of memory space, but does lessen the possibility of data being incorrectly processed.

The first module simply takes data from a location in ram and outputs it to the synthesizer. The data in ram is initially written to a particular location by the program itself, and contains the digits required to program the synthesizer to a particular frequency. Another module operates on the same source data as the synthesizer driver module. This module was designed to drive the frequency read-out, taking into account the IF offset and frequency band in use.

The frequency read-out driver module has a fair amount of number crunching to perform, and is therefore broken down into a number of subroutines.

For the tuning control I selected a cheap and readily available rotary encoder, whose outputs are two square waves in anti-phase. This encoder needs only a very simple logic circuit to detect the direction in which the tuning knob is being rotated and at the same time generate an interrupt to the processor. This enables the interrupt routine to update the frequency data and call up the driver programs previously described.

The interrupt routine of the tuning control also scans the front panel controls to determine in what step size the frequency is to be altered. The interrupt routine is in turn broken down into sub-routines. This was necessary as the tuning rate could be 10, 100, 1k, 10k or 12.5kHz per step. Routines are therefore needed to add or subtract these amounts to the data operated upon by the driver routines.

Included in the interrupt routines are limits on the frequency data, to ensure that the radio is not tuned out of band, and that the tuning wraps around at the band edges.

Also included are memory and scanning routines which enable the radio to scan spot frequencies on either band, automatically switching from band to band as required.

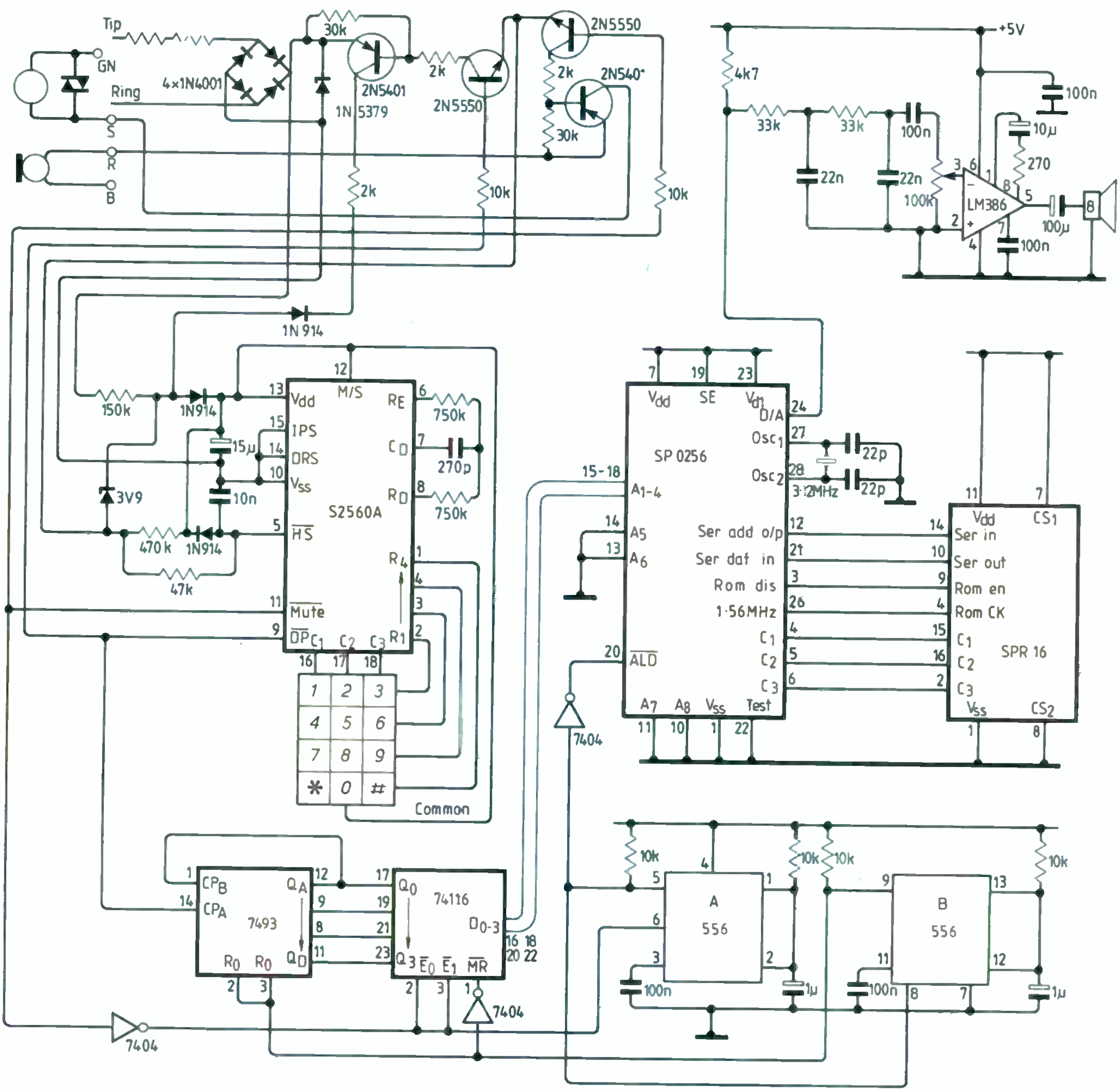
A further feature of the software is the ability to operate cross-band; that is to transmit on one band, then receive on the other. The control line which switched band pass filters in the radio was already being controlled by the program; and it was therefore an easy task to test the state of the transmit and receive band buttons, before outputting data from the appropriate ram location to the driver routines.

Microprocessor hardware

The 6805 microprocessor contains two PIAs, 112 bytes of ram and a clock generator. To interface the processor to the rest of the radio, one PIA is used as an input output bus, while the other PIA is used to enable various signals on to the PIA bus. Extra circuitry is included to de-bounce the rotary encoder and to generate interrupts when either the tuning knob is operated or the power supply falls below about 10 volts. If an interrupt is generated by low power supply volts, the processor is shut down and all present settings saved in the processor's internal ram.

When the processor is shut down it draws only a fraction of a milliampere of supply current, which is provided by a back-up battery. ■

Fuller details of this design will appear later in publications of the RSGB.



Speaking telephone keypad for the blind

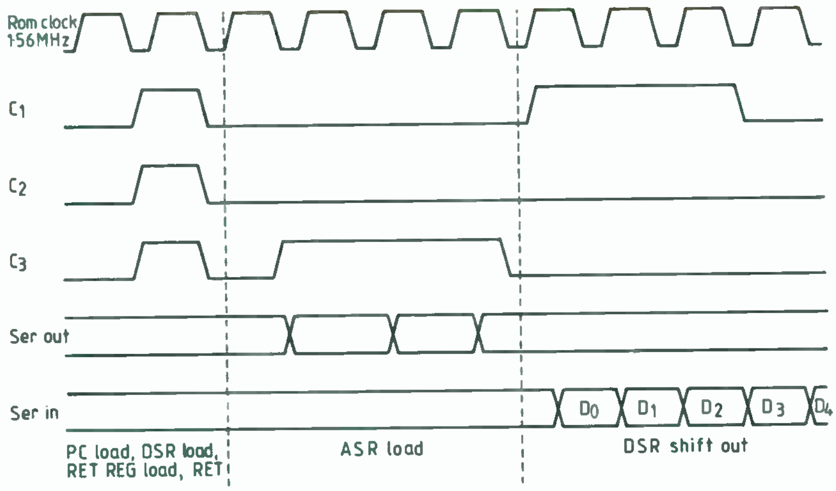
A low-cost speech processor IC and a speech rom vocalize the dialled number in a modified electronic telephone for the blind. The circuit gives an audible output when each digit is keyed, which is a useful confirmation of the number dialled.

When a digit is dialled, the dial pulse output, DP, of the 2560 pulse dialler outputs a pulse train, the number of pulses depending on the number dialled. Output pulses are counted by a four-bit binary counter (7493) which connects to the address lines of the 0256 speech processor.

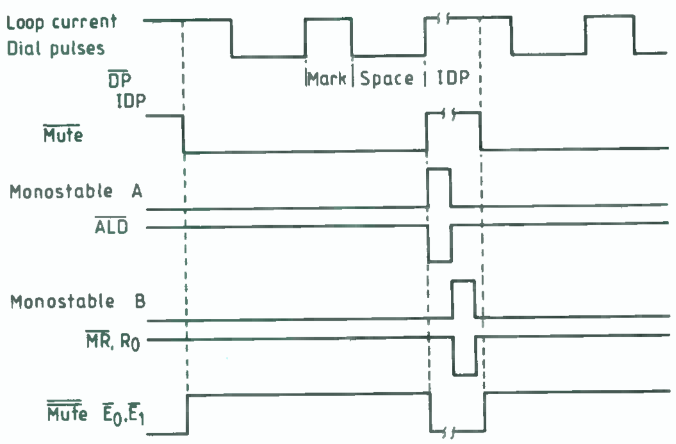
The pulse dialler gives a MUTE output, shown in the timing diagram, for muting the receiver during the dial pulsing. This output is used to trigger a negative-edge triggered monostable of 10ms pulse width.

After a digit is dialled, there is a pause during which the MUTE output goes high. The inverted MUTE signal latches the counter value in the binary counter into the four-bit 74116 latch. This transition triggers the left-hand monostable device whose output pulse is inverted and used to load the address into the speech processor using the ALD input. Output of the first monostable device triggers the second monostable section on its negative edge to obtain a 10ms pulse; this is inverted and used to reset the binary counter and the latch. Thus both the counter and the latch are reset during the inter-digit pause.

The 0256 speech processor is cabable of synthesizing speech or complex sounds using its stored program. Within the 0256, a microcontroller controls data flow from the SPR-16 speech rom to the digital filter, the concatenation of the word strings necessary for linking speech elements together and the amplitude and pitch information to excite the digital filter. The pulse-width modulator in the speech processor creates a digital output which is converted to an analogue signal when filtered by an external low-pass filter. Addresses from the 74116 latch feed a 2K by 8-bit rom (SPR-16) and data is extracted for the speech processor arithme-



SPR 16 interface timing



tic logic unit for coefficient transfer. Coefficients are then manipulated via a 'vocal tract model' block in the form of a 12-pole digital filter. Bits are then pulse-width modulated from digitized waveforms to analogue sinewaves.

The ALD strobe pulse given to the speech module enables the speech to reach a transducer through a passive filter.

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Hybrid audio preamplifier with low distortion

One of the main drawbacks of vacuum triodes, when used in the common-cathode configuration, is their high output impedance when a high gain is requested. The usual solution is to use two triodes for each stage, with the second one connected as a cathode follower or in a shunt-regulated push-pull configuration.

This circuit – a hybrid audio gain stage – achieves a low output impedance and a low distortion using only one half of an ECC88 dual-triode and a solid-state buffer formed by Tr_1 and Tr_2. The triode operates in constant-current mode by the bootstrap connection (C_1) to improve linearity and achieve the maximum gain, in spite of the relatively low supply voltage and of the lack of the usual cathode capacitor.

Typical applications for this circuit include 600Ω headphone driving and line stages in vacuum tube preamplifiers. Measurements on this stage show a gain of 30dB, 100V/μs slew rate, 270Ω output impedance and 0.15% distortion at 1kHz with a 10Vpk-pk output signal and 10kΩ load (mainly second harmonic).

Having no overall feedback, the circuit is virtually free from instability (even when capacitively loaded) and transient intermodulation distortion. However, the application of 10dB of negative feedback (smaller diagram) reduces the output impedance below 100Ω and the distortion well below 0.1%, with a gain of 20dB, which is a typical value found in line amps.

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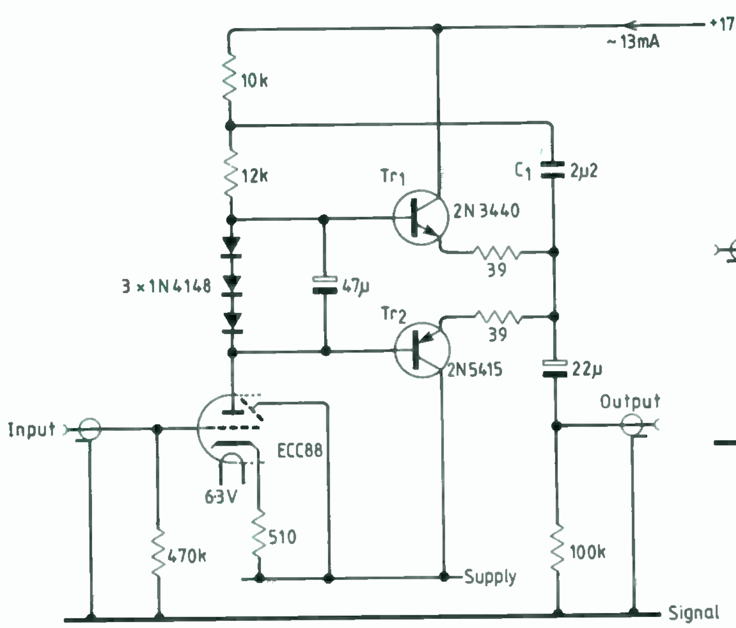
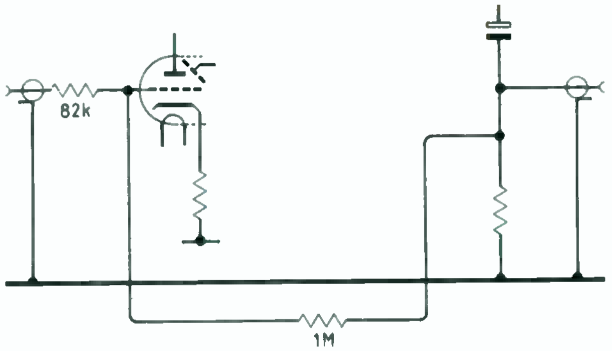




Designing with cad

Computer-aided design of printed-circuit boards on a PC is becoming commonplace. Mike Walsh, a cad consultant, describes the process.

Until about seven years ago, computer-aided design facilities were limited to the large design departments of multinational companies. This limitation was due, in the large part, to the high cost of the computing power required by cad programs. The introduction and rapid adoption of the personal computer, however, influenced a sudden surge in the number of cad applications available at a price well within the reach of even the smallest company; the innovative design of these products offered close to mainframe facilities on the humble PC.

DESIGN CYCLE

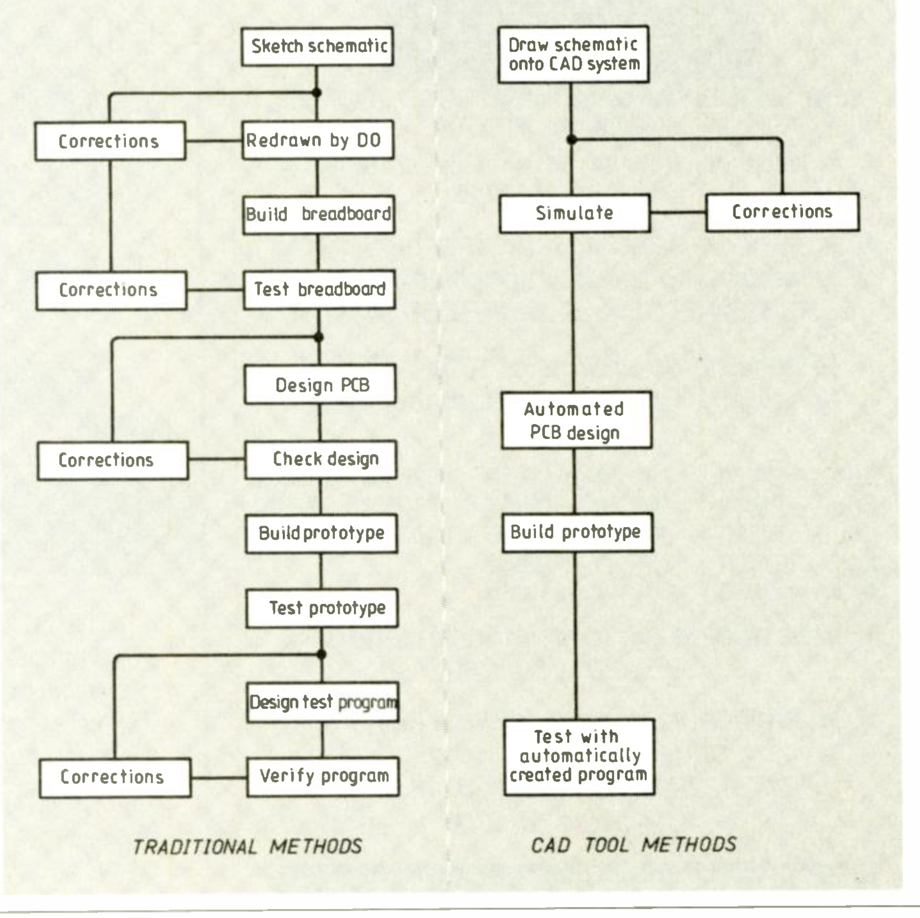
Nearly all the activities that the average engineer indulges in when designing a circuit or product can be enhanced by the use of cad, as can be seen in **Fig.1**. Indeed, some disciplines have only become practicable because of cad. Let us consider a typical design for a moment and mention the application of automated methods at each step.

Normally, the engineer would construct a block diagram of his design before deciding how to implement each function. Schematic capture systems invariably offer a hierarchical approach, allowing unlimited levels of "black boxing" down towards the component-level circuit diagram. Verifying that the circuit works to specification conventionally requires the building of a prototype and subsequent bench testing. The cad approach tackles this requirement by using a simulation of the circuit – either analogue or digital as appropriate. Modern circuitry often uses roms and PLDs to implement glue logic: constructing fuse maps by hand is a tedious and error-prone operation and is much better automated. The design may also contain asics (application-specific integrated circuits) and many manufacturers now offer tools which allow their design to be carried out by the engineer using a Personal Computer.

Production requires that a PCB be designed and again, a range of packages is available to assist in this task. Assembly of the design into a casing or rack has implications with regard to heat dissipation. Thermal analysis packages can provide an early indication of potential dissipation problems which would otherwise cause malfunction or poor reliability. Finally, the product has to be tested and even here, tools are available to automate the task.

Although, as can be seen, the computer can help at every stage, one more important point should be appreciated: that of integration. In many cases, each of the tools mentioned above is integrated with the others in such a way that there is a flow of data possible between them. This is one of the major benefits of cad, since it minimises the chance of errors creeping into the design process. To best appreciate this facility we might regard the schematic as the "documentation" or "specification" for the rest of the design. Under no circumstances may we alter design data anywhere other than in our schematic.

Fig.1. Traditional and computer-aided design processes compared.



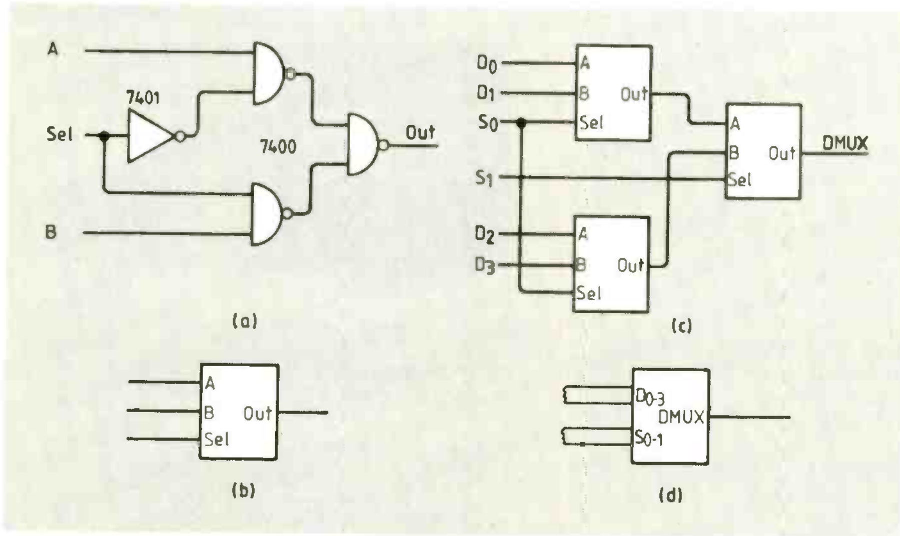


Fig.2. The hierarchical method of information capture. Four levels of the hierarchy are shown, starting with the circuit at (a) and ending at (d) with a composite symbol incorporating several (a) circuits. The final diagram using symbols as at (d) is uncluttered with unnecessary detail.

Thus, if the schematic is correct, everything else must be correct. This is, of course, an ideal and most cad systems allow a less formal interaction to better match a designer's more normal working methods.

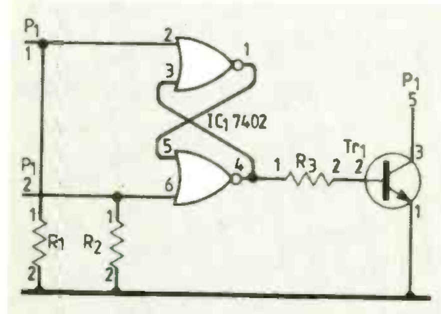
To see how each activity discussed above benefits from the application of cad I will elaborate on the principal advantages to be gained in each discipline. There are, incidentally, one or two seeming disadvantages at various points, but these usually turn out to be a matter of changing one's thinking process to accommodate new methods of working.

Schematic capture. At the start of most designs comes the initial sketching of the circuit on paper, either directly at the component level or using a black-box representation. Hand drawn schematics are then either tidied up or, often, completely redrawn by a different department. When using a cad system in this environment an ideal method is to design directly on the screen, dispensing with the manual approach completely. This ideal is often not followed precisely since the brainstorming approach to circuit design is often quicker and easier, using traditional methods. But, the sooner the design is entered on to the cad system, the sooner one can get the benefits of all the supporting tools. Thus a certain amount of discipline is necessary to try and minimise the paper and pencil exercise, since it represents a duplication of effort. Most schematic-capture systems provide a means of abstracting information in the form of a hierarchy. Each layer or level of the circuit can contain black boxes representing circuits at a lower level: **Figure 2** shows an example of this type of construction. For large designs this representation is extremely advantageous, since large amounts of detail which may otherwise cloud the understanding of the circuit can be hidden inside the boxes. Features available from the cad system allow traversal up and down the hierarchy at will.

The new user often finds capturing the schematic time consuming when compared with more traditional methods. The important point to grasp here, however, is that not only is the result a quality hard-copy plot, but that a database of information about the design is being built. Thus, at the expense of some extra time, the information which will be used by the rest of the cad process has been stored by the computer.

Libraries. During schematic capture, frequent use will be made of standard schematic symbols such as gates, transistors and resistors. A selection of these components is normally provided by the manufacturer of the cad product, but the user should be wary of the size of library supplied, since creating new symbols can be time consuming; some lower-cost systems are supplied with a few hundred symbols – some with several thousand. There is frequently the need to create new symbols, however, since designs often use innovative components that the cad manufacturer may not have anticipated in his libraries. There is usually a fully graphical approach available in the system to fulfil this task and various items of "intelligence" are normally added to enable the symbol to convey all the information required to other sections of the cad system.

Netlists. Not all of the schematic data is normally required by the other elements of the system; for example, most of the graphical data is simply for human recognition. To drive the rest of the design process, it is usually enough to have a list of components and their associated connections. This type of structure, called a netlist, is derived by processing the schematic database and may either be held in the machine as ASCII text or as a binary data base. **Figure 3** shows a simple schematic and its related netlist.



Components	Connect
7402: IC1	UN000000 IC1 5 IC1 1
Res: R1, R2, R3	UN000010 Tr1 2 R3 2
NPN: Tr1	UN000006 R1 1 IC1 2 P1 1
Plug: P1	UN000008 R1 2 R2 2 Tr1 1
	UN000005 IC1 6 R2 1 P1 2
	UN000012 Tr1 3 P1 5
	UN000009 IC1 4 IC1 3 R3 1
	End

Fig.3. A simple schematic diagram and its associated netlist.

Electrical checking. The first benefit one receives from having patiently entered the schematic is the ability to check all sorts of electrically related items; for example, that no outputs have been shorted together or that there are no floating inputs or that pull-up resistors have been added to open collector outputs – and so on. High-end systems are able to provide additional facilities such as fan-in and fan-out checking of logic gates.

Simulation. Both analogue and digital circuits can be verified for correct operation by using the appropriate simulator. The traditional method of breadboarding a design to test it is no longer a necessity. Indeed, in the case of asic designs it is not even practical to verify the functioning of the circuit in this way.

Digital simulators. The operation of the circuit is emulated by applying a series of stimuli (input signals) to a computerised model of the circuit elements and evaluating the response; the simulator software has algorithms within it that can emulate the behaviour of the gates in the design. Many simulators can only model a small range of "primitives" such as Nand, Nor and Inverter in this way and cad suppliers will provide libraries of models which build up the simulation of more complex elements like counters or registers from these primitives. Alternatively, the user may create his own models. The accuracy of the models supplied or constructed is of paramount importance, since a behavioural inconsistency will cause the simulation results to be incorrect.

It may seem at first sight that simulators only need to be able to handle logic states of 0 and 1, but this would limit their effectiveness unnecessarily. In the case of a tri-state driver circuit, for instance, the simultor must also emulate the high-impedance state with, for example, a Z level. There are several other situations where the accuracy of the simulation can be enhanced by defining other states such as resistive or supply strength and, finally, an unknown or "X" state is usually used when the simulator is unable to compute the exact state. Thus, the capabilities of commercial simulators are often described in terms of the number of states they can handle. Low-end products start at between 6 and 12 states and go through to the high end of 32 or greater states. Table 1 shows the states and levels used by a commercial 12-state product. Simulators of this type will normally also handle timing and can identify errors such as setup or hold-time infringements for flip-flops or latches.

Table 1. States and levels for a 12 state simulator.

Level	High	Low	Unknown
Supply	S1	S0	SX
driving	D1	D0	DX
resistive	R1	R0	RX
high-Z	Z1	Z0	ZX

A word of caution, however: simulation at the one extreme can show design problems that no amount of bench work ever would and, in this case, the technique is extremely valuable. But, at the other extreme, an inexperienced or careless user who accepts blindly the results that a simulator gives can run into deep trouble. Simulators are, after all, only giving an approximation of the way a circuit will behave and are clearly unable to react to the external influences which a real design needs to tolerate, such as power-supply variations and noise effects. Thus, the designer must still follow good engineering practice in his design methods.

As a general rule, simulation should not be used as a way to synthesize logic – only to analyse it.

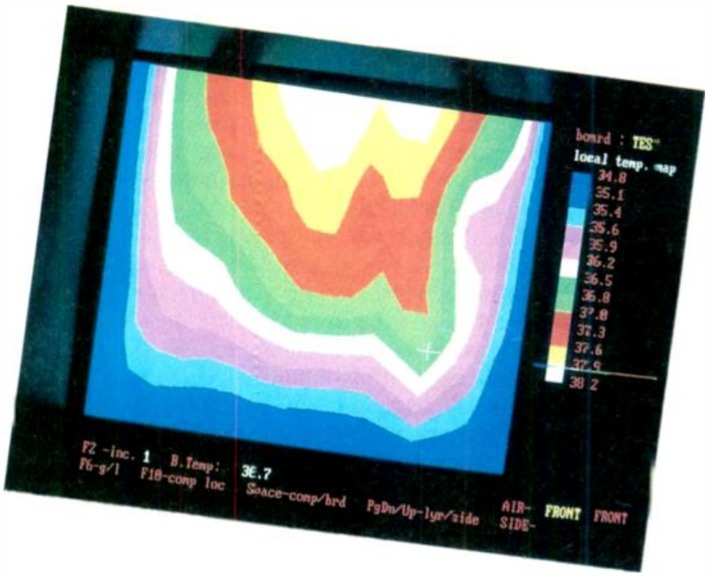


Fig.4. A typical isothermal display from a thermal-analysis package – Thermax, from P-CAD EDA.

Analogue simulation. Complex analogue circuits can be a nightmare to design and test, particularly when one is faced with verifying performance over temperature and component tolerance. This is one region where the analogue simulator can be invaluable. Such products use iterative, numerical techniques to solve the complex equations describing the circuit and can then produce a range of results such as transient or frequency-response data or voltage-transfer functions. Analysis over a range of temperatures can quickly show design problems and so-called Monte Carlo analysis can show the circuit's sensitivities to component tolerance.

Once again, simulations of this sort are only as good as the models supplied. Modelling in this case refers to the types of model used to represent active devices and the range of devices that have been characterised with this model. Some simulators also provide special tools to allow the user to develop his own models.

Mixed-mode simulators. In an ideal world, a mixed analogue/digital circuit would be simulated as a whole using a composite or mixed-mode simulator. In practice, such simulators are rare and require considerable computing power, so the PC user will normally find himself testing the digital and analogue portions of his circuit separately.

PLD DESIGN

Programmable logic devices have become an economic and popular way to reduce the IC count in designs. Miscellaneous logic functions can be "mopped-up" into one or more PLDs, thereby reducing space and cost and increasing reliability. As PLDs have matured into relatively complex devices, various tools have been developed to allow the design engineer to implement his requirements quickly and accurately. These programs provide the designer with the ability to define his logic requirement in terms of what could be considered a high-level language using truth table and/or state-machine syntax. The PLD program will then be able to derive the correct fuse maps to implement the functions required. Logic minimisation algorithms are frequently included in this type of program to allow the user to concentrate on the result and let the program determine methods of achieving it efficiently. Simulation of the completed PLD is also normally provided, although it may not necessarily be integrated with the simulation tools above.

PCB DESIGN

Probably the one area where most products exist to computerise the task in question is that of printed-circuit board design. The very low-end products offer what we could call an "electronic taping' facility, meaning that the traditional technique of laying tape down on to Mylar has been duplicated on the computer, with the added advantages of easy editing and redesign. Medium to high-end products offer much, much more in terms of a wide range of interactive editing functions, facilities to work with ground planes, multilayer board capability and surface-mount technology support. Additionally, many products now provide automatic placement and automatic routeing tools as well as real-time short-circuit detection and even real-time design-rule checking. Once again, the power of the cad approach derives from the integrated design cycle, where the PCB design function accesses the initial database constructed from the schematic.

Good PCB design tools normally have the ability to drive pen plotters and photoplotters for the creation of artwork and the derivation of suitable data to drive automatic drilling machines and automatic insertion equipment.

THERMAL ANALYSIS

A topic that many designers ignore or leave to trial and error is the thermal performance of the board, either alone or as part of the final assembled product. Until recently no suitable automated tools were available to address this topic. Whilst not of importance to everybody, poor thermal design can have an adverse affect on the performance and reliability of a product. Products are available for use on the PC which allow the user to generate isothermal maps for the board in question when considered either in a two-dimensional manner or in full 3-D. **Figure 4** shows an example of the output available from a product of this type.

TESTING

Lastly comes the subject of verification of production pieces. Again, the integrated approach can be of assistance since much of the information about the location of components and tracks can be derived from the PCB database. The test patterns should also be obtainable from the results of the simulations which have, of course, characterised a fully functioning system. It is simply a case of massaging the data to produce a tester program.

PLATFORMS

I think that a few introductory comments on the types of machine being utilised in the field of electronic cad are in order at this point. By far the largest number of products are intended for use on dos-based Personal Computers, although there are certainly useful products to be found running on Apple equipment and even the BBC micro. In general though, cad programs are demanding on the resources needed to run them expeditiously. Ram, disc capacity and operating speed affect the resulting performance; thus, the latest 25MHz (or even 33MHz) 80386 machines with plenty of memory will provide the optimum system. But this general statement needs some clarification: if an application is relatively undemanding, in terms of, say, size of schematics or PCBs, and if the cad system is not going to be used day in day out, then a more modest approach is perfectly adequate.

Also, designers of cad products running under dos are always faced with a limitation of 640K memory and normally take special measures to create their databases in a compact manner. They also understand that only relatively few users will be using state-of-the-art hardware and are at pains to implement program operations as efficiently as possible.

Many of the tasks the cad user performs are graphical in nature; that is, sitting at the terminal drawing a schematic or PCB. The resolution of the display and the capabilities of the graphics card driving it are of great importance here. A low resolution will produce "chunky" graphics and the screen will only be capable of showing a small area of whatever is being viewed. A poor display is tiring to view and frequent pans and zooms will be required if the resolution is low. Once again, it depends very much on the application as to whether this is a problem. A workable range of resolutions is from the EGA standard of 640×350 to the very high end of 1280×1024.

This article has attempted to show how cad may be utilised in the design flow of a typical electronic product from concept to production. As we have seen, almost every area can be enhanced in term of throughput, reliability and accuracy by the application of the PC-based design system. The integration of the various tools that go to make up the end-to-end design approach is also very important to obtain consistency of operation and to minimise translation errors. There are many systems on the market that address individual items in this design flow and other systems that address groups of design steps. The potential user should be aware by now that the more heavily integrated the application, the easier it will be to get optimum performance and have available a range of upgrade paths as requirements grow. Thus, when embarking upon the initial purchase of a cad system or even upgrading from one product to another, time spent evaluating the integration of the system well spent.

Mike Walsh runs his own independent cad consultancy specialising in training, software development and support of electronic cad products.

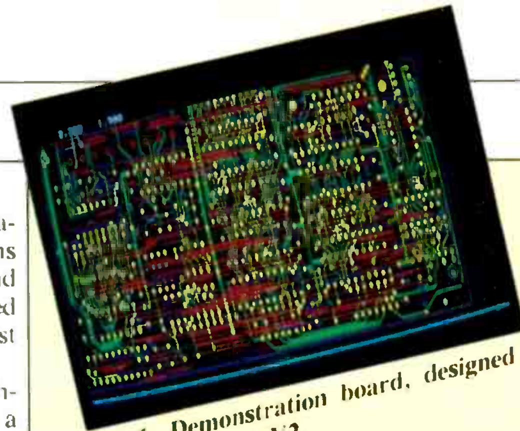


Fig. 1. Demonstration board, designed using PC Turbo V2.

PCBTURBO V2 is Instagraphic's second-generation design and draughting software package for printed-circuit boards.

The demonstration software did not have the full functionality provided by the retail version. Component libraries were not included, only three of the main menu options were usable and all of the output options were intentionally disabled, including storage of constructed components and trial layouts. However, the facilities provided by the package were sufficient to demonstrate the capabilities of the retail package and to identify its limitations.

PCBTURBO V2 is a specialised draughting tool for the production of between one and six layers of circuit wiring on a single board. The maximum board size that the system can deal with is 32in by 32in although, at maximum scaling, the display screen provides only 32in by 15in.

A library of standard component drawings is provided with the retail software but, if the demonstration software is representative, all 14-pin dil devices will use the same component model. Pin numbers are not provided and the wiring connections cannot be specified explicitly. All wiring 'connections' are made manually and there is no user reference for identifying individual wires.

Getting started

If the computer configuration matches the requirement, then installation is quite simple. The hard disc must be drive C: because the software specifies the directory structure and the path internally.

There is ample storage space on two floppy discs for the demonstration software, so that with a little reorganisation of the files it could be run on a twin floppy disc system. The full version includes component libraries and will need the hard disc capacity for storing finished layouts.

Batch files are provided for automatic installation and a further batch file sets up the path structure, loads the device drivers and invokes the program.

PCBTURBO V2

A specialised tool for 32-in square boards of up to six layers

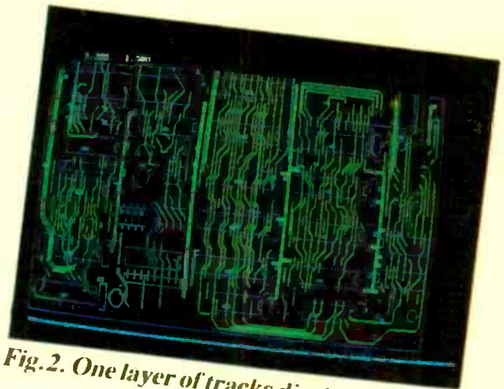


Fig.2. One layer of tracks displayed.

Display screen resolution

The package can work with CGA graphics, but the resolution is not adequate for professional use and the four colours available from a CGA palette are not enough to distinguish individual layers when they are superimposed on the screen.

Two EGA screen formats are available: the first requires 64Kbyte of screen memory and provides a resolution of 640 × 200 pixels in a range of 16 colours; the second uses 256Kbyte of screen memory and provides a resolution of 640 × 350 pixels in the same colours.

A board length of 32in accommodated on a single screen provides a resolution of 32/640 = 0.05 in, which is insufficient to display small-diameter holes or thin tracks at this scale.

Six distinct drawing scales are provided, the smallest devoting the whole screen area to a view of 0.6in × 0.3in of board space – this provides a maximum resolution of 0.6/640 = 0.001in. Working at this resolution produces very satisfactory results.

Screen scale factors of 4 or 5 provide a working compromise between available resolution and sufficient board space to display several adjacent components.

Some visual aspects of the scaling were noticeable – circles appeared oval and short fat components rotated into long thin ones. Changing from EGA256K to EGA64K altered the aspect ratio of the Demo board. None of these effects distort the output and they are preferable to a loss of resolution.

PCB design facilities

Separate layers are provided for silk-screen printing and for copper circuits on each side of the board; these four layers can be extended to eight with four additional internal wiring layers. Each layer is displayed in a different colour and layers may be superimposed in any mixed combination. The display colours used for each layer are not selectable.

The silk-screen layer is used to specify the outline of a board, components then being positioned on the board with their terminal pads. Layers are then wired up manually or by using the autorouter.

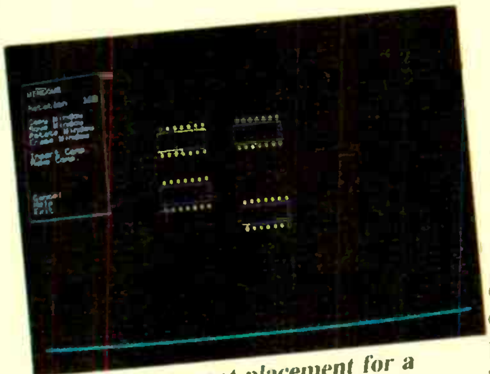


Fig.3. Component placement for a simple board.

Relative positioning of the components determines the track lengths. Wire crossings can be largely avoided by routeing horizontal tracks on a different layer to the vertical tracks. Each conducting layer may be plotted out separately for PCB production.

The output plots obtainable include: silk-screen plot; top and bottom side plots; a drilling drawing; top and bottom solder-resist masks; internal layer plots; and a multilayer plot. The outputs can also be recorded in computer files for record purposes or for sending out to a bureau for plotting.

Design notes may be recorded in the system using the built-in word processor.

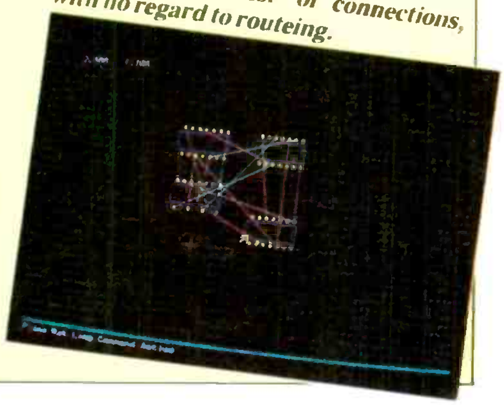
> **EQUIPMENT REQUIRED**
>
> Prospective PCBTURBO V2 users need a minimum of an IBM PC/XT or compatible, with 640 Kbyte of ram, a 10 MByte hard disc, one 5.25in floppy-disc drive, one RS232 serial port and an EGA graphics adaptor with compatible colour monitor.
>
> A mouse or tracker-ball pointing device is required for easy graphics-screen manipulation and for making selections from the pop-up menus. Alternatively, the arrow keys can be used for menu selection or for locating the cursor. Software drivers are provided for a number of serial pointing devices. A high-resolution device is required for graphic output.

Operating features

The top line of the screen can display the X-Y co-ordinates of the cross-wire cursor position, as measured from the bottom left corner of the largest viewing area. It can also show the current position of the cursor relative to a local origin at the centre of the viewing screen. This latter facility is a convenient ruler for measuring distances in Imperial or metric units.

When the scale of the display is changed, the centre of the field of view on the new screen is placed at the position of the cursor on the previous screen. The screen can be 'adjusted' in position at the current scale. The planning facility moves the view in steps of half a screen size to left and right and up and down. As soon as this is realised it is no longer difficult to appreciate where the screen is located on the board.

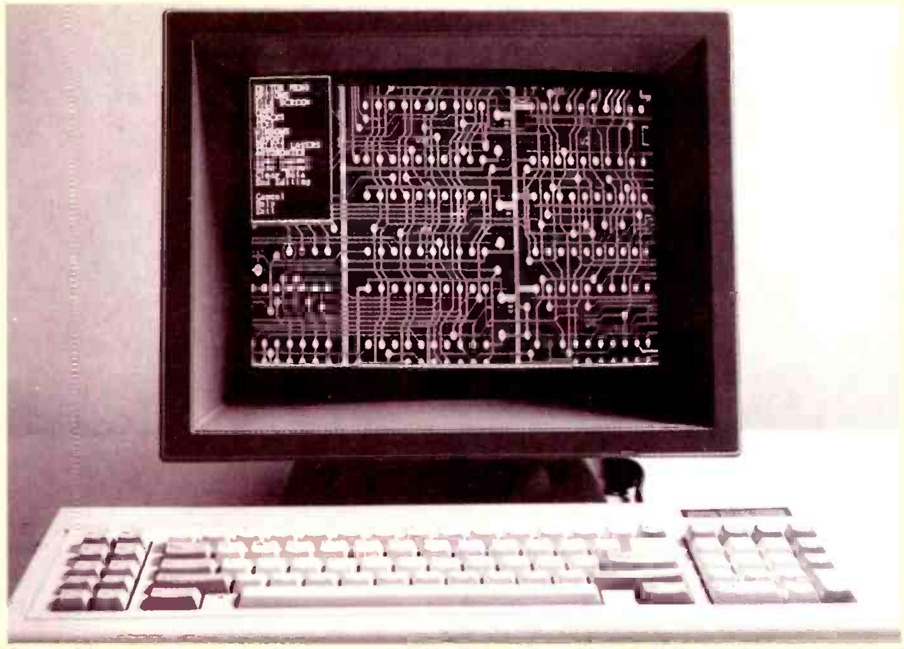
Fig.4. The "ratsnest" of connections, with no regard to routeing.



The pop-up menu windows provided are excellent. However, it is more convenient to use the pointing device for graphics and the arrow keys for menu selection.

Autorouteing appears to have been a recent development – its facilities are not available on manually positioned tracks. Separate 'ratsnest' lines are first drawn manually, directly between the terminal points. The autorouter is then activated to re-arrange those lines so that they avoid the obstacles on the straight path between the ends. The autorouter is not infallible and any lines that it is unable to deal with must be removed and re-arranged manually.

When a new PCB is being laid out, a silk-screen layer is used to define the board outline. Positioning prepared component outlines on this layer automatically provides, and displays, the associated pads on another layer. A menu facility called 'Windows' is used to capture components in a square 'net' so that they may be moved about on the board and copied.



Part of demonstration board, "zoomed", of Instagraphics' PC Turbo V2.

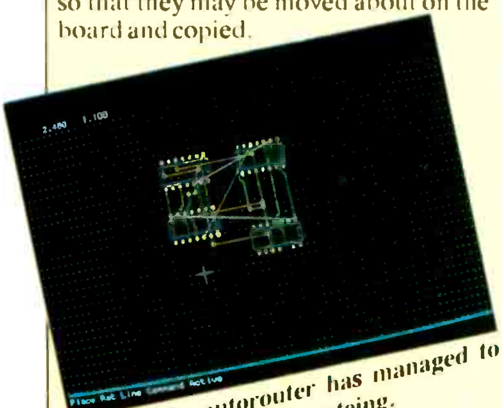


Fig.5. The autorouter has managed to complete most of the routeing.

Text of different sizes may be placed on either the component legend artwork or in copper on either side of the board.

A point to watch: the board is viewed from below and, if the dil component drawings are unpolarised and unnumbered, then lateral inversions could result in incorrect wiring. It was not possible, on the demonstration package, to check that the plotter outputs of the various layers were as viewed from the appropriate side of the board.

Repositioning the view of the circuits on the screen requires the whole screen to be redrawn, all of the selected layers and filled-in colours. The redrawing process can be speeded up with the quick-draw facility, which displays coloured outlines instead of filled in tracks; the speed gain is significant but not large.

The software does not appear to move a viewing window over an extensive precalculated layout; it simply redraws a different portion of the layout – each layer in turn.

Minor problems

The tracks are made up from straight segments, with adjacent segments rotated about the centre of the track width. One result of this is that the wider tracks can have some severe notches in them at the corners. These should be 'patched' up, at high magnification, with tiny track segments to maintain the current rating of the track.

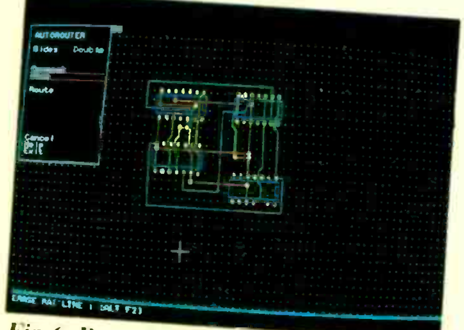


Fig.6. Rest of routeing completed manually.

It can be difficult to erase lines if they have been wrongly placed.

The Track Resize and Break facilities did not work on the demonstration package.

There were the usual minor discrepancies between the manual and the actual system behaviour – for example, the book said Ctrl-F6 would erase an arc, whereas the footnote on the screen said [D].

In practice, the layouts and tracking will be prepared from a circuit diagram for simple boards and from a wiring list for more complex ones. A wiring list would be an ideal input medium for a package of this kind; the computer could provide a data base which stored component pin-out information.

Value for money?

To use the package, you will need at least £1200 for the computer system and a minimum of £600 for the simplest plotting device. The software itself retails for £695. Thus, an investment of at least £2500 is needed. Offsetting this against labour costs would not be difficult to justify if artwork for more than a few PCBs has to be produced.

Facilities provided by the package are limited to the production of artwork. Circuit design and development is a separate activity which has to be completed before the artwork can be started.

However, the package performs a useful function, and it will speed up the production process. It will find a ready market in the smaller electronics companies who need the services that it can provide at prices they can afford.

It can be operated by technical staff who do not have the extensive knowledge of circuits and components that is needed for the full design process. R.L.

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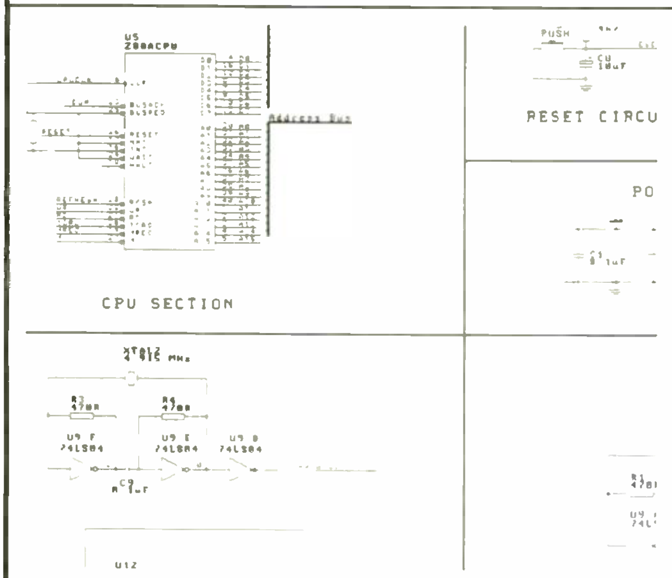

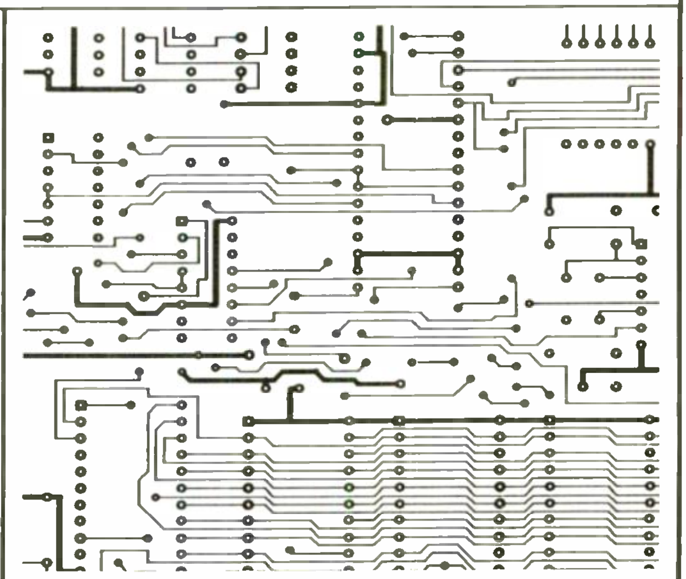

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Starting cad

If you are about to take the plunge into computer-aided design techniques for electronics, start here: Mark Pavitt of Microtel has the water wings.

Computer-aided design (cad) has been with us now for several years and, as with all technological advances, has matured with a process involving many brave failures. These have sadly led to many conceptions and misconceptions that serve only to cloud the real issues for the newcomer. The fact is that cad is a reality which no engineer can afford to ignore. It is therefore the objective of this discussion to present a resumé for the engineer who is about to become involved in cad. The first element in any such discussion must be a definition of objectives.

Objectives of a cad system

The first objective of a cad system is to achieve an improvement in design efficiency. This begins with the capability to emulate the traditional tools of the manual designer. A computer can easily reproduce the function of such aids as rulers, compasses and set-squares, but can additionally provide tools which have no manual analogy. When combined with a user interface which provides immediate access to extensive information about the design and allows easy editing of such information, an improvement in design efficiency is bound to result. The manipulation of information is undoubtedly one of the great strengths of cad systems and this leads to a far better overlap between the activities of the design process. An engineer may wish, for example, to complete critical layout features before passing the design on to a PCB layout artist. With cad, this is simply a question of transferring the layout between two computers. The final feature of a cad system which improves design efficiency is the automation of design tasks, which range from simple tools for the automatic numbering of components to the advanced tools now available for automatically designing the actual layout of a circuit.

A second objective when installing a cad system is to improve the quality of a design. The old adage that computers never make mistakes may not be entirely true, but is certainly a major aspect in the use of cad to improve quality. The system can monitor the designer's progress according to a set of design rules and identify potential infringements, which can range from the connection of two output pins to the placing of tracks too close together.

An adjunct to the quality issue is that of design maintenance. Since very few designs are completed from concept to hardware without modification, a stringent set of documentation standards is a requirement. A change at the circuit diagram stage, for example, will have implications for the layout and probably for tabular documentation such as the parts list as well. Maintaining documentation is notoriously prone to human error in manual systems, but is a task which is easily automated in an integrated cad system.

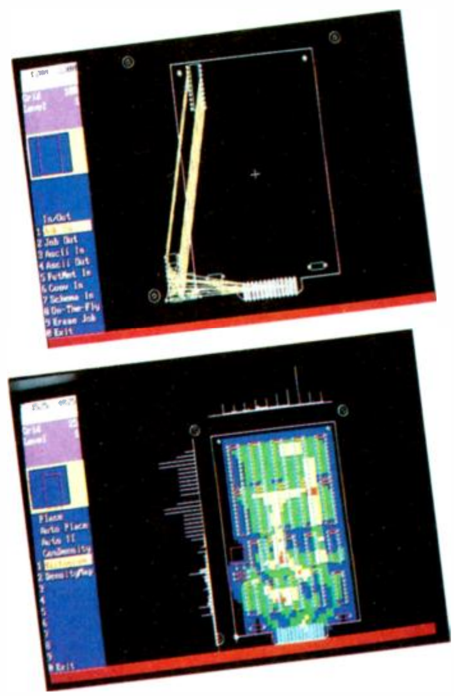

Fig. 1. Placement routine. Partial manual placement is shown at (a), while (b) shows full placement with connection density map and histogram.

The final key objective in the use of cad is the improvement in communications which can be achieved with computers. Since all the information for a design is contained in some form of database it can be easily disseminated among the design team, where information can be automatically extracted in its most useful form. The other great advantage in this form of storage is that, being in a machine-readable format, it is relatively easy to generate output in a form which can be used to automate the manufacture of the hardware. Outputs suitable for driving photoplotters, numerically controlled (NC) drilling machines and automatic test equipment are all possible using cad.

Terminology

The best way to introduce electronic cad and the inevitable associated jargon is to consider a design example. The first task is clearly one of input: the designer's ideas must be communicated to the system. In cad, this is known as "schematic capture" and is simply the generation of a schematic diagram which represents the circuit. A typical schematic-capture package offers the designer a library of parts which he or she may select and place on the screen. Once the parts have been placed, a pointing device such as a mouse may be used to draw in the connections until a complete circuit schematic has been created. This graphical representation of the circuit must next be converted into a precise connectivity specification known as a "netlist". The term "net" (or "node") is used to describe a group of connections within a design. For example, the "ground net" specifies all points in the circuit which are connected to ground. The netlist assembles all nets and parts together into a format suitable for transfer into the next module of the cad system.

Although the vast majority of electronic designs are constructed on printed-circuit boards, the concepts behind electronic layout apply equally to hybrids and even IC design. Having taken in the netlist, a typical layout package will present the designer with a display showing the required parts with connectivity identified by straight lines between pins. At the outset no particular placement is established and, typically, the parts are stacked up on top of each other (**Fig.1**). The first task which must

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be confronted is therefore the placing of the parts within the design outline. A basic cad package will offer a manual capability which is analagous to the traditional process, while more advanced packages may offer tools to automate the task.

Once placement is complete, the point-to-point connections (known as the ratsnest) must be converted into physical conductors. Like placement, this may be done either manually or automatically (or a combination of the two). Typically, design-critical tracks such as high-speed signals or power connections must be routed manually at the outset. An autorouter may then be used to complete the bulk of the connections. Finally, manual alterations may be required to complete and optimise the layout.

The final stage of the layout process is the generation of the output necessary to produce the hardware, which is generally known as computer-aided-manufacture (cam). The required output may be of three different types. Firstly, artwork must be generated. This includes photoplotted artwork delineating the conductor scheme for photo-lithography and pen-plotted artwork for design record and assembly purposes. Additional artworks may also be required for items such as a component silkscreen or solder-resist mask on a PCB. The second type of output that is needed is the statistical information pertaining to the design. This might include parts lists, job dimensions, layout area, component density and drilled hole count. Finally, output is required to automate the production process. Control of NC drilling machines, pick-and-place and automatic test equipment is possible.

This overview has illustrated each stage of the design process in general terms. It is now appropriate to discuss the concepts involved in more detail. The discussion will be divided into two parts: schematic capture and layout.

Schematic capture

As I have said, schematic capture is the process of converting a designer's ideas into a circuit schematic. There are two fundamental approaches to this process. The first of these is the sheet methodology, in which the display becomes a sheet of "electronic paper". The design is then assembled into a set of such sheets, which are exactly analogous to drawings laid out on a desk. Connectivity may be defined between sheets using a suitable schematic symbol so that circuit elements on different sheets become connected within the netlist.

The second approach is the hierarchical methodology. The concept of the sheet is the same, but the sheets are stacked up on top of each other with hierarchical access between them. This means that circuit primitives may be defined at a low level in the hierarchy and are subsequently organised at higher levels until the top level constitutes a simple block diagram of the design.

Another feature which characterises a schematic-capture package is its library organisation. Each entry in a schematic library contains detailed information about a part; this includes not only a graphical symbol, but also electrical information such as input and output identification (to offer a checking capability) and implied connections such as power and ground which may not actually appear on the diagram.

While the methodology and library form the hub of a schematic-capture package, it is completed by a set of tools for the organisation and connection of parts, either emulating manual design aids or offering unique cad functions. An example of such a function is the ability to define a group of parts and manipulate the whole group at once.

In addition to a powerful set of tools, the user interface of a schematic-capture package may offer certain features for the automation of design tasks. A macro capability is one such feature. This allows a set of operations to be organised into a sequence which can be replaced at a single keystroke. Using this technique, laborious command sequences can be easily automated.

Layout design

A layout package takes as its input a netlist (either manually generated or derived from a schematic-capture package). The design is then processed using a set of tools for component manipulation and connection. Finally, output is generated in the form of artwork, CNC datafiles and design documentation.

A layout package in its basic form allows the user to create and organise a design database through a graphical interface. This database is organised as a set of levels which may be individually or globally manipulated. It is important to distinguish between a database level and an electrical layer, since confusion between the two often arises. An electrical layer is a conductor plane within the design. Hence single layer, double layer and so on. In contrast, a database level is a design plane which may contain not only conductor information but also virtually any graphical information pertaining to the design.

Having defined the nature of a cad database, it is necessary to consider the organisation of the information within it. There are three object types to consider: graphical objects, electrical objects and part objects. Purely graphical objects are used to complete the presentation of the design and include dimensioning lines, alignment symbols and free text. Electrical objects are also represented graphically, but have some form of electrical significance, such as tracks, copper areas and the board outline. Finally, part objects define the actual components in the design. A part definition includes both graphical information to identify the footprint of the part and electrical information such as pin assignment for power connections and gate information, which is used by certain automatic routines which will be discussed later.

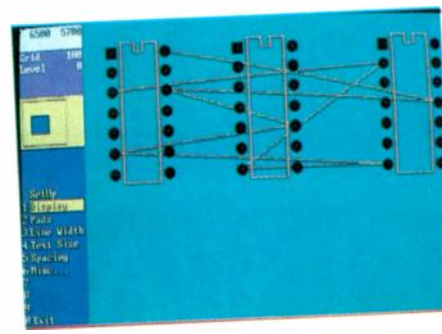
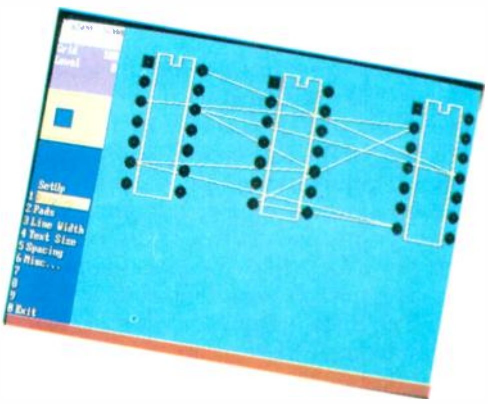


Fig. 2. Length minimisation – before (a) and after (b).

Placement. The first set of tools which the layout designer is likely to encounter is the placement set. The placement of a layout is in many ways the most critical part of the design process, since errors at this stage will have a detrimental effect on the track layout stage later. The key concept in the placement task using cad is that of connection length. As a general rule, the designer will always attempt to minimise the connection path between components. This may seem obvious, but there are certain subtleties associated with cad which are important. Consider the ratsnest display, which is a set of connections defined by the netlist. But consider further a multi-connection net such as V_{CC}. The connections to the V_{CC} net are pre-defined by the netlist in an order that may well not be ideal for the particular placement scheme chosen by the designer. **Figure 2** shows how a cad system can automatically reorganise the connections to minimise the connection length. Clearly, this has no effect on the connectivity but is a critical indicator towards the routeability of a design. The concept of automatic length minimisation may be extended to that of pin and gate swapping – a feature which allows input pins to logic devices to be swapped to reduce connection length. Whole gates may even be swapped around in the design in an attempt to achieve the shortest connection scheme.

The process of placement begins with design-critical items such as edge connectors, high-voltage parts, thermally critical components and RF devices. These must always be placed manually by the designer and fixed in place so that no automatic function can subsequently move them. The remainder of the parts may be placed either manually or automatically.

Routeing. Once placement is complete,



the next phase of the design is the conversion of the connections into tracks. When performed manually the operation of a cad system is closely analogous to the use of tape in a conventional layout. The great advantage which cad offers is the speed and accuracy of manual track placement. Editing is also considerably simpler, with modifications being quickly and easily made to 0.001 in resolution.

The alternative to manual routeing is, of course, autorouteing. Unfortunately, there are many misconceptions surrounding autorouteing tools, and opinions vary from the deeply suspicious to the devotedly enthusiastic. The truth is that what an autorouter can do for you depends very much on what you need.

Although there are several different approaches to autorouteing, there is one concept which binds all routers together. This is the use of layout feature cost. All routers use a system of feature cost to assess the feasibility of a proposed route. As the name implies, the feature-cost system assigns a notional cost to the various features of a route and generates a total cost by adding each feature up. The route with the lowest total cost is then chosen from the various alternatives. Costed features typically include: vias, routeing in the non-preferred direction, routeing in dense areas of the layout and routeing between adjacent component pins. **Figure 3** shows set-up for autorouteing.

What distinguishes different autorouters is the way in which the feature-cost concept is applied. The vast majority of routers operate on a grid and calculate the cost of each route for successive grid points. The difference between routers lies in the qualification of connections, which is the process by which the router selects the order in which to perform its function. In practice, several passes are performed which have costs optimised for different types of connection.

The routeing process that has been described so far is present on the vast majority of autorouters. There are, however, certain refinements which have achieved popularity in more advanced autorouteing tools. The first of these is the "rip up and re-try" algorithm, which uses the costed-maze principle, but includes the capability to correct earlier mistakes by removing previously routed tracks which are causing an obstruction, routeing new tracks and then re-routeing the ripped-up tracks. This approach has a far greater chance of achieving 100% completion of the layout.

The final role of the layout module is to generate the necessary outputs that are required to fabricate the hardware; in this operation, the organisation of the database into levels is of key significance. Features from different levels can be merged to assemble the information that is required for each output process. A drilling detail, for example, may take pad symbols from one level, a board outline from another and a title block from yet another.

The ultimate extension of these principles is the integration of the design database into a manufacturing environment. Output from the layout package could be used to control automatic production and testing equipment, while maintaining a record for the stock-control and accounting departments. **Figure 4** shows the selection.

Practical considerations

So far, the discussion has dealt with the operation and facilities of electronic cad systems. There are, however, certain important practicalities which must be considered when initially investigating cad, the first of these being hardware.

The CPU in a cad system may be judged according to two primary factors: processing speed and memory capacity. In the context of cad, the clock speed of a CPU offers a good indication of the actual processing speed, since cad makes extensive use of integer operations rather than using floating-point arithmetic. By the same token, arithmetic co-processors may well not offer a significant advantage. The only area where this guideline does not apply is in the field of simulation, which most definitely does require a powerful floating-point capability.

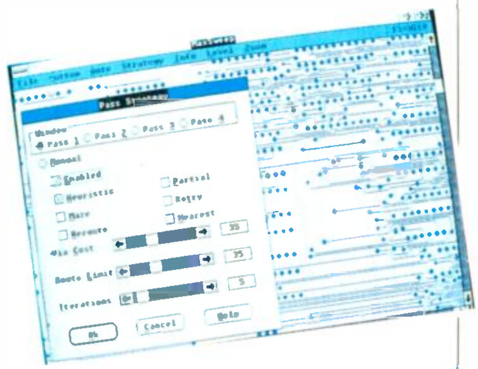


Fig.3. Strategy set-up window for an autorouter.

Fig.4. Selection menu for output to a plotter.

Memory capacity is, of course, the limiting factor in the database size and is therefore significant in the complexity of designs that may be tackled with a particular system. Autorouteing is a particularly memory-intensive activity, since it often requires several words per grid point. On a 0.025in grid, a four layer, 6×6in layout might typically require around 1mbyte of ram.

The next item of hardware to be considered is the display. This is, of course, an important feature of any cad system, but electronics cad has slightly different requirements to its mechanical counterpart. A full-colour display is a virtual necessity, since this is the most effective way of identifying different layers, but outright graphical resolution is not of primary importance. This is because, unlike mechanical drawings, electrical designs consist primarily of simple, geometrical objects.

Finally, the input and output devices must be considered. On the input side, a pointing device of some kind is a great time saver. The majority of systems use the humble mouse with great effect, but digitizing tablets and lightpens may provide useful alternatives. For output, the minimum requirement is a dot matrix printer. While this may be used primarily for printing statistical information, some systems support the output of graphics for checking purposes. If a better graphical output is required, then a pen plotter is essential. This is particularly useful when generating schematic hard copy and can also provide good results for layouts. The final artwork generation for photo-lithography, however, requires the use of a photoplotter, which is the only way to ensure dimensional correctness. In view of the cost of photoplotters (typically several tens of thousands of pounds) most cad users take advantage of plotting bureaux, which can accept job files in machine-readable format.

A second consideration when investigating cad is learning time – very important when evaluating a system and forming an important requirement for most prospective users. If the system is to be used primarily by a single "expert", then the training time required to learn a complex package may be justified by the advanced capabilities of the system. If, on the other hand, the system is for the use of several less skilled operators who may only use it occasionally, then it is quite probably worth sacrificing complex features for ease of use.

Another consideration in cad is the issue of interfacing. The shortcomings of so called "standards" in hardware interfaces are well known and are no less prevalent in software systems. When evaluating a package, the interfaces should be clearly identified and tested for their integrity.

The final issue in a cad evaluation is simply one of capability. It is important to establish exactly what cad can and can't do. This must always be seen in the context of the requirement, but one single principle always applies: cad is quite literally a design aid and must be recognised as such. Cad will never replace engineers and skilled layout artists. It acts, rather, as a productivity tool. Seen in this context, the benefits will become clear to anyone contemplating using computers as part of their design effort. ■

Nettlister and EE Designer III

Two packages for PCB design from Racal-Redac and Betronex Elektronik

RACAL-REDAC NETTLISTER

This program accepts input from the keyboard, mouse or both in any combination. There are two menu panels, one for control and one to add to the display. These pull down at the top right corner and toggle. At other times they are out of sight. A message bar across the top announces the current function and requests action when necessary. There is a full set of ten general actions called by the function keys.

A schematic is built up and the resulting file(s) can be output to a plotter, a printer, a network and to layout-generating software. It does not produce layouts itself, but the schematic, data files and parts list are completed within the package. The data is intended to be passed to Cadstar or certain other programs for generating PCB conductor layers, resist layers and print screens. Cadstar is available with or without an autorouter and in versions for PC-AT and 80386 machines.

The box contains five 5¼in or three 3½in discs, a two-volume reference manual, a study course in paperback, and keyboard templates. The latter comprise a moulded plastics frame for the 83/4-key keyboard and a sheet of sticky labels which have to be cut up and stuck on to the 101/2-key keyboard. In my experience sticky labels either dry up and drop off, or they go slimy and make a mess. A small point, maybe, but it hits your eye every day. They aren't even in sequence. Every one has to be cut up separately.

Installation takes a few minutes only. The user has to modify CONFIG.SYS to include ANSI.SYS and the optional MOUSE.SYS, and it is convenient to add a path to the new subdirectory in AUTOEXEC.BAT. If a proprietary graphics card is in use, and if network software is required, the drivers have to be added to AUTOEXEC.BAT. Instructions for this are explained in detail, including the use of EDLIN, for those not familiar with DOS level working.

The first disc has an installation routine which calls the discs in turn and copies them to the hard disc in a subdirectory REDAC. When they are all loaded a configuration menu appears for the selection of the appropriate display, printer and mouse drivers. Nettlister's own CONFIG.EXE can be called at any time to reconfigure the system. The space occupied on the hard disc is about 1.6Mbyte in 115 files. Finally the user is advised to create a working sub-directory of his/her own and to log on to it.

Self study course

The self study course is very well put together. Three fold-out diagrams are found at the back and can be seen at all times; if it would stay flat it would be perfect. The reader can skip the section dealing with the creation of symbols, but it is well worth following because it is extremely detailed and leads the student gently into the look and feel of the system. The later section on the creation of a schematic gradually moves

The operating environment is an IBM PC-XT, PC-AT or compatible with 512Kbyte ram and DOS 2.0 or later, or one of the IBM PS-2 range of computers. The software supports CGA, EGA, VGA and seven display cards by other manufacturers, including high-resolution models. It supports IBM or Microsoft mouse and 17 pen plotters. Files can be created to interface with other plotters. It will output graphics to an Epson FX series or IBM Proprinter or equivalent dot-matrix printer. Parts lists are plain ASCII and go to any printer.

faster, taking earlier work as needing less and eventually no further explanation. There are a few minor omissions, which I resolved immediately with the reference manual. The company claims that one to one-and-a-half days' work completes the course, and I found this estimate generous.

The manuals are organized in sections. Appendices are not at the back of the book but at the end of the relevant section, as are the error message explanations. There is no index, but all the menu choices appear in the table of contents. Each has a new page.

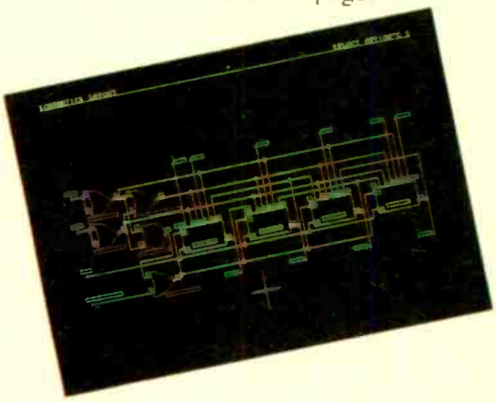


Fig.1. Nettlister: a bi-directional shift register, executed in discrete logic and reduced in scale to put the whole drawing on screen at once. Text would be too small, and it is replaced by small rectangles of appropriate size. The larger rectangles represent hierarchical drawings, one of which is shown in Fig.2.

There are few idiosyncrasies. One is the terminal numbering on the symbols, which is unlike any real component. The component numbering is substituted when components are assigned later. It allows the use of a symbol for more than one component, and facilitates component substitution, but does the operator need to know? Another is found in the library: P12V and N5V and the rest are intuitive supply rail symbols, so why does the 5V supply have to use VCC? It takes two or three minutes only to add the P5V symbol to the library. Incidentally, the parts library only lists digital ICs. I included an edge connector; when preparing an output file for PCB layout the programme asked for a name and number, which I was able to bypass by entering 500 – a random shot. When the parts list was printed out another library number had been substituted, suggesting that the part had been recognized after all.

The overall impression is one of considerable user-friendliness. There is a relatively small number of menu selections, and one easily learns their purpose and location. One calls a programme from the DOS command line for each major function, in effect a third unwritten menu. Other programmes in the Nettlister suite create parts lists, data for PCB layout preparation and so on by question and answer. Anyone who can read a circuit diagram ought to commence productive work on the second day.

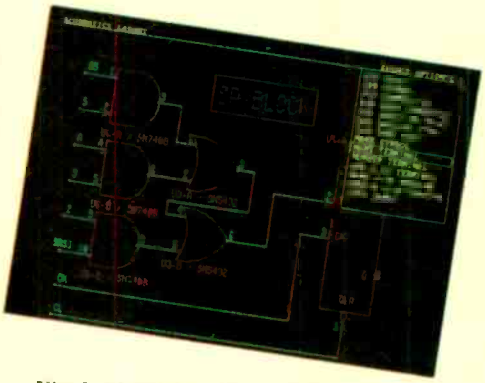


Fig.2. Nettlister: hierarchical drawing, with the menu box displayed. There are four of these in the whole circuit, each stored separately on disc with its own name.

Initializing provides for one invisible and eight visible line types. Five of the visible lines, once laid down, are protected. To alter them one first converts to an unprotected type. These line types apply to text as well as graphics. There are eight assignable line widths, and default values can be changed.

The working area is limited to 8192×8192 DSUs (data structure units), which are definable. In addition the working grid and the optional displayed grid can each be defined by intervals of a number of DSUs. Symbols and connections are located on the intersections of the working grid. Moving the symbol takes the test with it and rubber-bands the connections. Substitution of symbols preserves connections according to the system's own numbering. Labels are automatically incremented as they are supplied: quad gates started ..A increment to ..D and so on.

Commands are selected by their initial letter or the mouse. Routeing is either by mouse or by stepping with the arrow keys. A toggle selects either grid point size or fine DSU-sized steps. There is an automatic back-up at irregular intervals which seem to be tied to the exit form individual operations.

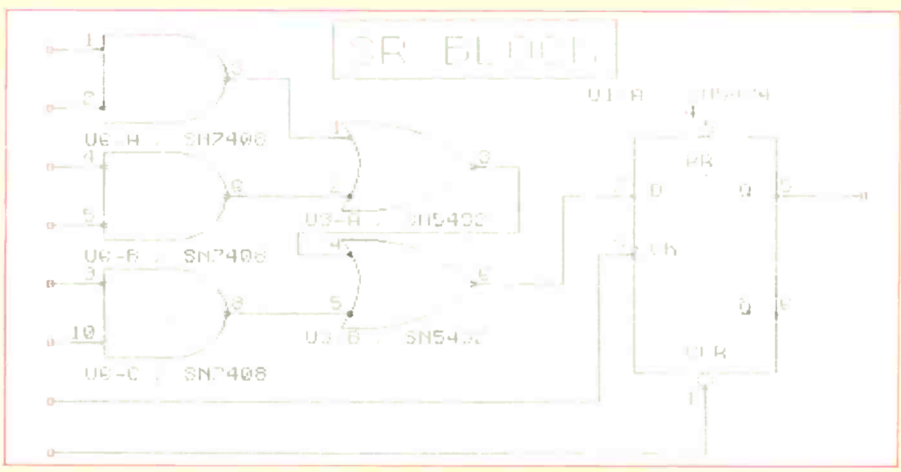
The libraries can hold up to 1023 symbols (236 listed in the manual but 252 claimed by the directory display function) and up to 5280 parts descriptions (759 listed, counting 7400 and 74LSOO as different). No microprocessor chips are included, but there are a few memory chips in sizes up to 64Kbyte. There is a large selection of TTL family devices; I only noticed one omission from among those I have used.

There will almost certainly be occasions when new components have to be created and added to the libraries, and there is a symbol creation program and library editor. Symbol create has two menus like the schematic programme, and some of the choices are the same. Learning one is good preparation for the other. The symbols used are the traditional ones, D-shaped And gates and so on.

Graphics are serviceable, but curves are a bit ragged. The cursor has a curious way of attracting attention: it gives a double wink every half second or so, which looks random until one studies it.

The program supports up to 20 levels of hierarchy. This is useful when trying to keep everything on screen, or when

Fig.3. Nettlister: screen dump of the original drawing used to generate the hirearchical box of Fig.2. Setting the screen dump going caused total loss of the screen display. I had to do a system reset when printing was completed.



reducing large schematics to several small sheets for a manual. At the top layer one creates a box containing a circuit from another sheet. The program takes the user through this in such a way that all terminals are matched between the two. The circuit for the box can have further boxes in it, and so on. An existing hierarchical file can be used in a new place; the program extracts all the terminal data from that file and so saves a lot of time.

It is possible to draw two identical components one on top of another; I did it with an hierarchical box. The parts list is correct when the part numbers are the same, but the PCB data preparation program pours out an enormous number of errors, which don't help if you aren't aware that there are superimposed components.

Figure 1 shows an exercise example, a bidirectional shift register in discrete logic, reduced to put it all on-screen. The text is replaced by rectangular boxes in the same colour to indicate the area covered. **Figure 2** is the contents of an hierarchical box, with the add menu displayed. The other menu is the control menu. The circuit used for the hierarchical box was dumped to the printer (**Fig.3**).

Although the box which arrived was shrink-wrapped, it contained neither registration card nor help telephone number. The former may have been an omission, the latter is probably unnecessary, but it does make one feel abandoned. A.B. ■

NETTLISTER
Racal-Redac Ltd
Green Lane
Newtown Industrial Estate
Tewkesbury, Gloucestershire
GL20 8HE
0684 294161 £495

EE DESIGNER III

Input to this system is by mouse. There is no choice most of the time. A narrow menu at the right hand side is visible at all times, a message bar across the top expands the short title of the menu selection when it is highlighted and another bar at the bottom displays typed entries and other data. All the features of the program (and there are many) are available through the menu system.

The operating environment is an IBM PC-XT or PC-AT or compatible with 640Kbyte ram and a hard disc. LIM (Lotus Intel Microsoft) expanded memory is supported, and I would say required. Extended memory is not supported. The mouse may be one of four types. Graphics may be CGA, EGA, or one of five proprietary adapters. For hard copy, five families of dot-matrix printer and five families of plotter are supported. It will drive a tape punch for NC drilling machines.

Beside the initial data capture the programme generates schematics and PCB layouts, does digital and analogue simulations and prepares data fields for a variety of purposes. The graphics are generally good, but the dark blue found in the simulation graphs is difficult to see and I didn't find a way to change it. Other graphics allow changes of colour. All the data can be sent to printers and plotters as required, and output files can be prepared for a Gerber photoplotter and for PSPICE.

This program is idiosyncratic in a variety of ways. As one who is naturally at home with a keyboard, I don't use a mouse. For this program I had to go out and buy one. On powering up, the first menu selection can be made only with a mouse. The function keys are used less than with Nettlister and no templates are supplied. Second, there is an enormous number of menus. One can step through five or six, sweeping up or down each time, to perform a simple action, and then one has to step back again. While there is a large number of commands, some are duplicated or nearly so in different menus, and other menus aren't full. Third, the manuals are not arranged in a manner conducive to finding the answer to an immediate problem. All of this is very hard on the newcomer.

Software installation requires a good book. It took me two and a half hours' continuous disc reading. At the end of it all I had was a new CONFIG.SYS (the old renamed) and six new subdirectories. Two were for my creations, while the other four between them held 1999 files. I jest not. Very roughly, it occupies 6.5Mbyte of disc space. The first system disc has a batch file to load the system and the first library disc has the same for the library. System configuration is by menu.

Tutorial

The tutorial can really only scratch the surface of this amount of software. In two places at the start the student is instructed not to use any commands other than those indicated, and to adhere strictly to the method of working described. In other words, the wrong key can land one in trouble. Some menus do not allow one to return without doing something, and this can cause confusion.

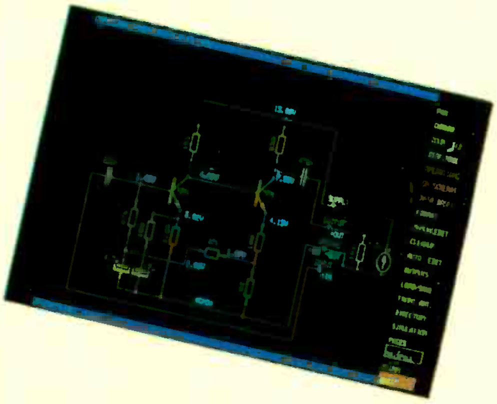


Fig. 1. EE Designer III: A two-transistor 40dB amplifier designed at the console. The voltage figures are the result of a DC simulation, which assumes all component values are exact. One can simulate, adjust and simulate again until satisfied.

The backup system ensures that nothing is lost; it operates at intervals of less than one minute, and beeps while doing so. There are two beep tones about four octaves apart, the upper one being a warning and the lower an acknowledgement. I am used to working in silence, but I quickly adapted.

The graphical facilities correspond to those available in Nettlister, and are similar for both schematic and layout preparation.

The tutorial uses a disc in drive A and not the installed library material. One can destroy this with ease. The commonly-used graphics commands are exercised, and a digital example is built up. Symbol creation is covered, and simulation. The digital simulation uses the exercise example, while analogue simulation uses three very simple examples already present on disc.

There is a good reason why the analogue examples are ready made; finding the data required is no easy task. One component I wanted was the analogue power supply (reference *@E). In the update manual there was a list of PSPICE primitives with some equivalents. There was a *$E listed. That is the nearest I found to *@E (I rang the hot line for that). The only index is in the Reference Manual, not at the end, and not up to now containing many of the key words I have sought. The contents list uses paragraph numbering, and the index, page numbering.

The mode of advancement is well summed up by the final remark in the tutorial: 'The best method is "trial and error"'. Many changes have been made to the software since the manual was written, and the screen messages sometimes use different words. Cross-referencing is hampered. I am told there is a new manual in preparation, which will, I hope, resolve these problems. The copyright message "1987" on each page identifies the old manual.

With use, the menu entries make more sense, but idiosyncrasies remain. Why does it deposit a junction point if a corner is created and moved on to another segment of the same net, when it doesn't if an existing corner is moved on to another segment of the same net? (you can add them separately). Why are corners not available in the same menu

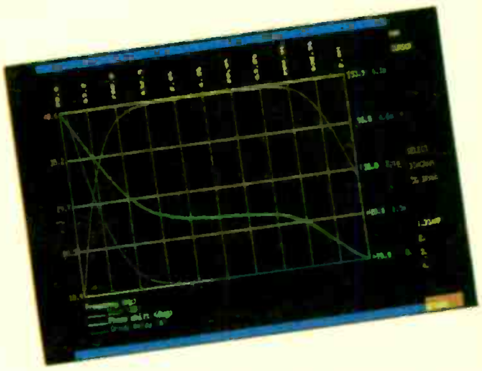


Fig.2. EE Designer III: AC simulation of the circuit in Fig.1. I couldn't change the deep blue colour, which was not easy to read when light fell on the screen. The fall in gain at HF is due to the parasitic capacitances in the models used.

as those used to lay down connections? One is supposed to rubber-band connections from terminal to terminal, and then change menus to sort it out. During connecting, especially if designing at the console, one might easily find that another component is required. It takes five menu changes each way to go and get it. It all adds up to a lot of clicking and swishing.

This is a programme for engineers. One can design at the keyboard, do a simulation, and switch back to modify the design as often as needed to arrive at the desired result. Having done that, one can prepare a PCB layout with up to twelve layers of conductors, and solder mask and silk screen for each of the two sides (I tried only two!). There is an autorouter which will accommodate whatever the designer fixes in advance, or tracks can be laid down manually. It is possible to alter the circuit at this stage, as for example to use spare gates and save a package of inverters, and feed the change back to the schematic. It is also in order to change a schematic and feed the change forward to an existing layout.

These facilities lay traps for the unwary. It is apparently possible to transfer from the schematic generating section to the layout section with the schematic still resident. Saving from here overwrites an existing layout file of the same name if you let it, and bang goes the layout. I say apparently because, in retrospect, it seems the only way I could have lost half a day's work.

The maximum plotting area is 800×800mm, and the area to be used is specified in absolute measurements, metric or imperial. Component data is referenced through a file with the extension .DEV. There are 12 categories of line and text in different colours, and 16 colours are used for the 12 track layers, masks and silk screens. There are 16 trace widths, seven text sizes and pad details all presettable and with defaults. There are macro facilities for sections of both schematics and layouts. I saved a macro consisting of a coil and a capacitor, which took a quite remarkable number of disc accesses to complete. For some reason the simulator regarded these as undefined when I used them, probably because I took the macro from one of the preset tutorial exercises.

The .DEV files have their own subdirectory holding 1168 files. Each device has its own file, and provides links to other files with symbol and package outline data which is shared. There are facilities to create new symbols and device files, and the content of these files is explained in some detail.

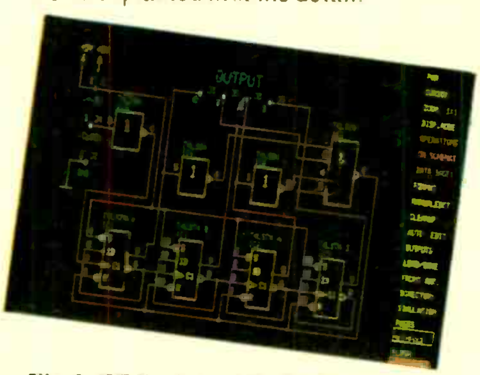


Fig.3. EE Designer III: decade counter, in discrete logic. This is a modified form of the tutorial exercise.

Once a feature of the programme has been uncovered, it is seen as powerful and useful. **Figure 1** depicts a discrete amplifier using two transistors. Voltages shown are the result of a DC simulation. The AC simulation produces the data for the curves of **Figure 2**.

The phase range is limited to 360°, with a choice of four starting values 180° apart. Intervals of 90° would be more useful, but phase overrun simply causes a switch across the diagram.

Time domain simulation (TD) is also provided. I was sure the data must be tucked away somewhere and I made it a crusade to find it. The chapter dealing with TD barely mentions input. There is a parameter entry described in the tutorial book and one is aware that to ascribe parameters one must select the component on the schematic to attach the data. The symbol is all.

Entries like *$E (and 10 others) won't do. Model data can't be attached. In the update manual I found a generator for analogue simulation, with a simulation code of –7, and in another place a –7 entry had the mnemonic @G in brackets after it, the only one in the list so annotated. I find in the library a schematic symbol file @G.SCH. The schematic capture doesn't load it. There are detailed instructions for creating a DEV file, but they hang if no layout symbol is provided. Another possibility is the disc model edit I came across in the analogue simulation group. This lists a voltage generator, precisely as required, which allowed me to create a file on disc with the parameters for sine or pulse waveforms. But no symbol to hang them on.

At 11.30pm the hot line isn't open. At one point I entered the voltage generator definition sequence from the edit disc model menu selection after entering TD. I instructed it to load the model I had written, and the menu on screen came up with no exit – everything else, but no exit. I had to do a general reset to get out.

Next day it turns out that the entry required is *@G. I now understand the displayed message about DEV or (*) symbol. I started a simulation, which hung. Clearly some of my data requires overhaul. My deadline for photographs passed, so there's no illustration of a time-domain simulation. Subsequent processing of the file branded my *@G as undefined, and it wouldn't accept a definition. I also tried the disc model edit from the TD menu again, and I still needed a general reset to get out. I also find that if I do a model edit from the main analogue simulation menu before going to TD (the same menu comes up) I get a return function. Furthermore, it will now go through the motions of a simulation, producing a table of (incorrect) data. It does look as though I will get there in the end, but I can't report that at this stage.

I describe this episode in detail as it is an example (albeit one of the worst) of the trial and error needed to get to grips with the program.

Figure 3 is a decade counter in discrete logic. **Figure 4** is the corresponding layout for a two-sided board produced by the autorouter. I straightened a couple of tracks after the routeing and optimizing, which removes unnecessary vias, on the principle of try everything; but the layout and component placing (I fixed the connectors) is the program's.

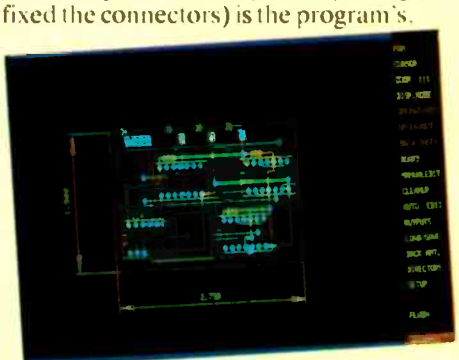


Fig.4. EE Designer III: layout for a two-sided printed circuit board. It can be displayed with trace widths to scale, as here, or with uniform thin lines. Components, except the connectors, and the traces were all placed automatically by the programme.

There are two digital simulation routines; the second being more comprehensive with a number of discrete components included in the repertoire, and some other improvements. The first was used to simulate the counter, with the results shown in **Figs.5,6.** The flip flops can be preset for the start, or random settings can be provided by the programme. The figures illustrate two random starts. Where memory chips are involved, memory data can be pre-

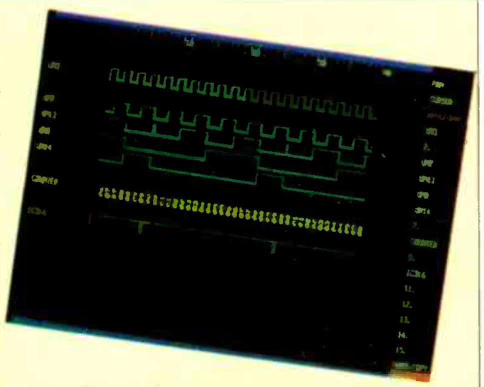


Fig.5. EE Designer III; waveforms for the circuit of Figure 3 calculated by the digital simulator. Initial conditions were set at random by the simulator. The row of figures is defined by assigning node voltages to bits in a word, in this case those giving the value of the count.

loaded. The tables of data produced by all the simulation routines can also be saved in a file or dumped.

The simulation routines permit insertion of user-coded routines. I haven't tried this but it seems a powerful feature.

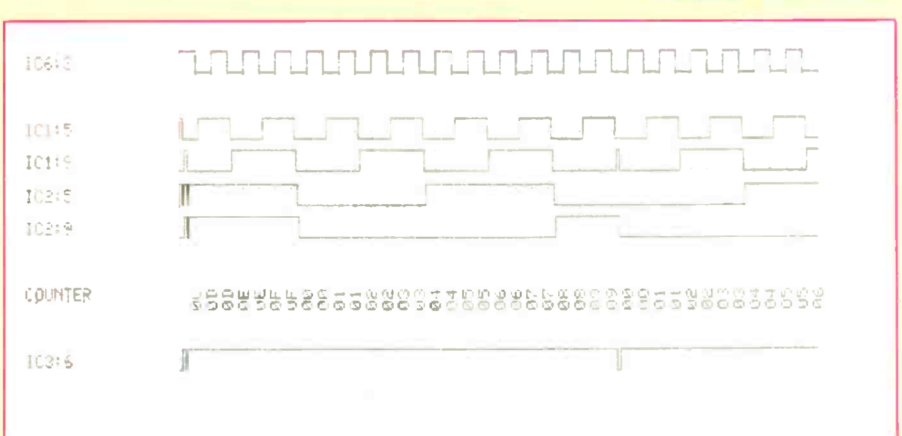
The data in the schematic can be used to generate a bill of materials which includes costings. A file of data for each component is saved once entered, and can be modified when necessary. Three price levels are covered according to quantity.

This programme tackles the electronic design process in its entirety. Its facilities cover circuit design, simulation and PCB artwork and tape generation. Since the last printing of the manual, much new material has been added. ■

A.B.

EE DESIGNER
Betronex (UK) Ltd.
1 Wells Yard
High Street
Ware, Hertfordshire
SG12 9AS
0920 469131 £3990

Fig.6. EE Designer III: screen dump of a further simulation run of the circuit simulated in Fig.5. This dump did not affect the display.



In the past, most components were both fixed and electrically connected to the PCB by passing the terminal lead-outs through holes in the board, then soldering to a copper pad. This technology is often referred to as "through-hole" and has, within the past two years, been largely superseded by SMT (surface-mount technology).

SMT (**Fig.1**) provides major benefits by increasing packing densities over conventional through-hole technology by at least a factor of three; it also introduces cost savings due to reduced component count and board area. However, SMT imposes severe constraints on the manufacturing and production cycle and demands a high level of automation.

Electrical inter-connection between the component terminals is made by strips of copper on the surface of the board, the spaces between the tracks forming the electrical isolation. All component terminals which connect to a piece of copper can be considered to form a common "tree" or "net". Where there is a high density of tracks on the board, then the number of layers of copper can be increased.

So, how does the engineer go about transferring his schematic drawing to the various copper layers, and how did PCB design technology develop to cope with the changing demands of SMT? The first step is to capture the circuit data in a suitable format: a list of components used with their outlines and pad positions, plus a "netlist" which details the point-to-point connections which form the trees or nets mentioned

High-density PCB design

The advent of surface-mount technology has led to the need for extremely closely packed boards. Bob Sadowski of Racal Redac looks at the techniques now available to the designer.

above, with details of the track widths to be used. This data can be generated manually or as an output from a cad (computer-aided design) schematic capture system (**Fig.2**).

Most early designs were (and some still are!) produced manually on a drawing board by laying down strips of tape to represent the copper interconnections after the component footprints had been placed in position, different colour tape being placed on separate overlaid sheets of tracing paper to signify the different layers. Engineers may still occasionally be heard referring to a "red and blue" artwork, which was commonly used to denote a two-layer design. To ensure some degree of accuracy, the design was laid out to a large scale and then reduced photographically to produce the true-scale artworks used to manufacture the board.

There are three major problems with this manual approach: accuracy, connectivity and post-processing. Imagine that the specification for the design lays down a minimum spacing between

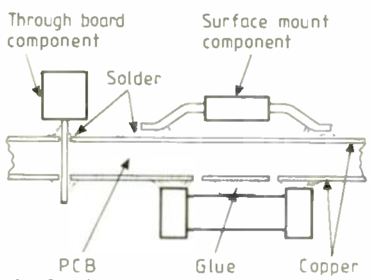


Fig. 1. Surface mounting allows greater packing density than through-hole mounting, but needs automation in design and production.

tracks of 0.020in. Even designing at a scale of 10:1 would require that the designer manually position the tracks with a minimum spacing of 0.200in to guarantee conformance. Reducing the design scale factor or setting the track spacing rule to a more realistic level of 0.010in makes the layout engineer's job very difficult!

Maintaining the original connectivity of the netlist is also difficult: it relies upon the dexterity of the PCB layout engineer to ensure that the tape is firmly fixed to the backing paper and that tracks line up between layers; the engineer must also remember to add pads to represent "via" holes. Modifying a layout, where the PCB layout engineer may have to relocate a component and re-route existing tracks, introduces a major risk that short or open circuits may be introduced.

Finally, when it comes to post-processing the design to extract manufacturing data, for example hole drilling data or the information for a solder-resist mask, the manual method has a very wide margin of error.

PCB cad systems provide an invaluable design tool to overcome these problems, and also to allow engineers to produce complex multi-layer designs which are beyond the capability of manual methods. Six- and eight-layer boards are now commonplace, with occasional specialist applications demanding over 50 layers! To understand how using PCB cad can achieve such benefits, we first need to review the design process, which can be split simply into three sections: preparation of data, component placement and track routeing.

Data preparation

As outlined above, the most essential data required for a PCB design is a list of the parts to be used and their component footprints, together with a netlist of the connectivity of the design. Schematic capture packages (Fig.2) available within most modern cad systems allow the user to capture his schematic diagram on screen using customisable parts and shapes libraries and produce a netlist automatically.

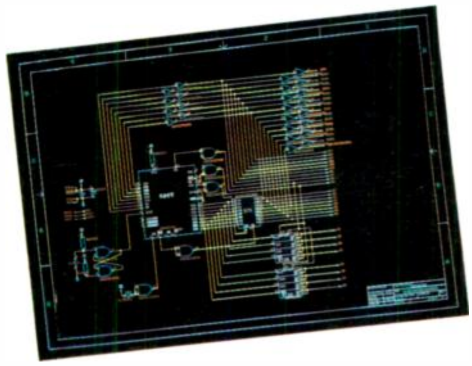


Fig. 2. From a layout like this, a netlist is generated.

In using such a cad system, however, it is necessary to specify additional data which the manual designer might take for granted. This data includes the spacing rules on what track-to-track, track-to-pad and pad-to-pad clearances are allowed; the sizes of component pads and their associated drills for through-hole designs; the size and shape of pad variants to be used for different soldering technologies; the sizes of text items; the size and shape of the board; and, not least important, what colour should be

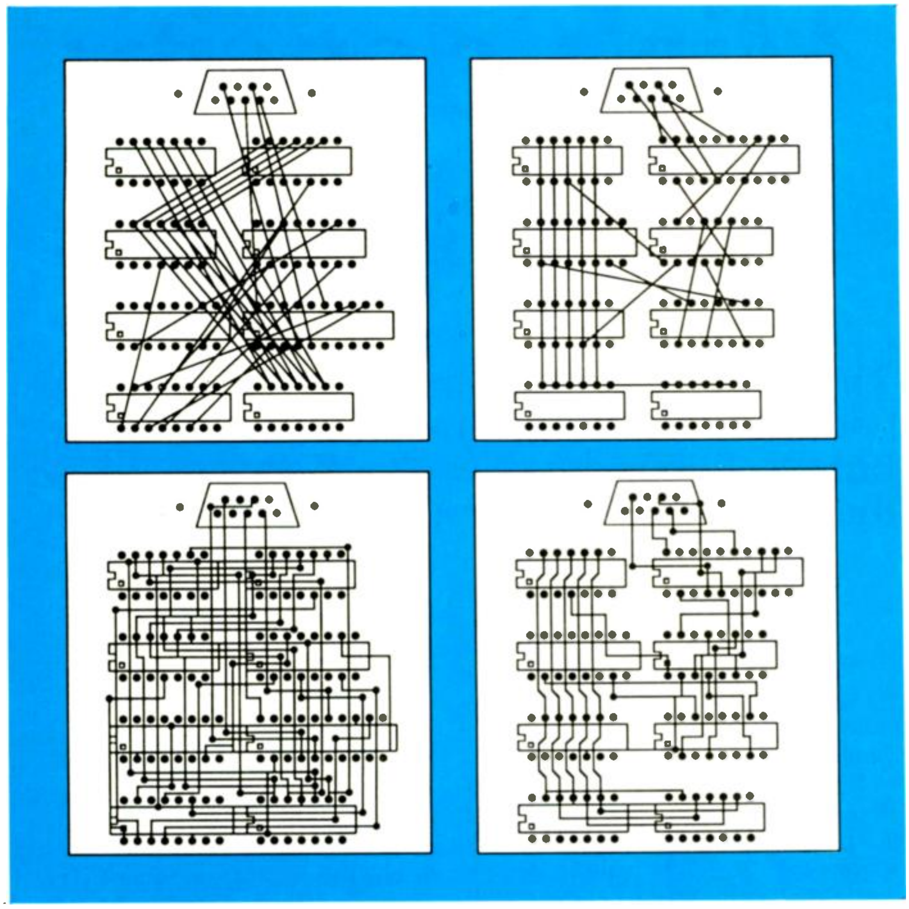


Fig.3. Component placement can be either random, as seen on the left, or according to the Manhattan algorithm, shown on the right. The improvement is obvious.

used to display all these items on the computer screen!

In practice, most of this data does not vary from one design to the next and can be stored in a default file, thus simplifying the layout engineer's job.

Component placement

Once the basic design information has been fed into the PCB cad system, the next task is to place the components within the board outline (see **Fig.3**). Although this sounds simple, it is actually the most important part of the design process, since bad component placement may make it impossible to route – that is to position the connecting tracks on – a layout which could otherwise be easily routed.

To achieve the optimum placement, the layout engineer needs to take advantage of all of the cad tools available to minimise connection length (the sum of the point-to-point or pythagorean connections for all nets) and produce the best pattern for routeing. However, these tools must be used in a sensible and logical way.

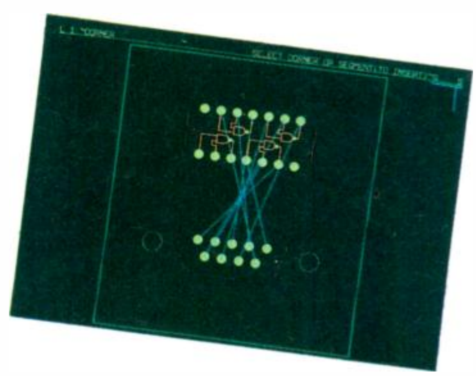
Automatic component-placement tools vary widely, from simple routines which merely fill up the available space with no consideration of the routeing pattern, to those which use artificial intelligence techniques to determine the order, rotation and position of each component, even taking into account the ability to automatically flip or mirror SMT components from one side of the board to the other. The layout engineer still needs to exercise discretion and run these routines as a number of passes to optimise machine time, grouping together components, such as memory devices, which are logically inter-connected. Running more and smaller passes of a routine is more effective in terms of both man and machine resources (that is, the PCB layout engineer takes less coffee breaks!)

As an example, consider the negative biased Manhattan algorithm used in the automatic placement tools within Cadstar, Racal-Redac's PCB cad system running on IBM-compatible PCs (**Fig.4**, heading). This algorithm attempts to emulate the placement process by applying weighting penalties to selected groups of connection types (e.g. bus signals); this ensures that components commonly connected by those signals are placed together, in logical order, in a clear area of the board where a minimum number of cross-overs will be created. Similarly, components with few common inter-connections with other devices will be placed in any available area of the board where their potential track lengths will be minimised.

Use of the Manhattan algorithm ensures that the resulting placement will provide a routeing pattern with the orientations of connections biased toward the X and Y axes, which simplifies routeing. The ability to selectively bias the connection pattern is particularly useful before routeing power tracks on conventional through-hole boards, when an un-biased minimisation of the connection nets would produce a more random, and hence more difficult, pattern to route.

The connection pattern can be further optimised by running automatic pin- and gate-swap routines (**Fig.5**). These routines swap compatible pins or gates, or exchange equivalent gates within and between compatible parts, to minimise the length and cross-over of connections. The types of swap allowed for each part type are defined in a library, the data being extracted from data books supplied by the part manufacturers.

Since these changes alter the connectivity pattern of the design, they should all be stored automatically by the PCB



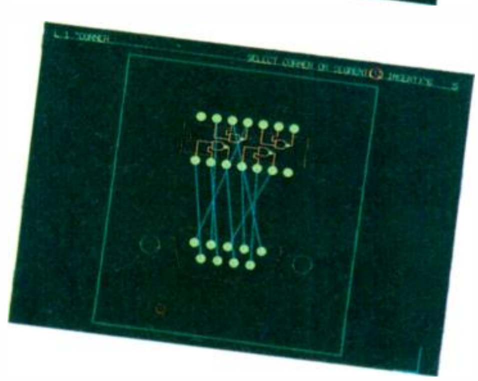


Fig.5. Optimising the layout by pin and gate swapping. The effect of swapping is shown below.

cad system so that they can subsequently be back-mounted to the schematic drawing by manual or automatic means.

The result of using these placement tools is to reduce the total connection length within a design sometimes by over 25%, which results in a much simpler pattern for routeing. In some cases, however, the PCB layout engineer may wish to produce a non-optimised connection pattern, for example on an analogue design using high-speed logic, where specific connectivity must be maintained to minimise crosstalk. In such circumstances, the ability individually to optimise connection nets or components with respect to their position is very important.

Track routeing

After a number of iterations, the PCB layout engineer will be satisfied with the component placement and connection flow, and will be ready to begin routeing. Important decisions must be taken on how many track layers are required, how many additional layers are required for power or screening planes, and how the track layers should be biased by routeing axis.

Deciding how to build the board at this stage requires a measure of experience, a pinch of information and a twist of luck, since making the wrong decision can be very expensive in both development time or production cost. Trying to squeeze tracks on to two layers where four are really required will either lengthen (perhaps infinitely!) the design cycle, or compromise the design rules by forcing the engineer to use lower track widths or track-to-track spacings. The alternative, to add additional layers, is complicated by the fact that track layers are normally manufactured in pairs, so increasing the cost disproportionately. Some cad systems provide a board-status report which provides essential information such as the board area, component-to-board density ratio, number of equivalent ICs, etc. to assist the layout engineer in his decision. **Figure 6** shows a high-density PCB layout designed and routed using a modern PC-based cad system.

Deciding whether to bias the routeing axis on a layer will depend on the types of components used, the soldering method to be used and the connection density. All routers, manual and automatic, find it much easier and faster to route a board using biased layers. Most through-hole boards using dip technology are routed with paired layers of X-biased and Y-biased tracks (**Fig.7**).

Assuming that the board will be wave

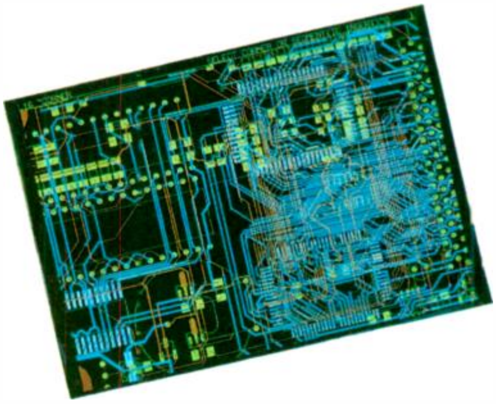


Fig.6. A high-density PCB designed by means of a PC-based system.

soldered, then the solder side is biased to run in the axis of the direction of travel over the solder wave, to minimise spikes and short circuits. The decision to allow unbiased routeing is usually forced on the layout engineer when SMT components are used, since they can require track entries from all four points of the compass (dips are usually X or Y biased, not both), and can in addition be placed on the board in any orientation or on either side, to optimise the connection pattern. SMT also implies finer track widths with smaller spacing requirements: whereas a "typical" dip board will use 0.01in tracks and 0.01in spaces, an SMT board may use 0.004in tracks with 0.006in spaces!

When the track density is high or when a mixture of technology types are used, then the type of autorouter used is critical. Autorouters can be separated into two broad categories: cell-based and gridless.

Cell-based routers work on a grid principle whereby all obstacles (pads, existing tracks, copper area, text etc.) are mapped on to the grid points which are marked as either blocked or unblocked. When routeing a track, the router searches for unblocked points which will form a path between the source and destination of the connection. Tracks are placed on the grid points on the assumption that there are no off-grid obstacles; to properly map off-grid obstacles the resolution must be increased by lowering the routeing grid.

For example, to map a one-inch square board on a routeing grid of 0.2in would require storage of 36 grid points for each layer; doubling the resolution to 0.010in increases the number of grid points to 121 per layer, while running on a routeing grid of 0.001in – the resolution of the majority of PCB cad systems – increases the number of grid points to over one million per layer!

Memory availability within the design system and constraints on run times impose a practical limitation for gridded routers on either the routeing grid or the physical size of the design. An added complication is that gridded routers have difficulty routeing designs where the routeing gird is less than the sum of the track size and track-to-track spacing, which makes them ineffective on mixed-technology boards where the variable component-pin pitch means that the majority of pins will be off-grid, increasing the possibilities for error.

Gridless routers operate on the principle of storing all objects and design parameters as absolute entities in a list. Since the gridless router understands the absolute size and position of all obstacles, it can follow their contours (**Fig.8**), allowing for specified spacing rules; this produces a much higher track density with no spacing errors.

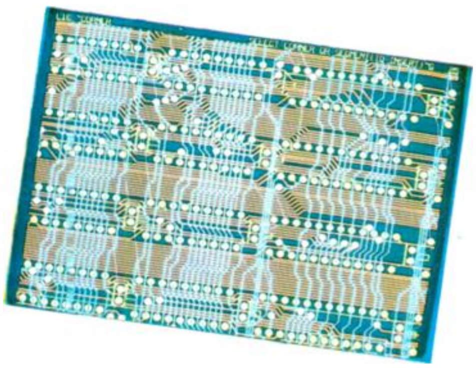


Fig.7. Two layers of a board layout using X and Y biasing.

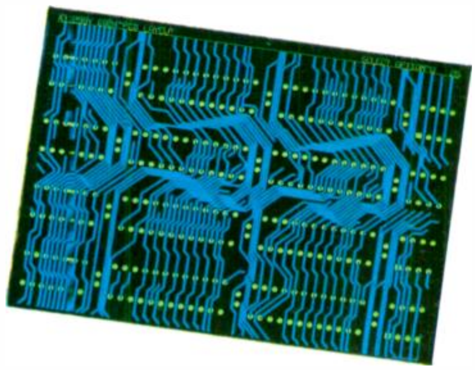


Fig.8. Gridless routeing produces a higher track density.

Some of the more competent routers have the ability to "rip up and retry" individual routes to find alternative paths when the going gets tough. The Bloodhound autorouteing algorithm, as implemented on both workstations and PCs in Racal-Redac's Visula Plus and Cadstar software suites, has additional intelligence which allows it to "push aside" groups of existing routed tracks in busy areas to clear a way for the new track, much as a manual designer would do (but the software does it much faster).

When routeing is complete, smoothing passes must be run to minimise the number of track segments, optimise the track density and minimise the number of vias. Optional mitreing (45 degree cornering) helps to produce a more reliable and manufacturing board. The gridless router may require more system memory initially than a gridded router, but the requirement does not increase with the resolution, making gridless routers the only real choice for mixed-technology high-density SMt designs.

Manufacturing links

A good PCB cad system will provide major benefits when it comes to post-processing the design data to produce consistent, high-quality documentation for manufacture. In addition to individual plots of each electrical layer to produce the copper etch patterns, today's PC-based cad systems can often provide the required data for silk-screen, solder resist, paste mask, NC drill etc. in the appropriate format for pen plotters, photoplotters or as paper-punch tapes. Any modifications to the PCB layout then only require that the designer produce new output files to reflect the design changes.

More advanced workstation-based EDA systems should also be able to provide direct-drive data for automatic assembly tools and automatic test equipment.

It is generally the case that the capabilities of PCB cad software packages are reflected in the price. However, it should be borne in mind that cad is supposed to be an aid to the designer; it should not become the master. Most of a designer's time will be spent in interaction with the system, so it must be technically competent, user friendly, but most of all it must allow YOU to control IT.

CADSTAR
Racal-Redac Systems
Green Lane
Newtown Industrial Estate
Tewkesbury
Gloucester, GL20 8HE
0684 294161 £4500–£12000

AutoSketch

An object-oriented drawing package, providing output to a laser printer

Autodesk, the makers of *the* cad drawing package, AutoCad, introduced this product some years ago to fill a gap in the market. AutoCad is a full-featured, professional, expensive drawing package, capable of three-dimensional work and with a host of features.

For the single user or small business looking for something to draw occasional or less-complicated material and not requiring 3-D capabilities, AutoCad is way over the top in most respects, not least the price, which can exceed the cost of the hardware it is run on. AutoSketch filled that gap, being a 2-D drawing package with sufficient features for everyday use. As AutoDesk put in the manual, 'you can get your feet wet in cad without drowning in a sea of commands and options.' Having battled (unsuccessfully) with AutoCad on a few occasions, I totally agree with that concept.

The program still maintains compatibility with AutoCad in terms of file format, so that you could later upgrade and still be able to use any drawings produced in the lower-cost package.

AutoSketch is *object oriented*. That is, it holds all the information on the lines, circles and other material that you draw as a series of mathematical descriptions. When you later change their size, the resulting image is a true scaled up or down version of the original. And any drawings sent to a printer, be it a laser, plotter or dot-matrix, are printed at the maximum resolution the device is capable of.

Simpler drawing packages, often termed 'paint' packages, use *bit-mapped* images. These deal in individual pixels, usually at the same resolution as the screen display. The problems come when you want to scale such an image, either on the screen or in print – if you make it larger, the pixels making up the image are also scaled up, giving a ragged appearance. If you make it smaller, detail often vanishes when the resolution of the printing device or screen is no longer an integral multiple of the original image.

Operating environment

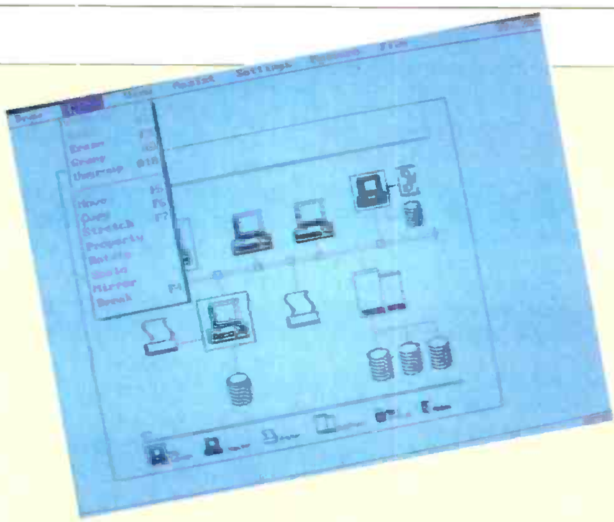
Installation is easy and the program will run on just about anything. If you have a choice of equipment, go for something with a co-processor fitted – Autodesk supplies two versions of the program on the master discs. One is speed-enhanced with the program code tailored to specifically use the co-processor – you cannot use the speed-enhanced version without one fitted. Autodesk claims that it performs up to 10 times faster than the standard version without a co-processor and I can validate this claim 100%. It will run with 512K of memory, but 640K is better, since you can produce more complex drawings, and you use it with any display from CGA up. CGA gives the worst screen resolution and is hard on the eyes, so go for VGA, EGA or Hercules (in that order) if you can. A hard disc is useful but not mandatory, since it will run quite happily on a dual floppy setup, and there is no copy protection.

Needless to say, you need a mouse or other pointing device (such as a trackerball, joystick or graphics tablet) to make real use of the program. It will work with the keyboard arrow keys but you end up taking all day to do a simple drawing.

No problems of this nature exist with AutoSketch and, once you master the interface, you can expect high-quality output, especially if you have a laser printer or pen plotter.

AutoSketch's start-up main screen is empty except for a status line at the bottom and a menu line at the top. Menus drop down in the fashion familiar to any Mac or GEM user, and a continuous display of memory usage by percentage keeps you informed of how large your drawing is. The main menu options are Draw, Change, View, Assist, Settings, Measure and File, from where all operations are conducted. Each has further sub-menus with everything being fairly intuitive to use.

As you would expect, AutoSketch can draw and manipulate virtually any object you care to draw, and on up to 10 layers. It produces spline and ordinary curves, polygons, lines, arcs, circles together with text, and you can move, copy, rotate, mirror image, size and stretch just about anything. Small draw-



ings, such as circuit symbols, can be saved and later retrieved into any other drawing to save time. I had some difficulty with the sizing function, which seems extraordinarily sensitive to mouse movement, making an object a few millimetres wide expand and disappear off the screen very easily. The lack of any resident on-screen ruler facility makes it very difficult to relate to the size of objects you are drawing on the screen, forcing you to watch the co-ordinate display all the time. It is possible to make a sort of ruler by using the auto-dimensioning facility, but this is inconvenient.

The most frustrating aspect of Auto-Sketch is its manual. While this runs to 116 pages and is very informative, it is also very difficult to use. Autodesk have gone for a narrow A5 format with a rather wide perfect binding. To lay it open and flat for reference is impossible without breaking the spine. Then when you try to close it, it pops open again, just like the well-read pages in a copy of Lady Chatterley's Lover.

While the program is well designed and, for the price, a bargain, it is more suited to drawings of the architectural and similar types than electronics. For schematics and certainly printed-circuit board design, a program designed specifically with those applications in mind makes life easier. Many of Auto-Sketch's functions are redundant in such applications, and it lacks many of the useful features present in software such as EASY-PC, reviewed next. A.B.

AUTOSKETCH
Autodesk Ltd,
99 London Road,
London SE16 6LN
01-928 7868 £91.54

Easy PC

A "manual" package for board design and circuit drawing, which copes with up to eight track layers.

Number One Systems, the UK manufacturers, supplied us with both a complete working package and a demonstration version of EASY-PC. The complete package consists of one main component, EASY-PC itself, and two optional subsidiary programs: EASY-PLOT and EASY-GERB. EASY-PLOT is a post-processor for printing stored PCB or schematic disc files on a Hewlett-Packard plotter or any device capable of understanding HPGL (Hewlett-Packard Graphics Language) instructions. EASY-GERB is a photo-plot post processor, converting disc files into GERBER photo-plot format – this is stored on disc then downloaded to a photo-plotter at a suitable bureau. The latter component of the package was not reviewed.

There is also a lower-cost option called TINY-PC. This is aimed at the hobbyist and works in machines with only 256K of memory, but at the price of speed. Although all files/libraries are compatible, a typical operation such as Zoom, taking two seconds on EASY-PC, takes 25 seconds on TINY-PC. Incidentally, a maths coprocessor makes no difference to the speed of execution of any of this program's facilities.

EASY-PC is not an automated package in the sense that it makes any layout decisions on the user's behalf. You still have to lay out and design the printed circuit board manually. But this is a much easier process, especially when alterations are called for, than the classical pen and ink or sticky tape procedures. The same applies to schematic design, essentially no different to the computer, since the process involves the same idea of placing and linking objects. So, what can EASY-PC do, and why is using it an advantage over traditional methods?

The main features are:
- up to eight track layers available;
- up to two silk screen layers;
- automatic generation of solder resist master;
- selectable pad and track sizes;
- true track width/pad size shown on screen;
- full library facilities;
- output to dot-matrix printer (plotter optional).

For the average small electronics business or one-man band, these facilities are probably more than adequate – many people will never need to produce more than the two layers required for a double-sided PCB. Having designed many PCBs in the past, of varying complexity, I must admit that a package like this would have been of great help, had a suitable PC been available at the time.

The manual is a short, A4, loose-leaf production, taking the approach of running through a tutorial using supplied exampled files. It is competent and to the point, running to 39 pages with an index, plus technical information, library contents and lists of error messages.

Once you run the program and choose your startup mode (PCB layout or schematic diagram) EASY-PC presents an uncluttered startup screen with a rectangular outline representing the largest size it can handle – a board or piece of paper 17 inches square. Along the top of the screen are three small blocks used for popping down menus. The left controls mostly editing functions, such as New Track, New Pad, Edit Pad etc., while the centre looks after operations performed in Block mode, such as printing and reversals. The right menu contains mostly commands affecting the screen appearance such as Pan, Zoom, Scale, Grid and Cursor size.

Many of the menu commands have keyboard equivalents, either using function keys or letter keys, sometimes in combination with Shift. This approach is usually quicker than relying entirely on the mouse, since one hand is generally free anyway when using a mouse.

EASY-PC does have one bad point in its choice of a cancel key for certain operations. The majority of PC graphics programs use the Escape key and/or the right-hand button of the mouse as an abort or cancel key; this program adopts this approach when using menus, but most of the time the right-hand mouse button acts as a confirmation key, such as when laying down tracks. This became extremely frustrating, since I spend most of my time working with two other graphics packages that take the opposite and more normal approach.

Designing a printed-circuit layout is very easy once you do get the hang of the keys. With the optional snap grid shown and set to the standard spacing of 0.1 or 0.2 in, you can start designing. The basic library is extensive, including all the standard dil and SMD pad outlines with each symbol coming with both pads and a silk-screen overlay outline for the component. Some of the more exotic symbols are a PGA68 pin-grid aray and a EUROcard outline (more libraries are available from the manufacturers). On-screen, the silk screens and pads appear white, with tracks in different colours depending on the layer selected – using two layers, the first layer shows as blue with the second in red, although you can change this and many other settings via a defaults menu.

Placing a symbol is simply a matter of selecting it from the library, then moving it around and pressing Esc to confirm the placing. It is a shame that the symbols do not move as you move the mouse as with most graphics programs – each time you move you need to press Enter or the left mouse button to see the repositioning. Compare this with track laying where there is an optional rubber band feature that shows you where the track is currently placed before you drop it.

Within the 17-in square maximum, the PCB can be of any size. A zoom feature with seven levels aids design, as does the pan facility, using the mouse or keyboard. One striking feature is the speed of redraw when panning or zooming – even without a maths coprocessor this is fast. A quick check of the program on an XT PC gave a slower but still respectably quick redraw.

Once the symbols are down, adding the pads is easy – select New Pad from the menu (or press F4) and drop them down. Sizes are selectable from 0.010in to 0.3in and the program will place them on all layers or just the current one.

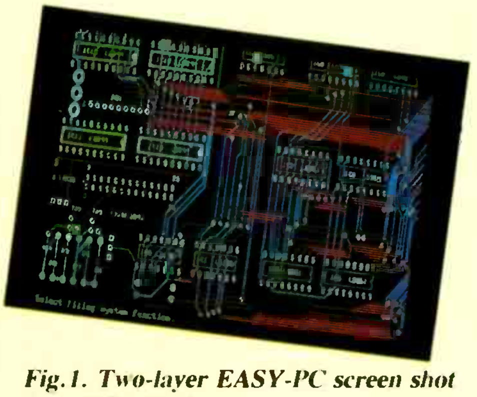


Fig. 1. Two-layer EASY-PC screen shot from EGA display.

Fig. 2. Typical schematic drawing screen.

Laying tracks is perhaps the easiest, rather than the most complex operation. The first press of the left mouse button establishes the origin which, if the grid snap is on, will be the nearest pad to the cursor, while subsequent presses establish the next point or node of the track. Only when you press Esc or the right mouse button does the track become permanent – if you get into trouble, the Edit function lets you delete or change nodes at will. In accordance with good PCB design, EASY-PC's default is to allow only right angle or 45° angles in running tracks, although you can change this to allow any angle – you need to do this when drawing schematics rather than PCBs. The optional rubber-band feature lets you see where a track is heading at all times (in white rather than the colour of the current layer) as you move the mouse about and I found this feature speeded up track laying immensely.

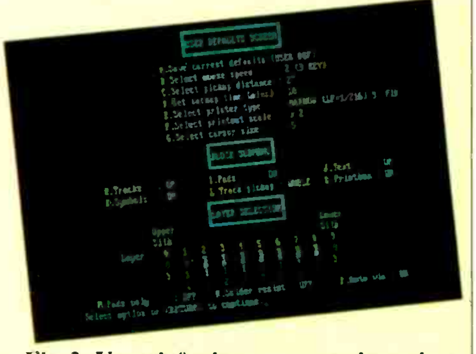


Fig. 3. User defaults screen used to select displayed layers and other screen defaults.

Track widths are variable at any time, even in the middle of a track run if, for instance, you are running between two IC pins. The available widths are 0.002in (the standard default) to 0.531 in, the latter being useful for laying ground planes quickly. All size changes are reflected accurately on screen within the limits of the display resolution, but are obviously seen best using an EGA or VGA adaptor.

While designing a multi-layer board, you can instantly change from one layer to the next if you need to. There is even an automatic 'via-hole' option to link a track from one layer to the next – as you change layers a prompt asks whether you want a via-hole laid down. If you answer Yes, a default-size 0.035in via pad appears, linking you to the next layer, from where you can continue.

A somewhat more complex operation is editing tracks, although not as complex as the manual warns. It is possible to add sections to tracks without laying

Operating environment

It should be said that you really need a mouse to use EASY-PC packages effectively. Although all will function using the keyboard and cursor control keys, operation is smoother, faster and altogether easier with a mouse. Like all good programs, EASY-PC allows you to adjust the mouse response to suit your own preference.

Until recently, EASY-PC used the CGA graphics mode with its fairly low resolution for all work. As a README file now indicates, there is an EGA version supplied with much higher resolution – you can use this on any machine with an EGA or VGA adaptor and was the choice for this review. Unless your equipment budget prevents it, an EGA screen is without question the best choice for work like this. With CGA, the screen resolution is 320 × 200 pixels, while for EGA it is 640 × 350 – the difference is readily apparent in the screen shots shown here.

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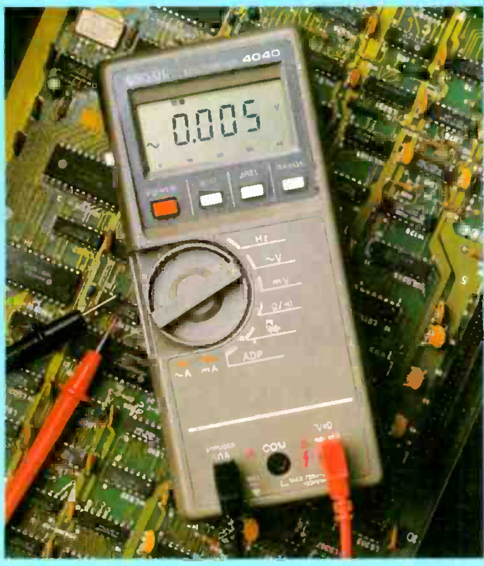

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down the whole track again, and even to drop a section of an existing track down to a new layer using via-holes if you run into layout problems.

Text options are extensive in the same way as for pads and tracks with full editing facilities. You can add text to either copper or silk screen layers, and in varying sizes from 0.05in to 0.4in high, with the line widths composing the characters variable from 0.005in to 0.05 in. Text is also rotatable in 90° angles.

Once your layout becomes complex, it is easy to change the screen display to show only a single layer, or the upper silk screen or just the pads as required. This would probably only be necessary for boards with more than three layers, since the colours make it relatively simple to see what is going on, even with the majority of a complex board displayed at once.

There are many more options within the various menus to aid the PCB design. These include repeat and block move/edit facilities, text flip (mirror image), and the ability to create new symbols for permanent storage in the library.

If, as is likely with a complex design, you lose track (!) of the exact size or layer location of a pad or track, you can easily check it using the Status function. After selecting the offending item for editing, pressing the grey + key on the right of the keyboard displays a status line at the bottom of the screen showing pertinent data – for a track, this would be the Layer, Width, Current Node, and Total number of nodes in the track.

All of EASY-PCs defaults are user-definable if the supplied settings do not suit you. For instance, with Drawing defaults, you can change any of the pad sizes through a range of 128 possible values, altering both the outer diameter and the hole size. Any changes are stored in a lookup table that is stored with each layout, so you can have different defaults for different PCB designs if needed.

The above has covered PCB design – EASY-PC is very suitable for drawing schematic diagrams although, as mentioned earlier, you cannot use these in any way for later automatic PCB design, such as through the production of Net Lists. A matching symbol library for schematics contains all the usual C,R,L and transistor symbols, plus over 40 logic symbols and 16 often-used labels, such as +5V and EARTH. Drawing a schematic is really no different from designing a PCB as far as program usage is concerned. It is simpler, however, and you don't have to worry about

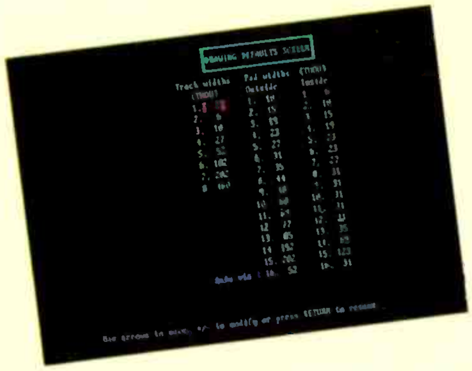

Fig.4. Drawing defaults screen used to define track and pad widths.

layers since these are fixed in this mode.

Throughout any design work, EASY-PC prompts you periodically to save your work. This backup function is time based, and defaults to 10 minutes. Easily changeable, it can also be turned off if it annoys you. There is also an efficient backup system which, although using lots of disc space, does ensure you should never lose your work. Three files are kept at all times – the current file, and the two versions before that. So, if you make a really bad error like deleting half of a layout and then saving it, you should still be able to recover it via the third oldest copy.

Once design is over, you need to produce hard copy of the output. The basic version of EASY-PC supports any dot-matrix printer capable of IBM/Epson graphics in either 9– or 24-pin modes. Using a 9-pin printer with output scaled at 2:1 (or higher) for subsequent photo-reduction, the results could be acceptable for many production jobs, although better results are obviously obtained from a 24-pin printer. The examples in this article show what can be obtained from a 9-pin printer, reduced down from 2:1. I would have expected to see a laser printer driver of some kind, since these machines are now realistically priced and becoming more common.

When printing, you can choose which layers to print, the scale of the output (from ¼ to ×4) and the density, such as Draft, Normal or Bold. 10-in or 15-in platen printers are catered for, as is the smallest line-feed increment of 1/180th or 1/216th of an inch, depending on the age of your printer. When printing double-sided PCB masters, you obviously need to be able to mirror image the bottom layer before printing – this is done using the block mode facility on the selected layer before selecting print.

Two very useful options are the ability to print the pads only (perhaps for a drilling master template), and to produce a solder resist master. The latter prints the pads only, enlarging the outline by a selectable amount and filling in the drill holes.

For higher quality, the separate EASY-PLOT option allows output to any plotter capable of accepting HPGL commands – this covers the majority of those on the market including the ubiquitous HP7475A used for the examples reproduced here of both PCB and schematic design.

Again, virtually any of the settings are user-definable, from the area plotted and pen speed/size, to a choice of whether the pad drill holes are to be filled or not. The latter option has a major effect on print time, and unless you are producing a single-sided PCB master where the holes are needed to spot the drill, producing hole outlines takes an awful lot of plot time and is usually unnecessary.

Besides outputting direct to the plotter on COM1: or LPT1:, you can elect to save to a file. The latter is especially useful if you require several copies of an artwork, since you do not have to go through the post-processing process preceding each plot. If the plotter has sheet feeder or uses continuous paper, it would also be possible to print overnight using a dos batch file to process several different files consecutively.

A.B.

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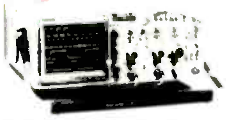

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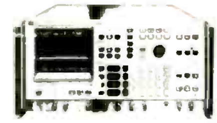

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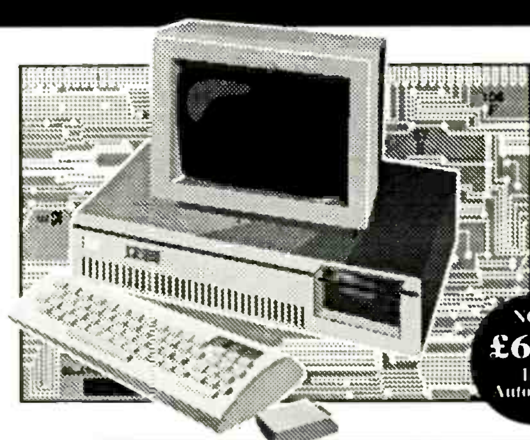

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Betronex EE Designer running on an Olivetti M380C

CAD – pitfalls and possibilities

Even the smallest companies can now afford the advantages of computer-aided design for PCBs. Jonathan Hewer of Betronex explains how to avoid making expensive mistakes.

There is no doubt that the advantages of cad, in terms of increased productivity and design efficiency, can be enormous. Time saving is one of the most important factors. Libraries of schematic symbols and/or PCB layout components are usually included with the system, and these can be quickly arranged on screen. Connections can be made or deleted as required and areas of circuitry that are to be used again can often be kept in the computer's memory as a macro, thus eliminating the need to "re-invent the wheel" every time a change is made to an existing section of a design. Any system worth its salt now includes autorouteing and automatic component placement in the PCB design area; and design-rule checking means that laborious manual checks for short circuits and the like are no longer necessary. Logic and analogue simulation is now available with many systems and this, again, can greatly improve efficiency.

Nevertheless, there can be pitfalls along the way, and only by taking a cautious approach can these be avoided.

CHOOSING A SYSTEM

No two companies involved in electronics design are the same. Different products, different working practices and different mental attitudes make the electronics industry highly diversified in approach, which dictates that the software available, especially at the low-cost end of the market, must be a compromise if it is to be suitable for the largest number of users. That is how producers have managed to reduce prices so drastically over the last few years. Mass production has great financial benefits, but it means that the system you buy was not produced specifically to meet your requirements.

Although a cad salesman may take the view that his software is perfect for your needs, nobody else knows what you need as well as you do. Think carefully about what you need the system to do for you, and make sure for yourself that the system you are considering does what you want, not what the salesman thinks you should want.

Remember that there is a wide variety of cad systems available and taking the trouble to compare them can be an excellent investment in time.

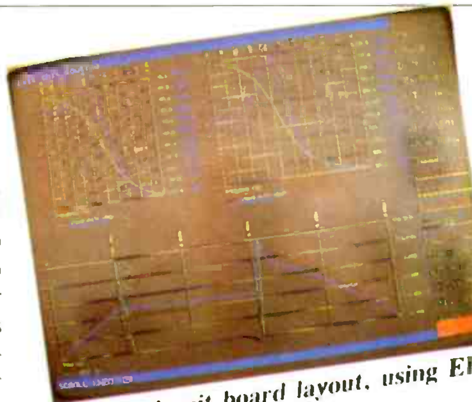
A full demonstration of the software, by someone with enough technical knowledge to be able adequately to show the features that are important to you, is a must. If the demonstrator doesn't know his product, but makes vague promises without full explanations of how they will be achieved, steer clear.

Your first step should be to collect as much written information as possible about all the systems you can find which appear to do what you want at a price you can afford. Examine the literature carefully, and try to reduce the list of possibles down to about three or four which warrant detailed investigation. Care should be taken at this eliminating stage, or you could find yourself wasting time on a white elephant or, worse still, ignoring a system which could have been just right. Do not assume that the vendor with the glossiest brochure or best known name should necessarily be an automatic choice.

Specialist exhibitions can be an excellent place to narrow down the field. Here you can have a quick look at the many offerings available and ask a few pertinent questions face to face with the various producers. If the exhibitors are busy, they won't want to waste time any more than you do on trying to sell you a system which is totally wrong for you. Seeing all the options available at the same place in a very short period of time can greatly clarify the comparison process, but try to make notes; otherwise, at the end of the day the alternatives may become blurred.

By the time you start evaluating your chosen few in earnest, you must have a list of your minimum requirements. If there are features over and above your minimum, that's fine – you may be able to use them as well. But do not be deflected from what you consider necessities. Think hard about the board size and density you produce, for example. Perhaps you produce large complex boards only occasionally. In this case, it may be more cost-effective to go for a low-cost system yourself and subcontract the more complex jobs.

When you begin to analyse the systems on your short-list in detail, make sure that anyone else who will have to use the system has a say in the final choice. Often, somebody else may spot a flaw in a particular system which had escaped your notice. And do not forget that an operator who starts off with a negative attitude to the equipment he is using is unlikely to be as productive as one who has been involved in the decision-making process. It is easy for the user to pass off his own operational inadequacies as faults with the system when he is only grudgingly using it. Conversely, if he has given the equipment his blessing in advance, he'll do everything in his power to try to demonstrate that it was the right choice.

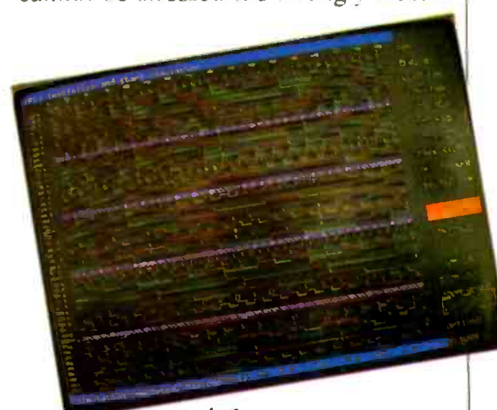


Printed-circuit board layout, using EE Designer

While the system is being demonstrated, beware of euphoric statements about its capabilities. For example, there is a lot of talk at present about 100% autorouteing. As soon as one vendor made this claim, others were obliged to follow suit. 100% autorouteing is often possible and, in fact, practically any autorouter will complete 100% if the parameters are generous enough. But at the same time, no autorouter (and no human manual router) will succeed if an attempt has been made to squeeze an impossible amount of circuitry on to too small a board. The same applies to other claims which may be made on a system's behalf. The salesman may be able to answer "yes" to your questions, but will the system perform the operations the way you want it to? Only a detailed demonstration of the functions will tell you.

You will probably find that after your demonstrations there is more than one contender that apparently fits the bill. Now is the time to look at the less technical aspects of your purchase. Obviously, price must be an important factor – after all, the system should be expected to pay for itself in productivity gains in a fairly short time. But look further than initial cost alone. Some vendors make very high charges for maintenance agreements. They aim to be "locked in" to a large slice of your cad budget for years to come. Any maintenance agreement should include regular updates, as the electronics design industry is constantly changing and you do not want to be saddled with a system that rapidly becomes obsolete. The software should be "living" – constantly improving with the industry's demands. If you select equipment at the low-cost end of the market, make sure there is an upgrade path so that, as your requirements increase to higher levels, you can transfer to a more advanced system.

Look into the support you will be given once you have bought the system. Stories of vendors "washing their hands" of users once the equipment has been paid for have been all too common in the past. Training facilities should be available, as well as written learning aids, and you should try to obtain an assurance from the vendor that your telephone enquiries while you are familiarising yourself with the system will be welcomed and dealt with promptly. It cannot be stressed too strongly that, if you are floundering around trying to overcome a string of minor difficulties, you will be wasting a great deal of valuable design time. Often, a quick telephone call, efficiently handled by the vendor's technical staff, can save hours of needless frustration.



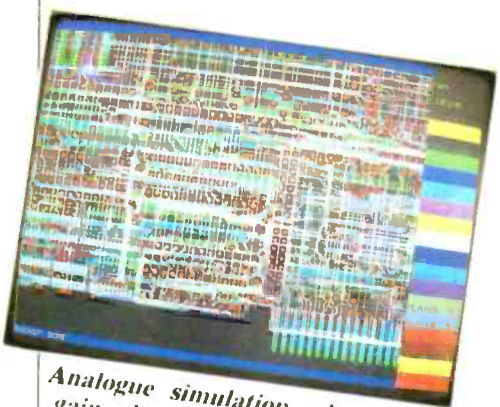
Logic simulation

One important point to remember about any system is that it is only as good as the person who operates it. Some cad vendors encourage the belief that, if the user enters the schematic information at one end and moves the mouse about a bit, a few minutes later a completed PCB design will emerge, as if by magic, at the other end. But the truth of the matter is that a novice will not be able to produce such good results as a seasoned professional, no matter how good the equipment he is given. The old saying "a bad workman blames his tools" certainly applies here.

For example, when an inexperienced

user sits down for the first time with an autorouter, he will often complain that an unacceptably low proportion of routeing is completed, or that the routeing has not been carried out as he would have wished. This necessitates a manual redesign which the operator blames on the autorouter. However, the truth is that the original design would have been unacceptable whatever the routeing method, and the autorouter has simply brought this to light early in the design process. Continual use of the system will soon indicate how to obtain the best results.

There are many other factors to consider before making your final decision. Speed of autorouteing alone is not all important, but should be taken in the context of the complete package. If the routeing is like lightning, but requires a great deal of manual rerouteing afterwards to bring it up to an acceptable standard, the benefits are lost.



Analogue simulation, showing gain, phase and group-delay plots

Make sure that there is one integrated database to cover all your requirements. A complete system written by a single vendor, which covers schematics, simulation, PCB layout, autorouteing and manufacturing outputs is worth a lot more than a rag-bag of non-integrated bits and pieces, all of which may be all right by themselves, but as a complete solution are useless. Smooth transition from schematic to layout and back-annotation the other way can make the difference between a highly efficient design aid and a set of software that causes you to tear your hair out.

Another factor which is becoming more important is the ability to exchange information with other cad systems. Look for DXF file production if you are going to wish to output your PCB information to one of the major drawing packages. To communicate with other electronics packages, the EDIF (Electronic Design Interchange Format) standard is becoming accepted as the norm. As more companies with whom you do business adopt cad, it may be important to be able to exchange information. They may not use the same equipment as you, so the ability to use a common communications language is vital.

It is possible to spend a lot more on a cad system than is really necessary. Obviously, the vendors at the top end of the price spectrum will encourage the view that "you gets what you pays for", and to a certain extent this is true. But do not ignore the lower-cost offerings just because of their price alone. PC-based systems have improved beyond recognition in the last few years, and if you go for software which can use expanded memory, for example, you overcome the limitations traditionally associated with systems priced at a more humble level. If you have a generous budget available, you could contemplate several networked PCs with a complete, integrated design/engineering system for each operator.

Make sure that the system you choose has been written specifically for electronics design. There are many "add-ons" for general drawing packages which enable them to be used for this purpose, but it costs no more to buy a specialized PCB package which should do the job much more efficiently.

So, there can be many pitfalls along the tortuous route of cad system purchase, but by a careful process of research and examination you should finally decide on a system which will be one of the best investments you can make. The time you will save once you are familiar with the system will enable you to increase your productivity or spend more time on other aspects of your business. Your output should be more professional, and the image you portray will be enhanced. Once the decision has been taken to step into the cad arena, it is a very rare occurrence to hear of a user reverting to old fashioned methods.

CODAS and PCS

Control systems, with calculations on their associated response characteristics and stability, form a specialised branch of engineering. Yet the ability to design and simulate performance of such systems reaches into many fields, not just electronic engineering. Traditionally, the performance of closed-loop systems has centred on establishing the damping, response time and general stability by means of the frequency and phase reponse characteristics and the associated transfer function. Each feedback control system has an open-loop as well as a closed-loop transfer function, given by,

$$\frac{E(s)}{R(s)} = \frac{G(s)}{1+G(s)\beta(s)}$$

In which $E(s)/R(s)$ is the closed-loop function and $G(s)\beta(s)$ is that for the open loop. The ability to plot the poles and zeros of the transfer function, which ultimately derive from the Laplace transform of the system (differential) equations, remains an important part of the control engineer's toolkit. Such plots are satisfactory for stable systems, but do not yield much information about unstable systems. With a low enough open-loop gain, all systems are stable, so by plotting the pole/zero positions as a function of open-loop gain as it varies from zero to infinity, a root-locus graphic is obtained on the "s" plane, showing the gain factor where instability sets in. In the practical system, this enables closed-loop design to be carried out with open-loop measurements.

Returning to the transfer function, this is a complex quantity. By replacing the variable s with $j\omega$, the sinusoidal response is obtained. The transfer function under this restriction now becomes the frequency response and can be plotted in a variety of ways. One is amplitude against phase, another is amplitude *vs* frequency, and a third possibility is of its real part against the imaginary part, with ω as a parameter, yielding the Nyquist plot. A modern powerful technique involves the state-space approach, in which vector and matrix relationships appear in the analysis and design procedures.

CODAS

The CODAS program from Golten and Verwer Partners carries out many of the techniques outlined above. It does time-domain step or impulse response and plots the frequency and phase response if required. It also outputs the Nyquist plot in response to a single-function key stroke and it carries out a root locus plot. It does not have vector matrix computing power for the state-space approach.

The program is designed for single-input, single-output control systems and runs under MSDOS on PC-compatible machines. Because of this, multi-loops and inputs cannot be handled on CODAS, but the associated program PCS goes some way to obviate this limitation.

The system equation is entered directly after "$G_c(s)=$" in a horizontal window. The "N" key enters the numerator, the "D" key the denominator; no fraction bar appears, but there is no ambiguity. Control engineers analyse the plant performance with regard to frequency response, time delay, phase and so forth, then add a compensator or controller in the loop to add phase lags/leads to widen stability margins or otherwise doctor the overall system response. These notionally separate functions are clearly handled in CODAS, the various plots giving immediate visual indications of the effects of changes in the parameters.

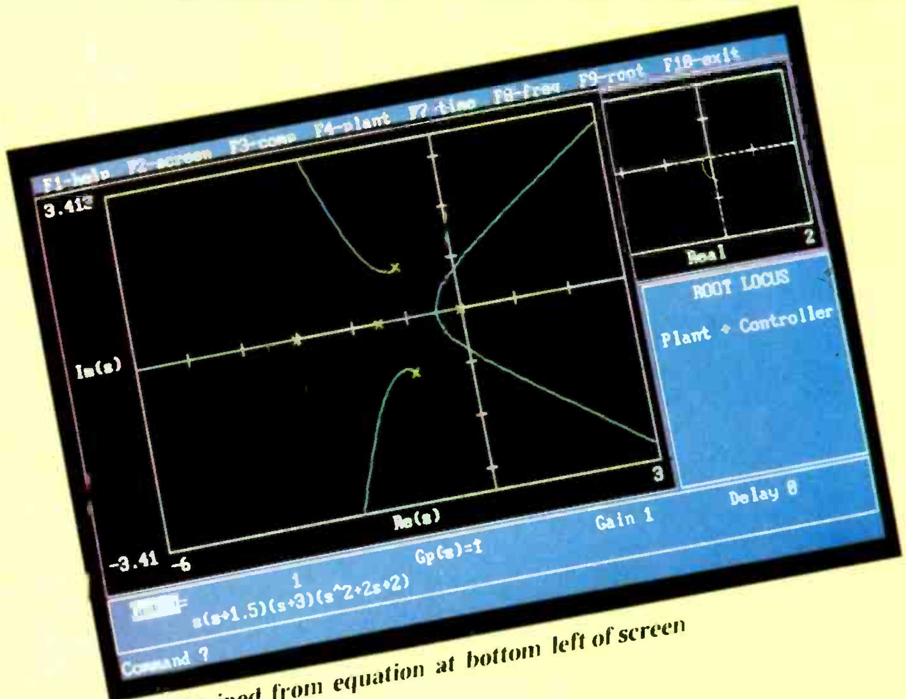
The status window along the top of the screen is clear, enabling the various plots to be called up instantly. The reviewer entered,

$$G_c(s)=\frac{1}{s(s+1.5)(s+3)(s^2+2s+2)}$$

as a hypothetical control system transfer function and obtained the plot in the illustration. This figure shows the quality of the graphics; clearly, EGA standards have been used. The clear layout and screen window structure as described can be seen.

Golten & Verwer have concentrated on control systems engineers with this product, but clearly for electronic engineers, the same processing can be imported for negative-feedback amplifier design and, with some thought, to such systems as phase-lock-loop designing. Of course, the ability to plot the impulse response and immediately to move into the frequency domain implies that Fourier relationships are embedded in this program suite.

On the other hand, some critical remarks could be made about the sketchy nature of the documentation for this material. The slim pamphlet has hardly any illustrations. (How often we see this even with fairly costly products!) The vendors would no doubt counter this by pointing out that the software was meant for experienced control systems engineers. But is this true? There surely would be a very good market indeed among those electronics engineers mentioned above, and certainly with educators and their students.



Plot obtained from equation at bottom left of screen

Operating environment
PC XT/AT or compatible computer.
MS-DOS operating system.
Mouse or cursor keys can be used.
For CODAS-EGA display;
for PCS-GGA.

PCS

Coming from the same people, this program "Process Control Simulation" in some ways complements CODAS. The program could very well have formed an option in CODAS, but there are arguments for a "stand-alone" version such as this. The function of PCS is mainly to simulate typical three-term controllers, the three terms originating as the direct proportional component, plus the derivative term, plus the integral action. The system can be modelled with outputs to a similar screen to CODAS and load changes, noise, other interference, together with control-effort limiting etc. can all be investigated. Again, the manual is even more slim than that for CODAS. Nevertheless, some convincing examples appear in the manual, showing the step response of three-term controllers when only one term (proportional control) is present. The offset and oscillatory tradeoffs are clearly shown. Then introducing the integral term shows how the offset is completely removed.

One consideration potential customers need to look at would be how quickly the cost of CODAS at £350 and PCS at £100 would be recovered in time saving. One cost saving can be made if both programs are purchased together; bundled, they cost £400. The deeper consideration involves value for money, by considering non-dedicated software in near-competition to this product. The reviewer has in mind general processing programs such as MATHCAD, which contain (for the same cost level) enormously more calculating power but much less immediate convenience. Users would have to write processing programs first, then use the plot power of say, the MATHCAD to yield similar results. A time penalty would be involved. As dedicated software for cad in control and negative-feedback systems, CODAS and PCS are excellent, if you can justify the investment. K.L.S.

CODAS and PCS
Golten and Verwer Partners,
33 Moseley Road,
Cheadle Hulme,
Cheshire SK8 5HJ
061 485 5435
CODAS £350 PCS £100

Using photovoltaic relays in multiplexers

Microelectronic power relays such as International Rectifier's PVA series are replacing electromechanical relays in many advanced multiplexer and instrument designs. Dave Moore of IR shows how they can provide designers with the benefits inherent in solid state performance.

Modern instrumentation system designs are almost entirely solid-state. One notable exception to this has been in analogue multiplexer inputs, which demand a level of performance that, until now, could only be met by the electro-mechanical relay (EMR).

The introduction of International Rectifier's photovoltaic relay (PVR) has brought a number of important benefits to multiplexing applications. These include greatly increased operating life, higher reliability and the ability to operate at higher scanning rates. In addition, measurement errors caused by thermally generated offset errors are eliminated. Operating power is reduced, greater mechanical ruggedness is achieved, and instrument board sizes are minimized. PVRs can be used as replacements for reed relays, stepper switches, crossbar switches and monolithic c-mos integrated circuits.

These advantages are made possible by recent advances in mosfet technology which enable the nearly-ideal open/closed contact parameters of EMRs to be essentially duplicated by semiconductor structures.

This is achieved by combining the linear switching characteristics of a bidirectional power mosfet (**Fig. 1**) with the electrical isolation provided by a photovoltaic generator (PVG) energized by a led (**Fig. 2**).

The PVG consists of a compact series connection of photodiodes in which p-n junctions are diffused into individual silicon wafers, stacked and alloyed together (**Fig. 3**). This configuration can generate several volts into an open circuit but can deliver only microamperes of output current (**Fig. 4**). The PVG is well suited to the drive characteristics of a modern mosfet, which requires several volts of signal for full conduction but draws virtually zero steady-state current. A charging current of only a few microamps can turn on a typical mosfet in a few microseconds – much faster than the response time of an electromechanical relay.

The release time of a PVR can be greatly reduced by the use of additional, active circuit elements (**Fig. 5**). In this circuit, the source-to-gate charge on Tr_1

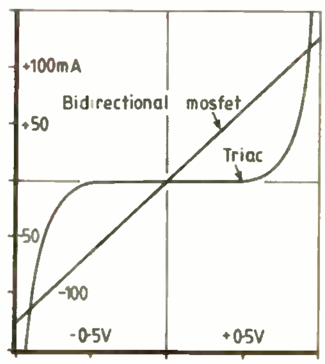


Fig. 1. Output characteristics of a typical bidirectional power mosfet.

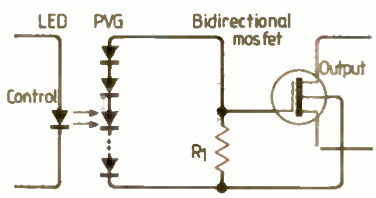


Fig. 2. Photovoltaic relay consists of led plus photovoltaic generator plus bidirectional mosfet.

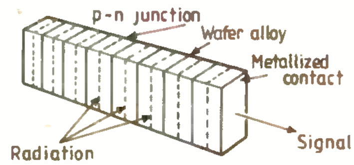


Fig. 3. Photovoltaic generator is a stack of series-connected photodiodes, edge-illuminated.

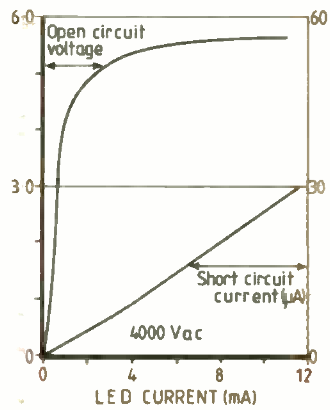


Fig. 4. Output characteristics of a 12-cell PVG.

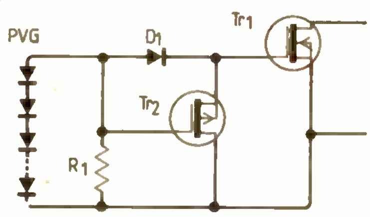


Fig. 5. Gate discharge circuit greatly reduces the release time of the PVR.

is short-circuited by Tr_2 whenever the gate voltage of Tr_1 is significantly more positive than the voltage across the PVG.

This configuration, requiring only a single PVG, achieves bounce-free drop-out release times in the 10 to 50µs range.

By capitalizing on features that are unique to the PVR, the innovative designer can now create higher performance systems of smaller size. For example, switching a 50V, 20mA (1W) load load, the PVR achieves an operating life in excess of 10^{10} operations. The best reed delays achieve only 10^9 operations at much lower power switching levels, even after screening and burn-in.

Actuation power, typically 50mW for a reed relay, is only 3mW for a PVR and therefore produces negligible heating. The simple output structure of a PVR minimizes thermal junctions resulting in thermal offset voltages of less than 0.2µV. Solid state switching also engenders bounce-free switching at speeds of less than 50µs, approximately twenty times faster than EMRs. Speeds of this order make higher scanning rates eminently practical and break-before-make operation is assured by a special fast turn-off circuit integrated into the power output stage.

Input drive, as well as requiring only 3mW of power, is non-inductive, eliminating the need for a coil suppression diode in the drive circuit. Greater packing density, too, can be achieved through both the small size of the PVR – less than 0.002 cubic inches per pole – and its total insensitivity to orientation, external magnetic fields and magnetic crosstalk, as well as very high shock and vibration resistance. Other features include up to 4000V AC isolation, high voltage blocking capability, very low on-state resistance and total freedom from latch-up. The switches remain open when the logic power is removed, and signal sources remain isolated without disconnection or short circuit protection precautions being necessary.

MULTIPLEXING

Analogue multiplexing requires an array of switches operating individually or in groups to connect each of several signal sources to a common amplifier or system. Multiplexing may be in either random order or sequential order (sometimes referred to as 'scanning'). **Figure 6** illustrates a low-level differential multiplexer using three switches per channel to connect the signal and shield or guard to a measurement system comprising a high gain amplifier, sample-and-hold, and an a-to-d converter.

Many important performance characteristics can be demonstrated using the simple test circuit of **Fig. 7**. This employs the PVA3354 as the switching element in a single-ended, eight-channel multiplexer configuration. DC leakage through individual switches can be observed by removing the logic drive power and connecting a 200V supply to the multiplexer (mux) common. A 10MΩ input impedance voltmeter connected between any input and analogue ground will show the leakage current as

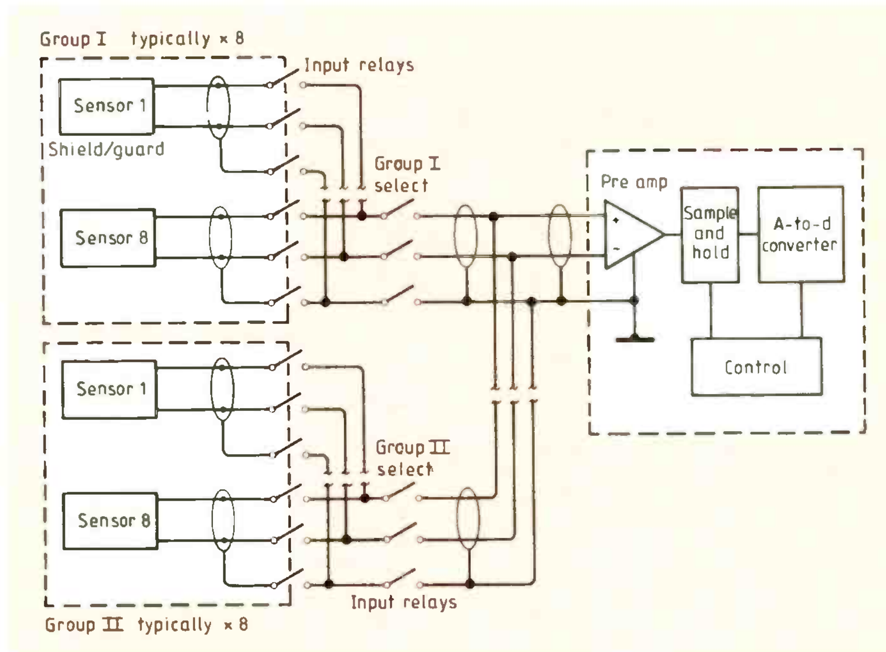


Fig. 6. Typical multiplexer system.

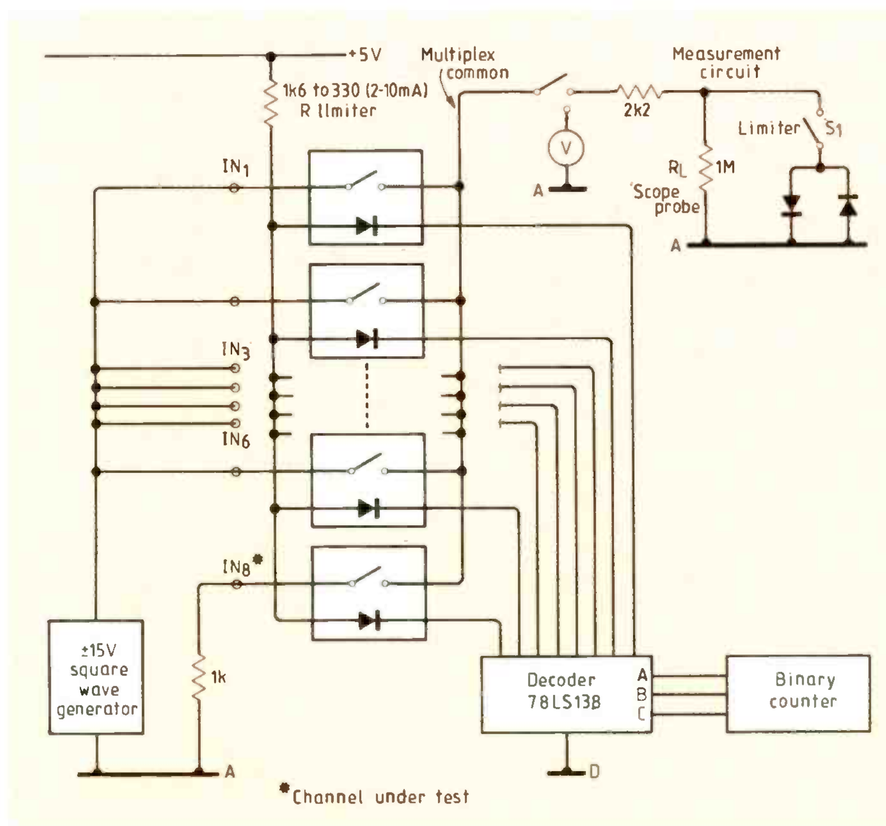


Fig. 7. Eight-channel multiplexer test circuit using photovoltaic relays.

the voltage drop across the 10MΩ input impedance. Conversely, connecting all inputs to a 200V source and measuring the mux common output yields the leakage through all eight switches. Typically, this measurement shows about 20nA, equal to an average off-resistance per channel of $10^{11}Ω$.

With logic power applied, the binary counter and decoder scan all eight channels sequentially. Because of the make-before-break operation of the PVA, no delay is required between successive addresses. A zero-volt, 1kΩ source is connected to the channel under test. By connecting the remaining channel inputs to a 30V pk-pk square wave generator, the effects of crosstalk and settling after extreme preconditions on the previous channel can be simulated. By adjusting the control current limiting resistor, the effect of varying control current on switching speed can also be determined. The use of a square wave shows the effects of crosstalk as a disturbance of the settled 0V signal.

On turn-on, a short delay occurs before the previous channel is disconnected from the mux common. The mux drifts slowly toward 0V until the channel under test begins to turn on and rapid settling occurs. At turn-off, the short delay is experienced but the mux common does not appear to move until the next channel begins to turn on. The full transition occurs in less than 50μs. The traces are taken with the diode clamp circuit connected to prevent overloading of the oscilloscope input.

Switching speed is dependent upon control current (**Fig. 8**) and speeds an order of magnitude faster than a high quality reed switch can be readily achieved with a 74LS series driver. The turn-off delay remains fairly constant until the drive pulse becomes too narrow to allow complete charging of the fast turn-off circuit, extending the delay before turn-off occurs. Charging speed may be increased with greater control current or by means of an RC circuit to speed charging while limiting the steady current to a nominal value.

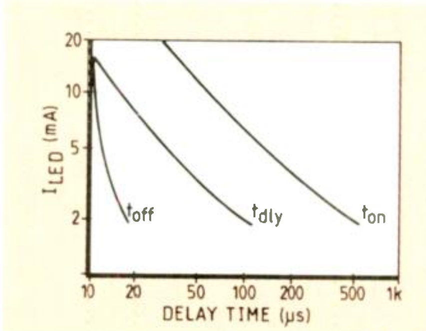


Fig. 8. Typical switching delay for the multiplexer of Fig. 2.

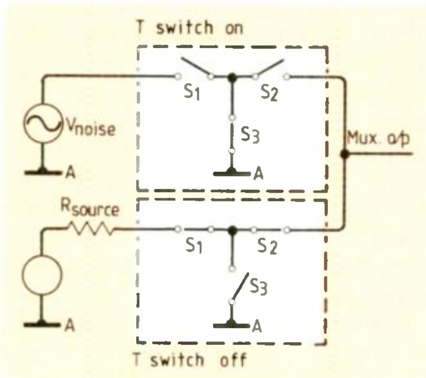


Fig. 9. Simplified arrangement of T-switch multiplexer.

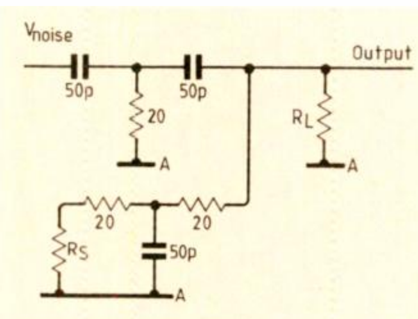


Fig. 10. Equivalent of T-switch circuit.

The closed-circuit resistance of a PVR is greater than that of a metallic contact. The PVA3354, for example – a bidirectional 300V relay – has a typical on-resistance of 20Ω. The PVA1354, a 100V relay, offers a 5Ω resistance. Comparable unidirectional relays such as the 300V PVD3354 and the 100V PVD1354 have on resistances of 5Ω and 1Ω respectively. However, although the on-resistance is significant it is constant and stable and does not degrade throughout the switching life of the relay. This allows compensation to be made in the design or calibration of the system.

MULTI-LEVEL MULTIPLEXING

The maximum voltage appearing across an open switch must be limited to less than the maximum blocking voltage in order to prevent breakdown occuring. A multi-level multiplexing scheme such as that shown in Fig. 6 can be used to double the number of switches in a circuit, thereby doubling the breakdown voltage.

To achieve a low on-resistance, a solid-state switch requires a large area chip. This results in increased capacitance which must be taken into consideration in evaluating crosstalk for high frequency signals. The non-linear open circuit capacitance of a PVA series device varies from 50pF to 10pF with applied voltage. Larger signals or signals with a large DC bias therefore tend to reduce capacitance and result in less crosstalk.

Cascading through two switching levels also reduces cross-talk. For example, the worst case capacitive coupling for a 64-channel mux is reduced by a ratio of 14/63 or −13dB over a single level multiplexer.

THE T-SWITCH

Where pulses or high frequencies are to be multiplexed, improved crosstalk rejection can be obtained by use of the T-switch configuration shown in **Fig. 9**. By attenuating the capacitively-coupled noise signal using shorting switch S_3, a much smaller error signal is passed through to the mux output. The equivalent circuit shown in **Fig. 10** may be used to calculate the worst case crosstalk for the PVA3354 device.

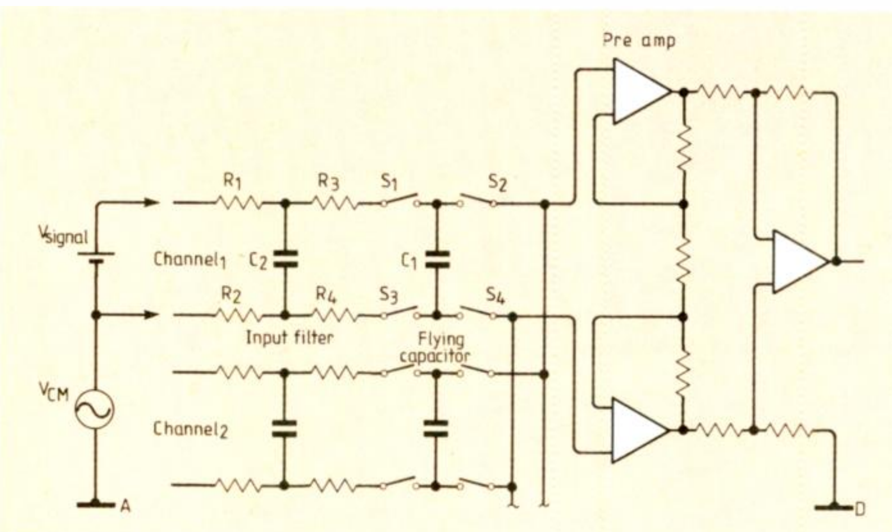


Fig. 11. Flying capacitor multiplexer: this offers excellent common mode rejection and isolation of the common mode source from the measurement system.

FLYING CAPACITOR MULTIPLEXER

A flying capacitor multiplexer (**Fig. 11**) uses two pairs of switches per channel to isolate both signals and return from the measurement system. Mainly used with low-level, low-frequency inputs such as thermocouples with accompanying high common mode voltages, this technique offers excellent common mode rejection and isolation of the common mode source from the measurement system. A low-pass filter, R_1, R_2, C_1 is often used on the input. The flying capacitor C_2 is initially charged through S_1 and S_2. Resistors R_3 and R_4 are necessary to avoid pitting of the metallic contacts by limiting transient currents on switch closure. The use of semiconductor switches eliminates the need for R_3 and R_4 and consequently also eliminates their scaling error. The PVR can easily handle switching transients and therefore has a greatly extended life compared with that of a high quality reed switch.

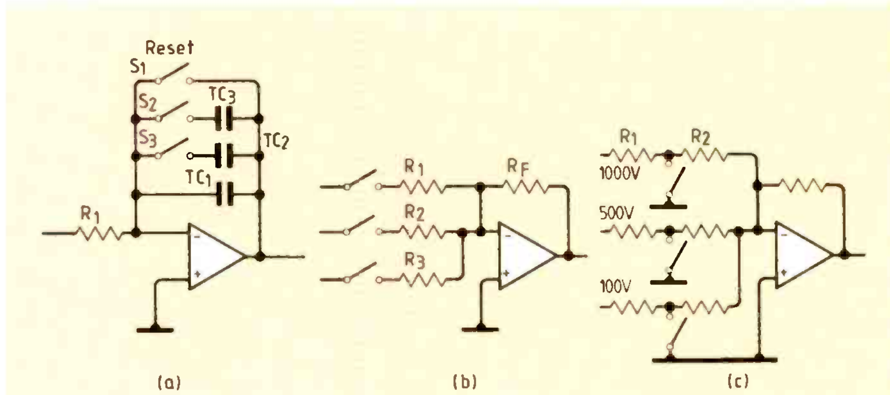


Fig. 12. Applications of photovoltaic relays: (a) integrator time constant and reset selector; (b) input selector; (c) high voltage selector.

VARIATIONS

Figure 12 illustrates three typical applications of PVA series relays. At (a), switch S_1 provides a reset by shortening the feedback capacitor – an operation which can prove fatal to reed relay contacts. Switches S_2 and S_3 vary the integration time constant.

Figure 12b illustrates an input selector for use with an operational amplifier. **Figure 12c** illustrates how high-voltage signals can be attenuated using PVRs to achieve accurate selection for multiple inputs. The 300V blocking capability of the PVA3354, for example, allows a relatively high ratio of R_2 and R_1, thereby minimizing loading and interference between channels. ■

Exploiting millimetre waves

The DTI is seeking to encourage civil use of the enormous, still largely unused, radio spectrum above 30GHz. But DTI still has not finalized the national frequency plan or the degree of regulation or deregulation to which such installations will be subject.

At present, apart from Defence systems not subject to DTI licensing, the only approved allocations appear to be the 49.2–50.2GHz band taken up by Mercury Communications and the 47–47.2, 75.5–76, 142-144 and 248-250GHz allocations in the current UK amateur licence.

In September 1988 the Radiocommunications Division of the DTI published a 40-page consultative document "The use of the radio frequency spectrum above 30GHz" and an associated article "Making the most of millimetres" (*British Business Supplement* 23 September, 1988). These drew attention to a considerable number of potential applications and invited potential users and manufacturers to suggest other uses and to report on the latest technical developments.

Altogether 41 responses were made: 12 from potential users; nine from manufacturers; nine from research organizations; 10 from standards/regulatory bodies; 10 from central/local government; and three in other categories (some respondents fell into more than one category). The DTI considers that about 30 of these offered substantial comment.

A one-day IEE colloquium "Radio communication in the range 30–60GHz" gave an opportunity to review the current regulatory and technical situation at a time when the DTI is preparing to issue licences for two bands, one near 40GHz (provisionally 37–39.5GHz) and the other close to the 60GHz oxygen absorption band (provisionally 54.25–58.2GHz) which is attracting interest for short-range (1–2km) broadband radio networks. The excess attenuation of around 10–16dB/km means that the same channel could be re-used within about 5km or less where signals are screened by buildings or trees or the antenna dishes mounted on the sides of buildings in an urban environment. Oxygen absorption, unlike water vapour, is the same in all countries (**Fig.1**).

Range in the oxygen absorption band is reduced by a factor of ten compared to that about 40GHz and this band is also of particular interest to the Defence services because of its resistance to interception or jamming. The colloquium chairman, Dr R.C.V. Macario, however, was highly critical of what he felt to be an unduly pessimistic DTI assessment of frequency-reuse distances for other segments of the 30–60GHz spectrum. L. Powis (Plessey Research) described potential applications of millimetre-wave communications to military systems in general rather than specific terms since most current projects are classified.

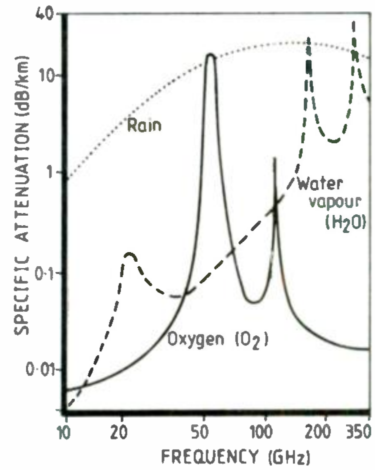


Fig.1. Attenuation of millimetre-waves by atmospheric gases and rain. Oxygen (O_2) has a particularly sharp peak at about 60GHz, cutting signal intensity by 95% for each kilometre. The effect of the various attenuations is cumulative.

In general, civilian applications tend to be stymied by the current cost of millimetric devices, for which costs are unlikely to come down until in quantity production – and this will not come about until the regulatory situation is determined, and specific frequencies released; even then there may be something of a "chicken and egg" situation.

Apart from broadband local area networks and private building-to-building links in situations unsuitable for optical fibre cables, the most promising mass use of mm-waves appears to be by BT for its M^3VDS video distribution system (see *E&WW* December 1988, p.1249 and December 1987, p.1274) for which the Saxmundham demonstrator unit operates on 29GHz but which seems likely to use 38-42GHz in service.

This system was initially developed to provide local links for the SIS racecourse video coverage relayed via satellite to betting shops, some of which are unable to receive the satellite signals directly because of screening. BT believes that M^3VDS could be introduced by 1991: "It will be economic. It will happen".

BTRL is making good progress with monolithic millimetric integrated circuits on GaAs wafers. At present the down-converter uses a chip set including a single-balanced mixer, two monolithic IF amplifier chips and a hybrid 27GHz local oscillator using a chip fet

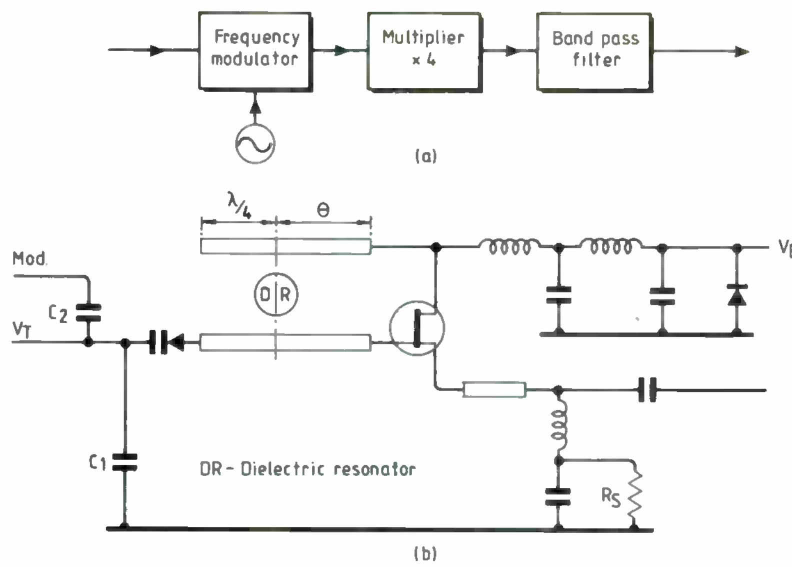


Fig.2. 40GHz source developed at Leeds Polytechnic based on a 10GHz fet DRO and a times-four varactor diode multiplier.

and a dielectric resonator mounted on an alumina ceramic substrate. This remains within ±3MHz over a temperature range −20/+40°C. Currently a GaAs monolithic oscillator is being developed and will be incorporated with the mixer and IF amplifier chips to produce a fully monolithic down-converter. Provided a reasonable yield can be achieved, BTRL believes that viewer terminal costs should be comparable to those for 12GHz satellite television reception.

LEP of France has recently reported (*Electronics Letters*, 30 March, 1989, pp442-3) monolithic LNAs for 12–16GHz with less than 2.5dB noise figure, 9dB gain, using high-electron-mobility transistors (HEMTs) fabricated on MOVPE structures.

At the colloquium, R. Davies (Plessey Research) reviewed new mm-wave devices with particular reference to HEMT devices. By allying modern material growth techniques with advances in device physics, low noise performance has been demonstrated up to 94GHz. While GaAs fets with 0.25μm gate lengths can operate at up to about 40GHz, the latest generation of HEMTs offers the promise of high performance up to 100GHz with low cost in volume production. The use of indium phosphide (InP) for HEMTs has great potential although this is a difficult material to work with.

Millimetre-wave oscillators usually take the form of backward-wave or klystron valves or Gunn or impatt semiconductor diodes but Dr L.A. Trinogga (Leeds Polytechnic) argued that the present solid-state sources suffer from excessive heat dissipation, poor frequency stability and modulation difficulties. He presented the design of a 40GHz source (**Fig.2**) comprising a 10GHz dielectric resonator based on a GaAs fet with a tuning range of 22.5MHz (without variation in output power) and having a stability of 2.76ppm/°C integrated with a modulator and followed by a four-times frequency multiplier using a high-Q GaAs varactor diode (type D5002-48, which has a breakdown voltage of −10V and a cut-off frequency of 550GHz at −6V) with microstrip low-pass and band-pass filters.

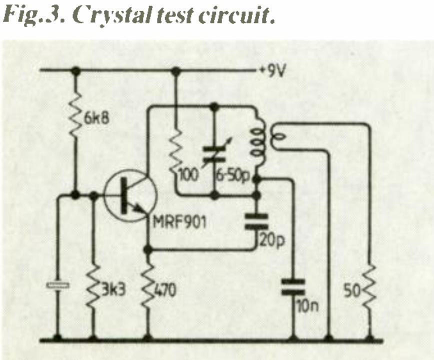
RF Connections is written by Pat Hawker.

Test circuit for overtone crystals

Progress in quartz crystal fabrication has resulted in crystals of ever higher fundamental frequencies, suitable for overtone operation and sometimes fundamental operation throughout the VHF spectrum. It is however still useful to be able to check quickly the suitability of older crystals for use at high overtones. Clint Bowman, a retired American engineer, has described in *RF Design* (January 1989, page 58) a novel test oscillator suitable for use over a range of about 65 to 200MHz, initially intended to test fifth overtone crystals cut for 65 to 72MHz at higher-order overtones, up to and including the 15th at about 200MHz.

His circuit (**Fig.3**, below) is a variation of the classic "tuned-plate, tuned-grid" valve oscillator, where the grid circuit provides a selective filter to sustain oscillation, or not, dependent upon the filtering bandwidth and frequency relationship with the plate (anode) circuit. In this arrangement, feedback is provided to the unbypassed emitter circuit. When the tank circuit is tuned to the fundamental or overtone frequency, oscillation is sustained. Since the 0.01μF disc ceramic tank bypass capacitor becomes progressively less effective as the frequency increases, thus increasing the degree of feedback, while the 20pF capacitor is placed close to the "cold" end of the tank circuit to provide additional feedback, it is claimed that the circuit provides reliable and repeatable oscillation to at least 200MHz when used with a suitable crystal. The upper frequency is limited by the shunt capacitance and/or activity of the individual crystals. Excessive shunt capacitance results in a broad area of uncontrolled oscillation, with some crystals showing this effect as low as 150MHz. Correct operation results in stable, crystal-controlled oscillation as the tank circuit is tuned through each of the usable overtone frequencies with no output at intermediate frequencies.

Fig.3. Crystal test circuit.



Elevated vertical antennas

Radio Broadcast (*E&WW*, August 1988, page 832) drew attention to an American computer study that confirms in principle the experimental work carried out in the early 1980s by a small group of retired engineers who were also radio amateurs: Archibald Doty, John Frey and Harry Mills. They investigated monopole antennas using elevated wire "counterpoise" radials rather than the conventional 120 or more buried radials favoured for medium-wave broadcasting since the classic work in the 1930s of the late Dr George Brown. The results showed the feasibility of using a few elevated wire radials and so of reducing the cost and complexity of MF and HF broadcast and communication antenna systems.

In effect, instead of buried radials, the antenna becomes the familiar "ground-plane" elevated vertical with three or four wire or rod radials widely used by radio amateurs on HF and for the base antennas of VHF land and sea mobile services (**Fig.4**).

Practical development of this form of elevated vertical antenna is generally credited to Dr George Brown of RCA although an earlier description can be found in a series of patents: "Aerials: directive wireless signalling" awarded to Dr Maurice Ponté of CSF, France: French patent No 764,473 (1933), US patent No 2,026,652 (1933) and UK patent No 414,296 (1934).

About 1981, Dr Brown, on one of his many visits to London, told me the story of how he came to develop the ground-plane antenna and how it was subsequently modified to make it more readily marketable. It is a story that could help to simplify the construction of elevated monopoles further.

He told me that the antenna was devised in the 1930s to meet an early requirement for communicating with American police cars, then using frequencies of the order of 30 to 45MHz. Its success was immediately apparent when, at the very first demonstration, the transmissions reached well beyond their expected service range. This original design used only *two* horizontal radials, but the RCA sales engineers soon reported that they could not persuade potential users that a two-radial antenna, with the radials resembling a half-wave dipole, would provide omnidirectional radiation. On the classic principle that the customer is always right, Dr Brown and his colleagues promptly added two more radials at right angles to the others in a configuration that soon became firmly established, although there was little reason to suppose that either radiation efficiency or the horizontal radiation pattern was improved by the extra radials.

Since then it has become increasingly difficult to persuade people that configurations other than the four-rod or four-wire radials will form an effective ground-plane antenna. It also seems to be a common fallacy that the elevated ground-plane has the same 35Ω feed-point impedance and vertical radiation pattern as the earthed-monopole with its "infinite" ground-plane. In fact, the elevated ground-plane with horizontal radials has a base impedance of roughly 19Ω, although this can be increased by sloping the radials downwards.

During recent years there have been further investigations, some computer-based, that point to yet further simplification of elevated vertical antennas. For example, Les Moxon, G6XN, in "HF antennas for all locations" (RSGB, 1982) advocates the use of a single short loaded radial. Then there is the "zero-extent ground-plane" with no radials but with a lossy ferrite (or coaxial) choke on the co-axial feeder to stop RF current flowing down the outer braid. This form of antenna has been analysed in the book "Monopole elements on circular ground planes" by Melvin Weiner (Mitre Corporation) *et al.* (Artech House, 1987), **Fig.5.** The effect of the size of the ground-plane was also considered in some detail in a paper "The radiation patterns of ground rod antennas" by W.V. Tilston and A.H. Secord (Sinclair Radio Laboratories Ltd. Canada) in *Electronics and Communications*, August 1967, pages 27 to 30. This showed that the two common but conflicting assumptions about the vertical radiation pattern (VRP) of a ground rod antenna are both wrong. The radiation is neither always tilted up nor always directed towards the horizon. In fact the VRP of ground rod antennas varies markedly with changes in monopole and radial length and the degree to which current is kept off the feeder line.

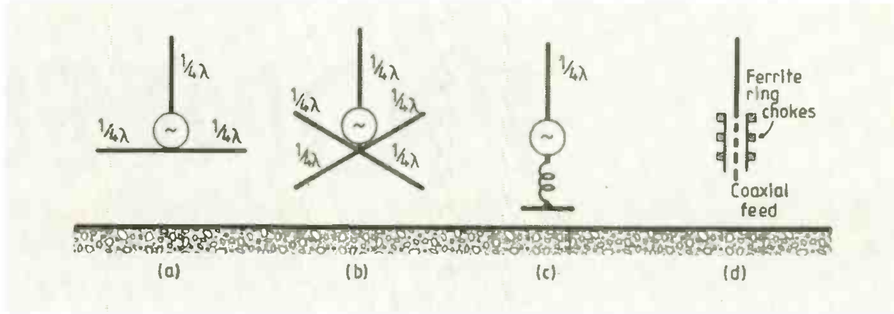


Fig.4. Elevated monopole ("ground plane") antennas: (a) original configuration as developed by Dr George Brown; (b) conventional four-rod antenna; (c) antenna with short loaded "counterpoise" as developed by Les Moxon; (d) zero-extent ground-plane antenna.

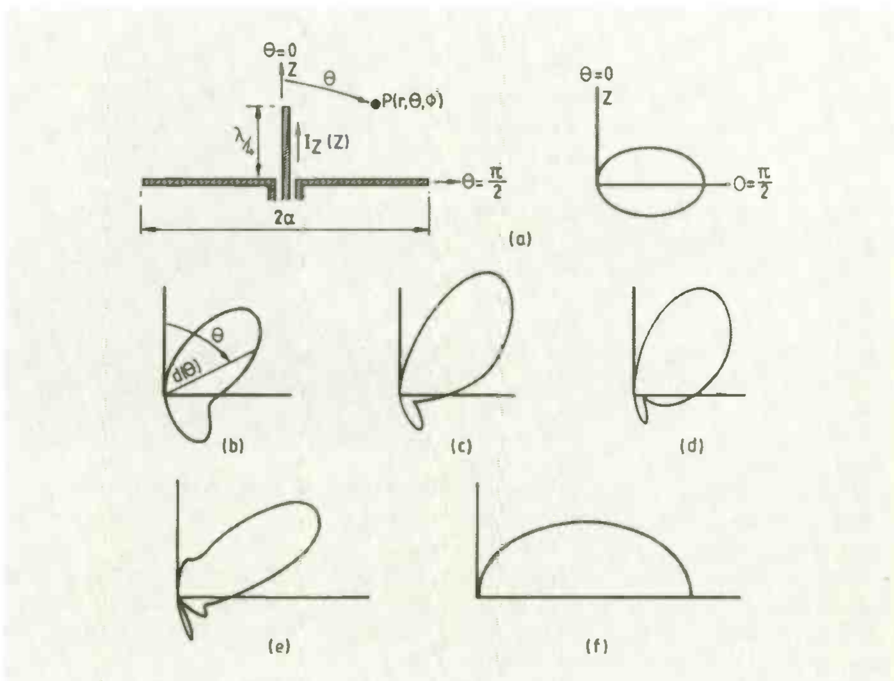


Fig.5. Vertical radiation patterns showing effect of the extent of the ground plane, as analysed by Melvin Weiner. Diagrams show elevation directive gain pattern of a thin quarter-wave element mounted on a ground plane of radius a: (a) $2\pi a=\infty$ (i.e. wire radials in free space); (b) $2\pi a/\lambda=3$; (c) $2\pi a/\lambda=4$; (d) $2\pi a/\lambda=5$; (e) $2\pi a/\lambda=\sqrt{42}$; (f) infinite ground plane (i.e. monopole over a perfect earth such as sea water).

Les Moxon has been concerned primarily with the radiation efficiency rather than the VRP. He has found himself facing much the same situation as that which faced Dr Brown. It is proving difficult to convince others of the efficiency of short radials and of the value of just one radial, providing that it is short enough. His views seem to be regarded as heresy of the worst kind. The result is that much effort (amateur and professional) continues to be misdirected at "improving" multiple buried earth systems or using three or four-wire elevated radials. Such an approach inflicts maximum inconvenience and cost and inhibits the construction of directional arrays. Multiple quarter-wave elevated radials also have a major disadvantage since the rapid change of impedance close to resonance can cause severe problems of equalization.

Les Moxon insists that over a wide range there is no significant difference between short and long HF radials in respect of any important aspect of performance. In regard to the VRP for long-distance, low-angle radiation, it seems likely that a short or zero-extent ground plane would be better.

Much of the confusion arises from considering the elevated ground-plane antenna as a monopole when in fact it is a bent dipole configuration with reduced radiation from one side.

PIONEERS

31. Konrad Zuse: inventor of the first successful computer.

W.A. ATHERTON

The world's first successful digital computer was destroyed by an Allied bomb during a raid on Berlin in World War II. Now known as the Z3, it was designed by Konrad Zuse and built at home with the help of friends. Another Zuse computer aided the design of aircraft wings at the Henschel factory in Berlin and was the only German computer to see war service. An improved model was probably captured by the Russians when they overran Berlin in 1945, though Zuse doubts that they knew what to do with it.

Surprisingly, Konrad Zuse is still relatively unknown, despite being recognized as the designer and builder of the first working computer. For a long time it was thought that the Americans had designed the first computers; but then came news of the British code-breaking machines, and then Zuse's work. In fact Zuse began his first design before the war started. He did much of the work in his spare time and even during the war there was relatively little official help. After the war he set up his own company and at one time he was the major continental manufacturer. His firm employed about a thousand people in its heyday.

Zuse is now approaching eighty, and one might expect him to look back reflectively over his life; but not so. He is a successful artist and painting vies with computers as his first love. Whilst he appreciates the honours heaped on him, he is still an active engineer and rather wishes people would give him problems to solve instead of passing him around "like a museum piece"[1].

He was born in Berlin on June 10, 1910, but his parents soon moved: first to Braunsberg in East Prussia and then to Hoyerswerda in Saxony, where his father was the local postmaster. It was here, about 35 miles north east of Dresden, that his school awakened his interest in engineering at a time when his talent as an artist was also developing.

Professor Dr. mult. Konrad Zuse

This combination and rivalry between art and engineering caused him to drop out of university and is still a part of his life.

At the Technical University in Berlin-Charlottenburg he found the work stultifying, especially the technical drawing. So he quit the university, horrifying his parents in the process, and decided to become a commercial artist. He also turned to inventing, and devised a machine to develop and print colour photographs automatically.

But times were hard, economies bad, and millions were out of work. So he did the "sensible" thing and went back to university, re-emerging in 1935 with a degree in civil engineering.

The mother of invention

The Henschel aircraft works in Berlin offered Zuse a job as a stress analyst, the beginning of an on-off relationship between the two. The work proved boring; it involved repetitious calculations for which, thought Zuse, there must be a better way – a machine, perhaps. It was not the first time he had entertained such thoughts because his degree course had exposed him to equally tedious work with a slide rule.

It was not only the calculations that bothered him but also the "traffic control": noting intermediate solutions, transferring them to other parts of the problem, and so on. His first thoughts (around 1933-34) had been to devise pre-printed forms to control and record the flow of work in a standardized way for some common problems. This was followed by ideas for punched cards and mechanical calculation. In fact, whilst still a university student, Zuse had already arrived at fundamental ideas for information control, the reduction of problems to a sequence of simple operations, and the concept that a machine could be built to carry out that sequence. By 1934 he was using the terms "memory unit", "selector" and "control device". When work at the Henschel factory reinforced his thoughts he set about building a machine in his spare time using the living room of his parents' home in Berlin as his workshop[2].

Necessity was not the mother of invention, says Zuse, it was laziness and boredom: the desire to rid himself of those tedious calculations[3].

Launching the V1

One of his first decisions proved crucial to success: to use binary arithmetic instead of decimal. One of the friends whose help was enlisted, Walther Buttmann, was asked to research the published work of Gottfried Liebniz in the Berlin University library. It was Liebniz who had first studied binary arithmetic in the 17th century.

So in 1936 Zuse started making the component parts of his first all-mechanical machine: using metal pins and slotted metal plates, the ends of the slots representing ones and zeroes. The memory was to hold 64 binary numbers of 16 bits each and he successfully completed it with help from friends who laboured to make the thousands of parts by hand. However, the more complex arithmetic unit required greater manufacturing precision than they could achieve. Programs were coded by punching series of up to eight holes into discarded 35mm movie film, which was far cheaper than the commercially-available paper tape.

This machine was named the Versuchsmodell-1 (experimental model 1) or V1 for short. It was followed by a V2, both of which were later renamed the Z1 and Z2 to avoid confusion with the V1 flying bomb and the V2 rocket.

The Z2 re-used the successful memory unit of the Z1 but with an arithmetic unit made from second-hand telephone relays. Here another friend, Helmut Schreyer, came into his own. Like others, Schreyer had done his share of cutting out metal plates for the Z1. Now he suggested using electromechanical relays instead of the mechanical pins and slots.

"At first I thought it was one of his student pranks..."

New relays were expensive, and since funding was coming out of their own pockets and those of friends and friends' parents, every penny counted. A fully mechanical computer had proved impracticable and a full-sized relay machine would need thousands of relays; so a test model was built using just 200 second-hand relays.

By this time, Zuse had developed the design of his future computer to the stage where he had achieved the yes-no (binary) logical structure for the machine and recognized that it was independent of the physical methods used to build it.

An electronic computer

The possibilities for a relay computer looked optimistic when Schreyer suddenly suggested using electronic valves instead. Though they were not then commonly employed for switching between two states, valves could be used in that way and would be far faster than relays. "At first I thought it was one of his student pranks – he was always full of fun and given to fooling around", Zuse has recalled.[4]

About 2000 valves would be needed. Asking for them, and getting them, were two different things in a Germany then at war. Private enterprise stood no chance so they talked to the German Army Command (OKH). Whilst the initial reaction was favourable, the idea foundered when they said it would take about two years to build. "And just how long do you think it'll take us to win the war?" they were asked.

So little help came, but by the end of the war Schreyer had built an experimental computer with just 100 to 150 valves, and gained his doctorate on the way for his work on valve switching circuits. Like the other computers, this too was a casualty of the war. After the war the development of electronic equipment was banned in Germany and so Schreyer emigated to Brazil. It was there that he died in 1985.[2,4]

Whilst Schreyer worked part-time on the electronic machine Zuse completed the electromagnetic relay computer, the Z3, encouraged by the Experimental Aircraft Institute. The Z2 had convinced the Institute of the usefulness of Zuse's ideas and so it financed the Z3, though Zuse still had to work alone and at home. And he had to escape a recall to active duty for service on the Eastern Front.

The Z3 was the first general-purpose digital computer in the world. It was completed in 1943. It employed binary numbers, floating-point arithmetic and a 22-bit wordlength, and it has been estimated that it used around 2000 relays (and eight uniselector switches) and cost the equivalent of between $6000 and $7000. "The most important thing", says Zuse, "seemed to be to keep the frequency absolutely even, so that one cycle equalled one addition"[4]. This he achieved using a rotating disc or roller.

Konrad Zuse (right) and his friend Helmut Schreyer (left) at work in Zuse's parents' apartment in Berlin, c.1936. (Photographs in this article are by courtesy of Konrad Zuse).

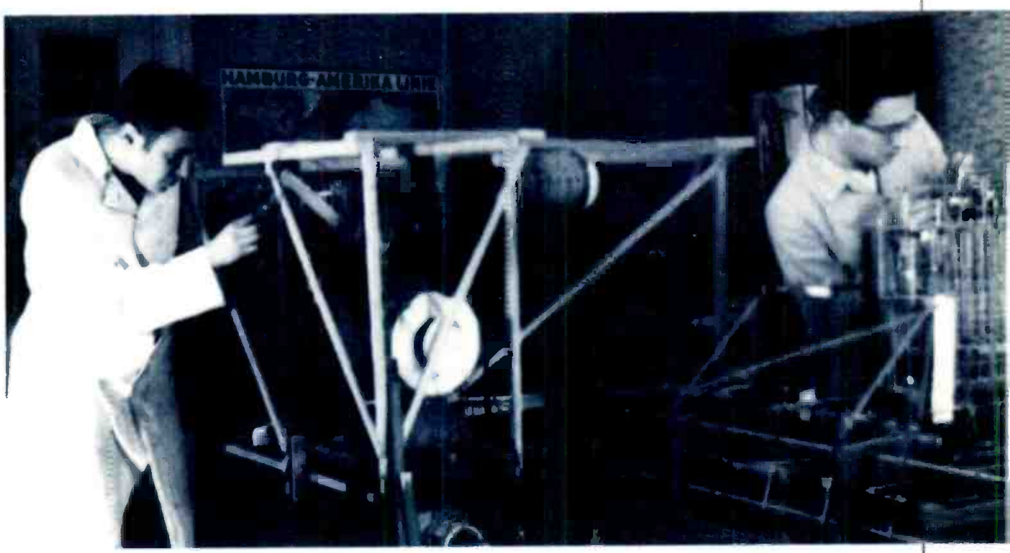
each revolution defining one operation. As the disc's speed could be varied, so too could the operating speed of the computer. Sparking at the relay contacts was eliminated by making or breaking them before any current flowed, so increasing reliability. Post-war Zuse machines are said to have been "legendary" for their reliability.[2]

Although the Z3 was completed (with the help of friends) it served mainly as an experimental machine and, according to Ceruzzi, it never went into routine use probably because of the limited capacity of its memory.[2] There are no doubts, however, that it was fully functional, because there are several witnesses to its operation. Though the original Z3 was blitzed out of existence a reconstruction was made years later, based on the surviving patents, and is now in the Deutsches Museum in Munich.

The survivor

Somehow Zuse found time to build other computers as well. The S1 was a non-programmable machine using hard-wired programs. It served in the design of the Henschel flying bomb HS-293, a pilotless aircraft guided by radio from a bomber. It replaced a dozen calculators. An improved design, the S2, was too late for routine service and is the one that Zuse thinks might have been captured by the Russian army. But the big one was the Z4: a full-sized general-purpose computer, the only one to survive the war.

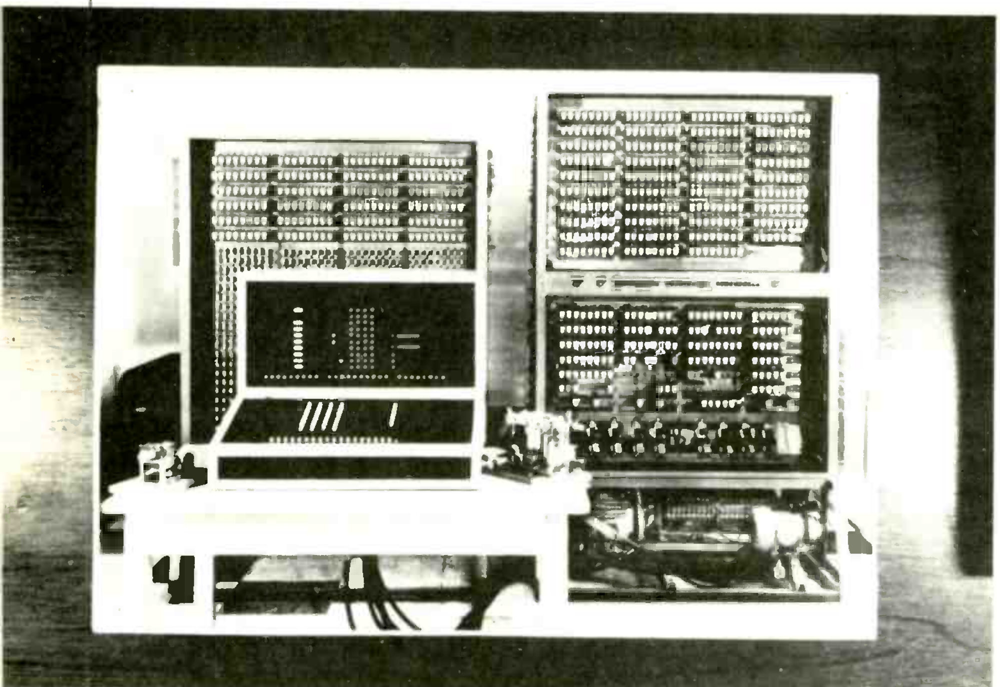
Construction of the Z4 began in 1943, even before the Z3 was finished. For this large machine Zuse returned to his successful mechanical memory design. Whilst this now seems a retrograde step it was the only way he could achieve a large memory (1024 32-bit words) in a



reasonable volume. Using the Z3 relays approach would have required 32 of the Z3 memory cabinets.

Work on the computer began in Berlin but Allied bombing posed an ever-present threat. "My workshop was damaged several times, and three times during the war we had to move the Z4 around Berlin."[2] As allied bombing increased in 1945, the authorities decided to move Zuse and his new computer out of the capital to Göttingen, 160 miles to the west. There construction was completed and on April 28, 1945, demonstration programs were run for the authorities. "This was the moment for which I had waited for 10 years – when my work finally brought the success I desired." The irony for Zuse was that the machine was immediately dismantled, because the American army was by then just a few miles away.

The odyssey continued as they were ordered to underground works in the Harz mountains where the V1 and V2 weapons were being built. Zuse has described the conditions there as terrible. "We refused to leave the machine there." With great difficulty it was moved to an alpine village just north of the Austrian border where it was set up in a barn. There it stayed until 1949 when it was rescued, rebuilt and established in the Technical University in Zürich in 1950. For a time it was the only functional digital computer on the continent.[2] It too is now in the Deutsches Museum.



The reconstructed Z3 computer at the Deutsches Museum, Munich. Left, memory unit; right, control and arithmetic unit; front, keyboard/display with paper tape reader to the right. In the original were two cabinets for the memory unit, each measuring about 6×3×1 feet.[2]

After the war

Zuse continued to develop his ideas for computers and planned what was probably the first algorithmic computer language. The game of chess served as a test subject.

In 1949 he re-established his own firm which became known as Zuse KG. With contracts initially from Switzerland and then Germany the firm prospered and for many years was second only to IBM in Germany. One of the first clients was the camera manufacturer Leitz, and by the mid-1950s Zuse KG almost had a monopoly in the area of scientific computers for the optical industry in central Europe. The Z series continued with relay computers and then fully electronic machines. The last of the relay machines was the Z11 which became a byword for reliability. As competition grew, and technology changed, so life got tougher and outside funding was required. This eventually led to the company's being absorbed by Siemens.

Zuse is still a consultant; but even more he is a painter, whose work has been described as "a synthesis of expressionism and surrealism, in brilliant colours that border on the psychedelic". One engineering task that he did take up in the 1980s, however, was to rebuild the Z1 from memory – as a museum piece. ■

The Z4 at the Technical University, Zürich, 1950.

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Next: Charles Tilston Bright, British pioneer of submarine cables.

Tony Atherton is a principal lecturer at the IBA Harman Engineering Training College, Seaton, Devon.

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Digital tv receivers for the satellite age

ITT Semiconductors' Digit 2000 system, launched in 1981, is still the only receiver system to offer all-digital processing of picture, sound and teletext. Hans G. Keller shows how the system has been updated to handle digital video recording and satellite transmission decoding.

In principle, it is possible to implement all the signal processing operations required in a tv receiver digitally. However, technical limitations still exist in the high frequency and power range. At present therefore, digital signal processing only begins after the demodulation stage with the video and audio baseband signals and ends with the drive signals for the video and audio output stages.

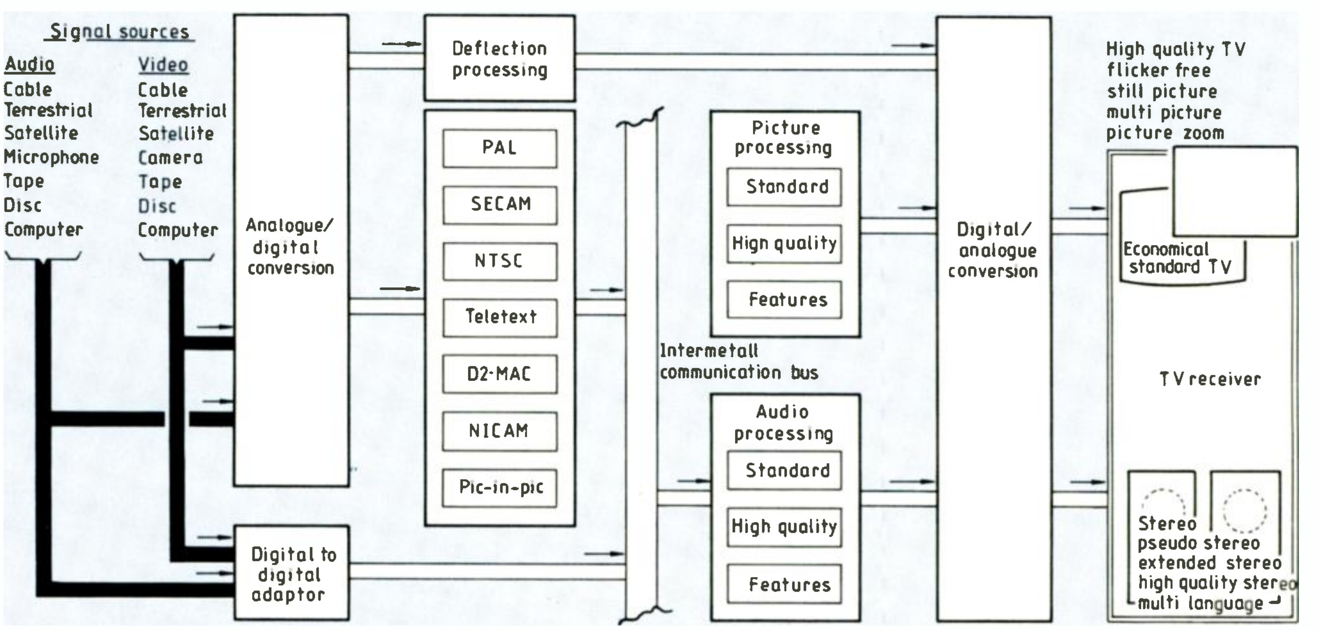
An outline of ITT's Digit 2000 receiver is shown in the block diagram below. Three digital processing blocks for video signals, picture processing and audio signals are arranged between A/D conversion of the input signal and D/A conversion of the output signal. They are grouped around the ITT (Intermetall) communication bus (IM Bus), over which the entire video and audio data traffic takes place. In parallel, synchronization and deflection signal processing take place directly between the A/D and D/A converters.

The processing block contains a large number of expansion stages for every conceivable type of television receiver, from the low-cost standard unit to the full-feature, multi-standard satellite receiver incorporating a host of special functions.

Signals that are to be processed digitally arrive via the high-frequency section of the receiver. According to whether the input signals are analogue or already digital, they are fed to the signal processing sections in Digit 2000 via analogue-to-digital converters or digital-to-digital converters.

Video processing

In addition to the established PAL, SECAM and NTSC standards, the new D2-MAC and Nicam standard signals are now also processed in the video signal processing section. With the new



ITT's Digit 2000 digital television receiver scheme.

standards, the digital audio signal is contained in the baseband. It is separated and conditioned for further processing in the audio signal section.

Chrominance and luminance components of the video signal, transmitted in time-division multiplex mode in any of the MAC standards (C-MAC, D-MAC and D2-MAC), are expanded and converted to the standard format of the ITT communication bus. This is achieved by the new DMA2280/2285 multi-standard MAC decoder chip set developed by ITT to fit all current European MAC standards. The DMA2280 decodes the signal and the DMA2285 is the descrambler IC. The set is automatically switched to the correct standard by its software. Hence the Digit 2000 television set can receive satellite transmissions in any European country.

Digital processing also permits digitally generated text and graphics to be represented on the television screen. The TPU2734, the latest text processing IC in the Digit 2000 system, automatically selects the appropriate character set, from the eight different national sets it is able to recognize.

The full Fastext teletext capability is now possible with just the TPU2734 and a single 16K or 64K standard dynamic ram. The display control unit selects one of eight stored pages for display. Eight-bit character words are transformed into a 6×10 dot matrix with PAL, or 6×8 with NTSC, by a rom character generator of 96 characters.

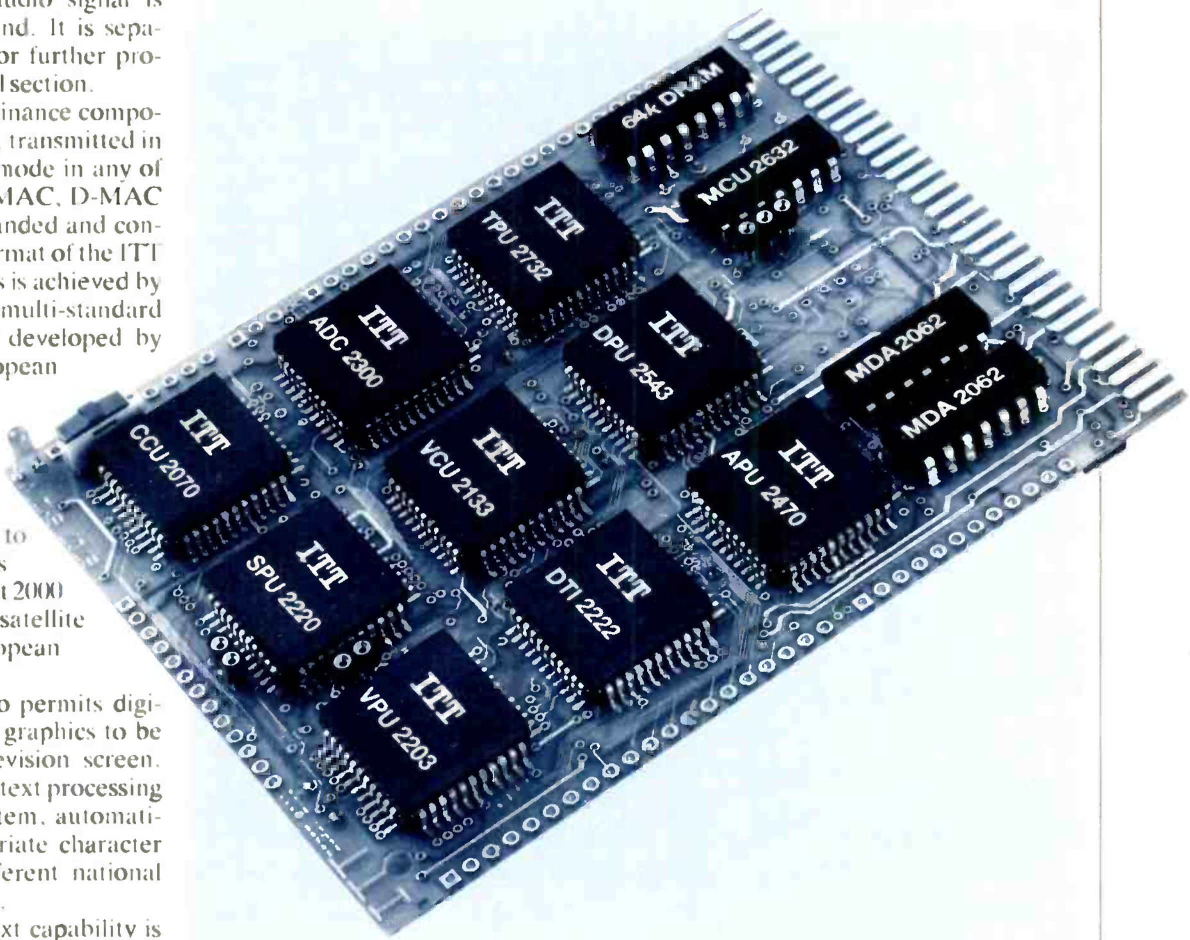
Through the use of the picture memory described later on, the capacity of the teletext page memory can be increased to more than one hundred pages.

ITT's next generation of teletext ICs implements the additional features of Level 1.5 Teletext, including vertical text scrolling, user-definable characters, and hardware magazine and page selection. To enhance the display, a higher resolution character matrix (10×12) and an optional 100Hz flicker-free display mode are provided.

The text processing section can also be used to display information concerning the receiver settings on the screen, to simplify the operation of the set.

The video signal processing section also includes picture-in-picture processing. The PIP2250 processor allows a smaller, moving colour picture to be superimposed on the normal television picture. This smaller picture can reproduce a programme being broadcast on another channel so that the viewer can see what is being broadcast there without having to switch over. The processor works by converting the Y, R−Y and B−Y signals into a form which can be stored in a standard d-ram and presented at the appropriate time. The additional RGB inputs of the video control unit are used to create a border around the small picture, the colour of which can be selected.

The signal for the small picture may also be derived from an external source, for example from a computer, video recorder, or from a camera monitoring another room. Additional RGB inputs for such external signals are incorporated into the IC.



This prototype board, measuring 8×10cm, accommodates the complete system for all standards; it includes text processing and other functions.

Audio processing

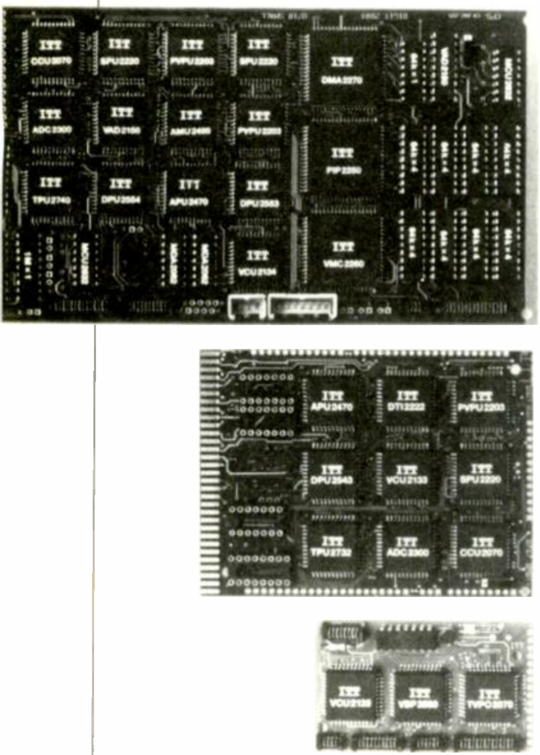
With the new television standards (D2-MAC, Nicam etc.), satellite radio, new audio storage media (CD, DAT), and of course computers, the sound is already digital to start with. For this reason, digital audio signal processing is essential nowadays even on otherwise analogue receivers.

Audio signal processing in the Digit 2000 system is designed for four channels as standard – two for the loudspeaker and two for the headphones. Amplification, tone control and balance adjustment are carried out and controlled digitally. Mono, stereo and bilingual broadcasts are identified automatically through the software. Thanks to the high resolution that is used in A/D and D/A conversion, the stereo sound quality is on a par with that of compact disc. There is also provision for artificially broadening the stereo image width to achieve full spatial sound without the need for additional loudspeakers. With mono broadcasts, the viewer can switch to pseudo-stereo.

In top-of-the-range television sets, several audio processing sections may be used, for instance for processing multi-language stereo broadcasts simultaneously or even for emulating a graphic equalizer.

Picture display techniques

The Digit 2000 system contains a special picture processing section which does



From top to bottom: digital HDTV, complex digital tv, standard digital tv.

not exist in analogue receivers.

With all television standards that use a composite video signal, such as PAL, NTSC and SECAM, the bandwidth of the chrominance signal is narrower than that of the luminance signal. This results in a visible degree of blurring at the colour transitions. To minimize this, the chrominance signal is adaptively measured, conditioned and matched to the luminance signal by the video memory controller IC, VMC2260.

In NTSC receivers, with their smaller number of picture lines, Digit 2000 improves the picture quality dramatically by displaying each line twice in succession at half the normal line spacing. By doubling the number of lines in this way, the otherwise conspicuous line structure of the picture becomes virtually invisible.

With the conventional television standards today, especially those with 50Hz field frequency, large surfaces represented on screen give rise to troublesome flicker. This can only be avoided by increasing the picture scan frequency. For this purpose, the Digit 2000 system has provision for buffering a field and then writing it on to the screen at twice the frequency, twice in succession.

The video memory controller also enables further picture improvements to be realised through, for example, distortion correction, noise suppression, and the prevention of edge flicker. Furthermore it can be used to advantage for implementing special features. For example the number of teletext pages that can be stored can be increased enormously. A detail of the centre of the picture can be enlarged by a factor of two (zoom facility) and, in conjunction with the picture-in-picture processing section, up to nine freeze frames from different programmes can be displayed simultaneously.

• Further information: contact ITT Semiconductors, Rosemount House, Rosemount Avenue, West Byfleet, Surrey KT14 6NP (0932-336116).

Hans G. Keller is with ITT Semiconductors at Freiburg in the Federal Republic of Germany.

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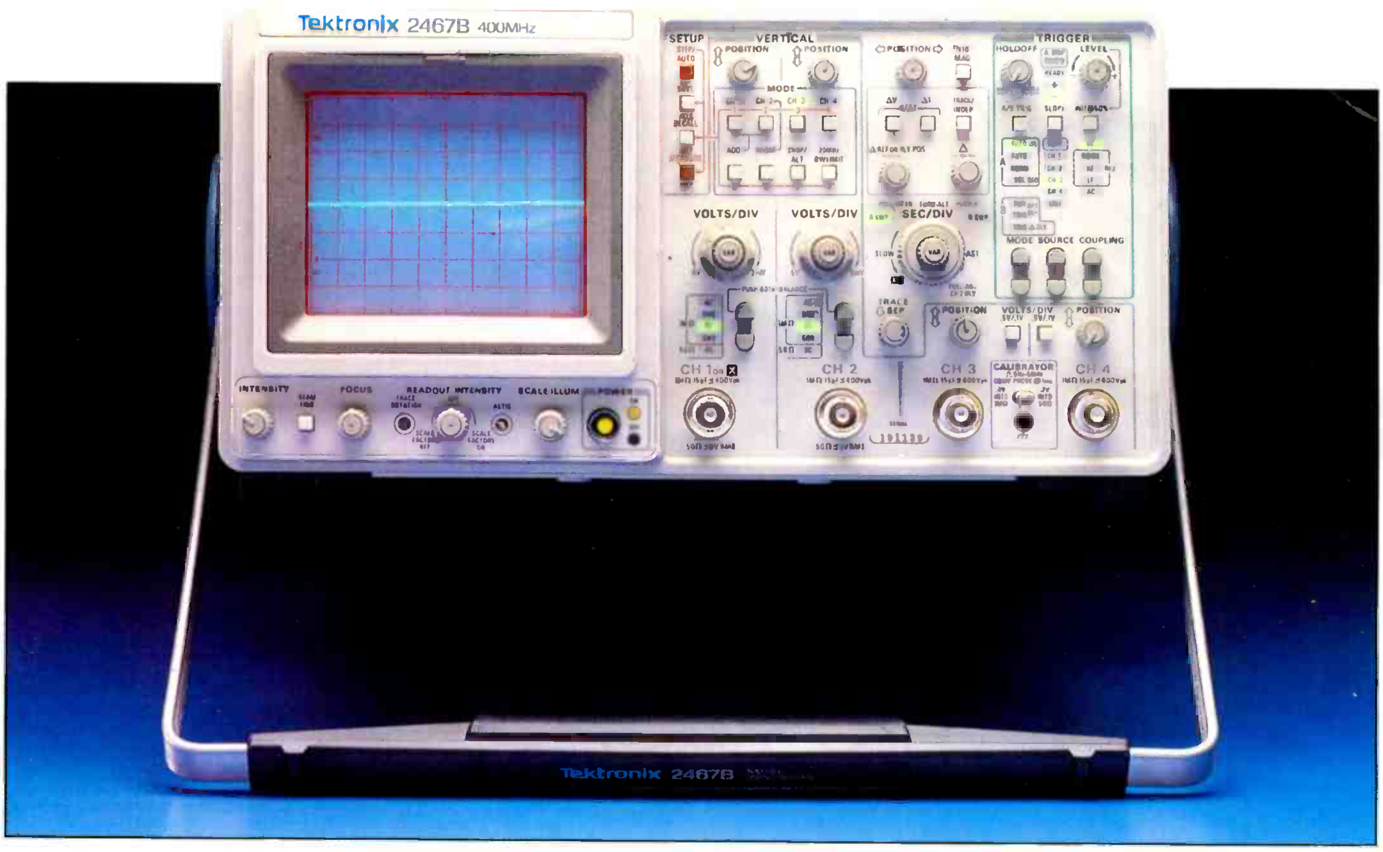

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