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	IRFP450A	TO-247	500V	400mΩ	14A	Same
	IRF840A/S	TO-220/D <sup>2</sup> -Pak	500V	850mΩ	8A	Same
	IRF830A/S	TO-220/D <sup>2</sup> -Pak	500V	1400mΩ	4.5A	Same
	IRFPC50A	T0-247	600V	600mΩ	11.A	Same
	IRFBC40A/S	TO-220/D2-Pak	600V	1200mΩ	6.2A	Same
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Proteus differs from circuit simulation packages reviewed so far in that it has no virtual instruments. But might its alternative analysis tools suit you better? Turn to page 831 to find out.



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New sensor detects a moving human body using four 1.35 by 1mm sensing elements – one of dozens of new products featured on pages 841-846.

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#### EDITOR

Martin Eccles 0181 652 3614

#### CONSULTANTS

Ian Hickman Philip Darrington Frank Ogden

EDITORIAL ADMINISTRATION

Jackie Lowe 0181-652 3614

EDITORIAL E-MAILS jackie.lowe@rbi.co.uk

ADVERTISEMENT MANAGER Richard Napier 0181-652 3620

DISPLAY SALES EXECUTIVE Joannah Cox 0181-652 3620

ADVERTISEMENT E-MAILS joannah.cox@rbi.co.uk

ADVERTISING PRODUCTION 0181-652 3620

PUBLISHER Mick Elliott

EDITORIAL FAX 0181-652 8111

CLASSIFIED FAX 0181-652 8938

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# Aromatherapy and audiophools

n most fields of electronics charging £120 for a short piece of wire with a plug at either end would not win you many customers. The audiophile, or rather audiophool, business is different; it turns the rules of business – and of science – apparently on their head.

Let me explain, for those of you unfamiliar with this fascinating market.

Successful retailing, they say, is the painless extraction of money from the pockets of satisfied customers. This is normally achieved by providing them with goods at competitive prices that meet their genuine needs.

Supplying audiophools is different; it's akin to selling aromatherapy essences, or those copper bracelets that combat rheumatism.

It's a profitable business too, with apparently rational adults – all men by the way; womankind is honourably exonerated – spending serious amounts of money on something they cannot see, cannot feel and cannot justify the cost of.

No scientific backup is offered for the claims made for the betterment of music. If these traders were selling patent medicines, they'd be outlawed within weeks, but in audiophool circles the Trades Descriptions Act appears not to apply.

Looking through current British hi-fi magazines I see vendors offering:

- mains plugs with rhodiumplated pins for better audio listening;
- 'sublime' glass platter mats for sheer three-dimensional detail resolution;
- overlay mats for realising better sound from CDs;
- interconnects (you mustn't called them connecting leads any more, oh no!) made from oxygen-free copper with crystals aligned in the direction of the music;
- other interconnects containing 'a particular inorganic chemical' to

improve sonic qualities;

- replacement capacitors of guaranteed 'musical' sound quality;
- long-grain pure silver wire for building better amplifiers.

The strange thing is that most audiophools are not ignorant peasants; far from it. To be duped in this way implies significant material achievement (put another way, deep pockets) and a maturity of personal development that properly appreciates highend sound and musicality, if not music for its own sake.

Music has to be chosen very carefully of course; most audiophools are aggressively analogue and will not countenance those silver beer mats. A few, however, will embrace CDs – so long as these are the remastered gold substrate variety. In either case, whatever individual preference the audiophool once had for music is now subjugated since he now listens only to reference recordings, for facilitating participation in comparisons with other audiophools.

In all this pursuit of aural excellence, the established techniques developed and proven over the years by audio professionals are studiously ignored. So signal cables made of sensible, affordable copper are rejected in favour of sexier affairs made of pure silver – or else of refined virgin unobtainium.

Sensible, solid XLR connectors with contacts having large surface areas are abandoned for slender phono plugs with expensive gold plating. Proper balanced audio cables with a grounded lapped foil screen are ignored in favour of interference-prone twin-line.

Design logic counts for little in the equipment too. Even though MOVs for eliminating mainsborne transients are very cheap, it would not occur to the manufacturer of a £1500 CD player to build suppression into the device. Instead the solution is sold as an outboard add-on – naturally with an audiophool seal of approval. Its price is a drop in a bucket compared with the price of the other toys so vendors are laughing all the way to the bank.

The effects of mains-related quackery may be positively dangerous too.

There's a story – it may be urban legend – of one audiophool who short-circuited his house fuses in order to reduce the internal resistance of the mains supply, thus improving his equipment's voltage regulation.

His house burned down. Responsibility for perpetrating all this pseudo-science lies with the audiophool journals. An unbealthy collusion between

unhealthy collusion between advertisers and publishers perpetuates this aura of mystique, with few titles prepared to prejudice their revenue stream by exposing the emperor's new clothes.

Sanity still exists in some quarters of course, particularly in the letters department of this very journal. Anything to do with audio that's loopy or even slightly subjective soon gets knocked down to Earth here.

Some refreshing candour is also appearing in some of the Internet discussion groups for high-end audio; one pundit recently suggested that for genuine 'liquid sound' the only solution was to use mercury-filled speaker cables – and then devalued this advice by admitting this was an April Fool's joke.

But perhaps we should live and let live. If aromatherapists or other practitioners of fringe medicine can successfully relieve suffering and make the world a happier place, then why shouldn't audiophools enjoy their expensive pleasures too? It's easy to misjudge people anyway; some audiophools regard 'professionals' as cloth-eared cretins, who are too stupid and/or deaf to appreciate the audio art at the (superior) audiophool level. Keep smiling!

Andrew Emmerson

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# UPDATE

# **Recovery showing for Europe's chip market**

Despite the continuing DRAM debacle, the semiconductor market recovery in Europe is under way, according to a report from analysts Future Horizons of Sevenoaks, called 'The European Semiconductor Market Report 1996-2004.

Describing the DRAM market as a 'Fubar' (Fouled Up Beyond All Reason), Malcolm Penn, chairman of Future Horizons, commented: "It's out and out obsession with who's going to be No 1 in worldwide DRAM production,

whatever the cost."

A price war between Micron of Idaho and the Korean companies has seen prices of 64Mbit DRAMs drop from \$8 to \$4. "At these prices no one is profitable," says the report.

On the upside, business at silicon foundries is growing at twice the industry rate, with product allocations threatened later this year. High-end logic and flash are also rebounding.

The report warns of a capacity shortage later this year and next which may accelerate plans for 12in wafer production. It believes the first users of 12in wafers will be Infineon, Intel, NEC, Samsung, STMicroelectronics and TSMC

European	semiconduct	or market fo	orecast. (\$bn)
Year	1999	2000	2001
Discretes	3.3	3.7	4.1
Opto	0.9	1.2	1.6
IC	28.3	35.1	45.5
Total	32.5	40.0	51.2

# 2000 fix turns off 2000 lights

wo thousand Londoners were left without electricity recently when a Year 2000 upgrade to pre-pay meters went wrong.

London Electricity was trying to make its meters millennium compliant before the date change, but ended up cutting off over 2000 customers.

"Our Powerkey meters don't recognise the date change," said a London Electricity spokesperson. "They would continue to supply electricity, but wouldn't recognise

any price changes."

The electric company came up with a plan to upload new software when customers next recharged their meters.

"About 8000 people tried to do the fix, of which 2000 did not work," said the spokesperson. When the credit on these meters ran out, customers were left without power.

"The majority were put back on within 24 hours," he said "We're not aware of anyone that's been off any longer than 48 hours."

London Electricity's remaining 400 000 Powerkey customers will wait until the problem with the keys is rectified before having their meters upgraded.

The government's Year 2000 watchdog, Action 2000, and Offer, the electricity watchdog, has graded 95 per cent of electricity firms as 'blue' in their traffic light grading system of compliance. This indicates 'no material risk of disruption', although the London Electricity case shows disruption several months before the date change.

# Smaller, lighter microphone responds to air flow, not pressure

Researchers at the University of Twente in the Netherlands have developed a microphone that is smaller and lighter than conventional units.

Rather than measuring sound pressure, the device, called a 'microflown', measures particle velocity, or air flow.

Micromachining is used to create two closely spaced silicon-nitride wires. These are coated with a platinum resistor. Each wire is 1mm long.

Current passed through the platinum elements heats the wires to between 200°C and 400°C. The flow of air due to sound waves causes the wire closer to the sound source to be cooled, with the amount of cooling being linearly dependent on the velocity of the airflow.

Because the wires are close

together, convective heat flow causes the temperature of the other wire to rise. The temperature difference is measured as a voltage output by placing the resistive wires in a Wheatstone bridge.

The sensor acts as a low pass filter. because thermal mass of the wires limit their ability to follow fast changing signals. At low frequencies the response is flat while higher frequencies show a 6dB/octave drop.

Two types of microflown have different responses. The cantilever type (pictured) has a relatively low corner frequency of 400Hz. The bridge type, where both ends of the wires are supported, has a higher corner frequency of 1kHz.

Both types can be used for speech, providing the low pass behaviour is corrected electrically, or through

digital signal processing. A frequency range of 100 to 3.4kHz is possible, the researchers claim.



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October 1999 ELECTRONICS WORLD

# New tapping measures for Internet and mobiles

A re you and 'arf-a-dozen of yer chinas down the East End' planning a bank job? Are you worried about the old Bill listening in on your dog-and-bone?

No problem, my son. Today you can get instant, off-the-shelf, secure communications that will cost you only the price of a drink. Just buy a few pre-pay mobile phones down at Dixons. Set up a free Internet account, preferably with ready-made encryption software. The police will have no idea who owns them, or which company is transmitting your conversations. Throw your equipment away afterwards, and most of the incriminating evidence is gone forever.

This is the problem now facing the police. Because of the boom in new types of telecoms networks and the Internet, they can no longer

With the boom in telecoms networks, phone tapping is getting harder for the police. Now the Home Office plans to bring police phone tapping into the era of mobiles and the Internet. Pete Mitchell reports

reliably eavesdrop on criminal activities through telephone tapping – or so claims the Home Office.

Authority for the police to listen in on suspects' phone conversations comes from the Interception of Communications Act. Passed in 1985, the IOCA merely confirmed the decades-old gentleman's agreement between the former GPO – which operated the public switched network – the exchange suppliers such as GEC and Plessey, and the Home Office. It enables the police to get a warrant to monitor any fixed subscriber line owned by a public telecommunications operator, using purpose-built functions in the BT switch.

But the IOCA's authors had obviously never heard of cellphones, satellites, the Internet, or even cable. They completely ignored the existence of private voice or data networks, which were much rarer and more localised then than they are today, and which now carry a substantial amount of public traffic for much of its journey. An even bigger limitation is that the IOCA warrants only apply to licensed public telecommunications operators, whereas the industry now contains many unlicensed service providers. It, and the crooks, have moved on, and the Home Office now wants to move with them.

So it recently produced a consultation paper outlining its plans for an extended IOCA, and sent it for comments to the telecoms industry – an industry now consisting of cellular network operators, Internet service providers, about 150 fixed-line phone companies (rather than two when IOCA was written), bandwidth-resale companies, and private network owners.

**ISPs, comms and net operators in panic** These firms are now in some panic. Not only will the reborn IOCA require all firms to install new infrastructure – capable of secretly monitoring the entire traffic of any of their customers within a few minutes of receiving a warrant – but it will also demand that the operators themselves pay the entire cost of this privilege. As the consultation paper puts it, "... communication service providers will be required to take reasonable steps to ensure that their system is capable of being intercepted. This will be an ongoing requirement which CSPs will have to consider each time they develop their network or introduce new services".

The costs will run into millions. And some of the functions that the Home Office is demanding cannot be delivered at all using current technology, said Keith Mitchell, chairman of the LINX association of Internet service providers.

"The requirements were constructed by police officers who seem to have assumed that the Internet works just like the voice telephone network, which it doesn't at all," he said. "They want listening devices installed on every Internet backbone router. Personally, I don't see how that could be done, but even if it could, it might be open to abuse and could potentially compromise the overall security of the Internet.

"Some of the services they want could degrade the performance seen by someone who was being monitored, and it's quite possible that they could detect that they were being monitored as a result."

#### **Cost implications**

Such performance penalties would affect the innocent Internet user too, he adds. So, of course, would the cost – estimated at between

20 and 40 per cent of the total infrastructure costs of a typical ISP – that would be passed on to customers. Some ISPs would probably even have to re-design their backbones to match the topology assumptions made in the proposals, he said.

"It's most unfair that they are proposing service providers should pay for this," he said. "Some of the technology isn't available off the shelf yet, so it's not just a question of ISPs going out and buying a box. The equipment manufacturers would have to commit R&D money to develop it."

The cellphone operators are equally alarmed, and much less well prepared. The Federation of Communications Services, the mobile operators' trade association, has not yet agreed on its response. It is still consulting its members and trying to work out the financial impact on their business, said Chris Webb, an FCS spokesman: "What is certain is that it will affect both the service providers and the networks quite dramatically."

It is expected that some of the larger networks – those linked to telecoms companies who have dealt with the Home Office for many years – will have seen this coming and made at least some preparations for it. But the smaller operators have been caught completely on the hop.

#### What will the customers think?

And re-engineering their network management systems is not the only issue: operators are privately worried about how the new legislation will affect their relations with customers, too.

"It will be a tricky balancing act to convince our subscribers we are respecting their confidentiality at the same time as we have to work in the new framework," said one.

To forestall objections, the Home Office is trying to bluff the industry into believing that, "these proposals are consistent with existing legislation and practice in many other countries including France, Germany, the Netherlands, Sweden, the USA, Canada and Australia".

But, "What they mean is that other countries have signed up for this, but not implemented it yet," said Mitchell. He warns that the UK is in severe danger of giving its Internet industry the most stringent monitoring requirements in the world.

"Other countries will then choose not to route their traffic through here for fear that confidentiality safeguards will be breached, and that could be very harmful to our information economy."



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Because of the good hardware specs (two channels, 12 bit, 200 kHz sampling on both channels simultaneously, 32 KWord memory, 0.1 to 80 volt full scale, 0.2% absolute accuracy, software controlled AC/DC switch) and the very complete software (oscilloscope, voltmeter, transient recorder and spectrum analyzer) the HANDYSCOPE 2 is the best PC controlled measuring instrument in its category.

The four integrated virtual instruments give lots of possibilities for performing good measurements and making clear documentation. The software for the HANDYSCOPE 2 is suitable for Windows 3.1 and Windows 95. There is also software available for DOS 3.1 and higher.

A key point of the Windows software is the quick and easy control of the instruments. This is done by using: - the speed button bar. Gives direct access to most settings.

the mouse. Place the cursor on an object and press the right mouse button for the corresponding settings menu.

- menus. All settings can be changed using the menus.

#### Some quick examples:

The voltage axis can be set using a drag and drop principle. Both the gain and the position can be changed in an easy way, The time axis is controlled using a scalable scroll bar. With this scroll bar the measured signal (10 to 32K samples) can be zoomed live in and out.

The pre and post trigger moment is displayed graphically and can be adjusted by means of the mouse. For triggering a graphical WYSIWYG trigger symbol is available. This symbol indicates the trigger mode, slope and level. These can be adjusted with the mouse.

The oscilloscope has an AUTO DISK function with which unexpected disturbances can be captured. When the instrument is set up for the disturbance, the AUTO DISK function can be started. Each time the disturbance occurs, it is measured and the measured data is stored on disk. When pre samples are selected, both samples before and after the moment of disturbance are stored.

The spectrum analyzer is capable to calculate an 8K spectrum and disposes of 6 window functions. Because of this higher harmonics can be measured well (e.g. for power line analysis and audio analysis)

The voltmeter has 6 fully configurable displays. 11 different values can be measured and these values can be displayed in 16 different ways. This results in an easy way of reading the requested values. Besides this, for each display a bar graph is available.

HANDYSCOPE

CH1

When slowly changing events (like temperature or pressure) have to be measured, the transient recorder is the solution. The time between two samples can be set from 0.01 sec to 500 sec, so it is easy to measure events that last up to almost 200 days.

The extensive possibilities of the cursors in the oscilloscope, the transient recorder and the spectrum analyzer can be used to analyze the measured signal. Besides the standard measurements, also True RMS, Peak-Peak, Mean, Max and Min values of the measured signal are available.

To document the measured signal three features is provided for. For common documentation three lines of text are available. These lines are printed on every print out. They can be used e.g. for the company name and address. For measurement specific documentation 240 characters text can be added to the measurement. Also "text balloons" are available, which can be placed within the measurement. These balloons can be configured to your own demands.

For printing both black and white printers and color printers are supported. Exporting data can be done in ASCII (SCV) so the data can be read in a

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spreadsheet program, All instrument settings are stored in a SET file. By reading a SET file, the instument is configured completely and measuring can start at once. Each data file is accompanied by a settings file. The data file contains the measured values (ASCII or binary) and the settings file contains the settings of the instrument. The settings file is in ASCII and can be read easily by other programs.

Other TiePie measuring instruments are: HS508 (50MHz-8bit), TP112 (1MHz-12bit), TP208 (20MHz-8bit) and TP508 (50MHz-8bit)

Convince yourself and download the demo software from our web page: http://www.tiepie.nl.

When you have questions and / or remarks, contact us via e-mail: support@tiepie.nl

#### Total Package:

The HANDYSCOPE 2 is delivered with two 1:1/1:10 switchable oscilloscope probe's, a user manual, Windows and DOS software. The price of the HANDYSCOPE 2 is £ 299.00 excl. VAT.

TiePie enginering (UK), 28 Stephenson Road, Insdustrial Estate, St. Ives, Cambridgeshire, PE17 4WJ, UK Tel: 01480-460028; Fax: 01480-460340

TiePie engineering (NL) Koperslagersstraat 37 8601 WL SNEEK The Netherlands Tel: +31 515 415 416 Fax+31515418819

# Gigabit speed comms through air via a light beam

Lucent Technologies' Bell Labs has put dense wave division multiplexing, or DWDM, technology into use for transmitting data through the air using beams of light.

The optical system called WaveStar OpticAir is claimed to be the first to use DWDM directly through the air and can cope with voice, data or video traffic. The system builds on Lucent's existing fibre optic system using a lot of the same technology.

A high power optical amplifier is used to boost the signal up to 1W before it is transmitted down a singlemode fibre optic cable to a telescope.

The signal is coupled to four 3cm transmitting apertures in the telescope which are configured in a square pattern around a 20cm receiving aperture. The light from the apertures diverges as it is transmitted so at a distance of 2km the diameter of the beam will be approximately a metre.

In the multichannel system each signal is sent on a different frequency boosted by its own amplifier. At the telescope the signals are mixed and each aperture sends all the signals.

The four transmitting apertures are all focused on the receiving aperture at the other end. When the signal is received it is sent down a multimode fibre into an avalanche photo diode. A DWDM multi-mode demultiplexer splits out the signals.

The system is still being worked on in the lab and Jim Auborn, Bell Labs' head of communications technology department, is very enthusiastic about its performance. "In principle you can do just about what you can do with fibre systems," explains Auborn.

The first version is expected in March 2000 and will support one wavelength at speeds up to 2.5Gbit/s. This will be followed in the summer by a four wavelength system with a maximum capacity of 10Gbit/s for distances up to 5km.

Auborn says that the transmission distance can be greater depending on the atmospherics. "We can really transmit as far as you can see," he comments. "If the weather gets bad you can increase the power or transmit data at a lower rate."

#### E-commerce could spark UK industry boom

B ritish electronics manufacturers have a major opportunity to prosper through the use of the Internet. That is the message of Dr David Cleevely, a member of the government's steering group on e-commerce.

"The UK is very good at inventing and has a strong understanding of how things are made," said

#### Engineers patently spy on rivals

Engineers are using patent information to keep a close eye on their competitors, according to a survey commissioned by Derwent Information. The Europewide survey showed that 55 per cent of respondents use patent information for 'competitive intelligence'. Cleevely. Where it is less effective is in volume production.

What e-commerce offers, claimed Cleevely, is a way of bridging the gap between idea generation and innovation, and final distribution. "You don't need to manufacture here," said Cleevely, who is also managing director of telecoms consultancy Analysys. "What is important is to understand how things are made."

"I agree with him 100 per cent," said Cliff Hardcastle, chairman of display manufacturer Densitron. "I also think it [this approach] is the only way forward."

His belief is that the UK is unique in its ability to respond quickly to development opportunities. "It is good at design and it is good at organising it."

Hardcastle plans to exploit these strengths by setting up a propagation company that will use the Internet to offer customers access a raft of key companies not just for manufacturing but design too. "It will take advantage of opportunities wherever they occur," he said.

Meanwhile, Cleevely argues is that if UK manufacturers successfully exploit e-commerce, "we could start to see year-on-year growth way above anything we've seen since the Second World War."

# Chips form part of pet passport plan

The government is to introduce a microchip-based pet passport scheme. A pilot scheme for Western Europe will start next April with a wider scheme planned for 2001. Under the scheme, the animals travelling from Britain or entering the country from abroad will have to be vaccinated against rabies and have an identifying microchip inserted under their skin. The process will cost £150 with a further £30 a year for annual booster injections, compared to £2000 for six months in quarantine.

They're no test dummies... Test dummies certainly did not design the airbag deployment test system that Rugged Systems is offering to vehicle manufacturers. The system designed by **ARIES in Spain allows** manufacturers to determine the threshold trigger speeds and decelerations of airbags.



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"Five stars for its mechanical design" WRTH 1999 Review



Model Name/Number	WR-1000	WR-1500	WR-3100
Construction of internals	WR-1000i/WR-1500i-3100iD	SP- Internal full length ISA ca	ards
Construction of externals	WR-1000e/WR-1500e - 310	0e - external RS232/PCMCIA	(optional)
Frequency range	0.5-1300 MHz	0.15-1500 MHz	0.15-1500 MHz
Modes	AM,SSB/CW,FM-N,FM-W	AM,LSB,USB,CW,FM-N,FM-W	AM,LSB,USB,CW,FM-N,FM-W
Tuning step size	100 Hz (5 Hz BFO)	100 Hz (1 Hz for SSB and CW)	100 Hz (1 Hz for SSB and CW)
IF bandwidths	6 kHz (AM/SSB),	2.5 kHz(SSB/CW), 9 kHz (AM)	2.5 kHz(SSB/CW), 9 kHz (AM)
	17 kHz (FM-N), 230 kHz (W)	17 kHz (FM-N), 230 kHz (W)	17 kHz (FM-N), 230 kHz (W)
Receiver type	PLL-based triple-conv. super	rhet	
Scanning speed	10 ch/sec (AM), 50 ch/sec (FM	1)	
Audio output on card	200mW	200mW	200mW
Max on one motherboard	8 cards	8 cards	3-8 cards (pse ask)
Dynamic range	65 dB	65 dB	85dB
IF shift (passband tuning)	no	±2 kHz	±2 kHz
DSP in hardware	no - use optional DS softwar	e	YES (ISA card ONLY)
IRQ required	no	no	yes (for ISA card)
Spectrum Scope	yes	yes	yes
Visitune	yes	yes	yes
Published software API	yes	yes	yes (also DSP)
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CIRCLE NO. 105 ON REPLY CARD

Michael Slifkin, Ziv Mayan and Zachy Globinsky

# A DSP VHF FM push-button receiver

igital techniques are very much the in-thing in electronics, but most radio receivers still use analogue circuitry. Some fully-digital radios are available – as for example advertised on page 801 of this issue – but they are expensive.

The techniques used in digital receivers of this kind are very different from those used in their analogue counterparts. It would be a daunting task even for a very experienced radio ham to design such a receiver. Nevertheless, one who built his first 1-v-1 radio some forty-five years ago has attempted it – with the aid of younger hands.

In this article we discuss digital signal processing, or DSP, techniques in radio and then describe a working push-button VHF FM radio that we have developed and built. A good introduction to DSP techniques can be found at http://www.bores.com/courses/intro/. Note that this is not a cheap design. While prices of DSP ICs are going down all the time, they are currently still expensive.

#### **Design outline**

Controlling the receiver are an EPROM and a programmed microprocessor. If you intend implementing this design, you will need access to an EPROM programmer. Putting the design together is easy since most of the components are ICs.

The circuit diagrams are presented in two sections, the analogue section and the digital section. Using eight voltage regulators may seem rather excessive, but this reflects the rather specialised needs of the various ICs. Note the separation of digital and analogue earths.

Programming can be arduous, but *Electronics World* is supplying the necessary assembly language programs on disk for anyone wanting them.

# So what's wrong with analogue receivers?

The big question is why would one want to abandon techniques of radio reception which have served us well for over 60 years? Currently the answer would be not to do so because of the high cost. But clearly in the not too distant future, the costs will plummet.

A major advantage of a digital receiver is that changing its programming can alter the entire reception mode, tuning range or channel width. The tuning frequency, bandwidth, mode etc., can all be entered through a key pad, making for very simple use. In addition, a digital receiver's characteristics remain constant throughout its lifetime, resulting in much lower maintenance costs and greater reliability.

By contrast, analogue communication receivers can be difficult to tune. Furthermore, their performance and features cannot be readily changed. In addition, their characteristics can drift, requiring periodic retuning for maximum performance.

In a digital receiver, the use of wide band receivers allows much of the hardware to be shared over all the channels. Thus a completely generalpurpose receiver can be built and then programmed to suit the user. It can be changed as conditions and requirements change simply by reprogramming.

Mass production of such radios could

VHF tuner – outline specifications

Frequency range Audio frequency Channel width Tuning resolution Dynamic range 88-108MHz to 15kHz 200kHz 0.1MHz 40d<u>B\*</u>\_\_\_\_

Audio AGC is provided. The default channel at switch on is 101MHz \*See panel entitled 'Dynamic range'

#### **RF DESIGN**



bring the cost to less than that of the analogue communications receiver. In addition to being cheaper, digital radios should offer more versatility and features. An excellent summary of the advantages of digital radio receivers over analogue receivers has been given by B. Brannon.<sup>1</sup>

#### No superheterodyne

The techniques used for DSP in radio reception are quite different from the usual superheterodyne methods used in analogue radio receivers. A DSP receiver works as follows. The signal is digitised after being received on the aerial and will contain all signals in the frequency range. This digitised signal is then down converted to zero frequency -i.e. base band.

The precess so far selects a particular signal at some frequency, which is now at zero frequency but still in the form of the original transmitted signal. A digital signal processor now applies a mathematical algorithm to transform the signal into audio, but still in a digitised form. This digital audio signal is converted to audio sound by a digitalto-analogue converter.

#### **Receiver outline**

First we'll describe the general arrangement of the receiver, then the

specific stages in more detail.

The radio signal enters the system via the aerial and is amplified by an RF amplifier with a band-pass filter. This amplifier includes an automatic gain control, or AGC, so that the output is about a volt, this being the optimal voltage for the following stage.

Normally of course with a superheterodyne arrangement, AGC is derived from the audio or IF stages, not the RF stage.

This 1V signal now enters a 10-bit analogue-to-digital converter. This converter samples the analogue signal but at a frequency less than the Nyquist frequency – a technique discussed in Fig. 1. Schematic Diagram of the DSP VHF FM Receiver



Fig. 2. Schematic of the HSP50016 digital down converter comprising a complex sine generator producing two mixing signals, 90° out of phase. It is fully programmable, but rather complicated.



**ELECTRONICS WORLD October 1999** 

**RF DESIGN** 



LCD







#### Software availability

If you want the object code in electronic form, e-mail jackie.lowe@rbi.co.uk and it will be forwarded to you as text embedded in an e-mail. It will not be sent as an attachment to avoid distributing viruses. If you want the object code on disk, again free of charge, send us a PC formatted 3.5 in floppy with a protective self-addressed envelope and enough stamps to allow us to return the disk to you. Post it to the Quadrant House address below

For those of you wanting to exploit the design further, the source code is available on disk, or as an e-mail attachment, for £25 fully inclusive. E-mail the above address with your credit card number, expiry date and card-holder address or fax 0181 652 8555 with the details. Alternatively, send your order to Receiver software, Electronics World Editorial, Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS.







Voltage supply







#### **RF DESIGN**





Fig. 3. Schematic of signals as they pass through the VHF receiver.





#### What is under sampling?

Most of you will be familiar with the Nyquist criterion, which states that if one samples a signal at less than twice the highest frequency found in that signal then the restored signal will be distorted – a phenomenon known as *aliasing*.

A well-known version of this is seen at the cinema when the stagecoach rolls into town and the wheels appear to be moving backwards. This occurs because each film piece is shown at 24 times a second. When the spokes are rotating at more than 12 times a second, the wheel appears to be moving backwards.

The stroboscope works on the same principle by flashing a powerful light at a frequency just slightly lower or higher than that of some repetitive motion. This makes the motion appear to move very slowly backwards or forwards or be stationary.

However, where you have a band-pass limited signal – in our case we are looking at signals in a 20MHz range from 88 to 108MHz – then it can be shown that you only need to sample at very slightly more than twice this bandwidth. This means that you sample at 40MHz, rather than 217MHz, without distorting the reconstructed signal. This technique is known as under sampling.

> the box entitled 'What is under-sampling'.

Containing digitised components lying within a 20MHz bandwidth, the sampled signal is down converted using a special digital IC called a digital down converter, or DDC. This device converts the signal in the frequencies between 88 and 108MHz down to DC.



Note that this is not a simple down conversion as used for instance in the synchrodyne receiver as described recently in *Electronics World*.<sup>2</sup> Instead, in this IC there is a complex process in which the incoming digital signal is mixed with a local oscillator which has both sine and cosine components.

After some processing, the mixed signal becomes an output which is a digitised FM signal at DC. This is then passed through a low-pass filter to minimise the bandwidth.

Now, the FM signal has to be demodulated using a digital signal processor to reform the original signal in a digitised form. This signal is then passed through a 16-bit digital-to-analogue converter to produce an analogue audio signal, which is passed through a low-pass filter to the speaker.

Control of the receiver is by an on/off switch and a simple six-key touch pad. There are up and down buttons for volume. In addition, a frequency up/down button moves up one FM channel or down one FM channel. There is also a button that searches up, and one that searches down. When a signal is encountered the search then stops.

The whole process is controlled by a microcontroller, which also functions as a user-interface. This microcon-

troller is responsible for getting the desired radio frequency by sending the mixing frequency to the DDC and outputting the frequency to an LCD display. It also searches for active channels and enables volume control.

-3644Hz

364kHz Frequency

The controller sends the volume control data to the signal processor, which is responsible for the output amplitude. Other than that, a program stored in the EPROM controls the signal processor.

#### **Elements of the receiver**

Figure 1 shows the various stages of this receiver in a pictorial form. The first stage is the antenna, a conventional ribbon dipole VHF aerial, which often comes with a music centre but can be bought from any radio shop.

The following RF stage is conventional. It consists of three *MAR3* monolithic broad-band amplifiers and four band-pass filters to give good selectivity.

Each filter has 3dB points at 80 and 145MHz. While consistency might demand that we use only digital filters, this option provides us with the simplest and cheapest solution to get the correct selectivity and gain.

Automatic gain control is derived from the output of this stage via the Schottky diode, the *OP27* operational amplifier and the *2N2219A* transistor. The derived voltage is fed back to the first *MAR3* in the chain to maintain the output at around 1V peak to peak. The RF chokes are used as high pass filters to remove higher frequencies and maintain stability in the amplifier chain.

The RF signal is next fed to the a-tod converter for digitisation. The converter is a Harris *H15766* with a 250MHz full-power input bandwidth and a maximum 60MS/s sampling rate. The sampling frequency of 55.296MHz is obtained as the third harmonic (second overtone) signal from an 18.432MHz crystal.

Next, the digitised signal is fed to the DDC. This is a Harris *HSP50016*, made to be compatible with the a-to-d converter, having a maximum 75MS/s input data rate.

The DDC is fully programmable and is rather complicated. It consists of a complex sine generator to produce two mixing signals, 90° out of phase.

When two signals are mixed together in a non-linear device, i.e. mixer, the sum and difference of the two frequencies are obtained. Thus, one of the results of mixing two signals of the same frequency is an output riding on DC plus a signal at double the original frequency.

Frequency-modulated signals are rather complex. One cannot simply down convert by mixing with a frequency the same as the carrier, as with AM or SSB signals. Instead in-phase (I) and quadrature (Q) signals have to be produced and recombined to reform the FM, as is done in this device. The block diagram taken from the manufacturers data sheet is shown in Fig. 2.

To prevent the doubled frequency produced in the mixing process breaking through, a low-pass filter has to be added. This is accomplished with a decimation filter followed by a fixed finite-impulse-response filter.

The decimation filter is not quite as lethal as it sounds. It passes every Nth pulse, not every tenth pulse, as its name implies. Its effect is to divide the clock frequency by N and to reduce the bandwidth by this ratio.

Output from the DDC is a digitised FM signal at DC. The signal processor performs the mathematical operation on this signal to convert it to a digitised audio signal. The signal processor is an *ADSP-2181* from Analog Devices. It is a microprocessor optimised to carry out all kinds of arithmetical functions.

This signal processor is the heart of this receiver and it is only with the introduction of such devices that a digital receiver becomes possible. These devices are of course fully programmable. The software can be altered to operate on any kind of signal

Object code for the microcontroller.	
:060000002002B0200CEFD :01000B0032C2 :0100130032BA :01001B0032B2 :0100230032AA :10002B00C29775401FD540FDD29775A805758805F9	
:10002B00C29775401FD540FDD29775A8037588037 :10003B007581607520041202EA12007812025612C2 :10004B0001D712022BD2AF80FED291D292C291C2B3 :10005B00927830754005E60875410833D29192903D :10006B00C291D541F6D540EED291C29122C2927582 :10007B00507B7551E77552EC7558AC755988755AAC	
:10008B00A2755B177544009000B075420675430569 :10009B007830E54493F6080544D543F61154D54220 :1000AB00EC753A4722380000000150000000007048 :1000BB0000000000900000069B002DA0B01D01DB7 :1000CB00524003C0D0C0E07545FF309518309622E2	
:1000DB0030934F30943C30B40630B50602013D02EC :1000EB0001A202016C7407B5200302013D05200239 :1000FB000106E520603C1520020106D2A3A2029264 :10010B00A2A20192A1A20092B6D2A0C2A0D2A0023A :10011B00013D74C9B53A06753A0102013A053A0236 :10012B00013A7401B53A06753AC902013A153A1209	
:10013B0002561201D712022B8545407541FF7542BD :10014B0001D542FDD541F7D540F175454030959528 :10015B0030969F3093CC3094B9758805D0E0D0D0D1 :10016B0032C2A3C2A7D2A0C2A0D2A0000000C2A6D6 :10017B00D2A630A5FD20A41B74CAB53A0B753A0064	
:10018B00D2A7C2A6D2A680D9053A120256C2A6D2CF :10019B00A680DF153A8098C2A3C2A7D2A0C2A0D274 :1001AB00A000000C2A6D2A630A5FD20A41AE53AF5 :1001BB00700B753ACAD2A7C2A6D2A680DA153A122C :1001CB000256C2A6D2A680E0053A213AC374C9955D	
:1001DB003A75F00A8485F03B245875F00A8485F053 :1001EB003C75F00A8485F03DF53E12032DD2B1E546 :1001FB003E6005243002020574201202FCE53D240A :10020B00301202FCE53C24301202FC742E1202FC6C :10021B00E53B24301202FCC2B190034512031322BA :10022B00120332900351120313D2B1AB200B743D66	
:10023B0012035290035112031352B1RB2600745003 :10023B001202FCDBF97408C39520FB74201202FC3C :10024B00DBF9C2B190035612031322E53AC3F553FF :10025B008550F0A4F54685F047E5538551F0A4F59C :10026B004885F049E5538552F0A4F54A85F04BC318 :10027B00854657E5472548F556E549354AF555E492	
:10028B00354BF554C3E5572558F557E5563559F514 :10029B0056E555355AF555E554355BF554D291D2A3 :1002AB0092C291C292743075410433D2919290C232 :1002BB0091D541F67854754004E60875410833D260 :1002CB00919290C291D541F6D540EE7410754104D0	
:1002DB0033D2919290C291D541F6D291C29122C262 :1002EB00B174381202FC740E1202FC74011202FC7F :1002FB0022F580D2B012033CC2B012033C22D2B121 :10030B0051FCC2B112033C22D2B1E4FB93B4000303	
:10031B00C2B122C083C08251FCD082D083EB048057 :10032B00EA22748051FC2274C051FC22740151FCEE :10033B00227F017E10DEFEDFFA224D487A20464DE9 :0F034B00202020202000564F4C20002020200092 :00000001FF	
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Vol. 104. No 1751.

Demodulation Using

a Digital Radio and

**Digital Signal** 

Florida 1995.

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Nov. 1998. 3. Shima, JM, 'FM for which a mathematical method for detection is available.

Finally, we have an audio signal, but in digitised form. The last stage is to convert the signal back to analogue form using a d-to-a converter. For this task, we chose the *PCVM56P* from Burr Brown.

Analogue output from the d-to-a converter is finally passed through a lowpass filter and an *OC27* op-amp to the speaker. Controlling the output from the signal processor controls the volume. We included a liquid crystal display, which shows both the frequency and volume magnitude.

All of these operations are supervised by the microcontroller. This is an 8C751 eight-bit controller. This device has anboard EPROM, into which the control program is loaded.

The control program for the signal processor is stored in a *TMS27PC512* EPROM. Both programs were written in assembly language on a PC. When they had been thoroughly checked and debugged, they were downloaded to their respective EPROMs.

Writing the programs is the most difficult part of this design. There are over 400 lines of source code. It is not possible in this article either to discuss it or present it. However, copies of the two programs are available from *Electronics World*. The algorithm controlling the signal processor has already been published.<sup>3</sup> Diagrammatic depictions of the signals as they pass through the receiver are shown in Fig. 3.

#### Further work

The receiver performs very well and has been the subject of much favourable comment.

The present limitation to a general purpose DSP receiver extending to the highest frequencies is the full-power bandwidth of the sample-and-hold circuit located at the front end of the analogue-to-digital converter, together with its aperture jitter. At the time of writing, it is at yet not possible to build a DSP receiver for the very popular 900MHz band.

#### Object code for the DSP chip's eprom in S format.

S22500000040060093FE2040020093FE1040000093FE3040087093FE403C008C000003C0083EF S2250002310B000F0A001F0A001F0A001F0A001F0A001F0A001F0A001F0A001F0A001F0A001F53 s2250002520A001F0A001F0A001F0A001F0A001F0A001F0A001F0A001F0A001F0A001F0A001F0A001FC3 S2250002730A001F0A001F0A001F0A001F0A001F0A001F3C017443E1F093FF6043E1F093FF20F2 S22500029447B30093FE603805A0381241380005380019381232380006380012381223380007B3 S2250002B538001B34001034000434001850000A23380F6800A034000234000634001A403240CC S2250002D668000A34002134000534001940324023380F6800A541C1F093FFF040000240000393 S2250002F74FFFF83C220302010F18058F0D03B80D03CA3FFF060E7B0F0E7C0F0D03A622621F0C S2250003180D009A0E430F0D006F0E440F0D007F0D0C860D0CA728889821810F2E7C5C180A24AB S22500033920800F51096A527CB518089356EC45526CCA0612000712000712000712000712006A s22500037B0D002421800F0E340F0D0CBE0D03280D033A0A001FCB2C5A566CCF06120007120095 \$22500039C07120007120007120007120007120007120007120007120007120007120007120007120028 \$2250003BD0712000712000712000D06421800F0E340F0D0CBE0D03280D033A0A001F20800F2C \$2250003FF0712000712000712000712000712000712000712000712000712000712000712000D0024AD \$22500042021000F0E340F0D0CBE0D03280D033A0A001FCA6C5A672CC506120007120007120081 S2250004620712000712000D006421000F0E340F0D0CBE0D03280D033A0A001F3C007483FE5A43 s2250004832382DF1811B1380E0040000A93FE5A0A001F40000440000E40200540200F380E6045 s2250004A40A001F83FE5A238A9F180E6140000A93FE5A83FE5A238A9F180E90238ADF18110193 \$2250004C540000040000120980F26105F380F600A001F0D03280D033A27100F18103021001F04 s2250004E6180FFC21011F180FFC0A001F22611F0D001A20980F0A001F0D000C22EF0F181132F3 s22500050718109422E60F18113522E90F1811321810E422E00F18113540030A93FE5A3805A098 \$2250005283C01740A001F0D00F50D00E40D00510D004040020A93FE5A380E600A001F83FE5A54 s22500054940007423820F2262BF0D008A3C01740A001F096C000C900000000FFFFFFFFFFF65 S9030000FC

Four leading researchers in the field of low-voltage, low-power analogue ICs explain how new topologies are being used to overcome the limitations of working with low supply voltages and small currents, to help you get the best from these new buiding blocks.

# Low voltage design II



he design of CMOS low-voltage op-amps is an important topic in low-voltage, low-power research. A primary aspect of this research is that amplifiers operating under these conditions have inherent limitations placed on their dynamic range and bandwidth.<sup>1</sup>

Dynamic range is limited by supply voltage and resistor noise. To achieve best results, both input and output stages have to be carefully designed.

In this article, input configurations compatible with lowpower, low-voltage operation are presented. These inputs are capable of handling rail-to-rail signal swings. Lowvoltage output stages also capable of handling rail-to-rail signal swings are the topic of a subsequent article. Their fundamental characteristics are: for the input stage; voltage efficiency and rail-to-rail swing: for the output stage; voltage and current efficiency. An output stage operating in class-AB is needed to minimise quiescent current.

Available bandwidth depends on how the frequency compensation is implemented. It needs an optimised constant- $g_m$  input stage. In particular, the multipath nested

#### The authors

Giuseppe Ferri, Università di L'Aquila, L'Aquila, Italy. Pierpaolo De Laurentiis, Università di L'Aquila, L'Aquila, Italy. Arnaldo D'Amico, Università di Tor Vergata, Roma, Italy. Giovanni Stochino, Ericsson Telecomunicazioni SpA, Roma, Italy.

#### **ANALOGUE DESIGN**



Miller compensation configuration combines a high bandwidth with a high gain.

Traditional op-amps are typically single ended, but fully differential topologies can also be useful. In this case, common-mode feedback is needed to control the output common-mode level.<sup>2</sup>

Typical low-voltage op-amps target specifications are set out in Table 1.

## New architectures for low voltage operation

Realising efficient CMOS low-voltage stages implies the design of new analogue circuit architectures. To make best use of the reduced supply voltage, each circuit has to be able to handle signals that swing from rail to rail at its outputs and inputs.

To maximise dynamic range, the signal voltages have to be as large as possible. Since the signal voltages can extend from rail to rail, the input and output stages of analogue systems – especially operational amplifiers – must be able to handle these signals correctly.

In the CMOS low-voltage field, it is possible to make a rough distinction based on the number of stacked gate-source voltages and saturation voltages. The term 'low-voltage' is consequently used for circuits capable of working at a supply voltage of two gate-source voltages and two saturation voltages; on the other hand, circuits that need only one gate-source voltage and a saturation voltage are called 'very low voltage' circuits.

#### Rail-to-rail input stages

The conventional differential pMOS input stage is shown is Fig. 1. It is appropriate where low commonmode input voltages are considered. For high input levels, a complementary input stage with nMOS transistors has to be used.

In applications where both low and high input values of common mode are needed, a rail to rail input stage is needed, Fig. 2. It comprises both a p-channel input pair and an n-channel input pair.

The n-channel pair allows the common-mode input voltages to reach the positive supply rail and the pchannel pair the negative rail. In this manner, the common-mode input range can extend from negative to positive supply rails.

The common-mode input range of Fig. 2 can be analysed considering the following three input signals:

- low common-mode input voltages (only the p-channel pair operates);
- intermediate common-mode input voltages (both the input pair operates);
- high common-mode input voltages (only the nchannel input pair operates).

A drawback of this input stage is the fact that its transconductance,  $g_m$ , changes by a factor of two

Table 1.	
Minimum supply voltage	1.8V
Quiescent current	250mA
DC gain	≥60dB
GBW	≥1MHz
Maximum output current	1mA
Input and output voltage range	Full (rail-to-rail)

within the common-mode input range, as in Fig. 3. Here it is assumed that the  $g_m$  of the p-channel and the  $g_m$  of the n-channel input pairs are equal. This can easily be achieved by selecting the right *W/L* ratio of the input transistors.

varying  $g_m$  doesn't allow optimal frequency compensation. Moreover, it causes undesired additional distortion.

In order to overcome these drawbacks, the transconductance has to be kept constant. The next section describes how to realise such input stages.

Owing to the fact that the bandwidth of an operational amplifier is proportional to the  $g_m$  of its input stage,

Constant-gm rail-to-rail input stages. The total transcon-

#### A new universal input stage for low-voltage op-amps<sup>3</sup>

Several methods for achieving a constant- $g_m$  with complementary, rail-to-rail input stages are given in the literature. All of these are based on an opportune control of the DC tail currents of the differential input stages.

The proposed examples include bipolar and CMOS input pairs operating in weak inversion. To achieve this, the sum of tail currents flowing through both the n and p type input pairs has to be kept constant.

Another set of examples is represented by CMOS input pairs operating in strong inversion. Here, constant transconductance is achieved by keeping the sum of the square roots of the tail currents constant.

None of these types of control can be applied universally at the same time to both bipolar and CMOS input stages operating in weak and/or strong inversion. In this section though, we present a novel and universal concept that is independent of input transistor types and their operating regions.

The new concept is based on the processing of signal currents rather than handling DC tail currents, **Fig. A**. The operating principle is based on the well known equation of the total instantaneous output current of a simple differential pair,

$$I_{0,lor2} = \frac{I_{tail}}{2} \pm g_m \frac{V_{id}}{2}$$
(P1)

Here,  $V_{id}$  is the small signal differential input voltage, and  $g_n$  is the transconductance depending on device type and its biasing.

With the notation and current direction shown in **Fig. B**, considering equation (P1) and assuming that  $V_{in+} > V_{in-}$ , the drain current pairs  $I_{n1}$ ,  $I_{n2}$  and  $I_{p1}$ ,  $I_{p2}$  of the complementary input stage can be expressed as follows,

$$I_{n1} = \frac{I_n}{2} + g_{m,n} \frac{V_{id}}{2}$$
(P2)

$$I_{n2} = \frac{I_n}{2} - g_{m,n} \frac{V_{id}}{2}$$
(P3)

$$I_{p1} = \frac{I_p}{2} + g_{m,p} \frac{V_{id}}{2}$$
(P4)

$$I_{p2} = \frac{I_p}{2} - g_{m,p} \frac{V_{id}}{2}$$
(P5)

With respect to the common-mode input voltage, three operating regions exist. In region 1, when  $V_{\rm CM}$  is close to negative supply rail,

$$I_n < I_p (= I_b), \quad g_{mn} < g_{mp} (= g_{m(max)})$$
 (P6)

In region II, when V<sub>CM</sub> is at middle rail,

$$I_n = I_p = I_b, \quad g_{mn} = g_{mp} = g_{m(max)}$$
 (P7)

And in Region III, when  $V_{CM}$  is close to the positive rail,  $I_n(=I_b) > I_p$ ,  $g_{mn}(=g_{m(max)}) > g_{mp}$  (P8) Considering equations (P2) to (P5), and under the condition developed for each region in equations (P6) to (P8), the main principle is that only  $g_{m(max)}$  is selected and used throughout the entire input common-mode voltage range. The result is a rail-to-rail constant- $g_m$ input stage.



ductance of the input stage,  $g_{mT}$ , is the sum of the transconductance of n and p-channel differential stages, respectively  $g_{mn}$  and  $g_{mp}$ ;

$$g_{mT} = g_{mn} + g_{mp} \tag{1}$$

If the input transistors operate in weak inversion, the total transconductance is given by,

$$g_{mT} = \frac{1}{nkT/q} \left( I_n + I_p \right) \tag{2}$$

where  $I_n$  and  $I_p$  are the biasing currents, respectively of n and p pairs.

If the input stage is biased in strong inversion, the total  $g_{\rm m}$  is given by,

$$g_{mT} = \sqrt{2\beta_n I_n} + \sqrt{2\beta_p I_p}$$
(3)

or, from a voltage point of view,

$$g_{mT} = 2\beta_n (V_{gsn} - V_{Tn}) + 2\beta_p (V_{sgp} - V_{Tp})$$
(4)

From equation (2), it can be concluded that the  $g_{mT}$  of a rail-to-rail input stage operating in weak inversion can be controlled by the tail currents of the input transistors. In strong inversion, according to expressions (3) and (4),  $g_{mT}$ can be regulated by either the input tail currents, or the gate-source voltages or even the transistors aspect ratios.

#### Input stages with current-based gm control

Several methods exist to make the gmT constant by regulating the tail currents of the complementary input pairs. Constant gm input stages operating in weak and strong inversion are now described.

Controlling  $g_m$  by one-time current mirror. In weak inversion, the transconductance of a MOS transistor is



Fig. 6. In this CMOS rail-to-rail input stage g<sub>m</sub> is held constant using a square root circuit.



directly proportional to its drain current. As a result, the  $g_{mT}$  term can be held to a constant value simply making sure that the sum of  $I_n$  and  $I_p$  is kept constant.

In Fig. 4, the sum of tail currents is constricted to obey the following law, consistently with (4),

$$I_n + I_p = I_{ref} \tag{5}$$

If the input stage of Fig. 4 is biased in strong inversion, the dependence of the transconductance on the tail current changes; it follows a square-root law. As a result, the  $g_{mT}$  of the complementary input stage can be proved to vary by about 41% over the common-mode input range. Therefore, for input stage transistors operating in strong inversion, a different method to control  $g_m$  has to be developed.

**Controlling**  $g_m$  via 'three times' current mirrors. From Fig 3, you can see that if  $g_m$  is increased by a factor of two at the lower and the upper part of the common-mode input range, the same  $g_m$  is constant with all input signals.

In order to increase the  $g_m$  when only one input pair is operating, the tail-current of the actual active input pair has to be increased. Since the  $g_m$  of an input pair is proportional to the square root of its tail current, the tail-current of the actual active input pair has to be increased by a factor of four.

This principle can be realised as in Fig. 5, by using 'three-times' current mirrors.

In this manner, the sum of the square roots of the tail currents is held constant. In fact,

$$\sqrt{I_n} + \sqrt{I_p} = 2\sqrt{I_{ref}} \tag{6}$$

This yields in all the three common-mode input ranges, except in the turn over range of the current switch, where the  $g_{\rm m}$  variation is only of about 15.5%.

**Controlling**  $g_m$  control by square-root current control. Controlling  $g_m$  with 'three times' current mirrors only roughly complies with equation (6). To obtain a more precise implementation of this control,  $I_n$  and  $I_p$  have to vary gradually with the input common-mode voltage.

In Fig. 6 is an input stage where the  $g_m$  control is implemented by means of a square-root circuit. The heart of this circuit is the translinear loop comprising transistors MP<sub>4.6.7&8</sub>. Applying Kirchoff's voltage law to the



Fig. 8. Another way to keep  $g_m$  constant in a rail-to-rail input is to use a zener diode.

translinear loop, it can be easily proved that,

$$\sqrt{Id_{MP6}} + \sqrt{Id_{MP4}} = 2\sqrt{Id_{MP7,8}}$$
(7)

where the aforementioned transistors are all matched.

In order to obtain a constant transconductance, the translinear loop is biased so that equation (7) matches expression (6). The diode-connected transistors are biased with a constant current of  $I_{b}$ , fixed at  $I_{ref}/4$ . Moreover, the currents through MP<sub>6</sub> and MP<sub>7</sub> are made equal to the tail current in the n- and p-channel input pairs, respectively. As a result,

$$\sqrt{I_n} + \sqrt{I_p} = 2\sqrt{I_b}$$

**Controlling**  $g_m$  using current switch only. In the circuit of Fig. 7,  $g_m$  control is implemented by four current switches. The current switches compare the common-mode input voltage with their respective gate voltage and subtract current to differential pairs in an opportune manner.

For low common-mode voltages,  $MP_{s1}$  and  $MP_{s2}$ , and consequently the n-channel input pair, are off. In this case,

all of  $L_{ef}$  is flowing through the p-channel pair. For high common-mode voltages,  $MN_{s1}$  and  $MN_{s2}$  and the p-channel input pair are off, so  $L_{ref}$  is flowing through the n-channel pair.

For common-voltages between the  $V_{ss}+V_{bias}$  and  $V_{ss}+V_{bias}+V_{ref}$ , the current switches take away a portion of the current of both tail current sources, controlling the  $g_m$  over the whole common-mode input range.

If the input stage of Fig. 7 is biased in weak inversion, a constant- $g_m$  can be obtained by connecting the gates of both pairs of current switches to the same voltage  $V_{\text{bias}}$ , provided that the input and switch pairs are equal. In Fig. 7 it is sufficient to make  $V_{\text{ref}}$  equal to 0.

This last circuit, with  $V_{ref}=0$ , can be improved for strong inversion operation by sizing the input transistors and the current switches as follows,

$$\frac{\left(\frac{W}{L}\right)_{MNs}}{\left(\frac{W}{L}\right)_{MN1}} = \frac{\left(\frac{W}{L}\right)_{MPs}}{\left(\frac{W}{L}\right)_{MP1}} = 3$$
(8)

This allows you to recover the condition (6).

### Rail-to-rail input stages with voltage-based gm control

In the previous sections, examples of input stage with current-based control have been given.

If the input stage is biased in strong inversion, its  $g_m$  can also be made constant by manipulating the gate-source voltage. In fact the  $g_m$  of a MOS transistor is proportional to its gate-source voltage.

Now, for a constant  $g_m$ , the gate-source voltages of the input devices have to obey the following relationship,

$$\left(V_{sgp} - |V_{Tp}|\right) + \left(V_{gsn} - V_{Tn}\right) = V_{ref}$$
<sup>(9)</sup>

As a result, in each part of the common-mode input range the following  $g_m$  is obtained,

$$g_m = \beta V_{ref} = \sqrt{2\beta I_{ref}} \tag{10}$$

where it is assumed that  $\beta_n = \beta_p = \beta$ .

The voltage reference can be realised with a zener voltage. A very simple implementation of an electronic zener is shown in Fig. 8. In this diagram, the zener diode has been realised by means of two stacked diodes,  $MP_z$  and  $MN_z$ . In order to give a zener voltage according to (9) to the two diodes, the diodes' *W/Ls* are made six times larger than those of the input transistors.

**Rail-to-rail input stages with** *W/L* **based**  $g_m$  **control.** In the previous section, the  $g_m$ -control circuits work properly in either weak or strong inversion. This limits the programming range of these types of input stage.

A control method can be realised that works in weak as well as in strong inversion. The basic principle of this method is to double the  $g_m$  at the outer parts of the common-mode input range by placing an additional input pair in parallel to the actual active input pair, Fig. 9.

Since this principle does not make use of transistor I-V relationships, it operates not only in weak and strong inversion, but also in moderate inversion.

The panel entitled, 'A new universal input stage for low-voltage op-amps,' shows a further solution for implementing constant- $g_m$ -input stages.

The next and final article in this set discusses CMOS output stages. The first article on this topic appeared last month. It introduced low-voltage analogue ICs and discussed bipolar designs in particular. It carried the full list of 19 references.

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Acombination of battery and dynamo – Aisolated from the frame – makes sure you have lights when your bike's stationary. You can use the circuit as a battery-backed dynamo system, or as a dynamo-backed battery system, in which case the batteries would be charged periodically. A J Bird Burntwood Staffordshire D41



Charge the bicycle lighting battery from the dynamo or run from battery alone for easier riding.

#### Line-powered music while you change 'phones

f you have two or more telephone handsets, this scr-based circuit holds the line while you go to another room to pick up the call, the handset having been replaced, and the caller hears music until you pick up the other handset.

The music comes from those little chips found in greetings cards, which need a 1.2V button cell, provided here by the line voltage via a pair of 1N4001 diodes and a 100-150 $\mu$ F smoother. Output of the chip goes to the 'phone line by way of an audio output transformer, the 0.1 $\mu$ F capacitor making the sound a little less shrill.

Pressing the switch and keeping it

pressed applies voltage to the chip, this being held on by the scr. The led illuminates and, when the 'phone is replaced on its hook, lights up a little brighter. When the handset is replaced the switch can be released. When the remote handset is picked up, the music stops and the led goes out since there is insufficient holding current for the scr.

Further such circuits may be used in parallel.

**Robert L A Trost** Duiven Holland D33



ELECTRONICS WORLD October 1999

#### **CIRCUIT IDEAS**

### 220VAC

### **Sleep switch for lamps**

This device will switch off a reading lamp after about half an hour, the reader then probably being asleep. After switching the circuit on, the led illuminates for around 25 minutes; at 19min, it starts to blink for two minutes, stops blinking for two minutes and blinks for another two, just before switching the lamp off.

The n-p-n and p-n-p combination are either both on or both off, taking very little current in the off state. Pressing  $P_1$  starts things off by turning the relay on to power the ics. The lamp comes on and the 4060 oscillator/counter is reset on pin 12. It oscillates at a frequency determined by its *CR* and pin 3 goes high after around 30min, turning the transistors off.

Blinking of the lamp is the function of the outputs 1, 2 and 15 of the 4060 to the nand gates, which are in parallel for a greater lamp current, the oscillator output at pin 9 setting the blinking frequency. You can connect a piezoelectric sounder, if required, to pins 1 and 14 of the

piezoelectric sounder, if required, to pins 1 and 14 of the nand pair.

Flavio Delliprave Genoa Italy D22

If you are in the habit of drifting off to sleep when reading in bed, this circuit switches off the reading lamp after half an hour or so.

(D22)

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# AC continuity testing

To provide a simple test of continuity in a multi-core cable, the ac tester injects an ac signal into one wire and indicates the signal on another resulting from interweave capacitance. This enables the correct end of the cable to be repaired. The circuit draws only  $25\mu$ A for most of the time.

Both halves of a Maxim *MAX922* dual comparator are used: one to

form a 60kHz relaxation oscillator and the other a detector. Output to the cable is a peak-to-peak signal at the supply voltage of 2.5-6V, this being rectified in the detector by the diode and integrated on a 10nF capacitor with a bleed across it to discharge it between tests.

A certain amount of circuit protection is afforded by the  $100\Omega$ resistors in series with the cable and by diodes  $D_{1,3}$ . A 2m IEC mains lead makes a good test lead, having a leadto-lead capacitance of 200pF, although the circuit works with C less than 100pF.

Output indicator is a led in this arrangement, but an audible device may be substituted. *Kevin Bilke Maxim UK Ltd* D35



# Dc step-up voltage converter

F rom an input of 10-40V DC, this circuit produces an output of up to 3kV DC.Control voltage for the output stage comes from the op-amp buffer taking its input from either an

C

outside source such as a d-to-a converter or from the 723 voltage regulator driven by the voltage at  $R_{\text{ctrl}}$ . The free-running flip-flop produces base drive for the power darlingtons  $Tr_{3-6}$  at about 3kHz.

The transformer need not be anything special for outputs to 3kV, an audio type being suitable, one with a split secondary having the two windings connected as the primary; diodes  $D_{1-4}$  being selected to cope with the highest output voltage, which is determined by,

Voltage converter to give up to 3000V DC from an input of 10-40V DC, which may be a varying waveform.





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Swift Eurotech Ltd., Twankhams Alley, 160 High Street, Epping, Essex, CM16 4AQ, UK.

Can



# Peak-video-to-dc converter



Peak-to-peak video voltage is converted by this circuit arrangement to a direct voltage.

Figure 1 shows the comparator circuit to detect the positive peak. Voltage at pin 2 follows that at pin 3, the input. If the input is greater than the voltage at pin 2, the op-amp open collector is off and base current for  $Tr_1$  comes through  $R_1$ , allowing the capacitor to charge to the input voltage. When the input reduces, the position is reversed and the transistor turns off, the peak voltage remaining on the emitter, since the emitter *CR* is long.

Negative peaks require a modification, as shown in the complete diagram of Fig. 2, in which the extra n-p-n transistor ensures rapid turn-off of the p-n-p device after the peak input voltage is past. J M Rowe Kowloon Hong Kong D37

+12V

Fig. 1. Comparator for detecting the positive peak.



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## Synchronous am detector

This produces a low-distortion baseband output after a 455kHz if strip, the *NE564* linear phase-locked loop generating a 455kHz signal in phase with the if carrier.

Output of the pll is 1820kHz, set by  $C_2$ , applied to the 4027 divide-byfour ic to produce 455kHz outputs in phase quadrature. One of these, from pin 15 of the 4027, is fed back to the reference of the *NE564* and is in quadrature with the if when the loop is locked. Outputs from pins 1 and 2 form a balanced drive, in phase with the if, for the 1496 mixer/demodulator.

Components  $C_1R_1$  are the pll loop filter to set the open-loop characteristics and therefore the critically damped closed-loop response, bandwidth being around 5kHz. The pll will track the input over  $\pm 150$ kHz.

The only adjustment is that of  $C_2$ , which is set to give a vco freerunning frequency of 455kHz on pin 10 of the 4027, with no input connected and after a warm-up time of two minutes. A dc level at pin 14 of the 564 may be used to drive a centre-zero tuning meter. The pll needs a small heatsink to reduce temperature effects; all components are of 5% tolerance.

Distortion was measured at 0.2% although, since this was also the distortion of the rf generator used, it is probably a good deal less than that. *P Goodson Bracknell Berkshire* D42





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# Voltage control for a digital delay line

**Figure 1** shows the arrangement of a tapped digital delay line, the precise delay between input and taps being determined by a control voltage.

Input  $v_i(t)$  is applied to a sampleand-hold whose clock is the output of a voltage-controlled oscillator. From the s/h, the sampled voltage  $v_i(nT)$ goes to a fast a-to-d converter whose output shifts into the first 8-bit parallel shift register of 12 in a line, the shift for the first being provided by the end-of-conversion signal from the a-to-d converter. Sampling clock pulses for the s/h are also used as clock pulses for the shift registers, each of which shifts right on every clock pulse.

Output from the fourth, eighth and twelfth registers are taken to d-to-a converters, which then provide the delay-line output in analogue form after the relevant delay: 4T, 8T and 12T, T being the clock period, so that the output from the fourth register will be

#### $\Phi_1 = v_i((n-4) T),$

and so on. The result of all this is that the delay periods are controlled by the control voltage to the voltagecontrolled oscillator. More registers and taps would, clearly, be used and perhaps the delay line could be developed as an ic.

One use of this delay line would be as a phased antenna array to provide electronic scanning.

K Balasubramanian K B Gayathri H Camur

European University of Lefke Turkish Republic of Northern Cyprus D25


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#### **CIRCUIT IDEAS**

# Quick-on, delayed-off switching

It is sometimes required to switch a piece of equipment on by means of a push-button switch operating a toggle of some kind, such as a flip-flop, immediate accidental switching off being prevented. This circuit consists simply of a 4013 flip-flop and part of a 40106 inverter.

Output Q is initially logic zero, operating the switch charging C through the diode and the flip-flop output impedance; the output now becomes 1. Releasing the switch discharges C through  $R_1$ , further switching having no effect since the diode will not conduct. However, holding the switch on for long enough for C to charge via  $R_2$  clocks the flip-flop and the output goes back to logic zero.

For delays of around 1s,  $R_2 = 10M\Omega$  and C = 100nF. On power-up, the flip-flop's set and reset inputs should be used to put the output into the required state.

#### **B** Vojnovic

**R G Newman** Gray Laboratory Cancer Research Trust Mount Vernon Hospital Northwood Middlesex D39



Power switching circuit to impose a delay after switch-on before switchoff can occur.

## Using a 555 for speed control

Offset circuit avoids problems in the use of the 555 for pwm speed control.

(D29)

Since the capacitor voltage in NE555 applications must be limited to between 33% and 67% of  $V_{cc}$ , there are problems with the ic when used for pulse-width modulation in speed control, as the

speed setting is usually between, for example, zero and 10V. This circuit provides an offset between capacitor voltage and the 555 sensed voltage to overcome that drawback.

+15V

Inserting  $R_2$  between  $R_1$  and  $C_2$ , makes the capacitor discharge to a lower level before it triggers the 555; the threshold is unaffected.

As shown, the capacitor starts to charge at 1.8V and to discharge at 10V. In this case, a pwm minimum duty cycle was 5%, so the capacitor voltage comes from pin 7 of the 555 to allow the negative input of the op-amp to stay near ground during the discharge. Bypassing the diode causes the pwm signal to disappear and the output to remain low during the capacitor discharge.

The reference voltage for the potentiometer comes from the internal reference in the 555, the transistor on the control-voltage pin, pin 5, allowing it to drive low impedances without affecting the control voltage.

**Bernard van den Abeele** Evergem Belgium



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#### **CIRCUIT IDEAS**

# Lead-acid battery charger

This battery charger for lead-acid batteries switches of the charge when the battery voltage rises above that of a fully charged battery, which has been used for calibration.

The potential divider incorporating  $VR_1$  must be adjusted so that the op-amp output just becomes high when the calibrating battery is in position, so that when the battery under charge is in place, an increase in its voltage to more than 100mV above that of a fully charged battery turns on the transistor by way of the led and the relay is activated to stop the charge.

D30

Ejaz Ur Rehman ACD-Pinstech Islamabad Pakistan



Lead-acid battery charger stops the charge automatically when the battery is fully charged.

## **Electronic load**

here are several methods of testing DC power supplies using variable loads, but they turn out to be unwieldy and difficult to adjust (rheostats), or to need heat sinks and insulation (power transistors). Wirewound resistors suffer from neither defect and can be obtained in metal-clad types with insulation.

Figure 1 shows one method. A fast-switching mosfet with a choke in



its drain draws the supply current, dissipation being low in the Class-D operation adopted. Waste power is simply dumped in the resistor, which is of fixed value, the variation being taken care of by varying the pulse width. In testing the circuit, it became clear that the diode is unnecessary, which gives more current from the supply; the choke  $L_1$  may also be left out to leave only the resistor in circuit.

However, it is best to keep the choke as part of a filter using  $C_{1,2}$  to smooth the pulses to the supply, as seen in Fig. 2. Variable-width pulses come from the 555, which takes its own supply from terminal B or from a secondary winding on the choke via D2.3

Pulse width is varied by  $P_1$  to

provide effectively a variable resistive load from around 33 $\Omega$  to 2.7 $\Omega$ . Switching frequency, determined by  $P_1R_{2,3}C_3$ , is about 15-60kHz, the off time of the mosfet being 15µs and the on time variable from 1.5µs to 50µs, so the duty cycle is theoretically 9%-77%, although switching times mean a lower limit of 6%.

The turns ratio of  $L_1$  is such that at least 12V goes to  $D_{2,3}$  from the ripple across the primary. Capacitor C2 must withstand the ripple caused by switching and must be a multiple unit. Resistance  $R_1$ , which consists of five resistors, is fixed to a 25 by 15cm aluminium sheet and the mosfet is fitted with a 10°C/W heat sink. C I D Catto D32

Cambridge

Fig. 1. One way of providing a variable load for power supply testing is to pulsewidth modulate a mosfet and dump the power into a fixed resistor.



Fig. 2. Variable load for testing power supplies avoids the use of rheostats and power transistors.





#### **Review subjects**

The first review covered *Electronics Workbench* version 5.12, whose maker is IIT Ltd of Canada. Workbench's UK supplier is Adept Scientific plc, tel 01462 480055. *Electronic Workbench*'s price is £199.

Rod looked at *CircuitMaker* in the August issue. This £199 package is made by MicroCode in the US and supplied by Labvolt in the UK, tel. 01480 300695.

*Tina Pro*, priced at £299, was featured in the September issue. Quickroute supplies Tina in the UK, tel 0161 4760202.

*Pulsar and Analyser* from Number One Systems, which are modules from the *Easy PC* package, are the subjects of Rod's next review. Rod Cooper investigates the comprehensive circuit CAD package Proteus, which has recently benefited from a new simulation engine. This design tool is different from those reviewed so far in that it has no virtual instruments. But does that matter?

# The route to simulation IV

Prospice is the newly developed engine at the heart of the LISA simulator, which is part of the Proteus IV version 4.6 package. LISA is an acronym that simply stands for Labcenter Integrated Simulation Architecture.

The other two parts of Proteus are ISIS, the schematic drawing and capture program, and ARES, the pcb drafting and routeing program. All three are tightly integrated into Proteus, with the same style of operation, menus, graphics and screen layout. The considerable benefits of having all three combined into one package have already been extolled.

Labcenter's Prospice is based on Spice 3F5 and is a true mixed-mode simulator, and a complete replacement for the analogue and digital enginespreviously used. LISA is fully integrated with ISIS; that is, you do not have to transfer out of ISIS into LISA to run a simulation.

When it comes to simulation, LISA and ISIS are fully integrated. Graphs and other results appear as an overlay on the schematic screen, and in this respect it is very similar to the other programs reviewed to date.

#### Pay for what you need

There are several levels of ISIS with corresponding prices. The aspect usually of most interest here is the pin and node limit. The price starts at £295 for the lowest level with a schematic limit of 1000 pins and a simulator limit of 250 nodes.

Having a node limit overcomes the frequent complaint that a pin-limited simulator gives a false impression of its capacity. This is because there can be several pins used up in just one node.

A few features are omitted from the lowest levels, such as the sweep ability. In view of so much variability, it is probably best to discuss your design requirement, and what you can afford, with the company. If you subsequently find the limit is too small, it is possible to upgrade at reasonable cost.

#### **Documentation**

Proteus's documentation is comprehensive. It covers every aspect of operation, including tutorials and technical reference. It comes as a single hefty A5 looseleaf book in three sections covering ISIS, LISA and ARES. Being loose leaf, the manual can be readily upgraded.

Like other makers, Labcenter has its own terminology, but this is well explained.

Background on the reasons for certain types of operation is also provided. This can be helpful in getting to grips with some aspects of Spice. Generally, the literature is clear, concise and plentiful. It is well complemented by the program's Help files. The CD includes a useful animated tutorial.



Fig. 1. This simple Sallen & Key filter shows the uncluttered drawing area of the schematic capture and simulator, with the parts bin on the right set up for general work on filters, from which a handful of symbols has been chosen for this circuit. Note how the signal generator on the input is attached, and the voltage probe on the output.



Fig. 2. The signal generator – the symbol highlighted in red on the left – is set up by this menu, contrasting with the virtual instrument approach. This type of menu system is used throughout the simulator.

#### Schematic capture

In brief, ISIS is an efficient schematic drawing program. It is well-endowed with features without being over-complex, and it has notably good graphics quality.

ISIS has a different style from the other Windows programs reviewed to date. For example there are no Windows-style scroll bars.

Panning is carried out by bumping the mouse against the edge of the drawing area. There are no expandable tool and symbol bars. Instead there is Labcenter's own method of accessing symbols, tools, etc., Fig. 1. On the right of the screen, the map area, tool area and parts bin all take up a fixed part of the monitor screen.

There are several other features characteristic only of Proteus, but this is a well-developed system, which has stood the test of time. It takes a little getting used to, but is rapid and effective in use once you have familiarised yourself with it.

The package has maintained its consistency through several upgrades. If you are an existing user of an earlier version, you should find upgrading reasonably painless.

Unlike Tina, Workbench and CircuitMaker, ISIS does not have predetermined parts bins. However, it is easy to set up the ISIS parts bins with a permanent stock of symbols of your choice and save it if you wish. This makes ISIS suitable for experimental designing on-screen. I covered this important aspect in the Introduction in the August 1999 issue.

Figure 1 shows a parts bin set up as a type of permanent template for designing audio filters. It contains some generic and some specific devices. I could just as easily have loaded the template with all-generic devices for use as a purely experimental tool, and added other selections for, say, power supply or RF design.

On the subject of templates, Proteus has a sophisticated system where every detail from background colour to font type can be stored as a template.

The number of available symbols has been increased to 6000, including a small volume of thermionic valves, backed by 4000 Spice models.

New symbols can be created or modified via a graphics editor. A substantial section of the manual describes how Spice models can be generated, either from scratch or imported from manufacturers' Spice data, and attached to them. Labcenter offer the best support in this review for other makers' net lists, in addition to its own SDF format. These include Boardmaker (Tsien), EEDesigner, Futurenet, Multiwire, Racal, Tango, Valid, Vutrax, Spice-Age (Dos) and of course Spice.

If you want more detailed information on schematic capturein ISIS, you will find it in my review in the May 98 edition of *Electronics World*.

#### Simulation

The new Prospice true mixed-mode simulator brings Labcenter's product into line with the other simulators reviewed so far. Most importantly, Prospice fulfils all the requirements for basic analyses listed in the introduction to these reviews. There are also several additional features, such as Fourier analysis, parameter sweeping and temperature modelling. Two points of special interest are described later.

Prospice does not use the virtual instrument concept. Instead, it uses icons that are handled within ISIS like ordinary schematic symbols. The icons are not wired in to terminals or nodes as they are in Workbench or Tina for example. Rather, they are dragged from the appropriate toolbox on the righthand side of the screen, and dropped onto wires in the schematic as shown in Fig. 1. The various icons representing signal sources, probes, etc., are then edited by a menu like that shown in Fig. 2 to set up the required parameters.

If you are a first-time buyer, don't be

#### Requirements

The Proteus software comes on a CD or six floppy disks. Installation is easy, with security by the registration name-and-number method.

This is a 32-bit program so runs naturally under Windows 95/98/NT. But it also runs under Windows 3.1 with the Win32s extension.

Labcenter has announced this is the last version that will run on Windows 3.1. All future versions will be for Windows 95/NT, or whatever OS Microsoft replaces them with.

A 50MHz 486DX with 12Mbyte RAM for Win3.1, or 16Mb RAM for NT are suggested as minimum hardware requirements. In addition, 20Mb of hard disk space is needed. put off by the absence of virtual instruments. True, the symbol/menu method is less intuitive, and and you will need to read the manual a little more. However, symbols and menus are easy to learn, and efficient in use. Some will prefer this method.

Generally, the range and scope of the menu system was good, and not too complex.

Analysis graphs are placed directly onto, or over, the schematic drawing,

Fig. 3. Analysis graphs, like this one of input impedance, are drawn on the schematic drawing area at a size to suit the user.





Fig. 4. Once you have produced your graph, in this case gain and phase, it can be run full-screen for closer examination or taking measurements.



Fig. 5. A typical timing chart in digital analysis. Note the glitches. The glitch threshold time can be easily set in order to discriminate the various glitches by editing the properties of the devices in the schematic. Fig. 3. First, the outline is drawn to whatever size and shape the user finds suitable. Conveniently, the graph is slotted into an unused corner of the drawing sheet, or over an unimportant part of the schematic. This is the opposite of other Windows programs, where you may get a pre-sized window after simulation, which you then have to resize and reposition.

For taking accurate measurements, the graphs can be expanded to full-screen as shown in Fig. 4.

Signals are extracted for analysis by attaching probes to schematic wires in the same way that icons are placed. The required analysis is picked from the menu bar and can be run from the menu system. For example, if you want a graph of amplitude and phase versus frequency, you click on 'graph' then use the menu to set the graph up.

There is often a choice of routes for manipulating the analysis. Some of the setting up is intuitive, but not all. For example, to set up the graph of Fig. 4, one voltage probe was dragged onto the left 'y' axis to assign this to amplitude and another dragged onto the right to assign this to phase, to produce the familiar double graph. This method has to be learned from the manual, but once assimilated it is a rapid and adaptable system. Such methods are repeated throughout the program. They allow flexibility, but also demand a fairly steep learning curve.

Like CircuitMaker and Tina, Prospice can produce graphs of input and output impedance versus frequency, as Fig. 3 shows. The method used is indirect, but easy to apply.

There are two features that I found interesting. One is the ability to listen to audio frequency signals, providing your PC has a sound card. If you are working on music effects such as flanging or phasing, frequency shifting for public address, or audio filters, this could be very useful.

Another feature offers an easy way for a part of a circuit to be simulated in isolation. This is an advantage on large or complex circuits.

#### Proteus

Produced and distributed by Labcenter Electronics, tel. 01756 753440, fax 01756 752857. Prices range from £295 to £1625 excluding VAT. Lower cost packages upgradable. E-mail info@labcenter.co.uk site address http://www.labcenter.co.uk. In digital analysis Prospice has a good method of allowing the operator to set the glitch threshold time. Having this control enables you to view only the glitches that you deem significant, avoiding the large numbers of small and unimportant glitches that some circuits produce when simulated. This avoids the idealised timing diagrams that other programs favour.

The digital analysis recognises strong high and low, weak high and low, floating, contention and three other states. Colours are allotted to the first six states so that they can be readily observed on the timing chart.

There are no concessions to education in Proteus. This is not to say it could not be used for teaching students in the later stages of their education. Indeed it would give them a good insight into a system they could be using for commercial designs in the outside world.

However, it is in the completeness and scope of the basic analyses where Prospice scores particularly well.

#### In summary

Once again, Labcenter has concentrated on the essentials and presented these in depth rather than providing a lot of peripheral features of marginal use. In doing so the company has produced an excellent all-round simulator.

You are unlikely to be in a position of needing a detailed basic simulation, but finding the program cannot do such a simulation. This is often the case with other programs in this sector of the market.

However, Prospice is not without its share of specialised features. The ability to listen to sounds is one example. Where these are provided though, they tend to have a strong practical purpose.

On the whole, Proteus has a moderately steep learning curve. This is offset by having the three functions of schematic drawing, simulation and pcb routeing all in one program. As I have pointed out, this means you only have to learn one system of operation.

The Labcenter method of offering a range of prices for various versions of the program, limited by the number of pins or nodes it can handle, is a good one. It means that, even if you are on a strict budget, you can start small and still get all the basic simulations. If you want, you can spread the capital expenditure by choosing to upgrade at a later date.

In last month's review, of Tina, Figs 4 and 5 were transposed. Sorry. Ed.

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# Finishing off

Ian Hickman looks at some of the many ways a prototype or one-off instrument can be given a professional look without the expense of using professional techniques.

have made a number of instruments for my own laboratory, and I have found that it is often possible to make them perform as well as expensive commercial equivalents, but at a fraction of the cost.

In the early stages of my career, I took a pragmatic view, being satisfied with the outcome however it looked, provided it functioned as desired. But for many years now, I have striven for a more professional looking finish. There are quite a few ways of achieving this and some of them are discussed below.

#### Working the enclosure

Unless you have a penchant for metalwork, and access to the necessary guillotine, bender etc, you will probably build most of your equipment in commercial ready-made cases. That way, whatever the innards may look like, you are guaranteed a professional finish, given only that the front panel legending is well laid out and neatly executed.

Legending can be done in various ways, of which one of the earliest was via 'Letraset'. This consists of rubdown lettering on transparent carrier sheets carrying letters, numbers and other symbols. Such sheets are available in various point sizes and colours, most commonly black.

With care and practice, a very neat front panel appearance can be created, on either metal or plastic surfaces. The art is to get all the letters of any particular legend exactly in line. This makes the process fairly time consuming, but that should not be a great problem for a one-off.

There are however one or two drawbacks to applying Letraset directly to a front panel in this way. The first concerns durability; it is advisable to protect the lettering with a clear coating of some description.

Clear copal varnish has been used, brushed over each legend individually. But the various varnished areas are usually visible – especially after a while when the varnish has yellowed a little.

A better result is obtained by spraying the whole panel with an aerosol clear lacquer, I use RS stock No 567-480. This no longer appears in the current catalogue, having been replaced by clear lacquer 562-307. This newer spray should work as well as its predecessor, but I have not yet tried it. Alternatively, you could use clear acrylic lacquer 215-1217.

The second drawback concerns applying Letraset after an instrument has been built and tested. You are faced with an awkward choice. You can either dismantle the front panel controls, to enable the lettering to be applied in a straightforward manner to a flat surface, or you can try to work around projecting switch shafts, panel connectors, meters etc.

Dismantling the instrument can be undesirable for a number of reasons, but working round projections is extremely inconvenient, and furthermore requires masking of connectors, etc., when spraying lacquer.

#### Other panel techniques

Another very neat panel legending method that I have used in the past involved an RS photo-imaging system. This consisted of negative-working photo-imaging film 556-553, a choice of laminating film in various colours, and aerosol developer 556-610.

I used the white/yellow laminate 556-575 on an instrument of mine pub-

lished a while ago.<sup>1</sup> It resulted in smart yellow lettering on a black background.

Positive artwork of the required panel legend was used to expose the photoimaging film, using e.g. the small RS ultra-violet exposure unit. The exposure time is not critical, and indeed contact printing using daylight is possible.

After exposure, the matt black side of the film is sprayed with the aerosol developer and left for 15 seconds. It is then washed off under running cold water, leaving clear lettering against a black background.

The developed film is dried and stuck to the double sided sticky laminating film, the white or yellow surface of the latter showing through as lettering at choice, against the black background. The other side fixes the finished artwork to the front panel of the instrument.

Alternatively, the developed film may be used as an intermediate artwork, to expose another sheet of the material. This gives four possibilities: white or yellow lettering on a black ground, or black lettering on a white or yellow ground.

The material does not seem to feature in the current RS catalogue. But it is so useful that I am sure it must be available from stockists of supplies for the graphics industries, along with laminating film of other two-colour combinations, giving a wide choice of lettering or background colouring.

#### If you make your own PCBs...

Speaking of UV exposure units, many of you are doubtless geared up for making your own PCBs. The same facilities can be used for making a front panel overlay. The result will be copper letters on a light brownish background



Fig. 1. The front panel of the THD Meter, shown 75% full size.

- assuming the common SRBP base material.

Tinning the letters then results in attractive silver lettering, which should then however be lacquer-sprayed to prevent tarnishing.\* If single sided SRBP is used, the lettered panel can be secured to the metal front panel of the instrument by means of the nuts securing the bosses of switches, pots, coax sockets etc.

If double sided material is used, it can do duty as the front panel in its own right, the rear copper providing screening.

Sometimes the technique is useful for just a small subpanel, to hold a BNC socket the outer of which must be insulated from the instrument case, for example. The single-sided material can also carry the legend relating to the function of the socket.

However, where the legend is carried on the same artwork as the rest of the front panel, the easiest solution to use an isolated BNC socket is the ready made variety, such as RS stock No 456-706 ( $50\Omega$ ) or 456-946 ( $75\Omega$ ).

#### Or if you don't ...

Those of you not yet into making your own PCBs might find a transfer system involving a photocopier more interesting.

This scheme makes use of a transfer medium, consisting of a clear plastic

carrier sheet, obtainable in A4 size from a UK supplier.<sup>2</sup> Onto this is printed the desired pattern, which should be in reverse, i.e. a mirror image. The printing is applied to the matt side of the sheet, which is indicated by its protective layer of paper.

The printed sheet is then laid onto the copper-clad board – which should be scrupulously clean – and the pattern is transferred under pressure and heat to the copper.

I have tried this material, transferring not a PCB pattern to copper-clad, but lettering onto a front panel. A little patience is needed to master the technique. If need be, any unsatisfactory results can be cleaned off the front panel with an organic solvent such as acetone (nail polish remover)<sup>†</sup> prior to repeating the operation.

While an ordinary domestic iron on its hottest setting can be used to apply both the heat and the pressure, a better scheme is to lay the panel on a hotplate and apply the pressure with a rubber roller. A suitable roller can be obtained, also from the company mentioned in reference 2.

Afterwards, the panel should be allowed to cool to room temperature, before carefully peeling off the clear carrier sheet. The finished lettering should be protected, either with one of the clear sprays already mentioned, self adhesive library film, or any other suitable method.

One wonders if the special sheets obtainable from some colour printer manufacturers, for printing tee shirts for example, could also be used for this purpose. This would allow the front panel to be livened up using colours rather than black.

#### My current method

I used the following method just recently to legend the front panel of my total harmonic distortion meter.<sup>3</sup>

This instrument was housed in a case previously used for another design. As a result, the front-panel layout of the new instrument was constrained by the already existing holes.

In the event, just two new holes were needed, one for the 'fine' tuning control, and one to accommodate the barrel of the meter. The panel of the meter also covered two redundant holes from the earlier use.

Positions of all the holes to be used were measured and plotted on half centimetre squared paper. Fortunately it turned out that I had been quite methodical with the original construction, all measurements being sensible metric quantities.

As the panel drawing would have been a tight fit across an A4 page, it was drawn rotated through  $90^{\circ}$  to a sideways 'portrait' orientation.

The circles drawn on the paper were



Fig. 2. Completed battery-powered THD meter, showing the flying supply lead, via which the unit can alternatively be powered from an external source of ±15 to 18V dc. marked in at a suitable size to just clear the retaining nuts of rotary switches and pots, and the front-of-panel flanges of BNC sockets. This meant that later, applying the legending would require only the removal of knobs and the meter; the inconvenience of dismantling controls and sockets from the front panel being avoided.

The squared paper with its panel outline and hole positions was scanned in to my computer. It was exported from Paperport<sup>TM</sup> as a bit-mapped .BMP file, for use as a template in an Adobe Illustrator<sup>TM</sup> .AI file. Illustrator files are vector files similar to Corel .CDR and .WMF files, as opposed to bit map files like .bmp and .tif.

As Illustrator complained that the area was too large to load as a template, it was suitably reduced in size first, using Paintshop  $Pro^{TM}$ . Using the template as a guide, an Illustrator .AI file was created, showing the panel outline and the clearance holes.

The portrait panel drawing was then rotated through  $90^{\circ}$  so that the legending relating to the various controls and sockets could be added conveniently.

Afterwards, the drawing was rotated  $270^{\circ}$  to restore the portrait orientation. A copy was run off, and the panel outline dimensions as printed were measured. These were compared with the actual panel dimensions, and the .AI file scaled to restore the required drawing size, the result being as shown in Fig. 1.

#### Protecting the print-out

The final version of Fig. 1 was printed out on white paper, the front surface of which was sprayed lightly with 3M Spray Mount<sup>TM</sup> adhesive. After waiting the recommended few seconds to allow the surface to become tacky, the print was carefully laid down onto a blank view-foil sheet, as used for overhead projectors.

Next, with a surgical scalpel, the holes were cut out, the ones for the BNC sockets being slightly undersize. The holes for controls were less critical, being completely covered by the flanges of knobs.

The view-foil/paper composite was then cropped to size using a small guillotine I bought many years ago for photographic work. The composite was offered up to the instrument, and slight enlargement adjustments made to the holes for the BNC sockets, to suit.

Finally, the reverse side of the composite was sprayed and, when tacky, placed in position on the instruments front panel. The result is a neat appearance, with the legending protected from dirt and smudging behind the plastic sheet.

Like some of the other methods mentioned, this scheme blanks off and hides any redundant holes, which is particularly useful when you are reusing an enclosure. However, two of the holes in the front panel that I originally intended to hide were in fact equipped with BNC sockets labelled -V and +V. These sockets are connected directly to the internal +18V and -18V battery supplies.

These sockets make it possible to measure the battery voltages with the instrument switched either on or off. The difference between the on and off voltages provides an indication of the state of the batteries.

#### A variant for plastic cases

I recently produced a special-to-type test box for a well known electronics company. This was built in one of the popular range of glossy grey ABS boxes, namely RS stock No 503-650.

The grey lid of the box, forming the front panel, was entirely acceptable aesthetically. It just needed legending added. So in this case, the front panel legending was produced as a .AI file, which was then reversed to give back to front lettering.

The legending was printed out on my Laserjet 5MP printer, on an overhead projector view-foil. The lettering thus looked the right way round when the foil was mounted on the front panel. Having the printing in contact with the panel protects it from dirt, abrasion etc.

A word of warning though. Do not use the grade of overhead projector foil sold for use in photocopiers. It might be alright, or it might result in an expensive repair. Be sure to use foil specifically stated as suitable for laser printers.

The foil could have been laid down as a whole, as described in the preceding section. However, this was another case where it was desirable to avoid dismantling the finished, tested product.

Most of the items on the front panel were LEDs, push-buttons, connectors etc., neatly arranged in rows. So instead of producing and fitting an overlay the size of the whole front panel, strips of the foil carrying the relevant legends were mounted where appropriate, as separate items, using 3M Spray Mount<sup>™</sup> adhesive.

The result was a neat appearance produced in the minimum of time, the separate areas of foil with their bold lettering blending in almost invisibly with the light-grey front panel.

#### References

- 1. The EnviroSynth, Ian Hickman, Maplin Magazine, June 1992.
- 2. TEC 200 Image Film, obtainable from PSS Services Ltd, 217 Prestbury Road, Cheltenham, Gloucs GL52 3ES.
- 3. Measure THD below 0.001%, Ian Hickman, *Electronics World*, Aug. 1999, pp 626 - 633.

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- \* Automatic solid-state antenna switch for single antenna use.
- \* Microcontroller with watchdog timer for added security.

# **NEW PRODUCTS**

#### Please quote Electronics World when seeking further information

#### Potentiometers

Xicor has announced two non-volatile, digital potentiometers. The X9250 and X9258 are quad, 256-tap devices with a standby current of 1µA maximum. They can be used to preset analogue system values or trim offset voltages during manufacture. The settings can be made automatically. The circuit has long-term temperature and time stability. *Xicor* 

Tel; 01993 700544 Enquiry No 502

#### 16-bit d-to-a converter

SPT has announced the SPT5510 16-bit digital-to-analogue converter. This 200MHz part has a settling time of 35ns to 16-bit accuracy and 15ns to 14-bit accuracy with glitch impulse energy of 30pV-s. Non-linearity is less than 1LSB typical INL and DNL. It comes In a 44-lead metric quad flat pack and works from -40 to +85°C. *Signal Processing Technologies Tel: 001 719 528 2300* **Enguiry No 503** 

#### Design software

Fast Analog Solutions has announced a version of its development software

#### Chip trio give voice to DSL

Ericsson has introduced three chips for voice over DSL, providing users with up to four additional telephone lines over their xDSL connection. The PBM 990 08/1 ATM multi-service chip handles clrcuit emulation for up to four POTS lines. The PBM 397 06/1 is a dual-channel PCM codec with on-chip DTMF support. The PBL 387 10/1 ring Slic is an analogue POTS interface, including voice, signalling and ringing. To incorporate them into existing data modems, no additional processing power is required because most of the ATM handling and circuit emulation are performed by the multi-service chip.

Ericsson Microelectronics Tel: +46 8 757 47 00 Enquiry No 501



# PAS TRADORDUM

with support for Windows NT for its Trac reconfigurable analogue circuit. The software has the look and feel of the existing versions, which support Windows 3.11, 95 and 98. It provides design and simulation tools, and lets designs be downloaded and uploaded to and from the device. Fast Analogue Solutions Tel: 0161 622 4567 Enquiry No 504

#### **Dual UART**

Philips Semiconductors has available the SC28L92 dual UART – the third member of its Impact line. It operates at 3.3 and 5V with the Intel or Motorola bus and supports commercial and industrial temperature ranges. The single-chip CMOS LSI chip provides two full-duplex asynchronous receiver and transmitter channels. It interfaces directly with microprocessors and can be used in polled or interrupt driven systems. It is a pin and function



equivalent to the company's other dual UARTs. Features include 16 character receiver, 16 character transmit first-in-first-out buffers, watchdog timer for each receiver, and a mode register. The chip comes in a 44-pin PLCC or PQFP. *Philips semiconductors Tel: 00 31 40 272 2091 Enquiry No 506* 

#### ADSL chip set

Two fully-programmable DSP-based ADSL chip sets for central office and customer premises applications are available from Texas Instruments. Both use the firm's TMS320C6000 DSP core. The TNETD4000C supports four full-rate or G.lite ADSL lines In central office applications while the TNETD4000R is for equipment such as external modems and remote access routers. *Texas Instruments Tel: 01604 663000 Enquiry No 508* 

#### Motor controller

OmnIrel has introduced the OMC507 three-phase brushless DC motor controller. Rated at a 5A continuous average phase current, 10A peak for 10s and 28V DC bus voltage without needing a heatsink, the unit provides linear control of motor current (torque) in proportion to the input current command. The controller contains the power, driver and logic



#### **RF** transistors

Zetex has introduced RF transistors in SOT323 surface mount packages. Six NPN types are available, from the ZUMTS20 with a transition frequency of 450MHz to the ZUMTSI7 at 1.3GHz. Power dissipation is 330mW at an ambient temperature of 25°C. Typical noise performance is 4.5 or 6.0dB. The ZUMT5179 has a maximum collector-base capacitance of 1pF at 1MHz. Maximum collector-emitter voltages are between 12 and 20V. Applications include RF security systems, crystal oscillators, FM tuners and IF amplification. Zetex Tel: 0161 622 4422 Enquiry No 505

circuits to regulate the speed of the motor, including a PWM controller, three-phase output power stage, onboard current sense resistor and 10pF motor bus capacitor. It lets the user provide either an external



#### **NEW PRODUCTS**

#### Please quote Electronics World when seeking further information

analogue or TTL PWM input command, or an analogue command can be provided onboard. *Omnriel Tel:* 01435 867499 *Enguiry No 509* 

#### **Power relay**

Matsushita has introduced the CP1-SA surface mount power relay for the automotive industry. Measuring 13 x 14 x 10.5mm, it has a nominal current rating of 20A at 14V DC, but it can switch 40A for up to two mInutes. Infineon Technologies Tel: 01908 231555 Enquiry No 511

#### **IR sensor**

Murata's IRA-E940ST1 IR sensor detects a moving human body using four 1.35 by 1mm sensing elements and two outputs with an OR-AND logic circuit. Applications are security systems, lighting and household appliances. Typical response at 1Hz Is 5120V/W. Field of view is 50 x 55°.

#### **D-sub connectors**

Conec has developed D-subminiature combination connectors using planar technology to increase attenuation, reducing EMI and RFI. Attenuation is up to 45dB at 100MHz and 90dB at higher frequencies. Standard peak capacitance is 360pF. Voltage capability is up to 1500V DC as standard and up to 2500V DC as an option. There are five shell sizes and various signal, power and coaxial pin combinations. Power pins are rated at up to 40A with AWG8 contacts. Infineon Technologies Tel: 01344 396313 Enquiry No 510



It works from 2 to 15V supply over a range of -25 to +55°C. Infineon Technologies Tel: 01252 811777 Engulry No 512

#### **GTLP clock driver**

Fairchild Semiconductor's latest addition to its GTLP portfolio is a low drive clock driver that is a device capable of LVTTL to GTLP (and vice versa) signal level translation in the same package. The device is designed for high-speed performance in back-plane and bus applications in data networking and telecoms. The GTLP6C817 is designed with internal edge-rate control and is process, voltage, and temperature compensated. The device also features 50mA GTLP drive capability and bi-directional LVTTL to GTLP signal level translation. Fairchild Semiconductor Tel: 01793 856811 Enquiry No 514

#### 0.5 to 2.5GHz amplifier

Maxim's latest wideband buffer amplifier provides dual open-collector outputs capable of delivering -5dBm while maintaining harmonic suppression of better than -25dBc. The dual output of the MAX2472 makes these devices suitable for simultaneously driving two mixers, or a mixer and a PLL, according to the company.

There is also a single open-collector output version (MAX2473) with an





#### Modem chip set for VDSL

Infineon has introduced a modem chip set for the VDSL standard, using frequency division duplexing (FDD). VDSL over conventional twisted-pair copper provides symmetrical and asymmetrical data transmission up to 13/Mbit/s. Based on the firm's Potswire technology, the three-device chip set uses FDD and QAM line code to handle POTS and ISDN services on the same twisted pair and XDSL services on the same bundle. It can also be configured to support spectral compatibility with amateur radio. The chip set comprises the PEB22810 VDSL line driver, the PEB22811 VDSL analogue IC and the PEB22812 digItal IC. The analogue IC handles analogue-digital conversion, pre and post filtering and power control, including a power down mode with warm-start capability in less than 100ms.

Infineon Technologies Tel: 01344 396313 **Enquiry No 507** 

added feature of a bias control pin to vary the output power as needed to save current. Output power can be adjusted from –10dBm to –2dBm while maintaining harmonic suppression of better than –25dBc. Both amplifiers operate over a 500MHz to 2500MHz frequency range providing 12dB gain and greater than 40dB isolation at 900MHz. Maxim Tel: 0118 930 3388

Tel: 0118 930 3388 Enquiry No 515

#### 2.5Gbit/s I/O driver cores

LSI Logic claims that its current generation of Gigablaze integrated gigabit per second CMOS transceiver cores support the physical requirements of next generation I/O (NGIO). The cores meet NGIO's double-speed serial transfer rate of 2.5Gbit/s. The transceiver cores can be Integrated into system-level Asics. The firm's I/O cores were the basis of a number of Fibre Channel and Gigabit Ethernet products and It claims they will play their part in the volume launch of NGIO products LSI Logic

Tel:01344 413204 Enquiry No 516

## 2.5Gbit/s SONET/SDH interface

Vitesse's latest chip set implements a 2.5Gbit/s channelised SONET/SDH interface for ATM, packet-over-SONET and SONET/SDH transmission equipment. The V-Frame 2.5/SLT offers full SONET/ SDH section and line termination, including byte interleaving/de-



interleaving and multiplexing/ demultiplexing functions. The chip set is the second group of products in the company's V-Frame 2.5 family. It includes the VSC9111, a section/line terminator, which acts as the framer, and the VSC814O 16-bit transceiver with integrated clock generation capabilities. Both chlps work from a single 3.3V supply rail. *Vitesse Tel*:01634 863494 *Engulry No 517* 

#### Switched regulator

National SemIconductor has launched its first dual output switched capacitor regulator designed for portable communications applications. The device integrates a switched capacitor doubler, a low-dropout (LDO) regulator and a switched capacitor



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inverter in a low profile, TSSOP-14 package. The LM2685 provides a dual output (+5V regulated and -5V unregulated) power supply by using switched capacitor and LDO techniques. The +5V regulated power supply is required for components such as audio codecs, amplifiers and SIMs. The -5V can be used for contrast bias for LCDs, and to increase the dynamic range of operational amplifiers used for analogue inputs. National Semiconductor Tel:01634 863494 Enquiry No 518

#### Voltage regulator with enable

Low dropout voltage regulators from Semtech, designated the SC1540 and SC1540A are 300mA and 500mA

#### Flash/SRAM on one BGA

STMicroelectronics has introduced a device consisting of 8Mbit flash and 1Mbit SRAM in a single BGA48 chip scale package. The M36W108A's footprint of 12 x 10mm occupies around 60 per cent less space than separate flash and SRAM devices, according to the supplier. The flash memory is functionally Identical to the firm's M29W008A device and is organised as 1Mbit x 8 in a boot block configuration and the device is available with Top and Bottom boot block options. Operation Is from a single 2.7 - 3 .6V supply, with the high voltage required for erasure and programming being generated internally. The flash memory includes a Security Protection area factoryprogrammed with 256bytes of ID. The SRAM component is a 128k x 8-bit SRAM with fully static operation requiring no external clocks or timing signals and with equal address access and cycle times.

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regulators with the new feature of an enable pin. This allows the user to turn on or turn off the regulator as required. This feature can be used to turn on voltage rails in a determined order to ensure start-up sequences are followed, or to turn a voltage rail off for power saving in perhaps a battery powered application. Thame Components Tel:01844 261188 Enquiry No 519

#### In-circuit test platform

GenRad has enhanced its GR TestStation in-circuit test platform which can be configured from 256 to 7680 pins. Evolved from GenRad's GR228X technology the TestStation can be populated with any of the current CR228X pin cards or with the company's Ultra 121 all-real pin card. Existing CR228X fixtures and programs are fully compatible.The TestStation can be re-configured by adding modules to increase node count up to 7680 pins, or to populate the system with the Ultra 121 pin card. *Genrad* 

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measuring range are accepted without damage to the transducer, making the range suitable for current control or protection in many industrial applications. *LEM Tel: 00695 720777 Enguiry No 521* 

## CMOS IC targets hands-free phone

Austria Mikro Systeme's programmable chip for hands-free speaker phones is a mixed-mode CMOS integrated circuit for analogue telephones incorporating hands free speech circuit, CPU/dialler and tone ringer all in a 44 pln TQFP. The AS2525's software programmable

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parameters allow adaptation to various standards, such as ETSI (ETS 300 001, TBR21, TBR38) and FCC Part 68. The AS2591 is capable of driving a 7-segment LCD with up to 16 digits and 12 symbols. Infineon Technologies Tel: 00 43 3136 500265 Enquiry No 523

#### Software radio

Harris has announced a digital software-radio chip for cellular base stations. The software-programmable down-converter integrates everything except the baseband processor on one chip. Called the Commlink HSP50216 PDC, it can support up to four cellular protocols simultaneously, including CDMA, TDMA, IS-95, GSM, 3G and legacy protocols such as



Amps. The IC contains four separate channels capable of simultaneous multiple channel processing. It lets cellular operators move between existing radio interface standards. *Microchip Tel*: 01344 350250 Enquiry No 524

#### **CMOS image sensor**

Toshiba Electronics claims to have the world's smallest CMOS image sensor with an integral lens measuring 3.6mm. The sensor is fully compatible with the common intermediate format (CIF) for videoconferencing. It Is 10mm wide and deep and 6mm high Available in both colour (TCM5023LU) and black and white (TCM5020LU) versions, samples of the sensor are available immediately, with commercial quantities available from September 1999. The low-power CMOS device is suitable for batterypowered camera and videophone applications. Operation requires a 2.8V single power supply, and consumption is 15mW Infineon Technologies Tel: 0990 550500 Enquiry No 525

#### Small 1k serial EEPROM

Microchip claims to have the world's smallest 1k serial EEPROM in a 5-lead SOT-23 package. This means the 24LC01B offers a 50 per cent reduction In board space compared with a standard 8-lead TSSOP



#### In-circuit test platform

Infineon Technologies' latest chip for T1/El echo cancellation, the SIDEC (Smart Integrated Digital Echo Canceller), PEB20954 suppresses both electrical and acoustic echo and effectively compensates for these unwanted delays. It provides TI/El echo cancelling for up to 32 channels In accordance with ITU-T G.165, G.168 and G.168 (2000) standards. It Integrates an array of different functional blocks onto a single device. These include: speech control, dlsabling logic, adaptive echo estimation unit, PCM I/O Interface with selectable p- and A-law coding, non-linear processor, subtractor, microprocessor interface and Universal Control and Communication interface for signalling highways with direct hardware control.

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package, and over 70 per cent compared with an 8-lead SOIC package. The EEPROM supports standard I<sup>2</sup>C protocol, 5µA typical standby current and 1mA read current, 200-year data retention and 1 000 000 erase/write cycles. *Microchip* Tel: 0118 921 5858 Enquiry No 526

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# Crystals made clear II

With the theory out of the way, Joe Carr now presents a variety of practical oscillator circuits for use with crystals ranging from 50kHz to 110MHz.

iller oscillators are analogous to the tuned-input/tuned-output variable-frequency oscillator. This is because they have a crystal at the input of the active device, and an *LC* tuned circuit at the output.

Figure 1 shows a basic Miller circuit built with a junction field effect transistor, or JFET. Any common RF device can be used for  $Tr_1$ , like for example the *MPF102*.

Direct-current bias is provided by  $R_2$ , which places the source terminal at a potential above ground due to the channel current flowing in  $Tr_1$ . The source must be kept at ground potential for AC, so a bypass capacitor,  $C_4$ , is provided. The reactance of this capacitor must be less than one-tenth the value of  $R_2$  at the lowest intended frequency of operation.

A parallel-resonant *LC* tank circuit,  $L_1/C_1$ , tunes the output circuit of the oscillator. The tuned circuit must be adjusted to the resonant frequency of the oscillator, although best performance usually occurs at a frequency slightly removed from the crystal frequency. If you monitor the output signal level while adjusting either  $C_1$  or  $L_1$  you will note a distinct difference between the high side and low side of the crystal frequency.

Best operation usually occurs at the low side. Whichever is selected though, care must be taken that the oscillator will start up reliably. Output can be taken either from capacitor  $C_2$ as shown, or through a link coupling winding on  $L_1$ .

The Miller oscillator of Fig. 1 has the advantage of being easy to implement, but it suffers from some problems as well. One is that the feedback is highly variable from one transistor to the next because it is created by the gate-drain capacitance of  $Tr_1$ . There are also output level variations noted, as well as frequency pulling, under output load impedance variations. These are not good attributes for an oscillator.

Also, there is a large difference in starting ability between JFETs of the same type number, and between different crystals of the same type number from the same manufacturer. I



#### Surely an equivalent transistor will do?

Be careful when using 'universal' replacement lines of transistors. Crystal oscillators may operate in an unwanted overtone mode – i.e. at a higher frequency. Or because of stray *LC* components they may parasitically oscillate on a VHF or UHF frequency.

Because of this, you will want to keep the gainbandwidth product of the active device low. But many replacement lines use a single high-frequency transistor with similar gain, collector current and power dissipation ratings as a 'one-size fits all' replacement for transistors with lower gain-bandwidth products.

I've seen that situation in service replacements on older equipment. The original component may not be available, so a universal service shop replacement line device is selected. It is then discovered that there are parasitic oscillations and other problems because the new replacement has a gain-bandwidth product of, say, 200MHz, whereas the old device was a 50MHz part.

This problem can show up especially severely in RF amplifiers and low-frequency oscillators where *LC* components naturally exist, or in any circuit where the stray and distributed *LC* elements provide the required phase shift on some frequency above the unity gain-bandwidth point.



have also noted problems with this circuit when either the JFET or crystal ages.

In the case of the JFET, I've seen oscillators that worked well, and then failed. When the JFET was replaced, it started working again. What surprised me was that the JFET appeared OK when tested.

Figure 2 shows an improved Miller oscillator. This circuit uses a dual-gate MOSFET, such as the 40673, as the active element. It is a fundamental-mode oscillator that uses the parallel-

resonant frequency of the crystal. The crystal circuit is connected to gate 1, while gate 2 is biased to a DC level. This circuit can provide a stability of 15 to 20 ppm if AT-cut or BT-cut crystals are used.

A problem that you might find with this circuit is parasitic oscillation at VHF frequencies. The MOSFETs used typically have substantial gain at VHF, so could oscillate at any frequency where Barkhausen's criteria are met.

There are two approaches to solving this problem. One approach is to insert a ferrite bead on the lead of gate 1 of the MOSFET. The ferrite bead acts like a VHF/UHF RF choke.

The second approach, shown in Fig. 2, is to insert a snubber resistor  $-R_S$  in Fig. 2 – between the crystal and gate 1 of the MOSFET. Usually, some value between 10 and  $47\Omega$  will provide the necessary protection. Use the highest value that permits sure starting of the oscillator.

One interesting aspect of the Miller oscillator of Fig. 2 is that it can be used as a frequency multiplier – not to be confused with an overtone oscillator – if the tuned network in the drain circuit of  $Tr_1$  is tuned to an integer multiple of the crystal frequency.

#### **Pierce oscillators**

The crystal being connected between the output and input of the active device characterises the Pierce oscillator. Figure 3 shows the basic Pierce crystal oscillator circuit using a bipolar n-p-n transistor such as a 2N2222or 2N5179.

The crystal connects directly from the collector to the base of  $Tr_1$ . Output is taken through capacitor  $C_2$  connected to the collector. This circuit is used extensively in low-cost receiver circuits, but is not recommended.

An improved Pierce oscillator is shown in Fig. 4. This circuit includes a capacitor,  $C_1$ , for pulling the crystal a small amount in order to tune the frequency precisely. With the capacitance values shown, this circuit operates at frequencies between 10 and 20MHz. If the output is lightly loaded, and  $C_4$  kept small, then the oscillator will provide reasonable output stability at a level of near 0dBm.

Figure 5 is a variation on the theme that works in the 50 to 500kHz region. This circuit is almost the same as Fig. 4, except for increased capacitance values to account for the lower frequency.

In both circuits ordinary n-p-n devices such as the 2N2222 can be used successfully.

#### **Butler oscillators**

Superficially, the Butler oscillator looks like the Colpitts in some manifestations, **Fig. 6**. The difference is that the crystal connects between the tap on the feedback network and the emitter of the transistor.

This particular circuit is a seriesmode oscillator. The value of  $R_1$ 





Fig. 3. In the Pierce oscillator, the crystal connects between the input and output of the active device – in this case an n-p-n transistor such as the 2N2222

#### **RF DESIGN**

should be whatever value between 100 and 1000 $\Omega$  that results in reliable oscillation and starting, while minimising crystal dissipation.

A table of capacitance values for feedback network  $C_1/C_2$  is provided. For the 3 to 10MHz range, use 47pF for  $C_1$  and 390pF for  $C_2$ ; for 10 to 20MHz select 22pF for  $C_1$  and 220pF for  $C_2$ .

The collector circuit is tuned by the combination of  $C_1$  and  $L_1$ . This circuit may well oscillate with the crystal shorted, and care must be taken to ensure that the 'free' oscillation and the crystal oscillation frequencies are the same. The crystal should take over oscillation when it is in the circuit.

The Butler oscillator of Fig. 6 is









Fig. 7. In this enhanced Butler oscillator, two additional transistors provide buffering and facilitate feedback. Its range is 300kHz to



capable of 10 to 20ppm stability if a buffer amplifier with good isolation is provided at the output. Otherwise, some frequency pulling with load variations might be noted.

The output signal is taken from a coupling winding over  $L_1$ . This winding is typically only a few turns of wire on one end of  $L_1$ . Alternatively, a tap on  $L_1$  might be provided, and the tap

connected to a low value capacitor. That approach might change some resonances unless care is taken.

Another alternative output scheme is to connect a small value capacitor to the collector of  $Tr_1$ . Keep the value low so as to reduce loading, and also to reduce the effects of the output capacitor on the resonance of  $L_1/C_1$ .

A somewhat more complex Butler

oscillator is shown in Fig. 7. This circuit is sometimes called an aperiodic oscillator circuit. It uses two additional transistors to provide buffering and also serve as part of the feedback circuit. The circuit will operate from about 300kHz to 10MHz, but the transistor may need to be selected carefully.

Many low-frequency crystals exhibit a lower equivalent series resistance, or



ESR, in one of the higher-frequency modes of oscillation than in the fundamental mode. As a result, you might find this circuit oscillating at some frequency in the medium wave or HF region, rather than at LF. The key to preventing this problem is to use a transistor with a lower gain-bandwidth product, such as a 2N3565. An explanation is given in the panel entitled, 'Surely an equivalent transistor will do?'

The circuit of Fig. 7 produces a sine wave output, but not without relatively strong harmonic output. The second and third harmonics are particularly evident. However, if harmonics are desired – when the oscillator is used in a frequency multiplier for example – then strong harmonics up to 30MHz can be generated from a 100kHz crystal if  $R_5$  is reduced to about 1k $\Omega$ .

The output of this oscillator is taken through an emitter-follower buffer. This circuit can be used as a general buffer for a number of oscillator circuits. It is generally a good practice to use a buffer amplifier with any oscillator in order to reduce loading and smooth out load impedance variations.

Another variation on the Butler theme is shown in Fig. 8. This circuit is similar to Fig. 7, but is a bit less sensitive to frequency pulling due to DC power supply voltage variations. It is good engineering practice to use a separate voltage regulator for all oscillator circuits though, in order to prevent such variation. The availability of low cost three-terminal integrated circuit voltage regulators makes this easy.

An improved Butler oscillator is shown in Fig. 9. This circuit is based on Fig. 7. Both circuits can be used at frequencies from LF up to the mid-HF region – about 12 to 15MHz – if appropriate values of  $R_3$  and  $R_5$  are used.

The improvement of Fig. 9 over Fig. 7 stems from the limiting diodes  $D_{1,2}$  between the two oscillator transistors,  $Tr_{1,2}$ . These diodes can be general-purpose 1N4148 small-signal types.

The circuit of Fig. 9 is preferred over Fig. 7 because it is more stable because crystal dissipation is limited, and it offers more reliable cold starting.

The Butler oscillators above are series-mode circuits, but because of the series capacitors, they are able to use parallel-mode crystals. For a strictly series-mode circuit, eliminate the capacitors in series with the crystal and replace them with a short circuit.

#### **Colpitts oscillators**

A feedback network consisting of a tapped capacitive voltage divider characterises the Colpitts oscillator. In Fig.



10 the feedback is provided by  $C_1$  and  $C_2$ , although the situation is somewhat modified by the gate capacitances of  $Tr_1$ . This circuit can be used with parallel mode crystals from about 3 to 20MHz with proper values of  $C_1$  and  $C_2$  as in the table in Fig. 10.

Frequency trimming of the oscillator can be done by shunting a small value trimmer capacitor across the crystal. Alternatively, the trimmer can be placed in series with the crystal.

If the oscillator tends to oscillate parasitically in the VHF region, then try using the snubber resistor method,  $R_4$ in Fig. 10. This could occur because the JFET used at  $Tr_1$  will have sufficient gain at VHF to permit Barkhausen to have his due at some frequency where strays and distributed *LC* elements produce the correct phase shift.

A value between 10 and  $47\Omega$  will usually eliminate the problem. Alternatively, a small ferrite bead can be slipped over the gate terminal of  $Tr_1$ to act as a small value VHF/UHF RF choke.



Figure 11 is the same as Fig. 10, except for two features. First, the active device is an n-channel MOS-FET rather than a JFET. Any of the single-gate devices, such as a *3N128*, can be used, but remember that such MOSFETs are very sensitive to ESD damage.

The other difference is a 1N4148 small-signal diode that shunts the gatesource path to provide a small amount of automatic gain control action. When the signal appearing across the crystal and feedback network is sufficiently large, the diode rectifies the signal and produces a DC bias on the gate that counters the source bias provided by  $R_2$ . This diode helps smooth out amplitude variations, especially when more than one crystal is switched in and out of the circuit.

Another variation on the Colpitts theme is the impedance inverting oscillator circuit of Fig. 12. It provides stability of 10ppm over a wide temperature range of 0°C to 60°C provided that the components are carefully selected. Bear in mind that  $C_{1-3}$  and  $L_1$ are particularly troublesome here.

The circuit will also remain within  $\pm 0.001\%$  over a DC power supply variation of 2:1 - provided the crystal

Fig. 14. Alternative impedanceinverting third-overtone circuit based on the Colpitts oscillator. Again, this circuit works from 15 to 65MHz.

Tr1

2N5770

C4

L1 (0.25in form)

12t, #30, CW

8t, #30, CW

6t, #22, CW

OUTP

V+

C5

0.001µF

1

R3

15k

C4 (pF)

33

33

22

C1 (pF)

100

100

68

Freq (MHz) 15 - 25

25 - 55

50 - 65

C2 (pF)

100

68

33

C3 (pF)

68

47

15

dissipation is not exceeded. Harmonic output of this configuration is typically low.

Frequency of oscillation is set by adjusting inductor  $L_1$ . The turns counts shown in the table in Fig. 12 assume a 6.5mm slug-tuned coil form designed for use in the frequency range 3 to 20MHz. Some experimentation is needed depending on the particular former used. The idea is to set the resonant frequency of the coil and  $C_{1-3}$  combined to something near the crystal frequency.

It is sometimes appealing to add a tuned circuit to the output circuit of oscillators. The harmonics of the oscillator are suppressed when this is done. But in this case, a transistor equivalent of the old-fashioned TGTP oscillator will result because of the action of the output tuned circuit and the  $L_1/C_{1-3}$  combination. Don't do it!

#### **Overtone oscillators**

So far I have only discussed the fundamental oscillating mode. But crystals oscillate at more than one frequency.

The oscillations of a crystal slab are in the form of bulk acoustic waves, or BAWs. These can occur at any frequency that produces an odd halfwavelength of the crystal's physical dimensions, for example  $1\lambda/2$ ,  $3\lambda/2$ ,  $5\lambda/2$ ,  $7\lambda/2$ ,  $9\lambda/2$ , where the fundamental mode is  $1\lambda/2$ .

Note that these frequencies are not harmonics of the fundamental mode. They are actually valid oscillation modes for the crystal slab. The frequencies fall close to, but not directly on, some of the harmonics of the fundamental – which often causes confusion.

The overtone frequency will be marked on the crystal, rather than the fundamental. It is rare to find fundamental mode crystals above 20MHz or so, because their thinness makes them more likely to fracture at low values of power dissipation.

The problem to solve in an overtone oscillator is encouraging oscillation on the correct overtone, while squelching oscillations at the fundamental and undesired overtones. Crystal manufacturers can help with correct methods, but there is still a responsibility on the part of the oscillator designer.

Figure 13 shows a third-overtone Butler oscillator that operates at frequencies between 15 and 65MHz. Inductor  $L_1$  is set to resonate close to the crystal frequency, and is used in part to ensure overtone mode oscillation. If moderate DC supply voltages are used -9 to 12 volts in most cases



Freq (MHz)	C1 (pF)	C2 (pF)	C3 (pF)	L1	L2
65 - 85	15	150	100	7 t, #24, 3/16in. CW	10t #34 over 10Ω 1/4W
85 - 110	10	100	68	4 t, #24, 3/16in. 1WD	10t #34 over 10Ω 1/4W

#### CW = close wound

1WD = spaced 1 wire diameter

- the harmonic content is low, at around -40dB. In addition, stability is at least as good as a similar fundamental mode Butler oscillator.

Figure 14 is a third-overtone impedance inverting Colpitts style oscillator that operates over the 15 to 65MHz range. As in similar circuits, inductor  $L_1$  is tuned to the overtone, and is resonated with  $C_1$ , combined with the capacitances of  $C_2$  and  $C_3$ . Values for  $C_1$  through  $C_3$ , and winding instructions for a 6.5mm low-band VHF coil former are shown on the diagram.

Note the resistor across crystal  $Y_1$ . This resistor tends to snub out oscillations in modes other than the overtone, including the fundamental. Take care not to make  $L_1$  too large, otherwise it will resonate at a lower frequency with  $C_{1.3}$ , forming an oscillator on a frequency not related to either the crystal's fundamental or overtones. The oscillator may well be perfectly happy to think of itself as a series-tuned Clapp oscillator!

Operation of the circuit of Fig. 14 to 110MHz, with fifth or seventh overtone crystals, can be accomplished by modifying this circuit to the form shown in Fig. 15.

#### In summary

The crystal oscillator is probably the best way to obtain a single-frequency source. Crystal oscillators are also used to provide accurate references and time base in such applications as frequency counters and frequency synthesisers.

With proper care and component selection, these circuits can be used to provide a stable, accurate signal.



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#### **Specifications**

Switch position 1 Bandwidth Input resistance Input capacitance Working voltage

Switch position 2 Bandwidth Rise time Input resistance  $1M\Omega$ Input capacitance Compensation range Working voltage DC to 10MHz 1M $\Omega$  – i.e. oscilloscope i/p 40pF+oscilloscope capacitance 600V DC or pk-pk AC

DC to 150MHz 2.4ns  $10M\Omega \pm 1\%$  if oscilloscope i/p is

12pF if oscilloscope i/p is 20pF 10-60pF 600V DC or pk-pk AC

**Switch position 'Ref'** Probe tip grounded via 9MΩ, scope i/p grounded



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# Anti-jitter: new circuits

Neil Downie reveals more details of a brand new building block for removing signal jitter, and presents some example circuits.

he anti-jitter circuit, or AJC, is a simple but novel configuration of circuit elements that has been overlooked until now. It is as fundamental and potentially as useful as time-honoured configurations such as the PLL or the active filter.

Practically all the circuit blocks we use today, from AGCs to PLLs, were developed in the first half of the twentieth century. Pioneers like Alan Blumlein or even Lee de Forest would have little difficulty in recognising most of the basic circuits we use today.

You might be forgiven for thinking that the electronics pioneers in the valve era had tried out every possible combination of fewer than a dozen circuit elements. Not so. Three years ago Professor Mike Underhill of Surrey University was looking for a simple circuit to reduce pulse time jitter or, equivalently, phase noise in communications systems.

New electronics technology such as digital radio and new cellular and satellite radios increasingly needs lower jitter values. Lower jitter would enhance the performance of key elements such as sigma-delta converters and make DSP subsystems better, Mike reasoned.

There were traditional solutions to reduce jitter around. If it is jitter from an oscillator that concerns you, for example, you can use high-Q *LC* combinations or other low-jitter designs. Alternatively, for externally sourced signals, locking onto the incoming signal with a phase-locked loop can reduce jitter.

However, Mike was unhappy with these solutions and their limitations and came up with a much simpler and more direct approach -a circuit to directly reduce jitter.

Mike, Mike Blewett, Thomas Bruchert, staff and students at Surrey and myself at Maran & Co have worked for three years developing AJCs. There is now a number of versions of the AJC concept.

Discussions with semiconductor companies have begun, and it seems likely that commercially produced AJC chips will become available within a year.

#### What is an AJC?

The concept behind the anti-jitter circuit is to generate pulses from an input waveform containing jitter, feed them into an integrator, then pass the result through a comparator. The reconstituted pulses emerge equally spaced, with jitter sidebands reduced by typically 20dB or more – a factor of 10x reduction in time jitter. The core of circuits adopting the AJC approach is shown in Fig. 1.

Note that there is no oscillator in this circuit. The output signal derives directly from the input, having been governed to the average input frequency by the action of the integrator and comparator.

The output can track the input over wide frequency deviations – around 3:1 to 10:1 with many simple designs. By making the monostable time constants track the input frequency to some extent, even wider ranges of frequency can be followed. The output can even track instantaneous frequency jumps up to a factor of two or so, as well as jitter values up to 150° in phase.

DC removal is required to keep the integrator circuit within the circuit voltage limits such as supply rails. Although this can increase the time needed for the circuit to begin func-



Fig. 1. Basic anti-jitter circuit – note the absence of an oscillator. Fig. 2. Basic functional blocks of the AJC, a). Waveform b) shows jitter on the output from the input monostable. Sawtooth c) is output from the integrator, op2, and comparator switching level, op3, together.



tioning at switch on, there are ways to avoid this, as discussed later.

Note how the circuit can easily be cascaded. If 25dB jitter suppression is insufficient in an application, connecting two AJCs in series will yield about 50dB. In some applications, perhaps, three or more AJCs in series might be used, although there is an ultimate noise floor, below which AJCs will not reduce noise.

Finally, the AJC is also a 'drop-in' separate circuit block which can be added to existing designs in a simple way. In an existing circuit with a jitter problem, an AJC can – conceptually at least – be soldered in across a cut track.

#### Basic action of the AJC

Figure 2a) reveals the basic operation of the AJC.

In the absence of a pulse, the charge on the integrator capacitor simply leaks away at a constant rate, the waveform sloping gently downward. As the same size pulses come in they push the integrator capacitor up by the same amount.

However, if a pulse arrives early, then that increment in charge builds on a higher base, and pushes the next downward slope to a higher point. Intriguingly though, that new downward slope, although it starts earlier and is longer, is actually coincident with the slope that would have occurred had the pulse arrived at the right time.

Think of the gentle sloping sides of the sawtooth as the sliding tubes of a trombone, and the pulse upward increment as the handle. This should give you an idea of how the waveform changes with different pulses arriving on an oscilloscope display.

Now the fact that the downward slopes are all in the same place means that a comparator placed between the sawtooth waveform and a reference can trigger output pulses at regular time intervals – i.e. without jitter. More picturesquely, the horizontal reference line always cuts the trombone tubes in the same place, even though the handle has moved.

## Simple AJC demonstration circuit

The block diagram of Fig. 1 can be implemented directly to make a practical AJC circuit. The demonstration circuit of Fig. 3 shows the principles of the AJC using only common lowfrequency glue logic circuits, and shows clearly the straightforward nature of AJC action.

For simplicity, a 4528 monostable wired to give a 200ns pulse is used for both input and output pulse shaping. The CA3140 single supply CMOS operational amplifier is used for the integrator, with the LM311 comparator comparing the integrator output with a half  $V_{cc}$  reference. Voltage  $V_{cc}$  is conveniently a 9V battery.

To show the action of the circuit, a jittered input of 100kHz-300kHz is required. An FM signal generator can be used, or a VCO such as a 4046. Alternatively a pair of multivibrator circuits such as 555s could be wired up. The input should be large enough – 5V or so – to trigger the 4528 monostable on the input.

Some elementary considerations apply to viewing the produced waveforms on an oscilloscope. Triggering on the input pulses, as given by the input monostable, and looking at the jitter on the next pulse(s) shows the jitter on the input signal.

Triggering on the output pulses and looking at the jitter on the next pulse(s) on the display shows the jitter on the output signal. Alternatively, the input and output frequency spectra can be compared.

At these low frequencies, no partic-



Fig. 3. Low-speed anti-jitter demonstration circuit. This configuration is useful from 100 to 300kHz. ular care is required over the construction of the circuit. A printed wiring board is not required, and because of the slow rise time of the low speed CMOS logic circuits, no radio-frequency or power supply precautions are necessary other than the decoupling capacitors indicated. Furthermore, standard oscilloscope and spectrum analyser probes can be used without disturbing the action of the circuit too much.

Figure 4 shows oscilloscope measurements of the integrator waveform at the top, with the input, 4a), and output, 4b), pulses below. Measurements were taken using a Tektronix TDS210 storage scope.

#### **AJC refinements**

For high-frequency operation, a variant called the 'adiabatic AJC' can be used. Here, the AJC integrator block is replaced by a diode/capacitor energy storage circuit, which is entirely passive: all its energy derives from the driving circuit.

The energy-conserving nature of this part of the circuit has led to it being dubbed an 'adiabatic AJC'. In this, a charging circuit pushes pulses of charge an integrator capacitor, while the charge on the capacitor is continuously leaked away.

#### The cup-and-leaky-bucket integra-

tor. For high-frequency operation, a true integrator operation is difficult to achieve. A circuit that is faster and also simpler is what might be dubbed the 'cup-and bucket' integrator. In this, the input is arranged to transfer 'cups' of a small standard charge to the 'bucket' (integrator capacitor), the charge being leaked away continuously by a constant current source.

The cup part of the circuit could be a diode pump or a grounded-base transistor stage. The constant current source could be a transistor mirror, or,



Fig. 4. Actual output from the anti-jitter demonstration circuit of Fig. 3. In each display shot, the upper waveform is integrator output. In the shot on the left, a), the pulses are the input while in the one on the right, b), the pulses represent output.



more simply, a FET with grounded gate, Fig. 5.

In a further refinement, using the FET current leak, a resistor and capacitor connected to the FET gate provide the DC subtract function as well.

**Tracking large frequency changes.** The 'lock on' time of an AJC – how long it takes to get pulses out – is not limited by the slewing of a voltagecontrolled oscillator output frequency, as a phase-locked loop jitter reduction system might be. In the AJC, signals flow directly through the circuit and thus the 'lock on' time is often just a fraction of an input pulse. However, on power up, and with large changes in frequency, the DC-subtract circuit needs charging up to operational voltage. This can be speeded up by the addition of diodes around the resistor, as shown on the simulation circuit below.

With these additions, it is often found that the AJC will not lose a single pulse during frequency switches – an important advantage in communications sys-

circuit for higher 5V frequency AJCs operating to 33 ≥1.0k 10MHz. BC557B 2N2904 1.2N 74HCT00 74HCT00 SN7400 1.0M 1.0n 82.0p 1 0k Output BSN10 1N3492 2N6755 560.0 330 BAW62 100n 56.0p 100r 22n 4.7n 47 56p 470 5 47.0n

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Fig. 6. Simulation

tems such as cellular radio where rapid switching is an absolute requirement. Be aware though that jitter suppression is reduced during a frequency switch: clearly it is a logical impossibility to reduce jitter to zero during switching unless the circuit had prior knowledge that the switch was coming.

In practice, jitter suppression may be reduced to only 10dB or so, with full 20-30dB jitter suppression reappearing after a time constant set by the circuit's DC subtraction.

The logic-gate AJC. The logic-gate AJC is the latest development, and will allow the widespread adoption of AJCs. As announced at the recent Besancon EFTF/FCS Conference, the new AJC design uses only straightforward logic gates for its active components.

This most recent step in the development of the AJC replaces another part of the block diagram of the conceptual AJC: the comparator output circuit. At high speed, true comparator circuits are relatively unusual on large, otherwise digital chips, and somewhat difficult, being an analogue technology.

In the AJC, the comparator can be replaced by using the preset logic threshold of a standard logic gate as the 'reference input', the logic gate input being the signal input, in the language of the comparator. Note that the AC coupling into the comparator needs to have a time constant longer by a factor of ten or so than the closest-in jitter sideband that needs to be suppressed. At the same time, it should not appreciably load the integrator.

The latest refinement of the AJC makes it simpler to implement, especially in IC technology, and especially when the AJC needs to be incorporated in a larger IC using standard cells, which often do not include a differential comparator function.

There's a number of other AJC variants for which there is insufficient space in this article. For example, the AJC can be used in a different mode where the input frequency is doubled before the first monostable, and then divided by two on the output. This gives some important facilities, such as the capability to de-jitter both leading and trailing edge of an input waveform, and can give a 'quieter' sawtooth waveform at the integrator.

We expect to uncover yet more versions of the AJC.

## Higher-speed demonstration circuits

The discrete higher-speed demonstration circuit is intended for demonstration only. But with a little further tweaking it could find practical application in digital systems at up to around 10MHz.

The AJC is certainly capable of much higher speed than this, however. The simulation described below shows operation up to 50MHz with discrete component values, and 5GHz with micrometre-sized IC components, showing the kind of performance IC implementations of the AJC will have.

1-10MHz logic-gate demonstration circuit. Still under development, this circuit illustrates some of the latest AJC design principles described above. Note that because of its higher operating frequency this circuit is sensitive to layout, can both emit and receive spurious signals, and is somewhat sensitive to oscilloscope probing, Fig. 6.

As explained earlier, the high-speed comparator action needed is supplied by means of a logic gate circuit, which is simpler and faster than a genuine comparator.

Note that the gate is connected to the

Need more information?

Contact Dr Neil Downie, Maran & Co Ltd, via fax on +44 (0)1483 302112 or via e-mail using <u>n.downie@maran.co.uk</u> for the latest information. Other sources of AJC information are: 'Jitter Buster,' *Electronics World*, June 1999 p. 516.

- 'The Adiabatic AJC Circuit,' MJ Underhill, European Frequency Time Forum (EFTF) Frequency Control Symposium (FCS) Conference, Besancon 1999.
- 'The anti-jitter circuit for low spurious DDS square waves and low cost fractional-N synthesis,' MJ Underhill, S Stavrou, M Blewett, N Downie, European Frequency Time Forum, Warsaw, 1998.

 'Performance assessment of a delay compensation phase noise and time jitter reduction method,' MJ Underhill, M Blewett, European Frequency Time Forum, Neuchatel, 1997.
 'Spectral improvement of direct digital frequency synthesizers and other frequency sources,' MJ Underhill, M Blewett, European Frequency Time Forum, Brighton, 1996. power supply rails via by-passed current-limiting resistors. Although these limit the output voltage swing to 2V or so, they avoid any possible excess current flow in the gate. Here, the gate is being used as a quasi-analogue device so it could conduct strongly at certain input voltages and overheat.

As before the integrator is provided by the cup-and-leaky-bucket approach. The p-n-p transistor here forms the 'cup' part of the circuit, while the current source 'leak' is provided by the MOSFET. Finally, note the use of logic gates to form simple short-pulse monostables.

**50MHz simulated circuit.** This circuit can be easily modelled in any Spicebased analogue circuit simulator. Many AJC circuits can easily be modelled. However, in using simulators, it is important not to use time constants that are too long in DC subtract.

It may also help to preset node voltages to the values to near their final settling values, once you have found out what those are. Although a second may not be long to wait with a real circuit on an oscilloscope, simulating 50 million cycles on the average PC-based simulator will require serious patience, to say the least!

The version below assumes a transistor of beta of  $0.5 \text{mA/V}^2$ , gate capacitances around 0.5 pF and threshold 0 V. Other values of these parameters will work too. The diodes must be high-speed, low-capacitance devices.

In practice, it may be difficult to make the circuit work because of the effects of stray capacitance and inductance and the effect of extended connecting wires in discrete circuits.

Figure 7a) shows the circuit, while diagram 7b) gives the printout from the SPICE-based TINA simulator, showing rapid 0.5µs lock-on of this simple circuit.

Removing jitter up to 5GHz. With the components shown, the circuit achieves around 50MHz. However, with components and stray capacitance values of the range normally encountered on submicron high speed IC circuits, the same simulator model can be made to run as high as 5GHz.

We expect that early IC versions of the AJC will not run quite this fast, but IC versions will run faster than the discrete circuits given above – certainly in the hundreds of megahertz. Such circuits could also form functional blocks within a much larger IC, for example,
one of the ICs in a cellular or broadcast radio chip set.

#### Who needs an AJC?

Anti-jitter circuits are not merely a laboratory curiosity. At least a dozen applications for the AJC are currently being explored. No doubt, more will occur to people as knowledge of the technology spreads.

The most obvious uses for AJCs involve the reduction of jitter in systems, where it occurs. The output of direct digital synthesisers for example typically contains significant spurious sideband components. Normally these are dealt with by spreading the sideband power over a wider band, the socalled 'noise spreading direct digital synthesiser'. However, an AJC would suppress jitter, eliminating the sidebands entirely, and giving a lower noise overall system.

Similarly, simply adding an AJC to a phase-locked loop may well turn out to be a popular application. A PLL with a wide bandwidth is easy to design and has the desirable properties of rapid lock and a large lock-in range. However, it has the less desirable property of a high jitter output.

The PLL used for locking CRT displays is a potential user of this approach: the AJC may allow very large displays to avoid completely the tendency to have 'crawling lines' down the edge of the screen.

#### Why not add some jitter?

Although many AJC applications will simply be to reduce jitter in an existing system, others will revolve around the concept of putting jitter deliberately into a system to obtain other advantages, and then using the AJC to get it out again.

The seasoned electronic engineers among you might observe that the noise-spreading algorithm used in direct digital synthesis follows a similar philosophy. An example will illustrate: consider the PLL-based frequency synthesiser of Fig. 8.

If it is a good one, the VCO will produce little output jitter, and the divider chain will further reduce any residual jitter. The relative time jitter is divided by two when a waveform is divided by two in frequency.

The phase comparator compares the reference with the divided waveform and outputs a signal via the loop filter to move the VCO either up or down in frequency. This locks the VCO output to the reference. All this is a standard PLL frequency synthesiser.

However, now consider the addition of the two blocks marked 'Pulse removal' and 'Fractional rate multiplier'. When it receives a signal from the rate multiplier, the pulse subtractor divides by 10 instead of 11, or simply blocks a single pulse.

Clearly, the new waveform is now just a fraction lower in average frequency. However, it also has a very high degree of jitter. The divide-by- $N_p$  circuit reduces this, but it does not not eliminate it.

Jitter penetrates the phase comparator and imposes a small variation on the loop-filter output. This results in the VCO having a small but highly undesirable frequency modulation. The addition of the AJC as shown allows this circuit to perform much better.

There are other circumstances where the ability to use circuits that add jitter can be useful. One example is clock restoration. On noisy lines, where a clock signal must be extracted, extra interference pulses may be present, or pulses may be missing. In this case, a pulse subtractor or pulse inserter may be used to correct the waveform.

Normally, such a situation is impossible, because the added pulses are too late, or the removed pulses are the wrong ones – the ones after the one that should have been removed. These problems raise the average jitter on the clock signal too much. With the AJC though, such circuits are practicable.

#### Other applications for AJCs

Anti-jitter circuit are likely be used in communications, for the main part. But there could be other significant application areas.

In high-quality oversampled digital audio systems for example, there may be a case for using an AJC to dejitter/retime the data. This would max-



FET is 300µA/VV, threshold 0V op1 and op2 feed a high-speed comparator



imise the additional quality given by the oversampling and extrapolation circuits.

Similarly, complex multiphase clock circuits used on modern microprocessors could benefit from AJCs. A development of the AJC employs multiple comparators, which generate multiphase signals in a very natural and versatile way.

There may even be applications of the AJC that do not involve jitter. Mike Underhill observes, for example, that the DC subtract loop of the AJC can be modified so that it constitutes an FM/FSK demodulator.

Can you think of other AJC applications?

Note that the AJC and variants are covered by a number of patents and patent applications. Manufacture of AJC ICs or other uses of the AJC on a commercial scale may require a licence. Contact Maran & Co for details. Fig. 7. Dejittering at up to 50MHz. This circuit simulation, a), works well, and locks in rapidly, as the plot in b) shows. This circuit will be difficult to implement though because of wiring inductance and stray capacitance.

(b)



Fig. 8. Adding an anti-jitter circuit to a frequency synthesiser removes jitter cause by the action of the pulse remover removing a pulse.



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# Hands-on Internet

All-pass filters, instrumentation amplifiers, simulated inductors and single-wire bidirectional communications links are among applications that benefit from transconductance op-amps, as Cyril Bateman has been finding out.

n the last issue of *Electronics World*, I mentioned a slightly unusual circuit function, the Norton current input amplifier, introduced by National in 1972. This month I take a look at circuits using an even earlier unusual technique – the transconductance op-amp, introduced in 1969.

I recall eagerly buying a *CA3080*, one of the first commercially available transconductance amplifiers, which I still have kept for posterity.

This early version was soon followed by improved versions. The most notable of these were the CA3094, which increased peak output current capacity to 300mA, and the *LM13600*, a dual transconductance amplifier.

#### What is an OTA?

A transconductance amplifier converts its input voltage into an output current proportional to the voltage difference at its differential input terminals, Fig. 1.

Traditionally, transconductance amplifiers have been used in gain-control circuits, modulators, multiplexers, multipliers, voltage-controlled oscillators and sampling circuits. These applications and many more for the *CA3080*, can be found in AN6668 from Harris Semiconductor, which is available for downloading.<sup>2</sup>

Two other Harris notes concentrate on applications that make use of the increased current output available from the CA3094. Note AN6077 details how to use the *CA3094*, together with three transistors to build a complete 12W audio amplifier. This design is provided with bass and treble tone controls located in the amplifier's feedback loops. A companion RIAA preamplifier based on the *CA3080* amplifier is also detailed.<sup>2</sup>

**Class-A instrumentation amplifier** One especially useful aspect of the transconductance amplifier is its ability to produce a class-A instrumentation amplifier. Its differential voltage-input signal is converted to a single-ended output.

Obviously this can also be done using an off the shelf instrument amplifier, or the usual discrete three op-amp circuits.

#### COMMUNICATIONS



Fig. 1. Basic structure of the CA3080 transconductance amplifier. Differential input voltage results in an output current that can be scaled as needed.



Fig. 2. Classical three amplifier in-amp requires precision matched resistors. A transconductance amplifier provides similar differential to single ended conversion but without needing precision resistors.

#### Y2K\_Bugs

The recent conflict in Kosovo demonstrated the important role played by the US military Global Positioning System. On 22 August a very different GPS civil role was also tested, perhaps the very first world wide trial in the countdown to the Millennium Bug, will have commenced.

The GPS navigation system relies on a precision clock which is used to calculate your position. This clock introduces its own particular version of the Millennium Bug consequently the GPS system



But these designs involving three opamps need accurately matched feedback resistor networks to provide acceptable common-mode rejection.

Gain of the transconductance amplifier's preamplifier section can be changed by altering its transconductance and load resistance. As a result, no matched resistor networks are needed, Fig. 2. It was this particular attribute that I choose to investigate using Internet. I was searching for a circuit that I could use in a balanced input probe for my oscilloscope. In the process, I found several other interesting transconductance applications.

# OTA fast enough for a 100MHz scope probe?

Many commercial instrument amplifiers provide excellent performance at low frequencies, but I wanted to avoid restricting my scope's 100MHz capability.

Prior to searching the Internet, I already had one particular integrated circuit in mind. Analog Devices produces a high-speed video difference amplifier. Known as the *AD830*, it has a unity-gain bandwidth of 100MHz.<sup>3</sup> It combines a common mode rejection of 60dB at 4MHz with minimal video differential gain and phase errors.

This chip performs excellently as a high-speed differential amplifier up to

10MHz, Fig. 3. Could this limit be bettered without too much design effort?

During my searches I came across two other especially intriguing integrated circuits. One was from Maxim,<sup>4</sup> the other from Burr-Brown.<sup>5</sup> These opened up many new design possibilities.

Maxim provides two similar wideband transconductance amplifiers, both having true-differential and fully-symmetrical inputs with relatively high impedance. Their unique architecture provides accurate gain without needing feedback, eliminating closed-loop phase shifts. Closed-loop phase shift is a primary cause of circuit oscillation in conventional high-speed amplifiers.

# Unity gain bandwidth of 275MHz

The MAX435 has a unity gain bandwidth of 275MHz and provides both differential inputs and outputs. Its companion, the MAX436, has single ended output and a 200MHz unity-gain bandwidth.

Both offer  $800V/\mu s$  slew rates and a 1% settling time of 18ns to a 0.5V step input. This performance is accompanied by a common mode rejection of 53dB at 10MHz and a  $300\mu V$  DC offset voltage.

While these characteristics indicate an excellent high frequency perfor-

has to survive a double whammy, 21 August and 31 December.

For technical reasons, the GPS system time counts in weeks from 6 May 1980, the 1023rd week ends on 21 August. On 22 August the week count 'rolls-over' from 1023 to restart at 0. As with the year 2000 date change, some receivers and ground equipment will exhibit rollover problems in August, with consequent positional errors.

This End of Week roll-over has a second perhaps more significant bearing on everyone. You may not need or use a GPS system yourself, but many commercial

Fig. A. The Global Positioning System provides its own unique Y2K date bug, called End of Week roll-over, which repeats every 20 years. Many nonmilitary time clocks depend on the GPS atomic reference for time stamping, but will they be affected ? institutions make use of its extremely precise global clock.

Some US banks use this clock to control their time locks, and to calculate the interest payable on international money transactions. Very fast digital networks, including Internet, can use this external clock to synchronise data transmissions. In the US, considerable fears have also been expressed concerning its use in electricity supply, switching control and power distribution.

Considerable data on the EOW roll over and its possible US implications can be found on Internet, but my searches revealed almost no details for other countries.

The US military performed its largest ever Y2K trial in April. This included all military uses for the GPS systems.<sup>1</sup> While these systems now claim compliance, the detailed test results are not yet publicly available, Fig. A.

#### COMMUNICATIONS

mance, both designs have a unique gain-control characteristic, which is even more interesting. Their gain is set by the ratio of two impedances and an internally set current gain factor, K.

The gain of many conventional instrument-amplifiers is set via the value of a resistor between two gain setting inputs. Gain of the MAX435 and MAX436 can also be set using a similar resistor. Amazingly though, both integrated amplifiers can also accept a complex impedance, rather than just a simple gain setting resistor. This is possible because their transconductance network's impedance has no interaction with output load impedance.

This complex impedance can be a series resistor and capacitor between the gain setting inputs. In this case the amplifier has a high-pass characteristic. The low corner frequency depends on the resistor and capacitor values. Adding a parallel capacitor resistor combination to ground at the amplifier's output then produces a band-pass amplifier.

Since no overall feedback is needed to control gain and ensure stability, these amplifiers can safely drive a highcapacitance load. Having no feedback network, the usual feedback phase shifts cannot occur, so the circuit remains stable.

The main effect of capacitive loading is a reduction in slew rate and output bandwidth, hence the low-pass amplifier characteristic.

# Changing the OTA's characteristics

In similar fashion a series capacitor/inductor combination can be used between the gain setting inputs. This provides a sharply tuned amplifier



Fig. 3. The AD830, is a high-speed video differencing amplifier providing 60dB common mode rejection at 4MHz with minimal gain and phase errors.

Where to surf

- 1. GPS systems achieve Y2K compliance
- 2. Harris Corporation
- 3. Analog Devices Inc
- 4. Maxim Integrated Products
- 5. Burr-Brown Corporation

whose resonant frequency is determined by the capacitor and inductor values.

Such an arrangement is especially useful in a differential input, tuned selective amplifier. The tuned circuit is placed as near as possible to the amplifier inputs, rejecting unwanted signals and noise. Using a conventional instrument-amplifier, several stages of broadband amplification precede any tuning circuits, reducing circuit performance http://www.cpf.navy.mil/ y2k/y2knews/y2kgps.htm http://www.harris.com http://www.analog.com http://www.maxim-ic.com http://www.burr-brown.com

when subject to out of band signals.

Most surprising of all, to increase the Q of a tuned amplifier, the MAX 435 and 436 can even be used with a crystal connected between their gain setting inputs. The data sheet shows the measured performance of a MAX436 tuned amplifier with a 25MHz crystal. The circuit produced a narrow gain peak of more than 40dB, while driving a 25 $\Omega$  load. This load can be a doubly terminated 50 $\Omega$  coaxial cable.

Video over a 5km twisted pair The final data-sheet application shows a 435 and 436 being used to transmit a single baseband video channel over a





 $Q = \sqrt{L/C} = 1/(R_1//R_2)$ 

Fig. 4. Using two MAX436 transconductance amplifiers to synthesise a 1.25mH inductor provides a DC accurate 3.2kHz notch filter. twisted-pair wire. Using these two amplifiers, good quality video can be transmitted up to 5km with a considerable cost saving compared to using coaxial cables. Maxim application notes, available from the company's web page, provide a further five applications which use the unique properties of these chips. Three of these applications use *MAX436* amplifiers to simulate inductors, providing freedom from EMI and improved circuit performance. These can all be quickly downloaded as small PDF files.



OV-

A DC accurate notch filter circuit is described in application note A2013.PDF. By separating the DC and AC paths, this circuit avoids using opamps in the DC path, making it free from DC offsets and gain errors.

The AC path uses a capacitor in series with a simulated inductor to ground. This simulated inductor is formed using two transconductance amplifiers, Fig. 4.

#### Simulating inductance

A 3.2kHz third-order high pass filter using two 436 op-amps to simulate a 1.25mH inductor is detailed in A1315.PDF. This filter attains a slope of 58.6dB per decade – very close to the theoretical 60dB slope of a perfect filter.

Achieving similar performance in a passive filter could prove difficult. A practical inductor of this value has significant ESR and its inductance falls at low frequencies.

Application note A1616.PDF describes a 50 $\Omega$  output 9.3MHz sinewave *LC* oscillator with 1% distortion, produced using a single 436.

While these are interesting application circuits, two others particularly caught my eye. Some time ago a reader asked for a circuit that could generate a 90° phase shift at moderate audio frequencies. Providing this phase shift at a discrete frequency is easy, but much more difficult with dynamic and mixed frequencies.

Application note A1610.PDF illustrates such a circuit. As presented it is intended for higher frequencies, but it can be re-scaled for audio frequencies. These transconductance amplifiers provide a current output. As a result, simply tying their output terminals together into a single resistor, Fig. 5, can sum the outputs from two or more amplifiers.

This application uses two transconductance amplifier pairs to form an allpass network. Each pair comprises one amplifier with a resistor between its gain setting terminals, the second having a capacitor between these terminals. Both amplifier outputs are then summed using a common output resistor.

By choosing appropriate corner fre-

quencies, one amplifier pair generates the cosine of the input waveform while the second pair generates the sine of the input, producing the desired 90° phase shift. It can be used with dynamic signals covering three octaves.

## Bidirectional drive over coaxial cable

The last application note was the most interesting. Entitled 'WTAs provide wideband, bidirectional drive for coaxial cable', it describes four 436s in a circuit arrangement similar to that used in telephone systems. It is able to send signals in two directions simultaneously on the one cable, Fig. 6.

In this case the cable is coaxial. Signals from audio up to RF can be transmitted in both directions at the same time. Using these high-speed transconductance amplifiers with 1% resistors produces around 30dB of cancellation of the unwanted signals on either output.

In my next piece, I will be looking at the versatile and interesting high speed 'diamond' transistor circuit from Burr-Brown.

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# SVGA GENERATOR

Roy Harding's VGA and SVGA test generator uses a PIC variant that's so fast that it is capable of producing the test signal without any external timing circuitry, making the hardware side easy to implement.

s an electronics design engineer in the computer industry, I often get asked by friends and relatives to check or repair computers and monitors. If someone arrives with just a monitor for checking this involves wiring up a PC with a keyboard and mouse, then loading software and waiting while the whole thing boots-up.

The addition of a computer also takes up valuable workspace if one is working in a confined area. There are a few SVGA generators already available on the market, but the cost of these can only be justified if you are doing servicing or repairs full time, rather than as a favour.

Last year I was introduced to a new microcontroller from Scenix. This micro uses a combination of PIC code with additional instructions to enhance performance.

The device can operate up to 50MHz. It has a turbo setting to cancel the clock's internal divide-by-four, as found in PICs. This gives you 50MIPS performance, coupled with 2048 bytes of E2 flash memory, an eight-level stack and easy page switching. There's also 30mA source/sink capability on the I/O pins, which makes the device very useful.

As this micro works so fast, I thought of the idea of using it to create a video

Fig. 1. Timings for a VGA signal's frame and line sync pulses.

Table 1. Forms of the signals needed to drivean SVGA monitor.

Vertical sync	5V TTL, negative going
Horizontal sync	5V TTL, negative going
Red	1V analogue signal, positive going
Green	1V analogue signal, positive going
Blue	1 V analogue signal, positive going

generator that could work up to high resolutions. The generator described will generate standard VGA signals at 640 by 480 pixels and popular SVGA displays of 800 by 600 and 1024 by 768, all at 60Hz frame rate.

#### How it works

As already mentioned, the micro is the basic building block for the complete design, only a handful of additional parts being required to complete the implementation. All timings are created in software by the microprocessor using an external 40MHz-oscillator clock IC.

Although a crystal and capacitors can be used for the oscillator circuit I have found crystals over 30MHz difficult to obtain. A voltage regulator and a few LEDs are the only additional semiconductors.

My PCB has two buttons, a power connector, a 15-way video connector and a few resistors and capacitors to complete the component count.

The LEDs indicate the display resolution setting, as it is not obvious from



the monitor display which resolution is being used. Also, if the monitor is not capable of displaying SVGA you will possibly be looking at a black screen.

Although the design can run on batteries and tags are provided on my PCB, I use a ready available 9V mains adapter. After all, you need the mains to power the monitor anyway and batteries have a habit of going flat just when you need them.

There are five signal lines used to drive a standard video monitor, as in Table 1. There are also ground returns for all these signals at the connector.

An example of the timings for a VGA signal is shown in Fig 1. Vertical and horizontal sync signals are driven directly from the microprocessor. The RGB analogue signals are attenuated by a resistor divider network to give a maximum of 1V output into a  $75\Omega$ load.

#### Software

Power P7

The whole design revolves around software running on the Scenix microprocessor

Timings for the functions are critical. Each scan line must be balanced to within a couple of instructions or tearing of the image will result.

Button presses are checked at the beginning of each frame and a software trap waits for the button to be released for the changes to take place.

The first button changes the displayed output and the second button changes the resolution. Each button press changes the parameters of the main loop which are present in a software table.

The complete code is shown in List 1. Note that a special Parallax serial programming adapter is required to program the Scenix parts.

On my PCB, the programmer plugs directly onto the four-way connector next to the micro and the crystal oscillator link removed while programming, Fig 2.

#### Implementing the design

The unit can be housed in a twopiece plastic moulding with built-in mounting posts for the PCB. All parts can be mounted directly on the board and no wiring needs to be involved in the construction.

As the unit is based on a crystal



Fig. 2. On my prototype PCB, the programmer plugs directly on to a four-way connector next to the microcontroller. The crystal oscillator link is removed while programming.

clock, no set-up procedure or calibration is required. I estimate only a two to three hour construction time if all parts are available. This will of course be extended if you decide to produce your own printed circuit board.

You may socket the microprocessor, but it can be reprogrammed on board making removal unnecessary.

The mains adapter can be regulated or unregulated, 9-12V at 300-500mA. Test the unit by connecting a VGA or SVGA monitor to the output and switching on the unit. The generator will default to colour bars in standard VGA mode of 640\*480. Pressing the buttons should change patterns and resolutions.

Implementation of the SVGA generator is kept simple since all the timings necessary to produce the SVGA test signal



 Components

 Resistors
 1/8 watt 5% carbon film:

 R<sub>1,2,3</sub>
 220

 R<sub>4,5,6</sub>
 10k

 R<sub>7,8,9</sub>
 150

 R<sub>10,11,12</sub>
 75

D <sub>1,2,3</sub>	3mm red leds
B <sub>1,2</sub>	vertical push switch
P <sub>1</sub>	4 way 0.1 pitch pins
J <sub>2</sub>	2 way 0.1 pitch pins + jumper
L is 15.	way min D-type 90° Maplin part

- J<sub>1</sub> is 15-way min D-type 90°, Maplin part JW85G. Connector P<sub>7</sub> is a 3.5mm power connector from Farnell, part 224-959.
- IC<sub>1</sub> is a 40MHz CMOS or universal oscillator 8-pin or 14-pin, Farnell 704-738 for example
- IC<sub>2</sub> is the Scenix SX18/AC/DP processor, 18-pin version
- IC<sub>3</sub> is a 7805 5V positive regulator

Suggested case, Farnell part 250-030. Mains adapter, 9-12V 300mA from CPC. Approximate build cost £20 plus mains adapter.

# New circuit board service from Quickroute

Electronics CAD specialist Quickroute, in conjunction *Electronics World*, is offering a new printed circuit board service to readers of *Electronics World*.

You can obtain single-sided boards based on Roy's original design direct from Quickroute for a fully inclusive price of £14.69. To order, fax your credit card number and expiry date together with the cardholder's address to 0161 4760505. Alternatively, ring Quickroute on 0161 4760202. If you wish to order by post, write to Quickroute at Regent House, Heaton Lane, Stockport SK4 1BS and send a postal order or cheque payable to Quickroute Systems Ltd.

Overseas readers should contact Quickroute before ordering for details of postage.

Alternatively, you can obtain a disk of the PCB layout in Quickroute form by sending £12.50 via postal order or cheque payable to Reed Business Information to SVGA, Electronics World, Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS.

#### Need a programmed controller?

All parts, pre-programmed chips and software on disk can be obtained from the author by sending an SAE marked 'SVGA software' to the Quadrant House address above for details.

#### A word of warning

If you try to run a monitor on a resolution that it is not capable of displaying, it is possible to cause damage to its internal circuitry. Therefore, if the display fails to appear on an increased resolution within a few seconds, switch back immediately to a lower resolution. I used a self-adhesive label on the front panel to make the unit more professional. The artwork was done on a PC and printed out on a colour ink jet printer using glossy self-adhesive paper.

List 1. Co	mplete soft	ware listing	for the SVG	A generato	or.
•	VGA & S	VGA Displa	у		
4 9	colour bar	and crossha	tch screen dis	plays, by C	R Harding
		s for 40MHz	crystal. Finis	shed version	1.01
	frame sync				
port bit 6					
port bit 5					
port bit 4					
port bit 3					
port bit 1					
port bit 0	Button2				
		device			,oschs,turbo
		device		ionx,protect	1
		id	CRH SV	GA'	
		reset	start		
ount	da	org 8			
count	ds ds	1			
oort		1			
emp empl	ds ds	1			
emp1	ds	1			
emp3	ds	1			
attern	ds				
lag	ds		;10h		
es	ds	1			
olour	ds				
11	ds	1			
12	ds	1			
3	ds	1			
[4	ds	1			
[5	ds	1			
6	ds		;18h		
F7	ds				
8	ds				
<sup>19</sup>	ds	1			
10	ds	1			
	ds	1			
C12 C13	ds ds	1			
113 114	ds ds				
	43	org 100h			
tart	;setup port	-			
	toorne beer	mov	!rb,#%000	00011	port B 6 out 2 in
		mov	!ra,#%000		port A all out
		mov	port,#255		
		mov	pattern,#0		;colour bars
		mov	res,#0		;vga
nainloop					
		mov	flag,#0		reset interupt flag
		cje	res,#0,vga	-	
		cje	res,#1,svg		
	1640+400	cje	res,#2,svg	az;svga2	
ga	;640*480		T1 #5	Enert	rah dalay
		mov	T1,#5	Front po	c width 3.6uS
		mov	T2,#26 T3,#30		ank lines start
		mov	T4,#12		ank lines end
		mov	T5,#32		ar width delay 26
		mov	T6,#160		of lines(*3)
		mov	T7,#2		of lines in fsync
		mov	T8,#97		y length 28uS
		mov	T9,#30	;chequer	
		mov	T10,#8	chequer	
		mov	T11,#59	;crosshate	ch lines
		mov	T12,#9	;chequer	delay
		mov	T13,#16		
		mov	T14,#10		
		mov	ra,#%0000	0011	;led 3
		jmp	frameloop		
vgal	;800*600 ;	37880hz			
		mov	T1,#4	Front po	-
		mov	T2,#23		c width 3.2us
		mov	T3,#24 T4,#8	;Blank lir ;Blank lir	
		mov			es end Continued on pag

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#### **INSTRUMENTATION & TEST**

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imp         frameloop         r3         cult         redue           ivga2         ;1024.768         cult         redue         temp2.76         160 vga           mov         T3,474         ;Blank lines start         r4         temp2.76         160 vga           mov         T3,474         ;Blank lines start         r4         cult         reduie           mov         T3,479         ;Colour bar width dalay 15         mov         reduie         temp,76           mov         T3,479         ;Colour bar width dalay 15         mov         firmeloop         firmeloop           mov         T1,4147         ;crosshatch lines         jubrouines lower half of page         opr1,446 (0111111           mov         T1,447         ;crosshatch lines         mov         reduie         opr1,446 (000000           mov         T1,447         ;crosshatch lines         mov         reduie         opr1,446 (0000000	200 svga
svga2       ;1024,768       call       refine         mov       T1,477       ibne sync width 2us       mov       temp2,76       ;160 vga         mov       T3,474       iblank lines surt       r4       rdine       refine         mov       T3,474       iblank lines surt       r4       rdine       refine         mov       T3,474       iblank lines surt       r4       rdine       refine         mov       T3,474       iblank lines surt       rdine       rdine       rdine       rdine         mov       T3,474       iblank lines surt       rdine       rdine       rdine       rdine         mov       T3,474       iblank lines surt       rdine       rdine       rdine       rdine         mov       T3,474       iblank lines surt       rdine       rdine       rdine       rdine         mov       T1,474       ichequer suras       gabrouines lower half of page       org 0       roit#K 10111111       rdine       rdine <td></td>	
mov     T1,47     iFrom porchalizy     mov     temp2,45       mov     T2,413     illank inces start     r4     r4       mov     T3,424     illank inces start     r4     redline       mov     T3,424     illank inces start     r4     redline       mov     T6,455     illansk inces start     r4     redline       mov     T6,456     illansk inces start     r4     redline       mov     T6,456     illansk inces start     redline     redline       mov     T6,456     illansk inces start     redline     redline       mov     T6,456     illansk inces start     redline     redline       mov     T6,457     illansk inces start     redline     redline       mov     T0,476     illansk inces start     redline     redline       mov     T1,447     crosshatch lines     intersyne     j.3.8a       mov     T1,447     crosshatch lines     mov     redline       mov     T1,447     crosshatch lines	
mov         T3,424         Blank lines start         r4           mov         T3,419         Colour par width delay 15         india         temp,74           mov         T3,459         Colour par width delay 15         india         temp,74           mov         T3,459         Lines*3         india         temp,74           mov         T3,459         Lines*3         india         temp,74           mov         T3,459         Linestyne         india         temp,74           mov         T10,816         Chequer functions         gubrouine lower half of page         ord#8(011111)           mov         T12,81         Chequer functions         gubrouine lower half of page         ord#8(011111)           mov         T12,81         Chequer functions         nord         rep,45         ord         port#8(0100000)           mov         T12,81         Linestyne         and         port#8(0100000)         india         temp,45         india	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	ank2
mov       T5,419       Colour par width delay 15       mov       rframe bo         mov       T7,46       120.0s       nov       mov       frame bo         mov       T7,46       120.0s       nov       frame bo       frame bo         mov       T7,46       120.0s       nov       frame bo       frame bo         mov       T10,416       chequer tines       subrotitions bove half of page       get         mov       T12,47       crosshatch lines       get bove       framebo       port#561011111         mov       T12,47       crosshatch lines       get bove       framebo       framebo       framebo         mov       T12,47       crosshatch lines       get bove       framebo       port#56101000000         mov       T12,47       crosshatch lines       get bove       framebo       framebo <td>ank2</td>	ank2
mov         TC#6256         :Liser33         mov         temp.74         frame bit           mov         TC#64         :Libus         r6         call         bitacking           mov         TD#64         :chequer squares         ;subroutines lower half of page         org bit           mov         T12,47         :chequer delay         innesyne         ;3.8us         port#%1011111           mov         T12,47         :cressharch lines         org bit         mov         rb,97.4           mov         T14,47         mov         mov         rb,97.4         mov         rb,97.4           mov         T14,47         mov         call         div         rb,97.4           mov         T14,47         mov         call         div         rb,97.4           mov         T14,47         mov         call         div         rb,97.4           mov         temp.45         :butons sheek         or         port,#%1000000         mov         rb,97.4           fameloop         call         butons         innetly         call         innetly           fameloop         call         butons         innetly         innetly           fameloop         innetly	ank2
mov     TX,859     ile delay feetper intees     inter inte	un K2
mov         TD9/42         schequer squares (schequer squar	
mov         T11,84 or chequer squares         subroutines lower half of page or g0h           mov         T12,84         chequer delay         innesyne         3.8us           mov         T12,84         chequer delay         innesyne         3.8us           mov         T12,84         chequer delay         innesyne         3.8us           mov         T13,89         and         port,8% 10111111           mov         T13,89         mov         count,72         delay 10           mov         temp,87         mov         count,72         delay 10           and         temp,87 skiit         skiit fibutions not pressed         call         linedly           cje         temp,87 skiit         skiit fibutions not pressed         call         linedly           fsyne         cjne         res,82,bv3         mov         rhoger           mov         rh,870111111         jbit 7 low vertical syne         innesyne         mov           fsyne         call         backline         jbit 4000000         jbit 7 ligh         con         port,876,1000000           mov         rhogor         mov         rhogor         mov         hogor         port,876,1000000           idot         temp,173 <t< td=""><td></td></t<>	
mov     T11,447     :croshatch lines     org 0h       mov     T12,49     inesyne     ;3.8us     and     port,4%1011111       mov     T13,49     mov     r0,07     mov     r0,071     (11111)       mov     r14,47     inesyne     ;3.8us     and     port,4%1011111       mov     r14,47     inesyne     inesyne     ;3.8us     and     port,4%1000000       frameloop     mov     temp,475     button scheck     mov     call     dig       ide     temp,475     button scheck     mov     rep,4%01000000     call     linedly       call     button     ited to stand     rep,4%1000000     call     linedly       fsync     call     port,4%0111111     jbit 7 low vertical sync     nop     res,4%2,bv3       fsync     call     blackline     icomplete horizontal sync line     inp     bv4       foop     call     blackline     icomplete horizontal sync line     inp     bv4       finz     temp,1000     jbit 7 high     bv4     or     port,4%0010000       idiz     temp,1000     jbit 7 high     bv4     or     port,4%0010000       idiz     temp,100     jbit 7 high     bv4     or     port,4%00100000	
mov         T12,81         :chequer delay         linesyne         :3.8us           mov         T14,87         mov         rb,90           mov         T14,87         mov         count,72         idelay lo           mov         temp,45         buttons check         or         port,4% (101111)           idelay lo         or         port,4% (100000         idelay lo         or         port,4% (100000           cide         temp,43         scali         linedly         cali         linedly           cide         temp,43         scali         linedly         cali         linedly           cide         temp,43         scali         linedly         cine         res,42,bv3           cide         temp,45         scali         linesyne         cine         res,42,bv3           fsyne         ad         port,476(100000         jbit 7 lob         bars         i7 bars celi to white         inesyne           fsyne         cali         blackline         comp,172         jeit 7 bit         nop         nop           fsyne         cali         blackline         comp,172         jeit 7 bit         nop         nop           fsyne         cali         bardly <td< td=""><td></td></td<>	
mov     T13,4%     and     port,4%1011111       mov     T4,4%7     mov     rb,ort       mov     ra,4%500000110     ;led 0     mov     count,12     adal       frameloop     intern,4%3     intern,4%3     mov     rb,ort       ind     tern,4%3     intern,4%3     mov     rb,ort       ind     tern,4%3     intern,4%3     mov     rb,ort       ind     tern,4%3     intern,4%3     mov     rb,ort       ind     port,4%4100000     intern,4%3     mov     rb,ort       ind     intern,4%3     intern,4%3     mov     rb,ort       ind     port,4%41000000     jump to mainloop if set     erep     erep       exit     if-4us wide neg pulse vga     lofus svga1     bars     i7 bars red to white       fsync     and     port,4%41000000     jbit 7 high     mov     mop       fdoop     call     blackline     complete horizontal sync     mop       idinz     temp,floop     bv3     nop       if ymr     call     blackline     go routines     mov     rb,ort,4%0100000       if ymr     bv4     or     port,4%0010000     ibit 7 high     call     linesync       idinz     temp,f13     iframe	
mov         T14,#7         mov         rb_port           mov         ra#%00000110         ;led 0         mov         call         dly           frameloop         mov         temp,#3         mov         temp,#3         mov         temp,#3           cip         temp,#3         isuitons check         or         port,#%0100000         mov         tbyot           cip         temp,#3         isuit ibutons not pressed         call         linedly         call         linedly           cip         flag,#1,mainloop         jump to mainloop if set         rep         rep           cip         flag,#1,mainloop         jump to mainloop if set         rep         rep           floop         and         port,#%0111111         bit 7 low vertical sync         nop         mov           mov         temp,floop         bv3         nop         call         linesync           dinz         temp,floop         bv3         nop         call         linesync           into         port,#%10000000         jbit 7 high         call         landly         port,#%00100000           ifor         temp,fl.acsshatch         or         port,#%00100000         port,floop         bv3         nop         call<	
frameloop         eail         dy           max         temp,th         jbuttons check         or         port,#%01000000           cip         temp,th         jbuttons not pressed         call         linedly           cip         flag,#1,mänloop         jump to mainloop if set         rep           cip         flag,#1,mänloop         jump to mainloop if set         rep           cip         flag,#1,mänloop         jump to mainloop if set         cip         res,#2,bv3           fsync         and         port,#%01111111         jit 7 low vertical sync         nop         res,#2,bv3           mov         https://res         call         blackline         scomplet horizontal sync line         nop           floop         call         blackline         scomplet horizontal sync line         jmp         bv4           floop         call         blackline         scomplet horizontal sync line         jmp         bv4           inters         call         blackline         scomplet horizontal sync line         jmp         bv4           inters         call         blackline         scomplet horizontal sync line         jmp         bv4           inters         call         blackline         scomp         jmp	
mov         temp, h         buttons check         or         prime         prime         mov         tr.b.port           call         button         call         linedly         call         linedly           call         button         call         linedly         call         linedly           exit         r.64us widt ng pulse vg 106us svga1         bars         ;7 bars red to white         rep           fsync         and         port,#%01111111         bir 7 low vertical sync         nop         res,#2,bv3           mov         thogot         mint virite value to port         nop         nop         nop           floop         call         blackline         complete horizontal sync line         ims ync         nop         nop           floop         or         port,#%1000000         ;bit 7 high         odd <ttd>call         bit3         nop           inde sync         or         port,#%1000000         ;bit 7 high         odd<ttd>port,#%1000000         port +           ;VGA 520 lines total 640-480 display 2.0250kHz 60Hz         or         port,#%1000000         port +         port +           ;odinz         temp,floo         port,#%2000000         ;bit 7 high         call         bardly          cje</ttd></ttd>	op
and         temp,#3,exit         ,exit         if buton         call         incelly           cip         flag,#1,mainloop         jump to mainloop if set         call         incelly           exit         ;64us wide neg pulse vga 106us syga1         bars         ;7 bars red to white         call           fsync         and         port,#%0111111         jbit 7 low vertical sync         nop         res,#2,bv3           mov         t.pop,17         vrite value to port         nop         nop         nop           mov         t.pop,17         nop         bias         ;7 bars red to white         nop           mov         t.pop,14%00100000         jbit 7 high         bv3         nop         nop           foop         or         port,#%0000000         jbit 7 high         call         linesync           v/GA 520 lines total 640*480 display 31.250kHz 60Hz         or         port,#%00100000         port,#%10010000           cje         patern,#J2,echedboard         and         port,#%00100000         port           cje         patern,#J2,echedboard         and         port,#%101111         port           colourbars         cip         port,#%101111         port         port,#%1011111           colourbars <t< td=""><td></td></t<>	
cill         temp.#3.exit         exit         fbuttom         call         linedly           exit         ;64us wide neg pulse vga 106us svga1         bars         ;7 bars red to white         rep.           fsync         and         port,#%01111111         ;bit 7 low vertical sync         nop         nop           mov         rbs,port         ;write value to port         nop         nop         nop           floop         call         blackline         ;complete horizontal sync line         jmg         bv4           djnz         temp.f70         bv3         nop         inesync           inesync         mov         rbport         jwrite value to pot         bv3         nop           inesync         inesync         inesync         call         linesync           inesync         inesync         mov         rbport         bv4         nop           inesync         inesync         call         blackline         inesync         inesync           inesync         inesync         call         bardly         inesync         inesync           inesync         inesync         call         bardly         inesync         inesync           inot         inop         inesync <td></td>	
call     button     call     linediy       cyc     flag,#1, mainloop     jump to mainloop if set     retp       fsync     cjne     res,#2,bv3       mov     rb,port     ivrite value to port     nop       mov     rb,port     ivrite value to port     nop       fig     call     blackline     ;complete horizontal sync     nop       fig     call     blackline     ;complete horizontal sync     nop       fig     temp.Tr7     call     linesync       or     port,#%10000000     ;bit 7 high     call     linesync       or     port,#%10000000     ;bit 7 high     call     linesync       ive     ine     ine     ine     ine       ive     pattern,#0,colourbars     igo routines     or     port,#%0010000       ive     pattern,#0,colourbars     igo routines     mov     rb,port       cie     pattern,#0,celoubars	
exit ;64us wide neg pulse vga 106us svga1 bars ;7 bars red to white fsync cipe res,#2,bv3 and port,#%01111111 ;bit 7 low vertical sync nop mov temp,T7 ;vrite value to port nop mov temp,T7 call blackline ;complete horizontal sync line djinz temp,floop bv3 nop or port,#%10000000 ;bit 7 high bv4 ;VGA 520 lines total 640°480 display 31.250kHz 60Hz ;vGA 520 lines total 640°480 display 31.250kHz 60Hz ;e pattern,#1,crosshatch cje pattern,#2,@cheqboard cje pattern,#2,@cheqboard cje pattern,#2,@cheqboard cje pattern,#2,@cheqboard cje pattern,#2,@cheqboard cje pattern,#2,@cheqboard cje pattern,#2,reskatch cje pattern,#2,reskatch cje pattern,#2,reskatch cje pattern,#2,reskatch clall blackline to vrb,port colourbars call blackline or port,#%0010000 b1 call blackline to vrb,port call blackline or port,#%0010000 b1 call blackline temp,T3 ;frame blank1 or port,#%0011000 b1 call blackline call blackline or port,#%00010000 invo temp,T3 ;frame blank1 or port,#%00010000 b1 call blackline call blackline or port,#%00010000 b1 call blackline temp,14 call blackline or port,#%00010000 b1 call blackline temp,2,15 ;160 vga 200 svga or port,#%1001111 lpa call black or port,#%1001111 lpb call bars call bardy or port,#%10011100 invo temp2,176 ;320 vga 400 svga or port,#%1001100 ipc call bars call bardy or port,#%0011000 ipc call bars call bardy or port,#%10011100 mov temp2,176 ;480 vga 600 svga or port,#%10011000 ipc call bars call bardy or port,#%0011000 ipc call bars call bardy or port,#%0011000 ipc call bars call bardy or port,#%10011100 mov temp2,176 ;480 vga 600 svga or port,#%10011100 ipc call bars call bardy or port,#%10011100 mov temp2,176 ;480 vga 600 svga or port,#%10011100 mov temp2,176 ;480 vga 600 svga or port,#%10011000 mov temp2,176 ;480 vga 600 svga or port,#%00110000 mov temp2,176 ;480 vga 600 svga or port,#%0011000 mov temp3	
fsync     cjne     res,#2,bv3       mov     rb,port     ;write value to port     nop       mov     tcmp,T7     nop       floop     call     blackline     ;complete horizontal sync line     jmp     bv4       djnz     temp,floop     bv3     nop       or     port,#%1000000     ;bit 7 high     bv4       ;VGA 520 lines total 640*480 display 31.250kHz 60Hz     or     port,#%0100000       cje     pattern,#0,zekcrean     or     port,#%0010000       cje     pattern,#0,zekcrean     or     port,#%0010000       ;vGA 520 lines total 640*480 display 31.250kHz 60Hz     or     port,#%0010000       cje     pattern,#0,zekcrean     or     port,#%0010000       ;vGuines must be complete loops, no changes in line timings.     call     bardly       colourbars     mov     temp,T3     frame blank1     or     port,#%0010000       bl     call     blackline     mov     rb,port     call     bardly       djnz     temp,L16     stady     call     bardly     call     bardly       ipz     mov     temp,L16     stady     call     bardly       ipz     temp,L16     stady     call     bardly       ipz     call     bars	
and port,#%0111111 ;bit 7 low vertical sync nop mov trp,T7 nov tremp,T7 call linesync all linesync imp bv4 call blackline ;complete horizontal sync line imp bv4 djnz tremp,floop bv3 call linesync and port,#%0010000 ;bit 7 high call linesync mov rb,port bv4 ;VGA 520 lines total 640°480 displag 31.250KHz 60Hz cje pattern,#2,ceheqboard call bardly cje pattern,#2,ceheqboard call bardly ;routines must be complete loops, no changes in line timings. coll bardly b1 call blackline imp,floo djnz tremp,floo call blackline imp,floo djnz tremp,floo djnz tremp,floo djnz tremp,floo djnz tremp,floo call bardly mov tremp2,T6 ;160 vga 200 svga or port,#%0010000 nov rb,port call bars djnz tremp2,lpa call bars djnz tremp2,lpa call bars djnz tremp2,floo; j320 vga 400 svga or port,#%0011000 nov rb,port call bars djnz tremp2,floo; j320 vga 600 svga or port,#%0011000 nov rb,port call bars djnz tremp2,floo; j320 vga 600 svga or port,#%0011000 nov rb,port call bars djnz tremp2,floo; j320 vga 600 svga or port,#%0011000 nov rb,port call bars djnz tremp2,floo; j320 vga 600 svga or port,#%0011000 nov rb,port call bars djnz tremp2,floo; j320 vga 600 svga or port,#%0011000 nov rb,port call bars djnz tremp2,floo; j320 vga 600 svga or port,#%0011000 nov rb,port call bars djnz tremp2,floo; j320 vga 600 svga or port,#%0011000 nov rb,port call bars djnz tremp2,floo; j320 vga 600 svga or port,#%0011000 nov rb,port call bardly or port,#%0011000 nov rb,port b2 call blackline call bardly or port,#%0011000 nov rb,port b2 call blackline call bardly or port,#%0011000 n	
movmovtwire value to portmopmovtemp,T7nopfloopcallblackline;complete horizontal sync linejmpbv4djnztemp,floopbv3noporport,#%1000000;bit 7 highcalllinesyncinovrb,portbv4orport,#%0010000;VGA 520 lines total 640*480 display 31.250kHz 60Hzorport,#%0010000cjepattern,#2,@cheqboardandport,#%0010000;routines must be complete loops, no changes in line timings.movrb,portcolourbarsciepattern,#3,redscreenmovrb,portblcallbiacklinemovrb,portcalldjnztemp,51iffame blank1orport,#%00010000lpacallbiacklinemovrb,portdjnztemp,51iffame blank1orport,#%00010000lpbcallbarscallbardlyignztemp,2,16;320 vga 400 svgaorport,#%1101111lpamovtemp2,176;480 vga 600 svgaorport,#%10011000lpbcallbarscallbardlyandport,#%10011000lpbcallbarscallbardlyorport,#%1001100lpbcallbarscallbardlyorport,#%1001100lpccallbarscallbardlyorport,#%10011100lpbcallbarscallbardlyor	
movtemp,T7nopfloopcallblackline;complete horizontal sync linejmpbv4djnztemp,floopbv3noporport,#%1000000jbit 7 highcalllinesyncmovrb,portbv4inesyncinesync;VGA 520 lines total 640*480 display 31.250kHz 60Hzorport,#%00100000cjepattern,#0,coisoshatchcallbardlycjepattern,#3,redscreenorport,#%00100000;routines must be complete loops, no changes in line timips.orport,#%0010000colourbarsmovtemp,73;frame blank1orblcallblacklinemovrb,portdjnztemp,b1callbardlydjnztemp,b1callbardlydjnztemp,2,T6;160 vga 200 svgaorport,#%00010000lpbcallbarsmovrb,portdjnztemp2,1pacallbardlyandippcallbarscallbardlydjnztemp2,1pacallbardlyippcallbarscallbardlyippcallbarscallbardlyippcallbarscallbardlyippcallbarscallbardlyippcallbarscallbardlyippcallbarscallbardlyippcallbarscallbardlyippcall <td></td>	
callblackline;complete horizontal sync linejmpbv4dinztemp,floopbv3noporport,#%10000000;bit 7 highcalllinesyncmovrh,portbv4;VGA 520 lines total 640*480 display 31.250kHz 60Hzorport,#%00100000cjepattern,#0,colourbars;go routinesmovrb,portcjepattern,#1,crosshatchcallbardlycjepattern,#3,redscreenorport,#%1011111colurbarscjepattern,#3,redscreenorport,#%0010000;routines must be complete loops, no chages in line timings.movrb,portcallcolurbarsmovtemp,T3;frame blank1orport,#%00110000b1callblacklinemovrb,portcall bardlymovtemp,b1callbardlymovrb,portdjnztemp,2,T6;160 vga 200 svgamovrb,portdjnztemp2,1pacallbardlymovrb,portdjnztemp2,1p6;320 vga 400 svgaorport,#%001000lpbcallbarscallbardlydjnztemp2,1p6;480 vga 600 svgaorport,#%0011000lpccallbarscallbardlydjnztemp2,1p6movrb,portcalldjnztemp2,1p6callbardlyorport,#%0011000lpccallbarscallbardlydjnztemp2,1pc <td< td=""><td></td></td<>	
djnztemp,floopbv3noporport,#%1000000;bit 7 highcalllinesyncmovrb,portbv4orport,#%00100000;vGA 520 lines total 640*480 display 31.250kHz 60Hzorport,#%00100000cjepattern,#0,colourbars;go routinescallbardlycjepattern,#2,@cheqboardandport,#%11011111cjepattern,#3,redscreenorport,#%10010000;routines must be complete loops, no changes in line timings.callbardlycolourbarsmovtemp,T3;frame blank1orb1callblacklinecallbardlymovtemp,D1callbardlymovtemp,D1callbardlymovtemp2,T6;160 vga 200 svgaorport,#%10011000lpbcallbarscallbardlyiptcallbarscallbardlyiptcallbarscallbardlyiptcallbarscallbardlyiptcallbarscallbardlyiptcallbarscallbardlyiptcallbarscallbardlyiptcallbarscallbardlyiptcallbarscallbardlyiptcallbarscallbardlyiptcallbarscallbardlyiptcallbarscallbardlyipt	
orport,#%1000000;bit 7 highcalllinesyncmovrb,portbv4;VGA 520 lines total 640*480 display 31.250kHz 60Hzorport,#%00100000cjepattern,#0,colourbars;go routinesmovrb,portcjepattern,#1,crosshatchcallbardlycjepattern,#3,redscreenorport,#%0010000;routines must be complete loops, no charges in line timings.movrb,portcolourbarscallbardlymovcolourbarsmovtemp,T3;frame blank1orbldjnztemp,b1movrb,portdjnztemp,b1callbardlyipamovtemp,2,T6;160 vga 200 svgaandipacallbarsorport,#%0001000ipbcallbarscallbardlyipacallbarscallbardlyipacallbarscallbardlyipacallbarscallbardlyipacallbarscallbardlyipacallbarscallbardlyipacallbarscallbardlyipacallbarscallbardlyipacallbarscallbardlyipacallbarscallbardlyipacallbarscallbardlyipacallbarscallbardlyipacallbarscall </td <td></td>	
movtb,portbv4;VGA 520 lines total 640°480 display 31.250kHz 60Hzorport,#%0010000cjepattern,#1,crosshatchcallbardlycjepattern,#2,@cheqboardandport,#%11011111cjepattern,#3,redscreenorport,#%10010000;routines must be complete loops, no changes in line timings.movrb,portcolourbarscallblacklinemovrb,portb1callblacklinemovrb,portdjnztemp,b1callblacklinemovrb,portdjnztemp,b1movrb,portcallbrddylpbcallbarsmovrb,portdjnztemp2,T6;320 vga 400 svgaorport,#%1001111lpbcallbarscallbardlydjnztemp2,T6;480 vga 600 svgaorport,#%10011000lpccallbarscallbardlydjnztemp2,T6;480 vga 600 svgaorport,#%1001100lpccallbarscallbardlydjnztemp2,T6;480 vga 600 svgaorport,#%1001100lpccallbarscallbardlydjnztemp2,T6;480 vga 600 svgaorport,#%1001100lpccallbardlyorport,#%1001100b2callbardscallbardlydjnztemp2,T6;480 vga 600 svgaorport,#%0011000hyportcallbardly </td <td></td>	
cjepattern,#0,colourbars;go routinesmovrb,portcjepattern,#1,crosshatchcallbardlycjepattern,#2,@cheqboardandport,#%01011111cjepattern,#3,redscreenorport,#%00010000routines must be complete loops, no changes in line timings.movrb,portcolourbarsmovtemp,T3;frame blank1orport,#%00110000b1callblacklinemovrb,portdinztemp,b1callblacklinecallbardlymovtemp2,T6;160 vga 200 svgaandport,#%1001111lpacallbarsmovrb,portcallbarsmovrb,portdjnztemp2,T6;320 vga 400 svgaorport,#%0011000lpbcallbarscallbardlyinvotemp2,T6;480 vga 600 svgaorport,#%0011000lpccallbarscallbardlyinvotemp2,T6;480 vga 600 svgaorport,#%0011000lpccallbarscallbardlyinvotemp2,T6;480 vga 600 svgaorport,#%0011000lpccallbarscallbardlyinvotemp2,T6;480 vga 600 svgaorport,#%0011000lpccallbardlyorport,#%0011000lpccallbardlyorport,#%0011000lpccallbardlyorport,#%0011000lpc	
cjepattern,#1,crosshatchcallbadlycjepattern,#2,@cheqboardandport,#%11011111cjepattern,#3,redscreenorport,#%00010000routines must be complete loops, no changes in line timings.movrb,portcolourbarsmovtemp,T3;frame blank1orport,#%00110000b1callblacklinemovrb,portdjnztemp,13;frame blank1orport,#%00110000b1callblacklinemovrb,portdjnztemp,16andport,#%00010000movtemp2,76;160 vga 200 svgaandport,#%11001111lpaorport,#%0001000movrb,portcallbarsimovtemp2,16;320 vga 400 svgaorlpbcallbarscallbardlymovtemp2,16;320 vga 400 svgaorport,#%00011000lpbcallbarscallbardlyipzcallbarscallbardlyipzcallbarscallbardlyipzcallbarscallbardlyipzcallbarscallbardlyipzcallbarscallbardlyipzmovtemp2,176;480 vga 600 svgaorport,#%0011000ipzcallbarscallbardlyipzcallbarscallbardlyipzcallbarscallbardly </td <td>;red</td>	;red
cjepattern,#2,@cheqboardandport,#%11011111cjepattern,#3,redscreenorport,#%00010000;routines must be complete loops, no changes in line timings.movrb,portcolourbarsmovtemp,T3;frame blank1orb1callblacklinemovrb,portdjnztemp,b1callbardlymovtemp,276;160 vga 200 svgaandport,#%0101000ipacallbarsmovrb,portdjnztemp2,176;320 vga 400 svgaorport,#%00101000lpbcallbarscallbardlymovtemp2,176;320 vga 400 svgaorport,#%00101000lpbmovtemp2,176;320 vga 400 svgaorport,#%00101000lpbcallbarscallbardlyandmovtemp2,176;480 vga 600 svgaorport,#%1101111lpccallbarscallbardlydjnztemp2,176;480 vga 600 svgaorport,#%0011000lpccallbardlycallbardlydjnztemp2,176;480 vga 600 svgaorport,#%0011000lpccallbardlyorport,#%00011000movtemp2,176;480 vga 600 svgaorport,#%0011000b2callbardlycallbardlyb2callblacklinecallbardly	
cjepattern,#3,redscreenorport,#%00010000;routines must be complete loops, no changes in line timings. colourbarsmovrb,portmovtemp,T3;frame blank1orport,#%00110000b1callblacklinemovrb,portdjnztemp,D1callbardlymovtemp,ZT6;160 vga 200 svgaandport,#%11001111lpaorport,#%00010000orport,#%00010000callbarsandport,#%11001111lpacallbarscallbardlyinztemp,I76;320 vga 400 svgaorport,#%0010000lpbcallbarscallbardlyinztemp2,I76;320 vga 400 svgaorport,#%0101000lpbcallbarscallbardlyinztemp2,I76;480 vga 600 svgaorport,#%0011000lpccallbarscallbardlyinztemp2,I76;480 vga 600 svgaorport,#%0011000lpccallbarscallbardlyinztemp2,Ipcmovrb,portcallinztemp2,Ipcmovrb,portcallinztemp2,Ipcmovrb,portcallinztemp2,Ipcmovrb,portcallbardlydjnztemp2,Ipcmovrb,portcallbarscallbardlyinztemp2,Ipcmovrb,portcallbars </td <td></td>	
routines must be complete loops, no changes in line timings. colourbars mov temp,T3 frame blank1 b1 call blackline mov temp,D1 mov temp,Z16 frame blank2 call bars call bardy djnz temp2,Ip6 frame blank2 call bardy djnz temp2,Ip6 frame blank2 call bardy call bardy	;green
mov         temp,T3         ;frame blank1         or         port,#%00110000           b1         call         blackline         mov         rb,port           djnz         temp,b1         call         bardly           mov         temp,2T6         ;160 vga 200 svga         and         port,#%11001111           lpa         call         bars         mov         rb,port           djnz         temp2,T6         ;320 vga 400 svga         or         port,#%00001000           lpb         call         bars         call         bardly           mov         temp2,T6         ;320 vga 400 svga         or         port,#%0010000           lpb         call         bars         call         bardly           djnz         temp2,T6         ;320 vga 400 svga         or         port,#%001000           lpb         call         bars         call         bardly           djnz         temp2,T6         ;480 vga 600 svga         or         port,#%0011000           lpc         call         bars         call         bardly           djnz         temp2,T6         ;480 vga 600 svga         or         port,#%0011000           mov         temp2,T6         ;480 vg	10.000
b1       call       blackline       mov       rb,port         djnz       temp,b1       call       bardly         mov       temp,2,T6       ;160 vga 200 svga       and       port,#%11001111         lpa       call       bars       mov       rb,port         djnz       temp2,T6       ;320 vga 400 svga       mov       rb,port         djnz       temp2,T6       ;320 vga 400 svga       or       port,#%001000         lpb       call       bars       call       bardly         djnz       temp2,T6       ;320 vga 400 svga       or       port,#%001000         lpb       call       bars       call       bardly         djnz       temp2,T6       ;480 vga 600 svga       or       port,#%0101000         lpc       call       bars       call       bardly         djnz       temp2,T6       ;480 vga 600 svga       or       port,#%00011000         lpc       call       bars       call       bardly         djnz       temp2,T6       ;480 vga 600 svga       or       port,#%0011000         mov       temp2,T6       ;480 vga 600 svga       or       port,#%0011000         b2       call       bar	
djnz         temp,bl         call         bardly           mov         temp2,T6         ;160 vga 200 svga         and         port,#%11001111           lpa         or         port,#%00001000           call         bars         mov         rb,port           djnz         temp2,Ipa         call         bardly           mov         temp2,Ipa         call         bardly           mov         temp2,T6         ;320 vga 400 svga         or         port,#%00101000           lpb         call         bars         call         bardly           djnz         temp2,Ip6         ;320 vga 400 svga         or         port,#%00101000           lpb         call         bars         call         bardly           djnz         temp2,Ip6         and         port,#%0101000           mov         temp2,Ip6         and         port,#%0011000           mov         temp2,T6         ;480 vga 600 svga         or         port,#%0011100           lpc         call         bars         call         bardly           djnz         temp2,Ipc         mov         rb,port         call           djnz         temp2,Ipc         call         bardly         or	;yellow
mov         temp2,T6         ;160 vga 200 svga         and         port,#%11001111           lpa         or         port,#%00001000           call         bars         mov         rb,port           djnz         temp2,T6         ;320 vga 400 svga         mov         rb,port           mov         temp2,T6         ;320 vga 400 svga         or         port,#%0010100           lpb         call         bars         call         bardly           djnz         temp2,T6         ;480 vga 600 svga         or         port,#%0101000           lpc         call         bars         call         bardly           djnz         temp2,T6         ;480 vga 600 svga         or         port,#%0011000           lpc         call         bars         call         bardly           djnz         temp2,T6         ;480 vga 600 svga         or         port,#%0011000           mov         temp2,T6         ;480 vg	
lpa     or     port,#%00001000       call     bars     mov     rb,port       djnz     temp2,lpa     call     bardly       mov     temp2,T6     ;320 vga 400 svga     or     port,#%00101000       lpb     mov     rb,port     call     bardly       djnz     temp2,T6     ;480 vga 600 svga     or     port,#%00011000       lpc     call     bars     call     bardly       djnz     temp2,T6     ;480 vga 600 svga     or     port,#%00011000       lpc     call     bars     call     bardly       djnz     temp2,T6     ;480 vga 600 svga     or     port,#%00011000       mov     temp2,T6     ;480 vga 600 svga     or     port,#%0011000       lpc     call     bars     call     bardly       djnz     temp2,lpc     mov     rb,port       or     port,#%00111000     mov     rb,port       b2     call     blackline     call     bardly	
djnz         temp2,lpa         call         bardly           mov         temp2,T6         ;320 vga 400 svga         or         port,#%00101000           lpb         call         bars         call         bardly           djnz         temp2,Ipb         call         bardly           mov         temp2,Ipb         and         port,#%11010111           mov         temp2,T6         ;480 vga 600 svga         or         port,#%0011000           lpc         call         bars         call         bardly           djnz         temp2,Ipb         call         bardly           mov         temp2,If6         ;480 vga 600 svga         or         port,#%00011000           lpc         call         bars         call         bardly           djnz         temp2,Ipc         or         port,#%0011000           mov         temp2,Ipc         or         port,#%00111000           mov         temp2,Ipc         mov         rb,port           djnz         temp2,Ipc         mov         rb,port           djnz         temp2,Ipc         mov         rb,port           djnz         temp2,Ipc         call         bardly           b2	;blue
mov         temp2,T6         ;320 vga 400 svga         or         port,#%00101000           lpb         mov         rb,port         mov         rb,port           call         bars         call         bardly           djnz         temp2,Ipb         and         port,#%00011000           mov         temp2,Ipb         and         port,#%00011000           lpc         call         bars         call         bardly           djnz         temp2,T6         ;480 vga 600 svga         or         port,#%00011000           lpc         call         bars         call         bardly           djnz         temp2,Ipc         mov         rb,port           djnz         temp2,Ipc         or         port,#%00111000           mov         temp,T4         ;frame blank2         mov         rb,port           b2         call         blackline         call         bardly	
lpb     mov     rb,port       call     bars     call     bardly       djnz     temp2,lpb     and     port,#%11010111       mov     temp2,lpc     or     port,#%00011000       lpc     call     bars     call     bardly       djnz     temp2,T6     ;480 vga 600 svga     or     port,#%00011000       lpc     call     bars     call     bardly       djnz     temp2,lpc     or     port,#%0011000       mov     temp2,lpc     or     port,#%0011000       b2     call     blackline     call     bardly	;magenta
call     bars     call     bardly       djnz     temp2,lpb     and     port,#%11010111       mov     temp2,T6     ;480 vga 600 svga     or     port,#%00011000       lpc     call     bars     call     bardly       djnz     temp2,Ipc     call     bardly       djnz     temp2,lpc     or     port,#%0011000       mov     temp2,lpc     or     port,#%0011000       b2     call     blackline     call     bardly	,magema
mov     temp2,T6     ;480 vga 600 svga     or     port,#%00011000       lpc     mov     rb,port       call     bars     call     bardly       djnz     temp2,1pc     or     port,#%00111000       mov     temp2,1pc     or     port,#%00111000       b2     call     blackline     call     bardly	
lpc     mov     rb,port       call     bars     call     bardly       djnz     temp2,lpc     or     port,#%00111000       mov     temp,T4     ;frame blank2     mov     rb,port       b2     call     blackline     call     bardly	
call     bars     call     bardly       djnz     temp2.lpc     or     port,#%00111000       mov     temp,T4     ;frame blank2     mov     rb.port       b2     call     blackline     call     bardly	;cyan
djnztemp2,lpcorport.#%00111000movtemp,T4;frame blank2movrb.portb2callblacklinecallbardly	
b2 call blackline call bardly	;white
jmp frameloop mov rb,port	
crosshatch mov count,T14 ;trim end	
mov temp,T3 ;frame blank l trim	
b3 call blackline djnz count,trim	
djnz temp,b3 ret mov temp2,T10 ;8 lines vga bardly	
cra mov count.T5 ;width de	lav
call whiteline ;1 boop	-,
mov temp1,T11 ;1+59 vga djnz count,boop	
crb retp	
call hatch dly djnz templ,crb loop2 nop ;delay se	in count
djnz templ,crb loop2 nop ;delay set djnz temp2,cra djnz count,loop2	in count
nop retp	
call whiteline ;end line linedly	
mov temp,T4 ;frame blank l mov count,T1 ;porch de	
b4 call blackline loop3 djnz temp,b4 djnz count,loop3	lay
ujiz coult, loops	lay

#### **INSTRUMENTATION & TEST**

hatah	retp				call	linedly	
atch	cje	res,#1,hv2		hutton	retp		
				button			
	cje	res,#2,hv3			mov	w,rb ;buttons	check
	call	linesync			and	w,#2	
	mov	temp,#10 ;vertical b	ars		test	W	
1					jz	reschange	
	ог	port,#%00111000	;white	patchange			
	mov	rb,port			add	pattern,#1	;next pattern
	and	rb,#%11000111	;black		cjbe	pattern,#3,bexit	
11	mov	count,#22	;delay between bars		mov	pattern,#0	;back to start
n1 lp					jmp	bexit	
	djnz	count,h11p		reschange			
	djnz	temp,hl			add	res,#l	;next resolution
nloop					mov	flag,#1	;set res change flag
	or	port,#%00111000	;white		cjbe	res,#2,bexit	
	mov	rb,port			mov	res,#0	;back to start
	and	rb,#%11000111	;black	bexit			
	call	linedly			mov	temp,rb	;buttons check
	and	port,#%11000111	;black		and	temp.#3	
	ret				cjne	temp,#3,bexit	;wait release
1v2					retp		
	call	linesync			org	200h	
	mov	temp,#6		cheqboard	6		
12					mov	temp,T3	;frame blank l
	Oľ	port,#%00111000	;white	b5	call	@blackline	,
	mov	rb,port			djnz	temp,b5	
	and	rb,#%1100 <b>0</b> 111	;black		mov	temp2,T10	;vertical squares
	mov	count,#14	delay loop	cheq	11.5 *	terribadi v ro	, entreur squares
12lp			,, .oop	ed	mov	temp1,T9	;chequer lines
P	djnz	count,h2lp		chb	11101	winp (, i )	senequer miles
	djnz	temp,h2		cheque l			
	mov	temp,#6		cheque	000		
2a	mov	tomp, no			nop		
124	0.5	mont #07.001111000	uuhita		nop	Olineare	
	or	port,#%00111000	;white		call	@linesync	
	mov	rb,port		1.1	mov	temp3,T10	
	and	rb,#%11000111	;black	ch1			1.
	nop		1.1. 1.		Oľ	port,#%00111000	;white
01	mov	count,#14	;delay loop		mov	rb,port	
n2lpa		1.01			mov	count,T12	;delay loop
	djnz	count,h2lpa			call	@dly	
	djnz	temp,h2a			and	port,#%11000JJ1	;black
	jmp	hloop			mov	rb,port	
1v3					mov	count,T12	;delay loop
	nop				call	@dly	
	call	linesync			djnz	temp3,chl	
	mov	temp,#7			and	port,#%11000111	;black
13					mov	rb,port	
	OT.	port,#%00111000	;white		call	@linedly	
	mov	rb,port			nop		
	and	rb,#%11000111	;black		nop		
	nop				mov	count,T13	;trim end
	mov	count,#8	;delay loop	trim l			
<b>3</b> lp					djnz	count,trim1	
	djnz	count,h3lp			djnz	temp1,chb	
	djnz	temp,h3			mov	temp1,T9	
	mov	temp,#7		cha		, ,	
3a				cheque2			
	or	port,#%00111000	;white		пор		
	mov	rb,port	,		nop		
	and	rb,#%11000111	;black		call	@linesync	
	mov	count.#8	;delay loop		mov	temp3,T10	
31pa	nov	count,#o	delay loop			temps, 110	
wiha	djnz	count,h3lpa		ch2	пор		
	djnz	temp,h3a		0112	and	port,#%11000111	black
		tempinoa			mov	rb,port	DIACK
	imp	hloon					delay loop
lackline mov	jmp	hloop 60000000			call	count,T12	;delay loop
lackline mov		line				@dly port,#%0011.1000	;white
vhiteline mov	jmp colour #9	600111000			OF	rb,port	,winte
machine mov		line			mov		:delay loop
edline	jmp				mov	count,T12	;delay loop
cuntie	mov	colour,#%00100000			call	@dly	
	nop				djnz	temp3,ch2	uhlanda
	nop				and	port,#%11000111	;black
	nop				mov	rb,port	
ine	- 11	line and a			call	@linedly	
	call	linesync			nop		
	nop				mov	count,T13	;trim end
	ΟΓ	port,colour		trim2			
	mov	rb,port			djnz	count,trim2	
	mov	count,T8	;delay loop		djnz	temp I, cha	
	call	dly			djnz	temp2,cheq	
	mov	count,T8	;delay loop		mov	temp,T4	;frame blank2
	call	dly		b6	call	@blackline	
	and	port,#%11000111			djnz	temp,b6	
	and						



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