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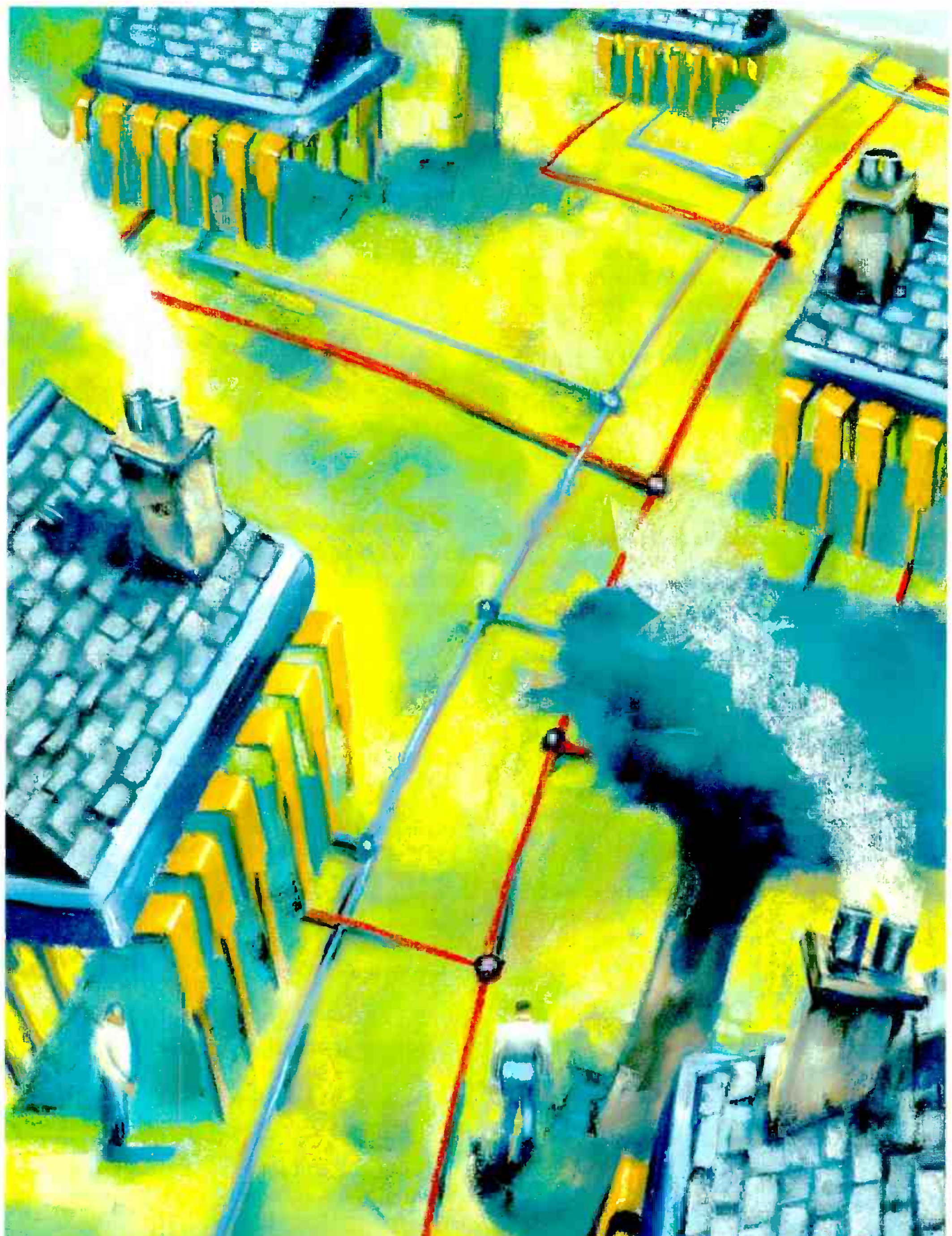

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A nasty case of slipped disks

Please allow me to share with you a personal dream. All desktop computer operating systems rely on hard disks, which in a world of solid-state electronics, are anachronistic. The majority of computer failures derive from mechanical components. Replacing mechanics with electronics results in faster, more reliable products. I contend that what the desktop computing world needs is not *Chicago*, *Windows NT*, Apples and Acorns but machines which integrate all aspects of their operation into electronics.

Of course, this is not an original thought. Every high street techie shop is alive with things called PDAs – personal digital assistants. These are miniature computer devices which combine all sorts of features which nobody has asked for with a data entry system which nobody wants to use. But they do have technical merit. They contain their operating systems in silicon and are thus probably reliable while their absence of motors reduces power consumption to the point where they can do more than boot themselves up before the battery goes flat. I would like to see a desktop computer, full sized keyboard and a built-in solid state operating system. And, of course, the applications software to run on it. This remains a dream because solid-state storage devices with sufficient capacity do not exist… yet.

Here is the reality. Microsoft and other vendors of computer operating systems have misplaced objectives. First, a few facts. Microsoft has spent more than £100 million developing *Windows NT*, a true 32-bit operating system designed to subvert the unix world. As such it provides all sorts of security mechanisms for networked computer applications. However, it occupies no less than 70Mbytes of disk space and is noticeably slower in use than the already sluggish and restrictive *Windows* 3.1.

On the plus side, it breaks away from the Intel monopoly by eventually being available for *PowerPC* and other microprocessor architectures. This should allow applications software to become independent of machine and microprocessor type. Indeed, since IBM opened its doors to merchant chip sales, I would only buy a PC with *IBM Inside*, preferably the 100MHz *Blue Lightning* which knocks spots off Intel's *Pentium*. But that is another story.

Ignore for a moment the needs of the power user; you don't want to run a network or file-serving system or sort a 200MB of mailing list. Just the ordinary things which 90 per cent of computer users want: spreadsheets, wordprocessors, calculators and graphics. These are the uses which are ripe for a solid-state computer.

With current technology, your probable choice of operating system will be *Chicago*, the forthcoming successor to *Windows* 3.1 combining its own Dos 7 operating layer. You won't be alone. Its predecessor has already sold some 40 million copies. Once again it is slow and cumbersome and will eat up16 Mbytes of disk space. One might have chosen an Apple Macintosh or something else but these alternatives aren't much better.

This raises a couple of points. Firstly software writers no longer feel constrained to writing compact code. I suggest that current user applications simply incorporate more unused features than their smaller forbears. Most could usefully be compacted to fit restricted memory space without a return to command line programming: an effective GUI would be part of the silicon operating system.

Secondly, semiconductor companies think too conventionally. The largest flash eeprom chips, currently some 16Mbit/chip, are guaranteed 100 per cent functional which makes large memory arrays built from them expensive. The concept of wafer scale integration is some 25 years old but deserves rediscovery. In the same way that bad disk sectors are mapped and excluded, a similar redundancy EDC system could be made for large, low cost silicon storage. I would like to buy silicon memory arrays with their own built-in operating system rather than as individual chips. My consultant Derek Rowe – a founder of Abacus Computers – insists that if WSI were that easy, it would have been done years ago. Also, a viable computer system requires a low cost data exchange – floppy disk. I insist that, if semiconductor companies directed as much of their effort into memory system function as they put into process technology, WSI could be reality. I also say "smart card".

It seems incredible that the computer industry alone shows virtually no technological progress while making so much money out of inappropriately engineered products.

Frank Ogden.

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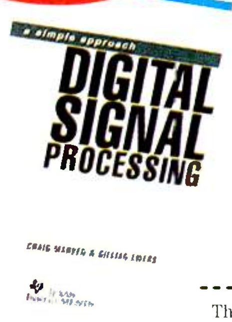

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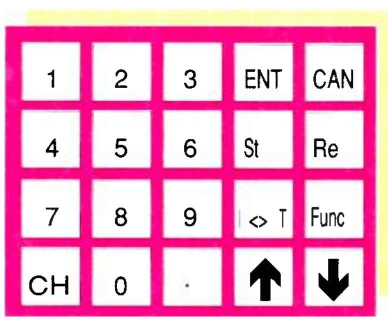


REGULARS

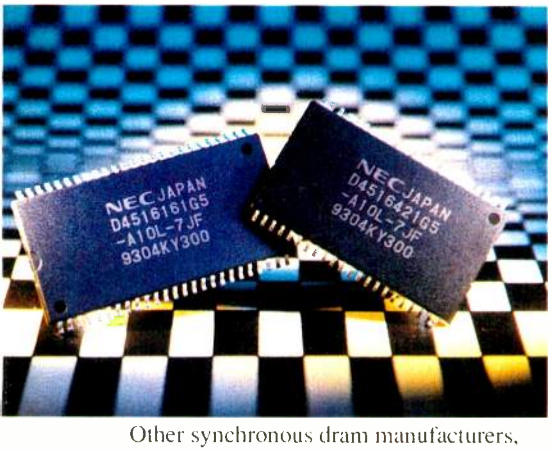
In next month's EW+WW: Special bass issue.

Bass reproduction tends to be the single most significant factor in determining the perceived performance of an audio system. Five separate luminaries look for the ultimate in bass reproduction technology. We consider the theory, the practice, the materials, the size, the electronics, the arrangement and the room. A heavyweight investigation for heavyweight bass reproduction.

JANUARY ISSUE IS ON SALE DECEMBER 30

Synchronous drams: better mass memory technology?

A recent annoucement by NEC that it is ready to begin production of 16Mbit synchronous drams places the technology on the starting blocks. But it is clear there is little – almost minimal – demand for the devices currently and that future demand will depend on whether it is a practical and cost effective solution for high speed system design.



Other synchronous dram manufacturers, principally Hitachi, Samsung and Toshiba, are in a similar position to NEC. However, they are being more reticent in forecasting production of 16Mbit devices and some are sceptical of there being a sizeable market much before 1995.

In synchronous dram all inputs and outputs are synchronised to the rising edge of the system clock operating up to 100MHz. This contrasts with traditional dram technology which is controlled asynchronously: the processor dispatches a set of addresses and waits, while the DRAM performs several internal functions such as activating the word and bit lines, until the data is returned.

Conversely under synchronous control of the system clock, the addresses are latched in the dram until the device is ready to deliver the data after a preprogrammed number of clock cycles. During this time the processor can perform other functions.

The synchronous dram has two internally interleaved banks and the row address strobe will need only a single pulse signal while hidden precharge and a programmable burst sequence provide the high bandwidth.

The row address is strobed in on the rising edge of the system clock activating a row or word line. A column address in then latched in after three clock cycles (30ns minimum). A byte of data appears on the outputs after three more cycles are taken to decode the address and deliver data to the output buffers – just six cycles in total.

Synchronous dram can reduce access time further by pipelining addresses. The input latch stores the next address while the dram is processing the previous one.

Burst mode is similar to the old nibble mode in which four bits of sequential data are provided in rapid succession without having to provide new address information. In the synchronous dram however, as much as an entire page, typically 1024-bits, can be provided after the first 60ns access at the rate of one byte every 10ns. This burst mode can also be combined with a wrap feature to give access to strings of data stored both before and after the initial bit location. It will be useful for cache line filling where data tends to have spatial locality properties. The wrap feature has a programmable length of 1, 2, 4 or 8 bytes or a full page.

A further benefit of the interleaving is that active rows in separate banks can emulate a cache; the row is held active and reselected simply by supplying a new column address.

There are many other features such as clock enable/disable which will suspend the device, in its current state and put it into a low power standby mode. Self refresh is also included.

Jedec published the specification for synchronous dram in October. To date the only bus interface contained in the specification is low voltage LVTTL.

According to Desi Rhoden, one of the subcommittee chairmen on the JC42.3 committee which is overseeing the development of synchronous dram, the LVTTL interface is good for 100MHz, but no higher. The committee is therefore looking at other interfaces including GTL, CTT and ECL to raise performance to 200 to 250MHz.

"GTL is under investigation and is not yet proven to work in a system at any reasonable frequency," said Rhoden. "I expect some modifications will be needed. ECL and CTT are also high power alternatives and that doesn't really track well with what we are trying to do. GTL is also actually high power because of all the terminations needed in a system."

All of these interface standards have limited voltage swing in common. Our overall goal is to limit the amount of charge flowing between buffers. So a 1V swing would seem a logical objective. We may have to go for a compromise between all the alternatives to get the kind of performance we want."

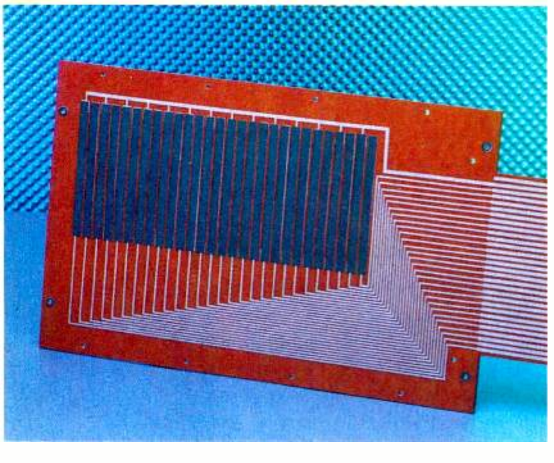
Rhoden admits though that 200MHz dram performance is unlikely to be demanded by systems designers for at least two years – pretty much when the current generation of synchronous drams is expected to be in volume production.

The ultimate success of synchronous dram will depend on whether it can effectively replace a second level cache, which currently relies on expensive sram, and on there being little or no price premium for the chips.

According to some industry experts, how successful synchronous dram is at replacing caches cannot be judged at present because most major systems houses are keeping their conclusions to themselves.

The price issue is more easily judged. Anne West, NEC UK's assistant product manager for memory, says the current price of an ordinary 16Mbit dram is about £50. A 16Mbit synchronous dram will be at least double that initially," she said. Only market demand will drop that price".

Simon Parry, Electronics Weekly



A team from University College London has been researching new ways to help measure disabled peoples' feet so that correctly fitting shoes can be made. Their 'three dimensional' measurement method involved carbon tracks custom printed onto a PCB. According to the source of the PCB, Omeg, theirs was the only company in Europe able to produce it.

Space for Silicon Valley

If NASA has its way, there will be two Silicon Valleys – one in California and the other in space.

In January of next year, the Space Shuttle will launch the Wake Shield Facility – the first commercial production facility designed to produce near-perfect gallium arsenide wafers while circling the Earth in low orbit.

The space-grown wafers will result in integrated circuits which can run eight times faster than circuits made from silicon and three times faster than gallium arsenide chips made on earth, according to University of Houston researchers.

Conceived by the Space Vacuum Epitaxy Center at the University of Houston and by Space Industries in League City, Texas, the Wake Shield Facility will use molecular beam epitaxy to produce near perfect crystal wafers of gallium arsenide. The gallium arsenide wafers are made by laying down ultrathin layers of molecules in a vacuum.

During the flight, the Wake Shield Facility, a 12ft stainless steel disc, will travel at close to 17,000 miles an hour, pushing the thin atmosphere out of its way and leaving in its wake a vacuum more than 10,000 times purer than the best vacuum chambers on earth.

Because the vacuum created in space is so pure, the crystals will not be contaminated by unwanted atoms, which slow down conduction of electronic signals.

If all goes well in January, NASA is planning to use the Wake Shield Facility to make other thin crystalline films for lasers and superfast computer circuits.

Warning on digital TV

Europe should move as fast as possible to establish digital terrestrial television services, with simulcasting of existing TV channels in digital and analogue forms starting as early as 1997, and it should also move as soon as possible to an all-digital world. So says a report published last week by city firm Coopers and Lybrand. Co-author Dermot Nolan said existing terrestrial broadcasters are likely to go under if they miss the digital boat.

Picture firms up for digital HDTV

There is still a considerable amount of HDTV research in the pipeline if the recent conference in Ottawa is anything to go by. But a number of the remaining problems stem from the sometimes diverse interests of the broadcast, cable, satellite and computer industries.

For example, to placate the latter, square pixels have been included in the latest North American draft specification even though the corners will become rounded in the display medium.

The digital tv system is now defined as a four layer model: the picture or image layer; the compression layer; the transport layer; and the transmission layer.

The picture layer defines a strategy that is perhaps future proof, providing for 24, 30 and 60 frames a second with progressive scanning. The long term aim of 1050 lines has been upgraded to 1080 lines with 1920 samples per line.

The compression layer is defined around the MPEG-2 standard, at least as far as the video signal is concerned. It has been decided that Dolby AC-3 at 384Kbit/s suits the North American environment better than the European Musicam system. But the final specification may include both as alternative sound systems.

The transport layer relates to the protocol of packetisation, prioritisation and universal headers in the bitstream and is accepted as pure MPEG-2.

And the transmission layer is to be based on quadrature amplitude modulation or vestigial sideband, rejecting the European coded orthogonal frequency division multiplex system.

It was reported at the conference that the MPEG-4 committee is close to producing a draft report dealing with the future needs for audio-visual processing, addressing the applications and operational environment for very low (a few 10s of kHz) bit rate coding.

The introduction of HDTV will mean simulcasting from existing transmission sites and many masts won't be able to take the extra weight. It poses a particular problem in the US where a substantial number of the 1600 or so US transmitters operate in the vhf band. Because their masts are ageing, it is doubtful if they can meet current construction standards because of the heavier vhf arrays. A similar situation may arise in Europe.

As well as nuts and bolts issues, a significant number of papers dealt with ultra high definition TV – pictures made up from more than 2000 lines and pictures in 3D.

On hardware, German company Digitale Videosystems showed its ISP500 image sequence processor using up to 16Mbyte of ram. It can store several minutes of real time video images in any format, including high definition versions, under software control.

Geoff Lewis

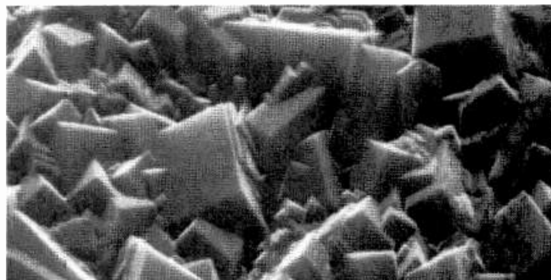
Diamonds and bucky balls feature in new films

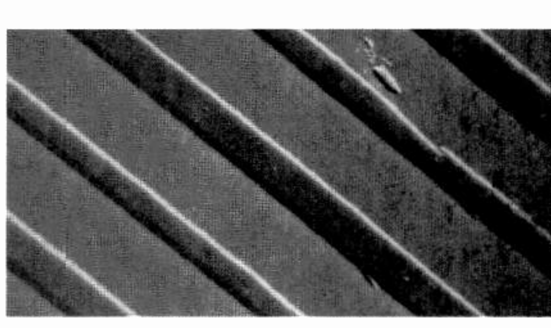
Two newly developed carbon-based films, one diamond and one fullerene C_{60}, are being explored by researchers at Bell Labs for use in microelectronics.

The films have radically different properties. As is well known, diamond is extremely hard with excellent thermal properties. Fullerene C_{60} on the other hand has unique properties that could trigger "thousands of new uses" according to AT&T.

Thin-film diamond, shown in the top photo, makes a highly efficient heat sink for high-power semiconductor lasers such as those used for long distance communications via optical fibres.

Derived from soot, fullerene C_{60} has recently been found to be photoresistive and sensitive to ultraviolet light. There may be uses for it in semiconductor manufacture. Earlier research showed that C_{60}, shown in the bottom photograph, becomes superconducting when compounded with potassium or rubidium.





Significant bits first speeds up digital filters

Digital signal processing system designers are doing their arithmetic the wrong way round, jokes Professor John McCanny of Belfast University. To prove his point, engineers there have designed an IIR (infinite impulse response) filter chip which is about 500 times faster than a comparable implementation on a programmable DSP.

Samples of the chip were recently delivered to Professor McCanny's team. Maufactured by GEC-Plessey using its CLA70000 series gate array, the IIR chip has a 30MHz clock speed and has five modes, giving filters up to 16th order, and operates on 16bit two's complement data. GPS is considering making the chip one of its standard signal processing products.

The crux of the IIR filter, however, is that the latency is only two clock cycles despite the extensive pipelining employed in the chip's architecture and is independent of word length. The reason is an arithmetic scheme used in the chip's architecture which calculates the most significant bits (MSBs) first – unlike traditional approaches which start at the least significant bit (LSB).

Professor McCanny says MSB-first arithmetic offers significant performance benefits and these are most apparent in high speed systems that require some form of pipelining. "If MSB-first arithmetic is used in a pipeline then, crucially, you do not have to wait until the end of the pipeline to begin using the result," he said. "This is how you can reduce the latency of feedback loops.

The outcome is that for signal processing operations that are recursive in nature (hence which require a feedback loop) the sampling rate can be lower to attain a chosen performance, or the silicon can operate at much higher sampling rates than would otherwise have been possible.

The breakthrough at Belfast University was to realise that MSB-first arithmetic – made possible by use of a signed binary number representation – could be implemented on conventional 'carry-save' arithmetic circuits widely used in digital signal processing systems. Carry-save arithmetic is inherently redundant making it an ideal fit to an MSB first scheme. Also, these circuits need only conventional binary numbers and, hence, would not require special conversion circuitry.

The IIR chip comprises two biquad filter sections (since any order IIR filter can be built from cascaded biquad sections) with each section integrating four multiply-accumulate (MAC) blocks and a shifter circuit. Carry-save and MSB-first arithmetic is used inside the MACs.

The MAC blocks generate the most significant digits of the result after just two clock cycles which can be fed back immediately and used in another computation. For this reason the chip can process two separate data streams allowing two independent fourth order IIR filters to be implemented. Both of them can operate at a sampling rate of 15MHz (corresponding to a clock speed of 30MHz).

Professor McCanny says that the success of the IIR filter chip has proved the concept but there are other benefits to be gained from MSB-first arithmetic. "Signal processing operations usually have some truncation or rounding process after a calculation in which the LSBs are thrown away," he said. "So why start at the LSBs? It would be quicker and less computationally intensive if the MSBs were done first." The arithmetic can also be successfully extended to other mathematical functions such as division and square root extraction. "In a processor the multiply operation is typically much faster than division or square root operations," said Professor McCanny.

"But, if you think about it, a square root calculation is inherently most significant digit first. Using our technique we can perform division and square root calculations in times comparable to a multiply operation."

However, Professor McCanny thinks the efficiency of the technique is perhaps its biggest advantage. The filter chip contains 30,000 gates and can perform up to 300 million multiplications and additions per second. That is 10,000 per gate which is impressively high." *Simon Parry* ■

Plasma leaves soldering out in the cold

Cold plasma technology can be used to remove organic contaminations from pcbs, eliminating fluxing and post cleaning in production.

The process leaves pcbs clean, dry and solder ready says German firm Grasmann.

To work, a vacuum chamber with a pressure of 1000Pa is needed, incorporating a high frequency generator that ionises oxygen and passive tetrafluoromethane (CF_4) gas.

This plasma cloud oxidises organic compounds on the solder surfaces leaving them ready for wave soldering. Even small voids are penetrated so that through holes are correctly conditioned.

Low temperatures from 30 to 100°C may be used since the free wavelength of the elemental parts is very high.

This treatment can be used on any components and has no visible effect on plastics surfaces; ram chips are already prepared in plasma for printing.

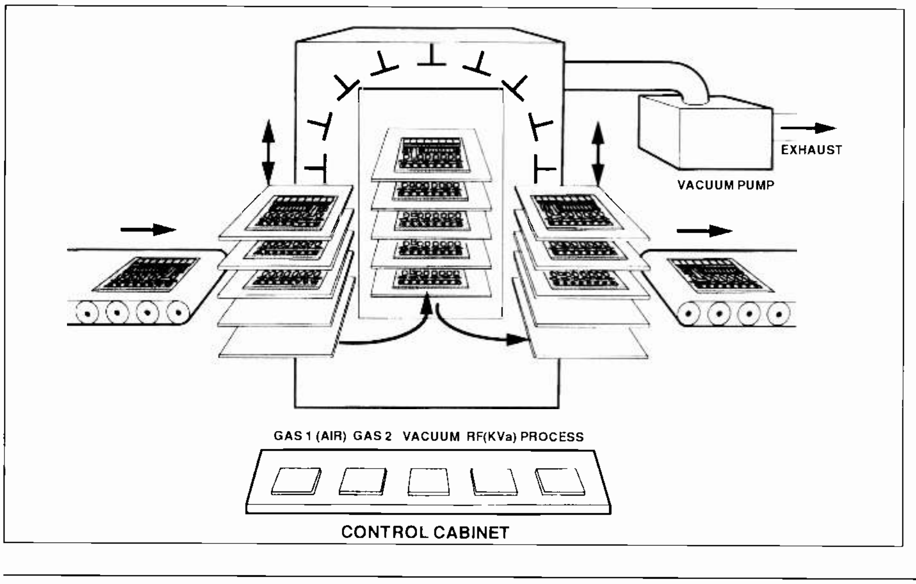
And the treated solder surface degrades very slowly so that fast transfer between plasma treatment and soldering process is not essential.

Grasmann has developed a two-stage production machine available in the UK from Parkheath of Cardiff. It comprises a plasma preparation unit and a soldering module. The plasma unit can be used separately with an existing inert atmosphere soldering line.

Tests on the process include metallographic analysis, REM photographs, x-ray analysis, temperature cycle, shear, and wetting angle.

The firm describes beta test results as "excellent" saying they resulted in "yields of perfect pcbs as high as could be achieved by conventional methods".

The major benefit though is savings in materials and machine cleaning time, which the firm claims gives a projected payback period of two years.



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VIEWDATA SYSTEMS Brandnew units made by TANDATA complete with 1200/75 built in modem, infra red remote controlled keyboard. BT approved, Prestel compatible, Centronice printer port, RGB colour and composite output (works with any TV) complete with power supply and fully cased. Price is just £20 **REF: MAG20** Also some customer returned units available at £10 each **REF: MAG10**

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***FM CORDLESS MICROPHONE** Small hand held unit with a 500' range! 2 transmit power levels. Reqs PP3 9v battery. Tuneable to any FM receiver. Price is £15 **REF: MAG15P1**

LOW COST WALKIE TALKIES Pair of battery operated units with a range of about 200'. Ideal for garden use or as an educational toy. Price is £8 a pair **REF: MAG 8P1** 2 x PP3 req'd.

***MINATURE RADIO TRANSCEIVERS** A pair of walkie talkies with a range of up to 2 kilometres in open country. Units measure 22x52x155mm. Complete with cases and earpieces. 2xPP3 req'd. £30.00 pair **REF: MAG30**.

COMPOSITE VIDEO KIT. Converts composite video into separate H sync, V sync, and video. 12v DC operation. £8.00 **REF: MAG8P2.**

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PHILIPS LASER 2MW helium neon tube. Brand new full spec £40 REF: MAG40. Mains power supply kit £20 **REF: MAG20P2.** Fully built and tested unit £75 **REF: MAG 75.**

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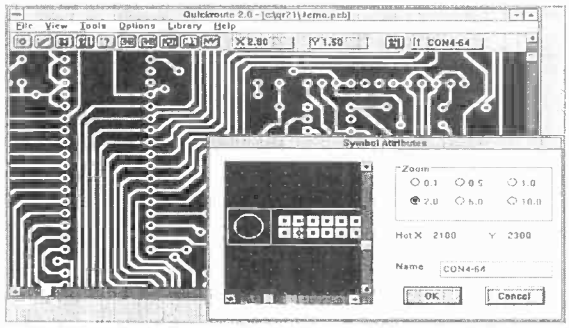

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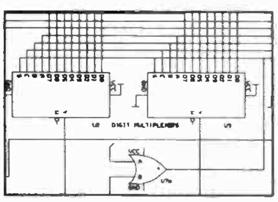

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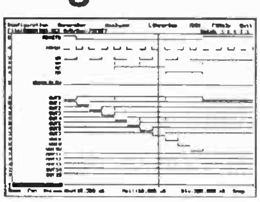

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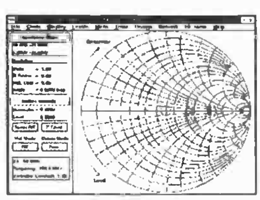

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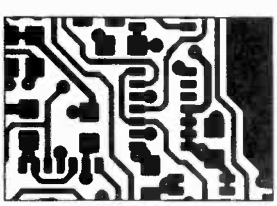

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CIRCLE NO. 106 ON REPLY CARD

Macho behaviour that could unlock the universe

Three separate groups of astronomers say they have tracked down the mysterious dark matter that is believed to permeate the universe.

Cosmological theory has long suggested that there is much more to space than meets the eye – at least 90% more. So far this dark matter has remained elusive, with evidence for it coming largely from its effect on the universe we can see.

For the cosmos to behave as it does, scientists believe there must be something exerting a pronounced gravitational effect, a phenomenon that dominates the movements of the stars and something that will ultimately determine the fate of the universe.

Charles Alcock, Head of astrophysics at the Lawrence Livermore Laboratory in California, says that current measurements of the mass of our own Galaxy exceed the mass of what we can directly observe by a factor of between 10 and 20. So where is all this "missing mass"?

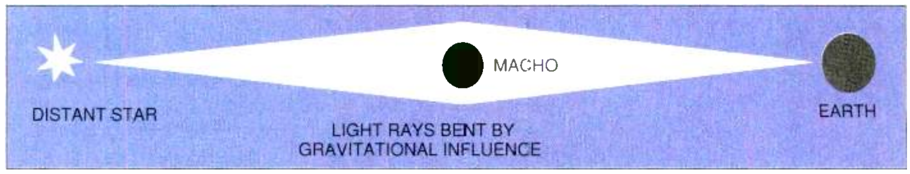
The first (and obvious) conclusion is that it can not exist in the form of stars or gas clouds, because if it did, it would not be dark. Nor can it exist as dust clouds, because it would periodically eclipse other, more luminous, objects. Cosmologists have therefore proposed the existence of several forms of exotic matter, such as axions, massive neutrinos and wimps – weakly interacting massive particles.

There is no real evidence that any such particles actually exist. So attention has turned to the search for more conventional forms of dark matter, objects such as planets and defunct stars. Real evidence for the existence of such objects in a halo around our galaxy has led astronomers to coin the memorable acronym for non-radiating things around the galaxy: machos - massive compact halo objects.

Back in 1986, Princeton Astronomer Bohdan Paczynski (with colleagues at the University of Warsaw and the Carnegie Institute in Washington) suggested machos might be detected by an effect called microlensing.

The idea is simple, and depends on a fact recognised earlier this century by Einstein, namely that a gravitational field can act as a sort of converging lens on light from a distant source. Astronomers have already discovered examples of what purport to be two identical stars, but which are actually a single star whose rays are bent along two different paths by the gravity of an intervening galaxy.

Paczynski reasoned that a macho would have a similar but less pronounced effect. Being small, it would not split the image of a distant star completely, but it might



How a macho results in microlensing – and points to the presence of dark matter.

modulate its intensity considerably as it passed between that star and Earth. Teams from Australia, France and the USA have all now simultaneously announced the discovery of what appears to be the first observations of microlensing. The groups found their evidence for dark matter from computer analyses of overlapping sky images.

Paczynski's group published its findings in the quarterly journal *Acta Astronomica*; the US/Australian and French groups gave details at scientific conferences in Italy, followed by publication in *Nature* (Vol 365, No 6447). The fact that only a few microlensing events have been observed is not surprising, considering the precise alignment necessary. Paczynski calculates that the odds of any star being microlensed is about one in a million – even if 90% of the Universe consists of such stuff.

Ken Freeman of the Australian team at Mt Stromlo observatory says that, for each team to have found a single event strongly suggests that the halo around the galaxy is made up very largely of this kind of object, probably a dim star known as an M-dwarf.

Organic leds offer bright prospects

Organic materials are set to make further inroads into electronic devices, following the announcement of a massive increase in the efficiency of polymer leds.

Polymer leds were first created by a Cambridge group in 1990 using PPV poly (*p*-phenylene vinylene) sandwiched between electrodes with a forward bias of 14V. This arrangement emitted yellow/green light with an internal efficiency of 0.01%. The system worked, but only just. For every 10,000 electrons injected into the material, only one caused the emission of a photon. Since then, the Cambridge team, from the University Chemical Laboratory and the Cavendish Laboratory, have made a leap forward. Using ingenious techniques they have raised the efficiency of their polymer light-emitting diodes to 4%, higher than for many inorganic leds.

First step in this search for greater efficiency lay in confining the singlet exciton generated in the polymer when opposite charges meet. In a led, these singlet excitons should ideally decay by emission of a photon. But what they often do is migrate to a quenching site where they decay without emitting any radiation.

Last year the Cambridge scientists published details of a co-polymer system designed to confine the singlet state and prevent non-radiative decay. Efficiency rose to 0.3% and it was possible by clever chemical processing to produce two colour emission (*J Am Chem Soc*, 1993, Nov 3). Further improvements came about by tackling the fact that, for most semiconducting polymers, holes are much

Patterned films of copolymer viewed in fluorescence. These are not the first polymer LEDs but they represent a significant step forward in terms of efficiency.

more easily injected than electrons.

Addition of a special electron-transporting layer was one ingenious way by which the team lifted the efficiency figure to 1%. What the Cambridge group have now done is to balance charge injection by chemically increasing the electronegativity of the polymer.

But the most recent development (*Nature*, Vol 365, No 6447) shows how cooperation between chemists and physicists can bring breakthroughs. Chemists Stephen Moratti and Andrew Holmes used what is called a Knoevenagel condensation to prepare co-polymers with cyano groups substituted along a PPV backbone. Physicists Neil Greenham, Donal Bradley and Richard Friend then designed a bi-layer device using this material, in conjunction with PPV and stable aluminium electrodes, to produce working leds.

The team attributes the 4% efficiency of the latest devices to the significant charge confinement at the interface between the PPV and the cyano-substituted material.

Statistics complicate power line cancer search

Publication of more studies showing a positive, though small, correlation between AC fields from power lines and cancer means the still-inconclusive debate is set to rumble on.

Two studies, one in Finland and the other in Denmark (*The British Medical Journal*, Vol 307, No 6909) looked at children living near overhead power lines where exposure to an AC magnetic field was an order of magnitude greater than the level normally found in a typical home away from overhead power lines. They found the cancer risk was increased.

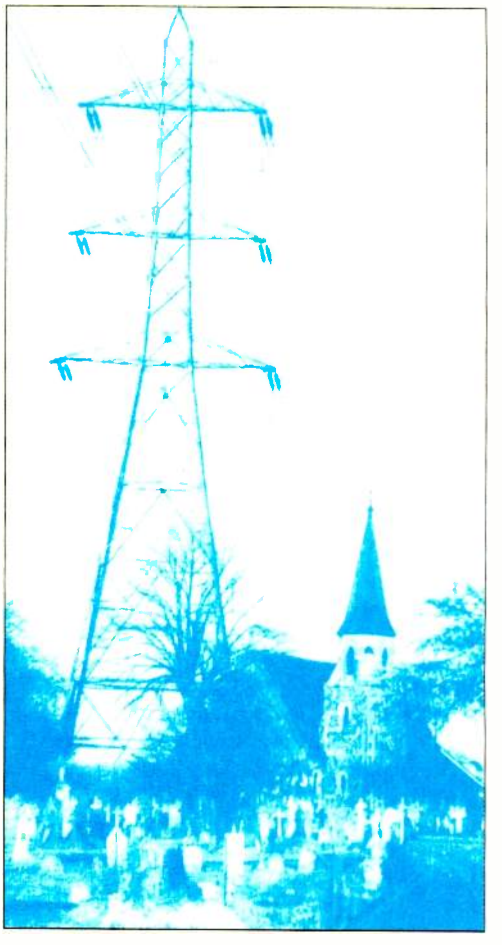
But Jorgen Olsen of the Danish Cancer Society and principal author of one of the studies admits that research in this area is made extraordinarily difficult by the fact that people frequently move home and that, at any one time, fewer than 0.5% of the childhood population live near power lines.

To make the statisticians' job even worse, cancer in children is extremely rare – regardless of where they live. With those provisos, Olsen explained in an interview for the BBC World Service that: "For those children who live near power lines [in Denmark] there is a significantly increased risk of childhood cancer when they are exposed to a magnetic field of more than 0.4μT."

To avoid undue alarm, Jorgen Olsen emphasises that there is no hard evidence to implicate the AC magnetic fields directly. It could, he says, be some socio-economic factor or exposure to other factors that are merely associated with power lines. It is also worth pointing out, he says, that if magnetic fields are responsible, the risk must be extremely small. Otherwise, the widespread introduction of electricity 50 years ago would have led to a massive public health problem.

Olsen and his colleagues have checked the registration of cancer deaths in Denmark since the 1940s and as he says with blunt conviction: "We don't see any increase."

To make the whole scenario even more intriguing, there are reports from Russia of 100Hz magnetic fields being used to *treat* cancer. Researchers at the AZ Science and Production Association are said to have developed a "magnetoturbotron", a device rather like the stator of a large AC motor. The patient sits inside the device and is exposed to a powerful field that rotates at 6000rev/min. The rotating field produced is claimed to suppress the growth of various kinds of cancerous cells, especially those of the thyroid, breast and skin. The patient apparently sits inside and is given a dose appropriate to the condition, usually about 40min. No detailed results are available and no mechanism is suggested. The only curious observation is that the patient's temperature falls by one degree during the treatment.



Could a Magic Flute make you smarter?

Developing a taste for classical music could improve your intelligence… at least for a short while. But don't listen while you work, according to the Center for the Neurobiology of Learning and Memory at the University of California, Urvine, or you could overload your neurones.

The conclusions are the results of studying the IQs of 36 college students before and after they had listened to a variety of audio tapes.

Those who listened to a Mozart piece experienced a temporary IQ boost compared to those who had heard either a relaxation tape or nothing at all. Researcher Frances Rauscher, who led the study (*Nature*, Vol 365, No 6447) says that the results were conclusive beyond any doubt.

Tests were designed to measure one particular aspect of intelligence – spatial ability – and a typical example would be to imagine how a piece of paper with complex folds would look when unfolded.

All 36 students completed the exercise several times, following a period of silence, after listening to a relaxation tape or after listening to a recording of Mozart's Sonata in D major for two pianos (K448).

The IQ improvements were so marked that Rauscher estimates the odds of it happening by chance are only two in a thousand.

Lots of unanswered questions remain. The team still does not know how long the effect lasts. All that can be said is that it is less than 25 minutes.

Why Mozart boosts IQ is also a mystery. The only hypothesis is that the neuronal firing patterns of the brain in both music and in abstract reasoning skills are similar. So if those firing patterns are stimulated by listening to music, then they will be more ready to perform the sort of skills needed for spatial tasks.

Rauscher believes that Mozart is particularly good because the music has a complex structure and is therefore more effective in exercising the relevant parts of the brain. She is now about to undertake experiments to demonstrate another hypothesis: that dull, thumping, repetitive music dulls the reasoning powers.

Eventually the Californian research team plans to carry out studies to find out if a person's taste in music affects the results, and whether musicians differ from non-musicians.

One thing is already abundantly clear: you can not boost your performance at any task requiring abstract thought if you listen to music at the same time. The reason is quite simply that the nerve pathways become overloaded trying to perform two similar functions in parallel.

So the next time someone claims their irritating tzz-t-t-tzz-t-t-tzz personal stereo is helping them concentrate – you can now offer at least two good reasons why it won't.

Life found – but is it intelligent?

Of the 60-odd planets, comets, asteroids and moons encountered by our spacecraft, no mission has ever sent back unequivocal evidence of life. But would we recognise ET life, even if it were there?

This was a question tackled by a team of scientists led by Carl Sagan, Director of the Laboratory of Planetary Sciences at Cornell University. The team decided to turn the usual search for life upside down – and look for it on Earth. They did this with the help of an interplanetary probe that swooped in from space and visited the Earth three years ago.

Fiction? Not at all! The probe in question was Galileo, a spacecraft launched primarily to explore Jupiter. To reach the giant planet, Galileo had to head away from earth, then swoop back, using the Earth's gravitational attraction as a sort of slingshot to gain extra momentum before heading off to the giant planet. It was on this return path that Sagan and his colleagues decided to put its equipment to the test by studying our own planet. They agreed, for the purposes of this study, that life on Earth would be a "hypothesis of last resort".

Galileo analysed reflected light from the Earth to determine the nature of the atmosphere and the surface chemistry. Sagan says: "We saw the continents of the Earth tainted with a strange pigment that absorbs light in a very special way, just beyond the red end of the spectrum." The team had discovered chlorophyll, the green pigment in plants.

They also discovered oxygen in the atmosphere, something that would be hard to explain except for the existence of some sort of life processes.

Where Galileo failed to find any trace of life was when it looked for evidence of artificial structures. In the course of examining 4% of the Earth's surface at a resolution of 1km, nothing was found at all – a cautionary lesson for those who expect to find huge artificial structures on alien planets. But Galileo scored a resounding triumph when it searched the Earth in the radio spectrum.

Scanning the hf region, the probe discovered hundreds of signals with forms of modulation that could not have been generated by any known natural system. These signals, say the scientists, must have been coming from the Earth's surface because their escape was blocked by ionised layers (the ionosphere) in a way that was dependent on the presence or absence of sunlight.

Reluctantly, the team concludes from the Galileo observations that there must be some sort of intelligent life on Earth. A trivial exercise? Not at all. The real lesson is that if we want unequivocal evidence of life elsewhere in the cosmos, we might as well forget photography and chemistry and concentrate on good old short wave radio!

To test how successful we might be at detecting whether there is life on other planets, scientists tried finding it here on Earth via Galileo.

Making less of a meal of image analysis

In theory a computer can solve any problem – given enough processing power. But looking at all the options and choosing the best is a sledge-hammer approach. In the real world, computing power costs money and researchers are for ever striving to develop more efficient software.

At Rochester University in New York, graduate Ray Rimey has been looking at new ways for computer vision systems to analyse images. In the past, researchers involved with artificial intelligence have often overlooked the fact that robots need to be selective in where they put their attention. Ray's work is devoted to structuring which methods the computer should adopt and in what order.

"A computer only has so much processing power," says Rimey. "If it needs to solve a problem in a given amount of time, it needs to prioritise. A doctor analysing a patient could run endless tests costing thousands of dollars but it could take so long that the patient could die. Instead, a doctor uses prior knowledge to decide on tests needed to maximise useful information and minimise diagnosis time," adds Rimey.

Analysing different kinds of place settings for a dining table proved to be a perfect test. Rimey taught his robot to collect visual clues and sequentially gain confidence in its answer. It could tell, for example, whether the setting is formal or informal and whether it was breakfast, lunch, dinner or desert. The method extends to judging whether the table is messy, how many guests there are, and whether they have begun eating.

Dinner service – according to researchers at Rochester in New York, place settings are an excellent test of a robot's analytical capabilities.

The focus of the research is on teaching a processing system how to scan a scene and home in on the most important information. As well as helping set the table, this work is expected to be useful in applications including medical diagnostics and satellite image analysis.

Rimey taught the robot its analysis tricks through extensive programming using decision theory and mathematical constructs know as Bayes Nets. His computer vision system is due to be described in a forthcoming issue of *International Journal of Computer Vision.*

Honeywell is said to be interested in using Ray's ideas to analyse infrared images from roving vehicles. Colleagues of his are also interested in tracking moving objects such as trains and cows. Others are investigating decisions involving both observing and interacting with moving objects, namely herding mechanical sheep. We will be following that one closely.

Research Notes is written by John Wilson of the BBC World Service.

Microprocessor controlled power supply

Adding a microprocessor brings new meaning to the word power in power supply. This cost-effective design from Matthew Rahman and Robin Thick features a user friendly interface.

This design is for those of you who are fed up with tweaking a potentiometer every time you want to set the voltage on your power supply. As described, the system provides microprocessor control for two positive and two negative output supply lines. By breaking the design down into modules however, any combination of output rails can be created.

The design is economical yet comparable to commercial supplies costing many hundreds of pounds. It originally formed part of a project that we undertook as part of our training as air traffic engineers with the Civil Aviation Authority and is fully tested.

Specifications

When implemented in full, the design allows keypad entry of two independent positive and negative voltage outputs, each programmable to a resolution of 100mV from 0V to 25V. All outputs can deliver nominally about 1.2A across the whole voltage range. Below 18V current capability rises to 1.5A.

Each output can be monitored if need be. By feeding the monitoring information back to the microprocessor, software correction can be applied to the outputs to stop the voltage drifting. This feature also forms part of a digital voltmeter function included in the software.

A standard liquid-crystal display module displays all operations and other information. It is possible to use a larger display without modifying the design, but the software held in rom may need to be modified.

Other features when the full design is used with our software include audible feedback for the keypad, output voltage tracking and program memories to store all your settings. Single stepping of the voltage from the keypad in either 100mV or 1V steps is also possible.

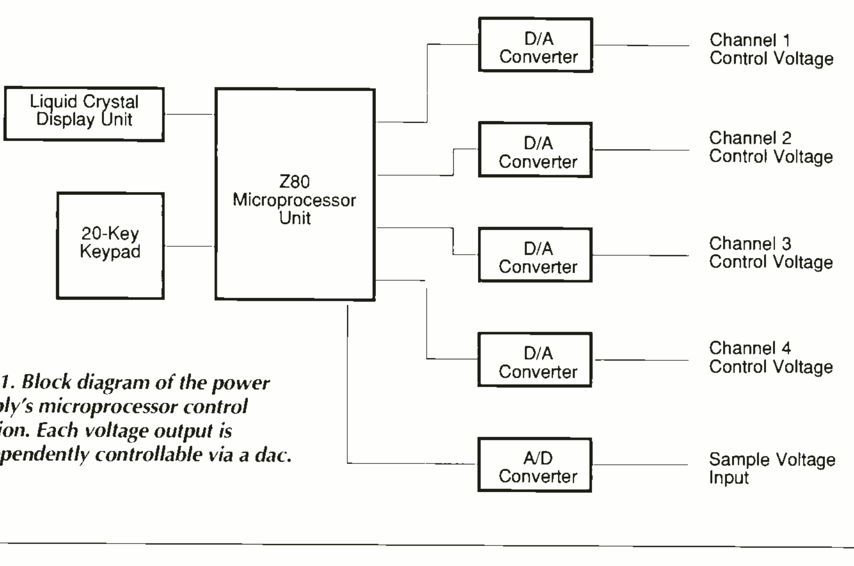


Fig. 1. Block diagram of the power supply's microprocessor control section. Each voltage output is independently controllable via a dac.

System overview

At the heart of the design is a *Z80* microprocessor with 8Kbyte rom and 2Kbyte ram. **Figure 1** is a basic block diagram of the microprocessor control unit showing that each voltage output can be independently controlled via a digital to analogue converter, or dac.

Sampled input voltage is in fact multiplexed and can be any one of the output voltages selected by an analogue switch controlled by the processor. This has the advantage of reducing costs by requiring only one analogue to digital converter, ADC.

There are 20 keys on the entry keypad. All of the decoding is done by software to simplify the keypad scanning electronics relatively simple.

The liquid crystal display is a 2-line-by-20-character module. We recommend a backlit type but a standard reflective type could easily be used.

Figure 2 shows a block diagram of two of the four voltage regulators used in this design. Channels 1 and 3 are positive outputs while channels 2 and 4 are negative, each with current limited outputs. These circuits will be discussed later.

Microprocessor unit

Figure 3 shows the circuit diagram of the main microprocessor unit and its related control circuits. The circuit is fairly standard and operates as follows.

Clocking of the *Z80* CPU, IC_1, at 2MHz is performed by the crystal oscillator circuit based on IC_4. This frequency is divided down using a ripple counter, IC_5, to provide a 125kHz clock for the analogue-to-digital converter. Note that it may be necessary to tweak the variable capacitor C_2 to obtain the correct pulse shape for the *Z80*.

On power-up, the reset line on pin 26 of IC_1 is pulsed low by means of C_1 and R_6. All unused control pins are taken to the positive supply via 10kΩ resistors. The clock pin is also pulled up via R_5 to ensure that the minimum 4.4V is present for a high pulse.

Address and data lines are connected conventionally to the 8K rom, IC_2, and 2K static ram, IC_3. Addresses for these and other devices are decoded by IC_7. This IC is a 3-to-8-line decoder dividing the 64K address space into 8Kbyte block outputs, used to select external devices when addressed. The ram only occupies 2K of address space and has not been fully decoded for ease of design. As a result, the ram is shadowed throughout the second 8K block. This is not a problem since nothing else occupies any of that block.

A select line for i/o devices, such as digital to analogue converters, and a line for the LCD are also provided by IC_7. A complete memory map of the system is shown under the software explanation later. The ram is battery backed. It holds data about the system and stores several user settings which need to be retained when the unit is switched off.

To prevent data being corrupted when the ram is in standby mode, the select line to the ram's chip select input, CS, is gated via $IC_{8a,b}$ with a line called POWER_STATE from the battery back-up circuit. This ensures that the ram is de-selected when the main power is not present. Circuit IC_8 is powered by the $+V_{bb}$ supply.

Finally, a free-running 555 timer, IC_6, is used to generate a pulse for the processor's interrupt line, INT. It runs at approximately 12Hz with a very small duty cycle to prevent it from still being low when the processor completes the interrupt service routine.

Details about the software used are presented further into the article.

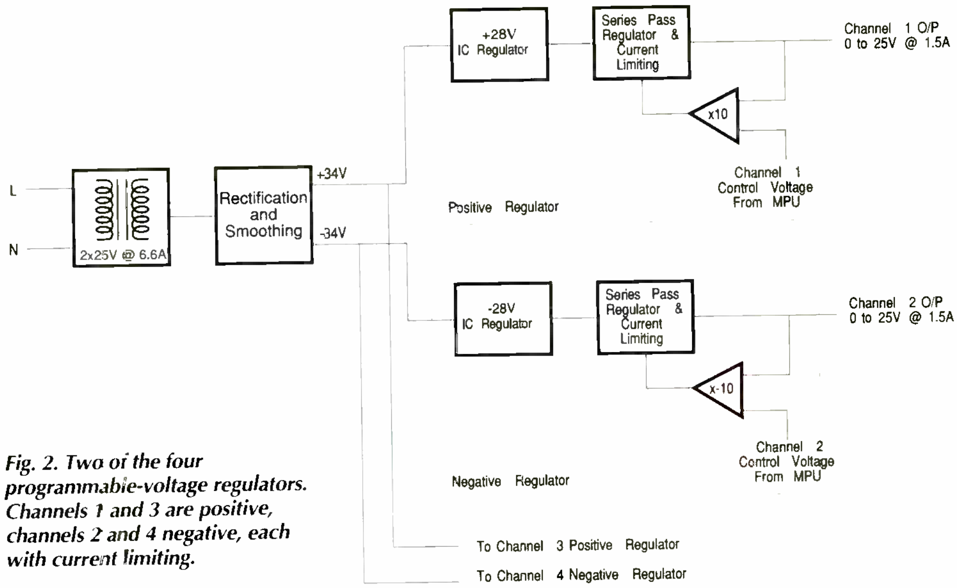


Fig. 2. Two of the four programmable-voltage regulators. Channels 1 and 3 are positive, channels 2 and 4 negative, each with current limiting.

Data input/output

Figure 4 shows the input/output address decoder for the processor. Decoder IC_9 is only

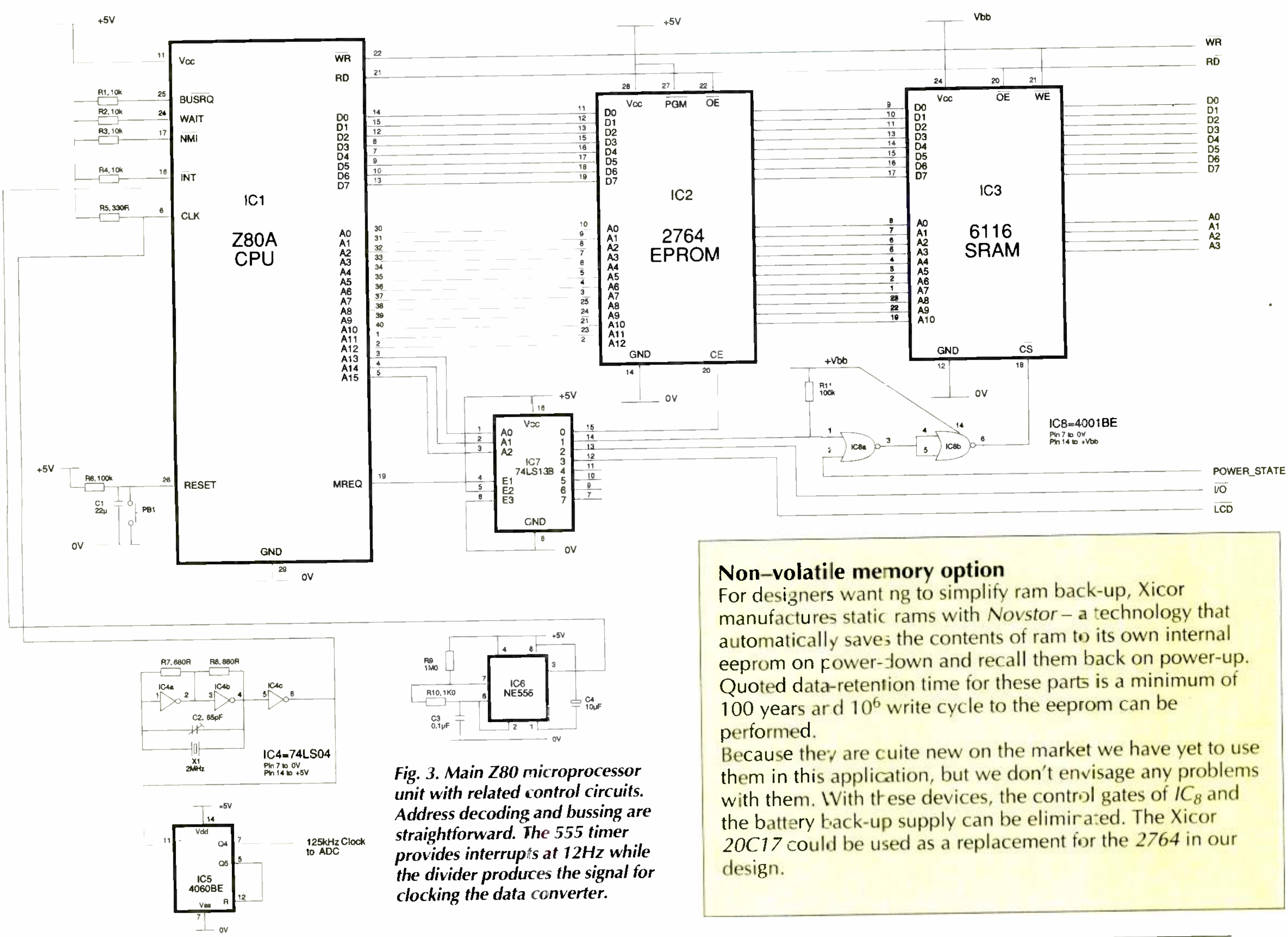


Fig. 3. Main Z80 microprocessor unit with related control circuits. Address decoding and bussing are straightforward. The 555 timer provides interrupts at 12Hz while the divider produces the signal for clocking the data converter.

Non-volatile memory option

For designers wanting to simplify ram back-up, Xicor manufactures static rams with *Novstor* – a technology that automatically saves the contents of ram to its own internal eeprom on power-down and recall them back on power-up. Quoted data-retention time for these parts is a minimum of 100 years and 10^6 write cycle to the eeprom can be performed.

Because they are quite new on the market we have yet to use them in this application, but we don't envisage any problems with them. With these devices, the control gates of IC_8 and the battery back-up supply can be eliminated. The Xicor *20C17* could be used as a replacement for the *2764* in our design.

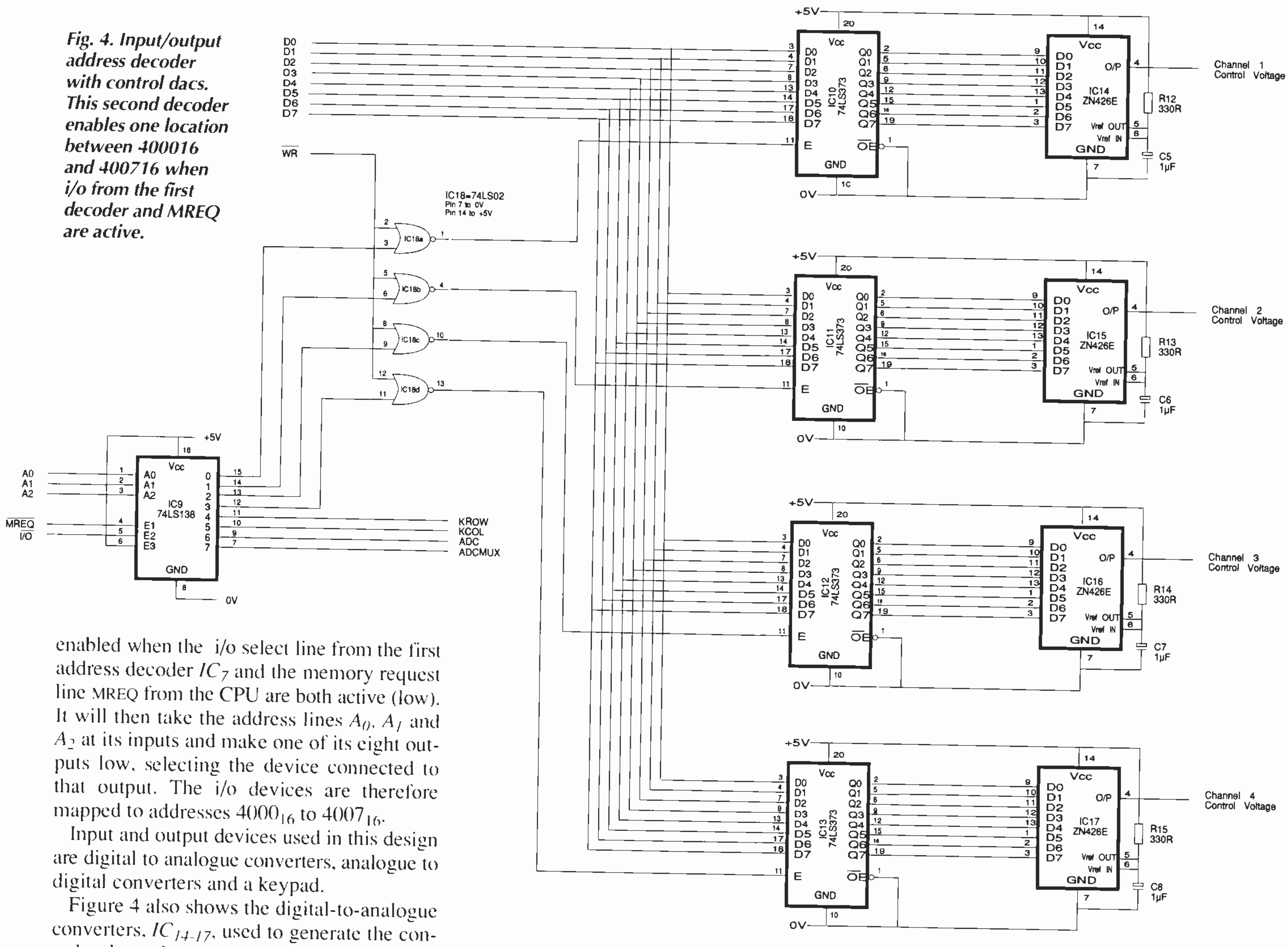


Fig. 4. Input/output address decoder with control dacs. This second decoder enables one location between 400016 and 400716 when i/o from the first decoder and MREQ are active.

enabled when the i/o select line from the first address decoder IC_7 and the memory request line MREQ from the CPU are both active (low). It will then take the address lines A_0, A_1 and A_2 at its inputs and make one of its eight outputs low, selecting the device connected to that output. The i/o devices are therefore mapped to addresses 4000_{16} to 4007_{16}.

Input and output devices used in this design are digital to analogue converters, analogue to digital converters and a keypad.

Figure 4 also shows the digital-to-analogue converters, IC_{14-17}, used to generate the control voltage for each of the voltage regulator circuits. The resistor on each dac, R_{12-15}, is required to load the internal reference voltage and capacitors C_{5-7} decouple the reference. Output from each dac is between 0V and 2.55V depending on the binary value in its data inputs (0 to 255).

The dacs used here do not have internal data latches so the job of latching the data from the processor is performed by *74LS373* octal latches, IC_{10-13}, between the data bus and each dac. When the *Z80* wants to write data to a dac, its corresponding latch is selected by the address decoder which clocks in the data from

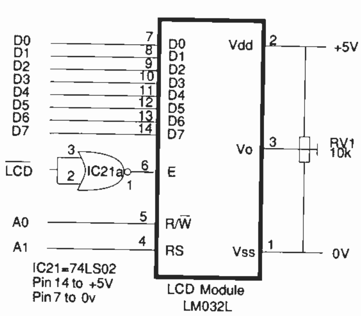


Fig. 5. Interfacing the Hitachi LM032L liquid-crystal display – a two line by 20-character display costing under £20. Viewing angle is optimised via the potentiometer.

the data bus and holds it until changed again by the *Z80*. The nor-gate IC_{18} on the clock input pin 11 of each latch ensures that data is changed only when write line WR is low, i.e. when the processor is actually writing.

It is quite feasible to replace these converters with other types, maybe ones that include latches or are more accurate, so long as the addressing is the same.

Lcd module

This design has the added flexibility of using a dot-matrix liquid crystal display, rather than the standard 7-segment led types found on commercial units. With this, the status of all four outputs can be monitored simultaneously and menus can be used when setting up the system. It is also more user-friendly when entering commands on the power supply's keypad.

Our design uses the Hitachi *LM032L* LCD module, a 2-line-by-20-character display which can be bought for less than £20. Connection of this to the processor is shown in **Fig. 5**.

You are not restricted to using this particular module, and you may want to use a larger 4-line display or any other Hitachi or Densitron display that has a *HD44780* controller IC. We recommend that if you use our software, then the *LM032L* type or its backlit equivalent should be chosen.

Circuit IC_{21a} acts as an inverter to provide an active high ENABLE line.

Keypad scanning

Rather than use a dedicated keypad scanning chip, we decided that a simple scanning circuit could be used under control from the microprocessor.

Figure 6 shows that the circuit uses just one octal latch IC_{20} and one octal buffer, IC_{19}. The processor writes data to the keypad latch and reads the result of any key presses by enabling the buffer to transfer data to the data bus. Details of how the software does this will be explained later.

In addition, the latch will control a 'KEYPAD ENTRY' led and a piezo sounder. Buffer IC_{19} also accepts the BUSY signal from the analogue to digital converter, discussed later.

Layout for the keypad switch matrix can be seen in **Fig. 7**, with the keypad's legend for each key also shown. The keypad used in the our original design was a Maplin 20-way membrane type. Pin connections shown in brackets in **Fig. 7** correspond to this particular keypad.

Output voltage regulation

Final output from the power supply is a regulated, current limited supply from 0 to 25V, providing up to 1.5A.

Figure 8 shows the circuit for one positive and one negative output. The positive regulator works as follows. The positive 34V rail from the mains transformer is regulated by a standard monolithic regulator, IC_{21}, programmed to provide 28V. This is a smooth, noise free output and gives protection against overload from the next stage. Devices $Tr_{1,2}$ and IC_{22} form the final output regulator.

Op-amp IC_{22} takes the control voltage from the dac and amplifies it by 10 to produce an output of 0 to 25V. Transistor Tr_1 current amplifies this voltage using the supply from IC_{21}, while Tr_2 and R_{28} form a fold-back current limiting circuit at approximately 1.5A. Feedback is provided by R_{29} and RV_2.

The negative regulator works in a similar way, except that the control voltage is inverted to a negative value by IC_{24a} before being amplified by IC_{24b}. Note also that IC_{24} uses a positive supply of +5V in addition to its -28V supply. The –28V regulator takes its power from the –34V supply. Heatsinks with suitable compound must be used for all the power transistors and voltage regulators, as a fair amount of heat needs to be dissipated by the devices. Additional cooling can be achieved by adding a small 12V fan. We found using a fan very effective in keeping the ambient temperature low inside the case.

Output voltage is set up using the variable resistors in the feedback circuit of the regulator, $RV_{2,3}$. To do this it requires the control voltage generated by the microprocessor unit. The output that you are trying to set up should be programmed to give a voltage of 25V, by entering it on the keypad. The variable resistor, which should be multi-turn for improved precision, should then be adjusted to give this voltage at the output. The same should be done for 5V.

When 15V is entered very little tweaking should be necessary, and the output should be accurate across the range 0 to 25V with an error of 200mV or so. When setting up the outputs, the correction option should be switched off if using our software.

Capacitors C_{11} and C_{14} are used for suppressing digital noise from the microprocessor. We found that these were best placed directly at the output connectors, inside the case, to eliminate any noise picked up in the wires along the way.

Analogue to digital converter

The analogue to digital converter circuit, **Fig. 9**, is included so that each output can be mon-

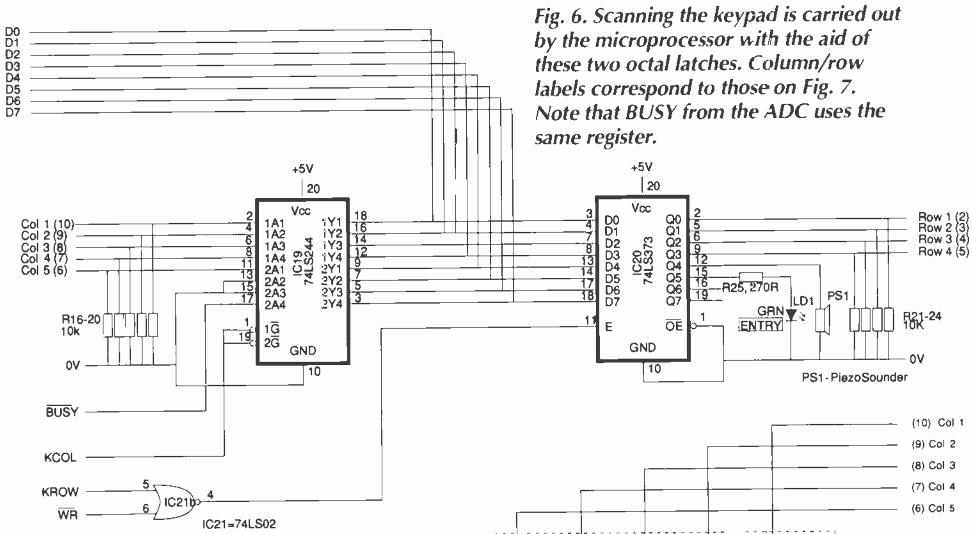


Fig. 6. Scanning the keypad is carried out by the microprocessor with the aid of these two octal latches. Column/row labels correspond to those on Fig. 7. Note that BUSY from the ADC uses the same register.

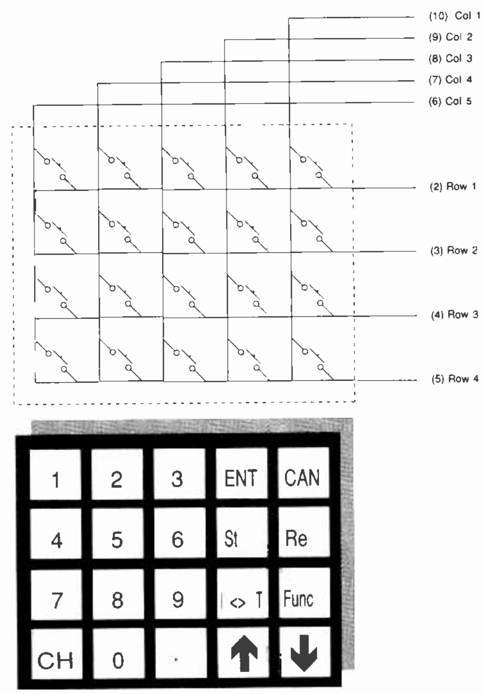
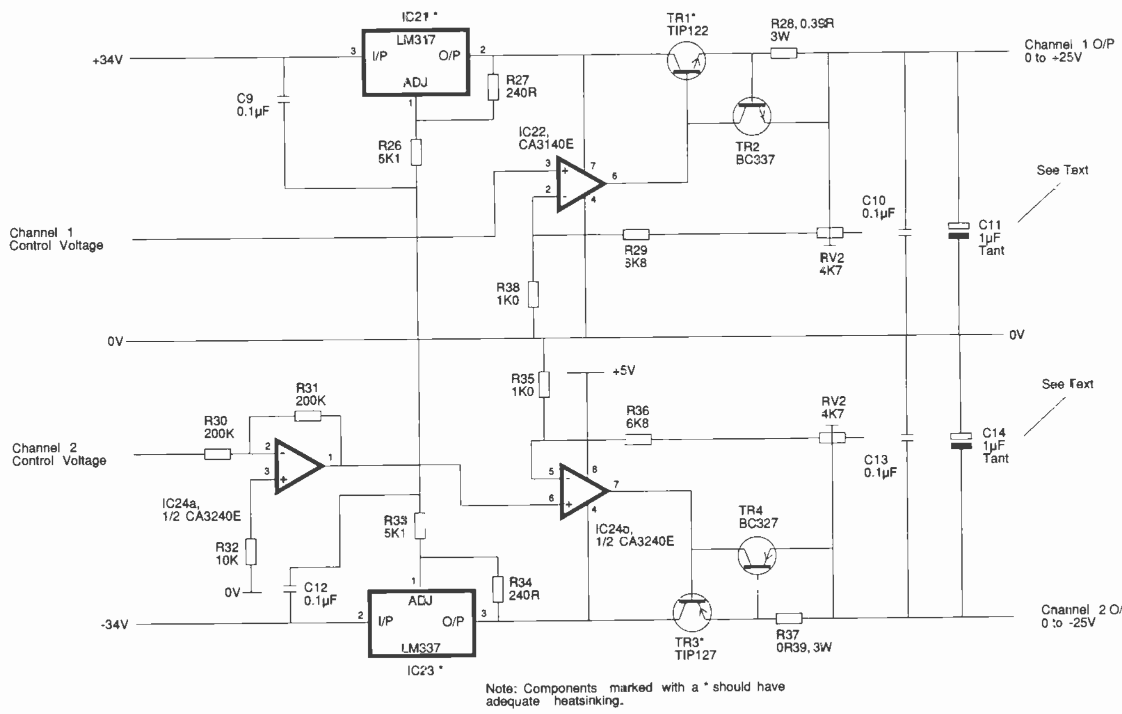


Fig. 7. Layout and legending for the power supply's keypad switch matrix. Using software to read the keypad avoids using a dedicated key decoder IC.

Fig. 8. Channels 1 and 2 of the main output voltage regulation circuitry. Two variable regulators provide preregulation down to 28V. The op-amps and TIP transistors vary output under control of the dacs while the BC transistors add current limiting.



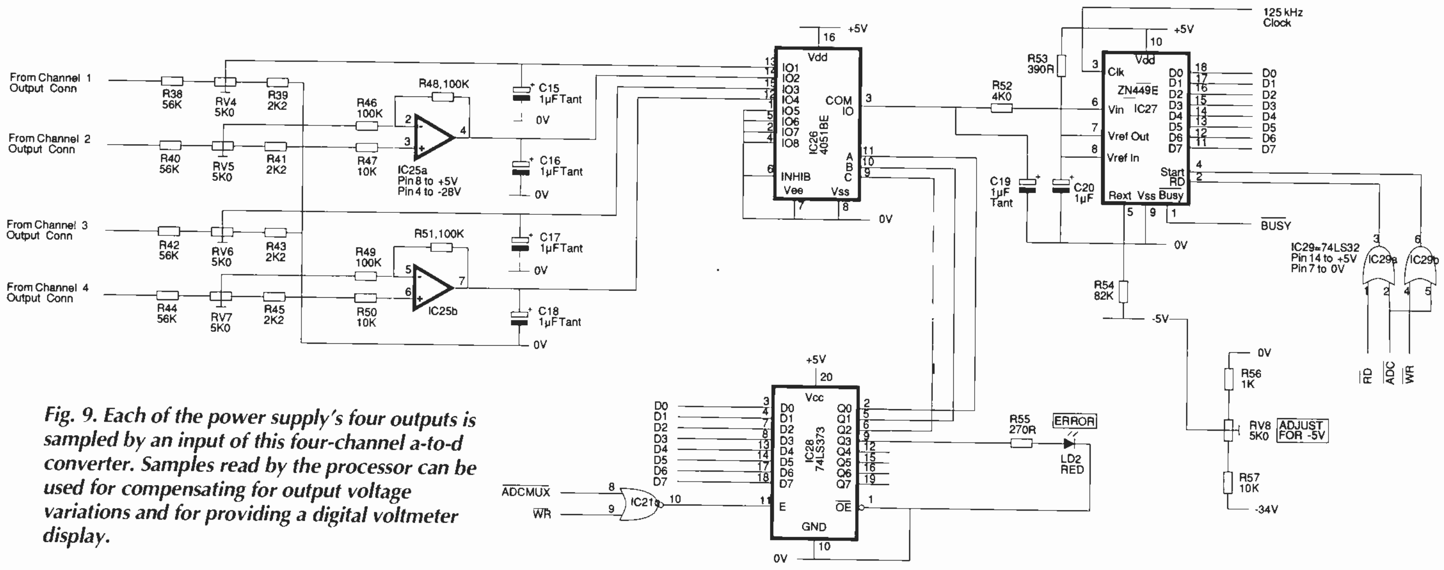


Fig. 9. Each of the power supply's four outputs is sampled by an input of this four-channel a-to-d converter. Samples read by the processor can be used for compensating for output voltage variations and for providing a digital voltmeter display.

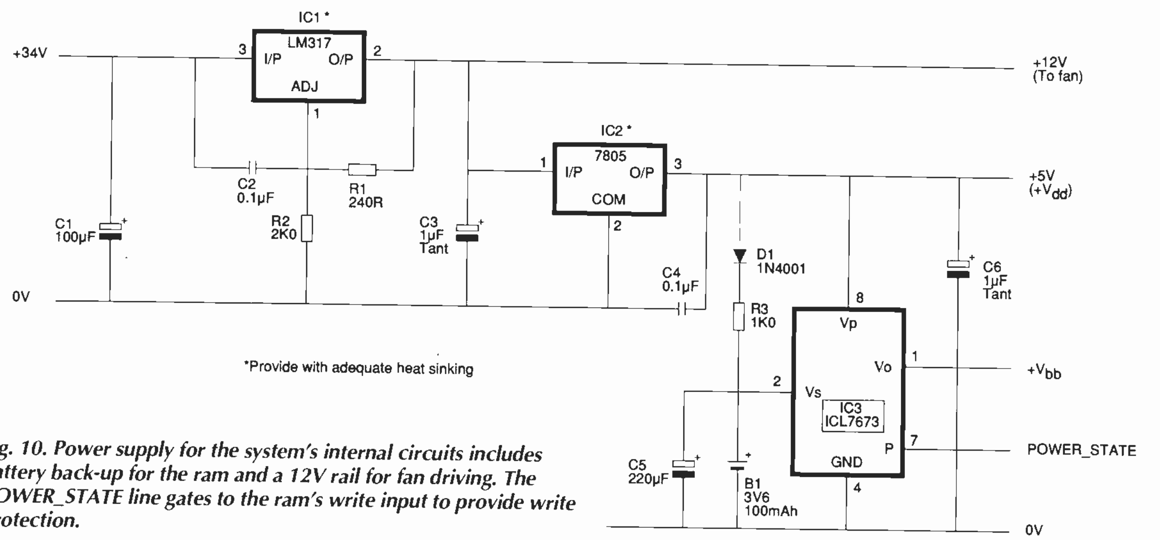


Fig. 10. Power supply for the system's internal circuits includes battery back-up for the ram and a 12V rail for fan driving. The POWER_STATE line gates to the ram's write input to provide write protection.

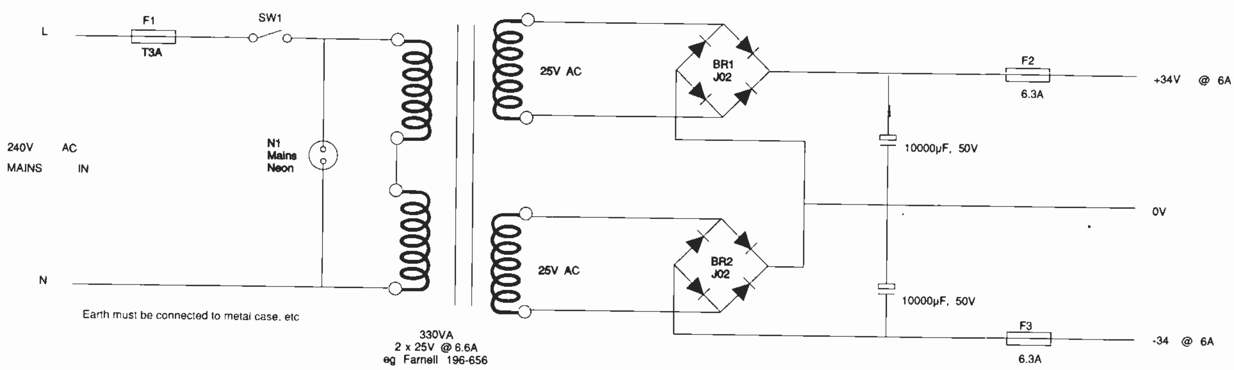


Fig. 11. Mains isolation and rectification. The toroidal transformer we used was conservatively rated. If a smaller one is used, it should be capable of providing at least 4A per winding.

itored and, if required, corrected for small errors. This allows the inclusion of a digital voltmeter function so that the true output voltages can be shown on the display.

First of all, each output voltage is tapped off and attenuated by a resistor network to give a tenth of its value. Current actually drawn from this tap-off is so minimal that it is perfectly feasible to use a resistor divider.

Variable resistors RV_{4-7} should be adjusted so that one-tenth of the channel output voltage appears at the input of the analogue switch. This ensures that the conversion will be fairly accurate. Using multi-turn pots improves the precision at which the voltages can be set-up.

Negative voltages are inverted by IC_{25} to give a positive voltage. Each sample of voltage is decoupled by C_{15-18} to remove any digital noise. The signals are then fed to analogue switch IC_{26}. Via latch IC_{28}, the microprocessor selects the channel to be converted by the ADC, IC_{27}. The latch also drives the ERROR LED.

The microprocessor tells the ADC when to

Microprocessor controlled power supply – features

- User-friendly interface
- Keypad programming of each output
- Switchable audio feedback for keypad
- Settings remembered from when the unit was last used
- Nine memories for storing different voltage configurations
- Single key stepping of voltage in 100mV or 1V increments
- Tracking of positive and negative channels – user-selectable
- Automatic error correction for outputs – user-selectable
- Digital voltmeter optional display
- Options all menu-driven

start converting and monitors the BUSY line, via IC_{19}. In this way it knows when the ADC has finished converting before reading the sampled data. A 125kHz sample clock is used, derived from the system clock, making a conversion period of approximately 75µs.

In the *ZN449* data sheet, it states that the chip needs a negative supply for the tail current of the fast comparator. This is a very low current of about 150µA maximum and can be derived by connecting pin 5 to a –5V supply via an 82kΩ resistor. Rather than generate another power supply regulator just for this, we used a potential divider, $R_{56, 57}$ with RV_8, to derive –5V from the main –34V supply. Potentiometer RV_8 should be adjusted for –5V *without* it being connected to the ADC and R_{54} to prevent any large voltages appearing at pin 5 of the chip.

Improving the accuracy of conversion can be done by using the pin-for-pin compatible *ZN447* or *ZN448* ADCs instead of a *ZN449* but these tend to be more expensive.

Internal circuit supplies

Nearly all of the internal control circuits run from a single +5V supply, apart from the ADC which has been dealt with above. A battery back-up supply is also required for the ram. **Figure 10** is the circuit for the internal supplies.

First of all, the main +34V has to be reduced since it is too high for the *7805* 1A voltage regulator, IC_2, used to power all of the internal circuits. Stepping-down is done by a *LM317*, IC_1, which can take a 34V input. It is programmed for a regulated output of 12V (it is actually more likely to be about 11.7V) at 1.5A. A 12V fan can be driven from this supply, if required. It is probably a good idea to use a fan, as the regulators and power transistors get hot.

Monitoring the +5V supply is a battery back-up switch, IC_3. This will switch in the battery to power the ram and its control gates. It generates a signal telling the ram control gates the state of the power to prevent writes to the ram when the main +5V is down.

The battery we used was a 100mAh 3.6V NiCd type which will probably preserve the data in the ram for many months without the unit being switched on. While the unit is on, the battery is charged via D_1 and R_3.

Figure 11 is the mains input and ±34V supply circuit. For stepping down the mains, we used a toroidal transformer with two 25V windings delivering up to 6.6A each. A smaller transformer will suffice, but it must be able to deliver at least 4A per winding. The 10000µF capacitors are recommended for a smooth supply when drawing large currents.

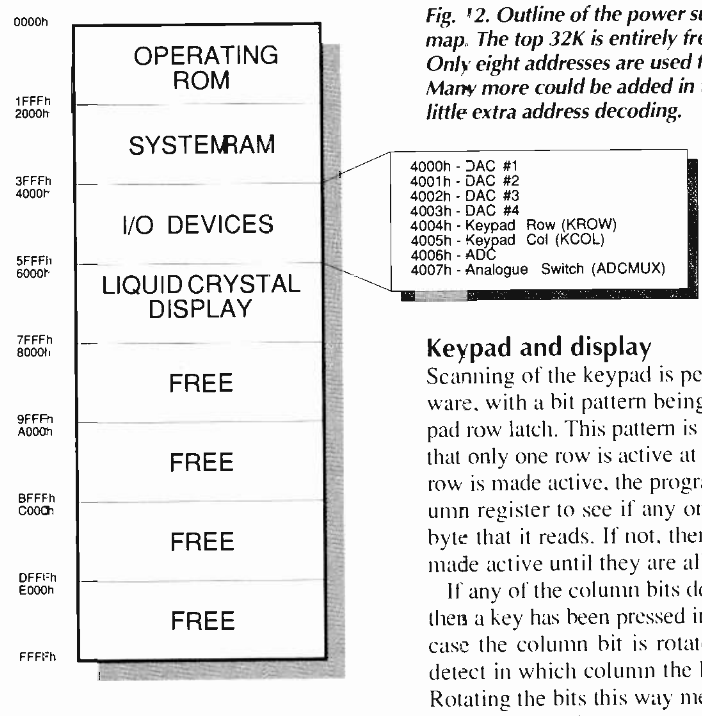


Fig. 12. Outline of the power supply's memory map. The top 32K is entirely free for expansion. Only eight addresses are used for i/o devices. Many more could be added in this area with a little extra address decoding.

Software

A disk is available from *EW&WW* containing all of the software required for a complete system that is even better than commercial systems we have seen. The complete rom dump is 4Kbyte and contains the features shown in the panel.

In **Fig. 12** you can see a diagram outlining the power supply's memory map. The first 8K of address space is taken up by the rom while the next 8K is occupied by the ram, only 2K of which is used). Input/output devices take up the next 8Kbyte but as you can see from Fig. 12, only eight addresses are used. This leaves plenty of room for expansion. The liquid crystal display occupies four addresses from 6000_{16}. Remaining address space is free.

Keypad and display

Scanning of the keypad is performed by software, with a bit pattern being sent to the keypad row latch. This pattern is a walking one so that only one row is active at any time. After a row is made active, the program reads the column register to see if any ones appear in the byte that it reads. If not, then the next row is made active until they are all done.

If any of the column bits does contain a one then a key has been pressed in that row. In this case the column bit is rotated so that it can detect in which column the key was pressed. Rotating the bits this way means that the first bit it comes to, it accepts, avoiding any ambiguity if more than one key is pressed.

Now that the program knows the row and the column in which the key was pressed, it can convert this into a key scan code, say between 1 and 20. This can be done by multiplying the column number (0 to 4) by 4 and then adding the row number, assuming a 20-way keypad is used.

This operation is laid out in the flow chart **Fig. 13**. Suggested layout for the keypad was shown earlier in Fig. 7. Functions of each key is explained in **Table 1**, along with its key scan number.

Programming the LCD is pretty straight forward, but we recommend that the data sheet is to hand so that you have access to all of the commands available. The LCD module used here has four addresses, **Table 2**.

To send a command to the display, you just write a command byte to address 6000_{16}. A list of some of the commands, along with their command byte is given in **Table 3**.

Flow diagrams are shown in **Fig. 14** for the processes of writing a character to the display, (a), and sending a command to the display, (b). Our software includes many subroutines for the display functions, taking all of the hard work out of dealing with cursor positions, displaying strings etc.

LED/beeper driving

Both LEDs and beeper are programmed via existing latches. Address and bit numbers of each device are as follows

Piezo beeper	Addr 4004_{16}	Bit 4	Used for audio feedback and warnings
Entry led	Addr 4005_{16}	Bit 5	Visual feedback for keypad
Error led	Addr 4007_{16}	Bit 3	Used when the system encounters an error

Table 1. Assigning these functions to the power supply's keypad makes for an ergonomical design.

Label	Function	Key scan No
Command entries...		
[CAN]	CANcel current operation	1
[ENT]	ENTer or accept command or entry	5
[ST]	STore present voltage and tracking settings to one of the nine memories	6
[RE]	REcall one of the nine memories	2
[I<>T]	Toggle tracked and independent output modes for channels 1&3 or 2&4, which ever was last selected	7
[FUNC]	Go into FUNCtion mode. Pressing one of the nine number keys will short cut into a function. Pressing [FUNC] again brings up the function menu.	3
[UP]	Increments currently selected output by 1V or 100mV, whichever is chosen	8
[DOWN]	Decrements currently selected output	4
[CH]	Select another CHannel to program. Followed by channel number, 1-4)	20
Numeric entries...		
[.]	Decimal point	12
[0]	Zero	16
[1]	One	17
[2]	Two	13
[3]	Three	9
[4]	Four	18
[5]	Five	14
[6]	Six	10
[7]	Seven	19
[8]	Eight	15
[9]	Nine	11

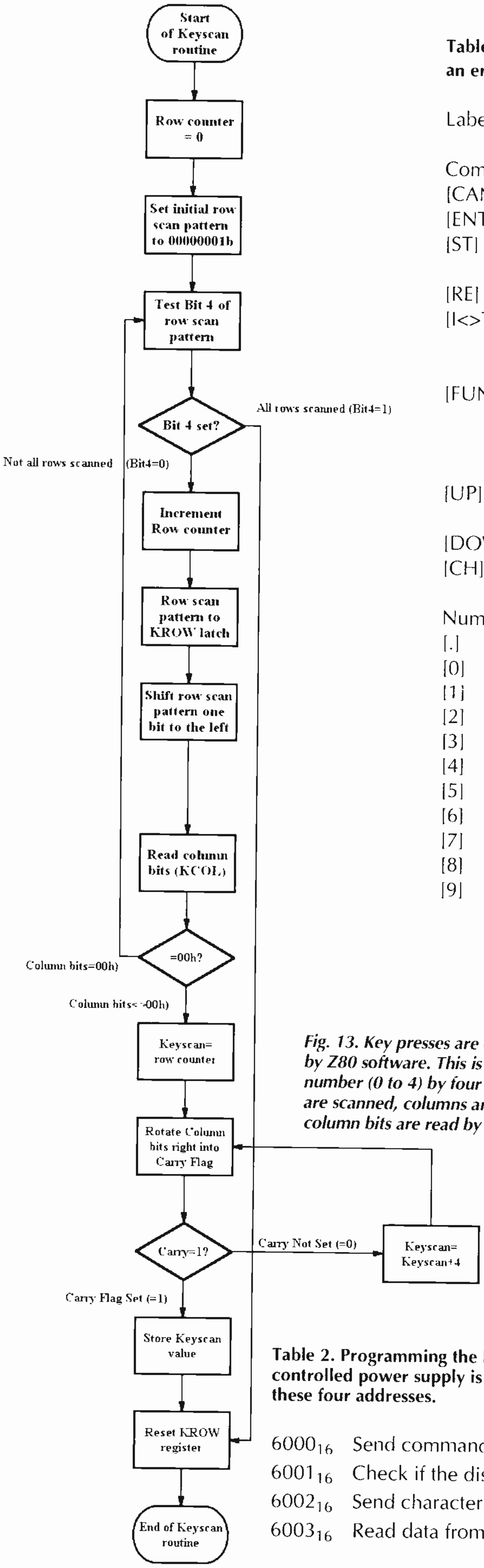


Fig. 13. Key presses are converted to a code between 1 and 20 by Z80 software. This is done by multiplying the column number (0 to 4) by four and then adding the row number. Rows are scanned, columns are read. If a key press is detected, column bits are read by rotating to avoid ambiguities.

Table 2. Programming the LCD used for the microprocessor controlled power supply is strasightforward. The display has these four addresses.

6000_{16}	Send command to display controller	Write
6001_{16}	Check if the display is ready or busy	Read
6002_{16}	Send character to display ram	Write
6003_{16}	Read data from display ram	Read

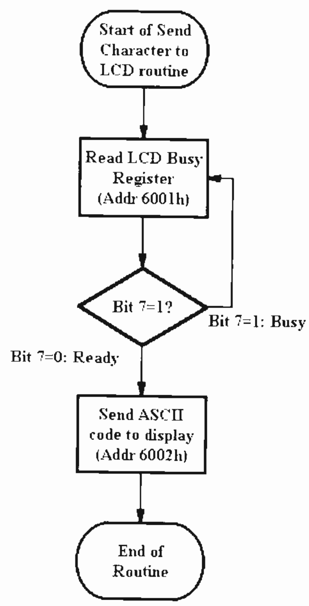


Fig. 14. Writing a character to the display. For sending a command to the display, the routine is identical except that ascii code 600016 is used instead of 600216.

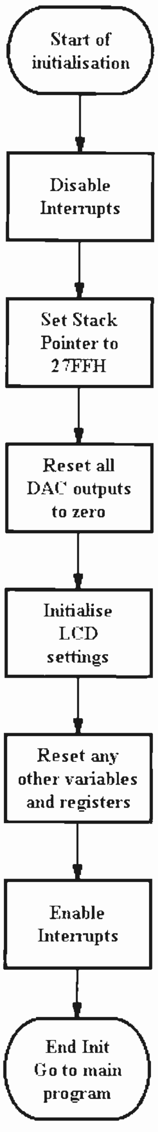


Fig. 15. System initialization. On power up, the processor's variables, registers, stack and interrupts are set up. To prevent spurious outputs, the dacs are reset then set to the voltage they were at when the supply was last switched off.

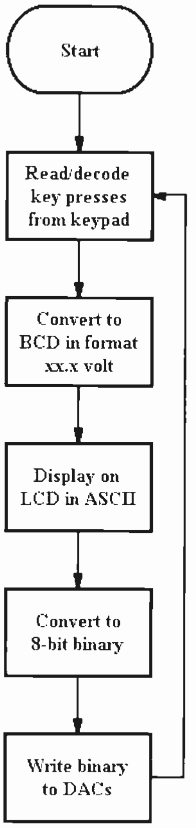


Fig. 16. Entering a voltage for a particular channel. This routine makes use of previous subroutines to read the keypad, display the request and set the voltage.

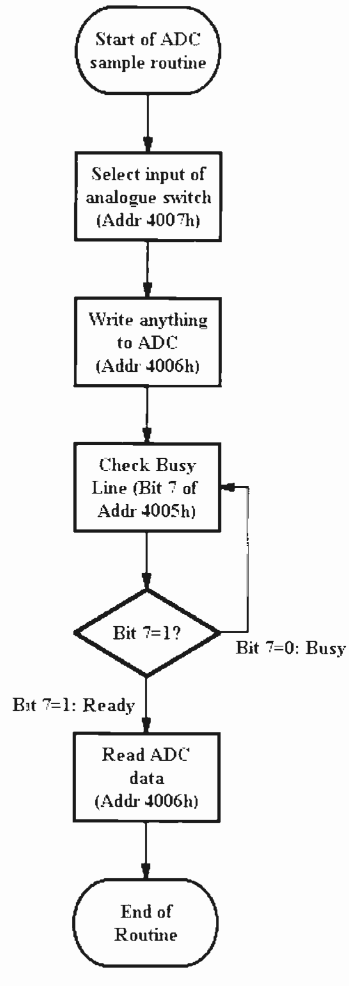


Fig. 17. Output voltage from each channel is read to provide feedback and/or digital voltmeter display. Each of the four output channels is routed via an analogue switch to a single analogue-to-digital converter.

Comprehensive software on disk

A disk containing software and supplementary information can be obtained by sending a cheque or postal order for £10 plus vat to *EW&WW*'s editorial offices at the address in the front of the magazine. Included on this disk is the hex dump in various formats – ascii, Motorola, etc. – for downloading into an eprom programmer. There is also a user manual that can be printed out, in various word processor formats and ascii, together with details of how you can obtain a preprogrammed rom. In addition, an assembly listing is included so that you can modify the program. The assembly listing is fully annotated, and is built up from a library of subroutines. This helps the programmer enhance the software easily as all entry and exit conditions are given for most subroutines. The program includes many arithmetic, i/o and display subroutines.

Table 3. Command codes for display operations. To send a command to the display, you simply write a command byte to address 6000_{16}.

Clear display and home cursor	011616
Home cursor	021616
Set next display data ram address (first line)	801616+column
Set next display data ram address (second line)	C01616+column
Cursor off	0C1616
Display blank (memory retained)	0A1616, 0B1616
Display on	0D1616

These are just a few options. There are many more relating to storing your own characters, changing the cursor type, shifting data etc and these will be found in the manufacturer's data.

System initialization

The first things that should be done when the unit is powered up are to initialise any variables and registers and set up the processor's stack and interrupts. A flow chart for general initialization is shown in **Fig. 15**. Initially, the dacs are reset to prevent spurious voltages from appearing at the outputs on power-up. In our software, the outputs are then restored to their previous state before the unit was switched off.

Figure 16 shows the process involved in entering a voltage for a particular channel. Routines are needed to decode keypad entries and error-check the entries, ensuring no illegal values are entered. This entry would then be converted to BCD for storage and conversion to ascii is required to echo entries to the LCD. Finally, the entered voltage has to be converted to an eight-bit binary number ready for writing to the appropriate dac address location.

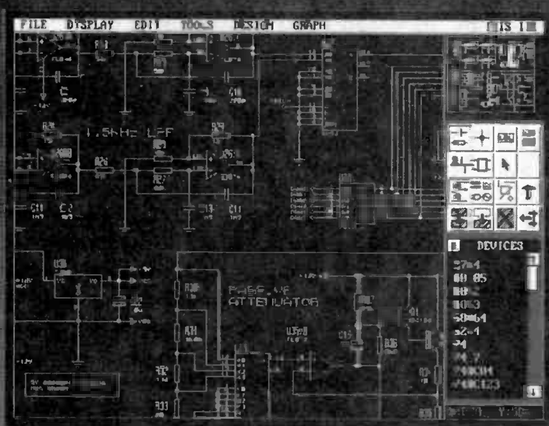
Adc sampling

Figure 17 shows the process of sampling a voltage via the analogue to digital converter. First, the analogue switch should be programmed to select the correct input. It may be a good idea to introduce a short delay of, say, a few milliseconds, to allow the voltage to settle. Conversion can then be started by writing any byte to the ADC. The status of the ADC can be monitored by reading bit seven of address 4005_{16}. When it is set, data is available for reading at address 4006_{16}.

By using the above functions, a more simple or a complex system can be built up with whatever features you want. There is plenty of expansion space, in regards to memory addressing, for adding features. For example, an RS232 interface could be added so that the unit may be connected to a PC for use as automatic test equipment. We are currently working on such an interface at the moment. ■

PROTEUS

The Complete Electronics Design System



Schematic Capture

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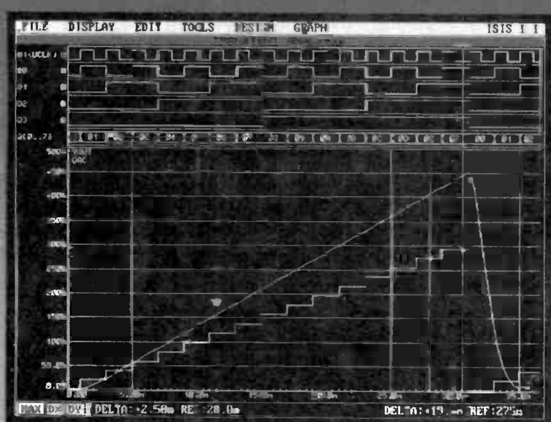
- Hierarchical Design.
- Extensive component/model libraries.
- Advanced Property Management.
- Seamless integration with simulation and PCB design.



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- Non-Linear & Linear Analogue Simulation.
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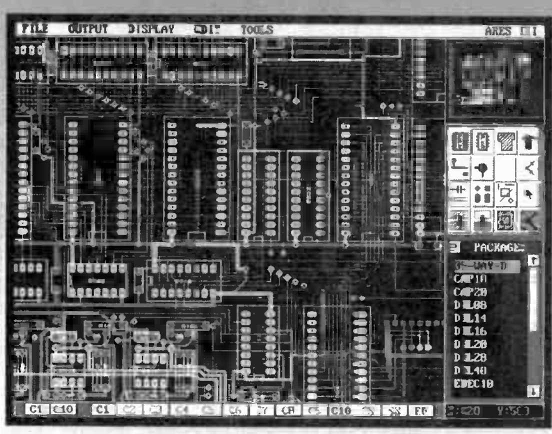
- Partitioned simulation of large designs with multiple analogue & digital sections.
- Graphs displayed directly on the schematic.



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Proteus software is for PC 386 compatibles and runs under MS-DOS. Prices start from £475 ex VAT; full system costs £1495.
Call for information about our budget, educational & Windows products. All manufacturers' trademarks acknowledged.

CIRCLE NO. 108 ON REPLY CARD

PC ENGINEERING

A suitable CASE for development?

For high-end applications, designing software via effective but expensive computer-aided engineering tools is becoming standard practice. John Anderson looks at Select Yourdon – a new CASE tool within the reach of small businesses.

Most of the software I review is intended to help design hardware. This month's review discusses a software design tool generically referred to as a computer aided software engineering, or CASE, tool. The term computer aided software engineering describes a range of tools aimed at formally describing and documenting computer software before – and during – its production.

Installation and manual

Called *Select Yourdon*, the package comes as a single disc together with a 250 page paperback manual. Installation follows the usual windows set-up routine, with the license identification being entered the first time the software is called up.

On running *Yourdon* I sometimes experienced Windows exception errors, but selecting the 'ignore' box started the software. The software was reinstalled to determine whether there had been an error at that stage but to no avail.

Tutorial

The tutorial represents a large section of the manual amounting to over 150 pages. With a volume of material like this, you would expect that the manual would cover the fundamentals of CASE and the ideas behind formal software control methodology. However this is far from the case.

Much of the tutorial is taken up with describing the obvious – how to click on a windows bar, how to insert an object (click on insert) etc. So if you need some background material on this subject don't expect to learn the technique from the *Select Yourdon* documentation. On the other hand, there are some good examples in the tutorial, and working through these should give a good idea of how the system operates.

As you would expect, full Windows-style help is available on screen.

Diagrams

Select Yourdon uses two types of diagram – one type for contexts and one for data flow. Context diagrams show how the information flows between the system being specified and the external entities. Data flow diagrams are the primary tool for depicting the functional requirements of the system being analysed. They partition these requirements into processes interconnected by data flows. In a CASE tool, it is this formal decomposition of complex programs into clear routes of data flow that enables formal control over software development and maintenance.

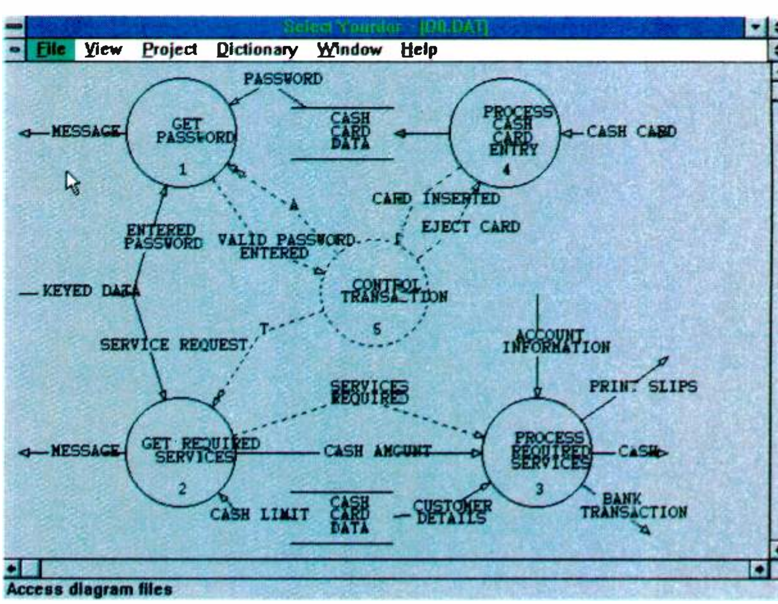
Diagrams are generated by selecting specific data entities from the menu, and then adding the flows between them. The diagrams can be arranged on the screen, and on page, by selecting an item and dragging it with the mouse. Flow lines move accordingly.

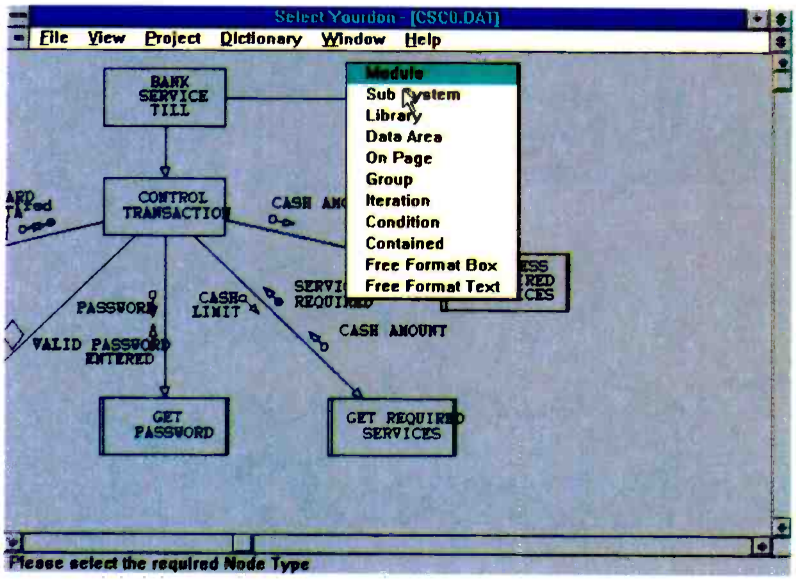
Unfortunately, the drawing outlines and the text fonts are not always scaled together properly. This can result in an unpleasant display with the text completely out of proportion to the boxes which should contain it.

Case background

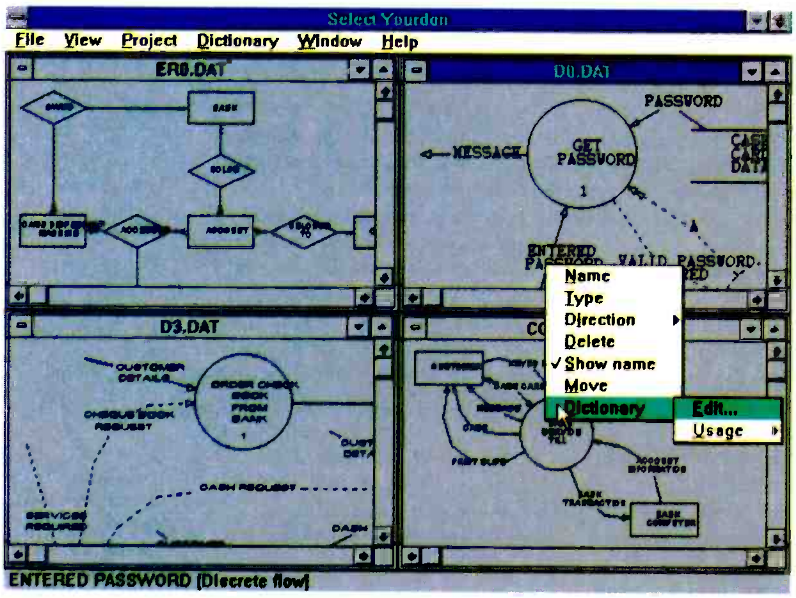
CASE is an embodiment of structured programming methods. It has been developed over the past twenty years in response to the need for better control over software

Writing software by linking action blocks makes structured programming unavoidable. This example of data flow is control software for a bank service till.

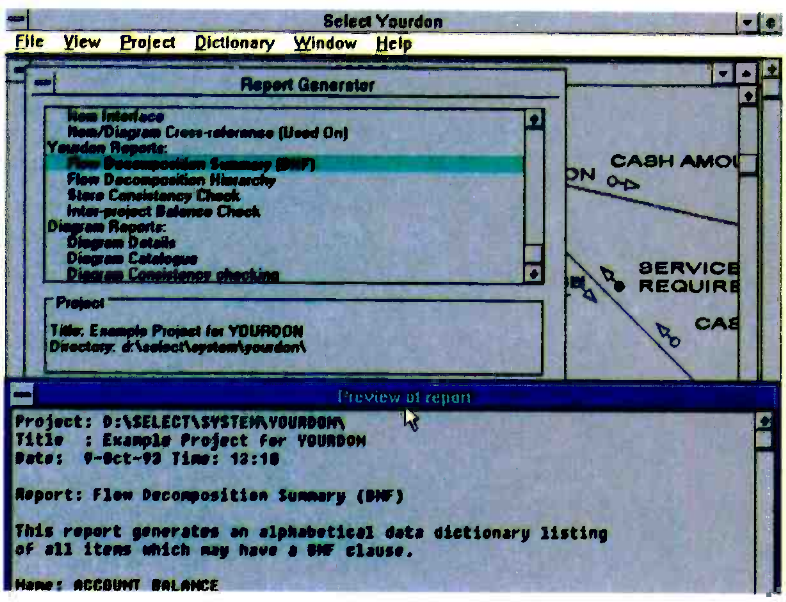




Amending software written with a CASE tool is simple. Add modules or other constructs – then specify the flows between them.



Modify a diagram by simply clicking on an entity. This automatically brings up a menu tree.



A wide range of reports are previewable on screen.

projects where reliability is critical - in military, life support or aerospace applications for example.

Edward Yourdon developed the original ideas in the 1970s He has been so influential in the subject that his name is now synonymous with structured analysis and design.

In the early 1980s two workers, namely Ward and Mellor, developed additional features within the Yourdon framework. These involved control information for data flow diagrams and the use of state transition diagrams to specify dynamic behaviour. These extensions make the Yourdon method applicable to documentation of real time event and multi-tasking systems.

Conclusion

Select Yourdon is a CASE tool for software systems with its roots in the control of large software projects. Its functionality and price however are targeted at more mundane microcontroller systems.

The Windows GUI environment is ideally suited to this type of product. Although the display sometimes looks untidy, the ability to switch quickly between between diagrams and layers is an important part of maintaining the diagrams.

With the Ministry of Defence demanding the use of CASE tools for its real time systems, and pressure from quality systems and life support applications for formal software documentation, *Select Yourdon* is assured part of a growing market. There are competitive products priced at an order of magnitude more than *Select Yourdon*. If you need to use formal software control methods with minimal outlay, then this package is well worth considering. ■

Further reading

Modern Structured Analysis by Edward Yourdon, Prentice Hall.
Software Design for Real-Time Systems by Jim Cooling, Chapman and Hall.

SYSTEM REQUIREMENTS

Windows 3.1 under MS Dos 5.0
Config.sys must have FILES=40
80386 or 80486 processor
VGA 640x480, 16 colours
3 Mbyte of ram
3 Mbyte hard disc space
Mouse
Windows supported printer

SUPPLIER DETAILS

Manufactured by Select Software Tools, Select Yourdon is available in the UK via Computer Solutions Ltd, 1A New Haw Road, Addlestone, Surrey KT15 2BZ. Tel. 0932 829460. Its price is £495.

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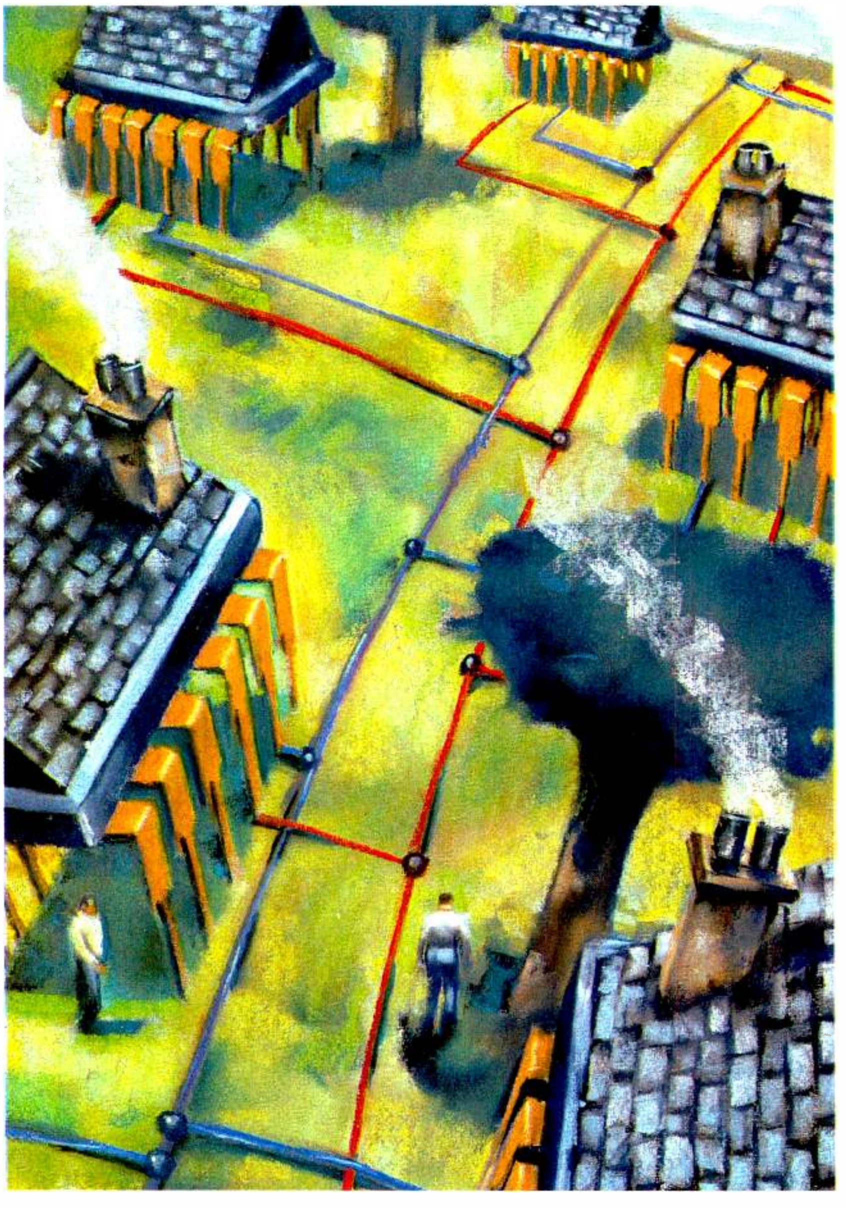


The I²C approach to distributed processing allows the designer to include every kind of processing and signal conditioning function on a simple two-wire bus. This proprietary Philips concept is so flexible and accommodating that other semiconductor companies have adopted it and added to the function range. Design consultant Mike Button reveals the secrets of its success.*

BUSMAN'S GUIDE TO I²C

The low cost of microprocessor devices makes it common sense to provide future compatibility in all but the most trivial of designs. Consequently the majority of electrical and electronic circuits employ the ubiquitous microprocessor to implement logical functions. With the advent of the microcontroller with on-chip prom or eprom in the 70's, single chip solutions are now a norm.

Control functions, often involving human reaction times, are the norm in the majority of systems. The high speed data transfer rate of an 8-bit parallel data bus is likely to be unnecessary and expensive. A simple, two-wire serial interface often provides enough performance for a surprising range of applications.

The Inter-Integrated Circuit Bus, written I²C for short and pronounced "I squared C", was invented and patented by Signetics and Philips and has become a *de facto* standard in chip to chip and board to board communication. Due to Philips' involvement in audio, television and telecoms, a legion of I²C bus devices is now available. Other semiconductor manufacturers are also making devices for the bus.

The range includes 8-bit data converters, adc/dac, audio frequency generators, clock timers, ram, eeprom, led/lcd display drivers and a range of audio, radio and television control circuits. Several microcontrollers have on-chip hardware to ease programming and relieve the processor of software overheads. The *PCB8XC552* and *PCB8XC652* are of particular note.

The ability to add more master devices at any time puts great power at the finger tips of a system designer. When the microcontroller software becomes overloaded additional microcontrollers can be added. Alternatively external test equipment can contain a master and slaves to exercise, test and report on system functionality. In control functions where response time in the order of 1ms is acceptable, the I²C bus provides a convenient adaptable and low cost solution.

Definitions

The I²C bus is a bi-directional two wire serial bus having a defined protocol which allows data transfer between compatible integrated circuits. The number of devices that can be

*TDR Ltd.

attached to the bus is limited only by the bus capacitance. The bus is so designed that the addition or removal of a device will not affect the working of any devices still on the bus. Philips defines the bus as multi-master, multi-slave working.

The standard-mode of operation can handle data and clock signals at baud rates up to 100kHz. Fast-mode devices are now being made available that will work at 400kHz. The low speed mode is used when microprocessors need to poll the bus in software. A 10-bit address mode was recently introduced to provide more independent slave addresses. All modes of operation conform to the same protocol and provide enhancements for use in special cases.

The I^2C bus uses two leads plus a common (earth) return. The SCL lead carries the clock pulses, the SDA lead carries the data information. Commencement of a data transfer is indicated by a START condition [S]. The end of transfer is indicated by a STOP condition [P].

Data is transferred in a 9-bit word, comprising of eight data bits plus an acknowledge bit. The acknowledge signal, ACK, is sent after every data byte to indicate that data transfer may continue. The NACK (not ACK) signal indicates that no further data transfer is possible and a STOP or repeated START condition should be sent. The device that generates the START and STOP conditions and provides clock pulses is called a MASTER. Devices that respond to a MASTER are called SLAVES.

All SLAVES devices are provided with a unique SLAVE ADDRESS. A MASTER, wishing to transfer data to or from a SLAVE must, prior to data transfer, generate the address appropriate to the required SLAVE. A SLAVE on recognising its own address will generate an ACK signal.

The device that sends data is called a TRANSMITTER. Conversely, the device that accepts data is called a RECEIVER. Except for the condition when a SLAVE acknowledges its own address, it is the RECEIVER that generates the ACK signal.

Thus an I^2C bus device can be any one of four types dependent on its function during data transfer. The majority of devices produced for the bus are slave devices and can be either transmitters or receivers dependent on function or mode of operation. The master function is normally provided from a microprocessor with an I^2C bus controller chip (*PCD8584*) or a microcontroller with on-chip I^2C bus hardware.

Master transmitter → *direction of data* → slave receiver

Master receiver → *direction of data* → slave transmitter

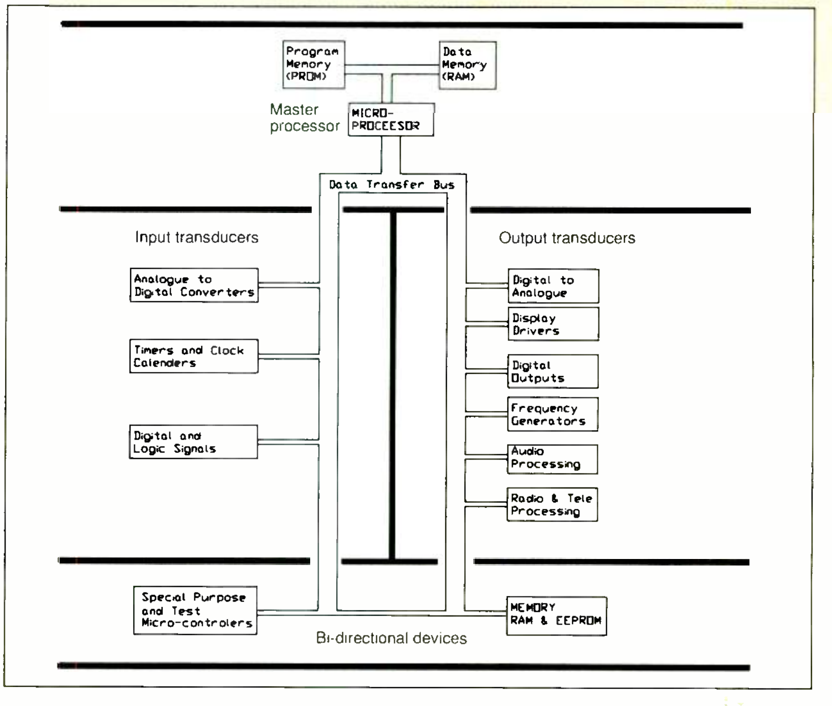
Subject to bus capacitance limitations, there can be any number of masters or slaves but only one transmitter-receiver pair are allowed to use the bus at any one time.

Hypothetical complex microcontroller system

The I^2C bus provides a two wire communications channel for both commands and data for all elements of the system. It replaces a multiple line address/data bus with consequent savings in PCB complexity and area. It was designed as a simple communications channel between individual ICs but is increasingly used as a local network between systems, providing they are not speed sensitive.

System inputs may include: converted analogue to digital signals from transducers such as temperature sensors, analogue joysticks, etc. and logical signals from level switches, key contacts, etc.

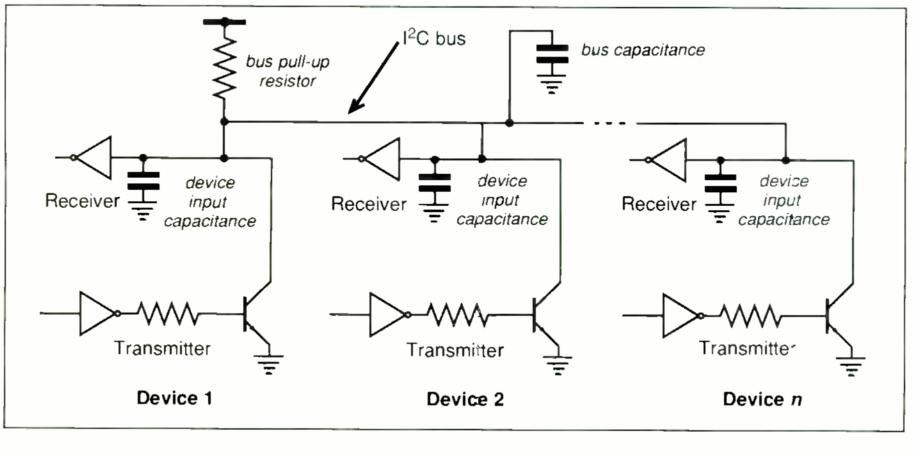
Transducer outputs may include: converted digital to analogue signals to drive motors, current loops, etc., digital signals to switch relays or lamps and drivers for led or lcd displays. Special functions such as television receiver channel selection or teletext reception and display may also be included.



Electrical properties

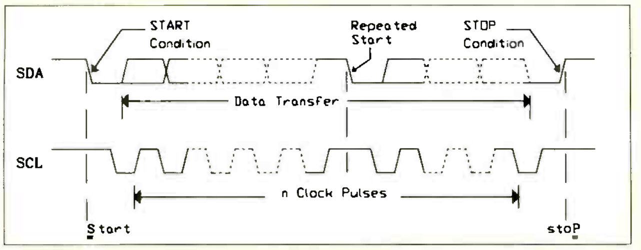
The electrical connections to the I^2C bus rely on open collector wired and-logic gating. Both the SDA and SCL leads have the same electrical configuration.

Figure 1 shows a typical bus connection for one of the wires (SCL or SDA). If all the device transmitters (devices 1 2... *n*) are at logic-high the bus wire will be pulled high to V_{CC} (normally but not necessarily +5V) via the bus pull-up resistor. All of the device receivers will see this high state on the bus as a logic-high signal. If any of the device transmitters go to logic-low the bus wire will be pulled to ground potential and all of the device receivers, including the receiver of the device

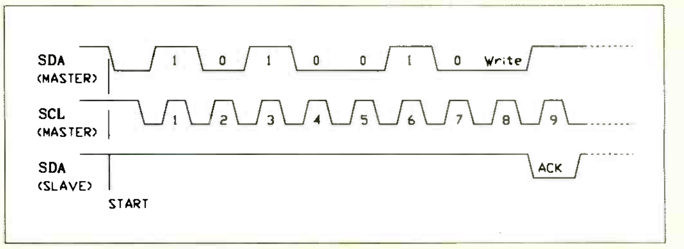


Electrical and logic circuit of the SDA & SCL leads. The wired-and connection allows each device to simultaneously monitor the bus while transmitting data. When a device transmits a logic-high it expects to see a logic-high on its input, if a logic low is received then another device is using the bus.

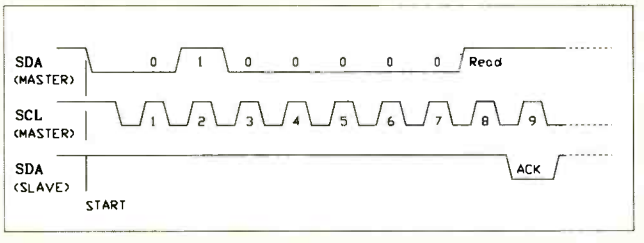
Data transfer under I²C



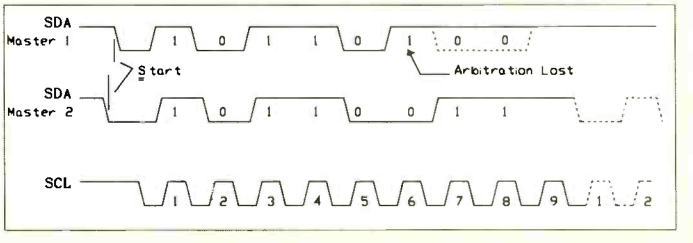
Start and stop conditions shows the relationship of the start, repeated start and stop conditions on the SDA lead with reference to the SCL Lead. The repeated start condition is used when a master needs to retain control of the bus during a combined write/read transfer, for example, when accessing a memory device.



Addressing a slave receiver. Shows waveform to write to slave address A0. (Eprom PCF8582). Note that the SDA lead is low (write) during the 8th SCL clock pulse. The ACK signal, during the 9th SCL clock pulse is generated by the slave.



Addressing a slave transmitter. Shows waveform to read from slave address 80. (8-bit I/O PCF8574). Note that the SDA lead is high (read) during the 8th SCL clock pulse.



Arbitration. When a master sends a start condition it must check the bus for arbitration. The waveform shows two masters starting at the same time. The first master to send a logic-low on the SDA lead when the other master sends a logic-high wins the arbitration. In the waveform above master 1 is attempting to address slave 1011 010 and master 2 addresses slave 1011 001. Master 1 loses arbitration on clock pulse 6 and releases the bus. (Leaves the SDA lead high).

transmitting the signal, will receive a logic-low signal.

Both the clock lead (SCL) and the data lead (SDA) use this wired-and function to perform checks on data transfer. If the MASTER monitors its own transmitted signals it will expect to see the bus responding to these signals. The presence of another device on the bus can be detected if a logic-low is received when transmitting a logic-high. This feature is used to control the clock rate on the SCL lead and to obtain data arbitration on the SDA lead.

A slave can optionally control the clock pulses received from the master by holding the SCL lead at logic-low. Thus data speed and synchronisation of data exchange may be controlled by the slave device.

The transmitting device can check for the presence of other transmitters on the bus by monitoring the state of the SDA lead. If a logic-low is received when transmitting a logic-high then another device is also transmitting on the bus. This condition is known as lost arbitration. The bus specification requires that any master transmitter shall check the bus for arbitration and, if the presence of another transmitter is detected, the master shall relinquish any control of the bus.

Data transfer

When the I²C bus is idle both the SDA and SCL leads are high. A start condition is

SDA & SCL lead DC requirements

Parameter	Symbol	Standard Mode Min	Max	Fast Mode Min	Max	Unit
Low level input voltage	V_{IL}	-	$0.3V_{DD}$	-	$0.3V_{DD}$	V
High level input voltage	V_{IH}	$0.7V_{DD}$	-	$0.7V_{DD}$	-	V
Low level output voltage						
at 3mA sink current	V_{OL}	0	0.4	0	0.4	V
at 6mA sink current		-	-	0	0.6	V
Input capacitance, each lead	C_i			10	10	pF

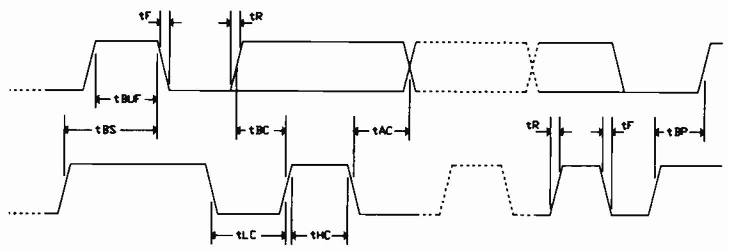
I²C bus line length limitations

Because of the non active pull-up feature of the wired-and bus, the capacitance on each of the bus wires restrict both the number of devices connected and the working distance. This capacitance comprises of the total input capacitance of the connected devices and the bus wire leakage capacitance. The minimum value of the pull-up resistor is defined by the maximum low level sink current of the devices. It may also be necessary to provide a resistor in series with each device to provide input protection against voltage spikes on the bus.

Data sheets for all of the Philips devices give information on how to calculate the pull-up and series resistor values for a given bus. To obtain maximum distance the pull-up resistor should be a minimum value, without series resistor. With a 5V system and 3mA maximum sink current the minimum value of the pull-up is 1.7kΩ (5.1V/3mA).

SDA and SCL lead timing requirements.

Parameter	Symbol	Standard Mode Min	Standard Mode Max	Fast Mode Min	Fast Mode Max	Unit	Philips Symbol
SCL clock frequency	f_{CL}	0	100	0	400	kHz	F_{scl}
Low period of SCL clock	t_{LC}	4.7	-	1.3	-	μs	t_{LOW}
High period of SCL clock	t_{HC}	4.0	-	0.6	-	μs	t_{HIGH}
Bus free time between stop & start condition	t_{BUF}	4.7	-	1.3	-	μs	t_{BUF}
Time SCL must be high before start or repeated start	t_{AS}	4.7	-	0.6	-	μs	$t_{SU.STA}$
Hold time SCL must be high after start or repeated start	t_{BS}	4.0	-	0.6	-	μs	$t_{HD.STA}$
Time SDA must be stable before rising edge of SCL	t_{BC}	300	-	300	-	ns	$t_{HD.DAT}$
Time SDA must be stable after falling edge of SCL	t_{AC}	250	-	100	-	ns	$t_{SU.DAT}$
Time SDA must be low after a rising edge on SCL prior to a stop (rising edge on SDA)	t_{BP}	4.0	-	0.6	-	μs	$t_{SU.STO}$
Rise time of both SDA and SCL signals	t_R	0	1000	0	300	ns	t_R
Fall time of both SDA and SCL signals	t_F	0	300	0	300	ns	t_F
Capacitance load for each line	C_b	0	400	0	400	pF	C_b



Conventional I²C devices handle clock signals and bit rates to 100kHz but fast mode devices are now appearing that are capable of working at 400kHz. These timings cover both fast and slow modes.

defined as a falling edge on the SDA lead when SCL is high. A stop condition is defined as a rising edge on SDA when the SCL is high. It follows that to avoid false start and stop conditions being generated during data transfer, the state of the SDA lead must be stable while the SCL lead is high.

The generation of a start condition indicates to all other devices that the bus is busy until a stop condition is generated. masters wait for this stop condition before attempting to send a start. All slaves, on detecting a start, will reset their hardware and prepare to receive the slave address. A slave recognising its own address will generate an ACK signal.

The ACK signal is a logic-low signal during the ninth clock pulse. The NACK signal is, therefore, a logic-high. The generation of a non existent slave device address automatically generates a NACK because the bus is inherently in the high state.

It is possible that two masters could simultaneously generate a start followed by a slave address. For this reason all masters must always check the SDA lead for arbitration. As two or more masters could attempt to address the same slave, the check for arbitration must continue for the whole of the data transfer. (Until the stop condition is generated.)

Slave addressing

All slave devices are designed with a unique address which, when recognised and accepted, sets the slave in data transfer mode. There are two modes of addressing, both using the same protocol. The "standard" seven bit address is used by most of the devices available at present. The ten bit address mode will be provided on some future devices.

To address a slave device, a master will generate a start followed by a nine bit word. This word comprises seven data bits (ADDRESS), a read/write (W) bit and an acknowledge (ACK) bit. The read/write bit determines the data direction. A logic-high (read) sets the slave as a transmitter, a logic-low (write) makes the slave a receiver.

If an addressed slave device is capable of responding to the master it will generate an ACK signal (a low level on the SDA lead during the ninth clock pulse) and set its internal hardware or software for the data transfer. Any slave not addressed will ignore any further action on the bus until another start condition is generated.

The seven bit address has several reserved codes used for special purposes.

Slave address byte

	Bit no.
Allocation	6543 210 W
General call	0000 000 0
Start byte	0000 000 1
CBUS	0000 001 X
Reserved	0000 1XX X
10 bit addressing	1111 0XX X
Reserved	1111 XXX X

X = any state

Data transfer

All currently available devices perform data transfer in a 9-bit word comprising eight data bits plus a ninth ACK bit. An astute reader will observe that the I²C bus protocol does not necessarily require an eight bit format for addressing and data transfer. Provided that a master is capable of generating the clock pulses and the slave is configured to receive them, then the word format can by any number of bits. Early bus formats, particularly systems using the *8048* type microcontroller, were open and allowed the user to choose the word length.

Transmitters send data on the SDA lead, receivers read data from the SDA lead and generate the ACK signal. Masters generate clock pulses on the SCL lead and control the bus by generating start and stop conditions.

A data transfer can be of any number of data words. The transfer is terminated when a (repeated) start or a stop condition is sent by the master. The bus is considered to be busy during the period between an initial start condition and a stop condition. A receiver can indicate that the transfer is over by sending a NACK signal but it is the responsibility of the master to send a stop.

General calls

The slave address 0000 0000 (a write to slave address 00) is reserved for a general call to devices that require "broadcast" information. The second byte of the transfer will indicate what type of information is being transmitted. General calls are used to globally set slaves to a defined state or to send global configuration data. A full discussion is beyond the scope of this article. Interested readers should obtain the relevant Philips data sheets.

Other modes

Low speed mode. This mode is an extension of the bus protocol to allow relatively slow slave devices to respond to a "normal" master using an optional lower clock rate, preceded by a longer start procedure. The start procedure is as follows:

- A standard start condition.
- A start-byte 0000 0001. (This is equivalent to "read address 0")
- A repeated START condition.

The start-word is seven clock pulses long

Putting in an extra feature

We had a requirement to add an auxiliary keypad to one of our existing designs. This product used a *PCB80C552* micro controller with I²C bus software drivers already installed (clock timer and a led display). Expecting future enhancements and modifications we arranged the original circuit layout such that all spare *'552* port leads were made accessible on suitable connecting points.

The *PCF8574*, a remote 8-bit i/o expander, has the necessary functions. It is an 8-bit quasi-bidirectional port similar in function to the *8051* microcontroller ports. It has an interrupt facility which is activated when the input to one or more of the port leads changes state. The interrupt signal is cleared when a bus read or write is sent to the device. There are two versions of the *PCF8574*; one version has an allocated slave address 0100 XXX, the other (*PCF8574A*) 0111 XXX.

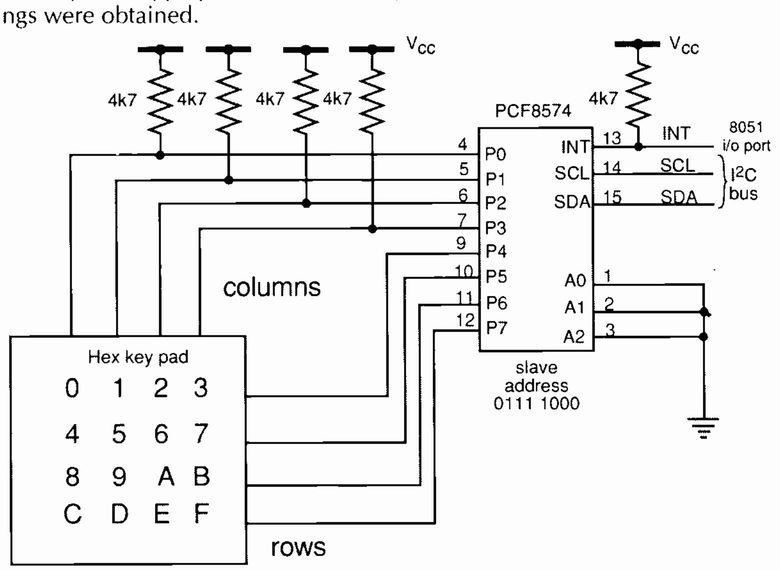
The *PCF8574* was mounted on a small daughter board attached to the hex keypad. The eight wires from the keypad were connected to the device ports. The 5V supply, ground, SCL, SDA and interrupt leads were wired to a suitable connector. Hardwire links set the address to 0100 000. In the idle (waiting for a key depression) state the *PCF8574* port bits 4-7 are set to binary 0000, which applies a ground potential to the four row pins on the keyboard. Bits 0-3 are set to binary 1111. When a key is pressed one of the column pins (bits 0-3) is pulled to ground via the key connection. This change of input causes the internal logic in the PCF8574 to apply a ground potential on the "int" pin 13 which is detected by the microcontroller. The software then performed the following I²C bus transfer.

	Slave address bit no. 6543 210	W		Transferred data bit no. 7654 3210		
S	0100 000	0	A	1110 1111	A	start & select column "0"
R	0100 000	1	A	1110 KKKK	A	Read state of keys 048C
R	0100 000	0	A	1101 1111	A	Select Column "1"
R	0100 000	1	A	1101 KKKK	A	Read state of keys 159D
R	0100 000	0	A	1011 1111	A	Select Column "2"
R	0100 000	1	A	1011 KKKK	A	Read state if keys 26AE
R	0100 000	0	A	0111 1111	A	Select Column "3"
R	0100 000	1	A	0111 KKKK	A	Read state of keys 37BF
R	0100 000	1	A	0000 1111	A P	Set "idle" state and STOP

S start; P stop sent or R repeated start; A ack; W read/write 1=read, 0= write

All of the bits (*K*) in the received data bits 0-3 will be logic-high except for the bit(s) corresponding to the pressed key(s). Note that only one stop condition is sent. The repeated start feature was used to prevent other masters from interfering, and thus delaying, the bus transfer. When the key is released the *PCF8574* will detect another change on its inputs and present a further signal on the "int" pin. The software must now perform another read or write to the device to clear this signal.

Initial concern whether the bus would be fast enough to detect and process the key depressions was soon dispelled by a calculation. With a baud rate of 100kHz and nine bits required for each data byte and with a total of 18 bytes, the maximum time to scan the keyboard was 9×18/100=1.6ms. This time was less than the contact bounce period of the keys and appropriate software delay routines were needed to insure that valid readings were obtained.



which, combined with a slower clock rate, gives ample time for microprocessor to respond and prepare for data transfer. After the repeated start condition the "real" slave address is sent. No slave device is allowed to acknowledge this start byte.

Fast mode. In fast-mode the I²C bus protocol remains unchanged. The maximum baud rate has been increased to 400kHz thus tightening the timing specification for the SDA and SCL leads. Devices designed for the fast-mode will still perform satisfactorily at standard-mode baud rates.

Ten bit slave addresses. The 10-bit addressing has been introduced because most of the 112 addresses allowed by the 7-bit scheme have been allocated more than once. The bus protocol and byte length remain the same. The reserved slave address 1111 0XX is used to provide an extra two bits for the address. The remaining eight bits are sent in the next byte. Full details of this mode are outside the scope of this article and, as I understand from Philips, there are no devices yet using this mode. Further information can be obtained from Philips Components and the handbook "*I²C Peripherals for Microcontrollers*" gives full details on this – at present fairly academic – mode.

A future article will deal with practical applications such as the use of an I²C bus controller to adapt an existing micro system and a list of available devices. ■

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Marconi's 200kW transatlantic transmitter

Enigma surrounds Marconi's massive 200kW wireless station, built nearly eighty years ago. George Pickworth pieces together the technology behind the world's most powerful spark transmitter.

Marconi's 200kW timed-spark continuous-wave transmitter was the ultimate spark-type transmitter. It was installed at Marconi's Caernarvon transatlantic 'super' station in Wales and came into service in 1916 to handle North Atlantic traffic. This was after the original synchronous-spark, wave-train transmitter was taken over by the military in 1914 for long range strategic signalling.

The timed-spark transmitter worked US stations at New Brunswick, Tuckerton, Marion and the Central Radio Station at Long Island. In 1919 it transmitted the first signals directly to Australia. Wavelength was given as 14km, which is approximately 21.5kHz.

To take advantage of the Earth/ionosphere waveguide effect, all transoceanic 'super' stations operated frequencies less than about 50kHz. However the lowest useable frequency, typically 20kHz, was set by physical constraints imposed by antenna structures; even the largest practical structures were very inefficient at 20kHz.

Because all transoceanic stations were confined to a 30kHz bandwidth, a high level of selectivity became vital to reduce mutual interference as the numbers of stations progressively increased. The only way of attaining this was with continuous wave systems. With these, oscillations progressively built up in the receiver tuner by virtue of resonance; this was known as syntony – a term invented by Lodge.

Remarkably, Marconi's 1906 Clifden transatlantic super-station in Ireland, which originally radiated continuous waves, was a quenched-arc type. It had a plain triple disc discharger that was inherently self cooling, and the draught created by the rotating discs dispersed ionized gases, **Fig. 1**.

On the other hand, Poulsen, with his quenched-arc system incorporated 'rod' type electrodes, comparable with an arc lamp. These required elaborate water cooling and a strong magnetic field to drive ionized gases from the arc-gap.

The Clifden transmitter was powered by a DC generator which charged 6000 lead acid accumulators. However, the Clifden discharger was modified by attaching transverse electrodes to the main disc, similar to the 1916 synchronous discharger. These electrodes, described in the November issue, radiated wave trains; the official explanation was so that signals could be received by Marconi's magnetic detector which responded only to wave trains. There is some evidence that the magnetic detector will demodulate AM signals but I have not been able to confirm it.

Options

Originally, the Caernarvon transmitter was a 200kW synchronous spark type radiating wave trains. It only allowed a very limited degree of syntony since there were too few waves in each train. These declined too quickly for resonance to be effective. In 1916 however, it was replaced with a continuous wave transmitter to increase receiver selectivity.

As early as 1906, Fessenden and Golsdschmidt adopted rf alternator-type continuous wave transmitters for their north Atlantic service. Poulsen adopted the quenched-arc continuous wave system for his Hawaii/San Francisco link. Marconi's approach on the other hand was to indirectly produce continuous waves. He used spark systems to generate wave trains in rapid succession so that in effect they overlapped in phase. This led to the development of the Caernarvon timed-spark discharger.

Although the waves were continuous, they undulated in amplitude. Provided they remained in phase, this in itself did not significantly effect syntony. Indeed the undula-

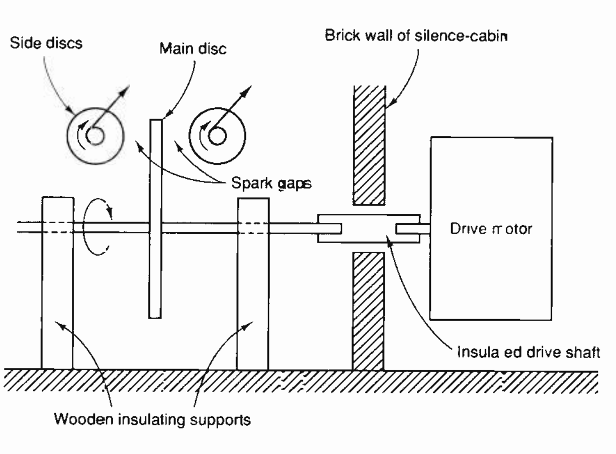

Fig. 1. Marconi's 1906 Clifden transatlantic super-station was powered by a DC generator charging 6000 lead acid accumulators. It radiated wave trains.

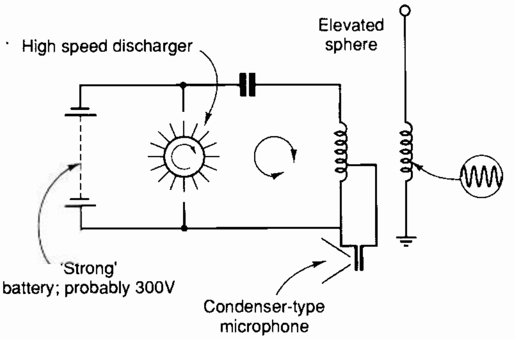

Fig. 2. Tesla's 1899 radio telephony transmitter. There is little information on how it worked but it probably relied on the battery's internal resistance to limit the capacitor charge rate and a critical hub rotation rate.

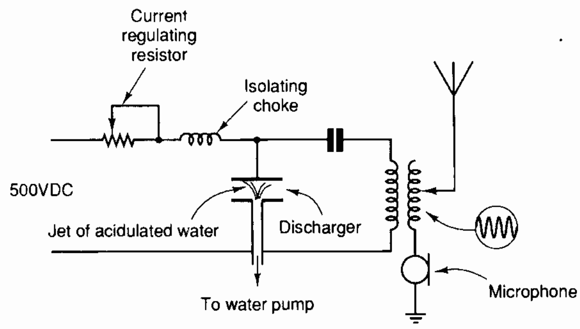

Fig. 3. Morrietti's 'hydrothermic' discharge transmitter. Unlike most of its contemporaries, it had no moving parts.

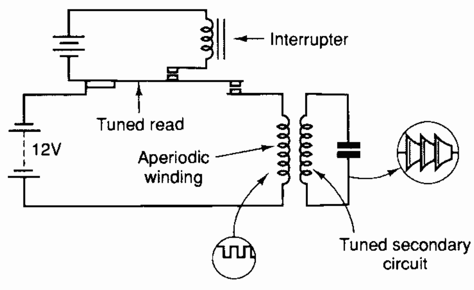

Fig. 4. Fessenden's continuous-wave oscillator was the first to use a vibrating reed interrupter tuned to set transmitter frequency.

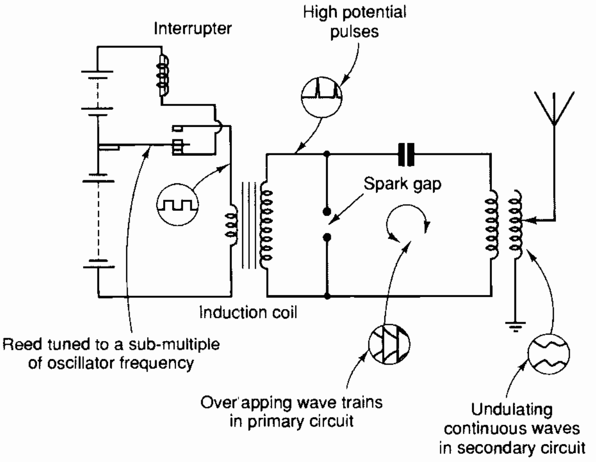

Fig. 5. Early cw spark transmitter with a tuned-reed interrupter had limited power and contact bounce problems when operating above a few kilohertz.

tions modulated the transmission with a tone. This article is about generating continuous waves by causing wave trains to overlap.

Overlapping wave trains

My experiments have shown the number of significant waves in a train to be around 25. When creating continuous waves by progressively reducing the period between trains they eventually overlap. Repetition rate must therefore be at least 1/25th of the transmission frequency, but undulation is unacceptable at this rate. The Caernarvon transmitter generated wave trains that overlapped every 13.5 waves which produced slightly undulating continuous waves.

A repetition rate equal to the 25th sub-multiple presented no particular problem at the 20 to 50kHz transoceanic frequencies. But timing the wave trains – hence the term 'timed'– so that they overlapped in phase required extraordinary technical expertise. However, at the 500kHz and 1MHz maritime frequencies used with mechanical dischargers this repetition rate was out of the question.

Tesla systems

Radio telephony, as pioneered by Tesla was the original motivation for continuous waves. In 1899 he employed a discharger, or 'break' as Tesla called it. This consisted of a hub with 16 – or sometimes more – radial electrodes rotating at very high speed between a pair of fixed electrodes. The device was energised with DC and a discharge occurred each time a pair of rotating electrodes aligned with a fixed pair. The discharge was quenched as the gaps widened, **Fig. 2**.

I am unsure how the device actually worked; indeed Tesla himself does not make this clear. A possible explanation is that the internal resistance of the battery limited the capacitor charge rate. During discharge, current is drawn from the capacitor faster than it is replaced, so potential falls. Then, as the hub continues to rotate, the discharge is quenched. In this way, the capacitor is charged and discharged synchronously with alignment of pairs of electrodes. At a critical rotation speed, this corresponds to the resonant frequency of the circuit.

The 'flywheel' effect of the tuned circuit converted charging and discharging into continuous sine waves. Operation can therefore be compared to the quenched-arc system. The effect of the capacitor-type microphone was to de-tune the circuit so that power output corresponded to sound pressure waves.

In later versions, Tesla used a pair of toothed wheels rotating at very high, but at slightly differing speeds, in opposite directions. This was reported to give up to 10,000 discharges a second. For an even greater discharge rate, Tesla added a jet of mercury intercepted by projections on a disc rotating at extremely high speed, but this was a low power device intended as an oscillator for use with his regenerative receivers.

Fessenden's experiments

In 1900, during early radio telephone experiments prior to adopting radio frequency alternators, Fessenden built a system whose main elements were a battery, a vibrating-reed type interrupter and a transformer. The interrupter was tuned to 10kHz, in series with the aperiodic primary winding of the hf transformer. In turn, the transformer's secondary winding was tuned to the interrupter frequency. This was the first transmitter to use a vibrating reed to set transmitter frequency, **Fig. 4**.

My replication of Fessenden's experiments showed that the method worked well when the vibrator was tuned to a low sub-multiple of the resonant frequency. Here, the oscillation trains overlapped. Operation seems to have been by each DC pulse shocking the tuned circuit into oscillation.

Before thermionic valve type oscillators, there were many ingenious spark systems. Despite these, rf alternators were the only devices capable of producing continuous waves pure enough for practical radio tele-

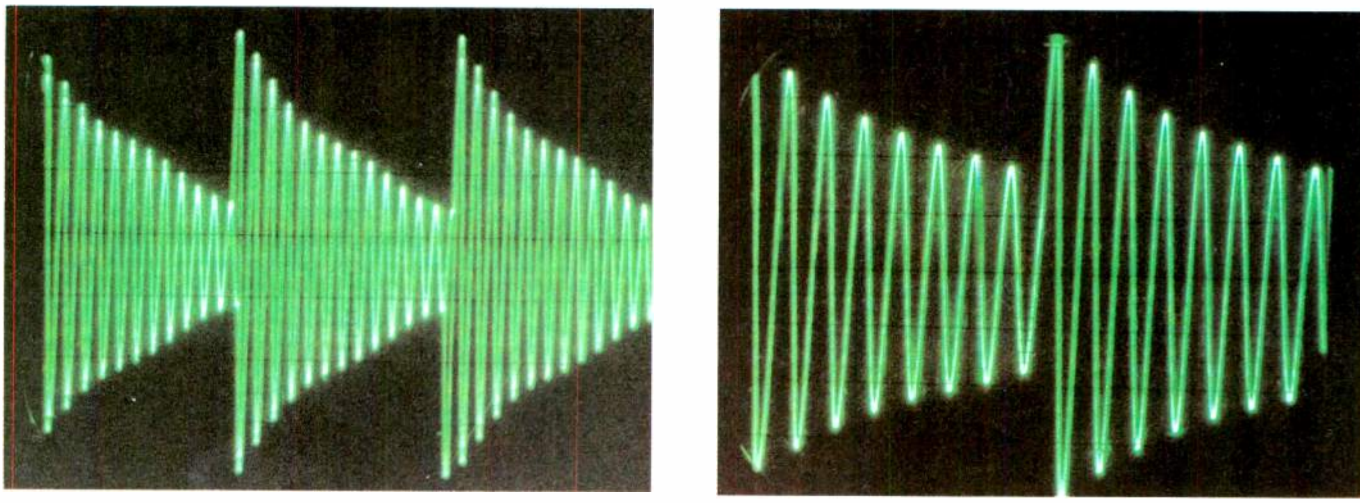

Fig. 6. Reproduction of Fessenden's experiments produced the overlapping wave trains of (a). Wave trains overlapping in phase are detailed in (b).

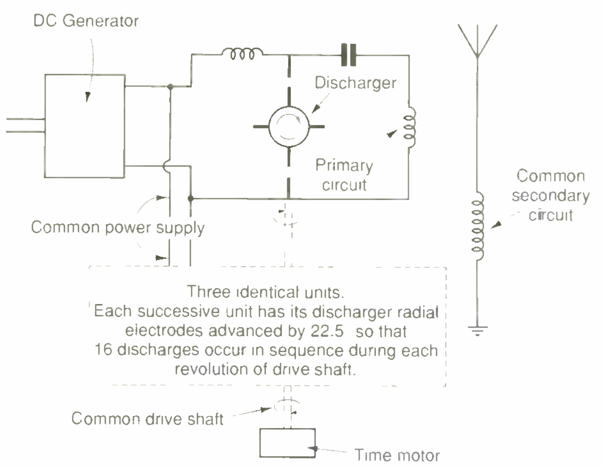

Fig. 7. Marconi's experimental timed discharger comprised four rotary dischargers each with four radial electrodes rotating between a pair of fixed electrodes. Each revolution of the common shaft caused 16 discharges.

phony. Using rf alternators, Fessenden radiated his voice from his Brant Rock station in the USA. As early as 1906, these broadcasts were reported to be heard by operators at his station in Scotland.

However, Marconi still rejected alternators, probably because they were still in their infancy and ran at very high speed. Frequency raisers which allowed alternators to run at lower speed had yet to be developed; so had the inductor type alternator, which eliminated windings on the rotor and thereby the major problem with rotor windings flying out of their slots.

Early spark cw

The Marconi company had considerable expertise in the manufacture of spark apparatus. Having progressed so far with arc/spark systems, particularly for maritime use, it is understandable that Marconi should have pursued this path.

Early attempts to produce continuous waves with spark systems were based on tuning the interrupter of an induction-coil type spark-transmitter to a sub-multiple of the oscillator frequency, **Fig. 5**. However, while tuning the vibrator to a sub-multiple presented no special problem. Contact bounce made precise timing extremely difficult and almost impossible to maintain at frequencies above a few kilohertz.

Moreover, the vibrating reed was essentially a low power device. In my 7kHz reproduction, fine tuning to bring the wave trains into phase was by adjusting the oscillator frequency, **Figs 6(a,b)**. I found using shock excitation simpler however.

Morrietti's system

Morretti's 'hydrothermic' discharger, used for experimental radio telephony between Rome and Tripoli around 1910, consisted of a pair of copper discs set horizontally, one above the other. The lower disc had a tiny hole drilled through the centre. Through this hole, acidulated water was steadily pumped so as to form a jet that impinged on the upper disc, Fig. 3.

Current immediately vapourised the jet. This interrupted the circuit which was then re-established – to be interrupted again to create current pulses. Operation was therefore automatic and required no moving parts. Each pulse shock excited the secondary circuit at a submultiple of its resonant frequency. In this way, oscillations persisting in the secondary circuit were continually reinforced to produce slightly undulating continuous waves.

Morrietti's device drew power from a 500V DC generator via a variable resistor. This component was presumably intended to synchronize the discharges and bring them in phase with oscillations in the antenna circuit.

Marconi's timed discharger

Marconi's 1913 experimental consisted of a bank of four rotary dischargers. Each comprised four radial electrodes rotating between a pair of fixed electrodes and driven by a common shaft extending from the drive motor. Individual primary circuits, one per discharger, were inductively coupled to a common secondary circuit. The device was powered by a DC generator, **Fig. 7**.

Discharge commenced while the gaps were still narrowing. Further narrowing as the electrodes rotated reduced resistance across the gaps. Amplitude of the oscillations declined and energy was transferred to the secondary circuit. Then the gaps widened and the draught created by the rotating electrodes dispersed ionized gases, thus quenching the discharge and returning the gaps to a high resistance state.

Bearing in mind that the device was energised by DC, I am not sure which mode it ran in. The primary circuit could have operated in quenched-arc mode and transferred energy to the secondary by induction. Alternatively, current pulses through the primary circuit could have shock excited the secondary circuit into oscillation. It was most probably a combination of both these modes. Whichever, discharges occurred consecutively, giving a total of 16 discharges per revolution.

Assuming operation in quenched-arc mode, the quenching effect caused by the rotating electrodes would limit the number of oscillations in each train to 15 or fewer, insufficient to overlap. As a result, wave trains in the primary circuit were discrete. Provided they were in phase with oscillations in the secondary circuit, they would be reinforced to create continuous oscillations with undulations corresponding to their reinforcement points, **Fig. 8**. Reinforcement of oscillations in the secondary circuit would be exactly the same with shock excitation of the secondary circuit.

Consider for example a frequency of 10kHz reinforced every 13th oscillation. This makes the reinforcement frequency $10^4/13$ which is 769 2Hz. As each revolution produces 16 reinforcements, it needs to run at 769.2/16, or

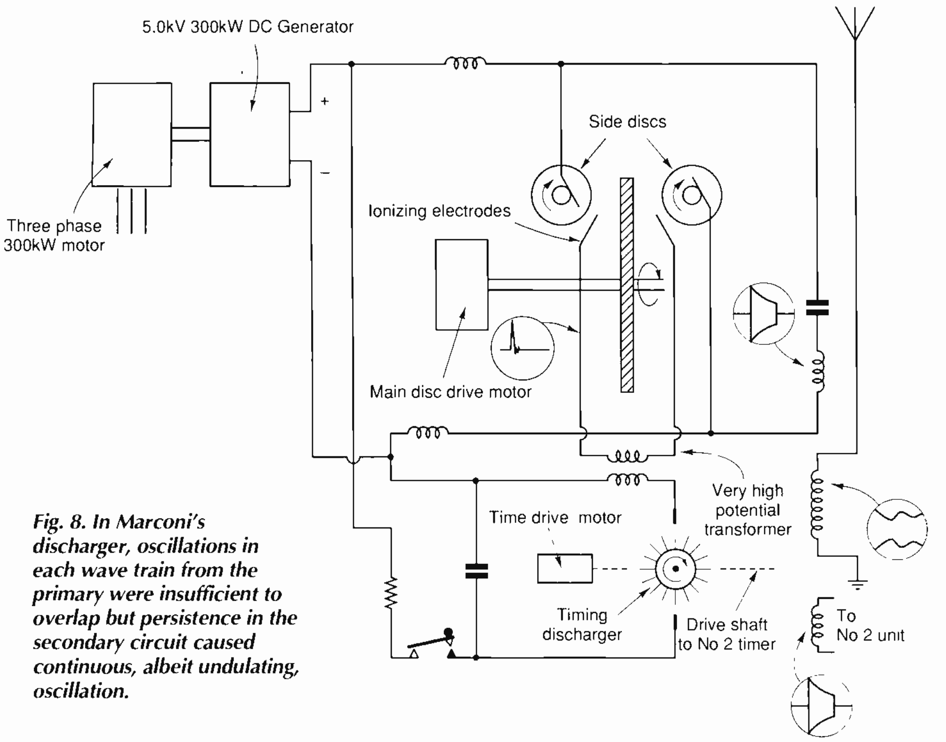

Fig. 8. In Marconi's discharger, oscillations in each wave train from the primary were insufficient to overlap but persistence in the secondary circuit caused continuous, albeit undulating, oscillation.

48rev/s (2888rev/min). Precise speed control was vital to keep the trains in phase.

Reinforcement could be made to occur at other points by changing drive speed. By the same token, resonant frequency of the tuned circuits could also be changed, but then drive speed would have to be adjusted to keep wave trains in phase with oscillations persisting in the secondary circuit. However, maximum drive speed was unlikely to have exceeded 50rev/s (3000rev/min) which limited operating frequency to the order of 15kHz. Moreover, the device had an inherent drawback.

In order to handle considerable power, the electrodes had large surface area. Because potentials were high, spark-gaps were fairly wide. Changes in atmospheric pressure, humidity and presence of ionized gases significantly altered the dielectric strength of air. Therefore, the point at which discharge occurred, varied and this upset timing.

Caernarvon 200kW timed discharger

Unfortunately very little information on the operation of the 200kW Caernarvon timed-spark transmitter has been published. Some information regarding the timer even seems to be misleading. This is understandable as there was great commercial rivalry between exponents of alternator and quenched arc systems. Nonetheless, by gleaning information from various sources, and by making a few assumptions, I believe that the following notes truly explain the operation of this remarkable transmitter, **Fig. 9**.

In essence, operation was similar to the experimental timed discharger, but the Caernarvon timed-spark discharger employed two pairs of discharge assemblies. Each of these consisted of a tuned primary circuit, a power discharger and a timing discharger. The timer had a common drive shaft arranged so that discharges occurred in sequence, but in alternate assemblies, as the shaft rotated. Both primary circuits were inductively coupled to the common secondary circuit.

The power dischargers were plain triple-disc types, i.e. with one main disc and two side discs. Discharge was from side disc to main disc to side disc. Independent electric motors rotated the main and side discs. This assisted cooling and created a draught that dispersed ionized gases. Drive speed was not critical and it seems as if they rotated at a relatively low speed, in the order of a few hundred rev/min.

The remarkable feature of these systems was that the distance between the main disc and the side discs was so wide that a discharge could not ordinarily occur at the energising potential of 5kV DC. However, set close to the side discs were a pair of ionizing electrodes.

Timing discharger

Both timing dischargers were connected to a common drive shaft and drive motor so that both timing dischargers rotated synchronously. Each discharger had a number of radial electrodes, probably 16, but because timing current was low, the timing electrodes had small face areas. Also, because the potential was relatively low, gap-width was narrow. This allowed close mechanical tolerances which minimised timing errors caused by changes in the dielectric strength of air. When the electrodes of the timing discharger were aligned, gap-width was less than a millimetre.

At each alignment the timer capacitor, charged to 5kV, discharged across the gap and through the primary of an induction-type coil. This induced a very high potential in its secondary winding which in turn caused a spark across the ionizing electrodes which created a conductive path for the main discharge. As a result, the timer can be likened to an automotive capacitor discharge ignition system. Because the power discharger electrodes were in the form of discs, discharge could occur at any time so timing could be precisely controlled.

The 5kV DC 300kW generator delivered 50A charging current to the primary circuit capacitors. This could be generated with dynamos without undue arcing across the commutator segments. Because of the ionizing spark, the power discharge occurred at this relatively low potential of 5kV; moreover, the wide spark gap caused the discharge to be quenched immediately the ionizing spark ceased. Keying was by interrupting the charging current to the timer capacitor as this circuit took only 300mA. Incidentaly, although

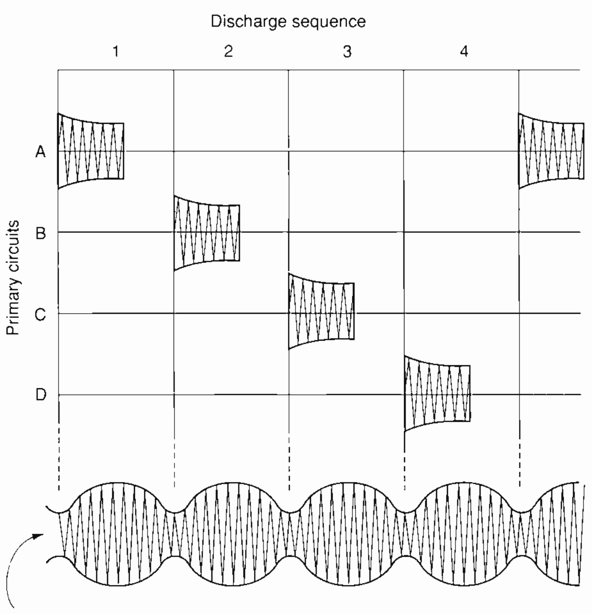

Fig. 9. Principles of Marconi's 200kW Caernarvon discharger. Distance between the main disc and side disc would have been too great for discharge were it not for ionizing electrodes.

installed in a brick-silence cabin, the noise caused considerable stress among operators.

Operation

My original experiments suggest that the time duration of the timing-spark, and consequently the main discharge was probably in the order of 250μs. On this assumption, at 21.42kHz, or 47μs, each train in the primary circuit probably consisted of about five oscillations. Subsequent research suggested that the primary circuit was effectively untuned and discharge was virtually a DC pulse which shock excited the secondary circuit into oscillation. But as I have already explained, the operating mode does not affect timing.

The reason for the half cycle was probably because the two primary inductors were arranged 180° out of phase so that trains started with alternate negative and positive half cycles. Rotational speed of the timer discharger can be determined in exactly the same way as for the experimental timed discharger.

Because the antenna system was in effect a large LC tuned circuit and the linear elements were only a fraction of a wavelength long, it was a poor radiator. This allowed oscillations to persist in the antenna system and progressively build up in amplitude as a result of periodic reinforcement. These aspects made the system workable. But, because of the significant time taken for oscillations to build up, signalling speed was limited to about 100 words a minute. Antenna current was 280A and efficiency from generator to antenna was given as 66%.

Although requiring careful adjustment and maintenance, the timed-spark transmitter was reliable. It proved so successful that the manufacture of a duplicate machine was put in hand immediately it came into service, but this was delayed because of difficulty in obtaining materials during the war. It does however seem to have been prone to radiating harmonics. In the meantime, a Poulsen quenched arc was installed as a reserve, but this was incapable of delivering antenna current of more than 170A and could not be worked for long periods without giving trouble.

Alternators

In 1921, it was decided that in order to increase keying speed and take advantage of improvements in receiver selectivity, it was necessary to replace the timed-spark transmitter with one that produced continuous waves of constant amplitude. Thermionic valve transmitters could meet this criterion with low power installations, but valves that could handle high power had yet to be developed. The only option was the radio frequency alternator. In September 1921, a pair of 200kW Alexanderson rf alternators were installed at Caernarvon and remained in service until about 1923.

In hindsight, Marconi might just as well have adopted alternators in 1906, rather than build the Clifden quenched-arc transmitter. Unfortunately, history never gives the alternative, so we will never know what the outcome would have been if he had. However one thing is certain – neither the synchronous-spark nor the timed-spark transmitters would have been made, and technical historians like myself would not be trying to figure out how these remarkable machines actually worked.■

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DESIGN BRIEF

Tuning in IF stages

Ian Hickman sheds light on synchronously tuned IF stages – the design route to the best-shaped IF response for rf instrumentation and pulse/data receivers.

Most of the selectivity in a single superheterodyne receiver is obtained in one of two sections. These are the intermediate frequency stages, IFs, following the mixer, or in those following the second or third mixer in a multiple superheterodyne design.

In a professional HF communications receiver covering typically 1.6 to 30MHz, the front-end tuning may consist of just a few half-octave filters. Designs with a wide-open front end, apart from a 30MHz low-pass filter, have even appeared. However with ever heavier use of the HF bands, proper front-end tuning is now reappearing.

Whatever the receiver, HF, MW AM, VHF FM or TV, the requirement is the same – to pass with equal amplitude the whole of the band of frequencies occupied by the wanted signal while rejecting all else. This leads to a brick-wall filter design with a flat top and very steep skirts.

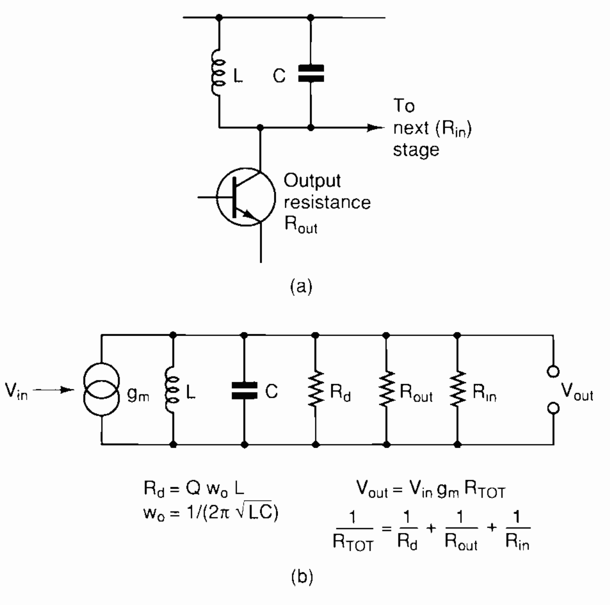


Fig. 1. Simplified single-tuned IF stage, (a). The transistor driving the tuned circuit has a mutual conductance. To avoid internal feedback to its input, it might be a grounded base stage or the output transistor of a cascode stage. To minimize the reduction of the tuned circuit's unloaded Q, the following stage might be an emitter follower. An equivalent circuit is shown in (b).

For a few specialised receivers, a flat IF filter pass-band with steep skirts is *not* desirable. Two examples are radar receivers and spectrum analysers. In both cases, the IF strip is required to pass pulses. In radar the pulses are reflections of transmitted pulses from a target while in analysers they are the energy of a signal as it is swept through the IF passband by the analyser's tuning sweep.

Of course, selectivity is still required. In the case of the radar receiver selectivity is needed to minimize the noise bandwidth so that only the return-pulse energy is passed. In the case of the spectrum analyser selectivity provides resolving power. A small signal, little removed in frequency from a large one, needs to be seen without it being lost in the skirt of the IF filter's response to the large signal.

According to Zverev[1] a Gaussian filter shape is optimum for pulse response, but he goes on to say that a true Gaussian response is not practicable. The group delay of such a filter would be infinite, so you would wait for ever for a signal applied at the input to come out the other end. So he goes on to give designs that approximate a Gaussian response down to 6 or 12dB.

Modern spectrum analysers often claim a Gaussian response, though how accurate it is is another matter: certainly earlier analysers made do with synchronously tuned IF strips. These are easy to design, build and adjust and are satisfactory for many applications. Further, as far as dynamic response goes, they have the advantage of being free from overshoot, however many stages are cascaded. It is these filters that form the subject of this design brief.

In a synchronously tuned IF strip, all the tuned circuits are usually identical not only in centre frequency but also in Q. This simplifying assumption is made here.

Figure 1 outlines a stage which is typical of the strip, together with its equivalent circuit. At an IF between 30 and 40MHz say, the high output impedance provided by a grounded base driver stage and the comparatively high input impedance of a subsequent emitter-follower buffer stage may result in over-heavy damping of the tuned circuit in Figure 1. As a result, the connection to the tuned circuit might be tapped down the coil[2].

Whatever the working Q, the stage gain exactly on tune is given approximately by g_mR_d. Parameter g_m is the transconductance of the driving stage while R_d is the operating dynamic resistance of the tuned circuit. Resistance R_d is equal to $Q\omega L$ in parallel with the shunt resistive components of the driving and load impedances, ignoring any regeneration.

Selectivity can be increased by tapping the connection further down the coil. This brings the tuned circuit nearer to its unloaded Q and reduces gain. Conversely increased gain can only be bought at the expense of reduced selectivity.

A good compromise is a working Q of half the unloaded Q. There is little more selectivity to be had but gain is much reduced. Demanding any more gain results in a disproportionate sacrifice in selectivity. If input impedance of the following stage is virtually infinite, the driving stage can be matched to the tuned circuit. This corresponds to the half-unloaded Q condition. Conversely, if the driving impedance is so high as to be an ideal current source, the following stage can be so matched. But in no way is it possible to match both simultaneously.

How the gain varies at frequencies other than the resonant frequency f_r is discussed in the panel. Armed with the results in the panel, the performance of a synchronously tuned IF strip can be calculated. **Figure 2(a)** shows the response of a single tuned circuit. It can also represent the response of several synchronously tuned identical circuits, since as Hot Carrier noted, you can "just add the dBs".

From the formula in the panel, you can calculate the 6dB and 60dB bandwidths and hence the 60dB to 6dB shape factor. For a brick-wall filter in a communications receiver this might be well under 3:1. For a spectrum analyser however, using either a Gaussian or a synchronously-tuned filter, it may be typically between 10:1 and 20:1.

To calculate the 60dB to 6dB shape factor for an IF strip with four synchronously tuned stages, Fig. **2(b)**, simply evaluate the 1.5dB to 15dB shape factor for a single tuned circuit. I have done this for several shape factors and numbers of stages, **Fig. 3**. If the working Q of the tuned circuits was very high, the 60dB to 6dB shape factor of the N=2 IF strip of Ref. 2 would be 31.7:1.

Also shown in Fig. 3 is the 6dB to 1dB shape factor, which it turns out actually improves with the number of stages. The passband becomes squarer with an increasing number of stages – something I had not previously realised. The improvement is not dramatic. There is little change beyond three stages. But it is nonetheless useful.

Note the assumption that $x_l - x_c$ (or *vice versa*) is still small compared to $2\pi f_{rL}$ or, equally, to the reactance of the capacitor at resonance. For a single tuned circuit, this means that the calculated detuning to A=60dB is only accurate if ωL is very much greater than 1000Ω. This is an impossible specification for a discrete LC circuit but not so for a crystal. Even a very mediocre crystal has a Q of 10,000 and some 100,000 or more.

Crystals are used in the more selective filters in a spectrum analyser to permit better resolution of closely spaced signals. This is especially important in an instrument having an on-screen logarithmic display of 60dB or more. In a simple instrument with a linear

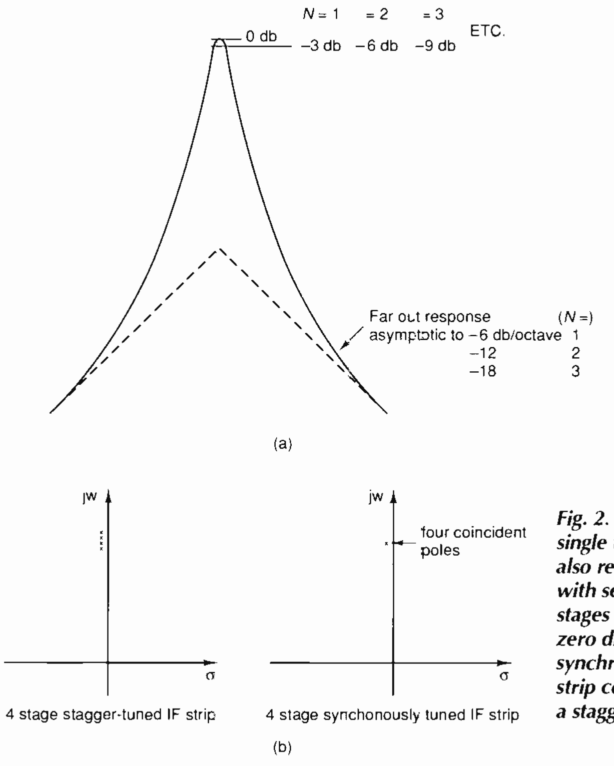


Fig. 2. Response curve for a single tuned circuit can also represent an IF strip with several identical stages (a). At (b) is a pole zero diagram of a synchronously tuned IF strip compared with that of a stagger tuned strip.

Shape factor ↓ / Poles (stages) →	1	2	3	4	5
1 : 60 db	1 : 1965	90.5	35.2	22.7	17.8
3 : 60 db	1 : 1002	49.2	19.6	12.7	10.0
6 : 60 db	1 : 579	31.7	13.0	8.6	6.8
1 : 60 db	1 : 3.4	2.85	2.71	2.64	2.62

Fig. 3. Pole versus shape-factor ratios for synchronously tuned IF strips with different numbers of stages.

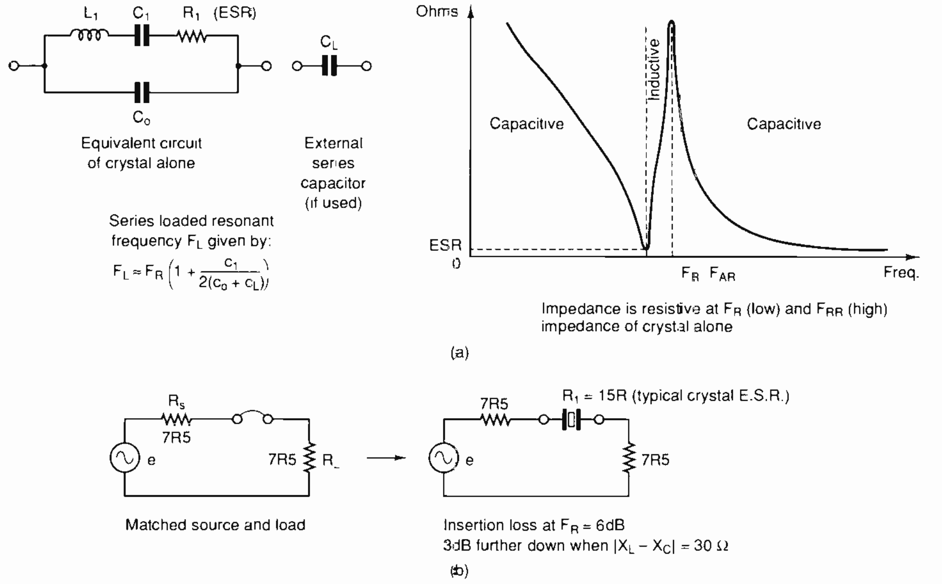


Fig. 4. Equivalent circuit of a quartz crystal, and the variation of its impedance in the vicinity of series resonance, including parallel resonance. Diagram (b) shows how, ignoring C_0, series resonance can provide a very narrow passband when working between source and load impedances comparable with its equivalent series resistance.

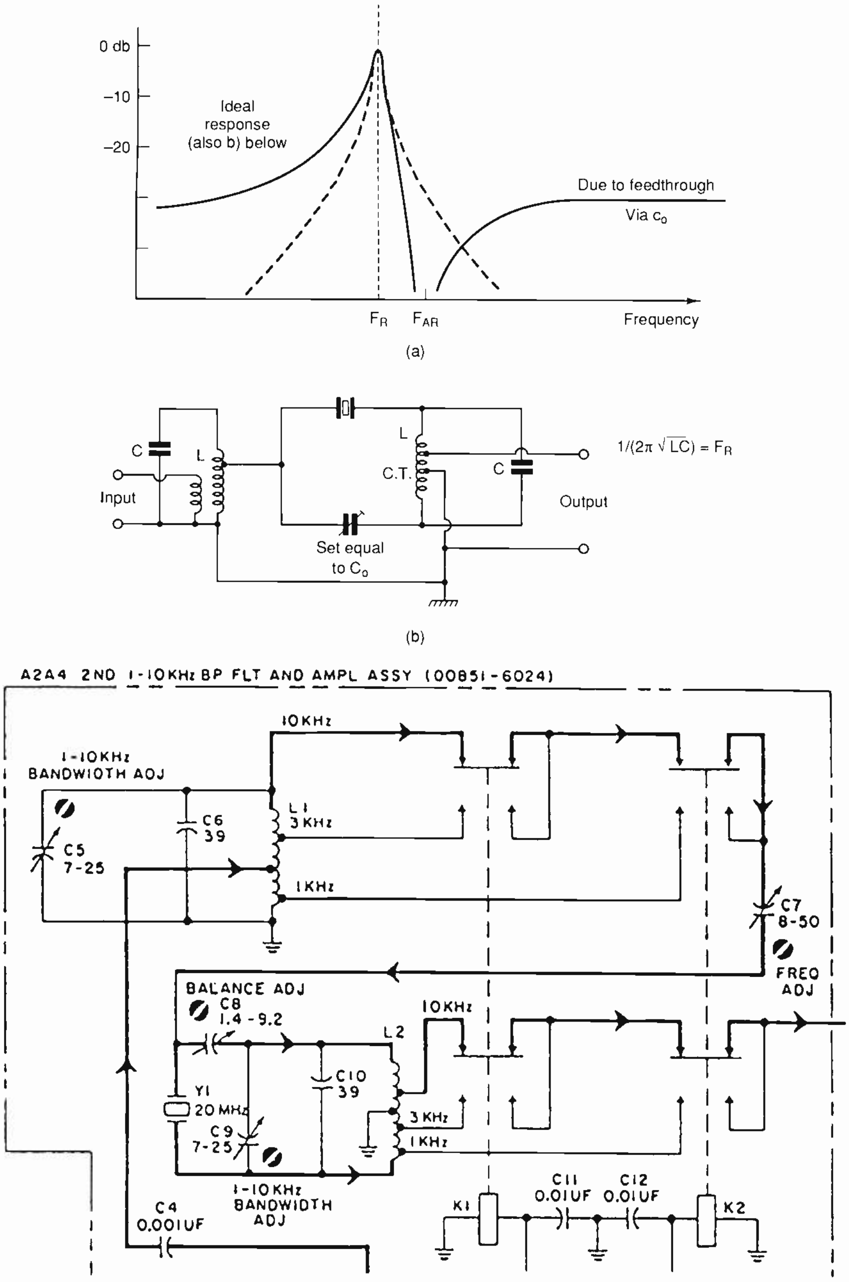
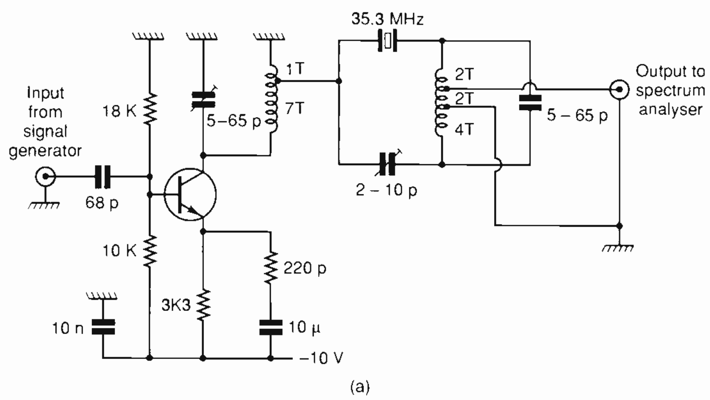


Fig. 5. Response of filter of Fig. 4 (b) taking into account C_0 is shown in the graph. Middle circuit illustrates obtaining a symmetrical response and high out-of-band attenuation by out-phasing the signal via C_0. Capacitance C_0, the trimmer and the centre tapped tank circuit form a balanced bridge, suppressing the effect of C_0. Main circuit (c) is as used in an early HP852A spectrum analyser to obtain resolution bandwidths of 1, 3 and 10kHz using a single crystal. Two such synchronously tuned stages were employed in cascade to obtain a satisfactory shape factor.



display however, as in Ref. 2, lower selectivity is acceptable.

Figure 4(a) shows the equivalent circuit of a crystal, C_0 being the capacitance between the two electrodes plus the strays due mounting and encapsulation. Components L_1, C_1 and R_1 are the electrical equivalents of the crystal's motional inductance and capacitance, and damping. Although the vibrational resonance of the crystal has a very high Q, there is some inevitable loss partly due to the quartz itself and partly due to the mounting arrangements.

In addition to a very high Q, the crystal has a very high L/C ratio, the significance of which will become apparent. A typical 35MHz crystal has an inductance of 8.8mH and a motional capacitance C_1 of 0.0023pF. The equivalent series resistance, R_1, might be typically 15Ω. The crystal's shunt capacitance C_0 is around 5pF. Figure **4(b)** shows how, ignoring C_0 for the moment, the series resonance of a crystal can be used to provide a very narrow bandwidth filter. When it is introduced into the particular circuit shown, insertion loss at resonance will be 6dB. Total circuit resistance will be 30Ω.

As an input signal is tuned away from resonance, the response will be a further 3dB down when the reactance of the crystal has risen to 30Ω. This corresponds to a fractional detuning δ which is easily arrived at. The reactance at resonance of L_1 or C_1 for

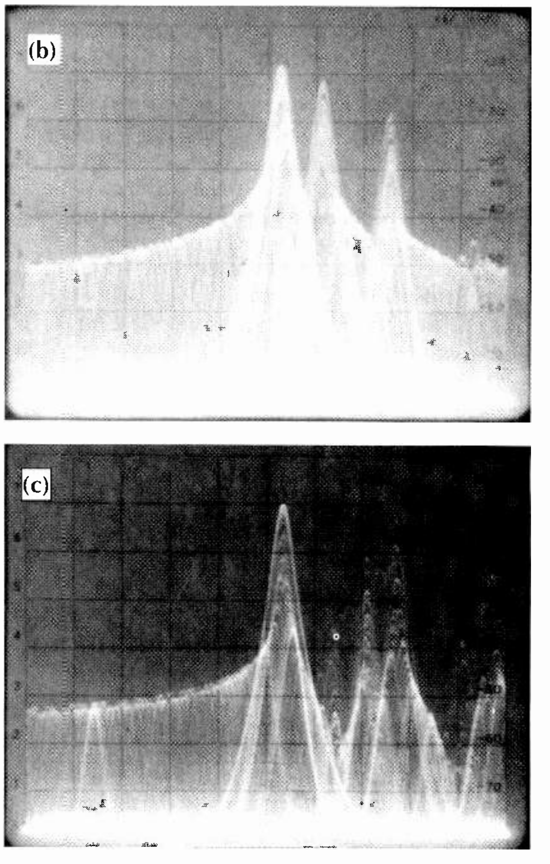


Fig. 6. Circuit diagram of an experimental crystal filter stage (a) using a 35.3MHz crystal with 5mm electrodes.

In (b), main (centre) and spurious responses of (a) are shown at 50kHz/div horizontal, 10dB/div. vertical, and analyser bandwidth of 10kHz. Actual filter responses are only a few hundred hertz wide. Much wider analyser bandwidth was selected for clarity.

Curve (c) is as (b) but for a crystal with 3mm electrodes. Note that spurious responses come in different places.

the typical crystal quoted is given by

$2\pi 35\ 000\ 000 \times 8.8 \times 10^{-3}$, or 1.935MΩ.

Reactance of the crystal will have risen to 30Ω when the reactance of the inductance has increased by 15Ω. This is because reactance of the capacitance will have fallen by the same amount. Since reactance of an inductor is directly proportional to frequency, it will have increased by 15Ω for a frequency increase of 15 parts in 1 935 000. At 35MHz, this amounts to 271Hz, giving a 3dB bandwidth of only 542Hz. The significance of the very high L/C ratio is now apparent. Assume however that the source and load impedances had each been 75Ω, giving an insertion loss in Fig. 4(b) of not 6dB but less than 1dB. Now the reactance of the crystal would need to rise to 165Ω to increase the loss by 3dB, giving about ten times as great a 3dB bandwidth.

Unfortunately, the presence of C_0 means the simple filter of Fig. 4(b) is not practical. At frequencies above the series resonance of L_1 and C_1, the series arm of the crystal looks inductive. At some frequency this inductance will form a parallel resonant circuit with C_0. This is often called the crystal's antiresonant frequency.

Reactance of 5pF at 35MHz is 910Ω so parallel resonance occurs when the reactance of L_1 has risen by 455Ω, i.e. at 35.008 230MHz. This is about 8kHz above the series resonance. In Fig. 4(b), this would result in a very large attenuation at that frequency. At other frequencies, the out-of-band attenuation would be limited to a modest figure due to signal feed-through via C_0.

Limiting can be avoided by the arrangement in **Fig. 5(b)**. Another capacitor, equal to C_0, is used to outphase the effect of C_0 itself, by incorporating it into a balanced bridge. Figure **5(c)** shows one of two such stages employed in the 20MHz IF stages of an early design of spectrum analyser. Working the crystal between a low source resistance (tapped well down the driving tank-circuit) and a low load resistance (second tank circuit very heavily loaded)

The tuned circuit

In the tuned circuit shown, drive is inductively coupled via a single closely coupled turn. This effectively generates a small voltage from a near zero source impedance generator in series with the inductor. The arrangement is actually a series resonant circuit. However for values of Q high enough to be useful, say twenty or greater, the performance is virtually the same as the current-fed parallel circuit of Fig. 1.

This is illustrated in the diagram below, which shows the situation at a frequency slightly above f_r. Here the reactance of the inductor is somewhat greater than that of the capacitor. The usual assumption that the capacitor is loss free, and the Q determined solely by the inductor, has been made. It is also assumed that Q is large so that $\omega L >> r$, the coil's series rf loss resistance.

At f_r, i.e. on tune, θ is zero and circulating current i is e/r. Output voltage across the capacitor V_o is $i.x_c$ where x_c is the capacitor's reactance at f_r, namely $1/(2\pi f_r C)$. If, for example, frequency rises by 1%, then so does the reactance of the inductor. Reactance of the capacitor on the other hand falls by 1% – almost exactly. This result is due to the Binomial Theorem. The difference between $x_l - x_c$, shown in the second diagram below, has risen from zero to 2% of the reactance of either at resonance.

The third side of the triangle z is the impedance in which i now flows. If the value of i at resonance is taken to be unity, the off-tune value is $r/z=\cos\theta$. So if in the example Q were 50, $x_l - x_c$ would be 2% of Q_r, namely equal to r. Thus θ would be 45° and $1/z=\cos\theta=0.707$, or –3dB. This is the fall in the value of i, but since x_c has only fallen by 1% it is also approximately the fall in V_0. Cosine θ is thus the approximate per unit response of the circuit, i.e. the output relative to an assumed on-tune output of unity. Tan θ is $(x_l - x_c)/r$ which works out to be $Q(\omega/\omega_o - \omega_o/\omega)$ or approximately, courtesy of the Binomial Theorem again, $2Q\delta$, where δ is the 'per-unit' detuning; for 5% off tune δ is 0.05.

Armed with these approximate results, finding the detuning corresponding to any given relative attenuation is easy. For example, for 6dB down, first convert the attenuation to a 'per unit' value, i.e. –6dB is equivalent to 0.5. Now take the inverse cosine, in this case 60°, take the tangent of 60° 1.73 and this value equals $2Q\delta$. So any tuned circuit for which our approximations are valid is 6dB down at $\delta=1.73/(2Q)$, e.g. at δ is 0.0173 (1.73% off tune) if Q is 50.

The following works out the 'per unit' or fractional detuning δ for any attenuation AdB down, for any number of stages N the selectivity of each being given by Q, on a calculator.

```
ENTER N Kinl ENTER A
divide Koutl = divide 20 =
10^x  1/x inv cos tan
divide 2 = divide Q =
(answer)
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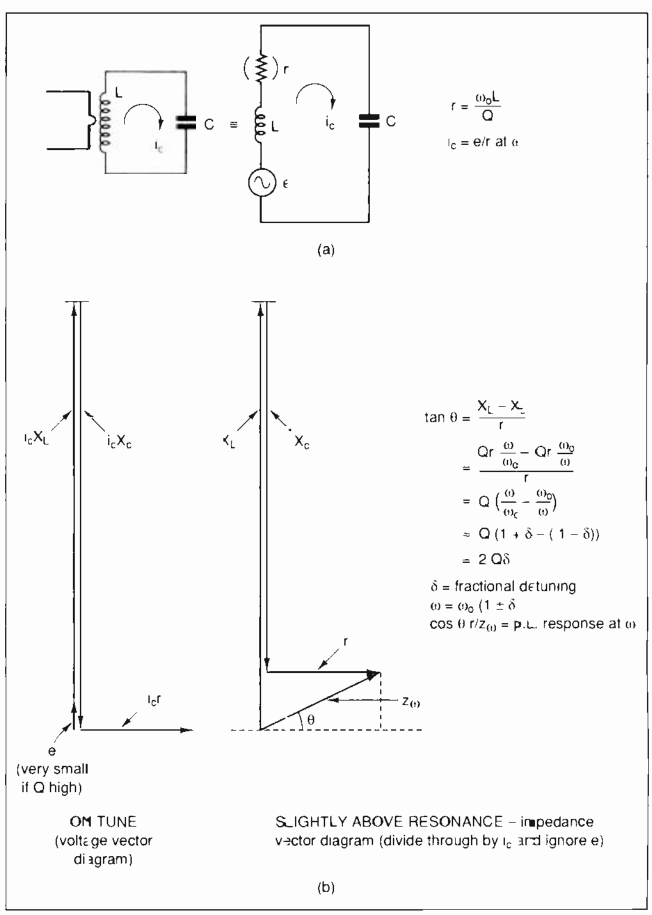
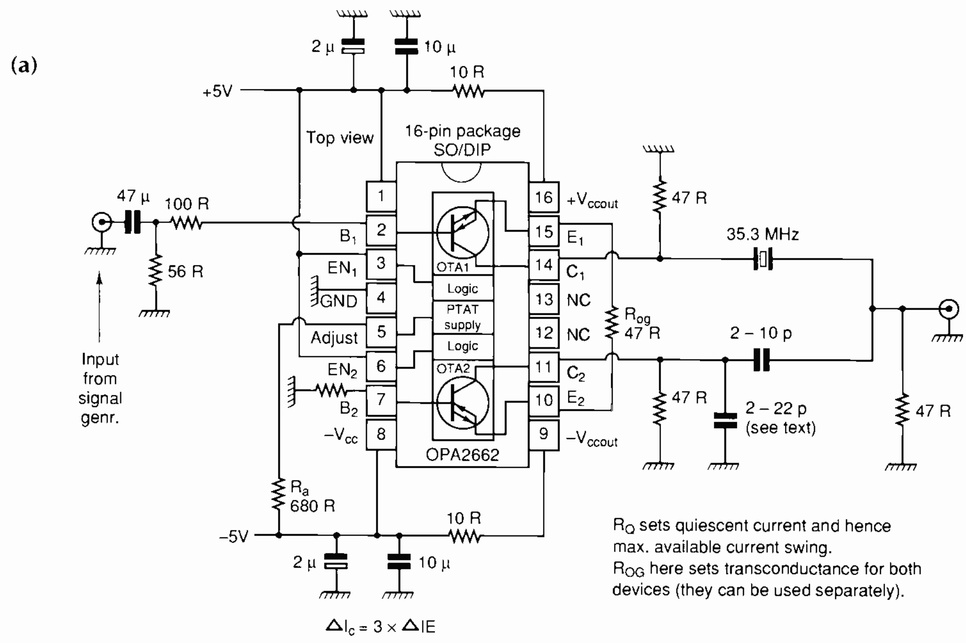


Inductively coupled tuned circuit and its equivalent in series-excited form. Associated vector diagrams are also shown.



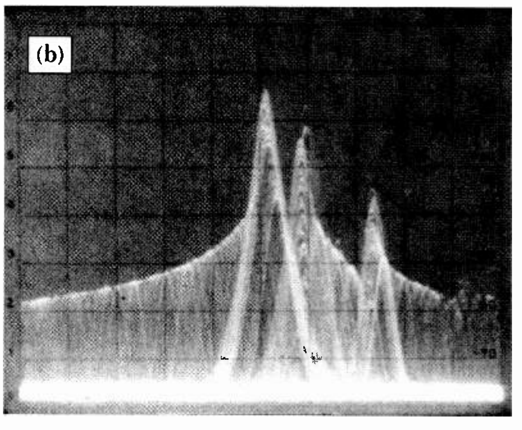


Fig. 7. Using a OPA2662 dual transconductance amplifier to provide a balanced drive to the filter section without a centre-tapped coil (a). In addition to providing complementary outputs, this IC also handles single-ended to balanced conversion. Performance of (a) using the 35.3MHz crystal with 5mm electrodes is shown in (b). It is identical to that of the circuit of Fig. 6(a) – compare with Fig. 6(b).

provides the narrowest bandwidth. Between high source and load resistances it provides the widest bandwidth.

When using crystals to implement narrow-band synchronously-tuned filters, there are other problems to cope with, in addition to C_0. For instance, at frequencies somewhat above f_r a crystal usually has one or more subsidiary resonances or "spurious responses". This is illustrated in **Figs 6(a)** and **(b)**. The spectrum analyser used had no built in tracking generator; a signal generator was swept slowly back and forth across the band. Actual filter responses are very narrow, a much wider analyser resolution bandwidth being selected for clarity.

Since at least two such stages would usually be necessary to obtain the required shape factor, the second stage would use a crystal with the same f_r, but where the spurious resonances fell at different frequencies. While that in Fig. 6(b) has 5mm electrodes, the crystal in Fig. **6(c)** has 3mm electrodes (from McKnight Fordahl, Hythe). Note that the two halves of the centre-tapped second tank-circuit, Fig. 6(a), should ideally be very tightly coupled, especially if output is being taken from another tap on the coil.

Alternatively, the coil could be replaced by a centre-tapped resistor, the two ends connecting to an op-amp whose common-mode rejection is maintained up to radio frequencies. Example of such ICs are the *LT1193* from Linear Technology and the *MAX436* from Maxim. Both these devices have gain-defining arrangements independent of the inverting and non-inverting inputs. This makes both inputs high impedance nodes. The filter section itself, being entirely passive, could be used in reverse, i.e. the balanced end could be the input.

Using the filter in reverse provides yet another opportunity to replace the centre-tapped tank circuit with an IC, as shown in **Fig. 7**. This circuit uses a Burr-Brown *OPA2662* dual transconductance amplifier. A small trimmer from pin 14 to ground was necessary to maximise the stop-band rejection by adjusting the balanced outputs for exact anti-phase.

When using crystals in synchronously tuned IF strips, the final hurdle to overcome is the selection tolerance on f_r. The tighter the tolerance the higher the cost. As a result, the final adjustment is made with the aid of a series trimmer, shown in Figure 5(c) as C_7. A fixed capacitor is used in this position as in the other crystal filter stage. The crystals are thus operated slightly above series resonance, where their inductive reactance resonates with the series capacitor or trimmer. ■

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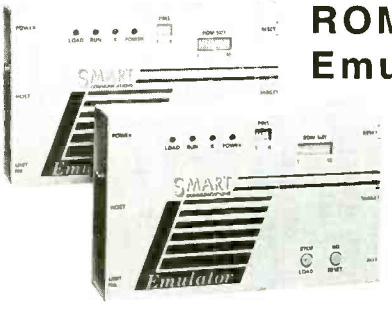

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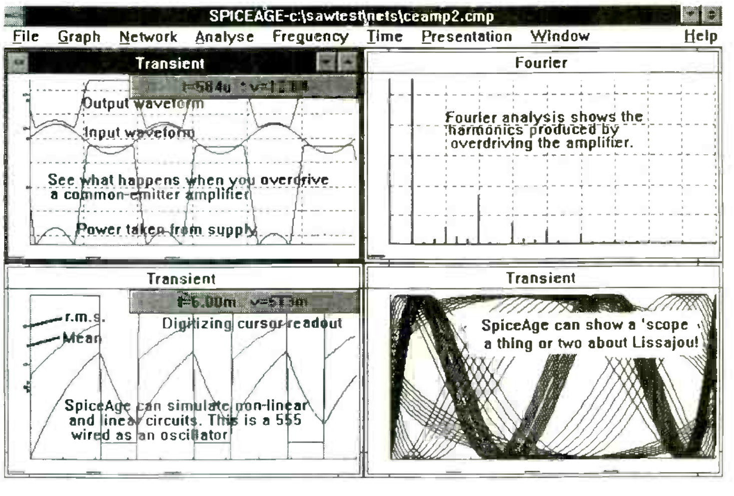
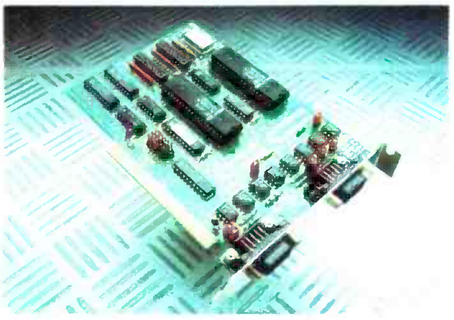
V3 provides digital simulation an order of magnitude faster than before. It has a 32 channel logic analyser display, input signal bus grouping plus more digital models, but unlike logic simulators, you can of course see the analogue effects of capacitive loads, pull-ups, diodes etc. Analogue developments include bundling of the Zetex SPICE library and a brand new opamp model.



Existing SpiceAge for Windows owners will be notified of these developments by post. Owners of the Original SPICE-AGE, BITSPICE, LOGANOU and NODALOU should contact us for upgrade details. If you are new to SpiceAge for Windows, please phone us for a demonstration kit. Those Engineers Ltd, 31 Birkbeck Road, LONDON NW7 4BP. Tel: 081-906 0155, Fax: 081-906 0969.

CIRCLE NO. 112 ON REPLY CARD

Dual port serial communications for your PC



The PC 47,48 and 49AT boards each provide two independent serial ports for any PC/XT/AT(ISA) computer. RS232, RS422 and RS485 standards are supported and all combinations are possible with this range of low power boards.

9 pin D connectors are provided for the RS422 and 485 ports. RS232 can be connected via 9 or 25 way D connectors and charge pump circuitry ensures signal levels in excess of 7V are transmitted.

Interrupt and base addresses are independently selectable for each port, full, half duplex and multidrop communications are fully supported and all boards use the industry standard 82C450, UART.

Designed and manufactured by Amplicon Liveline each board is supplied with a comprehensive technical manual and interrupt driven device driver software is available.

Write in number 1

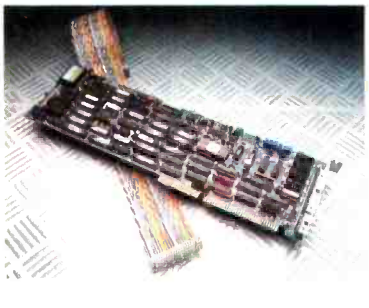
750kHz professional data acquisition with Windows support

PC226 from Amplicon Liveline provides 16 true differential 12 bit analog inputs each with dynamically programmable gain. PC226 has sample rates up to 400kHz multichannel and 750kHz single channel, programmable scanning hardware, flexible triggers and a 2048 sample FIFO to ease programming in high speed applications.

PC 226 is supplied with menu driven software for DOS and Windows, LabTech Notebook drivers and comprehensive well documented libraries for most popular high level languages.

Optional software support for Microsoft Windows includes a complete Dynamic Link Library (DLL) and two icon driven packages, Signal Centre for signal capture and analysis and TRACS for process monitoring, visualisation and control.

Write in number 2



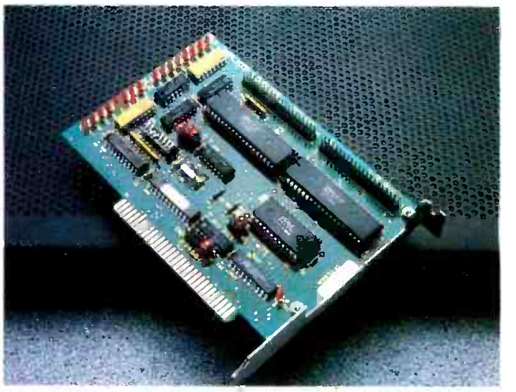
48 lines TTL I/O with 16bit counter timers

PC 14AT available from Amplicon Liveline is a high quality general purpose interface board for PC/XT/AT(ISA) computers.

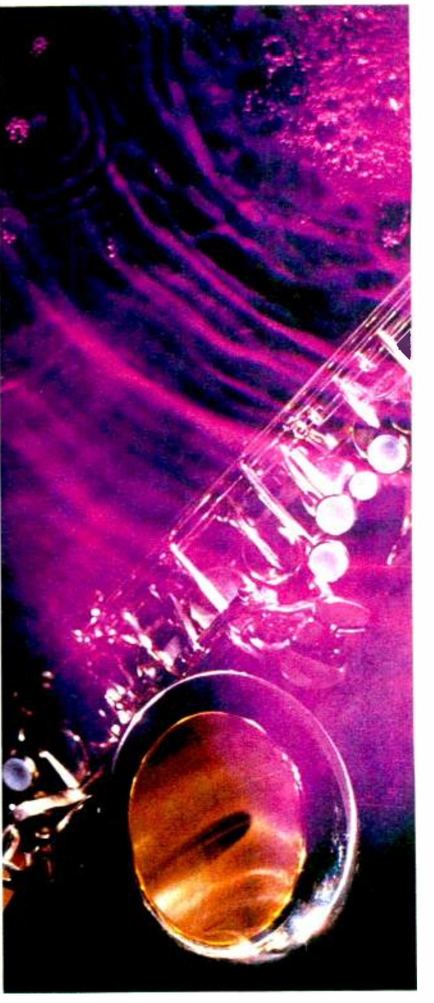
The board has 48 lines of TTL compatible digital I/O provided as six 8 bit ports four of which can be programmed to be all inputs or all outputs and two which can be split to be 4 inputs and 4 outputs if required. There are also three 16bit counter timers which can be used to generate and measure pulses at up to 5MHz.

An on board 4MHz crystal oscillator is also included on PC 14AT along with LEDs showing the status of a selection of the I/O ports, these can be used as programming and debugging aids.

PC 14AT is suitable for a wide variety of interface, monitoring and control applications



and an LP (low power) version PC 14LP is available for installation in laptop computers, both boards have flexible base address and interrupt support. **Write in number 3**



Some of the most common sources of distortion in audio power amplifiers relate to the electrical and physical layout of the circuit, an area overlooked by many designers. In his continuing search for the perfect audio amplifier Douglas Self explains the mechanisms.

Distortion in power amplifiers

6: the remaining distortions

The previous two parts of this series considered closely the distortion produced by amplifier output stages: a basically conventional but well designed Class-B amplifier with proper precautions taken against the various sources of nonlinearity can produce insignificant levels of distortion. That which is generated is mainly due to the difficulty of reducing high order crossover nonlinearities with negative feedback that has declining effectiveness with frequency. For 8Ω loads this is the major source of distortion. For convenience, I have chosen to call such a device a *blameless* amplifier.

Distortion 3: quiescent current control

An optimised amplifier requires minimisation of output stage gain irregularities around the crossover point by holding the quiescent current I_q at its optimal value. Increasing I_q to move into Class-AB makes the distortion worse, not better, as g_m-doubling artifacts are generated.

The initial setting of quiescent current is simple, given a distortion analyser to get a good view of the residual; keeping that setting under varying operating conditions is a much greater problem because I_q depends on small voltages established across low value resistors by power devices with thermally dependant V_{be} drops.

How accurately does quiescent current need to be maintained? I wish I could be more specific on this. Some informal experiments with Blameless CFP type outputs at 1kHz indicate that crossover artefacts on THD residual seem to stay at roughly the same level, partly submerged in the noise, over an I_q range of about 2:1, the centre of this region being around 20mA. Results may well be different for emitter follower type outputs.

This may seem a wide enough target, but given that junction temperature of power devices may vary over a 100°C range, this is not so. Some kinds of amplifier (eg current dumping types) manage to evade the problem altogether, but in general the solution is thermal compensation: the output stage bias voltage is set by a temperature sensor (usually a V_{be} multiplier transistor) coupled as closely as possible to the power devices.

There are inherent inaccuracies and thermal lags in this sort of arrangement leading to programme dependency of I_q. A sudden period of high power dissipation will begin with the bias current increasing above optimum, as the junctions will heat up very quickly. Eventually the thermal mass of the heatsink will respond, and the bias voltage will be reduced. When the power dissipation falls again, the bias voltage will now be too low to match the cooling junctions and the amplifier will be under biased, producing crossover spikes that may persist for some minutes. This is well illustrated in an important paper by Sato[1].

Emitter follower outputs

The major drawback of emitter follower output stages is thermal stabilisation. This can cause production problems in initial setting up since any drift of quiescent current will be very slow as a lot of metal must warm up.

For EF outputs, the bias generator must attempt to establish an output bias voltage that is a summation of four driver and output V_{be}'s. These do not vary in the same way. It seems at first a bit of a mystery how the EF stage, which still seems to be the most popular output topology, works as well as it does. The probable answer is **Fig. 1**, which shows how driver dissipation (averaged over a complete cycle) varies with peak output level for the three kinds of EF output, and for the CFP configuration. The Spice simulations used to generate this graph used a triangle waveform to give a slightly closer approximation to the peak-average ratio of real waveforms. The rails were ±50V, and the load 8Ω.

It is clear that the driver dissipation for the EF types is relatively constant with power output, while the CFP driver dissipation, although generally lower, varies strongly. This is a con-

Blameless amplifiers

I have adopted the term *blameless* to describe a Class-B amplifier designed in accordance with the philosophy of this series, with the use of simple circuit enhancements to minimise distortions 1,2 and 4, and correct layout to prevent distortions 5,6 and 7. Such a device will still suffer from output stage distortion 3, and so exhibit measurable distortion at high frequencies due to the difficulty that NFB has in dealing with the high order crossover distortion products generated by a conventional (but well designed) output stage. Distortion will usually be greater when driving loads below 8Ω.
The word is specifically chosen to imply the avoidance of error but not perfection.

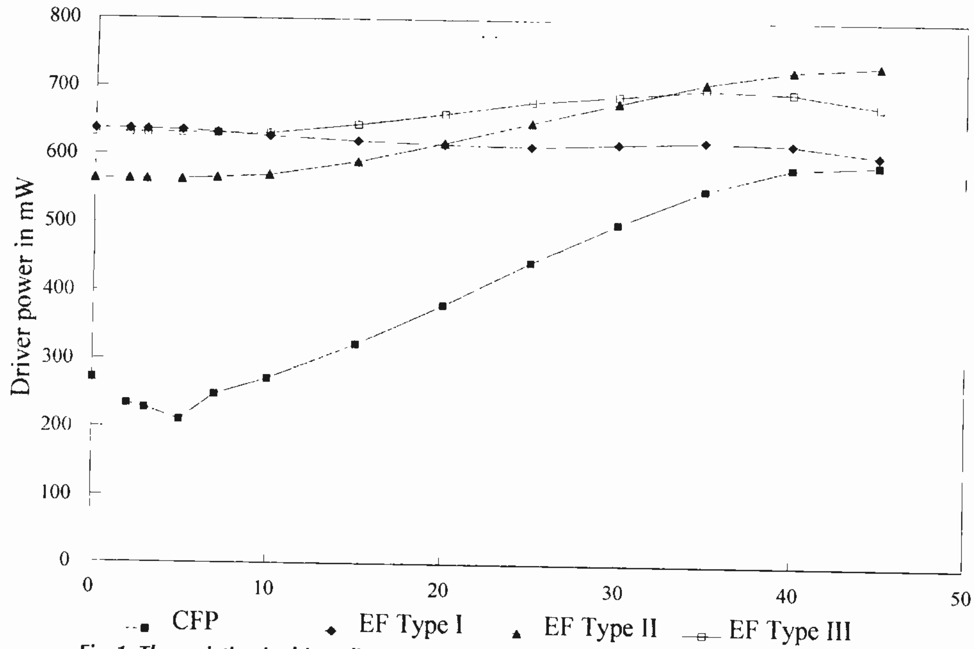


Fig. 1. The variation in driver dissipation with output for the three EF output topologies and the CFP output. All three EF types keep driver power fairly constant, simplifying the thermal compensation problem.

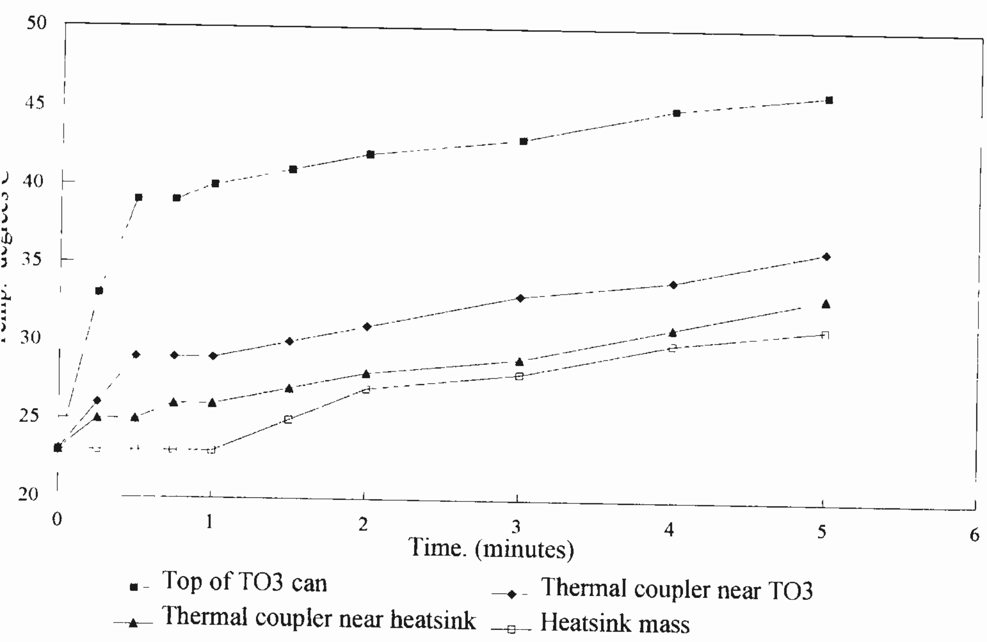


Fig. 2. Thermal response of a TO3 coupled to a large heatsink when power is abruptly applied. The top of the TO3 can responds most rapidly.

sequence of the different operation of these two kinds of output. In general, the drivers of an EF output remain conducting to some degree for most or all of a cycle, although the output devices are certainly off half the time.

In the CFP, however, the drivers turn off almost in synchrony with the outputs, dissipating an amount of power that varies much more with output. This implies that EF drivers will work at roughly the same temperature, and can be neglected in arranging thermal compensation; the temperature dependent element is usually attached to the heatsink to compensate for the junction temperature of the output devices alone. The Type I EF output keeps its drivers at the most constant temperature.

The above does not apply to integrated Darlington outputs, with drivers and assorted emitter resistors combined in one ill-conceived package where the driver sections are directly heated by the output junctions. This works directly against quiescent stability.

The drawback with most thermal compensation schemes is the slow response of the heatsink mass to thermal transients. The obvious solution is to find some way of getting the sensor closer to one of the output junctions. If TO3 devices are used, then the flange on which the actual transistor is mounted is as close as one can get without a hacksaw. This is however clamped to the heatsink, and almost inaccessible, though it might be possible to hold a sensor under one of the mounting bolts. A simpler solution is to mount the sensor on the top of the TO3 can. This is probably not as accurate an estimate of junction temperature as the flange would give, but measurement shows the top gets much hotter much faster than the heatsink mass, so while it may appear unconventional, it is probably the best sensor position for an EF output stage.

Fig. 2 shows the results of an experiment designed to test this. A TO3 device was mounted on a thick aluminium L-section thermal coupler in turn clamped to a heatsink; this construction represents many typical designs. Dissipation equivalent to 100W/8Ω was suddenly initiated, and the temperature of the various parts monitored with thermocouples. The graph clearly shows that the top of the TO3 responds much faster, and with a larger temperature change, though after the first two minutes the temperatures are all increasing at the same rate. The whole assembly took more than an hour to asymptote to thermal equilibrium.

The CFP output

In the CFP configuration, the output devices are inside a local feedback loop, and play no significant part in setting I_q, which is affected only by thermal changes in the drivers' V_{be}. Such stages are virtually immune to thermal runaway; I have found that assaulting the output devices with a powerful heat gun induces only insignificant I_q changes. Thermal compensation is mechanically simpler as the V_{be} multiplier transistor is simply mounted on one of the driver heatsinks, where it aspires to mimic the driver junction temperature. It is now practical to make the bias transistor of the same type as the drivers, which should give the best matching of V_{be}, though how important this is in practice I wouldn't like to say[2].

Because driver heatsinks are much smaller than the main heatsink, the thermal compensation time constant is now measured in tens of seconds rather than tens of minutes, and should give much shorter periods of non optimal quiescent current than the EF output topology.

Distortion 4: nonlinear loading of the voltage amplifier stage by the nonlinear impedance of the output stage.

This distortion mechanism was examined in Part 3 from the point of view of the voltage amplifier stage. Essentially, since the VAS provides all the voltage gain, its collector impedance tends to be made high. This renders it vulnerable to nonlinear loading unless it is buffered.

Making a linear VAS is most easily done by applying a healthy amount of local negative feedback via the dominant pole Miller capacitor, and if VAS distortion needs further reduction, then the open loop gain of the VAS stage must be raised to increase this local feedback. The direct connection of a Class-B output can make this difficult for, if the gain increase is attempted by cascoding with intent to raise the impedance at the VAS collector, the output stage loading will render this almost completely ineffective. The use of a VAS buffer eliminates this effect.

As explained previously, the collector impedance, while high at LF compared with other circuit nodes, falls with frequency as soon as C_{dom} starts to take effect, and so the fourth distortion mechanism is usually only visible at LF. It is also masked by the increase in output stage distortion above dominant pole frequency P1 as the amount of global NFB reduces.

The fall in VAS impedance with frequency is demonstrated in **Fig. 3**, obtained from the Spice conceptual model outlined previously, with real life values. The LF impedance is basically that of the VAS collector resistance, but halves with each octave once P1 is reached. By 3kHz it is down to 1kΩ and still falling. Nevertheless, it can remain high enough for the input impedance of a Class-B output stage to significantly degrade linearity, the actual effect being shown in **Fig. 4**.

An alternative to cascoding for VAS linearisation is to add an emitter follower within the VAS local feedback loop, increasing the local NFB factor by raising effective beta rather than the collector impedance. Preliminary tests show that as well as providing good VAS linearity, it establishes a lower VAS collector impedance across the audio band. It should be more resistant to this type of distortion than the cascode version.

Figure 5 confirms that the input impedance of a conventional EF Type I output stage is anything but linear; the data is derived from a Spice output stage simulation with optimal I_q. Even with an undemanding 8Ω load, the impedance varies by 10:1 over the output voltage swing. Interestingly, the Type II EF output (using a shared drive emitter resistance) has a 50% higher impedance around crossover, but the variation ratio is rather greater. CFP output stages have a more complex variation that includes a precipitous drop to less than 20kΩ around the crossover point. With all types under biasing produces additional sharp impedance changes at crossover.

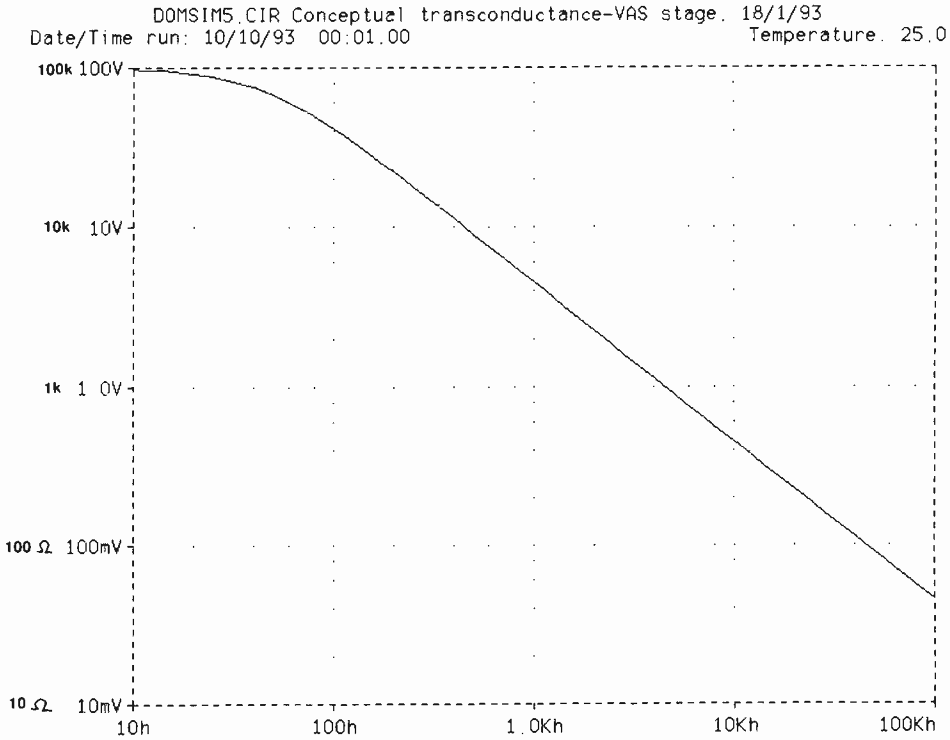


Fig. 3. Distortion 4. The impedance at the VAS collector falls at 6dB/octave with frequency.

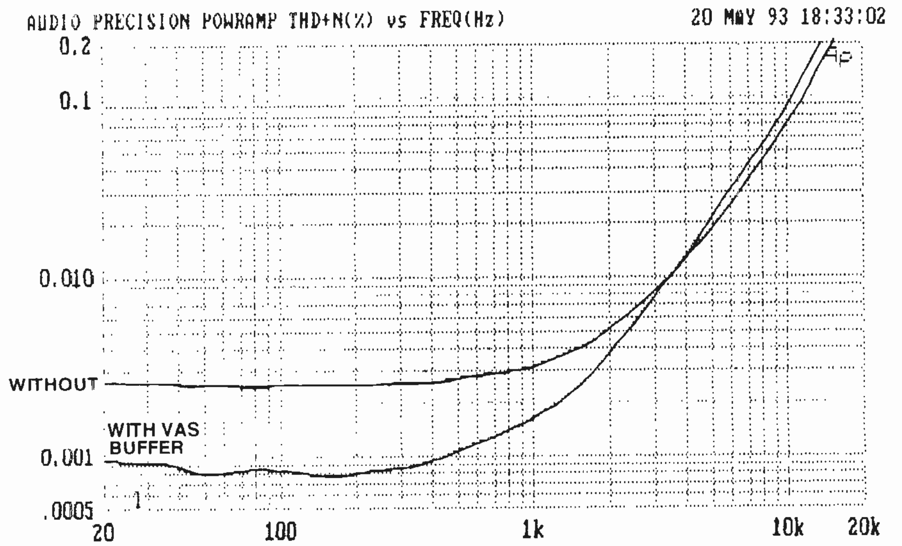


Fig. 4. Distortion 4 in action. The lower trace shows the result of its elimination by the use of a VAS buffer.

Distortion 5: supply ground loops

Virtually all amplifiers include some form of rail decoupling apart from the main reservoir capacitors; this is usually required to improve HF stability. The standard decoupling arrangements include small to medium sized electrolytics (say 10 - 1000μF) connected between each rail and ground, and an inevitable consequence is that voltage variations on the rails cause current to flow into the ground connection chosen. This is just one mechanism that defines the power supply rejection ratio (PSRR) of an amplifier, but it is one that can do serious damage to linearity .If we assume a simple unregulated power supply, (and there are excellent reasons for using such a supply[3]) then these rails have a significant AC impedance and superimposed voltage will be due to amplifier load currents as well as 100Hz ripple. In Class-B, these supply rail currents are halfwave rectified sine pulses with strong harmonic content, and if they contaminate the signal, then distortion will degrade badly. A common route for interaction is via decoupling grounds shared with input or feedback networks, and a completely separate decoupler ground usually effects a total cure. This point is easy to overlook, and attempts to improve amplifier linearity by labouring on the input pair, VAS, etc., are doomed to failure unless this distortion mechanism is eliminated first.

As a rule it is simply necessary to take the decoupling ground separately back to the ground star point, as shown in **Fig. 6**. Note that the star point A is defined on a short spur from the heavy connection joining the reservoirs; trying to use B as the star point will introduce ripple due to the large reservoir charging current pulses passing through it.

Figure 7 shows the effect on an otherwise optimised amplifier delivering 60W/8Ω, with 220μF rail decoupling capacitors. At 1kHz distortion has increased by more than ten times, which is quite bad enough. However, at 20Hz the THD has increased at least 100 fold, turning a very good amplifier into a profoundly mediocre one with a single misconceived connection.

If the residual on the supply rails is examined, the ripple amplitude will usually be found to exceed the pulses due to Class-B signal current, and so some of the "distortion" on the upper curve of the plot is actually due to

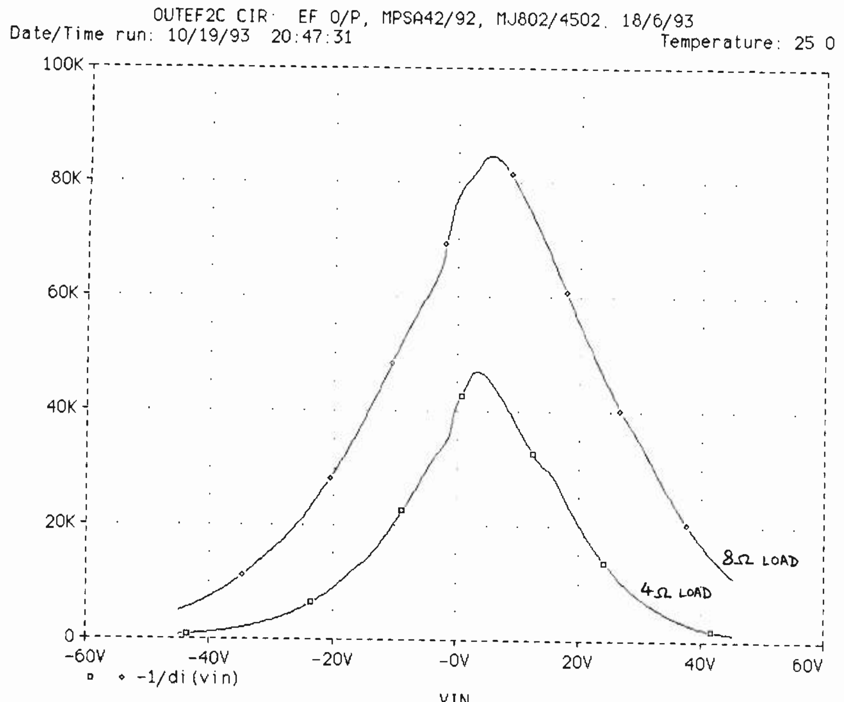


Fig. 5: Distortion 4 and its root cause. The nonlinear input impedance of an EF Class B output stage.

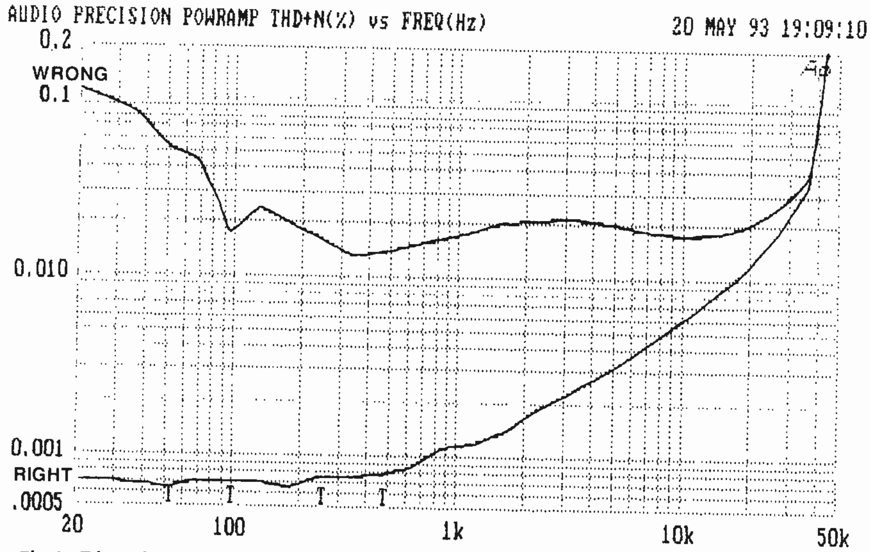


Fig. 7: Distortion 5 in action. The upper trace was produced simply by taking the decoupler ground from the star point and connecting it via the input ground line instead.

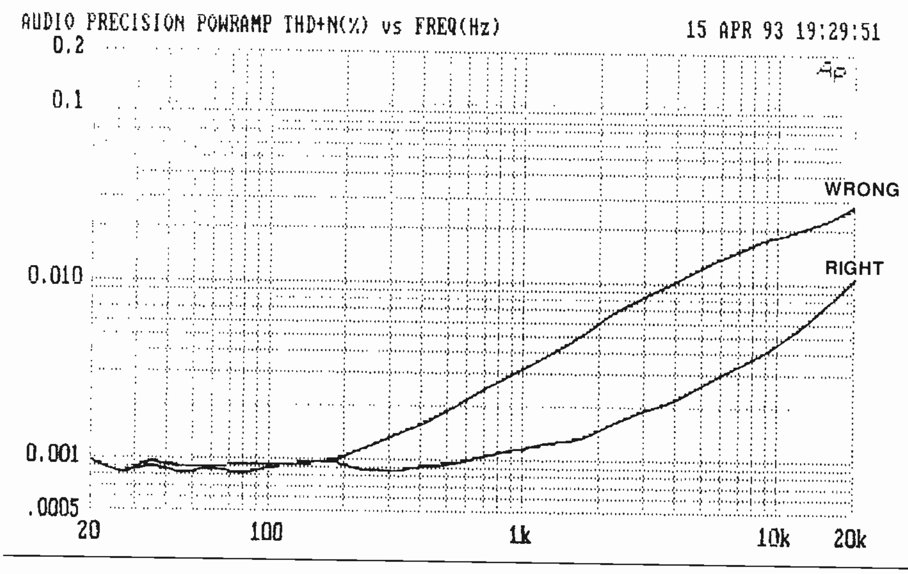


Fig. 8. Distortion 6 exposed. The upper trace shows the effects of Class B rail induction into signal circuitry.

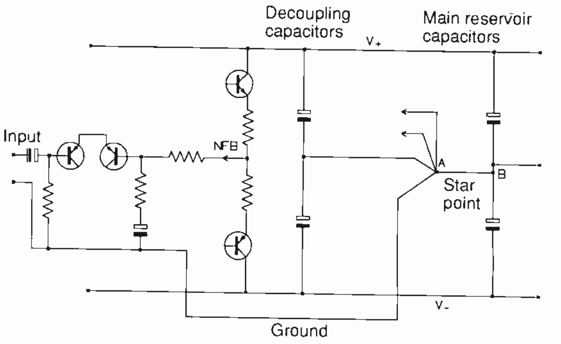


Fig. 6. Distortion 5. The correct way to route decouple grounding to the star point.

ripple injection. This is hinted at by the phase crevasse at 100Hz, where ripple partly cancelled the signal at the instant of measurement. Below 100Hz the curve rises as greater demands are made on the reservoirs, the signal voltage on the rails increases, and so more distorted current is forced into the ground system.

Generally, if an amplifier is made free from ripple injection under drive conditions, shown by a THD residual without ripple components, there will be no distortion from the supply rails and the complications and inefficiency of high current rail regulators are unnecessary.

There has been much discussion of PSRR induced distortion in *EW+WW* recently, led by Ben Duncan[4] and Greg Ball[5]. I part company with Ben Duncan on this issue where he assumes that a power amplifier is likely to have 25dB PSRR, making expensive high power DC regulators the only answer. He agrees that this sort of PSRR is highly unlikely with the relatively conventional amplifier topologies I have been considering[6].

Greg Ball also initially assumes that a power amp has the same PSRR characteristics as an op-amp, ie falling steadily at 6dB/octave. There is absolutely no need for this to be so, given a little RC decoupling, and Ball states at the end of his article that "a more elegant solution... is to depend on a high PSRR in the amplifier proper."

Power supply rejection

For low noise and distortion, all the obvious methods of rail injection must be attended to as a matter of routine. I therefore give here some guidelines that I have found effective with unregulated supplies:

- The input pair must have a tail current source. A tail made of two resistors decoupled mid way is simply not adequate.
- This tail source will probably be biased by a pair of diodes or a led fed from a resistor to ground. This resistor should be split and the midpoint decoupled with an electrolytic of about 10μF to the appropriate rail.
- If a cascode transistor is used in the VAS, then its base will need to be biased about 1.2V above whichever rail the VAS emitter sits on; if this is implemented with a pair of diodes then further decoupling seems unnecessary.
- Having taken care of the above, the PSRR will now be limited by injection from the neg-

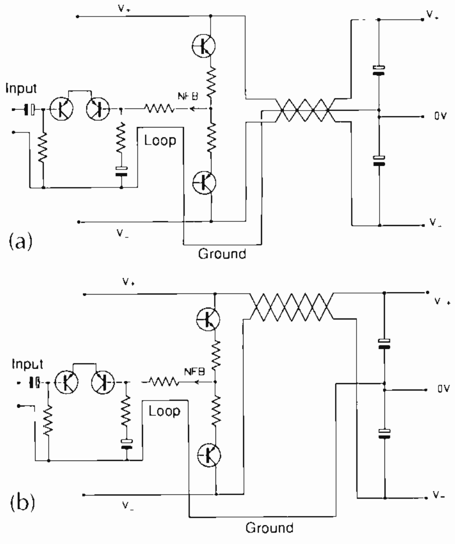


Fig. 9. Distortion 6. Countermeasures against the induction of distortion from the supply rails. 9b is usually more effective.

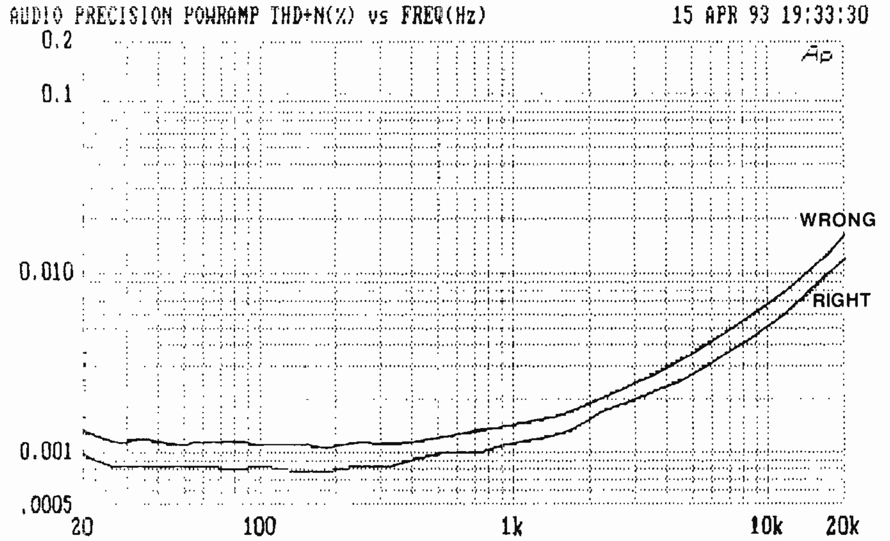


Fig. 11. Distortion 7 at work. The upper trace shows the result of a mere 6mm of heavy gauge wire between the output and the feedback point.

ative rail by a mechanism that is not yet fully clear. RC decoupling can however reduce this to negligible levels.

This is not the whole story on power rail rejection, but it does provide a starting point.

Distortion 6: induced output current coupling

This distortion mechanism, like the previous case, stems directly from the Class-B nature of the output stage. Assuming a sine input, the output hopefully carries a good sinewave, but the supply rail currents are halfwave rectified sine pulses, which are quite capable of inductive crosstalk into sensitive parts of the circuit. This can be very damaging to the distortion performance, as **Fig. 8** shows.

The distortion signal may intrude into the input circuitry, the feedback path, or even the cables to the output terminals. The result is a kind of sawtooth on the distortion residual that is very distinctive, an extra distortion component which rises at 6dB/octave with frequency.

This effect appears to have been first publicised by Cherry[7], in a paper that deserves much more attention than it appears to have got. Having examined many power amplifiers, I feel that this effect is probably the most widespread cause of unnecessary distortion.

Effects of this distortion mechanism can be reduced below the measurement threshold by taking care over supply rail cabling layout relative to signal leads, and avoiding loops that will induce or pick up magnetic fields. There are no precise rules for layout that would guarantee freedom from rail induction since each amplifier has its own physical layout and the cabling topology needs to take this into account. All I can do is give guidelines:

- Firstly, implement rigorous minimisation of loop area in the input and feedback circuitry; keep each signal line as close to its ground return as possible.
- Secondly, minimise the ability of the supply wiring to create magnetic fields.
- Thirdly, put as much distance between these two areas as you can. Fresh air beats shielding on price every time. **Fig. 9a** shows one straightforward approach to tackling the problem; the supply and ground wires are tightly twisted together to reduce radiation. In practice this doesn't seem too effective for reasons that are not wholly clear, but appear to involve the difficulty of ensuring exactly equal coupling between three twisted conductors.

In Fig **9b**, the supply rails are twisted together but kept well away from the ground return. This allows field generation, but if currents in the two rails butt together to make a sinewave at the output, they should do the same when the magnetic fields from each rail sum. There is an obvious risk of interchannel crosstalk with this approach in a stereo amplifier, but it does seem to deal most effectively with the induced distortion problem.

Distortion 7: nonlinearity from incorrect NFB connection point

Negative feedback is a powerful technique and must be used with care. Designers are repeatedly told that too much feedback can affect slew rate. Possibly true, though the greater danger is that an excess amplifier may produce tweeter frying HF instability.

However, there is another and more subtle danger. Class-B output stages are a hotbed of high amplitude halfwave rectified currents, and if the feedback takeoff point is even slightly asymmetric, these will contaminate the feedback signal making it an inaccurate representation of the output voltage. This will manifest itself as distortion, **Fig. 10**.

At the current levels in question, all wires and PCB tracks must be treated as resistances, and it follows that point *C* is not at the same potential as point *D* whenever TR_1 conducts. If feedback is taken from *D*, then a clean signal will be established here, but the signal at output point *C* will have a half wave rectified sinewave added to it, due to the resistance *C-D*. The output will be distorted but the feedback loop will do nothing about it as it does not know about the error.

Figure 11 shows the practical result for an

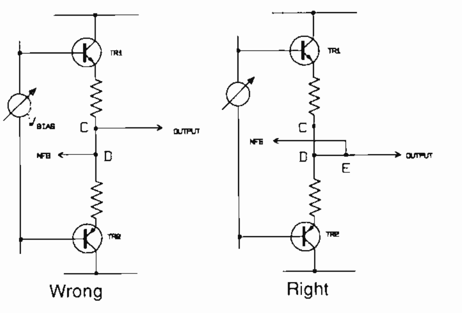


Fig. 10. Distortion 7. Wrong and right ways of arranging the critical negative feedback takeoff point.

amplifier driving 100W into 8Ω, with the extra distortion shadowing the original curve as it rises with frequency. Resistive path *C-D* that did the damage was a mere 6mm length of heavy gauge wirewound resistor lead.

Elimination of this distortion is easy, once you know the danger. Connecting the feedback arm to *D* is not advisable as it will not be a mathematical point, but will have a physical extent inside which the current distribution is unknown. Point *E* on the output line is much better, as the half wave currents do not flow through this arm of the circuit. ■

Next month: an example of a complete amplifier designed according to the principles in this series.

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LETTERS

Making ripples

I was very interested to see AM Wilkes' article "Simulating capacitor ripple" (*EW + WW*, September 1993), since I have analysed the behaviour of this circuit.

Wilkes' program makes the same assumption as most textbooks, that the transformer acts as a perfect voltage source, whose output voltage is not affected by the current drawn from it. One consequence of this assumption is that the peak voltage on the capacitor will always equal the V_{pk} of the supply.

In reality, the output voltage is subject to Ohms' Law due to the finite resistance of the secondary and primary windings. When the rectifier diodes are conducting, the transformer sees the capacitor effectively as a short circuit, and its own resistance is the predominant factor in limiting the charging current.

The effective voltage in the circuit equals the difference between the instantaneous induced voltage in the secondary and the voltage on the capacitor.

An immediate effect of this is to reduce the ripple voltage, since the peak voltage on the capacitor is reduced.

For example, suppose the load is such that the average voltage on the capacitor equals the rms of the transformer output. If the transformer was a perfect voltage source, the ripple voltage would necessarily be at least $V_{pk} - V_{rms}$. In reality, reasonable capacitor values can give a much smaller ripple voltage than this.

To give an example, I have just measured the dc resistance of the secondary of a nominal 10V, 1.2A transformer. It is about 0.4Ω.

Supposing the smoothing capacitor has 10V across it when the peak voltage of 14.1V occurs, then a charging current of 10.3A will be flowing (ignoring diode drops), and the voltage seen by the capacitor will be 10V, with dV/dt depending on the capacitor value.

This analysis is simplified since it ignores other current-limiting factors, such as the dc resistance of the transformer primary and the current drawn by the load.

John Harper
Valbonne, France

Lightning response

I found the report of a link between lightning and cosmic radiation (Research Notes, *EW + WW*, November 1993) established by Moscow and Los Alamos researchers rather exciting because it suggests the conditions close to terrestrial power lines may also enhance sky radiation and help explain the observations I reported in a previous article (*EW + WW*, November 1992).

Since the article appeared, a single joint test with the NRPB in mid 1993 on a 400kV line carrying 800A per phase showed a raw count increase of about 4% close to the line, which was not regarded as significant because it could have been due to local geology.

More recently, tests by the Swedish Radiation Research Institute using more sophisticated equipment produced rate curves rather resembling the plots in **Fig. 2** of the November 1992 article.

The problem is that relevant solar particle emission has fallen by about 70% since my original field work in 1990 and 1991, close to the peak of solar cycle 22, so exact replication of my original observations will have to wait for the peak of cycle 23 in about five years. In the meantime, research into the theoretical and practical implication of my observations may help to explain the growing body of epidemiological evidence that people living close to power lines may suffer some ill effects.

Research should also concentrate on detecting an 11 year cycle for human disease. Such a cycle would suggest that solar ionising radiation at levels well below those considered hazardous leads to power line focusing of natural radiation that may pose real dangers for those with a genetic susceptibility.

Anthony Hopwood
Upton-on-Severn, Worcester

Complex cables defy physics

The behaviour of an audio signal in a cable is far more complex than a simple first year text book explanation of Ohm's Law, which Drs Blake-Coleman and Yorke assume (*EW + WW*, May 1993).

The flow of ac electricity in a conductor is not uniform over the cross sectional area. Also the metal on the surface of a conductor is likely to be different from that at the centre due to oxidation. An oxidised metal is more likely to have semiconducting properties than the same conduction properties of the metal at the centre of the conductor.

There is no perfect insulator and insulating materials exhibit power loss and dielectric absorption, which can be easily measured.

The most significant influence on sound quality is the conductor used. Although copper is the most common metal used, other metals offer better sound, in particular silver. Silver plated copper offers a high quality performance where pure silver is too expensive.

Insulation will affect sound quality due to dielectric absorption. PTFE not only has the best sound quality as an insulator, but also the lowest measured dielectric absorption of common insulating materials. A PTFE insulated cable will give a more focused sound, like a pair of binoculars adjusted to give a sharper visual focus.

Conductor size affects sound quality. Even on high impedance connections between preamp and power amp, increasing the cross sectional area of conductor increases bass frequencies. Also some large diameter solid core cables attenuate treble frequencies.

Other factors claimed to influence sound quality include heat treatment, larger crystal size and purity of metal. Cables also sound better when the screen is removed, or when a shorter length of the same cable is used.

The engineering of a cable to reproduce music in the form of rapidly changing dynamically variable electrical voltage is a complex art that needs the scientific application of knowledge and skill to achieve success.

Graham Nalty Derby

Mr Nalty should have declared an interest – he sells exotic audio cables. Editor

Valve mystery

Older readers of your magazine will remember with nostalgia valves manufactured with trade names such as Cossor, Ferranti, Mullard, Marconi, Mazda, Osram and Tungsram.

There were also many lesser known companies who made or distributed valves during the 1920s and 1930s. Among these were Hivac, Lissen, Octron and 363.

I would be pleased to hear from readers who have any knowledge of these companies' valve manufacturing or distributing activities, particularly Lissen whose valve making is clouded in mystery.

Keith Thrower
Old Cedar, 12 Wychcotes
Caversham, Reading RG4 7DA

Sad subjectivism

I was interested to read Jerry Mead's defence of subjectivist listening tests (*EW + WW*, November 1993) but sad to see that his procedures apparently have no chance of deciding whether one amplifier is better than another.

The trouble is that his manifesto nowhere mentions double-blind A/B testing, or indeed any kind of A/B comparison at all. As far as I can discover, he simply listens to one amplifier, relying on his claimed ability to retain mental performance maps for several days between amplifier versions.

Such a procedure would be absolutely unacceptable even in a first-year psychology project, as decades of experience in psychoacoustics and related fields have shown beyond any possible quibble that experimenter expectancy renders the results valueless.

The fact that no audible differences are likely to exist unless the circuitry is seriously misconceived sets the final seal of sterility on the whole proceedings.

It is a well-worn debating technique to call for an open-mind when discussing these matters, though I can see no hint that Mead has considered the possibility that he might himself be wrong or misled.

Surely, to sail into an allegedly scientific investigation with an open-mind as to whether or not to measure things properly is not a triumph for tolerance, but a complete misunderstanding of what constitutes the scientific method.

Taking this philosophy to its logical conclusions debars us from any progress, as it becomes impossible to determine between truth and falsity.

Mead is absolutely correct when he says the mere fact that something cannot be measured or quantified does not mean it doesn't exist. However, if after 20 years of talking about it you still can't measure, or even demonstrate what you claim to be studying, most of us would regard this as a rather suspicious circumstance.

He also appears to overlook the two classic proofs that mysterious subjective nuances have no existence – the Hafler[1] and Baxandall[2] demonstrations. I have yet to meet a subjectivist who was able to argue his way past either of them.

Since no equally positive demonstration of the non-existence of ufos has been made one could argue that subjectivism is actually in rather worse shape than ufology.

I was glad to see the Mead-Duncan team take level matching seriously – until on a closer look I saw that it was just channel balance that was being so effectively policed.

Level matching between the A and

the B of an A/B comparison has long been known to be critical – the oldest trick in the book is to make amplifier A sound repeatably better by making it 1dB or so louder – the listener usually perceiving this as an improvement in clarity rather than amplitude. Of course, if you don't do A/B comparisons then this trick is harder to pull.

I refuse to believe in the existence of a sea-sickness capacitor until further proof is forthcoming. I simply can't believe that a capacitor in any position in an audio amplifier could induce anything resembling motion sickness.

How about showing us the circuit so we can judge for ourselves? The only audio-related uneasiness I usually experience is that which wells up when for the umpteenth time I am told: "I have evidence that backs up my views, but I am going to keep it secret."

I note Mead is curious about the mechanisms of hearing. Fortunately, there exists a huge body of knowledge on the subject of psychoacoustics and psychophysiology, though no-one would claim the subject is either an easy read or fully understood; after all, at the higher levels of processing it is the human brain doing the work, and understanding that may well be the ultimate challenge that faces us.

What is known in considerable detail is the low-level functioning of the ear, with particular reference to what is perceptible and what is not. It really is not on to claim that perceived amplifier performance is shrouded in mystery.

Douglas Self
Forest Gate, London

1. D Hafler, "A listening test for amplifier distortion", *HiFi News & RR*, Nov 1986.
2. P Baxandall, "Audible amplifier distortion is not a mystery", *Wireless World*, Nov 1977.

Doctor WHO

Douglas Self (Letters, *EW + WW*, October) should search a little wider before he condemns earlier writers on adverse and beneficial effects of exposure to elf, rf and microwave fields.

The World Health Organisation has just published in its environmental health series, "Electromagnetic fields 300Hz - 300GHz". It details hundreds of references from scientific, medical and physics authors on the effects on humans, animals and cell lines in *vivo* and in *vitro*.

He should also pause to muse that the WHO published in 1989 a text called "Non-ionising radiation protection". This is divided into sections on rf, ir, uv, sonic, elf and so on.

Is it likely that it would publish these books unless there are perceived hazards soundly based in research? Fracture and ulcer healing studies are reported from many sources worldwide. Indeed, St. Thomas' and Bart's hospitals are working on these lines.

It is especially interesting that many studies indicate that there are windows of frequency and amplitude which can, and do, affect immunocompetence (via free radical mechanisms at cellular level), bone healing, wound healing and subclinical electrosyndromes.

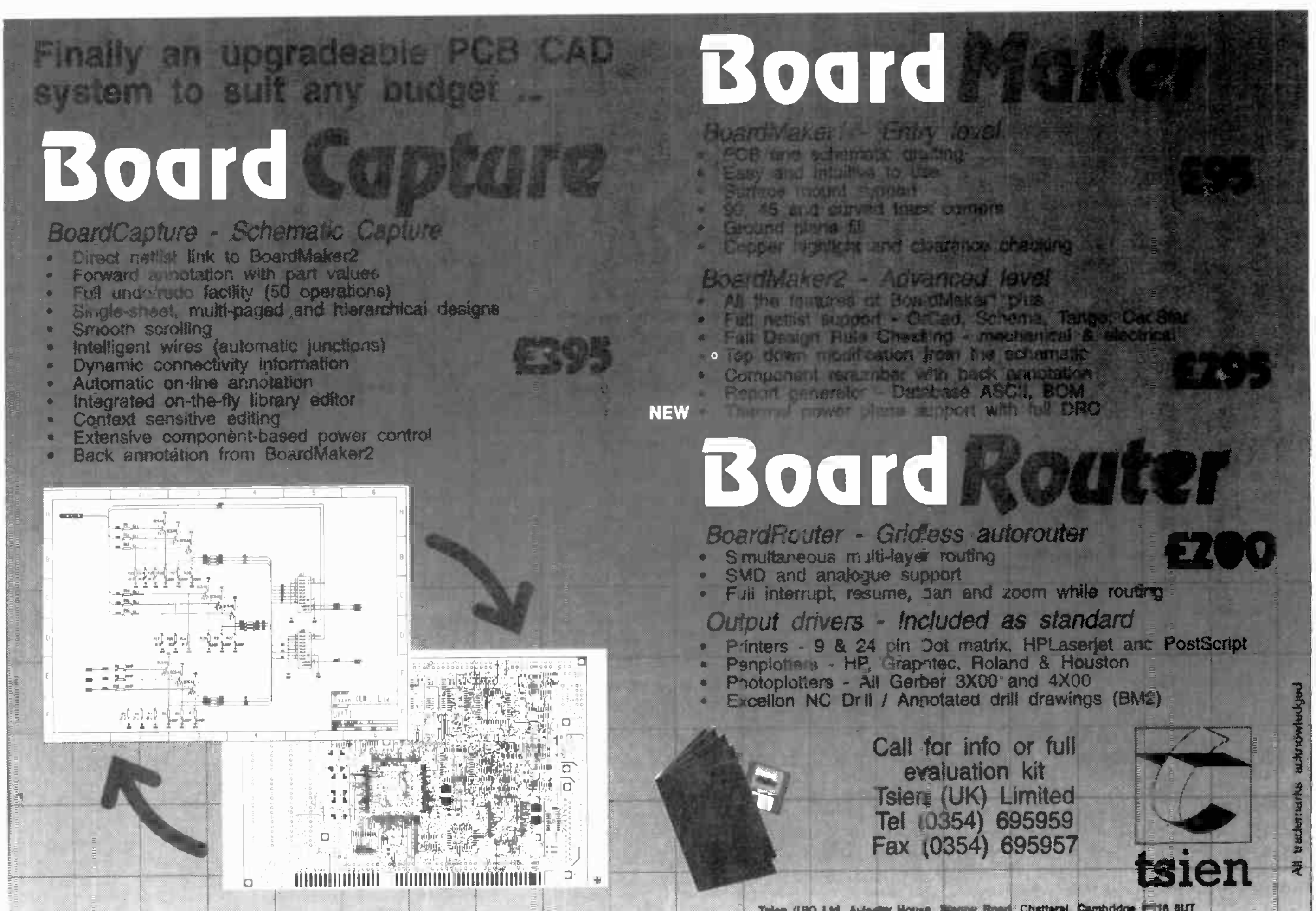
As a very wise military signals officer told me "all radiation is radiation". Too much uv from the sun can trigger malignant melanoma, too much ir from furnaces can lead to glass blowers cataract (unless protective measures are taken), and too much exposure to microwaves (WHO 1993) can trigger thermal and athermal effects, including brain damage of varying degree.

Dr Allen in *Journal of Radiological Protection* 1991 describes reactive near fields, which he says "can affect people and objects", as against radiating near and far fields.

In June the International Bioelectromagnetics Society met in the USA. There were 700 attendees with 486 papers and posters; 250 were from the US, 50 from China, 20 from most European countries, nine from Yugoslavia and seven from the UK. In November Eure held a conference in Bad Neuheim called "Biological effects of magnetic fields", (Verband Deutscher Elektrotechniker). *Radio Electronics* in the US in September 1960 carried a six page article on the effects of rf energy on the body and detailed many experiments carried out on healing, production of aggression, hallucinations and so on.

Lastly, Elizabeth Davies' paper "The healing face of electromagnetic fields" (*EW + WW*, April 1993) calls for research into the signal/tissue response. A timely invitation as the WHO calls for urgent multidisciplinary epidemiological research into the effects of fields on the human body.

Anne C Arnold Silk
Great Missenden, Bucks



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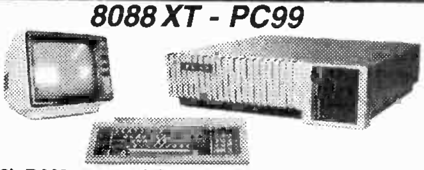

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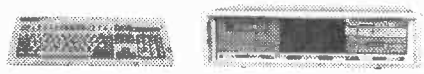

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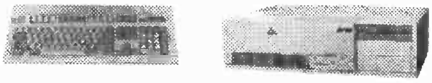

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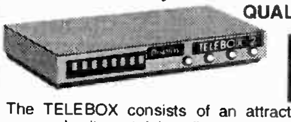

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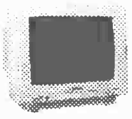

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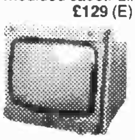

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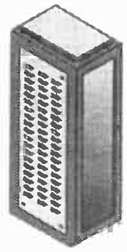

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CIRCLE NO. 115 ON REPLY CARD

Working with programmable logic

3: generic and gate array logic

The first two articles of this series considered methods of designing logic to fit into combinatorial and registered PLDs. In this final part, Geoff Bostock looks at generic logic and field programmable gate arrays

A common element among standard logic PLDs is their fixed architecture. For example, a *PAL16R6* has eight fixed inputs, two bidirectional i/o pins and six registered outputs; a *PLS173* has twelve fixed inputs and ten i/o pins.

In the mid-1980s, Lattice Semiconductor unveiled a device whose architecture itself could be programmed. It was designed to be capable of emulating any of the standard combinatorial or registered pals and, as a further innovation, it was fabricated with cmos technology.

This device, the *GAL16V8* and its 24-pin counterpart the *GAL20V8*, featured a programmable macrocell whose design is shown in **Fig. 1**.

The basis of gals (generic array logic) is the introduction of programmable multiplexers into the output structure. The basic device features four multiplexers: for output enable, register by-pass, feedback and the eighth product term.

The output enable can be driven in four ways. It may be always enabled as in an output pin of a simple *10L8* family pal, or it may be always disabled as in an input pin from the same range. In *PAL16L8*s it is derived from a dedicated product term, while in registered pals there is a common enable from pin 11 (or pin 13 in the 24-pin family).

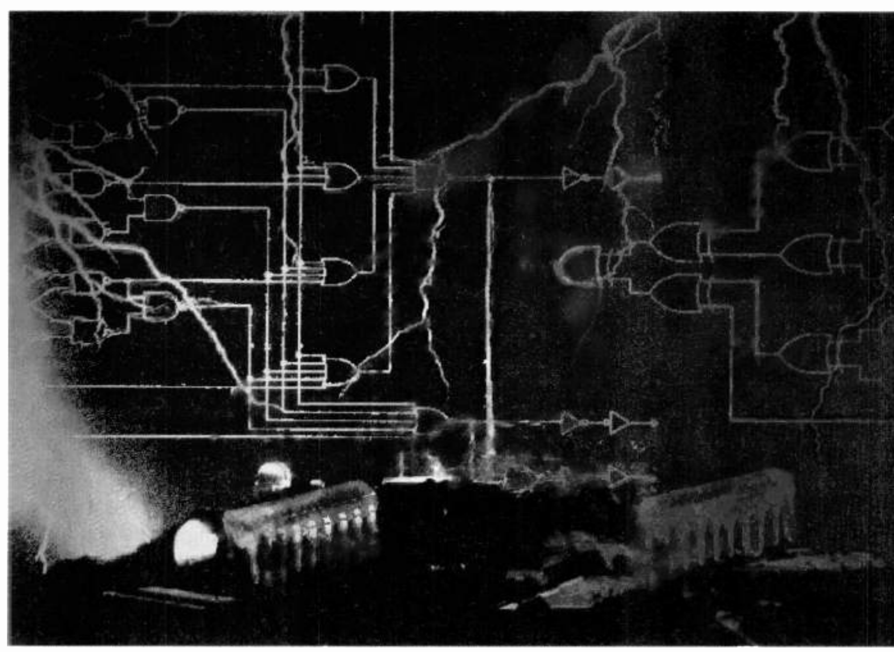
The 'eighth product term' is used as the output enable in the *PAL16L8*, but as a pure logic term in all other pals. Register by-pass allows both combinatorial and registered outputs to be derived from the same output macrocell. The feedback multiplexer has four possible signal sources. It must come from the output flip-flop in registered pals, from the output pin in bidirectional i/os and be disabled in fixed outputs.

The fourth source is an adjacent output pin.

In the *PAL16L8*, pins 12 and 19 are fixed outputs while pins 13 to 18 are i/o; in the *PAL12L6* family (apart from *10L8* and *10H8*) pins 12 and 19 are fixed inputs, and the middle pins may be either fixed input or output according to the device type. Also, pin 1 is the clock input in registered pals but a logic input in combinatorial pals.

The feedback from the top macrocell to the and-array must come from pin 1 in a combinatorial pal but from pin 19 in a *PAL16R6* or *PAL16R4* (where it is an i/o pin).

Likewise, the feedback from the second macrocell



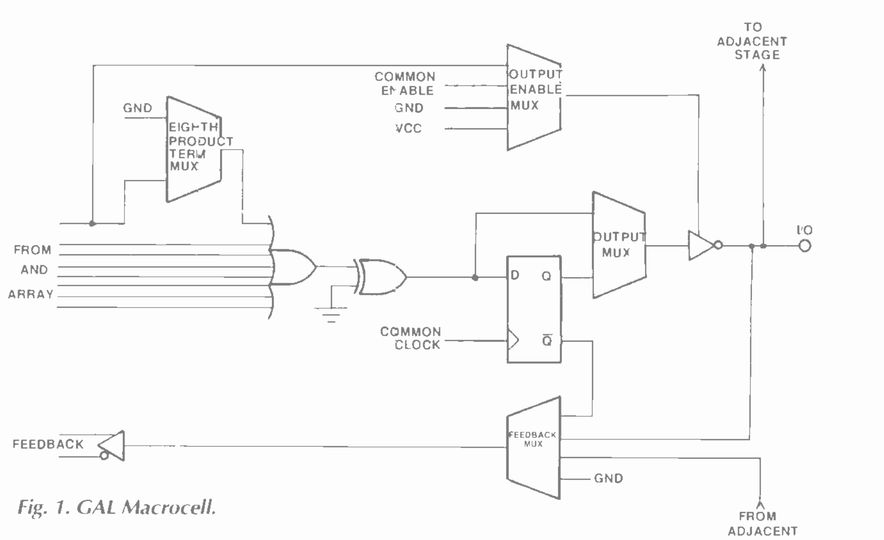


Fig. 1. GAL Macrocell.

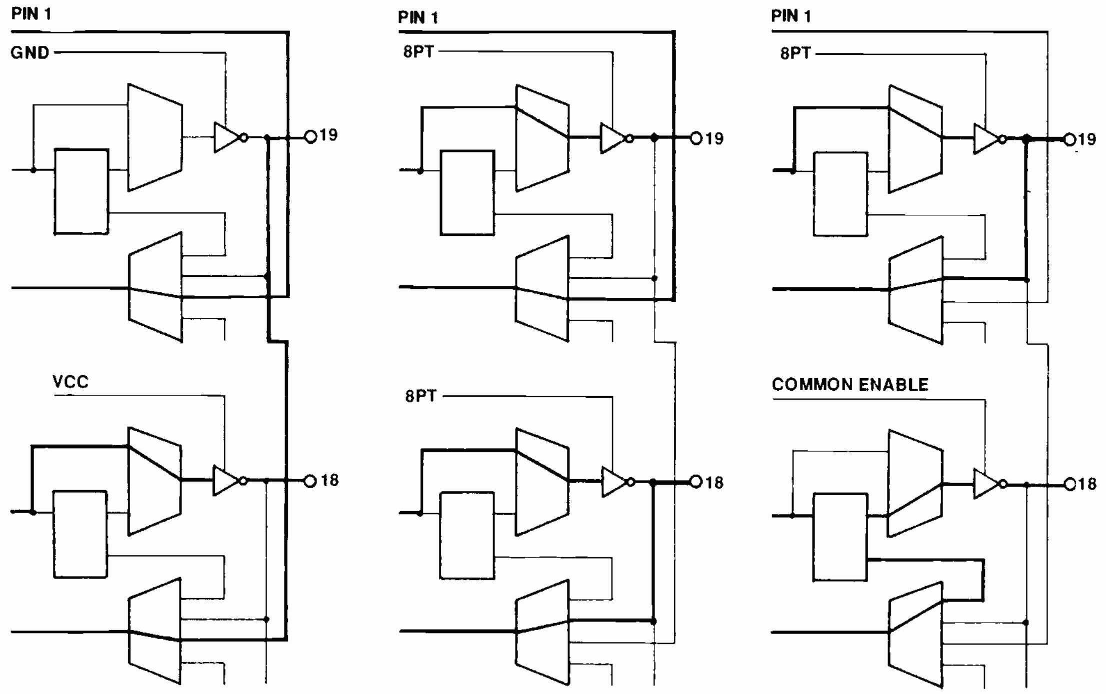


Fig. 2a. GAL16V8 top two macrocells in PAL12L6 configuration.

Fig. 2b. GAL16V8 top two macrocells in PAL16L8 configuration.

Fig. 2c. GAL16V8 top two macrocells in PAL16R6 configuration.

Complex PLDs, of which gals are an early example, rely on multiplexers to provide output function programmability. Gals, in particular, are able to emulate nearly all of the standard pals by routeing the output, feedback and enable signals through the output macrocell.

In the PAL12L6 emulation, the 'adjacent stage' lines route the pin 1 input to the pin 19 feedback multiplexer, and pin 19 to pin 18 feedback; pin 18 becomes a direct output.

The PAL16L8 also routes pin 1 to pin 19 feedback but pin 19 is also a direct output with no feedback. Pin 18 is an output with feedback. Both pins use the output mulitplexer register by-pass path and the 'eighth product term' in the enable multiplexer.

PAL16R6s have a mixture of combinatorial and registered outputs. Pin 19 is combinatorial so the register by-pass output, direct pin feedback and 'eighth product term' enable are selected. The registered pins, such as pin 18, use registered output, feedback from the flip-flop and common enable.

Fortunately, in practice these selections are performed automatically by the software built into most programmers, which set the correct bits for the macrocell multiplexers. Gal design software will also set the select bits if architectures which do not correspond to standard Pals are chosen.

comes from pin 18 in a *PAL16L8* or *PAL16R4*, but pin 19 in any other combinatorial pal in which pin 19 is an input.

The feedback and output multiplexing for the top two macrocells is shown in **Fig. 2** for emulations of pals *12L6*, *16L8* and *16R6*.

The other feature of the gal macrocell is the programmable polarity output. This makes it possible to emulate active-high as well as active-low pals.

Although gals can emulate nearly all standard pals, their architectural possibilities are not limited to these alone. For example, it is possible to use a gal as a pal with three registered and five combinatorial outputs, and to mix these as active-high and active-low, as desired.

There are a few restrictions though; for example, pins 12 and 19 cannot be used as inputs in some modes because of the way in which the multiplexer program cells set the feedback multiplexer.

We have not described the operation of the multiplexer program cells because this is all taken care of by the device programmer or the design software. Device programmers which can program gals have the emulations built into them so that the correct architecture fuses are set when the pal being emulated is selected. Assemblers for gals also set the appropriate bits for the chosen architecture even if this is not a pal emulation.

While Lattice were bringing out the *GAL16V8* and *GAL20V8*, AMD introduced the *PAL22V10*. This device also features output macrocells which can be set as combinatorial i/o or registered outputs, although their design differs slightly from the Lattice circuit. This is because the *22V10* is not aimed at replacing standard pals, although it can emulate the *PAL20L10* family, but it is a more complex device altogether.

The most powerful feature of the *22V10* is the variable number of and-terms in the and-array. As **Fig. 3** shows, the lowest number of and-terms in any output is eight (pins 14 and 23) and increases to sixteen for pins 18 and 19. This goes some way to overcoming the transition term restrictions which can be found when trying to use pals for state machines.

There is also a separate and-term for the output enable in each output pin. Separate and-terms are also provided for synchronous preset and asynchronous reset across the whole device. These features are also helpful in state machines for setting the device to a known state for test or start-up.

Low power logic

The gals were designed as cmos PLDs, and the *PAL22V10* is also available in cmos from several manufacturers. Their data sheets indicate that they still consume tens of milliamps of supply current, about half as much as the equivalent bipolar PLDs which they may replace. While this is still a useful saving, it is not much help to designers

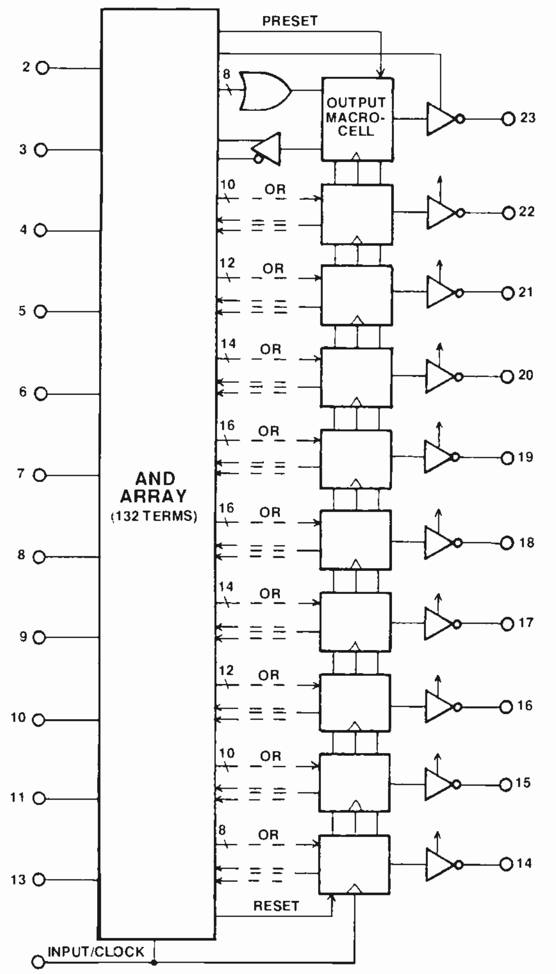


Fig. 3. Block diagram of PAL22V10.

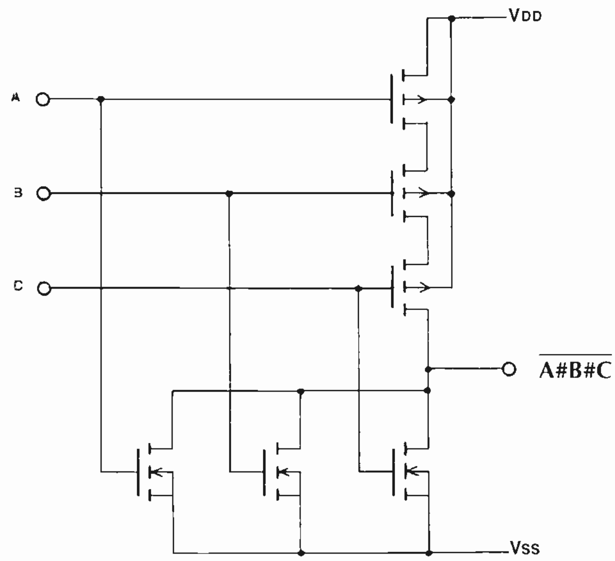


Fig. 4. Circuit diagram of cmos nor-gate.

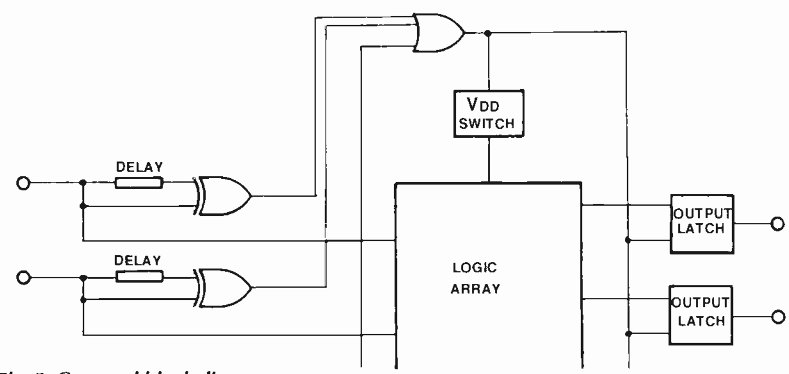


Fig. 5. Cmos pal block diagram

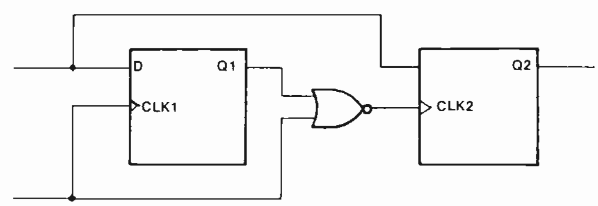


Fig. 6. Simple asynchronous circuit (detects relative position of data rising edge).

of portable or battery-powered equipment.

The reason is to be found in the structure of the internal logic. A standard cmos gate, as in **Fig. 4**, consists of a parallel transistor structure topped by a serial transistor structure, one half being p-channel the other n-channel. In this NOR gate, if all inputs are low the top conducts but none of the bottom n-channel transistors are turned on.

If an input goes high it switches off its p-channel transistor in the top half, thereby preventing conduction, but turns on its n-channel transistor, pulling the output low. The net result is that no direct current flows in the gate, only charging current when the output changes sense. A typical and-term in a PLD has 32 or more inputs, but it is not feasible to construct a cmos gate with 32 transistors in series because of the threshold voltage of the individual transistors in the chain, and the voltage drop across the channel resistance when current is taken from the chain. Instead, each and-term has to be powered by a current source which is always supplying some current to the multiple input gate. The main power saving comes from building the peripheral components, such as input and output buffers and flip-flops from true cmos.

Some PLDs are available with stand-by current of a few microamps. The way in which this achieved is shown in **Fig. 5**. The logic arrays are powered via a switchable current source; while there is no activity at the inputs the current is switched off, so there is virtually no current taken by the device. The activity detector at the inputs switches the current source on for a sufficient time to allow the logic array to react to the new inputs.

The resulting output is latched at the device outputs so that it remains in place when the array current source switches off again. Zero-power versions of many PLDs are now available such as the *GAL16V8Z*, *GAL20V8Z*, *PAL22V10Z* and *PLC18V8Z*, a more universal version of the *GAL16\'8Z*.

Asynchronous registered PLDs

All the registered PLDs described so far have a single clock signal input. This ensures that all the flip-flops in the output register are clocked simultaneously, a necessary condition in a state machine.

There are many instances of simultaneous clocking being unnecessary or not possible. Examples are multiple state machines and random logic.

It is quite conceivable that two or more state machines can be fitted into a single PLD; the only restriction is that the total number of inputs and outputs does not exceed the resources available. It is not necessarily the case that each machine will use the same clock, although they often will. If they do not, the PLDs described so far will not be suitable.

There is no reason why random logic cannot involve flip-flops as well as combinatorial devices. One example of a standard logic function which does not use simultaneous clocking is a ripple counter.

In this case, the output from one flip-flop is the clock input for the next.

Figure 6 illustrates a simple random logic circuit involving flip-flops; it detects whether the rising edge of the data input occurs before or after the falling clock edge. The output could be used to synchronise the data with the clock, by feeding it back to a voltage controlled oscillator.

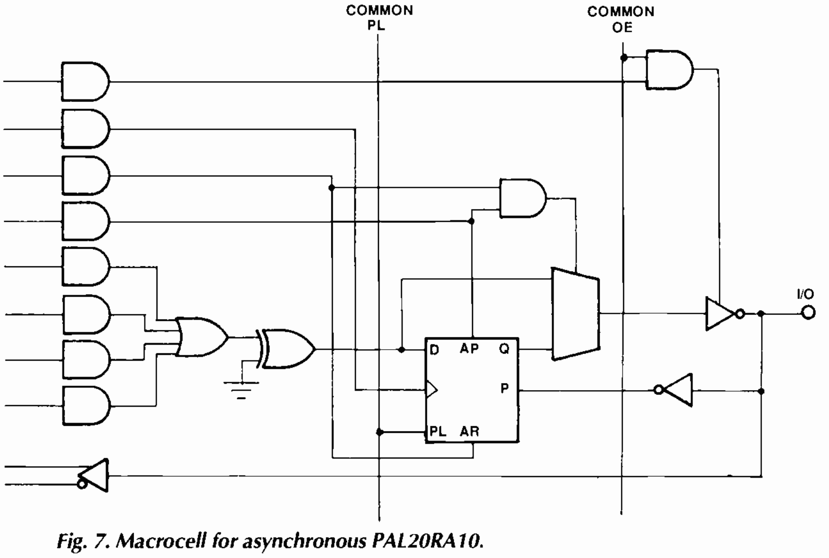


Fig. 7. Macrocell for asynchronous PAL20RA10.

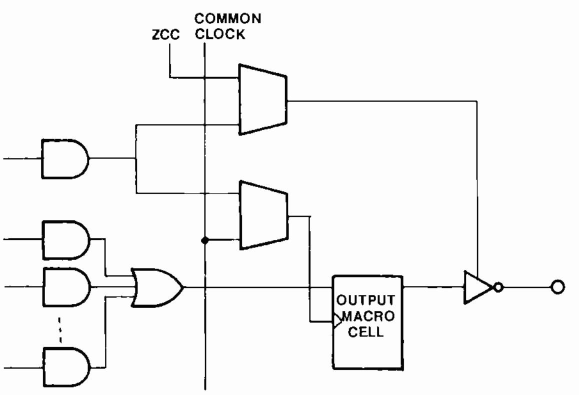


Fig. 8. General asynchronous macrocell.

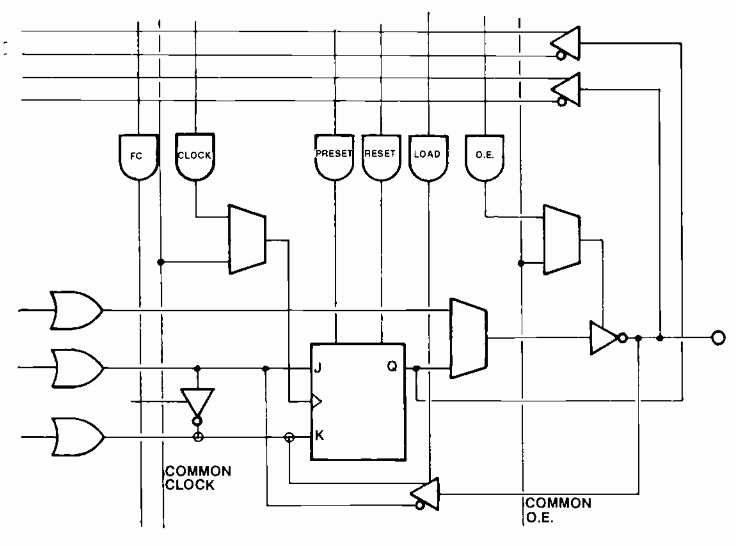


Fig. 9. PLC42VA12 macrocell

The equations for this circuit use the following format:

```
Q1 := D
Q1.CLK = CLK1
Q2 := D
Q2.CLK = !Q1 & !CLK1
```

the `CLK` extension denoting that this is the clock input to the flip-flop whose output is `Q1` or `Q2` respectively.

The *PAL20RA10* is a common asynchronous pal; a macrocell from this pal is shown in **Fig. 7**. Each macrocell has eight and-terms, four of these are logic terms, the other four drive the output enable, clock, set and reset. The clock input can be any logical combination of the input and output signals, provided that it can be described in a single and-term. In the above example, the clock input is drawn as `!(Q1 + CLK1)` but can be transformed to `!Q1 * !CLK1` to fit into one and-term.

The set and reset behave as usual for a flip-flop, except for the usually forbidden combination of set and reset both high. This condition in the *PAL20RA10* bypasses the flip-flop and converts the output into a combinatorial i/o.

Many other PLDs are now made with an asynchronous option. A common way of implementing this is to use a double multiplexer, as in **Fig. 8**. One multiplexer feeds the clock, the other drives the output enable.

The clock multiplexer has inputs from an and-term and the common clock, the output enable multiplexer is driven by the same and-term and either a common output enable or an 'always enabled' input. The multiplexer select bit is arranged so that the and-term is available to either clock or output enable.

Buried register PLDs

Although some FPLSs have buried registers, these are designed into the part and the designer has no choice in the proportion of flip-flops which are internal, and those which are outputs.

Another failing of some PLDs is the waste of resources when an output flip-flop is by-passed to provide a combinatorial i/o. Some of the more advanced PLDs overcome both of these shortcomings by allowing by-passed flip-flops to be used as internal components, but with no direct access to the outside world.

One of the most versatile programmable logic devices in the 20 to 28 pin range, is the *PLC42VA12*. This is an FPLS which can emulate the *PLS179, PAL22V10 or PAL20RA10*. **Figure 9** shows the output stage of the device. There are separate and-terms for the ten clock inputs and ten output enable signals, as well as the set and reset lines and direct load facility, which is found on the *PLS179*.

Each output has three or-terms and two feedback lines to the and-array. If the flip-flop is bypassed, so that the output becomes a combinatorial i/o pin, the feedback from the flip-flop is still available.

A by-passed flip-flop becomes a buried flip-flop, so this resource need not be wasted.

When designing for the *PLC42VA12* with *Snap*, which is the Philips PLD software, all nodes in the design can be defined irrespective of whether they are internal or external. All flip-flop outputs are treated equally, whether they are by-passed or fed to output pins.

It is only at the time when nodes are assigned to pins that the software will allocate logical nodes to physical elements within the PLD.

Many PLD compilers require the designer to define buried nodes at the start of the design.

The circuit of **Fig. 10a** can be used as an indication of the complexity of design which may be incorporated into the *PLC42VA12*. Eight internal flip-flops are used to form a two digit decade counter whose outputs feed a quadruple two-bit multiplexer. The multiplexer output drives a seven segment decoder which is output from the device. Selection of the multiplexer is by a two bit state machine which also provides digit select outputs. Different clocks are used for the counter and the digit select. This circuit uses only three inputs and nine outputs leaving three i/os and seven inputs unused. As we shall see, the counters need nine terms each, the decoder/multiplexer uses 32 terms while the digit select takes just two terms. There are, therefore, twelve and-terms spare for using with the leftover inputs and i/o.

The design may be split into four sections.

Let us first examine the decade counters; their state diagram is shown in Fig. **10b**. The most efficient way of building counters is, usually, with toggle flip-flops, so we will follow this approach. To find the minimum solution we can draw out the Karnaugh maps for each counter bit; this is done in Fig. **10c**.

A toggle must be entered on every occasion when a bit changes from 1 to 0 or from 0 to 1, remembering that above 9 (1001b) the counter must jump direct to 0 (0000b). The numbers 10 to 15 have been included in case the counter should find itself in one of these states, perhaps because of some malfunction. If they were not included, the counter could get stuck.

From the Karnaugh maps we can write the following equations:

```
B3.T = CE & (B3 & B2
            # B3 & !B1 & B0
            # B2 & B1 & B0
            # B3 & B1);
B2.T = CE & (B3 & B2
            # !B3 & B1 & B0);
B1.T = CE & (!B3 & B0
            # B3 & B1);
B0.T = CE & (!B3
            # B2 & B0
            # B1 & B0);
```

although there are eleven terms, two of them are duplicated, `B3 & B2` and `B3 & B1`, so a single and-term is used for each making nine terms needed in all. The MSB counter, `A3` to `A0`, will use the same equations except that it only toggles when the LSB is nine; the term `B3 & !B2 & !B1 & B0` must, therefore, be and-ed with every term giving:

```
A3.T = CE & B3 & !B2 & !B1 & B0 & (A3 & B2
                          #... etc.
```

We must also define the clock to be used; this is done as follows:

```
B3.CLK = CLK
B2.CLK = CLK
etc.
```

These definitions do not use up any and-terms.

The third section we can define is the multiplexer/decoder.

The seven segment decoder is a straightforward combinatorial design.

Segment 'a', for example, is used in every number except '1' and '4'; the basic equation for segment 'a' is therefore:

```
!SEGa = !B3 & !B2 & !B1 & B0
      # !B3 & B2 & !B1 & !B0 for the LSB
```

In order to select the MSB or LSB this basic function must be gated with the appropriate select function. We can define these as `D1 & !D0` for the MSB and `!D1 & D0` for the LSB. The full equation becomes:

```
!SEGa = !D1 & D0 & !B3 & !B2 & !B1 & B0
      # !D1 & D0 & !B3 & B2 & !B1 & !B0
      # D1 & !D0 & !A3 & !A2 & !A1 & A0
      # D1 & !D0 & !A3 & A2 & !A1 & !A0
```

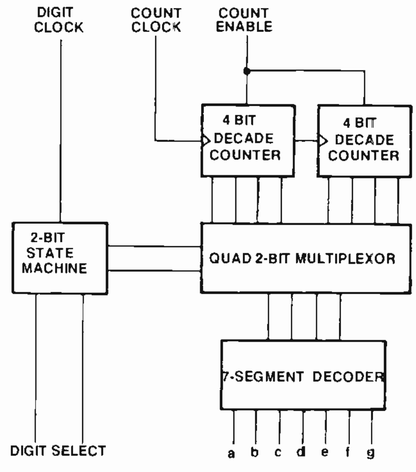


Fig. 10a. block diagram of multi state machine example.

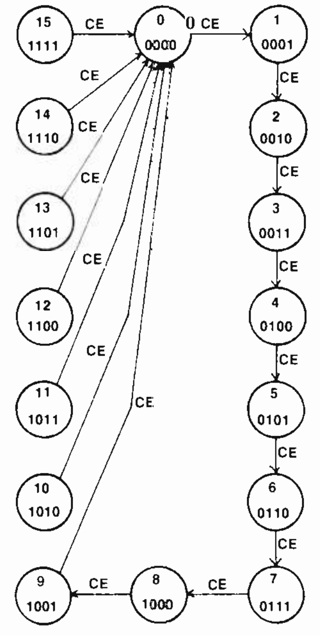


Fig. 10b. State diagram for decade counter

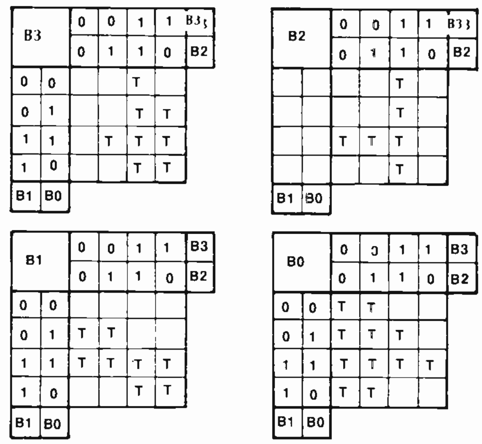


Fig. 10c. State diagram for digit select.

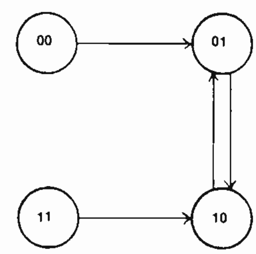


Fig. 10d. Karnaugh maps for decade counter

While asynchronous pals may be used for random logic which also includes flip-flops, it is also useful to be able to use them for systems where more than one clock is used. Fig. 10 illustrates a design which contains two state machines driven by different clocks.
One half of the circuit is a two stage decade counter whose design proceeds via a state diagram and Karnaugh Maps. A single seven segment decoder allows the count of each digit to be displayed in the standard format.
The second state machine merely toggles between two states to drive the multiplexer and select each digit in turn for the decoder. Outputs from this machine provide digit select signals for driving a multiplexed display.
This design fits PLC42VA12 or GAL6001. Both have selectable clock inputs for all flip-flops.

Similar equations may be derived for the other segments; in all, 32 terms are needed for the whole decode.

The state diagram for the final section is shown in Fig. **10d**. The basic function is a toggle between `D1 & !D0` and `!D1 & D0`, but we must also include the illegal states `D1 & D0` and `!D1 & !D0`. The transitions are unconditional so we can easily derive the equations as:

```
D1.J = D0D1.K = !D0
D0.J = !D0
D0.K = D0
D1.CLK = DCLK
D0.CLK = DCLK
```

These use just two and-terms as the two `D0` and the two

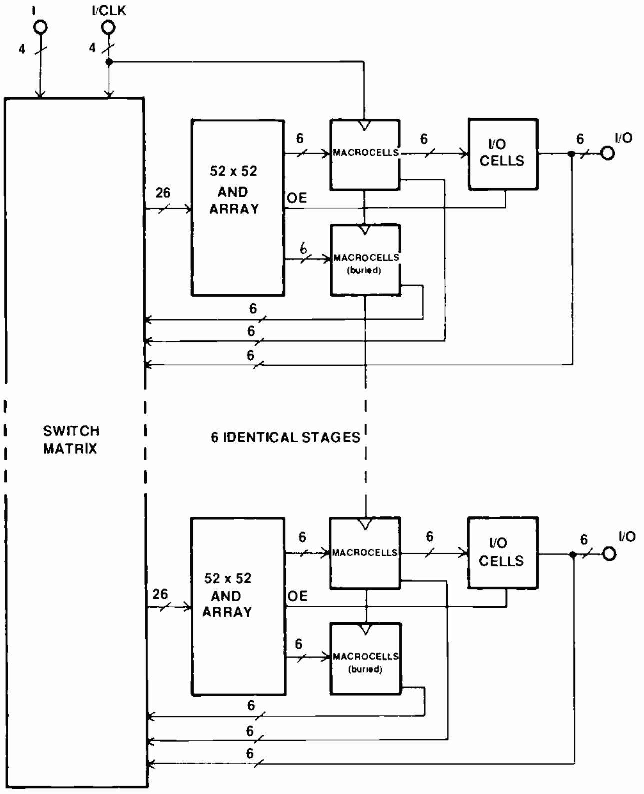


Fig. 11. Block diagram of MACH220.

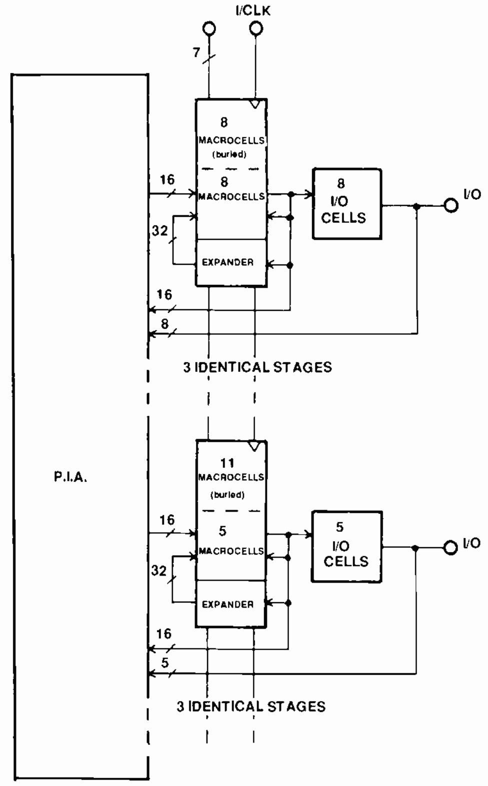


Fig. 12. Block diagram of EPM5128 (MAX).

!DO terms each use just one and-term which is used twice in the OR-array.

While this design has been aimed at the *PLC42VA12*, there are other PLDs with similar capabilities. Among these is the GAL6001; this device has input flip-flops but no direct load facility. It uses D-type flip-flops with a clock enable input allowing J-K flip-flop emulation.

It also has an eight bit wide dedicated buried register making it more powerful in some applications than the *PLC42VA12*.

Other complex PLDs exhibiting buried registers include the *PALCE29M16* and *PALCE29MA16* from AMD, *CY7C330* and *CY7C331* from Cypress, *5AC312* from Intel, *ATV750* from Atmel and *XL78C800* from Exel. All these use pal architecture (i.e. fixed or-array) except the *XL7C800*, which has a nor-nor structure in a single array.

This is equivalent to an and-or structure because:

```
!(!(A#B) # !(C#D)) = (A#B) & (C#D)
```

by de Morgan's Laws.

LSI PLDs

So far we have described PLDs with up to 28 pins but, in the last few years, technology has moved on to the point where PLDs are being made with over one hundred pins and the capability to replace a dozen or more *16V8s*.

LSI has followed three basic paths, the simplest of which is a multi-pal approach. The main families are the AMD *Mach* and Altera *Max*; the chief difference between them is the way in which the pal blocks are interconnected.

Large pal type devices engender problems with propagation delay introduced by the and-array. Each programmable cell adds capacitance to the array and, for example, in an 84 pin device, there could be about 160 inputs to the and-array if all the inputs and i/o were directly connected to the array. This compares with just 32 array inputs in a *GAL16V8* making the structure significantly slower than a basic gal.

In the *Mach* family, the device inputs are fed to a switch array which allocates them to the pal blocks, with a maximum of 22 or 26 into each block. The actual size of each pal block varies according the actual device, but they are of the form 22V12, 26V16 etc.

Each fixed-or term is fed by only four and-terms but a logic allocator combines up to four or-terms into each output. Thus, the and-terms associated with i/o used as inputs need not be wasted. Half the devices in the basic *Mach* family have macrocells which are all routed to i/o pins, while the rest have half the macrocells buried.

Figure 11 is the block diagram of the *Mach220*, a middle size device with 68 pins and buried registers.

Max devices are based on a logic array block (lab) which has sixteen i/o macrocells, some buried, and a logic expander. The logic expander consists of 32 nand-terms which are fed back into the and-array and may be used as additional logic for any of the macrocells in the lab.

Each macrocell has three and-terms, plus an exclusive-or for J-K emulation, but, unlike the *machs*, none of the i/o macrocells can be buried if the pin is used as an input. The signal routing is handled by the programmable interconnect array (pia), which has all the i/o and macrocell feedbacks available.

As with *Mach*s, each lab is fed those signals which it requires; unlike *Mach*s, all direct inputs and local lab feedbacks are always available to each lab. The block diagram of a 68 pin *Max*, the *EPM5128*, is shown in **Fig. 12**. Both families have similar logic capability with the slight edge going to the *Max* family. This advantage is bought by having a higher connectivity into each lab.

The result is a slightly slower device, and one with variable delays.

Because all *Mach* signals pass through the switch array they all have virtually the same delay time; in the *Max*

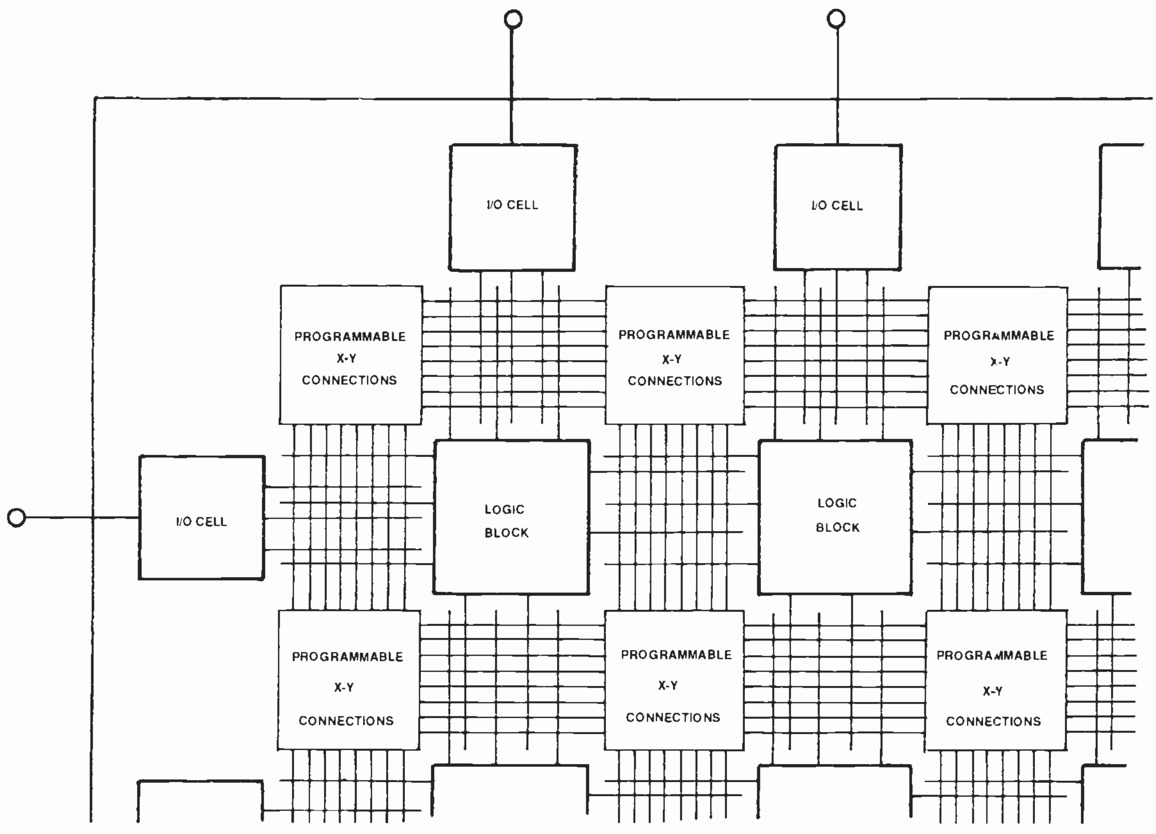


Fig. 13a. Floor plan of a typical FPGA.

The traditional way to mop up large quantities of logic elements has been with masked asics, particularly gate arrays. PLD design files can even be used as data input for many asic design packages. FPGAs are the PLD answer to masked asics. The floor plan of a typical FPGA is shown in Fig. 13a; the similarity to a gate array is self evident. The same four principal components exist in both structures.

Logic signals enter and leave the FPGA via i/o cells, which offer the usual features, such as tri-state, cmos/TTL interfacing, edge speed selection, and so on.

The logic functions are defined in internal logic blocks. These are often more complex than masked gate array logic cells. Two examples are shown in Figures 13b and 13c. The Xilinx cell is the more complex, and includes configuration bits to define the logic paths through the macrocell. The Actel macrocell is smaller and, apart from the flip-flop bypass, has a fixed architecture.

Connections between macrocells are made by horizontal and vertical routing lines in channels between the macrocells. Fuses or, in the case of Xilinx, ram cells at crossing points define the interconnections, and the logic paths in and out of the macrocells and i/o cells.

Design path is very similar to a masked asic, with logic capture, simulation, place and route, and timing simulation as the main steps. The advantage of FPGAs is that turn-round is very much quicker, and the minimum quantity is very much lower.

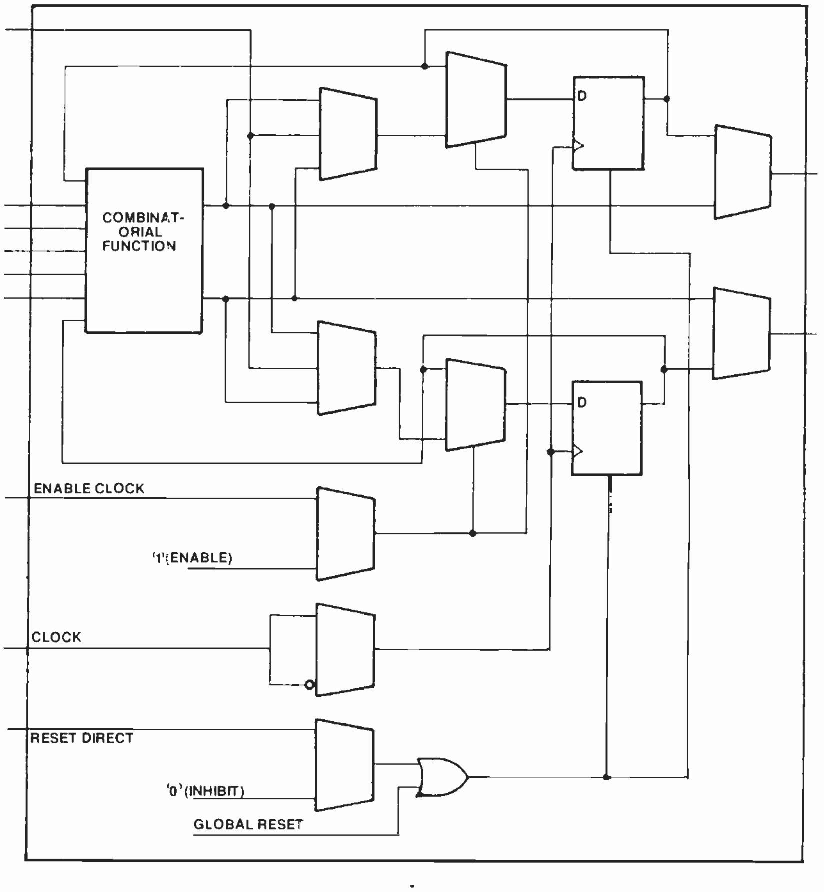


Fig. 13b. Xilinx macrocell.

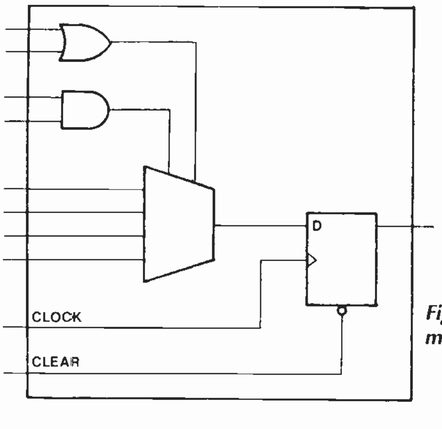


Fig. 13c. Actel macrocell.

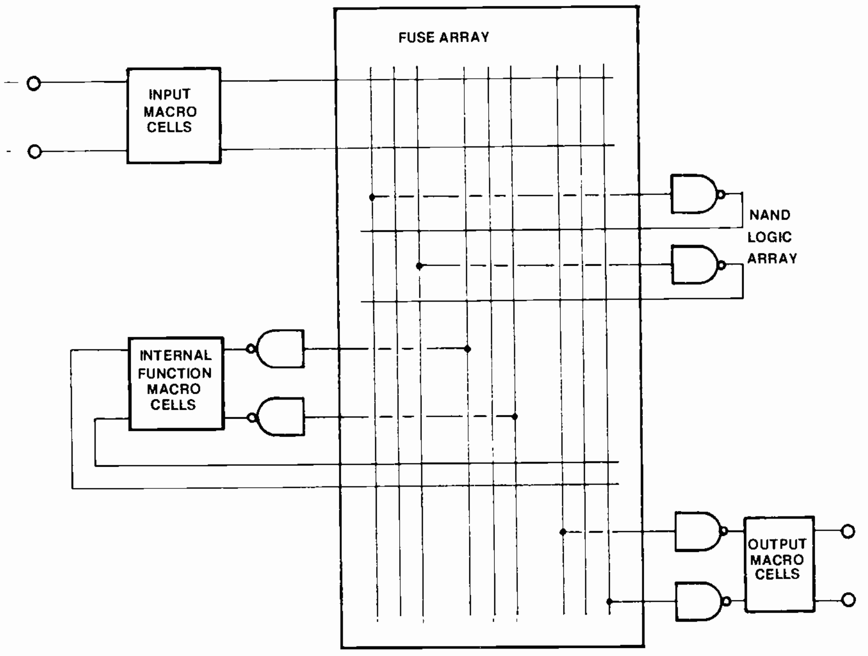


Fig. 14. PML structure.

family, signals can pass direct to the *Lab*, via the PIA or be further delayed in the logic expander. While these delays are predictable, they can lead to skews or races both internally and externally.

Similar architectures are also exhibited by the *ATV2500* and *ATV5000* from Atmel, and by the *Plus* family from Plus Logic.

AMD and Altera have also introduced advanced versions of their basic families.

The second type of LSI structure uses a more distributed architecture, more like masked gate arrays. In fact they are commonly known as field programmable gate arrays (FPGAs). This term is sometimes applied to all LSI PLDs but it is quite easy to distinguish between them.

Very large pal-type structures are just that; their primary logic capability is achieved by wide and-gates which are or-ed together in small groups, each or-gate being committed to one particular output pin. Much of the potential logic resource is wasted because only a few inputs are connected to each and-gate, and many of the and-gates in each or-grouping are often not used.

Figure 13a shows the structure of a typical FPGA. Each logic block has only ten or a dozen i/o lines; these are fed via programmable connections to the routeing channels which surround the logic blocks, allowing them to be joined to other logic blocks and the device i/o.

The logic blocks themselves contain relatively simple components which can be configured to a number of standard logic functions.

The internal structure of two types of FPGA are shown in figures **13b** and **13c**. These two devices, introduced by Xilinx and Actel respectively, exhibit some differences. The Xilinx logic block is more powerful than Actel's so the smallest arrays, both available in 68PLCC packages, contain 64 and 295 blocks respectively, although both claim to be equivalent to 1200 gates.

The most profound difference between the two is the way in which they are programmed. Xilinx arrays use ram cells to define both interconnections and logic block configuration. The program data is usually stored in an adjacent eprom which is automatically downloaded into the array on power up, because the ram cells lose their data when switched off. This additional board space can be a disadvantage, but product development can be much simplified, and it might be possible to use the same circuit board for more than one function.

The Actel FPGAs do not need their cells configuring, because they are a much simpler design. Array connections are made with an 'anti-fuse'; this consists of a thin dielectric layer sandwiched between polysilicon and the silicon surface. The programming pulse ruptures the dielectric and alloys the two silicon layers together. The connections in this case are therefore hard wired and the device cannot be reprogrammed.

Designing FPGAs involves more steps than pal structure devices.

The basic logic design is the same but, once the desired function is defined, it must be broken into modules which fit the architecture of the FPGA logic blocks. The modules must be allocated to blocks and then connections routed between them. These are the same place and route steps which are needed to define masked gate arrays.

Once the design is placed in the array, timing simulation is necessary for the delay of internal signals will be affected by the lengths of tracks they use. From this point of view it may be more difficult to achieve instant success than with a pal structure, but the final result should give more efficient use of silicon, and therefore a cheaper solution.

The third class of LSI is based on an FPLS structure; two examples are the MAPL (multiple array programmable logic) from National Semiconductor and PML (programmable macro logic) from Philips.

MAPL is a large FPLS with additional gal outputs on larger devices.

The chief innovation is the use of page mode power-up, so that only a small portion of the array is consuming power at any one time.

As well as a 'next state' output from each transition equation, there is a 'next page' which powers up the page containing possible jumps from the next state. This allows the array to achieve high speed without an excessive power consumption.

PML, in **Fig. 14**, uses a single foldback array of nand-gates for logic implementation. This uses the equivalence:

```
!(!(A * B) * !(C * D))
= (A * B) + (C * D)
```

which can be deduced from de Morgan's Laws.

In PML, the logic core is surrounded by macro logic elements with inputs and outputs to the NAND array. Device inputs and outputs are also connected to the logic core so that the macro elements can be used either internally or as output functions.

The *PML2552*, for example, has 29 dedicated inputs, 16 of which have by-passable flip-flops; there are 24 bi-directional i/o lines including 16 by-passable registered outputs.

Internally there are 20 J-K flip-flops with a separate clock array, and a logic core of 96 nand-gates.

This structure is freer than pal-type LSI, although this particular device has not quite the power of 68PLCC *Mach* or *Max* parts in terms of gate and flip-flop count. Neither does it match FPGAs for potential logic complexity. There is no reason why, with denser internal logic, this structure

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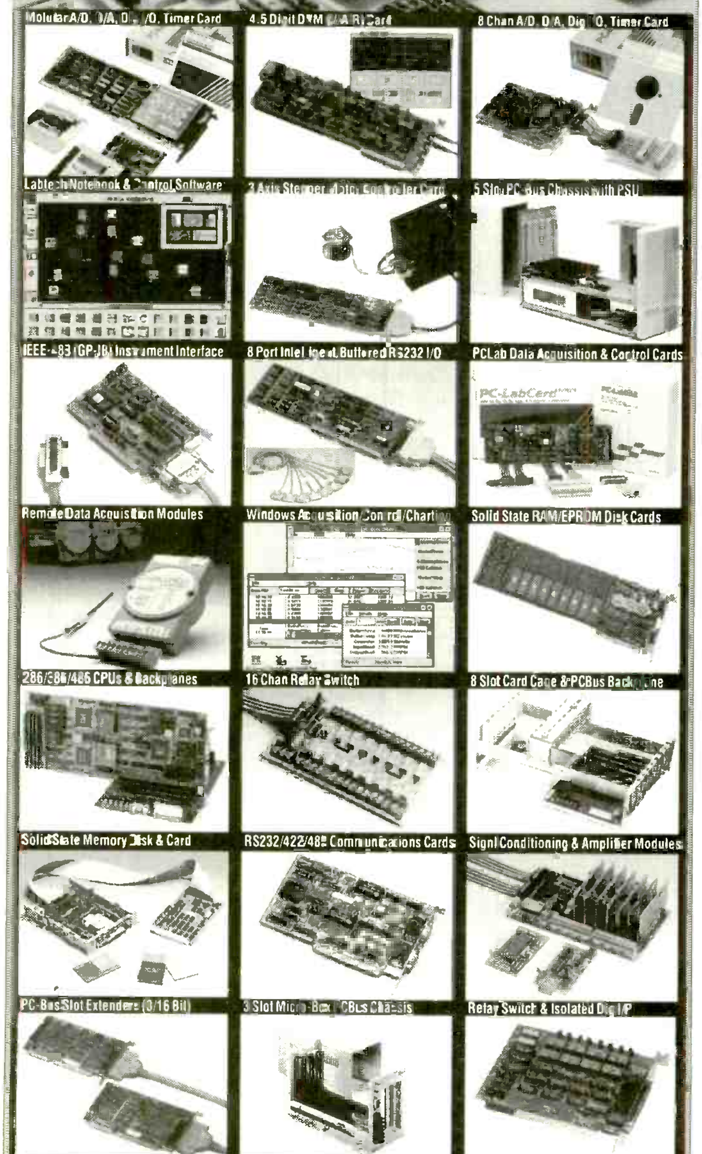

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CIRCLE NO. 118 ON REPLY CARD

Switched capacitor filter combines notch and low-pass functions

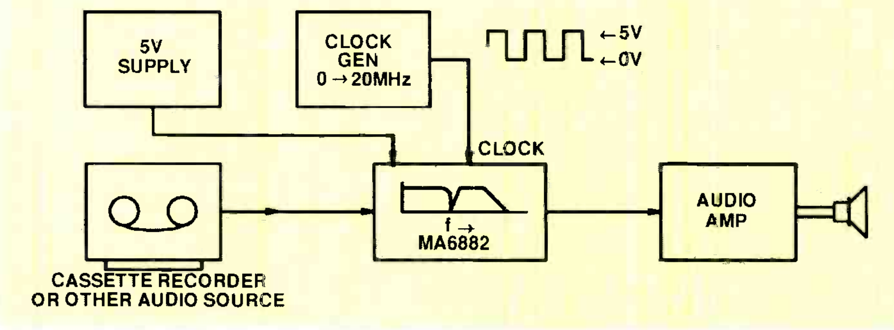
It is increasingly common to reserve a very narrow band of the audio spectrum for data, control or coding information. Provided that very sharp band stop and pass filtering is used for insertion and recovery, adding the information sacrifices very little in audio quality.

GEC Plessey has produced a switched-capacitor device in cmos asic technology called the *MA6882*. As *Application Note 137* describes, the device combines both sharp notch and low-pass filter functions.

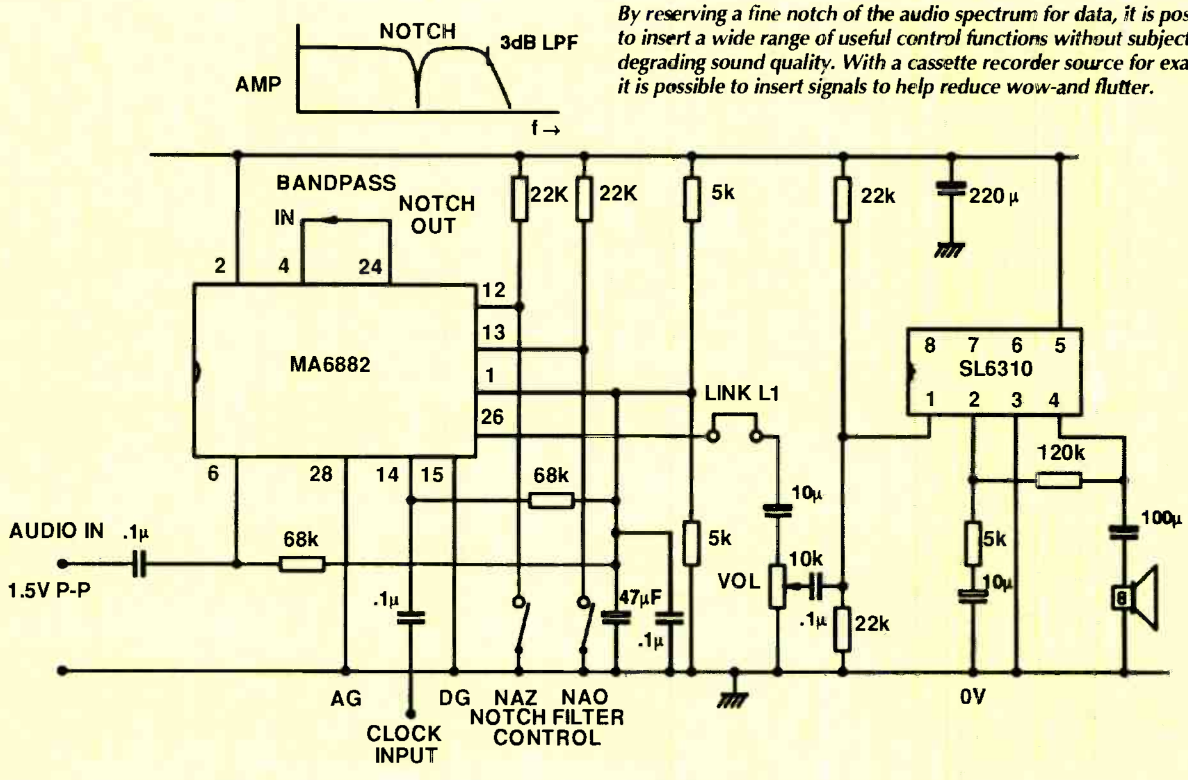
For the low-pass filter section, the –3dB point is fixed at the clock frequency divided by 1470. Clocking at 5MHz for example will cause cut-off at 3.4kHz. The notch filter however can be placed at four jumper-selectable points, at divisions of the clock frequency of 1870, 2493, 3740 or 7480.

Further suggested applications for the notch information are wow and flutter correction, AGC, noise reduction and sound effects.

GEC Plessey Semiconductors, Cheney Manor, Swindon, Wiltshire SN2 2QW. Tel. 0793 518000.



Combined switched-capacitor notch and low-pass filtering for audio frequencies. For the low-pass filter, the –3dB is entirely governed by the clock but the notch filter can be placed in any one of four frequency slots, depending on the NA switches.



By reserving a fine notch of the audio spectrum for data, it is possible to insert a wide range of useful control functions without subjectively degrading sound quality. With a cassette recorder source for example, it is possible to insert signals to help reduce wow-and flutter.

Low-noise microphone preamplifier exhibits less than 1nV/√Hz noise

Instrumentation amplifier configurations are useful as microphone preamplifiers. Besides allowing gain to be set via one resistor, they remove the need for a transformer while keeping common-mode rejection high.

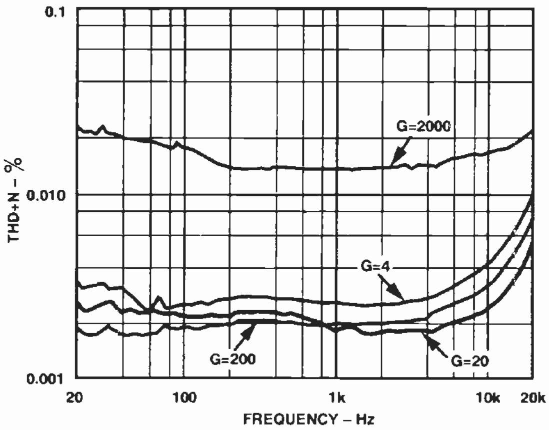
This low-noise circuit from Analog Devices note *AN242* features a phantom power option with input protection and is gain adjustable via one resistor, R_G.

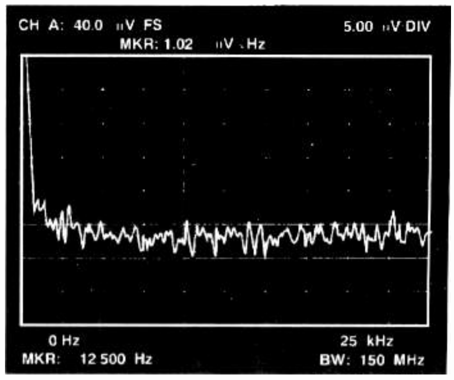
Input-referred noise is less than 1nV/√Hz over a gain range of 2 to 2000 while common-mode rejection capability is 90dB or more. For gains to 200, the THD plus noise figure is well below 0.01% at all frequencies to 20kHz.

Phantom power involves inserting a DC voltage, typically between 10 and 48V, on the preamplifier input. This voltage is needed to power capacitive microphones.

In its steady state the phantom voltage presents no problems. At power up or down, or when the microphone is plugged or unplugged however, protection is needed to avoid damaging the preamplifier inputs. Given a phantom voltage of 48V, the input capacitors can discharge several amps into the amplifier inputs.

In this circuit, protection is provided by two zener diode pairs and resistors for limiting peak current. The *1N752* diodes are 400mW types, equivalent to a European 5.6V *BZX79*, and limit peak transients to 10V or below.





CONDITIONS:
SSM-2017 GAIN = –500; OP-275 GAIN = –2
TOTAL GAIN = 1000
V_S = ±20V; R_L/ C_L = 1MΩ || <60pF

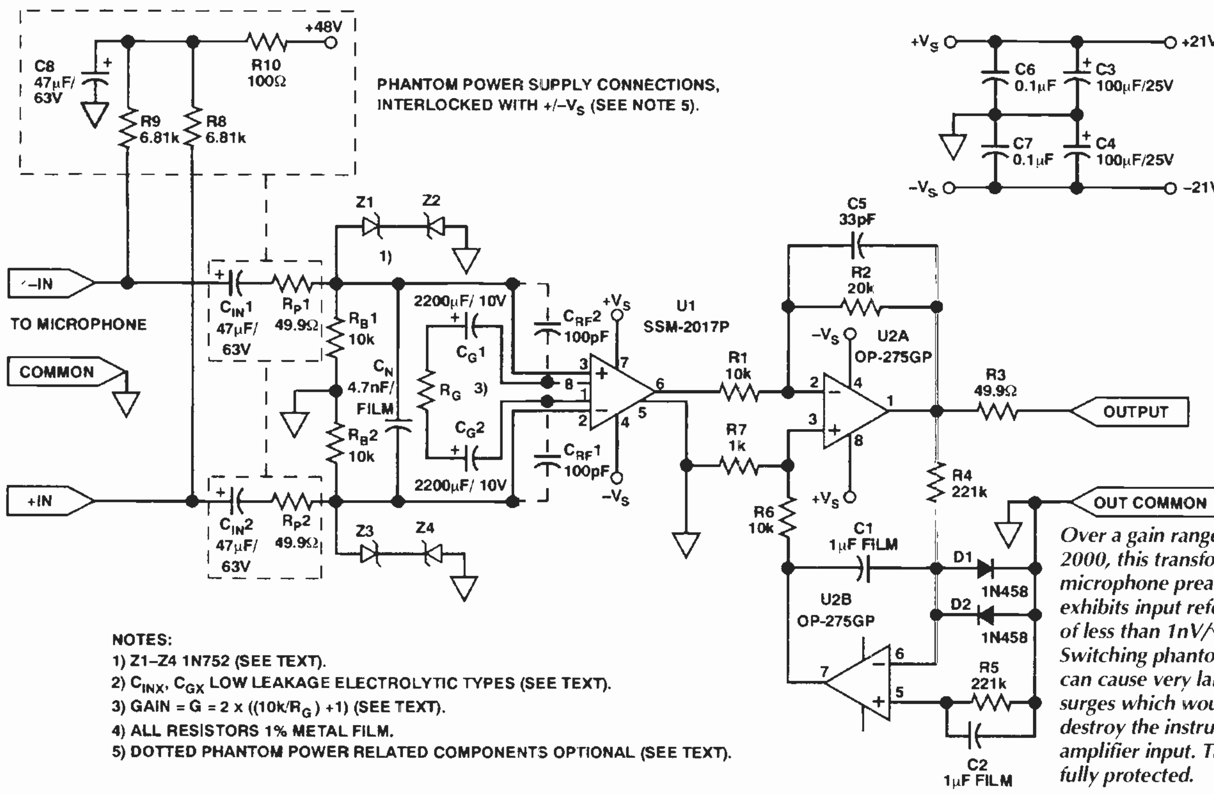
Noise display and distortion curves for the high-performance balanced microphone preamplifier. Although vertical graduations on the noise display are 1μV/√Hz, gain is 1000 so input referred noise is within 1nV/√Hz.

Adding protection circuitry increases noise slightly due to the input series resistances. This is countered to an extent however since phantom-powered microphones tend to have a higher than usual output.

Power supply circuitry should not allow the phantom power to be switched independently of the bipolar supply to the op-amp. Capacitor C_N is added to filter RFI above 130kHz while R_2 and C_5 provide roll-off above 240kHz in the second stage.

Further details in the note cover the op-amp, circuit design, performance and the importance of selecting the right components. There is also a discussion of how to further reduce the circuit's RF sensitivity.

Analog Devices, Station Avenue, Walton-on-Thames, Surrey KT12 1PF. Telephone 0932 232222.



Over a gain range of 2 to 2000, this transformerless microphone preamplifier exhibits input referred noise of less than 1nV/√Hz. Switching phantom power can cause very large current surges which would normally destroy the instrumentation amplifier input. This circuit is fully protected.

Bidirectional drive for coaxial cable

For voice-band signals, designing a single-cable bidirectional link is quite simple. Similar links for megahertz bandwidth however involve high-speed amplifiers and well-controlled impedance matching.

Programmable wideband transconductance amplifiers can provide such a wideband bidirectional coaxial interface, as illustrated in this diagram from Maxim's twelfth *Engineering Journal*.

Functionally, the circuit is similar to ones used in telephone interfaces and offers the same benefit – it saves the cost of a return cable. Components shown are for a 50Ω system but with appropriate modifications, the circuit is equally suited to 75Ω video and other impedance levels.

Identical circuits terminate each end of the cable. As well as performing signal reception, each return amplifier (the top two) also cancels all signals originating at its end of the link.

On either side, input signals drive both the inverting input of their receiver and the non-inverting input of their transmitter. In this way, the signal passes through the transmitter unchanged but is inverted in the receiver, which results in its cancellation.

To achieve the cancellation, the amplifier transconductances must be set for unity gain throughout. Several factors can degrade the cancellation. First, phase shift in the line driver prevents the return amplifier from subtracting identical signals.

Secondly, any transconductance mismatch in the amplifiers causes the signals to have different amplitudes, which again disturbs the output nulling. Finally, any impedance mismatch along the cable causes reflections. The non-adaptive circuits shown cannot distinguish between such echoes and the desired incoming signal.

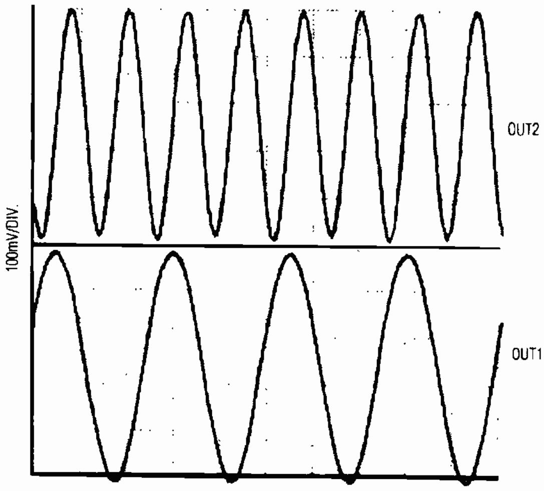
Signal cancellation depends on the tolerances of termination resistors $R_{1,5,6,10}$. Their degree of mismatch with the cable impedance is also important. Similarly, the transconductance for each amplifier is affected by resistors $R_{2,3,8,9}$. Transconductance, g_m, is $8/R$. The '8' is a property of the IC and guaranteed to be within ±2.5%.

Outputs test traces are shown. Those at the top show both outputs when one end of the link is driven with a 1MHz signal, the other with 2MHz. Both generators are 50Ω impedance.

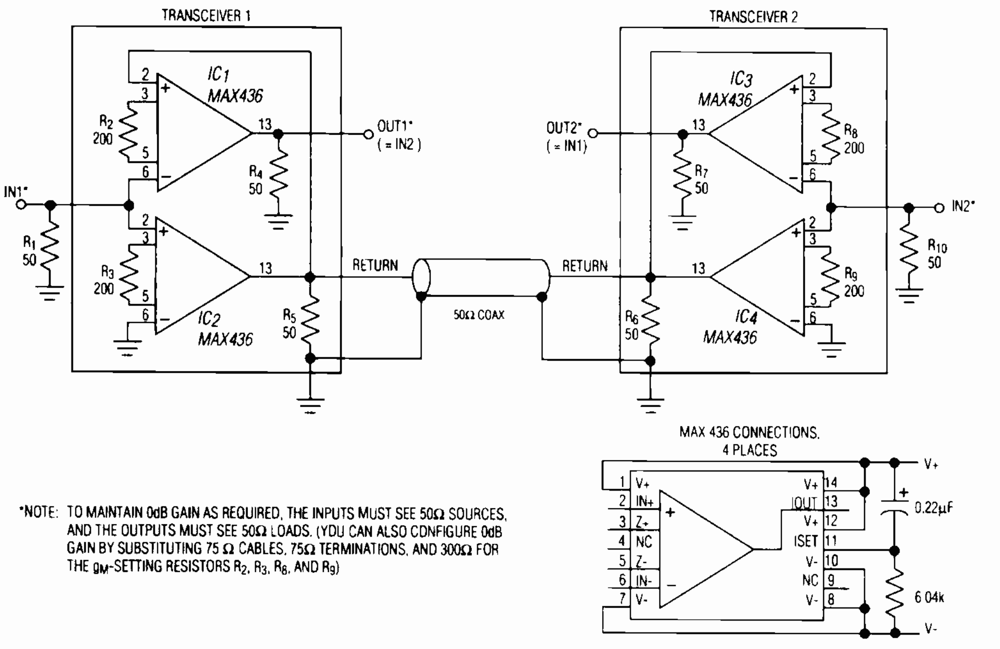
On the lower pair of traces, one input is driven while the other is terminated with 50Ω. On the receive side, the receiver outputs the full signal as required, top trace. The receiver on the transmit side however should show none of the transmitted signal.

The small residual signal shown in the lowermost trace results from 30dB cancellation in the low megahertz range, which will be acceptable for most applications. To achieve it, resistors need to be matched to 1%.

Maxim, *21C Horseshoe Park, Pangbourne, Reading RG8 7JW*. Tel. 0734 845255.

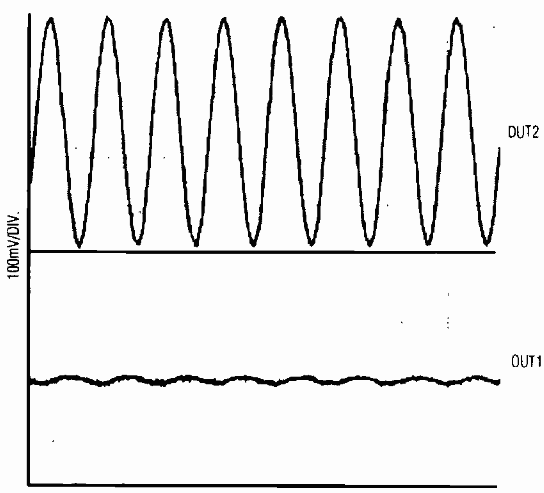


These two signals, recovered from either end of a single-cable bidirectional link, are 2 and 1MHz respectively.



*NOTE: TO MAINTAIN 0dB GAIN AS REQUIRED, THE INPUTS MUST SEE 50Ω SOURCES, AND THE OUTPUTS MUST SEE 50Ω LOADS. (YOU CAN ALSO CONFIGURE 0dB GAIN BY SUBSTITUTING 75 Ω CABLES, 75Ω TERMINATIONS, AND 300Ω FOR THE g_M-SETTING RESISTORS R_2, R_3, R_8, AND R_9)

Two transconductance amplifiers form a high-frequency coaxial cable interface similar to the hybrid-circuit interface found in telephones.



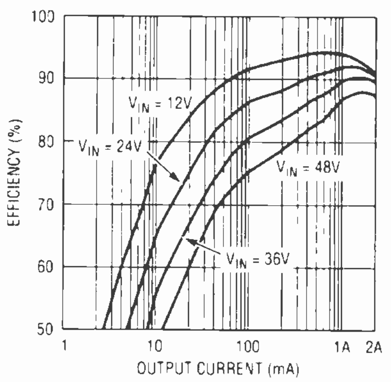
In a high-speed bidirectional link, one of the main problems is getting the receiver at the transmitting end to ignore the transmitted signal. If 1% resistors are used, the circuit shown can cancel to about 30dB (lowest trace).

Step-down converter remains efficient at low currents

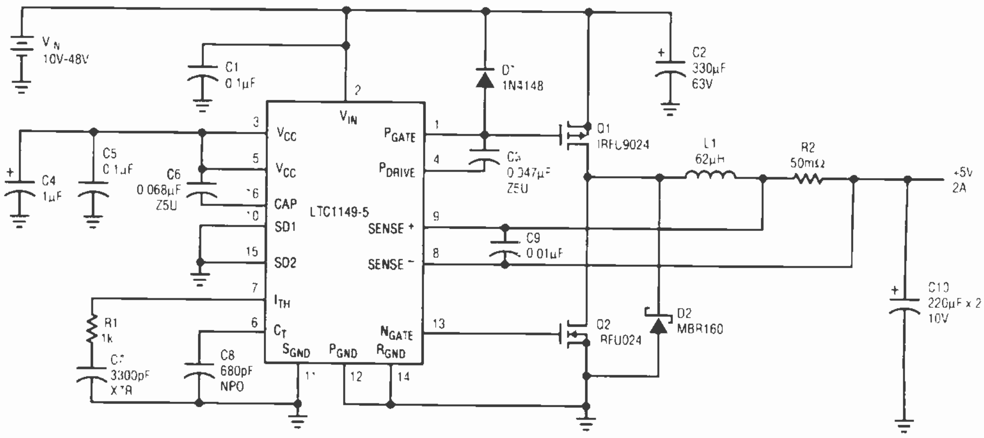
At currents of around an amp and an input of 12V, this step-down converter is 93% efficient. Many switching converters are highly efficient at a specific output current near their maximum but this design remains efficient as current falls. Although efficiency is highest at low input voltages, the circuit operates from supplies up to 48V.

Designed for use in battery and low power applications, the *LTC1149-5* is a synchronous switching step-down controller capable of operating in 'burst mode'. As Linear Technology's *Power Solutions 1993* brochure explains, it is this mode that allows the device to maintain efficiency with low output currents.

At very low battery voltages the IC produces a 100% duty cycle, i.e. the circuit stops switching and passes current directly to the output. The only losses are those in the mosfet, inductor and sense resistor.



Most switching regulators are efficient near the limit of their operating current but this one remains efficient at low currents.



C2 UNITED CHEMI-CON (AL) LXF63VB331M12.5 x 30 ESR = 0.170Ω I_{RMS} = 1.280A
C4 (TA)
C10 SANYO (OS CON) 10SA220M ESR = 0.035Ω I_{RMS} = 2.360A
Q1 IR PMOS BV_{DSS} = 60V RDS_{ON} = 0.280Ω C_{RSS} = 65pF Q_g = 19nC
Q2 IR NMOS BV_{DSS} = 60V RDS_{ON} = 0.100Ω C_{RSS} = 79pF Q_g = 28nC
D1 SILICON VBR = 75V
D2 MOTOROLA SCHOTTKY VBR = 60V
R2 KRL NP-1A-C1-0R050J Pd = 1W
L1 COILTRONICS CTX62-2-MP DCR = 0.040Ω MMP CORE

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QUIESCENT CURRENT = 1.5mA
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When battery input voltage falls to a predefind level, this switching converter stops switching so the only losses are those in the mosfet, inductor and sense resistor.

In normal mode, the two mosfets switch synchronously. Constant off-time control maintains constant ripple current in the inductor, easing the design in applications needing a wide input voltage range.

Current mode control ensures good line and load regulation. This circuit provides 5V at 2A load current with ±5% regulation over load and line variations. Although efficiency is maximum at low input voltages, it stays above 80% for load currents down to 20mA under most conditions. In shut-down mode, current consumption falls to less than 420µA.

A 3.3V version of the IC is available, namely the *LTC1149-3.3*. There are over forty more circuits in *Power Solutions 1993*.

Linear Technology Corporation, *Coliseum Business Centre, Riverside Way, Camberley, Surrey GU15 3YL. Tel. 0276 677676.*

New solution to current sensing

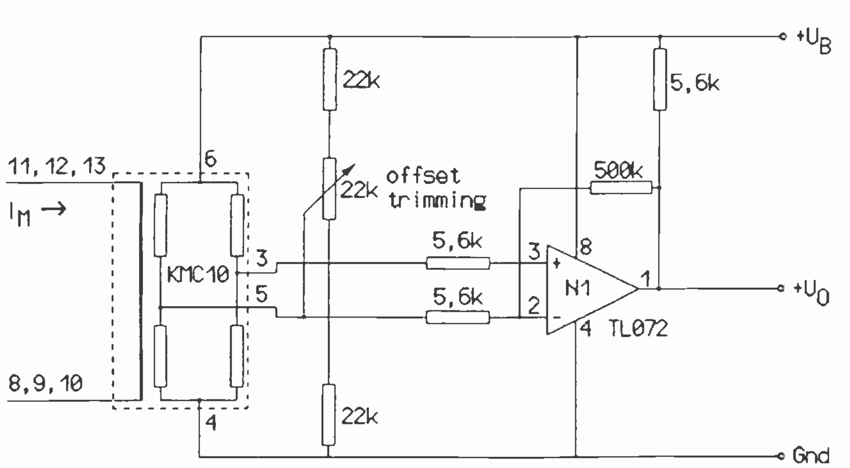
By sensing current via the magnetic field it produces, a new type of transducer from Zetex combines the features of low measurement voltage drop and galvanic isolation.

As this circuit from the *KMC10* data sheet implies, the shunt is isolated from the sensor to 2kV. In systems where only one power supply is available, this reduces grounding problems and removes the need for a separate supply. Additionally, the magnetic circuit is sensitive. As a result the shunt resistance is small and causes little effect when inserted in the circuit being measured.

Maximum current handled by the *KMC10* is 10A while resistance of its shunt is 0.7mΩ. Offset trimming is provided in the application circuit to compensate for the sensing bridge's maximum offset of ±2mV.

The bridge makes use of the magnetostrictive effect of thin-film permalloy and operates up to 100kHz. Temperature limits of the device are –65° and 120°C. ■

Zetex, *Fields New Road, Chadderton, Oldham OL9 8NP. Tel. 061 627 4963.*



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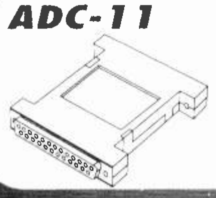

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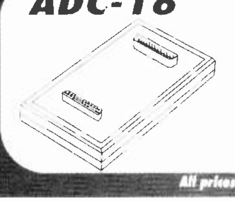

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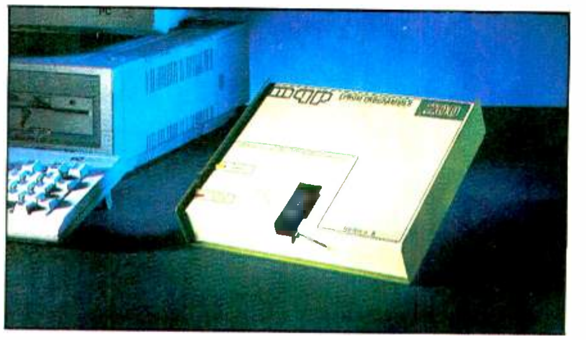

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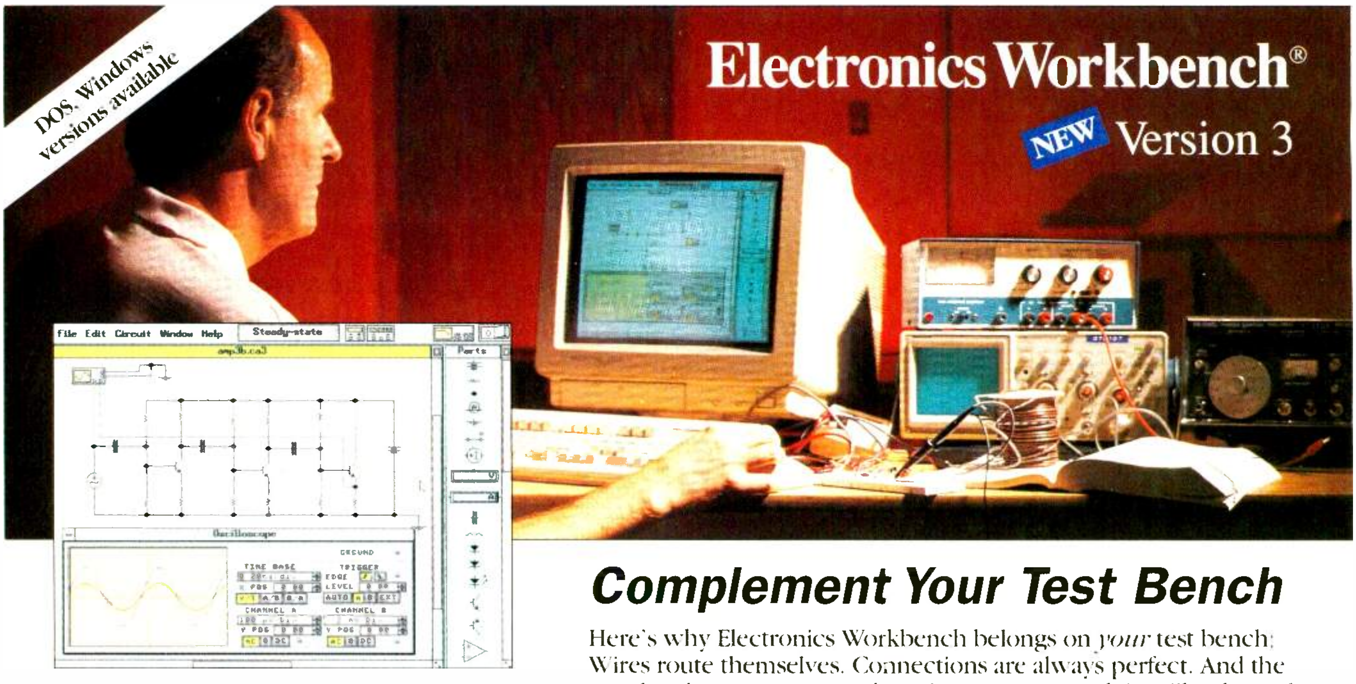

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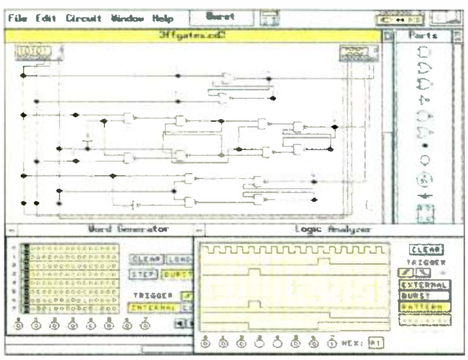

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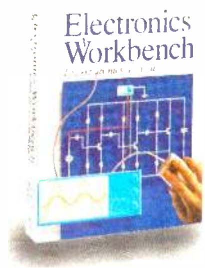

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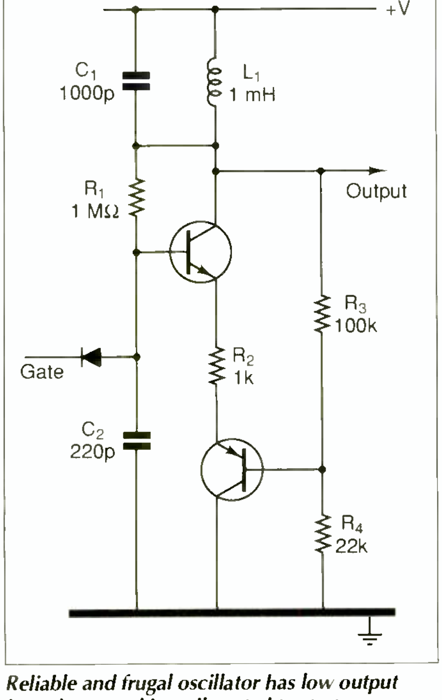
Cascode oscillator

£100 WINNER

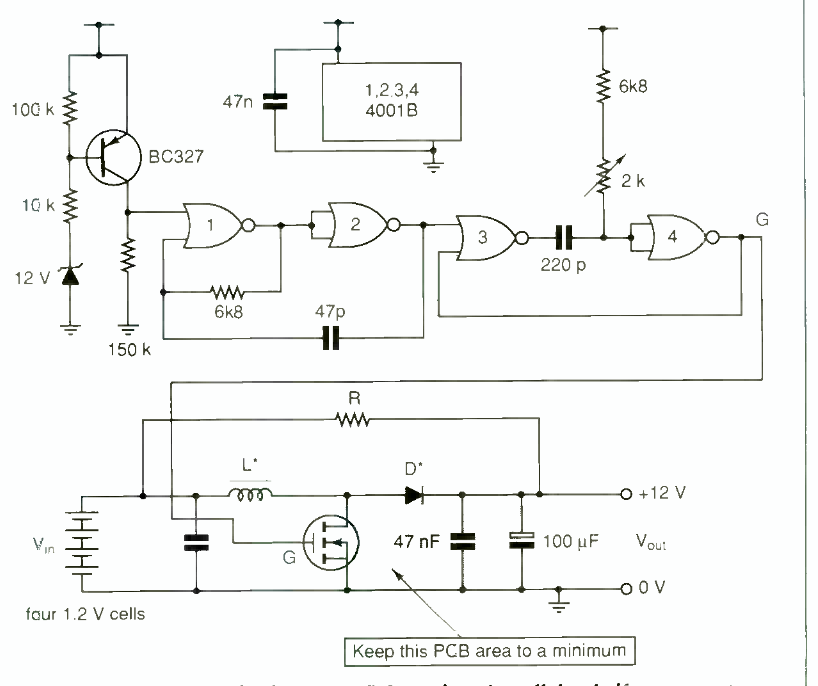
This is a simple oscillator, but is very reliable and exhibits many of the features of a near-perfect circuit.

It uses a two-terminal coil with no taps, self starts and draws only 1mA at 12V, the drive being inherently Class D. Output impedance is small and output swing large. Over the supply-voltage range of 2-24V, frequency stability and waveform purity are exceptional. Taking the gate input to 0V starts the oscillator at the same point in the cycle and the earthy end of R_4 has a similar, but reversed effect. Tuned circuit L_1C_2 determines frequency – 160kHz in the case shown – and the time constant R_1C_2 must be longer than the period.

J J Hyland
Glazertron Ltd
Rochester
Kent



Reliable and frugal oscillator has low output impedance and is easily gated to start consistently at the same point.



DC-to-DC boost converter backs up 12V DC supply, using off-the-shelf components. Cells are normally on charge.

Battery backup

This provides 12V DC to an alarm clock when the mains-derived supply fails, the 12V coming from four 1.2V cells in a boost converter. The circuit is simply connected in parallel with the existing DC supply, which maintains charge on the cells through R.

If the mains supply falls, the *BC327* circuitry detects the drop and turns on the 1MHz multivibrator of gates 1 and 2, which triggers the monostable of gates 3 and 4, the output pulse of which is variable in width.

The pulse, G, drives the converter mosfet, a low-voltage, low-$R_{DS(on)}$ type such as the *BUZ10*. Diode D is an ultra-fast device (an MUR110 was used) and inductor L is five turns of doubled 0.2mm diameter enamelled-copper wire on a ferrite bead, inductance being 20µH. It must not enter saturation.

With a 100kΩ load, 3V from the cells gives 12V output, this increasing to 5V for loads of 1kΩ or less down to a practical limit of a 220Ω load (around 50mA).

Dominique Bergogne
Saint Etienne
France

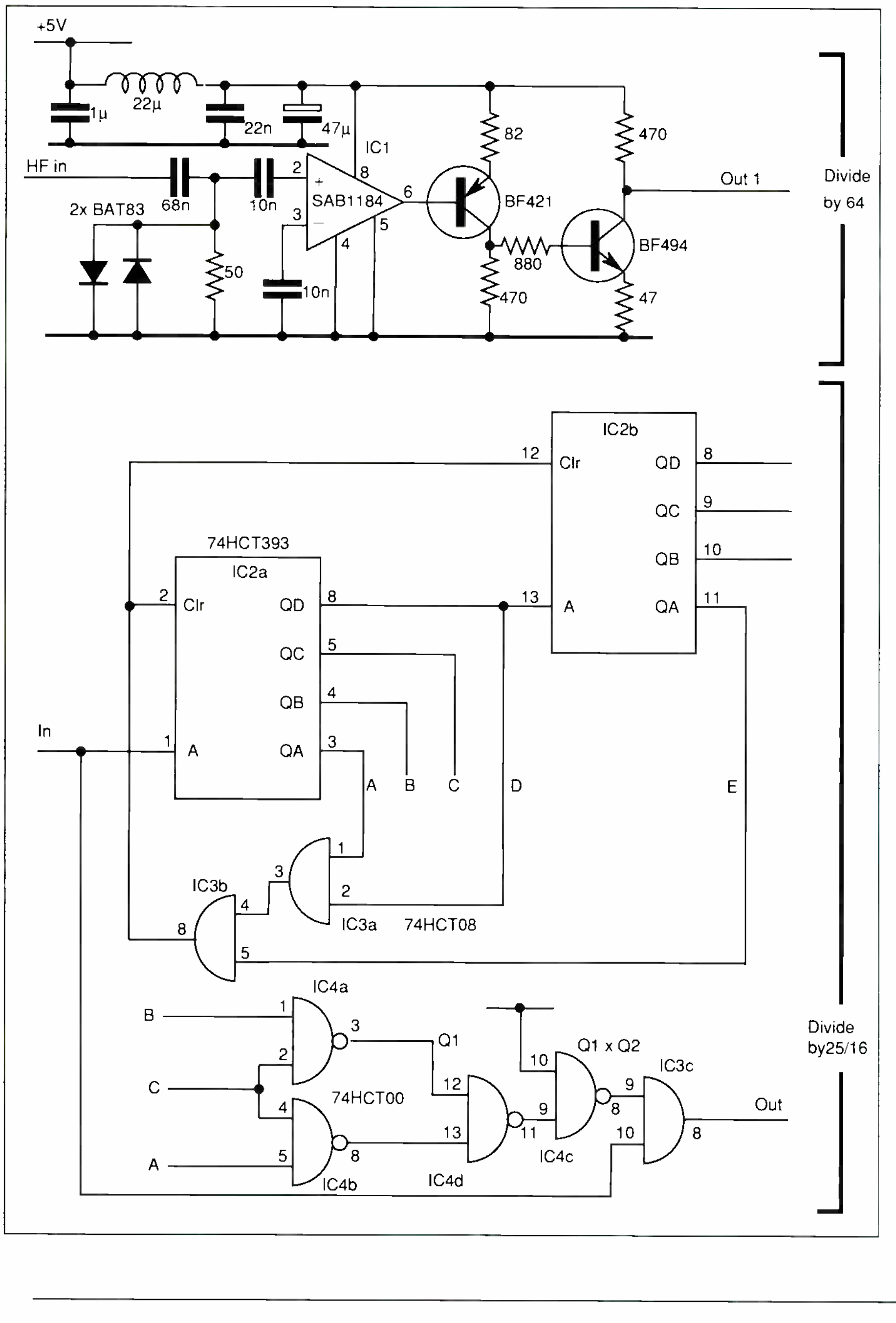
1GHz frequency divider

To extend the frequency range of a 10MHz counter frequency meter to 1GHz, the input frequency must be divided by 100, to give a convenient reading. The frequency divider used in PLL tuners, shown as IC_1 in the circuit diagram, divides by 64, so that a further division of 25/16 remains to be carried out.

$IC_{2a,b}$ are a dual binary counter, which would normally count to 256, but which is reset at a count of 25 by the fed-back A, D and E outputs via And gates $IC_{3a,b}$, as shown in the timing diagram. Outputs B, C and A are further used by IC_4 and IC_{3c} to allow 16 input pulses to proceed to the output during this time, so that the division ratio is 25/16.

W Dijkstra
Waalre
The Netherlands

Wide-band 64 divider, followed by 25/16 divider, gives division by 100 to extend measuring range of lower-frequency counter frequency meter.



Remote motor control

Using only the two DC power-supply leads, this circuit switches the motors in a remote unit such as a television camera over a distance up to 100m or more with a different control signal. An *LM3914* bar-graph IC in dot mode forms the core of the system, its input being the "raw" power supply itself, varied in steps at the remote control point.

Since the power line varies, a voltage regulator restores the correct level to the control circuitry, the type depending on the motors. Eight op-amps in two *LM324* quads, boosted by transistor pairs if necessary, select motors and direction. Op-amp IC_{4a} amplifies the IC_3 reference voltage and reapplies it to the internal resistor chain after adjustment to about 7V by RV_1. This output is also used as adjustable offset to IC_{4b}.

Resistors $R_{28,29}$ apply line changes to the input op-amp. **Figure 2** shows the selector circuit, in which a switched resistor chain varies the output of a regulator from 13V to 15V.

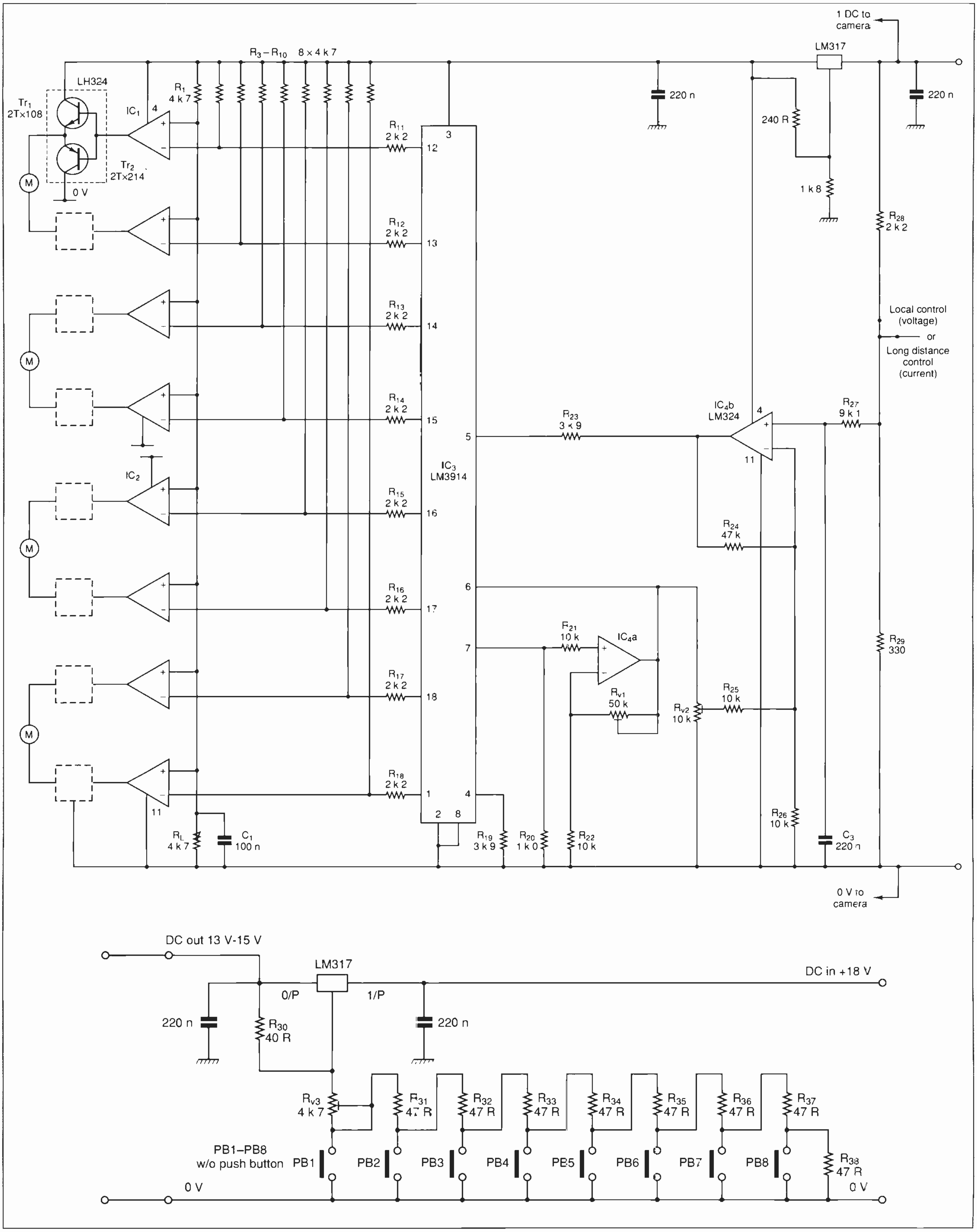
To set up, adjust RV_1 so that pin 12 of the bar graph is selected with 15V applied to the input (a led array on the bar graph output assists here). Then, with 13V applied, adjust RV_2 to select pin 1, repeating the process if necessary.

For greater distances than around 100m, a 4-20mA current loop could be used, R_{28} being removed.

Ken Bedwell
Rees Instruments Ltd
Godalming
Surrey

Shown top-right, Fig. 1. Bar-graph IC controls motors in response to remote signals carried on power lines.

Shown right, Fig. 2. Remote selector circuit for distances up to around 100m; for greater distances, a current loop would be better.


1 DC to camera
LM317
R3 – R10 8 x 4 k 7
LH324
Tr1 2Tx108
IC1
R1 4 k 7
220 n
240 R
1 k 8
Tr2 2Tx214
0 V
R11 2 k 2
R12 2 k 2
R13 2 k 2
R14 2 k 2
R15 2 k 2
R16 2 k 2
R17 2 k 2
R18 2 k 2
R28 2 k 2
Local control (voltage)
or
Long distance control (current)
IC2
IC3 LM3914
R23 3 k 9
IC4b LM324
R27 9 k 1
R24 47 k
R21 10 k
IC4a
Rv1 50 k
Rv2 10 k
R25 10 k
R29 330
R26 10 k
RL 4 k 7
C1 100 n
R19 3 k 9
R20 1 k 0
R22 10 k
C3 220 n
0 V to camera
DC out 13 V-15 V
LM317
DC in +18 V
0/P
1/P
220 n
R30 40 R
Rv3 4 k 7
R31 47 R
R32 47 R
R33 47 R
R34 47 R
R35 47 R
R36 47 R
R37 47 R
R38 47 R
PB1–PB8 w/o push button
PB1 PB2 PB3 PB4 PB5 PB6 PB7 PB8
0 V

Simple DC modulator

In addition to its requirement for only a single switch, this modulator does not isolate the input.

As the feedback loop of the op-amp in **Fig.1** is varied by v_{mod}, its gain changes and is given by $(R_2 + R_4 + R_2R_4/R_3)/R_1$. The output is not, however, symmetrical about zero.

In **Fig.2**, the op-amp forms either an inverting amplifier or a voltage follower, depending on v_{mod}, to give an output about zero.

N I Lavrantiev
Schiulkovo
Moscow Region

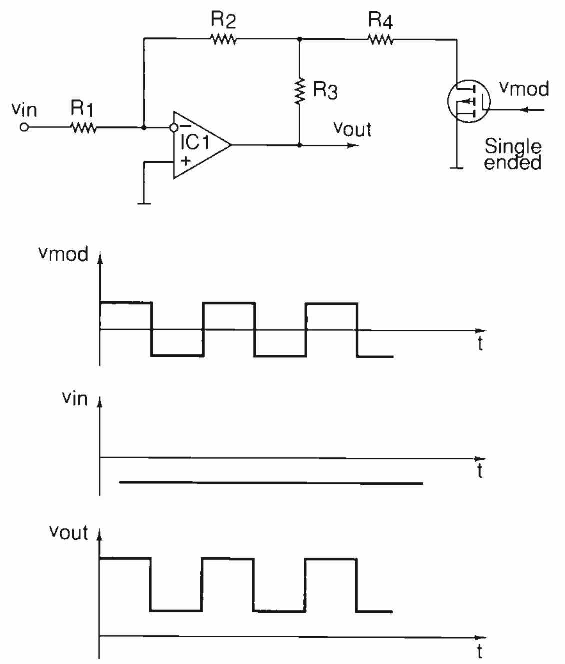


Fig.1. Modulator uses only one switching element, the signal not being isolated at any time.

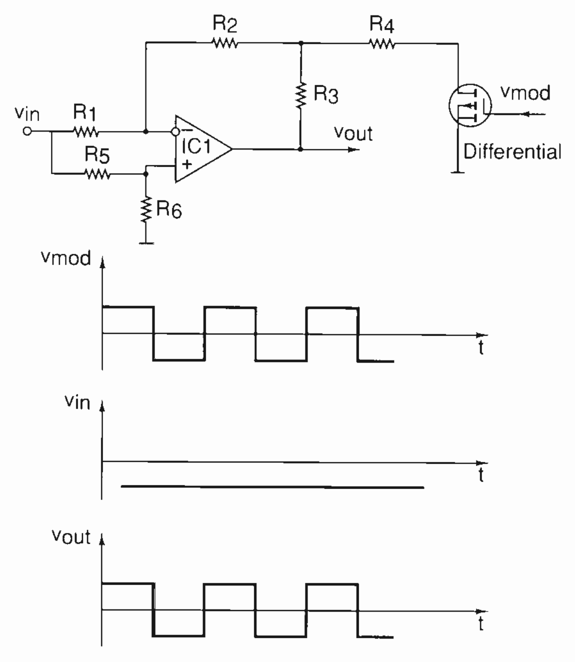


Fig.2. This connection either inverts or follows the input, depending on the modulating voltage, and gives a symmetrical output.

Electrolytic ESR tester

In sensitive circuitry, for example in a feedback loop, it is often necessary to know the equivalent series resistance of an electrolytic capacitor. This circuit measures ESR quickly and simply, assuming access to a digital storage oscilloscope.

Operation is simple: press the push-button switch and view the DSO trace. Calculate ESR from $ESR=(v_1/v_2)-1$ in ohms, the two voltages being those indicated in Fig. 2.

Replacement of the pushbutton switch with a logic switched mosfet would eliminate switch bounce effects. It would also allow operation at higher voltages for greater signal output. The channel resistance and self capacitance of the device need to be taken into account however.

A M Wilkes
Glasgow

Faulty circuit

There was an unfortunate printing error in my circuit idea (*EW+WW*, November 1993). Propagation delay decreases and not increases as V_{cc} is increased.

This is fundamental to understanding the whole design.

Laurence Richardson
Horsham, Surrey

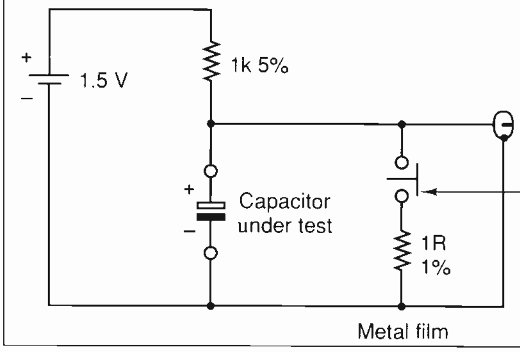


Fig.1. Very simple circuit to measure equivalent series resistance of an electrolytic capacitor.

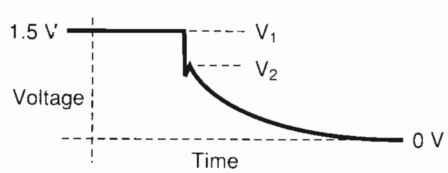


Fig.2. Trace on DSO resulting from capacitor discharge.

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Racal/Dana 9301A-9302 RF Millivoltmeter – 1.5-2GHz – £250-£400.
Racal/Dana Counters 9915M – 9916 – 9917 – 9921 – £150 to £450. Fitted FX standards.
Racal/Dana Modulation Meter type 9009 – 8Mc/s – 1.5GHz – £250.
Racal – SG Brown Comprehensive Headset Tester (with artificial head) Z1A2001/1 – £350.
Marconi AF Power Meter type 893B – £200.
Marconi RCL Bridge type TF2700 – £150.
Marconi/Saunders Signal Sources type – 6058B – 6070A – 6055B – 6059A – 6057B – 6056 – £250-£350. 400Mc/s to 18GHz.
Marconi TF1245 Circuit magnification meter + 1246 & 1247 Oscillators – £100-£300.
Marconi microwave 6600A sweep osc., mainframe with 6650 PI – 18-26.5GHz or 6651 PI – 26.5-40GHz – £1000 or PI only £600.
Marconi distortion meter type TF2331 – £150, TF2331A – £200.
Microwave Systems MOS/3600 Microwave frequency stabilizer – 1GHz to 40GHz £1k.
Tektronix Plug-ins 7A13 – 7A14 – 7A18 – 7A24 – 7A26 – 7A11 – 7M11 – 7S11 – 7D10 – 7S12 – S1 – S2 – S6 – S52 – PG506 – SC504 – SG502 – SG503 – SG504 – DC503 – DC508 – DD501 – WR501 – DM501A – FG501A – TG501 – PG502 – DC505A – FG504 – P.O.R.
Alltech Stoddart receiver type 17/27A – .01–32Mc/s – £2500.
Alltech Stoddart receiver type 37/57 – 30-1000Mc/s – £2500.
Alltech Stoddart receiver type NM65T – 1 to 10GHz – £1500.
Gould J3B Test oscillator + manual – £200.
Infra-red Binoculars in fibre-glass carrying case – tested – £100. Infra-red AFV sights £100.
ACL Field Intensity meter receiver type SR – 209 – 6. Plugs-ins from 5Mc/s to 4GHz – P.O.R.
Tektronix 491 spectrum analyser – 1.5GHz-40GHz – as new – £1000 or 10Mc/s 40GHz.
Tektronix Mainframes – 7603 – 7623A – 7633 – 7704A – 7844 – 7904 – TM501 – TM503 – TM506 – 7904 – 7834 – 7104.
Knott Polyskanner WM1001 + WM5001 + WM3002 + WM4001 – £500.
Alltech 136 Precision test RX + 13505 head 2 – 4GHz – £350.
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Alltech 757 Spectrum Analyser – 001 22GHz – Digital Storage + Readout – £3000.
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HP141T + 8552A or B IF-8556A RF – 20Hz–300kHz-A IF-A IF – £1200 or B IF – £1300.
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Marconi RF Power Amplifier TF2175 – 1.5Mc/s to 520Mc/s with book – £100.
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Schlumberger 2741 Programmable Microwave Counter – 10Hz to 7.1GHz – £750.
Schlumberger 2720 Programmable Universal Counter 0 to 1250Mc/s – £600.
HP 2225CR Thinkjet Printer – £100.
TEK 576 Calibration Fixture – 067-0597-99 – £250.
HP 8006A Word Generator – £150.
HP 1645A Data Error Analyser – £150.
Texscan Rotary Attenuators – BNC/SMA 0-10-60-100DBS – £50-£150.
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Alltech Stoddart P7 programmer – £200.
H.P. 6941B multiprogrammer extender. £100.
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H.P. 59501A – HP-IB isolated D/A/power supply programmer.
H.P. 3438A digital multimeter.
H.P. 6177C DC current source. £150.
H.P. 6207B DC power supply.
H.P. 741B AC/DC differential voltmeter standard (old colour) £100.
H.P. 6209B DC power unit.
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Fluke 431C high voltage DC supply.
Tektronix M2 gated delay calibration fixture. 067-0712-00.
Tektronix precision DC divider calibration fixture. 067-0503-00.
Tektronix overdrive recovery calibration fixture. 067-0608-00.
Avo VCM163 valve tester + book £300.
H.P. 5011T logic trouble shooting kit. £150.
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Telequipment CT71 curve tracer – £200.
H.P. 461A amplifier – 1kc–150Mc/s – old colour – £100.
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Tektronix oscilloscopes type 2215A – 60Mc/s – c/w book & probe – £400.
Tektronix monitor type 604 – £100.
Marconi TF2330 or TF2330A wave analysers – £100–£150.
HP5006A Signature Analyser £250 + book.
HP10783A numeric display. £150.
HP 3763A error detector. £250.
Racal/Dana signal generator 9082 – 1.5–520Mc/s – £800.
Racal/Dana signal generator 9082H – 1.5–520Mc/s – £900.
Claude Lyons Compuline – line condition monitor – in case – LMP1 + LCM1 £500.
Efratom Atomic FX standard FRT – FRK – .1–1–5–10Mc/s. £3K tested.
Racal 4D recorder – £350 – £450 in carrying bag as new.
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Alltech – precision automatic noise figure indicator type 75 – £250.
Adret FX synthesizer 2230A – 1Mc/s. £250.
Tektronix – 7S12–7S14–7T11–7S11–S1–S52–S53.
Rotek 610 AC/DC calibrator. £2K + book.
Marconi TF2512 RF power meter – 10 or 30 watts – 50 ohms – £80.
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Marconi digital simulator type 2828A.
Marconi channel access switch type 2831.
Marconi automatic distortion meter type TF2337A – £150.
Marconi mod meters type TF2304 – £250.
HP 5240A counter – 10Hz to 12.4GHz – £400.
HP 3763A error detector.
HP 8016A word generator.
HP 489A micro-wave amp – 1–2GHz.
HP 8565A spectrum analyser – .01–22GHz – £4k.
HP 5065A rubidium vapour FX standard – £5k.
Fluke 893A differential meters – £100 ea.
Systron Donner counter type 6054B – 20Mc/s–24GHz – LED readout – £1k.
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EG&G Parc model 4001 indicator + 4203 signal averager PI.
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Systron Donner microwave counter 6057 – 18GHz – Nixey tube – £600.
Racal/Dana synthesized signal generator 9081 – 520Mc/s – AM–FM. £600.
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Farnell TTS520 test set – £500 – both £900.
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Claude Lyons LCM1P line condition monitor – £250.
Rhodes & Schwarz power signal generator SLRD-280 – 2750Mc/s. £250–£600.
Rhodes & Schwarz vector analyser – ZPV + E1 + E3 tuners – .3–2000Mc/s.
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Trend Data tester type 100 – £150.
Farnell electronic load type RB1030-35.
Fairchild interference analyser model EMC-25 – 14kc/s–1GHz.
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Marconi 6700A sweep oscillator + 6730A – 1 to 2GHz.
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HP8505A network ANZ + 8502A test set – £3k.
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Racal Dana VLF frequency standard equipment. Tracor receiver type 900A + difference meter type 527E + rubidium standard type 9475 – £2750.
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B&K dual recorder type 2308
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HP signal generators type 626 – 628 – frequency 10GHz–21GHz.
HP 432A–435A or B–436A – power meters + powerheads – 10Mc/s–40GHz – £200–£280.
HP3730B down convertor – £200.
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Spectrascope SD330A LF realtime ANZ – 20Hz–50kHz – LED readout – tested – £500.
HP8620A or 8620C sweep generators – £250 to £1k with IEEE.
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Tektronix 7L12 analyser – .1Mc/s–1.8GHz – £1500 – **7L14 ANZ** – £2k.
Marconi TF2370 spectrum ANZ – 110Mc/s – £1200–£2k.
Marconi TF2370 spectrum ANZ + TK2373 FX extender 1250Mc/s + trk gen – £2.5k–£3k.
Racal receivers – RA17L–RA1217–RA1218–RA1772–RA1792 – P.O.R.
Systron Donner microwave counter 6057 – 18GHz – nixey tube – £600.
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SOLAR ENERGY EDUCATIONAL KIT. It shows how to make solar circuits and electrical circuits, how to increase voltage or current, to work a radio, calculator, cassette player and to charge nicad batteries. The kit comprises 8 solar cells, one solar motor, fan blades to fit motor and metal frame to hold it to complete a free-standing electric fan. A really well written instruction manual. £8, Order Ref. 842B.

POWER SUPPLIES – SWITCH MODE

(all 230v mains operated)
Astec ref. B51052 with outputs +12v .5A, −12v .1A, +5v 3A, +10v .05A, +5v .02A unboxed on pcb size 180x130mm, £5, Order Ref. 5P188.
Astec ref. BM4 1004 with outputs +5v 3½A, +12vc 1.3A, −12v 1.2A, £5, Order Ref. 5P199
Astec No. 12530 +12v 1A, −12v .1A, +5v 3A, uncased on pcb size 160x100mm. £3, Order Ref. 3P141
Astec No. BM41001 110W 38v 2.5A, 25.1v 3A part metal cased with instrument type main input socket & on/off dp rocker switch size 354x118x84mm, £8.50, Order Ref. 8.5P2
Astec model No. BM135-3302 +12v 4A, +5v 16A, −12v 0.5A totally encased in plated steel with mains input plug, mains output socket & double pole on/off switch size 400x130x65mm, £9.50, Order Ref. 9.5P4

POWER SUPPLIES – LINEAR

(all cased unless stated)
4.5v dc 150mA, £1, Order Ref. 104
5v dc 2½A psu with filtering & volt regulation, uncased, £4, Order Ref. 4P63
6v dc 700mA, £1, Order Ref. 103
6v dc 200mA output in 13A case, £2, Order Ref. 2P112
6-12v dc for models with switch to vary voltage and reverse polarity, £2, order Ref. 2P3
9v dc 150mA, £1, Order Ref. 762
9v dc 2.1A by Sinclair, £3, Order Ref. 3P151
9v dc 100mA, £1 Order Ref. 733
12v dc 200mA output in 13A case, £2, Order Ref. 2P114
12v 500mA on 13A base, £2.50, Order Ref. 2.5P4
12v 1A filtered & regulated on pcb with relays & Piezo sounder, uncased, £3, Order Ref. 3P80
Amstrad 13.5v dc at 1.8A or 12v dc at 2A, £6, Order Ref. 6P23
24v dc at 200mA twice for stereo amplifiers, £2, Order Ref. 2P4
9.5v ac 600mA made for BT, £1.50m, Order Ref. 1.5P7
15v 500mA ac on 13A base, £2, Order Ref. 2P281
AC out 9.8v @ 60mA & 15.3v @ 150mA, £1, Order Ref. 751
BT power supply unit 206AS, charges 12v battery and cuts off output should voltage fall below pre-set, £16, Order Ref. 16P6
Sinclair microvision psu, £5, Order Ref. 5P148

LASERS & LASER BITS

2mW laser, helium neon by Philips, full spec. £30, Order Ref. 30P1
Power supply for this in kit form with case is £15, Order Ref. 15P16, or in larger case to house tube as well, £18, Order Ref. 18P2.
The larger unit, made up, tested and ready to use, complete with laser tube, £69, Order Ref. 69P1

HEATING UNITS

Linear quartz glass tubes 360W, 2 in series for mains, £1, Order Ref. 907
1000W spiral elements for repairing fires etc. 3 for £1, Order Ref. 223
1000W pencil elements, 2 for £1, Order Ref. 376
1.2kW mini tangential heater, ideal for under desk etc, £5, Order Ref. 5P23
2kW tangential heater, £6, Order Ref. 6P30
3kW tangential heater, £8, Order Ref. 8P24
12' tubular heater, slightly storage soiled, £6, Order Ref. 6P31
Water-proof heating wire, 60ohms per metre, 15m is right length for connecting to mains, £5, Order Ref. 5P109

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ACTIVE

A-to-D & D-to-A converters

30Msample/s A-to-D. Two-step analogue-to-digital converter from Signal Processing Technologies, the *SPT1175*, produces 8-bit words at conversion rates up to 30msample/s. Signal-to-noise ratio is 45dB for 3.58MHz input at 20Msample/s and differential gain and phase are 1% and 0.7° respectively; large-signal bandwidth 12MHz; and input capacitance less than 15pF. Differential non-linearity is ±0.6LSB and there are no missing codes over the entire operating range. Ambar Cascom Ltd, 0296 434141.

Small, 12-bit A-to-D. *LTC1257* from Linear is a complete 12-bit, voltage-output, single-supply digital-to-analogue converter in a surface-mounting SO-8 package, with output buffer amplifier, 2.048V reference and three-wire serial interface. Differential non-linearity error is 0.5 LSB. Power supply needed is 4.7-15.75V, current being 350μA at 5V. Linear Technology (UK) Ltd, 0276 677676.

3.3V, 10-bit A-to-Ds. TI's new family of A-to-D converters have 10-bit resolution, 21μs conversion time, on-chip, microprocessor-controlled sample-and-hold and a serial interface supporting the Serial Peripheral Interface and Microwire. The single-input *TLV1549* is contained in an 8-pin dip or SO and the 11-input *TLV1543* in a 20-pin dip or wide-body SO. Texas Instruments, 0234 223252.

Discrete active devices

Disk-drive Schottky. Dual Schottky barrier diode from Allegro is meant chiefly for use in hard-disk drives. The *A8920SL* exhibits a 440mV forward drop at 150mA, a 500mA maximum forward current and 20V reverse voltage and reverse recovery time at 100mA of 32ns. A multi-chip version, the *TND8000*, has three pairs of diodes in a 16-lead SOIC package. Allegro Microsystems Ltd, 0932 253355.

Fast diodes. Silicon epitaxial planar diodes in ITT's new range provide extremely fast switching. *BAS16* handles 100Vpk reverse, 150mA average rectified current and 500mA surge forward at 25°C. Dual, common-cathode diodes. *BAZ70* and *BAV99*, and the *BAW56* common-anode type offer 70Vpk reverse and 250mA continuous forward. Power dissipation is 350mW. ITT Semiconductors, 0932 336116.

Smart fets. *IRSF3010* SmartFET transistors by International Rectifier feature over-current shutdown, gate/drain clamp and gate/source clamp for ESD protection. There is also over-temperature protection which is latched, as is the over-current circuit. Polar Electronics Ltd, 0525 377093.

Fast rectifiers. Super fast rectifier diodes from Semtech have reverse voltages from 2.5kV to 10kV, recovery time of 60ns and forward currents of 100mA-1A. Reverse current is 0.2μA-1μA. Type numbers are *1FFXX, 2FFXX, 5FFXX* and *10FFXX*. Semtech Ltd, 0592 773520.

Power mosfet. Siliconix's *Si9936DY Little Foot* power mosfet is meant for use in disk drives and portable computers, delivering 5A with a rated on resistance of 50mΩ. It is a dual n-channel device and replaces two typical SM or TO-220 devices. Voltage rating is 30V. Siliconix/TEMIC Marketing, 0344 485757

Digital signal processor

32-bit DSPs. TI announces its first low-power 32-bit digital signal processor. The 33Mflop/s performance achieved by the 5V *TMS320C31* is now available in the 3.3V version, the *TMS320LC31*, with no increase in price. Two power-down modes are provided to either reduce the instruction rate or shut down an inactive device while retaining memory contents. A new version of the 5V device runs at 50Mflop/s. Texas Instruments Ltd, 0234 223252.

Linear integrated circuits

Photodiode amplifier. A low-cost photodiode amplifier from Centronic, the *CA-100*, measures currents from 200pA to 2mA, giving an output of 2V at an accuracy of 1% FSD on all eight ranges. It can be operated in optical-power mode, in which the calibration adjust control sets the amplifier to a known optical power to give direct reading of optical power on the LC display. Detectors are available as extras. Centronic Ltd, 0689 842121.

Phase control. GEC Plessey's *TDA2088* bipolar IC is for current feedback phase control in motor-speed controllers; it is also usable in open-loop mode. Power comes from an AC or DC supply, the IC incorporating a –5V regulator for internal functions and to power external circuitry. Output triac drive is 100mA maximum. Gothic Crellon Ltd, 0734 788878.

Cheap 900MHz chipset. Five chips from Motorola, *MRFIC2001/2/3/4/5/6*, form a 900MHz chipset for personal communication. Costing $13.57 in low volumes, the set is designed for use as front end for CT-2 cordless telephones, but is also suitable for GSM, ISM and 915MHz cordless. The chipset consists of a down-converter LNA/mixer, transmit mixer, GaAs antenna switch, driver and ramp and a two-stage power amplifier. Motorola Inc., (USA) 602 994 6561.

TV signal encoders. *TDA8501* and *TDA8505* television signal encoders by Philips convert RGB or YUV video input to standard composite video, *8501* for Pal or NTSC and *8505* for Secam. Both types produce separate luminance and chrominance for equipment such as VHS-C recorders. A minimum of external components is needed: a luminance delay line, a few *CR*s and a crystal for the *8501*. *TDA8501* needs no alignment and *TDA8505* only one operation. Philips Semiconductors, (Europe)+31 40722091

ICE stereo decoder. *TDA1592* is a development of Philips's existing *TDA1591* stereo decoder/noise blanker for high-performance car radio. It features 50mV muting offset to give RDS switching without clicks, an S:N ratio of 82dB, input overdrive of 6dB and automatic FM/AM high-cut control for weak signal conditions. An analogue voltage from the level detector allows smooth stereo/mono changeover with signal level. Philips Semiconductors, (Europe)+31 40722091

Logic building blocks

Small clock. A clock module measuring 10.31 by 5 by 3.35mm, the *RTC-8583* by Epson, has a built-in 32kHz crystal oscillator, an I²C-bus interface and alarm and timer functions. It operates at supply voltages down to 2.5V and offers a data-hold range of 1-6V. Epson, 0442 227331.

Microcontroller. Hitachi has a new member of its *H8* series of microcontrollers operating with supply voltages of 2.7-5.5V. It is based on a 16-bit register architecture addressing up to 16Mbyte and has a 1.9Mi/s performance in a Dhrystone benchmark at 16MHz. Hitachi Europe Ltd, 0628 585000.

Microprocessors and controllers

Microcontrollers. New versions of Hitachi's *H8/500* microcontrollers in 0.8μm cmos offer a choice of higher speed or low-voltage operation and different packages. *H8/535* and */536* have 32K or 62K of rom or eprom and 2K of on-chip ram, the "*S*" versions operating at up to 16MHz at 5V to give a minimum instruction time of 125μs. 16 by 16-bit multiplications take up 1.4μs and 32/16-bit division 1.63μs. Several timers are provided, as is a 10-bit A-to-D converter. New packaging is the Thin QFP, which is only 1.2mm thick. Hitachi Europe Ltd, 0628 585000.

Low-power microprocessor. Motorola's *PowerPC 603* is a low-power design intended for use in notebook and laptop computers, running all the popular operating systems including *OS, OS/2, MS-Dos* via emulation, standard variations of *Unix* and pen-based systems. Its superscalar architecture allows three instructions per clock cycle at frequencies up to 80MHz. Motorola Ltd, 0296 395252.

64-bit risc processor. A low-power, low-cost, 64-bit risc processor, the *VR4200* by NEC, achieves an 80MHz clock speed, derived from a 40MHz external clock, and operates on 3.3V at 1.5W (0.4W standby). Functions include calibration adjustment, floating calculation unit and a cache memory for 16Kb of instructions and 8Kb of data. Packages are a 179-pin PGA or a 208-pin QFP. NEC Electronics (UK) Ltd, 0908 691133.

Fuzzy co-processor. The *VY86C570* is a 12-bit, high-performance fuzzy co-processor capable of carrying out full fuzzy rule evaluations 20-30 times faster than software-only methods, being capable of more than 850 000 rule evaluations per second at 20MHz. Its integral rule base eliminates the need for external rule-base memory in most cases. VLSI Technology Ltd, 0908 667595.

Mixed-signal ICs.

Data retiming. Analog's *AD805* is a 155Mb/s PLL for data retiming in which the clock-recovery technique eliminates incompatibility between types A and B regenerators, overcoming the jitter-tolerance limitations of type B circuits. The IC exploits the 1° RMS jitter of an external crystal oscillator and has an independent phase-control feedback path to track data with jitter. Analog Devices Ltd, 0932 253320.

Telecomm switch. C P Clare's *TS* series is a combined hookswitch and ring detector in an 8-pin dip, using an optically-isolated mosfet relay for hookswitch, dial pulse or loop start switching, with a bidirectional opto-coupler for ringing current or loop current detection. Switches handle voltages up to 400V pk, AC or DC, and currents to 170mA. Switching speed is 3ms. C P Clare Corporation, 0460 41771.

Audio decoder. Complete audio decompression system in one IC, the *CS4920* by Crystal, contains everything needed to receive and process compressed audio and convert it stereo analogue output; the built-in digital signal processor supporting a range of decompression standards. Signal-to-noise ratio is up to 90dB and THD less than 0.01%. A digital output derived from the decompressed audio conforms to the Sony/Philips Digital Interface Format or the AES/EBU format. Crystal Semiconductor, (US) (512)445-7222.

Real-time MPEG encoders. Details of C-Cube's VideoRISC Compression Architecture (VCA), the first architecture specifically designed to compress and decompress digital video in real time, have been announced. VCA supports encoding and decoding for a variety of international standards, including MPEG, JPEC and H.261. First in the range are the *CLM4600* broadcast MPEG 2 video encoder and the *CLM4500* consumer MPEG 1 version. Kudos Thame Ltd, 0734 351010.

Oscillators

Voltage-controlled oscillators. M/A-COM's *MLO 30000*, *40000* and *50000* series of VCOs use a resonator-stabilised bipolar transistor as a negative-resistance generator and have a Varactor diode for tuning. Doubling extends the fundamental to 18GHz. Low phase noise is obtained in the *30000* series by means of a hyperabrupt Varactor. M/A-COM, 0344 869595.

Programmable logic arrays

2500-gate device. With 282 registers and 2500 usable gates, Altera's *EPF8282* is the newest member of the *FLEX8000* family of programmable logic devices, which Altera claims gives better performance at lower cost than field-programmable arrays. The device is in a 0.8μm cmos static ram process in 3.3V and 5V versions. Average benchmark speed is 40MHz. Altera Ltd, 0628 488811.

Power semiconductors

8A IGBT. Harris claims its *HGTD8P5G1* to be the world's first p-channel, enhancement-mode, insulated-gate bipolar transistor. Main features are 8A collector current and 500V breakdown. The use of a p-channel device in conjunction with n-channel types greatly simplifies the design of circuitry such as half bridges. Harris Semiconductor (UK), 0276 686886.

Voltage regulators. Voltage regulators in SOT223 and E-line packages from Zetex come in five voltages from 3.3V to 10V and give a 200mA output. Power dissipation is 2W for the SM package or 0.6W for the E-line type. Voltage constancy is around 10mV under both line and load variation and quiescent current is held down to 400μA. Zetex plc, 061-627 5105.

Passive components

"Smallest" capacitors Panasonic claims its Series *EL Gold* double-layer capacitors to be the world's smallest, having values in the 0.1F-2F range and measuring 6.8mm in diameter by 1.4mm. Rated working voltage is 2.5V from –25 to 70°C and life is 100 000 charge/discharge cycles. The company also claims the world's largest capacitor — the *Power* range, with a value of 1500F. Panasonic Industrial Europe, 0344 853827.

Displays

Touch screen controller. The *SMT-1* miniaturised, surface-mounted touch screen controller by MicroTouch can be mounted on the back or at the bottom of a CRT and is designed for external retrofitting. It needs only one supply voltage between 5 and 16V at 70mA, obtainable from the monitor. MicroTouch Systems Ltd, 0844 260123.

Fluorescent panel. NEC's chip-in-glass fluorescent display panels have only 22 lead terminals instead of the 198 used in conventional types. The module has an in-built microcomputer, character generator, power supplies and reset. Serial receive data rate is 9600baud. NEC Electronics (UK) Ltd, 0908 691133.

Air-cored coils. Cambion air-wound coils come in any internal diameter from 1.5mm to 10mm as standard, using wire diameters from 0.315mm to 2mm in lengths up to 25mm. They are supplied with tinned or untinned leads and for through-hole or surface mounting. Interconnection Products Ltd, 0433 621555.

PASSIVE

Bargraph display. Babcock's *SP-410-003* DC planar gas display is hermetically sealed in a thin glass package for front-panel mounting. Only seven drivers are needed for the 201 elements in each bar, the display emitting neon-orange light at 40fL against a dark background, with a 130° viewing angle. Selectronic Ltd, 0993 778000.

Dot-matrix module. *GD-032D128-01* from Babcock is a dot-matrix display with a fully populated field of 32 by 128 pixels in an area of 3.15in by 12.75in, displaying four lines of 21 characters, each 0.8in high, or any combination of pixels to represent symbolic images or animation. Drive and signal conditioning is on-board. Typical brightness of the neon-orange light is 55fL. Selectronic Ltd, 0993 778000.

Hardware

Wavesoldering fluids. Soldering fluids from Fry's use nitrogen to produce an oxygen-free soldering path, so that extremely low-activity fluxes can be used to leave a minimum of residue. *1174*, *1175* and *1220* fluids leave even less than conventional low-solids fluxes and no cleaning is needed, giving good results in oxygen concentrations up to 500ppm. Fry's Metals Ltd, 081-665 6666.

Instrumentation

Miniature controller. CAL's model *3200* controller is contained in a 1/32 DIN unit and "auto-tunes" itself to configure it for a range of process variables. Inputs can come from most thermocouples, *PT100* or from five linear process ranges, the 4-digit led display presenting one-digit units, degrees of temperature or engineering units. CAL Controls Ltd, 0462 436161.

Cable data analyser. *Halcyon* is billed as the world's first parallel cable data analyser, which analyses a data stream at very high speed, byte-by-byte and bit-by-bit, correcting it before driving the printer. Its effectiveness is such that its maker, End Design, says it will handle 50kbyte/s over half a kilometre of cable. The unit is plugged into a cable run just before the printer, where it obtains its 2mA of supply current from the PC and printer. End Design Ltd, 0372 458080.

Low-cost H-P T&M. Hewlett-Packard has four new instruments in its low-cost range. Benchlink software allows the import of test data to a PC. *HP33120A* is a direct digital synthesised function generator producing standard or arbitrary waveforms to 12-bit resolution and with linear/log. sweep. *HP54610A* is a 500MHz oscilloscope with very accurate measurement and 1ns/division sweep rate. And the 35W *HPE3630A* triple-output power supply provides 0-6V at 1-2.5A and 0 to ±20V at 0.5A. Hewlett-Packard Ltd, 0344 362867.

EMC kit. Martron's EMC laboratory kit allows all electromagnetic compatibility and radio-frequency interference tests required by current and future EC legislation. The kit costs around £12 000 and covers both conducted and radiated emissions to CISPR over the 9kHz-1GHz frequency range. A PC-based software program produces a representation on screen of results and a hard-copy report. Martron Instruments Ltd. 0494 459200.

20MHz function generators. Three programmable function generators by Thurlby Thandar cover the 2mHz-20MHz frequency range to an accuracy within 0.1%. Model *8020* generates sine, triangle and symmetrical square waves, symmetrical pulses and DC, also including eight log/lin sweep modes, VCO, gating and triggering pulses. *8021* offers the same, but with six controllable pulse and two ramp modes. *8022* provides all that plus AM and carrier control. Thurlby Thandar Instruments, 0480 412451.

Multimeter with PC interface. Thurlby Thandar's *1906* benchtop digital multimeter is a 5.5-digit auto/manual ranging instrument that connects directly to the serial port of a PC, which controls function, range and configuration, reading results individually or in blocks. Up to 32 instruments can be controlled in this way, using the RS232 interface in addressable mode. The meter will perform linear scaling with offset, percentage deviation, limits comparison, min/max storage and data logging. Thurlby Thandar Instruments, 0480 412451.

Interfaces

Card readers. New versions of MR Sensors's magnetic card readers incorporate serial outputs and come in RS232, RS422 or RS485 versions. Since all is contained within the reader housing, no external interface is needed. Magnetoresistive techniques make for increased reliability and other features include selectable baud rate, handshake and parity and high/low level coercivity compatibility. MR Sensors Ltd. 0222 520022.

Talking modem. Mutek designs and makes the *DiSPatch* digital signal processor-based modem, a technique that, being software-based, allows simple addition of features by means of a rom exchange. It also enables the use of voice synthesis. The unit meets V42, V42bis, V32bis and G3 fax specifications and the relevant lower-speed function with sync. and async. input. Mutek Data Communications Ltd, 0225 866502.

PCMCIA interface kit. To connect laptop PCs to GPIB instruments, National Instruments has introduced an IEEE488 interface for the PCMCIA bus, including the PCMCIA-GPIB plug-in board, NI's *NI-488.2* for dos and Windows software and a GPIB-terminated 2m cable. National Instruments UK, 0635 523545.

Literature

Test & measurement catalogue. Fluke's 1994 catalogue is now available, covering a range of test and measurement equipment from basic multimeters to data acquisition systems. This is the first Fluke catalogue since the firm's acquisition of the Philips T&M operation. It is obtainable free. Fluke (UK) Ltd, 0923 240511.

Cambion guide. Interconnection Products has produced a guide to its wide range of Cambion electromechanical and magnetic product, which includes lists of product literature and quality approvals. Interconnection Products Ltd, 0433 621555.

Materials

Conductive paints. Enco has introduced a method of spray masking for the spraying of conductive paint, spraying being necessary for the paint to keep its properties. Instead of labour-intensive masking tape or precision hard masks, Enco's masks are CNC machined plastic inserts, economic up to 600 units per day, and the method is said to be one-third as expensive as hard tooling. Enco Industries Ltd, 05057 5151.

Power supplies

DC-to-DC converters. Ericsson announces the *PKF-MacroDens* series of 3-7W DC-to-DC converters usable as SM or through-hole components for automatic insertion. Isolation is 1.5kV and the devices may be paralleled. They are provided with output voltage adjustment and low-input turn-off for battery protection; outputs are from 2V/3W to 12V/7W. Ericsson Components AB, 0793 488300.

40W DC-DC converter. Ericsson's *PKE* series of low-profile DC-to-DC

power modules now includes the *PKE 4431 PI*, which measures 76mm square and 10.7mm high, while providing 40W in three outputs: 5V and ±12V. Input voltage range is 38-72V DC and efficiency is around 83%. There is under-voltage lockout and remote on/off switching. Ericsson Components AB, 0793 488300.

Radio communications products

Feedforward amplifiers. RF amplifiers from Pacific Amplifier are now available here in a range of broad-band, high-power amplifiers covering 0.1-2000MHz. Examples are a 400W design working at VHF for medical use and a 150-1200MHz, 50W type working in Class A with a flatness of ±1dB over the band, a 47dB gain and harmonics of less than −20dB. A recent model is microprocessor-controlled at 850MHz and −60dBc intermodulation at 80W. Anglia Microwaves Ltd, 0277 630000.

18GHz dividers/combiners. Two-way, stripline, in-phase power dividers in octave and multi-octave bandwidths to 18GHz are announced by KDI Electronics. The *YL* and *D300* series use a ceramic pad as the internal resistive element, handling 1W CW and 1kW peak powers. Isolation is 20dB and connectors

IR thermometers. Six instruments in Digitron's D200 range of infrared thermometers exhibit accuracies of ±1% of reading ±1°C over the −20 to 250°C temperature range. The seventh is a high-accuracy type, offering 0.1° resolution to an accuracy of ±1°C from −20 to 70°C. A new feature on these low-cost units is adjustable emissivity for direct setting or to obtain the emissivity of a material of known temperature. Digitron Instrumentation Ltd, 0992 587441.

include SMA, N or TNC types. Three, four, eight and sixteen-way models are available. Anglia Microwaves Ltd, 0277 630000.

UHF bandsplitter. Diplexer *Type 2800-660* splits or combines the lower and upper halves of the UHF band (4700-890MHz) to connect two UHF antennas to a single transmission line or to allow two low-power transmitters to use the same antenna. Crossover frequency is 630MHz and passbands, on separate connectors, are 470-600MHz and 660-890MHz, passband loss being 1dB maximum. Power rating is 5W. Communications & Energy Corp., (US)(315) 452-0709.

Please quote "Electronics World + Wireless World" when seeking further information

GPS IC set. GEC Plessey's three-piece chipset for GPS consists of the *GP1010* front end, the *GP1020* correlator and a *DW9230* saw filter, which works with both the GPS Coarse/Acquisition code or Glonass signal. *GP1010* is a silicon device in the company's 15GHz bipolar process, converting the L1-band spread-spectrum signal to two-bit digital data for correlation in *GP1020*. This is a six-channel, 1μm cmos gate array, using code from six satellites to calculate three-dimensional position to within 100m. GEC Plessey Semiconductors, 0793 518510.

GPS receiver. Rockwell's *NavCard* is a Global Position System receiver on a PCMCIA Type II card, with an average power consumption of 750mW. An integrated, removable antenna is provided, with external antenna kits available. The card provides a time-to-first-fix of 20-30 seconds and dynamic tracking, even in foliage and an urban environment and in the presence of vibration and shock. Rockwell International, 010 33 93 00 33 01.

Scanning telemetry. Designed solely for telemetry and thereby avoiding problems associated with voice radios adapted to telemetry, Wood & Douglas's *MPT1411 ScanLink* consists of a duplex base station, semi-duplex outstation and a monitor, providing scanning telemetry to public utilities. Outstations operate in semi-duplex, with receive and transmit separated by 5.5MHz, one version operating at 10W and the second at 500mW. Switching time is better than 10ms. Wood & Douglas Ltd, 0734 811444.

Switches and relays

HV relays. FR has a new series of high-voltage relays that handle stand-off voltages up to 10kV DC (7kV AC), with over 15kV DC isolation between coil and contacts. First model is in Form A and will shortly be followed by a Form B and a flying-lead version. FR Electronics, 0202 897969.

Optical relays. Having four relays in one sil package, Matsushita's *AQX photoMOS* device can be used as either four independent relays, each with its own input and normally open output or as a single input with four independent outputs. Each output carries up to 80mA at 400V AC or DC, with negligible output offset. Isolation is 1500V. Matsushita Automation Controls, 0908 231555.

Immersible microswitch. Matsushita's new microswitch conforms to IP67 for waterproofing and to IP50 against dust. An ultrasonic swaging process seals the rubber seal round the mechanism and the terminals are sealed by potting the base in epoxy resin. Capability is 3A at 250V AC or 1mA at 24V DC. Pin plunger, hinge lever or roller lever types are available and the smallest switch measures 12.8mm by 6mm by 6.5mm. Matsushita Automation Controls 0908 231555.

Transducers and sensors

Pressure transducer. The *Sensit P-192* pressure transducer is compatible with wet and corrosive substances by virtue of its construction, in which the bridge is fused into the rear face of an alumina diaphragm, which in turn is assembled into a brass housing carrying a male thread pressure port. Spans are in the 10-40bar range, with a twice-span overload without calibration. Burst pressure tolerance is four times span. Errors from all causes lie within 1% and are typically below 0.15%. Eurosensor, 071-405 6060.

Audio signaller. Producing a sound level of 75dBa at two feet, the Mallory Sonalert II measures only 23mm in diameter and 9mm in height. It operates at 3-20V DC, drawing 1-12mA, and produces a 3.4kHz signal. It is surface-mounted and an octagonal version is made for use with insertion equipment. Highland Electronics Ltd, 0444 236000.

COMPUTER

Computer board level products

PC A-to-D. Made by Amplicon Liveline, the *PC26AT* is a 16-channel, 12-bit analogue-to-digital converter add-on board for PCs that has a crystal oscillator to drive the three 16-bit counter timers, offering a DMA capability of 90kHz throughout. Conversion time of the successive-approximation device is 10μs and it can operate in unipolar mode with full scale of 3V-10V, or in bipolar mode from ±1.5V to ±10V. Demo software is written in *QuickBasic, Microsoft C, Turbo C* and *Turbo Pascal.* Amplicon Liveline Ltd, (Free)0800 525335.

12MHz DDS. The model *DDS3* PC 12MHz direct digital synthesiser on a PC card provides 5ppm accuracy, 10ppm/year stability and good spectral purity while generating sine and TTL/cmos clock signals simultaneously from 2Hz to 12MHz in 2Hz steps. Phase noise is less than –90dBc at 1kHz offset from carrier, spurious signals are below –45dBc and harmonics below –40dBc. The card comes with a C program running under dos. Novatech Instruments Inc., (US) 206 328 6902.

MPEG decoder card. Polar offer a PC card performing real-time MPEG decoding for video-by-wire and conferencing systems, claimed by the company to be the first in the field. It gives full audio and video decoding at resolutions of 720 by 376 at 25Hz or 720 by 480 at 30Hz. Decompressed video can be seen in a screen window, depending on system configuration. Polar Electronics Ltd, 0525 377093.

Image acquisition. *VideoWizard* is a low-cost image acquisition system for Windows that includes the VVL miniature *Peach* camera, tripod, mono framegrabber card and *PhotoFinish* software. The camera takes power from the PC. The six image formats include .TIF, .PCX and .BMP. Total cost is £285. VLSI Vision Ltd, 031-539 7111.

Development and evaluation

Windows FPGA design. Data I/O's *Synario* is a Windows-based FPGA design system to ease the transition from PLDs to FPGAs and to allow FPGA designers to work with multiple architectures. It allows the creation, simulation and verification of designs, independently of architecture, so that the best architecture for a given application may be selected. Since it runs under Windows, users can move between applications through a standard interface. Data I/O Ltd, 0734 440011.

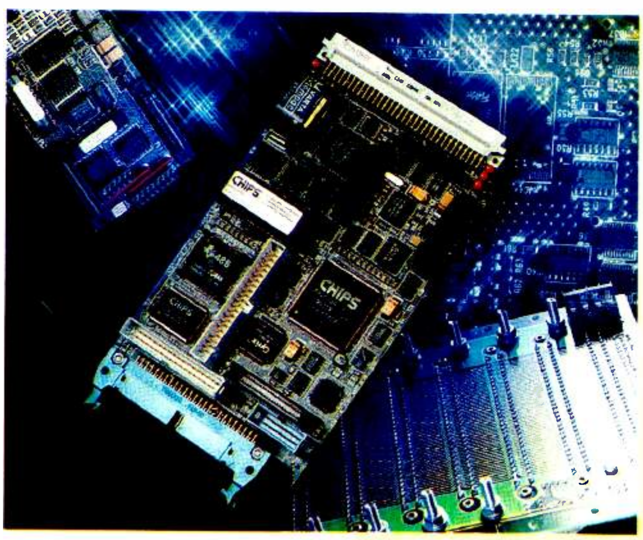
Return of the Stag. Stag ended production of the *SE100T* eprom eraser recently and stopped advertising it two years ago, but continuing demand has forced the company to restart manufacture. The UV instrument erases up to 104 24-pin devices at a time, a 60-minute timer and full safety interlocks being provided. Stag Programmers Ltd, 0707 332148.

Software

LabWindows/CVI. National has the new *LabWindows/CVI*, which is software running under Windows for developing virtual instruments using the C programming language. It expands on *LabWindows* for dos, which uses C and Basic. *LabWindows/CVI* is a 32-bit, multiplatform environment including all tools for C-compatible test, measurement and control applications on a PC or as *X* Window systems for *Unix SPARCstations.* Dos-based *Labwindows* applications run in */CVI.* National Instruments UK, 0635 523545.

Windows neural network. A new version of the *NeuDesk* Windows-based neural-network PC package is a low-cost means of evaluating the networks by means of an intuitive GUI, with the option of embedding programs so created in other Windows applications. Version 2.11 handles larger problems to greater accuracy and two optional algorithms optimise networks for classes of problem such as forecasting and classifying data. Neural Computer Sciences, 0703 667775.

PC STEbus board. Arcom has the *SCIM-X STEbus* board for embedded dos/Windows applications, using a *486SLC* CPU with over 10Mbyte of ram and flash eprom. It integrates the hardware of three *STEbus* modules. There is ample expansion facility, including enough ram to run systems such as *Unix*, and the display can take several forms, the drive being a plug-in module. Software can be developed on-board, since it is PC-compatible, and software is provided to blow the result into rom-disk or ram-disk for use in hostile conditions. Arcom Control Systems Ltd, 0223 411200.



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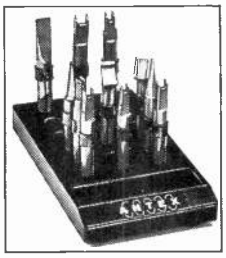

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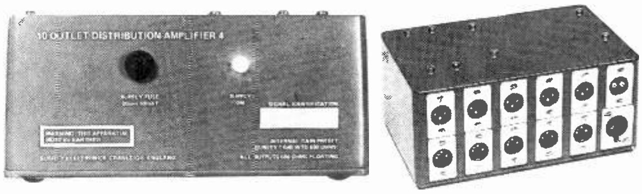

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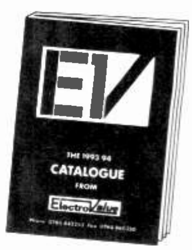

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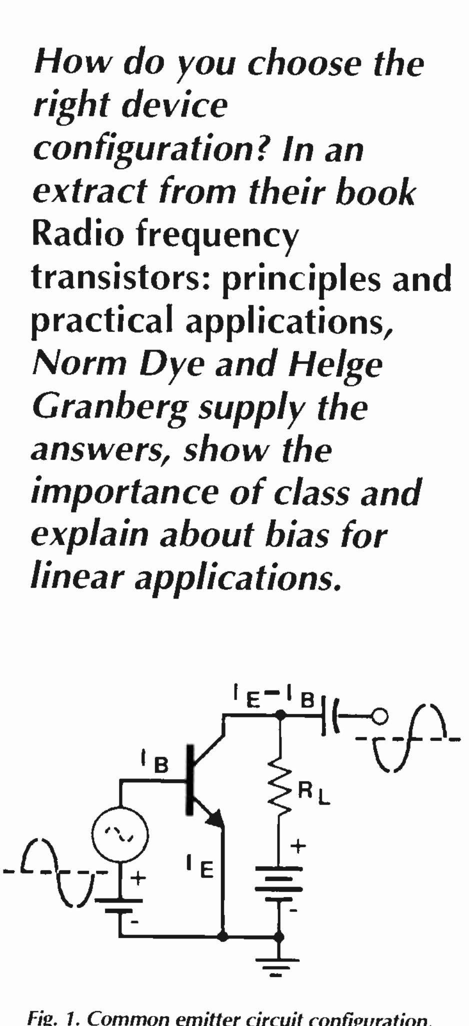


Fig. 1. Common emitter circuit configuration, the only one with phase reversal between input and output.

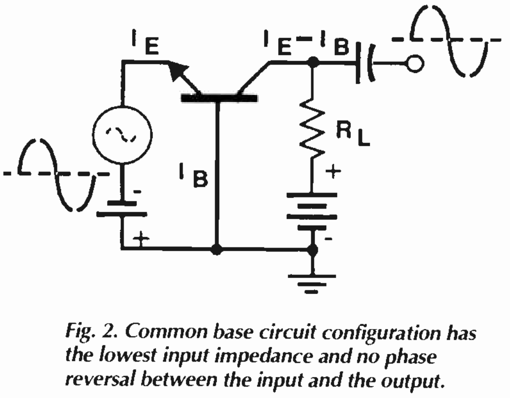


Fig. 2. Common base circuit configuration has the lowest input impedance and no phase reversal between the input and the output.

Common emitter and common source circuit configurations are some of the most widely used because of their stability, good linearity and high power gain up to uhf. They are also the only configurations where input and output are out of phase, enhancing their stability – except for the half f_0 mode and at frequencies where the feedback capacitance delays are close to 180°.

But if the common emitter or source inductance is increased, the power gain will drop due to the negative feedback generated by the reactance. So for proper operation the common element inductance must be kept as low as physically possible.

Gain is inversely proportional to the frequency and increases approximately 5dB per octave until the β cutoff is reached. At this point it may be as high as 30-40dB.

A common emitter circuit (**Fig. 1**) can be directly adapted to mosfets, but in that case since $I_B = 0$, $I_D = I_E$. Lumped-constant matching elements are practical in narrow band circuits up to vhf. But at over 300-400MHz, microstrip techniques – or a combination of microstrip and transformer impedance matching techniques – are normally used.

For broadband performance, the initially-higher device impedance levels make impedance matching easier to implement to a 50Ω interface with a push-pull configuration. In multi-stage systems the interstage impedance matching is usually carried out at lower than 50Ω levels, and in some instances very little impedance transformation is required. The result may be better broadband performance than with 50Ω interfaces between each stage, but it does not have the advantage that each stage can be individually tested in a standard 50Ω set-up.

Up to vhf and low uhf, input impedance of a mosfet is high compared to that of a bjt but at higher frequencies they reach similar values, and the matching procedures become almost identical.

In practice, virtually all multi-octave amplifier designs independent of frequency spectrum and device type are push-pull. Another advantage is that the power levels of two devices are automatically combined for higher power output levels. So electrically-smaller individual devices can be used for a given power output.

RF power transistors housed in push-pull headers have been available since the mid-1970s. But it was the development of high frequency fets that really made the push-pull package so popular. Now fets and bjts are both available in push-pull headers, most as the "Gemini" type where two individual and independent transistors are mounted on a common flange next to each other. Gemini packages are manufactured in several physical sizes, the largest being able to dissipate up to 500-600W. A big attraction of the push-pull transistor – whether in a single push-pull header or in a Gemini package – is the close electrical proximity of the two dice. Device performance of a push-pull circuit is greatly enhanced as a result, where the important factor is a low emitter-to-emitter (source-to-source) inductance and not the emitter-to-ground inductance.

In all Gemini housed devices, the emitter (or source) is connected to the mounting flange – the electrical dc ground.

No significant difference in efficiency is apparent between amplifiers using either fets or bipolars. The higher saturation voltage of fets probably make them less efficient but this may be true only at low operating voltages (12V and lower).

At higher frequencies, device output capacitance has a much larger effect on efficiency, though part of it can be tuned out in narrow band circuits.

Common base and common gate

At uhf and microwave frequencies, common base circuits with bjts are widely used because their α cut-off is higher than the β cut-off. Higher power gains are possible than with the common emitter configuration.

If base-to-ground inductance is added, power gain of a common base amplifier increases where positive feedback is generated. Add more inductance and the gain will increase to a point of instability, finally leading to steady oscillation – usually at a frequency where the matching networks resonate.

All common base transistors have some positive feedback, generated by the inductances of the base bonding wires and the internal part of the base lead. But this inductance is generally low enough not to generate sufficient positive feedback to create instability.

As in the common emitter circuit, a common base transistor's gain is inversely proportional to its frequency of operation. The slope is also the same, approximately 5dB/octave, but only up to the α cut-off. Below α cut-off, the gain flattens out to 12-15dB and remains at that level down to dc.

Input power need not be fed through in a common base amplifier circuit, so the power output is actual and not $P_{in} + P_{out}$ as in a common emitter amplifier. The effect is that device ruggedness (ability to withstand load mismatches) is probably improved through reduced dissipation.

In a common base circuit (**Fig. 2**), the total current flows through the emitter, so the input matching network, or an emitter dc return choke, must be able to carry $I_B + I_C$. The normal output capacitance (C_{ob}) and feedback capacitance (C_{rb}) are reversed. Fortunately, except at low bias voltages where C_{rb} can be several times higher than C_{ob}, their values are about equal.

Under normal drive conditions there should be little difference in output capacitance or impedance between common emitter and common base circuits. But the highly non-linear C_{rb} reportedly creates increased tendencies for the well known half f_0 phenomenon.

Common gate and base

Mosfets, operated as a common gate amplifier, create a totally different situation. Their feedback capacitance (C_{rss}) has a value many times lower than the output capacitance (C_{oss}). When these are reversed, the actual feedback capacitance goes high with respect to the input and output capacitances, creating an unstable condition.

Even if the common gate inductance can be minimised, stability may not be achievable. The input impedance is lower than in a common source circuit because of the high value of feedback capacitance enhanced by the Miller effect.

Stable single-frequency or narrow-band circuits with fractional octave bandwidths are possible using the common base configuration. But wide-band circuits are difficult to design if internal matching is required.

Neutralisation can improve stability in some cases, though it is not easy to implement except in push-pull designs. In high power circuits, biasing to a linear mode is difficult as an opposite polarity supply is required at the emitter. There is also a rectification effect which tends to reduce the bias voltage with rf drive.

In small signal circuits, where the class of operation is mostly class A, some bypassed base-to-ground resistance can be used to generate a self bias.

Push-pull common base circuits are not normally seen at higher power levels, at high uhf or higher frequencies. One reason may be that the 180° phase shift is difficult to achieve and hold except for very narrow band widths.

But push-pull common base circuits are widely employed at power levels up to 0.5-1W in applications such as cable tv amplifiers, where an un-bypassed common base resistance can be used for self biasing to a linear mode of operation.

For each configuration – common emitter and common base – push-pull offers the same advantages, the most important of which is the non-critical base or emitter common mode inductance.

Power gain and stability of the push-pull circuit depends to a large extent on base-to-base inductance. Mosfets must always be biased to a level close to or greater than the gate threshold voltage to overcome $V_g(th)$ with rf input drive (excluding class D and other switch-mode systems). The bias source must be able to carry the full drain current: at a gate threshold voltage of 4-5V this would amount to considerable dissipation. But with bjts the voltage is only 0.6-0.7V and so much more tolerable.

Common gate mosfet circuits are most useful in relatively low power applications, in circuits where neutralisation can be easily realised and their high agc range (power gain/gate voltage) is an advantage.

Disadvantages of the common base amplifier circuit include the need for two dc power supplies for classes A, AB and B; poor linearity due to regeneration; low input impedance; no possibility to implement negative feedback (except in push-pull), and high susceptibility to half f_0 instability.

Common collector

Common collector, emitter follower circuits (**Fig. 3**) are widely used for high input and low output impedance levels.

As in a common base configuration, there is no phase reversal between input and output. The emitter follower has a voltage gain of less than unity, and amplification is obtained from the current gain through impedance transformation. Output impedance is directly related to the input impedance divided by current gain (h_{FE}). Conversely, input impedance equals the output load multiplied by h_{FE}.

The circuit is less suitable for rf power amplifiers than the two other configurations since variations in load impedance are directly reflected back to the input. So its widest use is as a wideband buffer amplifier, driving low impedance or capacitive loads.

In fact, the circuit offers one of the best drivers for capacitive loads – especially in a complementary configuration providing active "pull-up" and "pull-down" in the output. Applications include crt video drivers and mosfet gate drivers in class D/E amplifier systems.

Common drain

In bipolar circuits, the emitter follower is represented by a common drain or source follower circuit configuration. As before, input impedance is high and output impedance low.

Compared to common source and common gate circuits, input capacitance, drain-to-gate, is low – considerably lower for the fet (because of absence of the forward biased collector-base diode junction) than for a bipolar of comparable electrical size. A source follower also has a voltage gain of less than unity, and since it is not a current amplifier, discussion of current gain is not appropriate.

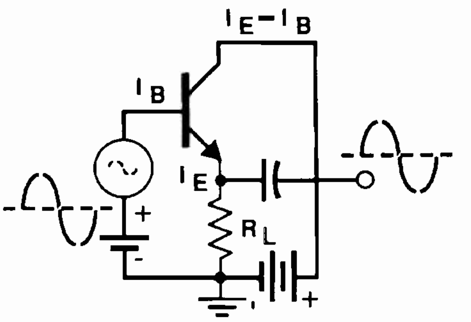


Fig. 3. The common collector circuit configuration has the highest input impedance and lowest output impedance. No phase reversal exists between input and output.

But amplification takes place through impedance transformation as is the case in a bipolar circuit.

Extremely high input impedance, more variable with frequency than in common source and common gate circuits, means heavy resistive loading at the gate must be used for any broadband application. Negative feedback is not needed, nor is it easy to implement due to equal phase of the input and output.

For these reasons, common source circuits exhibit exceptional stability. But excessive stray inductances in the circuit lay-out can lead to low frequency oscillations.

Unlike the emitter follower, variations in load impedance are not reflected to the input, making the source follower suitable for rf power amplifier applications – at least up to vhf.

Push-pull broadband circuits for 2-50MHz have been designed for 200-300W power levels, having inherent good linearity, stability and gain flatness without levelling networks.

High power linear amplifiers are probably the most suitable application for this mode of operation. The agc range is comparable to that in common source, but a higher voltage swing is required.

One problem to watch for is that during high voltage operation, gate rupture voltage can easily be exceeded, since during the negative half cycle of the input signal the gate voltage can approach the level of V_{DS}.

Biasing to linear operation

All solid-state devices and vacuum tubes intended for linear operation must have a certain amount of "forward bias" dc idle current to place their operating points in the linear region of the transfer curve (**Fig. 4**).

Perfect linearity means that power output follows the power input in a linear fashion: a P_{in} of 1W produces a P_{out} of 10W, 2W results in a P_{out} of 20W etc.

It can also mean that the power gain must be constant from almost zero to the maximum P_{out} level. This can also be expressed as gain compression in dB, or as the third order intercept point as widely used in low power and catv applications.

In large signal voice communication, linearity is usually measured as intermodulation

Performance of an amplifier depends on how it is biased.

Low power transistors are characterised as class A and many high power amplifiers are characterised as class C. Any user of rf transistors must understand these classes and their significance in determining amplifier characteristics and choice of transistors for a specific application.

Each of the basic classes of operation is limited to a specified portion of the input signal when current flows in the amplifying device. The class definitions apply regardless whether the amplifier is a vacuum tube or a transistor; or whether it is a bipolar transistor or a fet.

For example, Class A requires that current flows for all 360° (all the time) of the input signal which is assumed to be in the form of a sine wave. Likewise, class C requires current to flow for less than half the time, or less than 180° (Table 1).

Class D amplifiers split into two basic types: the current switching amplifier, driven by a square wave signal; and the voltage switching amplifier, driven by either a square wave or the more common sine wave input. With sine wave drive, the gate voltage swing must be large enough to ensure complete saturation and cut-off of the fet.

Input and output waveforms are approximately identical except that the current and voltage waveforms are reversed.

Demanding applications are better suited by the current switching class D amplifier, since its duty cycle is easily defined and is not affected by amplitude of input drive.

Table 1. Maximum theoretical efficiencies for basic classes of amplifier operation.

Class	Configuration	Efficiency %	Comments
A	all	50	
B	all	78.5	
AB	all	50-78.5	depending on angle of conduction
C	non-saturating	85-90	depending on angle of conduction
D	all	100	assumes infinite switching speed
E	–	100	assumes no overlap for the output rf currents and voltages

Class E is a variation of class D with an *LC* network added to the output. It compensates for part of the fet's output capacitance and helps to reduce overlap between the switching currents and voltages – boosting efficiency.

The improvement can be around 5-10%. But the system is relatively narrow band due to the *LC* network, whereas plain class D can operate at bandwidths of several octaves.

Output power of Class D/E amplifiers is limited by mosfet switching speeds and by the capacitive loads presented to driver stages.

Class questions

A logical question would be: "Can class A characterised transistors be used as class C amplifiers?". The obvious answer is yes. Similarly class C characterised transistors can be used in class A amplifiers – provided certain conditions are met. The condition involves a "derating" of the class C transistor to a lower power level, with the amount of derating depending on the class of operation.

If a class C transistor is used in a truly linear class A amplifier, it should be derated by a factor of four. So if it can deliver, say, 60W class C, it should not be used class A at level greater than 15W.

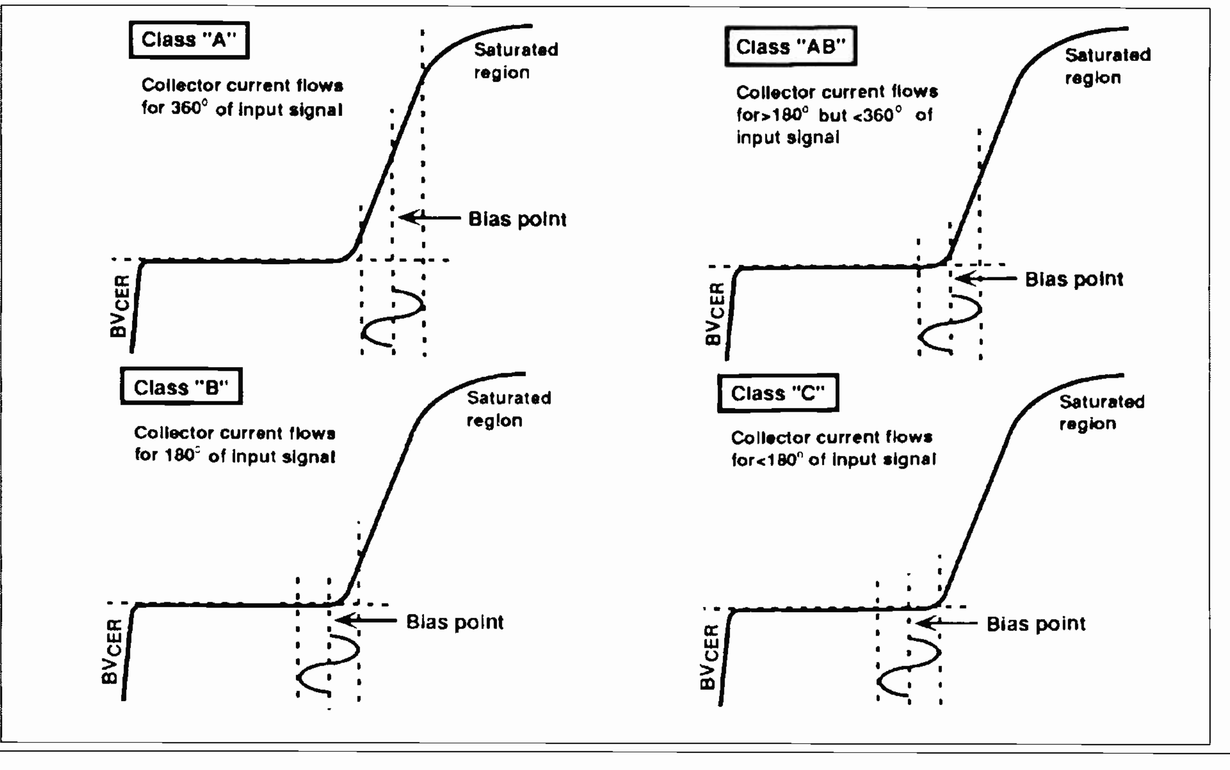
Class AB use requires a safe derating factor of three.

Two factors make these deratings necessary for use in a more linear mode.

First, linear classes of operation require bias. Not uncommonly, a Class AB high power transistor will be biased at several amperes of current, resulting in a large amount of power dissipated in the device.

Second, efficiency of the more-linear forms of amplification decreases as linearity increases. So for the same amount of output power, the power dissipated in the transistor will increase.

Dissipated power raises the die temperature of a device, for a given heat sink temperature, and for silicon devices this should not exceed 200°C.



distortion (imd) using two test frequencies (tones) spaced lkHz apart as a standard.

Testing amplifying devices for linear use in television, requires two or three test frequencies to be employed (depending on the specifications) with their spacings in the MHz range.

Three test frequencies (triple beat) are common with low power device specifications and are standard in catv device testing, where distortion levels are very low. A wider spectrum can be analysed as a result, which better simulates multichannel systems.

Distortion expressed as imd – because it is easier to relate to actual numbers – is the method by which linearity is initially measured, and can be converted to third order intercept. The test frequencies are viewed on a spectrum analyser screen and the distortion products (third, fifth, seventh order, etc.) appear on each side of the test tones. Their amplitudes can be read directly and are expressed either in dB below one of the tones (Mil Std) or below the peak power (EIA standard). Numerous ways can be used to generate the test tones.

Conversion to third order intercept can be done by

$$IP^3 = P_{out} + \text{imd}/2$$

where IP^3 = third order intercept point, P_{out} = power output (one tone, dBm), imd = third order intermodulation distortion below one tone (dB).

Reversing the equation gives imd = $2(IP^3 - P_{out})$. For example, if an amplifier has an IP^3 of +20dBm and the P_{out} = +5dBm/tone, the third order imd is 2[20–(+5)] which is 30dB below one of the +5dBm tones.

Either the power input or the power output can be used for the power reference. In circuits having an insertion loss, such as mixers, the P_{in} is generally used as a reference. P_{out} is preferred in circuits with power gain due to a smaller factor of possible error.

Bipolar devices require a constant voltage source, whereas mosfets can be biased with simple resistor divider networks. But both become more complex where temperature stability is required.

In addition, enhancement-mode mosfets always need some gate bias voltage to overcome the gate threshold. Exceptions are mosfets operated in class D or in other switch-mode classes.

Apart from those applications already discussed that call for amplifier linearity, examples include all amplitude-modulated systems for communications and broadcast, nuclear magnetic resonance, magnetic resonance imaging, digital cellular telephone, and signal sources for instrumentation.

One of the requirements for transistor linearity is the flatness of f_T (gain-bandwidth product) vs I_c (collector current). Variation in collector current results in a change of f_T, and so a variation in power gain.

The low I_c area (**Fig. 5**) is not very critical and produces only cross-over distortion, which in most cases can be reduced by increasing the bias idle current. If the "knee" from zero current to maximum f_T is sharp, a smaller amount of bias or idle current is required.

Mosfets will produce a similar f_T vs I_D curve, except that their low current knee is not as sharp as that of a bjt, explaining their need for higher bias idle currents.

The input signal can drive the transistor to peak current levels significantly above the bias current. So the slope of the f_T curve, from the bias current level to the maximum current caused by the input signal, determines the transistor's linearity performance at high current.

Some reduction with increasing current is tolerable without noticeable non-linearities, Fig. 5. Excessive downward sloping however would cause early saturation of the amplifier and flat topping of the output modulation peaks.

Finally, measurements of f_T vs I_c are usually carried out under pulse conditions, which excludes thermal effects. Thus the f_T vs I_c curve shows less sloping down than will be experienced in actual use of the transistor. ■

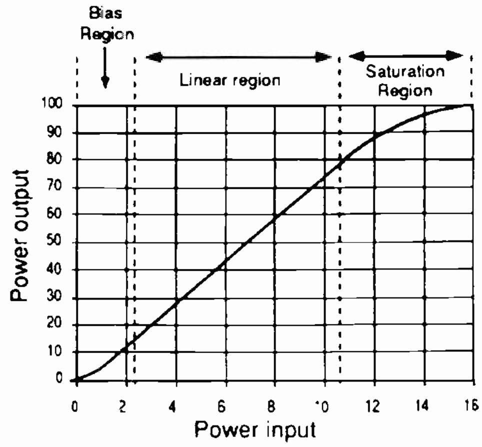


Fig. 4. Typical input-output transfer curve of a solid-state amplifier. Non-linearity can be seen in the bias region. The purpose of the forward bias is to move the operating point to the linear portion of the curve.

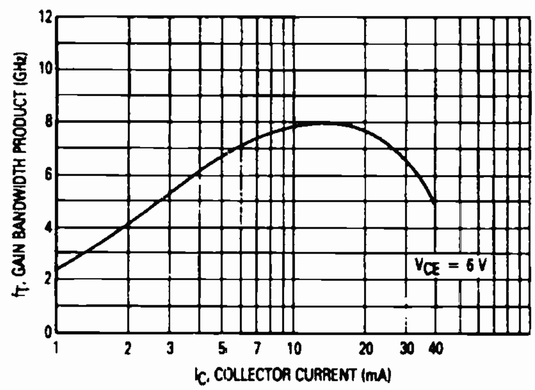


Fig. 5. Gain-bandwidth product vs collector current.

Norm Dye is Motorola's product planning manager in the Semiconductor Products Sector, and Helge Granberg is Member of Technical Staff, Radio Frequency Power Group (Semiconductor Products) at Motorola. Their rf transistors book includes practical examples from the frequency spectrum from 2MHz to microwaves, with special emphasis on the UHF frequencies .

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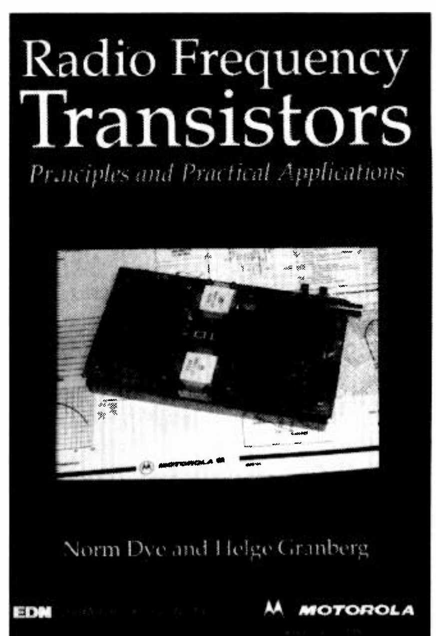

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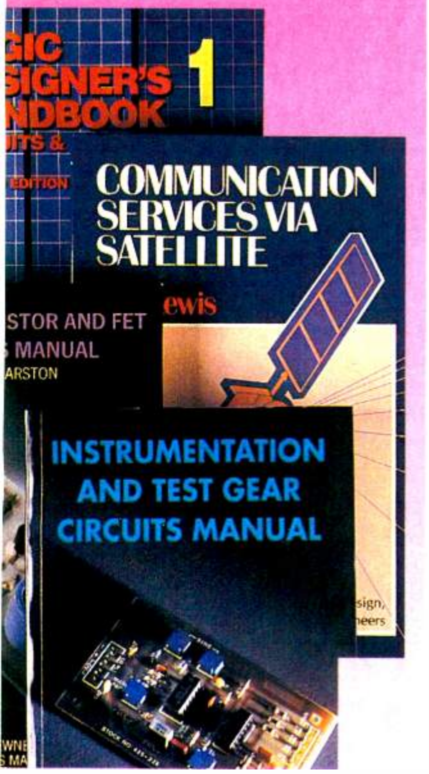

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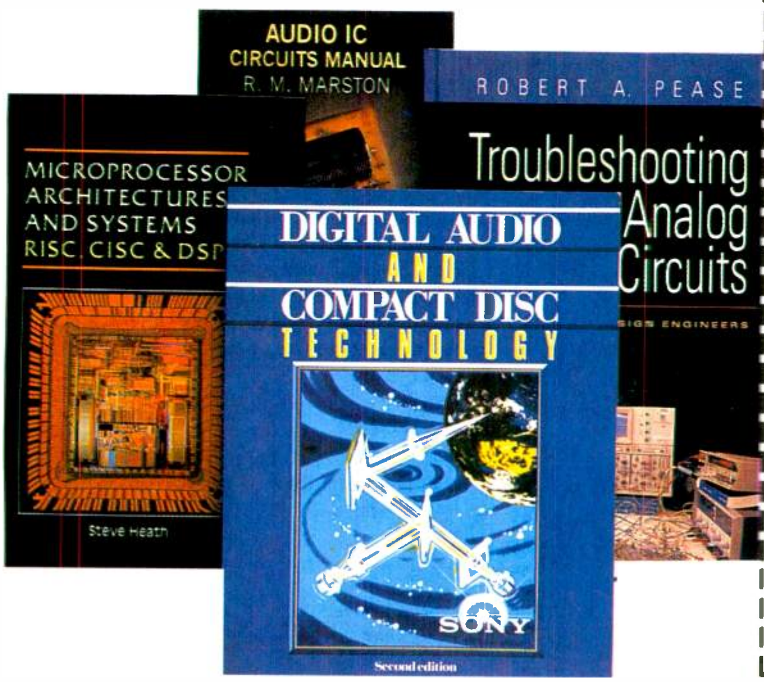

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Making a linear difference to square law fets

Michael Williams shows how the familiar "difference of two squares" could produce a linear output from a pair of fets, forming the basis for a perfect linear amplifier

Plot a graph of output volts versus input volts for an amplifier and the result will be a simple straight line through the origin – up to certain limits anyway. The implication is that the various devices in the amplifier must also have linear characteristics. Certainly some – resistors and capacitors for example – can be very linear and were once thought inherently perfect. Thermionic valve characteristics can also be pretty linear. But fets have a square law characteristic. My contention is that by using the familiar "difference of two squares" (D2S), a linear output could be produced. The law seems to offer the prospect of a perfect linear amplifier from devices with a perfect square law.

I have always been surprised to find that though books quote the square law formula – even give mathematical proofs of it – nobody actually offers any hard evidence for it. Graphs might be drawn, but only to illustrate the formula, which seems to be untested.

Finding matched pairs

While lecturing at the (then) Middlesex Polytechnic, I decided to test some devices, so set up a laboratory experiment for first year BEng electronics students. Their task was stated roughly as follows:

> "The FET is said to follow the law $I_o(1 - V/V_p)^2$ where I is the drain current through the fet. V is the input gate voltage and V_p (the "pinch-off voltage") is a value of V which just cuts off the current. Investigate how valid this is for your fet."

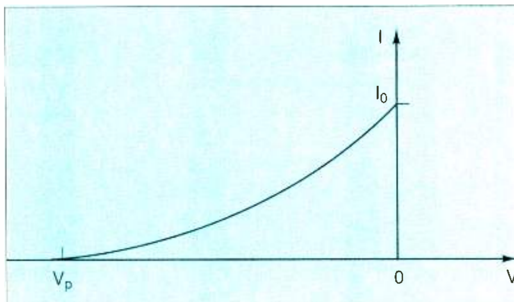

Fig. 1. Ideal fet square-law transfer characteristic: but does it exist in practice?

A graph of this form, **Fig. 1**, has an output current of I_o when input V is zero, falling smoothly to zero as V approaches V_p – negative for our students' fets – but the principles apply to all types.

Year after year, the exercise revealed that some fets had a characteristic very close to the square law over the whole range between pinch-off and zero bias: but many did not. Of these, most had a square law for higher currents, but the pinch-off region extended to the left more than expected from extrapolation from the upper part of the graph. Some graphs were well behaved at low currents, but then mysteriously reached a limit as they got near the vertical axis.

In addition to these deviations from the square law, fets are very variable devices – even two square law characteristics may be perfect but different. To find matched pairs of fets with perfect square law characteristics, implies mass testing and recording. So for many years I set the design of a square law tester as a project for all second-year BEng students. They found it extremely difficult. It took at least six weeks of team effort before anyone could even say roughly what the problem was. Working solutions were rare. Design is a lot harder than people think, especially of a new kind of device.

Effort repaid?

Is all the trouble worth the effort? To answer that, let us look at the way the two characteristics combine, and then at applications.

Square history

About three decades ago, I was working in a team researching superconductors. We were using a magnetoresistor to measure magnetic fields at low temperatures, and were grumbling about its non-linear characteristic; its square law behaviour, in fact.

But a colleague surprised us all by suggesting: "Why not use two?" He was referring to the standard mathematical method where a difference of two squares gives a linear characteristic. We were all baffled, not to say humiliated by the simple algebra: $(x + y)^2 - (x - y)^2 = 4xy$. Just fix x, and the difference is linear in *y*.

Examination of the formula for the difference of two squares – call it D2S for short – clarifies the technical problem: if we could apply opposite fixed bias fields to two magnetoresistors in the field to be measured, we should get a straight line graph of reading versus field. Well, we couldn't, so we didn't.

Nevertheless, the principle was intriguing though no application of D2S ever came up in my research days. But the strangest thing is that I have never found anybody (original proposer apart) who had heard of the "standard" D2S principle.

D2S at a glance

Write out a row of consecutive digits, and square the row. Then repeat this row of squares but displace it to one side by any amount. The differences between the latter rows form a linear sequence. For example:

−6	−5	−4	−3	−2	−1	0	+1	+2	+3	+4	+5	+6
36	25	16	9	4	1	0	1	4	9	16	25	36
25	16	9	4	1	0	1	4	9	16	25	36	49
11	9	7	5	3	1	−1	−3	−5	−7	−9	−11	−13

Results can be displayed graphically – just plot squares against the original numbers – and it does not have to be limited to integers. It works for all displacements. Just take the difference of offset identical-square-law graphs – and a linear graph results.

Take a simple circuit (**Fig. 2**) of a matched pair of fets with a positive bias V_b on their (joined) sources, and equal and opposite signals fed to their two gates. Push-pull triodes are hardly a novelty, but there is something new in this approach.

Bias V_b pushes the transfer characteristic $I_1(V_1)$ sideways (**Fig. 3**). Note that V_1 is the gate potential (ie pd from ground), whereas the resultant input to the fet is the potential difference between the gate and the positively biased source. (We could have used negative gate bias instead of positive source bias.)

This displaced characteristic can be written algebraically as:

$$I_1 = (I_0/V_p^2)\{V_1 - (V_p + V_b)\}^2$$

Amplification is proportional to the slope at the working point (V_1), ie to the mutual conductance, g_m and

$$g_m = dI_1/dV_1 = (2I_0/Vp^2)\{V_1 - (V_p + V_b)\}$$

This varies with bias and also with signal V_1, so V_1 has to be kept very small if g_m is not to change with signal change.

The characteristic $I_2(V_2)$ of the second fet is the same as the first, $I_1(V_1)$. But, to display the two currents and their differences together, they must all be plotted against V_1. $V_2 = -V_1$, so plotting I_2 against V_1, instead of against V_2, just reverses the characteristic left to right (**Fig. 4**). Since the difference curve is straight, the two non-linear devices have combined to make a linear one – at least, in the range where both fets are on. This range is for values of input V_1 in the range $\pm V_b$ or $\pm(V_p + V_b)$, whichever is the smaller. The largest range is found with the bias set half way to pinch-off, when the full characteristics can be used.

Algebraically, the second characteristic is

$$I_2 = (I_0/V_p^2)\{-V_1 - (V_p + V_b)\}^2$$

By subtraction, the difference graph has the equation

$$I_1 - I_2 = -(4I_0/V_p^2)(V_p + V_b)V_1$$

a straight line through the origin. Redefining mutual conductance as $g_m = d(I_1 - I_2)/dV_1$, then

$$g_m = -(4I_0/V_p^2)(V_p + V_b)$$

The first bracketed term is simply a constant. The second is constant for any fixed value of bias, V_b, but the bias can be varied. Remember that V_p is negative, whereas the (variable) source bias V_b is positive.

As the bias V_b goes from zero to $|V_p|$, g_m varies from $-4I_0/V_p$ to zero. But it never varies with the strength of the signal. So, even for large inputs, as long as the signal is kept in the range, amplification is distortionless.

The behaviour is in complete contrast to that of the old "variable mu" circuit, where only tiny segments of the curved characteristic can be considered even quasi-linear.

If the bias is set at $|V_p|/2$ for the largest symmetrical swing, then $g_m = 2I_0/|V_p|$, the value for a single fet at zero bias.

Figure 5 shows a set of linear characteristics calculated for a D2S pair with a pinch-off voltage of −4V as the bias varies between pinch-off and zero. The slopes of the characteristics vary by a factor of seven, as the bias

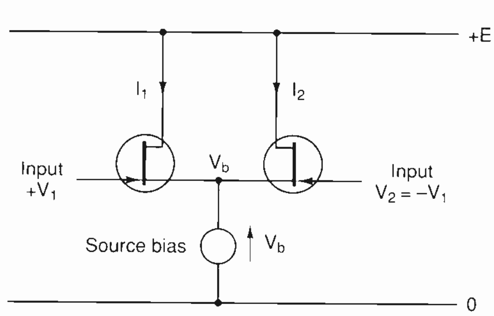

Fig. 2. Measured quantities in a push-pull matched pair of fets whose current difference should be linear in V1.

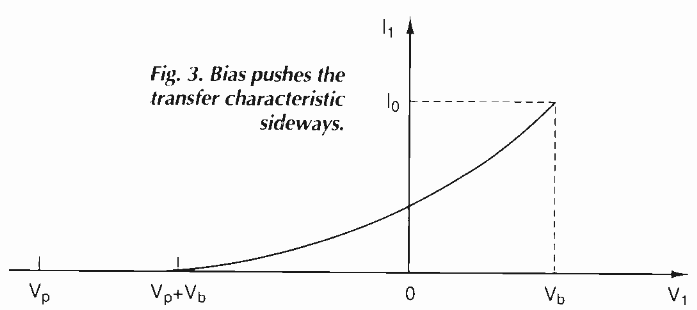

Fig. 3. Bias pushes the transfer characteristic sideways.

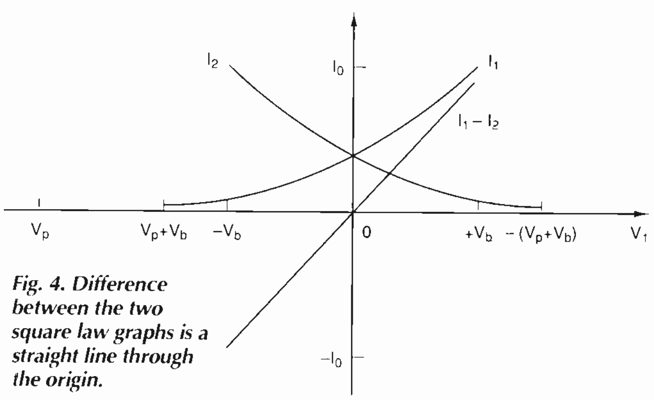

Fig. 4. Difference between the two square law graphs is a straight line through the origin.

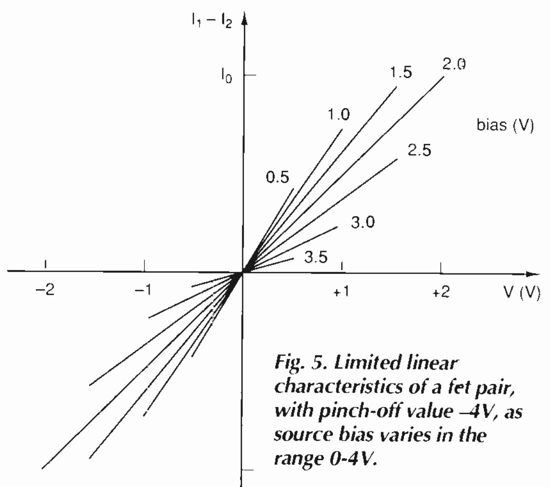

Fig. 5. Limited linear characteristics of a fet pair, with pinch-off value −4V, as source bias varies in the range 0-4V.

goes from –3.5V to –0.5V, and the minimum input range shown is ±0.5V.

Generally, with characteristics described by polynomials, sinusoidal input gives a distorted output, which can be described as linear plus added harmonics. Normally, push-pull reduces some of the harmonics; in the special case of a square-law, it cancels them completely.

Another useful feature is that with Class A mid bias, the standing current is not the usual half of the maximum – as it is in linear devices such as thermionic valves. Instead, it is only a quarter of the maximum current, giving less power loss in the quiescent state (perhaps it should have a special title, such as *Curvilinear Class A*).

The usual push-pull arrangement in small-signal stages, the "long-tailed pair", involves an unbiased resistor between the common source and ground. The effect is simultaneous equal but opposite current (rather than voltage) swings in the two fets, and so does not produce the distortionless result for all swings.

In principle, two fets can be paired to obey square laws which are not identical. Output current differences can be matched by use of different transformer tappings or different loads. The input voltage swing to one fet can be attenuated to balance differences in pinch-off voltage. It may not seem like a strategy for mass production, but will probably appeal to the amateur "tweaker".

Applications of D2S.

The most obvious application of the D2S pair is in audio power output stages. People must be doing this without realising what is happening, though few makers of amplifiers have probably consciously selected their output fet pair for square law characteristics. More likely is that devices are selected for best linearity – if at all. A recent article[1] shows curves for power fets following a square law at low current but a linear law at high current. With fets like these, biasing in the middle of the square law region should give a totally linear difference curve over the whole range, because just as one fet goes off the other goes linear.

In small signal amplifications, a D2S pair might provide a current feed to a bipolar transistor which is linear in current amplification.

For audio work, the variable gain might be useful in volume expansion or compression, while a mid-biased D2S pair would be useful in radio frequency amplifiers which amplify signals from many stations at once, as it would give no intermodulation of signals for peak inputs up to $V_p/2$.

Similarly, there are obvious uses in oscillators. All oscillators need some gain control or their outputs would go on rising for ever. In the simplest transistor oscillators, gain control is provided by saturation of the transistor – which then has a very distorted current waveform. The hope is always that the resonant circuit will clean up the output waveform.

An oscillator could use D2S to provide distortionless variable gain to keep the loop gain verging on unity. The effect would be to remove distortion in the oscillator.

Occasionally it should be possible to use just one fet twice over! In chopper amplifiers for dc amplification, an input direct voltage passes through a reversing switch, giving a symmetrical voltage square wave to the input electrode. With a square law fet amplifier stage, the output should be an asymmetrical square wave, whose pk-pk value is proportional to the input voltage.

To summarise, there seems little doubt that matched fets can offer truly linear amplification in push-pull circuits. This linearity can be expected for all bias settings, though the allowable input swing depends on bias. Varying the bias varies mutual conductance, allowing distortionless automatic gain control. The only drawback to the approach is that fets tend to vary widely, and practical testing and selection of matched pairs with suitable characteristics remains a problem. ■

Reference.

1. Finnegan, T. "Going linear with power mosfets, part 2, *Electronics World + Wireless World*, Vol 97, No 1678, September 1992.

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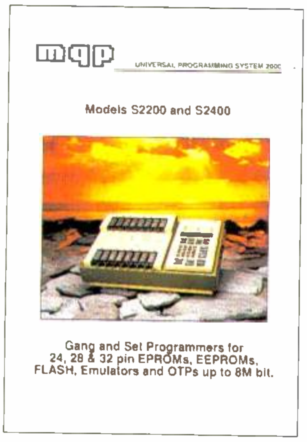

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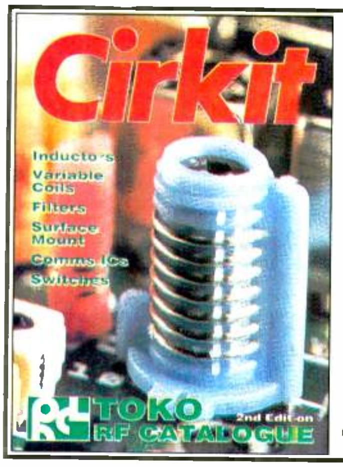

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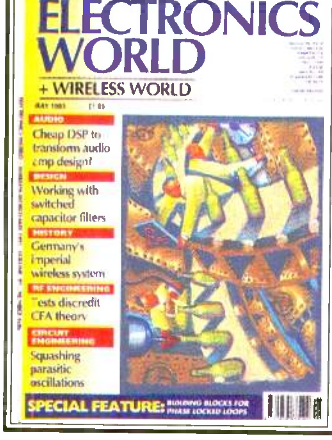

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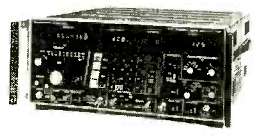

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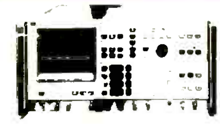

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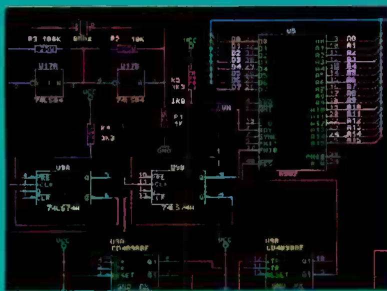
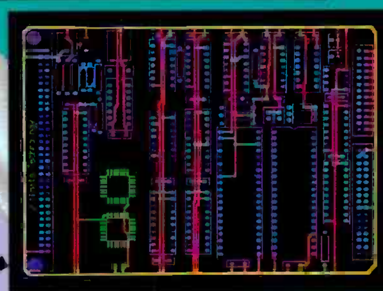
FROM CONCEPT TO ARTWORK IN 1 DAY

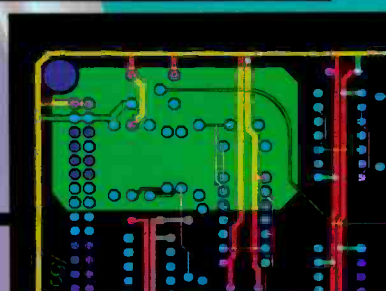


Your design ideas are quickly captured using the ULTIcap schematic design Tool. ULTIcap uses REAL-TIME checks to prevent logic errors. Schematic editing is painless; simply click your start and end points and ULTIcap automatically wires them for you. ULTIcap's auto snap to pin and auto junction features ensure your netlist is complete, thereby relieving you of tedious netlist checking.

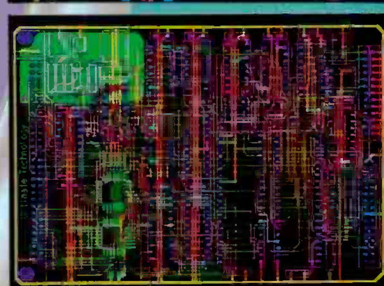
ULTIshell, the integrated user interface, makes sure all your design information is transferred correctly from ULTIcap to ULTIboard. Good manual placement tools are vital to the progress of your design, therefore ULTIboard gives you a powerful suite of REAL-TIME functions such as, FORCE VECTORS, RATS NEST RECONNECT and DENSITY HISTOGRAMS. Pin and gate swapping allows you to further optimise your layout.



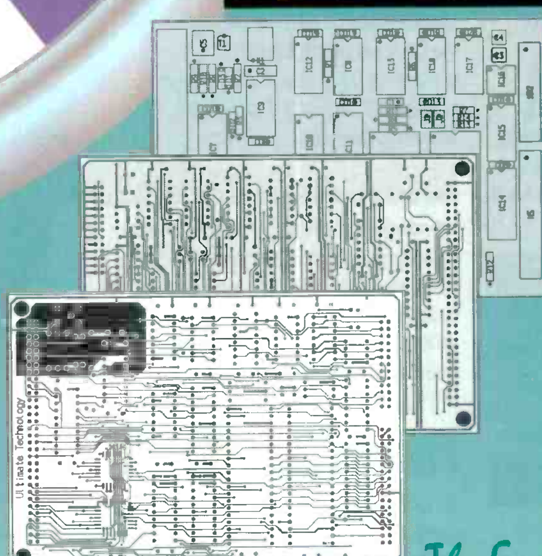
Now you can quickly route your critical tracks. ULTIboard's REAL-TIME DESIGN RULE CHECK will not allow you to make illegal connections or violate your design rules. ULTIboard's powerful TRACE SHOVE, and REROUTE-WHILE-MOVE algorithms guarantee that any manual track editing is flawless. Blind and buried vias and surface mount designs are fully supported.



If you need partial ground planes, then with the Dos extended board systems you can automatically create copper polygons simply by drawing the outline. The polygon is then filled with copper of the desired net, all correct pins are connected to the polygon with thermal relief connections and user defined gaps are respected around all other pads and tracks.



ULTIboard's autorouter allows you to control which parts of your board are autorouted, either selected nets, or a component, or a window of the board, or the whole board. ULTIboard's intelligent router uses copper sharing techniques to minimise route lengths. Automatic via minimisation reduces the number of vias to decrease production costs. The autorouter will handle up to 32 layers, as well as single sided routing.



ULTIboard's backannotation automatically updates your ULTIcap schematic with any pin and gate swaps or component renumbering. Finally, your design is post processed to generate pen / photo plots, dot matrix/laser or postscript prints and custom drill files.

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