Resistor-transistor and direct-coupled gates

Simple r.t.l.
The simplest resistor-transistor logic (r.t.l.) gate, which performs the positive logic NOR function, is shown left. A positive voltage applied to any input turns Tr1 on, causing Vout to fall from Vcc to a value that depends on the base drive. If sufficient base drive is applied, Tr1 saturates making Vout = Vce sat, representing the logical 0 state. Positive voltages applied to the other inputs increases the degree of saturation and only change Vout by a small amount.

If logical 0 voltages (Vcc sat) are supplied to all inputs the base-emitter junction of Tr1 will be only slightly forward biased (Vce sat ~ 0.1 to 0.4V) and Vout ~ +Vcc. For useful logic functions the gate must feed some load, causing an additional current Ic to flow in Re and hence reducing the logical 1 value of Vout below Vcc. The gate is also a negative-logic NAND gate.

Improved r.t.l.
Inclusion of a base bias resistor, RB in the middle circuit, returned to a negative supply ensures that Tr1 is definitely turned off when all inputs are below the input logical 1 threshold and reduces the transistors turn-off time.

Speed-up capacitors can be placed in parallel with each input RB to produce resistor-capacitor-transistor logic. However, if all inputs are at logical 1 voltages and one of them rapidly switches to the 0 state, its speed-up capacitor couples the negative-going transition to the base-emitter junction of Tr1, which can cause the transistor to temporarily switch off. For this reason r.t.l. gates are normally only used at fairly low switching speeds.

A clamping diode D1, shown right, can be connected to a supply +Vcc to make the logical 1 output voltage less dependent on the load current, provided that the drop across Re does not cause D1 to become reverse-biased.

Diode-transistor gates

Fig. 1 shows a diode-transistor logic (d.t.l.) NAND gate, using discrete components, which is effectively a diode-logic AND gate followed by an inverting transistor. Resistors R1, R2, and R3 act as a level-shifting potential divider designed to provide enough base drive to allow Tr1 to saturate, making Vout = Vce sat (logical 0), when all input diodes conduct due to logical 1 levels being present at all inputs. If any input is at logical 0 Vce sat, its associated diode conducts, causing V1 to fall to the forward voltage of the diode. The transistor is then held in the cut-off state by the reverse bias obtained by potential division of Vcc, between R1 and R2 and the output goes to the 1-level as its collector rises towards +Vcc. The turn-off of Tr1 is assisted by the negative base voltage and the turn-on time may be reduced by shunting RB with a speed-up capacitor. The fan-in is that of a diode logic gate and the fan-out depends on the current-sinking ability of Tr1. Preservation of logic levels may be improved by including a collector clamp diode—see card 1.

Another version of the d.t.l. NAND gate, sometimes called low-level logic, is shown in Fig. 2 where RB and its speed-up capacitor are replaced by the input-offset diodes D1 and D2, which are more suitable for monolithic integrated fabrication techniques. Only a relatively small voltage swing is required at the base of Tr1 to switch it on or off, but in Fig. 1 a relatively large swing in V1 is required to achieve this due to the large part of V1 lost across R1. The use of D1 and D2 in Fig. 2 leads to a much smaller required swing in V1 to achieve the desired base voltage swing. Hence the signal levels may be lowered to reduce gate dissipation which also falls due to the removal of RB. Other diodes may be placed in series with D1 and D2 to improve noise immunity. While the input diode should have a very short reverse recovery time, the level-shifting diodes D1 and D2 should be slow recovery types to ensure that they do not return to their high-impedance, reverse-biased state until Tr1 has cut off.
Direct-coupled logic

Direct-coupled-transistor logic is also referred to as direct-coupled logic and collector-coupled-transistor logic, but it is strictly incorrect to refer to it as resistor-transistor logic as it is done by some manufacturers since the input resistors have no logic function. The base resistors shown left serve only to divide the current between transistors when their inputs are paralleled. The gate is a positive-logic NOR gate which uses the transistors as summing elements. The transistors also provide input-output isolation and restoration of the logic levels in each gate in a cascade. A positive voltage at any input turns on its associated transistor causing $V_{out}$ to fall to $V_{CEsat}$, the logical 0 level. With all inputs at logical 0 the transistors are virtually cut off causing $V_{out}$ to rise towards $+V$ until the transistors in the following gates turn on.

For correct operation $R_C$ and $R_n$ values must be chosen to ensure that driven transistors turn on when the driving gate transistors turn off. Also, when the driving gate is on the driven transistors must be off, hence the threshold value of $V_{th}$ must exceed $V_{CEsat}$. The difference between these two values influences the gate's noise immunity. Discrete-circuit versions allow individual trimming of the base resistors to compensate for unequal $V_{BE}$ values. Integrated circuit versions have closely-matched $V_{BE}$ and $V_{CEsat}$ values due to simultaneous manufacture on the same substrate.

Fan-in capability is limited by collector leakage currents which, for several transistors off simultaneously, could cause $V_{out}$ to fall below the level required to ensure that the following transistors are turned on. This is particularly so in low-power versions of the gate. A typical transfer characteristic is shown above.

Further reading


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Elimination of the $V_{th}$ supply can simplify circuitry in many instances, a popular modified form of the d.t.l. NAND gate using a single supply being shown in Fig. 3. In comparison with Fig. 2, the offset diode $D_3$ is replaced by $T_{3}$ and $R_n$. This transistor provides amplification that allows a higher level of base drive to be fed to $T_3$, achieving a higher fan-out capability, and also permits a reduction in the value of $R_k$ compared with Fig. 2.

Gates used in industrial logic systems often require high noise immunity, rather than high speed and low power dissipation, as large transistors can be used in supply lines or picked up at inputs due to switching of relays, etc. Fig. 4 shows a modified form of Fig. 3 that exhibits higher noise margins largely due to $D_3$ being changed from a forward-biased diode to a reverse-biased diode exhibiting a zener-type characteristic when the p.d. across it reaches about 6.7V. Thus the input threshold voltage is increased by an amount equivalent to the p.d. that would occur across a further four forward-biased diodes connected in series with $D_3$ in Fig. 3, but is achieved by using only one such diode operating on its reverse characteristic. A higher supply voltage is required in Fig. 4 but to prevent large increases in currents, and hence gate dissipation, all resistor values are also increased. Fig. 6 shows typical transfer characteristics for the circuits of Figs. 3 & 4.

Fig. 5 shows the high noise-immunity gate of Fig. 4 with an active pull-up transistor $T_3$. When $T_3$ is off $R_k$ supplies base drive to $T_3$, which supplies load current via $R_3$. With the output in the 0-state $T_3$ is off and $T_3$ sinks load current through $D_3$ which causes the low logic level to exceed $V_{CEsat}$ of $T_3$. The table shows a comparison of some typical parameters for integrated circuit versions of Figs. 2 to 5.

Further reading


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Wireless World Circard Series 11: Basic Logic Gates—3

**Basic t.t.l. gate**

![Circuit Diagram]

**Typical parameters**
- Temperature range: 0 to 70°C
- `V` min 4.5V, `V` max 5.5V
- "0" supply current 22mA max
- "1" supply current 8mA max
- Fan out 10 t.t.l. loads
- Inputs:
  - "0" level 800mV max
  - "1" level 2V min
- "0" level 1.6mA max at `V` max
- "1" level 40µA max with `V_{IN}` = 2.4V

**Outputs:**
- "0" level 400mV max at `+ V` min
- "1" level 2.4V min at `+ V` max
- "0" level 16mA

**Short-circuit output current:** 18 to 55mA at `+ V` max

**Propagation delay** from "1" to "0" 15ns max
**Propagation delay** from "0" to "1" 22ns max

**"1" noise margin 400mV min**
**"0" noise margin 350mV min**

**Gate dissipation:** 10mW

*With output loaded by 400Ω//15pF.

**Circuit description**

Circuit shows the form of the basic transistor-transistor logic gate which performs the positive logic NAND function and which may normally have up to eight inputs. If all the inputs are at a high level (logical 1), base drive is provided to `Tr_2` through `R_1` and the base-collector junction of `Tr_1`. If any one or more input is at a low level (logical 0), the current in `R_1` flows through the base-emitter junction of `Tr_1`, to ground. The base will then be only `V_{BE}` above `V_{IN}` and `Tr_2` cut off due to lack of base drive. Transistor `Tr_1` thus performs the AND function as its collector is only high if all its inputs are high.

Transistor `Tr_2` acts as a phase splitter that saturates with only a moderate current gain—note the small ratio of of `R_1/R_2` with `R_2` ≈ `R_0`. When `Tr_2` is cut off its collector and emitter are approximately at `V` and 0V respectively. When `Tr_2` drives `Tr_3` on, its emitter rises to `V_{BE}` and its collector falls to `(V_{BE} + V_{CEsat})`. In this state `Tr_4` will be saturated so that the output will be at `V_{CEsat}` (logical 0) when all inputs are in the high state. In this condition the gate can sink current through `Tr_3` from a number of loads, normally a maximum of 10, in the 0-state, without causing `V_{CEsat}` to rise above the acceptable 0-threshold.

If any of the gate inputs is in the low state, `Tr_3` will be off as `Tr_4` is cut off. Transistor `Tr_3` will be on to an extent determined by the emitter current demanded at the output. This current will be small when the gate feeds a number of similar t.t.l. gates and its base current will be smaller still. Hence the p.d. across `R_3` due to `Tr_3` base drive will be negligible and the output will be in the high state with `V_{out}` at approximately `V` + (`V_{D1} + V_{bea})`.

Wireless World Circard Series 11: Basic Logic Gates—4

**NAND gate variations in t.t.l.**

![NAND Gate Diagram]

In the basic, or standard t.t.l. NAND gate (card 3), the resistance values affect performance. Resistor `R_1` influences the rate of voltage at `Tr_2` base and hence turn-on time. Gate dissipation, when the output is in the 0-state is affected by the value of `R_2`. Stored base charge in `Tr_3` is removed via `R_3` when the output state changes from logical 0 to 1. Turn-off time of the gate when feeding a capacitative load is influenced by the value of `R_3` which provides short-circuit protection.

**Low-power t.t.l.**

For low-power operation the resistor values must be increased to reduce the charging-discharging currents. But larger resistors imply slower switching speeds unless transistor size is reduced to lower their capacitances. This can be done due to the lower current levels and by reducing the degree of gold doping the transistors achieve higher current gains to better-utilize the smaller currents. The resulting NAND gate, left, has a power dissipation only one-tenth of that in a standard gate with a speed reduction penalty of only three times.

**High-speed t.t.l.**

To obtain higher switching speeds than are obtainable with standard t.t.l., the charge-discharge rates of the integrated and external capacitances must be increased. This implies larger transistor currents and hence lower resistor values. The higher currents require larger transistors having increased capacitances that tend to offset the speed increase due to higher currents. A distinct speed improvement is obtainable, the high-speed NAND gate shown right having about double the speed and slightly more than twice the dissipation of the standard gate.

The Darlington-connected pull-up transistors `Tr_3` and `Tr_4` provide higher active-region gain which reduces the output resistance and increases the ability to drive capacitative loads. Resistor `R_4` is sometimes returned to the output point, rather than to the 0-V rail, to reduce the gate dissipation. Sometimes a by-pass transistor, `Tr_3a`, is added to the pull-down transistor, `Tr_4`, as shown right. Resistance of the discharge path for stored base charge in `Tr_3` is reduced, improving the turn-off time. Transistor `Tr_3` cannot conduct through `R_4` until its emitter voltage exceeds the turn-on `V_{BE}` of `Tr_3`, which is approximately the same as that of `Tr_1`. Hence, the output remains in the 1 state until `V_{IN}` rises to a level sufficient to turn on `Tr_4`, which removes the low-slope region from the transfer characteristic improving noise immunity.
Switching action

When switching the output from the 0- to the 1-state, all inputs are initially high (logical 1). As the potential of one or more input falls, nothing happens until it reaches about 1.4V, when the source current via Tr1 base-emitter junction prevents base current flowing to Tr1 via the base-collector junction of Tr1, which rapidly removes the stored charge from Tr1 base and switching it off. The collector potential of Tr2 starts to rise as this transistor turns off, but stops rising as Tr1 begins to conduct heavily. This conduction occurs because Tr1 has not yet switched off, as the charge stored in its base decays only relatively slowly through R4. Therefore, a large current spike of short duration and limited in amplitude by R4 occurs in the supply line during the switch-off action due to Tr1 and Tr2 being simultaneously on.

This conduction in Tr2 removes some of the stored base charge, allowing the output voltage and Tr1 collector potential to rise. The rise continues until Tr1 becomes cut off and the output settles to the 1-level. Typical input, output and transfer characteristics are shown in Figs 2, 3 & 4 respectively. Width and amplitude of the current spike are virtually unaffected by the rate at which the gate is switched on and off. Hence a side effect of the current spike is an increase in power consumption as the switching frequency increases.

Unused inputs

Inputs that are unused in a particular application should be connected in parallel with used inputs for fastest switching speed. Unused inputs can be left open circuit, but excessive pick-up noise may result unless the open circuit is made at the integrated circuit package connection. If unused inputs are connected to the positive supply rail, it is advisable to do so via a resistor of around 1kΩ to prevent the gate being damaged by a supply line transient that exceeds the maximum rating.

Further reading

Scarlatt, J. A. Transistor-Transistor Logic and its Interconnections, chapters 1 to 6, Van Nostrand, 1972.

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<td>20mA</td>
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</tbody>
</table>

Further reading

Priel, U. Take a look inside the t.t.l. i.e. Electron, pp. 24, 26 & 30, 19 April 1973.

Murphy, R. H. Performance and reliability aspects of current trends in t.t.l., New Electronics, pp. 30, 33 & 34, 20 April 1971.


Cross references

Series 11, card 3; series 10, card 11.
Complementary m.o.s. gates—1

**Description**
The circuit shows the basic complementary-symmetry isolated-gate inverter stage, which uses both an n-channel and a p-channel enhancement-mode m.o.s.f.e.t. in a series-pair configuration. Such circuits can be directly coupled as either transistor will be in its non-conducting or off-state if its gate-source voltage is zero. Individual gates are tied together to form a single signal input gate, and the drains are communalised at the output.

Assume that the input signal excursion is from \( +V_{DD} \) to ground potential i.e. \( V_{GS} = 0 \). When the input is \( +V_{DD} \), the n-channel f.e.t. is biased to a high conducting state because \( V_{GS} \) is a high positive value. Simultaneously, the effective gate-source voltage of the p-channel f.e.t. is zero, and hence this transistor will be off, and the output will be at ground potential. When the input goes to zero volts (the low or 0-state for positive logic), the n-channel f.e.t. is biased off, but the p-channel transistor has now a large negative voltage between gate and source and is therefore biased into conduction, and the level then approaches \( +V_{DD} \) (the high or 1-state). In either logic state, one transistor is conducting and the other is cut-off. It follows that the quiescent power dissipation is exceedingly low—the transistor that is off will only conduct leakage current, typically 1mA. More significant power dissipation occurs during the switching from one level to the other, due to both a current spike which occurs when the inverter is in its linear region and to the charging and discharging of load capacitance. This depends on the frequency, the value of the capacitance and the square of the supply voltage.

If the p-channel source is connected to ground, the n-channel source should be connected to \(-V_{DD}\) and the drive signal excursion should be from \(-V_{DD}\) to 0V.

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**Complementary m.o.s. gates—2**

**Basic gate structure**
NOR and NAND functions are formed by series and parallel combinations of p and n pairs. For the NOR gate, the n-type f.e.t.s are in parallel and the p-type in series as shown left. The circuit configuration of the NAND is similar but where the p-types are in parallel, the n-types are in series, and the supply connections are changed over, see diagram right. The NOR logic action is described assuming \( V_{DD} \) is a positive voltage and \( V_{SS} \) is at 0V. Input excursions at A and B will be within the range 0V to \( V_{DD} \). If either A or B is positive, then one of the p-types will be off and one of the n-types on, thus connecting \( V_{out} \) to 0V via the on-resistance of the conducting transistor. If both A and B are at 0V, then both p-types will be biased off, due to the negative voltage at their gates, and both n-types will be off, and hence \( V_{out} \) will be at \(+V_{DD}\).

---

**Typical data**
- \( I_C \frac{1}{2} \) (CD4007AE)
- Working voltage range 3 to 15V
- Temperature range \(-40 \text{ to } +85^\circ C\)
- Input capacitance 5pF
- Input resistance > 10\(^{10}\)\(\Omega\)
- Output voltage (high) 9.99V
- Output voltage (low) 0.01V
- Fan-out d.c. \(>1000\)
- a.c. typically 20

---

**Typical data**

<table>
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<tr>
<th>Gate</th>
<th>drive (p/source) ( V_{out} ) (mA)</th>
<th>drive (n/sink) ( V_{out} ) (mA)</th>
<th>quiescent power delay ( \mu W ) (ns)</th>
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<td>Buffer</td>
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<td>16.0</td>
</tr>
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</table>

**General notes**
- **Noise immunity.** Typically the input may change by up to \( 0.45V_{DD} \) before the output begins to alter. Over the full range of \( V_{IN} - V_{SS} \) (3 to 15V), a noise immunity of 0.3\( V_{DD} \) is guaranteed.
- **Unused inputs.** NOR gates: Connect input terminals together or to the lower voltage terminal \( V_{SS} \). NAND gates: Connect input terminals together or to the voltage terminal \( V_{DD} \).
- **Parallel gates.** Gate outputs may be connected in parallel allowing greater output currents at the expense of increased power dissipation—current hogging need not be considered.
- **Pulse drive.** Rise and fall times should be less than 5\( \mu \)s typically to prevent the device spending too long in the linear region during switching and thus increasing power dissipation.
Construction

A cross-section depicting the formation of n-channel and p-channel transistors on the same chip is shown left, with associated symbols. The p-channel one is formed directly on an n-type substrate, but the n-channel device is formed in a p-region diffused into the substrate. This process creates parasitic diodes, and their relationship to the inverter terminals is shown right. As VDD is normally more positive than VSS, these diodes are in a reverse-biased state, and their leakage current contributes to quiescent power dissipation. It should be noted that if the voltage level at the output terminal is subjected to any transient condition, it is unable to go more positive than VDD or more negative than VSS, by more than the forward conducting voltage of these parasitic diodes.

Input protection

Because the input resistance of the device is so high, static charges may be sufficient to charge the input capacitance of the gate oxide to a high enough voltage to cause breakdown (~100V). The diode protection network shown is one type designed into same gates. If the gate terminal voltage is greater than VDD, diodes D2 and D3 can conduct, and if less than VSS, D1 may conduct—current magnitude should be limited to around 10mA (R may be around 2kΩ). For conditions where the diodes are either forward or reverse biased, the voltage across the oxide layer is limited to approximately 1 or 25V respectively.

Output characteristics

The two graphs shown left illustrate typical n-device and p-device drain current characteristics for the NAND and NOR gate. Drain currents for the n-type in the NOR gate are much higher than those available in the NAND gate for the same gate-source voltage.

Propagation delay

Delay periods are usually defined between 50% points on the input and output level transitions, and this will depend to a great extent on the capacitive loading at the output, as this itself affects the transition time. Third graphs show that typical propagation delays depend on supply voltage, though in the 10 to 15V region the delay spread is of the order of 10ns.

As the capacitive loading is increased (each c.m.o.s. gate is an effective 5pF load), it is fairly easy to slow down the circuits with external capacitance (right). The propagation delay is also temperature-dependent, increasing as the temperature increases due to fall-off in the gm of the transistors.

Development

Devices have been produced which operate with VDD values (VSS = 0V) in the range 1.1 to 1.6V, and recently 0.7V. Another technology known as dielectric isolation, applicable to both types of c.m.o.s., promises devices with propagation delays as low as 10ns.

Further reading

Ankrum, P. D.: Semiconductor Electronics, Prentice-Hall.
Funk, R. E. & Bishop, A.: C.o.s.m.o.s. simplifies equipment design, New Electronics, 1 May 1973, pp. 24-8.

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Emitter-coupled logic

**Typical operating data**
- R1: 270Ω, R2: 300Ω
- Rs: 1.2kΩ, R3: 1.5 to 2kΩ
- Vcc: 0V, Vref: -1.15V,
- VEE: -5V
- Logic 1 output: -0.75V
- Logic 0 output: -1.5V
- Propagation delay: 5 to 1ns
- Max. a.c. fan-out: 15

**Circuit description**

"Emitter-coupled logic" (e.c.l.) describes integrated logic circuits in which the switching transistors do not saturate as in other forms of bipolar transistor logic. Delays due to charge-storage effects in the saturated mode are avoided, leading to faster switching.

The above diagram is one form of a three-input basic e.c.l. gate, whose outputs provide an OR and the complementary NOR logic functions. The reference voltage must be well defined, and of a level midway between the logic swings. Rs, nominal logic high and low output of -0.75V and 1.55V respectively, this indicates Vref = -1.15V. The following evaluation is for guidance only.

If inputs A, B, C, are at the low logic level, Tr1, Tr2, and Tr3 are cut off, Tr4 is conducting and hence the potential at Q with respect to ground, assuming 0.75V drop across all emitter-base junctions, will be -1.9V, and the voltage across Rs is VEE - VQ. Assume VEE is -5V, then I = 2.6mA. This means that the drop across Rs is 0.78V and therefore the OR output will be -1.53V. As there is no current through Rs, VQ is 0V, and the NOR output is thus -0.75V due to the base-emitter junction drop.

When a logical 1 (-0.75V) is applied to, say, terminals A transistor Tr1 will conduct harder than Tr3, and the current in Rs is then supplied via Rs, i.e. the current has been diverted from Tr4 because the input voltage to Tr4 is half a logic level more than that of Vref, and the resultant reduction of the base-emitter drops of Tr4 is sufficient to decrease its emitter's current to almost zero. Hence the base of Tr4 is now at 0V and the OR output will be logical 1 at -0.75V. The related NOR is determined from the new VQ value of -1.5V, and hence the p.d. across Rs is -3.5V and thus I = 2.9mA. Therefore the p.d. across Rs, will be -0.48V and hence the NOR output is -1.53V.

---

Interfacing

d.t.l./t.t.l.-c.m.o.s.

The minimum t.t.l. 2.4V 1-level output is normally for a load current of 400μA, but as the c.m.o.s. gate input current is approximately 10pA, the more likely 1-output is 3.6V. This is an inadequate noise margin (0.1V) and an active pull-up resistor (typically 1 to 10kΩ depending on whether high speed or low power is required) is connected from the t.t.l. output to the positive supply rail of +5V. Hence when Tr1 is off the c.m.o.s. input will be at +5V giving a 1.4V noise margin. The threshold values of switching for the c.m.o.s. gate is typically 30% and 70% of the supply voltage, i.e. 1.5V and 3.5V respectively.

Note: Unshaded areas represent the 1- and 0-regions, the borders being the minimum 1-level and the maximum 0-level for minimum and maximum t.t.l. supply voltages.

c.m.o.s.-t.t.l.

The c.m.o.s gate must sink 1.6mA and source 40μA for the O- and 1-state of the bipolar input respectively. Not all c.m.o.s. devices can cope with one t.t.l. load (1.6mA) but gates on the same package may be paralleled to increase their current sinking capability, or preferably buffers such as CD4009, CD4041, CD4049 should be used. These devices can sink two t.t.l. load currents and still have an output of 0.4V, thus retaining a 0.4V noise margin.

**Low-power t.t.l.-c.m.o.s.**

Most c.m.o.s. devices can drive low-power t.t.l. directly as the logic zero-level sink-current is 0.18mA. Again for driving c.m.o.s., the t.t.l. output should have a pull-up resistor for adequate noise margin.
A temperature-compensated regulator package of the form shown left is available as the reference voltage, also frequently on the same chip as the gate structure. This minimizes variation of noise margin with temperature.

Faster circuits

- Centre circuit shows a type of e.c.i. gate where the reference is at ground potential. With the supplies shown, logic levels nominally -400mV for logical 0 and +400mV for logical 1. Suitable for driving into 50Ω loads, and up to 25mA d.c. when terminated in 50- and 270-Ω pull-down resistor to -3.2V.
- Fan-out: 12 (a.c.)
- Propagation delay 2 to 3ns
- Input level (high) 0.15 to 0.72V
- Input level (low) -1.5 to -0.15V
- Unused inputs: connect to -1V±0.5V
- Noise margin: ±200mV.

- Other e.c.i. gates with a basic configuration similar to the first provide multi-input, multi-emitter follower OR/NOR outputs, with optional pull-down resistors.
- $V_{CC} = 5V, V_{EE} = -5.2V±0.2V$
- Output (source current): up to 2.5mA
- Operating temperature range: -55 to 125°C
- Propagation delay (rising): 3.5 to 5ns
- Fall-time propagation delays up to 15ns due to emitter-follower

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c.m.o.s.-h.t.l-c.m.o.s.

Most high-threshold logic gates operate from a $V_{CC}$ supply of 15–1V. Hence direct connection with c.m.o.s. gates is possible. Noise immunity is high, of the order of 3V for high and low h.t.l. outputs, though this may be improved using a pull-up resistor as shown (in some cases this may be internal) which also improves the output rise-time. Rise and fall times of around 1µs should be the aim for the h.t.l-c.m.o.s. interface.

c.m.o.s.-e.c.i.

Both may be operated from -5V ± 20%, but speed is restricted to 1MHz. Speed is increased if $V_{SS}$ taken to a separate supply between -5 and -15V. The clamp diode $D_1$ keeps e.c.i. drive to a minimum of about -5.8V. Above typical figures indicate a high level noise margin of 225mV, and a low level of 4.3V.

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e.c.i.-c.m.o.s.

Output swing of e.c.i. (typically -1.55 to 0.75V) is inadequate to drive c.m.o.s. directly, i.e. switching levels are 30% and 70% of -5.2V. One technique is to use a two-input expandable gate driving a p-n-p transistor, with a pull-down resistor (≈ 3kΩ) to the negative supply. This provides noise margins amplitudes of 1.56 and 0.66V.

h.t.l.-t.t.l.

Fig. 7 shows a technique for interfacing high level logic to t.t.l. This uses a linear voltage comparator LM311, the component values used allowing an input level range of 0 to 30V. Capacitor $C_1$ may be added to decrease the effects of fast noise spikes.

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**Wireless World Circard Series 11: Basic Logic Gates—9**

### Threshold logic

![Threshold logic diagram](image)

#### Circuit description

Threshold logic gates are much more powerful and flexible than are the normal AND, OR gates. Majority, minority, AND, and OR gates are simply particular cases of threshold logic. A threshold gate has inputs A, B, C,... with weights a, b, c,... associated with the respective inputs. The output Z from such a gate is then:

\[ Z = \begin{cases} 1 & \text{if } <aA+bB+cC+...> > \text{some value } T_1, \text{the upper threshold,} \\ 0 & \text{if } <aA+bB+cC+...> < \text{some value } T_2, \text{the lower threshold.} \end{cases} \]

\[ T_1 > T_2 \] and normal arithmetic addition is involved in the above brackets. The output is more precisely written as:

\[ Z = \begin{cases} 1 & \text{if } <aA+bB+cC+...> > T_1, \text{the upper threshold gap} \\ 0 & \text{if } <aA+bB+cC+...> < T_1, \text{the lower threshold gap} \end{cases} \]

### Circuit data

Supply 6V. R1, R2, R3 = 1.5kΩ. Re, Rd = 560Ω. R4 = 3.3kΩ. Vref = 4.9V, A = B = C = Vref + 100mV. Vref = 1.8V. Sequentially applying A, B & C, Z changes in 0.4V steps from 0.9 to 5.1V. "1" = 5.1V (Vref + 200mV), "0" = 4.7V or less (Vref - 200mV). Vref can be reduced to below Vref cannot be reduced much beyond 4.90V. Rd and Re can be varied but are generally tied to the values for R1, R3 and R4 (ref. 1) and to the voltage swing required.

\[ Z = \begin{cases} 1 & \text{if } <aA+bB+cC+...> > T_1 \text{and} \\ 0 & \text{if } <aA+bB+cC+...> < T_2 \end{cases} \]

\[ T_1 > T_2 \] is the threshold gap and is that inadmissible sum which will give an ambiguous output. Generally A, B, C,... are binary (1 or 0); a, b, c,... need not be, but generally are, integers in which case the weighted sum can only take on integral values. The threshold performance is then quoted by those to integers between which switching takes place. We then obtain:

\[ Z = \begin{cases} 1 & \text{if } <aA+bB+cC+...> > \text{some value} \\ 0 & \text{if } <aA+bB+cC+...> < \text{some value} \end{cases} \]

where \( t_1 - t_2 \) are integers, \( t_1 - t_2 = 1 \), and \( t_1 > t_2 > T_1 - T_2 \). The symbol used is shown over (left).

Circuit shows a three-input threshold gate with identical weighting on each input. Basically it comprises three long-tailed pairs with a constant-current source (e.g. Tr1 and R1) in each tail. When A exceeds Vref by 100mV or more the full current flows through Tr1 and Rd and when A is less than Vref, by more than 100mV the current flows through Tr2 and

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**Wireless World Circard Series 11: Basic Logic Gates—10**

### Optical logic

![Optical logic diagram](image)

#### Circuit description

All the simple logic functions can be performed using optical couplers. Fan-out or speed difficulties preclude the use of these gates in complete logic system but in systems where simple logic is required and/or the input is in optical form, they can be very useful and show the usual advantages of optical coupling (cross ref. 1). Circuit shows an OR gate using optical couplers. If Vf1 is large enough (> 1.2V) to make D2 conduct then Tr2 conducts and V is applied to R. Similarly V is applied to R if Vf3 is high and if both Vf2 and Vf3 are high. Hence, in Boolean terms, \( V_o = V_{f1} + V_{f2} \). The transfer characteristic shown right for two different values of R indicates the static performance and shows noise immunities superior to that of transistors. For these two values of R with the given V the photo-transistors are being operated in their saturated mode (cross ref. 1) which permits a maximum current through each transistor of approximately 15mA. The normal parallel type of fan-out is, therefore, only one since the required Iy of succeeding stages is in the range 10 to 50mA. However, serial connection of succeeding stages could yield a fan-out of two or three if the appropriate resistance were chosen. This fan out could be increased if V were increased or, if speed was not essential, by using opto-couplers with Darlington output stages. The fan-in can easily be increased. Note that basically the drive signal is the diode current rather than the applied voltage so that current driving can easily be employed. Moreover Vf1 and Vf2 need not be the same, nor indeed do the two diode currents. All that is necessary is that each transistor be driven into saturation. With the quoted data pulse repetition frequencies of 40kHz can be handled. Higher frequencies but with lower current handling capacity can be
Resistors \( R_4 \) and \( R_5 \) act as summing resistors, summing the currents from the long-tailed pairs. Transistors \( T_{24} \) and \( T_{25} \) act as emitter-follower output stages for \( V_{C2} \) and \( V_{C3} \) so that 
\[
Z = V_{C2} - V_{BE} \quad \text{and} \quad Z = V_{C3} - V_{BE}.
\]
When \( Z \) is in the high state it must exceed \( V_{BE} \) by 100mV or more so that a succeeding stage will recognise it as logical 1. Likewise in the low state \( Z \) must be less than \( V_{BE} \) by 100mV or more. The following formulae apply to the circuit over.

- \[
I_1 = \frac{V_{BE} - V_{BE}}{R_1} ; \quad I_2 \text{ and } I_3 \text{ are obtainable similarly.}
\]
- When \( I_1 \) is switched from \( R_2 \) to \( R_3 \) on application of logical 1 at \( A \), then the change in \( V_{C2} = I_1 R_3 \). This change should be around 200mV or more to obtain decisive switching.
- Max \( Z = V_{CE} - V_{BE} \) occurs when no current flows in \( R_3 \).
- Min \( Z = V_{CE} - 3I_1 R_3 \). This assumes that all the tail currents are identical and flowing in \( R_3 \).

As shown, all three inputs must be applied before \( Z \) goes to logical 1. Hence:

\[
Z = \langle A + B + C \rangle_{2,3} = Z = A, B, C \text{ (Boolean) (middle diag.)}
\]

Clearly if any of the inputs is permanently tied to logical 1 we obtain a two-input AND gate. Moreover, if \( V_{BE} \) is dropped to 4.5V only two of the inputs are required to be high for \( Z \) to be 1 and hence:

\[
Z = \langle A - B - C \rangle_{2,3} \quad \text{simple majority gate.}
\]

If now \( C \) (say) is permanently tied to logical 0 we require the two remaining inputs to be high and we have obtained a two-input AND gate. On the other hand, if \( C \) is permanently tied to logical 1 only, one of the remaining inputs requires to be logical 1 for \( Z \) to be logical 1 and hence we have obtained a two-input OR gate (right).

Alteration of \( R_4 \) and \( R_5 \) is more generally used to alter the threshold.

If \( R_4 \) and \( R_5 \) are different then the outputs from \( T_{24} \) and \( T_{25} \) will not be the logic complement of one another. Any other threshold logic function that one wants can be obtained within the restriction that the weightings will remain the same. Furthermore if, say, \( R_4 \) is comprised of a string of series resistors then one can obtain a large number of different functions as well as the basic one.

Reference 3 shows how one can improve the tolerance of the circuit to large input voltages which otherwise can cause saturation and incorrect current summation.

**Further reading**


See also card 12.

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** Obtained using photo-diodes and lower frequencies with greater current handling capacity with photo-darlingtons (cross ref. 2).**

** Component changes**

\( V \) can be increased to 30V.

\( V_{F} \) and \( R_4 \) can be varied so long as \( I_{F} \) is in the range 10-50mA

Similarly for \( V_{F} \) and \( R_4 \)


** Modifications**

- A NOR gate can be constructed as shown left, in which the load \( R \) is placed in the positive supply rail.
- An AND gate can be constructed as shown centre. In this case \( V_0 \) when in the 1-state will be the supply volts minus the sum of the two saturated collector-emitter voltages.
  - A NAND gate can be constructed by placing the load \( R \) in positive supply line.
  - An exclusive-OR gate can be constructed as shown right.
  - Current flows through \( D_1 \) and hence in \( R \) only when \( A \) or \( B \), but not both, are "1". \( R \) serves to limit the current drawn from the supply when both \( A \) and \( B \) are "1".
  - Negative supply voltages can be used if p-n-p opto-transistors are used.

** Cross references**

Series 9, cards 8 & 9.

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Analogue gates

Circuit description

An analogue gate may be considered as an electronic switch which serially connects an analogue signal to a specific input point on the occurrence of a logic or control signal. This is the basis of many multi-channel multiplexers.

One gate that is particularly useful is the c.m.o.s. transmission gate. This comprises a series-pair inverter and two complementary transistors connected in parallel as shown, which allow bi-directional current flow when a control or logic signal is applied to the inverter. High and low signals applied to the separate gates, and hence both transistors are either on or off simultaneously. The sources and drains of the parallel transistors are tied together, and either terminal may be driven by analogue or digital signals, and the excursion must be within the range of the supply, $V_{SS}$ to $V_{DD}$.

If the control level is raised to the positive rail both transistors are off. This is because the gate-source or drain voltage of the p-type transistor will be zero or positive, and the n-type transistor gate-source voltage either zero or negative for a drive-signal swing limited to $V_{DD} - V_{SS}$. When the control signal is at $V_{SS}$, both transistors tend to be in the on-state. When the drive signal rises towards $V_{DD}$, the p-type f.e.t. will conduct harder because its gate-source voltage will increase negatively. At the same time the n-type f.e.t. conductance will begin to fall, as its positive gate-source voltage is decreasing. The resultant effect is for the parallel arrangement to exhibit a fairly constant conductance and hence constant resistance.

The graph is an idealized characteristic and assumes first-order linearity of n.m.o.s. and p.m.o.s. device conductance against input voltage, to give a constant GDS for the parallel connection. The actual characteristics exhibit some non-linearity, but the effect on the output-input voltage transfer function is most evident only at low supply voltages (e.g. $V_{DD} = V_{SS} = -2.5V$).

Three-state and majority logic

Three-state logic (t.s.l.) is now available from at least three companies: National Semiconductor, Texas Instruments and Signetics. Flip-flops, multiplexers, demultiplexers, line drivers, counters and r.o.m.s are among the devices available in this form. The three states are the normal 1 and 0 levels plus an off state which represents a high impedance condition in which the gate can neither sink nor source current--effectively an open circuit. Referring to the diagram, if the enable signal is logical 0 then normal logic inversion of the input signal is performed. However, if the enable signal is logical 1, then the input signals are over-ridden and the device goes into its hi-Z or off state as point A and with it point B are grounded. Hence, both $T_3$ and $T_4$ are switched off and present a high impedance to the load. This means, for example, that a large number of gates can be connected by means of a bus to a single load, only one gate at a time being connected to the load, all others being in the hi-Z state. If the number of gates connected to the bus is high then the leakage current (typically 40μA) of the off devices must be taken into account as the single on-device is supplying the load plus the leakage of all the off-devices. For this reason t.s.l. gates normally have a Darlington-connected output to protect against the source current capability by an order of magnitude over that for normal t.t.l. This in itself is an advantage of t.s.l. which in addition has the usual advantages of t.t.l. with respect to other logic families. The increased source current capability also carries with it a much reduced one-level output impedance which gives a one-level noise immunity an order of magnitude better than that for t.t.l.

To ensure in a bus-organized system that no two devices are ever on at the same time, all t.s.l. devices are arranged such that the time delay from on to off is less than that from off to on. Nevertheless, overlaps can occur and although no damage is done to the devices transients resulting from this or any other source can be longer than in a t.t.l. system, principally because more gates will probably be connected to the output of a t.s.l. device and this gives rise to increased load capacitance.

Note that all t.s.l. devices are fully t.t.l. compatible and that three-state buffer gates are available to convert any d.t.l. or t.t.l. device into a t.s.l. element.

Further reading


Circuit modifications

- Circuit left is a shunt-series chopper circuit using p-channel junction f.e.t.s to gate the analogue signal. The f.e.t.s must be fed in antiphase and can be driven from f.t.l. logic provided the f.e.t. pinch-off voltage is less than 4V. When Q is high (Q low), TR2 is conducting and TR1 is off. As TR2 is connected to a virtual earth point E, then the signal level at this f.e.t. input is minimum and hence the gate voltage exceeds the sum of the signal voltage and the f.e.t. pinch-off value, a necessary condition for switching. When Q is high, TR2 is off, and the signal is grounded via the on resistance of TR1. The analogue swing is limited by the maximum signal swing of the i.e. amplifier, and the speed of switching will depend on the slew rate of the amplifier.

- TR1 & TR2 2N5461, IC 741 or LM301A, R₁ = R₂ = 10 to 33kΩ.

- The junction f.e.t.s may be replaced by p-m.o.s. depletion types with similar pinch-off.

- The arrangement right, a series-shunt chopper, is best suited to voltage sources as neither the op-amp or TR2 draws significant current when TR1 is on, or when TR1 is off. The current from the source is negligible. Hence the input signal is gated to the op-amp with almost zero attenuation.

Further reading

CD4016A Data Sheet, RCA Solid State Databook Series SSD 203A.

Majority logic gates

A majority logic gate is a form of threshold logic gate where the numerical "weight" assigned to each of its inputs is unity. Majority logic uses combinational gates that provide an output that in the 1-state (true) only when more than half of its inputs are in the 1-state. To realize this requirement when the number of inputs in the 0-state by only one (an input majority of one), majority gates normally have an odd number of inputs.

- It has only recently become possible to design systems based on standard integrated-circuit packages employing majority logic. These packages are of the 16-pin dual-in-line type and contain two identical majority logic gates, each having five inputs and using c.m.o.s. technology. Such majority logic gates allow the design of certain functions, such as those required for communication in the presence of noise and correlation methods, that are difficult to implement with other types of gate.

- The flexibility of the majority gate can be seen by comparison with the normal AND, OR, NAND and NOR gates which select one input combination from a possible 2^n combinations of n inputs, whereas the majority gate can select 2^n−1 of the 2^n inputs. A majority gate with only three inputs is possible, as shown left, having an output function K = AB + AC + BC and, on inversion, this can produce the NOR majority function K = AB + AC + BC. The output function of the 5-input majority gate, shown centre, is more complex and is:

K = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + CDE.

By feeding this function to an exclusive-NOR gate together with another function, that may be at logical 0 or logical 1, further flexibility is introduced. When the W-input is at logical 1 (right) K provides the above 5-input majority logic function, K = M5 (say), and when W = 0 inversion occurs making K = M5. With D = 1 and E = 0, K provides the majority of the three inputs A, B and C when W = 1 (K = M3) and the NOT majority function K = M3 when W = 0. With D = E = 1, K provides the three-input OR function when W = 1 and the three-input NOR function when W = 0. With D = E = 0, the three-input AND function is realized when W = 1 and this becomes the three-input NAND function when W = 0.

Further reading


Cross references

Series 11, cards 5, 6 & 9.

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