Basic discrete-component circuits

Typical performance

- Tr1, Tr2: BC125
- Rb, Rc: 1kΩ
- R2: 22kΩ
- R3: 4.7kΩ
- R5: 10kΩ
- C1: 100pF
- Vb: 5V

Min. trigger pulse width 0.5μs
Trigger pulse height in range 1.4 to 3.6V
Output pulse width tP depends on C1/R1 — see graph
Recovery time tR depends on C1/R1 — see graph
Output pulse height 4.6V

By potential division via R6 and R4, the base of Tr1 is forced positive, thus forcing Tr1 further into conduction. This positive feedback action forces a rapid change in state of both Tr1 and Tr2. C2 then has one side at 0V, point Q, and the other side connected via R5 to Vb. It thus commences to charge towards Vb. This continues until the potential at the base of Tr2 reaches a value which causes Tr3 to start conducting. Point Q then starts to fall in potential causing the base of Tr2 to fall. This causes Q to rise, forcing the base of Tr2 even higher and the two transistors change back to the quiescent state. Length of the output pulse depends on C1/R1 — See graph.

The original quiescent state is not reached until C1 has returned to its original uncharged state. The discharge path is via R1 and the base-emitter junction of Tr2. Discharge time is what accounts for the recovery time, tR + the minimum time after the output pulse trailing edge at which a further trigger pulse will give correct operation; see graph above.

Maximum trigger pulse height is fixed by the negative-going voltage applied to the base of Tr1 on receipt of the trailing edge of the trigger pulse. If this

Circuit description
In the quiescent state with the trigger at 0V, Tr2 is held on due to base drive via R5. Point Q is therefore at zero volts and hence Tr1 is off, its base being at 0V. In receipt of the trigger pulse the base of Tr1 is forced positive, Tr1 conducts and its collector voltage drops. This is transmitted via C1 to the base of Tr2 and hence Tr2 is forced off, raising its collector voltage.

wireless world circard

Complementary circuits

Typical performance

- Tr1: BC126, Tr2: BC125
- Rb, Rc: 33kΩ
- R3: 1.2kΩ, R4, R5: 10kΩ
- D1: 1N914

With Vb = 12V, trigger frequency is 500Hz, trigger pulse width and height 10μs and 2V respectively graph opposite of output pulse width against C was obtained.

With C = 47nF and pulse width of 10μs, minimum trigger pulse height about 1.3V.

With pulse height at 2V, minimum pulse width about 2μs. Output pulse height about 12V; maximum mark-space ratio is 10:1 at this frequency.

and R4 principally. Insertion of D1 provides a low resistance discharge path giving a fast recovery time.

When Tr2 is cut off the output swings back to Vb so the output pulse period is determined by the charging time of the capacitor.

With the basic monostable circuit (card 1) the capacitor is, in the quiescent state, charged in one direction and this direction is reversed when triggered. Ignoring Vb effects, the capacitor during charging
is greater than the bias set by \( R_1 \) and \( R_3 \), then \( T_1 \) is switched off immediately and monostable action is prevented. Minimum trigger pulse height depends on \( C_2 \) and on the pulse rise time.

**Circuit modifications**

- Both of the above restrictions on the trigger pulse height may be reduced by applying the trigger pulse as shown Fig. 1. If this arrangement is used the min. pulse height should be about 0.7V and the maximum should be the breakdown voltage of the triggering transistor.
- A general-purpose diode e.g. 1N914 should be inserted in the base line of \( T_3 \) as shown Fig. 2, if the supply voltage used is above 6V or so which is the base-emitter breakdown voltage of most planar transistors. If this is not done the linearity of \( T_3 \) with respect to \( C \) is lost.
- If short recovery times are required between consecutive output pulses the circuit of Fig. 3 may be used. In the quiescent state both transistors are conducting, \( Q \) is low and \( Q \) is high. On receipt of the trigger pulse the p-n-p transistor (BC126) is switched off causing the base of the BC125 to fall in potential, thereby raising the voltage of \( Q \) and, via the 10kΩ resistor, the base of the BC126. The circuit thus latches into a condition where both transistors are off. Capacitor \( C_1 \) then charges via the 22k and 1kΩ resistors toward the supply and eventually turns the BC125 on and with it the BC126. Discharge of \( C_1 \) occurs more quickly in this case because the discharge path is through the collector-emitter junction of the BC126 and the base-emitter junction of the BC125. No external resistors are involved in this path as occurred previously. Hence, the circuit recovery time is considerably shorter.

**Further reading**


---

is going from \( +V_4 \) to \( -V_4 \) and the 0V or 50% point is sensed to bring the circuit back to quiescence. Because one is sensing a particular percentage of the attempted swing, the time taken is not supply voltage dependent. This is not the case here since a particular voltage is being sensed; the graph over shows the variation of pulse width with supply voltage. This could conceivably be used to produce a voltage-dependent monostable action.

**Component changes**

Increasing the pulse height allows a reduced pulse width (trigger pulse). Reducing \( R_1 \) to 4.7kΩ allows operation down to 6V and 0.1μs trigger pulse width. Value of \( R_2 \) is not critical; \( R_3 \) depends on \( T_3 \); \( R_1 \) and \( R_3 \) not critical.

**Similar circuits**

- The circuit of Fig. 1 will have zero stand-by power consumption but in this case has a positive-going output pulse. Again the output pulse width will depend on \( V_4 \), since in the quiescent state of \( C \) is uncharged. In addition the \( V_{CE\text{Sat}} \) of \( T_3 \) will affect the height of the pulse which should be \( V_4 - V_{CE\text{Sat}} \). The 0V level should be well defined. In the circuit over the \( V_{CE\text{Sat}} \) affects the 0V level but not the peak value (ref. 1).
- The circuit of Fig. 2 has a pulse width given by

\[
t = 0.69(R_1 + R_2)C \quad \text{and a recovery time given by}
\]

\[
t = R_2C/β.
\]

As recharging current is supplied by \( T_1 \), this recovery time is short. Pulse width is not supply dependent but since both transistors conduct in the quiescent state the standby power is large. Two outputs are available, at the collector of both transistors. They are the complement of one another (ref. 2).

Diodes are frequently included in monostable circuits to prevent too large a reverse voltage being applied to the base-emitter junction of a non-conducting transistor (Fig. 3). A diode may be inserted in the emitter lead or in the base lead. The last-mentioned is generally preferred in that it will not affect the output pulse levels.

**References**


**Cross references**

Set 18, card 1
Set 10, card 4
Op-amp/comparator circuits

Circuit description
This comparator features an open-collector output, and may be used with pull-up resistor \( R_s \) and a separate supply to give a wide switching range. Resistors \( R_s \) and \( R_e \) set the reference voltage equal to \( V_s / 2 \), but also determine the trigger pulse level necessary for switching. Resistor \( R_t \) should be much greater than \( R_s \) to avoid loading the output. With \( V_{ref} = V_s / 2 \) and the non-inverting input near 0V, the output transistor of the comparator is conducting and the output is at \( V_{out} \). A negative trigger pulse at the input causes this transistor to switch off and hence the voltage at the output rises to almost \( V_s \). Capacitor \( C_t \) now charges at a rate mainly determined by \( R_s \), and \( C_t \), which also control the width of the output pulse. The potential of the non-inverting input now falls exponentially from \( V_s \) and the comparator switches to its original condition when the non-inverting comes below \( V_s / 2 \). Diodes \( D_1 \) and \( D_2 \) prevent the inputs from being driven below zero volts, and \( D_1 \) also provides a low impedance discharge path for \( C_t \).

Component changes
IC \( 1 \): \( \times \) 3302P
Useful range of \( R_s \): 220p to 22nF

Useful range of \( R_t \): 47k to 470kΩ
Minimum trigger pulse width: 5μs
Minimum trigger pulse height: 5V (for \( V_{ref} = +10V \))
Range of \( V_s \): up to 28V.
- Increasing trigger pulse height of 8V decreases pulse width by 150 to 200μs.
- Variation of pulse width with capacitance shown, for trigger pulse 5V.
- Output pulse is supply dependent, see graph above.
(For \( C_t = 1nF \), \( R_t = 330kΩ \), p.w. is 50μs.)

Monostable using t.t.l. gates

Circuit description
The circuit above uses two of the four NAND gates available in the integrated circuit package. Positive trigger pulses are applied to the first gate which is connected as an inverter, the unused input being taken to the positive supply rail (logic 1 state) via a 1-kΩ resistor to prevent the gate being damaged by a supply line transient. With the trigger input in the logic 0 state (0V), the output of the first gate is at 1, as are both the inputs to the second gate in the steady state, causing its output to be at logic 0. A positive trigger pulse causes the output of the first gate to go to its logic 0 level. One of the two inputs to the second gate immediately goes to the logic 0 level but its other input receives the voltage across \( C_t \) which cannot change its charge instantaneously. The inputs to this gate are thus at logic 0 and 1 respectively, causing its output to switch to 1 where it remains until the trigger pulse returns to the 0-volt level. During this interval, capacitor \( C_t \) discharges towards 0 volt through \( R_t \), and the output impedance of the first gate and is recharge to the 1 level after the trigger pulse has returned to the 0-volt level.

Circuit changes
Useful range of \( V_{ee} \): +4.5V to +5.5V
Maximum useful \( R_s \): 470Ω
Maximum useful \( C_t \): 1.5μF
Minimum trigger pulse amplitude: +3V
Minimum trigger pulse width: 40μs
Output pulse shape improved by cascading a second gate (see waveform and graphs above). Cascading the fourth gate in the package provides a pair of complementary outputs.
Circuit variations

- Circuit shown left gives a pulse width that is supply independent, and is capable of a high duty cycle. Capacitor \( C_3 \) is initially charged to \( +V_e \) and \( V_{out} \) is at almost zero volts. Potentials at X and Y are defined by associated divider chains. A positive input trigger pulse to make \( V_X > V_Y \) causes \( IC_3 \) to switch (output driven low). Capacitor \( C_4 \) rapidly discharges, and \( IC_3 \) will switch when the voltage across \( C_4 \) falls below \( V_T \), defined by \( R_{11}, R_{19} \). Output voltage is now equal to \( V_{out} \), which is fed back via \( R_2 \) to \( IC_4 \), which again switches to off condition. Hence \( C_3 \) now charges up via \( R_4 \). Output pulse width is defined by the time for the voltage across \( C_4 \) to just exceed that of point Q; \( IC_3 \) then reverts to its on, or low-output state. \( IC_3, IC_4 \) \( \frac{1}{2} \) LM139, \( R_2, R_4 10k\Omega, R_4 1M\Omega, R_6 62k\Omega, R_{11}, R_{19} 10M\Omega, R_{10} 220k\Omega, R_{31} 560k\Omega, C_6 0.1nF \). Note that retriggering is not possible while \( IC_3 \) output is high—a useful lock-out feature.

- Circuit centre, using an op-amp, has a similar action to the comparator network. A negative reference voltage on the inverting input, with the non-inverting input tied to ground, gives a stable condition where \( V_{out} = -V_e \). A positive input trigger sufficient to cause the differential input polarity to change, the output switches to \( +V_e \). At this instant the potential of \( R_3 \) with respect to ground is \( -2V_e \). As \( C_4 \) charges, the potential across \( R_4 \) rises towards \( +V_e \), when switching again occurs, and circuit resets to initial condition.

Component values: \( IC_3 \) MCI1530/1531, \( C_3 23pF, R_3 100\Omega, C_1 10nF, R_1 10k\Omega, V_{ref} = 2V \). Pulse width typically 125\( \mu \)s. Diode and \( R_4 \) allow faster discharge of \( C_4 \), permitting an increase in p.r.f.

- Circuit right is a useful interface for delaying logic signals. When logic level is 1, capacitor charges quickly via diode, discharges via \( R_4 \) when logic level is 0, allowing \( V_{out} \) to rise above \( V_{ref} \). Using LM311, claimed delay is typically 0.04 to 370ms.

Cross reference
Set 17, card 8.

Circuit modifications

- The simple two-gate circuit shown in Fig. 1 has positive trigger pulses fed simultaneously to one input of each gate. These pulses appear at the output of the first gate inverted and delayed by the propagation time of the gate. Both of the inputs to the second gate are therefore at the 1 level for a short period, providing a narrow negative-going output pulse, delayed by the propagation time of one gate. This circuit has two defects: the output pulse is very narrow and non-adjustable and the trigger pulse must be wider than the output pulse.

- The circuit shown in Fig. 2 overcomes the first defect but still requires a trigger pulse wider than the output pulse. When the trigger input is at logic 0 the output of the first gate is at 1. Inputs to the second gate are at logic 0 and 1 since \( C \) is charged from the first gate, hence the output is at 1. When the trigger pulse goes to 1 the output of the second gate switches to the 0 state for an interval determined by the time constant, as \( C \) discharges through \( R \), and the output impedance of the first gate. When \( C \) has discharged to a level where its voltage crosses the switching threshold of the 1 to 0 transition the output from the second gate switches back to its 1 level. Trigger pulse width must be greater than the output pulse width, as the output of the second gate will always return to the 1 state whenever the trigger pulse returns to 0 volt.

- To overcome this problem the trigger pulses can be fed to the monostable via a third gate which has an output logic state determined by the monostable output, as shown in Fig. 3. Addition of this gate causes the monostable to be triggered when the input transition is from the 1 to the 0 state and the width of the input pulses is only that required to cause the input and output gates to change state. Since the same time constant controls the charge and discharge rates of both circuits have relatively low maximum duty cycles, typically around 25%.

- Circuit of Fig. 4 uses only two gates but has a very similar mode of operation, the output pulses controlling the state of the input gate. This gate will normally have a 0 output since both its inputs will be at 1 until the trigger pulse goes to 0 volt. This causes the output to switch states for a time determined by that required for the CR network to cross the logic threshold.

Cross reference
Set 17, card 3.

Further reading
Wilke, W., Operating a logic gate as a flip-flop, *Electronics*, 21 March 1974, pp.120/1.
Compensated c.m.o.s. circuits

Circuit description
Complementary m.o.s. monostables using one time constant suffer from the fact that the transfer voltage ($V_{tr}$) of i.c.s can vary by as much as ±33% so that replacement of an i.c. by another can result in a considerable change in the output pulse width. This defect can be removed by using two identical time constants with two inverters on the same chip. In this case the transfer voltage of both inverters is almost identical and the effect is cancellation of the variation in transfer voltage. This is taken advantage of in the circuit shown.

In the quiescent state with the input pulse low (ground), point 2 is high ($V_{RR}$), points 3, 4 and 5 are therefore low, low and high respectively. Capacitor $C_1$ is therefore in a charged state. On receipt of the input pulse this charge is removed rapidly via the source resistance and $D_1$ which is an internal protection device to prevent the input rising beyond $V_{DD}$. On the negative-going edge of the input pulse point 2 is taken down to ground and $C_1$ commences to charge towards $V_{DD}$ via $R_3$. Point 3 will go high and remain in this state until $C_1$ passes through the transfer voltage of inverter 1. When point 3 goes low $C_2$ will commence to discharge via $R_5$. $D_3$ acting to prevent discharge into inverters. When point 4 passes through the transfer voltage of inverter 2 point 5 will go high and the operation is complete. The graphs show that there are two possible outputs—at points 3 and 5. The output at point 5 is the only one in

Emitter-coupled circuits

Circuit description
In the stable state $T_3$ is on and saturated due to the base drive via $R_3$. The emitter current of $T_3$ causes the common emitter voltage to be at approximately 1.5V. Thus $T_3$ is held off by the $R_5$ potential divider which maintains its base at about 1.3V, slightly reverse-biasing the base-emitter junction. Output voltage at $T_3$ collector is at approximately 1.6V in this stable state. The $C_1$, $R_3$, $R_4$ network differentiates the input trigger pulses and, if these have a positive-going transition large enough to exceed the emitter voltage by $V_{BE}$, $T_3$ will switch on and saturate. The collector voltage of $T_3$ falls by about 4.5V and this negative-going transition passes to $T_2$ base through $C_3$ so this transistor switches off. Output voltage rises to $+V_{CC}$ and $T_4$ remains in the off state while $C_3$ charges via $R_8$, $T_1$ and $R_4$. As $C_3$ charges, the base voltage of $T_4$ rises exponentially towards $-V_{BE}$ but when it exceeds the emitter voltage, $T_4$ rapidly turns on and saturates. Current in $R_4$ increases, producing a corresponding rise in the emitter voltage which reverses the base-emitter junction of $T_2$, which switches off, and the circuit returns to its stable state.

Output pulse—see waveform below

Circuit changes
Minimum trigger pulse width 0.5μs. Output pulse width could be varied by $R_3$ but this would also change the d.c. conditions. Larger supply voltages may be used but then a silicon diode should be included in series with $T_3$ base to prevent reverse breakdown of its base-emitter junction by the switch-off transient.
which there is compensation for transfer voltage variation. Due to lack of feedback in the circuit the risetime of the output is decidedly long (see performance data) but this is acceptable if the circuit is supplying further c.m.o.s. circuitry.

Despite the protection of $D_1$ the fact that the circuit is being fed via a capacitor makes it advisable to ensure that the input pulse height is close to $V_{pp}$. This can be done if the pulse is fed via further c.m.o.s. supplied from $V_{mm}$.

This circuit can be re-triggered, i.e. the output 5 can be maintained in its low state by feeding in a succession of pulses, provided each pulse occurs before point 2 reaches the transfer voltage of the first inverter.

Circuit modifications
- Adding an emitter-follower to the original circuit, as shown in the top left diagram, allows the output pulses to be obtained from a low-impedance source and to be referred to ground. By adjustment of the supply voltage these pulses may be made compatible with t.t.l. logic circuitry.
- A p-n-p common-emitter stage may be added, as shown top right, to use the output pulses for driving a ground-connected load. For example, the load could be in the form of a filament lamp for alarm or monitoring purposes and as collector currents of at least 50mA may be obtained, the load could be a relay coil to provide control of some other circuitry. The inductive load provided by the relay coil should be shunted with a protective diode.
- The original circuit may be modified to be triggered by negative-going pulses as shown in the circuit shown bottom left. In this arrangement the trigger pulses are applied to the collector of $T_1$ via the small coupling capacitor $C_5$.

The negative-going trigger pulse edge is passed to $T_2$ base through $C_3$ switching this transistor off. $T_3$ turns on and the remaining cycle of operations are as described previously. The circuit will function with $C_1$ omitted but the transition to the quasi-stable state will be more rapid when it is included in the circuit.

- In all of the circuits discussed the output point was isolated from any internal coupling. If, see bottom right $R_1$ of the original circuit is taken to $T_2$ collector instead of the $+V_{cc}$ rail this is no longer the case and changes in emitter voltage may be very small. The simplest way to provide faster switching is to prevent $T_1$ and $T_2$ from saturating by increasing $R_4$.

Further reading
- RCA applications note ICAN6267.

Further reading

Cross references
- Set 18, cards 1 and 7.
Wireless World

Voltage-controlled monostables

**Circuit description**
Transistors Tr1, Tr2 form a complementary-pair positive feedback switch, and are either both off or both on. In the rest state, this switch is closed. Tr3 is on, D1 is non-conducting, and C1 is charged. A negative trigger pulse applied at the trigger terminal causes the regenerative switch (Tr1, Tr2) to open. Collector current of Tr3 is now 2I, where I is common base current gain and I = (V2 - VBB)/R3. Hence C1 discharges at a constant rate giving a run-down linear sweep at point A. This sweep continues until the potential of point A is less than Vcontrol - V2, when the complementary switch again conducts. The switch also acts as a comparator, besides providing a low impedance path for recharging capacitor C1.

Notice that the sweep termination depends on the level of the control voltage, which therefore controls the width of the output pulse.

**Component changes**
Tr1, Tr2: BC125, BC127
R1: 22Ω, R2: 1.2kΩ
R3: 10kΩ
C1: 1nF, C2: 100pF
VC: +10V
VC: +10V
D1: 1N914
Trigger pulse magnitude: --13V
Trigger pulse width: 0.1μs
Vcontrol: 8V
Output pulse duration: 7μs
Waveforms and timing graph shown opposite, curve (a)

Long-delay circuits using c.m.o.s. and unijunction devices

**Circuit description**
The high input impedance of c.m.o.s. integrated circuits offers a low leakage path for capacitor C1, and thus allows a wide range of delays from this D-type flip-flop configuration. The D-input is permanently connected to the positive supply rail, hence Q goes high when a positive trigger pulse is applied at the clock input. A positive voltage (approximately 50% VDD = VSS) at terminal R will reset Q to its initial condition of 0V.

On the occurrence of a trigger pulse, the reset threshold will be reached in a time defined by C1 and R1, which in turn defines the delay available at Q. This circuit is fairly insensitive to supply voltage change, because the threshold level for reset will alter pro-rata. However it should be noted that this level is not well defined, and hence the accuracy of time delays will depend on specific measurement with the components used. Unused inputs should be tied down to ground.

**Component changes**
Useful range of C1: 47μF to 32μF
For long time delays, low-leakage capacitors must be used
Supply voltage range: (VDD - VSS) 3 to 15V
Minimum pulse width: 0.1μs
Minimum pulse height: 2 to 4V
Alternative IC: MM74C74

UJT transistor monostable
The circuit shown over (top) employs a discrete transistor flip-flop, with the timing controlled by the firing of the unijunction transistor Tr1. The normal rest condition of
Circuit modifications
- Connect additional buffer stage Tr3 (BC126) and R4 (390Ω) for increased output pulse amplitude (above).
- Trigger pulse amplitude is 7V, when coupling capacitor C4 increased to 1nF; provides timing graph shown over at (b).
- Circuit (centre) is basically an emitter-coupled monostable circuit. Time duration may be extended by the inclusion of a complementary pair (Tr8, Tr9) with breakdown fixed by zener diode D2. This effectively increases the cut-in voltage, Vb, of Tr8, Tr9 is normally on.
- Trigger pulses cause Tr6 to conduct (Tr9 off), and circuit returns to its stable state when the voltage at B brings the regenerative switch into conduction. Pulse duration depends on I, which is controlled by voltage applied to base of transistor Tr8.
- Output pulse duration typically in the range 40 to 200ns for a control voltage of 3 to 6V.
- Operational amplifier IC1 (MC1530/MC1531), shown right, can provide variable delays by controlling the voltage at the inverting input. Diode clamps the negative amplitude of the output to about −0.7V. Positive output will approach +V.

Further reading
Motorola application note AN-258.

Cross references
Set 18, cards 3, 6.

An advantage is that the initial voltage across C4 is always the same at the start of a period no matter the pulse repetition frequency. It is claimed that with the supply voltage variation noted above, pulse duration changes are 2%.

Circuit (bottom) uses the transistor array CA3095E. Diodes D1, D2 and Tr2 act as a voltage-limiting network. Quiescent condition is with transistors Tr2 and Tr3 on, Tr5 and Tr6 off. A negative-going pulse at the trigger-input terminal which is coupled to the base of Tr4 via diode-connected transistor Tr5. Hence Tr5 (and Tr4) cut off and Vout rises to +Vs. Because Tr5 and Tr6 are emitter-coupled, Tr6 can now conduct when Tr5 is off, therefore the voltage across C6 i.e. is near ground. Capacitor C7 now charges via R4. When the base potential of Tr4 is high enough to bring it into conduction, Tr4 again goes off and Vout drops to its normal value of about 1.8V.

Time duration is \( t = 0.47R_C \).

Cross references
Set 18, cards 5, 9.

Further reading
Unijunction Transistor Timers and Oscillators. Motorola application note AN-294.
Dual monostable applications using 555 timer

Circuit description
The i.e. shown is a dual 555-type timer (internal details of which are shown in cross references 1 and 2). In this application the output of the first timer is capacitively coupled via C1 to the input of the second. Both timers are triggered when the input to each drops below \( \frac{1}{3} \) Vcc. In this case the trigger pulse operates timer 1 and the output of timer 1 triggers timer 2. Both timers are connected in their monostable mode. Formulae for \( T_1 \) and \( T_2 \) quoted are valid for all conditions and are fixed entirely by the external \( R_1, C_1 \) and \( R_2, C_2 \). Any succeeding trigger pulses are ignored. Both \( T_1 \) and \( T_2 \) can be anywhere in the range 10\( \mu \)s to 100s with two provisos: \( T_1 \) cannot be reduced below \( T_{pp} \), but since \( T_{pp} \) can be less than 3\( \mu \)s this is not serious. Secondly low values of \( T_1 \) and \( T_2 \) should not be obtained by reducing \( R_1 \) and \( R_2 \) to a level at which current drain from the supply is serious. A minimum value of 1k\( \Omega \) is

Typical performance
- \( V_{cc} \): 10V (range 4.5 to 16V)
- Output pulse height: 9.3 to 9.9V
- \( C_2, C_1 \): 10nF
- \( C_3 \): 1nF
- \( R_1 \): 47k\( \Omega \)
- \( R_2 \): 33k\( \Omega \)
- \( R_3 \): 1.1R1R2C1
- \( R_3 \): 1.1R2C2
- \( V_{cc} \): Vcc
- IC: XR2556

High duty-cycle monostable

Circuit description
In this circuit the timing capacitor \( C_3 \) not only determines the width of the output pulse obtained from \( T_2 \) collector but also delays the setting-up of the circuit in readiness for the next cycle of operations. This prevents an early trigger pulse from producing an output pulse having too short a duration. Because the circuit may be re-triggered immediately after completing its cycle, an output-pulse duty cycle approaching 100% may be obtained. The conventional "cross-coupled" monostable allows only about 95% duty cycle, even when its timing capacitor is rapidly recharged from a low-resistance source. In the stable state, \( T_3 \) is biased off and \( T_1 \), \( T_2 \) and \( T_4 \) are on. Input trigger pulses are differentiated by \( C_1 \), \( R_1 \), the positive component passing to \( T_2 \) base via \( D_1 \). If of sufficient amplitude, these overcome the reverse bias on \( T_3 \), which switches on, \( T_2 \), \( T_3 \) and \( T_4 \) switching off. Transistor \( T_4 \) remains off for approximately 0.7\( \tau \), as its base potential rises under the control of \( C_2 \). When \( T_2 \) turns on again, \( T_3 \) collector potential rises as \( C_3 \) recharges with time constant \( \tau = C_3 R_3 \) until it exceeds approximately 0 V. Transistor \( T_4 \) and hence \( T_2 \) then switch on regeneratively and the circuit returns to its stable state and may be re-triggered immediately.

Typical performance
- Input: 4V positive pulses, pulse width 1\( \mu \)s, p.r.f. about 10kHz
- Output rise time: 0.5\( \mu \)s
- Output fall time: 0.2\( \mu \)s *depending on value of \( C_3 \)

Component changes
- Minimum useful supplies: ±2 V
- Useful range of \( R_1 \): 1k to 100k\( \Omega \)
- Use range of \( R_2 \): 1k to 470k\( \Omega \)
- Minimum trigger pulse amplitude: approximately 2.5 V
- Minimum trigger pulse width: less than about 0.1\( \mu \)s
- Maximum useful p.r.f.: 200kHz
recommended for both \( R_1 \) and \( R_2 \). The only restriction on \( R_2 \) is that it must not be so low as to exceed the current rating (200mA) of the i.c.

Typical waveforms are shown above. These are suitable for sequential timing circuits. Note that trigger pulses occurring during the period set by \( R_1, C_1 \) and \( R_2, C_2 \) are ignored.

**Circuit modifications**

- Obviously the i.e. may be used as two separate timers or monostables by omitting \( C_3 \) and \( R_3 \) and by applying the trigger pulses directly to pins 2 and 12.
- Referring to the main diagram, control over the total period \( (T_1 + T_2) \) can be achieved by connecting the arm of a potentiometer to \( V_{cc} \) and the ends to pins 3 and 9, \( R_4 \) and \( R_5 \) being now the two segments of the potentiometer shown above. If \( C_1 = C_2 = C \) then \( (T_1 + T_2) = \frac{C}{R_4} + R_5) \) which is constant no matter the individual \( T_1 \) and \( T_2 \).
- Each individual timer can be regarded as a frequency divider in its own right. For example, in the waveforms shown over, the lower two graphs indicate that output 1 is running at half the trigger pulse frequency and output 2 is running at half the frequency of output 1. By correct choice of \( T_1 \) one can make output 1 run at any submultiple frequency of the trigger and likewise with correct choice of \( T_1 \) output 2 can run at any submultiple frequency of output 1.
- A combined frequency divider and pulse width controller can be achieved by setting \( T_1 \) so that it is greater than the trigger period and by ensuring that \( T_2 < T_1 \). The value of \( T_1 \) sets the frequency division and the value of \( T_2 \) sets the pulse width, the output (pin 8) being output 2. Furthermore, the “phase” of the output with respect to the trigger can be controlled since, for example, frequency division by 3 allows \( T_1 \) to lie anywhere between two and three trigger periods. See waveforms above.

**Further reading**


**Cross references**

Set 3, card 9
Set 13, cards 3 and 5

© 1974 IPC Business Press Ltd

---

**Circuit modification**

- The circuit shown top is a logical representation of a high duty-cycle monostable which may be realised with logic gates or discrete transistor circuits.

A pair of pulse-steering AND gates and a flip-flop used as a toggle cause the positive-going input trigger pulses to be alternately applied to the pair of monostables (M). The monostable outputs are combined in the OR gate to provide the output pulse and to toggle the flip-flop which changes state when the output pulse is completed. Hence, the start of the next output is only delayed by the time taken for the flip-flop to change its state, which can be a small percentage of the output pulse duration. A discrete version produced 700ms pulses every 705ms.

- Circuit shown next uses a flip-flop in conjunction with a Shottky-diode SD1 to achieve a high duty cycle. An input pulse causes the flip-flop to change its state producing an exponential voltage rise across \( C_2 \). When this voltage reaches a critical value the diode breaks down rapidly discharging \( C_2 \) and producing a negative pulse to reset the flip-flop via \( C_2 \) in readiness for the next input pulse. Pulses of 2us duration may be produced after only a 250ns recovery time.

Typically, \( R_1, R_5, 1M\Omega \), \( R_4, R_6, 10k\Omega \), \( R_7, 150k\Omega \), \( R_7 \\ 2.2M\Omega \), \( C_1, C_2, 20pF \), \( C_4, 500nF \), \( D_1, 1N914, \) SD1 4E20-8, with \( V_{cc} \) +25V.

- Circuit shown bottom can provide a recovery time of only \( 1\% \) of its period and may be triggered by positive pulses at \( T_6 \) base or negative pulses at \( T_6 \) base causing both transistors to switch from their on to off states. Transistor \( T_4 \) can recharge \( C_1 \) with a large collector current to rapidly regain its initial voltage. Diode \( D_1 \) and \( D_2 \) may be omitted if \( T_6 \) and \( T_7 \) have a large reverse \( V_{BR} \) rating.

**Further reading**

Shagen, J. L. & Mall, A.

**Cross reference**

Set 19, card 9.