High current-gain pairs—1

Darlington pair

Components
Tr1: BFR41
Tr2: TIP3055

Description and characteristics
A Darlington pair as shown above is a frequently used two-transistor circuit, the purpose being to obtain high gain through cascading two transistors. Because large currents are obtained in the second transistor one frequently finds this to be a power transistor and that the arrangement is used in many switching applications. As the circuit has only three terminals it can be regarded as a single high-gain transistor. The basic action is that $I_b$ produces, through $Tr_1$, a large base drive for $Tr_2$. The total $I_e$ is the sum of the two collector currents although the contribution of $Tr_1$ to $I_e$ will be small if the gain of $Tr_2$ is large.

The characteristics obtained for the components quoted are as shown. From graph 1 we obtained an $h_{fe}$ of about 25 mS and an $h_{re}$ of about 11,000. Graph 2 shows an $h_{oe}$ of around 70. These figures are in line with theory (see reference). Graph 2 also shows the dependence of $I_e$ on $I_b$, the two graphs being indistinguishable because of the scales chosen.

For switching applications the value of $V_{CE}$ is important. $V_{CE}$ is defined as that $V_{CE}$ corresponding to an arbitrarily low $I_e/I_b$ ratio, in this case 1,000 (graph 3). With higher $I_e/I_b$ ratios, corresponding to lower $I_b$ values the value of $V_{CE}$ will be lower. The corresponding graph of $V_{CE}$ against $I_e$ is shown in graph 4.

Graph 5 shows the dependence of $h_{fe}$ on $I_e$. The drop in $h_{re}$ at high $I_e$ being due to saturation and that at low $I_e$ being due to lack of base drive to $Tr_1$.

High current-gain pairs—2

Components
Tr1: BFR41
Tr2: TIP3055

Performance and description
The Darlington circuits on card 1 are both super $\beta$ circuits but have the additional characteristic that they only have three terminals and so can be regarded as a single transistor. The circuit shown above also has high gain but has four terminals, three of which can be regarded as base, emitter and collector, the fourth being connected to a voltage which gives some control over the characteristics. The principal difference in performance of this circuit is that a low saturation voltage is obtained. From graph 1 we obtained an $h_{fe}$ of 7,000 and an $h_{oe}$ of 25 mS for $V_a=2.0 V$.

Characteristics for $V_a=4.0 V$ are virtually identical. Graph 3 shows the low $V_{Cesat}$ values obtained, slightly lower values being obtained for $V_a=4.0 V$.

Graph 4 shows the expected $V_{Cesat}$ values around 1.5 V since two base-emitter junctions are between $b$ and $e$. Again slightly lower values are obtained for $V_a=4.0 V$. The graph of $h_{re}$ is shown in graph 5, the figures being in line with the previously obtained $h_{re}$.

Note that in this configuration $Tr_1$ will have supply voltage $V_a$ across it and will normally require a current-limiting resistor in its collector lead.
Complementary Darlington pair

Graph 1 shows the output characteristics: not eminently suitable for a small-signal amplifier, but as the circuit tends to be used for switching applications, this is not serious. We obtained for these components an hfe of 8,500 approx and an hfe of greater than 0.18.

Graph 2 shows I_b and I_e against V_1b, and these again coincide because of the scale chosen. Note in this case that V_ce during conduction is about 0.7V as opposed to 1.5V for the normal Darlington; this is due to the fact that there is only one junction between h and e. This shows up again in graph 4.

By the same token, the graph of V_c (graph 3) is much the same as for the normal Darlington. Graph 5 again has much the same shape as that for the normal Darlington though with a lower maximum value, which is in line with the reduced hfe.

Further reading

Reference

Components
T1: BFR81
T2: TIP3055

Description and characteristics
The basic action of this circuit is the same as that of the normal Darlington pair. Note that the circuit in this format is acting as a single p-n-p transistor. An n-p-n version is shown to the right. It is the input transistor which indicates whether the combination is p-n-p or n-p-n but one can readily check the bias voltages.

Components
T1: BFR81
T2: TIP3055

Circuit description
First given by Baxandall and Shallow, this circuit has a gain producing action similar to that of the Darlington's and the circuit overleaf. Base current to T1 produces large base drive to T2 thereby giving large gain. In this case, however, bias (I_b) must be provided for correct action. As there are more than three terminals it cannot be considered as identical to a single transistor, and it displays some characteristics that one does not obtain with single transistors. In particular, one obtains collector current I_c, the absence of any V_T, this being due to the action of I_b. The characteristics shown were obtained with a V_CE of 1V and exhibit an overall gm of 6A/V, obtained at V_B of zero.

The components used were chosen for comparison with the other super pair type of transistor pair, but certain features would dictate other choices. For example, the circuit simulates a p-n-p transistor whilst having an n-p-n output stage. In monolithic i.e. with lateral transistors, n-p-n transistors have low gain so that T1 would dictate the overall gain. As T1 has a very low voltage across it, viz V_CE of T2, then T1 can be made to have high gain—see MC1538R.

When used as shown above, the circuit exhibits extremely high output resistance which, allied to the high current gain, gives large voltage gain. The reason for this is that V_1 + V_2 and V_3 cancel, both being base-emitter voltages, then V_1 + V_2 + V_3 and the current in R1 is thus defined by I_b and the current in R, no matter the value of R2.

The circuit therefore, must have a large output resistance. Values as high as 50MO have been quoted.

Further reading
**wireless world** circard

### Cascode amplifier

Components
- Tr₁, Tr₂: BFR41
- Vₜ: 10V
- Z: 660mH coil plus stray capacitance plus c.p.o. loading
- C: coupling capacitor
- Rₘ: see graph
- Vₜ: see graph

**Circuit description**

Tr₁ is a common-emitter amplifier which is feeding Tr₂ in common-base mode. The load on Tr₁ is therefore a near short-circuit a.c.-wise. In addition, the current gain of Tr₂ is near unity but its output impedance is high, due to the common-base mode of operation. The combination therefore shows the gain characteristics of a short-circuited c.e. stage plus the output impedance characteristics of c.b. It is therefore ideally suited for the driving of tuned resonant loads or indeed of any high impedance load.

The basic equations are

\[ I_o = g_m V_{in} \]

\[ I_o \approx I_i \]

\[ g_m = I_o / 26mV \]

The second equation assumes unity current gain through Tr₂ and the last equation assumes that hᵦₗ (for Tr₂) is very low. The net result is

\[ V_{o} / V_{in} = g_m R_m \]

Since Iₑ is almost linearly related to Iₑₑ, particularly if \( V_{CE} \) of Tr₁ is constant which it is in this case, then \( g_m \) is controllable by \( R_B \). The net result is the graph shown. For each result the circuit was retuned for resonance, the change in resonant frequency being of around 1.5% over the complete range. With \( R_B = 1Ω \), the resonant frequency was 924kHz and the bandwidth 18.5kHz giving a Q of 50. \( V_A \) is not critical—it is only required to produce correct transistor action. In these results it was 3V. A 1.5nF supply decoupling capacitor was necessary. Note that the graph represents a range of voltage gain from 50dB to 71dB and that the range of \( R_B \) is 20:1.

---

**wireless world** circard

### Set 20: Transistor pairs—3

**Long-tailed pair**

(a) **Differential in—differential out**

**Circuit description**

This emitter-coupled differential amplifier should have a large value for \( R_s \) to provide a high common-mode rejection ratio (c.m.r.r.). This implies that the differential output voltage between collectors for a common signal at the bases, is very small and ideally zero. In general, the output signal depends on the difference between the signals at the transistor bases. Each transistor receives half the signal i.e. the gain to each output is half of that provided by a single transistor under the same conditions.

**Performance data**

Tr₁, Tr₂: matched pair from CA3086.
- \( R_1, R_2, R_2 = 100kΩ \)
- \( R_s, R_f = 150kΩ, R_V1 = 1kΩ \)
- \( V_s = 15V \)

**Gain slope:** typically 230.

**Variation in gain:** ±1% for several choices of CA3086.

Reducing \( R_1, R_2 \) by similar ratios will maintain slope at same order of magnitude.

(b) **Single-ended in, differential out**

\[ V_{in} = 10mV \text{ d.c.} (20mV) \]

\[ V_{out} = 2.39V \text{ d.c.} (4.79V) \]

\[ \Delta V_{out} = \text{i.e. gain slope similar to (a)} \]

\[ \Delta V_{in} = 240 \]

For single-ended output:

\[ V_{tit} = \text{voltage between X and ground.} \]

\[ \Delta V_{out} = 10.28V - 9.06V = 122. \]

\[ \Delta V_{in} = \text{20mV - 10mV} = \text{122.} \]

\[ \text{i.e. gain is halved.} \]

(c) **Common mode input**

\[ \Delta V_{xy} = 0.149 - 0.142 \]

\[ \Delta V_{in} = \frac{2}{1} = 0.007 \]

For single-ended output (terminal X to ground):

\[ \Delta V_{out} = 0.0045 \]

\[ \Delta V_{in} = \text{c.m.r.r. improved by trimming} \]

\[ R_s, R_f \text{ for zero balance.} \]

Figure of merit is c.m.r.r. or voltage gain for differential inputs divided by voltage gain for common-mode inputs that is 0.007/230.
The circuit overleaf has two disadvantages viz, it is not a three-terminal device and also requires a biasing voltage. The above circuit suffers from neither of these disadvantages. The circuit is self-biasing provided only that $I_a$ is less than $I_b$ by an amount sufficient that the resulting $V_{eb}$ keeps the bipolar transistor well out of saturation. Typically $V_{ce}$ would need to be in the range 0.2 to 1.0V (though a higher value would be preferable for higher gain). This means that the operating current is restricted to the $I_a$ of the f.e.t. with $V_{gs}$ in the range of $-0.2$ to $-1.0V$. In practice the current is defined by some other requirement (drift, matching etc) and is often much less than $I_{bias}$—the f.e.t. current with $V_{gs}=0$ (which would give no gain from the bipolar anyway). The f.e.t. will frequently be required to operate near pinch-off.

The circuit, above centre, is a less common form which loses the merit of low capacitive feedback. It does, however, have the merit of increased current capability since the f.e.t. can operate with $V_{gs}=0V$.

Cross references
Set 20, cards 4, 10.

© 1975 IPC Business Press Ltd.

Useful relationships
Bipolar transistor collector current related to base-emitter voltage by

$$I_c = I_b \exp \left[ qV_{be}/kT \right]$$

$$dI_c/dT = qI_b$$

$$dV_{be} = kT$$

At room temperature

$$g_m \approx 26 (\text{mA/V})$$

Differential input signal can be considered as

$$v_{in} = g_m R_{c} \frac{V_{in}}{2}$$

$$V_{ce} = g_m \frac{V_{in}}{2} R_{c}$$

Differential output given by

$$v_o = v_{c1} - v_{c2} = -g_m R_{c} v_{in}$$

Voltage gain $A_v$

$$A_v = V_{out}/V_{in} = -g_m R_{c} = -I_b R_c/26 = -V_i/26$$

For identical transistors the collectors are at equal potentials for common-mode signals. Hence they can be considered connected together

$$-V_{in} - V_{out} = V_{out}/2$$

Note: If $R_b$ replaced by a constant-current circuit, $V_{out}(cm)$ can be <<1.

$$c.m.r.r. = -\frac{g_m \cdot R_c}{R_c/2 + R_b} = \frac{-g_m R_b}{2}$$

Temperature drift

$$\frac{dT}{dt} = kT$$

At room temperature (300K) drift is $3.3 \mu V/\deg C$ for each mV of initial offset.

Further reading


Cross reference
Set 12, card 10
wireless world circard

SET 20: TRANSISTOR PAIRS

CURRENT MIRRORS

Description (bipolar)
The current mirror is an extremely useful two-transistor circuit extensively used as an integral part of monolithic operational amplifiers to define a current, the mirror current \( I_{M} \), in terms of a reference current \( I_{R} \). With identical transistors the base-emitter voltages are identical and if \( \text{T}_{1} \) has a high current gain the collector currents \( I_{K} \) and \( I_{M} \) are matched, to a first order. Any matched pair of n-p-n transistors may be used but those on a single chip are preferred; the variable temperature sensitivity of discrete devices reduces reliability of the circuit. An important requirement in many applications of the current mirror is a high output resistance. The left-hand graph above shows that the static output resistance \( R_{O} = \frac{V}{I_{M}} \) increases with \( V \) for a given reference current value. However, the right-hand graph shows that whilst the dynamic output resistance \( R_{D} = \frac{\delta V}{\delta I_{M}} \) also increases with \( V \), the far more rapid rise in \( R_{O} \) causes the ratio of dynamic to static output resistance to fall rapidly with increasing \( V \). Hence, a compromise must be made between the values of \( R_{O} \) and \( R_{D} \) to be used with a given value of \( I_{M} \).

For currents in the microamp range the output resistance of the current mirror can be increased by inserting a negative feedback resistor in the emitter lead of \( \text{T}_{2} \). For higher current requirements, transistors on the same chip can be connected in parallel to increase the junction areas.

COMPLEMENTARY SWITCHING TRANSISTORS

Circuit Description
The arrangement of the complementary pair of transistors, with or without the resistor \( R \), connected between two other points, is a frequently used combination (see earlier refs.). With the resistor \( R \) as shown, the circuit acts over a portion of its I-V characteristics as a negative resistance, of value \( -R \approx R_{Sat} \) approximately. Graphs obtained are shown for values of 1k and 10kΩ.

Components
\( \text{T}_{1}: \text{BFR81}, \text{T}_{2}: \text{BFR41}, R: 1k, 10kΩ \)

Performance
Slope in negative resistance region 0.75kΩ and 8kΩ for \( R = 1kΩ, 10kΩ \) respectively (see graph).

Initially with low I, V may be considered as \( V_{EB1} - V_{BE1} + V_{BE2} \). As \( V_B \) is low initially V is the sum of the two exponential emitter-base voltages. As I increases these two voltages tend to 0.6V but \( V_B \) continues to rise and because of the minus sign \( V \) starts to fall, at a value slightly less than 1.2V. The fall continues (negative resistance region) until both transistors saturate. At this point we can no longer assume that all the current is passing through both collectors and \( R \) and we are best to view \( V \) as being \( V_{CE1} + V_{BE} + V_{CE2} \). Since the two transistor voltages are relatively fixed, \( V \) then starts rising again. The value of the trough is given by \( V_{BE1} + V_{BE2} \approx V_{BE1} \). The voltage range of the circuit is readily increased by the modification shown opposite with Zener diodes appropriate to the application.

These circuits are described as being open-circuit stable, i.e. for any current drive there is a unique voltage. The dual of this is the voltage driven, short-circuit stable device. An f.e.t. realization of this is shown with the corresponding characteristic (see Further reading).
Description (m.o.s.)
Current mirror circuits can also be produced using m.o.s. transistors, the basic form using n-channel devices shown above left. Transistor TR₂ is diode-connected performing as a transistor with 100% feedback. Thus its drain current is still controlled by its gate-source voltage VGS, i.e.,
\[ I_\text{D} \approx g_{\text{m}} V_{\text{GS}} \]
where \( g_{\text{m}} \) is the forward transconductance. Forcing a current \( I_\text{D} \) into this diode-connected transistor causes \( V_{\text{GS}} \) to rise until a state of equilibrium is attained when \( TR_1 \) sinks the reference current. The gate-source voltage of \( TR_2 \) is identical to that of \( TR_1 \), due to the parallel connections. Hence if both have identical characteristics, \( TR_2 \) is also capable of sinking an identical current, the mirror current \( I_\text{R} \). A reasonably good degree of matching can be obtained between the n-channel devices on a monolithic chip, the mirror current being typically within 10% of the reference current.

A current mirror using monolithic p-channel i.e., \( I_\text{D} \), shown centre left, provides better performance than the n-channel type due to the ability to provide much closer matching of the characteristics of p-channel devices. Such a circuit provides an \( I_\text{D}/I_\text{R} \) ratio which is to a first order independent of \( V_{\text{DS}} \), as shown centre right. The graph above right shows that the normalized ratio of \( I_\text{D}/I_\text{R} \) is within 1% of its nominal value over a wide range of ambient temperatures and \( I_\text{R} \) values.

Further reading

RCA Solid State Databook

Cross references
Set 3, card 9.
Set 6, card 4.
Set 9, card 5.
Set 10, cards 1, 3, 7.
Set 12, cards 4, 7.
Set 15, card 6.
Set 16, card 1.
Set 20 card 0.

Circuit description
The circuit shown overleaf, with \( R = \infty \), is the basis of simulated thyrists, silicon controlled switches and simulated unijunction transistors. The action, with \( R = \infty \), can be deduced from the V-I graph shown, bearing in mind that the negative resistance slope is now \( -\infty \). Alternatively, the circuit above can be considered as follows. Initially \( TR_1 \) and \( TR_2 \) are in the non-conducting state. A positive voltage of about 0.7V on the base of \( TR_2 \) causes the transistor to conduct and lower its collector voltage. This causes \( TR_1 \) to conduct and providing \( TR_1 \) and \( TR_2 \) produce sufficient current through \( R_1 \) and \( R_2 \) respectively to keep the transistors conducting, then the action is self-sustaining with a voltage of approximately one \( V_{\text{BE}} \) across the circuit. The circuit can thus be used as a switch, triggered by a suitable voltage at either base. With \( R_1 = R_2 = 1k\Omega \), a value of 1.3mA for \( I_\text{R} \) was found to be the minimum which would maintain conduction. This value is as expected as the current \( I_\text{R} \) will split fairly evenly between \( TR_1 \) and \( R_1 \) and \( TR_2 \) and \( R_2 \). Since approximately 0.65V is required at the base of each transistor to maintain conduction, it will be provided by 0.65mA in each path. For high-speed switching it is important to prevent the transistors from saturating. Addition of the anti-saturation diodes shown prevents the collector voltages from dropping below \( V_{\text{BR}} \). The base lead diodes are not essential. Increasing \( R_4 \) increases the trigger voltage necessary and reduces the effect of trigger point transients. Transients in the supply line give rise to false triggering due to rate effect. This can be reduced as \( R_4 \) is reduced although this increases the holding current necessary.

Further reading
Negative resistance shown in dual e.f.t. device, *Electronics*, April 18, 1974, p.5E.

© 1975 IPC Business Press Ltd.
**Complementary emitter-follower**

The basic circuit comprises a complementary n-p-n/p-n-p pair operating under class-C bias, and is the basis for many audio power amplifiers. When a positive-going input signal exceeds about 0.7V, transistor $T_1$ will turn on, increasing its collector current which develops a voltage across the load $R_L$, but with a voltage gain of less than unity. At the same time $T_2$ is biased off. Similarly, a negative-going input signal turns $T_2$ on and $T_1$ off, and the circuit thus provides bidirectional currents through the emitter load. The base-emitter diode characteristic is non-linear at low voltages, resulting in cross-over distortion (approximately $2V_{BE}$) across the load. The resulting distortion on a sine wave input is shown in Fig. 1. Without an additional bias network, the effect of this distortion can be minimized by ensuring that $V_{DS} > V_{BE}$. Using both positive and negative power supplies permits operation down to zero frequency. For a single supply a capacitor is required in series with the load, to provide the base and collector currents of $T_2$ during negative-going input signals.

**Typical data**
- $V_{CC} = \pm 6V$
- $T_1$: BFR41, $T_2$: BFR81
- $R_1$: 330Ω, $R_2$: 1kΩ
- Signal frequency: 1kHz
- Fundamental/3rd harmonic output/input shown on graphs

**Component changes**
- $R_2$: Range from 100 to 1kΩ
- Variation in gain minimal
- Frequency: Up to 30kHz, little difference from lower frequency operation.
- Variation of mean current with input level in Fig. 2.
- $R_2$: Chosen to suppress parasitic oscillations.
- Alternative may be to keep interconnections very short to minimize series inductance.

---

**CMOS circuits**

**Description**
The CMOS inverter shown above comprises a p-type and n-type enhancement mode m.o.s. transistor on the same chip. $V_{DD} - V_{SS}$ may be in the range 3 to 15V. The pair is useful in digital circuits because of well-defined threshold that $V_{in}$ must exceed before the device turns on.

- n-type: $V_{GG}$ positive for ON
- p-type: $V_{GG}$ negative for ON

Where the output has to sink or source current, the pair can be envisaged as the series switches. Fig. 1 is a source condition, obtained for $V_{in} = V_{SS}$ and $V_{out} = V_{DD} - I_D R_D$ where $R_D$ is the output resistance of p-transistor in the on state. For $V_{in} = V_{ss}$ the n-type sinks current for Fig. 2; $V_{out} = I_D R_D$.

Basic I.C. package CD4007 contains one inverter and two complementary pairs with the drains unconnected. This permits a variety of interconnections: n-types are paralleled to increase sink current capability, Fig. 3.

p-types are paralleled to increase source current capability, Fig. 4. Fig. 5 is a dual bi-directional transmission gate where the two outputs and input may be interchanged for two inputs and one output. Note that the position of the transistors in the middle pair have been reversed.

The CD4049 package contains six inverters with current drive capability almost an order of magnitude greater than basic package. Parallel connection for increasing current sinking indicates typical current sharing for d.c. condition, Fig. 6.
Effect of bias (Figs. 5 & 6)
Rn varied until transistors just on the point of conduction. Graph shows 3rd harmonic distortion optimized by Rn. The above is a basic method of biasing to ensure class B or AB operation. Diodes D1, D2 may be chosen to achieve temperature independence of quiescent current.
Where increased current gain is needed for high power outputs, the Darlington pair of Fig. 8 (a) and compound emitter followers of (b) and (c) are useful, but may provide more difficult biasing problems.

Line driver (Fig. 7)
Driving 50-Ω cable with line capacitance slows pulse edges. Improved using complementary pair. Typical: fall time > 100ns but dependent on simulated cable capacitance (R0 = 50Ω, C: 3nF, t0 = 75ns).

Further reading
Williams, P. Voltage following.


Cross references
Set 7, cards 1, 3.
Set 20, card 1.

CD4016 i.c. package contains four analogue switches (transmission gates). Each switch comprises an inverter and a parallel pair of n- and p-channel transistors, Fig. 7. For a threshold of approximately 2V in each channel and control voltage 10V, the gate control voltage of the p-m.o.s. is 0V. If Vin > 8V, the n-channel will be open, but the gate-source voltage of the p-m.o.s. is -8V (greater than threshold) and signal is switched through because the VGS of each transistor never equals the threshold of the transistors, the full supply range can be switched through.

A.C. amplifier
Best linearity and voltage swing of Vout = VDD/2 and this is provided by the resistive connections below
Supply drain ≈ 2mA for 10V supply.

Further reading
Design Ideas with COS/MOS New Electronics, April 30, 1974.
I.C. op-amp has CMOS output Electronics, Sept. 19, 1974.

Cross references
Set 8, card 1.
Set 10, card 7.
Set 11, card 5.
Set 12, card 1.
wireless world circard

Set 20: Transistor pairs—9

Triples & mixed pairs

The principle of using transistors in pairs can often be usefully extended to the use of devices in triples, the resulting equivalent transistor having a current gain equal to the product of those of the individual transistors. In all such arrangements, two of which are shown above, the equivalent transistor has the same "polarity" as the input transistor.

The three n-p-n transistors in Fig. 1 act as a compound emitter-follower having a current gain of approximately \( e \), for large \( h_\text{ie} \), and is useful for driving currents of several amps from a driver stage delivering less than a milliamp. The complementary transistor triple in Fig. 2 is useful in voltage regulators as a low-dissipation series element.

The \( V_{\text{BE}} \) and \( V_{\text{CE}} \) values of the equivalent transistor being the lowest possible for a triple.

In this arrangement the temperature coefficient of only one transistor affects the output. The operating current in the input transistor will be very small, reducing its current gain. This effect can remove much of the benefit of using a triple instead of a pair. By using resistors as shown in Fig. 3 the operating currents in the earlier stages are increased and stabilized.

Thinking of the various pairs of devices discussed on other cards as elementary building blocks can prove a powerful method of developing more complicated circuit functions. For example, a long-tailed pair \( T_1 \), \( T_2 \), and \( T_3 \) may be used to drive a current mirror \( T_4 \) and \( T_5 \) as shown in Fig. 4 to produce a waveform generator which provides a symmetrical triangular output when driven by input pulses. This circuit uses the long-tailed pair to

wireless world circard

Set 20: Transistor pairs—10

Pot pourri

n-p-p/p-n-p simulation at high voltage

Optical couplers are used to provide fast high voltage switching with a simulated complementary pair. Transistors \( T_1 \) and \( T_2 \) are high-voltage n-p-n types: \( T_1 \) is on when \( T_2 \) is off and vice versa. With \( T_1 \) off, \( C \) charges to \( V_2 \), storing charge. This is used to turn \( T_1 \) on fast when the optical coupler operates.

Optical coupler provides the polarity inversion when \( T_3 \) and \( T_4 \) are driven by 5V pulses.

\( T_1 \), \( T_2 \), \( T_3 \): 2N2222

\( R_1 \): 270kΩ (10W), \( R_2 \): 1kΩ

\( R_3 \): 100Ω, \( R_4 \): 47Ω \( R_5 \)

R4: 680Ω, C: 10nF

D1: 6.8V zener, OC1: Monsanto MC01

Rise and fall times of around 2μs are claimed for components used.

Unijunction from bipolar pair

When the potential at \( E \) exceeds \( V_{\text{BE}} \) and \( V_X \), both transistors saturate, and \( R_3 \) is short-circuited. This condition is maintained for a potential at \( E \) down to \( V_{\text{BE}}+V_{\text{CEsat}} \) of \( T_2 \). Switching speed depends on maximum frequency of operation of the transistors. For \( T_2 \), \( T_3 \) silicon drift of \( V_{\text{BE}} < 3 \text{mV/deg C} \).

Shunt-series d.c. feedback pair

Current feedback via \( R_1 \) is proportional to \( T_2 \) collector current, and thus the circuit provides current-shunt
switch a defined current into two paths; which combined with a closely-matched current mirror permits the capacitor to be charged and discharged at the same rate when the charging current is varied. This concept of mixing elementary pairs of devices can be developed to build a single-supply operational amplifier using bipolar and m.o.s. transistor pairs, as shown in Fig. 5, having a unity-gain bandwidth of about 10MHz. The operational amplifier, which requires two CA3600E and one CA3046 packages, has three stages. The differential input stage uses two p-channel m.o.s. transistors $T_{R_1}, T_{R_2}$, the second stage uses an n-p-n bipolar transistor $T_1$, and the output stage is a complementary m.o.s. transistor pair $T_{R_3}, T_{R_4}$. The zener network, using two diode-connected transistors $D_1, D_2$ of the CA3046, feeds a p-channel current mirror $T_{R_2}, T_{R_3}$ that establishes a 400nA constant current in the input stage. This differential-input amplifier is loaded by four resistors, $R_2$ to $R_4$, and a bipolar current mirror, $T_{R_3}, T_{R_4}$, to provide optimum balance, any voltage offset being nulled with the potentiometer $R_p$. The current in the second stage, determined by $R_p$, is adjusted to equal the 400-$\mu$A first-stage current to provide similar negative and positive slew rates. The output stage is biased as a class-A amplifier by $R_4$ and may be driven to within a few millivolts of the ground rail. The overall voltage gain varies inversely with the load resistance which, as with a monolithic operational amplifier, would have a value of about 2k$\Omega$. Compensation requires inclusion of the feedback capacitor $C_f$, with $C_f$ added when using the operational amplifier as a unity-gain follower. In this configuration, $R_s$ and $C_f$ should be added to avoid the possibility of latch up and $D_4$ and $D_5$ added to the inputs to prevent negative-going input signals exceeding about 700mV which could also cause latch up. Typical values are: $V=+15V$; $R_1, R_3, R_4, R_5200\Omega \pm 1\%$; $R_2 20k\Omega \pm 1\%$; $R_4 11k\Omega \pm 1\%$; $R_6 7.5k\Omega \pm 1\%$; $R_7 10k\Omega$; $R_8 1k\Omega$; $C, 39\mu F; C_f 300\mu F$; $C_1 150\mu F$; $D_6, D_7 1N914$.

Further reading

negative feedback, which primarily controls the overall current-gain. Effective current gain is $A_i(1+\beta A_i)$ where $A_i$ is the current gain of the two stages, with $R_i$ connected between $T_{R1}$ base and ground. $\beta = R_i/R_1$. For $\beta = 0.1$, input resistance is $R_1/(1+\beta A_i)$ where $R_1$ is input resistance without feedback. Voltage gain is $R_1/R_2$ where $R_1$ is source resistance. Voltage gain can be increased by by-passing $R_c$, or by-passing the mid-point of the feedback resistor $R_f$.

Series-shunt d.c. feedback pair

In this connection, the voltage gain is now mainly affected by the feedback, and the input resistance is increased. Voltage gain is $A_i(1+\beta A_i)$ if $A_i$ is large. $A_i$ is the product of the gains of each stage, with $R_1$ connected from $T_{R_1}$ collector to ground, and $\beta = R_1/R_2$. Input resistance is $R_1(1+\beta A_i)$, where $R_1$ is effective input resistance of the first stage. Note: Biasing networks for those CE-CE amplifiers are not shown.

Common emitter pairs with composite transistors

For high voltage switching,
2. Shyne, N. A. Bipolar pair simulates unjunction,
4. Millman & Halkes,

Cross references
Set 20, cards 6, 7.
Set 12, card 9.