Unijunction voltage-to-frequency converter

Components
IC: 741, ±15V supplies
Tr: 2N2646
C: 10nF
R: 100kΩ
V*: 3.3V
Vin: see graph
Vo: see graph

Circuit description
With the removal of the unijunction transistor the circuit of Fig. 1 is simply an integrator which, with a positive Vin, gives a negative-going ramp Vo. The i.c. gain is sufficiently high then Vo is -VinRC. The unijunction serves to discharge the capacitor each time the voltage between e and b1 reaches the unijunction trigger voltage. The circuit therefore goes through the cycle shown right. Lower limit of -1.8V is the voltage at which the unijunction reverts to being an open circuit. Upper limit of -11.7V is arbitrary and is the result of choosing V*, R and C so that Vin=10V gave a frequency of 1kHz. With ±15V supplies this obviously cannot be extended beyond 15V.

The degree of linearity in the plot of frequency against Vin shown in Fig. 2 is quite high e.g. 10V gave 1kHz, 5V gave 498Hz, 1V gave 96Hz and 0.15V gave 16Hz.

Rise time of the output waveform (Fig. 1 circuit gave the waveform of Fig. 3) corresponding to the time when C is discharging, was 15μs i.e. 1.5% of the period at 1kHz, so the circuit cannot be recommended for much higher frequencies.

But from the expression for the downward ramp it is clear that the same frequency range can be achieved by the use of different values of R and C, and also of V*. It will, of course, be generally desirable to keep R relatively high to give high input impedance.

Multiplier voltage-to-frequency converter

Circuit description
The circuit of Fig. 1 is basically a closed-loop integrator-comparator square-triangle generator, comprising IC1 and IC2, with a multiplier (IC3) inserted in the loop to provide control of frequency. The value of the output voltage from the multiplier is a scaled version of the product Vdub and the control voltage Vc. Thus the amplitude of the signal to be integrated is directly proportional to a scaled value of the control voltage. A positive voltage applied to the inverting integrator charges C1 with its output end negative relative to the input end (held close to 0V by negative feedback through C4 and the high gain of IC3). Thus, Vout goes negative until the current it feeds through R3 exceeds the positive current in R1b, resulting in a negative current to the non-inverting input of the Schmitt comparator. Vout then rapidly switches to a negative value due to positive feedback applied to IC3, causing the multiplier output to go negative (Vo is always positive). The output from the integrator then starts rising until it reaches a positive voltage sufficient to make the comparator change.

Typical performance
Supplies: ±15V, ±8.5mA
IC1 XR2308, IC2, IC3 741
D1, D2, 3.3V Zeners R1, R2, 22kΩ
R3, R4, 330kΩ
R6, 68kΩ
R7, 100kΩ
R8, R9, R10 1kΩ
R11 2.2kΩ
C1, 22pF, C2 1nF
See Fig. 3 for graph of f/Vo and Fig. 2 for waveforms.
Circuit modifications
The modification shown in Fig. 4 to the circuitry around the unijunction transistor will provide a pulse train at \( V' \), the frequency being the same as that of the main circuit. The leading edge of this pulse train will correspond to the rising edge of \( V \) shown in Fig. 3. This \( V' \) will, of course, have the advantage of going much closer to zero in the time between the pulses.
An alternative voltage-to-frequency converter reported by Swarup and Banerjee is shown in Fig. 5. It is basically a unijunction oscillator with constant-current drive to the capacitor, this current being proportional to the voltage \( V_n \).
A linear relationship between \( V_n \) and the output frequency is claimed in the range 0 to 300Hz. The basic action of the unijunction oscillator and modifications to reduce the discharge time of \( C \) are fully described in Circard's set 3 (waveform generators) card 4.

Reference
Swarup & Banerjee, Linear voltage to frequency and voltage to pulse width converters using unijunction transistors. *Int. J. Electronics*, vol. 32, 1972, pp. 377-81.

Further reading

Cross references
Set 2, card 1
Set 3, cards 1, 5
Set 13, card 9
Set 17, cards 3, 6
Set 21, card 4
**Delta-sigma voltage-to-frequency converter**

Typical performance of Fig. 1
IC1: 741, IC2: 1 x CD40134E, IC3: 1 x CD4011AE
Supplies: VDD: +10V, VSS: -10V
R1, R2: 100kΩ, R3: 1kΩ
C1: 100nF
Clock: 6V positive pulses, p.r.f.: 1kHz, duty cycle: 10%
See Figs 4 and 5.

Circuit description
A class of voltage-to-frequency converter gives an output in the form of a pulse train where the repetition frequency is directly proportional to the instantaneous value of the control voltage but the pulses are generated asynchronously. The output from a delta-sigma encoder is again a pulse train but its average pulse repetition frequency is proportional to the control voltage and the pulses are generated in synchronism, with a clock pulse waveform.

**Sinewave voltage-to-frequency converters**

Typical performance
Supplies: ±15V
IC1, IC4: 741
TR1, TR2: 1/6 × CD4007AE
R1: 150Ω
R2: thermistor type R13
C1, C2: 100nF
Vout1: 520mV pk-pk
Vout4: 1.04V pk-pk
See graph for f/Vo (Fig. 2)

Circuit description
This circuit (Fig. 1) is one of the many forms of Wien bridge oscillators with TR1 and C1 forming the series-connected frequency-dependent arm with TR2 and C1 forming the parallel connected arm of the bridge. For oscillation to occur the closed-loop gain must be unity, the required amount of gain being provided by the inverting operational amplifier ICa, the gain being determined by the ratio R3/R1. With this configuration the common-points of the frequency-determining resistors are connected to the virtual-earth inverting input of IC1. This is a convenient arrangement for replacing these resistors with elements which have a resistance that can be controlled by a ground-referred voltage source. In the above circuit these elements take the form of a pair of matched c.m.o.s. transistors which have gate-source resistances that depend on the control voltage Vo. Linearity of the voltage-to-frequency conversion characteristic is not particularly good over a wide range of frequencies but may be adequate for many purposes where only a restricted frequency range is required. Resistance of the f.e.t.s depends on their drain-source signal voltages as well as on the control voltage Vo but this can be reduced, and the linearity of f.e.t. resistance-to-control voltage characteristic linearized, by using local feedback around the f.e.t.s as shown in Fig. 3, where R3, R4, R6 and R7 may be of the order of 1MΩ.

If the closed-loop gain deviates from unity the amplitude of
inverting input of IC\textsubscript{2} is a virtual earth, \( V_{\text{in}} = V_{\text{ref}} \), and \( f_i = f_{\text{ref}} R_1 \) where \( k \) is pulse duty cycle required to keep \( I_1 = I_0 \). Equating these currents gives
\[
\frac{V_{\text{in}} - V_{\text{ref}}}{R_1} = \frac{V_{\text{ref}}}{R_2}
\]
where \( k \) is the ratio of the output pulse repetition rate (f) to the clock pulse repetition rate (f\textsubscript{c}). Hence
\[
f = \frac{R_2 f_c}{R_1 V_{\text{ref}}}
\]
By making \( R_2 = R_1 \) and \( V_{\text{in,max}} = V_{\text{ref}} \) the maximum output p.r.f. is that of the clock source and the average output pulse rate is proportionally smaller for smaller values of \( V_{\text{in}} \).

The arrangement of Fig. 2 uses an analogue transmission gate to realize the switch S. IC\textsubscript{3} is a precision comparator which determines when the reference voltage source is to be switched to \( R_s \) by monitoring the polarity of the output from the integrator IC\textsubscript{1}. This switching action is synchronized to the clock pulses by using gating pulses derived from the output of a D-type flip-flop which receives the comparator's output at its data input. The circuit of Fig. 1 is that to which the typical performance data refers. This is a simplified form of the arrangement previously discussed with the electronic switch, external reference source and precision comparator removed. (Note that whilst the integrator used both positive and negative supplies the D-type flip-flop is connected only across the positive supply.) As the D-type produces output pulses equal in amplitude to the VDD rail voltage only when its data input receives a positive pulse from the integrator, a separate switched reference is not essential. Also, the precision comparator can be replaced by \( R_s \) which limits the negative-going pulses to the data input of the D-type which acts as the comparator. Average frequency/V\textsubscript{e} graph (Fig. 4) has a linearity of ±0.1% up to \( f = f_c \) when \( V_e = V_{\text{DD}} \). No further increase in frequency is possible except by increasing the p.r.f. of the clock source. Output pulse waveform of Fig. 5, inverted by IC\textsubscript{3}, is that of \( V_e = V_{\text{DD}}/2 \), the dashed pulse only being present when \( V_e \) is raised to \( V_{\text{DD}} \).

The circuit of Fig. 6 is another simplified form of the more general system where the comparator had been omitted and the electronic switch is realized by a junction f.e.t. The positive supply rail is used as the voltage reference source and the output is taken from the \( \Omega \) terminal of the D-type flip-flop IC\textsubscript{3}, which is a complementary m.o.s. version to conserve power. This circuit is capable of linear v-to-f conversion within ±0.05% almost independently of temperature changes. Typical values are:
\[
\begin{align*}
V & = \pm 2.7V \\
I_{\text{CC}} & = L 42500 \\
I_{\text{CC}} & = \frac{1}{2} \times MC14013CL \\
R_1 & = 10k\Omega \\
R_2 & = 5.6M\Omega, C_1 = 100nF \\
Tr_1 & = 2N4693 \\
\end{align*}
\]

Further reading
Defreitas, R. Low-cost way to send digital data, Electronics Design, pp. 68-73, Jan. 18.
Ross, P. J. Simple accurate voltage to frequency converter, Int. of Physics E, vol. 7, pp. 706/7.

oscillation will vary with time, so as to avoid extremely precise setting of gain is it initially set slightly high and then automatically controlled. The a.g.c. being achieved with a thermistor in the above circuit. In addition to the use of local feedback on the f.e.t., these elements could be connected to form only part of the frequency-determining resistances with bulk of the values in the form of series-connected resistors which would tend to swamp out the non-linearities in the f.e.t. whilst restricting the range of control.
The f.e.t.s could be replaced by matched photodiode resistors or by bipolar transistors which are switched on and off by current pulses to the bases, the mean collector-emitter resistance being controlled by the pulse repetition frequency. A voltage-to-frequency converter using a pair of all-pass active networks is shown in Fig. 4. These networks, using \( A_1 \) and \( A_2 \), have a constant gain magnitude but a phase shift given by \( \phi_1 = 2\tan^{-1}(\omega CR_1) - 180^\circ \) and \( \phi_2 = 2\tan^{-1}(\omega CR_2) - 180^\circ \) respectively. With the 180° phase shift through the a.g.c. amplifier \( A_2 \), the current will oscillate at a frequency
\[
1/(2\pi C \sqrt{R_1 R_2})Hz
\]
which shows that a voltage-to-frequency conversion may be obtained by making \( R_1 \) or \( R_2 \) or both voltage-dependent resistors, e.g. f.e.t.s. For a wide range of frequency variations \( R_1 \) could be a voltage-dependent resistor and \( R_2 \) a range-switching resistor. For \( R = R_1 = R_2 \), the outputs are generated with a controllable phase difference \( \phi = (\phi_1 - \phi_2) = -2\tan^{-1}(\omega CR) \).

Circuit of Fig. 5 uses two active integrators and two multipliers to produce a voltage-to-frequency converter having quadrature outputs that can have a very fast response to changes in \( V_e \) provided a fast a.g.c. system is added to the basic circuit. Under this condition the circuit will oscillate at a frequency which allows the double integration to take place without changing the amplitude of the signal. Multiplier \( M_2 \) provides an output \( V_1 = V_e \), \( V_{\text{out}}/10 \) and \( M_1 \) gives an inverted output, to maintain the loop phase shift, of \( V_{\text{e}} = -V_e \), \( V_{\text{out}}/10 \). With the 1/10 scaling factor, frequency of oscillation is \( 20\pi/vRC \). Multiplier \( M_2 \) could be replaced by an inverting operational amplifier. Further reading
**Multiphase voltage-to-frequency converter**

Circuit description
This is a twin circuit based on R-C integration to provide the triangular waveform and level sensing to provide a square wave which operates an electronic switch controlling polarity applied to the integrator. Outputs X and Y are cross-connected giving control of electronic switches TR2 and TR1 respectively and triangular waveforms which are 90° out of phase. IC3 and IC4 provide high open-loop gain, and at low frequencies provide faster switching than comparators. VOUT is a positive-going ramp until TR1 changes state and this occurs at the instant of zero-crossing of VOUT, which then switches IC3. VOUT then ramps down and changes the state of TR2 when a zero-crossing point is reached. The time taken to go from say a positive peak to zero level depends on the RC time constant and the value of VCONTROL. It should be noted that as no amplitude controls for the output are imposed, one or other of the integrators (no. 11) must be grounded for continuous output at the output terminal. Output is disabled if this terminal is taken to logic high or open-circuited. Graphs opposite indicate linearity over a restricted range for each capacitor value, and waveform deteriorates at very low values of C1 and thus at high frequencies.

**Monolithic voltage-to-frequency converters**

Circuit description
An emitter-coupled astable multivibrator uses a single capacitor for timing. The circuit has high switching speed because charge storage effects are avoided by using the transistors in a non-saturated mode. This circuit is the basis of the above medium-scale integration package, where variable frequencies are obtained by charging the external capacitor at different rates via an internal voltage-controlled current source. The I.C. package contains two identical networks, but if only one is being used, it is essential that both ground connections (pins 8 & 9) are earthed to ensure earthing of the substrate and good isolation. The enable terminal supply voltage 4.5 to 6.5V, frequency maintained constant.
will reach saturation before the other output reaches its zero crossing point.

**Circuit modifications**

- Use a switched integrator rather than a switched gain amplifier. This makes IC₁, IC₃ redundant (Circard Set 3, No. 5). LM3900 quad package may be now arranged to provide the two outputs.
- Phase shift oscillator (above) provides three outputs with 60° phase relationship. IC₁-IC₃: 1/6 × CD4049, R: 10kΩ, C: 2700pF, frequency: 13kHz.
- As the c.m.o.s. gates are being used in their linear region, both the n- and p-type transistors will be conducting and hence power consumption will depend on the supply voltage. Typically the total current drain from the supply for the above network is

\[ V_{DD} - V_{SS} = 3V, \quad I_C = 0 \]
\[ V_{DD} - V_{SS} = 10V, \quad I_C = 12mA \]
\[ V_{DD} - V_{SS} = 15V, \quad I_C = 30mA \]

Frequency may be controlled by substituting voltage-dependent resistors for each \( R_i \) and maintaining as close a ratio as possible between the \( R \) values. Frequency is approximately \( 1/3RC \).

Note that with the CR values necessary for 60° phase shift at a specific frequency, the output of each buffer stage is attenuated by about one half and hence the minimum gain of each stage must be > 2.

- An alternative arrangement is shown above right, using similar c.m.o.s. buffer inverters. In this case the resistor ratio is critical and theoretically in infinite gain amplifiers, \( R_i \), and a much better approximation to sinusoidal outputs is obtained from each buffer, again phase shifted by 60°. Typical values \( R_1 \): 100Ω, \( R_3 \): 33 to 39kΩ, C: 2700pF, \( V_{DD} - V_{SS} = 6V \), frequency 1kHz.

These buffers have gain-frequency responses which give higher gains for lower supply voltages. Typically 50dB at \( +3V \) up to 100kHz and 30dB at \( +10V \) up to 100kHz. Hence since the gains are finite, then \( R_i \) must be less than \( R_i/2 \). But at the lower values of the supply range 3 to 15V, some flexibility of this value, between each \( R_i \) is permitted. At higher levels the ratio is more critical, \( R_i \) may be replaced by \( f.e.s. \) employed as v.c.r. to obtain a restricted frequency range.

**Further reading**

AN-88 CMOS Linear Applications, National Semiconductor, p. 170.

**Cross references**

Set 11, card 6.
Set 8, card 1.

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**Components (circuit above)**

Supply ±10V
IC₁, SH54S124N IC₃ LM301
R₁, R₃ 10kΩ
R₂, R₄ 100kΩ
C₁, C₃ 1μF
C₄, C₅ MV16408

IC₃ is connected as a non-inverting amplifier with a voltage gain of two, so that the biasing voltage in this case is twice the control voltage. This gain can be altered for appropriate voltage range. A claimed frequency range of 2 to 20MHz using varactors MV1403 and MC1456 for IC₄ is documented in the referenced literature.

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**Components (circuit right)**

IC₄ LM566, SE/NE566
General-purpose voltage-controlled oscillator.
C₅ 4.7nF C₆ 0.047μF
R₄ 4.7kΩ R₅ 10kΩ
Maximum sweep rate 1MHz
\( R_i \) and \( C_i \) are the frequency range determining components. For a fixed value of \( C_i \) 10:1 variation in frequency is possible via a variable input at \( V_{fontrol} \) which should be within the range 3 to 3.5V for \( V_{ce} = -6V \).

The above values provide for a maximum free-running frequency of about 10kHz for \( T_r \) off. For \( V_{ce} = -3V \), \( T_r \) is saturated, hence increasing timing capacitor 10 times, free-running frequency is then approximately 1kHz.

Control voltage measured between pins 2 and 3 should be in the range 0 to 0.25\( V_{ce} \). (It is this voltage divided by \( R_i \) which defines capacitor charging current.) Frequency is

\[ \frac{2(V_{out} - V_{control})}{R_iC_iV_{ee}} \]

**Further reading**

Klein, E. Medium-scale integration for instrumentation and control, *Semiconductors* (Motorola) vol. 2 no. 1 1971, p. 20.

Signetics: SE/NE566 function generator.

**Cross references**

Set 17, card 3
Set 8, card 9
Linearized voltage-to-frequency converter

**Components**
- R 100kΩ, C 0.22μF
- IC 741
- Unijunction V-f converter—see over, centre. Monostable—see over, right V<sub>10</sub> 0→10V

**Performance**
- Graphs of V<sub>f</sub> and V<sub>f</sub> are shown in Figs. 2 and 3. Graph V against V<sub>f</sub> corresponding to open-loop V-f conversion, is shown in Fig. 2. with V<sub>10</sub> against V<sub>f</sub> shown in Fig. 3. Linearity achieved was better than 0.5%—clearly much better than the open-loop performance.

**System description**
- If the loop gain of a closed-loop system is high then the effect of non-linearities in the forward path is much reduced. In this case we have a highly non-linear V to f<sub>0</sub> converter and an integrator/error detector is then included to provide the feedback. In d.c. terms, the integrator can be regarded as having infinite gain since for finite input voltage the output voltage after infinite time is infinite, ignoring the effect of saturation. Alternatively: \( AV = \frac{1}{RC} \int_0^T V_{in} dt + \frac{1}{RC} \int_0^T \frac{1}{5} dt \)
- The steady-state condition of constant V<sub>f</sub> can only occur when V is constant and this occurs when V is zero i.e. when the integrator is reset. The integral of the input signal and the integral of the feedback signal exactly cancel. Hence exact correspondence between V<sub>10</sub> and V<sub>f</sub> can be expected if the integrator and feedback signal are “perfect”. Immediate improvement in the system would be obtained if an i.e. with much lower input current requirements were used e.g. 308. Further improvement would be obtained by the use of a low-loss capacitor. The

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Linear voltage-to-frequency converters

**Circuit description**
- The circuit comprises an integrator whose output ramps toward positive and negative target values defined by diodes D<sub>3</sub> and D<sub>4</sub> i.e. the potential at the non-inverting input of comparator IC<sub>3</sub> is V<sub>0f</sub> = V<sub>D</sub> + V<sub>D</sub> + V<sub>B</sub> (or V<sub>D</sub>) (approx. +9V). When the transistor is off (V<sub>0f</sub> negative), capacitor current is

\[
I = \frac{V_{control}}{R_2} \left( \frac{R_2}{R_2 + R_4} \right) \frac{1}{R_3 + R_4} \tag{1}
\]

When Tr conducts, I is

\[
I = \frac{V_{control}}{R_2} \left( \frac{R_2}{R_2 + R_4} \right) \frac{1}{R_3 + R_4} \tag{2}
\]

For equal slopes at the triangular output, V<sub>0f</sub>, the current magnitudes are equal, provided

**Typical performance data**
- Supply ±15V
- IC 741S IC<sub>n</sub> LM311
- Tr, ME4002
- R<sub>1</sub>, 68kΩ, R<sub>2</sub> 22kΩ, R<sub>3</sub> 33kΩ
- R<sub>4</sub> 1kΩ, R<sub>4</sub> 3.3kΩ
- R<sub>5</sub> 12kΩ, R<sub>6</sub> 4.7kΩ all ±5%
- C<sub>1</sub> 100μF, C<sub>2</sub> 1nF
- D<sub>1</sub>, D<sub>2</sub> reference diodes 6.8V e.g. BZY88
- V<sub>control</sub> range 0 to 10V
- Triangular output ±8V peak
- Frequency range 30Hz to 33kHz

\[
R_1 = 1 + \frac{R_2}{R_4}
\]

If V<sub>control</sub> is positive, Tr is on, and integrator output rises towards +9V at which level the comparator IC<sub>3</sub> switches over to make V<sub>0f</sub> negative, bringing Tr<sub>n</sub> out of conduction. C<sub>2</sub> changes according to the first equation, and integrator output ramps towards −9V, when comparator again changes state.

**Components**
- C<sub>n</sub>, R<sub>2</sub>, R<sub>4</sub> form a phase-advance network to compensate for the switching delays of IC<sub>2</sub> and Tr<sub>n</sub> at the higher frequencies. The invert mode of Tr<sub>n</sub> provides a very low collector-emitter drop (few millivolts), i.e. the effect on the second equation is neglected.
c.m.o.s. monostable was included to give an output pulse train of well defined height and width and overall shape. A better $t'_o$ to $t_o$ converter could have been used. It should be noted that the overall characteristics are now dictated by the feedback signal and the integrator so that forward path changes, causing changes in $t_o$, will be completely cancelled, apart from transient effects. Changes in the shape of $t_o$, e.g. impulse height and width, will however have an effect on $t'_o$, although not linearly.

System modification
Effectively, the combination of the monostable and integrator is an $f'_o$ to $v$ converter. The system could therefore be changed to that shown in Fig. 4. $K$ would be chosen to be sufficiently high such that the linearity of the overall system is equivalent to that of the $t$ to $v$ converter. This is only satisfactory if the shape of the $f'_o$ pulses is satisfactory.

Element description
The circuit of Fig. 5 shows the detail of the unijunction $v$ to $f$ converter (card 1) used. The opto-elements are included to show that their inherent isolating properties can be used not least to produce a very non-linear $v$ to $f'_o$ characteristic. This is because $D_2$ requires approximately 1.6V to conduct and is due to the fact that the charging current is not linearly related to $I$. Resistor $R_3$ is included to protect the transistor and $R_4$ is large to produce a sufficiently large pulse to trigger the monostable. Resistor $R_5$ may be reduced to allow much lower input voltages to be used. The limit is set by the opto-diode input current. Any opto-isolator may be used e.g. TIL112.

Linearity is better than 0.5% over the range of control voltage, 0.1V to 8V, based on deviation from 6V value.

Component changes
This slew rate is typically 10V/μs. If 741 used, slew rate (0.5V/μs) restricts higher frequency to which linearity is maintained (see graph).

Range of $C_3$: Typically 47 to 200pF. Frequency variation shown on graphs. Frequency is power supply dependent, hence need for good stability of supply. Vary mark/space ratio of output at $V_{os}$ by $R_3/R_2$ ratio change; this also modifies frequency.

Range of $R_3$, $R_2$ 22 to 68kΩ
Range of mark/space 1:1 to 1:3.

Circuit modifications
- A variable output voltage is obtainable via the circuit shown in Fig. 1. Comparator hysteresis can be changed by varying the fraction fed back via a potentiometer $R_V$. This will control the output amplitude. The triangular output is shaped by the circuit of Fig. 2. Potentiometer $R_V$ is adjusted for a minimum even-harmonic content, to provide an approximate cissoidal wave form at $V_{os}$.

- The field-effect transistors of Fig. 3 provide a similar switching action to $Tr_5$ in first circuit to provide the integrator capacitor current charging paths. $IC_3$ as an integrator employs a speed-up network of 150pF in series with 10MΩ resistor.

Transistors $Tr_5$ and $Tr_9$ are controlled by square-wave output from the Schmitt circuit of $IC_4$. When $Tr_5$ is on, $Tr_9$ is off and $C_5$ charges via $Tr_5$ and 10kΩ resistor. With $Tr_9$ off, and $Tr_5$ on, current reverses through the capacitor with magnitude defined by $V_{os}$ and 10kΩ resistor. $V_{os}$ should be adjusted to provide a symmetrical square-wave output when $V_{os}$ is 5mV. Input control voltage range: 5mV up to 5V. Frequency range 10Hz to 10kHz.
Diode-pump voltage-to-frequency converter

Components
Supplies: ±15V
IC: 748C
R₁: 12kΩ, R₂: 3.9kΩ
R₃: 10kΩ, R₄: 4.7kΩ
C₁: 4.7μF, C₂: 1nF
C₃: 33μF, C₄: 56pF
C₅: 500pF
D₁ to D₄: 1N914

Performance
Vin: 0 to +4.00V
Output pulse train: pulse width about 20μs swinging from +14V to -14V with a maximum frequency of around 14kHz, corresponding to a mark-space ratio approaching 3:1.
Linearity better than 0.3% over two decades.

Circuit description
Elements R₁, R₂, D₁, D₂, and C₅ are not basic to the action of this circuit and will be ignored initially. Suppose the i.c. output is sitting at +14V. Then C₃ will have been charged to this level via D₂.
However as C₅ charges via R₃ under the influence of Vin, the negative terminal of the i.c. eventually reaches 0V and the amplifier output swings negative. The network comprising C₄, R₄ and C₅ provides sufficient positive feedback to make this swing very rapid—hence the use of a high speed op-amp. Capacitor C₅ then deposits its charge via D₃ into C₄ in a diode pump fashion thereby lowering the voltage across C₅. However the

Differential input voltage-to-frequency converter

Components
Supplies: ±15V
IC₁: 741, IC₂: NE555
Tr: 2N5457
R₁: 270Ω
R₂: 1.2kΩ
R₃: 47Ω
C₁: 1nF
C₂: 22nF
D₁, D₂: 1N914

Circuit description
The above circuit is of a form published by Woodward but with what appear to us as corrections, although we have to admit to not achieving the performance claimed in his article, viz linearity better than 0.05% from 10Hz to 10kHz.
The results we achieved are shown roughly in Fig. 2, measured linearity being 0.15% over the two decades, 100Hz to 10kHz.
Pin c of IC₂ is the R (reset) terminal and its action is not necessary in a brief explanation. Pins a and b are the trigger and threshold terminals of the i.c. When the C₅ capacitor voltage goes below the trigger potential, V₅/3, the output swings high, and when the voltage exceeds the threshold voltage, 2V₅/3, the output swings low—see waveforms of

Fig. 2
Fig. 3

The basic principle is that of charge dispensing in which a current proportional to a voltage is balanced by the periodic charging of a capacitor to a precise voltage. In this case, the current through the f.e.t. is fixed by the input voltage at Vin/R₁. This current flows for time T as a result of the charging of C₁ from V₅/3 to 2V₅/3. Thus

\[
V_{in}, T = \frac{C_1 V_0}{3}
\]

and

\[
f_0 = \frac{3V_{in}}{R_1 C_1 V_0}
\]
positive feedback network consists of elements with a short time constant and the voltage on the positive terminal quickly becomes less negative than the negative terminal voltage and so the amplifier voltage swings back to $+14$V. In the $-14$V period the circuit is acting rather like a monostable, the delay being fixed by the $C_3$, $R_4$, $C_6$ network and by the $R_2$, $C_5$ network. Because there is again positive feedback the rising edge will be equally sharp but the period will be difficult to define accurately, partly because of the complexity of the CR networks and partly because two voltages both going in the same direction (positive) are being compared. This, however, is not serious since the pulse width does not affect the amount of charge on $C_3$, and it is this charge which is being balanced by the current in the input network.

The maximum frequency we obtained was close to the limit of the op-amp but the mark-space ratio could have been made even lower if required by reducing $C_6$, $R_4$, or lengthening the time constant of $C_6$, $R_4$, $C_5$. The network comprising $R_1$, $R_3$, $C_4$, and $D_2$ prevents the device from locking into a saturated condition by too large an input voltage (positive). Diode $D_3$ prevents the negative input terminal being overdriven by a negative input voltage.

Circuit modifications

- A high-speed comparator would be preferable to an op-amp which was used in our experiments.
- The pulse width does not theoretically affect the result but the pulse height does. A c.m.o.s. buffer amplifier could be included to give a well-defined output pulse height—see reference 2.

This expression is valid so long as $T$ is large compared with the pulse width. When the output goes high $C_2$ charges via $R_3$ and $D_2$ from $V_a/3$ toward $V_a$. During this period $D_3$ is reverse biased and at the same time $C_1$ is providing some current to the f.e.t. When $C_2$ reaches $2V_a/3$ the output goes low, $D_2$ conducts, $C_1$ and $C_3$ share the charge on $C_2$ and the parallel combination discharges linearly through the f.e.t. Diode $D_3$ is reverse biased in this period.

The sharing of the charge between $C_3$ and $C_4$ causes the sharp drop in the $C_4$ voltage when $2V_a/3$ is reached. The discharge is linear because the f.e.t. current is fixed by the input voltage. The results obtained required adjusting of the op-amp offset voltage to zero. Common-mode rejection ratio is independent of input resistor match and is dictated by the op-amp used. However, common-mode voltage should not exceed $\pm2V$.

Component changes

The charging time depends on $C_2/R_3$ and should be short without $R_3$ being so low as to overload $IC_3$. This is not difficult to achieve since it is the open collector terminal which is used to charge $C_4$. Capacitor $C_5$ serves to cut off $D_3$ whilst $C_3$ is charging, so its value is not critical. Generally speaking though it should be less than $C_3$ to minimize the drop in $C_3$ voltage when $D_1$ starts conducting again, thereby keeping the slope of the downwards ramp as large as possible and clearly defining the time at which the voltage drops below $V_a/3$. Actually, $C_1$ and $D_1$ can be removed altogether without complete failure of the circuit, although linearity and output pulse shape are affected.

Diodes $D_2$ and $D_4$ can be any general-purpose diodes unless very high speed operation is required.

Reducing the values of the op-amp input resistors and choosing a suitable op-amp will allow values of $V_{in}$ in the millivolt region to be used to give the same output frequencies.

Circuit modifications

Any circuit which will successfully draw constant current from the junction of $C_4$ and $D_4$ will produce the same result and such a circuit is shown in Fig. 4. The photodiode current is proportional to light intensity so an intensity-to-frequency converter would be produced by this arrangement. The differential input aspect is lost, however, unless one puts a second photodiode, connected the opposite way round, across the one shown.

Reference