I.C. package modulators

Typical performance
Supplies: ±10V, 10mA
\( I_{CC} \): MC1445L
\( R_1 \): 47Ω
\( R_2 \): 220Ω
\( C_{1} \): 100nF

Amplitude modulator
Vo 2V d.c.
\( V_{IN} \) (carrier) 130mV pk-pk
\( f_c = 1 \text{MHz} \)
\( V_{IN} \) (modulation) 1.3V pk-pk
\( f_m = 10 \text{kHz} \), to produce maximum useful modulation depth of 78%.

Vout (pin 1 or 7) 800mV pk-pk unmodulated, see waveform opposite.

Balanced modulator
Vo 2.5V d.c. to balance out carrier
\( V_{IN1} \) (carrier) 130mV pk-pk
\( f_c = 1 \text{MHz} \)
\( V_{IN2} \) (modulation) 2.4V pk-pk (max)
\( f_m = 10 \text{kHz} \)
Vout (pin 1 or 7) see waveform opposite.

Circuit description
Many integrated circuit packages are available either in the form of purpose-designed modulators for producing a.m. or d.s.b. outputs or in the forms which can be readily adapted to these applications. An example of the latter type is the gate-controlled, two-channel-input wideband amplifier shown left. This integrated circuit consists of a pair of differential-input amplifiers having a constant current switched between them under the control of a gating signal which cuts off one amplifier when the other is conducting. The output from each of these amplifiers is available via low-output-impedance Darlington emitter followers. Although the gating signal would normally be at t.t.i-compatible logic levels, the characteristics of the gate circuit allows the i.c. to be used as an amplitude modulator when connected as shown. Although the voltage/gain/gate voltage characteristic is far from linear over the full gate voltage range, it is virtually linear over a range of a few hundreds of mV with respect to a suitable d.c. bias. This bias is obtained by connecting a coarse/1984 control (R3, R4) between the gate (pin 2) and ground. The low-frequency modulating signal is superimposed on this bias by coupling it to the gate through C2 and the carrier input is coupled via C1 and R1 to either of the input channels, pins 3 or 6 (as shown) or pins 3 and 4 (unused in circuit shown). The amplitude modulated output is available at either output, pin 1 or pin 7. With defined input signal levels, the output modulation depth may be varied using R2 and R3.

Linear amplitude modulator

Typical performance
Supplies: V±15V±7.5mA, -9.3mA; \( V_{IN} \pm 5V \) 0.75mA
\( A_1 \): 741
\( R_2, R_6, R_7, R_8, R_{U1}, R_{U2} \): 10kΩ
\( R_5 \): 100kΩ
\( R_9 \): 33kΩ
\( R_{U2} \): 4.7kΩ
\( R_8 \): 6.5kΩ
\( R_{U1} \): 22kΩ
\( R_4 \): 39kΩ
\( V_{E} \): -5.5V

\( V_{IN} \) (carrier) 8V pk-pk square wave at \( f_c = 10 \text{kHz} \).
\( V_{IN} \) (modulation) 1.2V pk-pk sinewave at \( f_m = 1 \text{kHz} \) to produce a.m. output with 100% modulation (see graph right) Vout see waveforms opposite for 100% modulation.

Circuit description
The modulating signal (\( V_{IM} \)) is applied via \( R_9 \) to the inverting, summing operational amplifier \( A_1 \) and receives a gain of \(-R_7/R_5 \). Although this input is bipolar in nature the output from \( A_1 \) is not permitted to go more negative than 0V due to the presence of a d.c. bias obtained from the -V rail via \( R_2 \) \( V_2 \) which receives an inverting "gain" of \( R_7/R_5 \). This composite, positive signal is applied over separate paths to the inverting input of \( A_2 \) (via \( R_8 \) and \( R_{U2} \)) and to the non-inverting input of \( A_2 \) (via \( R_4 \) and \( R_{U1} \)). The junctions of these pairs of resistors are connected to ground through \( Tr_2 \) and \( Tr_3 \) when these "chopper" transistors are switched on by the square-wave carrier \( V_{IN2} \).
A double-sideband suppressed-carrier signal may be produced by applying the carrier simultaneously to both channels of the input differential amplifiers which then have their outputs cross-coupled. The resulting balanced modulator is as shown overhead but with pin 5 earthed and the junction of $R_3$ and $C_1$ taken to pins 6 and 3. If the carrier has sufficient amplitude to switch these channels completely off and on, the modulating signal is switched between the channels at the carrier frequency, which is equivalent to multiplying the modulating signal by a switching function—the required condition for producing a pair of side-frequencies and suppressing the carrier. If a reduced-amplitude carrier is required, this can be produced by slightly changing the d.c. bias applied to the gate terminal by means of $R_4$.

**Component changes**

Useful range of supply: ±4 to 12V

Maximum useful carrier input $\approx 280\mu$V pk-pk producing unmodulated carrier output of $\approx 3.3V$ pk-pk $f_a$ (max) $= 75$ MHz Maximum load current $\approx 25$ mA. Examples of integrated circuits purpose-designed as balanced modulators are the MCI596G and the SL640C. These packages are essentially intended to replace diode-bridge (or ring) modulators with transistor double-balanced modulators to overcome the disadvantages of the former type of less than unity gain the need for a high level signal at one input and the need to use up to three transformers. The inherently good switching of the monolithic transistors ensures that excellent carrier suppression is obtained with little need for balancing by external components when the devices are used as double-sideband suppressed-carrier generators.

An arrangement of the SL640C for this purpose is shown above. Typically, $V = \pm 6V$; $R_1, R_2, 10k\Omega$; $R_3, 330k\Omega$; $C_1, C_2$ and $C_4$ should have low reactance compared with the source and output resistance, except for high frequency applications (i.e. $f_2$ approaching 75 MHz) where the modulation source resistance should be low and $C_4$ of comparable reactance.

In the absence of a carrier input, $T_3$ is held off by the reverse bias on its base from the $-V_{BB}$ supply via $R_4$ and $T_4$ is held in the off state by the reverse base bias from the $+V_{BB}$ rail through $R_{11}$. With $R_{22} = 3R_1$ and $R_{11} \approx 3R_4$, a square-wave carrier having a peak value slightly less than $V_{BB}$ is sufficient to overcome the reverse base voltages in the transistors and drive them hard into conduction. On positive half-cycles, the carrier, $T_3$, remains off and $T_4$ is switched on causing the junction of $R_1$ and $R_11$ to fall to within $V_{CREAT}$ of ground, effectively removing the modulation input to $A_2$. On the following negative half-cycles of the carrier, $T_4$ switches off and $T_3$ switches on taking the junction of $R_2$ and $R_{11}$ to within $V_{CREAT}$ of ground, effectively removing the modulation input to $A_2$. Thus, the signals applied to $A_2$ and $A_3$ are in the form of the summing amplifier which has been chopped at the carrier output signal which is the linear sum of its inputs. The output waveform will contain the original carrier frequency and its harmonics with sets of upper and lower sidebands centred around each of the carrier components. For a pure amplitude-modulated wave the output waveform should be passed through a bandpass filter centred on the input carrier frequency and having a bandwidth sufficient to accommodate the sidebands of the highest modulating frequency. As shown overhead, modulation depth is a linear function of the modulating signal input voltage, 100% modulation being achieved when the peak value of the modulation at $A_2$ output is equal to the d.c. bias at that point.

With the low-cost operational amplifiers shown the circuit can function with carrier frequencies up to about 25 kHz. Higher carrier frequencies can be produced if operational amplifiers having a high gain-bandwidth product than the 741 are used, and in principle, the circuit should operate with carrier up to several MHz. With suitable adjustment of the input signal levels and bias voltages the circuit can work from supplies between about ±4 and ±18 V. For the circuit as shown the maximum and minimum useful carrier-frequency inputs are approximately 11 V pk-pk and 6.4 V pk-pk respectively.

Further reading

Modulator using precision rectifiers

Circuit description

K is a summing amplifier with a summing point at IC1 and IC2 which rectify and invert the input voltage. The output of the summing amplifier is passed through a high-pass filter and a low-pass filter, before being rectified and inverted again. The output of the inverter is then applied to a voltage-controlled oscillator (VCO)

IC and IC respectively. When the summed input is positive, the output of IC tends toward a negative level due to inverter action and hence IC is forward biased. Therefore the negative peak outputs are clipped to a

Typical data

Supply: ±10V
IC1 = 741
R1 = 1MΩ, R2 = 10kΩ
R3 = 4.7kΩ
R4 = R5 = 3.3kΩ
D1 = 1N914
Vmod: 1V pk-pk at 1500Hz
Vcarrier: 2V pk-pk at 10kHz

level approaching zero because D1 is in the feedback loop. The output is characterized by V0, that at V0 being similar, but of course the carrier is inverted. Non-linearity of the rectifier impedences introduces some distortion which is evident in the troughs of the modulated output and very slightly distorted at the higher levels of modulated carrier, though not the peaks of the envelope. Output filtering is unnecessary and hence drift of carrier-frequency offers no great problem.

Component changes

Maximum carrier amplitude to obtained 100% modulation 8V pk-pk (V0 ≈ 8V pk-pk). Maximum carrier frequency 23kHz before peaks distort.

Modulated crystal oscillator

Components

Crystal: 1MHz
R1, R2: 1kΩ
R3: 600Ω
R4: 100kΩ
C: 27pF

Vcc: 6V
IC: CA3000
C.c.o. probe used had impedance of 10MΩ in parallel with 10pF.

Performance

Graph shown of V0 (not V0) was obtained with d.c. values of V0 and indicates a modulation sensitivity of 1.07V/V and a modulation depth of approximately 25% over the range shown. Range was limited by the fact that increasing V0 beyond +700mV caused limiting on the negative peaks of V0. Lower limit was very much lower than that shown but there is no point in going beyond a symmetrical condition.

With the c.c.o. probe on V0 the modulation depth fell to 11% (due to the loading of the probe) and this was maintained from d.c. to approximately 2kHz without appreciable distortion. Higher frequencies caused phase distortion. With R1 set at 500Ω no carrier oscillations were obtained. With higher R1, however, little effect was observed, e.g. R1 = 10kΩ produced a modulation depth of 10.5% although with approximately 12% increase in carrier amplitude.

Variation of R2 in the range 1.5Ω to 1500Ω produced very little effect; thereafter limiting
Use 741CS for faster slew-rate and slightly greater carrier frequency capability. R₁ is fairly critical. Maximum variation of ±200 Ω. Other resistors variable over wide range provided ratios maintained. R₁₁, R₁₂ etc i.e. accurately matched resistors are suggested. Use centre-tapped transformer to provide carrier and its inverted form, as shown above.

Useful range of this modulator is in the audio band, provided that the non-linearity is not significant. Crossover distortion will be minimized for high carrier frequencies, and large peak-to-peak carrier excursions.

Circuit modifications
High-frequency performance is limited by slew rate and gain of the op-amp in turn off say diode D₁, and turning on diode D₂. This switching speed is increased by the circuit shown middle. Additional gain is added during the switching transition of the order of 250 up to 30kHz obtained with the addition of TR₁ to TR₄ circuitry. At the switching instant, D₁ and D₂ are off, thus opening the feedback loop, and do not shunt this additional network. When conduction commences, one diode heavily conducts, shunts the high output impedance of this additional stage giving again an overall gain of near unity. Low-value resistors provide small time constants for stray capacitance.

Frequency response will be above that of op-amp when additional stage driven from supply currents of the i.c. This reduces peak-to-peak swing requirement of amplifier and should be within slew-rate limit at higher frequencies. Typical data Small-signal bandwidth 30kHz to 300kHz IC, BB350B.
R 100Ω. Chosen to limit rated output current for a 1V swing at output. Other components as before.

Further reading
Graeme, J. Boost precision rectifier BW above that of op-amp used. EDN, July 5, 1974.

Description
The CA3000 is a d.c. amplifier in a 10-pin TO-5 package. The schematic is shown over. Emitter follower inputs TR₁ and TR₂ provide high input impedance (0.2MΩ), the remainder of the circuit being conventional long-tailed pair (TR₃ and TR₄) differential amplifier design with constant current tail (TR₅). With external connections as shown in the main diagram the circuit becomes a crystal oscillator with feedback to pin 1. These oscillations are modulated by Vm which controls the tail current. Output at pin 10 contains the (carrier) oscillations plus harmonics modulated by Vm plus V₂ itself, plus d.c. The high-pass filter consisting of C and R₄ eliminates the d.c. and Vm, leaving the amplitude modulated signal.

Since the oscillator is a crystal oscillator the frequency of oscillation is extremely well defined so variations in other components, supply voltages etc. will produce very little frequency modulation.

Modifications
Due to the symmetry of the CA3000 one can reverse the roles of pins 10, 8 and pins 1, 6; no advantage or disadvantage accrues.
All the unwanted terms in V₂ (including carrier harmonics) can be removed by use of a suitable bandpass filter. Because the output impedance of the amplifier is high (8kΩ) a tuned L-C filter may be used as shown centre: in our case with a carrier of 1MHz and modulating signal of 2kHz a Q of 250 is permissible but would reduce the modulation depth by 0.707 at 2kHz. Since the modulation depth is inherently low, a lower Q would appear advisable and if possible one would be better with a more rectangular bandpass filter.
If one simply wants to remove the modulating signal from V₂, the arrangement shown right can, with suitable adjustment of R₃, simply cancel the offending term. We achieved this with a value of R of approximately 15kΩ. This has the additional effect of reducing the carrier at V₁ by approximately 30% but enabled one to increase the modulation depth to approximately 43%, Vm being 6.8V pk-pk. C and R₃ were retained for direct comparison but obviously do not help to give the max. obtainable. Modulation depth of approximately 47% at Vm was achieved by increasing the positive supply to 12V. Alteration of the negative supply had little effect. No change in carrier amplitude was observed with this increased supply. One cannot guarantee this performance since the device is being driven outside the manufacturer's recommendations. Presumably if the alterations of modification no. 1 were used it would be the negative supply which would require alteration.

References
RCA applications notes ICAN-0030.
Card 8, this set.
Low-cost 2-stage circuit forms versatile a.m. oscillator. 100 Ideas for Design, Hayden, 1966
Diode bridge modulators

Typical performance

\( V_{110} \) carrier: 10V pk-pk
\( V_{110} \) modulation: 6V pk-pk

Typical performance

\( V_{110} \) carrier: 1.2V pk-pk
\( V_{110} \) modulation: 2V pk-pk

Component changes

\( D_1 \rightarrow A \) Any general purpose, discrete or monolithic silicon, germanium or Schottky types. A square-wave carrier source may be used in either circuit together with an output filter. A floating source for carrier in Cowan modulator (left) can be simulated from grounded-type using a transformer.

Circuit descriptions and modifications

Both modulators are widely used at low carrier frequencies. In the Cowan arrangement diode switching in the bridge is under the control of the carrier alone provided that its amplitude is much greater than that of the modulating signal. Assuming this condition exists, then during the half-cycles of the carrier when point \( C \) is positive with respect to point \( A \), the diodes will be reverse-biased and they present a high impedance shunted across the path between the modulation source and the output. When the carrier goes through its other alternate half-cycles, point \( A \) is positive with respect to point \( C \), the diodes become forward-biased and the bridge provides a low-impedance shunt path across the modulation source. The higher frequency carrier voltage therefore causes the diode bridge to act as a single-pole single-throw switch which passes the modulating signal to the output during one half-cycle of the carrier and attenuates the modulation during the other half-cycle. As the magnitude of the modulating signal increases the carrier controlled switching of the diodes becomes less perfect (see waveform over) and a ripple appears on the output waveform at the modulation frequency. This

Single sideband generation

Filter method

A single-sideband signal can be produced by feeding the carrier \( V_{110} \), and modulating signal \( V_{110} \) to a balanced modulator to produce a double-sideband suppressed-carrier output which is then passed through a bandpass filter to select either the upper or lower sideband as required. The degree of carrier suppression depends on the design of the balanced modulator and the rate of cut—of the bandpass filter, which must have a bandwidth equal to that of the baseband modulating signal. A number of different filter realizations may be used, their suitability depending on the carrier frequency at which the filtration is performed. The rise of L-C ladder filters is normally restricted to carriers in the approximate range of 20kHz to about 100kHz due to the relatively low Q-factor values obtainable with low-cost inductors. The much higher Qs obtainable with quartz crystals allow the design of bandpass filters using a lattice structure at frequencies above about 500kHz. Ladder-type mechanical filters provide much higher Qs than L-C resonant circuits, which give them excellent selectivity characteristics in a useful carrier range of about 50kHz to 1MHz. Ceramic elements using the piezo-electric effect, but having lower Q values than quartz crystals, can be used in a ladder structure over a carrier range of about 250kHz to 1MHz. Whatever the nature of the bandpass filter the same filter could be used to select either the upper or lower sideband by shifting the carrier frequency to the appropriate edge of the filter response, assuming the filter to have a similar rate of cut at both of edges. The balanced modulator could be replaced by an amplitude modulator in certain applications, the degree of carrier suppression depending on the filter attenuation characteristic. The unwanted sideband can be removed without the use of bandpass filters by means of phase shift techniques. The basic form of a phasing method s.s.b. generator is shown below. The carrier frequency is applied to balanced modulators A and B with a 90° phase shift introduced in one path. The modulating signal is also applied to both balanced modulators, to A directly and to B via a wideband 90° phase-shifting network. The output signals from the modulators, when combined, result in the suppression of one sideband. If the other sideband is required instead this can be achieved by reversing the phase of the carrier applied to one modulator, or by reversing the phase of the modulating signal to one modulator, or by reversing the output of one of
ripple is due to the larger-amplitude modulating signal causing some small amount of conduction on the diodes during their off state. When \( V_{in} \) polarity makes point B positive with respect to point D, a diode leakage path exists through \( D_2 \) the carrier source and \( D_1 \), and through \( D_3 \), the carrier source and \( D_4 \). When B becomes negative with respect to D. This modulator produces an output waveform containing the original modulating-frequency components and sets of upper and lower sidebands centred on the original carrier frequency and its harmonics, all of which are ideally suppressed. To remove all components except the sidebands around the original carrier frequency a band-pass filter must be incorporated at the outputs. A simple method of achieving this filtration, at the same time isolating the output from the bridge and simulating the floating-source-carrier by means of a transformer, is shown top. In this arrangement \( R_5 \) should be about 10\( R_1 \); (1 + \( h_\beta \)) \( R_4 \) should be much greater than \( R_2 \) and \( R_3 \) chosen to damp the output tuned circuit sufficiently to pass the desired sidebands.

The double-balanced bridge-ring modulator obtained its name from its ability to suppress both the original modulating signal and the carrier from its output. Hence it is to be preferred to the Cowan modulator when the carrier frequency does not greatly exceed the highest modulating frequency. In the circuit shown over, when point A is positive with respect to point B, \( D_1 \) and \( D_2 \) are forward-biased and \( D_3 \) and \( D_4 \) reverse-biased. When B becomes positive with respect to A, \( D_1 \) and \( D_2 \) are forward-biased with \( D_3 \) and \( D_4 \) reverse-biased. Hence the modulating signal will pass from \( T_1 \) to \( T_2 \) over two different paths during alternate half cycles of the carrier causing a 180° phase shift of the output after each carrier half-cycle. When wideband transformers are used the output waveform consists of sets of upper and lower sidebands centred on the original carrier frequency and its harmonics, all of which are, ideally, suppressed. The output waveform shown over differs from the above due to the use of a.f. transformers with a 10-kHz carrier so that very little of the sidebands of harmonic carrier frequencies are present at the output due to transformer imperfections.

Many other forms of bridge-ring modulators exist, the basic form of one type using two diode bridges to simulate the effect of a reversing switch being, as shown left, bottom.

The number of different networks that could be used to realize the \( \alpha \) and \( \beta \)-networks is almost limitless, but to meet the required conditions over a range of frequencies indicates the need to combine an all-pass characteristic with a non-uniform time delay as a function of frequency over the required frequency range, which results in a type of ladder structure.

An example of such a realization is shown above. This configuration is capable of maintaining the phase difference at the outputs to within about \( \pm 1^\circ \) of the desired 90° phase difference over a frequency range of about 10:1. For the speech bandwidth of approximately 300Hz to 3kHz typical values are given below.

Supply +15V, \( T_1 \), \( T_2 \),

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Further reading


FET modulators

Circuit description
This circuit uses an n-channel junction FET, in its voltage-controlled resistance mode, and hence the gain of the inverter-amplifier will be dependent on the slope resistance of TR1. The drain-source conductance gds of TR1 is fairly well defined by:
\[ g_{ds} = \frac{2I_{DSS}V_{DS}^2}{V_{DS}} \]
provided \( |V_{DS}| < 100 \text{mV} \).

The output from IC1 is Vo and is \( -R_1g_{ds}V_{carrier} \) hence
\[ V_{out} = -R_1 \frac{2I_{DSS}V_{DS}^2}{V_{DS}} \text{(V carriers)} \]
i.e. proportional to the product of the carrier and modulation signals. Note that point x is a virtual earth point and \( |V_{carrier}| = |V_{DS}| \). This restricts the carrier to a maximum of 100mV pk-pk to limit distortion. Positive values of Vmod much greater than \( |V_{carrier}| + 0.7 \text{V} \) will forward-bias the gate-source junction, hence this determines the maximum allowable modulating signal.

Component changes
R1 10 to 20kΩ to provide increased output.

Carrier peaks can be equalized by biasing carrier with Vc, say. For \( V_c = 29 \text{mV} \), other parameters as before, output envelope is shown below.

Circuit modification
- Operational amplifier may be replaced by a single transistor in circuit over (see ref. 1). Output will contain a signal proportional to the carrier and modulating signal product which can be applied to a bandpass filter centred at fc. C is large enough to be an ac. short-circuit for the carrier frequency. Is is chosen to make \( h_{ib} \) of the transistor small, given by \( h_{ib} = 26/\text{IcmA} \).
  This ensures that \( V_{carrier} \approx V_{DS} \).

Typical data
IC1: 741, TR1: 2N5457
Supply: ±15V
R1: 10kΩ
fmod = 1V pk-pk, fmod ≈ 1kHz
Vcarrier 100mV pk-pk
fcarrier ≈ 10kHz
Vout at Vo as shown top.
D.C. transfer function between input carrier and Vout for varying VDS of f.e.t., provides information on linear regions.

Long-tailed pair modulators

Circuit description
Circuit shown above is an example of an amplitude modulator having one input channel which is linear and the other channel highly non-linear. Although the multiplication from such a circuit is far from ideal, amplitude modulation can be obtained by applying the carrier to the non-linear input channel, applying the modulating signal to the linear input channel and taking the output across a bandpass filter centred on the carrier frequency. In this circuit the collector current of TR2 is a linear function of the common tail current but a highly non-linear function of the voltage between the bases of TR1 and TR2 due to the voltage drive from the carrier source to TR2 base. Transistors TR1 and TR2 form a current mirror that acts as a current source for the differential pair TR1 and TR2. Quiescent tail current is determined by R1 with the single-ended (grounded) modulation source VR1 set to zero. This quiescent current is then varied by the modulating signal. The collector current of TR2 thus contains the modulating signal as well as the carrier and its sidebands, together with carrier harmonics and their sidebands due to the non-linear relationship between the collector current and the carrier drive voltage between TR1 and TR2 bases.

To obtain an output amplitude-modulated wave the bandpass filter, in this case the parallel tuned circuit L1C1R1, must have a sufficiently high loaded Q-factor to remove the modulation-frequency components and the harmonic carrier and sideband components. For the circuit shown the theoretical value of the centre-frequency for the tuned circuit is \( f_0 = -1/2\pi \sqrt{L_1C_1} \text{Hz} = 1.592 \text{MHz} \) which is within 1% of the value in practice. The loaded Q-factor is \( Q_L = 2\pi R_1C_1 = 47 \) which provides a passband (to 3dB down points) having a width of \( f_0/Q_L = 33.8 \text{kHz} \) which is suitable for audio.

Typical performance
Supply: ±12V, ±2.7mA
TR1 to TR2: 1/3 of CA3086
(pins 13 substrate connected to −Vcc)
R1, R2: 4.7kΩ

\[ \text{L1: } 10 \mu\text{H} \]
\[ \text{C1: } 1 \mu\text{F} \]

Vcarrier 100mV pk-pk
Vmodulation 25V pk-pk
Supply for 1kHz sine wave at \( f_m = 1.61 \text{MHz} \) to produce unmodulated carrier output from tuned circuit of 3.6V pk-pk.

Vout = modulation 25V pk-pk (max) sine wave at \( f_m = 1 \text{kHz} \) to produce approximately 100% modulation depth output from tuned circuit.

Vout: see waveform left.
modulation, up to 15kHz. By suitable choice of L1 and C1 carrier frequencies up to about 100MHz may be used, with adjustment of Q1, by means of R4 to provide a suitable bandwidth for the highest modulating frequency.

Whereas the above circuit is formed by interconnecting the monolithic individual transistors to produce the long-tailed pair, other integrated circuits are manufactured in the long-tailed pair configuration. Examples of these are the CA3004, CA3005 and CA3006 the last type being particularly suited to use as a balanced modulator due to the small input offset voltage (typically 1mV). The internal structure of this integrated circuit is shown left. The i.e. consists of a well-balanced differential-input amplifier Tr1 and Tr2, fed from a constant-current source Tr3. Due to the versatile biasing arrangements a number of different operating modes may be used but pin 8 must be connected to the most negative direct voltage in the circuit and pin 9 to the most positive direct voltage used. Pin 12 is normally connected to ground. A typical balanced modulator circuit using this integrated circuit is shown above. In this application, the diodes R3 and R4 of the integrated biasing network are short-circuited, the modulating signal is applied between the differential pair bases V1 and the carrier applied to the base of the constant-current transistor Tr3 via transformer T1. The differential-output double-sideband suppressed-carrier signal between Tr3 and Tr5 collectors is converted to a single-ended output by the tuned transformer T2 which suppresses the unwanted output components. Attention should be paid to careful printed circuit layout and screening to obtain the best performance. Typically the carrier suppression is around 25dB below the wanted double-sideband output.

Also, since \( i_f = g_{ds} V_{mod} \) and \( i_v = \alpha (I_c + i_f) \) then \( V_v = V_{cc} - \alpha I_c R_2 - g_{ds} R_L V_{carrier} \). This provides an a.c. product of \( 2 x R_L I_DSS/V_{P}^2 \times V_{carrier} \) (\( V_{mod} \)). Similar limitations to levels apply in this circuit (a common base current gain).

- Figure (bottom) comprises a combination of a dual gate m.o.s.f.e.t. and inverting amplifier.
  - Tr1, 4084, IC1, SN72709, supply ±12V.
  - For double-sideband suppressed-carrier operation, the carrier is fed forward through R4. If \( V_{mod} \), then \( V_{DS} \) is given by \( -I_2 R_1 V_c \) i.e. \( V_{DS} = -I_2 R_1 V_c \)
  - Provided \( R_4/R_3/V_c \), then the above condition is obtained, i.e. \( V_{out} \) is proportional to the product of the two signals.
  - To obtain amplitude modulation the circuit is opened at X. Modulation depth must be limited to around 60%. At these levels of carrier and modulating signals where \( V_m \) is no longer much greater than \( V_c \) the \( g_m \) of the f.e.t. is a function of both signals causing unwanted harmonics. Modulation depth may be increased if output filters are employed. Note that other analogue multipliers may be used as amplitude modulators, but an important limitation will be their frequency responses.

Further reading

Cross reference
Set 22, card 1.

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When \( V_{in} \) is adjusted to produce 16mV r.m.s. at pin 1 and \( V_{in} \) adjusted to produce 31.5mV r.m.s. across the primary winding of \( T_1 \) at a frequency of 1.75MHz. Typical values:
- Supplies \( V_{cc} +6V, V_{ee} -6V, R_1, R_2, R_3 \) part of i.e.
- \( R_4, R_5, R_6, R_7, 50 \Omega \) to 870pF; \( C_1, 10nfF; C_2, 90 \mu fF \) to 400pF; \( T_1, 9:1 \) step-up
- \( T_2, \) bifilar wound 9:1 step-down with primary tapped 3:1

This degree of carrier suppression may make the circuit suitable for double-sideband systems requiring the transmission of a pilot carrier. For applications requiring a higher degree of suppression an improvement may be obtained by increasing the modulation signal input and decreasing the carrier input voltage.

Further reading

Set 22: Amplitude modulators

Micropower amplitude modulator

Components
- \( R_1: 33\,\text{k}\Omega, R_2: 5\,\text{k}\Omega \)
- \( R_3: 1\,\text{M}\Omega, R_4: 5.6\,\text{k}\Omega \)
- \( R_s: \text{see graph} \)
- \( R_L: 10\,\text{k}\Omega \) load resistor
- \( C_1: 47\,\mu\text{F}, C_2: 1.5\,\mu\text{F} \)
- \( C_3: 250\,\mu\text{F}, L: 400\,\mu\text{H} \) (total)
- \( C_3 \) and \( L \) tuned for 460kHz
- Transistors from CA3086 i.e.

and lower values gave a rapidly diminishing value of \( m \).
Maximum carrier amplitude was 1.32V pk-pk with \( R_3 = 15\,\text{k}\Omega \). The modulating frequency was 400Hz and linear modulation was maintained over the frequency range 10Hz to 1kHz typical. Maintaining \( R_4 \) at 6.8k\Omega, the frequency of \( v_{th} \) at 400Hz, and altering the magnitude of \( v_{th} \) at all points to produce maximum \( m \) produced the graph of \( m \) versus \( V_{th} \), above right. The lower limit of 0.8V was chosen as being that of the end-of-life voltage of a dry cell. The corresponding range of \( v_{th} \) was 0.48 to 1.25V pk-pk. Power consumption is less than 500\mu\text{W} throughout the voltage range; considerably so at the lower end.

Circuit description
This circuit is due to Venkatesanwali & Sonde (see ref.) who claim slightly

Direct tuned-circuit modulator

Circuit description
This circuit demonstrates the principle that may be used to perform the initial modulation of a carrier signal, which may then be used to drive a power amplifier. Transistor \( T_3 \) is driven hard into conduction once every carrier-cycle so that its base-collector junction is forward biased. The related collector current pulses excite the tank circuit \( LC \), which is tuned to the carrier frequency which therefore rings between pulses at a frequency \( f_c \). The waveform at the transistor collector or across the tuned circuit is shown opposite at (b). The envelope is approximately the superposition of \( v_{cc} + v_{mod} \) and is of the form

\[
V = \frac{V_{cc} + V_{th}}{1 + m \cos \omega t}
\]

where

\( m = \frac{v_{mod}}{V_{cc} + V_{th}} \)

To maintain approximately 100% modulation for variation of \( V_{cc} \), the modulating signal is linearly related as shown in graph.

Circuit notes
- Tuned circuit \( Q \) in the range 30 to 50.
- Filter circuit (high pass) of \( C_4 R \), provides useful demonstration technique only. Normally output coupled out via tapped-down transformer
- \( R_2 \) is necessary at the higher frequency to maintain symmetry of waveform.

Applications
In certain situations, a.m. is performed at low power levels, and power levels suitable for transmission are developed by power amplifiers. An example of such a circuit is shown over, top. To preserve a wideband performance a push-pull configuration of \( T_1, T_2 \) minimizes unwanted harmonic content. Typical performance data:
- \( V_{cc}: 12.5V \)
- Peak envelope power: 40W
- Modulation: 95%
- Carrier frequency: 118 to 136MHz
- Carrier input power: 5mW

A similar concept but at a low power level is described in the circuit shown over, bottom. Typical output 100mW depending on transistor at a
better results than we achieved. Consider first the circuit shown above. This is a gain-stabilized block for which can be shown that

$$I_c/I_B \approx \exp(\lambda V_B)$$

(Ref. 1) over a wide range of operating conditions ($\lambda$ having the usual connotation). To understand the circuit in a simplified manner assume that both base currents are negligible. Both transistors are governed by the same exponential relationship such that for a given $\Delta V_B$ (which must be the same for both transistors) the collector currents change by the same percentage. Hence, if $V_B$ sets different initial values of collector currents, which it will, a signal $V$ at A will result in the same ratio of a.c. to d.c. in each transistor. As the direct current ratio is fixed by $V_B$, (a.e.g. 10:1), the ratio of a.c. is also fixed and since the collector current of the diode connected transistor is approximately equal to the input current $I_1$, then the current gain $I_2/I_1$ both small signal and large signal is likewise fixed or stabilized. Clearly changes in $V_B$ cause changes in $I_2$ if $I_1$ is fed from a current source, i.e. $I_1$ can be modulated. It can be shown (see ref.) that

$$m = \frac{\Delta I_c}{\Delta I_B} = \exp(\lambda \Delta V_B) - 1.$$  

The above block can be seen in the main diagram in the form of $I_{TR}$ and $I_{TR}$. $V_B$ is produced across $R_2$ and $C_1$ simply acting as a short to carrier frequency signals. The section of the main diagram enclosed by the broken line is, after a fashion, a mirror image of the gain-stabilized block and produces

$$D V_B = (1/2) \ln(1 + V_B/R_4 I_B).$$

Substituting this in to the expression for $m$ produces

$$m = V_B/R_4 I_B.$$  

$V_B/R_4$ is the modulating input current leaving $I_B$ as the only variable. $I_1$ is the quiescent current in $R_2$ and is dependent on the biasing arrangements in the dotted section. $m$ was found to be insensitive to variations in $R_2$ and $R_4$ and the graph of $m$ versus $R_4$ shows $m$ to be somewhat insensitive to $R_4$ also. This is not surprising as $T_{RB}$, $T_{RC}$ is a stabilized block in the same way that $T_{TR}$ is. Note from the expressions quoted that $T_{TR}$, $T_{RC}$ etc comprises a linear-log converter and $T_{TR}$ and $T_{RC}$ effectively take the anti-log. $T_{TR}$ is a cascaded transistor to improve the voltage gain characteristics and may be omitted at the expense of reduced $m$.

The tapped transformer is included to minimize the loading effect of $R_L$, again improving voltage gain characteristics. A straightforward L-C circuit could be used at the expense of reduced $m$.

Circuit modifications

Possible modifications in respect of $T_{TR}$ and the transformer have already been mentioned. In addition it appears possible to remove $R_2$, $R_4$ and $C_1$ altogether and simply connect the $T_{TR}$ and $T_{RC}$ by increasing $R_4$. Any linear to log converter may be used e.g. the circuit above right may be used although the micro power aspect is lost and a bias signal would be required with $V_B$.

Reference


Further reading

2. RCA application note AN-3749, 1968.
3. 100 ideas for design, no. 4, Hayden 1964.
5. 100 ideas for design, no. 3, Hayden 1964.

Cross reference

Set 7, card 6.