Wireless World Circard  

Basic diode rectifiers

**Circuit description**
The basic forms of half-wave diode rectifier are the mean and peak circuits shown above and suffer from the flaw that a minimum potential difference must be developed across the diode itself (0.6V for silicon, 0.4V for Schottky barrier diodes). The only limit to the h.f. response is that of the diode itself, and possibly the source impedance, the graphs above being typical. The transfer function of $V_{out}/V_{in}$ for the resistive load is shown over the frequency range, being broadly linear, but with no output until $V_{in}$ exceeds 0.6V. If the output is to be read on a moving-coil meter in the upper circuit then the inertia of the coil ensures that the reading is that of the average value of a half-wave rectified signal. At low frequencies the meter needle will vibrate, preventing accurate readings. Typically, readings are adequate to lower audio frequencies. For the lower circuit the continuous d.c. output should be fairly close to the positive peak value of the input, provided the capacitor does not discharge significantly between positive peaks. Hence the time constant comprising $C$ and the effective load resistance (e.g. meter) must be long compared with the period of the input waveform. e.g. a 100-μA meter movement would allow a 1-μF capacitor to decay by approximately 1V in 10ms, corresponding to a 100-Hz signal frequency.

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Peak/mean/r.m.s. calibrated rectifier

**Circuit description**
The second i.e. is used as a buffer to transfer the rectified output to the load with unity gain and without the load or feedback network presenting any adverse effect to the rectifier. When $D_2$ conducts, the feedback path is closed and the high gain of $IC_1$ results in a virtual earth at its inverting input. The output voltage during this period is thus an accurate (inverted) multiple of the input. For switch position (a), the amplifier gain is -1 when the diode is conducting, given that $R_2 = R_1$. Hence the capacitor charges to a positive voltage almost equal to the negative peak input. For all other inputs the output of $IC_1$ reverse biases the diode and the capacitor stores the peak voltage, which value is transferred to the output by $IC_2$. The time constant chosen is a compromise between the need for accurate storage of long-period inputs and the need for the circuit to be able to respond to a lower input amplitude in a reasonable period of time. During the period when $D_2$ is not conducting, $D_1$ is used to clamp the output of $IC_1$ by feedback action; this minimizes the recovery time of the circuit prior to the next period when $C_1$ is to be charged. Mean reading is achieved by removing $C_1$ and doubling the value of feedback resistance. If the output is fed to a moving-coil meter the reading is twice the mean rectified half-wave value i.e. equal to the mean rectified full-wave input, assuming a symmetrical waveform. Switch position (c) increases the gain of the amplifier in the ratio r.m.s.: mean rectified value for a sine wave. The meter, though deflecting in proportion to the mean rectified value, is now calibrated in terms of the r.m.s. value of the input.

**Typical performance**

- Circuit left:
  - $R$: 1kΩ; diode: PS01
  - Input signal level: 3V r.m.s.
  - Source impedance: 50Ω
  - Useful frequency range: up to 18MHz; onset of distortion occurs around 2MHz
- Circuit right:
  - $C$: 56nF; diode: PS01
  - Useful frequency range: up to 25MHz

**Component changes**

- Use Schottky diode (HP 2800) to reduce forward voltage drop.
- Buffer peak detector with a voltage-follower to avoid loading the capacitance. This will also mask the effect of moving-coil meter inductance if this becomes a predominant feature (centre, over).
- If frequency performance not important use germanium diode for lower forward voltage drop.

**Components**

- $IC_1$: LM301A
- $IC_2$: LM302
- Supplies: ±15V
- $R_1$, $R_2$, $R_3$: 100kΩ
- $R_4$: 22kΩ
- $R_5$: 47kΩ
- $R_6$: 6.8kΩ; $R_7$: 100MΩ
- $R_8$: 2.2kΩ; $C_1$: 68nF
- $D_1$, $D_2$: 1N914

*needs 30pF compensating capacitor
Circuit modifications

Simplest means to eliminate forward voltage drop is to mechanically offset a moving-coil meter, but this does not eliminate non-linearity.

- Linearity at the low level improved slightly with superimposed d.c. offset from a power supply or diode connected as shown right. Further improvement by placing D2 by the collector-base junction of a germanium transistor, but this still does not approach the performance of a diode in the feedback loop of an op-amp.
- For resistive load, connect diode in shunt with load—this is a more suitable arrangement for rectifying a current source.

Further reading

Stewart, H. E. Engineering Electronics, Allyn and Bacon, 1969, pp.130-40 and 738-44.

Cross reference

Series 4 card 2

Component changes

Varying $R_1$ from 1kΩ to 1MΩ gives proportional change in input resistance and input voltage required for given output.
- Increase $C_1$, $R_1$ to allow peak detection for lower frequency inputs e.g. for $C_1 > 1\mu F$ peak rectification possible for signals of frequency 1Hz.
- For true mean-value half-wave rectification let $R_3 = 0$. To retain r.m.s. equivalent increase $R_4$ to 120kΩ.
- Replace IC1 by any general-purpose op-amp (741 or 748 with 30-pF compensation capacitor). Replace IC2 by 310 (improved voltage follower) removing restriction on supply voltage minimum imposed by 302, and further increasing input resistance of stage. For reduced cost, substitute source emitter follower, checking that reverse breakdown on stage input cannot be exceeded. Direct current offset drift in follower have no effect on performance provided that any changes are slow i.e. not within one cycle.

Circuit modifications

- Input signal may be applied to the non-inverting input of IC1. This greatly increases the input impedance at the expense of introducing common-mode input voltages, usually with some worsening of high frequency performance. Addition of capacitors $C_2$, $C_3$ in conjunction with $R_1$ may be necessary with some combinations of amplifiers to avoid risk of high-frequency oscillation. For $R_1 = 100k\Omega$, $C_2$, $C_3$ may be around 100pF.
- Using IC2 as an integrator, the additional inversion provided within the feedback loop must be countered by taking the feedback to the non-inverting input of IC1. Diode D2 still provides clamping to avoid saturation of IC1 and $R_1$ limits charge rate to $C_1$.

Further reading


Cross references

Series 4, Cards 3, 9 & 10.
Absolute-value circuits

Circuit description
This form of precision rectifier uses two parallel paths feeding currents to summing amplifier A2. For negative input voltages, the output of the operational amplifier A1 swings positive causing D1 to conduct and D2 to be reverse biased. Thus, for this polarity of input voltage, there is no contribution of current to A2 through its R2 inverting input path. The only input current to A2 is therefore \(-V_{in}/R\) causing \(V_{out}\) to be an inverted (positive) version of \(V_{in}\). For positive input voltages, the signal fed to A1 causes its output to swing negative which through D2 biases D1 and brings D2 into conduction. Amplifier A1 thus acts as a unity-gain inverter causing the voltage at the junction of D2 and R2 to be \(-V_{in}\). Amplifier A2 therefore senses the sum of two input currents having values of \(V_{in}/R\) and \(-2V_{in}/R\). The resultant current at the input to A2, and in its feedback resistor, is \(-V_{in}/R\) which therefore makes \(V_{out}\) equal to \(V_{in}\). Hence for any input signal \(V_{out}\) will be equal to its magnitude or absolute value. Tolerance of the resistors in A1 are critical if accurate reversal of the gain of the system is to be achieved because for positive input signals the current fed to A2 represents the difference between those in the two parallel paths. Slew-rate limiting of A1 for positive-going inputs results in a different amplitude-frequency response to that obtained with negative-going input signals where only the resistive parallel path is relevant. This imposes a separate limit from the slew-rate limitation of A2 causing the outputs to have different magnitudes for positive and negative inputs.

Component changes
Replacing PS101 diodes with Schottky barrier diodes (e.g. 042–82HP–8211) typically produces amplitude response shown in curve 2. Low-frequency error in \(V_{out}\) (mean) is 3.3%. Using Schottky diodes with 741s replaced by 301s with feed-forward compensation as shown over (left) typically produces response shown in curve 3, whose low-frequency error in \(V_{out}\) (mean) is +2.2%.

High-frequency voltmeter for a.c.

Circuit description
The transfer function at this circuit is \(G = A_v(1-\beta_2A_2)\) where the transadmittance \(A_v\) is ideally defined by the desired full-scale meter current for a given value of \(V_{in}\) and where the feedback factor \(\beta_2\) is defined by \(R_2\). The input signal is inverted by \(T_1\) and again by \(T_2\) before being applied to the bridge rectifier through \(C_2\) which removes the d.c. error that would arise from the collector voltage of \(T_2\). Meter current flows in \(R_3\) which with perfect follower action would cause the p.d. across it to equal \(V_{in}\). However \(R_2\) also carries the emitter current of \(T_2\) which is not a perfect follower. Therefore the choice of \(R_2\) to make the meter read \(V_{in}\) (r.m.s.) directly for a given full-scale meter current, will be less than the value predicted by using \(R_2 = V_{in}/1.1 I_{in}\). Overall d.c. shunt-derived shunt-applied negative feedback is provided by \(R_3\) and \(R_4\) is decoupled by \(C_3\). Capacitors \(C_2\) and \(C_3\) cause the amplifier to exhibit a lower cut-off in its response.

Component changes
Meters requiring different full-scale deflection currents can be accommodated by a suitable choice of \(R_3\) for a given \(V_{in}\). For \(R_2\) greater than about 100Ω and a full-scale deflection sensitivity of around 100mV for a 1mA movement, the transfer function is defined by \(R_2\) with a typical full-scale error of about 2mV. Careful printed circuit layout, using a single ground point, is necessary to achieve an extended amplitude-frequency response. To prevent instability, the use of ferrite beads on the supply leads and a tantalum bead decoupling capacitor are recommended. It may be necessary to connect a small capacitor between collector and base of \(T_2\) and possibly a resistor of around 1000Ω in series with the source.
Circuit modifications

- Middle circuit shows a precision rectifier that uses five resistors of the same value which makes their matching somewhat easier than with other circuits. For positive inputs $A_1$, output goes negative so that $D_1$ conducts and $D_2$ is reverse biased. Therefore the junction of $R_3$ and $R_4$ is at $-V_{in}$ and as $A_2$ acts as a unity-gain inverter (non-inverting input of $A_2$ is virtually grounded), $V_{out} = V_{in}$. For negative inputs $A_1$, output goes positive, $D_2$ conducts and $D_1$ is reverse biased. The input current in $R_1$ now divides between $R_3$ and $R_2$ plus $R_4$ in the ratio 2:1, so that $A_2$ output (and non-inverting input of $A_3$) is at $-2V_{out}/3$. Amplifier $A_3$ now acts as a follower with a gain of $1 - R_6/(R_5 + R_3) = 3/2$ for $R_5 = R_3 = R_S$, hence $V_{out} = -V_{in}$. Thus $V_{out}$ is a full-wave rectified version of $V_{in}$. The inverting input of $A_1$ is a virtual earth and may be used as a summing junction for $n$ inputs from current sources or from voltage sources via $n$ resistors.

- Circuit shown right provides an output that is the absolute value of $V_{in}$ when $R_1 = R_2 = R_3 = R_4$, and has a high input impedance since the signal source sees the high common-mode input impedances of $A_1$ and $A_3$. For positive inputs $A_1$ acts as a unity gain follower as $D_1$ conducts and $D_2$ is reverse biased. Thus $V_+ = V_{in}$ and as $R_4 = 2R_3$, $V_{out} = -2V_+ - 3V_{in} = V_{in}$. For negative inputs $D_1$ is reverse biased and $D_2$ conducts so that $A_3$ acts as a follower with a gain of 2 making $V_+ = 2V_{in}$ and again as $R_4 = 2R_3$, $V_{out} = -2V_+ - 3V_{in} = -4V_{in} + 3V_{in} = -V_{in}$. Hence $V_{out}$ is the absolute value of $V_{in}$.

Further reading


Linear Applications Handbook, National Semi-conductor application note AN-31/12, 1972.

Cross reference

Series 4, card 12.

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Circuit modifications

- Replacing the input stage by a long-tailed pair, as shown left, decreases the loading on the feedback resistor $R_f$ and allows the transconductance to approach closer to the ideal value $1/R_f$. If the input may contain a d.c. component, capacitive coupling may still be used to remove it from the amplifier input with separate resistors to return the input base to ground potential. The resistors are tapped and driven by a capacitor from $R_f$, the bootstrapping effect reducing the alternating current in the resistors allowing lower d.c. values for good bias-point stability but without lowering the input impedance.

- Shown centre is a three-stage amplifier with overall series-applied shunt-derived negative feedback that raises the input impedance, fixes the voltage gain and provides a well-defined current into the fourth transistor. This has a bridge-rectifier giving shunt-applied feedback for low input impedance ensuring that the a.c. component of the collector current of $T_3$ is diverted into the meter. The emitter of $T_3$ provides a convenient point from which to derive overall shunt-applied d.c. negative feedback, to stabilize the operating conditions. In addition the emitter of $T_3$ provides an amplified voltage output for waveform monitoring. Any loading increases the meter current for a given signal.

- If some non-linearity can be tolerated while maximizing the frequency response of a meter rectifier it is possible to remove the non-linear elements from the feedback loop and drive them far from any r.f. amplifier. If the amplifier is designed to have a high $Z_{out}$ rather than low, as shown right the non-linearity is minimized.

Further reading


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Class-B economy rectifier

Circuit description
An ideal half-wave rectifier conducts for precisely one half-cycle of the input i.e. conduction angle is 180°. Such a conduction angle defines class B operation in an amplifier and suggests a description of the rectifier as a class-B single-ended amplifier of unity voltage and current gains. Conversely the analogy suggests the use of any class-B amplifier to provide an output proportional to the positive or negative peak only of the input i.e. rectification with amplification in which neither voltage nor current gain need be restricted to unity. The example given uses the most widely available operational amplifier, and suffers from a number of disadvantages which are obviated by designing the amplifier or the output stage for this particular purpose. Any standing current in the amplifier affects the reading in two ways: the meter reading for zero input is finite (1 to 2mA for circuit shown over, left) and requires scale-changing or mechanical offset. If the current is in the output stage i.e. it is operating in class AB, then for small input signals the current remains substantially constant. In practice the peak current obtainable is limited to ~ 25mA and the current in the output stage may be ~ 1mA. This latter current ensures that the supply current changes little for signals up to 5-10% of maximum. The circuit has a number of advantages to offset these limitations: the input impedance is very high; the circuit is uncritical of supply voltages, lower values minimizing dissipation and consequent changes in meter readings; sensitivity is easily adjusted; amplitude-frequency response up to 50kHz with suitable low-cost amplifier; output of amplifier available for oscilloscope monitoring.

Wireless World Circard

Potentiometric peak-sensing circuit

Circuit description
A comparator is a high-gain amplifier specifically designed for minimum response time. It is therefore a good choice for detecting specific amplitudes of a short-duration signals or pulses. If one input of the comparator is biased to a suitable reference level, then for all input signals below that reference, the output rests in its low state. When the input amplitude exceeds the reference by a small amount, the high gain of the amplifier (typically > 1000) causes the output to change state. This change may be observed on an oscilloscope, and input pulses of short duration can therefore be detected. As the input current is low, this method of detection imposes the minimum loading on the source. By reversing polarity of the reference, opposite polarities of input signals can be observed and combinations of such comparators may be used as with the window comparator of card 11, series 2. As the input current changes at the non-inverting input, is finite, though small, the source resistance of the reference should be low enough that the reference itself does not change during the process. The output voltage change is constrained by the design of the comparator used to be within the range suitable for driving circuitry such as t.t.l. stages.

Component changes
- Useful range of R1: 10k to 100Ω.
- Same principle can be applied to any other comparator (e.g. 311) to give equal positive or negative output states (over, right).
Component changes
Useful range of R: 50 to 500Ω
Useful range of supplies: -5V to +15V
There is no advantage to increasing negative supply if meter is in positive line and vice-versa. Use minimum supply voltages possible to minimize heating effect, which changes standing current in class AB stage. Any other feedback configuration can be used such as follower with gain, see-saw amplifier. Reduction of feedback increases sensitivity and allows reduced value of compensating capacitor with op-amps such as 301, 748. Bandwidth may be increased to 500kHz with gain of 10 using compensating capacitor of 3pF for 301 type op-amp. Bandwidth is already improved over some circuits, since small output voltage swing minimizes slew-rate limitations.

Circuit modifications
- The output stage of 741-type op-amps is basically a complementary pair of emitter followers. Driving current into the output uses the transistors instead as common-base stages, i.e. with unity current gain, but developing any desired unipolar output voltage across the meter (circuit left). Effective input resistance \( \rightarrow 0 \); same limitations on minimum signal registered as before.
- Using an existing amplifier, add a separate emitter follower to the output, monitoring the current only in the collector of one transistor. A second transistor may be added to retain both polarities of output and prevent undistorted waveform to oscilloscope if required, and to maintain closed feedback loop, avoiding saturation on negative-going inputs (middle circuit).
- Alternately add clamping diode if amplifier has suitable access point, normally at base of one output transistor (right circuit). To avoid class A operation, which prevents detection of small signals in this mode of operation, while retaining linearity the novel approach to class B proposed by Blomley is indicated (see Further reading).

Further reading
National Semiconductor application note AN31-11, 1972.

Cross references
Circard series 4, cards 1, 2 & 8.

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Circuit modifications
To obtain a square-wave output, drive a divide-by-two t.t.l. bistable. Load the comparator output with 220Ω to ensure a sufficient current sink in the off condition. A moving-coil meter or light-emitting diode may be used to give a visual indication that the pulse has reached the reference level (circuit left).
- Introduce positive feedback to improve switching speed but at the expense of switching level, as shown centre. The diode ensures that the positive feedback only affects one of the switching levels. If it is arranged that the on-level is unaffected, the switch-on will occur at an accurately-controlled amplitude, but the circuit does not switch off for small transients or ripple on the pulse and only when the pulse has fallen by a defined amount.
- For the circuit shown right and with the reference voltage positive an input that is greater than the reference will cause the output voltage to be positive. When the input falls below the reference the output will be negative. Resistor \( R_2 \) has to be less than \( R_1 \) for small hysteresis, but \( R_1 \) should not be so small as to load the source.

Further reading
Application of linear microcircuits, SGS 1969, p.68.
National Semiconductor application note AN41, 1970.

Cross reference
Series 2 card 6.

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Low-frequency measurement of a.c. waveforms

![Circuit diagram](image)

**Circuit description**

The circuit is used to determine the integral of an input waveform over the duration of the first complete positive period following the receipt of a reset pulse. It does this using IC3 as a comparator and NOR gates N3, N4 as a schmitt trigger circuit to generate pulses via C1, C2 at each zero-crossing of the input. Gate G1 is opened and G2 closed, discharging C1 and leaving the initial output of IC3 at zero. The first positive-going zero-crossing acts via C2 and the RS (set-reset) flip-flop composed of NOR gates N3, N4 to open G2 and close G1. The input is then integrated by IC3 until a negative-going zero-crossing changes the state of the NAND gate RS flip-flop A1, A2. This opens G1 and no further integration takes place, while leaving G2 open so that the final integral can continue to be read. Gate G2 is used to suppress the negative-going step that may occur prior to the start of an integrating period, as when the original reset pulse is fed in during a positive period. The non-zero input current of IC3 together with leakage effects in G1, G2 cause the output voltage to drift and readings should be taken as soon as possible after the end of the positive period normally a single half-cycle of a repetitive waveform. Similar circuits can be produced using all NAND or all NOR elements but with no reduction in package count. Normal gating techniques could be used in place of G2 but in the present version it avoided the use of a further logic circuit.

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High-current peak/mean rectifier

![Circuit diagram](image)

**Circuit description**

The circuit is related to the comparator of card 4, (series 2). In place of a diode to pass or block output signals depending on their polarity a transistor is used which is driven in and out of conduction, depending on the input. This boosts the peak output current available, and the transistor can be driven with relatively low output-voltage swing at the normal op-amp output, minimizing the effect of slew-rate limit in the amplifier. When the input is positive the amplifier output goes positive, the resulting current in R3 being drawn through R1. The p.d. developed across R3 drives TR1 into conduction charging C until the potential at the amplifier inverting input increases to match that at the non-inverting input. As the input falls the p.d. between the input terminals reverses its direction and the amplifier output swings negative, the current in R1 falling to some minimum level insufficient to maintain conduction in TR1. For the remainder of the cycle C1 discharges under the combined action of R3 and the small input current drawn by the op-amp. Provided the resulting time constant is long compared with the lowest frequency of the input voltage, the peak voltage is accurately retained. Some discharge has to be allowed, so that the capacitor p.d. can decay, when the succeeding measurement is of a signal with lower peak amplitude. Similar circuits can be used for driving low-resistance loads without the shunt capacitor.

**Component changes**

Replace BFR81 by any general-purpose silicon transistor. For peak current ratings less than 200mA add suitable limiting resistor in series with collector (50 to 1000). Op-amp may be replaced by compensated 301, 748 etc. provided.
Component changes

IC1: Any operational amplifier/comparator as speed is not critical—low offset voltage an advantage.

IC2: Minimum input current for lowest drift, e.g. LM308. Alternatively use drift compensation methods.

G1 to G3: Any m.o.s. gates; possibly reed switches for minimum drift at low frequencies.

A1 to A4, N1 to N4: Any RS flip-flops, though c.m.o.s. convenient as compatible with gates and op-amps, at Vcc = 5V.

R1: 100k to 10MΩ.

R2: > 1kΩ, R3 < 1MΩ.

R4: dependent on signal being integrated. Choose for output between 0.5 and 2.5V for given waveform—higher if higher supply available.

Circuit modifications

- Simpler versions of the circuit may be made in which no provision is made for the precautions listed above to avoid integration on succeeding cycles i.e. readings should be taken between cycles or a cumulative answer taken after multiple cycles. Equally, confusion may arise if it is attempted to start during a positive cycle as only a partial integral is achieved. To determine the mean value, time may be measured by any convenient means and the possibility shown is of a second similar integrator fed with a constant voltage. Alternatively the same integrator may be used for a later cycle if the waveform is repetitive.

- Insertion of a good voltage follower to the inverting input of the integrator is an alternative if a low-drift amplifier is not available. Standard drift compensation by feeding a small direct current derived from the positive supply rail.

Further reading


Cross references

Series 4 Cards 2, 3 & 12.

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Simple precision rectifiers

Typical performance
IC: 741
Diode: PS101
Supplies: ± 15V
R3: 10kΩ; R2: 3.3kΩ
R1: 6.8kΩ
Signal level: 5V pk-pk
Amplitude response: see graphs

Linearity maintained for input signal level down to 0.5V pk-pk.
Reduction to 0.2V using compensated op-amp also improving amplitude response.

Circuit description
This circuit has the advantage that only one op-amp is required, but the load must be maintained constant to preserve full-wave rectified waveform. When an alternating signal is applied at V_in, diode D1 is alternately forward and reverse biased. When V_in is positive with respect to ground the op-amp output is negative. D1 is non-conducting and V_in is developed across R1, R2 and R3 in series. When V_in goes negative, the op-amp output is positive, D1 is forward biased, and V_out is then defined by the ratio of R2: R1. One ratio of R2: R1 to ensure that the alternative positive half-cycles are equal is deduced in the analysis shown. Note that the effect of the diode forward voltage drop is minimized as it is within the feedback loop. As the amplifier supplies the output only during one half-cycle, the amplitude response for this condition and that when only the resistors are in circuit must be different. Further, no mechanism is shown for limiting amplifier saturation for negative outputs i.e. the recovery time from this saturated condition is long, and includes the slew-rate limitation, which may be well below 1V/μs.

Positive/negative peak detector

Circuit description
The peak detector shown is based on a particular comparator though the method is similar to that described for other peak detectors. The difference lies in the output stage of this comparator which may be considered as equivalent to a switch controlled by the relative potentials of the amplifier input, but where the switch may be effectively floated with respect to the supply lines. While the polarity of the switch p.d. must be defined, it allows either end of the switch to be connected to the appropriate supply point (in the given circuit pin 7 is taken to the positive line with pin 1 as the output; if pin 7 is used as output, pin 1 is taken to the negative line). This change in connection introduces an additional inversion in the loop, equivalent to changing from common-emitter to common-collector output configuration. This necessitates interchange of the input to which the feedback is returned.

Typical performance
IC1: LM311
IC2: LM310
Supplies: ±15V
R1: 2.2kΩ
R2: 1MΩ
C: 1μF (35-V tantalum)
R3: 10kΩ
Ripple <1% down to 200Hz

Peak detection for inputs <100mV to >20V pk-pk.
For supplies of ±10V, max V_in for accurate peak detection reduced to 16V pk-pk.
Max frequency >500kHz

When the input voltage goes positive the output stage goes into conduction supplying a large current to the capacitor C, which charges until the potential returned to the inverting input matches the signal. As the input signal falls, the output stage cuts off and the capacitor C holds this peak potential until it receives current on any succeeding positive input peak greater than its stored potential. To ensure that the capacitor discharges at a controlled rate and is capable of responding to lower peak inputs within some defined time, resistor R3 is included. The voltage follower allows normal load resistances to be used, including e.g. moving-coil meters, without changing the time constant of the circuit.

Component changes
IC1: For this particular circuit only comparators having this kind of output stage can be used i.e. equivalents to the LM311 (or the higher specification LM211 and LM111).
Component changes
- Supply voltages can be reduced to ±3V with appropriately reduced signal level.
- Use of Schottky diode (HP 2800) will reduce cross-over peaks.
- R₃ may be altered over a wide range, but the relationship with R₁ and R₂ described above must be maintained.

Circuit modifications
- Reverse diode D₂ to obtain negative voltages.
- Use 301 with feedback compensation capacitors to improve response; C₁: 15pF, C₂: 150pF.
- Use clamping diode D₁ between pin 8 on 301 and ground to improve low-level performance (circuit left).
- Cross-over troughs on output waveform are minimized by pre-biasing the clamping diode D₁ (middle circuit). About 40% of +15V reduces a trough to 40mV above zero level.

IC₂: Any voltage follower including standard op-amps such as 741 connected in voltage-follower mode. The lower input resistance that results reduces the time-constant somewhat but this is often not serious.
R₁: 1.5k to 4.7kΩ.
R₂: 220k to 3.3MΩ; too high a value allows output stage leakage to charge capacitor beyond range at which positive peaks may be sensed; too low a value increases ripple at low frequencies.
C: Determines low-frequency limits in conjunction with R₂. Use of tantalum for higher values ensures that risk of r.f. oscillation on peaks is minimized. Supply voltage: ±5 to ±18V.

Circuit modifications
- Interchanging the output connections and the output connections allows a negative-peak detector of comparable performance. Note reversal of capacitor polarity. Other buffers such as f.e.t.s may be used with the penalty of d.c. offset and drift.
- If other comparators are used which have a ground referred output-voltage swing, they cannot be used directly to charge the capacitor on peaks since they will also discharge the capacitor during the remainder of the cycle. Interposing a t.i.l. inverter with open-collector output adds further gain providing larger charging current than could be provided through a diode. As shown, the input and output are with respect to the ±5V line of the system though this could equally be made the common line of the remaining system, renaming the positive supply as +5V and the most negative supply as −10V. For amplitudes of ±5V pk-pk the circuit provides low-cost peak detector up to several MHz using 710 comparator, one gate from quad-nor t.i.l. package 7401 or inverter type 7404.
- The basic similarity between peak-detectors and sample-and-hold circuits allows an electronic switch to be used to isolate the capacitor at a desired point in the cycle. Location of feedback depends on whether output stage is class A or class B.

Further reading
Positive peak-detector for fast pulses, Applications of Linear Microcircuits, SGS, vol. 1, p. 98.

Cross references
Series 4, cards 1, 2, 6 & 8.

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Wireless World Circuit

Square-law meter circuit

Circuit description
True r.m.s and power measurements by purely electronic methods (not depending on devices such as thermocouples, moving-iron meters) can be performed using logarithmic amplifiers. The method is of broad application and is intended as the subject of a separate series; however an example of a low-cost circuit is included to demonstrate the principle. Devices IC1 and TR1, IC2 and TR2 comprise amplifiers whose outputs are proportional to the logarithm of the input currents. As these currents can be made proportional to voltage sources V1 and V2, the p.d. applied between base and emitter of TR2 is of the form \( \log A - \log B \) where A and B depend on V1, V2, respectively. Collector current of TR2 is then proportional to the antilog of the p.d. between its base and emitter (see Theory). By tapping the base of TR1 onto R3 the effective output voltage from this circuit can be made any desired multiple of TR1 base-emitter p.d. provided that the base current is much less than the current in R3. The output voltage fed to the emitter of TR2 then becomes proportional to \( 2 \log V_1 \) or \( \log V_2^2 \) when R3 tap is set to its centre value. The second logarithmic stage is required for temperature compensation even where \( V_2 \) is made a constant reference voltage. All the transistors should be well matched and operate at equal junction temperatures. Circuit is designed to use n-p-n types throughout and these are available in a standard low-cost multi-transistor package. As shown, the circuit deals only with positive-going voltages for \( V_1 \) and \( V_2 \), but a modification is shown that extends the operation to bipolar form. The second amplifier may also be used to provide power-law action such that the output current becomes proportional to \( V_1^{(n-m)}V_2^m \) with the restriction \( n-m = 1 \) for temperature-compensated operation.

Wireless World Circuit

A.C. adaptor for digital voltmeter

Circuit description
This circuit is basically an inverting amplifier having its gain defined by \( R_2/R_1 \). All of the amplifier's output current flows in the bridge rectifier and then divides between \( R_3 \) and \( R_4 \). For negative input voltages the output of the operational amplifier goes positive, producing a current in \( R_4 \) from node B to A via diodes D1 and D2. For positive values of \( V_{in} \) the amplifier's output swings negative bringing diodes D2 and D3 into conduction, with D1 and D4 reverse biased, again producing a unidirectional current in \( R_3 \) from B to A. The p.d. across \( R_3 \) is thus a measure of the mean value of \( V_{in} \), its value depending on the choice of the resistors. As the r.m.s. value is 1.11 times the mean value for a sinewave input it is possible to scale a moving-coil instrument connected in place of \( R_3 \) to read r.m.s. values directly. Full-scale current will be determined by \( R_5 \) in parallel with \( R_4 \). By making \( R_2 \) about ten times \( R_4 \) the full-scale current can be set by \( R_4 \), which allows the r.m.s. scaling factor of the movement to be determined largely by \( R_5 \) for a given value of \( R_1 \). A digital voltmeter having a differential input may be connected between nodes A and B to measure \( V_{in} \) (r.m.s.) directly provided that the ripple component of the p.d. across \( R_1 \) is sufficiently smoothed. This can be achieved by the use of a sufficiently large capacitor across \( R_1 \) or by replacing \( R_1 \) with a circuit of the form shown over (left). In either case, the value of \( R_4 \) should be chosen to prevent overloading of the operational amplifier during the initial charging of the capacitor. To provide a reasonably small degree of loading on the source, \( R_1 \) and hence \( R_2 \) and \( R_3 \) must be made much larger than the source resistance. The amplitude response of the circuit can be improved by making \( A_1 \) an operational amplifier that allows the use of feed-forward compensation, as shown in card 3.
Component changes

IC1, IC2: General-purpose op-amps tend to oscillate due to additional gain of transistors in feedback path. Heavier compensation of amplifiers such as 301, 748: shunt capacitance from output to inverting input if speed not important. R3, R4: may be omitted if other means used to avoid oscillation (they reduce loop gain in conjunction with R3, R4). R5: May be omitted subject to above precautions or may be tapped as with IC.

R1, R6: 1k to 600Ω, setting sensitivity of circuit. At both high (C> 1mA) and low (<1μA) current transistors depart from log law; op-amp input current limits low-level operation for particular circuit given.

Circuit modifications

• If IC2 drives the transistor, but with the base of the transistor taken to a tap on R4, the output of the amplifier is some multiple of the transistor Vbe i.e. proportional to a multiple of log V2. This results in TR2 receiving a base-emitter p.d. depending on different power laws of V1 and V2: IC2 \propto V1^n V2^m. For the single junction of TR2 base-emitter to maintain temperature compensation the choice of n, m is restricted by n = m + 1.

Component changes

Replacing the CA3019 diode bridge with 4 x PS101 silicon diodes typically produces the response shown in curve Z: low-frequency error in Vout (mean) \approx +3.7%

Using the PS101 diodes with the 741 operational amplifier replaced by a 301 with a 33-pF compensation capacitor typically produces the response shown in curve 3: low-frequency error in Vout (mean) \approx +3.7%.

Useful range supplies: ±3 to ±18V.
Useful range of Vin: 350mV to 4.2V r.m.s. R4 min for Vout in min and no significant peak clipping \approx 150V.

Circuit modifications

• To measure alternating voltages on a differential-input digital voltmeter the resistor R1 should be replaced with a network that is capable of passing the d.c. and which has a long enough time constant to sufficiently smooth the a.c. ripple. A circuit of the form shown left may be used for this purpose with TR1: BC126, TR2: BC125, R5, R4: 1MΩ, R2, R4: 10kΩ C1: 4.7μF, C2: 22μF, A: 741, D1 to D4: PS101, the response was typically as shown in curve 4: low-frequency error in Vout (mean): +5.4%. Lowest useful frequency was approximately 10Hz. TR1 may be replaced by an f.e.t. or

some other high input impedance circuit such as a follower to allow the use of larger-value bias resistors and a smaller C2 value. Vout can be made equal to the r.m.s. value of Vin by scaling R4 = 2√2/R2.\frac{R1}{R2}.

• The circuit shown centre may be driven from a grounded source and exhibits a very high input impedance but is subject to a common-mode error. The circuit shown right also has a high input impedance, does not have a common-mode problem but must be supplied from a floating source.

Further reading


Cross references
Series 4, card 3.

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