Complementary m.o.s. astable circuit

Circuit description
This integrated circuit package comprises three n-channel and three p-channel enhancement-type m.o.s. transistors which may be arranged to form three separate inverters. The above circuit uses two inverters, the first inverter being biased to its amplifying region by resistor R₁, and in this region the loop gain is sufficient to initiate multivibrator action. When the output of inverter 2 goes high, the input is low and the input of inverter 1 is high. As the capacitor charges up via resistor R₂, the voltage across R₁, and hence the voltage applied to the gate of the first inverter, falls. When this voltage at the junction of C and R₂ passes through the threshold voltage of the first inverter, the output becomes high, switching the output of inverter 2 to a low state. Capacitor C will now charge in the opposite direction via resistor R₁ and when the voltage at the junction of C, R₁ and R₂ rises towards and crosses over the threshold level, the output of inverter 1 again goes low, the output of inverter 2 is switched to the high state and the cycle repeats.

R.f.l. astable circuit

Circuit description
The L914 contains two identical resistor-transistor logic (r.f.l.) gates. In the above arrangement one input to each gate is not used, pins 2 and 3 being grounded to effectively remove Tr₁ and Tr₂ from the circuit. Transistors Tr₃ and Tr₄ are interconnected to form a cross-coupled astable which may be considered to be a two-stage amplifier with its output fed back to its input and having very high loop gain. The circuit is inherently self-starting; any dissimilarity however small between the two halves of the circuit causes one transistor to be off and the other saturated.

Typical performance
IC: CD 4007-AE
Supply: +10V
R₁: 100kΩ; R₂: 1MΩ
C: 10µF; f: 424Hz
Load resistance: ∞
Supply current: 280µA
Square wave available at Vout
Output excursion: 0.03 to 9.9V
Mark-to-space ratio: 0.93
Rise time: 200ns

The waveform achieved is fairly symmetrical because the threshold point is close to half the supply voltage value. However, this means that the mark-to-space ratio is not unity, but this may be arranged by circuit modification. Resistor R₄ also improves the frequency stability of the circuit with respect to supply voltage changes, and should be at least twice the value of R₄.

Component changes
- With supply of +10V, R₄ of 100kΩ, and C of 2.2nF, mark-to-space ratio varies from 0.76 to 0.92:1 for R₄ from 0 to 1MΩ.

Consider Tr₃ on and Tr₄ off. In this state the circuit levels are: Tr₃ collector: Vc(Quat), Tr₃ base: Vbe(on), Tr₃ collector: +V and Tr₃ base: approx. -V due to the negative-going transition at Tr₄ collector. When switched from off to on the charge on C₁ cannot change instantaneously. C₁'s charge will then change with a time constant C₁R₁, as its right-hand plate attempts to change to +V from -V. However, when this potential slightly exceeds 0V, Tr₃'s base-emitter junction becomes forward-biased and it rapidly turns on, its collector voltage falling to Vc(Quat). The negative step passes to Tr₃ base through C₁, switching Tr₃ off. The circuit is now in its other quasi-stable state. This action repeats continuously, producing antiphase square waves at Tr₃ and Tr₄ collectors. The off-times of Tr₃ and Tr₄ are given by t₃ = 0.6931C₁R₁ and t₄ = 0.6931C₂R₂ sec. The p.r.f. of the square waves is thus: f = 1/T, where T = t₃ + t₄. The mark-to-space ratio is adjustable by altering the ratio C₁/C₂ and/or R₁/R₂.
- Components as listed in typical performance data but with finite load resistance $R_L$. Output pulse level down by 10% when $R_L$ is 2.2kΩ.
- Minimum value $R_T$ for acceptable waveform: 6.8kΩ. Waveform improved by using third inverter as buffer. With $R_s$ of zero, $R_T$: 6.8kΩ, C: 39pF, f = 610kHz (supply 10V).
- With $R_s$ of zero, $R_T$: 10kΩ, C: 10pF, f = 650kHz (supply 10V). If supply is increased to 15V, f = 900kHz.

Circuit modifications
- Output waveform duty cycle may be controlled by replacing $R_T$ with the arrangement shown left. The adjustment of this diode shunt causes the frequency of the circuit to vary, and another variable resistance can be added to compensate the change. If a 50% duty cycle is not obtained, reverse the diode $D_3$.
- A voltage-controlled oscillator is obtained when $R_T$ is replaced by the arrangement shown centre. With $V_0$ in the range 0 to +10V using an n-channel device, frequency is variable from approximately 20 to 30kHz for a supply of +10V and $R_T$: 10kΩ, $R_s$: 100kΩ and C: 2.2nF.

A simple way of synchronizing the circuit with an external source is shown right. Components $R_s$, $C_s$ change the natural multivibrator frequency. With components shown, free-run frequency is 2220Hz increasing to 3985kHz when synchronizing components are connected but with zero source signal. Locking frequency range approximately 221 but can depend on level of synchronizing pulse. Suitable pulse level 0.5 to 1.0V.

Further reading
Low-speed astable uses c.m.o.s., Electronic Components, 6 April, 1973, p. 294.
Clock oscillator for telemetry systems uses c.m.o.s. chip to minimize power drain, Electronics Design, vol. 20, 1972, p. 84.

Cross references
Series 8, card 3.
Series 3, card 11.

Component changes
Useful range of supply +1 to +6V (exceeds rating, not guaranteed).
Frequency stability: +2% for 1V increase in supply, -3.5% for 1V decrease.
Useful range of $C_1$ and $C_2$: 220pF to 660pF (p.r.f. ≈ 1.4Hz).
Mark-to-space ratio: 6.8:1 ($C_1$: 100nF, $C_2$: 22μF) to 1.85 ($C_1$: 100nF, $C_2$: 220pF), $V_{out,max}$: 1.8V.
Useful range of $R_1$ and $R_2$: 2.2kΩ, $V_{out,max}$: 2.8V to 33kΩ ($V_{out}$ distorted in “0V” region).
Complementary square wave is available at $V_{out}$.
At either output $V_{out,max}$ falls by 10% when loaded with 4.7kΩ.

Circuit modifications
- As p.r.f. and mark-to-space ratio depend on the $C_1$, $R_1$, and $C_2,R_2$ time constants, a variable-frequency square wave is obtained by switching in different, but equal, values of capacitance and varying the p.r.f. continuously with $R_1$ and $R_2$ in the form of ganged potentiometers. See circuit left, where $R_1$, $R_s$ are 2.2kΩ and $R_s$, $R_s$ are 22kΩ. If only one resistor is variable, the mark-to-space ratio is variable but so also is the p.r.f.
- A modification allows the mark-to-space ratio to be made greater or less than unity by adjusting the position of the slider of $R_s$ (middle circuit) without changing the p.r.f. since $f = 1/T$ and $T = t_1 + t_2$. Hence, with $C_1 = C_2 = C$ and $R_1 = R_s = R$ then $T \propto C (R + R_s) + C[R + (R_s - R_s)] \propto C (2R + R_s)$ which is independent of $R_s$.
- Circuit on right shows modification to use only one capacitor. Useful ranges of $C_1$ and $R_s$ are 100pF to 100μF and 470Ω to 100kΩ respectively. The circuit may be externally synchronized by positive pulses at $T_1$ or $T_3$ base and locks over a frequency range of at least 2:1. Minimum trigger pulse amplitude about 500mV, minimum trigger pulse width about 200ns.

Further reading
Fenwick, P. M., Pulse generator using r.t.i. integrated circuits, Radio and Electronic Engineer, 1969, pp. 374-6.

Cross references
Series 8, cards 8, 12.
Complementary astable circuit

Circuit description
When the supply is connected, \( T_1 \) base and \( T_2 \) collector are at a potential determined by the ratio \( R_1/R_2 \), which could be in the form of a potentiometer to set the upper level of \( V_{\text{out1}} \) and \( V_{\text{out2}} \). The p.d. across \( C_1 \) is zero, so the base-emitter junction of \( T_1 \) is reverse-biased and both transistors are cut off. Capacitor \( C_1 \) begins to charge exponentially with time constant \( C_1R_1 \), causing the p.d. across it to rise towards \( +V_{\text{ee}} \). When the capacitor voltage slightly exceeds the base potential of \( T_1 \), the base-emitter junction begins to be forward-biased, significant conduction occurring when the capacitor voltage is approximately 0.5V more positive than \( T_1 \) base.

Typical performance
Supply: +9V, 4.5mA
\( T_1 \): BC126; \( T_2 \): BC125
Diode: HP5082-2800
\( R_1 \): 27k\( \Omega \); \( R_2 \): 47\( \Omega \)
\( R_3 \), \( R_4 \): 1k\( \Omega \); \( C_1 \): 10nF
P.r.f.: 6.1kHz
Mark-to-space ratio: 49:1
Rise time of \( V_{\text{out1}} \): 1.2\( \mu \)s

Positive feedback, due to the interconnection of the bases and collectors of the complementary pair of transistors, ensures that this transition to the on-state is very rapid. Thus \( C_1 \) discharges through \( T_1 \) and \( T_2 \) with \( R_2 \) providing a discharge current-limiting action. Diode \( D_1 \) prevents the transistors saturating and ensures that the circuit can re-cycle.

The capacitor does not completely discharge, but as the current in the transistors falls the loop gain around \( T_1 \) and \( T_2 \) reduces to a value that cannot maintain conduction, which ceases when \( T_2 \)'s emitter voltage falls to about 1V. Both \( T_1 \) and \( T_2 \) rapidly switch off allowing \( C_1 \) to recharge through \( R_3 \) and \( V_{\text{out1}} \) returns to its initial value determined by \( R_2/R_3 \). During the discharge of the capacitor, a narrow negative-going pulse is obtained at the junction of \( R_3 \) and \( R_4 \) due to the conduction of \( T_2 \).

T.t.l. Schmitt astable circuit

Circuit description
This circuit is internally constructed to behave as a Schmitt trigger, i.e. having two distinct output states, switching between them according to the voltage at the input, with a constant hysteresis between the input levels for switching. The relationship between the input and output states is shown above. The output remains low for \( V_{\text{out}} > V_{\text{inL}} \) and \( V_{\text{inH}} \) would remain at this level until the input voltage was reduced to less than \( V_{\text{inH}} \).

In the circuit, a convenient starting point of the output high and the input low may be assumed. The capacitor will tend to charge up towards the output voltage, but when the capacitor voltage reaches the transition level for the i.c., the output falls to near zero voltage. The capacitor then discharges through \( R \) until its potential reaches that at which the reverse of the output states occurs, where the output again goes high.

Typical performance
IC: 1 SN7413
Supply: 5V
\( R \): 330 \( \pm 5\% \)
\( C \): 220nF \( \pm 5\% \)
f: 10.8kHz
Mark-to-space ratio: 0.5:1

Component changes
Useful range of \( R \): 220 to 1000\( \Omega \). Astable will not function for \( R \geq 1.5\k\( \Omega \).
Useful range of \( C \): 2.2nF to 22\( \mu \)F.
Useful range of supply: 4.5 to 5.5V. Operation outside this rated range is possible, but performance not guaranteed. Typically with \( R \): 680\( \Omega \) and \( C \): 47nF, frequency range is 1.9 to 2.4kHz for supply ranging from 3.5 to 7V.
For supply of 4.5 to 5.5V, frequency stability is approximately \( \pm 3\% \). Circuit will supply loads from infinity down to 1k\( \Omega \), with a reduction of frequency of less than 2.5%.

Circuit modifications
- Normally the four inputs of the input nand gate may be used in parallel or taken to the supply rail.
Component changes
Useful range of supply: +2 to +18V.
Useful range of C1: 100pF to 1,000μF.
Minimum load resistance at V\text{outs} ≈ 220Ω.
Frequency stability: +0.3%/V increase in supply.
Tr1: ME0413, 2N3906, BCY71
Tr2: ME4103, 2N3904, BC107.

Circuit modifications
- Replacing R1 and R2 by a potentiometer across the supply changes the value of the capacitor voltage required to trigger the transistors into conduction and hence controls the period and amplitude of the output waveforms for given values of C1 and R1.
- Narrow positive-going pulses in antiphase with those at V\text{outs} can be obtained by including a small resistor in series with Tr2 emitter to the 0-V rail.
- The 'exponential' waveform, V\text{outs}, can be made into a more linear sweep by replacing R1 with a constant-current source. This sweep output can be extracted without significant loading by using an emitter follower. Linearity of the sweep output may be improved by splitting R1 into R1a and R1b and bootstrapping their junction with C2, as shown left, where C2 should be of the order of 100μF.
- If D1 is required to be a silicon diode, additional silicon diodes D2 and D3 should be added as shown centre where all diodes could be of the 1N914-type.
- A dual-supply version of the circuit, which is otherwise identical with the single-supply form, is shown right where both outputs are taken w.r.t. ground. Both outputs can then be made to switch between more widely-varying levels and by adjusting the ratio R7/R8 to set Tr1 base to zero volt in the off-state, negative pulses may be obtained at V\text{outs}.

Further reading

Cross references
Series 2, cards 5, 12.
Series 6, card 8.
Series 3, card 6.
Series 8, card 1.

Further reading
Texas Instruments: SN7413 Data Sheet.

Cross references
Series 2, cards 3, 8.
Series 8, card 10.
Wireless World Circard Series 8: Astable Circuits

Operational amplifier astable circuit

Typical performance
IC: 301
Supply: ±15V
C1: 4.7nF ± 5%
P1: 4.7kΩ ± 5%
R1, R2: 5kΩ ± 5%
Output square wave:
28V pk-pk
Slew rate: 8V/μs
Variation of frequency with feedback factor and capacitance C1 shown on graphs.

Circuit description
The circuit shown uses an operational amplifier where the output switches between the positive and negative saturation levels of the amplifier, giving a square wave output. The period of the waveform depends on the time constant CR and the feedback factor, determined by the ratio of Rf/(R2 + R1). When the output has switched to the positive saturation level, the voltage at the non-inverting input is +VRsat Rf/(R2 + R1) and the voltage at the inverting input is negative with respect to this value. However capacitor C1 now begins to charge towards +VRsat, but when the capacitance voltage is almost equal to the feedback voltage, the amplifier comes out of saturation, and the regenerative action due to the positive feedback drives the amplifier quickly into negative saturation before the capacitance voltage can alter. C1 will now charge towards −VRsat, but again a rapid transition to the positive saturation state will occur when the voltage across C1 reaches −VRsat Rf/(R2 + R1), and the cycle repeats. The duty cycle of this astable circuit is almost independent of the pulse repetition frequency, because the threshold levels are fairly well specified to each op-amp.

Component changes
Useful range of R1: 6.8k to 22kΩ.
Useful range of C1: 10μF to 470μF for R1 = 4.7kΩ.
Frequency stability: For C1 = 22nF, R1, R2, Rf = 5kΩ; R1 = 4.7kΩ. supply of ±15V and f = 4470Hz, decreasing supply to ±10V reduces frequency by < 1%.
Operation possible down to ±3V; frequency down by 8%.
Any other operational amplifier may be used, e.g. 741, but frequency range restricted because at higher frequencies

Wireless World Circard Series 8: Astable Circuits

Astable blocking oscillator

Typical performance
Supply: ±10V, 860μA,
−3V 1.1mA
Tr1: BC125, D1: SP2
R1: 6.8kΩ; C1: 4.7μF
L1: 30 turns of 36 s.w.g.
en. Cu
L2: 15 turns of 36 s.w.g.
en. Cu; both on FX2049 ferrite core.
P.r.f.: 46.6kHz
Pulse width: 1.15μs

At switch-on the base-emitter junction is forward-biased and the collector current rapidly rises to almost equal the emitter current which depends on R1 and −V. The transformer ensures that a much larger emitter current flows to saturate Tr1 and C1 charges in a direction that reverse-biases the base-emitter junction causing Tr1 to cut-off. A very narrow pulse is generated and the circuit will not regenerate until C1 has discharged through R1. When Tr1 cuts off D1 protects the base-collector junction from the large induced e.m.f. In L1 and restricts Vem to −V. Capacitor C1 should be large enough to ensure that the magnetizing inductance of L1 controls the pulse width and C1 controls the off-time. The pulse width depends on C1 rather than L1 if C1 is too small.

Component changes
Useful range of −V: −4 to +14V; −Vmin: −1V.
Useful range of R1: 470Ω to 10kΩ.
waveform becomes trapezoidal. Typically, for \( R_1 = 2.2k\Omega \), \( R_2(R_3 + R_4) = 0.7 \) and \( C_1 \) from 10\( \mu \)F to 220nF, frequency in the range 24Hz to 1.8kHz. Slew rate 0.6V/\( \mu \)s.

A comparator such as the 72710 will give an output pulse excursion of \(-0.5 \) to \(+2.8V\) for supplies of \(+12V\) and \(-6V\). For \( R_4 \), \( R_2 \): 5k\( \Omega \), useful range of \( R_1 \) is 1.5k \( \Omega \) to 6.8k\( \Omega \) and \( C_1 \) 47pF to 22uF giving frequencies in the range 630kHz to 3Hz.

**Circuit modifications**

- Interchange \( C_2 \), \( R_3 \) and the input connections as shown left. For similar component values as in main diagram, frequency is reduced to approximately one third. Note that the derivative of square-wave output is obtained at the non-inverting input.
- Output levels may be clamped for driving t.t.l. loads by connecting a zener diode/resistance network across the output. Clipping at much lower current levels is possible with some amplifiers (e.g. 301), where access is available to the drive point of the output stage. An adjustable arrangement is shown in the middle circuit.

\[ C_1(\text{min}) = 470nF. \]

Minimum load resistance at \( V_{out} = 2.2k\Omega \).

Frequency stability: \(-0.96\% / V \) increase in \(+V\), \(-0.77\% / V \) increase in \(-V\).

**Circuit modifications**

- It is often convenient to obtain the output pulse from a third winding \( L_2 \) to provide d.c. isolation, a suitable transformer turns ratio for \( L_1 \), \( L_3 \) and \( L_4 \) being 1:1:1.
- A diode \( D_2 \) can be connected as shown left to prevent saturation of the transistor. As the collector current increases during switch-on, the collector voltage falls until it reaches \(+V_A\) causing \( D_2 \) to conduct clamping the collector at approximately \(+V_A\). The current shunted from the collector by \( D_2 \) decreases as that in the magnetizing inductance of \( L_1 \) increases, the on period of \( T_{tr} \) ending when the diode current falls to zero.
- Middle left circuit shows a single-supply version of the circuit with \( R_1 \) and \( C_1 \) in the emitter. The \( R_1 \), \( C_1 \) time constant determines the time for which \( T_{tr} \) is off and hence the mark-to-space ratio can be varied by means of \( R_1 \). Alternatively, the p.r.f. may be adjusted by means of \( R_4 \) which controls the base potential and hence the timing of the off/on transition.

- An unequal mark-to-space ratio may be obtained by using the circuit shown right. The two resistors \( R_{1a} \) and \( R_{1b} \) are selected by the switching action of diodes \( D_1 \) and \( D_2 \), \( D_3 \) conducting when the output is negative, and \( D_4 \) when the output is positive.

**Further reading**


National Semiconductor application note AN4-1.

\[ \begin{align*}
C_1(\text{min}) &= 470nF. \\
\text{Minimum load resistance at } V_{out} &= 2.2k\Omega. \\
\text{Frequency stability: } -0.96\% / V \text{ increase in } +V, -0.77\% / V \text{ increase in } -V. \\
\text{Circuit modifications} \\
- \text{It is often convenient to obtain the output pulse from a third winding } L_2 \text{ to provide d.c. isolation, a suitable transformer turns ratio for } L_1, L_3 \text{ and } L_4 \text{ being } 1:1:1. \\
- \text{A diode } D_2 \text{ can be connected as shown left to prevent saturation of the transistor. As the collector current increases during switch-on, the collector voltage falls until it reaches } +V_A \text{ causing } D_2 \text{ to conduct clamping the collector at approximately } +V_A. \text{ The current shunted from the collector by } D_2 \text{ decreases as that in the magnetizing inductance of } L_1 \text{ increases, the on period of } T_{tr} \text{ ending when the diode current falls to zero.} \\
- \text{Middle left circuit shows a single-supply version of the circuit with } R_1 \text{ and } C_1 \text{ in the emitter. The } R_1, C_1 \text{ time constant determines the time for which } T_{tr} \text{ is off and hence the mark-to-space ratio can be varied by means of } R_1. \text{ Alternatively, the p.r.f. may be adjusted by means of } R_4 \text{ which controls the base potential and hence the timing of the off/on transition.} \\
- \text{An unequal mark-to-space ratio may be obtained by using the circuit shown right. The two resistors } R_{1a} \text{ and } R_{1b} \text{ are selected by the switching action of diodes } D_1 \text{ and } D_2, D_3 \text{ conducting when the output is negative, and } D_4 \text{ when the output is positive.}
\end{align*} \]
T.T.L. dual inverter astable circuit

Circuit description
Capacitor C1 alternately charges and discharges through R2, because loop gain of the system ensures that the output of the second inverter switches between logic 0 and logic 1 states. When the potential difference with respect to ground at the input of I2 crosses the critical level, Resistor R1 is necessary to bias the first inverter I1, and thus prevent the possible stable state of inverter I1 output at approximately 0V in the logic zero state, and the output of I2 in the logic 1 state. Charge and discharge cycles have different durations because the input switching level is not symmetrical with respect to the output 0 and 1 states, and also there is an additional charging path for the input of the second inverter at 0 state. Note that when using nor gates as inverters, the unused input should be tied to logic 0 voltage level.

Typical performance
Supply: 5V
IC: 7402.
R1, R2: 1kΩ ±5%
C: 100pF ±5%
Frequency: 2.78MHz
Stability: ±1% for supply in the range 4.75 to 5.25V for a span of 3kHz to 3MHz

Component changes
Useful range of C: 100pF to 22μF.
Useful range of R1: 220Ω to 1kΩ.
Useful range of R2: 150Ω to 1kΩ.
Alternative IC: SN7404 hex inverter.
Circuit operates within the supply range 4.5 to 6V, but not guaranteed outside t.t.l. voltage limits.
In an attempt made to achieve high frequencies, the range of resistance values is critical. Typical values R1: 1kΩ, R2: 330Ω, C: 120pF, f: 6.7MHz. With nor or nand gates, a spare input is available for external synchronization. Frequency will lock over the range of 4:1 with input pulse widths down to 100ns (positive-going pulse for nor, and negative-going for nand). Capacitive coupling of the trigger source may be used with the inverters of SN7404. Typically C7 = C/100. Three separate, harmonically-locked astables can then be produced.

Coupled logic gates astable circuit

Circuit description
The values of the current sinking resistors R1 and R2 are critical in this type of circuit, which uses nor logic gates in a cross-coupled mode. It is possible for both gate inputs to sink logic 0 level input currents simultaneously, and this produces a stable state in which both outputs are at logic 1. To avoid this choose values of R1 and R2 so that the gate input levels are near the logic threshold level; as the capacitors go through their charging cycles, one gate will be above and one below the threshold level. Assume the Q output has changed from the 0 to 1 logic level of approximately +3V due to the input having reached the threshold value. This output transition is coupled through the capacitor C2 to make the input of the first gate high, and hence the output Q is low or logic 0. As C2 charges up towards the positive supply via R1, the voltage across R2 and hence the input level at the first gate decreases. At the same time C1 charges via the base resistor of the input transistor of the gate. The output will change state at a time dependent on whichever gate input first crosses the threshold level. Output Q will then be high (approximately +3.0V) and free of feedback. Capacitor C1 will now tend to charge in the opposite direction towards +5.0V due to the input having reached the threshold value. This output transition is coupled through the capacitor C2 to make the input of the second gate high, and hence the output Q is low or logic 1. As C1 charges up towards the positive supply via R2, the voltage across R1 and hence the input level at the first gate decreases. At the same time C1 charges via the base resistor of the input transistor of the gate. The output will change state at a time

Typical data
Supply: 5V
ICs: 74102
R1, R2: 2.2kΩ ±5%
C1, C2: 0.1μF ±5%
Frequency: 2015Hz
Mark-to-space ratio: 1.27:1
Pulse excursion: 0.3 to 3.2V
Connect unused inputs to ground to avoid inverter operation.

Frequency of oscillation is determined by C1, C2, R1 and R2. If C1 = C2 = C, R1 = R2 = R, the frequency is approximately f = 1/(2CR ln(2)) where C is in farads and R in ohms. Provided resistors are carefully chosen to ensure self-starting, a wide range of frequencies are available by changing C1 and C2. This type of circuit using standard gates or inverters does not provide stable frequencies as the threshold voltages depend on temperature and supply voltage.
Circuit modifications
- Remove $R_4$ and connect the capacitor in the feedback loop (circuit left). The third inverter sharpens up the waveform. With supply of $+5V$, $C_{22nF}$, $R_1$: $1k\Omega$ max. to $100\Omega$ min., frequency is in the range $22.5$ to $165kHz$; mark-to-space ratio approximately $0.6/1$.
- Middle circuit uses the SN7404 again, where frequency of oscillation is determined by the propagation delays through the gates. The external capacitance changes the delay associated with two gates and thus alters the frequency. Useful range of $C$: $1$ to $10nF$. Frequency 4 to $0.5MHz$. Waveform essentially square, but deterioration evident above about $3MHz$. Frequency stability fairly poor. Approximately $\pm 10/\%V$.
- Tuning resistors in the middle network comprise the integrated circuit resistors. With perhaps resistance variations of $\pm 20/\%$ from device to device, and a like tolerance over the temperature range $-55$ to $+25^\circ C$, the possibility of frequency and pulse width variations exists. This effect can be minimized for a given output by connecting precision external components as shown right. Output frequency may then remain within $\pm 5/\%$ for device or temperature changes. Typically $R$ should be $1k\Omega \pm 1/\%$.

Further reading
MDTL Multivibrator Circuits, Motorola application note AN-409.

Cross reference
Series 8, card 8.

Circuit changes
Use MC7402F, though note pin numbers different.
Useful range of $R_1$, $R_3$ is restricted to ensure that circuit starts $2.2$ to $3.3k\Omega$.
Useful range of $C_1$, $C_3$: $27pF$ to $10\mu F$ with the above resistor values.
With $C$: $0.1\mu F$, and a supply of $+5V$, a variation of supply voltage of $\pm 5\/%$ produces a percentage frequency change of $+5/\%$ or $-9/\%$ respectively.
Nand gates may be used in place of nor gates. In this case, unused pins should be connected to the positive supply line. Waveform of basic astable circuit is improved when the output is applied through an additional gate.
Mark-to-space ratio adjustable by having different values of $C_1$ and $C_3$.

Circuit modifications
- Range of resistance values for $R_1$ and $R_4$ ensuring self-starting increased slightly, if $R_4$ is taken to output (left). Range then $1.5$ to $3.3k\Omega$.
- Emitter-coupled logic gates in the middle configuration can provide a high frequency signal, but the component values tend to be critical. $IC_1$, $IC_4$, $IC_3$: $1/2$MC1011 quad-nor gates using $1.5k\Omega$ pull-down resistors; supply: $-5.2V$. Unused input pins connected to $-V_8$. Repetition frequency $25MHz$. Waveform improved by third gate.
- Arrangement shown right would use a single quad two-input nand gate, useful $C$ range being $10pF$ to $1\mu F$. Self-starting problem may be overcome with an extra gate, but a $3$-input nand gate then required (cf. Mullard).

Further reading
2MHz Square Wave Generator uses two TTL gates, p. 110, 400 ideas for design, vol. 2, Hayden.

Cross reference
Series 8, card 7.
Emitter-coupled astable circuit

Circuit description
Compared to a conventional saturating, cross-coupled astable circuit, this emitter-coupled circuit uses a single timing capacitor, is capable of producing an improved output waveform, and can operate at higher frequencies and can be designed to provide a much better frequency stability. The higher switching speeds are obtained because neither transistor is allowed to saturate and the output waveform does not switch between wide limits.

Consider the circuit to be in the state of Tr1 off and Tr2 on. Tr2 emitter current of R6 divides into a component in R4 and a charging current in C1 and R4. At the instant that Tr1 switches on this charging current produces negligible p.d. across C1 and a p.d. across R4 sufficiently large to ensure that Tr2 is off. As C1 charges, its p.d. increases and that across R4 falls until the base-emitter junction of Tr1 becomes forward-biased. Transistor Tr1 begins to conduct and the emitter current of Tr1 falls causing the collector potential of Tr1 and the base potential of Tr2 to rise. This action causes Tr2 to conduct more heavily and Tr1 to switch off. This sequence is then repeated with Tr2 emitter providing the current to charge C1 through R4 until the switching action restores the circuit to its original state of Tr2 off and Tr1 on.

\[ t_a = \frac{C_1 (R_4 + R_5)}{\left(1 - \frac{V + V_{BE off}}{V + V_{CE on}} \right) \left[ \frac{R_5}{R_1 + R_5} + \frac{R_4 (R_1 + R_5)}{R_1 R_5} \right] - \frac{R_4}{R_5} - 2} \]

Discrete-component Schmitt astable

Circuit description
This circuit is a Schmitt trigger with overall feedback provided via R1 and C1. Consider C1 to be uncharged, then when the supply is connected Tr1 emitter is initially at 0V but Tr2 immediately conducts due to the base drive through R2. Thus Tr2 emitter rapidly switches to a level close to +Vcc and, with R2 = R6, Tr1 emitter rises to half this value. However, Tr1 remains cut off due to the lack of base drive. Capacitor C1 begins to charge "exponentially" through R1 aiming to reach the emitter potential of Tr1, but when the capacitor voltage exceeds that at Tr1 emitter the capacitor begins to discharge mainly through R3, R4 and R5 and partially through R4, Tr1 base-emitter junction and R4 driving Tr1 on and into saturation. The collector potential of Tr1 falls to a low value as also does Tr2 emitter, its being insufficient p.d. available to keep Tr2 in conduction so that it switches off. C1 continues to discharge until Tr1 comes out of saturation, when its collector potential rises sharply. This rise is transferred to Tr2 emitter, which begins to conduct, and hence to the emitter of Tr1. This positive feedback rapidly cuts off Tr1 leaving Tr2 in full conduction until, as C1 charges again through R3, the higher potential needed at Tr1 base to restart the cycle is attained.

Component changes
Useful range of \(+V_{cc}\): +4 to +15V.
Useful range of C1: 100pF to 1000pF.
Frequency stability: \(-0.46\% / \text{V increase in } +V_{cc}\).
R1 = 10k\Omega; R2 = 4.7k\Omega
R3 = 2.2k\Omega; C1 = 10nF
P.r.f.: 9.83kHz
Mark-to-space ratio: 1.13/1
Rise time: 400ms
Fall time: 300ms
Component changes
Useful range of $+V$: +2 to +14V.
Useful range of $-V$: -2 to -10V.
Useful range of $R_s$ and $R_f$: 220Ω  to 4.7kΩ.
$R_{4\text{min}}$: 1kΩ (m-s ratio 3:4:1), $R_{4\text{max}}$: 27kΩ (m-s ratio 1:10).
$R_{4\text{min}}$: 1kΩ (m-s ratio 1:4), $R_{4\text{max}}$: 33kΩ (m-s ratio 8:1).
Useful range of $C_1$: 180pF to 1000μF.
Frequency stability: $-1.2\%/V$ increase in $+V$, $-6\%/V$ increase in $-V$.
$T_1$ and $T_2$: ME4103, 2N708, HE301, BSY95A.

Circuit modifications
- If $R_s$ and $R_f$ are replaced by a potentiometer connected across $C_1$ with its sliding contact taken to the $-V$ rail, the mark-to-space ratio of the output waveform may be varied without changing its frequency.
- The on-time of $T_1$ is independent of the supply voltages and the on-time of $T_2$ depends on the ratio $+V/[1 - +V/V_{\text{BE(on)}}]$. Hence, high frequency stability is obtained if the ratio of the supply voltages is constant. This condition is assured if only a single supply is used as shown left which can provide a frequency stability of 1% for a ±50% change in $+V_{CC}$.

$R_{4\text{min}}$: 47Ω (m-s ratio 1:2.8, $f \approx 33$kHz), $R_{4\text{max}}$: 2.2kΩ ($V_{\text{out}}$ reduced to 5V pk-pk).
Useful range of $R_s$: 220Ω to 4.7kΩ.
$T_1$ and $T_2$: ME4103, BC107, BC109, 2N3904.
Observe $V_{\text{BE(on)}}$ as well as $V_{\text{CE(max)}}$ rating.

Circuit modifications
- If $R_s$ is not too large the p.r.f. only is affected by adjusting the $R_s/C_1$ time constant; this will not be the case when $R_s$ reaches a value that is comparable with the relatively high resistance discharge path through $R_s$. The base-emitter junction and $R_s$. Both the p.r.f. and mark-to-space ratio can be made variable by varying the $R_s/R_s$ potential divider ratio. Resistors $R_s$ and $R_f$ can conveniently be made into a continuously-variable potentiometer or $R_s$ can be made a voltage-variable resistor, e.g. by use of a f.e.t.
- When a small, but controlled, mark-to-space ratio is required $R_s$ may be replaced by the resistor-diode combination shown left. Both diodes could be of the 1N914 type. The circuit may be synchronized with an external oscillator by resistive coupling to the emitter of $T_1$ or by capacitive coupling to its base.

- $R_s$ and $R_f$ in the original circuit may be replaced by constant-current tails. Middle circuit shows a pair of parallel current mirrors making the emitter currents of $T_1$ and $T_2$ equal and controlled by $R_s$, allowing the frequency to be varied without affecting the mark-to-space ratio.
- The constant-current sources may be voltage controlled, by $R_s$ in the circuit shown right and the currents in $T_1$ and $T_2$ controlled independently by $R_s$ and $R_f$ respectively. A larger amplitude output, at slower speed, may be obtained by connecting the original output point to the base of a n-p-n transistor with its emitter connected to the $+V$ rail and its collector returned the $-V$ rail through a $1\Omega$ resistor. If this resistor is connected instead to the $0-V$ line a t.t.l.-compatible output is obtainable using $+V = +5V$.

Further reading
Cross reference
Series 3, card 2.

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- Addition of $T_3$, as shown middle, allows the timing of the output square wave to be more nearly controlled by the $R_s/C_1$ time constant. $T_1$ and $T_2$ form a long-tailed pair so that the junction of $C_1$ and $R_s$ are effectively connected to one input of a differential operational amplifier.
- Circuit right shows a similar form of modification which has the merit of allowing $V_{\text{out}}$ to swing almost between the levels of the supply rail potentials.

Further reading

Cross references
Series 2, cards 2, 7.
Series 8, cards 4, 5 & 12.

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Dual-monostable astable circuit

Typical performance
Supply: +5V, 46.5mA
ICs: SN74121N
(monostable)
Tr1, Tr2: ME0413;
D: PS101
C1, C2: 10nF
R1: 2kΩ
R2, R3: 1kΩ
Frequency: 28.6kHz
Pulse excursion: 0.2 to 3.6V
Rise time: 100ns
Fall time: 50ns

Circuit description
Astable circuits can be constructed out of cross-coupled monostable circuits provided that the output of one monostable can be used to initiate the timing cycle of the other. The circuit shows the interconnection between two i.f.l. monostable i.c.s. The timing capacitors for the two parts of the period are C1 and C2, and these might be equal or different, depending on the need for unity or other mark-to-space ratios. In place of the resistive part of the timing circuit, Tr1 and Tr2 provide constant currents, so that the capacitors charge linearly. This allows a ramp waveform to be extracted at pin 11 on either i.c. It has the further advantage that varying the common potential at the bases of Tr1 and Tr2 with R3 allows both charging currents to be varied simultaneously, i.e. a change in frequency without change in mark-to-space ratio. By varying the tapping point on R3, the balance between the currents in Tr1, Tr2 collectors are changed and the mark-to-space ratio is varied with a relatively small change in total period, i.e. in frequency. Diode D2 gives temperature compensation for the base-emitter potential changes of Tr1 and

Astable circuit with f.e.t.

Typical data
Supply: +9V, 760μA
Tr1: 2N5457;
Tr2: BC126
R1: 100kΩ; R2: 10MΩ
R3: 3.3kΩ; R4: 6.8kΩ
C1: 1nF
P.f.s: 31.2Hz
Mark-to-space ratio:
1.71:1

Circuit description
When the supply is connected both active devices conduct with currents determined by the negative feedback due to R4 and R5. The collector potential of Tr2 jumps sharply to a level approaching +Vcc and the source of Tr1 jumps towards Vcc R4(R5 + R6). With C1 initially uncharged, the full positive step at Tr2 collector is passed to the gate of Tr1 so that the gate-source junction becomes forward biased by about 500mV and the charging current flows through it to ground via R4. The initial charging current in C1 is thus larger than it would have been if C1 charged simply through R5. The p.d. across R2 falls rapidly as C1 charges through R4 causing the f.e.t. junction to be reverse biased and the charging time constant of C1 to charge to the much larger value of C1R5. Capacitor C1 continues to charge until the gate potential of Tr1 falls below its source potential by an amount that approaches the pinch-off value causing Tr2 to switch off due to the reduction of base current.

The output switches back to virtually 0V as C1 discharges through R2, R3 and R6, where R4 >> R5 + R6, until the gate source p.d. allows sufficient drain current in Tr1 to switch Tr1 on and the circuit re-cycles. Due to the low reverse-bias gate current of the f.e.t., long time intervals can be obtained between the changes of state using reasonable component values, provided that C1 is a low-leakage type. The accuracy of these long time intervals however depends on ill-defined value of the pinch-off voltage of the f.e.t.

Component changes
Useful range of supply: +6 to +30V.
Useful range of C1; 10pF to 100μF, low-leakage type.
Tr₂. Long periods may be attained by lowering R₄ so that the charging currents in the transistors are small, but the period then becomes more temperature and supply sensitive. Independent anti-phase voltages are obtainable at the Q outputs of the two ICs without any loading effects on the interconnection circuitry.

Component changes
With C₁, C₂: 10μF and minimum setting of R₄, frequency is 1.6kHz. With C₃, C₄: 100nF, and maximum setting of R₁, mark-to-space ratio is variable from 0.03 to 0.98.
Frequency stability within ±3% for a supply change of ±0.5 on 5V.
Resistive loading may be reduced to 2.2kΩ to maintain pulse height within 90% of maximum level. Absolute minimum load 150Ω where pulse level is then down to 1.9V.
For fixed capacitance, frequency range roughly 10/1 by varying R₁.

Circuit modifications
- Replacement of Tr₁, Tr₂ by resistors connected from pin 11 on each IC to supply line, i.e. replacing the current source by the more normal resistive source, gives non-linear charging of C₁ and C₂, but is a lower cost arrangement (left).
- Any other current source may replace Tr₁ and Tr₂, e.g. p-channel field-effect transistors, with either variable voltage on the gate, or variable resistance in the source (middle circuit).
- Use a retrigerable monostable SN74L122 in the configuration shown right. This monostable has a similar behaviour to a Schmitt trigger when the timing capacitor is driven from the Q output. Pins 1 and 2 may be taken to supply line and 3 and 4 to ground.

Further reading

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R₁min: 4.7kΩ.
Useful range of R₄: 1 to 200MΩ.
Useful range of R₂: 2.2 to 33kΩ.
Useful range of R₃: 33Ω to 10kΩ.
Minimum load resistance: 220Ω.
Frequency stability: +1%/V increase in Vcc.

Circuit modifications
- Another circuit that can produce output pulses separated by a long time interval is shown left. When the supply is connected, the low-leakage capacitor C₁ charges through R₁ until the gate potential of the n-channel j.f.e.t. reaches the threshold voltage of the programmable unjunction transistor Tr₂ minus Vgs(off) of Tr₁. On reaching this gate voltage of +VccR₁(R₂ + R₄ - Vgs(off)), the gate-source junction of Tr₁ becomes forward biased and C₃ discharges through it to ground via Tr₂ and R₄ providing an output pulse across R₄. Transistor Tr₁ then cuts off and the charge-discharge cycle of C₃ is repeated.
- Caution is necessary in replacing bipolar junction transistors, in circuits that are known to work by field-effect transistors. In the middle circuit Tr₁ of a Schmitt astable has been changed to an n-channel j.f.e.t. but for a given pinch-off voltage and R₄ value there may be insufficient drain-source p.d. to allow the switching action to take place, except by critically adjusting the ratio R₂/R₄. This situation is improved by inserting a zener diode between the drain of Tr₁ and the base of Tr₃.
- Circuit right shows a cross-coupled astable where n-p-n transistors have been replaced with n-channel j.f.e.ts. This circuit will not switch unless R₄ and R₅ are returned to ground instead of +Vcc and should be returned to a slightly negative rail to ensure self-starting.

Further reading
FET and UJT provide timing over a wide temperature range, in 400 Ideas for Design, Hayden, 1971, pp. 192/3.

Cross references
Series 8, cards 2, 5 & 10.

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