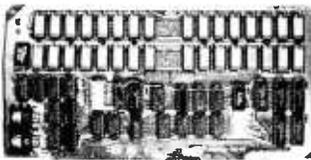


S-100 Boards from S. C. Digital



256K DYNAMIC RAM

features: **Model 256KE**
 ● 18 or 24 bit address. ● 8/16 bit wide data ● Transparent refresh with unlimited DMA, immune to Wait States, halts, resets. ● Fast access time 180nsec from Memr or Psync high, will run with Z80, Z8000 to 8mhz, 8080, 8085, 8086 to 8mhz without Wait States. ● Accepts 4116, 4164's.

64K DYNAMIC RAM 'Uniselect: 2'

features: **Model 64KUS**
 ● 16 or 24 bit address. ● 8 bit data. ● Bank select by SW settable port, bits in two blocks. ● Two 32kb (128kb) addressing. ● Transparent refresh - same as M:256KE. ● Fast access time - 220nsec, will run with Z80, Z8000 to 4mhz, 8080, 8085, 8088, 8088 to 5mhz without Wait States. ● Can be configured to various multiusers OS's. ● Expandable to 256KB using 4164's.

32K STATIC RAM 'Uniselect: 3'

features: **Model 32KUS**
 ● Fully Static using 2k by 8 NMOS chips. ● 16 or 24 bit address. ● 8/16 bit wide data. ● Bank Select by port and bit in 32K block. ● Two 16K block addressing with window capability in 2k increments. ● EPROM can be mixed with RAM. ● Fast access - 250nsec from address valid - will run with Z80, Z8000 to 4mhz, 8080, 8085, 8088, 8088 or 88000 to 8mhz without Wait States. ● Provision for Battery Backup.



Z80 CPU Board

features: **Model CPU1 Z80**
 ● 2 or 4mhz clock. ● Jump on Reset. ● 8 levels of prioritized vectored interrupts.

I/O, Memory Interface 'Interface: 1'

features: **Model 3SPC**
 ● 3 serials using UART, RS-232C or 20ma current loop. ● 1 Parallel I/O with hand shakes. ● 4k Ram, 4k EPROM (not supplied). ● Built in Kansas City Audio Cassette interface. ● Baud rate generator from 19.2kbaud to 110 baud.

2K Z80 Monitor Program available for M:3SPC

features: many routines including breaker points, cassette record and play back . . . etc. Comes in 2 EPROMs and 1K RAM.

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256KE-128	\$535	128KB	AGT
64KUS-64	\$395	64KB (4164's)	AGT
64KUS	\$395	64KB (4116's)	AGT
64KUS-16	\$285	16KB	AGT
32KUS	\$395	32KB	AGT
32KUS-16	\$285	16KB	AGT
32KUS-N	\$140	no memory	AGT
CPU1-Z80	\$219	with interrupt	AGT
CPU1-Z80-K	\$140	no interrupt	KI
3SPC	\$229	with cassette	AGT
3SPC-KC	\$159	with cassette	KI
2K Monitor	\$ 55	with 1K Ram	

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because its extensive instruction set has to be mapped to the 8086 instructions, as well as the 8080 registers.

The 8086 does, however, have a rich instruction set that covers all the bit instructions and most of the block instructions. The problems encountered in mapping instructions and registers can be formalized and solved by using a variety of software tools.

To convert a source file running under CP/M-80 so as to assemble it with an 8086 assembler requires either the use of a code translator or a considerable effort with a program editor. At least three commercial products come under the translator category:

- XLT86 from Digital Research Inc.
- TRANS86/ACT86 from Sorcim
- The Z80-to-8086 translator from Seattle Computer Products

Intel also has a translator, CONVERT 86, but it is sold only as part of a large software package intended for its OEM customers and doesn't run under CP/M. In addition, some reports indicate that Microsoft may soon bring out a translator.

Two issues must be addressed when converting from a CP/M-80 source:

1. Where is the source coming from?
 Z80 instruction mnemonics?
 (a) Zilog
 (b) TDL (Technical Design Labs)
 (c) Intel (Digital Research with macros)
 (d) Sorcim/ACT-80

or

Straight 8080/8085 code with no macros?

2. Where is the resultant code going?
 CP/M-86 or MS-DOS?

The three translators under review do not always approach these issues in the same way. Furthermore, they all handle register mapping somewhat differently. We'll look at the

translators now one at a time. Then we'll see how they translated the same CP/M-80 listing. With the listing in hand, we'll see how each of the translators handled register mapping. Finally, we'll turn to the subject of how the two different 16-bit operating systems affect program translation.

XLT86 from Digital Research

Digital Research's XLT86 takes standard 8080 source code in a format compatible with ASM, MAC, or RMAC assemblers and converts the 8080 source code to 8086 source code in a format compatible with ASM86 operating under either CP/M-80 or CP/M-86. Since XLT86 is written in PL/I-80, the translator can run either stand-alone under CP/M-80 or for cross development under VAX/VMS. It produces optimized 8086 code in a five-phase, multipass process, doing global data-flow analysis to determine optimal register usage.

Although macro definitions are not supported, conditional-assembly directives are. The *XLT86 User's Guide* suggests that if you want macro expansion, you can use a pass through MAC or RMAC to produce a PRN file that can be edited (removing the first few columns of generated hexadecimal code) to produce an expanded source file for input acceptable to XLT86. XLT86 does not recognize Z80 instructions. XLT86 passes repeat loops through to the 8086 source code.

XLT86 analyzes the source program in its entirety, determining the block structure and the register/flag usage. Working from this information, it translates the code to 8086 assembler code in an optimized way. The decision algorithm for each instruction type is given in a section of the manual to allow the user to see what happens in each situation.

Register mapping generally follows the correspondence shown in figure 4, with a loose relationship between the 8086 AX and the 8080 PSW; the exact relationship is determined from register usage at translate time.

Many run-time options are available to control the translation pro-